IC MASTER 1979

- **FIVE MASTER SELECTION GUIDES**
  102 companies' IC's organized by type, function, key parameters
- **OVER 2400 PAGES OF TECHNICAL INFORMATION**
  Provided directly by manufacturers covering over 25,000 IC's and 46,000 Alternates
- **ALTERNATE SOURCE DIRECTORY**
  The only industry-wide, pin-for-pin version available
- **MILITARY PARTS INDEX AND CROSS REFERENCE CHART**
  Identifies all IC's with JAN qualification
- **MILITARY DEVICE TESTING TABLE**
  List companies that screen to Mil. Std. 883
- **MILITARY PARTS INDEX**
  The first function guide to JAN qualified parts
- **PART NUMBER INDEX**
  Parts from 84 manufacturers, in numerical sequence
- **APPLICATION NOTE DIRECTORY**
  Digest of currently active application note material
- **PART NUMBER GUIDE**
  Instantly decodes each company's part numbering system
- **MANUFACTURERS AND DISTRIBUTORS DIRECTORY**

IC MASTER 1979

THE FIRST STEP

IC MASTER is the **first** and **only** complete guide to Integrated Circuits. Now you can turn to the one source that has become the first step in the critical selection of Integrated Circuits. Whether an IC exists in new design or is one of thousands, you'll find it out in seconds by using the MASTER. . . .

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The IC MASTER saves you time and lots of it . . . no longer do you have to spend long tedious hours and days searching through manufacturer's catalogs and data sheets for information. The MASTER gives you — at your fingertips — an easy way to narrow your IC choices quickly, accurately and systematically with the knowledge that you have just surveyed the entire industry.

IC MASTER and its quarterly updates are published by United Technical Publications, the largest electronic publisher in the world.

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A quick guide to your IC MASTER

PART NUMBER INDEX This revolutionary index takes all device types made by 102 IC manufacturers and arranges them in numerical sequence excluding prefixes or suffixes. You can now find a device number even though you do not know either the full part number or even the manufacturer. Once a basic device number is located in the index, you can obtain instant identification of all manufacturers making a device by that number and determine the full part number designation. All page references to data sheet material and any existing application notes abstracts are also provided.

PART NUMBER GUIDE An instant decoding kit. Information in this guide, provided by the manufacturers, allows you to break each company's part numbering system down into product temperature ranges, packaging variations, and functions. An invaluable tool for the elimination of costly and time consuming ordering errors caused by lack of standardization in part numbering systems.

APPLICATION NOTE DIRECTORY To prepare this directory each IC manufacturer reviewed his own application note inventory and identified all those application notes considered to be currently active. Thus, in addition to providing a directory of active application note abstracts, the IC MASTER directory also provides the first industry wide purge of obsolete material. Application note descriptions are arranged by Digital, Linear, Memory, and Microprocessor categories. Beneath those headings, material is arranged alphabetically by function and applications category. Each application note is listed by title, identifies the specific device featured, provides a 25 to 50 word abstract, and includes identity of both the authoring manufacturer and the specific application note number. This section provides all the information necessary for the engineer to update his application note files speedily or thoroughly research the existance of application note material for a specific design problem.

MILITARY PARTS DIRECTORY Cross Reference Chart identifies all IC devices having received JAN qualification. This chart includes a cross reference feature converting device numbers to Mil. Std. 38510 slash number and vice versa.

MILITARY DEVICE TESTING TABLE Lists more than 50 major manufacturers and shows, in matrix form, those device types tested to Mil. Std. 38510 as well as screening performed to Mil. Std. 883. Those companies willing to perform special screening to customer's unique military requirements are also identified.

MILITARY PARTS INDEX A "first ever" functional guide to JAN qualified parts. Now it is possible to search by device and function to determine whether a JAN qualified part exists for your application, and if so, obtain both the device and 38510 slash numbers.

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ALTERNATE SOURCE DIRECTORY The first industry-wide, pin-for-pin functional equivalent Alternate Source Directory ever available. This directory was developed by asking each IC manufacturer to identify each competitive device for which he made a pin-for-pin interchangeable alternate. This unique approach took nearly three years to complete, is updated quarterly, involving countless manhours of catalog searching and specification comparison.

MASTER SELECTION GUIDE This Guide, covering virtually every facet of the industry, organizes ICs into these categories: Digital, Interface, Linear, Memory and Microprocessors. In each category, products are further classified by type (CMOS, ECL, TTL, etc.) and function (Arithmetic, Counters, Gates, etc.). You'll find every IC performing that function listed by part number and manufacturer. The Five Master Selection Guides will allow you to search for ICs by your specific requirements and identify all major available devices and sources.

MANUFACTURER & DISTRIBUTOR DIRECTORY Locate the nearest local source for additional information or quick delivery of needed products. A fingertip communications guide listing the location and phone number for all manufacturer's field sales offices, reps, and distributors, both domestic and international.

QUARTERLY UPDATES This service assures that all this vast body of information is constantly refreshed. Each issue updates your Master book on a CUMULATIVE basis. Your guarantee that the IC MASTER will remain the most complete and current industry-wide source available for the first step in IC selection.

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PART NUMBER INDEX
(pg. 15-111)

PART NUMBER GUIDE
(pg. 114-128)

MILITARY PARTS DIRECTORY
(pg. 134-141)

APPLICATION NOTE DIRECTORY
(pg. 150-305)

MASTER SELECTION GUIDE INDEX

Use this index to determine which of the five Master Selection Guides (Digital, Interface, Linear Memory, Microprocessor) to turn to by simply looking up alphabetically the function in which you are interested.

how to use the five master selection guides

These guides provide sufficient information to make initial product selections, to lead you to a group of device numbers and manufacturers' names. They enable you to find the products most apt to fulfill your major requirements and then provide data to help you make your final choice. All devices that appear in this section, both in the initial selection guide and in the data pages, are included in the Part Number Index. These index listings lead to the page and the line on that page where each device appears.

The coverage of industrial and consumer circuits is identified by model number and covers digital, linear and digital-linear combinations under one heading, **Linear** — Consumer Circuits. The TTL major families, TTL, TTL-LS, TTL-H and TTL-S have been combined under one heading to facilitate function comparisons. And the **Microprocessor** section has been enlarged, grouping microprocessor system components together by processor type and adding many new system descriptions.

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Function	Section
A	
AC Detector	Linear—Other Devices
ACE	*See Asynchronous Communications Element*
ACIA	Interface—Transmitters-Receivers
Active Filter	Linear—Other Devices
Active Terminator	Digital—ECL 10000, Miscellaneous
Adders	Digital—CMOS, Arithmetic Functions
	Digital—ECL 10000, Arithmetic Functions
	Digital—TTL, Arithmetic Functions
	Digital—Special
Address Latch Element	Microprocessors—Systems Components
Address Register	Microprocessors—Systems Components; 10800
Address Selector	Linear—Telecommunication Circuits
Alarm Circuits	Linear—Other Devices
ALU	*See Arithmetic Logic Unit*
Amplifier/Detector FM IF	Linear—Consumer Circuits
Amplifiers	
AC	Linear—Other Devices
	Linear—Special Purpose
AGC/Squelch	Linear—Amplifiers, Special Purpose
	Linear—Consumer Circuits
AM/FM IF	Linear—Consumer Circuits
AM/FM IF and AF	Linear—Consumer Circuits
Audio	Linear—Amplifiers, Special Purpose
Audio, Power	Linear—Consumer Circuits
CATV	Linear—Consumer Circuits
Current	Linear—Amplifiers, Special Purpose
Differential/ Cascode	Linear—Amplifiers, Special Purpose
Differential Input/ Output	Linear—Amplifiers, Special Purpose
Followers	Linear—Followers
Front End	Linear—Amplifiers, Special Purpose
Hearing Aid	Linear—Consumer Circuits
Instrumentation	Linear—Amplifiers, Special Purpose
	Linear—Operational Amplifier Characteristics
Isolation	Linear—Amplifiers, Special Purpose
Limiting	Linear—Amplifiers, Special Purpose
Linear/Antilog	Linear—Amplifiers, Special Purpose
Log/Antilog	Linear—Amplifiers, Special Purpose
Microphone	Linear—Amplifiers, Special Purpose
Mixer/RF	Linear—Consumer Circuits
Operational	Linear—Operational Amplifier Characteristics
	Linear—Operational Amplifiers, General Purpose
	Linear—Operational Amplifiers, High Output Current
	Linear—Operational Amplifiers, High Voltage
	Linear—Operational Amplifiers, Low Bias Current
	Linear—Operational Amplifiers, Low Drift
	Linear—Operational Amplifiers, Programmable
	Linear—Operational Amplifiers, Single Supply
	Linear—Operational Amplifiers, Wide Band
Preamplifier	Linear—Amplifiers, Special Purpose
	Linear—Consumer Circuits
RF	Linear—Amplifiers, Special Purpose
RF Detector/ Video	Linear—Consumer Circuits
Sense	Interface—Sense Amplifiers
Single Ended Input/Output	Linear—Amplifiers, Special Purpose
Tone	Linear—Consumer Circuits
Transconductance	Linear—Amplifiers, Special Purpose
Video, IF and RF	Linear—Amplifiers, Special Purpose
Voltage Controlled	Linear—Amplifiers, Special Purpose
Wideband	Linear—Amplifiers, Special Purpose
AM Radio Components	Linear—Consumer Circuits
AM/FM Radio Components	Linear—Consumer Circuits
Analog Input	Microprocessor—System Components; F8, SC/MP, Z80, 6500, 6800, 8008, 8048, 8080, 8085, General Purpose
Analog Memories	Linear—Other Devices
Analog Output	Microprocessor—System Components; General Purpose
Analog Shift Registers	Linear—Other Devices
Analog Switches	Interface—Analog Switches
AND Gates	*See Gates*
Appliance Control Devices	Linear—Consumer Circuits
Arithmetic Functions	Digital—CMOS, Arithmetic Functions
	Digital—CMOS, Miscellaneous
	Digital—ECL, Arithmetic Functions
	Digital—HNIL/HTL, Arithmetic Functions
	Digital—TTL, Arithmetic Functions
	Digital—TTL, Miscellaneous
	Digital—Special
Arithmetic Generator/ Processor	Digital—Special
	Microprocessor—System Components; 1000, 8080, General Purpose
Arithmetic Logic Element	Digital—TTL, Arithmetic Functions
Arithmetic Logic Register Stack	Digital—CMOS, Arithmetic Functions
	Microprocessor—System Components; Macrologic Bipolar, Macrologic CMOS
Arithmetic Logic Unit	Digital—CMOS, Arithmetic Functions
	Digital—ECL 10000, Arithmetic Functions
	Digital—ECL 100K, Arithmetic Functions
	Digital—TTL, Arithmetic Functions
	Microprocessor—System Components; IMP, 10800
Arrays	
Bipolar	Linear—Arrays
CMOS	Linear—Arrays, Special Arrays
Custom Digital	Digital—ECL 100K, Miscellaneous
	Digital—Special
	Linear—Other Devices
Thyristor/ Transistor	Linear—Arrays, Special Arrays
Transistor	Linear—Arrays, Transistor Arrays
Transistor/Diode	Linear—Arrays, Special Arrays
ASTRO	Interface—Transmitters-Receivers
Asynchronous Communication Controller	Microprocessors—System Components

Function	Section
Asynchronous Communications Element	Microprocessor—System Components; 8080
Asynchronous Communications Interface Adapter	*See ACIA*
Asynchronous/ Synchronous Transmitter/ Receiver	*See ASTRO*
Audio Circuits	Linear—Consumer Circuits
Audio Noise Reduction Dolby	Linear—Consumer Circuits
Automotive Circuits	Linear—Consumer Circuits

B

Balanced Modulator/ Demodulator	Linear—Other Devices
Bandpass Filters	Linear—Telecommunication Circuits
Bar Graph Display Driver	Interface—Display Drivers
Baseband Channel Amplifier	Linear—Telecommunication Circuits
Baseband Modem	Linear—Telecommunication Circuits
BASIC Interpreter	Microprocessor—System Components; SC/MP, 8080
Baud Rate Generator	Digital—Special Interface—Serial Transmitters, Receivers
BCD Rate Multiplier	Digital—CMOS, Miscellaneous
Bidirectional Bus Driver	Microprocessor—System Components; 3,000, 8,008, 8048, 8080, 8085
Bidirectional Port	Microprocessor—System Components; 2650
Bidirectional Transceiver	Interface—Line Circuits, Line Transceivers Microprocessor—System Components PACE
Binary Rate Multiplier	Digital—CMOS, Miscellaneous
Bit Programmable I/O	Microprocessor—System Components; SC/MP
Bit Rate Generator	Digital—CMOS, Miscellaneous Interface—Transmitters-Receivers Microprocessor—System Components; Macrologic CMOS, 6100
Blowout Resistant Transistor	Linear—Other Devices
Branch Control Unit	Microprocessor—System Components
Bubble Memories	Memory—Bubble Memories
Bubble Memory Controller	Interface—Display Drivers
Bucket Brigade Device	Linear—Other Circuits *Also See Analog Shift Registers*
Buffers	Digital—CMOS, Buffers/Inverters Digital—ECL 10000, Buffers Digital—HNIL/HTL, Buffers/Inverters Digital—TTL, Buffers/Inverters Digital—TTL, Drivers Microprocessor—System Components
Bus Interface Circuits	Interface—Line Circuits Microprocessor—System Components
BOART (Bus Oriented ART)	Interface—Transmitters-Receivers
Bus Receiver	Digital—ECL 10000, Miscellaneous Interface—Line Circuits
Bus Switch	Digital—TTL, Miscellaneous
Bus Transceiver	Digital—ECL 10000, Miscellaneous Digital—TTL, Miscellaneous Interface—Line Circuits Microprocessor—System Components; MicroNOVA, 2900, 6800
Bus Translator	Microprocessor—System Components

C

Calculator Circuits	Linear—Consumer Circuits
Calculator, Display Interface	Linear—Consumer Circuits
Calculator, Keyboard Entry Sequence Memory	Linear—Consumer Circuits
Calculator, Printing	Linear—Consumer Circuits
Camera Exposure Control	Linear—Consumer Circuits
Camera, Strobe Light Control	Linear—Consumer Circuits
Capacitive Input	Microprocessor—System Components; 1000
Cassette Controller	Microprocessor—System Components; 8080, 8085, General Purpose
CATV Amplifiers	Linear—Consumer Circuits
CB Circuits	Linear—Consumer Circuits Linear—Phase Locked Loop Circuits
CCD Memories	Memories—RAMs, CCD Memories
CCD Memory Driver	Interface—Memory and Peripheral Drivers
Central Processing Unit	Microprocessor—System Components; F8, MicroNOVA, M380, PACE, PPS-4 SBPO400, TLCS-12, Z80, 1600, 1800, 3000, 4000, 6100, 6500, 6800, 8008, 8080, 8085, 9440, 14500
Character Generators	Memory—Character Generators
Citizens Band Radio Circuits	*See CB Circuits*
Clock	Digital—CMOS, Oscillators/Dividers Linear—Consumer Circuits
Clock Buffer	Interface—Memory and Peripheral Drivers Microprocessor—System Components; 6800
Clock Driver	*See Drivers*
Clock Generator	Microprocessor—System Components; PPS-4, 2900, 4004, 8000, 8080
Clock Generator/ Driver	Digital—TTL, Miscellaneous
Codec	Linear—Telecommunication Circuits
Code Converters	Memory—Code Converters
Code Identification System (Manchester)	Digital—CMOS, Miscellaneous
Coin Box Circuits	Linear—Telecommunication Circuits
Compander	Linear—Telecommunication Circuits

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Function	Section
Comparators, Digital	Digital—CMOS, Arithmetic Functions
	Digital—ECL 10000, Arithmetic Functions
	Digital—ECL III, Arithmetic Functions
	Digital—HNIL/HTL, Arithmetic Functions
	Digital—TTL, Arithmeic Functions
Comparators, Linear	Linear—Comparators, Single Comparators
	Linear—Comparators, Dual Comparators
	Linear—Comparators, Quad Comparators
	Linear—Phase Locked Loop Circuits
Comparator, Voltage (Analog Input-Digital Output)	Digital—TTL, Miscellaneous
Complementary Output Elements	Digital—TTL, Miscellaneous
Complementer	*See Nines Complementer*
Compressor (Compander)	Linear—Telecommunication Circuits
Constant Current Source	Linear—Other Devices
Contact Bounce Eliminator	Digital—CMOS, Miscellaneous
	Digital—TTL, Miscellaneous
Control Element	Microprocessor—System Components; 4004
Control ROM	Microprocessor—System Components; IMP, 5781
Control Store Sequencer	Microprocessor—System Components; 2900, General Purpose
Converters	
Analog to Digital	Interface—Analog to Digital Converters, Binary Output
	Interface—Analog to Digital Converters, Decimal Output
	Linear—Other Devices
BCD to Binary	Digital—TTL, Miscellaneous
BCD to Binary/ Binary to BCD	Digital—TTL, Miscellaneous
Binary to Phone Pulse	Digital—CMOS, Miscellaneous
Digital to Analog	Interface—Digital to Analog Converters
Frequency to Voltage	Linear—Other Devices
Logic Level	Digital—CMOS, Buffers/Inverters
Serial to Parallel	Digital—Special
Voltage to Frequency	Linear—Other Devices
Correlation	Digital—Special
	Linear—Other Devices
Counter	Digital—CMOS, Counters, Miscellaneous
	Digital—ECL III, Counters
	Digital—HNIL/HTL, Counters
	Digital—TTL, Counters, Miscellaneous
	Digital—Special
Binary	Digital—CMOS, Counters, Binary
	Digital—ECL 10000, Counters, Binary
	Digital—ECL 95000, Counters
	Digital—ECL III, Counters
	Digital—HNIL/HTL, Counters
	Digital—TTL, Binary Counters Up
	Digital—TTL, Binary Counters Up/Down
	Digital—Special
Decade	Digital—CMOS, Counters, Decade
	Digital—ECL 10000, Counters, Decade
	Digital—ECL 95000, Counters
	Digital—ECL III, Counters
	Digital—HNIL/HTL, Counters
	Digital—TTL, Decade Counters Up
	Digital—TTL, Decade Counters Up/Down
	Digital—TTL, Miscellaneous
	Digital—Special
Counter Logic Control	Linear—Phase Locked Loop Circuits
Counter Time Base	Digital—Special
	Microprocessor—System Components; Z80
Count Extender	Linear—Phase Locked Loop Circuits
Counting Register	Digital—ECL 100K, Counters
CPU	*See Central Processing Unit*
CRC Generator/ Checker	Interface—Error Checking Circuits
	Microprocessor—System Components; Macrologic Bipolar
CROM	*See Control ROM*
Crosspoint Array	Linear—Telecommunications Circuits
Crosspoint Switches	Interface—Analog Switches, Multiplexers
CRT Controller	Microprocessor—System Components; 6500, 6800, 8048, 8080, 8085, General Purpose
CRT Video Timer Controller	Microprocessor—System Components; General Purpose
Crystal Oscillator	*See Oscillators*
Current Sensing Interface Gate	Digital—TTL, Miscellaneous
Custom Arrays	Digital—CMOS, Miscellaneous
	Digital—Special

D

Darlington Switch	Interface—Memory and Peripheral Drivers
	Linear—Arrays
Data Access Register	Digital—CMOS, Arithmetic Functions
	Microprocessor—System Components; Macrologic Bipolar, Macrologic CMOS
Data Acquisition System	Linear—Other Devices
Data Encryption System	Digital—TTL, Miscellaneous
	Microprocessor—System Components; Macrologic Bipolar, 8080
Data Link Controller	Microprocessor—System Components; 6800
Data Path Switch	Digital—CMOS, Arithmetic Functions
	Linear—Analog Switches
	Microprocessor—System Components; Macrologic Bipolar, Macrologic CMOS
Data Selector/ Multiplexer	*See Multiplexers*
Decade Sequencer	Digital—TTL, Miscellaneous
Decoder	Digital—CMOS, Decoders
	Digital—CMOS, Drivers
	Digital—ECL 10000, Decoders
	Digital—ECL 100K, Decoders
	Digital—TTL, Decoders
	Digital—CMOS, Drivers
	Digital—Special
	Interface—Display Drivers
	Microprocessor—System Components
FM Stereo	Linear—Consumer Circuits
Keyboard	Interface—Keyboard Encoders, Decoders
Tone	Linear—Phase Locked Loop Circuits

Function	Section
Deglitcher	Linear—Telecommunication Circuits
Delta Modulation System	Linear—Other Devices Linear—Telecommunication Circuits
Demultiplexer	*See Decoders*
Deskew FIFO	Memory—FIFO Microprocessors—General Purpose
Deskew—Queue Register	Interface—Error Checking Circuits
Detectors	Linear—Consumer Circuits Linear—Other Devices
Development System	Microprocessor—System Components; F8, IMP, PACE, SC/MP, Z80, 3000, 6800, 8048, 8080, 8085, 9900
Dialer Circuits	Linear—Telecommunication Circuits
Digital Filter Switch	Linear—Telecommunication Circuits
Digital Mixer	*See Mixer*
Digital Modulator	Microprocessor—System Components; 6800
Digital to Analog Converters	Interface—Digital to Analog Converters
Diode Matrix, Programmable	Digital—Special
Direct Memory Access Controller	*See DMA Controller*
Disk Memory Drivers	Interface—Memory and Peripheral Drivers
Fault Detector	Interface—Memory and Peripheral Drivers
Head Selector	Interface—Memory and Peripheral Drivers
Video Amplifier	Interface—Memory and Peripheral Drivers
Display Controller	Microprocessor—System Components; Macrologic Bipolar, PPS-4, 8080, General Purpose
Display Drivers	Interface—Display Drivers *Also See Drivers*
Dividers	Digital—CMOS, Oscillators/Dividers Digital—TTL, Miscellaneous Digital—Special Linear—Phase Locked Loop Circuits Linear—Other Devices
DMA Address Generator	Microprocessor—System Components
DMA Controller	Microprocessor—System Components; F8, PPS-4, Z80, 1600, 6800, 8080, 8085, 9900, General Purpose
Double Balanced Mixer	Linear—Phase Locked Loop Circuits
DPDT Switches	Interface—Analog Switches
DPST Switches	Interface—Analog Switches
Drivers	Digital—CMOS, Drivers Digital—CMOS, Miscellaneous Digital—ECL 10000, Drivers Digital—ECL 100K, Drivers Digital—HNIL/HTL, Drivers Digital—TTL, Decoders Digital—TTL, Drivers Digital—TTL, Miscellaneous Interface—Analog Switches, Drivers Interface—Display Drivers Interface—Line Circuits Interface—Memory and Peripheral Drivers
Audio	Linear—Consumer Circuits
Counter Display	Digital—Special
DVMs	Digital—Special Interface—Analog to Digital Converters, Decimal Output
Dynamic Memory Interface	Interface—Memory and Peripheral Drivers Microprocessor—System Components; F8
Dynamic Memory Refresh Controller	Digital—TTL, Miscellaneous Interface—Memory and Peripheral Drivers Microprocessor—System Components; 6800

E

Encoders	Digital—CMOS, Miscellaneous Digital—ECL 10000, Miscellaneous Digital—ECL 100K, Miscellaneous Digital—TTL, Miscellaneous Digital—Special
Keyboard	Interface—Keyboard Encoder-Decoders
Keyboard to Binary	Digital—CMOS, Miscellaneous
Tone	Digital—CMOS, Miscellaneous Linear—Telecommunications Circuits
Error Checking Circuits	Digital—ECL10000, Miscellaneous Interface—Error Checking Circuits
Error Pattern Register	Interface—Error Checking Circuits
Expander	Digital—TTL-Gates, AND-OR/AND-OR Invert Digital—TTL, Miscellaneous
Expander (Compander)	Linear—Telecommunication Circuits
Extender	Digital—TTL-Gates, AND-OR/AND-OR Invert

F

Fast Carry Extender	Digital—TTL, Arithmetic Functions
Field Programmable Array Logic	Digital—TTL, Miscellaneous Memory—PLAs
Field Programmable Logic Array	Memory—PLAs Microprocessor—System Components
First In First Out Memory	Memory—FIFO Microprocessor—System Components
Flasher (LED)	Linear—Other Devices
Flip-Flops	Digital—CMOS, Flip-Flops Digital—ECL 10000, Flip-Flops Digital—ECL 95000, Flip-Flops Digital—ECL 100K, Flip-Flops Digital—ECL III, Flip-Flops Digital—HNIL/HTL, Flip-Flops Digital—TTL, Flip-Flops Digital—Special
Floating Point Arithmetic	Microprocessor—System Components; 8080
Floppy Disc Amplifier System	Linear—Amplifiers - Special Purpose
Floppy Disc Controller	Microprocessor—System Components; PPS-4, 1600, 6800, 8048, 8080, 8055, General Purpose
Fluid Detector	Linear—Other Devices
Fluorescent Display Drivers	Interface—Display Drivers

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Function	Section
FM Muting/Tuning Point System	Linear—Consumer Circuits
FM Radio Circuits	Linear—Consumer Circuits
FM RF/IF Amplifier	Linear—Consumer Circuits
Followers	Linear—Followers
Four Channel Sound	Linear—Consumer Circuits
Frequency Divider	Digital—Special Linear—Consumer Circuits
Frequency Sensitive Switch	Linear—Telecommunication Circuits Linear—Other Devices
Frequency to Voltage Converter	Linear—Other Devices
FSK Modulator/ Demodulator	Linear—Phase Locked Loop Circuits
Function Generator	Linear—Phase Locked Loop Circuits Linear—Other Devices

G

Games, T.V.	Linear—Consumer Circuits
Gas Discharge Display Drivers	Interface—Display Drivers
Gates	Digital—CMOS, Gates, Miscellaneous
	Digital—HNIL/HTL, Gates, Miscellaneous
	Digital—TTL, Gates, Miscellaneous
AND/NAND	Digital—CMOS, Gates, AND/NAND
	Digital—ECL 10000, Gates, AND/NAND
	Digital—HNIL/HTL, Gates, AND/NAND
	Digital—TTL, Gates, AND/NAND
AND-OR/AND-OR Invert	Digital—CMOS, Gates, AND-OR/ AND-OR Invert
	Digital—ECL 10000, Gates, AND-OR/ AND-OR Invert
	Digital—ECL 100K, Gates, AND-OR/ AND-OR Invert
	Digital—HNIL/HTL, Gates, AND-OR/ AND-OR Invert
	Digital—TTL, Gates, AND-OR/ AND-OR Invert
Complex Gate w/ Persistance Detector	Digital—Special
Exclusive OR/NOR	Digital—CMOS, Gates, Exclusive OR/NOR
	Digital—ECL 10000, Gates, Exclusive OR/NOR
	Digital—ECL 100K, Gates, Exclusive OR/NOR
	Digital—ECL III, Gates, Exclusive OR/NOR
	Digital—HNIL/HTL, Gates, Exclusive OR/NOR
	Digital—TTL, Gates, Exclusive OR/NOR
Majority Logic	Digital—CMOS, Gates, Miscellaneous
	Digital—TTL, Gates, Miscellaneous
OR/NOR	Digital—CMOS, Gates, OR/NOR
	Digital—ECL 10000, Gates, OR/NOR
	Digital—ECL 95000, Gates, OR/NOR
	Digital—ECL 100K, Gates, OR/NOR
	Digital—ECL III, Gates, OR/NOR
	Digital—TTL, Gates, OR/NOR
	Digital—Special
Gate Expander	Digital—HNIL/HTL, Gates, Miscellaneous

Function	Section
General Purpose Interface Circuit	Microprocessor—System Components; 6800, General Purpose
General Purpose Input/Output	Microprocessor—System Components; PPS-4, TLCS-12, 1600, 4004
General Purpose Keyboard and Display	Microprocessor—System Components; PPS-4
GPIB Talker Listener Interface	Microprocessor—System Components; 8080, 8085
Ground Fault Interrupter	Linear—Consumer Circuits
Gyrator	Linear—Telecommunications Circuits

H

Hall Effect Devices	Digital—Special Linear—Other Devices
Hammer Driver	Interface—Memory and Peripheral Drivers
Hamming Code Detector and Generator	Digital—TTL, Miscellaneous Interface—Error Checking Circuits

I

Identity Comparator	Digital—TTL, Arithmetic Functions
Image Sensor	Linear—Other Devices
Impedance Converter	Linear—Other Devices
Input/Output Control Unit	Microprocessor—System Components
Interface Latch Element	Microprocessor—System Components; PACE
Interrupt Control Unit	Microprocessor—System Components; 3000
Interrupter, Ground Fault	Linear—Consumer Circuits
Interval Timer	Linear—Timers Microprocessor—System Components; PPS-4, 8008, 8048, 8080, 8085
Inverters	Digital—CMOS, Buffers/Inverters Digital—HNIL/HTL, Buffers/Inverters Digital—HNIL/HTL, Gates, Miscellaneous Digital—TTL, Buffers/Inverters Digital—Special
I/O Buffer	Microprocessor—System Components; 1600, 8000
I/O Expander	Microprocessor—System Components 1000, 8048, 8080, 8085
I/O Port	Digital—TTL,Miscellaneous Microprocessor—System Components; SC/MP, 1800, 6100, 8X300, 8008, 8048, 8080,8005
I/O Transceiver	Microprocessor—System Components; MicroNOVA
I/O Transceiver Buffer	Microprocessor—System Components; MicroNOVA

Function	Section
K	
Keyboard/Display Controller	Microprocessor—System Components; 8008, 8048, 8080, 8085
Keyboard Encoders	Interface—Keyboard Encoders, Decoders
L	
Lamp Driver	Interface—Display Drivers
Last In First Out Memory	Memory—LIFOs
Latches	Digital—CMOS, Latches
	Digital—CMOS, Drivers
	Digital—ECL 10000, Latches
	Digital—ECL 95000, Latches
	Digital—ECL 100K, Latches
	Digital—ECL III, Latches
	Digital—HNIL/HTL, Latches
	Digital—TTL, Latches
	Microprocessor—System Components
LCD Display Drivers	Interface—Display Drivers
LED Display Drivers	Interface—Display Drivers
Level Detector	Linear—Other Devices
Level Meter	Linear—Other Devices
Level Shifter	Digital—CMOS, Translators
	Digital—ECL-10000, Translators
	Digital—HNIL/HTL, Translators
	Digital—TTL, Translators
	Interface—Memory and Peripheral Drivers
Light Activated Switch	Linear—Other Devices
Light Dimmer	Linear—Consumer Circuits
Light Detector	Linear—Other Devices
Light to Current Converter	Linear—Other Devices
Light to Frequency Converter	Linear—Other Devices
Line Drivers	Interface—Line Circuits, Single Ended
	Interface—Line Circuits, Differential
Line Receivers	Digital—ECL 10000, Miscellaneous
	Digital—ECL 100K, Miscellaneous
	Digital—ECL III, Miscellaneous
	Interface—Line Circuits, Single Ended
	Interface—Line Circuits, Differential
Line Transceiver	Interface—Line Circuits, Transceivers
Logic Processor	Microprocessor—System Components; 8000
Look Ahead Carry Generator	Digital—CMOS, Arithmetic Functions
	Digital—ECL 10000, Arithmetic Functions
	Digital—TTL, Arithmetic Functions
	Microprocessor—System Components; 2900, 3000
Loop Disconnect Dialer	Linear—Telecommunication Circuits
Low Battery Indicator	Linear—Other Devices
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Macroprogram Sequencer	Microprocessor—System Components; 2900
Magnitude Comparator	Digital—CMOS, Arithmetic Functions
	Digital—TTL, Arithmetic Functions

Function	Section
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Mask Merge	Digital—ECL100K, Shift Registers
MEDIC	Microprocessor—System Components
Memories	
Active Element	Digital—TTL, Memories
CAM	Digital—CMOS, Memories
	Digital—TTL, Memories
Character Generators	Memory—Character Generators
Code Converters	Memory—Code Converters
FIFO	Digital—CMOS, Memories
	Digital—TTL, Memories
	Memory—FIFO
LIFO	Digital—CMOS, Memories
	Memory—LIFO
PLA	Memory—PLAs
PROM	Digital—ECL 10000, Memories
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	Microprocessor—System Components
RAM	Digital—CMOS, Memories
	Digital—ECL 10000, Memories
	Digital—ECL 95000, Memories
	Digital—ECL 100K, Memories
	Digital—TTL, Memories
	Memory—RAMs, Bubble Memories
	Memory—RAMs, Dynamic
	Memory—RAMs, CCD Memories
	Memory—RAMs, Static
	Microprocessor—System Components
ROM	Digital—CMOS, Memories
	Memory—EAROMs
	Memory—ROMs, Static
	Memory—ROMs, Dynamic
	Microprocessor—System Components
Memory Address Driver	Microprocessor—System Components; MicroNOVA
Memory Control Unit	Microprocessor—System Components; TLCS-12, 9440,
Memory Controller, MNOS	Interface—Memory and Peripheral Drivers
Memory Drivers	*See Drivers*
Memory Interface	Interface—Memory and Peripheral Drivers
	Microprocessor—System Components; 8000, 10800
Memory Refresh Logic Circuits	Digital—TTL, Miscellaneous
	Interface—Memory and Peripheral Drivers
Micro Address Generator	Digital—TTL, Miscellaneous
MICROM	Microprocessor—System Components
Microcomputer	Microprocessor—System Components; μCOM-4, SX200, 1000, 1400, 1600, 2000, 8048, 8085, 9900
Microcontroller	Digital—TTL, Arithmetic Functions
	Microprocessor—System Components; WD40, 67000
Microprocessor	Digital—TTL, Arithmetic Functions
	Microprocessor—Selection Tables
	Microprocessor—System Components; SC/MP, 2650, 2900, 4004, 5781, 5799, 8X300, 9900
Microprocessor Development System	*See Development System*

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Microprogram Sequencer	Digital—TTL, Miscellaneous
	Microprocessor—System Components; Macrologic Bipolar, Macrologic CMOS, 2900
Mixer	Linear—Amplifiers, Special
	Linear—Phase Locked Loop Circuits
Modem	Digital—CMOS, Miscellaneous
	Interface—Transmitters-Receivers
	Linear—Telecommunication Circuits
	Linear—Other Devices
	Microprocessor—System Components; 6800, 9900
Modulator	Linear—Other Devices
	Linear—Consumer Circuits
Motor Control Devices	Linear—Consumer Circuits
	Linear—Other Devices
Motor Load Control	Linear—Other Devices
Motor Speed Regulator	Linear—Consumer Circuits
	Linear—Other Devices
Multifunction Converter	Linear—Other Devices
MPCC	*See Multi-Protocol Communications Controller*
Multiplexers	
Analog	Interface—Analog Switches, Multiplexers
Digital	Digital—CMOS, Multiplexers
	Digital—ECL 10000, Multiplexers
	Digital—ECL 100K, Multiplexers
	Digital—HNIL/HTL, Multiplexers
	Digital—TTL, Multiplexers
	Digital—Special
Multiplier	Digital—CMOS, Arithmetic Functions
	Digital—ECL 10000, Arithmetic Functions
	Digital—TTL, Arithmetic Functions
	Microprocessor—System Components;
Binary	Digital—CMOS, Arithmetic Functions
Binary Rate	Digital—CMOS, Miscellaneous
	Digital—TTL, Miscellaneous
Decade Rate	Digital—TTL, Miscellaneous
Multipliers/ Dividers, Analog	Linear—Other Devices
	Microprocessor—System Components
Multi-Protocol Communications Controller	Interface—Transmitters-Receivers
	Microprocessor—System Components; 2650, 8080
Multivibrators	Digital—CMOS, Multivibrators
	Digital—ECL III, Multivibrators
	Digital—HNIL/HTL, Multivibrators
	Digital—TTL, Multivibrators
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Monostable/ Astable	Digital—CMOS, Multivibrators
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	Digital—ECL 100K, Multivibrators
	Digital—HNIL/HTL, Multivibrators
	Digital—TTL, Multivibrators
Music Circuits	Linear—Consumer, Organ Circuits

N

Function	Section
NAND Gates	*See Gates*
Next Address Control Unit	Microprocessor—System Components; 2900
Nines Complementer	Digital—CMOS, Arithmetic Functions
Noise Generator	Linear—Other Devices
NOR Gates	*See Gates*

O

Function	Section
Offset Control System	Linear—Phase Locked Loop Circuits
Organ Circuits	Linear—Consumer Circuits
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Oscillators	Digital—CMOS, Oscillators/Dividers
	Linear—Phase Locked Loop Circuits
	Linear—Other Devices
Overvoltage Protector	Linear—Other Devices

P

Function	Section
Parallel Data Controller	Microprocessor—System Components; PPS-4, Z80
Parallel Interface Element	Microprocessor—System Components; 6100
Parity Generator	Digital—CMOS, Miscellaneous
	Digital—ECL 10000, Miscellaneous
	Digital—ECL 100K, Miscellaneous
	Digital—TTL, Miscellaneous
	Interface—Error Checking Circuits
Parity Tree	Digital—CMOS, Miscellaneous
	Digital—TTL, Miscellaneous
PCM Repeater	Linear—Telecommunication Circuits
Peak Detector	Linear—Other Devices
Peripheral Drivers	Interface—Memory and Peripheral Drivers
Peripheral Interface Input/Output	Microprocessor—System Components; F8, SC/MP, 8008, 8048, 8080, 8085, General Purpose
Peripheral Interface Adapter	Microprocessor—System Components; 6500, 6800
Phase Comparator	Digital—CMOS, Miscellaneous
	Interface—Phase Locked Loop Circuits
Phase Frequency Detector	Digital—TTL, Miscellaneous
	Linear—Phase Locked Loop Circuits
Phase Locked Loop Circuits	Digital—CMOS, Miscellaneous
	Digital—TTL, Miscellaneous
	Linear—Phase Locked Loop Circuits
Stereo Decoders	Linear—Consumer Circuits
Phase Sensitive Demodulator	Linear—Other Devices
Phase Shifter	Linear—Other Devices
PIA	*See Peripheral Interface Adapter*
PIN Diode Drivers	Digital—Other Digital Devices
	Linear—Other Devices

Function	Section
Plasma Display Controller	Interface—Display Drivers Microprocessor—System Components; General Purpose
Plasma Display Axis Driver	Interface—Display Drivers
Polynomial Generator	Digital—TTL, Miscellaneous Interface—Error Checking Circuits
Position Scaler	Digital—TTL, Miscellaneous
Power Strobe	Digital—TTL, Miscellaneous
Power Supply Control	Linear—Voltage Regulators, Switching Regulators
Power Transistor Driver/Amplifier	Linear—Amplifiers, Special Purpose
Preamplifier Audio	Linear—Amplifiers, Special Linear—Consumer Circuits
Prescalers	Digital—Special Linear—Phase Locked Loop Circuits
Pressure Transducer	Linear—Other Devices
Printer Controller	Interface—Memory and Peripheral Drivers Microprocessor—System Components; 8080, General Purpose
Printer Driver	Interface—Memory and Peripheral Drivers
Printer Interface	Microprocessor—System Components; PPS-4, 5799
Printing Calculator Circuits	Interface—Memory and Peripheral Drivers
Priority Encoder	Digital—CMOS, Miscellaneous Digital—TTL, Miscellaneous
Priority Interrupt	Microprocessor—System Components; 2900, 6800, 8008, 8048, 8080, 8085, General Purpose
Processing and Control Element	Microprocessor—System Components; PACE
Programmable Array Logic	Digital—TTL, Miscellaneous Memory—PLAs
Programmable Communications Element	Microprocessor—System Components; 2650, 8008
Programmable General Purpose I/O	Microprocessor—System Components; 8080
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Program Storage Unit	Microprocessor—System Components; F8
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Protocol Controller	Microprocessor—System Components; 8080
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PSART	Interface—Transmitters-Receivers
PSAT	Interface—Transmitters-Receivers
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Pulse Group Encoder	Digital—Special
Pulse Stretcher	Digital—HNIL/HTL, Miscellaneous
Pulse Synchronizer/ Driver	Digital—TTL, Miscellaneous
Pulse Width Modulator	Linear—Voltage Regulators, Switching Regulators
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R

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Radio Transmitter	Linear—Other Devices
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Regulator, Motor Speed	Linear—Consumer Circuits
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Function	Section
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Ring Modulator	Linear—Other Devices
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ROM Patch	Memory—PLAs
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S

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T

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PART NUMBER INDEX

This index shows the page and line on that page where each device appears in the Master Selection Guide. The list is prepared by a computer from the data in these sections so every device in them is listed. The devices are arranged in order by basic numbers so similarly numbered devices from various manufacturers are grouped together. Bold faced listings lead to the data supplied by the manufacturers. Use this index to locate key operational characteristics, application notes, and devices data whenever you have a model number.

how to use the part number index

This Part Number Index is arranged in alpha-numeric sequence, ignoring the manufacturer's prefixes and suffixes and using the basic model numbers. This basic number sequence is sorted by reading the digits from **left** to **right,** assuming that letters come before numbers. (As an example, these numbers would appear in the following order: 5301, 531, 54H01, 54139, 5414.) Under each basic number, the manufacturer's name and full model number is listed. The page references in **BOLD FACE** lead to manufacturers' data and application notes. Short editorial descriptions of all Active Applications Notes available from every manufacturer are indicated by a ¶ sign.

The arrangement of this index by base number gives you several advantages. It allows you to find a device by its basic number whether or not you know the name of the manufacturer or the manufacturer's prefixes. Also it groups similar devices together so that when you are looking for data you can quickly determine if the data has been provided in the book by any of the manufacturers and where that data is. Similarly it groups any references to application notes close together so that you do not need to guess which manufacturer might publish application notes on a device before you can locate them.

Once you become familiar with the alpha-numeric numbering sequence, you'll find that this index is very easy to use.

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53LS1641	**MMI**	**53LS1641**	⋆**1458**
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53LS1681	**MMI**	**53LS1681**	⋆**1458**
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53LS281	**MMI**	**53LS281**	⋆**1458**
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53LS440	**MMI**	**53LS440**	⋆**1458**
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53LS441	**MMI**	**53LS441**	⋆**1458**
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53LS480	**MMI**	**53LS480**	⋆**1458**
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53LS481	**MMI**	**53LS481**	⋆**1458**
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53PS280	MMI	53PS280	1162-35
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53PS440	MMI	53PS440	1165-20
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53S281	**MMI**	**53S281**	⋆**1453**
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	Motorola	SN54LS160A	432-18
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54LS161	AMD	SN54LS161	430-92
	Fairchild	54LS161	430-96
	Motorola	SN54LS161A	430-99
	National	DM54LS161	430-102
	Raytheon	54LS161	430-108
	Signetics	54LS161A	430-110
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54LS162	AMD	SN54LS162	432-55
	Fairchild	54LS162	432-59
	Motorola	SN54LS162A	432-62
	National	DM54LS162	432-64
	Raytheon	54LS162	432-72
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54LS163	AMD	SN54LS163	430-33
	Fairchild	54LS163	430-37
	Motorola	SN54LS163A	430-40
	National	DM54LS163	430-42
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	Signetics	54LS163A	430-50
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	Fairchild	54LS164	454-153
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54LS166	Motorola	SN54LS166	454-125
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54LS169	AMD	SN54LS169A	431-35
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54LS170	Fairchild	54LS170	448-188
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54LS170	Motorola	SN54LS170	1171-52
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	National	DM54LS173	439-33
	Signetics	54LS173	439-35
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54LS175	AMD	SN54LS175	439-60
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	Motorola	SN54LS175	439-67
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	Fairchild	54LS181	426-100
	Motorola	SN54LS181	426-102
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	Signetics	54LS181	426-110
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54LS183	TI	SN54LS183	425-109
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	National	DM54LS189	1172-113
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	Fairchild	54LS190	432-154
	Motorola	SN54LS190	432-156
	National	DM54LS190	432-158
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54LS191	AMD	SN54LS191	430-161
	Fairchild	54LS191	430-165
	Motorola	SN54LS191	430-167
	National	DM54LS191	430-169
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	Signetics	54LS191	430-177
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54LS192	AMD	SN54LS192	432-198
	Fairchild	54LS192	433-4
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54LS193	AMD	SN54LS193	431-10
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	Motorola	SN54LS193	431-16
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	Raytheon	54LS196	431-172
	TI	SN54LS196	431-175
54LS197	Fairchild	54LS197	429-191
	Motorola	SN54LS197	429-193
	National	DM54LS197	429-195
	Raytheon	54LS197	429-199
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54LS20	Fairchild	54LS20	442-60
	Motorola	SN54LS20	442-63
	National	DM54LS20	442-65
	Raytheon	54LS20	442-71
	Signetics	54LS20	442-73
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54LS21	Fairchild	54LS21	440-155
	Motorola	SN54LS21	440-158
	National	DM54LS21	440-160
	Raytheon	54LS21	440-165
	Signetics	54LS21	440-167
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54LS215	TI	SN54LS215	1177-45
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54LS22	Fairchild	54LS22	442-168
	Motorola	SN54LS22	442-171
	National	DM54LS22	442-173
	Raytheon	54LS22	442-177
	Signetics	54LS22	442-179
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54LS221	Motorola	SN54LS221	452-114
	National	DM54LS221	452-116
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54LS222	TI	SN54LS222	1159-60
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54LS241	AMD	SN54LS241	459-35
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54LS245	AMD	SN54LS245	459-113
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	Motorola	SN54LS245	459-123
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54LS247	Fairchild	54LS247	601-134
	Motorola	SN54LS247	601-149
	National	DM54LS247	601-155
	TI	SN54LS247	601-168
54LS248	Fairchild	54LS248	601-49
	Motorola	SN54LS248	601-60
	National	DM54LS248	601-70
	TI	SN54LS248	601-84
54LS249	Fairchild	54LS249	601-92
	Motorola	SN54LS249	601-98
	National	DM54LS249	601-104
	TI	SN54LS249	601-114
54LS251	AMD	SN54LS251	451-182
	Fairchild	54LS251	451-186
	Motorola	SN54LS251	451-189
	Raytheon	54LS251	451-196
	Signetics	54LS251	451-198
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	TI	SN54LS251	451-199
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54LS253	AMD	SN54LS253	450-193
	Fairchild	54LS253	450-197
	Motorola	SN54LS253	450-200
	National	DM54LS253	450-202
	Raytheon	54LS253	451-8
	Signetics	54LS253	451-10
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54LS255	Raytheon	54LS255	434-168
54LS256	Fairchild	54LS256	447-153
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54LS257	AMD	SN54LS257	450-47
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	Motorola	SN54LS257A	450-54
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54LS258	AMD	SN54LS258	450-13
	Fairchild	54LS258	450-17
	Motorola	SN54LS258A	450-20
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54LS259	Fairchild	54LS259	447-146
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54LS26	Fairchild	54LS26	444-126
	Motorola	SN54LS26	444-129
	National	DM54LS26	444-131
	Raytheon	54LS26	444-135
	Signetics	54LS26	444-137
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	Motorola	SN54LS266	446-102
	National	DM54LS266	446-104
	Raytheon	54LS266	446-108
	Signetics	54LS266	446-110
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54LS27	Fairchild	54LS27	447-24
	Motorola	SN54LS27	447-27
	National	DM54LS27	447-29
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54LS273	AMD	SN54LS273	440-45
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	Motorola	SN54LS273	440-53
	Raytheon	**54LS273**	★ **531**
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54LS275	TI	SN54LS275	426-53
54LS279	Fairchild	54LS279	448-120
	Motorola	SN54LS279	448-122
	National	DM54LS279	448-124
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	Signetics	54LS279	448-131
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54LS28	Motorola	SN54LS28	447-73
	Raytheon	54LS28	447-84
	Signetics	54LS28	447-88
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54LS280	Fairchild	54LS280	457-21
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54LS281	AMD	SN54LS281	426-187
54LS283	Fairchild	54LS283	425-51
	MMI	54LS283	425-55
	Motorola	SN54LS283	425-59
	National	DM54LS283	425-63
	Raytheon	54LS283	425-72
	Signetics	54LS283	425-76
	TI	SN54LS283	425-80
54LS289	Motorola	SN54LS289	1172-69
	National	DM54LS289	1172-114
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54LS290	Fairchild	54LS290	431-102
	Motorola	SN54LS290	431-106
	National	DM54LS290	431-110
	Signetics	54LS290	431-118
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54LS293	Fairchild	54LS293	429-115
	Motorola	SN54LS293	429-119
	National	DM54LS293	429-123
	Signetics	54LS293	429-131
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54LS295	Fairchild	54LS295	453-140
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	Motorola	SN54LS295A	453-142
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	Raytheon	54LS295A	453-147
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54LS297	TI	SN54LS297	457-51
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54LS298	AMD	SN54LS298	449-136
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54LS299	AMD	SN54LS299	454-57
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	Fairchild	54LS299	454-61
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	National	DM54LS30	441-183
	Raytheon	54LS30	441-188
	Signetics	54LS30	441-190
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54LS314	TI	SN54LS314	1177-54
54LS315	TI	SN54LS315	1177-43
54LS319	TI	SN54LS319	1172-80
54LS32	Fairchild	54LS32	446-138
	Motorola	SN54LS32	446-141
	National	DM54LS32	446-143
	Raytheon	54LS32	446-148
	Signetics	54LS32	446-150
	TI	SN54LS32	446-152
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54LS321	TI	SN54LS321	458-22
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	MMI	54LS322	425-184
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	Raytheon	**54LS322**	★ **537**
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	TI	SN54LS322A	425-190
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54LS323	AMD	SN54LS323	454-59
			1190-95
	Fairchild	54LS323	454-63
			1190-99
	MMI	54LS323	454-68
			1190-103
	Motorola	SN54LS323	454-72
	Raytheon	**54LS323**	★ **540**
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			1190-113
	TI	SN54LS323	454-88
			1190-117
54LS324	TI	SN54LS324	458-17
			899-56
54LS325	TI	SN54LS325	458-28
			899-115
54LS326	TI	SN54LS326	458-30
			899-117
54LS327	TI	SN54LS327	458-32
			899-119
54LS328	TI	SN54LS328	458-36
			899-121
54LS33	Fairchild	54LS33	447-108
	Motorola	SN54LS33	447-110
	Raytheon	54LS33	447-114
	Signetics	54LS33	447-116
	TI	SN54LS33	447-118
54LS347	TI	SN54LS347	601-124
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54LS348	TI	SN54LS348	456-172
54LS352	Fairchild	54LS352	451-22
	Motorola	SN54LS352	451-24
	National	DM54LS352	451-26
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54LS353	Fairchild	54LS353	451-31
	Motorola	SN54LS353	451-33
	National	DM54LS353	451-35
	TI	SN54LS353	451-37
54LS360	TI	SN54LS360	456-34
54LS361	TI	SN54LS361	456-37
54LS362	TI	SN54LS362	1762-115
54LS363	TI	SN54LS363	447-182
54LS364	TI	SN54LS364	440-88
54LS365	Fairchild	54LS365	428-30
	Motorola	SN54LS365A	428-35
	National	DM54LS365	428-39
	Raytheon	54LS365	428-47
	Signetics	54LS365A	428-53
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54LS366	Fairchild	54LS366	429-28
	Motorola	SN54LS366A	429-33
	National	DM54LS366	429-37
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54LS368	Fairchild	54LS368	429-30
	Motorola	SN54LS368A	429-35
	National	DM54LS368	429-39
	Raytheon	54LS368	429-49
	Signetics	54LS368A	429-53
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	Motorola	SN54LS37	443-180
	National	DM54LS37	443-182
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	Signetics	54LS37	443-189
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	Motorola	SN54LS373	447-170
	Raytheon	**54LS373**	★ **543**
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	TI	SN54LS373	447-184
54LS374	AMD	SN54LS374	440-67
	Fairchild	54LS374	440-70
	MMI	**54LS374**	★ **505**
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	Motorola	SN54LS374	440-74
	National	DM54LS374	440-78
	Raytheon	**54LS374**	★ **543**
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	TI	SN54LS374	440-90
54LS375	Fairchild	54LS375	448-89
	Motorola	SN54LS375	448-93
	Signetics	54LS375	448-104
	TI	SN54LS375	448-108
54LS377	AMD	SN54LS377	440-115
	Fairchild	54LS377	440-117
	MMI	**54LS377**	★ **509**
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	Motorola	SN54LS377	440-123
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	Raytheon	**54LS377**	★ **549**
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	TI	SN54LS377	440-132
54LS378	AMD	SN54LS378	439-177
	Fairchild	54LS378	439-179
	Motorola	SN54LS378	439-181
	TI	SN54LS378	439-184
54LS379	AMD	SN54LS379	439-99
	Fairchild	54LS379	439-101
	Motorola	SN54LS379	439-103
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54LS38	Fairchild	54LS38	444-104
	Motorola	SN54LS38	444-107
	National	DM54LS38	444-113
	Raytheon	54LS38	444-111
	Signetics	54LS38	444-117
	TI	SN54LS38	444-118
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	TI	SN54LS381	426-131
54LS382	TI	SN54LS382	426-134
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	Motorola	SN54LS384	425-165
	Raytheon	**54LS384**	★ **551**
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54LS385	AMD	SN54LS385	425-121
	Motorola	SN54LS385	425-123
	Raytheon	**54LS385**	★ **554**
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54LS386	Motorola	SN54LS386	446-23
	National	DM54LS386	446-27
	Raytheon	54LS386	446-36
	Signetics	54LS386	446-40
	TI	SN54LS386	446-44
54LS388	AMD	SN54LS388	439-122
54LS390	Fairchild	54LS390	432-110
	Motorola	SN54LS390	432-115
	TI	SN54LS390	432-121
54LS393	Fairchild	54LS393	429-143
	Motorola	SN54LS393	429-145
	TI	SN54LS393	429-148
54LS395	Fairchild	54LS395	453-155
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	Motorola	SN54LS395	1189-13
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	TI	SN54LS395A	453-166
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54LS396	TI	SN54LS396	448-151
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54LS398	Motorola	SN54LS398	439-153
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54LS399	AMD	SN54LS399	439-145
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	Motorola	SN54LS399	439-155
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	TI	SN54LS399	439-166
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54LS40	Fairchild	54LS40	442-121
	Motorola	SN54LS40	442-124
	National	DM54LS40	442-126
	Raytheon	54LS40	442-131
	Signetics	54LS40	442-133
	TI	SN54LS40	442-135
54LS42	Fairchild	54LS42	434-26
	Motorola	SN54LS42	434-29
	National	DM54LS42	434-31
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			1763-77
			¶ 204-10
672	Motorola	MC672	423-131
6721	GI	AY1-6721/5	856-135
		AY1-6721/6	856-142
673	Motorola	MC673	423-166
			¶ 182-3
	Plessey	TBA673	915-150
	Signetics	TBA673	915-151
674	Motorola	MC674	423-167
67401	**MMI**	**67401**	★**1472**
			1159-88
			1763-42
		67401A	★**1476**
			1159-90
67402	**MMI**	**67402A**	★**1476**
			1159-92
6741	RCA	CA6741	880-53
675	Hybrid Sys.	R675B-1	918-129
		R675B-2	918-131
		R675B-3	918-166
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		R675C-4	918-135
		R675C-5	918-137
		R675C-6	918-169
		R675C-7	918-139
	Motorola	MC675	424-64
67508	**MMI**	**67508**	★ **498**
			426-13
67516	**MMI**	**67516**	★ **498**
			426-44
67518	**MMI**	**67518**	★ **498**
			426-46
67558	**MMI**	**67558**	★ **495**
			426-4
			1763-45
		67558-1	★ **495**
			426-6
67559	MMI	67559	426-16
676	Motorola	MC676	423-57
			603-75
			603-93
677	Motorola	MC677	423-17
678	Motorola	MC678	423-22
679	Motorola	MC679	423-64
			423-77
68	**AMI**	**68**	★**1838**
68A00	**AMI**	**S68A00**	★**1780**
			1757-124
	Fairchild	**F68A00**	★**1887**
			1757-129
	Motorola	**MC68A00**	★**2002**
			1757-141
68A02	**Fairchild**	**F68A02**	★**1887**
			1757-150
68A09	**Fairchild**	**F68A09**	★**1887**
			1757-132
		F68A09E	★**1887**
			1757-163
	Motorola	**MC68A09**	★**2005**
			1757-144
		MC68A09E	★**2005**
			1757-166
68A10	**AMI**	**S68A10**	★**1794**
			1758-166
	Fairchild	**F68A10**	★**1887**
			1173-58
			1758-170
	Motorola	MCM68A10	1173-60
			1758-176
68A21	**AMI**	**S68A21**	★**1798**
			1758-130
			1763-157
	Fairchild	**F68A21**	★**1887**
			1758-136
			1763-162
	Motorola	**MC68A21**	★**1991**
			1758-149
			1763A-2
68A30	**Motorola**	**MCM68A30A**	★**1530**
			1185-28
			1759-2
68A308	**Fairchild**	**F68A308**	★**1887**
			1185-26
			1758-195
	Motorola	**MCM68A308**	★**1530**
			1185-29
			1759-4
68A308P7	**Motorola**	**MCM68A308P7**	★**1530**
			1185-30
68A316	**Fairchild**	**F68A316**	★**1887**
			1759-15
	Motorola	MCM68A316	1759-19
		MCM68A316A	★**1530**
			1185-106
		MCM68A316E	1185-107
68A316EP91	Motorola	MCM68A316EP91	1185-108
68A332	Motorola	MCM68A332	1186-73
			1759-21
68A332P2	Motorola	MCM68A332P2	1186-74
68A364	**Motorola**	**MCM68A364**	★**1530**
			1186-99
68A364P3	**Motorola**	**MCM68A364P3**	★**1530**
			1186-100
68A40	**Fairchild**	**F68A40**	★**1887**
			1758-55
	Motorola	**MC68A40**	★**1989**
			1758-61
68A44	**Motorola**	**MC68A44**	★**1985**
			1758-39
68A45	**Motorola**	**MC68A45**	★**1983**
			1758-27
68A46	**Motorola**	**MC68A46**	★**1981**
			1758-186
68A488	**Motorola**	**MC68A488**	★**1975**
			1758-122
68A50	**AMI**	**S68A50**	★**1818**
			1758-85
			1763-136
	Fairchild	**F68A50**	★**1887**
			1758-89
			1763-140
	Motorola	**MC68A50**	★**1977**
			1758-98
68A50	Motorola	MC68A50	1763-142
68A52	**Fairchild**	**F68A52**	★**1887**
			1758-68
	Motorola	**MC68A52**	★**1973**
			1758-76
68A54	**AMI**	**S68A54**	★**1826**
			1758-103
	Fairchild	**F68A54**	★**1887**
			1758-105
	Motorola	**MC68A54**	★**1971**
			1758-112
68A708	Motorola	MCM68A708L	1166-82
68B00	**AMI**	**S68B00**	★**1780**
			1757-125
	Fairchild	**F68B00**	★**1887**
			1757-130
	Motorola	**MC68B00**	★**2002**
			1757-142
68B02	**Fairchild**	**F68B02**	★**1887**
			1757-151
68B09	**Fairchild**	**F68B09**	★**1887**
			1757-133
		F68B09E	★**1887**
			1757-164
	Motorola	**MC68B09**	★**2005**
			1757-145
		MC68B09E	★**2005**
			1757-167
68B10	**AMI**	**S68B10**	★**1794**
			1758-167
	Fairchild	**F68B10**	★**1887**
			1173-53
			1758-171
	Motorola	MCM68B10	1173-54
			1758-177
68B21	**AMI**	**S68B21**	★**1798**
			1758-131
			1763-158
	Fairchild	**F68B21**	★**1887**
			1758-137
			1763-163
	Motorola	**MC68B21**	★**1991**
			1758-150
			1763A-3
68B30	Motorola	MCM68B30A	1185-20
			1759-3
68B308	**Fairchild**	**F68B308**	★**1887**
			1185-19
			1758-196
	Motorola	MCM68B308	1185-21
			1759-5
68B316	**Fairchild**	**F68B316**	★**1887**
			1759-16
68B364	Motorola	MCM68B364	1186-97
68B40	**Fairchild**	**F68B40**	★**1887**
			1758-56
	Motorola	**MC68B40**	★**1989**
			1758-62
68B44	**Motorola**	**MC68B44**	★**1985**
			1758-40
68B45	**Motorola**	**MC68B45**	★**1983**
			1758-28
68B46	**Motorola**	**MC68B46**	★**1981**
			1758-187
68B488	**Motorola**	**MC68B488**	★**1975**
			1758-123
68B50	**AMI**	**S68B50**	★**1818**
			1758-86
			1763-137
	Fairchild	**F68B50**	★**1887**
			1758-90
	Motorola	**MC68B50**	★**1977**
			1758-99
			1763-143
68B52	**Fairchild**	**F68B52**	★**1887**
			1758-69
	Motorola	**MC68B52**	★**1973**
			1758-77
68B54	**Fairchild**	**F68B54**	★**1887**
			1758-106
	Motorola	**MC68B54**	★**1971**
			1758-113
680	Motorola	MC680	423-6
	Plessey	SL680	915-161
	RTC	MS680	861-156
6800	**AMI**	**S6800**	★**1776**
6800	**AMI**	**S6800**	★**1780**
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			1722-3
		S6800M	★**1780**
			1757-123
	Fairchild	**F6800**	★**1886**
			★**1888**
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			1725-2
		F6800CL	★**1888**
		F6800CP	★**1888**
		F6800L	★**1888**
		F6800P	★**1888**
	Fujitsu	MBL6800E	1757-134
		MBL6800H	1757-135
		MBL6800N	1757-136
		MBM6800	1726-4
	Motorola	**MC6800**	★**2002**
			1757-139
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			¶ 199-10
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			¶ 201-10
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			¶ 205-1
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		MC6800M	★**2002**
			1757-140
		M6800	¶ 201-9
	Siemens	SAS6800	857-118
68000	Motorola	MC68000	1763-52
			1737-1
6801	**AMI**	**S6801**	★**1784**
			1757-169
	Fairchild	**F6801**	★**1887**
			1757-170
			1725-3
		F6801E	★**1887**
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	Motorola	MC6801	1757-171
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		MC6801E	1757-175
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6802	**AMI**	**S6802**	★**1785**
			1757-147
			1722-3
	Fairchild	**F6802**	★**1887**
			★**1888**
			1757-149
		F6802L	★**1888**
		F6802P	★**1888**
	Fujitsu	MBL6802E	1757-153
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	Motorola	**MC6802**	★**1995**
			1757-156
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6803	Fairchild	F6803	1757-178
	Motorola	**MC6803**	★**1993**
			1757-179
68047	**AMI**	**S68047**	★**1830**
			856-67
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6809	**AMI**	**S6809**	★**1789**
			1757-161
	Fairchild	**F6809**	★**1887**
			1757-131
			1725-4
		F6809E	★**1887**
			1757-162
	Motorola	**MC6809**	★**2005**
			1757-143
			1736-3
		MC6809E	★**2005**
			1757-165
681	**Datel**	**DAC-681**	★ **674**
		DAC-681C	★ **674**
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		DAC-681M	★ **674**
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	RTC	MS681	861-157
6810	**AMI**	**S6810**	★1790
			1173-65
			1758-163
		S6810A	★1790
			1758-164
		S6810M	★1794
			1758-165
	Fairchild	**F6810**	★1887
			★1888
			1173-62
			1758-169
		F6810L	★1888
		F6810P	★1888
	Motorola	MCM6810	1758-174
		MCM6810A	1173-56
		MCM6810A-1	1173-64
		MCM6810M	1758-175
	Siemens	SAS6810	857-119
6814	**Fairchild**	**F6814**	★1887
6816	**Fairchild**	**F6816**	★1887
682	Motorola	MC682	424-18
	RTC	MS682	861-158
6820	**AMI**	**S6820**	★1802
			1758-126
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	Fairchild	**F6820**	★1887
			1758-132
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	Fujitsu	MBL6820E	1758-138
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	Motorola	MC6820	1758-146
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6821	**AMI**	**S6821**	★1798
			★1802
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		S6821M	★1798
			1758-129
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	Fairchild	**F6821**	★1887
			★1889
			1758-135
			1763-161
		F6821L	★1889
		F6821P	★1889
	Fujitsu	MBL6821E	1758-141
		MBL6821H	1758-142
		MBL6821N	1758-143
	Motorola	**MC6821**	★1991
			1758-147
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		MC6821M	★1991
			1758-148
6828	Motorola	MC6828	1757-184
			1763-103
683	GI	C/CF683	853-116
		C683D	853-115
	Motorola	MC683	424-1
	RTC	MS683	861-159
6830	Fairchild	F6830	1185-50
			1758-192
68308	**Fairchild**	**F68308**	★1887
			★1889
			1185-52
			1758-194
		F68308L	★1889
		F68308P	★1889
6831	**AMI**	**S6831**	★1215
			★1806
			1186-37
			1759-8
		S6831A	★1215
			★1806
			1186-10
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		S6831B	★1215
			★1806
			1186-12
			1759-12
		S6831C	1186-13
68316	**Fairchild**	**F68316**	★1887

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68316	**Fairchild**	**F68316**	★1889
			1759-14
		F68316L	★1889
		F68316P	★1889
	Motorola	F68316	1186-38
		MCM68316	1158-74
68317	Fairchild	F68317	1759-17
6832	Motorola	MCM6832	1186-40
			1186-48
		MC6832	1759-18
68332	**AMI**	**S68332**	★1216
			1186-80
6834	**AMI**	**S6834**	★1809
			1164-105
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		S6834-1	★1809
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684	Motorola	MC684	423-35
6840	**AMI**	**S6840**	★1813
			1758-52
	Fairchild	**F6840**	★1887
			★1890
			1758-54
		F6840L	★1890
		F6840P	★1890
	Fujitsu	MBL6840	1758-57
	Motorola	**MC6840**	★1989
			1758-59
		MC6840M	★1989
			1758-60
6842	Motorola	MPQ6842	1758-20
6843	**Fairchild**	**F6843**	★1887
			1758-42
	Motorola	**MC6843**	★1987
			1758-44
6844	**Fairchild**	**F6844**	★1887
			1758-35
	Motorola	**MC6844**	★1985
			1758-37
		MC6844M	★1985
			1758-38
6845	**Fairchild**	**F6845**	★1887
			1758-22
	Motorola	**MC6845**	★1983
			1758-25
		MC6845M	★1983
			1758-26
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6846	**AMI**	**S6846**	★1817
			1758-179
	Fairchild	**F6846**	★1887
			★1890
			1758-181
		F6846L	★1890
		F6846P	★1890
	Fujitsu	MBL6846	1758-182
	Motorola	**MC6846**	★1981
			1758-184
		MC6846M	★1981
			1758-185
6847	**Fairchild**	**F6847**	★1887
			1763A-8
	Motorola	**MC6847**	★1979
			856-68
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68488	**AMI**	**S68488**	★1834
			1758-115
	Fairchild	**F68488**	★1887
			★1890
			1758-117
		F68488L	★1890
		F68488P	★1890
	Fujitsu	MBL68488	1758-118
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	Motorola	**MC68488**	★1975
			1758-120
		MC68488M	★1975
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685	AMD	685	¶ 171-9
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6850	**AMI**	**S6850**	★1818

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			1758-83
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		S6850M	★1818
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	Fairchild	**F6850**	★1887
			★1891
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			1758-88
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		F6850L	★1891
		F6850P	★1891
	Fujitsu	MBL6850E	1758-91
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	Motorola	**MC6850**	★1977
			625-8
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		MC6850M	★1977
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6852	**AMI**	**S6852**	★1822
			1758-64
	Fairchild	**F6852**	★1887
			★1891
			1758-66
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	Fujitsu	MBL6852E	1758-70
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	Motorola	**MC6852**	★1973
			1758-74
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		MC6852M	★1973
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6854	**AMI**	**S6854**	★1826
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	Fairchild	**F6854**	★1887
			1758-104
		F6854L	★1891
		F6854P	★1891
	Fujitsu	MBL6854	1758-109
	Motorola	**MC6854**	★1971
			1758-111
6856	**Fairchild**	**F6856**	★1887
			★1892
			625-56
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		F6856DC	★1892
		F6856DL	★1892
		F6856DM	★1892
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6860	Fairchild	F6860	625-13
			1758-46
	Motorola	MC6860	625-14
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		MC6860L	★1968
			1758-49
6862	Fairchild	F6862	1758-32
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	Motorola	**MC6862**	★1966
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687	AMD	687	¶ 171-9
		687AL	847-27
		687AM	847-8
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6870	Motorola	MC6870	1758-16

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68701	Motorola	MC68701	1757-181
68708	**Fairchild**	**F68708**	★1887
			1166-99
	Motorola	MCM68708L	1166-108
		MCM68708ML	1166-107
6871	Motorola	MC6871	1758-17
68716	**Fairchild**	**F68716**	★1887
			1167-104
6875	Motorola	MC6875	1758-18
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688	Motorola	MC688	423-96
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6880	Motorola	MC6880	616-5
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6881	Motorola	MC6881	458-55
			1758-11
6885	Motorola	MC6885	1758-6
6886	Motorola	MC6886	1758-7
6887	Motorola	MC6887	1758-8
6888	Motorola	MC6888	1758-9
6889	Motorola	MC6889	458-108
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689	GI	CF689	853-121
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690	Motorola	MC690	423-7
691	Motorola	MC691	424-60
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696	Motorola	MC696	424-53
697	Motorola	MC697	423-8
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70	**Burr-Brown**	**DAC70**	★ 658
		DAC70/CCD	★ 658
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	TI	SN74LS163A	430-53
74LS164	AMD	SN74LS164	454-152
			1191-38
	Fairchild	74LS164	454-154
			1191-42
	Hitachi	HD74LS164	454-155
			1191-46
	Motorola	SN74LS164	454-157
			1191-49
	National	DM74LS164	454-159
			1191-55
	NEC America	μPB74LS164	454-160
			1191-57
	Raytheon	74LS164	454-164
			1191-61
	Signetics	74LS164	454-166
			1191-65
	TI	SN74LS164	454-168
74LS164	TI	SN74LS164	1191-70
74LS165	Fairchild	74LS165	454-107
			1191-12
	Motorola	SN74LS165	454-109
			1191-20
	TI	SN74LS165	454-111
			1191-26
74LS166	Motorola	SN74LS166	454-126
	TI	SN74LS166	454-128
			1191-30
74LS168	AMD	SN74LS168A	433-32
	Fairchild	74LS168	433-35
	Motorola	SN74LS168	433-37
	National	DM74LS168	433-39
	TI	SN74LS168	433-41
74LS169	AMD	SN74LS169A	431-36
	Fairchild	74LS169	431-39
	Motorola	SN74LS169	431-41
	National	DM74LS169	431-43
	TI	SN74LS169	431-45
74LS170	Fairchild	74LS170	448-189
			1171-48
	Motorola	SN74LS170	448-191
			1171-53
	National	DM74LS170	448-193
			1171-57
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			1171-44
	Signetics	74LS170	449-5
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	TI	SN74LS170	449-7
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74LS173	Fairchild	74LS173A	439-30
	Motorola	SN74LS173A	439-32
	National	DM74LS173	439-34
	Signetics	74LS173	439-36
	TI	SN74LS173	439-38
74LS174	AMD	SN74LS174	440-11
	Fairchild	74LS174	440-15
	Hitachi	HD74LS174	440-16
	Motorola	SN74LS174	440-17
	National	DM74LS174	440-19
	Raytheon	74LS174	440-25
	Signetics	74LS174	440-27
	TI	SN74LS174	440-29
74LS175	AMD	SN74LS175	439-61
	Fairchild	74LS175	439-65
	Hitachi	HD74LS175	439-66
	Motorola	SN74LS175	439-70
	National	DM74LS175	439-72
	NEC America	μPB74LS175	439-73
	Raytheon	74LS175	439-79
	Signetics	74LS175	439-81
	TI	SN74LS175	439-83
74LS181	AMD	SN74LS181	426-97
	Fairchild	74LS181	426-101
	Motorola	SN74LS181	426-103
	Raytheon	74LS181	426-107
	Signetics	74LS181	426-111
	TI	SN74LS181	426-113
74LS183	TI	SN74LS183	425-110
74LS189	**Fairchild**	**74LS189**	**★ 485**
			1172-46
	Motorola	SN74LS189	1172-44
	National	DM74LS189	1172-107
	TI	SN74LS189A	1172-84
74LS190	AMD	SN74LS190	432-151
	Fairchild	74LS190	432-155
	Motorola	SN74LS190	432-157
	National	DM74LS190	432-159
	Raytheon	74LS190	432-165
	Signetics	74LS190	432-167
	TI	SN74LS190	432-169
74LS191	AMD	SN74LS191	430-162
	Fairchild	74LS191	430-166
	Motorola	SN74LS191	430-168
	National	DM74LS191	430-170
	Raytheon	74LS191	430-176
	Signetics	74LS191	430-178
	TI	SN74LS191	430-180
74LS192	AMD	SN74LS192	432-199
	Fairchild	74LS192	433-5
	Motorola	SN74LS192	433-7
	National	DM74LS192	433-9
	NEC America	μPB74LS192	433-10
	Raytheon	74LS192	433-16
74LS192	Signetics	74LS192	433-18
	TI	SN74LS192	433-20
74LS193	AMD	SN74LS193	431-11
	Fairchild	74LS193	431-15
	Motorola	SN74LS193	431-17
	National	DM74LS193	431-19
	NEC America	μPB74LS193	431-20
	Raytheon	74LS193	431-26
	Signetics	74LS193	431-28
	TI	SN74LS193	431-30
74LS194	AMD	SN74LS194A	453-110
			1188-53
	Fairchild	74LS194A	453-114
			1188-109
	Hitachi	HD74LS194A	453-115
			1188-66
	Motorola	SN74LS194A	453-117
			1189-6
	NEC America	μPB74LS194	453-118
			1188-75
	Raytheon	SN74LS194A	1189-28
		74LS194A	453-124
	Signetics	74LS194	1188-85
		74LS194A	453-125
	TI	SN74LS194A	453-127
			1188-97
74LS195	AMD	SN74LS195A	453-30
			1188-101
	Fairchild	74LS195	453-34
		74LS195A	1188-115
	Hitachi	HD74LS195A	453-35
			1189-2
	Motorola	SN74LS195A	453-37
			1189-10
	NEC America	μPB74LS195	453-38
			1189-22
	Raytheon	74LS195A	453-44
			1189-32
	Signetics	74LS195A	453-46
			1189-40
	TI	SN74LS195A	453-48
			1189-46
74LS196	Fairchild	74LS196	431-165
	Motorola	SN74LS196	431-167
	National	DM74LS196	431-169
	Raytheon	74LS196	431-173
	Signetics	74LS196	431-174
	TI	SN74LS196	431-176
74LS197	Fairchild	74LS197	429-192
	Motorola	SN74LS197	429-194
	National	DM74LS197	429-196
	Raytheon	74LS197	429-200
	Signetics	74LS197	429-201
	TI	SN74LS197	430-3
74LS20	Fairchild	74LS20	442-61
	Hitachi	HD74LS20	442-62
	Motorola	SN74LS20	442-64
	National	DM74LS20	442-66
	NEC America	μPB74LS20	442-67
	Raytheon	74LS20	442-72
	Signetics	74LS20	442-74
	TI	SN74LS20	442-76
74LS207	TI	SN74LS207	1174-80
74LS208	TI	SN74LS208	1174-81
74LS21	Fairchild	74LS21	440-156
	Hitachi	HD74LS21	440-157
	Motorola	SN74LS21	440-159
	National	DM74LS21	440-161
	NEC America	μPB74LS21	440-162
	Raytheon	74LS21	440-166
	Signetics	74LS21	440-168
	TI	SN74LS21	440-170
74LS214	TI	SN74LS214	1177-51
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74LS22	Fairchild	74LS22	442-169
	Hitachi	HD74LS22	442-170
	Motorola	SN74LS22	442-172
	National	DM74LS22	442-174
	Raytheon	74LS22	442-178
	Signetics	74LS22	442-180
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			608-16
	Fairchild	74LS240	458-184
			608-20
	MMI	**74LS240**	★ **768**
			458-188
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	Motorola	SN74LS240	458-196
			608-40
	Raytheon	**74LS240**	★ **522**
			459-5
			608-48
	Signetics	74LS240	459-6
			608-49
	TI	SN74LS240	459-8
			608-51
74LS241	AMD	SN74LS241	459-36
			607-21
	Fairchild	74LS241	459-40
			607-31
	MMI	**74LS241**	★ **768**
			459-44
			607-37
	Motorola	SN74LS241	459-48
			607-53
	Raytheon	**74LS241**	★ **525**
			459-54
			607-63
	Signetics	74LS241	459-55
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	TI	SN74LS241	459-57
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74LS242	AMD	SN74LS242	458-69
			616-28
	Fairchild	74LS242	458-75
			616-33
	Motorola	SN74LS242	458-79
			616-35
	Raytheon	**74LS242**	★ **528**
			458-87
			616-39
	Signetics	74LS242	458-94
			616-43
	TI	SN74LS242	458-97
			616-45
74LS243	AMD	SN74LS243	458-73
			616-32
	Fairchild	74LS243	458-77
			616-34
	Motorola	SN74LS243	458-81
			616-36
	Raytheon	**74LS243**	★ **528**
			458-93
			616-42
	Signetics	74LS243	458-95
			616-44
	TI	SN74LS243	458-99
			616-46
74LS244	AMD	SN74LS244	459-73
			607-27
	Fairchild	74LS244	459-75
			607-33
	MMI	**74LS244**	★ **768**
			459-77
			607-41
	Motorola	SN74LS244	459-81
			607-55
	Raytheon	**74LS244**	★ **525**
			459-87
			608-4
	Signetics	74LS244	459-88
			608-6
	TI	SN74LS244	459-90
			608-12
74LS245	AMD	SN74LS245	459-114
			618-30
	Fairchild	74LS245	459-116
			618-31
	MMI	**74LS245**	★ **774**
			459-118
			618-32
	Motorola	SN74LS245	459-124
			618-35
74LS245	Signetics	74LS245	459-129
			618-38
	TI	SN74LS245	459-132
			618-40
74LS247	Fairchild	74LS247	601-137
	Hitachi	HD74LS247	601-142
	Motorola	SN74LS247	601-150
	National	DM74LS247	601-156
	TI	SN74LS247	601-169
74LS248	Fairchild	74LS248	601-50
	Hitachi	HD74LS248	601-54
	Motorola	SN74LS248	601-61
	National	DM74LS248	601-71
	TI	SN74LS248	601-85
74LS249	Fairchild	74LS249	601-93
	Hitachi	HD74LS249	601-95
	Motorola	SN74LS249	601-99
	National	DM74LS249	601-105
	TI	SN74LS249	601-115
74LS251	AMD	SN74LS251	451-183
	Fairchild	74LS251	451-187
	Hitachi	HD74LS251	451-188
	Motorola	SN74LS251	451-190
	NEC America	μPB74LS251	1762-131
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	TI	SN74LS251	451-200
			1762-133
74LS253	AMD	SN74LS253	450-194
	Fairchild	74LS253	450-198
	Hitachi	HD74LS253	450-199
	Motorola	SN74LS253	450-201
	National	DM74LS253	451-2
	NEC America	μPB74LS253	451-3
	Raytheon	74LS253	451-9
	Signetics	74LS253	451-11
	TI	SN74LS253	451-13
74LS255	Raytheon	74LS255	434-169
74LS256	Fairchild	74LS256	447-154
	Motorola	SN74LS256	447-156
74LS257	AMD	SN74LS257	450-48
	Fairchild	74LS257	450-52
	Hitachi	HD74LS257	450-53
	Motorola	SN74LS257A	450-55
	National	DM74LS257	450-57
	Raytheon	74LS257	450-64
	Signetics	74LS257	450-66
	TI	SN74LS257A	450-68
74LS258	AMD	SN74LS258	450-14
	Fairchild	74LS258	450-18
	Hitachi	HD74LS258	450-19
	Motorola	SN74LS258A	450-21
	National	DM74LS258	450-23
	NEC America	μPB74LS258	450-24
	Raytheon	74LS258	450-30
	Signetics	74LS258	450-31
	TI	SN74LS258A	450-33
74LS259	Fairchild	74LS259	447-147
	Motorola	SN74LS259	447-149
	TI	SN74LS259	447-151
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74LS26	Fairchild	74LS26	444-127
	Hitachi	HD74LS26	444-128
	Motorola	SN74LS26	444-130
	National	DM74LS26	444-132
	Raytheon	74LS26	444-136
	Signetics	74LS26	444-139
	TI	SN74LS26	444-141
74LS260	Fairchild	74LS260	446-193
	Motorola	SN74LS260	446-195
	Signetics	74LS260A	446-197
74LS261	Raytheon	74LS261	425-139
	Signetics	74LS261	425-141
	TI	SN74LS261	425-143
74LS266	Fairchild	74LS266	446-101
	Motorola	SN74LS266	446-103
	National	DM74LS266	446-105
	Raytheon	74LS266	446-109
	Signetics	74LS266	446-111
	TI	SN74LS266	446-113
74LS27	Fairchild	74LS27	447-25
	Hitachi	HD74LS27	447-26
	Motorola	SN74LS27	447-28
	National	DM74LS27	447-30
	NEC America	μPB74LS27	447-31
	Raytheon	74LS27	447-35
	Signetics	74LS27	447-37
74LS27	TI	SN74LS27	447-39
74LS273	AMD	SN74LS273	440-46
	Fairchild	74LS273	440-48
	MMI	**74LS273**	★ **509**
			440-50
	Motorola	SN74LS273	440-54
	Raytheon	**74LS273**	★ **531**
			440-60
	Signetics	74LS273	440-61
	TI	SN74LS273	440-63
74LS275	TI	SN74LS275	426-54
74LS279	Fairchild	74LS279	448-121
	Motorola	SN74LS279	448-123
	National	DM74LS279	448-125
	NEC America	μPB74LS279	448-126
	Raytheon	74LS279	448-130
	Signetics	74LS279	448-132
	TI	SN74LS279	448-134
74LS28	Fairchild	74LS28	447-67
	Motorola	SN74LS28	447-74
	Raytheon	74LS28	447-85
	Signetics	74LS28	447-89
	TI	SN74LS28	447-93
74LS280	Fairchild	74LS280	457-22
	TI	SN74LS280	457-24
74LS281	AMD	SN74LS281	426-188
74LS283	Fairchild	74LS283	425-52
	Hitachi	HD74LS283A	425-54
	MMI	74LS283	425-56
	Motorola	SN74LS283	425-60
	National	DM74LS283	425-64
	Raytheon	74LS283	425-73
	Signetics	74LS283	425-77
	TI	SN74LS283	425-81
74LS289	Motorola	SN74LS289	1172-45
	National	DM74LS289	1172-110
	TI	SN74LS289	1172-79
74LS290	Fairchild	74LS290	431-103
	Motorola	SN74LS290	431-107
	National	DM74LS290	431-111
	Signetics	74LS290	431-119
	TI	SN74LS290	431-123
74LS293	Fairchild	74LS293	429-116
	Motorola	SN74LS293	429-120
	National	DM74LS293	429-124
	Signetics	74LS293	429-132
	TI	SN74LS293	429-137
74LS295	Fairchild	74LS295	453-141
		74LS295A	1188-119
	Motorola	SN74LS295A	453-143
			1189-12
	NEC America	μPB74LS295	453-144
			1189-23
	Raytheon	74LS295A	453-148
			1189-36
	Signetics	74LS295A	1188-45
		74LS295B	453-149
	TI	SN74LS295B	453-151
			1189-48
74LS297	TI	SN74LS297	457-52
			898-53
74LS298	AMD	SN74LS298	449-137
	Fairchild	74LS298	439-150
			449-139
			450-112
	Hitachi	HD74LS298	450-113
	Motorola	SN74LS298	439-152
			449-141
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	Raytheon	74LS298	439-160
			449-147
			450-123
	Signetics	74LS298	439-161
			450-124
	TI	SN74LS298	439-163
			449-149
			450-126
74LS299	AMD	SN74LS299	454-58
			1190-69
	Fairchild	74LS299	454-62
			1190-98
	MMI	74LS299	454-66
			1190-102
	Motorola	SN74LS299	454-71
	Raytheon	**74LS299**	★ **533**
			454-81
74LS299	TI	SN74LS299	454-87
			1190-116
74LS30	Fairchild	74LS30	441-179
	Hitachi	HD74LS30	441-180
	Motorola	SN74LS30	441-182
	National	DM74LS30	441-184
	NEC America	μPB74LS30	441-185
	Raytheon	74LS30	441-189
	Signetics	74LS30	441-191
	TI	SN74LS30	441-193
74LS314	TI	SN74LS314	1177-50
74LS315	TI	SN74LS315	1177-44
74LS319	TI	SN74LS319	1172-81
74LS32	Fairchild	74LS32	446-139
	Hitachi	HD74LS32	446-140
	Motorola	SN74LS32	446-142
	National	DM74LS32	446-144
	NEC America	μPB74LS32	446-145
	Raytheon	74LS32	446-149
	Signetics	74LS32	446-151
	TI	SN74LS32	446-153
74LS320	TI	SN74LS320	458-21
74LS321	TI	SN74LS321	458-23
74LS322	AMD	SN74LS322	425-183
			454-199
	MMI	74LS322	425-185
			455-4
	Motorola	SN74LS322	425-187
			455-6
	Raytheon	**74LS322**	★ **537**
			455-10
	TI	SN74LS322A	425-191
			455-12
74LS323	AMD	SN74LS323	454-60
			1190-96
	Fairchild	74LS323	454-64
			1190-100
	MMI	74LS323	454-69
			1190-104
	Motorola	SN74LS323	454-73
	Raytheon	**74LS323**	★ **540**
			454-85
			1190-114
	TI	SN74LS323	454-89
			1190-118
74LS324	TI	SN74LS324	458-18
			899-57
74LS325	TI	SN74LS325	458-29
			899-116
74LS326	TI	SN74LS326	458-31
			899-118
74LS327	TI	SN74LS327	458-33
			899-120
74LS328	TI	SN74LS328	458-37
			899-122
74LS33	Fairchild	74LS33	447-109
	Motorola	SN74LS33	447-111
	Raytheon	74LS33	447-115
	Signetics	74LS33	447-117
	TI	SN74LS33	447-119
74LS347	TI	SN74LS347	601-125
			601-171
74LS348	AMD	SN74LS348	1762-142
	TI	SN74LS348	456-173
			1762-143
74LS352	Fairchild	74LS352	451-23
	Motorola	SN74LS352	451-25
	National	DM74LS352	451-27
	TI	SN74LS352	451-29
74LS353	Fairchild	74LS353	451-32
	Motorola	SN74LS353	451-34
	National	DM74LS353	451-36
	TI	SN74LS353	451-38
74LS360	TI	SN74LS360	456-35
74LS361	TI	SN74LS361	456-38
74LS362	TI	SN74LS362	1762-116
74LS363	Signetics	74LS363	447-180
	TI	SN74LS363	447-183
74LS364	Signetics	74LS364	440-86
	TI	SN74LS364	440-89
74LS365	Fairchild	74LS365	428-31
	Motorola	SN74LS365A	428-36
	National	DM74LS365	428-40
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	Motorola	SN74LS366A	429-34
	National	DM74LS366	429-38
	NEC America	μPB74LS366	429-41
	Raytheon	74LS366	429-46
	Signetics	74LS366A	429-52
	TI	SN74LS366A	429-56
74LS367	Fairchild	74LS367	428-33
	Hitachi	HD74LS367	428-34
	Motorola	SN74LS367A	428-38
	National	DM74LS367	428-42
	NEC America	μPB74LS367	428-44
	Raytheon	74LS367	428-52
	Signetics	74LS367A	428-56
	TI	SN74LS367A	428-60
74LS368	Fairchild	74LS368	429-31
	Hitachi	HD74LS368	429-32
	Motorola	SN74LS368A	429-36
	National	DM74LS368	429-40
	NEC America	μPB74LS368	429-42
	Raytheon	74LS368	429-50
	Signetics	74LS368A	429-54
	TI	SN74LS368A	429-58
74LS37	Fairchild	74LS37	443-178
	Hitachi	HD74LS37	443-179
	Motorola	SN74LS37	443-181
	National	DM74LS37	443-183
	NEC America	μPB74LS37	443-184
	Raytheon	74LS37	443-188
	Signetics	74LS37	443-190
	TI	SN74LS37	443-192
74LS373	AMD	SN74LS373	447-165
	Fairchild	74LS373	447-167
	MMI	**74LS373**	★ **505**
			447-169
	Motorola	SN74LS373	447-171
	Raytheon	**74LS373**	★ **543**
			447-179
	Signetics	74LS373	447-181
	TI	SN74LS373	447-185
74LS374	AMD	SN74LS374	440-69
	Fairchild	74LS374	440-71
	MMI	**74LS374**	★ **505**
			440-73
	Motorola	SN74LS374	440-75
	National	DM74LS374	440-79
	Raytheon	**74LS374**	★ **543**
			440-85
	Signetics	74LS374	440-87
	TI	SN74LS374	440-91
74LS375	Fairchild	74LS375	448-90
	Motorola	SN74LS375	448-94
	NEC America	μPB74LS375	448-97
	Signetics	74LS375	448-105
	TI	SN74LS375	448-109
74LS377	AMD	SN74LS377	440-116
	Fairchild	74LS377	440-118
	MMI	**74LS377**	★ **509**
			440-122
	Motorola	SN74LS377	440-124
			448-59
	Raytheon	**74LS377**	★ **549**
			440-130
	Signetics	74LS377	440-131
	TI	SN74LS377	440-133
74LS378	AMD	SN74LS378	439-178
	Fairchild	74LS378	439-180
	Motorola	SN74LS378	439-182
	Signetics	74LS378	439-183
	TI	SN74LS378	439-185
74LS379	AMD	SN74LS379	439-100
	Fairchild	74LS379	439-102
	Motorola	SN74LS379	439-104
	TI	SN74LS379	439-106
74LS38	Fairchild	74LS38	444-105
	Hitachi	HD74LS38	444-106
	Motorola	SN74LS38	444-108
	National	DM74LS38	444-114
	NEC America	μPB74LS38	444-115
	Raytheon	74LS38	444-112
	Signetics	74LS38	444-116
	TI	SN74LS38	444-119
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	Hitachi	HD74177	429-158
	Motorola	MC74177	429-164
	National	DM74177	429-174
	Signetics	74177	429-183
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74178	Fairchild	74178	453-171
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	TI	SN74178	453-179
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74179	Fairchild	74179	453-185
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	TI	SN74179	453-193
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74180	Fairchild	74180	457-2
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	Ferranti	ZN74181	426-78
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74187	National	DM74187	1183-41
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74190	Fairchild	74190	432-137
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74247	TI	SN74247	601-165
74248	TI	SN74248	601-81
74249	TI	SN74249	601-111
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74259	AMD	SN74259	447-135
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7426	Fairchild	7426	436-6
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74265	TI	SN74265	457-102
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74276	TI	SN74276	438-144
74278	TI	SN74278	456-141
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	Ferranti	ZN7432	446-127
	Hitachi	HD7432	446-128
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74366	National	DM74366	429-13
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74368	National	DM74368	429-15
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7438	Fairchild	7438	444-84
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7439	Fairchild	7439	444-85
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74390	TI	SN74390	432-107
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7440	Fairchild	7440	442-101
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	Hitachi	HD7440	442-106
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7443	Fairchild	7443	433-150
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74468	Motorola	MC74468	455-87
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7475	Fairchild	7475	448-71
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7489	AMD	SN7489	1172-87
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7550	AD	AD7550B	582-45
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75530	TI	SN75530	602-100
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7621	**Harris**	**HM7621**	★1284
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76242	TI	SN76242	859-43
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7625	**Harris**	**HM7625**	★1300
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7629	**Harris**	**HM7629-5**	★1302
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76298	TI	SN76298	859-47
7640	**Harris**	**HM7640**	★1284
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7642	**Harris**	**HM7642**	★1284
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		HM7642-5	★1284
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76428	TI	SN76428	856-38
76429	TI	SN76429	856-39
7643	**Harris**	**HM7643**	★1284
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76442	TI	SN76442	856-42
76443	TI	SN76443	856-43
76445	TI	SN76445	856-44
7645	Harris	HM7645	★1314
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76450	TI	SN76450	856-45
76460	TI	SN76460	856-46
76462	TI	SN76462	856-47
7647	**Harris**	**HM7647R**	★1318
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76477	TI	SN76477	856-61
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7648	**Harris**	**HM7648**	★1320
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7649	**Harris**	**HM7649**	★1320
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76565	TI	SN76565	858-2
76600	TI	SN76600	861-3
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76642	TI	SN76642	855-84
76643	TI	SN76643	855-85
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76644	TI	SN76644	861-4
76650	TI	SN76650	861-5
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76676	TI	SN76676	855-12
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76689	TI	SN76689	855-88
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7681	**Harris**	**HM7681**	★1322
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7683	**Harris**	**HM7683**	★1331
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7684	**Harris**	**HM7684**	★1333
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7685	**Harris**	**HM7685**	★1333
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772	**Fairchild**	**μA772**	★ 938
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		μA772ADC	★ 938
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78	**Fairchild**	**μA78CB**	★ 934
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78C08	**Fairchild**	**μA78C08C**	★ 935
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78C10	**Fairchild**	**μA78C10C**	★ 935
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78C12	**Fairchild**	**μA78C12C**	★ 935
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78C15	**Fairchild**	**μA78C15C**	★ 935
			906-68
78C17	**Fairchild**	**μA78C17C**	★ 935
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78C18	**Fairchild**	**μA78C18C**	★ 935
			907-23
78C20	**Fairchild**	**μA78C20C**	★ 935
			907-67
	National	DS78C20	612-51
78C22	**Fairchild**	**μA78C22**	★ 935
			907-83
78C24	**Fairchild**	**μA78C24C**	★ 935
			907-99
78C29	National	MM78C29	417-26
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78C30	National	MM78C30	417-23
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78C82	Fairchild	μA78C82C	905-31
78HV05	Signetics	μA78HV05	903-113
78HV06	Signetics	μA78HV06	904-63
78HV08	Signetics	μA78HV08	905-16
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78H05	**Fairchild**	**μA78H05**	★ 934
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78H15	**Fairchild**	**μA78H15**	★ 934
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78L006	Toshiba	TA78L006	904-24
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78L007	Toshiba	TA78L007	904-83
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78L008	Toshiba	TA78L008	904-103
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78L010	Toshiba	TA78L010	905-53
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78L012	Toshiba	TA78L012	905-85
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78L015	Toshiba	TA78L015	906-60
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78L018	Toshiba	TA78L018	907-19
		TA78L018A	907-20
78L02	Motorola	MC78L02C	903-5
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78L020	Toshiba	TA78L020	907-65
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78L05	**Fairchild**	**μA78L05C**	★ 935
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	Signetics	μA78L05C	903-18
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78L06	**National**	**LM78L06A**	★1060
			904-22
		LM78L06C	★1060
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	Signetics	μA78L06C	904-80
	TI	μA78L06AC	904-82
		μA78L06C	904-81
78L075	Toshiba	TA78L075	904-87
		TA78L075A	904-88
78L08	**Fairchild**	**μA78L08C**	★ 935
			904-93
	Motorola	MC78L08C	904-94
	National	**LM78L08A**	★1060
			904-98
		LM78L08C	★1060
			904-99
	NEC America	μPC78L08	904-100
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78L09	**Fairchild**	**μA78L09C**	★ 935
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78L10	National	LM78L10A	905-49
		LM78L10C	★1060
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	TI	μA78L10AC	905-52
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78L12	**Fairchild**	**μA78L12C**	★ 935
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	Motorola	MC78L12C	905-75
	National	DS78L12	455-111
		LM78L12A	★1060
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78L132	Toshiba	TA78L132	906-37
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78L15	**Fairchild**	**μA78L15C**	★ 935
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	Motorola	MC78L15C	906-50
	National	**LM78L15A**	★1060
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		LM78L15C	★1060
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	NEC America	μPC78L15	906-56
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78L18	**Fairchild**	**μA78L18**	★ 935
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	Motorola	MC78L18C	907-13
	National	**LM78L18A**	★1060
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		LM78L18C	★1060
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78L24	**Fairchild**	**μA78L24**	★ 935
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	Motorola	MC78L24C	907-89
	National	**LM78L24A**	★1060
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78L26	Fairchild	μA78L26C	903-4
78L62	Fairchild	μA78L62C	904-79
78L82	Fairchild	μA78L82C	905-32
78MHV05	Signetics	μA78MHV05	903-61
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78MHV06	Signetics	μA78MHV06	904-39
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78MHV08	Signetics	μA78MHV08	904-116
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78MHV12	Signetics	μA78MHV12	905-106
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78MHV15	Signetics	μA78MHV15	906-78
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78M05	**Fairchild**	**μA78M05C**	★ 935
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		μA78M05M	★ 935
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	Motorola	MC78M05C	903-51
	National	**LM78M05**	★1060
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	NEC America	μPC78M05	903-54
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78M06	**Fairchild**	**μA78M06C**	★ 935
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		μA78M06M	★ 935
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	Motorola	MC78M06C	904-30
	National	**LM78M06**	★1060
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78M08	**Fairchild**	**μA78M08C**	★ 935
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		μA78M08M	★ 935
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78M20	**Fairchild**	**μA78M20C**	★ **935**
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78M24	**Fairchild**	**μA78M24C**	★ **935**
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78PO5	**Fairchild**	**μA78PO5**	★ **934**
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78P05	**Fairchild**	**μA78P05**	★ **934**
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78S40	**Fairchild**	**μA78S40**	★ **935**
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7805	**Fairchild**	**μA7805C**	★ **935**
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		9LS112M	437-184
9LS113	Fairchild	9LS113C	437-114
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	Raytheon	9LS113C	437-124
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9LS114	Fairchild	9LS114C	437-145
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	Raytheon	9LS114C	437-154
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9LS12	Raytheon	9LS12C	443-83
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9LS122	Raytheon	9LS122C	452-95
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9LS123	Raytheon	9LS123C	452-163
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9LS125	Fairchild	9LS125C	427-157
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	Raytheon	9LS125C	427-165
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9LS126	Fairchild	9LS126C	427-188
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	Raytheon	9LS126C	427-196
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9LS13	Fairchild	9LS13C	457-128
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	Raytheon	9LS13C	457-138
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9LS132	Fairchild	9LS132C	457-159
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	Raytheon	9LS132C	457-168
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9LS133	Fairchild	9LS133C	442-23
		9LS133M	442-24
9LS136	Fairchild	9LS136C	446-67
		9LS136M	446-69
	Raytheon	9LS136C	446-77
		9LS136M	446-78
9LS138	Fairchild	9LS138C	435-15
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	Raytheon	9LS138C	435-25
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9LS139	Fairchild	9LS139C	434-175
		9LS139M	434-176
	Raytheon	9LS139C	434-185
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9LS14	Fairchild	9LS14C	457-193
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	Raytheon	9LS14C	458-8
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9LS15	Fairchild	9LS15C	441-33
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	Raytheon	9LS15C	441-42
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9LS151	Fairchild	9LS151C	451-126
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	Raytheon	9LS151C	451-137
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9LS152	Fairchild	9LS152C	451-64
		9LS152M	451-65
	Raytheon	9LS152C	451-72
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9LS153	Fairchild	9LS153C	450-156
		9LS153M	450-157
	Raytheon	9LS153C	450-166
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9LS155	Fairchild	9LS155C	434-116
		9LS155M	434-117
	Raytheon	9LS155C	434-126
		9LS155M	434-127
9LS156	Fairchild	9LS156C	434-148
		9LS156M	434-149
	Raytheon	9LS156C	434-157
		9LS156M	434-158
9LS157	Fairchild	9LS157C	449-90
		9LS157M	449-91
	Raytheon	9LS157C	449-100
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9LS158	Fairchild	9LS158C	449-176
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9LS160	Fairchild	9LS160C	432-13
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	Raytheon	9LS160C	432-22
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9LS161	Fairchild	9LS161C	430-94
		9LS161M	430-95
	Raytheon	9LS161C	430-104
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9LS162	Fairchild	9LS162C	432-57
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	Raytheon	9LS162C	432-66
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9LS163	Fairchild	9LS163C	430-35
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	Raytheon	9LS163C	430-44
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9LS164	Raytheon	9LS164C	454-161
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9LS168	Fairchild	9LS168C	433-33
9LS169	Fairchild	9LS169C	431-37
9LS170	Fairchild	9LS170C	448-186
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9LS173	Fairchild	9LS173C	439-27
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9LS174	Fairchild	9LS174C	440-12
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	Raytheon	9LS174C	440-20
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9LS175	Fairchild	9LS175C	439-62
		9LS175M	439-63
	Raytheon	9LS175C	439-75
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9LS181	Fairchild	9LS181C	426-98
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9LS190	Fairchild	9LS190C	432-152
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9LS191	Fairchild	9LS191C	430-163
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9LS192	Fairchild	9LS192C	432-200
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9LS193	Fairchild	9LS193C	431-12
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9LS194	Fairchild	9LS194C	453-111
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9LS195	Fairchild	9LS195C	453-31
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	Raytheon	9LS195AC	453-39
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9LS196	Fairchild	9LS196C	431-162
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9LS197	Fairchild	9LS197C	429-189
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	Raytheon	9LS22C	442-175
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9LS240	**Raytheon**	**9LS240C**	★ 522
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9LS241	**Raytheon**	**9LS241C**	★ 525
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9LS242	**Raytheon**	**9LS242C**	★ 528
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9LS243	**Raytheon**	**9LS243C**	★ 528
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9LS244	**Raytheon**	**9LS244C**	★ 525
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9LS251	Fairchild	9LS251C	451-184
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9LS253	Fairchild	9LS253C	450-195
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	Raytheon	9LS253C	451-4
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9LS255	Raytheon	9LS255C	434-166
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9LS257	Fairchild	9LS257C	450-49
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	Raytheon	9LS257C	450-59
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9LS258	Fairchild	9LS258C	450-15
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9LS259	Fairchild	9LS259C	447-144
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9LS26	Fairchild	9LS26C	444-124
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9LS260	Fairchild	9LS260C	446-190
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9LS261	Raytheon	9LS261C	425-136
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9LS266	Fairchild	9LS266C	446-98
		9LS266M	446-99
	Raytheon	9LS266C	446-106
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9LS27	Fairchild	9LS27C	447-22
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9LS273	**Raytheon**	**9LS273C**	★ 531
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9LS279	Fairchild	9LS279C	448-118
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9LS28	Fairchild	9LS28C	447-66
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9LS28	Raytheon	9LS28M	447-83
9LS283	Fairchild	9LS283C	425-47
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	Raytheon	9LS283C	425-69
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9LS290	Fairchild	9LS290C	431-98
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9LS293	Fairchild	9LS293C	429-111
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9LS295	Fairchild	9LS295C	453-138
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9LS298	Fairchild	9LS298C	439-147
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9LS299	**Raytheon**	**9LS299C**	★ 533
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9LS30	Fairchild	9LS30C	441-176
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9LS322	**Raytheon**	**9LS322C**	★ 537
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9LS323	**Raytheon**	**9LS323C**	★ 540
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9LS33	Fairchild	9LS33C	447-107
	Raytheon	9LS33C	447-112
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9LS365	Fairchild	9LS365C	428-26
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	Raytheon	9LS365C	428-45
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9LS366	Fairchild	9LS366C	429-24
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	Raytheon	9LS366C	429-43
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9LS367	Fairchild	9LS367C	428-28
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	Raytheon	9LS367C	428-49
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9LS368	Fairchild	9LS368C	429-26
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	Raytheon	9LS368C	429-47
		9LS368M	429-48
9LS37	Fairchild	9LS37C	443-175
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9LS373	**Raytheon**	**9LS373C**	★ 543
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9LS374	**Raytheon**	**9LS374C**	★ 543
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9LS377	**Raytheon**	**9LS377C**	★ 549
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9LS38	Fairchild	9LS38C	444-102
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9LS384	**Raytheon**	**9LS384C**	★ 551
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9LS385	**Raytheon**	**9LS385C**	★ 554
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9LS393	Fairchild	9LS393C	429-141
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9LS42	Fairchild	9LS42C	434-24
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9LS43	Raytheon	9LS43C	433-159
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9LS44	Raytheon	9LS44C	433-174
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9LS490	Fairchild	9LS490C	432-112
9LS51	Fairchild	9LS51C	445-88
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	Raytheon	9LS51C	445-98
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9LS54	Fairchild	9LS54C	444-179
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	Raytheon	9LS54C	444-189
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9LS55	Fairchild	9LS55C	445-107
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9LS670	Fairchild	9LS670C	449-10
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9LS73	Fairchild	9LS73C	438-44
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9LS74	Fairchild	9LS74C	438-167
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9LS75	Raytheon	9LS75C	448-98
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9LS76	Raytheon	9LS76C	438-117
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9LS77	Raytheon	9LS77C	448-61
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9LS78	Raytheon	9LS78C	437-67
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9LS83	Fairchild	9LS83C	425-45
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9LS86	Fairchild	9LS86C	446-15
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9LS92	Fairchild	9LS92C	433-84
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9LS93	Fairchild	9LS93C	429-109
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9LS95	Fairchild	9LS95C	453-77
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9S05	Fairchild	9S05AC	428-199
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9S41	Fairchild	9S41C	441-155
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			¶ 194-12
		93453C	★1264
			1165-13
		93453DC	★1264
		93453DM	★1264
		93453FM	★1264
		93453M	★1264
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93454	Fairchild	93454C	1184-85
		93454M	1184-92
93457	Fairchild	93457C	1183-24
		93457M	1183-32
93458	**Fairchild**	**93458**	★1269
			1160-2
		93458DC	★1269
		93458FM	★1269
		93458PC	★1269
93459	**Fairchild**	**93459**	★1269
			1160-7
		93459DC	★1269
		93459FM	★1269
		93459PC	★1269
93464	Fairchild	93464C	1184-86
		93464M	1184-93
93467	Fairchild	93467C	1183-26
		93467M	1183-37
93470	**Fairchild**	**93470**	★1234
		93470C	★1234
			1180-62
		93470DC	★1234
		93470DM	★1234
		93470FM	★1234
		93470M	★1234
			1180-75
		93470PC	★1234
93471	**Fairchild**	**93471**	★1234
		93471C	★1234
			1180-63
		93471DC	★1234
		93471DM	★1234
		93471FM	★1234

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93481	Fairchild	93481	1169-40
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936	Reticon	RL936	916-150
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9364	GI	RO3-9364B	1186-102
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	Raytheon	RC9366	430-200
		RM9366	430-201
9368	Fairchild	9368C	601-28
9370	Fairchild	9370C	601-118
9374	Fairchild	9374C	601-41
9386	Fairchild	9386C	446-90
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	Teledyne S	9400	916-96
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9401	AMD	9401C	1187-100
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	Fairchild	**9401**	★1893
		9401C	★1893
			★1894
			457-45
			604-2
			1751-164
		9401DC	★1894
		9401FC	★1894
		9401M	★1893
			★1894
			457-47
			604-4
			1751-166
		9401PC	★1894
	GI	AY3-9401	901-66
9403	**Fairchild**	**9403**	★1893
		9403C	★1893
			★1896
			1159-57
			1751-141
		9403DC	★1896
		9403FC	★1896
		9403M	★1893
			★1896
			1159-59
			1751-143
		9403PC	★1896
9404	**Fairchild**	**9404**	★1893
		9404C	★1893
			1751-132
		9404M	★1893
			1751-133
9405	**Fairchild**	**9405A**	★1893
		9405AC	★1893
			427-13
			1751-127
		9405AM	★1893
			427-14
			1751-129
		9405C	★1893
			1751-126
		9405M	★1893
			1751-128
9406	**Fairchild**	**9406**	★1893
		9406C	★1893
			1159-93
			1751-159
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9407	**Fairchild**	**9407**	★1893
		9407C	★1893
			1751-136
		9407M	★1893
			1751-137
9408	**Fairchild**	**9408**	★1893
		9408A	★1893
		9408AC	★1893
			1751-121
		9408AM	★1893
			1751-124
		9408C	★1893
			1751-120
		9408M	★1893
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9409	**Fairchild**	**9409**	★1893
			1754-147
			1724-2
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		9409AM	427-29
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9410	**Fairchild**	**9410**	★1893
		9410C	★1893
			449-42
			1171-103
			1751-173
		9410M	★1893
			449-43
			1751-174
	GI	AY3-9410	901-68
9411	**Fairchild**	**9411**	★1893
		9411C	★1893
			★1894
			457-49
			604-6
			1751-168
		9411DC	★1894
		9411FC	★1894
		9411M	★1893
			★1894
			604-8
			1751-170
9412	Fairchild	9412C	1751-156
		9412M	1751-157
9413	Fairchild	9413	427-30
			1754-150
9414	Fairchild	9414-1	457-108
			1751-151
		9414-2	457-109
			1751-152
		9414-3	457-110
			1751-153
		9414-4	457-111
			1751-154
9415	Fairchild	9415	617-12
			1755-117
9416	Fairchild	9416	617-19
			1755-118
9417	Fairchild	9417	617-26
			1755-119
9419	Fairchild	9419	459-155
			1755-9
9420	Fairchild	9420	1754-185
9421	Fairchild	9421	459-158
			1755-10
9423	**Fairchild**	**9423**	★1893
			1159-87
		9423C	★1893
			★1896
			1751-147
		9423DC	★1896
		9423FC	★1896
		9423M	★1893
			★1896
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		9423PC	★1896
9424	Fairchild	9424	1755-75
9425	Fairchild	9425	615-37
			1755-120
9426	Fairchild	9426	615-45
			1755-121
9427	Fairchild	9427	615-47
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943	NEC America	μPD943	853-187
9440	**Fairchild**	**9440**	★1903
			1726-1

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			1762-89
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947	NEC America	μPD947	853-189
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			1189-88
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95003	Fairchild	F95003	421-7
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9501	GI	RO3-9501	856-11
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95010	Fairchild	F95010	420-154
95016	Fairchild	F95016	420-152
9502	GI	RO3-9502	1186-63
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9503	GI	RO3-9503	856-12
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95106	Fairchild	F95106	420-166
95107	Fairchild	F95107	420-160
95109	Fairchild	F95109	421-1
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	NEC America	μPD952	853-192
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954	BEI	FM954	901-7
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		96LS02M	★ 472
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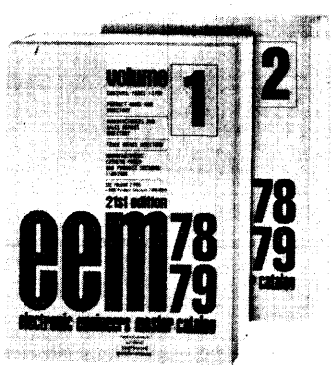
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9709	**National**	**AM9709**	★**1073**
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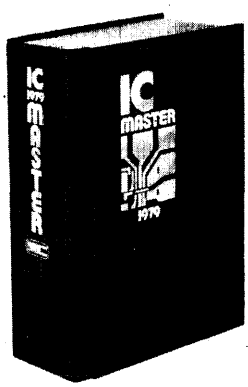
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PART NUMBER GUIDE

Each IC manufacturer has his own special method of identifying products, usually through a system of logos, device number prefixes and suffixes. This Part Number Guide is arranged alphabetically by manufacturer and describes each company's part number system. JAN nomenclature is also covered.

Manufacturer	Part Number: Prefix	Part Number: Suffix	Example
ADVANCED MICRO DEVICES  Note: Alternate source devices follow original manufacturer's part number and marking system.	**Functional Group** 25 MSI 26 Computer Interface 27 Bipolar Memory 28 MOS 29 Bipolar Microprocessor 90 MOS 91 MOS 92 MOS 94 MOS 95 MOS **Type** L Low Power S Schottky LS Low Power Schottky (Blank) Standard	**Package** D Hermetic DIP P Molded F Flat X Dice **Temperature Range** C Commercial M Military	Prefix: AM25 — Functional Group Device: S — Type; 05 — Device Number Suffix: D — Package; M — Temperature Range
AMERICAN MICROSYSTEMS (Current)  (Discontinued)	**Family** S Standard	**Package Type** P Plastic E Cer-DIP S SLAM C Ceramic (Three Layer) T TO Type **Package/Pins** C 22 Pin Plastic or Cer-DIP D 14 Pin Plastic or Ceramic F 12 Pin TO H 16 Pin Cer-DIP, SLAM, or Ceramic I 28 Pin Cer-DIP or SLAM L 24 Pin Cer-DIP or SLAM M 40 Pin SLAM P 18 Pin Plastic or Cer-DIP T 40 Pin Plastic U 16 Pin Plastic W 24 Pin Plastic Z 28 Pin Plastic	Prefix: S — Family Device: 103X-Z — Version Suffix: P — Package Type
ANALOG DEVICES  ICs are marked with an **AD** prefix.	**AD** Analog Devices	**Temperature Range** A,B,C Industrial Range J,K,L Commercial Range S,T,U Military Range **Package** D 8 Pin Ceramic DIP DN Ceramic DIP F Ceramic Flatpack H TO-5 Type Can N Plastic DIP	Prefix: AD Device: 7516 Suffix: JN — Temperature Range; Package
BECKMAN INSTRUMENTS, INC. BECKMAN Beckman® (Discontinued)	**Family (Model Number)** 801-809, 851-859 Voltage Regulators 811-816, 862, 863 Ladder Networks 822, 823, 833, 866 Amplifiers 840 Voltage References 845-872, 877 D/A Converters 873, 876 A/D Converters 882, 883 Active Filters	**Package Type** M Metal C Ceramic G Glass **Version (Function)** I Current V Voltage **Accuracy Level** D1 Best Level D2	Prefix: 877- — Family Device: 85 — Model No.; MV- — Package Type; Version (Function) Suffix: D1 — Accuracy Level
BURR-BROWN BURR-BROWN BB		**Temperature** H, J, K, L 0°C to +70°C R, S, T −55°C to +125°C A, B, C −25°C to +85°C **Package** M Metal P Plastic Q MIL-883 Screening	Prefix: Device: 3532 Suffix: AMQ — Temperature Range; Package; MIL-883 Screening

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Manufacturer	Part Number: Prefix	Part Number: Suffix	Example

CHERRY SEMICONDUCTOR (Micro Components)

(Older ICs may be marked with MCC prefix instead of CS prefix.)

Prefix
- CS Cherry Semiconductor
- D Diode Flip Chip
- N NPN Flip Chip
- P PNP Flip Chip

Package
- 0 Loose Component
- D Dual-In-Line
- P "Pill," Small Round Package
- T TO-Can
- 4 4 Leads
- 8 8 Leads

Circuit Style
- B National Dual Source
- S Signetics Dual Source

Prefix	Device	Suffix
CS	122	0D8
CS	555	B
D	823	

Package/Circuit

DATEL SYSTEMS

Family
- ADC A/D Converters
- AM Amplifiers
- DAC D/A Converters
- DAS Data Acquisition System
- FLT Filters
- MV, MX Multiplexer
- SHM Sample-Hold
- VF Voltage to Freq. Converters

Package — Monolithic
- 1 14 Pin DIP
- 2 TO-99

Seal — Hybrid
- G Epoxy
- M Hermetic

Temperature
- C 0°C to 70°C
- M −55°C to 125°C
- R −25°C to +85°C

Prefix	Device	Suffix
AM	490	2 A

Package

Selection

Prefix	Device	Suffix
DAC	HZ12B	G C

Seal

Temperature

ELECTRONIC ARRAYS

Note: Alternate source devices follow original manufacturer's part number and marking system.

Family
- 10 Static Shift Register
- 12 Dynamic Shift Register
- 15 N Channel ROM
- 20 Keyboard Encoder
- 3X Dynamic ROM
- 4X Static ROM
- Clock Circuit
- EPROM

Package
- D Hermetic DIP
- F Flat Pack
- P Molded DIP
- T TO-Can
- X Dice

Temperature Range
- C 0° to 70°C
- I −55°C to 85°C
- L −55°C to 100°C
- M −55°C to 125°C
- X Other

Prefix	Device	Suffix
EA	1500A	DM

Family

Package

Temperature Range

EMM/SEMI

A. Semi Product

EMM SEMI, INC.

Special Application
- B Reduced Power Supply Level Operation
- L Very Low Power Operation
- M MIL-STD-883, Condition B

Electrical Variation
- U Standard
- A Variation A
- B Variation B, etc.

Temperature Range
- C 0°C to +70°C
- D 0°C to +70°C Plus 168 Hour Supplemental Burn-in
- M −55°C to +125°C Plus 168 Hour Supplemental Burn-in
- S −35°C to +85°C Plus 168 Hour Supplemental Burn-in

Package
- A DIP, Ceramic, 18 Pin
- B DIP, Plastic, 18 Pin
- C DIP, Ceramic, 22 Pin
- D DIP, CERDIP, Ceramic, 22 Pin
- E DIP, CERDIP, Ceramic, 18 Pin
- G Chip Carrier, Ceramic, Leadless, 22 Pin
- P DIP, Plastic, 22 Pin

Prefix	Device	Suffix
M	4200	UCC

Special Application

Electrical Variation

Temperature Range

Package

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Manufacturer	Part Number: Prefix	Part Number: Suffix	Example

EXAR INTEGRATED SYSTEMS



Prefix: XR Exar

Grade
- C Commercial
- M Military (Ceramic package and −55°C to 125°C)
- ( ) The absence of C or M Indicates a Commercial Part with Tighter Specs

Package
- D Dice
- P Plastic
- N Ceramic
- T TO-99, TO-100, TO-101 Metal Can

Prefix	Device	Suffix
XR	567	CP

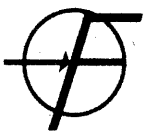
Grade — CP
Package — CP

FAIRCHILD


(Current)



(Current)


(Discontinued)

Note: Alternate source devices follow original manufacturer's part number and marking systems.

Prefix:
- F Fairchild
- SH Hybrid
- μA Linear

Package
- D Ceramic DIP
- E Plastic Can
- F Flat Pac
- H Metal Can
- J Metal Power Package (TO-66)
- K Metal Power Package (TO-3)
- P Plastic DIP
- R Ceramic Mini DIP
- T Mini DIP
- U Power Package (Molded, TO-220)
- W Plastic TO-92

Temperature — Check Device Data for Specific Values
- C 0°C to 70°C/75°C (CMOS −40°C to 85°C)
- L MOS −55°C to 85°C Hybrid −20°C to 85°C
- M −55°C to 125°C

Prefix	Device	Suffix
μA	741	AHM

Electrical Class (if used) — AHM
Package — AHM
Temperature — AHM

FUJITSU



FUJITSU LIMITED

Prefix:
- MB Micro Block
- MBM Micro Block Modified and Industry Standard Numbers

Speed
- N Slowest
- E
- H
- Y Fastest

Package
- C Ceramic
- M Molded (Plastic)

Prefix	Device	Suffix
MB	8227	E M

Speed — E M
Package — E M

GENERAL INSTRUMENT



Prefix — Designation
- CU Array
- AY Array
- DL Shift Register Dynamic ≥ 50 Bits
- DS Shift Register Dynamic < 50 Bits
- LC Linear Circuit
- LG Logic Cells
- MEN N and P Channel FETs
- MU Multiplexer
- RA RAM
- RO ROM
- SL Shift Register Static ≥ 50 Bits
- SS Shift Register Static < 50 Bits

Temperature and Processing
- 0 MTOS −55°C to 85°C
- 1 MTOS 0°C to 70°C
- 4 N Channel
- 5 MTNS 0°C to 70°C
- 6 −55°C to 125°C
- 7 MTNS

Package Identification (Not Marked on Package)
- 01 Dice
- 12 8 Lead DIP
- 14 TO-5 4 Lead
- 15 TO-78 8 Lead
- 16 TO-5 8 Lead
- 17 TO-5 8 Lead High Profile
- 21 TO-5 10 Lead
- 22 TO-5 10 Lead Isolated
- 23 TO-100 10 Lead
- 29 24 Lead Plastic DIP
- 30 14 Lead Plastic DIP
- 31 16 Lead Plastic DIP
- 32 24 Lead Plastic DIP
- 33 40 Lead Plastic DIP
- 35 36 Lead Plastic Flat Pack
- 51 TO-8 12 Lead Low Profile
- 55 16 Lead DIP
- 60 10 Lead Flat Pack
- 61 14 Lead Flat Pack

Prefix	Device	Suffix
RO-6	WXYZ	(XX)

Desig-nation — RO-6
Temp. and Processing — RO-6
Description — WXYZ
Package Identification — (XX)

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GENERAL INSTRUMENT (cont)

Part Number

Prefix

8 Silicon Gate −55°C to 125°C
9 Silicon Gate 0°C to 70°C

Description — Multiplexers
WX Indicates Typical R_{ds}(on)
In Hundred Ohms Steps:
01 ≤ 100 ohms
02 ≤ 200 ohms
03 ≤ 300 ohms, etc.
YZ Total Number of Channels

Custom
Custom Number Assigned

ROM/RAM
WXYZ Total Number of Bits

Shift Registers
W Indicates the Number of Redundant Configurations:
1 Single 3 Triple
2 Dual 4 Quad, etc.
XYZ Total No. of Bits per Configuration

Arrays/Linear/Logic
WXYZ Arbitrary Number Assigned

Suffix

62 16 Lead Flat Pack
63 20 Lead Flat Pack
64 24 Lead Flat Pack
65 40 Lead Flat Pack
66 36 Lead
68 44 Lead Flat Pack
69 14 Lead DIP
71 16 Lead DIP
72 24 Lead DIP .6 MIL Centers
73 24 Lead DIP .5 MIL Centers
74 40 Lead DIP .6 MIL Centers
75 40 Lead DIP 1.05 MIL Centers
76 28 Lead DIP
77 18 Lead DIP
79 24 Lead DIP .6 MIL Centers
80 14 Lead Ceramic RIP
81 16 Lead Ceramic DIP

HARRIS

Family
A Analog
B PC Board
D Digital
I Interface
M Memory
S Programs Division

Package
1 DIP
2 TO-5 Type
3 Plastic DIL
4 Leadless
7 Mini DIP
9 Flat Pack
0 Chip Form

Exceptions
HPROMX-0512

Temperature Range
2..−55°C to 125°C
4 −25°C to 85°C
5 0°C to 75°C
6 25°C Probe
8 Dash 8 Program, MIL-STD-883, Class B — Example: HA-2700-8
9 −40°C to 85°C

Prefix	Device	Suffix
HM1	— 7620	— 5

Family
Package
Temperature Range

HITACHI

Type
HA Analog
HD Digital
HM Memory (RAM)
HN Memory (ROM)

Package
P Plastic

Prefix	Device	Suffix
HM	472114	AP

Description
Model No.
Modification
Package

HUGHES AIRCRAFT

Prefix
H Standard
S Special

Family
CMP Microprocessor
CTR Counter
CUS Custom
DSR Dynamic Shift Register
SSR Static Shift Register
SUB Subsystem
MUL Multiple
DIG Discrete Insulated Gate
DGP Discrete General Purpose
DSW Discrete Switch
PLA Programmable Logic Array

Package
D Cerdip or Ceramic DIP
F Flat Pack
P Plastic DIP
T TO

Prefix	Device	Suffix
H CTR	0320	D

Family
Package

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Part Number

Manufacturer	Prefix	Suffix	Example

HYBRID SYSTEMS

Hybrid Systems

Family
- **DAC3** Digital to Analog Converter
- **ADC5** Analog to Digital Converter
- **R6** Precision Voltage Reference

Processing
- **C** Commercial Industrial Use
- **B** Per MIL-STD883B, Class B

Resolution
- **8** 8-Bits Binary
- **10** 10 Bits Binary
- **11** 11-Bits Binary
- **12** 12-Bits Binary
- **14** 14-Bits Binary
- **16** 16-Bits Binary
- **20** 20-Bits Binary
- **2D** 2-Decade BCD
- **3D** 3-Decade BCD
- **4D** 4-Decade BCD

Prefix	Device	Suffix
DAC3	31	C-14

Processing

Resolution

INTEL

intel®

Package
- **B** CerDIP (Ceramic or Window Lid) (Hermetic)
- **C** Ceramic (Metal Lid) DIP (Hermetic)
- **D** CerDIP (Glass Seal) DIP (Hermetic)
- **P** Plastic DIP
- **M** Metal Can Package (Hermetic)

On military temperature devices /B indicates MIL-STD-883 level B processing; /C, level C processing.

Prefix	Device	Suffix
P	5101	L
C	8080	A
M D	3601	/C

Military Temp.

Package

Suffix

INTERNATIONAL MICROCIRCUITS

- **OM** Omnichip (Analog Bipolar)
- **MM** Master MOS Array (Digital CMOS)
- **SCC** Special Custom Circuit

Package
- **CD** Cerdip
- **P** Plastic DIP
- **SB** Side Brazed

Gate Capacity
- **50** 64 Gates
- **100** 112 Gates
- **150** 160 Gates
- **200** 220 Gates
- **250** 264 Gates
- **300** 312 Gates
- **350** 364 Gates
- **400** 420 Gates
- **450** 480 Gates
- **500** 512 Gates
- **555** 544 Gates

Prefix		Suffix
MM	100	P-28

Family

Gate Capacity

Package

No. of Pins

(Most ICs are custom and are marked only with the purchaser's marks)

INTERSIL

A. General

INTERSIL (Current)

AMI (Discontinued)

Package
- **D** Dual-In-Line Package Ceramic
- **E** Small TO-8 Type
- **F** Flat Package, Ceramic
- **I** 16 Pin DIP (0.6 x 0.7 Lead Space)
- **J** Dual-In-Line Cerdip
- **K** TO-3 Metal Can
- **L** Leadless Ceramic
- **P** Dual-In-Line Package, Plastic
- **Q** 2 Lead Metal Can
- **T** TO-5 Type
- **DR** TO-72 with No. 4 Lead Connected to Case

Family
- **DG** Analog Switch
- **D** Driver
- **G** Multi-Channel FET
- **IH** Hybrid/Analog Gate
- **ICL** Linear
- **ICM** Watch & Clock Circuit
- **IM** Memory

Temperature
- **C** Commercial (0°C to 70°C)
- **I** Industrial (−20°C to 70°C)
- **M** Military (−55°C to 125°C)

Pins (No. of)

A 8	F 22
B 10	G 24
C 12	I 28
D 14	J 32
E 16	K 36
N 18	L 40
V 8, .230" Pin Circle	M 48
W 10, .230" Pin Circle	
Y 8, No. 4 Lead Connected to Case	
Z 10, No. 5 Lead Connected to Case	

Prefix	Device	Suffix
DG	126A M	D D

Analog Gate

Temperature

Package

No. of Pins

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Manufacturer	Part Number Prefix	Part Number Suffix	Example

INTERSIL (cont)

B. Memory Circuits

INTERSIL (Current)

AMI (Discontinued)

Process
- **5** Bipolar
- **6** CMOS
- **7** MOS

General Type
- **1** Processing Element
- **2** Field Programmable Logic Array (FPLA)
- **3** Read Only Memory (ROM)
- **4** Interface Element
- **5** Random Access Memory (RAM)
- **6** Programmable Read Only Memory (PROM)

Speed Select
- Alpha Bipolar
- Numerical MOC and CMOS

Prefix **Suffix**

I M 5 5 08 - ACJ E

- I — Intersil
- M — Memory
- 5 — Circuit
- 5 — Process
- 08 — General Type
- ACJ — Specific Type
- A — Speed Select
- C — Temperature
- J — Package
- E — No. of Pins

JAN NOMENCLATURE

- **J** **JAN** Qualified Device
- **M38510** Military Designation

Device
The "Slash" numbering signifies the specification and specifies the device type. See Military Parts Directory.
Note: The J or JAN prefix is very important. If it is not there it is not a JAN device.

Device Class
- **A** Missiles and Manned Spacecraft
- **B** General Military
- **C** Less Critical Military Applications

Case Outline
- **A** ¼″ x ¼″ Flat Pack, 14-Pin
- **B** ⅛″ x ¼″ Flat Pack, 14-pin
- **C** ¼″ x ¾″ Dual-In-Line, 14-Pin
- **D** ¼″ x ⅜″ Flat Pack, 14-Pin
- **E** ¼″ x ¾″ Dual-In-Line, 16-Pin
- **F** ¼″ x ⅜″ Flat Pack, 16-Pin
- **G** 8-Lead Can
- **H** ¼″ x ¼″ Flat Pack, 10-Lead
- **I** 10-Lead Can
- **J** ½″ x 1¼″ Dual-In-Line, 24-Pin
- **K** ⅜″ x ½″ Flat Pack, 24-Pin
- **L** ⅜″ x ½″ Flat Pack, 24-Pin
- **Z** ¼″ x ⅜″ Flat Pack, 24-Pin

Lead Finish
- **A** Kovar or Alloy 42, with Hot Solder Dip
- **B** Kovar or Alloy 42, with Bright Acid Tin Plate
- **C** Kovar or Alloy 42, with Gold Plate

Prefix **Device** **Suffix**

JM38510 /XXXXX B C B

- B — Device Class
- C — Case Outline
- B — Lead Finish

LAMBDA

- **L** Overvoltage Regulator
- **LAS** Regulator
- **LPD** Dual Power Driver
- **PM** Switching Transistor
- **PMD** Discrete
- **PMR** Dual Rectifier

Prefix **Device** **Suffix**

LAS 14 12

- 12 — Voltage

MASTER LOGIC

(Most ICs are marked with ML prefix as well as purchaser's marks)

Family
- **ML** CMOS Gate Array
- **MLA** CMOS Custom
- **F** Other

Gate Capacity
- **50** 50 Gates
- **75** 75 Gates
- **100** 100 Gates
- **150** 150 Gates
- **200** 200 Gates
- **350** 350 Gates

Package
- **P** Plastic
- **CD** CerDIP
- **SB** Side Brazed

Pins
- By Count

Prefix **Device** **Suffix**

ML 150 P-24

- ML — Family
- 150 — Gate Capacity
- P — Package
- 24 — Pins

Manufacturer	Part Number Prefix	Part Number Suffix	Example

MICRO NETWORKS

MN Micro Networks

Temperature Range
- **(No Suffix)** 0°C to 70°C
- **E** −55°C to 85°C
- **H** −55°C to 125°C
- **B** Processing to MIL-STD-883

Prefix	Device	Suffix
MN	3000	H B

Temperature Range — H
Processing — B

MICRO POWER SYSTEMS

MP Micro Power

Temperature Range
- **J, K, L** Commercial
- **S, T, U** Military

Package
- **D** Ceramic DIP
- **N** Plastic DIP
- **H** TO-100 Type Can

Prefix	Device	Suffix
MP	7520	T D 0025

Level of Performance — T
Package — D
Special Processing — 0025

MITEL SEMICONDUCTOR

Description
- **MA** Linear
- **MH** Hybrid
- **MT** Telecom
- **MS** Special
- **MD** Digital
- **SIL** Silek CMOS

Version
- **A** Modified Version,
- **B** Standard Parameters (3-18V)

Package Style, Temperature Range:
- **C** Ceramic DIP, −40°C to 85°C
- **D** Ceramic DIP, −55°C to 125°C
- **E** Plastic DIP, −40°C to 85°C
- **H** Chip, −40°C to 85°C
- **I** Chip, −55°C to 125°C
- **K** Ceramic Flat Pack, −55°C to 125°C
- **L** Leadless Chip Carrier, as specified
- **W** Wafer, as specified

MIL Process Option
- **B** MIL-883, 5004.1

Prefix	Device	Suffix
MT	8804	BEB

Version — BE
Package/Temperature — B
MIL Process Option — B

MITSUBISHI

M Mitsubishi

Temperature
- **5** Industrial/Commercial
- **9** Military

Series

1 Linear Circuit	**47** TTL
17 Linear Circuit	**5S** TTL-Schottky
3 TTL	**53** TTL
32 TTL	**51** Linear
33 TTL	**81** MOS
43 TTL	**85** MOS
44 TTL	**86** MOS
45 TTL	**9** DTL
46 TTL	

Package
- **E** Plastic-Sealed Metal DIL
- **K** Glass-Sealed Ceramic DIL
- **L** Plastic-Molded SIL
- **P** Plastic-Molded DIL
- **S** Metal-Sealed Ceramic DIL
- **T** Can-Sealed Glass Metal
- **Y** Can-Sealed Glass Metal

Prefix	Device	Suffix
M 5 1	99	A Y

Temp. — 5
Series — 1
Version — A
Package — Y

MONOLITHIC MEMORIES

MMI

(Current)

(Discontinued)

Temperature Range
- **5** Military
- **6** Commercial

Memory Type
- **3** PROM
- **2** ROM

Family
- **S** Schottky
- **LS** Low Power Schottky
- **PS** Power Switched Schottky
- **RA** Registered Asynchronous, Schottky
- **RS** Registered Synchronous, Schottky
- ***LA** Latched

Performance
- **(None)** Standard
- **A** Enhanced (Speed)

Package
- **J** Cerdip
- ***D** Side Brazed
- **N** Plastic
- ***F** Flatpack

Prefix	Device	Suffix
5 3 S	4 8 0	A J

Temperature Range — 5
Memory Type — 3
Family — S
Memory Size — 4
No. of Outputs — 8
Output/Pinout — 0
Performance — A
Package — J

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MONOLITHIC MEMORIES (cont)

MMI

(Current)

(Discontinued)

Part Number

Prefix

Memory Size
- **0** 256 Bit
- **1** 1024 Bit
- **2** 2048 Bit
- **4** 4096 Bit
- **8** 8192 Bit
- **16** 16384 Bit
- ***65** 65536 Bit

Number of Outputs
- **4** 4
- **8** 8
- ***9** 9
- ***0** 10

Output/Pinout
- **0** Open Collector
- **1** Tri-State
- **2** Open Collector
- **3** Tri-State

Suffix

Example

MOSTEK

MOSTEK

MK Mostek

Package
- **E** Leadless Chip Carrier
- **F** Flat Ceramic Package
- **K** Tin Plated Frit-Sealed Ceramic
- **N** Plastic Dual-In-Line
- **P** Ceramic Dual-In-Line
- **T** Ceramic Dual-In-Line with Transparent Lid

Prefix	Device	Suffix
MK	4096	P

Package

MOTOROLA

(ICs may not have the circle on the marking)

Some second source ICs follow the original marking system.

Description
- **MC** Packaged Integrated Circuits
- **MCB** Packaged Beam-Lead Integrated Circuits. (Followed by F Suffix When in Flat Pack)
- **MCBC** Beam-Lead Integrated Circuit Chips Unencapsulated Integrated Circuit Chips
- **MCC** Unencapsulated Integrated Circuit Chips
- **MCCF** Flip-Chip Linear Integrated Circuits
- **MCE** Dielectrically Isolated Integrated Circuits
- **MCM** Integrated Circuit Memories
- **LM** Pin-for-Pin Equivalent to Linear Integrated Circuits Made by National Semiconductor
- **MMS** Memory Systems

Package
- **F** Flat Ceramic Package
- **G** Metal Can Package (TO-5 Types)
- **K** Metal Power Package (TO-3 Types)
- **L** Ceramic Dual-In-Line Case
- **P** Plastic Package
- **PQ** ICs Packaged In Staggered-Lead Plastic DIP Packages
- **R** Metal Power Packages (TO-66 Types)
- **U** Ceramic Package

Prefix	Device	Suffix
MC	14510	L

Description

Package

NATIONAL

DEVICE NUMBER (for Digital Devices):
CDXXXX-CMOS —
C Suffix −40°C to 85°C,
M Suffix −55°C to 125°C.

DM54XX — All numbers beginning with 5 denote −55°C to 125°C temperature operation.

DM74XX — If the "74" is indicated, the operating temperature is 0°C to 70°C.

DM7XXX — All other numbers beginning with 7 (besides the "74" shown above) are NSC proprietary products and a 7 here indicates −55°C to 125°C.

Description
- **AD** Analog to Digital
- **AH** Analog Hybrid
- **AM** Analog Monolithic
- **CD** CMOS
- **DA** Digital to Analog
- **DH** Digital Hybrid
- **DM** Digital Monolithic
- **DS** Digital Special
- **LFT** Linear FET Monolithic
- **LH** Linear Hybrid
- **LM** Linear Monolithic
- **LX** Transducer
- **MA** Module
- **MH** MOS Hybrid
- **MM** MOS Monolithic

Form
- **C** Complete
- **B** Building Block
- **D** Digital Panel Meter Chip
- **M** Module
- **S** Card Systems

Characteristics
- **A** Improved Electrical Specs
- **C** Reduced Temperature Range

Package
- **D** Glass/Metal DIP
- **F** Flat Pack (0.25" Wide)
- **G** TO-8 (12 Lead) Metal Can
- **H** TO-5 (Multi-Lead) Metal Can
- **J** Glass/Glass
- **K** TO-13 Power Pack
- **M** Wide Trak Power Pack
- **N** Molded DIP
- **P** TO-202 Plastic Power Pack
- **R** Low Temperature Ceramic Pack
- **S** 14 Lead Power Pack SGS Power Pack
- **T** TO-220 Plastic Power Pack
- **W** Flat Pack (0.275" Wide)
- **Z** TO-92

Prefix	Device	Suffix
AD C	08 00	P C N

Converter Products:

Form

Resolution

More Than One in Family

Technology

Temperature Range

Package

Manufacturer	Part Number Prefix	Part Number Suffix	Example

NATIONAL (cont)

DM8XXX — All numbers beginning with 8 denote 0°C to 70°C temperature operation.

(Current)

(Discontinued)

Resolution
- **08** 8 Bits
- **10** 10 Bits
- **12** 12 Bits
- **25** 2½ Digit
- **35** 3½ Digit
- **37** 3¾ Digit
- **45** 4½ Digit

Technology
- **P** PMOS
- **C** CMOS
- **H** Hybrid
- **B** Bipolar
- **N** NMOS
- **L** Linear
- **I** I^2L

Linear Devices
With proprietary linear circuits, a 1-2-3 numbering system is employed.
The 1 denotes a Military temperature range device (−55°C to 125°C), the 2 denotes an Industrial device (−25°C to 85°C), and the 3 denotes a Commercial device (0°C to 70°C). i.e. LM101/LM201/LM301. Exception to this are the LM1800 Series; some hybrid circuits which employ a "C" Suffix; and second-source products which follow the original manufacturers numbering system.

Example	Prefix	Device	Suffix
	LM	101	A F

Characteristics — Package

NEC

μP Micropackage Family
- **A** Discrete
- **B** Digital Bipolar
- **C** Linear
- **D** Digital CMOS

Package
- **C** Plastic
- **D** Ceramic or CerDIP

Prefix		Suffix
μP B	xxxx	C S

Family — Package — Modification

NITRON

Description
- **NC** Standard
- **SC** Custom

Family
- **3xx** Siliconix Second Source, Telecom
- **11xx** Music Circuits
- **22xx** Motorola Second Source, TNRX
- **36xx** CMOS ROMs
- **64xxx** Proprietary Frequency Synthesizers
- **65xxx** Motorola Second Source, ROMs
- **70xxx** Proprietary MNOS Memories
- **71xxx** Proprietary MNOS Counters

Temperature Range
- **C** Commercial, 0°C to 70°C
- **E** Extended, −20°C to 85°C
- **T** Telecom/Auto, −40°C to 85°C
- **M** Military, −55°C to 125°C

Package
- **D** Cer-DIP (Glass/Glass) Hermetic
- **F** Flat Pack
- **L** Ceramic (Glass/Metal) Hermetic
- **P** Plastic
- **T** TO-5 Type Metal Can
- **W** Wafers, Probed and Inked
- **X** Die in Waffle Carriers

Prefix	Device	Suffix
NC	6405B	PC-0246

Standard — Family — Package — Temperature Range — Custom Code (for Custom Devices)

NORTEC

NE Nortec Electronics
NE 6003BZD
NE 1103-146D

Electrical Selections
- **11**
- **BZ** Electrical Selections
- **146**
- **etc.**

Package
- **D** Ceramic DIP
- **F** Flatpack
- **H** Metal Can
- **J** CerDIP
- **N** Molded DIP
- **P** 8-Pin DIP
- **Y** Dice

Prefix	Device	Suffix
NE	6003	11 D

Electrical Selections — Package

OPTICAL ELECTRONICS

Description
- **2000** Log/Anti-Log
- **3000** V/F - F/V
- **5000** Non-Linear Functions
- **7000** A/D, D/A, μC
- **9000** Op Amps, Comparators, etc.

PANASONIC (MATSUSHITA)

MATSUSHITA

Description
- **AN** Analog
- **DN** Digital Bipolar
- **M,J** Development Type
- **MN** MOS

Prefix	Device
DN	830

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Manufacturer	Part Number: Prefix	Part Number: Suffix	Example

PLESSEY

(All ICs are marked **PLESSEY**)

Description

- **ML** MOS Linear (w/Gate Protection)
- **MP** MOS Digital
- **MT** MOS Linear (without Gate Protection)
- **NOM** MNOS Memory Elements and Arrays
- **SAA, SBA** Alternate Sourced Consumer Devices
- **SL** Bipolar Linear
- **SP** Bipolar Digital

Package

- **CM** Multilead TO-5
- **DC** Dilmon
- **DG** Ceramic Dual-In-Line
- **DP** Plastic Dual-In-Line
- **EP** Power Stud
- **FM** Ten Lead Flatpack
- **GM** Fourteen Lead Flatpack
- **KM** TO-3
- **QG** Ceramic Quad-In-Line
- **QP** Plastic Quad-In-Line
- **RP** Power Findip
- **SP** Plastic Single-In-Line

Prefix	Device	Suffix
SP	8735B	DG

Description

Package

PRECISION MONOLITHICS

Description

- **BUF** Voltage Follower (Buffer)
- **CMP** Voltage Comparator
- **DAC** Digital to Analog Converter
- **MAT** Matched Transistors
- **MUX** MUX Analog Multiplexer
- **OP** Operational Amplifier
- **PM** Second Source Devices
- **REF** Voltage Reference
- **SMP** Sample and Hold
- **SSS** Second Source Devices

Package (Last Alphabetical Character)

- **H** 6-Pin TO-78
- **J** 8-Pin TO-99
- **K** 10-Pin TO-100
- **L** 10-Pin Flatpack
- **M** 14-Pin Flatpack
- **N** 24-Pin Flatpack
- **P** 8-Pin Plastic Mini DIP
- **Q** 16-Pin Hermetic DIP
- **V** 24-Pin Hermetic DIP
- **X** 18-Pin Hermetic DIP
- **Y** 14-Pin Hermetic DIP

Prefix	Device	Suffix
DAC	01	C Y

Grade

Package

PRO ELECTRON

First Two Letters

Digital

- **FA - FZ**
- **GA - GZ** Identify the Family
- **etc.**

Solitary Circuits

- **S** Solitary Circuit
- **T** Analog Circuit
- **U** Mixed Analog/Digital

(The second letter has no special significance, except H means Hybrid.)

Third Letter

Temperature Range

- **A** Temp. Range not specified below
- **B** 0°C to +70°C
- **C** −55°C to +125°C
- **D** −25°C to +70°C
- **E** −25°C to +85°C
- **F** −40°C to +85°C
- **G** −55°C to +85°C

If a circuit is designed for a wider temperature range, the letter indicating a narrower temperature range or the letter "A" can be used.

Device or Serial Number

Either a 4-digit number assigned by PRO ELECTRON or the serial number (even a combination of figures and letters) of an existing type designation which can be extended to a minimum of a 4-digit number by adding zeros in front of it.

Suffix or Version Letter (Recommended)

Single Letter

- **C** Cylindrical
- **P** Plastic DIL
- **D** Ceramic DIL
- **Q** Quad-In-Line
- **F** Flat Pack
- **U** (Uncased) Chip

Other letters have no fixed meaning except Z means customized wiring.

Prefix	Device	Suffix
GFB	7400	-DP
GMB	74LS00A	-DC
SAC	2000	
TDA	1000	P

Two Letters

First Letter: General Shape

- **C** Cylindrical
- **D** Dual-In-Line (DIL)
- **E** Power DIL (with External Heat Sink)
- **F** Flat (Leads on 2 Sides)
- **G** Flat (Leads on 4 Sides)
- **K** Diamond (TO-3 Family)
- **M** Multiple-In-Line (Except Dual-, Triple-, Quad-In-Line)
- **Q** Quad-In-Line (QUIL)
- **R** Power QUIL (with External Heat Sink)
- **S** Single-In-Line (as TO-127 or TO-220)
- **T** Triple-In-Line

Second Letter: Material

- **C** Metal-Ceramic
- **G** Glass-Ceramic (cerDIP)
- **M** Metal
- **P** Plastic

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Manufacturer	Part Number: Prefix	Part Number: Suffix	Example

RAYTHEON SEMICONDUCTOR

Temperature
- **LH1, LM1** −55°C to 125°C
- **LH2, LM2** −25°C to 85°C
- **LH3, LM3** 0°C to 70°C
- **RC** 0°C to 70°C
- **RM** −55°C to 125°C
- **RV** −40°C to 85°C
- **54** −55°C to 125°C
- **74** 0°C to 70°C
- **MAX-xxxx-2** −55°C to 125°C
- **MAX-xxxx-5** 0°C to 70°C

HA Series
- **HA1** 14-Pin Ceramic DIP
- **HA3** 14-Pin Plastic DIP

Microcomputer Components
- **AM**
- **R**
- **93**

Package

Most Devices
- **BM** 16-Pin Epoxy-B DIP
- **CH** Gold-Backed Chip, Visually Inspected to MIL-STD-883A, Method 2012, and Packaged in Waffle Pack.
- **CJ** 14-Pin Ceramic Flatpak
- **CL** 16-Pin Ceramic Flatpak
- **CK** 14-Pin Ceramic Flatpak
- **D** 14-Pin Metal DIP
- **DB** 14-Pin Epoxy-B DIP
- **DC** 14-Pin Ceramic DIP
- **DD** 16-Pin Ceramic DIP
- **DE** 8-Pin Ceramic DIP
- **DM** 16-Pin Ceramic DIP
- **DZ** 40-Pin Ceramic DIP
- **F** Flatpak
- **FV** 28-Pin Ceramic Flatpak
- **FZ** 42-Pin Ceramic Flatpak
- **H** 3, 8 or 10-Pin Metal Can
- **J** 14 or 16-Pin Ceramic DIP
- **K** TO-3 Power Pack
- **MB** 16-Pin Epoxy-B DIP
- **ML** 16-Pin Ceramic DIP, Side Brazed
- **MS** 20-Pin Ceramic DIP, Side Brazed
- **MZ** 40-Pin Ceramic DIP, Side Brazed
- **N** 24-Pin Glass/Metal Flatpak
- **N** Epoxy-B DIP (LM Series)
- **NB** 8-Pin Epoxy-B DIP
- **PS** 20-Pin Epoxy-B DIP
- **PU** 24-Pin Epoxy-B DIP
- **PV** 28-Pin Epoxy-B DIP
- **PZ** 40-Pin Epoxy-B DIP
- **Q** 10-Pin Flatpak (¼″ x ¼″)
- **R** 24-Pin Ceramic DIP
- **T** 3, 8, 10 or 12-Pin Metal Can
- **TK** 9-Pin TO-66 Power Pack
- **W** 14-Pin Ceramic Flatpak

Beam Lead Chip
- **BL**

HA Series
- **2** −55°C to +125°C
- **5** 0°C to +70°C
- **8** −55°C to +125°C

XR Series
- **M** Ceramic −55°C to +125°C
- **N** Ceramic −40°C to +85°C
- **P** Epoxy −40°C to +85°C
- **CN** Ceramic 0°C to +75°C
- **CP** Epoxy 0°C to +75°C

Microcomputer Components Package
- **D** Hermetic DIP
- **F** Flatpak
- **P** Plastic DIP
- **X** Chip

Temperature
- **C** 0°C to +75°C
- **M** −55°C to +125°C

Process to MIL-M-883B
- **B**

Prefix	Device	Suffix
54	153	DD
RC	4130	DB
LM	118	H
HA1	4741	5
XR	2207	CN

Prefix	Device	Suffix
AM	2901	D M B

Package
Temperature Range
Processing

Raytheon ICs are identified by an **RAY** prefix to the date code.

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Manufacturer	Part Number: Prefix	Part Number: Suffix	Example

RCA

RCA Solid State

Description
- **CA** Linear ICs
- **CD** Digital ICs
- **CDP** Microprocessor ICs
- **MW** MOS ICs

Version
- **A** Modified Version, Unilaterally Interchangeable with Prototype
- **B** Modified Version, Unilaterally Interchangeable with A Version, and with Prototype
- **C** Modified Version, Unilaterally Interchangeable with B, A, and Prototype Versions

Package
- **D** Ceramic DIP
- **E** Plastic DIP
- **F** Ceramic DIP, Frit Seal
- **G** Hermetic Chip in Plastic Package
- **H** Chip
- **K** Ceramic Flat Package
- **L** Beam-Lead Device
- **Q** Quad-In-Line Plastic Package
- **S** TO-5 Package with DIL-CAN
- **T** TO-5 Package

Prefix	Device	Suffix
CD	4070	BD

Version — BD

Package — BD

RETICON

RETICON®

Previous Products
- **RA** Area Array
- **RL** Linear Array
- **SAD** Serial Analog Delay
- **SAM** Serial Analog Memory
- **SAP** Serial Analog Processor
- **TAD** Tapped Analog Delay

New Analog Products
- **R5** Reticon Analog

Family
- **0** Complex Special Functions
- **1** Simple Delays
- **2** Tapped Delay
- **3** Analog Memory
- **4** Correlator
- **5** Multiplexer, Parallel to Serial Converter
- **6** Filters

Code (for Corresponding Products)
- No. of Columns and Lines
- No. of Elements
- No. of Storage Elements
- No. of Storage Elements
- No. of Storage Elements
- No. of Taps

Prefix	Device	Suffix
RA	50x50	A
RL	1024	C
TAD	12	

Code — 12

Revision — C

Prefix	Device	Suffix
R5 X	YY	A -1

Family — X

Revision (If Required) — A

Member of Device Type (If Required) — -1

ROCKWELL (COLLINS)

Rockwell

- **CRC** Products
- **RBM** Bubble Memory
- **R** Rockwell

CRC Devices

Package
- **1** Ceramic DIP
- **2** Flatpack
- **3** Plastic DIP

Temperature
- **1** −55°C to 125°C
- **2** −25°C to 85°C
- **3** 0°C to 70°C

Prefix	Device	Suffix
CRC	1504	-1 -2

Package — -1

Temperature Range — -2

SANYO

Designation
- **LA** Bipolar Linear
- **LB** Bipolar
- **LC** CMOS
- **LM** PMOS

Prefix	Device
LA	1230

SGS-ATES SEMICONDUCTOR

(Current)

SGS ATES

(Discontinued)

(Prefixes assigned by the European Association "PRO ELECTRON")
- **H** High Level Logic
- **HB** CMOS
- **L** Linear Professional
- **M** MOS
- **TAA** Linear Consumer
- **TBA** Linear Consumer
- **TCA** Linear Consumer
- **TDA** Linear Consumer

Prefix	Device
TDA	1200

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SIGNETICS

Part Number

Prefix

Temperature
- **N or NE or None** 0°C to 70°C
- **N8** 0°C to 75°C
- **S(E)** −55°C to 125°C
- **SA** −40°C to 85°C
- **5400 Series** −55°C to 125°C
- **7400 Series** 0°C to 70°C

Linear ICs (Second Source)
- **55** −55°C to 125°C
- **75** 0°C to 70°C
- **78**
- **78L**
- **78M**
- **79**
- **79M**
- **DS**
- **MC**
- **TL**
- **UDN**
- **ULN**
- **μA**

Suffix

Package
- **N** 8, 14, 16, 18, 20, 22, 24, 28, 24 Slim Line, 40 Lead DIL Plastic
- **F** 8, 14, 16, 18, 20, 22, 24, 28, 40 Lead Ceramic DIP
- **I** 8, 14, 16, 18, 22, 24, 28, 40, 50 Lead Ceramic DIP Side Brazed
- **W** 10, 14, 16, 24 Lead Ceramic Flat Pack
- **Q** 10, 14, 16, 24 Lead Ceramic Flat, Bottom Brazed
- **K** 10 Lead TO-100 Header, Low Profile
- **L** 10 Lead TO-100 Header Tall Can
- **T** 8 Lead TO-99 Header
- **DA** TO-3 Solid Header, Can
- **DB** TO-5 Solid Header, Can
- **R** 16, 18, 24, 28, 40 Lead Beryllia Flat Pack
- **S** TO-92 Plastic
- **U** 3, 4, 5, 7, 9 Lead SIL Plastic

K, T, L, and **DB** Suffixes to be converted to **H**
DA Suffix to be converted to **K**

Example

Prefix	Device	Suffix
	74123	N
N	8X02	N

Temperature
Package

SILICON GENERAL

SG Silicon General

Characteristics
- **A** Improved Electrical Specifications
- **C** Reduced Temperature Range

Package
- **F** Flat Pack
- **J** 14, 16-Pin DIP (CerDIP)
- **K** TO-3 Power Pack
- **M** 8-Pin Plastic DIP
- **N** 14, 16-Pin Plastic DIP
- **T** TO-5 Metal Can (TO-39/99/100/101)
- **Y** 8-Pin DIP (CerDIP)

Example

Prefix	Device	Suffix
SG	1524	J
SG	108A	T

Characteristics
Package

SILICONIX

Description
- **D** Driver for FET Switch
- **DF** Digital LSI
- **DGM** Driver with FET Switches (Monolithic Version of Hybrid Device)
- **G** Multi-Channel FET Switches
- **H** High Voltage (28V) Logic
- **L** Linear IC
- **LD** A/D Converter
- **LH** Hybrid Linear IC (2nd Source)
- **LM** Linear IC (2nd Source)
- **Si** 2nd Source Part
- **S** Power Logic Switch.

Temperature
- **A** −55°C to 125°C
- **B** −20°C to 85°C
- **C** 0°C to 70°C

Package
- **A** Metal Can
- **F** Flatpack
- **J** Plastic DIP
- **K** Ceramic DIP
- **L** Flatpack
- **P** Hermetic DIP
- **R** Hermetic DIP

MIL Process Option

MIL-883, Class A
- **2** MIL-883, Class B
- **3** MIL-883, Class C
- **4** In-House Screening Plus 168 Hr. Burn-In

Example

Prefix	Device	Suffix
DG	200	BA-X

Temperature
Package
MIL Process Option

SOLID STATE SCIENTIFIC

Reliability
- **A** MIL-883-A
- **B** MIL-883-B
- **C** MIL-883-C
- **S** Standard

Other Letters
- **C** Complementary
- **L** Logic
- **M** Memory
- **P** Microprocessor
- **S** System/Software

Process
- **A** AL Gate Bulk
- **B** High Voltage AL Gate
- **L** 4-6 V Range
- **S** Silicon on Sapphire

Package
- **C** Cerdip DIP
- **D** Ceramic DIP
- **E** Epoxy DIP
- **H** Chip
- **F** Flat Pack
- **T** TO-5

Example

Prefix	Device	Suffix
SCL	4000	AE+

Reliability
Process
Package
Special Screening

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Manufacturer	Part Number Prefix	Part Number Suffix	Example
SOLITRON S (Current) S (Discontinued)	**CM** CMOS	**Package Style, Temperature Range** **AD** Ceramic DIP, −55°C to 125°C **AE** Epoxy Encapsulated DIP, −40°C to 85°C **AF** CerDIP, −55°C to 125°C	Prefix **CM** Device **4000** Suffix **AD** Package/Temperature
SPRAGUE ELECTRIC **A. UC Series** **UD Series** **UG Series** **UL Series** SPRAGUE ②	**Family** **C** CMOS **D** Display Drivers **G** Hall Effect Circuits **L** Linear Circuits **Temperature** **N** Limited Temperature Range, −25°C to 70°C Typical **S** Extended Temperature Range	**Package** **A** Plastic DIP **B** Plastic DIP with Heat Sink Tabs **C** Chip **D** TO-99 **E** 8-Pin Plastic DIP with Pins 1, 4, 5, 8 Only **F** TO-86 or 30 Lead Flat Package **G** TO-99 **H** 9-Pin Hermetic DIP **J** TO-87 **K** TO-100 **L** TO-100 **M** 8-Pin Plastic DIP **N** 14-Pin Plastic Quad-In-Line **P** Batwing DIP **Q** Batwing Quad-In-Line **R** 8-Lead DIP with Unformed Leads **S** 4-Pin SIP **T** 3-Pin SIP **W** TO-100 with Miniature Tube Base Adapter Base	Prefix **ULN** Device **2111** Suffix **A** Family Temperature Package
B. UH Series		**Package** **C** Hermetic Flatpack **D** Hermetic DIP **P** Plastic DIP	Prefix **UHP** Device **400** Package
STANDARD MICROSYSTEMS	**Family** **CG** Character Generator **COM** Communications **CRT** CRT Display **KR** Keyboard Encoding	**Package** **P** Plastic **C** Ceramic **Temperature** **T** −25°C to 85°C **(Blank)** 0°C to 70°C An H in the Suffix Indicates High Speed A U in the Suffix Indicates Ultra High Speed	Prefix **COM** Device **2502** Suffix **P** Family Package Temperature Range
SYNERTEK	**Temperature Range** **None** 0°C to 70°C **M** −55°C to 125°C **X** Special **Package** **C** Ceramic **P** Molded **D** Cerdip **X** Dice **F** Flat Pac **T** TO Can		Prefix **SY M C** Device **2114** Suffix **L3** Temperature Range Package Device Code Performance or Processing Designator
TELEDYNE PHILBRICK TELEDYNE PHILBRICK	**Description** **1000 Series** Operational Amplifier, Module **1300 Series** Operational Amplifier, IC **1400 Series** Operational Amplifier, FET IC **1700 Series** Operational Amplifier Chopper Stabilized **2200 Series** Power Supply, AC Input, PC Mount **2300 Series** Power Supply, DC Input, PC Mount **2400 Series** Power Supply, AC Input, Chassis Mount **4000 Series** Digital to Analog Converters **4100 Series** Analog to Digital Converters **4300 Series** Non-Linear Function Modules **4400 Series** Non-Linear Function Modules **4500 Series** Multiplexers **4700 Series** Voltage to Frequency and Frequency to Voltage Converters **4800 Series** Sample-Hold Amplifiers		

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Manufacturer	Part Number Prefix	Part Number Suffix	Example

TELEDYNE SEMICONDUCTOR

For alternate source devices, the original manufacturer's part number and marking system is used.

Temperature/Electrical
- **A** −55°C to 125°C, Selected Electrical Performance (HiNIL −30°C to 70°C) 15V Supply
- **B** −55°C to 125°C, Premium Electrical Performance
- **C** 0°C to 70°C, Industrial Electrical Performance (HiNIL −30°C to 85°C); 12V Supply
- **M** −55°C to 125°C

Package
- **H** Flat Pack
- **J** Plastic DIP
- **L** CerDIP
- **N** Ceramic DIP
- **Y** Dice

Device	Suffix
8700	CJ

Temperature/Electrical — CJ
Package — CJ

TELEFUNKEN

Note: ICs are marked **TFK**

(Prefixes Assigned by the European Association "PRO ELECTRON")

Proprietary Devices
- **U** Integrated Circuits

Suffix
- **B** Bipolar
- **M** MOS

Prefix	Device	Suffix
U	113	B

TEXAS INSTRUMENTS

- **RSN** Radiation Hardened Circuit
- **SBP** Bipolar Processor
- **SMC** MOS High Reliability
- **SN** Standard Prefix
- **SNM** High Reliability, Level I
- **SNA** High Reliability, Level II
- **SNC** High Reliability, Level III
- **SNH** High Reliability, Level IV
- **TL** Linear
- **TMS** MOS

Temperature (Most Devices)
- **52 Series** −55°C to 125°C
- **54 Series** −55°C to 125°C
- **55 Series** −55°C to 125°C
- **62 Series** −25°C to 85°C
- **72 Series** 0°C to 70°C
- **74 Series** 0°C to 70°C
- **75 Series** 0°C to 70°C
- **TF Series** −40°C to 85°C
- **TP Series** −55°C to 125°C
- **TMS C Series** −25°C to 85°C
- **TMS L Series** 0°C to 70°C
- **TMS M Series** −55°C to 125°C
- **TMS R Series** −55°C to 85°C

Package
- **FA** Flat Package
- **J** Ceramic Flat Package
- **JA** DIP
- **JB** DIP
- **JP** DIP
- **L** Metal Can
- **LA** Metal Can
- **N** Plastic DIP
- **ND** Plastic DIP with Tab
- **NE** Plastic DIP with Tabs
- **P** Plastic DIP
- **RA** Flat Package
- **SB** Flat Package
- **T** Metal Flat Package
- **W** Ceramic Flat Package

Speed (MOS Only)
- −15 150ns Max. Access
- −20 200ns Max. Access
- −25 250ns Max. Access

Prefix	Device	Suffix
SN 74	S188	J

Description — SN 74
Temperature Range — SN 74
Package — J

Prefix	Device	Suffix
TMS	4027	-15 JL

Speed — -15
Package — JL
Temperature Range — JL

TOSHIBA

Description
- **TA** Bipolar Linear
- **TC** CMOS
- **TD** Bipolar Digital
- **TM** MOS

Package
- **P** Plastic
- **M** Metal
- **A** Improved Type
- **C** Ceramic

Prefix	Device	Suffix
TA	7173	AP

WESTERN DIGITAL

Package
- **A** 40 Lead DIP, Ceramic
- **B** 40 Lead DIP, Plastic
- **C** 24 Lead DIP, Ceramic
- **D** 24 Lead DIP, Plastic
- **E** 28 Lead DIP, Ceramic
- **F** 28 Lead DIP, Plastic
- **G** 22 Lead DIP, Ceramic
- **H** 22 Lead DIP, Ceramic

Prefix	Device	Suffix
TR1602	A	01

Package — A
Special Parameter — 01

ZILOG

Family
- **Z80**
- **Z**

Speed
- **A** 4.0 MHz
- **blank** 2.5 MHz

Device
- **CPU** Central Processor Unit
- **PIO** Parallel Input/Output Unit
- **CTC** Counter Timer
- **SIO** Serial Input/Output
- **DMA** Direct Memory Access

Package
- **C** Ceramic
- **P** Plastic

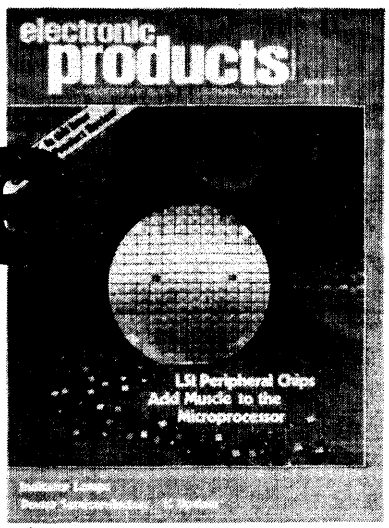
Screening
- **S** Standard
- **M** Military

Prefix	Device	Suffix
Z80 A	CPU	CM

Family — Z80
Speed — A
Package — CM
Screening — CM

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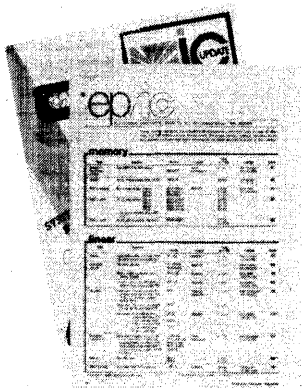
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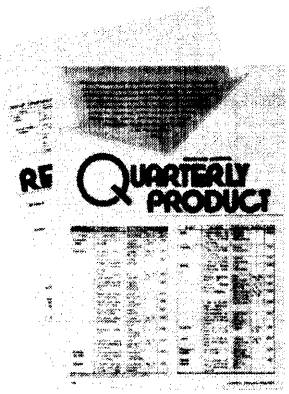
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ABBREVIATIONS OF COMPANY NAMES

AD	Analog Devices
AMD	Advanced Micro Devices
AMI	American Microsystems, Inc.
Amperex	Amperex Electronics Corp.
Analogic	Analogic Corp.
Beckman	Beckman Instruments, Helipot Division
BEI	BEI Electronics
Burr-Brown	Burr-Brown Research
Cermetek	Cermetek
Cherry	Cherry Semiconductor
CMA	Consumer Microcircuits of America
Cybernetic	Cybernetic Micro Systems
Data General	Data General
Datel	Datel Systems
DDC	Data Devices Corp.
Delco	Delco Electronics
Dionics	Dionics Inc.
EA	Electronic Arrays
EMM/Semi	EMM Semi, Div. of Electronic Memories & Magnetics
Essex	Essex International
Exar	Exar Integrated Systems
Fairchild	Fairchild
Ferranti	Ferranti Electric
Fujitsu	Fujitsu
GI	General Instrument
Harris	Harris Semiconductor
Hitachi	Hitachi America Ltd.
Holt	Holt Inc.
Hughes	Hughes Aircraft Solid State Products
Hybrid Sys	Hybrid Systems
HyComp	HyComp
IMI	International Microcircuits, Inc.
Intech/FMI	Intech/Function Modules Inc.
Intel	Intel
Interdesign	Interdesign
Intersil	Intersil
IPI	Integrated Photomatrix, Inc.
Lambda	Lambda Electronics
LSI	LSI Computer Systems
Maruman	Maruman Integrated Circuits
Master Logic	Master Logic
Matrox	Matrox Electronics Systems
Micro Net	Micro Networks
Micropac	Micropac Industries
Micro Power	Micro Power Systems
Micro Tech	Microcircuits Technology
Mitel	Mitel Semiconductor
Mitsubishi	Mitsubishi Electric Co.
MMI	Monolithic Memories, Inc.
Monosil	Monosil
MOS	MOS Technology
Mostek	Mostek
Motorola	Motorola Semiconductor
National	National Semiconductor
NCR	NCR Corp., Microelectronics Division
NEC America	NEC America
NEC Micro	NEC Microcomputers
Nitron	Nitron
Nortec	Nortec Electronics
Novonics	Novonics
NPC	Nucleonic Products Co.
OEI	Optical Electronics, Inc.
OKI	OKI Semiconductor
Panasonic	Panasonic, Matsushita Electric Corp.
Photo Therm	Photo Therm
Plessey	Plessey Semiconductors
PMI	Precision Monolithics, Inc.
Raytheon	Raytheon Semiconductor
RCA	RCA Solid State Division
Reticon	Reticon
RIFA	RIFA
Rockwell	Rockwell Microelectronic Devices
RTC	Real Time Corp.
Sanken	Sanken Electric
Sanyo	Sanyo Electric
SGS	SGS-Ates Semiconductor
Siemens	Siemens
Signetics	Signetics (Philips)
Silicon G	Silicon General
Siliconix	Siliconix
Silicon Sys.	Silicon Systems, Inc.
Silitronics	Silitronics
SMC	Standard Microsystems
Solitron	Solitron Devices
Sprague	Sprague Electric Company
Supertex	Supertex, Inc.
SSM	Solid State Microtechnology for Music
SSS	Solid State Scientific
Synertek	Synertek
Telaris	Telaris
Teledyne C	Teledyne Crystalonics
Teledyne P	Teledyne Philbrick
Teledyne S	Teledyne Semiconductor
Telefunken	AEG-Telefunken
TI	Texas Instruments
TMX	TMX
Toshiba	Toshiba
Trans-Data	Trans-Data
TRW	TRW
Unitrode	Unitrode
Western	Western Digital
Zilog	Zilog

GUIDE TO IC LOGOS

The following logos and symbols are provided to help you identify the manufacturers of IC products. Sometimes different marks are used on a company's products, depending upon individual package sizes.

LOGO	MANUFACTURER
AM	ADVANCED MICRO DEVICES
AMI Ai*	AMERICAN MICROSYSTEMS
ANALOG DEVICES	ANALOG DEVICES
ANALOGIC	ANALOGIC
BECKMAN Beckman*	BECKMAN INSTRUMENTS
BURR-BROWN BB	BURR-BROWN
CS MCC	CHERRY SEMICONDUCTOR (Micro Components)
	CONSUMER MICROCIRCUITS
CY	CYBERNETIC MICRO DEVICES*
DDC	DATA DEVICE CORPORATION
	DATA GENERAL
	DATEL SYSTEMS
	ELECTRONIC ARRAYS
EMM SEMI, INC. SEMI*	EMM/SEMI

LOGO	MANUFACTURER
	EXAR INTEGRATED SYSTEMS
F FAIRCHILD F*	FAIRCHILD
FERRANTI	FERRANTI
FUJITSU LIMITED	FUJITSU
	GENERAL INSTRUMENT
	HARRIS
	HITACHI
HUGHES	HUGHES AIRCRAFT
Hybrid Systems	HYBRID SYSTEMS
fmi	INTECH/FMI
	INTEGRATED PHOTOMATRIX
intel	INTEL
interdesign	INTERDESIGN

LOGO	MANUFACTURER
INTERSIL IMS*	INTERSIL
LSI	LSI COMPUTER SYSTEMS
	LAMBDA
ML	MASTER LOGIC
MN	MICRO NETWORKS
mii	MICROPAC INDUSTRIES
	MICRO POWER SYSTEMS
	MITEL SEMICONDUCTOR
	MITSUBISHI
MMI MMI*	MONOLITHIC MEMORIES
MOS	MOS TECHNOLOGY
MOSTEK	MOSTEK
M	MOTOROLA
NCR	NCR
NEC	NEC

* DISCONTINUED LOGOS PROVIDED TO IDENTIFY OLDER DEVICES.

Continued

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LOGO	MANUFACTURER
NS *	NATIONAL
NC *	NITRON
NORTEC	NORTEC
NPC	NUCLEONIC PRODUCTS
OKI	OKI
oei OEI *	OPTICAL ELECTRONICS
MATSUSHITA	PANASONIC (Matsushita)
PLESSEY	PLESSEY
PMI PMI *	PRECISION MONOLITHICS
RCA Solid State	RCA
RAY	RAYTHEON SEMICONDUCTOR
RETICON	RETICON

LOGO	MANUFACTURER
Rockwell	ROCKWELL (COLLINS)
SGS-ATES *	SGS-ATES SEMICONDUCTOR
	SANYO
	SIGNETICS
SILICON GENERAL	SILICON GENERAL
	SILICONIX
Si	SILICON SYSTEMS
SSS	SOLID STATE SCIENTIFIC
S S *	SOLITRON
② SPRAGUE	SPRAGUE ELECTRIC
	STANDARD MICROSYSTEMS
	SUPERTEX

LOGO	MANUFACTURER
S	SYNERTEC
	TELARIS COMMUNICATIONS (formerly Telenetics)
	TEXAS INSTRUMENTS
TMX	TMX
TRW	TRW
TELEDYNE CRYSTALONICS	TELEDYNE CRYSTALONICS
TELEDYNE PHILBRICK	TELEDYNE PHILBRICK
	TELEDYNE SEMICONDUCTOR
TELE FUN KEN TFK	TELEFUNKEN
Toshiba	TOSHIBA
	WESTERN DIGITAL
Zilog	ZILOG

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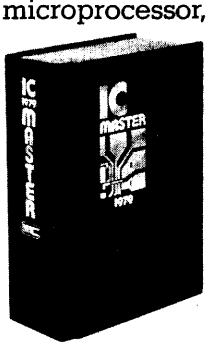
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MILITARY PARTS DIRECTORY

This section is divided into three parts: a table of those manufacturers willing to perform MIL-STD-883 screening, a two way military to commercial cross reference index, and the Qualified Parts List broken down into functions. It not only shows what devices are on the list and which manufacturers supply them, but also it decodes the military numbers into familiar terms.

how to use the military parts directory

The next page contains a table showing the manufacturers who have advised that they want to screen devices to MIL-STD-883 and/or perform other environmental screening. The table also indicates which companies are currently qualified to supply one or more devices on the QPL list. Such achievement is apt to indicate that these companies are well equipped to perform 883 testing. The following two pages provides convenient cross references between M38510 numbers and their commercial equivalents; plus indication of what devices are listed in the latest QPL.

The heart of this section is the functional QPL parts list. It is based on the latest Defense Electronics Supply Center Qualified Products List (QPL-38510-XX) at the time of publication. The revision and date of this list are indicated at the bottom of each page. Like the Master Selection Guide, the devices are classified my major functions; within each function the devices are arranged in alphanumeric order, which automatically groups CMOS together, 5400 Series together, etc.

A complete military part number includes a three letter suffix signifying the device class and packaging. The definitions of these letters are given in the Part Number Guide under "JAN Nomenclature." All the devices listed here meet class B and C requirements, a few devices (CMOS) meet class A specifications. The package styles and lead finishes that each manufacturer is qualified to supply can be determined by consulting the official QPL or by contacting the individual manufacturers. Once you have found the names of the companies you need to contact, you can reach them by using the information in the Manufacturers and Distributors Directory.

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MANUFACTURER	MIL-M-38510 QPL				MIL-STD-883 SCREENING			OTHER SCREENING	
	Linear	TTL	Other Bipolar	CMOS	Class A	Class B	Class C	Military	Industrial
Advanced Micro Devices	X	X			X	X	X	X	X
American Micro-systems, Inc.						X	X	X	X
Analog Devices						X	X		
Beckman Instruments					X	X	X	X	X
Burr-Brown Research						X	X	X	X
Cherry Semiconductor					X	X	X	X	X
Data Device						X	X	X	X
Datel						X	X	X	X
Electronic Arrays						X	X	X	X
EMM/Semi						X	X	X	X
Exar Integrated Systems						X	X	X	X
Fairchild Semiconductor	X	X	DTL		X	X	X	X	X
General Instrument						X	X		X
Harris Semiconductor			PROM		X	X	X	X	X
Hughes					X	X	X	X	X
Hybrid Systems					X	X	X	X	X
Intel			μP			X	X	X	X
Interdesign						X	X	X	X
International Microcircuits					X	X		X	X
Intersil	X				X	X	X	X	X
LSI Computer Systems					X	X	X	X	X
Micro Networks						X	X	X	X
Micropac					X	X	X	X	X
Micro Power Systems					X	X	X	X	X
Mitel Semiconductor					X	X	X	X	X
Monolithic Memories			PROM		X	X	X	X	X
Mostek						X	X	X	X
Motorola Semiconductor		X	ECL, μP	X	X	X	X	X	X
National Semiconductor	X	X		X	X	X	X	X	X
NEC America						X	X		X
NEC Microcomputers						X	X		X
Nitron						X	X	X	X
Nortec						X	X	X	X
Optical Electronics								X	X
Plessey Semiconductor					X	X	X		
Precision Monolithics					X	X	X	X	X
Raytheon Semiconductor		X			X	X	X	X	X
RCA Solid State	X			X	X	X	X	X	X
Rockwell						X	X	X	X
Signetics	X	X	PROM		X	X	X	X	X
Silicon General					X	X	X	X	X
Siliconix					X	X	X	X	X
SMC Microsystems						X	X	X	X
Solid State Scientific				X	X	X	X	X	X
Solitron					X	X	X	X	X
Sprague Electric					X	X	X	X	X
Standard Microsystems					X	X	X	X	X
Synertek						X	X	X	X
Teledyne Crystalonics					X	X	X	X	X
Teledyne Philbrick					X	X	X	X	X
Teledyne Semiconductor						X	X	X	X
Texas Instruments	X	X	RAM		X	X	X	X	X
TRW					X	X	X	X	X
Zilog						X	X	X	X

EXPLANATION:

The "MIL-M-38510" section indicates the IC manufacturers currently providing Q.P.L. ICs. More detailed information on the specific devices is given in the Qualified Products lists which follow.

The "MIL-STD-883 Screening" section lists those manufacturers who are both set up and actively want to screen devices to the levels indicated. "Other Screening" shows those who report that they want business calling for special military and industrial environment screening procedures.

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Cross Reference
Commercial to Military

Device	M38510/	QPL	Device	M38510/	QPL	Device	M38510/	QPL	Device	M38510/	QPL
HPROM0512	20101	X	54LS126	32302	X	54S08	08003		5446	01006	
LM109	10701		54LS13	31301	X	54S09	08004		5447	01007	
TMS4050	23502	X	54LS132	31302	X	54S10	07005	X	5448	01008	X
TMS4060	23501		54LS138	30701	X	54S11	08001	X	5449	01009	X
0026	03501		54LS139	30702	X	54S112	07102	X	5450	00501	X
101A	10103	X	54LS14	31303	X	54S113	07103		5451	00502	X
102	10601		54LS15	31002	X	54S114	07104		5453	00503	X
10501	06001	X	54LS151	30901	X	54S133	07009	X	5454	00504	X
10502	06002	X	54LS153	30902	X	54S134	07010	X	5470	00206	X
10504	06201		54LS157	30903	X	54S135	07502		5472	00201	X
10505	06003	X	54LS158	30904	X	54S140	08101	X	5473	00202	X
10506	06004	X	54LS160	31503	X	54S15	08002	X	5474	00205	X
10507	06005	X	54LS161	31504	X	54S151	07901	X	5475	01501	X
10509	06006	X	54LS162	31511	X	54S153	07902	X	5476	00204	X
10531	06101		54LS163	31512	X	54S157	07903	X	5477	01502	X
10535	06104		54LS164	30605	X	54S158	07904	X	5479	00207	X
10576	06103		54LS168	31505	X	54S174	07105	X	5480	00604	X
10597	06202		54LS169	31506	X	54S175	07106		5482	00601	X
106	10303		54LS174	30106	X	54S181	07801	X	5483	00602	X
10631	06102		54LS175	30107	X	54S182	07802		5485	15001	X
108A	10104	X	54LS181	30801	X	54S194	07601	X	5486	00701	X
110	10602	X	54LS190	31513	X	54S195	07602		5490	01307	X
111	10304	X	54LS191	31509	X	54S20	07006	X	5492	01301	X
118	10107	X	54LS192	31507	X	54S22	07007	X	5493	01302	X
148	11001	X	54LS193	31508	X	54S251	07905		5495	00901	X
2101	10105	X	54LS194	30601	X	54S257	07906	X	5496	00902	X
2108	10106		54LS195	30602	X	54S258	07907	X	55107	10401	X
2110	10603		54LS196	32001		54S30	07008	X	55108	10402	X
2111	10305		54LS197	32002		54S40	07201	X	55113	10405	X
2680	23501	X	54LS20	30007	X	54S51	07401	X	55114	10403	X
3018	10801	X	54LS21	31003	X	54S64	07402	X	55115	10404	X
3045	10802	X	54LS22	30008	X	54S65	07403	X	555	10901	X
4000	05201	X	54LS221	31402	X	54S74	07101	X	556	10902	X
4001	05202	X	54LS251	30905	X	54S85	08201	X	5603	20201	
4002	05203	X	54LS253	30908	X	54S86	07501	X	5623	20202	
4006	05701	X	54LS257	30906	X	5400	00104	X	6604	23602	
4007	05301	X	54LS258	30907	X	5401	00107	X	6605	23601	
4008	05401	X	54LS26	32102	X	5402	00401	X	6800	4001	X
4009	05501	X	54LS266	30303	X	5403	00109	X	710	10301	X
4010	05502	X	54LS27	30302	X	5404	00105	X	711	10302	X
4011	05001	X	54LS28	30204	X	5405	00108	X	723	10201	X
4012	05002	X	54LS283	31202	X	5406	00801	X	733	10501	X
4013	05101	X	54LS290	32003	X	5407	00803	X	741	10101	X
4014	05702	X	54LS293	32004	X	5408	01601	X	747	10102	X
4015	05703	X	54LS295	30606	X	5409	01602	X	76L42	02906	X
4017	05601	X	54LS30	30009	X	5410	00103	X	76L70	02805	X
4018	05602	X	54LS32	30501	X	54107	00203	X	78M05	10702	X
4019	05302	X	54LS365	32201	X	5412	00106	X	78M12	10703	X
4020	05603	X	54LS366	32202	X	54116	01503	X	78M15	10704	X
4021	05704	X	54LS367	32203	X	54121	01201	X	78M24	10705	X
4022	05604	X	54LS368	32204	X	54122	01202	X	78U5	10706	X
4023	05003	X	54LS37	30202	X	54123	01203	X	7812	10707	X
4024	05605	X	54LS38	30203	X	54125	15301		7815	10708	X
4025	05204	X	54LS395	30607	X	54126	15302	X	7820	10408	
4027	05102	X	54LS40	30201	X	5413	15101	X	7824	10709	X
4030	05303	X	54LS42	30703	X	54132	15103	X	7830	10409	X
4031	05705	X	54LS47	30704	X	5414	15102	X	7831	10406	
4034	05706		54LS51	30401	X	54145	01005	X	7832	10407	
4041	05505	X	54LS54	30402	X	54147	15601		8080A	42001	X
4049	05503	X	54LS73	30101	X	54148	15602		82S126	20301	X
4050	05504	X	54LS74	30102	X	54150	01401	X	82S129	20302	X
4136	11004	X	54LS76	30110	X	54151	01406	X	82S130	20401	X
5280	23505		54LS83	31201	X	54153	01403	X	82S131	20402	X
5303	20101		54LS85	31101	X	54154	15201	X	82S136	20601	
5304	20102		54LS86	30502	X	54155	15202	X	82S137	20602	
54H00	02304	X	54LS90	31501	X	54156	15203	X	8250	15204	X
54H01	02306	X	54LS92	31510	X	54157	01405	X	8251	15205	X
54H04	02305	X	54LS93	31502	X	5416	00802	X	8252	15206	X
54H08	15501	X	54LS95	30603	X	54160	01303	X	9093	03304	
54H10	02303	X	54LS96	30604	X	54161	01306	X	930	03001	X
54H101	02205	X	54L00	02004	X	54162	01305	X	9300	15901	X
54H103	02206	X	54L02	02701	X	54163	01304	X	9304	00603	X
554H11	15502	X	54L03	02006	X	54164	00903	X	9309	01404	X
43H20	02302	X	54L04	02005	X	54165	00904	X	9312	01402	X
54H21	15503	X	54L10	02003	X	5417	00804	X	9314	01504	X
43H22	02307	X	54L121	04201		54170	01801	X	9317	15802	
54H30	02301	X	54L122	04202		54174	01701	X	9318	15603	X
54H40	02401	X	54L164	02802		54175	01702	X	932	03101	
54H50	04001	X	54L193	02503		54180	01901	X	9321	15801	
54H51	04002	X	54L20	02002	X	54181	01101	X	9322	01405	X
54H53	04003	X	54L30	02001	X	54182	01102	X	9324	15002	X
54H54	04004	X	54L42	02901		54192	01308	X	9328	15902	
54H55	04005	X	54L43	02902		54193	01309	X	933	03105	
54H72	02201	X	54L44	02903		54194	00905	X	9334	16001	
54H73	02202	X	54L46	02904		54195	00906	X	9338	15701	
54H74	02203	X	54L47	02905		5420	00102	X	93410	23001	
54H76	02204	X	54L51	04101		5423	00402	X	93411	23002	
54LS00	30001	X	54L54	04102		5425	00403	X	93412	23003	
54LS02	30301	X	54L55	04103		5426	00805	X	935	03002	X
54LS03	30002	X	54L71	02101	X	5427	00404	X	936	03003	X
54LS04	30003	X	54L72	02102	X	5428	16201		940	03002	X
54LS05	30004	X	54L73	02103	X	5430	00101	X	944	03102	
54LS08	31004	X	54L74	02105	X	5432	16101	X	945	03301	
54LS10	30005	X	54L78	02104	X	54365	16301	X	946	03004	X
54LS107	30108	X	54L86	02601	X	54366	16302	X	948	03302	
54LS109	30109	X	54L90	02501	X	54367	16303	X	950	03303	
54LS11	31001	X	54L91	02806		54368	16304	X	951	03201	
54LS112	30103	X	54L93	02502	X	5437	00302	X	957	03103	
54LS113	30104	X	54L95	02801	X	5438	00303	X	958	03104	
54LS114	30105	X	54S00	07001	X	5440	00301	X	9601	01204	X
54LS12	30006	X	54S02	07301	X	5442	01001	X	9602	01205	X
54LS122	31403	X	54S03	07002	X	5443	01002	X	962	03005	X
54LS123	31401	X	54S04	07003	X	5444	01003	X	00101	5430	X
54LS125	32301	X	54S05	07004	X	5445	01004	X	00102	5420	X

NOTE: Items marked X in the QPL column are listed on QPL-38510-36 with at least one source.

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Cross Reference
Military to Commercial

M38510/	Device	QPL
00103	5410	X
00104	5400	X
00105	5404	X
00106	5412	X
00107	5401	X
00108	5405	X
00109	5403	X
00201	5472	X
00202	5473	X
00203	54107	X
00204	5476	X
00205	5474	X
00206	5470	X
00207	5479	X
00301	5440	X
00302	5437	X
00303	5438	X
00401	5402	X
00402	5423	X
00403	5425	X
00404	5427	X
00501	5450	X
00502	5451	X
00503	5453	X
00504	5454	X
00601	5482	X
00602	5483	X
00603	9304	X
00604	5480	X
00701	5486	X
00801	5406	X
00802	5416	X
00803	5407	X
00804	5417	X
00805	5426	X
00901	5495	X
00902	5496	X
00903	54164	X
00904	54165	X
00905	54194	X
00906	54195	X
01001	5442	X
01002	5443	X
01003	5444	X
01004	5445	X
01005	54145	X
01006	5446	
01007	5447	
01008	5448	X
01009	5449	X
01101	54181	X
01102	54182	X
01201	54121	X
01202	54122	X
01203	54123	X
01204	9601	X
01205	9602	X
01301	5492	X
01302	5493	X
01303	54160	X
01304	54163	X
01305	54162	X
01306	54161	X
01307	5490	X
01308	54192	X
01309	54193	X
01401	54150	X
01402	9312	X
01403	54153	X
01404	9303	X
01405	9322	X
01405	54157	X
01406	54151	X
01501	5475	X
01501	5475	X
01502	5477	X
01503	54116	X
01504	9314	X
01601	5408	X
01602	5409	X
01701	54174	X
01702	54175	X
01801	54170	
01901	54180	X
02001	54L30	X
02002	54L20	X
02003	54L10	X
02004	54L00	X
02005	54L04	X
02006	54L03	X
02101	54L71	X
02102	54L72	X
02103	54L73	X
02104	54L78	X
02105	54L74	X
02201	54H72	X
02202	54H73	X
02203	54H74	X
02204	54H76	X
02205	54H101	X
02206	54H103	X
02301	54H30	X
02302	54H20	X
02303	54H10	X
02304	54H00	X
02305	54H04	X
02306	54H01	X
02307	54H22	X
02401	54H40	X
02501	54L90	X
02502	54L93	X
02503	54L193	
02601	54L86	X
02701	54L02	X
02801	54L95	X
02802	54L164	
02805	76L70	
02806	54L91	
02901	54L42	
02902	54L43	
02903	54L44	
02904	54L46	
02905	54L47	
02906	76L42	
03001	930	X
03002	935	X
03003	936	X
03004	946	X
03005	962	X
03101	932	
03102	944	
03103	957	
03104	958	
03105	933	
03201	951	
03301	945	
03302	948	
03303	950	
03304	9903	
03501	0026	
04001	54H50	X
04002	54H51	X
04003	54H53	X
04004	54H54	X
04005	54H55	X
04101	54L51	X
04102	54L54	X
04103	54L55	
04201	54L121	
04202	54L122	
05001	4011	X
05002	4012	X
05003	4023	X
05101	4013	X
05201	4000	X
05102	4027	X
05202	4001	X
05203	4002	X
05204	4025	X
05301	4007	X
05302	4019	X
05303	4030	X
05401	4008	X
05501	4009	X
05502	4010	X
05503	4049	X
05504	4050	X
05505	4041	X
05601	4017	X
05602	4018	X
05603	4020	X
05604	4022	X
05605	4024	X
05701	4006	X
05702	4014	X
05703	4015	X
05704	4021	X
05705	4031	X
05706	4034	
06001	10501	X
06002	10502	X
06003	10505	X
06004	10506	X
06005	10507	X
06006	10509	X
06101	10531	
06102	10631	
06103	10576	
06104	10535	
06201	10504	
06202	10597	
07001	54S00	X
07002	54S03	X
07003	54S04	X
07004	54S05	X
07005	54S10	X
07006	54S20	X
07007	54S22	X
07008	54S30	X
07009	54S133	X
07010	54S134	X
07101	54S74	X
07102	54S112	X
07103	54S113	
07104	54S114	
07105	54S174	X
07106	54S175	X
07201	54S40	X
07301	54S02	X
07401	54S51	X
07402	54S64	X
07403	54S65	X
07501	54S86	X
07502	54S135	
07601	54S194	X
07602	54S195	
07801	54S181	X
07802	54S182	
07901	54S151	X
07902	54S153	X
07903	54S157	X
07904	54S158	X
07905	54S251	
07906	54S257	X
07907	54S258	X
08001	54S11	X
08002	54S15	X
08003	54S08	X
08004	54S09	
08101	54S140	X
08201	54S85	X
10101	741	X
10102	747	X
10103	101A	X
10104	108A	X
10105	2101	X
10106	2108	
10107	118	X
10201	723	X
10301	710	X
10302	711	X
10303	106	
10304	111	X
10305	2111	
10401	55107	X
10402	55108	X
10403	55114	X
10404	55115	X
10405	55113	X
10406	7831	
10407	7832	
10408	7820	X
10409	7830	X
10501	733	X
10601	102	
10602	110	X
10603	2110	X
10701	LM109	
10702	78M05	X
10703	78M12	X
10704	78M15	X
10705	78M24	X
10706	7805	X
10707	7812	X
10708	7815	X
10709	7824	X
10801	3018	
10802	3045	X
10901	555	X
10902	556	X
11001	148	X
11004	4136	X
15001	5485	X
15002	9324	X
15101	5413	X
15102	5414	X
15103	54132	X
15201	54154	X
15202	54155	X
15203	54156	X
15204	8250	X
15205	8251	X
15206	8252	X
15301	54125	
15302	54126	X
15501	54H08	X
15502	54H11	X
15503	54H21	X
15601	54147	
15602	54148	
15603	9318	X
15701	9338	
15702	9328	
15801	9321	
15802	9317	
15901	9300	X
16001	9334	
16101	5432	X
16201	5428	
16301	54365	X
16302	54366	X
16303	54367	X
16304	54368	X
20101	HPROM0512	X
20102	5304	
20201	5603	
20202	5604	
20301	82S126	X
20302	82S129	X
20401	82S130	X
20402	82S131	X
20601	82S136	
20602	82S137	
23001	83410	
23002	93411	
23002	93421	
23501	2680	X
23501	TMS4060	
23502	TMS4050	X
23505	5280	
23601	6605	
23602	6604	
30001	54LS00	X
30002	54LS03	X
30003	54LS04	X
30004	54LS05	X
30005	54LS10	X
30006	54LS12	X
30007	54LS20	X
30008	54LS22	X
30009	54LS30	X
30101	54LS73	X
30102	54LS74	X
30102	41574	X
30103	54LS112	X
30104	54LS113	X
30105	54LS114	X
30106	54LS174	X
30107	54LS175	X
30108	54LS107	X
30109	54LS109	X
30110	54LS76	X
30201	54LS40	X
30202	54LS37	X
30203	54LS38	X
30204	54LS28	X
30301	54LS02	X
30302	54LS27	X
30303	54LS266	X
30401	54LS51	X
30402	54LS54	X
30501	54LS32	X
30502	54LS86	X
30601	54LS194	X
30602	54LS195	X
30603	54LS95	X
30604	54LS96	X
30605	54LS164	X
30606	54LS295	X
30607	54LS395	X
30701	54LS138	X
30702	54LS139	X
30703	54LS42	X
30704	54LS47	X
30801	54LS181	X
30901	54LS151	X
30902	54LS153	X
30903	54LS157	X
30904	54LS158	X
30905	54LS251	X
30906	54LS257	X
30907	54LS258	X
30908	54LS253	X
31001	54LS11	X
31002	54LS15	X
31003	54LS21	X
31004	54LS08	X
31101	54LS85	X
31201	54LS83	X
31202	54LS283	X
31301	54LS13	X
31302	54LS14	X
31303	54LS132	X
31401	54LS123	X
31402	54LS221	X
31403	54LS122	X
31501	54LS90	X
31502	54LS93	X
31503	54LS160	X
31504	54LS161	X
31505	54LS168	X
31506	54LS169	X
31507	54LS192	X
31508	54LS193	X
31509	54LS191	X
31510	54LS92	X
31511	54LS162	X
31512	54LS163	X
31513	54LS190	X
32001	54LS196	
32002	54LS197	
32003	54LS290	X
32004	54LS293	X
32102	54LS26	X
32201	54LS365	X
32202	54LS366	X
32203	54LS367	X
32204	54LS368	X
32301	54LS125	X
32302	54LS126	X
40001	6800	X
42001	8080A	X

NOTE: Items marked X in the QPL column are listed on QPL-38510-36 with at least one source.

DIGITAL

ARITHMETIC FUNCTION

Device	M38510/	Description	Source
4008	05401	4-Bit Full Adder	RCA
5480	00604	Gated Full Adder	Motorola
5482	00601	2-Bit Binary Full Adder	Motorola
5483	00602	4-Bit Binary Full Adder (Look-Ahead Carry)	Motorola National Signetics TI
5485	15001	4-Bit Magnitude Comparator	Motorola Signetics
54181	01101	Arithmetic Logic/ Function Generator	Motorola National
54182	01102	Look-Ahead Carry Generator	Motorola Signetics
54LS83	31201	4-Bit Binary Full Adder	Fairchild Raytheon Signetics TI
54LS85	31101	4-Bit Magnitude Comparator	Signetics TI
54LS181	30801	ALU/Function Generator	Raytheon Signetics
54LS283	31202	4-Bit Binary Full Adder	Fairchild Raytheon Signetics TI
54S85	08201	4-Bit Magnitude Comparator	Signetics
54S181	07801	ALU/Function Generator	Signetics
9304	00603	Dual Full Adder	Motorola
9324	15002	4-Bit Magnitude Comparator	Motorola

BUFFERS, INVERTERS

4007	05301	Dual Complementary Pair plus Inverter	National RCA SSS
4009	05501	Hex Buffer/Converter, Inverting	National RCA
4010	05502	Hex Buffer/Converter, Non-Inverting	National RCA
4041	05505	Quad True/ Complement Buffer	RCA
4049	05503	Hex Buffer/Converter, Inverting	National RCA SSS
4050	05504	Hex Buffer/Converter, Non-Inverting	National RCA SSS
5404	00105	Hex Inverter	Fairchild Motorola National Signetics TI
5405	00108	Hex Inverter, O/C	Fairchild Motorola National Signetics TI
5437	00302	Quad 2-Input NAND Buffer	Motorola National Signetics TI
5438	00303	Quad 2-Input NAND Buffer, O/C	Fairchild Motorola National Signetics TI
5440	00301	Dual 4-Input NAND Buffer	Fairchild Motorola National Signetics TI
54125/6	15301/2	Quad Gated Buffer, 3 State	Signetics
54365	32201	Hex Buffer, TS	Signetics
54366	32202	Hex Inverter, TS	Signetics
54367	32203	Hex Buffer, TS	Signetics
54368	32204	Hex Inverter, TS	Signetics
54H04	02305	Hex Inverter	Fairchild Motorola Signetics TI

BUFFERS, INVERTERS (cont)

Device	M38510/	Description	Source
54H40	02401	Dual 4-Input NAND Buffer	Motorola Signetics TI
54LS04	30003	Hex Inverter	Fairchild Motorola National Signetics TI
54LS05	30004	Hex Inverter, O/C	Motorola National Signetics TI
54LS28	30204	Quad 2-Input NOR Buffer	Signetics
54LS37	30202	Quad 2-Input NAND Buffer	Motorola National Signetics TI
54LS40	30201	Dual 4-Input NAND Buffer	National Signetics
54LS125	32301	Quad Gated Buffer, TS	Signetics
54LS126	32302	Quad Gated Buffer, TS	Signetics
54LS293	32004	Dual Quad Inverter, TS	TI
54LS365	32201	Hex Buffer, TS	Fairchild Signetics TI
54LS366	32202	Hex Inverter, TS	Fairchild Signetics
54LS367	32203	Hex Buffer, TS	Motorola
54LS368	32204	Hex Inverter, TS	Fairchild Motorola Signetics
54L04	02005	Hex Inverter	National
54S04	07003	Hex Inverter	Signetics
54S05	07004	Hex Inverter, O/C	Signetics
54S40	07201	Dual 4-Input NAND Buffer	Signetics
935	03002	Hex Inverter	
936	03003	Hex Inverter	

COUNTERS

4017	05601	Decade Counter/Divider, Decoded Output	RCA SSS
4018	05602	Presettable Divide-by-N Counter	RCA
4020	05603	14-Bit Binary Counter	RCA
4022	05604	Divide-by-8 Counter/ Divider, Decoded Output	RCA
4024	05605	7-Bit Binary Counter	RCA SSS
5490	01307	Decade Counter, Ripple	Motorola
5492	01301	Divide-by-12 Counter (÷2, ÷6)	Motorola Signetics
5493	01302	4-Bit Binary Counter	Motorola Signetics
54160	01303	Synchronous Decade Counter	AMD Motorola National Signetics
54161	01306	Synchronous 4-Bit Binary Counter	AMD Motorola National Signetics
54162	01305	Fully Synchronous Decade Counter	Motorola National Signetics
54163	01304	Fully Synchronous 4-Bit Binary Counter	Motorola National Signetics
54192	01308	Decade Up/Down Counter	Motorola
54193	01309	Binary Up/Down Counter	Motorola Signetics
54LS90	31501	Decade Counter	TI
54LS92	31510	Divide-by-12 Counter	TI
54LS93	31502	4-Bit Binary Counter	TI
54LS160	31503	Synchronous Decade Counter	TI
54LS161	31504	Synchronous 4-Bit Binary Counter	TI
54LS162	31511	Fully Synchronous Decade Counter	TI

COUNTERS (cont)

Device	M38510/	Description	Source
54LS163	31512	Fully Synchronous 4-Bit Binary Counter	TI
54LS190	31513	Synchronous Decade Up/Down Counter	TI
54LS191	31509	Synchronous Binary Up/Down Counter	TI
54LS192	31507	Decade Up/Down Counter	TI
54LS193	31508	Binary Up/Down Counter	TI
54LS290	32003	Decade Counter, Divide-by-2 and 5	TI
54L90	02501	Decade Counter, Ripple	National
54L93	02502	4-Bit Binary Counter	National

DECODERS

5442	01001	BCD-to-Decimal Decoder	Motorola National Signetics
5443	01002	Excess 3-to-Decimal Decoder	Motorola Signetics
5444	01003	Excess 3-Gray-to-Decimal Decoder	Motorola Signetics
5445	01004	BCD-to-Decimal Decoder, O/C	Motorola
5448	01008	BCD-to-Seven Segment Decoder/Driver with 30V Output	Motorola
5449	01009	BCD-to-7 Segment Decoder, O/C	Motorola
54145	01005	BCD-to-7 Segment Decoder	Motorola
54148	15602	8-Bit Priority Encoder	Signetics
54154	15201	4-Line to 16-Line Decoder/Demultiplexer	Motorola
54155	15202	Dual 2-Line to 4-Line Decoder/Demultiplexer	Motorola
54156	15203	Dual 2-Line to 4-Line Decoder/Demultiplexer	Motorola
54LS138	30701	3-to-8-Line Decoder/ Demultiplexer	Fairchild Motorola
54LS139	30702	Dual 2-Line to 4-Line Decoder/Demultiplexer	Fairchild Motorola
54LS42	30703	BCD to Decimal Decoder	Motorola
54LS47	30704	BCD to 7-Segment Decoder	TI
8250	15204	Binary-to-Octal Decoder	Signetics
8251	15205	BCD-to-Decimal Decoder	Signetics
8252	15206	BCD-to-Decimal Decoder	Motorola
9318	15603	8-Input Priority Encoder	Motorola

DRIVERS

5406	00801	Hex Inverter Buffer/ Driver, O/C High Voltage Output	Fairchild Motorola TI
5407	00803	Hex Buffer/Driver, O/C High Voltage Output	Fairchild Motorola TI
5416	00802	Hex Inverter Buffer/ Driver, O/C High Voltage Output	Fairchild Motorola TI
5417	00804	Hex Buffer/Driver, O/C High Voltage Output	Fairchild Motorola TI

FLIP-FLOPS

4013	05101	Dual "D" Flip-Flop with Set/Reset	Motorola National RCA SSS
4027	05102	Dual J-K Master-Slave Flip-Flop	National RCA
5470	00206	Positive Edge-Triggered J-K Flip-Flop	Fairchild Motorola Signetics TI
5472	00201	J-K Master Slave Flip-Flop (AND Inputs)	National Signetics TI

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FLIP-FLOPS (cont)

Device	M38510/	Description	Source
5473	00202	Flip-Flop Dual J-K Master Slave	Motorola National Signetics TI
5474	00205	Dual D-Type Edge-Triggered Flip-Flop	Fairchild National Signetics TI
5476	00204	Dual J-K Master Slave Flip-Flop with Preset and Clear	National Signetics TI
5479	00207	Dual D-Type Flip-Flop	Motorola
54107	00203	Dual J-K Master Slave Flip-Flop	Motorola National Signetics TI
54174	01701	Hex D-Type Flip-Flop	Fairchild Motorola Signetics
54175	01702	Quad D-Type Flip-Flop	Motorola Signetics
54H72	02201	J-K Master-Slave Flip-Flip (AND Inputs)	Motorola Signetics
54H73	02202	Dual J-K Master-Slave Flip-Flop	Signetics Motorola
54H74	02203	Dual D-Type Edge-Triggered Flip-Flop	Signetics
54H76	02204	Dual J-K Flip-Flop	TI Signetics
54H101	02205	J-K Negative Edge-Triggered Flip-Flop (AND-OR Inputs)	Motorola Signetics
54H103	02206	Dual J-K Negative Edge Triggered Flip-Flop	Motorola Signetics
54LS73	30101	Dual J-K Master Slave Flip-Flop	Signetics TI
54LS74	30102	Dual D-Type Positive Edge-Triggered Flip-Flop with Preset and Clear	Motorola Signetics TI
54LS76	30110	Dual J-K Master Slave Flip-Flop with Preset and Clear	TI Signetics
54LS107	30108	Dual Master Slave Flip-Flop	Signetics TI
54LS109	30109	Dual J-K Positive Edge-Triggered Flip-Flop with Preset and Clear	Fairchild Signetics TI
54LS112	30103	Dual J-K Negative Edge-Triggered Flip-Flop with Preset and Clear	Signetics TI
54LS113	30104	Dual J-K Negative Edge-Triggered Flip-Flop with Separate Preset and Clock	Signetics TI
54LS114	30105	Dual J-K Negative Edge-Triggered Flip-Flop with Clock, Clear, and Preset	Signetics TI
54LS174	30106	Hex D-Type Flip-Flop	AMD Fairchild Motorola TI
54LS175	30107	Quad D-Type Flip-Flop	AMD Motorola TI
54L71	02101	J-K Master-Slave Flip-Flop (AND-OR Inputs)	National
54L72	02102	J-K Master-Slave Flip-Flop (AND Inputs)	National
54L73	02103	Dual J-K Master-Slave Flip-Flop	National
54L74	02105	Dual D-Type Edge-Triggered Flip-Flop	National
54L78	02104	Dual J-K Master-Slave Flip-Flop	National
54S74	07101	Dual D Flip-Flop	Signetics
54S112	07102	Dual J-K Negative Edge-Triggered Flip-Flop with Preset and Clear	Signetics
54S174	07105	Hex D-Type Flip-Flop	AMD Fairchild
54S175	07106	Quad D-Type Flip-Flop	Fairchild AMD

GATES, AND/NAND

Device	M38510/	Description	Source
4011	05001	Quad 2-Input NAND Gate	National RCA SSS
4012	05002	Dual 4-Input NAND Gate	National RCA SSS
4023	05003	Triple 3-Input NAND Gate	National RCA SSS
5400	00104	Quad 2-Input NAND Gate	Fairchild Motorola National Signetics TI
5401	00107	Quad 2-Input NAND Gate, O/C	Fairchild Motorola National Signetics TI
5403	00109	Quad 2-Input NAND Gate, O/C	Fairchild Motorola National Signetics TI
5408	01601	Quad 2-Input AND Gate	Fairchild Motorola National Signetics
5409	01602	Quad 2-Input AND Gate, O/C	Fairchild Motorola Signetics
5410	00103	Triple 3-Input NAND Gate	Fairchild Motorola National Signetics TI
5412	00106	Triple 3-Input NAND Gate, O/C	TI
5420	00102	Dual 4-Input NAND Gate	Fairchild Motorola National Signetics TI
5426	00805	Quad 2-Input NAND Gate, O/C	Signetics
5430	00101	8-Input NAND Gate	Fairchild Motorola National Signetics TI
54H00	02304	Quad 2-Input NAND Gate	Fairchild Motorola Signetics TI
54H01	02306	Quad 2-Input NAND Gate, O/C	Motorola Signetics TI
54H08	15501	Quad 2-Input AND Gate	Motorola Signetics
	15504	Quad 2-Input AND Gate	Motorola
54H10	02303	Triple 3-Input NAND Gate	Fairchild Motorola Signetics TI
54H11	15502	Triple 3-Input AND Gate	Motorola Signetics
54H20	02302	Dual 4-Input NAND Gate	Fairchild Motorola Signetics TI
54H21	15503	Dual 4-Input AND Gate	Signetics
54H22	02307	Dual 4-Input NAND Gate, O/C	Fairchild Motorola Signetics
54H30	02301	8-Input NAND Gate	Fairchild Motorola Signetics TI
54LS00	30001	Quad 2-Input NAND Gate	Fairchild National Motorola Signetics TI
54LS03	30002	Quad 2-Input NAND Gate, O/C	Motorola Signetics TI
54LS08	31004	Quad 2-Input AND Gate	Fairchild Motorola National Raytheon Signetics TI

GATES, AND/NAND (cont)

Device	M38510/	Description	Source
54LS10	30005	Triple 3-Input NAND Gate	Fairchild Motorola National Signetics TI
54LS11	31001	Triple 3-Input AND Gate	Fairchild National Motorola Raytheon Signetics TI
54LS12	30006	Triple 3-Input NAND Gate, O/C	Signetics TI
54LS15	31002	Triple 3-Input AND Gate, O/C	National Signetics TI
54LS20	30007	Dual 4-Input NAND Gate	Fairchild National Signetics TI
54LS21	31003	Dual 4-Input AND Gate	Fairchild National Raytheon Signetics TI
54LS22	30008	Dual 4-Input NAND Gate, O/C	National Signetics TI
54LS26	32102	Quad 2-Input NAND Gate, O/C, to 15V	Signetics
54LS30	30009	8-Input NAND Gate	Fairchild Motorola National Signetics
54LS38	30203	Quad 2-Input NAND Gate, O/C	National Raytheon Signetics TI
54L00	02004	Quad 2-Input NAND Gate	National
54L03	02006	Quad 2-Input NAND Gate, O/C	National
54L10	02003	Triple 3-Input NAND Gate	National
54L20	02002	Dual 4-Input NAND Gate	National
54L30	02001	8-Input NAND Gate	National
54S00	07001	Quad 2-Input NAND Gate	Fairchild Signetics
54S03	07002	Quad 2-Input NAND Gate, O/C	Fairchild Signetics
54S08	08003	Quad 2-Input AND Gate	Fairchild Signetics
54S10	07005	Triple 3-Input NAND Gate	Fairchild Signetics
54S11	08001	Triple 3-Input AND Gate	Fairchild Signetics
54S15	08002	Triple 2-Input AND Gate, O/C	Signetics
54S20	07006	Dual 4-Input NAND Gate	Fairchild Signetics
54S22	07007	Dual 4-Input NAND Gate, O/C	Signetics
54S30	07008	8-Input NAND Gate	Fairchild
54S133	07009	13-Input NAND Gate	Signetics
54S134	07010	12-Input NAND Gate, 3 State	Signetics
930	03001	Dual 4-Input NAND Gate, Expandable	Fairchild
946	03004	Quad 2-Input NAND Gate	Fairchild
962	03005	Triple 3-Input NAND Gate	Fairchild

GATES, AND-OR/AND-OR-INVERT

4019	05302	Quad AND-OR Select Gate	National RCA SSS
5450	00501	2-2-Input AOI Gate, Expandable	Motorola National Signetics TI
5451	00502	2-2-Input AOI Gate, Expandable	Motorola National Signetics TI

GATES, AND-OR/AND-OR-INVERT (cont)

Device	M38510/	Description	Source
5453	00503	2-2-2-2-Input AOI Gate, Expandable	Motorola National Signetics TI
5454	00504	2-2-2-2-Input AOI Gate	Motorola National Signetics TI
54H50	04001	2-2-Input AOI Gate, Expandable	Motorola Signetics
54H51	04002	Dual 2-2-Input AOI Gate	Motorola Signetics
54H53	04003	2-2-2-3-Input AOI Gate, Expandable	Motorola Signetics
54H54	04004	2-2-2-3-Input AOI Gate	Motorola Signetics
54H55	04005	4-4-Input AOI Gate, Expandable	Motorola Signetics
54LS51	30401	Dual 2-3-Input AOI Gate	Motorola National Signetics TI
54LS54	30402	2-2-2-3-Input AOI Gate	Motorola National Signetics TI
54S51	07401	2-2-Input AOI Gate	Signetics
54S64	07402	4-2-3-2-Input AOI Gate	Signetics

GATES, EXCLUSIVE OR/NOR

4030	05303	Quad Exclusive OR Gate	National SSS
5486	00701	Quad 2-Input Exclusive OR Gate	Fairchild Motorola National Signetics TI
54LS86	30502	Quad 2-Input Exclusive OR	Motorola National Signetics
54LS266	30303	Quad 2-Input Exclusive NOR Gate, O/C	National Signetics TI
54S86	07501	Quad 2-Input Exclusive OR Gate	Signetics
10507	06005	Triple 2-Input Exclusive OR/NOR Gate	Motorola

GATES, OR/NOR

4000	05201	Dual 3-Input NOR Gate plus Inverter	RCA SSS
4001	05202	Quad 2-Input NOR Gate	National RCA SSS
4002	05203	Dual 4-Input NOR Gate	National RCA SSS
4025	05204	Triple 3-Input NOR Gate	National RCA SSS
5402	00401	Quad 2-Input NOR Gate	Fairchild Motorola National Signetics TI
5423	00402	Dual 4-Input NOR Gate with Strobe, Expandable	Motorola TI
5425	00403	Dual 4-Input NOR Gate with Strobe	Motorola TI
5427	00404	Triple 3-Input NOR Gate	Fairchild Motorola Signetics TI
5432	16101	Quad 2-Input OR Gate	Signetics
54LS02	30301	Quad 2-Input NOR Gate	Fairchild Motorola National Raytheon Signetics TI
54LS27	30302	Triple 3-Input NOR Gate	Fairchild Motorola National Signetics TI

GATES, OR/NOR (cont)

Device	M38510/	Description	Source
54LS32	30501	Quad 2-Input OR Gate	Fairchild Motorola National Signetics
54L02	02701	Quad 2-Input NOR Gate	National
54S02	07301	Quad 2-Input NOR Gate	Signetics
10501	06001	Quad 2-Input OR/NOR Gate	Motorola
10502	06002	Quad 2-Input Gate (3 NOR, 1 OR/NOR)	Motorola
10505	06003	2-3-2-Input OR/NOR Gate	Motorola
10506	06004	4-3-3-Input OR/NOR Gate	Motorola
10509	06006	4-5-Input OR/NOR Gate	Motorola

LATCHES

5475	01501	Quad Bistable Latch, Complementary Output	Motorola Signetics
5477	01502	Quad Bistable Latch	Motorola Signetics
9314	01504	Quad Multifunction Latch	Motorola

MULTIPLEXERS

54150	01401	16-Channel Data Selector/Multiplexer	Motorola
54151	01406	8-Input Multiplexer	Motorola National Signetics
54153	01403	Dual 4-Channel Data Selector/Multiplexer	Motorola National Signetics
54LS151	30901	8-Input Multiplexer	Motorola Raytheon
54LS153	30902	Dual 4-Channel Data Selector/Multiplexer	AMD Fairchild Motorola Raytheon Signetics TI
54LS157	30903	Quad 2-Input Multiplexer, Non-Inverting	AMD Fairchild Raytheon Signetics TI
54LS158	30904	Quad 2-Input Multiplexer, Inverting	AMD Raytheon Signetics TI
54LS251	30905	8-Input Multiplexer, Complementary Input, Strobe, TS	Fairchild TI
54LS253	30908	Dual 4-Input Multiplexer, TS	Fairchild Motorola Signetics TI
54LS257	30906	Quad 2-Input Multiplexer, Non-Inverting, TS	Signetics TI
54LS258	30907	Quad 2-Input Multiplexer, Inverting, TS	TI
54S151	07901	8-Input Multiplexer	Fairchild Signetics
54S153	07902	Dual 4-Channel Data Selector/Multiplexer	Signetics
54S157	07903	Quad 2-Input Multiplexer, Non-Inverting	AMD Fairchild Signetics
54S158	07904	Quad 2-Input Multiplexer, Inverting	AMD Fairchild Signetics
54S257	07906	Quad 2-Input Multiplexer, Non-Inverting, TS	AMD
54S258	07907	Quad 2-Input Multiplexer, Inverting, TS	AMD
9309	01404	Dual 4-Input Multiplexer	AMD Motorola Signetics
9312	01402	8-Channel Data Selector/ Multiplexer	AMD Motorola
9322	01405	Quad 2-Input Data Selector/Multiplexer (Non-Inverting)	AMD Motorola National Signetics

MULTIVIBRATORS

Device	M38510/	Description	Source
54121	01201	Monostable Multivibrator	Motorola Signetics
54122	01202	Retriggerable Monostable Multivibrator with Clear	Motorola
54123	01203	Dual Retriggerable Monostable Multivibrator with Clear	Motorola Signetics
54LS122	31403	Retriggerable Monostable Multivibrator with Clear	TI
54LS123	31401	Dual Retriggerable Monostable Multivibrator with Clear	TI
54LS221	31402	Dual Monostable Multivibrator, Schmitt Trigger Input	TI
9601	01204	One Shot Multivibrator	Motorola
9602	01205	Dual One Shot Multivibrator	Motorola

MISCELLANEOUS

5413	15101	Dual 4-Input NAND Schmitt Trigger	Motorola Signetics
5414	15102	Hex Schmitt Trigger, Inverting	Motorola Signetics
54132	15103	Quad 2-Input NAND Schmitt Trigger	Motorola Signetics
54180	01901	9-Bit Odd/Even Parity Generator/Checker	Motorola National Signetics
54LS13	31301	Dual 4-Input NAND Schmitt Trigger	Signetics TI
54LS14	31302	Hex Schmitt Trigger, Inverting	Signetics TI
54LS132	31303	Quad 2-Input NAND Schmitt Trigger	Motorola Signetics TI

INTERFACE

LINE DRIVERS AND RECEIVERS

54S140	08101	Dual 4-Input Positive NAND Line Driver	Signetics
55107	10401	Differential Line Receiver	Fairchild TI
55108	10402	Differential Line Receiver	Fairchild TI
55113	10405	Dual Differential Line Driver, Three-State	TI
55114	10403	Dual Differential Line Driver	Fairchild TI
55115	10404	Dual Differential Line Receiver	Fairchild TI

LINEAR

AMPLIFIERS

101A	10103	Operational Amplifier	AMD Fairchild National
108A	10104	Operational Amplifier	Fairchild National
118	10107	Operational Amplifier	National
148	11001	Quad Operational Amplifier	Fairchild
741	10101	Operational Amplifier	AMD Fairchild National Raytheon
747	10102	Dual Operational Amplifier	AMD Fairchild National
2101	10105	Dual Operational Amplifier	Fairchild
4136	11004	Quad Operational Amplifier	Signetics

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COMPARATORS

Device	M38510/	Description	Source
111	10304	Voltage Comparator	Fairchild National AMD
710	10301	Voltage Comparator	Fairchild
711	10302	Dual Voltage Comparator	Fairchild

FOLLOWERS

110	10602	Voltage Follower	Fairchild

TIMERS

555	10901	Timer	Signetics
556	10902	Dual Timer	Signetics

TRANSISTOR ARRAYS

3045	10802	Transistor Array	Fairchild

VOLTAGE REGULATORS

723	10201	Voltage Regulator	Fairchild
78M05	10702	5V, 500mA Voltage Regulator	Fairchild
78M12	10703	12V, 500mA Voltage Regulator	Fairchild
78M15	10704	15V, 500mA Voltage Regulator	Fairchild
78M24	10705	24V, 500mA Voltage Regulator	Fairchild
7805	10706	5V, 1A Voltage Regulator	Fairchild
7812	10707	12V, 1A Voltage Regulator	Fairchild
7815	10708	15V, 1A Voltage Regulator	Fairchild
7824	10709	24V, 1A Voltage Regulator	Fairchild

MEMORY

PROM

Device	M38510/	Description	Source
HPROM0512	20101	512-Bit Programmable Read Only Memory	Harris
82S226	20301	PROM, 256x4, OC	Harris MMI Signetics
82S129	20302	PROM, 256x4, TS	Harris MMI Signetics
82S130	20401	PROM, 512x4, OC	Harris MMI Signetics
82S131	20402	PROM, 512x4, TS	Harris MMI Signetics

RAM

2680	23501	4096x1 Dynamic RAM	TI
TMS4050	23502	4096x1 Dynamic RAM	TI

SHIFT REGISTERS

4006	05701	18-Bit Static S.R.	National RCA SSS
4014	05702	8-Bit Static S.R. (Synchronous)	National RCA
4015	05703	Dual 4-Bit Static S.R.	National RCA SSS
4021	05704	8-Bit Static S.R. (Asynchronous)	National RCA
4031	05705	64-Bit Static S.R.	National RCA
54L95	02801	4-Bit Parallel Access S.R.	National
5495	00901	4-Bit Parallel Access S.R.	Motorola Signetics National

SHIFT REGISTERS (cont)

Device	M38510/	Description	Source
5496	00902	5-Bit S.R.	Motorola Signetics National
54164	00903	8-Bit Serial-In Parallel-Out S.R.	National Signetics
54165	00904	8-Bit Parallel-Serial S.R.	Motorola
54194	00905	4-Bit Universal S.R.	Motorola National
54195	00906	4-Bit Parallel Access S.R.	Motorola
54LS95	30603	4-Bit Parallel Access S.R.	Signetics TI
54LS96	30604	5-Bit S.R.	Signetics TI
54LS164	30605	8-Bit Serial In, Parallel Out, S.R.	AMD National Signetics TI
54LS194	30601	4-Bit Universal Bidirectional S.R.	AMD Signetics TI
54LS195	30602	4-Bit Parallel In, Parallel Out, S.R.	AMD Signetics TI
54LS295	30606	4-Bit Parallel In, Parallel Out, Right/Left S.R.	Signetics TI
54LS395	30607	4-Bit Parallel In, Parallel Out, Cascadable S.R.	Signetics TI
54S194	07601	4-Bit Universal S.R.	AMD
9300	15901	Universal 4-Bit S.R.	Motorola
9328	15902	Dual 8-Bit S.R.	Motorola

MICROPROCESSOR

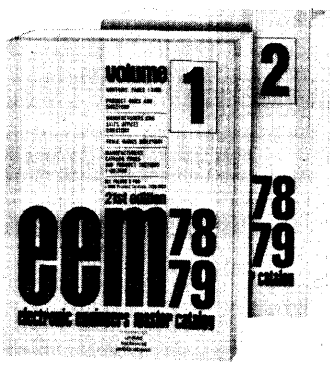
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8080A	42001	Microprocessor	Intel

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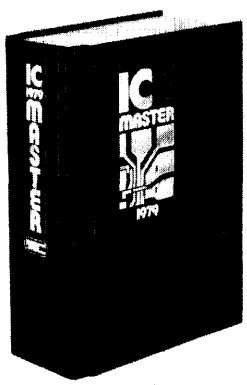
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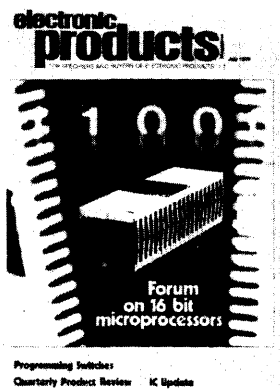
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APPLICATION NOTE DIRECTORY

The Application Note Directory is a comprehensive guide to the many IC application notes available. It lists the devices covered, describes each note, and tells who publishes each one.

how to use the application note directory

The application notes in this directory can be located by function or device number.

1. To find out what is published by function, locate the closest topics in the index below, turn to the pages indicated, and scan through the listings.

2. To find all the application notes covering a given device, look up the device in the Part Number Index at the front of this book. The ¶ sign leads to application notes.

The application note descriptions are organized under the headings: Digital, Linear, Memory and Microprocessor. Beneath those headings are functional and applications categories arranged alphabetically. Within each category the notes are arranged in alphabetical sequence by manufacturer. The mixing of functions and applications is necessary, since application notes do not lend themselves to classification entirely by function or entirely by application. When an application note fits under several categories, it is listed in one and cross referenced by the others. This may mean that you have to spend five minutes checking a number of categories to be sure you've found everything you want, but finding suitable information can save you considerable design time.

If an application note covers specific devices or it shows in some detail how certain devices are used, these device numbers are listed in parentheses just below the title.

The application note descriptions are as short as possible. They are designed to save you time in reading while giving an overall sense of the contents. The length of each note is indicated in parentheses on the last line; if the note is bound into a book, the last line will show that it is part of a handbook, databook, catalog, etc.

Once you have determined which application notes you need, check to see if the manufacturer has placed the complete application note in the back of this section (immediately following the short descriptions). If not, contact the manufacturer's sales office or write to the manufacturer. Be sure to give both the title and the application note number. Addresses and phone numbers are listed in the Manufacturers and Distributors Directory.

APPLICATION NOTE SUBJECTS

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DIGITAL

Arithmetic

1 **"The AM2506 — A Latching ALU"**
(AM2506)
Combines four-bit arithmetic logic unit and four-bit latch. Describes application in high-speed multiple word adder, multiple master-slave registers, 16-word arithmetic register, multiplication at 16 MHz rate.
Advanced Micro Devices Application Note (4 pg.)

2 **"Overflow Detector in Binary Adders"**
(AM9309)
Discusses the detection of overflow errors using an IC multiplexer.
Advanced Micro Devices (2 pg.)

3 **"AM25S10 Four-Bit Shifter"**
(AM25S10)
Provides functional description and discusses logic equivalents. Applications: up-shift, down and around end shifts, scaling and fixed multiplication.
Advanced Micro Devices Application Note (10 pg.)

4 **"Applications of the TTL/MSI 93S43 4-Bit by 2-Bit Two's Complement Multiplier"**
(93S43)
How to implement a combinatorial multiplication array of any size for two's complement numbers. How to multiply in other number representations. Speed/hardware tradeoffs, normalization of floating point numbers after multiplying, rounding or truncation of double length products.
Fairchild Application, Note 329 (15 pg.)

5 **"MECL 10,000 Arithmetic Elements MC10179, MC10180, MC10181"**
See listing under (Digital) High Speed Logic (Motorola).

6 **"NBCD Sign and Magnitude Adder/Subtracter"**
(MC14560, MC14561)
Describes CMOS parallel adder-subtracters for both signed and unsigned natural binary coded decimal (NBCD) numbers.
Motorola AN-738 (7 pg.)

7 **"High-Speed TTL Adders"**
(DM5483, DM7483)
Describes 16-bit parallel adders, using the DM7283/DM8383, and connections for ripple-carry addition. Also describes BCD adder techniques implemented with these devices. Shows how the devices can be used to improve the performance of MOS storage systems.
National AN-35 (6 pg.)

8 **"Arithmetic Arrays Using Standard COS/MOS Building Blocks"**
(CD4001, CD4008, CD4011, CD4013, CD4019)
Describes design of a 32-bit full adder/arithmetic logic system. Discusses four-bit full adder, quad AND-OR select gate, dual D-type flip-flop, input NAND gates, input NOR gates, and arithmetic register.
RCA ICAN-6600 (6 pg.)

9 **"COS/MOS Rate Multipliers — Versatile Circuits for Synthesizing Digital Functions"**
(CD4089, CD4527)
Describes operation of a rate multiplier, and the effects of cascading. Covers addition, subtraction, multiplication, division, square and higher order roots, frequency ratios and integration. Also discusses symmetric operations.
RCA ICAN-6739 (12 pg.)

10 **"Converting To and From Binary Using the SN74184 and SN74185A"**
(SN74184, SN74185A, SN74283, SN74284, SN74285)
Compares conventional shift and add technique to conversion from binary to BCD using the 74185A. Tells how to interconnect these converter packages for 6-bit through 20-bit binary inputs and 4, 5 or 6 decade BCD inputs. Describes conversion of fractions using the 74283, 74284 and 74285.
Texas Instruments Application Report CA-171 (19 pg.)

11 **"Fast Multipliers Using TTL Read Only Memories"**
See listing under (Memory) ROMs. (Texas Instruments)

CMOS

12 **"Intrinsically Safe Data Acquisition"**
Presents methods by which CMOS circuitry can be used in the construction of intrinsically safe low-level multiplexers, A/Ds, and instrumentation amplifiers.
Burr-Brown AN-84 (4 pg.)

13 **"Minimizing Gate Oxide Failures Due to Handling"**
Describes oxide failure mechanisms, evaluates input protection techniques, and recommends handling procedures to avoid failure.
Harris Application Report 208 (3 pg.)

14 **"CMOS: Some Application Guidelines"**
Presents General Guidelines when using CMOS.
Harris Application Note 209 (7 pg.)

15 **"Using Junction Isolated CMOS"**
Covers problems and application rules related to forward biasing CMOS inputs and outputs.
Harris Application Note 210 (4 pg.)

16 **"Avoiding CMOS Noise-Sensitivity Problems"**
Describes noise sensitivity problems peculiar to MOS technologies and solutions to these problems.
Harris Semiconductor AN-211 (6 pg.)

17 **"CMOS Analog Multiplexers and Switches; Applications, Considerations"**
Covers selection criteria, parameter definitions, handling and design precautions, typical applications, and other topics concerning CMOS analog multiplexers and switches.
Harris Semiconductor AN-520 (9 pg.)

18 **"Getting the Most Out of CMOS Devices for Analog Switching Jobs"**
Describes latch-proof junction isolation, floating-body junction isolation, and dielectric isolation as solutions to CMOS problems when applied to analog design.
Harris Semiconductor AN-521 (7 pg.)

19 **"MasterMOS, a Custom CMOS System"**
(MasterMOS)
Describes the construction of these devices which are customized by changing the metalization pattern.
International Microcircuits (6 pg.)

20 **"MasterMOS Design Manual"**
(MasterMOS)
Detailed instructions and drawing for customizing these arrays.
International Microcircuits $35.00 (70 pg.)

DIGITAL

CMOS (cont)

1 **"A New CMOS Analog Gate Technology"**
See listing under (Linear) Switches. (Intersil)

2 **"NBCD Sign and Magnitude Adder/Subtracter"**
See listing under Arithmetic (Motorola)

3 **"A 3½ Digit DVM Using an Integrated Circuit Dual Ramp System"**
See listing under (Linear) Instrumentation (Motorola)

4 **"Noise Immunity Comparison of CMOS Versus Popular Bipolar Logic Families"**
Compares the noise immunities of TTL, DTL, HTL, and CMOS logic families. Discusses common noise sources, precautions against noise, noise specification, and standard noise tests.
Motorola AN-707 (8 pg.)

5 **"Introduction to CMOS Integrated Circuits with Three-State Outputs"**
Describes a wide variety of CMOS ICs incorporating transmission gates with standard logic. Gives design rules. Covers applications in analog switching and multiplexing, digital multiplexing, and data bussing.
Motorola AN-715 (19 pg.)

6 **"Scanning Logic for RF Scanner-Receivers Using CMOS Integrated Circuits"**
Describes rf scanner-receiver control functions using standard CMOS devices. Covers crystal switching and priority channel monitoring with mention of phase-locked loop designs.
Motorola AN-753 (7 pg.)

7 **"CMOS Monostable Multivibrators"**
(MC14538B)
Covers theory of operation with emphasis on pulse widths, retriggerable and non-retriggerable operation. Describes use in a tachometer.
Motorola AN-772 (7 pg.)

8 **"CMOS Linear Applications"**
(MM74C00, MM74C02, MM74C04)
Describes use of CMOS devices biased to operate at the midpoint of the transfer characteristics.
National AN-83 (3 pg.)

9 **"CMOS Oscillators"**
Describes square wave oscillators that can be built with CMOS logic elements.
National AN-118 (4 pg.)

10 **"54C/74C Family Characteristics"**
(MM54C Series, MM74C Series)
Discusses output, noise and temperature characteristics, power consumption, and propagation delay for the 54C/74C logic family.
National AN-90 (6 pg.)

11 **"MM54C/74C Voltage Translation/Buffering"**
See listing under Interface (National)

12 **"Designing with MM74C908, MM74C918 Dual High Voltage CMOS Drivers"**
(MM74C908, MM74C918)
Presents curves for power dissipation design limits. Shows simple driver circuits plus flasher, oscillator, siren and latch applications.
National AN-177 (12 pg.)

CMOS (cont)

13 **"COS/MOS Integrated Circuits Manual"**
(CD4000 series)
Discusses fabrication, logic system design, and applications of RCA COS/MOS circuits.
RCA CMS-272 $2.50 (224 pg.)

14 **"Noise Immunity of COS/MOS Integrated-Circuit Logic Gates"**
(CD4000A, CD4001A)
Evaluates noise immunity of the CD4000A/01A gates with respect to external noise, crosstalk, transmission-line reflections, power-line noise, and ground-line noise. Includes schematics and logic diagrams.
RCA ICAN-6176 (8 pg.)

15 **"A Typical Data-Gathering & Processing System Using CD4000A-Series COS/MOS Parts"**
(CD4000 Series)
Describes data-gathering and processing system using CMOS circuits. Includes discussion of input signal conditioning and transmission, the digital processor unit, receiver, memory, arithmetic unit, display unit, output buffer, output transmitter, receiver, and control unit.
RCA ICAN-6210 (11 pg.)

16 **"Radiation Resistance of the COS/MOS CD4000A Series"**
(CD4000A Series)
Provides a graph plotting permanent radiation resistance of CD4000A series. Discusses design considerations for increasing resistance.
RCA ICAN-6224 (2 pg.)

17 **"Guide to Better Handling and Operation of CMOS integrated Circuits"**
Recommends specific handling and operating practices to minimize the probability of damage in the manufacturing and field environments.
RCA ICAN-6525 (5 pg.)

18 **"Using the CD4047A in COS/MOS Timing Applications"**
(CD4047)
Compares this monostable-astable multivibrator with simpler types of oscillator circuits and discusses applications, including a noise discriminator, low-pass and band-pass filters, a frequency discriminator, and a pulse generator.
RCA ICAN-6230 (13 pg.)

19 **"Astable and Monostable Oscillators using RCA COS/MOS Digital Integrated Circuits"**
(CD4000 Series)
Describes several techniques used to compensate for the normal threshold variation of MOS devices in the design of stable multivibrator circuits for operation at frequencies up to 1 MHz. Also covers applications for multivibrator circuits including VCOs, voltage controlled pulse-width circuits, and phase-locked VCOs.
RCA ICAN-6267

20 **"A COS/MOS PCM Telemetry and Remote Data Acquisition Design"**
(CD4000 Series)
Describes data transmission formats and the following data acquisition sections: analog and digital multiplexers, A/D converters, transmission formatters and system programmers.
RCA ICAN-6289 (12 pg.)

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DIGITAL

CMOS (cont)

1 **"Power Supplies for COS/MOS"**
(CD4000 Series)
Discusses the factors involved in the selection of CMOS supply voltages including the system operating frequency, noise immunity and power dissipation. Examples of simple power supply circuits are also given.
RCA ICAN-6304 (5 pg.)

2 **"Applications of the RCA-CD4093B COS/MOS Schmitt Trigger"**
(CD4093B)
Describes characteristics of the CD4093 quad 2-input Schmitt trigger. Covers applications in waveshaping (sinewave to square-wave, edge delay, edge detection), power-on reset, astable multivibrators and use as a Schmitt trigger for noise immunity.
RCA ICAN-6346 (6 pg.)

3 **"Using the CD4520B to Design Dividers with Symmetrical Outputs"**
(CD4520B)
Describes how to use this CMOS counter to divide an input frequency by N where N is any integer from 2 to 256 and obtain outputs with approximately 50% duty cycles.
RCA ICAN-6362 (10 pg.)

4 **"Fundamentals of Testing COS/MOS Integrated Circuits"**
Describes the techniques employed in testing CMOS devices to assure their adherence to data sheet specs.
RCA ICAN-6532 (14 pg.)

5 **"Understanding Buffered and Unbuffered CMOS Characteristics"**
Presents the relative merits of buffered and unbuffered CMOS devices. Provides background, definitions, and an applications chart.
RCA ICAN-6558 (8 pg.)

6 **"Radiation Resistance of the COS/MOS CD4000A and CD4000B Series"**
(CD4000 Series)
Studies permanent and transient radiation as they affect CMOS devices.
RCA ICAN-6563 (3 pg.)

7 **"Applications of CD40107BE COS/MOS Dual Buffer"**
(CD40107BE)
Details the characteristics of the CD40107BE and the variety of applications including a lamp driver, an LED driver, and a relay driver.
RCA ICAN-6564

8 **"COS/MOS Electrostatic-Discharge Protection Networks"**
(CD4000 Series)
Discussion and illustrations of the various electrostatic-discharge protection networks provided on RCA CMOS parts.
RCA ICAN-6572 (2 pg.)

9 **"Power-Supply Considerations for COS/MOS Devices"**
(CD4000 Series)
Includes discussion of quiescent device dissipation, switching characteristics, ac dissipation and ac performance characteristics, calculating system power, power supply regulation and filtering requirements.
RCA ICAN-6576 (6 pg.)

CMOS (cont)

10 **"Noise Immunity of COS/MOS B-Series Integrated Circuits"**
(CD4000UB Series, CD4000B Series)
Evaluates noise immunity of B-series CMOS devices with respect to noise-energy immunity, and dc/ac noise-immunity. Includes definitions of test terms, discussion of logic-system noise and rejection, and schematics.
RCA ICAN-6587 (9 pg.)

11 **"Interfacing Analog and Digital Displays with CMOS Integrated Circuits"**
(CD4000 Series)
Details some of the CMOS ICs most suitable for interfacing the electronic circuit and the display. For digital displays, basic display operation is also covered as an aid in selecting the appropriate interfacing device.
RCA ICAN-6595 (12 pg.)

12 **"Interfacing COS/MOS with Other Logic Families"**
(CD4000A Series)
Describes conditions governing interface of CMOS 4000A series with other logic families.
RCA SSD-203 ICAN-6602 (12 pg.)

13 **"Battery-Powered Digital-Display Clock/Timer and Metering Applications Utilizing the RCA CD4026A and CD4033A Decade Counters 7-Segment Output Types"**
(CD4009, CD4010, CD4026, CD4033)
Describes the CD4026A/33A ICs and their use with 7-segment display units. Discusses interface packages and methods to help the designer optimize his system. Includes a discussion of battery-operated systems for digital clocks and watches.
RCA ICAN-6733 (16 pg.)

14 **"CMOS/MOS Interfacing Simplified"**
See listing under (Digtial) Interface (RCA)

15 **"CMOS/MOS Rate Multipliers — Versatile Circuits for Synthesizing Digital Functions"**
See listing under (Digital) Arithmetic (RCA)

16 **"Design of Fixed and Programmable Counters Using the RCA 4018A COS/MOS Presettable Divide-by-"N" Counter"**
See listing under (Digital) Counters. (RCA)

17 **"Application of CD4016A Quad Bilateral Switch"**
See "Transmission and Multiplexing of Analog or Digital Signals Using the CD4016A Quad Bilateral Switch" Under (Digital) Data Transmission. (RCA)

18 **"Using Complementary MOS Circuits"**
(SCL4013A, SCL4046A, SCL4018A, SCL4026A, SCL4029A, SCL4404A)
Reviews CMOS operation, cost, and reliability. Discusses application of the SCL4018A in a three decade rate multiplier; the SCL4029A in counting devices; the SCL4404A and SCL4031A in A/D converters; and SCL4016A in analog switching.
Solid State Scientific AN-101 (6 pg.)

19 **"CMOS Expandable Gates"**
(SCL4402A, SCL4412A)
Compares the transfer characteristics of ordinary CMOS gates to those gates using double buffered output. Includes performance characteristics and discusses expansion of SCL4412A and SCL4402A to 12-input NOR, 16-input OR, and other combinations.
Solid State Scientific AN-102 (3 pg.)

DIGITAL

CMOS (cont)

1 **"CMOS Integrated Circuits in Automotive Applications"**
General discussion, also includes discussion of high current circuits, constant current or constant impedance circuit, digital time delay circuit, digital low-pass filter.
Solid State Scientific AN-103 (5 pg.)

2 **"Interfacing with CMOS"**
Describes electrical characteristics of CMOS inputs and outputs. Discusses interfacing CMOS with CMOS, PMOS, NMOS, DTL/TTL, HTL, and CL.
Solid State Scentific An-104 (5 pg.)

3 **"Improved CMOS Gate Design"**
(SCL4000 Series)
Description of the output buffering of the SCL4000 Series
Solid State Scientific AN-105 (3 pg.)

4 **"A Simplified Approach to Testing CMOS Inverters and Gates"**
Bench tests using a lower supply and a V-O-M are described. They include continuity, input leakage, quiescent device current, output voltage, noise immunity, output drive current and threshold voltage.
Solid State Scientific AN-107 (4 pg.)

5 **"Applications of CMOS Integrated Circuits in Communications Equipment"**
(SCL4000 Series)
Uses of SCL4000 Series circuits as frequency synthesizers, digital frequency displays, frequency scanners, and squelch circuits.
Solid State Scientific AN-108 (4 pg.)

6 **"CMOS Wave Shaping and Level Detection"**
Describes methods to obtain modified transfer charactertistics of double buffered NAND gates, by connecting inputs together, connecting extra inputs to V_{cc}, etc. Shows how to obtain variable amounts of hysteresis, and describes systems of level detection using trigger circuits.
Solid State Scientific AN-109 (5 pg.)

7 **"Using the SCL 4528 Dual Monostable Multivibrator"**
(SCL4528)
Describes operating modes and timing, equations for pulse width calculations.
Solid State Scientific AN-111 (6 pg.)

Consumer

8 **"A Navigation Receiver That Uses A Digital Frequency Synthesizer"**
(μA719)
Gives schematics for a navigation receiver. Discusses the digital frequency synthesizer, varactor tuned RF amplifier, AGC amplifier, mixer, IF amplifier, and detector portions.
Fairchild Application Note 178 (6 pg.)

9 **" 'Little Teacher'. Using the C593/C597 Calculator Circuit"**
(C/CF593, C/CD597)
Describes a calculator circuit used as a teaching toy. If a child answers a given problem correctly a pass lamp is lit; otherwise a fail lamp is lit.
General Instrument Bulletin 0202 (3 pg.)

Consumer (cont)

10 **"12/24 Hour Digital Auto Clock"**
(AY9-1000, CK3300)
Provides circuit diagram and description of a 12 or 24 hour auto clock.
General Instrument Bulletin 0301 (3 pg.)

11 **"Industrial Clock/Timer Featuring Back-up Power Supply Operation"**
Describes the design and operation of a clock timer with digital readout suitable for industrial control applications. CMOS circuits are used for reduced power.
Motorola AN-718A

12 **"Calculator Learns to Keep Time"**
Describes stopwatch and keyboard controlled interval timing functions using the MM5736 calculator chip.
National AN-119 (8 pg.)

13 **"Handheld Calculator Battery Systems"**
Describes the tradeoffs in battery performance for 6.5-9.5v calculators driven by 2, 3 and 4 cell as well as 9v. batteries.
National AN-149 (4 pg.)

14 **"High Voltage Shift Registers Move Displays"**
See listing under (Memory) Shift Registers (National)

15 **"Timekeeping Advances Through COS/MOS Technology"**
Discusses basic oscillator design considerations, practical oscillator circuits, and some typical timing-circuit applications, including wrist watches, wall clocks, and auto clocks.
RCA ICAN-6086 (12 pg.)

16 **"CMOS Integrated Circuits in Automotive Applications"**
See listing under (Digital) CMOS. (Solid State Scientific)

17 **"Automotive Electronics: Choosing the Right Technology"**
Defines operational considerations and compares CMOS, PMOS, and bipolar.
Sprague TP 74-5 (10 pg.)

Counters

18 **"Single IC Forms 2-to-9-Bit Ring Counter"**
(AM2503)
Describes use of device to make a ring counter.
Advanced Micro Devices (2 pg.)

19 **"Design for a Battery Operated Frequency Counter"**
(ICM7207A, ICM7208)
Describes the design, circuit and layout of a 7 digit frequency and period measurement counter.
Intersil A015 (6 pg.)

20 **"Using the MK5009P MOS Counter Time-Base Circuit"**
(MK5009)
Describes the use of the MK5009 along with complete circuits for a digital frequency meter, pulse generator and digitally-programmable one-shot. Discusses operation of the units oscillator circuit.
Mostek AN-104 (4 pg.)

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DIGITAL

Counters (cont)

1 **"Applications Using the MK50395 Six Decade Counter Display Totalizer"**
(MK50395, MK50396, MK50397)
Discusses use of the counter in batch control position measurement, greater-than less-than detection, automatic stop, frequency counter, darkroom timer, digital tuning, and N-Pulser applications.
Mostek (16 pg.)

2 **"Application Information Using Mostek's Six-Decade Counter/Display Totalizer"**
(MK50395)
Covers circuit operation and input/output requirements. Describes use in a batch control system, a position measurement system and greater-than less-than detection.
Mostek (8 pg.)

3 **"Programmable Counters Using the MC10136 and MC10137 MECL Universal Counters"**
(MC10136, MC10137)
Circuit operation and use in programmable counters with no external gating. Also use in high-frequency counters operating up to 110 MHz.
Motorola AN-584 (4 pg.)

4 **"Battery-Powered 5 MHz Frequency Counter"**
Describes a battery operated 5 MHz counter built with CMOS for low power operation. Discusses methods to minimize power consumption.
Motorola AN-717 (9 pg.)

5 **"A 200 MHz Autoranging MECL-McMOS Frequency Counter"**
(MC10000 Series)
Presents basic frequency counter design along with the schematics and diagrams needed to build a 200 MHz autoranging frequency counter.
Motorola AN-742 (11 pg.)

6 **"Five Digit Accumulator/Elapsed Time Indicator"**
(MC14534)
Describes in detail the circuit for a CMOS 5 digit elapsed time indicator and a 99,999 count accumulator with a 1-999 prescaler.
Motorola AN-743 (5 pg.)

7 **"The Logical Design of Shift Counters"**
Presents two techniques to aid in designing shift-register counters. Gives results for "sequence tree" and "count multiplication" techniques for cycle lengths of 30 or less. Shows solutions for both "D" flip-flops and J-K flip-flops as the input elements of the shift register.
Motorola AN-576 (8 pg.)

8 **"An MSI 500 MHz Frequency Counter Using MECL and MTTL"**
See listing under High Speed Logic. (Motorola)

9 **"Calculator Chip Makes A Counter"**
(MM5736, MM5739)
Discusses use of the MM5736 calculator chip as a counter operating up to 120 Hz.
National AN-112 (6 pg.)

10 **"Keyboard Programmable Divide-by-"N" Counter with Symmetrical Output"**
(MM54C922, MM74C922)
Describes a circuit to divide by 1 through 16 by pushing a single key for each division ratio.
National DB-5 (2 pg.)

Counters (cont)

11 **"Design of Fixed and Programmable Counters Using the RCA 4018A COS/MOS Presettable Divide-by-"N" Counter"**
(CD4018)
Describes the use of this device in single-decade and multi-decade fixed and programmable divide-by-"N" counters. System considerations, such as switch simplifications, components minimization, and speed are also discussed.
RCA ICAN-6498 (6 pg.)

12 **"A Basic Selection Guide to Digital Counters"**
(CD4017, CD4024, CD4518)
Discusses the advantages of the binary ripple counter and compares it with the Johnson decade counter and the BCD counter. Also covers selection of the most suitable counter for specific applications.
RCA ICAN-6552 (6 pg.)

13 **"Using the SN74160 Family of Synchronous Counters"**
(SN74160, SN74161, SN74162, SN74163)
Describes carry circuit operation, cascading and programming.
Texas Instruments Application Report CA-174 (7 pg.)

Data Transmission

14 **"Line Drivers and Receivers"**
(AM2614, AM2615, 9614, 9615, 9620, 9621, DM7831, DM8831)
Discusses single ended, differential, unbalanced differential digital communications systems and line matching methods. Describes the above circuits and their use in systems.
Advanced Micro Devices Application Note (12 pg.)

15 **"Remote Multiplexing"**
Discusses acquisition of data at sensors distant from the location where the data is required and the control of actuators at a distance from the control system. Topics include interconnection, data transmission integrity, temperature, and electrical and mechanical protection.
Burr Brown AN-80 (6 pg.)

16 **"Distributed Data Processing"**
Outlines design considerations dealing with remote data acquisition systems. Discusses distributed data processing and related topics such as system reliability, maintenance, network configurations and partitioning, and data base management.
Burr Brown AN-81 (5 pg.)

17 **"Intrinsically Safe Data Acquisition"**
See listing under (Digital) CMOS. (Burr-Brown)

18 **"Stable FSK Modems Featuring the XR-2207, XR-2206, and XR-2211"**
(XR2206, XR2207, XR2211)
Describes designing a modulator-demodulator for use in frequency-shift keying. Circuit designs and the adjustment procedure for frequency tuning is included.
Exar AN-01 (5 pg.)

19 **"Tri-State FSK Modem Design Using XR2206/XR2211"**
(XR2206, XR2211)
Design of FSK modems with carrier detection and control capability are discussed.
Exar AN-05

Data Transmission (cont)

1 **"Using the Data Concentrator in Data Communications"**
(AY5-1016)
Presents description of device and outlines general operating considerations. Provides schematics of its use in a commutator/decommutator, a polling system, and a digitally programmed gain amplifier.
General Instruments Bulletin 0801 (8 pg.)

2 **"Using the UAR/T in Data Communications"**
Describes device and operation of both receiver and transmitter portions of circuit. Outlines use in computer interfacing, terminal interfacing, and a location identifier.
General Instruments Bulletin 0802 (6 pg.)

3 **"The UAR/T in Data Communications"**
(AY5-1013)
Describes this full duplex receiver/transmitter and discusses its application in computer, terminal and slow speed device interfacing. Also covers use in polling.
General Instrument Microelectronics (4 pg.)

4 **"Using the Data Concentrator in Data Communications"**
(AY5-1016)
Describes counter, decoding matrix, and multiplexer switch sections of the AY5-1016 data concentrator. Describes commutator.decommutator and polling system applications plus use as a digitally programmable gain amplifier, and as a clock generator.
General Instrument Microelectronics (11 pg.)

5 **"The AY-5-1011 Terminal Transmitter for Key-To-Tape Data Accumulation System and Other Applications"**
(AY5-1011)
Describes features of this parallel-to-serial converter and discusses its use in key-to-tape systems.
General Instruments Microelectronics (6 pg.)

6 **"High Speed Digital Communications"**
(HD245, HD246, HD545, HD546)
Describes the use of the HD-245 family in a current mode digital communication system (up to 2 Mbs over 1,000-ft-long line.)
Harris Application Note 205 (4 pg.)

7 **"Receiver/Transmitter Noise Immunity"**
(HD245, HD246, HD545, HD546)
Discusses HD-245 transmitter/receiver system noise: External magnetic and capacitive effects, crosstalk, and ground line noise. Includes a comparison with voltage mode and differential voltage switching type systems.
Harris Application Note 207 (4 pg.)

8 **"Using the 8251 Universal Synchronous/Asynchronous Receiver/Transmitter"**
(8251)
Describes this USART, covering its use as a component and as a communication-link in 8080 systems. Includes flowcharts and program listings.
Intel Application Note AP-16 $1.00 (32 pg.)

9 **"Using the 8273 SDLC/HDLC Protocol Controller"**
(8273)
Explains the 8273 as a component and shows its use in a generalized loop configuration.
Intel AP-36 (44 pg.)

Data Transmission (cont)

10 **"Bussing with MECL 10,000 Integrated Circuits"**
(MC10111, MC10123)
Describes use of MECL 10,000 circuits in high speed data transmission systems with emphasis on transmission line construction and termination.
Motorola AN-726 (6 pg.)

11 **"Low Speed Modem Fundamentals"**
(MC6860)
Describes interface circuitry and performance of the MC6860 low speed modem. Evaluation of the system performance in the presence of Gaussian noise is given, as well as a brief description of data couplers.
Motorola AN-731 (15 pg.)

12 **"Low Speed Modem System Design Using the MC6860"**
(MC6860)
Describes the MC6860 modem. Provides filter design tables and equations to develop a complete 100 series compatible system.
Motorola AN-747 (13 pg.)

13 **"Device Operation and System Implementation of the Asynchronous Communications Interface Adapter"**
(MC6850)
Provides information on ACIA transmitter and receiver operation, initialization, status register bits, use in a microcomputer based communications system, software requirements, and transmission subroutines.
Motorola AN-754 (11 pg.)

14 **"Revised Data — Interface Standards"**
(MC3486, MC3487, MC3488)
Compares RS232, RS422, and RS423 standards and discusses cable length.
Motorola AN-781 (4 pg.)

15 **"Integrated Circuits for Digital Data Transmission"**
(DS7820, DS7830, DS8820, DS8830)
Describes the operation and use of the DS7830 line driver and DS7830 line receiver for transmission systems using twisted-pair lines. Includes a mathematical design analysis of this line receiver.
National AN-22 (16 pg.)

16 **"Data Bus and Differential Line Drivers and Receivers"**
(DS7820, DS7830, DS7831, DS7832, DS7833, DS7834, DS7835, DS7836, DS7837, DS7838, DS7839, DS8820, DS8830, DS8831, DS8832, DS8833, DS8834, DS8835, DS8836, DS8837, DS8838, DS8839, DS1488, DS1489)
Includes schematics and describes the operation of these line drivers, receivers and transceivers.
National AN-83 (12 pg.)

17 **"Transmission Line Characteristics"**
(DM7400, DS7820, DS7830, DS75452, DS8820, DS8830)
Describes the characteristics of digital signals in transmission lines and the characteristics of the line that effect transmission quality. Also compares the performance of unbalanced and balanced circuits in digital systems.
National AN-108 (6 pg.)

18 **"Operational Aspects of Nitron's Data Terminal Transmitter and Receiver"**
(NC2257, NC2259, NC2260)
Discusses basic operation of the NC2257/2259/2260 IC's, and application in various types of communications systems.
Nitron Communications Note 1 (24 pg.)

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Data Transmission (cont)

1 **"Using High Speed Memory in Pulse Code Modulated Systems for Switching Applications"**
Discusses digital message switching and implementation with a conventional digital crossbar switch as well as with a switch using high speed memory and data multiplexing.
Nortec Applications Note. No. 29 (4 pg.)

2 **"Transmission and Multiplexing of Analog or Digital Signals Utilizing the CD4016A Quad Bilateral Switch"**
(CD4016A)
Describes features and operation of this switch. Discusses applications, including switching, gating digital or analog signals, multiplexing and demultiplexing, D/A conversion, sample and hold, and squelch-control.
RCA ICAN-6601 (12 pg.)

3 **"A COS/MOS PCM Telemetry and Remote Data Acquisition Design"**
See listing under (Digital) CMOS (RCA)

4 **"A Typical Data-Gathering and Processing System Using CD4000A-Series COS/MOS Parts"**
See listing under (Digital) CMOS (RCA)

5 **"Asynchronous Receiver/Transmitter"**
(TR1602)
General description of asynchronous transmission and operation of TR1602, which is capable of full or half duplex operation. Describes application in distributed computer networks.
Western Digital Application Report 1 (12 pg.)

Encoders

6 **"Using the AY-5-9100 in Telephone Equipment"**
(AY5-9100)
Describes use of this four phase dynamic logic circuit in mains powered dialers, line powered telephones, card readers, and in standard multifrequency tone dialer keyboards.
General Instrument Microelectronics (10 pg.)

7 **"Keyboard Encoder and PROM/EPROM Application"**
(AY5-3600)
Describes use of the device in 64 key 4 mode and 90 key 4 mode applications. The device's binary outputs are organized to provide direct interface with a PROM/EPROM thus enabling the specific pattern format to be verified prior to a "custom" encoder commitment.
General Instrument Bulletin 1401 (4 pg.)

8 **"AY5-3600 Keyboard Encoder Operation"**
(AY5-3600)
Characterizes the device and supplies a chart of the code assignments it uses.
General Instrument Bulletin 1402 (3 pg.)

9 **"Designing with the HD-0165 Keyboard Encoder"**
(HD0165)
The organization and truth table for this encoder are presented. The use of two circuits for encoding up to 256 keys, battery operation, examples of a teletypewriter keyboard and universal keyboard encoders are described.
Harris Application Note 204 (8 pg.)

Encoders (cont)

10 **"Using the MM5704 Keyboard Interface in Keyboard Systems"**
(MM5704)
Discusses features, operation, and programming of this device. Discusses use with the MM5702 timing and control chip of the Microprogrammable Arithmetic Processing System, and in a standard ASCII encode system.
National AN-52 (11 pg.)

11 **"MOS Encoder Plus PROM Yield Quick Turnaround Keyboard Systems"**
(MM5740)
Describes use of a binary coded keyboard encoder with a PROM to build prototype or small volume keyboard systems.
National AN-139 (4 pg.)

12 **"Exclusive-OR Code Converters"**
(DM7086)
Covers use of exclusive-OR gates to do Gray/Binary and Binary/Hamming code conversion.
National DB-2 (2 pg.)

13 **"Interface Circuitry and Performance Optimization TMX2141 Encoder, TMX2151 Decoder"**
(2141, 2151)
Provides design notes including pulse width and timing considerations for these pulse width signaling devices.
TMX Bulletin 751 (7 pg.)

General

14 **"Don't Be Confused by Switching Time Specifications"**
Uses a TTL J-K flip-flop to explain switching time specifications.
Advanced Micro Devices (4 pg.)

15 **"HMOS Reliability"**
Describes HMOS technology and device operation. Presents failure mechanisms, reliability testing, and test results.
Intel RR-18 (9 pg.)

16 **"Worst Case Design For Integrated Circuits"**
(MONOCHIP)
Discusses defining worse case conditions of an IC design parameter variations, breadboarding for verification of worse case conditions and parasitic effects.
Interdesign APN-2 (5 pg.)

17 **"How Cost Effective Are Custom IC's?"**
(MONOCHIP)
Looks at the relative economies of discrete circuit designs versus semicustom IC's at various volume levels. Economic costs often not analyzed such as rework, supervisory overhead, inventory maintenance, quality assurance, and purchasing and stocking costs are included.
Interdesign APN-5 (6 pg.)

18 **"MOS 100-Bit Word Generator"**
Describes how to build a 100-bit word generator using MOS ICs.
National MB-1 (2 pg.)

19 **"MOS Clock Savers"**
Design and use of MOS Clock-Drive Networks. Offers tips for saving power and lowering component costs.
National MB-5 (2 pg.)

DIGITAL

General (cont)

1 **"Solid-State Devices Manual"**
Provides tutorial information on discrete devices and IC's with emphasis on consumer, hobbyist and experimenter applications.
RCA SC-16 $5.00 (750 pg.)

2 **"Criteria for Choosing Resins and Evaluation Tests for Discrete and Integrated Power Devices in Plastic Packages"**
See listing under (Linear) General (SGS-ATES)

High Speed Logic

3 **"F10,000 Series ECL"**
(ECL Series)
Operation and circuit parameters are described for the Fairchild ECL series.
Fairchild Application Note 330 (6 pg.)

4 **"IC Crystal Controlled Oscillators"**
(MC1023, MC1662, MC10101, MC10116)
Describes use of MC1023 OR/NOR gate as an amplifier and oscillator. Discusses square wave oscillator circuits with crystal control capable of output frequencies up to 150 MHz. Examples use MC10116/10101, and MC1662.
Motorola AN-417B (4 pg.)

5 **"The MC1600 Series MECL III Gates"**
(MC1660, MC1661, MC1662, MC1663, MC1664, MC1665)
Gives typical operating characteristics and explains the operation of various gates in the MECL III family. Describes recommended layout, breadboarding, and testing procedures.
Motorola AN-504 (14 pg.)

6 **"Interconnection Techniques for Motorola's MECL 10,000 Series Emitter Coupled Logic"**
(MECL)
Describes some of the characteristics of high digital signal lines and gives wiring rules for MECL 10,000 circuits. Discusses p-c board interconnects, board-to-board interconnects, and wirewrapping techniques.
Motorola AN-556 (22 pg.)

7 **"Using Shift Registers as Pulse Delay Networks"**
(MC10135)
Discusses a high-speed delay shift register using the MC10135 flip flop.
Motorola AN-565 (3 pg.)

8 **"MECL Positive and Negative Logic"**
(MECL)
Describes equivalences between positive and negative ECL logic and provides guides for converting between them.
Motorola AN-567 (2 pg.)

9 **"Testing MECL 10,000 Integrated Logic Circuits"**
(MECL)
Describes AC and DC tests in a 50 ohm transmission-line environment for measuring logic levels or noise margins, circuit current, input currents, propagation delays, edge speeds, and flip-flop toggle rates.
Motorola AN-579 (6 pg.)

High Speed Logic (cont)

10 **"An MSI 500 MHz Frequency Counter Using MECL and MTTL"**
(MECL)
Describes design of 8-digit LED readout counter using MECL III, 10,000 and TTL. Discusses two prescalers using MECL, two input amplifier designs, and a time-base controller for the counter's multiphase clock.
Motorola AN-581 (9 pg.)

11 **"Measure Frequency and Propagation Delay with High Speed MECL Circuits"**
(MECL)
Describes ECL frequency counter useful to 160 MHz and a propagation delay measuring circuit capable of 100-picosecond resolution.
Motorola AN-586 (2 pg.)

12 **"AC Noise Immunity of MECL 10,000 Integrated Circuits"**
(MECL)
Discusses AC noise immunity. Describes test circuits for measuring this immunity and the results to be expected for MECL 10,000 circuits.
Motorola AN-592 (6 pg.)

13 **"Simulate MECL System Interconnections with a Computer Program"**
Develops a basic computer program that allows the user to simulate the performance of signal lines and to analyze termination techniques. Applies to ECL and other high speed digital systems.
Motorola AN-700 (10 pg.)

14 **"Understanding MECL 10,000 DC and AC Data Sheet Specifications"**
(MECL)
Discusses basic MECL 10,000 gate structure, transfer curve and dc levels. Covers specifications data sheet, including power supply drain current, high and low output voltages, propagation delay, rise and fall times, and toggle frequency.
Motorola AN-701 (7 pg.)

15 **"MECL 10,000 Arithmetic Elements MC10179, MC10180, MC10181"**
(MC10179, MC10180, MC10181)
Describes 10180 dual adder/subtractor, 1018 4-bit arithmetic logic unit/function generator, and 10179 lookahead carry block. Discusses their operation in parallel adders, in both ripple and lookahead systems.
Motorola AN-709 (11 pg.)

16 **"Interfacing with MECL 10,000 Integrated Circuits"**
(MC1650, MC1692, MC10115, MC10116, MC10124, MC10125, MC10128, MC10129, MC10216)
Discusses circuits to interface ECL with TTL, TTL and IBM busses, MOS, low level signals, and LEDs.
Motorola AN-720 (9 pg.)

17 **"A High Speed FIFO Memory Using the MECL MC1143 Register File"**
(MCM10143)
Describes the required features of a high speed FIFO design. Different approaches are compared and a design is shown using the MC10143 Multiport Register File.
Motorola AN-730 (6 pg.)

18 **"Bussing with MECL 10,000 Integrated Circuits"**
See listing under (Digital) Data Transmission (Motorola)

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High Speed TTL

1 "The MC3000/MC3100 Series Transistor-Transistor Logic Flip-Flops"
(MC3050, MC3051, MC3052, MC3060, MC3061, MC3062, MC3150, MC3151, MC3152, MC3160, MC3162)
Describes basic operation of the various flip-flops available in the MC3000/3100 (54H/79H) series and gives typical operating characteristics of each.
Motorola AN-493 (14 pg.)

2 "Series 54S/74S Schottky TTL Applications"
(SN54S Series, SN74S Series)
Analyzes Schottky clamping techniques and circuits, reviews circuit performance, including discussion of transfer characteristics, switching times, and a-c noise. Discusses power supply considerations, line driving and receiving, noise sources and their abatement. Normalized loading/driving capability information and the pinouts of ICs are discussed.
Texas Instruments Application Report CA-176 (45 pg.)

HNIL/HTL

3 "Noise Immunity with Motorola High Threshold Logic"
(MC660 Series)
Compares noise immunity characteristics between High Threshold Logic (HTL) and standard saturated logic devices. Discusses noise injection and noise reduction techniques.
Motorola AN-298 (5 pg.)

4 "Operation and Application of MHTL I/C Flip-Flops"
(MC663, MC664)
Describes operation and characteristics of the J-K MC663P and the master-slave R-S MC664P flip-flops. Discusses applications as ripple and decade shift counters.
Motorola AN-414 (8 pg.)

5 "Using Motorola High Threshold Logic"
(MC660 Series)
Describes MC660 series ICs and provides many of the characteristics of these units. Application examples include logic translation, line driving, and trigger circuits.
Motorola AN-467 (11 pg.)

6 "Converting Relay Control Systems to Digital I/C's"
(MC660 Series)
Defines and discusses basic Boolean algebra and logic functions and presents method of converting relay diagrams to logic diagrams. Gives examples of conversion method using High Threshold Logic circuits and presents a system design to accomplish this.
Motorola AN-524 (11 pg.)

7 "Design Techniques with HiNIL 367 Quad Schmitt Trigger"
(367)
General discussion of Schmitt Trigger and the differences of the 367, which ignores open inputs and offers 3.5v noise immunity. Applications include line receivers, pulse stretchers, ac detectors, free-running and voltage-controlled oscillators.
Teledyne Semiconductor HiNIL Application, Note 2, (4 pg.)

8 "HiNIL 375 Universal Shift Register"
(375)
Operation and applications of this synchronous 4-bit device as a 4 and 8-bit shift-left, shift-right register, 7 and 8-bit parallel-to-serial and serial-to-parallel converters and various counters.
Teledyne Semiconductor HiNIL Application Note 4 (10 pg.)

HNIL/HTL (cont)

9 "High Noise Immunity Logic — Powerful, Versatile, and Growing"
(300 Series)
Generally describes the HiNIL family use and features. Covers interface to other families, noise immunity, operating considerations and input protection.
Teledyne Semiconductor Digital Application Note 5 (5 pg.)

10 "The HiNIL 347-A Dual Retriggerable One Shot with High Noise Immunity"
(347)
Description and application details for this device are provided along with diagrams showing its use in pulse generators, coincidence detectors, frequency dividers, voltage to frequency and frequency to voltage converters, a pulse absence detector and an ac line presence detector.
Teledyne Semiconductor Digital Application Note 6 (6 pg.)

11 "High Noise Immunity Logic"
(300 Series)
Discussion includes noise immunity, loading rules, fanout, passive pull-up loading, collector or-ing, second level gating, driver pull-up, system interfaces.
Teledyne Semiconductor Digital Catalog (7 pg.)

12 "Combining HNIL and CMOS — An Optimum Design Technique"
See listing under (Digital) Interface (Teledyne Semiconductor)

I^2L

13 "Custom IC Design Using I^2L Technology"
(XR-IIL-CHIP)
Compares I^2L to other technologies. Describes design procedure for linear and digital circuits using master chips.
Exar (5 pg.)

14 "Monolithic I^2L Test Circuit Using XR-C409"
(XR-C409)
A monolithic test circuit has been developed for evaluation of speed and performance capabilities of Exar's (I^2L) technology. This test circuit, designated the XR-C409, is intended to familiarize the I^2L user and the system designer with some of the performance features of I^2L such as its frequency capability and power-speed tradeoffs.
Exar AN-17

Interface

See also Decoders.

15 "Digital Display Systems"
Discusses decoding, format, multiplexing, zero suppression for LED, LCD, incandescent, fluorescent and gas discharge displays.
Fairchild Application Note 212/2 (24 pg.)

16 "9616/9617 EIA Interface Driver and Receiver"
(9616, 9617)
Gives performance characteristics for these devices and describes their use in data communications equipment. Describes EIA standard RS232-C.
Fairchild Application Note 320 (6 pg.)

DIGITAL

Interface (cont)

1 "The Interface Handbook, Line Drivers and Receivers"
(9612, 9613, 9614, 9615, 9616, 9617, 9627, 9634, 9635, 9636, 9637, 9638, 9640, 8T13, 8T14, 8T23, 8T24, 55107, 55108, 55109, 55110, 55121, 55122, 75107, 75108, 75109, 75110, 75112, 75121, 75122, 75123, 75124, 75154, 75207, 75208)
This comprehensive book covers the basics of transmission line theory along with methods for determining signal quality. Major chapters are titled: Data Transmission Lines and their Characteristics; Reflections, Computations and Waveforms; Long Transmission Lines and Data Signal Quality; and Forms of Operation (single/differential, direction of flow, analysis of common interfaces, etc.)
Fairchild Interface Handbook (118 pg.)

2 "ASCII Bus Interface Logic Uses IM5200 FPLA"
(IM5200)
Explains ASCII interface bus and how IM5200 provides discrete logic and address storage required by it.
Intersil Application Bulletin MB002 (6 pg.)

3 "Semiconductors for Plated-Wire Memories"
(MC4006, MC4007, MC4038, MC4040, MC4043, MC1514, MC1546)
Discusses operation and electrical characteristics of plated wire memories. Covers applications of drivers, sense amplifiers, and decoders as interface circuits. Also discusses memory organization and memory-related semiconductor applications.
Motorola AN-533 (15 pg.)

4 "Interface Techniques Between Industrial Logic and Power Devices"
Presents worst case design approaches to illustrate methods of interfacing McMOS and MHTL logic to various ac and dc power load levels.
Motorola AN-712A (19 pg.)

5 "Interface Considerations for Numeric Display Systems"
(MC14511, MC14543)
Gives basic information on LCD, LED, gas discharge, fluorescent and incandescent displays. Discusses interfacing 7 segment displays to logic with emphasis on multiplexed systems.
Motorola AN-741 (25 pg.)

6 "Interfacing with MECL 10,000 Integrated Circuits"
See listing under (Digital) High Speed Logic (Motorola)

7 "MM54C/MM74C Voltage Translation/Buffering"
(MM54C901, MM54C902, MM54C903, MM54C904, MM74C901, MM74C902, MM74C903, MM774C904)
Interfacing PMOS to CMOS, CMOS to CMOS with different voltage levels, and CMOS to two standard TTL loads, are illustrated using 74C901 series devices.
National MB-18 (2 pg.)

8 "Driving 7-Segment LED Displays with National Semiconductor Circuits"
(DM5446A, DM5447A, DM5448A, DM7446A, DM7447A, DS75491, DS75492, DS7856, DS7858, DS8856, DS8857, DS8858, DS8861, DS8863, DS8864, DS8865, DS8866)
Discusses configurations and construction of 7-segment LEDs and drive modes. Describes BCD to 7-segment decoder drivers, BCD to 7-segment LED drivers, MOS to LED segment drivers, four and five segment drivers, as well as digit drivers. Describes calculator and digital clock applications.
National AN-99 (12 pg.)

9 "Using the MM5704 Keyboard Interface in Keyboard Systems"
See listing under (Digital) Encoders (National)

Interface (cont)

10 "TTL/MOS/DTL Interfaces"
Techniques for coupling the above devices and characteristics of the interfaces.
National MB-7 (2 pg.)

11 "COS/MOS Interfacing Simplified"
(CD4000 Series)
Covers interfacing 4000A and B series with TTL, DTL, ECL, NMOS, PMOS, industrial and power control circuits, op amps and displays.
RCA ICAN-6315 (7 pg.)

12 "Applications of the RCA CD4093B COS/MOS Schmitt Trigger"
See listing under (Digital) CMOS (RCA)

13 "Interfacing COS/MOS with Other Logic Families"
See listing under (Digital) CMOS (RCA)

14 "Interfacing with CMOS"
See listing under (Digital) CMOS (Solid State Scientific)

15 "Completely Monolithic IC Series for Gas Discharge Display Interface"
(UDN-6144, UDN-6164, UDN-6184, UDN-7183, UDN-7184, UDN-7186)
Describes operation of high voltage IC's to drive the digits and segments of 200v (Panaplex) gas discharge displays.
Sprague Electric Microcircuit Application Report MAR75-1 (8 pg.)

16 "Expanding the Frontiers of IC Interface for Electronic Displays"
Presents interface IC basics concerning incandescent, gas discharge, LED, plasma, fluorescent, and hot wire displays.
Sprague Electric (10 pg.)

17 "Using Bipolar Logic to Improve Performance in CMOS and Microprocessor Systems"
Suggests the use of HiNIL for improving noise performance, input protection, and output drive, and of LP Schottky for improved speed/power.
Teledyne Semiconductor Digital Application Note 7 (4 pg.)

18 "Combining HNIL and CMOS — An Optimum Design Technique"
(300 Series)
Discusses noise immunity, HNIL/74C interface, Schmitt trigger input and high current output.
Teledyne Semiconductor Digital Catalog (3 pg.)

19 "TTL to MOS and MOS to TTL Interface Circuits"
(SN7400, SN75107, SN75207, SN75270, SN75370, SN75450, SN75451, TMS1103, TMS4062)
Describes MOS/TTL interface circuits using bipolar transistors, JFETs, MOSFETs, and ICs.
Texas Instruments Application Report CA-170 (11 pg.)

LSI, General

20 "Semi-Custom LSI Design with I^2L Gate Arrays Using XR300 and XR500"
A design approach to developing complex LSI systems using the devices is described.
Exar AN-16

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LSI, General (cont)

1 **"Design of Custom LSI Circuitry for Modern Digital Systems"**
Discusses design of LSI devices. Covers size considerations, numbers of input/output connections, number of output drivers, use of repetitive patterns, use of computer aided design techniques, speed versus size and power, and interfacing.
General Instrument Microelectronics (7 pg.)

Multiplexers

2 **"TTL MSI Multiplexers and Demultiplexers"**
(DM7210, DM7842, DM8210, DM8842)
Describes features of DM7210 multiplexer and DM7842 demultiplexer and discusses their use in a synchronous digital data transmission system, a keyboard entry decoder, and as minterm generators.
National AN-37 (8 pg.)

PLAs

3 **"How to Design with Programmable Logic Arrays"**
(DM8575, DM8576)
Discusses operation of PLAs and use as code converters, decode elements in digital processors and sequential controllers.
National AN-89 (8 pg.)

4 **"Single Chip Multiprocessor Arbiter"**
Shows how the Field Programmable Logic Sequencer (FPLS) can use state logic to implement a multiprocessor arbiter conveniently and cost effectively.
Signetics (4 pg.)

5 **"FPLA Adds Display Flexibility to CRT Controllers"**
(6845)
Describes how field programmable logic arrays can adapt the 6845 CRT controller to display different foreign formats.
Signetics (6 pg.)

6 **"Field Programmable Logic Arrays — An Application Manual"**
Covers basic FPLA operation and describes various applications, including a data cartridge tape drive controller, an op-code decoder for the PDP-11, and a combination sync and video generator.
Signetics (116 pg.)

7 **"MOS Programmable Logic Arrays"**
(TMS2000 Series, TMS2200 Series)
Describes TMS2000 and TMS2200 Series programmable logic arrays. Describes their internal logic and operations. Provides ordering instructions.
Texas Instruments Application Report CA-158 (13 pg.)

Pulse Handling

8 **"Nanosecond Pulse Handling Techniques in I/C Interconnections"**
Discusses problems of pulse transmission and measurement for TEM mode on coax, stripline, and above-ground wire systems.
Motorola AN-270 (6 pg.)

Trigger Circuits

9 **"Advantages of the AM26123 Compared with the AM54/74123"**
(AM26123, SN54123, SN74123)
Discusses changes in the pulse width circuits and the addition of on output latch.
Advanced Micro Devices Application Brief (4 pg.)

10 **"CMOS Schmitt Triggers"**
(MC14093B, MC14583B, MC14584B)
Operating characteristics, theory of operation, and Schmitt trigger applications are covered for digital logic systems.
Motorola AN-768 (8 pg.)

11 **"1.3 Volt IC Flasher, Oscillator, Trigger, or Alarm"**
See listing under (Linear) Timers (National)

12 **"Series ULN-3300M Schmitt Trigger Integrated Circuits — Typical Applications and Operation"**
(ULN-3303, ULN-3304, ULN-3305, ULN-3306)
Describes device and use in multivibrators, switches, timers, and more.
Sprague AN-27450.19

13 **"CMOS Schmitt Trigger — a Uniquely Versatile Design Component"**
(MM54C14, MM74C14)
Analyzes CMOS Schmitt triggers and outlines applications including a light activated switch, an RC oscillator, and a pulse stretcher. Also outlines the benefits of hysteresis.
National AN-140 (6 pg.)

14 **"Designing with SN54/SN74LS123"**
(SN54LS123, SN74LS123)
Describes use of this multivibrator in various applications including a missing pulse detector, a low pulse generator, and a pulse width detector.
Texas Instruments Application Report CA-196 (11 pg.)

TTL, General

15 **"Medium Scale Integration in the Numerical Control Field"**
(MC4016, MC4018, MC4024, MC4044, MC4324, MC4344)
Discusses operation of MC4016 decade programmable cascadeable counter, MC4324/4024 dual voltage controlled multivibrator, and MC4344/4044 frequency phase detector. Describes applications of these devices in audio frequency comparator, frequency synthesizer, and motor speed control circuits.
Motorola AN-541 (10 pg.)

16 **"TTL Integrated Circuits — Applications of MSI Devices"**
Covers counters, modulo-N dividers, decoders, switches, adders, comparators, parity generators, shift registers and bus-ORable flip-flop. Describes many applications, including up/down counters, a stepping waveform generator, shift registers, frequency synthesizers, digital data demultiplexer, analog commutator, minterm generator, ripple carry parallel adder and tape position locator.
National AN-36 (23 pg.)

17 **"Tri-State Logic in Modular Systems"**
(DS7831, DM8093, DM8094, DM8214, DM8230, DM8551, DM8552, DM8598, DS8831, DM8840, DM8842, DM8846)
Discusses output drive characteristics, logical control, safety factors in Tri-State Logic circuits. Describes applications, including complex switching functions, driving and transmitting, multiplexing, data storage, decoding, and data manipulation.
National AN-43 (16 pg.)

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TTL, General (cont)

1 **"Characteristics and Applications of Tri-State IC's"**
(DM7093, DM7490, DM7214, DM7230, DM7551, DM7598, DS7831, DS8831)
Describes application of the general configuration of the Tri-State logic family and discusses application of the following: quad bus-buffer gates, dual 4:1 multiplexer, demultiplexer and bus-interchange switch, quad-D flip-flop, expandable 256-bit ROM, and quad driver.
National AN-45 (12 pg.)

2 **"Tri-State Logic in High Speed Memories of Microprogrammed Computers"**
(DM8551)
Discusses tri-state logic in general and its use in scratchpad memories. Covers storage of microinstructions and program constants in high-speed ROMs.
National AN-47 (5 pg.)

3 **"Tri-State Logic Applied in a Computer System Can Reduce System Cost and Provide Added Performance"**
(DM8556)
Analyzes Tri-State characteristics using the DM8556 counter/register as an example. Shows how performance of PDP-8 can be improved using TSL.
National AN-73 (7 pg.)

LINEAR

Active Filters

4 **"Function Circuits, Design and Applications"**
See listing under (Linear) General (Burr-Brown)

5 **"Active Filter Design with IC OP Amps"**
(XR3403, XR4136, XR4202, XR4558)
Provides table of transfer functions and equations for low, high and bandpass filters as well as filter responses for Bessel, Butterworth and Chebychev types. Working schematic of an active filter in a modem application included.
Exar AN-03 (8 pg.)

6 **"Designing Active Filters with Universal Filter Building Blocks"**
(ACF7032, ACF7092)
Provides users with the data necessary to design filters with low pass, high pass, and band reject magnitude frequency responses using the device. Contains basic theory as well as table of parameters.
General Instrument Bulletin 0703 (8 pg.)

7 **"The Effect of Operational Amplifier Performance Limitations on State-Variable Active Filters"**
(ACF7092)
Derives simplified expressions which predict second-order effects for a state-variable filter. For verification, the formula is applied to a commercially available hybrid IC active filter.
General Instrument Bulletin 0704 (4 pg.)

8 **"Design of a Hybrid Integrated Circuit Elliptic Active RC Filter"**
Discusses design details and experimental results obtained in building hybrid IC sharp rolloff filters.
General Instrument Bulletin 0705 (4 pg.)

9 **"High Q Notch Filter"**
(LM102, LM202, LM302)
Describes use of LM102 connected to a twin "T" network to form a high Q, 60 Hz notch filter.
National Linear Applications Handbook, Vol. I LB-5 (2 pg.)

Amplifiers, Current

10 **"Application of the LH0002 Current Amplifier"**
(LH0002)
Circuit operation. Describes uses in a differential input-output op amp, booster amplifier, level shifter, pulse transformer driver, and transmission line driver.
National AN-13 (4 pg.)

Amplifiers, Instrumentation

11 **"AD520 Monolithic Instrumentation Amplifier"**
(AD520)
Describes performance of this instrumentation amplifier. Covers application as a bridge amplifier, ground loop eliminator, and floating measurement amp. Appendix compares instrumentations amplifier to several multiple op amp circuits.
Analog Devices (6 pg.)

12 **"A User's Guide to IC Instrumentation Amplifiers"**
(AD522)
Explains where and when an instrumentation amplifier may best be employed. Provides basic theory, specifications and examples of use.
Analog Devices (12 pg.)

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Amplifiers, Instrumentation (cont)

1 **"Instrumentation Amplifiers — Versatile Differential Input Gain Blocks"**
(3660, 3670)
Describes the features and general operation of instrumentation amplifiers. Depicts their use in bridge circuits, in reducing ground loop interference, and in driven guard input circuits.
Burr-Brown AN-75 (6 pg.)

2 **"Optical Coupling Extends Isolation-Amplifier Utility"**
(3450, 3650)
Explains isolation amplifier fundamentals, optical coupling, and use of the amp in medical electronics and industrial motor control.
Burr-Brown AN-85 (8 pg.)

3 **"Instrumentational Amplifiers"**
(LM114, LM118)
Discusses general purpose instrumentation amplifier, using LM114 matched transistors ahead of an LM118 op amp that is optimized for wide bandwidth.
National Linear Application Handbook, Vol. II, LB-21 (2 pg.)

4 **"Instrumentation Amplifier"**
(LM101A, LM102, LM107)
Describes a differential-input instrumentation amplifier using LM102 and LM107 and variable gain version that also uses LM101A.
National Linear Applications Handbook, Vol. I LB-2 (2 pg.)

5 **"OP-10 Instrumentation Amplifier CMRR Versus Frequency Improvement"**
(OP-10)
Discusses optimization of CMRR versus frequency response of a three op amp instrumentation amplifier.
Precision Monolithics AB-2 (1 pg.)

6 **"Application of the RCA CA3000 Integrated-Circuit DC Amplifier"**
(CA3000)
Describes circuit and application as modulated oscillator, crystal oscillator, low-frequency mixer, cascaded RC-coupled feedback amp, narrow-band tuned amp, and Schmitt trigger.
RCA ICAN-5030 (11 pg.)

7 **"The Instrumentation Amp vs the Op Amp: Which, Where, and How to Use Them"**
Compares an op amp connected as a differential amp with an instrumentation amp built from several general purpose op amps. Discusses how to put each one together, and when and where to use them.
Teledyne Philbrick AN-29 (6 pg.)

Amplifiers, Operational

8 **"An IC Amplifier User's Guide to Decoupling, Grounding, and Making Things Go Right for a Change"**
Contains considerable information on good grounding practices and op amp decoupling.
Analog Devices Application Note (8 pg.)

9 **"Applying the AD504 Precision IC Operational Amplifier"**
(AD504)
Describes this amplifier and offers notes on its noise, thermal and dynamic performance. Applications: instrumentation amplifier, stable reference regulator, instrument input amplifier and high gain ac amplifier.
Analog Devices Technical Bulletin (7 pg.)

Amplifiers, Operational (cont)

10 **"Protect Op Amps from Overloads"**
Discusses protection from power-supply faults, keeping input voltages at safe levels, and limiting output currents.
Burr-Brown AN-60 (3 pg.)

11 **"Combine Two Op Amps to Avoid the Speed Accuracy Compromise"**
(3521)
Discusses interconnecting low drift and wideband op amps to form a composite op amp.
Burr-Brown AN-64 (2 pg.)

12 **"Check Five Op Amp Specs in One Test"**
Describes a test circuit that generates signals providing measurements of open loop gain, offset voltage, input bias current, quiescent current, and output voltage swing.
Burr-Brown AN-65 (1 pg.)

13 **"Using Op Amps in Low Noise Applications"**
Discusses shot noise and noise from source resistances.
Burr-Brown AN-68 (2 pg.)

14 **"Design of a Unique Precision Controlled Current Source"**
(3500)
Diagrams a current source using an op amp and a complementary FET pair to form a current source with differential input and bipolar current output.
Burr-Brown AN-74 (2 pg.)

15 **"Designing with Operational Amplifiers: Application Alternatives"**
Amplifier improvement techniques, signal analyzers, signal conditioners, absolute value circuits, signal generators, computing circuits, data transmission circuits, as well as test and measurement circuits are discussed. Circuit designs and explanations of circuit operation are provided.
Burr-Brown $17.50 (220 pg.)

16 **"Operational Amplifiers — Design and Application"**
Covers basic theory, amplifier design techniques and applications.
Burr-Brown $24.50 (470 pg.)

17 **"Applications of Operational Amplifiers"**
Presents op amp applications including designs for signed controls, processors, waveform generators, and special purpose circuits. Provides information on error sources, circuit values, and design equations.
Burr-Brown $19.50 (220 pg.)

18 **"Frequency Compensation Techniques for an Integrated Operational Amplifier"**
(μA702A)
Presents design techniques for frequency compensation of μA702A which are applicable to other IC operational amplifiers.
Fairchild Application Bulletin 117/2 (8 pg.)

19 **"The μA739 — A Low-Noise Dual Operational Amplifier"**
(μA739)
Describes the circuit and operating characteristics. Covers d-c circuit performance, low-frequency analysis, power consumption, noise, short-circuit protection, amplifier isolation, and compensation techniques.
Fairchild Application Note 175/1 (8 pg.)

Amplifiers, Operational (cont)

1 **"The μA776, an Operational Amplifier with Programmable Gain, Bandwidth, Slew-Rate, and Power Dissipation"**
(μA776)
Describes methods for setting the master bias current, discusses amplifier frequency response as a function of this current. Discusses applications, including a 600 nanowatt amplifier, a low-cost sample and hold circuit, a current controlled oscillator, multiplexing, and phase shifting.
Fairchild Application Note 218 (5 pg.)

2 **"A Low Drift, Low Noise Monolithic Operational Amplifier for Low Level Signal Processing"**
(μA725)
Describes operation of μA725, which offers low offset drifts, low input currents, low noise performance, and massive open loop gain. Shows how to minimize offset voltage drift with temperature in IC operational amplifiers and how to improve the common-mode rejection.
Fairchild Application Note 277 (10 pg.)

3 **"The μA715 — A Versatile High Speed Operational Amplifier"**
(μA715)
Describes application as an image orthicon head amplifier, general purpose video amplifier, 40dB high input impedance amplifier, and high speed sample and hold circuit.
Fairchild Application Note 265 (4 pg.)

4 **"Applications of the μA749 Dual Operational Amplifier"**
(μA749)
Describes applications as a dual level comparator, positive or negative peak detector, peak-to-peak detector, and as an offset null circuit.
Fairchild Application Note 268 (2 pg.)

5 **"The μA749 Dual Operational Amplifier"**
(μA749)
Discusses the circuit, input voltage range, latch-up, output voltage range, power dissipation, noise, separation, high frequency compensation, and output capability.
Fairchild Application Note 269 (8 pg.)

6 **"Applications of the μA741 Operational Amplifier"**
(μA741)
Describes applications of this amplifier as a unity gain voltage follower, integrator, differentiator, voltage regulator reference amplifier, high voltage regulated power supply control element, clipping amplifier, and a comparator.
Fairchild Application Note 289/1 (4 pg.)

7 **"An Improved Sample and Hold Circuit Using the μA740"**
(μA740)
Basic discussion of acquisition and hold times. Description of circuit using this op amp as the buffer amplifier.
Fairchild Application Note 297 (3 pg.)

8 **"Applications of the μA777"**
(μA777)
Discusses use of this operational amplifier as a pulse amplifier, Wein Bridge oscillator, variable gain differential amplifier, power amplifier.
Fairchild Application Note 300 (3 pg.)

9 **"Radiation Testing of Linear Microcircuits"**
See listing under (Linear) General (Fairchild)

Amplifiers, Operational (cont)

10 **"Operational Amplifiers as Inductors"**
(μA777)
Includes derivation of equivalent circuit and necessary component values to obtain inductances from millihenries to kilohenries, using the μA777 as an example. Describes application in voltage controlled sinewave oscillators and in bandpass and notch filters.
Fairchild Application Note 321 (5 pg.)

11 **"Applications of the Gated Linear Amplifier ZN424"**
(ZN424)
Details the operation of the ZN424 and describes a variety of specific applications including filters, comparators, and peak hold circuits.
Ferranti (46 pg.)

12 **"HA-909 Operational Amplifier"**
(HA-909, HA-911)
Discusses applications as a unity gain breadboard op amp, servo preamplifier, high-Q bandpass filter, Wien bridge oscillator, and phase-delay filters.
Harris Application Note 501 (2 pg.)

13 **"HA-909 Operational Amplifiers Performance Tailoring"**
(HA-909, HA-911)
Discusses how to optimize HA-909's offset, power dissipation, bandwidth, large signal bandwidth, slew rate, transient response, and stability with reactive loads.
Harris Application Note 502 (3 pg.)

14 **"A High Impedance Hysteresis Circuit"**
(HA-2520, HA-2620)
Describes HA-2520/HA-2620 used as a hysteresis amplifier and covers output voltage limiting.
Harris Application Note 505 (2 pg.)

15 **"Test Procedures for Operational Amplifiers"**
Circuit for measuring offset voltage, bias current, offset current, open loop voltage gain, common mode and power supply rejection ratios, output voltage/current, power dissipation, and making continuity checks.
Harris Application Note 508 (2 pg.)

16 **"A Simple Comparator Using the HA-2620"**
(HA-2620)
Describes op amp comparator circuit capable of driving approximately ten logic gates.
Harris Application Note 509 (1 pg.)

17 **"A Simple Square-Triangle Waveform Generator"**
(HA-2510, HA-2600, HA-2620)
Circuit for waveform generator using three op amps.
Harris Application Note 510 (2 pg.)

18 **"The HA-2400 PRAM Four Channel Operational Amplifier"**
(HA-2400, HA-2405)
This is a programmable input stage, operational amplifier. This note describes its applications including an analog multiplexer with buffered input and output, an inverting or non inverting amplifier with a programmable gain, a sine wave oscillator with programmable frequency, and a track and hold/sample and hold circuit.
Harris Application Note 514 (8 pg.)

19 **"Operational Amplifier Stability: Input Capacitance Considerations"**
(HA-2600, HA-2605)
Discusses overcoming stray capacitance in op amps, such as the HA-2600.
Harris Application Note 515 (2 pg.)

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Amplifiers, Operational (cont)

1 **"The HA-2530/2535 Wideband High Slew Inverting Amplifier"**
(HA-2530, HA-2535)
Briefly discusses internal circuit. Shows how closed-loop frequency response can be predicted. Describes application as a fast settling coaxial driver, a 10 MHz coaxial line driver, a wide range signal separator, a high frequency triangular wave generator, and a current-to-voltage converter.
Harris Application Note 516 (11 pg.)

2 **"Applications of a Monolithic Sample-and-Hold/Gated Operational Amplifier"**
(HA-2420, HA-2425)
Describes HA-2420/2425 circuit. Applications include various track-and-hold/sample-and-hold configurations, an A/D converter, a demultiplexer, an integrated-hold-reset amplifier, a gated operational amplifier, and a peak detector with reset.
Harris Application Note 517 (8 pg.)

3 **"The HA-2900 Monolithic Chopper Stabilized Amplifier"**
(HA-2900)
Discusses offset voltage and current drift and chopper stabilization, then describes the circuit. Applications include a high impedance differential instrumentation amplifier, use as an integrator, and several wide bandwidth configurations.
Harris Application Note 518 (8 pg.)

4 **"Operational Amplifier Noise Prediction"**
Provides a noise model, a procedure for computing output noise, and spot noise curves for many Harris amplifiers.
Harris Semiconductor AN-519 (10 pg.)

5 **"Precision Op Amp on a Semicustom Chip"**
(MONOCHIP)
Discusses building an op amp on a semicustom chip with performance comparable to standard precision units. Covers all phases of design and thermal considerations as well.
Interdesign APN-9 (10 pg.)

6 **"The 8007 — A High Performance FET-Input Operational Amplifier"**
(ICL8007)
Circuit description, applications as log and antilog amplifiers, photocell amplifier, peak detector, sample and hold circuits, high impedance buffer, and Wien Bridge oscillator.
Intersil Application Bulletin A005 (6 pg.)

7 **"The 8043 — A Low Cost Dual FET-Input Operational Amplifier"**
(ICL8043)
Summary of circuit characteristics. Applications as automatic offset suppression circuit, staircase generation, sample and hold circuit, and instrumentation amplifier.
Intersil application Bulletin A008 (6 pg.)

8 **"Power Op-Amp Heat Sink Kit"**
(ICH8510, ICH8520, ICH8530)
Discusses mounting the devices on heat sinks.
Intersil Application Bulletin A029 (2 pg.)

9 **"Getting More Value Out of an Integrated Operational Amplifier Data Sheet"**
Discusses the open loop characteristics of operational amplifiers and their relation to overall circuit operation. Defines parameters and describes their significance with respect to closed loop considerations as well.
Motorola AN-273A (10 pg.)

Amplifiers, Operational (cont)

10 **"D.C. Servo Motor Systems Using the ICH8510"**
See listing under (Linear) Amplifiers, Power (Intersil)

11 **"The MC1535 Monolithic Dual Operational Amplifier"**
(MC1435, MC1535)
Gives complete ac and dc circuit analysis and discusses electrical characteristics. Discusses applications in a differential input-differential output circuit configuration, and as a signal envelope detector. Describes an input compensation scheme for fast slew rate.
Motorola AN-41 (9 pg.)

12 **"The MC1539 Operational Amplifier and its Applications"**
(MC1439, MC1539)
Discusses dc and ac operation and the performance of this amplifier. Describes a high frequency feed-forward scheme and application as a comparator, voltage follower, differential amplifier, and a summing amplifier.
Motorola AN-439 (22 pg.)

13 **"The MC1556 Operational Amplifier and its Applications"**
(MC1456, MC1556)
Gives characteristics and describes operation. Discusses application as a voltage follower, high impedance bridge amplifier, and a logarithmic amplifier.
Motorola AN-522 (8 pg.)

14 **"Analysis and Design of the Op/Amp Current Source"**
Develops expressions for the transfer function and output impedance of voltage controlled op amp current source using both ideal and non-ideal models. Discusses effects of parameter and temperature variations on performance.
Motorola AN-587 (7 pg.)

15 **"Drift Compensation Techniques for Integrated DC Amplifiers"**
Op amp bias current and offset voltage compensation are discussed. Current compensation techniques for high impedance levels and methods to achieve chopper-stabilized drift performance at low impedance levels are covered.
National Linear Applications Handbook, Vol. I, AN-3 (4 pg.)

16 **"Monolithic Operational Amplifiers — The Universal Linear Component"**
(LM101, LM102)
Applications of the LM101 and, in some cases, the LM102, include free-running multivibrator, level shifting amplifier, voltage comparator, servo preamplifier, and computing circuits. Frequency compensation techniques are discussed in detail.
National Linear Applications Handbook, Vol. I, AN-4 (10 pg.)

17 **"Low Power Operational LH0001 Amplifier"**
(LH0001)
Operation of circuit offering 0.2 mv typical offset voltage at 25°C and quiescent supply currents in 100 μA range.
National Linear Applications Handbook, Vol. I, AN-10 (4 pg.)

18 **"Noise Specs Confusing?"**
Explanation of terms and factors contributing to noise, calculation of noise figure and signal to noise ratio. Gives points on selecting low noise amplifiers.
National AN-104 (8 pg.)

19 **"An Applications Guide for Operational Amplifiers"**
(LH101, LH201, LM101, LM201, LM301)
Discusses application of operational amplifiers, grouping them in five categories: simple amplifiers, operational circuits, transducer amplifiers, wave shapers and generators, and power supplies.
National AN-20 (12 pg.)

LINEAR

Amplifiers, Operational (cont)

1 "A Simplified Test Set for Operational Amplifier Characterization"
(LM101, LM201, LM301, LM709)
Gives a functional description of set that allows quantitative characterization of the dc operational amplifier parameters for the LM101 and LM709. Discusses the circuit, includes construction information, and gives a layout for the tester circuit boards.
National AN-24 (12 pg.)

2 "IC Op Amp Beats FETs on Input Current"
(LM108, LM208, LM308)
Describes LM108 operation and performance. Applications: sample and hold circuit, integrator, sine wave oscillator, capacitance multiplier, instrumentation amplifier, logarithmic converter, transducer amplifier, current source and voltage comparator. Discusses PC board construction.
National Linear Applications Handbook, Vol. I, AN-29 (20 pg.)

3 "Logarithmic Converters"
(LM101A, LM102, LM108)
Describes log generators, anti-log generators, cube generators, and multiplier/dividers, using the LM101A and LM108 op amps.
National Linear Applications Handbook, Vol. I, AN-30 (4 pg.)

4 "Op Amp Circuit Collection"
(LM101A, LM102, LM107, LM108)
Gives schematics only for some 90 circuits using one or more of the following operational amplifiers: LM101A, LM102, LM107, LM108. Includes basic, signal generation and signal processing circuits.
National Linear Applications Handbook, Vol. I, AN-31 (20 pg.)

5 "New Design Techniques for FET Op Amps"
(LH0022, LH0022C, LH0042C, LH0052, LH0052C)
Gives parameters for LH0022, LH0042 and LH0052 operational amplifiers. Discusses rationale for FETs in these devices, describes the circuits. Describes application as voltage followers, integrators, sample/hold amplifiers, comparators, instrumentation and charge amplifiers.
National Linear Applications Handbook, Vol. I, AN-63 (12 pg.)

6 "Micropower Circuits Using the LM4250 Programmable Op Amp"
(LM4250, LM4250C)
Describes LM4250 circuit and bias current setting procedure. Applications: 500 nano-watt amplifier, micro-power comparator meter amplifier, pulse generator, instrumentation amplifier and a 5v regulator for CMOS logic circuits.
National AN-71 (8 pg.)

7 "The LM3900 — A New Current-Differencing Quad of ±Input Amplifiers"
(LM3900)
Describes Norton "current mirror" circuit. Emphasizes the amplifiers' application in circuits for single power supply systems. Discusses use in ac and dc amplifiers, voltage regulators, RC active filters, waveform generators, phase locked loops, and voltage controlled oscillators.
Also covers designing digital and switching circuits, and special applications, including tachometers, squaring amplifiers, positive feedback oscillators, line operated audio amplifiers, and power circuits.
National AN-72 (39 pg.)

Amplifiers, Operational (cont)

8 "Applications for a High Speed FET Input Op Amp"
(LH0062, LH0062C)
Describes circuit, performance, compensation techniques for LH0062. Discusses applications in high speed sample and hold circuit, high speed peak detector, programmable integrator, and wide band ac voltmeter. Covers heat sinking, guarding, and bootstrapping.
National AN-75 (4 pg.)

9 "Use the LM158/LM358 Dual, Single Supply Op Amp"
(LM158, LM258, LM358)
Proposes using this dual op amp with a single supply in place of the MC1458/MC1558 with a split supply.
National AN-116 (4 pg.)

10 "LM143 Monolithic High Voltage Operational Amplifier Applications"
(LM143, LM243, LM343)
Describes circuit. High voltage applications: 130v p-p drive, ±34 CMV instrumentation amplifier, high compliance current source. Current boosted applications: 100 ma, 1 amp, high compliance. 90 W audio amplifier. High voltage power supplies. Also application tips.
National AN-127 (12 pg.)

11 "A Linear Multiple Gain-Controlled Amplifier"
Discusses gain control with FETs in the feedback path of an operational amplifier. Considers remote or multichannel gain control, volume expansion, and volume compression/limiting as possible applications.
National AN-129 (8 pg.)

12 "A Linear Multiple Gain Controlled Amplifier"
Portrays a linear control function with over three decades of gain achieved with a FET in the feedback path of a non-inverting amplifier. Gain control with FETs, distortion, bandwidth, and the control time constant are other subjects touched upon.
National FET Databook (8 pg.)

13 "Binary/BCD Gain Programmed Amplifiers"
Illustrates construction of a gain programmed amplifier using an FET quad current mode switch, 4 binary weighted resistors, and an op amp.
National FET Databook (3 pg.)

14 "The Monolithic Op Amp: A Tutorial Study"
Detailed paper on the design of IC operational amplifiers.
National Linear Applications Handbook, Vol. II (18 pg.)

15 "Feedforward Compensation Speeds Op Amp"
(LM101A, LM201A, LM301A)
Compares standard frequency compensation with feedforward frequency compensation of LM101A. Charts open loop response for both compensation networks. Shows fast integrator circuit.
National Linear Applications Handbook, Vol. I, LB-2 (2 pg.)

16 "Fast Compensation Extends Power Bandwidth"
(LM101A, LM201A, LM301A)
Describes frequency compensation technique that extends power bandwidth of LM101A for non-inverting gains of unity to ten and also reduces gain error at moderate frequencies.
National Linear Applications Handbook, Vol. I, LB-4 (2 pg.)

17 "Precision AC/DC Converters"
(LM101A, LM201A, LM301A)
Describes the use of the LM101A in a circuit for eliminating diode threshold potential, use as a precision clamp, as a fast half wave rectifier, and precision AC to DC converter.
National Linear Applications Handbook, Vol. I, LB-8 (2 pg.)

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Amplifiers, Operational (cont)

1 **"Universal Balancing Techniques"**
Describes offset voltage adjustment: for inverting amplifiers using less than 10 K source resistance or using any type of feedback element, for non-inverting amplifiers, for voltage followers, and for differential amplifiers.
National Linear Applications Handbook, Vol. I, LB-9 (2 pg.)

2 **"Speed Up the LM108 with Feedforward Compensation"**
(LM108, LM208, LM308)
Describes simple feedforward network for use with LM108 to achieve a factor of five improvement in speed.
National Linear Applications Handbook, Vol. I, LB-14 (2 pg.)

3 **"Easily Tuned Sine Wave Oscillators"**
(LM101A, LM111, LM201A, LM211, LM301A, LM311)
Describes a circuit using the LM101A and LM111 that provides both a sine and square wave output for frequencies for below 20 Hz to above 20 KHz. Also describes low distortion sine wave oscillator using two LM101As.
National Linear Applications Handbook, Vol. I, LB-16 (2 pg.)

4 **"Predicting Op Amp Slew Rate Limited Response"**
Discusses slew rate limiting and gives curves for sine wave and step voltage response.
National Linear Applications Handbook, Vol. I, LB-19 (2 pg.)

5 **"Low Drift Amplifiers"**
(LM121, LM725, LM741, LM308)
Discusses problems causing drift in amplifiers and recommends solutions. Includes discussion of thermal and electrical shielding, resistor choice, circuit layout, and offset balancing.
National Linear Application Handbook, Vol. II, LB-22 (2 pg.)

6 **"True RMS Detector"**
Describes circuit using operational amplifiers that provide dc output equal to rms value of input with 2% accuracy for a 20 $V_{p\text{-}p}$ input signal from 50 Hz to 100 kHz.
National Linear Applications Handbook, Vol. II, LB-25 (2 pg.)

7 **"Low Current Ammeter"**
(LM216A)
Depicts construction of an ammeter using the LM216A op amp.
National LB-37 (2 pg.)

8 **"Specifying Selected Op Amps and Comparators"**
See listing under (Linear) Comparators (National)

9 **"IC Preamp Challenges Choppers On Drift"**
See listing under (Linear) Pre-amplifiers (National)

10 **"Digital Nulling of OP-05 and SSS725"**
(DAC-08, OP-05, SSS725)
Shows digitally controlled offset nulling achieved by imbalancing the first stage collector currents of the op amp with a D/A.
Precision Monolithics AB-3 (1 pg.)

11 **"Simple Precision Millivolt Reference Uses No Zeners"**
(OP-05)
Describes −3.5 mv to 3.5 mv reference built with instrumentation op amp and a potentiometer.
Precision Monolithics AN-10 (1 pg.)

Amplifiers, Operational (cont)

12 **"The OP-07 Ultra-Low Offset Voltage Op Amp — A Bipolar Op Amp that Challenges Choppers, Eliminates Nulling"**
(OP-07)
Describes circuit design, compares performance to other devices. Covers application in a voltage reference, a high accuracy buffer, a D/A test system, a composite summing amplifier, an absolute value circuit, an analog computer building block, and as a thermocouple amplifier.
Precision Monolithics AN-13 (12 pg.)

13 **"Minimization of Noise in Operational Amplifier Applications"**
(OP-07)
Describes internal and external sources of noise. Helps to locate noise sources by frequency. Gives examples of noise calculation using the OP-07 as an example.
Precision Monolithics AN-15 (11 pg.)

14 **"The OP-17, OP-16, OP-15 as Output Amplifiers for High Speed D/A Converters"**
(DAC-08, DAC-20, DAC-76, OP-15, OP-16, OP-17)
Illustrates design of high speed, voltage output D/A converters using these devices. Circuit diagrams for high speed, low drift, and low power applications are provided.
Precision Monolithics AN-24 (3 pg.)

15 **"Applications of the RCA CA3048 Integrated Circuit Amplifier Array"**
(CA3048)
Discusses operating parameters for this 4-amplifier array and covers applications, including Hartley and Colpitts oscillators, an astable multivibrator, four-channel linear mix, and a gain-controlled amplifier.
RCA ICAN-4072 (8 pg.)

16 **"Application of the RCA CA3008 and CA3010 Integrated-Circuit Operational Amplifiers"**
(CA3008, CA3010)
Describes operating characteristics of two op amps and their application in video amplifiers, frequency-shaping amplifiers, comparators, integrators, differentiators, scaling adders. Also covers the addition of a power output stage and/or input emitter followers.
RCA ICAN-5015 (15 pg.)

17 **"Application of the RCA CA3015 and CA3016 Integrated-Circuit Operational Amplifiers"**
(CA3015, CA3016)
Describes operating characteristics at ±12 v. Applications covered are: 50-dB amplifier; twin-T bandpass amplifier, 20-dB, 10 MHz bandpass amplifier; and voltage follower.
RCA ICAN-5213 (6 pg.)

18 **"Application of RCA CA3033 and CA3033A High Performance Integrated-Circuit Operational Amplifiers"**
(CA3033, CA3033A)
Describes the basic circuit and operation. Covers application as a 250 mw, power amplifier and shows use in a DVM as a multivibrator, staircase generator, and comparator.
RCA ICAN-5641 (8 pg.)

19 **"Applications of the CA3080 and CA3080A High-Performance Operational Transconductance Amplifiers"**
(CA3090, CA3080A)
This device has an additional control terminal for flexibility. Circuit operation is discussed. Applications covered: communications and industrial systems, modulators, multiplexers, sample and hold circuits, gain control circuits, and micropower comparators. Appendix discusses current mirrors.
RCA ICAN-6668 (16 pg.)

Amplifiers, Operational (cont)

1 **"Measurement of Burst (Popcorn) Noise in Linear Integrated Circuits"**
Discusses "pass-fail" criteria and describes a test set-up for measuring burst noise. The set-up includes a high grain amplifier-filter, a bipolar comparator, and a counter-latch-timer control circuit.
RCA ICAN 6732 (8 pg.)

2 **"L144 Programmable Micro-Power Triple Op Amp"**
(L144)
Describes device function, elements of programming, effects of slew rate limiting. Applications discussed include instrumentation amplifier, tone detectors, triple-amplifier active filters, and a micropower double-ended limit detector.
Siliconix AN73-6 (6 pg.)

3 **"Operational Amplifier Parameter Definition and Measurement Guide"**
Defines parameters and means of measuring them.
Teledyne Philbrick AN-23 (8 pg.)

4 **"Logarithmic Amplifiers and Operators Parameter Definition and Measurement"**
Defines and explains logarithmic amplifier parameters.
Teledyne Philbrick AN-27 (3 pg.)

5 **"The Instrumentation Amp vs the Op Amp: Which, Where, and How to Use Them"**
See listing under (Linear) Amplifiers, Instrumentation (Teledyne Philbrick)

6 **"Designing with TL080 BIFET Op Amps"**
(TL080, TL081, TL082, TL083, TL084)
Presents data sheet information, performance characteristics, and various applications including an IC preamplifier, a positive feedback bandpass filter, and a quadrature oscillator.
Texas Instruments CA-193 (11 pg.)

Amplifiers, Power

7 **"D.C. Servo Motor Systems Using the ICH8510"**
(ICH8510)
Explains servo systems in general and use of the device for velocity control, position control, and torque control in particular.
Intersil Application Bulletin A026 (4 pg.)

8 **"Power D/A Converters Using the IH8510"**
See listing under (Linear) Converters (Intersil)

9 **"The MC1554 One-Watt Monolithic Integrated Circuit Power Amplifier"**
(MC1554)
Describes the circuit, including dc characteristics, frequency response, and distortion. Shows how to calculate package power dissipation using the curves on the data sheet. Describes application, as one watt non-inverting, inverting, pulse power, and three-watt differential output amplifiers.
Motorola AN-401 (7 pg.)

10 **"Audio Handbook"**
See listing under (Linear) Consumer, Audio (National)

11 **"LM380 Power Audio Amplifier"**
See listing under (Linear) Consumer, Audio (National)

Amplifiers, Power (cont)

12 **"LM377, LM378, LM379 Dual Two, Four, and Six Watt Power Amplifiers"**
(LM377, LM378, LM379)
Discusses operation, choice and use of these circuits in audio applications. Covers distortion and heat dissipation. Also covers use in a bridge configuration, plus use as a Wein bridge power oscillator, motor drive, power comparator, relay and lamp driver.
National AN-125 (11 pg.)

13 **"Application of the RCA CA3020 and CA3020A Integrated Circuit Multi-Purpose, Wide-Band Power Amplifiers"**
(CA3020, CA3020A)
Circuit description and operation. Both circuits operate from single supply voltage as low as +3 v, offer voltage gains over 60 dB with a 3 dB bandwidth of 8 MHz. Discussion of audio, broadband and video amplifier, video line driver, motor controller and servo amp applications.
RCA ICAN-5766 (8 pg.)

14 **"TBA820 Two-Watt Monolithic Audio Amplifier"**
(TBA820)
Lists main electrical characteristics of device and presents typical applications.
SGS-ATES Technical Note 114 (11 pg.)

15 **"TCA940 Fully Protected Audio Amplifier"**
(TCA940)
Presents temperature and output short circuit protection features of the device along with a description of its performance. Illustrates use of the device in a stereo amplifier and an equalized amplifier for magnetic pickups.
SGS-ATES Technical Note 119 (15 pg.)

16 **"TBA810S/AS Thermally Protected Power Amplifier"**
(TBA810)
Description of the device followed by discussion of its performance. Also shows examples of use in tone control, TV, radio and tape playback channel applications.
SGS-ATES Technical Note 120 (16 pg.)

17 **"TCA830S-Thermally Protected Audio Power Amplifier"**
(TCA830S)
Briefly describes how the device functions followed by an examination of performance under different supply and load conditions. Portable AM/FM receiver, intercom, and magnetic tape player circuits are shown.
SGS-ATES Technical Note 126 (15 pg.)

18 **"TDA2020/TDA2010 HI-FI Monolithic Amplifiers"**
(TDA2020, TDA2010)
Describes these power amplifiers and how to apply them.
SGS-ATES Technical Note 130 (12 pg.)

Amplifiers, RF

19 **"An Integrated Circuit AGC IF Amplifier"**
(μA757)
Describes circuit and performance of μA757, which is recommended for applications in military and industrial equipment, also speech compressor amplifiers.
Fairchild Application Note 204 (4 pg.)

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Amplifiers, RF (cont)

1 **"A High Gain Integrated Circuit RF-IF Amplifier with Wide Range AGC"**
(MC1590G)
Describes operation and Y parameters of the MC1590G. Applications include mixer plus IF, video, single and two-stage RF amplifiers.
Motorola AN-513 (10 pg.)

2 **"A Two-Stage 1kW Solid-State Linear Amplifier"**
Discusses the design of 50W and 300W linear amplifiers for the 1.6 to 30 MHz frequency band.
Motorola AN-758 (16 pg.)

3 **"Linear Amplifiers for Mobile Operation"**
Discusses the design of a portable amplifier suitable for amateur radio applications.
Motorola AN-762 (8 pg.)

4 **"A Complete Monolithic AM/FM/SSB IF Strip"**
See listing under (Linear) Consumer, AM/FM (National)

5 **"Applications of the LM173/LM273/LM373"**
(LM173, LM273, LM373)
Discusses FM, AM, and SSB operation of this multi-mode IF amplifier/detector.
National Linear Applications Handbook, Vol. I, LB-13 (2 pg.)

6 **"Tuned Circuit Design Using Monolithic RF/IF Amplifiers"**
(LM171, LM703)
Discusses operating parameters for the LM171 and LM703 in emitter-coupled and cascode configurations. Brief description of 10.7 MHz emitter-coupled stage and 100 MHz cascode amplifier.
National Linear Applications Handbook, Vol. I, AN-6 (6 pg.)

7 **"Logarithmic IF Strips Using Monolithic Integrated Circuits"**
(SL521)
Describes operation of this log amplifier in successive detection type IF strips with center frequencies from 10 to 100 MHz. Covers broadband and narrow band circuits and describes in detail a 60 MHz wide-range logarithmic amplifier.
Plessey Semiconductor Technical Communication (3 pg.)

8 **"Logging IF Strip"**
(SL1521)
Describes a logging IF strip using Plessey IC's.
Plessey Semiconductor (2 pg.)

9 **"Application of the RCA CA3004, CA3005, and CA3006 Integrated-Circuit RF Amplifiers"**
(CA3004, CA3005, CA3006)
Discusses operating modes, Y parameters, noise performance, video amp capabilities, gain control, cross modulation and modulation distortion. Covers application as single-ended RF amplifier, tuned IF amplifier, mixer, suppressed-carrier modulator and product detector.
RCA ICAN-5022 (26 pg.)

10 **"Application of the RCA CA3002 Integrated-Circuit IF Amplifier"**
(CA3002)
Describes circuit, operating modes, characteristics, and application as an envelope detector, product detector, and a Schmitt trigger.
RCA ICAN-5036 (9 pg.)

Amplifiers, RF (cont)

11 **"Application of the RCA CA3028A and CA3028B Integrated-Circuit RF Amplifiers in the HF and VHF Ranges"**
(CA3028A, CA3028B)
Describes circuits and operating modes. Covers use as an RF amp, autodyne converter, IF amp, and limiter.
RCA ICAN-5337 (10 pg.)

12 **"Application of the RCA CA3021, CA3022, and CA3023 Integrated-Circuit Wideband Amplifiers"**
(CA3021, CA3022, CA3023)
Describes circuit and operating characteristics. Covers video, 10 MHz IF, 455 KHz IF, 28 MHz two-stage limiter, and 500 kHz limiting amplifier applications.
RCA ICAN-5338 (12 pg.)

Amplifiers, Sense

13 **"Semiconductors for Plated-Wire Memories"**
See listing under (Digital) Interface (Motorola)

14 **"An Integrated Sense Amplifier for Core Memories"**
(MC1440, MC1540)
Discusses core memories and design considerations for a sense amplifier. Establishes performance and environment specs for amplifier design, analyzes design of MC1540, and discusses measured performance.
Motorola AN-245A (7 pg.)

Amplifiers, Video

15 **"A Wide Band Monolithic Video Amplifier"**
(MC1552G, MC1553G)
Describes basic operation of the MC1552G and MC1553G, and the characteristics obtained as a function of the devices' operating modes. Applications: pulse amplifier, summing/scaling amplifier, oscillator, and tuned amplifier.
Motorola AN-404 (13 pg.)

16 **"Using the MC1545, A Monolithic Gated Video Amplifier"**
(MC1445, MC1545)
Describes ac and dc operations and discusses applications as a video switch, amplitude modulator, balanced modulator, pulse amplifier, frequency shift keyer and wideband differential amplifier.
Motorola AN-475 (7 pg.)

17 **"Gated Video Amplifier Applications — The MC1545"**
(MC1445, MC1545)
Reviews basic operation and discusses applications, including several modulators, gated multivibrators, gated oscillators and FSK systems. Also discusses AGC, single supply operations, and temperature compensation of the active gate.
Motorola AN-491 (15 pg.)

18 **"Television Video IF Amplifier Using Integrated Circuits"**
See listing under (Linear) Consumer, TV (Motorola)

19 **"Application of the RCA CA3001 Integrated-Circuit Video Amplifier"**
(CA3001)
Describes circuit and operating characteristics. Covers cascaded stages and use as a Schmitt trigger.
RCA ICAN-5038 (9 pg.)

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Amplifiers, Video (cont)

1 **"The SG1401 Video Amplifier"**
(SP1401)
Discussion of fixed and variable gain. The high frequency stability is discussed to aid in optimizing the various configurations for this device.
Silicon General Linear IC Product Guide (2 pg.)

Arrays

2 **"Using the SL362C Low Noise Transistor Pair"**
(SL362)
Provides general data on noise performance plus application in DC to 200 MHz amplifier.
Plessey Semiconductor Technical Communication (4 pg.)

3 **"Application of the RCA CA3018 Integrated Circuit Transistor Array"**
(CA3018)
Array of two isolated silicon epitaxial transistors plus two transistors with emitter-base common connections, suited for closely matched device requirements or interconnections with non-integrable components. Applicationes covered include IF-RF, video, AGC, audio and dc amplifiers.
RCA ICAN-5296 (5 pg.)

4 **"Application of the RCA CA3019 Integrated-Circuit Diode Array"**
(CA3019)
Describes circuit configuration, operating characteristics and applications, including balanced modulator, high-speed gates, balanced mixer, and a ring modulator.
RCA ICAN-5299 (6 pg.)

5 **"Designing with an IC Transistor Array Containing Matched Super-Beta Transistors"**
(CA3095)
Describes CA3095 IC array. Applications: low frequency amplifier, low noise video amplifier, long-delay monostable multivibrator, low-input-bias current comparator, analog timer for long delays, high input impedance dc-voltmeter circuit, and tape-head preamplifier.
RCA ICAN-6222 (9 pg.)

6 **"Monolithic Darlington Arrays Reduce Interface Cost and Complexity"**
(ULN-2001A, ULN-2002A, ULN-2003A)
Discusses packaging and heat dissipation of these 50v, 100-350 ma units. Covers parallel operation, input currents and control of up to 125 watts.
Sprague Electric Microcircuit Application Report MAR 75-2 (8 pg.)

7 **"Series ULN-2000A Darlington Transistor Arrays-Description and Application"**
(ULN-2001A, ULN-2002A, ULN-2003A ULN-2004A)
Describes circuit capabilities and its use as an interface.
Sprague (7 pg.)

Communications

See also (Digital) Data Transmission

8 **"S2559 Digital Tone Generator"**
(S2559)
Describes a tone generator designed specifically to implement a dual tone telephone dialing system.
American Microsystems (12 pg.)

Communications (cont)

9 **"XR-C240 Monolithic PCM Repeater"**
(XR-C240)
Provides device description, description of circuit operation, and schematics for a typical repeater system.
Exar AN-02 (6 pg.)

10 **"XR-C277 Low-Voltage PCM Repeater IC"**
(XR-C277)
Explains PCM repeater fundamentals, device operation, and presents schematic for a repeater application.
Exar AN-04 (6 pg.)

11 **"Dual Tone Decoding"**
(XR567, XR2567)
Discusses and presents diagrams for a fast, narrow band tone decoder, a touch-tone decoder, and a low cost frequency indicator.
Exar AN-08 (2 pg.)

12 **"High Performance PCM Repeater Using XR-C262"**
(XR-C262)
The design principle and the electrical characteristics of the XR-C262 high performance PCM repeater IC are described. Circuit connection and application examples are given in its use in 1.5 Megabit or 2 Megabit PCM systems.
Exar AN-10

13 **"Pushbutton Dialer with Memory"**
(AY5-9100, AY5-9200, AY5-9500)
Provides instructions, diagram, and PC board layout for an add-on device that connects to any telephone and permits dialing via a separate keyboard. The module has a redial mode and a 20-digit 10 number expandable memory.
General Instrument Bulletin 0701 (7 pg.)

14 **"A 10-Number Repertory Pulse Dialer"**
(AY5-9100, AY5-9200, AY5-9500)
Diagram and short description of a telephone pulse dialer with capability for storage and reference of 10 numbers of up to 22 digits each.
General Instrument Bulletin 0702 (2 pg.)

15 **"One-Button 32 Number Repertory Dialer/Calculator"**
(AY5-9200, AY5-9120)
The circuit described features one-button redial of one of 32 storable telephone numbers of up to 22 digits each. The 8-digit calculator features five functions, including percent.
General Instrument Bulletin 0706 (6 pg.)

16 **"The Impact of LSI on the Design of PCM Codecs"**
Discusses the changes existing telephone systems will go through as LSI circuits are increasingly used for PCM and computer controlled switching.
General Instruments Bulletin 0707 (4 pg.)

17 **"HC-55516/32 CVSD Concept and Operations"**
(HC55516, HC55532)
Outlines Continuously Variable Slope Delta Modulation and compares it to pulse code modulation.
Harris (5 pg.)

18 **"A CB Audio Compression System"**
(MONOCHIP)
Describes using the device to provide an on-chip regulator, audio pre-amp, AGC amplifier, DC volume control, and a headphone driver amplifier for use in a CB transceiver.
Interdesign APN-10 (7 pg.)

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Communications (cont)

1 **"Communication System Transmission Losses"**
Derives equations for computing insertion losses for components in a communication system. Gives computer generated tables, series resistance and reactance plus parallel resistance and reactance for various system impedances.
Motorola AN-710 (5 pg.)

2 **"Two Wire Current Transmitters"**
(LM304)
Describes a method for accurately transmitting analog data over long distances using only two wires.
National Semiconductor LB-40 (2 pg.)

3 **"A Unique Monolithic AGC/Squelch Amplifier"**
(LM170, LM270, LM370)
Describes operation of LM170. Applications: AGC circuits with peak or with transistor detectors, squelch preamplifier with hysteresis, voice-operated-relay controls, Wein bridge oscillators, decade tunable oscillators, and a modulated 455 kHz signal generator.
National AN-51 (12 pg.)

4 **"SL600 Series — Integrated Circuits for Radio Communications"**
(SL600 Series)
Describes circuits and applications for the following: RF/IF amplifiers; limiting RF amplifier/detector; AGC generators; AF amplifier, VOGAD side tone amplifier, AM detector, AGC amplifier and SSB demodulator; multimode detector; microphone/headphone amplifier; double balanced modulators; and a square log device. Describes synchrodyne, superhet, SSB and multimode receivers; SSB and AM transmitters; SSB transceiver, a multi/mode transceiver and a Morse keyer.
Plessey Semiconductor Applications Manual (92 pg.)

5 **"CRC8030 Telephone DTMF Receiver"**
(CRC8030)
Discusses dual-tone multi-frequency signaling. Includes specifications, test data, and interface capabilities.
Rockwell Application Note (28 pg.)

6 **"The CRC8030 Dual Tone Multi-Frequency Receiver"**
(CRC8030)
Discusses various approaches to DTMF receiver design and DTMF signaling. Includes a chart of receiver specifications and a description of the device.
Rockwell (11 pg.)

7 **"Applications of CMOS Integrated Circuits in Communications Equipment"**
See listing under (Digital) CMOS. (Solid State Scientific)

8 **"Modems"**
See listings under (Digital) Data Transmission

Comparators

9 **"AM685/AM686/AM687 Designing with High Speed Comparators"**
(685, 686, 687)
Gives a mathematical analysis of circuit operation. Discusses use as a pulse detector, precision monostable and applications requiring hysteresis.
Advanced Micro Devices Application Note (10 pg.)

Comparators (cont)

10 **"Varying Comparator Hysteresis without Shifting Initial Trip Point"**
Describes adding a positive feedback circuit to introduce precise variable hysteresis into the usual comparator switching action.
Burr-Brown AN-62 (1 pg.)

11 **"The μA760 — A High Speed Monolithic Voltage Comparator"**
(μA760)
Gives a functional description and cites typical performance characteristics. Discusses applications, including level detectors and line receivers, zero crossing detectors, high speed A/D converters, pulse width modulators, and fast peak detectors.
Fairchild Application Note 311 (8 pg.)

12 **"The μA750 Dual Comparator Subsystem"**
(μA750)
Discusses the circuit, design considerations and applications, including use in a combined heater/air conditioner control, a malfunction indicator, an analog status indicator and display, and a minimum frequency detector.
Fairchild Application Note 315 (7 pg.)

13 **"Radiation Testing of Linear Microcircuits"**
Includes the 702. See listing under (Linear) General. (Fairchild)

14 **"A Simple Comparator Using the HA2620"**
See listing under (Linear) Amplifiers, Operational (Harris)

15 **"A High Speed Dual Differential Comparator — the MC1514"**
(MC1414, MC1514)
Describes circuit operation and applications, including level and limit detectors, multivibrators, line receivers, sense amplifiers, zero crossing pulse generator and a peak voltage detector.
Motorola AN-547 (13 pg.)

16 **"Precision IC Comparator Runs from 5V Logic Supply"**
(LM111, LM211, LM311)
Describes the LM111 circuit. Applications: photodiode level detector, zero crossing detectors, digital interface circuits, multivibrators, oscillators, and a frequency doubler. Includes application hints.
National Linear Applications Handbook, Vol. I, AN-41 (6 pg.)

17 **"LM139/LM239/LM339 — A Quad of Independently Functioning Comparators"**
(LM139, LM239, LM339)
Describes LM139 circuit. Applications: comparators with hysteresis, limit comparators with lamp drivers, zero crossing detectors, oscillators, MOS clock drivers, wide range VCO, AND/NAND gates, OR/NOR gates, multivibrators, time delay generators, pulse width modulator, temperature alarm, tape reader and peak detector.
National AN-74 (16 pg.)

18 **"Application of Programmable Micropower Comparators"**
(L161)
Describes the device and how to program it. Also describes the effects of programming on AC characteristics, limit, zero crossing, and level detectors; DC to DC converter applications.
Siliconix AN76-7

19 **"Comparing the High Speed Comparators"**
(LM160, LM161, LM260, LM261, LM360, LM361)
Compares LM360 to μA760 and LM261 to NE529. Covers application as a peak detector for tape and disk file channels and in a high-speed 3-bit A/D converter.
National AN-87 (6 pg.)

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Comparators (cont)

1 **"Fast Voltage Comparators with Low Input Current"**
(LM102, LM106, LM202, LM206, LM302, LM306)
Describes use of LM102 to buffer the input of the LM106 comparator. Applications: comparators for fast A/D converters, for zero crossing detectors, and for ac coupled signals.
National Linear Applications Handbook, Vol. I, LB-6 (2 pg.)

2 **"An IC Voltage Comparator for High Impedance Circuitry"**
(LM111, LM211, LM311)
Describes LM111 circuit and comparison to LM106/LM710. Applications: zero crossing detector driving an analog switch, detector for a magnetic transducer, comparator for a low level photodiode, and driving a ground-referred load.
National Linear Applications Handbook, Vol. I, LB-12 (2 pg.)

3 **"Specifying Selected Op Amps and Comparators"**
Discusses the most common parameters that are tested on operational amplifiers and comparators and the relative difficulty of testing on high speed equipment. Gives a guideline to tightened specifications.
National Linear Applications Handbook, Vol. II, LB-26 (2 pg.)

4 **"Circuit Techniques for Avoiding Oscillations in Comparator Applications"**
(LM111)
Details design techniques for avoiding oscillations when using high gain, wide bandwidth comparators like the LM11.
National Semiconductor LB-39 (2 pg.)

5 **"Microvolt Comparator"**
(LM111, LM211, LM311, LM121A, LM221A, LM321A)
Describes an LM121A preamplifier driving an LM111 comparator.
National Linear Applications Handbook, Vol. II, LC-32 (2 pg.)

6 **"The 725 Op Amp as a Low Level Comparator"**
(PM725)
Provides the circuit and design curves for a submillivolt level comparator based on the 725 op amp.
Precision Monolithics AN-25 (4 pg.)

Consumer, AM/FM

7 **"Frequency Selective AM Detection Using Monolithic Phase-Locked Loops"**
(XR2228, XR215, XR2212)
Design of frequency selective coherent AM and AM/FM demodulator systems using these devices is described.
Exar AN-13

8 **"Integrated Circuits for FM Receivers"**
(μA703, μA753, μA758, μA3075)
Describes ICs capable of performing all basic functions of an FM stereo receiver, except the front end. Discusses 753 IF block, CA3075 2nd IF block, 758 stereo multiplex decoder, 706 audio power amplifier.
Fairchild Application Note 318 (7 pg.)

9 **"The μA758 — A Phase Locked Loop FM Stereo Multiplex Decoder"**
(μA758)
Gives functional description of this device, including input buffer/amplifier and bias supply, demodulator, stereo switch and lamp driver, VCO, frequency dividers, pilot phase and amplitude detectors. Discusses operating characteristics, testing and alignment.
Fairchild Application Note 319/1 (11 pg.)

Consumer, AM/FM (cont)

10 **"The μA732 and μA767 Integrated Circuit Stereo Multiplex Decoders"**
(μA732, μA767)
Discusses stereo demodulation, stereo/monaural switching, and interstation audio mute switching sections of these devices. Describes performance characteristics, external components required, alignment and user options.
Fairchild Application Note 286 (8 pg.)

11 **"A Fully Integrated High Quality AM/FM Stereo Receiver"**
(μA706, μA720, μA739, μA753, μA758, μA3075)
Describes receiver using ICs with a comparison to discrete design.
Fairchild Application Note 328/1 (6 pg.)

12 **"ZN414 — The One Chip Radio Receiver"**
(ZN414)
Describes various applications for single-chip IC radio, and suggests a new approach to AM receiver design.
Ferranti (16 pg.)

13 **"FM Tuner Using the Economega I Digital Tuning System"**
(Economega)
Describes modification of a Goodman model 1-20 tuner amplifier to include a GI automatic tuning system and display. Presents schematics as well as descriptions of various changes made.
General Instrument Bulletin 0407 (7 pg.)

14 **"Digital Frequency Display for a Radio-Receiver"**
(AY5-1200A, AY5-8100)
Explains details of interfacing the devices with a radio receiver. Provides circuit description and diagram plus a layout for a PC board showing pre-amp and display connections.
General Instrument Bulletin 0409 (11 pg.)

15 **"Adjusting the IF Offset of the AY5-8100"**
(AY5-8100)
Depicts adjusting the IF offset of the device in 10 KHz steps.
General Instrument Bulletin 0410 (2 pg.)

16 **"Radio Receiver Frequency Counter/Clock"**
Supplies diagram and operating instructions for using each device to display time or frequency on a 3½ digit display.
General Instrument Bulletin 0411 (3 pg.)

17 **"Stereomega Phase-Locked Loop Digital Tuning Systems"**
(Stereomega, AY3-8115, AY3-8116, AY5-8450, AY5-8460, ER1400)
Presents use of system in four applications which provide full electronic control of a varactor-tuned AM/FM radio: basic manual, basic manual with clock, basic remote controlled, and deluxe remote-controlled. Includes diagrams and schematics.
General Instrument Bulletin 0412 (11 pg.)

18 **"Manual and Automatic FM Tuning System Using Economega I"**
(Economega, AY3-8203, ER1400, MEM4956)
Describes a system that allows manual tuning of a Goodman 1-20 tuner with non-volatile electronic storage of tuning data for 16 stations. Diagrams, schematic.
General Instrument Bulletin 0414 (4 pg.)

19 **"Integrated Circuit IF Amplifiers for AM/FM and FM Radios"**
(MC1350, MC1355, MC1357, MFC4010, MFC6010)
Discusses the use of ICs in four IF amplifiers: a high performance FM, a quadrature detector FM, a composite AM/FM, and an economy model FM receiver.
Motorola AN-543A (14 pg.)

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Consumer, AM/FM (cont)

1 **"Scanning Logic for RF Scanner-Receivers Using CMOS Integrated Circuits"**
See listing under (Digital) CMOS (Motorola)

2 **"A Complete Monolithic IF Strip for AM/AGC Applications**
(LM172, LM272)
Circuit operation of LM172/LM272. Covers application in superheterodyne and low frequency T.R.F. receivers.
National Linear Applications Handbook, Vol. I, AN-15 (6 pg.)

3 **"A Complete Monolithic AM/FM/SSB IF Strip"**
(LM273, LM373, LM274, LM374)
Discusses LM273/LM373, and LM274/LM374 IF amplifier/detectors. Includes description of FM, SSB, and AM detection. Applications include: FM slope detector, double conversion IF strip, and coherent phase locked receiver. Also includes application hints.
National AN-54 (8 pg.)

4 **"Low Cost IC Stereo Receiver"**
(LM1800, LM1820, LM3089)
Describes the complete circuit and performance of an AM/FM/Stereo receiver.
National AN-147 (4 pg.)

5 **"FM Remote Speaker System"**
Describes an FM transmitter which couples to its companion receiver thru the power lines. The system transmits speech or music and is suitable for home use as well as some factory applications.
National AN-146 (4 pg.)

6 **"Low Cost AM Radio System Using LM1820 and LM386"**
(LM1820, LM286)
Presents circuit diagram of a simple AM radio without an rf preamplifier ahead of the mixer.
National Linear Applications Handbook, Vol. II, LB-29 (2 pg.)

7 **"Audio Handbook"**
See listing under Consumer, Audio (National)

8 **"AM/SSB Transceivers and Noise Blanking Using SL1600 Series Circuits"**
(SL1623, SL1626, SL1640, SL1641)
Describes the sub-systems used in AM-SSB transceivers.
Plessey Semiconductor (10 pg.)

9 **"An SSB Transceiver for Citizens' Band Using Plessey SL1600 Integrated Circuits**
(SL1600 series)
Describes the design of a SSB transceiver.
Plessey Semiconductor (4 pg.)

10 **"An AM Receiver Using the Plessey SL1600 Series"**
(SL1600 series)
Describes the design of a simple AM receiver.
Plessey Semiconductor (7 pg.)

11 **"SL1600 Series Transceiver Applications"**
(SL1600 series)
Discusses simple SSB and multimode transceiver design.
Plessey Semiconductor (32 pg.)

12 **"Integrated Circuits for FM Broadcast Receivers"**
(CA3005, CA3011, CA3012, CA3013, CA3014)
Discusses circuits for FM tuner, IF amplifier, limiter, and detector applications.
RCA ICAN-5269 (7 pg.)

Consumer, AM/FM (cont)

13 **"Integrated-Circuit Frequency-Modulation IF Amplifiers"**
(CA3012, CA3028)
Describes CA3012 and CA3028 differential amplifiers and application in IF-amplifier strips.
RCA ICAN-5380 (7 pg.)

14 **"Application of the CA3089E FM-IF Subsystem"**
(CA3089)
Discusses stability considerations and following circuits: quadrature-detector, audio and AFC, mute, tuning meter and rf-agc, if amplifier/detector system and stereo decoder. Also covers operation at frequencies other than 10.7 MHz.
RCA ICAN-6257 (8 pg.)

15 **"Integrated-Circuit Stereo Decoder Using the CA3090AQ Stereo Multiplex Demodulator"**
(CA3090AQ)
Gives circuit description. Describes the LC oscillator, reactance, stereo defeat, dc coupled flip-flop preamplifier and phase splitter circuits.
RCA ICAN-6259 (10 pg.)

16 **"TDA1200 FM-IF System for High Performance Radio Receivers"**
(TDA1200)
Gives a detailed description of the device. Describes relative performance of device when used in an FM tuner, an AM/FM car radio, and a portable AM/FM radio.
SGS-ATES Technical Note 117 (12 pg.)

17 **"ULN-2204A AM/FM Receiver System"**
(ULN-2204)
Presents operation of device and discusses typical applications.
Sprague AN-27121.51 (12 pg.)

18 **"A Complete AM/FM Single Processing System"**
(ULN-2242)
Describes a circuit which simplifies AM/FM receiver design and improves performance. Includes diagrams and graphs.
Sprague TP77-6 (10 pg.)

Consumer, Audio

19 **"MOS Circuit for Electronic Organs"**
(S2193, S2688, S8890, S10110, S10129, S10130, S10131, S50240, S50241, S50242)
Describes the use of ICs for various electronic organ circuits.
American Microsystems AP74-10 (7 pg.)

20 **"An Electronic Music Synthesizer Using the XR2207 and the XR2240"**
(XR2207, XR2240)
Design of a simple, low-cost "music synthesizer" system is described.
Exar AN-15

21 **"Applications of the μA739 and μA749 Dual Preamplifier Integrated Circuits in Home Entertainment Equipment"**
(μA739, μA749)
Describes circuit operation. Discusses d-c and a-c considerations, compensation and noise performance. Covers applications as a stereo tape amplifier, a high fidelity phonograph preamplifier, and a TV remote control amplifier.
Fairchild Application Note 171 (7 pg.)

Consumer, Audio (cont)

1 **"A High Output Power, (5 Watt), Low Distortion, IC Audio Amplifier"**
(μA706)
Describes circuit, functions, design considerations of the μA706. Discusses application as an audio amplifier with the speaker load connected to ground, with the speaker load between supply and output, and discusses use in an FM stereo receiver.
Fairchild Application Note 317/1 (6 pg.)

2 **"An Electronic Piano Using the AY-1-1320"**
(AY1-0212, AY1-1320, AY1-5050)
Presents circuit diagrams and description of an electronic piano using a divider, a top octave generator and the device.
General Instrument Bulletin 0501 (5 pg.)

3 **"Designing a Basic Organ System Using the MK50240"**
(MK50240)
Describes an organ system using the MK50240 Top Octave Generator for each octave.
Mostek (3 pg.)

4 **"LM380 Power Audio Amplifier"**
(LM380)
Describes the circuit and general operating characteristics. Applications: phono amplifier, bridge amplifier, and intercom.
National AN-69 (7 pg.)

5 **"Audio Handbook"**
(LM171, LM377, LM378, LM379, LM380, LM381, LM382, LM384, LM386, LM387, LM388, LM389, LM390, LM391, LM703, LM1303, LM1310, LM1351, LM1800, LM1820, LM2111, LM3011, LM3065, LM3075, LM3089, MM5837)
Contains discussions and design particulars on many areas including preamplifiers; AM, FM, and Stereo; power amplifiers; controls, networks and power supply design—covers practical as well as theoretical aspects.
National $4.00 (188 pg.)

6 **"Audio Applications for the DAC-76 Companding Converter"**
(DAC-76)
Discusses the multiplying and control characteristics of the DAC-76 with regard to 2C inputs, as an aid to optimizing high-performance digitally-controlled gain circuits.
Precision Monolithics AN-28 (8 pg.)

7 **"Application of the RCA CA3007 Integrated-Circuit Audio Amplifier"**
(CA3007)
Describes circuit. Covers application as dual-supply audio driver in a direct-coupled audio amp, and as single-supply audio driver in a capacitor-coupled audio amp.
RCA ICAN-5037 (4 pg.)

8 **"Use of Analog Delay Lines for Audio Speed Change without Pitch Changes"**
(SAD1024A)
Describes technique for increasing or slowing the speed of a recording.
Reticon Application Note No. 112 (4 pg.)

9 **"Build a Simple Comb-Filter or Flanger with a Bucket Brigade Delay Line"**
(SAD1024A)
Describes a flanger (electronic sound modifier) and what is needed to build one.
Reticon Application Note No. 113 (4 pg.)

Consumer, Audio (cont)

10 **"TDA1054M — Cassette Recorder Preamplifier with ALC"**
(TDA1054M)
Discusses features of the device and preamplifier noise. Applications in Hi-Fi, stereo, and dynamic range compressors are described.
SGS-ATES Technical Note 124 (24 pg.)

11 **"M252 and M253 Rhythm Generators for Electronic Organs"**
(M252, M253)
Defines and describes rhythm generators. Presents these two devices, and describes their use in electronic organs.
SGS-ATES Technical Note 131 (21 pg.)

12 **"TCA600/900 and TCA610/910 Integrated Motor Speed Regulators"**
See listing under (Linear) Industrial Control (SGS-ATES)

13 **"The ULN-2280 Amplifier"**
(ULN-2280)
Describes this single power amplifier circuit and discusses applications as a low-cost phonograph amplifier, amplifier with tone controls, common mode amplifier, full bridge amplifier, and a mono FM receiver.
Sprague Electric Microcircuit Application Report MAR 73-2 (8 pg.)

14 **"Low-Cost-Dual Class B Driver"**
(ULN-2277, ULN-2278)
Describes the ULN-2277/78 ICs and describes use in dual 2-watt and dual 15-watt amplifiers.
Sprague Electric Microcircuit Application Report MAR 73-5 (3 pg.)

Consumer, Medical

15 **"A Personalized Heart-Rate Monitor with Digital Readout"**
(MC1776, MC14013, MC14040, MC14572)
Describes digital heart-rate monitor using the MC1776 op amp and CMOS digital ICs.
Motorola AN-714 (4 pg.)

Consumer, TV

16 **"A Ten Game Color Video System Using the AY3-8610-1"**
(AY13-8610-1, AY3-8615)
Furnishes diagram and PC board layout of a color TV game circuit incorporating the devices.
General Instrument Bulletin 0401A (3 pg.)

17 **"A Tank "Battle" TV Game Using the AY3-8710-1"**
(AY3-8710-1)
Supplies diagram and description of a TV game circuit which provides an NTSC compatible signal to operate a standard 525-line TV receiver and produces a black and white picture.
General Instrument Bulletin 0402A (4 pg.)

18 **"World Television Systems"**
Furnishes, in chart form, the characteristics of various television systems. Includes such data as line standards and channel frequency assignments.
General Instrument Bulletin 0403 (2 pg.)

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Consumer, TV (cont)

1 **"PAL Colour Encoding Systems for the AY3-8500 TV Game Circuit"**
(AY3-8500)
Briefly describes the PAL system, then presents two alternate circuits for color encoding the AY3-8500 TV game according to PAL.
General Instrument Bulletin 0404 (8 pg.)

2 **"Video Game FM Sound Generator"**
Describes a system that enables a TV sound system to be used for game sounds as well.
General Instrument Bulletin 0405 (2 pg.)

3 **"Wireless Remote Control of the AY3-8710-1 Battle Game"**
(AY3-8710-1, SAA1024, SAA1025)
Presents system diagrams, logic, and pin connections for an ultrasonic remote control unit utilizing the devices.
General Instrument Bulletin 0408A (5 pg.)

4 **"Economega I Digital Tuning for Television Receivers"**
(Economega, MEM4956, ER1400, SAA1025)
Describes a digital TV tuning system capable of automatic search and acquisition of up to 16 different TV programs. Supplies system block diagram as well as schematics for individual circuits.
General Instrument Bulletin 0413 (7 pg.)

5 **"On-Screen Displays for Television"**
(AY3-8330, AY5-8321)
Examines an on-screen tuning display with 16 selectable programs. Includes TV interface and system schematics.
General Instrument Bulletin 0415 (4 pg.)

6 **"The Gimini Economy 8600 Programmable Game System"**
(AY3-8615)
Describes use of the AY3-8615 game/color processor in a system designed to be priced near that of dedicated game systems, but with a cartridge expandability.
General Instrument Bulletin 0416 (4 pg.)

7 **"Videovox II: Video Color Organ"**
(AY3-8515)
On receiving an audio input from either a crystal mike or an external source, the circuit described generates a color composite video signal, modulated and suitable for use with color TV.
General Instrument Bulletin 0417 (4 pg.)

8 **"Economega I Digital Tuning for UK Televisions"**
(Economega)
Describes two eight program UHF band versions of the Economega System specifically for U.K. market. Conventional AFC is retained for simplicity. Includes a manually controlled search feature.
General Instrument Bulletin 0420 (4 pg.)

9 **"Television Video IF Amplifier Using Integrated Circuits"**
(MC1330, MC1350, MC1352, MC1353)
Discusses requirements of the video IF section of a TV receiver. Describes MC1350/2/3 amplifier and MC1330 detector circuits. Includes design for a practical TV IF amplifier and detector.
Motorola AN-545 (11 pg.)

10 **"Television Horizontal APC/AFC Loops: The Last 10 Percent"**
Discusses some of the common problems that may be encountered in the design of horizontal APC/AFC loops and methods to avoid or overcome them.
Motorola AN-727 (15 pg.)

Consumer, TV (cont)

11 **"A Medium Cost PLL Varactor Tuning System Utilizing Off-the-Shelf Logic"**
Describes a frequency domain tuning scheme for varactor TV tuners.
Motorola AN-729 (14 pg.)

12 **"A Synthetic Spectrum Tuning System for TV"**
Describes a tuning system which generates a complete spectrum of TV channel markers to achieve precise tuning on any channel.
Motorola AN-739 (12 pg.)

13 **"A Phase-Locked Loop Tuning System for Television"**
Describes a frequency domain tuning system using direct digital count down of the local oscillator.
Motorola AN-744 (10 pg.)

14 **"A Disassociated Intercarrier Television Video IF Amplifier"**
(MC1331)
Discusses a video IF system using the MC1331 low level multiplier detector.
Motorola AN-751 (9 pg.)

15 **"Video Amplifier Design: Know Your Picture Tube Requirements"**
(MC1323)
Describes video systems designed to alleviate design compromises associated with driving a unitized gun picture tube.
Motorola AN-761 (26 pg.)

16 **"The MC1323 — A Fully Programmable Demodulator"**
(MC1323)
Describes operation of this NTSC demodulator and use with various picture tube phosphors, especially color temperature D6500.
Motorola AN-763 (16 pg.)

17 **"An Approach to a Low-Noise TV IF System"**
(MC1331)
Discusses TV system noise figure and system trade offs, a technique to measure the IF contribution and ways to minimize the IF noise.
Motorola AN-765 (8 pg.)

18 **"A Color TV Primer for the EE"**
Describes the basic circuits in a TV and the IC's used therein.
National Linear Applications Handbook, Vol. II.

19 **"Programmable TV Timer/Time-Channel Display"**
(MM53107, MM53100, MM5840)
Describes an on-screen TV real time and channel display based on the devices. Includes schematics and PC board layout.
National Semiconductor AN-196 (10 pg.)
(CA3126)

20 **"Application of the RCA CA3044 and CA3044V1 Integrated Circuits In Automatic-Fine-Tuning Systems"**
(CA3044)
Describes circuits, operating characteristics and dynamic performance of this wideband amplifier for AFC applications.
RCA ICAN-5831 (5 pg.)

21 **"Feedback-Type Volume-Control Circuits for RCA CA3041 and CA3042 Integrated Circuits"**
(CA3041, CA3042)
Describes several types of volume controls for television receivers using these ICs, with a detailed discussion of feedback control.
RCA ICAN-5841 (4 pg.)

Consumer, TV (cont)

1 **"Application of the CA3126Q Chroma-Processing IC Using Sample-and-Hold Circuit Techniques"**
(CA3126Q)
Detailed circuit description of this device, which requires only one adjustment; a trimmer capacitor to tune the crystal filter. Discusses performance data, the phase detector, sample and hold circuits, the VCO loop, first chroma amplifier and ACC servo loop, and the second chroma amplifier.
RCA ICAN-6247 (8 pg.)

2 **"Description and Application of the RCA CA3120E Integrated-Circuit TV-Signal Processor"**
(CA3120)
Describes the operation and application of this device which includes TV video noise processor, agc and sync separator circuits.
RCA ICAN-6302 (9 pg.)

3 **"A Single IC for the Complete PIX-IF-System in TV Receivers"**
(CA3068)
Gives a detailed description of the circuit functions of the CA3068 and its use in color and b/w TV receivers.
RCA ICAN-6303 (17 pg.)

4 **"A Flexible Integrated-Circuit Color Demodulator for Color Television"**
(CA3067)
Describes circuit operation of the CA3067, including its output amplifiers, demodulator, demodulator preamp, and tint control amplifier. Describes use of this circuit in a red-green-blue system.
RCA ICAN-6724 (8 pg.)

5 **"Vertical Deflection Output Stages Using Audio Integrated Circuits"**
(TAA611, TAA621, TBA641, TBA800, TBA810, TBA820)
Characterizes the advantages and working principles of vertical deflection circuits using audio IC's. Seven circuits, covering small and large screen performance, are included.
SGS-ATES Technical Note 118 (18 pg.)

6 **"An Approach to a Unified Chroma System"**
Describes design approach that will eventually allow fabrication of a complete single-chip chroma system.
Sprague Electric TP 74-3 (9 pg.)

7 **"An Integrated Two-Watt Sound System for Television Applications"**
(ULN-2211)
Describes the design and use of the ULN-2211 limiter-detector-amplifier.
Sprague Electric TP 72-05 (9 pg.)

Converters

Also see Instrumentation.

8 **"Data Conversion with Companding DAC Devices"**
Introduces companding principles and use of companding DACs in industrial and PCM transmission systems. Provides companding DAC circuit description and discussion of how μ-Law and A-Law characteristics are generated. Application cover μP based data acquisition systems, motion control, audio systems, and telecommunication systems.
Advanced Micro Devices (36 pg.)

Converters (cont)

9 **"Analog-Digital Conversion Notes"**
Covers many aspects of A/D and D/A converters including use, testing and specifying. Extensive applications information includes data systems, acquisition, distribution, communication.
Analog Devices $5.95 (254 pg.)

10 **"The Multiplying DAC Application Guide"**
(AD7520, AD7521, AD7522, AD7523, AD7524, AD7525, AD7530, AD7531, AD7533, AD7541)
Discusses applications which take advantage of the MDAC's ability to accept AC or DC references, which can be of either polarity. Applications include digitally-controlled gain and attenuation circuits.
Analog Devices (40 pg.)

11 **"Beckman Model 845 Digital-to-Analog Converter"**
(845)
Discusses basic D/A converter performance including interface and transfer characteristics, then covers the performance of the 845 Series.
Beckman Instruments (9 pg.)

12 **"D/A Converter Differential Linearity Error — It Really Shows Up"**
Discusses differential linearity, the difference in analog output for a change between two successive digital input codes. Gives graphs of two examples with the same linearity specification.
Burr-Brown AN-58 (2 pg.)

13 **"Don't Forget D/A Converter Tempco"**
Discusses offset, gain and linearity drift with temperature.
Burr-Brown AN-59 (3 pg.)

14 **"Principles of Data Acquisition and Conversion"**
Discusses basic principles of analog to digital systems including sampling rate, aperture error, accuracy, resolution, throughput, and codes.
Burr-Brown AN-79 (5 pg.)

15 **"Squeeze High Performance Out of Low-Cost Hybrid Data Converters"**
Lists ways in which converter performance can be improved by the addition of a few external components.
Burr-Brown AN-86 (4 pg.)

16 **"What Designers Should Know About Data-Converter Drift"**
Examines components of drift as they apply to A/D and D/A converters. Includes discussion of the effect of reference drift and computation of worst case error.
Burr-Brown AN-89 (4 pg.)

17 **"Intrinsically Safe Data Acquisition"**
See listing under (Digital) CMOS (Burr-Brown)

18 **"FX-209 AP Notes"**
(FX-209)
Describes use of the FX-209 delta modulation analog to digital converter as an AGC amplifier, audio delay line and as an audio scrambler.
CMA (6 pg.)

19 **"Graphs Give Aperture Time Required for A-D Conversion"**
Presents two graphs, aperture time versus rate of voltage change and versus frequency, for resolutions from 4 to 16 bits.
Datel Technical Note V-14 (4 pg.)

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Converters (cont)

1 **"Know Your Converter Codes"**
Describes the various A/D and D/A converter codes.
Datel Bulletin V-12 (6 pg.)

2 **"Designer's Guide to V/F Converters"**
Spells out the theory and operation of V/F and F/V converters. Calibration procedures and such applications as ratiometric measurement and frequency difference measurement are covered.
Datel (18 pg.)

3 **"Applications of the ZN425E 8-Bit A-D/D-A Converter"**
(ZN425)
Covers converter definitions, calibration, bipolar operation. Applications: ramp generation, peak detect, channel selection, weighing system, bargraph drive, multiply/divide, and function generation.
Ferranti (31 pg.)

4 **"Digital-to-Analog Converter Applications"**
(HI1080, HI1085)
Operating modes and applications of HI-1080 converter, which features resistor ladder network and switching devices on same chip. Discusses cascaded D to A converter as well as up-down counter and successive approximation A to D converters.
Harris Application Note 511 (7 pg.)

5 **"Counter Type A to D Converter"**
(HI1080)
Circuit details of an A to D converter employing a unidirectional digital counter and the HI-1080 eight-bit D to A converter to generate a ramp voltage.
Harris Application Note 512 (3 pg.)

6 **"Data Conversion Handbook"**
Defines the qualities, specifications, and techniques that combine to give D/A and A/D converters their special character. Also covers sample/hold amplifiers, multiplexers, and coding.
Hybrid Systems $1.50 (175 pg.)

7 **"Applications of a Monolithic Sample-and-Hold/Gated Operational Amplifier"**
See (Linear) Amplifiers, Operational (Harris)

8 **"A-8400 User Guide"**
(A8400)
Theory, circuit details, operation, and design examples of this v/f and f/v converter.
Intech/FMI (18 pg.)

9 **"A-8402 User Guide"**
(A8402)
Theory, circuit details, operation, and design examples of this v/f and f/v converter.
Intech/FMI (30 pg.)

10 **"Digital-to-Analog Converter Circuits Using the 8018A"**
(ICL8018A, ICL8019A, ICL8020A)
Discusses D/A converters, both in general and their electrical specifications. Describes circuit operation for 8018A and covers its expansion to 8 and 12 bit units. Also discusses generating reference currents using zeners, pnp transistors or high-gain operational amplifiers as references. Describes system interface requirements.
Intersil Application Bulletin A010 (8 pg.)

Converters (cont)

11 **"8052A/8053A — A Low Cost Precision Pair for A/D Converters"**
(ICL8052, ICL8053)
Discusses the characteristics of the 8052/8053 dual pair and how they can be interfaced with one another to implement a dual-slope converter design.
Intersil A014 (30 pg.)

12 **"Selecting A/D Converters"**
Compares and contrasts successive approximation and integrating A/D conversion techniques with respect to speed, accuracy, and cost.
Intersil A016 (6 pg.)

13 **"The Integrating A/D Converter"**
Discusses the dual slope technique with considerable attention to error analysis.
Intersil A017 (4 pg.)

14 **"Do's and Don'ts of Applying A/D Converters"**
Examines topics concerning proper system design when using A/D converters. Subjects treated include ground loop errors, components, references, capacitive coupling, and thermal effects.
Intersil A018 (2 pg.)

15 **"Power D/A Converters Using the IH8510"**
(IH8510, AH8520, IH8521, 7105, 7120)
Discusses the addition of a power amplifier to a D/A converter. Briefly describes use for motor control and programmable power supplies.
Intersil A021 (4 pg.)

16 **"The ICL7104 — A Binary Output A/D Converter for μ Processors"**
(ICL7104, ICL8052, ICL8068)
Describes the operation of the ICL7104, and either the ICL8052 or ICL8068, as a dual-slope integrating converter.
Intersil A030 (14 pg.)

17 **"Voltage Transients (Glitches)"**
(MN3008)
Discusses D/A converter analog voltage spikes appearing in the output following a change of input code.
Micro Networks AN-101 (2 pg.)

18 **"Truncation of A/D Converters"**
Describes how to reduce or to program the number of bits converted.
Micro Networks AN-102 (2 pg.)

19 **"When Should a Sample Hold Amplifier be Used?"**
Covers the use of sample-hold amplifiers with A/D converters. Discusses use with dynamically changing signals and the droop rate of the sample-hold circuit.
Micro Networks AN-103 (2 pg.)

20 **"MN312 Connections for Bipolar Output"**
(MN312)
Shows use of an external op amp to convert a unipolar output to bipolar.
Micro Networks AN-104 (2 pg.)

21 **"Serial to Parallel Conversion"**
(MN502, MN5200, MN5210)
Covers timing considerations in the conversion of A/D converter output from serial to parallel form.
Micro Networks AN-106 (2 pg.)

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Converters (cont)

1 **"Simplifying the Digital to Analog Converter through Hybrid Technology"**
Considers basic design problems of D/A converters and gets into hybrid design. Includes construction techniques, specifications and testing.
Micro Networks (10 pg.)

2 **"Build a Low Cost Data Acquisition System with Standard DIPs"**
(MN7130, MNADC80)
Shows how a complete 12-bit, 16-channel data acquisition system can be built by adding a few standard ICs to the MN7130 multiplexed sample/hold amplifier.
Micro Networks AN201 (6 pg.)

3 **"Analog-to-Digital Conversion Techniques"**
Discusses open-loop and feedback techniques: frequency, pulse width, cascade, ramp, counter, successive approximation, multiple comparison subranging, nonlinear conversion, double and triple ramp conversion.
Motorola AN-471 (21 pg.)

4 **"Analog-to-Digital Cyclic Converter"**
(MC1456)
Discusses circuits and operation of medium speed-medium accuracy converter that uses successive approximation technique in which unknown analog input voltage is successively compared to reference voltage to determine each bit of digital output. A comparison of gray and binary code operation and an error analysis are provided.
Motorola AN-557 (10 pg.)

5 **"A Single Ramp Analog-to-Digital Converter"**
Discusses an A/D converter which incorporates a calibration cycle to insure 12 bit accuracy. Briefly covers errors encountered in the converter described.
Motorola AN-559 (9 pg.)

6 **"High Speed Digital-to-Analog and Analog-to-Digital Techniques"**
Gives overview that includes voltage and current output D/As; parallel (flash), tracking, successive approximation, and parallel ripple A/Ds as well as nonsynchronous and synchronous VTF A/D. Glossary of terms.
Motorola AN-702 (14 pg.)

7 **"Binary D/A Converters Can Provide BCD-Coded Conversion"**
(MC1408, MC1508)
Describes the MC1508 D/A converter used as a 2 or 2½ digit BCD converter. Describes application in a 2½ digit digital voltmeter.
Motorola AN-713 (4 pg.)

8 **"Successive Approximation A/D Conversion"**
(MC1408, MC14559)
Describes advances in successive approximation techniques with emphasis on SARs (Successive Approximation Registers.) Shows both a normal and a high speed A/D using these methods.
Motorola AN-716 (8 pg.)

9 **"Autoranging Digital Multimeter Using the MC14433 CMOS A/D Converter"**
(MC14433)
Describes using the MC14433 A/D converter to build an autorange digital multimeter. The multimeter includes ac and dc voltage ranges from 200mV to 200V, ac and dc current from 2mA to 2A full scale, and resistance ranges from 2 kilohms to 2 megohms full scale.
Motorola AN-769 (5 pg.)

Converters (cont)

10 **"Data Acquisition Networks with NMOS and CMOS"**
See listing under (Microprocessors) Applications (Motorola)

11 **"Analog-to-Digital Conversion Techniques with the M6800 Microprocessor System"**
See listing under (Microprocessor) Systems (Motorola)

12 **"Applications of the MC1405/MC14435 in Digital Meters"**
See listing under (Linear) Instrumentation (Motorola)

13 **"Digital Voltmeters and the MM5330"**
(MM5330)
Describes basic counting techniques for building digital voltmeters and shows how the MM5330 can be used in a dual slope system.
National AN-155 (8 pg.)

14 **"Specifying A/D and D/A Converters"**
Explains and defines the data sheet terms for these converters.
National AN-156 (6 pg.)

15 **"Data Acquisition System Interface to Computers"**
(ADC1200, ADC1210, MM5357)
Compares three configurations for multiple input analog to digital converter systems—Random Addressed Multiplexed, Parallel Conversion, and Multiplexed with Memory. Gives detailed comparisons of costs, A/D and interface requirements.
National AN-159 (18 pg.)

16 **"Analog-to-Digital Converter Testing"**
(ADC0800, ADC1210, ADC1211)
Describes a low cost test circuit with board layout for testing A/Ds using a storage scope readout.
National AN-179 (6 pg.)

17 **"A Cheap and Easy DC-DC Converter"**
(LM555)
Design equations, derivations, and schematics used to construct a DC-DC converter.
National AN-183 (4 pg.)

18 **"High Speed Warning Device for Automobiles"**
Proposes a tachometer device operating from the spark coil primary.
National Linear Applications Handbook, Vol. II, LB-33 (2 pg.)

19 **"CMOS A/D Converter Chips Easily Interface to 8080A Microprocessor Systems"**
(ADC3511, ADC3711, INS8080A)
Outlines techniques for interfacing AID converter devices to 8080A μP systems. Includes description of A/D conversion, BCD output capability, flowcharts, schematics, and block diagrams.
National AN-200 (9 pg.)

20 **"Application Circuits of μPC603D, 610D"**
(μPC603, μPC610)
Discusses functions and operating principles of each device as well as applications including a digitally programmable power source and a waveform generator.
NEC America IEP-543 (24 pg.)

21 **"Application Information for μPC614D"**
(μPC614)
Provides application hints and parameters for a pulse width modulation converter in a digital multimeter application.
NEC America (6 pg.)

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Converters (cont)

1 **"The SP750 in A/D Converters"**
(SP750)
Describes a parallel A/D converter using the device. Diagrams and device characteristics are included.
Plessey (8 pg.)

2 **"Strobing the DAC-08 Under Logic Control"**
(DAC-08)
Gives connections for strobing the output of this DAC.
Precision Monolithics AB-1 (1 pg.)

3 **"A Low Cost, High-Performance Tracking A/D Converter"**
(DAC-100, CMP-01)
Basic operation of 8-bit tracking converter that uses DAC-100 series 10-bit D/A converter, CMP-01 series comparator, and 4-bit MSI up/down counters.
Precision Monolithics AN-6 (8 pg.)

4 **"A Low Cost, Easy-to-Build Successive Approximation Analog-to-Digital Converter"**
(DAC-100, CMP-01)
General discussion of feedback A/D converters. Operation of A/D converter capable of 8-bit conversions in 6 μs. The system is expandable to 10-bit resolution. It uses DAC-100, CMP-01, and a successive approximation register.
Precision Monolithics AN-11 (8 pg.)

5 **"Interfacing Precision Monolithics Digital-to-Analog Converters with CMOS Logic"**
(DAC-100, DAC-01)
Analyzes input circuits of these DACs and CMOS interfaces. Describes a complete 10-bit DAC and an 8-bit A/D.
Precision Monolithics AN-14 (4 pg.)

6 **"Low Cost, High Speed Analog-to-Digital Conversion with the DAC-08"**
(DAC-08)
Discusses the successive approximation technique to A/D and describes three designs with conversion times of 1, 2, and 4 μsec.
Precision Monolithics AN-16 (7 pg.)

7 **"DAC-08 Applications Collection"**
(DAC-08)
Discusses the dual output, and high compliance. Covers use in a CRT display driver, bridge transducer control system, A/D converter, waveform generator, digital additions/subtraction with analog output, digital attenuator and microprocessor controlled A/D converter.
Precision Monolithics AN-17 (12 pg.)

8 **"Differential and Multiplying Digital-to-Analog Converter Applications"**
(DAC-08)
Describes use in 2-quadrant, 4-quadrant and AC-coupled multiplication. Also covers differential and ratiometric conversion, a nulling bridge circuit, a power monitor, and algebraic computation circuits with analog output.
Precision Monolithics AN-19 (8 pg.)

9 **"Exponential Digitally Controlled Oscillator Using DAC-76"**
(DAC-76)
Depicts a 4-IC microprocessor-controlled oscillator with a 8159 to 1 frequency range covering 2.5 Hz to 20 kHz. The circuit uses an exponential current output D/A converter as a programmable current source.
Precision Monolithics AN-20 (3 pg.)

Converters (cont)

10 **"3 IC 8-Bit Binary Digital to Process Current Converter with 4-20 mA Output"**
(REF-01, DAC-08, OP-14)
Delineates the construction of a process current converter operating from −5v and 23v supplies. Complete theory of operation followed by calibration procedures and a detailed parts list are included.
Precision Monolithics AN-21 (2 pg.)

11 **"Software Controlled A/D Conversion Using DAC-08 and the 8080A Microprocessor"**
(DAC-08, 8080A)
Describes software controlled, 8-bit A/D conversion using the DAC-08 and the 8080A. Subjects include I/O interface considerations, I/O control using memory mapping, and a successive approximation A/D conversion algorithm.
Precision Monolithic AN-22 (4 pg.)

12 **"D/A Converter Generates Hyperbolic Functions"**
(DAC-20)
Explains operating theory and design considerations of a two IC hyperbolic function generator. Includes circuit diagrams.
Precision Monolithics AN-23 (3 pg.)

13 **"Low Cost Four Channel DAC Gives BCD or Binary Coding"**
(DAC-08, DAC-20)
Describes the construction of a four-channel digital-to-analog converter using four multiplying DACs, a precision quad op amp, a system IC voltage reference, and a DIP-packaged thin-film resistor network.
Precision Monolithics AN-26 (4 pg.)

14 **"IC F/V Converters Readily Handle Other Functions, Such as F/V, A/D"**
(RC4151, RM4151)
Describes use of the 4151 as an F/V converter, a V/F converter, and an FSK demodulator.
Raytheon Semiconductor Application Note (6 pg.)

15 **"Digital-to-Analog Conversion Using the RCA CD4007A COS/MOS IC"**
(CD4007A)
Discusses resistance networks for DAC's and a voltage-follower amp for single-supply operation. Describes a 9-bit COS-MOS DAC.
RCA ICAN-6080 (6 pg.)

16 **"The 4151 Voltage to Frequency Converter"**
(RC4151, RM4151, RV4151)
Describes various uses of this v/f and f/v converter.
Raytheon Semiconductor Application Note (8 pg.)

17 **"Function and Application of 3½ Digit A/D Converter Set"**
(LD110, LD111)
Describes the operation of the LD110 digital processor and the LD111 analog processor. Various DVM circuits are shown including circuits for ratio, current, ac voltage and frequency measurements. A detailed error analysis is provided.
Siliconix AN74-1 (12 pg.)

18 **"More Applications of the LD110/LD114 ±3½ A/D Converters"**
(LD110, LD111, LD114)
Provides circuits to construct LCDs, multiplexed displays, gas discharge displays, and a DC-DC converter. Also details the differences between the LD110 and LD114.
Siliconix AN76-4 (8 pg.)

Converters (cont)

1 **"Applying the LD130 ± Digit A/D Converter"**
(LD130)
Discusses device features and its use in displays, interface, and instrumentation.
Siliconix AN76-5 (16 pg.)

2 **"Solve Your Measurement Problems"**
Discusses v/f and f/v converters and their use in data acquisition problems.
Teledyne Philbrick AN-20 (6 pg.)

3 **"Designing High Speed Data Acquisition Systems"**
Discusses the basics of data acquisition systems; focusing on sample-and-hold circuits and multiplexer modules.
Teledyne Philbrick AN-21 (12 pg.)

4 **"How to Specify and Test Voltage to Frequency and Frequency to Voltage Converters"**
Defines device parameters, specifications, and test techniques.
Teledyne Philbrick AN-22 (4 pg.)

5 **"Specifying and Testing Analog-to-Digital Converters"**
Defines the basic parameters, specifications, and test methods.
Teledyne Philbrick AN-24 (7 pg.)

6 **"Specifying and Testing Digital-to-Analog Converters"**
Defines basic parameters, specifications and test methods.
Teledyne Philbrick AN-25 (7 pg.)

7 **"Repetitive Mode Operation for Models 4109/4111 Integrating A/D Converters"**
(4109, 4111)
Runs through external trigger generator and sure start circuit schemes which are used when the devices must run without ceasing to convert.
Teledyne Philbrick AN-28 (2 pg.)

8 **"Specifying and Testing Sample-Hold Amplifiers"**
Defines various sample-hold amplifier parameters and outlines methods of testing for them.
Teledyne Philbrick AN-30 (5 pg.)

9 **"Modular V/F's and F/V's: Simple Solutions to Everyday Conversion Problems"**
Examines applications of V/F's and F/V's. Also demonstrates how accuracy can be improved with the addition of more components.
Teledyne Philbrick AN-32 (7 pg.)

10 **"Applications of the 8700 Series A/D Converters"**
(8700)
Supplies diagrams showing interface to autoranging circuits, to gas discharge displays, and to two independent displays, operated from one A/D.
Teledyne Semiconductor AN-9 (16 pg.)

11 **"Applications for the 9400 Voltage to Frequency/ Frequency to Voltage Converter"**
(9400)
Contains 25 block diagrams of applications in which the device is used.
Teledyne Semiconductor AN-10 (8 pg.)

Drivers

12 See also (Digital) Interface

13 **"Interfacing and Level-Shifting with the MEM4900"**
(MEM4900)
Describes device and application in a TTL to MOS interface buffer, a data selector, analog signal multiplexing, and an A/D de-multiplexer.
General Instrument Bulletin 1603 (3 pg.)

14 **"CMOS Line Drivers"**
States reasons for using CMOS line drivers.
National AN-158 (4 pg.)

15 **"Driving Burroughs' Bar Graph Display"**
Shows the use of comparators and flip-flops to drive these displays.
National DB-4 (2 pg.)

16 **"MOS Clock Drivers"**
(MH0007, MH0009, MH0012, MH0013)
Lists the characteristics of various MOS clock drivers and how they differ in their input stages.
National MB-9 (2 pg.)

17 **"PIN Diode Drivers"**
See listing under (Linear) Switches. (National)

18 **"Driver Circuits for the JFET Analog Switch"**
See listings under (Linear) Switches. (Siliconix)

19 **"Logic to Power Converter Circuits"**
(400-series, 500-series)
Covers the operation of the 400 and 500 high current driver series.
Sprague Electric TP 71-3 (6 pg.)

Followers

20 **"A Fast Integrated Voltage Follower with Low Input Current"**
(LM102)
Circuit description. Use of the LM102 for analog commutator, sample and hold ac amplifier and active filter applications.
National Linear Applications Handbook, Vol. I, AN-5 (11 pg.)

21 **"The LM110 — An Improved IC Voltage Follower"**
(LM110, LM210, LM310)
Compares LM102 and LM110 circuits. Shows diagrams of LM110 as a high pass active filter, high Q notch filter, bandpass filter, and low drift sample and hold circuit.
National Linear Applications Handbook, Vol. I, LB-11 (2 pg.)

22 **"Monolithic Operation Amplifiers — The Universal Linear Component"**
See (Linear) Amplifiers, Operational (National)

23 **"Applications for a New Ultra-High Speed Buffer"**
(LH0033, LH0033C)
Describes LH0033 fast voltage follow/buffer. Applications; high speed dual limit comparator for MOS logic, instrumentation shield/line driver, high speed sample and hold circuit, 4.5 MHz notch filter, high input impedance AC coupled amplifier, output buffer.
National AN-48 (4 pg.)

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General

1 "Nonlinear Circuits Handbook"
Covers principles, circuits, performance, specifications, testing and applications for multipliers, dividers, squares, log circuits, multifunction and rms-to-dc converters.
Analog Devices $5.95 (535 pg.)

2 "Function Circuits, Design and Applications"
Covers design theory and applications for such analog functions as multipliers, dividers, logarithmic amplifiers, exponentiators, RMS converters, and active filters. Includes notes on specifying and testing these functions.
Burr-Brown $21.00 (300 pg.)

3 "Intrinsically Safe Data Acquisition"
See listing under (Digital) CMOS (Burr-Brown)

4 "Custom IC Design Using I^2L Technology"
See (Digital) I^2L (Exar)

5 "Radiation Testing of Linear Microcircuits"
(μA702, μA709, μA710, μA711)
Describes tested performance of μA702 and μA709 operational amplifiers and μA710 and μA711 comparators after having been irradiated with fast neutrons of energies greater than 0.01 MeV.
Fairchild Application Note 195 (13 pg.)

6 "Using the MEM4962 Smoke Detector IC"
(MEM4962)
Describes the device and provides two exemplary applications in smoke sensing circuits.
General Instrument Bulletin 0601 (3 pg.)

7 "Alarm Circuit"
(MONOCHIP)
Discusses an alarm sensing circuit capable of driving a loud speaker or LED or triggering a logic level. The design and performance is described in detail, including all component values, layout and characteristics over the military temperature range.
Interdesign APN-1 (7 pg.)

8 "IC Crystal Oscillators"
(MONOCHIP)
Covers crystal oscillator basics and interfacing them with device.
Interdesign APN-4 (3 pg.)

9 "Rectifier Circuits for Linear IC's"
(MONOCHIP)
Discusses techniques for designing rectifiers using the components available on semicustom IC's. Design precautions are examined in detail and illustrative diode, peak detector, and averaging rectifier circuits are presented.
Interdesign APN-6 (7 pg.)

10 "Integrated High Speed Operational Amplifier"
(MONOCHIP)
Explains how modern high speed, high stability circuits can be constructed using semicustom IC technology. A representative op amp with a bandwidth of 40 MHz and an open loop gain of 10,000 is presented.
Interdesign APN-7 (7 pg.)

11 "Computer Analysis of Linear Semicustom IC's"
(MONOCHIP)
Describes a computer aided design program jointly developed by Interdesign and UCC. Illustrates the use of this program by analyzing a high performance integrated phase-locked loop.
Interdesign APN-12 (6 pg.)

General (cont)

12 "Solid State Gas/Smoke Detector Systems"
Describes semiconductor and ionization chamber systems with some discussion of the use of these with CMOS ICs.
Motorola AN-735 (9 pg.)

13 "Noise Sources"
Reviews noise basics. Includes discussion of resistive, capacitive, and inductive noise sources.
National FET Databook (3 pg.)

14 "The Noise Figure Fallacy"
Describes problems of defining and calculating the noise figure.
National FET Databook (2 pg.)

15 "Linear Applications, Vol. 1"
Feb. 1973, includes National application notes (AN) 1-6, 8, 10, 13, 15, 20, 21, 23, 24, 28-34, 38, 41, 42, 46, 48, 49, 51, 53, 54, 56, 63, 64, 69-72, 74, 75 and Linear Briefs (LB) 1-20, individually described elsewhere.
National $4.00 (432 pg.)

16 "Linear Applications, Vol. 2"
Includes National application notes (AN) 79, 81, 82, 87, 88, 97, 103, 104, 110, 115, 116, 125, 129, 132, 146, 147, 151, 153, 154, 156, 161, 162 and Linear Briefs (LB) 21-34, individually described elsewhere.
National $4.00 (256 pg.)

17 "CMOS Linear Applications"
See listing under (Digital) CMOS (National)

18 "Constant Current LED"
See listing under (Linear) Regulators (National)

19 "Surface Acoustic Wave Technology"
Presents surface acoustic wave fundamentals and use in delay lines, pulse compression filters, bandpass filters, oscillators and discriminators.
Plessey Semiconductor (10 pg.)

20 "Polarity Programmable Peak Detector"
Details a circuit that gives positive or negative peak detection and reset levels over a $\pm$10 V range.
Precision Monolithics AN-27 (2 pg.)

21 "Solid-State Devices Manual"
Provides tutorial information on discrete devices and ICs, with emphasis on consumer, hobbyist and experimenter applications.
RCA SC-16 $5.00 (750 pg.)

22 "Linear Integrated Circuits"
Basic circuit elements, fabrication, packaging, and interconnection techniques are discussed. Data and application information on RCA linear IC's is included.
RCA IC-43 $2.50 (416 pg.)

23 "Criteria for Choosing Resins and Evaluation Tests for Discrete and Integrated Power Devices in Plastic Packages"
Describes the criteria and experimental procedures used in the choosing of moulding resin for plastic packaged devices.
SGS-ATES Technical Note 132 (15 pg.)

LINEAR

Industrial Control

1 **"Electronic Controller with an Equilibrium Sustaining Mode"**
(3500 series)
Discusses a controller formed with two operational amplifiers in a pulse width modulation circuit with feedback. The feedback operates from a heater through the medium being heated to sense amplifiers.
Burr-Brown AN-63 (2 pg.)

2 **"Sequential Industrial Control Using the IM5200 FPLA"**
(IM5200)
Describes theory and advantages of using this FPLA. Example included.
Intersil Application Bulletin MB0001 (6 pg.)

3 **"Variable Speed Control System for Induction Motors"**
(MC673, MC688)
Describes control scheme implemented with discrete components and IC logic coupled by an LED and a photo transistor. Gives example of a circuit used to drive a Class F, 60 Hz, permanent-split, capacitor induction motor with a 13 oz. in. load rating.
Motorola AN-575A (5 pg.)

4 **"A ROM-Digital Approach to PWM-Type Speed Control of AC Motors"**
Describes a pulse width modulation scheme to control motor speed. Shows a CMOS-ROM system to provide variable frequency drive for 1, 2, or 3 phase motors.
Motorola AN-733 (12 pg.)

5 **"A Variable Frequency Control for 3ϕ Induction Motors"**
Describes a variable frequency, variable voltage drive system for 3-phase induction motor controls.
Motorola AN-766 (10 pg.)

6 **"Temperature Measurement Method Based on Matched Transistor Pair Requires No Reference"**
(MAT-01, OP-10)
Discusses properties of matched transistor pairs, then describes temperature measuring systems built with a matched pair, constant current sources, and a differential amplifier (OP-10)
Precision Monolithics AN-12 (8 pg.)

7 **"TCA600/900 and TCA610/910 Integrated Motor Speed Regulators"**
(TCA600, TCA610, TCA900, TCA910)
Introduces speed regulator basic and describes device performance. Portable and car mounted applications are depicted.
SGS-ATES Technical Note 113 (10 pg.)

8 **"Signetics Analog Manual"**
(μA723, LM381, LM382, MC1488, MC1489, MC1496, PA239, ULN2111, 521, 522, 526, 529, 540, 542, 550, 555, 560, 561, 562, 565, 566, 567, 592) Covers linear IC processing and design, operation amplifier characteristics and applications, voltage regulators, interface circuits, timers, communications circuits, consumer circuits, phase locked loops, telecommunication circuits and data sheets (321 pg.)
Signetics $7.00 (916 pg.)

Instrumentation

Also see Converters

Instrumentation (cont)

9 **"Application Notes AN-205"**
(FX205)
Describes use of the FX205 pseudo sinewave generator as a tone generator, tone-burst generator, a divide by eight sinewave source and an fsk generator.
Consumer Microcircuits of America AN-205 (16 pg.)

10 **"A Universal Sinewave Converter Using the XR2208 and XR2211"**
(XR2208, XR2211)
A circuit technique is described which can convert any periodic waveform into a low-distortion sinewave. The circuit operation is completely independent of input waveform amplitude and frequency as long as the input signal is periodic and can operate over a frequency range of 1 Hz to 100 kHz.
Exar AN-11

11 **"A Complete Function Generator System Using the XR2206"**
(XR2206)
A self contained function generator system is described, using the device. Complete circuit connection diagram, parts list and assembly instructions are given for a DC to 100 kHz self-contained function generator system with AM/FM capability and triangle, sine and square wave output.
Exar AN-14

12 **"A Simple Digital Voltmeter Using the AY5-3500 DVM Circuit"**
(AY5-3500)
Gives the schematics for the digital and analog circuitry needed to build a voltmeter with a $\pm$1.999 V full scale reading and capable of driving a 0.4" common anode LED display. Options available with minor modifications include BCD outputs, display hold, measurement initiate, and additional ranges of $\pm$0.999 V or $\pm$2.999 V.
General Instrument Bulletin 0901 (3 pg.)

13 **"A Deep Freeze Digital Thermometer Using the AY5-3500 DVM Circuit"**
(AY5-3500)
Provides circuit diagrams for a 0 to -30°C thermometer using a negative temperature coefficient thermistor as the sensing element and an AY5-3500 as the measuring and display device.
General Instrument Bulletin 0902 (3 pg.)

14 **"A Digital Thermometer Using the AY5-3507 Circuit"**
Supplies description and schematic for a -20 to 50°C (-4 to 122°F) thermometer that will display temperature in Farenheit or Centrigrade.
General Instruments Bulletin 0903 (2 pg.)

15 **"A Digital Voltmeter Using the AY-5-3507"**
(AY5-3507)
Gives schematics for the analog section, reference voltage generator, clock oscillator, and display circuitry required in addition to this logic IC to build a 3½ digit voltmeter.
General Instrument Microelectronics (5 pg.)

16 **"Waveform Generator"**
(MONOCHIP)
Describes using two of the devices in a wave form generator application that produces sine, triangle, and square wave outputs. Provides schematics and a discussion of performance.
Interdesign APN-8 (10 pg.)

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Instrumentation (cont)

1 **"A Precision Waveform Generator and Voltage Controlled Oscillator"**
(ICL8038)
Discusses the 8038 circuit and operation. Covers external adjustments, power-supply connections, frequency modulation, sweeping, and use in phase locked loops.
Intersil Application Bulletin A012 (8 pg.)

2 **"Everything You Always Wanted to Know About the 8038"**
(ICL8038)
Presents answers to the most frequently asked questions about the 8038 function generator and its applications.
Intersil A013 (4 pg.)

3 **"4½ Digit Panel Meter Demonstrator/Instrumentation Boards"**
(ICL8052A, ICL7103A)
Describes two versions of the complete circuit for a 4½ digit DPM with ±2.000 V full scale and LED readout.
Intersil A019 (8 pg.)

4 **"Low Cost Digital Panel Meter Designs"**
(ICL7106, ICL7107)
Supplies complete assembly instructions for Intersil's LCD and LED evaluation kits as well as descriptions of individual components.
Intersil A023 (6 pg.)

5 **"Building an Auto-Ranging DMM with the ICL7103A/8052A A/D Converter Pair"**
(ICL7103A, ICL8052A, ICL8007)
Describes the design and operation of two 10 μV resolution, 4½ digit auto-ranging DMMs using the 7103A/8052A pair.
Intersil A028 (6 pg.)

6 **"The Integrating A/D Converter"**
See (Linear) Converters (Intersil)

7 **"Instrumentation Amplifiers — They're Great Problem Solvers When Correctly Applied"**
(MN2200)
Covers basic operation and application considerations for instrumentation amplifiers.
Micro Networks AN202 (4 pg.)

8 **"A 3½ Digit DVM Using an Integrated Circuit Dual Ramp System"**
(MC1405, MC14435)
Describes a complete digital voltmeter based on the MC1405/14435 device pair. Includes input buffers and autopolarity.
Motorola AN-746 (6 pg.)

9 **"Applications of MC1405/MC14435 in Digital Meters"**
(MC1405, MC14435)
Provides a detailed applications reference for this two chip, dual slope A/D converter system.
Motorola AN-748 (18 pg.)

10 **"Solid State Altimeter for Transponder Applications"**
(LX3702)
Describes a solid state altimeter using a pressure transducer. The unit provides an altitude transmission code for use with transponders, plus digital readout.
National AN-109 (8 pg.)

Instrumentation (cont)

11 **"Wide Range Function Generator"**
Construction of a function generator for sine waves as well as square and triangular waveforms that operates below 10 Hz up to 1 MHz, with usable output to approximately 2 MHz. Design technique, circuit design, and construction directions.
National AN-115 (4 pg.)

12 **"Dual Polarity 3½ Digit DVM Realized with Simple CMOS Interface"**
(ADC3711, LF11300)
Describes an auto-zero, auto-polarity 3½-digit DVM using the LF-11300 and the MM74C928 (ADC3711).
National AN-165 (2 pg.)

13 **"LM2907, LM2917 Tachometer/Speed Switch Building Block Applications"**
(LM2907, LM2917)
Covers basic circuit and use. Applications illustrated include: speed switch, analog display driver, automotive tachometer, motor speed controls, skid sensor, A/D converter, frequency doubler.
National Linear Applications Handbook, Vol. II, AN-162 (16 pg.)

14 **"RMS Converters and Their Applications"**
(LH0091)
Covers RMS converter basics and specifications. Sketches applications including spectrum analysis, harmonic distortion, noise, vibration analysis, and DVM uses.
National AN-180 (4 pg.)

15 **"A Digital Multimeter Using the ADD3501"**
(ADD3501)
Describes a 3½ digit multimeter capable of measuring ac and dc voltages, currents and resistance with the device. Includes circuit diagram.
National Semiconductor AN-202 (4 pg.)

16 **"A Fully Differential Input Voltage Amplifier"**
(LM3900)
Describes operation of instrumentation amplifier built with LM3900. Also shows how a transducer bridge amplifier system can be developed with LM3900.
National Linear Applications Handbook, Vol. I, LB-20 (2 pg.)

17 **"Precise Tri-Wave Generation"**
(LM118, LM119)
Describes triangle-wave generator consisting of the LM118 integrator and two LM119 comparators. Discusses applications including VCO, regulator and operational amplifier testing.
National Linear Application Handbook, Vol. II, LB-23 (2 pg.)

18 **"3½ Digit DVM Demonstrator Board"**
(LD110, LD111)
Supplies the schematics, parts-list and art-work for a DVM demonstrator board.
Siliconix DA74-1 (4 pg.)

19 **"LD130 ±3 Digit DVM Demonstrator Board"**
(LD130)
Presents a DVM circuit and the PC board layout used to build a demonstrator board.
Siliconix DA76-2 (2 pg.)

20 **"Build an Autoranging DMM with the LD130 A/D Converter"**
(LD130)
Discusses the construction of a DMM using this device.
Siliconix DA76-3 (7 pg.)

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Instrumentation (cont)

1 **"Build a Portable 0 to 99.9°F Liquid Crystal Display Thermometer"**
(DF411, LD130)
Furnishes all pertinent equations, component lists, schematics, and the PC foil pattern need to build a battery operated thermometer.
Siliconix DA77-1 (4 pg.)

2 **"LD120/LD121 4½ Digit DVM"**
(LD120, LD121)
Details construction of a DVM using these devices.
Siliconix DA77-2 (4 pg.)

3 **"A Fully Integrated Motion Detector"**
(ULN-2232)
Discusses circuit, system layout, and basic operation of a fully integrated motion detector for use in security systems, video games, and toys.
Sprague TP78-4 (9 pg.)

4 **"EPN2100 Thermal Printer"**
(EPN2100)
Detailed discussion of this solid state thermal printer and its interface requirements.
Texas Instruments Application Report CA-163 (6 pg.)

5 **"EPN2500 Thermal Printer"**
(EPN2500, SN74492, SN74495, TMS2502)
Discusses this thermal printer and its interface requirements. Includes a description of the SN75495 Row Driver and the SN75492 Digit Driver to interface the printhead to MOSFET logic circuits, and the TMS2502 character generator for providing alphanumeric characters.
Texas Instruments Application Report CA-175 (10 pg.)

Modulators

6 **"MC1596 Balanced Modulator"**
(MC1496, MC1596)
Describes device operation and applications, including modulators and demodulators for AM, SSB, and suppressed carrier AM, frequency doublers; and HF/VHF double balanced mixers.
Motorola AN-531 (12 pg.)

7 **"Simplifying Converter Design with a New Integrated Regulating Pulse Width Modulator"**
(SG1524, SG2524, SG3524)
Describes various functions within the device and describes such applications as a low current polarity converter, a DC to DC converter, and a +5 to ±15V flyback converter.
Silicon General (7 pg.)

8 **"Deadband Control with the SG1524 Regulating Pulse Width Modulator Circuit"**
(SG1524, SG2524, SG3524)
Discusses techniques to control the amount of deadband in push-pull inverter applications.
Silicon General Linear Brief 6 (1 pg.)

Multipliers

9 **"Multiplier Application Guide"**
(AD530, AD531, AD532, AD533, AD534, AD536)
Explains multiplier basics, upkeep, and use in a variety of applications including instrumentation functions, signal generators and filters, and to augment the performance of other circuits.
Analog Devices (40 pg.)

Multipliers (cont)

10 **"AD530 Complete Monolithic Multiplier, Divider, Square Rooter"**
(AD530)
Describes the device, its circuit, external connections and adjustments. Applications include use in a precision rectifier, a phase sensitive demodulator, an automatic level control, a voltage controlled filter, a voltage controlled oscillator, an amplitude modulator and a frequency discriminator.
Analog Device Technical Bulletin (11 pg.)

11 **"A Practical Guide to Applying IC Multipliers"**
Describes theory, gives definitions, covers use in dividers, squares, vector summation, rms to dc conversion, 2ϕ oscillator, and balanced modulators.
Analog Devices (11 pg.)

12 **"Reducing the Total Error of the AD530, AD531, AD532, and AD533 Multipliers"**
(AD530, AD531, AD532, AD533)
Describes method of empirically reducing errors using external resistors.
Analog Devices Application Brief (2 pg.)

13 **"Analog Modules Multiply User's Options"**
Discusses various types of multipliers, logarithmic converters, dividers and square rooters, peak detectors and comparing circuits. Applications: electron beam welder, 3-mode carriage control, position control, fog visionmeter, optical measuring system, and lab pressure standard.
Burr-Brown AN-55 (6 pg.)

14 **"A Primer on Analog Multiplier Specifications"**
Discusses dc and dynamic performance specifications, including output and input offset, gain error, linearity, small signal and full power frequency response, output slewing rate, and settling time.
Burr-Brown AN-51 (6 pg.)

15 **"Analog Shaping"**
(4301)
Describes the use of the 4301 multifunction circuit which has the transfer function XY/Z. Includes rms to dc conversion, exponentiation, trigonometric functions, vector computation, and use as a log amp.
Burr-Brown AN-70 (5 pg.)

16 **"Function Circuits, Design and Applications"**
See listing under (Linear) General (Burr-Brown)

17 **"A-8595 Operation and Applications Information"**
(A8495, A8595)
Reviews device theory and design. Applications include a basic multiplication circuit, a squaring circuit, and a divide circuit.
Intech/FMI (16 pg.)

18 **"Log/Lin Multiplier"**
(MONOCHIP)
Describes an IC multiplier which achieves low noise and distortion. Covers all phases of development from initial concept and breadboarding to integration in an audio sweep function generator.
Interdesign APN-3 (11 pg.)

19 **"Analysis and Basic Operation of the MC1595"**
(MC1495, MC1595)
Gives equations for the analysis of this linear four-quadrant multiplier and discusses characteristic performance. Covers multiplication, division, mean squares, square roots, roots and powers.
Motorola AN-489 (14 pg.)

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Multipliers (cont)

1 **"Wideband Amplifier/Multiplier"**
(SG1402)
Operation and applications of the SG1402. Describes use as a single-ended variable gain amplifier, a modulator, and a demodulator.
Silicon General Linear IC Product Guide (4 pg.)

2 **"Linear-Antilog Voltage Controlled Amplifiers"**
(SSM2000, SSM2020)
Discusses control circuits, voltage controlled amplifiers, and a four quadrant multiplier among other applications.
Solid State Music (9 pg.)

Phase Locked Loops

3 **"Precision PLL System Using the XR2207 and the XR2208"**
(XR2207, XR2208)
Defines phase locked loop parameters and describes this two-chip PLL system. Includes circuit interconnections for both single supply and split-supply operation. Also gives PLL design equations.
Exar AN-06 (6 pg.)

4 **"Sinusoidal Output from XR-215 Monolithic PLL Circuit"**
(XR215)
Discusses obtaining a sinusoidal output signal which is synchronized to a desired reference or clock output using the device. Provides schematics of device and application.
Exar AN-09 (2 pg.)

5 **"A Wide Tracking Range Precision PLL System Using the XR2212 and XR4151"**
(XR2212, XR4151)
A two-chip PLL system is described which offers extremely wide tracking range without harmonic locking.
Exar AN-12

6 **"The μA758, a Phase-Locked Loop FM Stereo Multiplex Decoder"**
See listing under (Linear) Consumer, AM/FM. (Fairchild)

7 **"Introduction to the Phase Locked Loop"**
(HA-2820)
General discussion of phase locked loops. Describes applications including a bandpass filter, FM receivers, data modems and synchronizers, a motor speed control, and a frequency synthesizer. Discusses features of HA-2800 and 2820 PLL.
Harris Application Note 601 (7 pg.)

8 **"A General Analysis of the Phase Locked Loop"**
Discusses a linear model, stability considerations and steady state response for phase locked loops.
Harris Application Note 602 (8 pg.)

9 **"The HA-2820/2825 Low Frequency Phase Locked Loop"**
(HA-2820, HA-2825)
Explains circuitry of these phase locked loops in 0.1 Hz to 3 MHz operation. Discusses methods for obtaining parameters of a linear model from device's performance curves. External connections are illustrated with an FM demodulator circuit.
Harris Application Note 605 (7 pg.)

10 **"MTTL and MECL Avionics Digital Frequency Synthesizer"**
Describes phase detector, emitter coupled oscillator, prescaler, programmable counter and gives phase locked loop analysis, for a 118 MHz to 136 MHz synthesizer.
Motorola AN-532A (10 pg.)

Phase Locked Loops (cont)

11 **"Phase-Locked Loop Design Fundamentals"**
(MC4016, MC4024, MC4044, MC4316, MC4324, MC4344)
Outlines fundamental design concepts for phase locked loops implemented with ICs. Gives equations using Laplace Transforms needed to evaluate the basic loop performance and briefly describes a design using MC4000 series devices.
Motorola AN-535 (11 pg.)

12 **"A New Generation of Integrated Avionic Synthesizers"**
Discusses several different types of servo phase locked loop systems and describes a synthesizer for avionic equipment.
Motorola AN-553 (9 pg.)

13 **"An ADF Frequency Synthesizer Utilizing Phase-Lock-Loop ICs"**
(MC1648, MC3062, MC4016, MC4018, MC4044, MC7400)
Describes circuit for a synthesizer suitable for the local oscillator function in aircraft Automatic Direction Finder equipment. Covers programming, trouble shooting, power supply requirements, performance, circuit modifications, and circuit construction.
Motorola AN-564 (9 pg.)

14 **"Crystal Switching Methods for MC12060/MC12061 Oscillators"**
(MC12060, MC12061)
Discusses methods of using diodes as rf switches to select crystals for these oscillators. The techniques are useful for electronic selection of one of a group of crystals with minimum disturbance to the series resonant frequency of the selected crystal.
Motorola AN-756 (5 pg.)

15 **"A Medium Cost PLL Varactor Tuning System Utilizing Off-the-Shelf Logic"**
See listing under (Linear) Consumer, TV (Motorola)

16 **"A Phase-Locked Loop Tuning System for Television"**
See listing under (Linear) Consumer, TV (Motorola)

17 **"The Phase-Locked Loop IC as a Communication System Building Block"**
(LM565, LM1496, LM1596)
Discusses basic phase locked loop operation, design considerations, noise performance and describes the LM565 circuit. Applications: IRIG channel demodulator, FSK demodulator, and weather satellite picture demodulator.
National Linear Applications Handbook, Vol. I, AN-46 (12 pg.)

18 **"SL650 Phase-Locked Loop Applications"**
(SL650, SL651)
Describes the circuit and application of this device that can operate to 0.5 MHz. Applications: Modulators-AM, FM, FSK, PAM, SCAM, tone burst, phase shift, delta, PWM, Waveform Generators-sine, triangle, mark/space ratio, staircase: Demodulators; Modem Systems, and a Digital Voltmeter.
Plessey Semiconductor SL650 Applications (32 pg.)

19 **"The RCA COS/MOS Phase-Locked-Loop: A Versatile Building Block for Micro-Power Digital and Analog Applications"**
(CD4046A)
Discusses PLL basics, characteristics of device, and circuit elements. Describes application in FM demodulation, a frequency synthesizer, split-phase synchronization and decoding, and PLL lock detection.
RCA ICAN-6101 (4 pg.)

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Phase Locked Loops (cont)

1 **"Applications of the COS/MOS CD4059A Programmable Divide-by-N Counter: Digital Frequency Synthesis for FM Tuners and CB Transceivers"**
(CD4059)
Discusses frequency synthesis using the counter for an FM digital tuner and a CB transceiver.
RCA ICAN-6374 (12 pg.)

2 **"Low-Power Digital Frequency Synthesizers Utilizing COS/MOS ICs"**
(CD4000 Series)
Reviews digital phase-locked loops. Describes their implementation with CMOS for use in FM receiver synthesizers, both heterodyne and prescaling types.
RCA ICAN-6716 (15 pg.)

Photosensitive Devices

3 **"Light Sense"**
Covers optoelectronic sensors and systems including light activated switches and selfscanned photodiode arrays.
Integrated Photomatrix $6.00 (147 pg.)

4 **"Applications of Reticon Photodiode Arrays in Electron and X-Ray Detectors"**
(RL Series)
Describes the use of self-scanning photodiode arrays for detecting soft X-rays (1 to 10A) and electrons in the 10 to 100 KEV range.
Reticon Application Note 101 (4 pg.)

Power Control

5 **"A Monolithic Zero-Crossing AC Trigger (Trigac) for Thyristor Power Controls"**
(μA724)
Describes the μA742 zero-crossing ac trigger, which minimizes radio frequency interference generation. Discusses the circuit and operation of this device. Covers application with an SCR in a half wave circuit, full wave circuits, isolated system connections, and multi-phase power systems.
Fairchild Application Note 208 (5 pg.)

6 **"Servo Motor Drive Amplifiers"**
Discusses design of transformerless, AC servo amps using power Darlington transistors and IC op amps. Describes two power amplifiers, one using a 28 V power supply, the other, high voltage transistors. Also covers four op amp preamps and 90° phase shifters.
Motorola AN-590 (7 pg.)

7 **"Phase Control of AC Power with the SL440"**
(SL440)
Describes the operations of the SL440 power control circuit, and supply requirements. Applications include use with inductive loads, three phase systems, lighting, heating, motor and power supply control.
Plessey Semiconductor (38 pg.)

8 **"Some Applications of a Programmable Power Switch/Amplifier"**
(CA3094)
Brief circuit description of CA3094. Device delivers three watts average power, 10 watts peak power to external load. Applications include Class A power amplifiers and driver amplifiers for complementary transistors, wideband power multivibrators, oscillators, comparators, voltage regulators, analog timers, and motor-speed controllers.
RCA ICAN-6048 (12 pg.)

Power Control (cont)

9 **"Triac Power Controls for Three-Phase Systems"**
(CA3059)
Describes basic approach to designing triac control circuits for use in the switching of three-phase power. Outlines basic design rules and describes CA3059 zero-voltage switch. Discusses methods of isolation of dc logic circuitry. Covers recommended configurations for power control circuits.
RCA AN-6054 (6 pg.)

10 **"Features and Applications of RCA IC Zero-Voltage Switches"**
See listing under (Linear) Switches. (RCA)

11 **"ICs for Phase and Burst Control of SCR or Triac"**
(L120, L121)
Examines 2 ICs which are suitable for SCR and Triac firing. Description includes diagrams, equations, and applications in ON-OFF control and proportional control.
SGS-ATES Technical Note 116 (12 pg.)

12 **"A Monolithic Amplifier-Detector SCR Firing Circuit"**
(ULN-2300)
Describes the operation of the ULN-2300 linear differential amplifier with integral SCR. Covers response, impedance characteristics and closed loop charactertistics, open loop gain vs. temperature, and describes use as a sensitive control, as a drive amplifier in a typical control system and as a control for counters, relays, motors.
Sprague Electric TP69-4 (12 pg.)

13 **"Applications of High-Voltage/High-Current Monolithic Interface Circuits"**
(060, 400 Series, 500 Series)
Application of Series 060 Dual Darlington Switch and Series 400/500 Power Drivers in aircraft lamp drive circuit, solenoid printer, and 4-phase bipolar stepping motor.
Sprague Electric TP 72-4 (5 pg.)

Power Supplies

14 **"Power Supply Design Using the ICL8211 and ICL8212"**
(ICL8211, ICL8212)
Describes use of these devices as positive and negative voltage regulators, constant current sources, high voltage and overvoltage protection circuits, supply window detectors and power failure-shutdown systems.
Intersil A027 (8 pg.)

15 **"Fast IC Power Transistor with Thermal Protection"**
(LM195)
Circuit design of the LM195 IC power transistor, a three terminal device with safe area protection plus current and thermal limiting. Applications: 6 amp variable output switching regulator, 1 amp positive and negative voltage regulators, time delay circuit, and optically controlled switch, power amplifier and voltage follower.
National AN-110 (6 pg.)

16 **"General Purpose Power Supply"**
(LM395)
Diagrams a 25V, 10A supply using parallel LM395s for pass elements.
National Linear Applications Handbook, Vol. II, LB-28 (2 pg.)

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Preamplifiers

1 **"Audio Preamplifiers"**
(MONOCHIP)
Provides schematics and parameters for using the device in three separate preamplifier configurations.
Interdesign APN-11 (6 pg.)

2 **"Applications of the μA739 and μA749 Dual Preamplifier Integrated Circuits in Home Entertainment Equipment"**
See listing under (Linear) Consumer, Audio. (Fairchild)

3 **"Audio Handbook"**
See listing under (Linear) Consumer, Audio (National)

4 **"LM381 Low Noise Dual Preamplifier"**
(LM381)
Describes the circuit. Discusses application as various tape amplifiers, phono preamplifier, and an audio mixer.
National AN-64 (12 pg.)

5 **"LM381A Dual Preamplifier for Ultra-Low Noise Applications"**
(LM381A)
Gives detailed description of circuit operations of LM381A.
National AN-70 (4 pg.)

6 **"IC Preamp Challenges Choppers on Drift"**
(LM108A, LM121)
Describes circuit of the LM121 preamplifier and discusses offset balancing, achieving of low drift, and typical operating performance. Also covers effects of the associated operational amplifier citing the LM108A as an example.
National AN-79 (8 pg.)

7 **"Versatile IC Preamp Makes Thermocouple Amplifier with Cold Junction Compensation"**
(LM321, LM308A)
Discusses use of LM321 preamp with LM308A operational amplifier to form a precision, low-drift operational amplifier that also acts as a cold junction compensator.
National Linear Application Handbook, Vol. II, LB-24 (2 pg.)

Regulators

8 **"The Voltage Regulator Applications Handbook"**
(μA104, μA105, μA109, μA723, μA7600, μA7800, μA78L00, μA78M00, μA79E00)
Gives specifications and parameters for various IC regulators and includes a selection guide. It devotes two chapters to each major regulatory family, the first chapter describes design and electrical characteristics, the second discusses electrical and thermal considerations which are useful as application guidelines.
Includes appendices covering switching regulator and power supply design and a guide to the selection and operation of suitable power transistors. Applications of 7800 and 78M00 include fixed output, current and dual polarity regulators.
The 79E00 applications include use as a high current negative voltage regulator. The 723 is discussed in 150 mA maximum, positive shunt regulators with high line rejection or high input voltage, floating positive regulators, medium/high output current negative regulators, and several other applications.
The 104, 105, and 109 applications include high current, switching and floating regulators.
Fairchild Voltage Regulator Applications Handbook (96 pg.)

Regulators (cont)

9 **"Resolving the Problems of Switching Mode Power Supplies with the ZN1066"**
(ZN1066)
Describes switching mode power supplies and problems involved in using, including current limit and switching transistor protection, low voltage cutoff, and impulse starting.
Ferranti (20 pg.)

10 **"Hybrid Voltage Regulators"**
(42050 Series, 42051 Series)
Describes device and discusses current foldback and thermal considerations. Also notes application precautions.
Micropac (9 pg.)

11 **"Designing Digitally-Controlled Power Supplies"**
(MC1406, MC1408, MC1466, MC1723)
Discusses two approaches to designing power supplies, one using the MC1723 voltage regulator, the other using the MC1466 floating regulator with optoelectronic isolation. Also discusses BCD-to-binary converter and memory options.
Motorola AN-703 (8 pg.)

12 **"A New Approach to Switching Regulators"**
Describes a 24 volt 3 ampere switching mode supply which operates at 20 kHz from a 120 volt AC line with 70% efficiency. Briefly discusses load-line shaping to reduce power losses and to reduce noise.
Motorola AN-719 (11 pg.)

13 **"Voltage Regulator Handbook"**
(MC78L00, MC78M00, MC7700, MC7800, MLM109, MLM209, MLM309, MC79L00, MC7900, MLM105, MLM205, MLM305, MLM104, MLM204, MLM304, MC1723, MC1469, MC1569, MC1463, MC1563, MC1468, MC1568, MC1466, MC1566, MC3420, MC3423, LM117, LM317, LM123, LM323)
Discusses basic voltage regulator theory and design including such relevant topics as series pass elements, heatsinking, layout, input power supply design, reliability, and troubleshooting. Also contains product data sheets.
Motorola $2.50 (202 pg.)

14 **"A Versatile, Monolithic Voltage Regulator"**
(LM100)
Circuit operation. Applications for the LM100 between 2 v to 30 v (up to 2 amps with two external transistors) are discussed. Includes high power, switchback current limiting, negative voltage, temperature compensating, and switching regulators.
National Linear Applications Handbook, Vol. I, AN-1 (11 pg.)

15 **"Designing Switching Regulators"**
(LM100)
LM100 applications discussed include high current, driven switching, current limiting, negative and high voltage regulators, as well as switching, and linear regulator combinations.
National Linear Applications Handbook, Vol. I, AN-2 (12 pg.)

16 **"Tracking Voltage Regulators"**
(LM104, LM105, LM204, LM205, LM304, LM305)
Describes adjusting several regulator voltages with one potentiometer, tracking positive and negative regulators using the LM104 as an amplifier, and tracking regulators with different output voltages.
National Linear Applications Handbook, Vol. I, LB-7 (2 pg.)

Regulators (cont)

1 **"New Uses for the LM100 Regulator"**
(LM100)
Applications include shunt regulator, switching regulator with overload shutoff, temperature controller, power amplifier, SSB transmitter, light-intensity regulator, and photomultiplier tube supply.
National Linear Applications Handbook, Vol. I, AN-8 (12 pg.)

2 **"IC Regulators Simplify Power Supply Design"**
(LM104, LM105, LM204, LM205, LM304, LM305)
Describes use of LM104 and LM105, in 0.2 and 2A regulator circuits. Provides circuit construction hints.
National Linear Applications Handbook, Vol. I, LB-10 (2 pg.)

3 **"High Stability Regulators"**
(LM108A, LM109, LM208A, LM209, LM308A, LM309)
Describes design and gives schematics for high stability positive and negative regulators using LM109 and LM108A.
National Linear Applications Handbook, Vol. I, LB-15 (2 pg.)

4 **"Designs for Negative Voltage Regulators"**
(LM104, LM204, LM304)
Describes the LM104 and covers pitfalls that cause unexpected failures as well as protection schemes. Includes discussions of high current regulators, symmetrical power supplies, high voltage regulators, switching and high current switching regulators, and driven switching regulators.
National Linear Applications Handbook, Vol. I, AN-21 (16 pg.)

5 **"IC Provides On-Card Regulation for Logic Circuits"**
(LM109, LM209, LM309)
Discusses design of regulators in general and describes the LM109. Covers application as a fixed 5V regulator, adjustable-output regulator, current regulator and high stability regulator.
National AN-42 (6 pg.)

6 **"LM125/LM126/LM127 Precision Dual Tracking Regulators"**
(LM125, LM126, LM127)
Circuit description, operation and applications, including current boosting, are discussed along with charts depicting external current limiting characteristics and a discussion of foldback current limiting. Electronic turn-off of the output without removing the input voltage is also described.
National AN-82 (15 pg.)

7 **"LM340 Series — Three Terminal Positive Regulators"**
(LM340)
Describes this 1 ampere regulator circuit. Applications: constant current source, high current regulator with short circuit current limit, 5 v regulator for TTL, adjustable output voltage regulators, tracking dual regulator, and high voltage regulators.
National AN-103 (12 pg.)

8 **"Constant Current LED"**
(NSL4944)
Describes how this two lead LED/IC device can be used not only as an indicator but also as a rectifier and constant current source.
National AN-153 (4 pg.)

9 **"Applications for an Adjustable IC Power Regulator"**
(LM117, LM217, LM317)
Covers basic LM117 circuit operation. Shows basic applications plus use for multiple outputs, current regulation, constant voltage/constant current, and a voltage to 2-wire (10-50 ma) current transmitter.
National AN-178 (4 pg.)

Regulators (cont)

10 **"Three-Terminal Regulator is Adjustable"**
(LM117, LM217, LM317)
Covers basic LM117 circuit operation, overload protection circuits and operating considerations. Includes applications with logic shutdown, multiple regulators with single control, switching regulators and battery chargers.
National AN-181 (3 pg.)

11 **"Improving Power Supply Reliability with IC Power Regulators"**
(LM117, LM217, LM317)
Describes various regulator circuit design practices to improve system reliability.
National AN-182 (3 pg.)

12 **"Worst Case Power Dissipation in Linear Regulators"**
(LM100, LM104, LM200, LM204, LM300, LM304)
Discusses problems of excessive dissipation in regulators and suggests solutions using LM100 and LM104.
National Linear Applications Handbook, Vol. I, LB-3 (2 pg.)

13 **"Adjustable Three-Terminal Regulator for Low Cost Battery Charging Systems"**
(LM317)
Discusses the ability to adjust the output of the LM317 voltage regulator as it relates to battery charging systems.
National LB-35 (2 pg.)

14 **"A Novel FET Micropower Voltage Regulator"**
Depicts the building of a micropower voltage regulator using FETs.
National FET Databook (2 pg.)

15 **"Voltage Regulator Handbook"**
(LM109, LM120, LM123, LM125, LM126, LM127, LM145, LM340, LM341, LM342, LM7800, LM78L00)
Covers product selection; heat flow and thermal resistance; commercial and custom heat sinks; applications of positive, negative and dual regulators; power supply design and includes data sheets for the product families listed above.
National Voltage Regulator Handbook, $3.00 (139 pg.)

16 **"The 4195 Regulator"**
(RC4195, RM4195)
Describes application as a ±15 v, 100 ma regulator; a ±2.5 a regulator; a ±15 to ±50 v unit, or a complementary ±3 to ±27 v device.
Raytheon Semiconductor Application Note (9 pg.)

17 **"Applications of the CA3085 Series Monolithic IC Voltage Regulators"**
(CA3085)
Circuit description of positive regulators with output currents up to 100 milliamperes from −55°C to +125°C. Applications include high-current and constant-current regulators; switching, dual-tracking and high-voltage regulators. Use as a general purpose amplifier, and various methods of current limiting are mentioned.
RCA ICAN-6157 (11 pg.)

18 **"A Switching Regulator Using an RCA P-N-P Power Darlington Transistor"**
(CA3085)
Gives a detailed discussion of a 28 v input, 4-16 v, 11 a, switching regulator.
RCA AN-6195 (8 pg.)

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Regulators (cont)

1 **"Using a Dual-Polarity, Tracking Voltage Regulator"**
(SG1501, SG2501, SG3501)
Describes the circuit and use of the SG1501 series of dual regulators.
Silicon General Applications Bulletin 1 (6 pg.)

2 **"Current-limited and Voltage-regulated Battery Charger"**
(TL430)
Outlines construction of a battery charger that will rejuvenate a totally discharged 44 ampere-hour lead-acid battery in 3 hours.
Texas Instruments CA-194 (9 pg.)

3 **"Designing Switching Voltage Regulators with the TL497"**
(TL497)
Covers principles of operation and use as a step-down, step-up or inverting regulator.
Texas Instruments Application Report CA-189 (16 pg.)

Switches

4 **"Touch Control Circuits for Capacitance Switching"**
(S9260 Series)
Discusses using the devices to replace mechanical switching systems. Covers noise immunity, determining touch switch sizes, multiplexed operation, and touch control panel material among other topics.
American Microsystems (16 pg.)

5 **"Applications of the μA742 TRIGAC — A Zero Crossing AC Trigger"**
(μA742)
Describes this TRIGAC circuit. Includes a discussion of the transfer characteristics and performance plus operation from ac and dc supplies. Applications: 110 V ac single threshold control; single phase, 110 V ac dual threshold control with hysteresis; 110 V ac dual threshold control with time proportioning; with time proportioning for Y or Δ loads; operating with transformer isolation between control circuit and ac line; output pulse amplifier with transformer; output pulse inverter; period extender for time proportioning; initial cycle delay; sensor failure detection circuit; time delay "relay" circuit; 208 V ac dual threshold control 110 V ac, 400 Hz dual threshold control with single TRIGAC for Y loads.
Also includes a section listing parts and component location diagrams for these applications and discusses operation with a fixed dc supply. Covers use of the TRIGAC with nonresistive loads, discusses thyristor cells, and full wave output power switches for use with the device.
Fairchild (30 pg.)

6 **"Applications of Ultra-High Speed N-Channel MOSFET Switches"**
(MEM780)
Presents design guidelines, considerations, and practical circuits for analog multiplex switching.
General Instrument Bulletin 1602 (6 pg.)

7 **"Understanding and Applying the Analog Switch"**
(IH5001, IH5009, IH5025, IH5040)
Compares parameters of analog switches. Applications of several switch families are discussed, including 3-channel differential multiplexer, gain programmable amplifier, gain ranging circuit, sample and hold circuit.
Intersil Application Bulletin A003 (16 pg.)

Switches (cont)

8 **"The IH5009 Series of Low Cost Analog Switches"**
(IH5009 Series)
Describes circuit parameters, logic compatibility, and virtual ground switching applications including 4-channel multiplexer, gain ranging circuit, gain programmable amplifier and 16-channel multiplexer.
Intersil Application Bulletin A0004 (8 pg.)

9 **"A New CMOS Analog Gate Technology"**
General discussion of "latch up." Describes "floating body" process, which eliminates this problem.
Intersil Application Note A006 (2 pg.)

10 **"Application of the MC3416 Crosspoint Switch"**
(MC3416)
Describes operation and use of this 4 × 4 balanced crosspoint switch in telephone applications including PABX. Appendices cover dielectric isolation, SCR action and testing.
Motorola AN-760 (15 pg.)

11 **"High Speed MOS Commutators"**
(MM451, MM453, MM454)
Discusses the lowered threshold voltages in commutators, on and off resistances, switching speed, noise and high-frequency noise control.
National Linear Applications Handbook, Vol. I, AN-28 (8 pg.)

12 **"Analog-Signal Commutation"**
(MM450, MM451, MM454, MM550, MM551, MM552)
Describes dc characteristics involved in MOS IC switching of analog signals when the signal input range varies between ± 10 v.
National Linear Applications Handbook, Vol. I, AN-33 (6 pg.)

13 **"Applications of MOS Analog Switches"**
(LH0014, LH0019)
Discusses basic commutation circuits and describes the use of the LH0014 and LH0019 in linear amplifier applications, including reset functions and chopper circuits. Covers use of MOS switches as suppressed carrier double-sideband modulators and double-sideband demodulators. Also describes a circuit for a phase-locked loop AM-FM detector without tuned circuits.
National Linear Applications Handbook, Vol. I, AN-38 (8 pg.)

14 **"PIN Diode Drivers"**
(DH0035, DH0035C)
Describes PIN diode switching requirements and application of DH0035 as a driver. Includes discussion of anode ground and cathode ground designs and of repetition rate considerations.
National AN-49 (6 pg.)

15 **"High Speed Analog Switches"**
(AM1000, AM1001, AM1002)
Discusses time domain multiplexing, current mode multiplexing, the switching characteristics of the AM1000 JFET switches, and drive circuits.
National AN-53 (6 pg.)

16 **"Features and Applications of RCA IC Zero-Voltage Switches"**
(CA3058, CA3059, CA3079)
Discusses zero-voltage switch operation in general. Operation primarily with thyristors in ac power control and switching applications, including electric heating, oven/broiler control, machine control, light control and industrial systems.
RCA ICAN-6182 (6 pg.)

Switches (cont)

1 **"Applications of the RCA CA3062 IC Photo-Detector and Power Amplifier in Switching Circuits"**
(CA3062)
Describes circuit operation and application in a latched memory circuit, a light activated triac control, a triac control with automatic shut off and alarm, and a triac intrusion alarm system.
RCA ICAN-6538 (6 pg.)

2 **"Some Applications of a Programmable Power Switch/Amplifier"**
See listing under (Linear) Power Control. (RCA)

3 **"FETs as Analog Switches"**
General discussion of FET operation: detailed discussion of factors affecting switch performance, including specific load problems and applicable driver circuits.
Siliconix AN72-2 (12 pg.)

4 **"IC Multiplexer Increases Analog Switching Speeds"**
(DG506, DG181)
Describes single and two level IC multiplexing systems, including the advantages and disadvantages of each.
Siliconix AN73-2 (5 pg.)

5 **"Switching High-Frequency Signals with FET Integrated Circuits"**
(DG133, DG171, DG181, DG200)
Discussion of DG133/171/181/200 as rf switches. Gives equivalent circuits. "Off" isolation and "On" performance data. Applications: control of video monitor and switching between two video cameras.
Siliconix AN73-3 (16 pg.)

6 **"Driver Circuits for the JFET Analog Switch"**
Discussion and comparison of resistor-coupled diode charge transfer, space transistor charge transfer, and switched resistor driver circuits for JFET switches.
Siliconix AN73-5 (12 pg.)

7 **"Analog Switches in Sample and Hold Circuits"**
Covers the effects of FET analog switch current handling capability on settling time and the effects of offset characteristics on sample and hold system accuracy. Describes inverting and non-inverting sample and hold circuits.
Siliconix AN74-2 (4 pg.)

8 **"CMOS Analog Switches — A Powerful Design Tool"**
Describes CMOS switch construction, characteristics and operating precautions. Applications include: a four channel switch to multiplex a scope input, a low pass filter with digitally controlled frequency response, an amplifier with programmable inputs and gain, a sample and hold circuit, a latching switch, high frequency switching and multiplexer systems.
Siliconix AN75-1 (16 pg.)

9 **"Designing with Monolithic FET Switches"**
Describes MOSFET and JFET switch operation plus driver considerations.
Siliconix TA73-2 (4 pg.)

10 **"Analog Switches and Their Applications"**
(DG300 Series, DG506)
Introduces basic semiconductor theory and discusses in detail FET analog switches. Various circuit combinations including driver circuits, multiplexing, sample-and-hold circuits, N-path filters, and converters are also analyzed.
Siliconix $4.00 (324 pg.)

Switches (cont)

11 **"High Speed CMOS Analog Switches"**
(DG300 Series, DG181 Series)
Discusses the devices in low power, multiplexing, and thermocouple applications. (Includes AN76-6)
Siliconix (24 pg.)

12 **"Specifying and Testing Multiplexers"**
Describes how Teledyne Philbrick defines and measures analog multiplexer parameters with emphasis on CMOS types.
Teledyne Philbrick Applications Bulletin AN-31 (4 pg.)

Thermal Considerations

For Temperature Sensors see (Linear) Transducers

13 **"Thermal Evaluation of Integrated Circuits"**
Describes four methods for thermal evaluation, including reverse biasing substrate diodes.
Fairchild Application Note 205 (8 pg.)

14 **"Mounting Procedure for, and Thermal Aspects of, Thermopad Plastic Power Devices"**
Covers various methods of mounting and heat-sinking Motorola case number 77, 90, and 199 plastic power devices. Also discusses thermal resistance considerations, lead forming, and circuit board cleaning.
Motorola AN-290B (9 pg.)

15 **"Transient Thermal Resistance — General Data and Its Use"**
Discusses transient thermal resistance and its use and describes methods using various degrees of approximations to determine the junction temperature rise of a device. Also covers the concept of a duty cycle family of curves to simplify calculation of junction temperature rise under a repetitive pulse train.
Motorola AN-569 (15 pg.)

16 **"Mounting Techniques for Metal Packaged Power Semiconductors"**
Discusses preparation of mounting surfaces, using thermal compounds, and fastening techniques. Gives typical interface thermal resistance for a number of packages.
Motorola AN-599 (5 pg.)

17 **"Low Cost LED Thermometer"**
See listing under (Linear) Transducers. (National)

18 **"Micropower Thermometer"**
See listing under (Linear) Transducers. (National)

19 **"Thermal Resistance of Integrated Circuit Packages"**
Describes method of measuring package thermal resistance while package is immersed in a constant-temperature, circulating oil bath that acts as an infinite heat sink.
Sprague Electric TP 72-7 (5 pg.)

20 **"Thermal Design for Plastic Integrated Circuits"**
(ULN-2277)
Discussion of chip power dissipation—using amplifier as an example, heat dissipation, ULN-2277 dual 2-watt audio power heat sinks, heat sink finishes, and forced air cooling.
Sprague Electric TP 74-1 (7 pg.)

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Thermal Considerations (cont)

1 **"New Heat Sinking Techniques for Hermetic DIPs"**
Describes use of stamped and extruded heat sinks and method of reversing IC die and bonding chip directly to Kovar base.
Sprague Electric TP 74-4 (4 pg.)

Timers

2 **"Single-Chip Frequency Synthesizer Employing the XR2240"**
(XR2240)
Describes use of this timer/counter as a single-chip frequency synthesizer: $f_o = f, (m/n + 1)$ Where $f_o < 200$ kHz. Describes generating 100 Hz synchronized to 60 Hz line.
Exar AN-07 (3 pg.)

3 **"Precision Timer"**
(ZN1034E)
Explains the device and its use in various applications including a wiper control, a metronome, and a battery charger.
Ferranti Electric (19 pg.)

4 **"Digital Timer for Your Darkroom"**
(C685)
Describes a digital timer that counts down in either minutes and seconds or seconds only for darkroom use.
General Instrument Bulletin 0204 (12 pg.)

5 **"12-Hour Digital Electronic Automotive Clock"**
(CK3500)
Covers the use of the CK3500 I^2Lclock chip in a typical automobile application. Briefly introduces I^2L technology and provides circuit diagram.
General Instrument Bulletin 0302 (6 pg.)

6 **"AM/FM Frequency Display"**
(AY3-8112)
Describes a frequency and time display that can be an add-on accessory or built into a modified AM/FM set. Provides schematics and parts lists.
General Instrument Bulletin 0418 (8 pg.)

7 **"Wire Range Timer"**
(LM122, LM301A)
Describes a timer that, through the use of a single logarithmic control, can be adjusted from 2 ms to 2000 seconds.
National Semiconductor LB-38 (2 pg.)

8 **"Versatile Timer Operates from Microseconds to Hours"**
(LM122)
Describes the LM122 circuit and its operation. Includes discussion of pin functions, timing errors and noisy environments. Discusses use as various timers, as a pulse width detector, a comparator, an oscillator, a two-terminal time delay switch, and a frequency to voltage converter.
National AN-97 (12 pg.)

9 **"Using National Clock Integrated Circuits in Timer Applications"**
(MM5309, MM5311, MM5312, MM5315)
Describes demultiplexing techniques to generate time intervals and low frequency square waves. Gives as an example a fail-safe lighting timer.
National AN-143 (4 pg.)

Timers (cont)

10 **"1.3 Volt IC Flasher, Oscillator Trigger, or Alarm"**
(LM3903)
Describes circuit operation. Covers various flasher, tone generator and trigger circuits, especially for low voltage applications in anything from toys to laboratory equipment.
National AN-154 (10 pg.)

11 **"MM5865 Universal Timer Applications"**
(MM5865)
Provides block diagram and system description, discusses general timing and programming capabilities, suggests timing and counting applications.
National AN-168 (10 pg.)

12 **"A 4-Digit, 7-Function Stop Watch/Timer"**
(MM5865)
Gives detailed instructions for the circuit and construction of a 4-digit, 7-function timer with a display resolution of 0.01, 0.1, and 1 second, using the MM5865.
National AN-169 (14 pg.)

13 **"Problem Solving with the Dual Set Point Timer"**
(DF215)
Describes the device and its use as various timers and controls.
Siliconix AN76-2 (10 pg.)

Transducers

14 **"The LX1602A Pressure Transducer and Altimeter Applications"**
(LX1602A)
Describes how to use this transducer along with additional electronics to build an altimeter that operates over a range of −1,000 feet to +50,000 feet.
National AN-91 (3 pg.)

15 **"Installation Ideas for Pressure Transducers"**
(LX1600, LX1700, LX1400, LX1701)
Provides suggestions for mounting National transducers for various applications. Includes diagrams and typical mounting configurations.
National AN-92 (4 pg.)

16 **"Transducers in Fluid Flow Applications"**
(LX1602A)
Discusses application of LX1602A in pressure vessel, open flow and closed flow applications.
National AN-93 (8 pg.)

17 **"LX Series Pressure Transducers: Design and Applications Information"**
(LX1600A, LX1601A, LX1602A)
Describes hybrid transducer circuit and applications, including pressure to frequency converter, latching altitude detector, digital readout barometer and altimeter.
National AN-94 (8 pg.)

18 **"Pressure Transducer Load Cell"**
(LX1700G)
Describes use of LX1700G pressure transducer to measure weight.
National AN-95 (4 pg.)

LINEAR

Transducers (cont)

1 **"Pressure Transducers as Accelerometers"**
(LX1700G)
Discusses uses of accelerometers and describes scheme of converting LX series pressure transducers to cover ranges from fractions to thousands of g's.
National AN-96 (4 pg.)

2 **"A New Interfacing Concept: The Monolithic Temperature Transducer"**
(LX5600, LX5700)
Covers alternate methods of powering the LX5600, load isolation and an unusual active thermal shield (the shield tracks the surface temperature of the sensor.) Describes use as a thermal transducer, temperature to frequency converter, and a temperature controller with rate-of-change sensing. Discusses use of differential temperature measurements for liquid or moving air detection (including) wind) and for position sensing (using a heat source as a position reference.
National AN-132 (10 pg.)

3 **"Micropower Thermometer"**
(LX5600)
Describes use of the LK5600 as a thermometer whose output is a current proportional to temperature and can drive a meter for direct readout.
National Linear Applications Handbook, Vol. II, LB-27 (2 pg.)

4 **"Low Cost LED Thermometer"**
(LX5700)
Presents circuit for a −40° to 100°C thermometer with a conversion circuit for −40° to 199°F.
National Linear Applications Handbook, Vol. II, LB-30 (2 pg.)

5 **"Crystal Oven Controller and Precision Voltage Reference"**
(LM199, LM299, LM399, LM199A, LM299A, LM399A)
Shows the use of the LM199 both as an oven temperature controller and a voltage reference at the same time.
National Linear Applications Handbook, Vol. II, LB-31 (2 pg.)

6 **"Simple Temperature Control"**
(LX5600)
Discusses setting up a temperature control system using the LX5600.
National LB-36 (2 pg.)

7 **"The Multi-Level Switch Kit, Part No. SK1007"**
Details the use of any LX series pressure transducer to produce a high level analog output as well as three independent switch points.
National TB-1 (2 pgs.)

8 **"Transducer Sensor Diaphram 15 Million Cycle Life Test"**
Findings in the continuing test of National's transducer sensing elements — a silicon membrane approx. 1 mil. thick.
National TB-3 (1 pg.)

9 **"Use of the SK1007 Pressure Transducer Kit in Vault Alarm Systems"**
Describes application of this multi-level switch kit with a pressure transducer in vault alarm systems.
National TB-7 (2 pg.)

10 **"Transducer Fluid Filled Option"**
Describes the "Fluid-Filled" methods of protecting transducers from hostile environments. Rates the resistance of silicone rubber to some common fluids.
National TB-8 (2 pg.)

Transducers (cont)

11 **"Application Circuits of Temperature Sensor and Temperature Controller IC's"**
(μPC616, μPC3911)
Provides device characteristics and four basic applications with diagrams.
NEC America (6 pg.)

12 **"REF-02 Temperature Controller"**
(CMP-02, REF-02)
Describes temperature control using the REF-02 and the CMP-02 comparator.
Precision Monolithics AB-4 (1 pg.)

13 **"Thermometer Application of the REF-02"**
(REF-02)
Discusses thermometer essentials, bandgap voltage reference theory, and basic circuit design using device.
Precision Monolithics AN-18 (4 pg.)

Voltage References

14 **"1.2 Volt Reference"**
(LM113, LM313)
Describes the LM113 temperature compensated shunt regulator diode. Applications: low voltage regulator circuits, bias current source for a differential amplifier, and an electronic thermometer circuit.
National Linear Applications Handbook, Vol. I, N-56 (4 pg.)

15 **"IC Voltage Reference has 1 PPM per Degree Drift"**
(LM199, LM299, LM399, LM199A, LM299A, LM399A)
Describes this device with a sub surface Zener and an on-chip temperature stabilizer. Several applications are also covered.
National Linear Applications Handbook, Vol. II, AN-161 (6 pg.)

16 **"IC Zener Eases Reference Design"**
(LM129, LM329)
Describes LM129 circuit and operation. Covers use in voltage reference and regulator applications.
National AN-173 (3 pg.)

17 **"References for A/D Converters"**
(LM199, LM399, LM199A, LM399A)
Discusses requirements of references for various accuracies of A/D converters. Gives reference circuit designs.
National AN-184 (4 pg.)

18 **"A Micropower Voltage Reference"**
Describes a voltage reference made by operating a JFET slightly below pinch-off along with an op amp to convert current to voltage.
National Linear Applications Handbook, Vol. II, LB-34 (2 pg.)

19 **"Crystal Oven Controller and Precision Voltage Reference"**
See listing under (Linear) Transducers (National)

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MEMORY

Analog

1 **"Delaying AF Signals with MOS Delay-Lines TCA350"**
(TCA350)
Discusses bucket brigade circuits and practical applications employing this device.
ITT Semiconductors (7 pg.)

2 **"MOS Delay Lines"**
(DM8000, DM8510, DM8830, MM506)
Covers use of MOS shift registers to build delay lines.
National MB-4 (2 pg.)

3 **"Acoustic Applications of Serial Analog Delay Devices"**
(SAD1024)
Covers use in reverberation, vibrato, chorus, wow and flutter control plus considerations in using this device.
Reticon Application Note 104 (8 pg.)

4 **"Bucket Brigade Devices Circa 1976"**
Gives history of development, construction features, and advantages of bucket brigade devices.
Reticon Technical No. 107 (11 pg.)

5 **"A Tapped Analog Delay for Sampled Data Signal Processing"**
Introduces tapped analog delays and gives various applications heretofore accomplished by digital techniques.
Reticon Application Note No. 105 (11 pg.)

6 **"Serial Operation of Clocked Analog Delay Lines to Obtain Long Delay"**
(SAD1024A)
Describes advantages, coupling, and performance of device.
Reticon Application Note No. 109 (8 pg.)

7 **"Implementation of Discrete-Time Analog Filter and Processing Systems"**
(TAD32A)
Discusses tapped analog delay device operation and areas of application, including transversal and recursive filters.
Reticon Application Note No. 111 (10 pg.)

8 **"Charge Transfer Devices for Sampled-Data Processing"**
Discusses the application of charge transfer devices to analog and digital signal processing. Compares CTD devices. Describes Tapped Analog Delay, the Binary Analog Correlator, the Analog Correlator and the Transversal Filter.
Reticon Application Notes No. 114 (11 pg.)

Character Generators

9 **"A CRT Display System Using NMOS Memories"**
(MC6545, MCM6570, MCM6571)
Discusses basic CRT operation, character formation and describes the 8K-bit MCM6570 character generators. Describes a 128-character system in detail, including counter and retrace control, memory select, and address register sections.
Motorola AN-706A (15 pg.)

10 **"American and European Fonts in Standard Character Generators"**
(MM4240, MM5240, MM4241, MM5241)
Depicts the standard 64 character subsets for these devices.
National AN-57 (6 pg.)

Character Generators (cont)

11 **"DM8678 Bipolar Character Generator"**
(DM8678)
Explains the operation of the device and the various features which include circuit address latches, the line counter, the 7-bit shift register, and the output buffer.
National AN-167 (4 pg.)

12 **"The Systems Approach to Character Generators"**
See listing under (Memory) ROMs. (National)

13 **"Digital Display Systems"**
Using TTL compatible MOS ROMs to generate displays. Gives circuit diagrams and a sample readout.
National MB-8 (2 pg.)

14 **"7 x 9 Display Character Generator"**
Uses three MOS ROMs and some TTL logic to create a font of 64 7 × 9 dot-type characters. A circut diagram and suggested character forms are provided.
National MB-13 (2 pg.)

15 **"1024 Step Programmable Calculator with Non-Volatile EAROM Memory"**
(ER3401)
Describes a programming circuit that can store up to 1024 program steps, each being a digit or function key entry, and interfaces to a calculator chip. Supplies diagrams and example program.
General Instrument Bulletin 0203 (4 pg.)

16 **"EAROM Technology"**
Describes Electrically Alterable Read Only Memories built with MNOS transistors. Discusses reliability and provides diagrams of application in a phase-locked loop tuner, a lock, and a telephone repertory dialer.
General Instrument Bulletin 1201 (8 pg.)

17 **"The Role of Non-Volatile Memories in Consumer Electronics"**
Briefly describes MNOS technology, updating EAROMs, and use of EAROMs to store data, to keep track of system status, and store programs for microcontrollers.
General Instrument Bulletin 1202 (3 pg.)

18 **"Electronic Digital Lock"**
(ER2050)
Schematic and description of an 8-digit electronic lock that has 4 different "open" codes and a programming mode that allows any of the codes to be changed.
General Instrument Bulletin 1206 (3 pg.)

19 **"Using the ER3401"**
(ER3401)
Presents basic device operation and supplies diagrams for a bench-top evaluator/programmer and a dc inverter.
General Instrument Bulletin 1203 (5 pg.)

20 **"An ER2051 Programmer"**
Presents a programmer that automatically erturns an EAROM to standby condition following read, erase, or write commands, and provides stable timing controls for all modes of operation.
General Instrument Bulletin 1204A (3 pg.)

21 **"A Voltage Switching Circuit for the ER2401/ER2800"**
(ER2401, ER2800)
Furnishes a diagram of a voltage switching circuit for the devices and the control signal truth table describing its operation.
General Instrument Bulletin 1205 (2 pg.)

Character Generators (cont)

1 **"Eight and Sixteen-Bit EAROM Module For Minis & Micros"**
(ER3400)
Describes the design of an 8K byte EAROM module with a 1.2 μsec access time. The memory module can be read and written like conventional memory, and it can be reconfigured to sixteen-bit words with the change of a single logic level. Also details an EAROM sequencer.
General Instruments Bulletin 1208

Interface

2 **"The Recovery of Recorded Digital Information in Drum, Disk and Tape Systems"**
Reviews methods for converting the analog signal obtained from a magnetic recording into digital format.
Motorola AN-711 (10 pg.)

3 **"Applying Modern Clock Drivers to MOS Memories"**
(DS0025, DS0026)
Covers use of 0025/26 drivers in MOS memory systems. Information includes selection of packages and heat sinks, power dissipation, rise and fall time, power supply decoupling, system clock line ringing and crosstalk, input coupling techniques, and sample calculations.
National AN-76 (12 pg.)

4 **"Interfacing Circuits for MOS Dynamic Random Access Memories"**
Discusses interfacing methods employing level shifters (TTL to MOS levels) with boosters, level shifters (MOS to TTL levels), and sense amplifiers.
Nortec Applications Note No. 25 Rev. A (3 pg.)

5 **"Charge Pump Driver for 7001 RAMs"**
(SN54508)
Defines a method for driving the charge storage pump input of a 7001 RAM. Provides a description of the basic storage pump RAM cell and the charge pump circuit diagram. Gives performance curves.
Texas Instruments Application Report CA-178 (6 pg.)

6 **"High Speed TTL Interfacing for 7001 Static RAMs"**
(SN75261, SN75365)
Illustrates interface techniques for driving the 7001 RAM chip-select input, and sensing the memory output.
Texas Instruments Application Report CA-179 (8 pg.)

Microprogramming

7 **"Tri-State Logic in High Speed Memories of Microprogrammed Computers"**
See listing under (Digital) TTL, General. (National)

8 **"How to Design with the 8X02 Control Store Sequencer"**
See listing under (Microprocessor) Systems (Signetics)

9 **"Signetics Micro Assembler Reference Manual"**
See listing under (Microprocessor) Programming (Signetics)

PROMs

10 **"Programming AMI S6834 and S5204A EPROMs"**
(S5204A, S6834)
Compares on-board versus dedicated-socket programming and suggestions on programming system design.
American Microsystems (3 pg.)

11 **"EA2708 EPROM Application Note"**
(EA2708)
Comments on read characteristics of the device and its use in microprocessor systems.
Electronic Arrays (8 pg.)

12 **"Programmable Read Only Memories"**
(93417, 93427, 93436, 93438, 93448, 93452, 93453)
Gives general background on PROMs, describes programming procedures, discusses power switching, address expansion, 8-bit binary to decimal decoding and programmed logic controller.
Fairchild Application Note 333 (16 pg.)

13 **"The MB8518 EPROM"**
(MB8518)
Characterizes device and discusses programming and erasing it. Provides a schematic for incorporating a switching power supply to save power.
Fujitsu AN201 (14 pg.)

14 **"Application of the Intel 2708 8K Erasable PROM"**
(2708)
Covers characteristics, operation, programming and erasure, reduced power and interface.
Intel Application Note AP-17 (15 pg.)

15 **"Power Switching"**
Describes a method for power switching Intersil's PROMs and FPLAs, and specifies the design tradeoffs and performance to be expected.
Intersil Application Bulletin MB003 (4 pg.)

16 **"Intel Memory Design Handbook"**
See listing under (Memory) RAMs (Intel)

17 **"Programming the MCM5003/5004 Programmable Read Only Memory"**
(MCM5003, MCM5004)
Discusses programming methods for this 64 × 8 bit memory, describes circuit and operation. Describes a simple programmer using five ICs and a more sophisticated version using 25 ICs offering automatic sequencing.
Motorola AN-550 (12 pg.)

18 **"PROM Power-Down Circuits"**
(DM74S287)
Describes several ways to power-down bipolar, three-state PROMs.
National AN-171 (4 pg.)

19 **"A PROM Programmer for the SC/MP LCDs"**
(SC/MP, MM4204, MM5204)
Provides a method for the user of the SC/MP LCDs to program MM4204 PROMs. Using wire-wrap techniques the user can construct a programmer that plugs into the SC/MP LCDs backplane and programs a 512 x 8 PROM in 10 seconds.
National AN-189 (23 pg.)

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MEMORY

RAMs

1 **"Application of First-In First-Out Memories"**
(AM2812, AM2813, AM2814, 3341)
Describes the function of a first-in, first-out memory, methods of constructing FIFO buffers and the operation of the above P-channel MOS devices. Discusses storage and control, expansion methods, interfacing, and applications in an N-bit shift register and as a key encoder on key matrix.
Advanced Micro Devices Application Note (9 pg.)

2 **"The AM9338 Multiple Port Memory"**
(9338)
Describes applications for this 8-word by 1-bit three-address memory, including the working store for high-speed, three address computers; first in, first out (asynchronous buffer) memory; and direct address/indirect address memory.
Advanced Micro Devices Application Note 4 (pg.)

3 **"Application of the EMM/SEMI 4200 Static RAM to the Intel 8080A Microprocessor"**
(4200)
Describes suggested logic interface to connect this 4K × 1 static RAM to 8080A MPU.
EMM/Semi Application Note S103A (4 pg.)

4 **"Application of EMM/SEMI 4K Static RAM to Motorola M6800 Microprocessor"**
(4200)
Describes suggested logic interface to connect this 4K × 1 static RAM to the M6800 MPU.
EMM/Semi Application Note S104 (6 pg.)

5 **"Checking Out the EMM/Semi 4200 in 2107B or 4060 Sockets"**
(4200)
Suggests circuit changes to permit acceptance of the 4200 static RAM in sockets wired for 2107B or 4060 Sockets.
EMM/Semi Application Note S102 (2 pg.)

6 **"TTL/MSI 9334 8-Bit Addressable Latch"**
(9334)
Describes operation and applications, including 16 and 32-bit addressable latches, 16-word by 4-bit memory, demultiplexer and decoder, 8-bit A/D converter and a 16-bit serial-to parallel converter.
Fairchild Application Note 220 (8 pg.)

7 **"Understanding the FIFO"**
(3351)
Covers 3351 FIFO operation, cascading, plus use in data rate buffering, parallel operation, and burst operation.
Fairchild APP 332 (8 pg.)

8 **"The MB8116 16K RAM"**
(MB8116)
Characterizes device and device operation. Discusses testing and use of the device in a 64K x 8-bit array.
Fujitsu AN202 (14 pg.)

9 **"The MB8227 4K RAM"**
(MB8227)
Characterizes device and illustrates use in a memory array.
Fujitsu AN200 (14 pg.)

RAMs (cont)

10 **"Designing Non-Volatile Memory Systems with Intel's 5101 RAM"**
(5101)
Describes internal circuits and operation of the RAM. Outlines circuit techniques for battery supported non-volatile operation. Describes use of the device with the MCS-40 microcomputer.
Intel Application Note AP-12 (28 pg.)

11 **"Which Way for 16k?"**
Considers various aspects of 16k RAMs including 64 and 128 cycle refresh and the advantages versus disadvantages of latching.
Intel Application Note AP-22 (7 pg.)

12 **"Applications of the Intel 2104A 4k RAM"**
(2104A)
Discusses operation of the device including power distribution and decoupling.
Intel Application Note AP-23 (13 pg.)

13 **"MOS Static RAMs"**
(2101, 2102, 2111, 2112, 5101)
Presents devices, failure mechanisms, testing methods and results.
Intel RR-9 (7 pg.)

14 **"2416 16K CCD Memory"**
(2416)
Describes device, failure modes, reliability tests and results.
Intel RR-11 (5 pg.)

15 **"Intel Memory Design Handbook"**
(1103, 2107A, 2107B, 2416, 3207A, 3222, 3245, 5101, 5235, 5244)
Combines various RAM, ROM, PROM and CCD application notes plus information on support circuits.
Intel $5.00 (265 pg.)

16 **"Operational Characteristics of the AMS 6002"**
(IM6002)
Describes the circuits required to interface the 6002 1K MOS RAM with TTL. Also discusses the internal and external circuit parameters that affect system performance.
Intersil AN-28 (4 pg.)

17 **"Designing Memory Systems with the AMS 6003 RAM"**
Provides the circuitry and timing information for building memory systems from the 6003 dynamic RAM.
Intersil AN-32 (9 pg.)

18 **"AMS7001 Basic Storage Module High Speed Memories"**
(IM7001)
Discusses AMS7001 storage module operation, backplane wiring, addressing scheme, and power requirements.
Intersil AN-35 (18 pg.)

19 **"Using the TM-200 Semiconductor Memory Card"**
(IM7001)
Describes this memory card using the AMS7001 RAM. Includes detailed diagrams.
Intersil AN-36 (22 pg.)

20 **"Layout Considerations Using 4K MOS RAMs"**
Discusses orientation, packing, drivers, power distribution, trace widths, signal levels, bypass caps, and bus bars.
Intersil AN-37 (4 pg.)

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MEMORY

RAMs (cont)

1 **"7005-4K RAM Application Information"**
(IM7005)
Provides a functional description of the 7005, and gives a typical design of a 16K x 16 system with timing information and suggested circuits.
Intersil AN-38 (7 pg.)

2 **"Battery Backup for Semiconductor Memory Systems"**
Provides information on the selection and application of batteries for backup power to both single-voltage and multiple-supply RAM systems.
Intersil AN-39 (6 pg.)

3 **"Memory System Reliability with Intersil 4K RAMs"**
(IM 7005, IM 7270, IM 7280)
Shows how memory system reliability can be predicted from device failure data and how, when necessary, system reliability can be increased through the use of error correction techniques.
Intersil AN-40 (7 pg.)

4 **"CMOS RAMs"**
(IM6508, IM6523, IM6524)
Provides a block diagram and describes the operation and interface requirements for these 256 × 1 and 1024 × 1 CMOS RAMs.
Intersil Application Bulletin M002 (8 pg.)

5 **"Considerations for Designing a High Density, Low Power Memory System"**
(MK4200)
Describes a 16K × 8 memory array using the MK4200 4K RAM and CMOS logic.
Mostek (3 pg.)

6 **"An In-Depth Look at Mostek's High Performance MK4027"**
(MK4027)
Describes operation of this 16-pin, 4K RAM.
Mostek (15 pg.)

7 **"Why 'Edge-Activated' Static Memories?"**
(MK4104, MK32000, MK36000)
Describes these devices with static memory cells and dynamic peripheral circuitry. Compares performance to fully static devices.
Mostek (4 pg.)

8 **"A MECL 10,000 Main Frame Memory System Employing Dynamic MOS RAMs"**
(MC10000 series)
Describes a dynamic RAM system that uses the MECL family for the control logic. Considers memory organization, layout rules, interfacing and generation of control signals.
Motorola AN-583 (20 pg.)

9 **"A Non-Volatile Microprocessor Memory Using 4K N-Channel MOS RAMs"**
(MCM6605, MC6800)
Describes the design of a 8192-byte non-volatile memory using the MCM6605 4K × 1 RAM and CMOS control logic to reduce the power requirement in the standby mode.
Motorola AN-732A (17 pg.)

10 **"The Design of an N-Channel 16K x 16-Bit Memory System for the PDP-11"**
(MCM6605, MC3450, MC3452, MC3459, MC3460)
Briefly describes operation of the MCM6605 NMOS RAM, the details, the design of a PDP-11 add-on mainframe memory using this device. The interface ICs and system performance are also discussed.
Motorola AN-740 (15 pg.)

RAMs (cont)

11 **"A CMOS Keyboard Data Entry System for Bus Oriented Memory Systems"**
(MC14419)
Describes a keypad to binary data entry system for placing data in RAM memories. It allows data to be entered through keystrokes, encoding 4-bits at a time.
Motorola Application Note AN-759 (4 pg.)

12 **"Semiconductor for Plated Wire Memories"**
See listing under (Digital) Interface. (Motorola)

13 **"A High Speed FIFO Memory Using the MECL MC10143 Register File"**
See listing under (Digital) High Speed Logic (Motorola)

14 **"A Method of Implementing Stacks with Existing Minicomputer Memory"**
Gives detailed description of a controller for a stack of programmable size up to 256 words for a 16-bit minicomputer with less than 16K of memory. Tells how stack size can be increased to 4096 words by adding ten ICs.
National AN-60 (4 pg.)

15 **"Using Tri State™ Logic for Rubber Band Memories"**
Describes the construction and use of scratch/pad memories to store data at a rapid rate and then release it as required. They serve as buffers between systems operating at different clock rates.
National AN-68 (4 pg.)

16 **"A Simple Power Saving Technique for the MM5262 2k RAM"**
(MM5265)
Describes method for decoding the clocks of unselected chips in a memory array to save power. Discusses application in 8K x 16 memory.
National AN-86 (4 pg.)

17 **"Designing Memory Systems Using the MM5262"**
(MM4262, MM5262)
Provides a detailed description of this 2048 × 1 PMOS dynamic RAM, operating instructions, and a diagram of a 16K × 10 memory using the device.
National AN-144 (14 pg.)

18 **"Pulsed Power Supply Operation of Selected MM2102 Static RAM"**
(MM2102, SM1480)
Covers method for operating selected 2102s (SM61480s) in a power-down mode.
National AN-172 (3 pg.)

19 **"MOS Scratch Pad/Content Addressable Memory System"**
Describes a 64-bit Scratch Pad/Content Addressable Memory using MOS devices. Includes circuit diagrams and discusses circuit operations.
National MB-11 (2 pg.)

20 **"Memory Systems Built with the Nortec 6002"**
(6002)
Describes circuits for the bit driver/sense amplifier required to interface the 6002 with TTL. Discusses external support circuit parameters and internal circuit operations that affect system performance.
Nortec Applications Note No. 28 (4 pg.)

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MEMORY

RAMs (cont)

1 **"Memory Systems Built with the Nortec 6002"**
(6002)
Describes use of this 1024-bit RAM in building a general purpose memory module with 425,984 bit capacity.
Nortec Applications Note No. 30 (14 pg.)

2 **"Printed Circuit Layout Considerations for Dynamic Memory Arrays"**
Gives P.C. layout guidelines for MOS dynamic memories (also applicable to standard TTL circuits.)
Nortec Applications Note No. 31 (2 pg.)

3 **"Designing Memory Systems with the Nortec 6003 RAM"**
(6003)
Describes operation of this 2048-bit RAM, including a discussion of memory timing, refresh control, array control signals, device output sensing, and array driver circuits.
Nortec Applications Note No. 32 (9 pg.)

4 **"Memory Systems Characteristics and Applications for the CD4061A"**
(CD4061A)
Describes basic device operation, application in memory systems, and testing including construction of an all CMOS memory tester.
RCA ICAN-6445

5 **"Driving the TMS4030 RAM Using the SN75363 or SN75322"**
(SN75322, SN7536, TMS4030)
Driving the TMS4030 chip enable clock with these ICs, switching speeds versus system size, general performance characteristics and performance comparisons are provided.
Texas Instruments Application Report CA-181 (7 pg.)

6 **"Memory System Design Utilizing TMS4050/4051 4k Dynamic RAMs"**
(TMS4050, TMS4051)
Reviews speed considerations, then steps through drafting a 4k dynamic RAM system. Two sample circuit examples are outlined.
Texas Instruments Application Report MOSA1 (56 pg.)

7 **"Introduction to Refreshing TI 4k Dynamic RAMs"**
(TMS2102, TMS4051)
Methods of refreshing dynamic RAMs are discussed. Compares static RAMs with dynamic RAMs also.
Texas Instruments Application Report MOSA3 (12 pg.)

8 **"Memory System Design Utilizing the TMS4044/4046, TMS4045/4047 4K Static RAMs"**
(TMS4044, TMS4045, TMS4046, TMS4047)
Provides general discussion of static RAMs and characteristics of devices. Two sample circuit examples are outlined.
Texas Instruments Bulletin S127R (44 pg.)

ROMs

9 **"Using the EA4600 ROM in M6800 Microcomputer Systems"**
(EA4600)
Takes up use of the ROM for use as memory, an I/O device, or as a data converter in the microcomputer system.
Electronic Arrays M-16 (14 pg.)

ROMs (cont)

10 **"ROM Application Note"**
(EA2708, EA3200, EA4700, EA8308A, EA8316E)
General discussion of ROMs and characteristics of each device.
Electronic Arrays (11 pg.)

11 **"Interfacing of the EA4900 16K ROM in an MCS-4 Microprocessor System"**
(EA4900)
Considers timing, power supplies, and logic levels for interfacing these devices.
Electronic Arrays (8 pg.)

12 **"Monolithic Diode Matrices"**
Describes programming and use of diode matrices. Applications: teletypewriter coding matrix, decimal decode for displays, nines complement-BCD, shift register matrices, and ROMs.
Harris Application Note 206 (16 pg.)

13 **"Intel Memory Design Handbook"**
See listing under (Memory) RAMs (Intel)

14 **"MCS2026-002"**
(MCS2026-002)
Describes connections to use this demonstrator version of the 16K (2048 × 8) dynamic ROM, which can be used as an adder, counter, encoder, decoder or shift register.
MOS Technology Application Note MCS2026-002 (8 pg.)

15 **"Code Conversion with Semiconductor Read Only Memories"**
(MCM4000)
Describes methods for converting data from binary to BCD and vice versa, from the Hollerith to the common 8-bit codes, and from one 8-bit code to another.
Motorola AN-506 (13 pg.)

16 **"Replacing Sequential Logic with ROMs"**
Describes design methods for using ROMs to replace sequential logic, that is to replace designs that would require random or combinational logic with feedback loops.
Motorola AN-722 (19 pg.)

17 **"The Systems Approach to Character Generators"**
(MM5240, MM5241)
Discusses use of MM5240 and MM5241 ROMs in character generation. Includes discussion of CRT raster scan displays, refresh memory modulation, control logic, bipolar compatibility, printing applications, and raster scan systems.
National AN-40 (12 pg.)

18 **"The Application of ROMs"**
(MM5203, MM5230, MM5232, MM5240)
Describes applications of read only memories in table look up, code conversion and generation, character generation, random logic generation, and microprogamming.
National AN-61 (12 pg.)

19 **"Saving ROMs in High-Resolution Dot-Matrix Displays and Printers"**
(MM5232, MM5240, MM5241, DM8596, MM8597)
Describes two-stage, column-generation approach called "intermediate coding" that saves more than 25% of ROM capacity when several ROMs are needed to store a font.
National AN-85 (8 pg.)

20 **"Custom ROM Programming"**
Gives forms for submitting truth tables for various National read only memories.
National AN-100 (8 pg.)

ROMs (cont)

1 **"Trig Function Generators"**
Instead of simply cascading ROM to increase resolution and accuracy of the look-up tables, this note describes interpolation techniques to increase trig function accuracy with less memory.
National MB-10 (2 pg.)

2 **"MOS Goes Bipolar"**
See listing under (Memory) Shift Registers. (National)

3 **"Fast Multipliers Using TTL Read Only Memories"**
(SN74182, SN74H183, SN74283, SN74284, SN74285)
Reviews fundamental algorithm of binary multiplication. Shows use of ROMs for multiplication, two's complement multiplication, and truncated multiplications.
Texas Instruments Application Report CA-172 (11 pg.)

Shift Registers

4 **"A Random Pattern Generator for Testing Digital Delay Elements"**
Describes the use of a linear feedback shift register for digital testing.
Advanced Micro Devices Application Note (3 pg.)

5 **"Applications of Dynamic Shift Registers"**
(1402A, 1403A, 1404A, 1405A, AM2802, AM2803, AM2804, AM2805, AM2806, AM2807, AM2808)
Discusses dynamic shift register storage in general, clock timing, circuits for clock drivers, interfacing with TTL, and recirculating registers.
Advanced Micro Devices Application Note (7 pg.)

6 **"Schottky TTL MSI Registers"**
(AM25S07, AM25S08, AM25S09, SN54S174, SN54S175, SN54S194, SN54S195, SN74S174, SN74S175, SN74S194, SN74S195)
Describes these 4 and 6-bit registers, their operation and applications. Contains logic diagrams and function tables. Applications covered include: longer words, use with dynamic shift registers, selective bus storage, use as a LIFO memory, psuedo random feedback, unique counting codes, permutation of inputs, and use in arithmetic.
Advanced Micro Devices Application Note (16 pg.)

7 **"High-Speed Shift Registers Use TTL RAMs and Counters to do all the Shifting"**
Describes how to build a high speed shift register using a RAM accessed by counters.
Advanced Micro Devices (2 pg.)

8 **"9338 8-Bit Multiple Port Register"**
(9338)
Describes the features of this device, the TTL/MSI equivalent and parallel serial expansion capabilities. Covers use as three address arithmetic unit with eight registers, and use in a first-in first-out memory.
Fairchild Application Note 294 (6 pg.)

9 **"The Logic Design of Shift Counters"**
See listing under (Digital) Counters. (Motorola)

10 **"Using Shift Registers as Pulse Delay Networks"**
See listing under (Digital) High Speed Logic (Motorola)
Microprocessors

Shift Registers (cont)

11 **"MOS Delay Lines"**
(MM506)
Describes the characteristics of static and dynamic shift registers used in delay lines. Discusses application as series/parallel delay lines and as substitutes for magnetic drum memories. Also covers specialized clocking techniques, such as two-speed clocking.
National AN-25 (8 pg.)

12 **"High Voltage Shift Registers Move Displays"**
(MM5081)
Describes use of the MM5081 high voltage shift register for driving gas discharge or lamp displays, i.e. moving messages or moving graphics.
National AN-44 (14 pg.)

13 **"Low Frequency Operation with Dynamic Shift Registers"**
Discusses operation of two forms of dynamic shift registers: ratioless and ratio. Recommends techniques, such as keeping clock amplitudes high, to design added margin into systems. Discusses temperature considerations, packaging.
National AN-55 (4 pg.)

14 **"Design Considerations of MOS Dynamic Shift Registers with Tri-State Outputs"**
(MM4012, MM4013, MM5012, MM5013)
Describes operation of MOS shift registers with Tri-State push-pull outputs. Includes discussion of the dynamic characteristics and maximum clock frequency.
National AN-65 (4 pg.)

15 **"MOS Goes Bipolar"**
Shows what voltages are required to combine MOS Shift Registers and Read Only Memories with bipolar devices. Presents interface diagrams.
National MB-12 (2 pg.)

16 **"Mask Programming Specializes MOS Shift Register Designs"**
(MM4007, MM4019, MM5007, MM5019)
Describes customizing MOS shift register bit lengths by programming a metalization mask used to manufacture these devices. Dual registers from 20 to 256 bits, and single registers from 40 to 512 bits are available. Describes single register taped output options.
National MB-14 (2 pg.)

17 **"COS/MOS MSI Counter and Register Design and Applications"**
See listing under (Digital) CMOS (RCA)

18 **"Static Shift Register Operating Curves"**
How to use the minimum/maximum clock pulse width operating curves included in National's static shift register data sheets.
National MB-15 (2 pg.)

19 **"Double-Clocking Cuts Standard Registers to Non-Standard Sizes"**
Describes a method of double-clocking for N data input periods to make the register appear shortened by N bits. When this is achieved, the clock rate resumes normal frequency.
National MB-16 (2 pg.)

20 **"HiNIL 375 Universal Shift Register"**
See listing under (Digital) HNIL/HTL (Teledyne Semiconductor)

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MICROPROCESSORS

Applications

1 **"A Musical S2000"**
(S2000)
Provides general description of the device programmed to generate musical frequencies and remember a set of twelve tunes. Includes schematic.
American Microsystems (4 pg.)

2 **"Application Techniques for the MCS-48 Family"**
(8748, 8048, 8355, 8243, 8755, 8155)
Introduces the MCS-48 family and describes the implementation of such subsystems as: analog input and output, the use of tables for function evaluation, receiving and transmitting serial code, and parity generation.
Intel Application Note AP-24 $1.00 (23 pg.)

3 **"CRT Terminal Design Using the 8275 and 8279"**
(8275, 8279, 8224, 8080, 8257, 8228, 8212, 8251, 2708, 2714, 2716)
Provides component descriptions and system design details needed to apply the 8275 programmable CRT controller and 8279 programmable keyboard/display interface in CRT systems. Flowcharts, sample code, and schematics included.
Intel AP-32 (57 pg.)

4 **"IM6100 CMOS Microprocessor Remote Data Station"**
(IM6100)
Describes a system capable of monitoring a number of different dc measurement channels under control of the IM6100.
Intersil DCE8001 (15 pg.)

5 **"Using Mostek F8 Microprocessor in a Scanned Seven-Segment Display Application"**
(F8)
Discusses the advantages of the F8 as a numeric display interface in μP based devices.
Mostek (16 pg.)

6 **"Using Mostek F8 in a Scanned Keyboard Application"**
(F8)
Discusses application of the F8 to eliminate hardware outside the processor to encode the keyboard. Uses a keyboard scanning technique.
Mostek (16 pg.)

7 **"A Floppy Disk Controller Using the MC6852 SSDA and Other M6800 Family Parts"**
(MC6852, M6820)
Discusses a floppy disk controller built using a synchronous serial data adapter as the primary data interface with the MPU. All non-data operation (seek, drive selection, etc.) in the controller are handled by a peripheral interface adapter.
Motorola AN-764 (17 pg.)

8 **"Data Acquisition Networks with NMOS and CMOS"**
(MC14433, MC6800)
Discusses an 8-channel data acquisition network using the MC14433 A/D converter and the MC6800 microprocessor.
Motorola AN-770 (11 pg.)

9 **"A Dual Processor System for Use in the EXORciser"**
Introduces dual processing and presents the design of a dual processor system for use in the EXORciser. In the system discussed, the μP's have control of a common bus on opposite phases of the clock.
Motorola AN-777 (13 pg.)

Applications (cont)

10 **"Interfacing and Controlling Digital Temperature Data Using the MC6800"**
(MC6800, MC6821)
Provides block diagrams, instruction set, and discussion of a temperature control system using the device.
Motorola AN-782 (4 pg.)

11 **"Simplify CRT Terminal Design with the DP8350"**
(DP8350, SC/MP)
Describes a low-cost CRT data terminal design based on the DP8350 CRT controller and SC/MP microprocessor. Features screen scroll, RS-232C interface, and adjustable band rate. Includes schematics, flowcharts, and PC board layout.
National Semiconductor AN-198 (10 pg.)

12 **"M6800 Microprocessor Application Manual"**
(MC6800)
Describes the use of the 6800 family of parts. Gives details of practical applications including the development of hardware and software, design of a point of sale terminal and interfaces to peripherals.
Motorola $25.00 (716 pg.)

13 **"Multiple Microprocessors in Instrument Systems"**
(IMP-8, IMP-16)
Discusses systems built with central microcomputers plus peripheral microprocessors to distribute intelligence. Illustrates concepts with a data acquisition and setpoint control system.
National AN-106 (8 pg.)

14 **"The IMP-8C as a Data Concentrator"**
(IMP-8C)
Describes the use of this microprocessor in data concentrator applications. Covers use with a full duplex modem, and the terminal controller interface.
National AN-113 (6 pg.)

15 **"Data Handling with the IMP-8"**
(IMP-8, IMP-16)
Covers basic concepts for transferring data from a memory to peripherals.
National AN-117 (4 pg.)

16 **"Microprocessor Mates with MOS/LSI Keyboard Encoder"**
(IMP-16)
Shows how to interface a keyboard to the IMP-16 microprocessor for text editing.
National AN-128 (6 pg.)

17 **"For Data Communications Systems: A Front-End Preprocessor for 16-Bit Minicomputer Hosts"**
General discussion of how preprocessing techniques used in large-scale host computers can be scaled down for application in mini-based systems.
National AN-131 (4 pg.)

18 **"The IMP-16 in Communication Applications**
(IMP-16)
Discusses communication processor functions, requirements for communications microprocessors and system considerations. Gives programming examples including status monitoring, data transmission, message routing, interrupt handling and error control.
National AN-134 (6 pg.)

MICROPROCESSORS

Applications (cont)

1 **"Communication Interfaces for the IMP-16"**
(IMP-16)
Describes the use of this microprocessor in leased line and switched line applications with the communications conforming to EIA standard RS232-C.
National AN-152 (13 pg.)

2 **"A Data Concentrator Using PACE"**
(PACE)
Describes the use of this microprocessor to take data from several slow speed lines and transmit it over one line.
National AN-164 (5 pg.)

3 **"Microprocessor Security Systems Made Easy"**
(SC/MP)
Describes program for sequencing through multiple inputs and actuating a simple output (relay, alarm, etc.) using NIBL.
National AN-174 (2 pg.)

4 **"SC/MP as an Analog-to-Digital Converter"**
(SC/MP)
Equations and diagrams for using the SC/MP as an A/D and D/A converter. Also lists sources of error that may result.
National AN-191 (3 pg.)

5 **"A Low Component Count Video Data Terminal Using the DP8350 CRT Controller and the INS8080 CPU"**
(DP8350, INS8080A, INS8250)
Describes a video data terminal system. Provides block diagrams and short descriptions of individual circuit elements as well as system schematic.
National AN-199 (10 pg.)

6 **"SC/MP Microprocessor Applications Handbook"**
(SC/MP)
Describes the SC/MP as a general purpose microprocessor covering applications, addressing, instruction set, implementing systems, buffering and interface. Covers use with A/D converters, keyboards, display systems, recorders and printers.
National $5.00 (160 pg.)

7 **"The CRT5027: Video Timer-Controller"**
(CRT5027)
Characterizes the device and explains how to program it. Provides examples for systems with 80 characters by 24 rows and 40 characters by 12 rows. Schematics and system block diagrams are included.
SMC Microsystems Application Note 1-1 (18 pg.)

8 **"TMS9900 Floppy Disk Controller"**
(TMS9900)
Illustrates use of the TMS9900 microprocessor system as floppy disk drive controller that interfaces to a RS-232C type terminal. Includes descriptions of hardware, diskette data transfer, and software.
Texas Instruments Application Report MOSA5 (68 pg.)

9 **"TMS9900 CRT Controller"**
(TMS9900)
Analyzes a CRT controller system that employs a TMS9900 microprocessor. Contains diagrams of the system and a software monitor routine.
Texas Instruments Application Report MOSA6 (32 pg.)

General

10 **"A Non-Volatile Microprocessor Memory Using 4K N-Channel MOS RAMs"**
See listing under (Memory) RAMS (Motorola)

General (cont)

11 **"Crystals: Specifications for Intel Components"**
Discusses crystal specifications, operation, and selection as they relate to use with various Intel components.
Intel AP-35 (4 pg.)

12 **"Microprocessors — An Introduction"**
Shows system components, defines terms and describes operation of an elementary computer system.
National AN-114 (4 pg.)

13 **"Increasing Throughput for IMP-16 Serial Input/Output"**
(MM5303)
Describes use of device to improve communication between microprocessor and peripheral with little increase in component count.
National AN-160 (7 pg.)

14 **"SC/MP Mates with Cassette Recorder"**
(SC/MP)
Describes a method of storing digital information on cassette tape.
National AN-163 (12 pg.)

15 **"Timesharing Users Manual"**
(IMP-8, IMP-16)
Gives user information to assemble IMP-8 or IMP-16 programs using Tymshare, Inc. services, or IMP-16 programs using the General Electric Computer Timesharing facility.
National (35 pg.)

Programming

16 **"Microprogramming Handbook"**
(2911, 2909, 29811, 2922, 29803)
Discusses microprogramming a bipolar processor. Includes sections on microprogram memory, sequencing, branching, jumping, and subroutines.
Advanced Micro Devices, $5.00 (44 pg.)

17 **"HM-6100 Microprocessor Basic 4K Software"**
(HM6100)
Describes the Digital Equipment Corp. PDP-8 software.
Harris Application Note HM003 (4 pg.)

18 **"HM-6100 ROM Based Subroutine Calls"**
(HM6100)
Describes two methods for returning to the proper program location after executing a subroutine.
Harris Application Note HM008 (4 pg.)

19 **"Series 3000 Cross Microprogramming System CROMIS Reference Specification"**
(3000)
Describes the CROMIS microprogramming system for the 3000 series computing elements. It supports the user who wants to generate microcode.
Intel $5.00 (77 pg.)

20 **"8080/8085 Assembly Language Programming Manual"**
(8080A, 8085A)
Primarily a reference manual, this manual describes the 8080/8085 instruction set, assembly language concepts, assembler directives, macros, programming techniques and interrupts.
Intel $5.00 (210 pg.)

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Programming (cont)

1 **"PL/M-80 Programming Manual"**
(8080, PL/M-80)
Provides in readable format a complete description of the PL/M language as implemented by the PL/M-80 compiler.
Intel $5.00 (134 pg.)

2 **"MCS-48 and UPI-41 Assembly Language Manual"**
(8041, 8048, 8741, 8748, MCS-48, UPI-41)
Describes the assembly language for programming the MCS-48 and UPI-41 single device microcomputers. Covers procedures and controls for operating the assemblers to translate the source file into object code.
Intel $5.00 (192 pg.)

3 **"Series 3000 Microprogramming Manual"**
(3000)
Fundamentals of the 3000 series microprocessor and Cross Microprogramming System are described. Presents XMAS, XMAP languages and microprogramming techniques.
Intel $5.00 (73 pg.)

4 **"IM6100 CMOS Microprocessor Basic 4K Software"**
(IM6100)
Describes use of the Digital Equipment Corp. PDP-8 software.
Intersil Application Bulletin M003 (7 pg.)

5 **"ROM Based Subroutine Calls with the IM6100"**
(HM6100)
Describes two methods for returning to the proper program location after executing a subroutine.
Intersil Application Bulletin M008 (6 pg.)

6 **"DECUS PDP-8 Software Program Library"**
(IM6100)
Describes the Digital Equipment Computer Users Society (DECUS) as a source of programs written for the PDP-8 family and also usable with the IM6100.
Intersil DCAN001 (4 pg.)

7 **"6500 Programming Manual"**
(MCS6500 Series)
Describes the software aspects of the 6500 microprocessor family and related support devices.
MOS Technology $6.95

8 **"F8 Programmer's Guide"**
(F8)
Describes how to write programs for the F8 microprocessor system which cause the system to function as a discrete logic element.
Mostek $5.95 (304 pg.)

9 **"M6800 Evaluation Module Users Guide"**
(MC6800)
Provides general information, installation instructions, preparation and operating procedures for the M6800 evaluation module.
Motorola $5.00 (150 pg.)

10 **"M6800 Microprocessor Programming Manual"**
(MC6800)
Provides information needed to program the unit, discusses the instruction set, source language, assembler, simulator, Build-Virtual-Machine and HELP programs. Gives program examples.
Motorola $10.00 (303 pg.)

Programming (cont)

11 **"IMP-16 Programming Techniques"**
(IMP-16)
Discusses several aspects of the instruction set to enable programmer to code more efficiently. Includes discussion of subroutines, subroute parameter passing, recursive subroutines, as well as sample programs.
National AN-111 (6 pg.)

12 **"A Microprogram Development System"**
(IMP-16)
Describes the application of microprogramming to LSI processors and the advantages of a microprogram development system for hardware and software.
National AN-123 (6 pg.)

13 **"SC/MP Microprocessor Assembly Language Programming Manual"**
(SC/MP)
Covers an overview, Assembly Language, statements, programming techniques, macros and I/O formats.
National $5.00 (108 pg.)

14 **"SC/MP NIBL Reference Guide"**
(SC/MP)
Reviews NIBL programming language basic including necessary hardware, expressions and functions, I/O, and control statements. Appendices cover formal grammar, error messages, and BAGELs-a simple game.
National (26 pg.)

15 **"μPD379 Application Note"**
(μPD379)
Bisync and SDLC protocols using the μPD379.
NEC Microcomputers $1 (20 pg.)

16 **"Microprocessor Interface Software"**
(NC7033)
Describes how to interface the NC7033 MN05 non-volatile memory directly with an 8085 or 8080 microprocessor.
Nitron AN101 (28 pg.)

17 **"COSMAC Software Development Program on GE Mark III Time Sharing System"**
(CDP 1802)
Describes the COSMAC Software Development Package (CSDP) available for the GE Mark III time sharing system. Briefly covers the assembler and the simulator debugger which make up the package.
RCA ICAN-6656 (4 pg.)

18 **"Timesharing Manual for the RCA CDP1802 COSMAC Microprocessor"**
(CDP1802)
Discusses two assembly languages in the COSMAC software development package. Examines using the package, tells how to use it and develops a sample program.
RCA MPM-202 $10.00 (58 pg.)

19 **"Bit and Byte Testing Procedures"**
(2650)
Describes several methods of testing the contents of the internal registers.
Signetics AS51 (4 pg.)

20 **"General Delay Routines"**
(2650)
Covers software routines to generate time delays.
Signetics AS52 (3 pg.)

MICROPROCESSORS

Programming (cont)

1 **"Binary Arithmetic Routines"**
(2650)
Covers routines for binary addition, subtraction, multiplication and division.
Signetics AS53 (15 pg.)

2 **"Conversion Routines"**
(2650)
Covers Binary to BCD, BCD to ASCII, Hexadecimal to ASCII and vice versa.
Signetics AS54 (17 pg.)

3 **"Sorting Routines"**
(2650)
Describes several examples for implementing sort routines on the 2650 microprocessor. Techniques covered include the "bubble" sort, "search" sort, and "linear" sort. Flow charts and sample programs included.
Signetics AS56 (18 pg.)

4 **"2650 Binary Floating Point Routines"**
(2650)
Describes routines for performing addition, subtraction, multiplication, and division of binary floating point operands in normalized two's complement notation. Includes sample programs and flowcharts.
Signetics AS57 (13 pg.)

5 **"2650 BCD Floating Point Routines"**
(2650)
Describes routines for performing addition, subtraction, multiplication, and division of BCD floating point operands in normalized signed-magnitude notation. Provides sample flowcharts and programs.
Signetics AS58 (14 pg.)

6 **"Generating the Cyclic Redundancy Check in Software"**
(2650)
Describes software method of generating the CRC character using the 2650.
Signetics M23 (2 pg.)

7 **"2650 Initialization"**
(2650)
Covers start up procedures.
Signetics MP51 (1 pg.)

8 **"2650 Evaluation Printed Circuit Board"**
(2650)
Covers features and connections for this card level evaluation and design tool.
Signetics SP50 (14 pg.)

9 **"2650 Demo System"**
(2650)
Complete demonstration system when used with the 2650 PC1001.
Signetics SP51 (7 pg.)

10 **"Support Software for Use with the NCSS Timesharing System"**
(2650)
Covers a cross-assembler, cross-simulator and two utility programs (to load the 2650 and to burn PROMs.)
Signetics SP52 (7 pg.)

11 **"Simulator, Version 1.2"**
(2650)
Changes to the simulator.
Signetics SP53 (1 pg.)

Programming (cont)

12 **"Support Software for Use with GE's Mark III Timesharing System"**
(2650)
Presents a series of programs that provide on-line support for the development of programs to be run on the microprocessor. Programs include a cross assembler and a cross simulator.
Signetics SP54 (8 pg.)

13 **"Pipbug"**
(2650)
Program for the 2650 PC1001 demonstration card.
Signetics SS50 (13 pg.)

14 **"Absolute Object Format"**
(2650)
Describes the format of the absolute code.
Signetics SS51 (1 pg.)

15 **"Signetics Micro Assembler Reference Manual"**
(N2901, N3002, 8X02)
Describes this FORTRAN program developed as a design tool for writing microprograms. This microprogram defines his own assembly language, writes the microprogram, then assembles it to generate tapes to load memory. Suitable for most microprogrammed applications.
Signetics $4.00 (74 pg.)

16 **"An Introduction to RIO Text Processing"**
Presents for the beginning microcomputer user an introductory overview of the fundamentals of Relocatable Modules and I/O Management.
Zilog Application Note AN1 (24 pg.)

17 **"The Z80 Family Program Interrupt Structure"**
(Z80)
Describes the Z80 interrupt structure, which includes one non-maskable and three software maskable interrupt modes. Provides flow charts, timing diagrams, and circuit diagrams.
Zilog Application Note (31 pg.)

Systems

18 **"AM2914 Priority Interrupt Encoder"**
(AM2913, AM2914, AM2900, 9080A)
Provides data sheet information on devices. Outlines construction of a microprogrammable, bipolar, LSI interrupt structure for the 2900 and 9080A processors using the 2914.
Advanced Micro Devices (33 pg.)

19 **"The 8080A/9080A MOS Microprocessor Handbook"**
(8080A, 9080A, 8212, 8255, 9555, 8251, 9551)
Provides descriptions of the 9080A CPU and the associated clock generator and system controllers. Supplies data sheet information on various I/O interfaces, support circuits, and memories. An application section covers clock generation, memory system design, timing, interrupts, and multiplication.
Advanced Micro Devices, $7.95 (280 pg.)

20 **"A Microprogrammed 16-Bit Computer"**
(AM2901, AM2902, AM2914, AM2913, AM29705)
Presents computer design starting with the specification of a computer from a functional standpoint. Describes architectural units including the ALU, the Program Control Unit, and memory.
Advanced Micro Devices $5.00 (47 pg.)

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Systems (cont)

1 **"An Emulation of the AM9080A: An example of a Microprogrammed Machine"**
(AM2901A, AM2909, 9080A)
Describes the emulation of an 8-bit μP built around four 4-bit slices and three microprogrammed sequences. Provides instruction set and clock cycle tables, block diagrams, a parts list, schematics, a printout of the microprogram definition, and a print out of the assembler statements and object code in an interleaved format.
Advanced Micro Devices $5 (47 pg.)

2 **"S2000 Extended Memory Applications"**
(S2000)
Shows four methods for connecting external memory to the S2000 single-chip microcomputer.
American Microsystems (5 pg.)

3 **"Microprocessor Systems Handbook"**
Explains μP hardware, the interaction of hardware and software, and the interfacing of μP's with A/D and D/A converters. Topics covered include memory addressing, I/O operations, and applications of various microprocessors.
Analog Devices $9.50 (218 pg.)

4 **"Analog Input/Output for Microprocessors Made Easy"**
(MP10, MP11, MP20, MP21)
Outlines features of devices and describes various ways each can be handwired to suit user configurations. Includes block diagrams of hookups with SC/MP, Z80, F8, 6800, 8080, 8085 and 9002 MPUs as well as discussion of memory mapped vs. accumulator I/O.
Burr Brown AN-87 (6 pg.)

5 **"Software Conversion of Analog Outputs to Analog Inputs"**
(MP10, MP11)
Discusses using the devices as an analog input system with diagrams illustrating hookups to the 6800 and 8080. Includes software program for each processor as well.
Burr Brown AN-88 (4 pg.)

6 **"F8 Microprocessor Application Manual"**
(F8)
Covers details concerning bit manipulation, RAM expansion of the I/O ports, subroutines and boot strap loaders.
Fairchild

7 **"PIC1650 8 Bit A to D Example Program"**
(PIC1650)
Provides diagram, flowchart, and example program for an A/D converter system using the device.
General Instrument Bulletin 1001 (3 pg.)

8 **"Advanced General Purpose Interface for Microcomputer Control Systems"**
(IOB1680, PIC1650)
Provides descriptions of both devices; one, a general purpose I/O buffer (IOB1680); the other, a peripheral microcomputer designed to take the load off a central processor. Supplies block diagrams of each and an instruction set summary for the PIC1650.
General Instrument Bulletin 1002 (5 pg.)

9 **"Static Memory Systems Utilizing the HM-6100"**
(HM6100)
Describes CMOS, nonvolatile CMOS and NMOS memory systems.
Harris Application Note HM004 (7 pg.)

Systems (cont)

10 **"HM-6100 CMOS Microprocessor Teletype Interface"**
(HD6402, HM6100)
Describes a teletype interface using the HM6100 and a UART.
Harris Application Note HM005 (7 pg.)

11 **"HM-6100 Operator Console"**
(HM6100)
Describes the 6900-CONTROL console for the prototyping system.
Harris Application Note HM006 (4 pg.)

12 **"HM-6100 CMOS Microprocessor Memory Extension"**
(HM6100)
Discusses a memory extension controller to increase the memory from 4096 to 32,768 words.
Harris Application Note HM007 (4 pg.)

13 **"8255 Programmable Peripheral Interface Applications"**
(8255)
Provides hardware and software information for this byte oriented I/O device. Examples cover character printer, paper tape and 8080-8080 interface applications.
Intel Application Note AP-15 $1.00 (32 pg.)

14 **"Intel MULTIBUS Interfacing"**
(MULTIBUS, 8080)
Describes this system bus structure, signals and characteristics. Includes electrical and mechanical information needed to build slave modules.
Intel AP-28 $1.00 (21 pg.)

15 **"Using the 8259 Programmable Interrupt Controller"**
(8259)
Reviews the concept of interrupts, then explains the 8259 as a component and shows its use in supporting a battery back up scheme for RAMs and a 78 level interrupt system.
Intel AP-31 (24 pg.)

16 **"Application Techniques for the 8085A Bus"**
(2117, 8085A, 8085A-2)
Discusses techniques for ensuring bus compatibility when using the 8085A and 8085A-2 microprocessor components. Covers interfacing the 8085A with the 2117 dynamic RAM, 8085A clock in vs clock out control timings, and bus loading limitations.
Intel AP-38 (31 pg.)

17 **"Simplify Your Dynamic RAM/Microprocessor Interface"**
(2104A, 2107A, 2107B, 2116)
Compares static and dynamic RAMs, then outlines elements of dynamic RAM/μP interface design including: refresh techniques, address multiplexing, memory overlap and transmission line effects.
Intel Application Note APR-1 $1.00 (65 pg.)

18 **"8080/8080A Microcomputer"**
(8080/8080A)
Presents device, failure mechanisms, testing methods and results.
Intel RR-10 (13 pg.)

19 **"8080 Microcomputer Systems User's Manual"**
(8080A)
Data sheets, architecture, timing requirements, and instruction sets for the MSC80 family.
Intel $5.00 (238 pg.)

MICROPROCESSORS

Systems (cont)

1 **"MCS-48 Microcomputer User's Manual"**
(8048, 8748, 8035, 8155, 8243, 8355, 8755, MCS-48)
Describes the system architecture, instruction set, programming, expansion, hardware and software examples, extensive data sheets.
Intel $5.00 (305 pg.)

2 **"UPI-41 User's Manual"**
(8041, 8741, 8243, UPI-41)
Describes this Universal Peripheral Interface device operation, instruction set, system design and interfacing.
Intel $5.00 (115 pg.)

3 **"MCS-85 User's Manual"**
(8085, MCS-85)
Describes this 8085 based system and peripheral components. Extensive coverage through data sheets.
Intel $5.00 (273 pg.)

4 **"Using the 8251 Universal Synchronous/Asynchronous Receiver/Transmitter"**
See listing under (Digital) Data Transmission (Intel)

5 **"Static Memory Systems for the IM6100"**
(IM6100)
Describes CMOS, nonvolatile CMOS and NMOS memory systems for the IM6100.
Intersil Application Bulletin M004 (14 pg.)

6 **"Teletype Interface for the IM6100 CMOS Microprocessor"**
(IM6100)
Describes a Teletype interface using the IM6100 and a UART.
Intersil Application Bulletin M005 (10 pg.)

7 **"IM6100 Operator Console"**
(IM6100)
Describes the 6900-CONTRL console for the prototyping system.
Intersil Application Bulletin M006 (17 pg.)

8 **"IM6100 CMOS Microprocessor Memory Extension"**
(IM6100)
Discusses a memory extension controller to increase the memory from 4096 to 32,768 words.
Intersil Application Bulletin M007 (6 pg.)

9 **"The ICL7104: A Binary Output A/D Converter for μProcessors"**
(ICL7104, ICL8052)
Describes designing with this 2 device A/D converter in detail. Discusses interfacing with and without handshakes, performance enhancement, and external auto-zero. Includes schematics, block diagrams, and graphs.
Intersil Application Bulletin A030 (14 pg.)

10 **"A Powerful Microprogram Controller: The 67110"**
(67110)
Describes features of the device including organization, internal interrupts, and memory expansion.
Monolithic Memories (5 pg.)

11 **"5701/6701: 4-Bit Expandable Bipolar Microcontroller"**
(5701, 6701)
Provides functional descriptions of the device, instruction set, timing and more.
Monolithic Memories Application Note (23 pg.)

Systems (cont)

12 **"6500 Hardware Manual"**
(MCS6500 series)
Describes the hardware aspects of the 6500 microprocessor family and related support devices.
MOS Technology $6.95

13 **"TIM Manual"**
(MCS6530)
Describes the program contained in the ROM portion of the 6530-004.
MOS Technology $5.00

14 **"F8 Microprocessor Hardware Support-Evaluation Kit"**
(F8)
Describes this kit and its use. Includes a sample program to acquaint the user with F8 machine language and shows how to program the kit.
Mostek (20 pg.)

15 **"Expanding Mostek's F8 Microprocessor External Interrupt Capability"**
(F8)
A detailed discussion of servicing control inputs in a F8 based system with emphasis on implementing interrupt driven systems.
Mostek (12 pg.)

16 **"Subroutine Nesting and Multiple Interrupt Handling Using Mostek's F8 Microprocessor"**
(F8)
Discusses the use and implementation of subroutines and interrupts as they apply to programming an F8 based system.
Mostek (16 pg.)

17 **"Z80 Interfacing Techniques for Dynamic RAM"**
(Z80, MK4027, MK4116)
Provides specific examples of interfacing 16-pin dynamic memories to the Z80 microprocessor. Includes timing diagrams and refresh information.
Mostek

18 **"Analog-to-Digital Conversion Techniques with the M6800 Microprocessor System"**
(MC1405, MC6800)
Describes successive approximation and dual ramp techniques for A/D conversion using the M6800. Gives flow diagrams, source programs and schematics. Appendix gives program for binary to BCD conversion.
Motorola AN-757 (35 pg.)

19 **"MEK6800D2 Microcomputer Kit System Expansion Techniques"**
(MC6800)
Covers techniques to add 8K or 16K of memory, I/O port expansion, power-up auto-reset, switch selectable monitor operation, and RS-232 or current-loop data terminal operation.
Motorola AN-771 (23 pg.)

20 **"A Simple High Speed Bipolar Microprocessor Illustrates System Design and Microprogram Techniques"**
(MC10801, MC10803)
Describes a complete bipolar LSI systems design using 10 ICs to perform 2's complement add, subtract, multiply and divide.
Motorola AN-774 (12 pg.)

21 **"M6800 Systems Utilizing the MC6875 Clock Generator/Driver"**
(MC6875)
Gives extensive design examples using the MC6875 in systems including slow or dynamic memories, and DMA (multiprocessor) applications.
Motorola AN-775 (20 pg.)

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Systems (cont)

1 **"The M10800 MECL LSI Processor Family — Three Descriptive Articles"**
(MC10800, MC6800)
Presents three articles about the device: "Get the Best Microprocessor Performance"; "The MSP: GTE Sylvania's Microsignal Processor"; "M10800 Microprogrammed Demonstrator". The first examines features of the processor; the second discusses a customer application; and the third describes a demonstrator treated as a peripheral to the M6800 system.
Motorola AN-776 (21 pg.)

2 **"Synchronizing Two Motorola MC6802s on One Bus"**
(MC6802)
Discussion, circuit and timing diagrams describing synchronizing two MPUs on the same data bus.
Motorola AN-783 (2 pg.)

3 **"M6800 System Microcomputer System Design Data"**
(MC6800)
Describes the family of parts including data sheets.
Motorola (165 pg.)

4 **"Device Operation and System Implementation of the Asynchronous Communications Interface Adapter MC6850"**
See listing under (Digital) Data Transmission (Motorola)

5 **"Applications of LSI Processors"**
(IMP-16)
Describes system architecture and operation of IMP-16C, 16-bit parallel processor with self-contained memory. Describes applications in a data communication link analyzer, in point-of-sales and in retailing systems.
National AN-98 (8 pg.)

6 **"Increasing the Number of Control Flags and Jump Conditions in the IMP-16C"**
(IMP-16C)
Describes simple and economical method of increasing the number of testable jump conditions and the number of control flags on the IMP-16C microprocessor.
National AN-101 (4 pg.)

7 **"Clock-Hold Schemes for the IMP Microprocessor Family"**
(IMP-8C, IMP-16C)
Presents scheme to extend the clock-hold function for additional periods of the main system clock, using the DM8570 shift register.
National AN-105 (4 pg.)

8 **"IMP-16 Interrupts"**
(IMP-16)
Describes various types of interrupts, including an overview of interrupt structure, example of interrupt request and service, multilevel and control panel interrupts.
National AN-107 (23 pg.)

10 **"IMP-16C Peripheral Interfacing Simplified"**
(IMP-16C)
Explores techniques for interfacing peripheral devices to the microprocessor.
National AN-124 (4 pg.)

11 **"IMP-16L DMA — What It Is and How to Use It"**
(IMP-16)
Discusses general theory of the DMA Bus, gives examples of priority expansion and data transfer.
Naitonal AN-135 (6 pg.)

Systems (cont)

12 **"Designing with the IMP Chip Set"**
(IMP-16)
Describes some of the major considerations in the implementation of 4 to 32 bit systems using the IMP series of devices. A 16 bit system is covered in detail.
National AN-141 (10 pg.)

13 **"Using a Microprocessor Beyond Apparent Speed"**
(IMP-16)
Covers the concept of cycle stealing, a technique in which a peripheral device communicates directly with memory or another peripheral device while the CPU is doing work other than using the data and address buses.
National AN-142 (6 pg.)

14 **"Number Cruncher (MM57109) Interface to Microprocessor"**
(MM57109)
Describes the MM57109 number cruncher unit which can perform most arithmetic functions found in complex hand-held calculators and interfaces either to a microprocessor or a random logic system. Provides schematics of interface logic and a flow chart for initialization of the device.
National AN-186 (10 pg.)

15 **"Clock Considerations For SC/MP-II"**
(SC/MP)
Shows several methods of providing a clock for the SC/MP-II.
National AN-188 (4 pg.)

16 **"Serial Data Transfers with SC/MP-II"**
(SC/MP)
Discusses serial data I/O data transfer using the SC/MP-II extension register.
National AN-190 (3 pg.)

17 **"Multiprocessing with SC/MP"**
(SC/MP)
Presents a brief analysis of the multiprocessing capabilities and characteristics of the SC/MP microprocessor based on measured data.
National Semiconductor AN-197 (6 pg.)

18 **"Bit-Slice Microprocessor Design Takes a Giant Step Forward with "Schottky-Coupled-Logic" Circuits"**
(IDM2900)
Covers a four-bit slice Schottky-coupled-logic design that combines the flexibility of the industry standard 2900 microprocessor architecture with advanced LSI processing.
National Semiconductor AN-203 (1 pg.)

19 **"GCP/P Product Description"**
(GCP/P)
Delineates the system, gives a functional description of the CROM and RALU devices, and presents the general purpose macroinstruction set. Appendices cover a microprogram to implement the IMP-16 instructions set and the use of the RALU status flag.
National (61 pg.)

20 **"POWER I/O CROM Technical Description"**
(IMP-16)
Describes the instruction repertoire and use of this unit which expands the variety of memory and input-output operations of the IMP-16.
National (22 pg.)

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Systems (cont)

1 **"PACE Technical Description"**
(PACE)
Defines and explains how to use the hardware and software that support the PACE system.
National (96 pg.)

2 **"N8080 System Design Manual"**
(INS8080A, DP8212, DP8216, DP8224, DP8226, DP8228, DP8238, INS8251, INS8255)
Describes the INS8080A μP including architecture, timing, data and instruction representation, and I/O operation and control. Also covers use of various support chips.
National $5.00 (72 pg.)

3 **"Data Acquisition System Interface to Computers"**
See listing under (Linear) Converters (National)

4 **"A PROM Programmer for the SC/MP LCDS"**
See listing under (Memory) PROMs (National)

5 **"μPD371 Magnetic Tape Cassette/Cartridge Controller Users Manual"**
(μPD371)
Gives description, timing and circuit diagrams. Assembly language listing for use with NEC's 8080A.
NEC Microcomputers $10.00 (58 pg.)

6 **"μPD372 Floppy Disk Controller Users Manual"**
(μPD372)
Provides text, timing diagrams and schematics plus software listings.
NEC Microcomputers $10.00 (70 pg.)

7 **"μPD372 Mini-Floppy Disk Controller Users Manual"**
(μPD372)
Supplements the Floppy Disk Manual for Mini-Floppy applications.
NEC Microcomputers $10.00 (44 pg.)

8 **"MN1400 Series 4-Bit One-Chip Microcomputers User's Manual"**
(MN1400, MN1402, MN1498, MN1499)
Introduces the MN1400 family. Encompasses system architecture, timing, and the instruction set including examples of various commands and routines.
Panasonic (65 pg.)

9 **"Hexadecimal Keyboard Interface for Use with RCA COSMAC Development Systems"**
(CDP1800)
Circuit and program including debounce routine for 16 key keyboard.
RCA ICAN-6516 (2 pg.)

10 **"Guide to Better Handling and Operations of CMOS Integrated Circuits"**
Recommends specific handling and operating practices to minimize the probability of damage in manufacturing and field environments.
RCA ICAN-6525 (5 pg.)

11 **"Register-Based Output Functions for RCA COSMAC Microprocessors"**
(CDP1802, CDP1852)
Describes circuits using the CDP1852 I/O port for outputting information from any of the 16 general purpose scratch pad registers of the CDP1802 microprocessor.
RCA ICAN-6562

Systems (cont)

12 **"Design of Clock Generators for Use with RCA COSMAC Microprocessor"**
(CDP1802)
Describes a crystal controlled clock generator using on-chip circuits and crystal and RC generators using external circuits.
RCA ICAN-6565

13 **"Power-On Reset/Run Circuits for the RCA CDP1802 COSMAC Microprocessor"**
Provides diagrams and discussions of several circuits which enable a power-on reset/run capability for the device.
RCA ICAN-6581 (2 pg.)

14 **"Use of the CDP1856 and CDP1857 Buffer/Separator in CDP1802 Microprocessor Systems"**
(CDP1802, CDP1856, CDP1857)
Describes use of the CPD1856 and CPD1857 four-bit buffers or separators in the CDP18S020 Evaluation Kit and CDP18C024 E-K/Assembled-Editor Design Kit. Includes functional diagrams.
RCA ICAN-6657 (4 pg.)

15 **"User Manual for the CDP1802 COSMAC Microprocessor"**
(CDP1802)
Describes the device architecture and its instruction set with examples of each command. Reviews basic programming techniques and suppiies timing diagrams.
RCA MPM-201B $5.00 (115 pg.)

16 **"Low Cost Crystal Oscillator for Clock Input"**
(R6500)
Describes a low cost oscillator circuit which produces the basic input frequency required by the clock generator circuits in the R650X series microcomputers. The circuit uses one of two readily available low cost crystals. Circuit diagram.
Rockwell Document No. 1 (1 pg.)

17 **"Techniques for Using Two or More SDC's in a PPS Microcomputer System"**
(PPS-4, PPS-8)
Details various addressing techniques to employ up to 16 Serial Data Controller input/output devices in a PPS-4 or -8 microcomputer system. Three different techniques are covered.
Rockwell Document No. 10930 N20 (1 pg.)

18 **"TDI Stand-Alone"**
(10371)
Describes the connections required to use the Telecommunications Data Interface for stand-alone operation. Circuit diagram.
Rockwell Document No. 29009 N.21 (2 pg.)

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(PPS-4/1)
Details a communications protocol that can be implemented between two PPS-4/1 microprocessors using only five interface lines.
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20 **"Microprocessor Prototyping Card"**
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Describes features of the 2650PC1001 microcomputer.
Signetics Application Memo (2 pg.)

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Categorizes the various components used to implement major sections of a typical microprocessor system.
Signetics AM-1 (4 pg.)

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Systems (cont)

1 **A User's Guide to the Series 3000 Microprocessor Chip Set"**
(N3001, N3002)
Describes devices, instruction sets. Design examples included.
Signetics AM-2 (14 pg.)

2 **"Interface Techniques for the 2651 PCI"**
(2651)
Covers interfacing the 2651 programmable communications interface with the SC/MP, Z80, 8085, and 6800 microprocessors.
Signetics M22 (8 pg.)

3 **"Using the 2651 with BISYNC"**
(2651)
Details how the 2651 PCI supports IBM's Binary Synchronous Communications protocol.
Signetics M24 (4 pg.)

4 **"Application Technique for the 2651 PCI"**
(2651)
Shows application technique for the 2651 programmable communications interface.
Signetics M26 (2 pg.)

5 **"Low Cost Clock Generator Circuits"**
(2650)
Presents several crystal oscillator clock generator circuits that can be used with the 2650 microprocessor. All use standard TTL 7400-series logic elements.
Signetics MP52 (5 pg.)

6 **"Address and Data Bus Interfacing Techniques"**
(2650)
Discusses address and data bus drive requirements. Covers methods for increasing the system drive capability.
Signetics MP53 (8 pg.)

7 **"2650 Input/Output Structures and Interfaces"**
(2650)
Examines the use of the 2650 microprocessor's set of I/O instructions and the interface between the 2650 and I/O ports. Examples for both serial and parallel I/O are given. Provides diagrams and sample programs.
Signetics MP54 (19 pg.)

8 **"2650 Demo System"**
(2650)
Describes hardware base for use with 2650 CPU printed circuit board (PC1001).
Signetics SP51 (6 pg.)

Systems (cont)

9 **"The ABC Adaptable Board Computer"**
(2650)
Describes a low cost system development card for the 2650 microprocessor. Supplies PC board diagram, assembly drawing, and memory organization map.
Signetics SP55 (14 pg.)

10 **"Application Memo to Control Store Sequencer 8X02"**
(8X02)
Presents a functional description and gives microprogramming system suggestions.
Signetics Bipolar Application Memo 3 (7 pg.)

11 **"Interfacing the 8700 A/D Converter with the 8080 μP System"**
(8700, 8701, 8702)
Presents use of the 8700 A/D converter with the 8080 microprocessor. Provides techniques for interfacing the two and methods for handling multiple converts with increased throughput.
Teledyne Semiconductor AN-8 (6 pg.)

12 **"Minimum System Design TMS 9900 16-Bit Microprocessor"**
(TMS9900)
Explains system design, system performance, and minimum system configuration.
Texas Instruments Application Report (CA-184A (7 pg.)

13 **"TMS 5501 I/O in TMS 8080A μP Systems"**
(TMS5501, TMS8080A)
Describes operation and use of this input/output controller.
Texas Instruments Application Report (CA-185A (18 pg.)

14 **"Software Design for Microprocessors"**
(SBP0400, TMS1000, TMS5501, TMS8080, TMS9900)
Presents basic microprocessor fundamentals. Includes such topics as basic terms, basic machine architecture, instruction sets, and programming. Sample design problems are examined.
Texas Instruments $12.50 (385 pg.)

15 **"Interfacing 16 Pin Dynamic RAMs to the Z80A Microprocessor"**
(Z80)
Presents the major design considerations, and a design example, for interfacing 16-pin dynamic RAMs, both 4k and 16k, to the Z80 and Z80A. Supplies circuit and timing diagrams.
Zilog Application Note (27 pg.)

"LAST PAGE THIS SECTION, NEXT PAGE 220"

APRIL 1976
Jim Sherwin
National Semiconductor Corp.

DATA ACQUISITION SYSTEM INTERFACE TO COMPUTERS

INTRODUCTION

The need of interfacing several analog data channels to computers has not escaped the attention of the data system firms. There are presently available a number of data acquisition units (DAUs) which will directly interface 8-64 analog data channels to one or more types of computers or microcomputers, and more appear on the market almost monthly. Some of these DAUs are even constructed to plug into the mainframe of the computer for which they are designed. Nearly all of these commercially available DAUs are of more or less conventional design, operating in either a random channel address or sequential address mode. Figure 1 shows a typical functional diagram of such a random channel address DAU. Its advantages are simplicity, straightforward design, and comparatively low cost (depending upon performance and special features). In operation, the computer addresses a specific channel, the analog multiplexer (MUX) is set to the desired channel, a sample and hold (S&H) circuit acquires and holds the analog signal, an analog-to-digital converter (ADC) digitizes the signal, a ready signal is returned to the computer, and the data is presented to the data bus via TRI-STATE® bus drivers. If the data is 12-bit and the data bus is 8-bit, the data word must be broken into two bytes and addressed separately. The prime disadvantage of these DAU designs is that the computer must either enter a wait mode while data is readied or it can proceed with its assigned task, watch for a data-ready flag signal, and return for the data.

From the standpoint of microprocessor system design, it is clearly desirable to access input data as if it were main memory. It is further desirable that input data access time be equivalent to that of main memory so that the processor need not enter a wait mode while data is readied for input. One attractive method of accomplishing this is to use one A/D converter (of a type containing TRI-STATE output data latches) on each input data channel. Henceforth I shall refer to this as parallel conversion. Figure 2 shows such a system containing only an address decoder and multiple A/D converters with all outputs wired in parallel onto the data bus. Note the absence of S&H modules.

The advantages of this DAU system are the immediate data access and its simplicity. However, one's first thought on considering a parallel-conversion system might be that the cost of ADCs would exclude their consideration on a one-per-channel basis. But, although this may have been true in the past, currently available monolithic and hybrid ADCs are priced such that this system concept is entirely feasible. Furthermore, the converter price trend is definitely downward as more monolithic units are released, so the economic feasibility can only improve in the next few years, thus extending the application to an ever larger segment of the market. The ideal converter for use in the system of Figure 1 includes converter, comparator, and buffered TRI-STATE output data latches in one package. The unit would

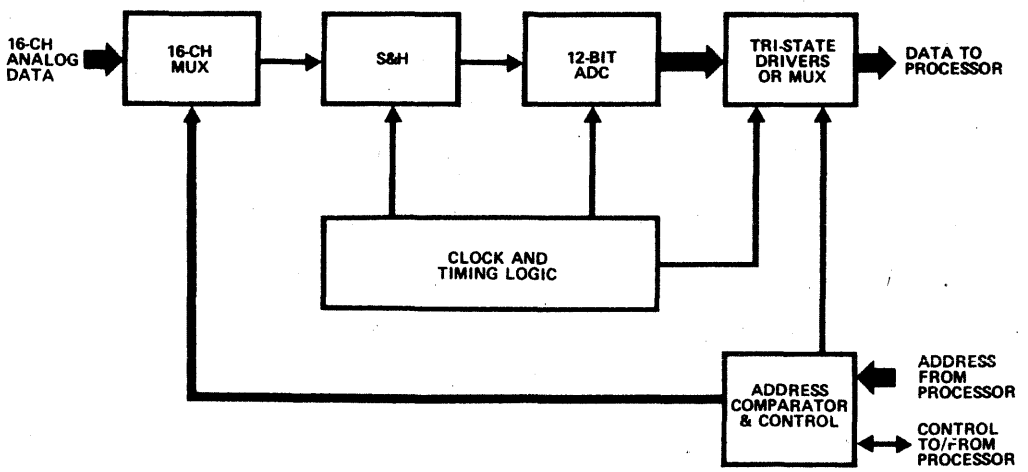


FIGURE 1. Random-Addressed Multiplexed DAU

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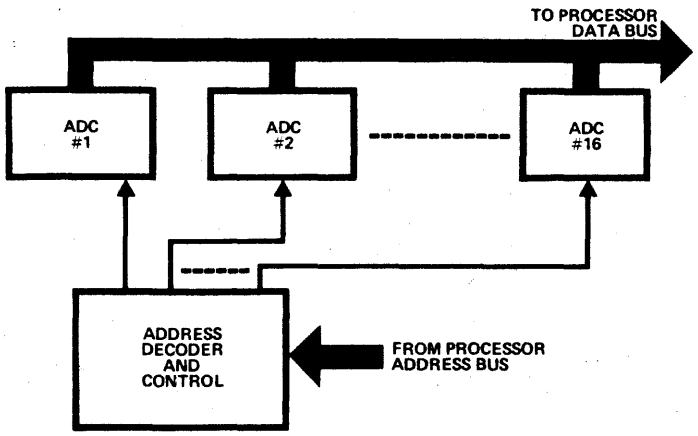


FIGURE 2. Parallel Data Conversion Concept

operate in the continuous convert mode with the last data remaining in the output latches until the next completed conversion shifts new data into the latches. Valid latest data is thus always available for readout on the data bus except for a brief period when the data is being updated. In contrast, a converter without buffered output latches does not hold data after a start-conversion signal and so must be operated in the command mode with a wait for data after the converter is started.

In spite of the advantages of the parallel-conversion DAU, there is (at present ADC prices) a more cost-effective way of providing the same immediate memory-access mode of operation, particularly for 12-bit data. Figure 3 shows a multiplexed DAU with self-contained memory which will interface to computer systems in the memory-access mode without a wait period.

The total package count of this system is lower than that of the parallel-conversion DAU, the cost/channel is lower, and the required space and power is lower. A disadvantage is that the accessed data may be as much as 800μs old, compared to a possible 1-4μs with parallel conversion. The key to the success of the system is the dedicated on-card 16x12 RAM. Neither does the system require a special ADC design with buffered output data latches. Main memory could, of course, be used instead, but then some machine time would be utilized as memory write time. This way, the latest data is always ready and waiting in the DAU (peripheral) memory, and software is considerably simplified.

Before exploring any of the three systems in more detail, it is worth considering the system limitations, the economics, and the probable market segment which could be served by the three types of DAU described.

The required data bandwidth has obvious strong effects on system cost and realization. The bandwidth of a sampled data system is limited by Shannon's sampling criterion and other practical considerations to, say,

$$f_{max} = \frac{1}{5\, t_{conversion}}$$

which is 4kHz for a 50μs conversion cycle time. However, when no S&H module is used ahead of the ADC, as in a parallel-conversion DAU, conversion must take place within the time it takes the input signal to change by ±½ LSB or 1 part in 2^{n+1}. For sine waves, the maximum rate of change is determined as follows:

$$\frac{\Delta v}{\Delta t} = \omega v_{pk},$$

but

$$v_{max} = \frac{2\, v_{pk}}{2^{n+1}}$$

therefore

$$\frac{2\, v_{pk}}{2^{n+1}\, \Delta t} = 2\pi\, f_{max}\, v_{pk}$$

and

$$f_{max} = \frac{2^{-(n+1)}}{\pi\, t_{conv}}.$$

For the same 50μs conversion time and an 8-bit accuracy requirement of ±½ LSB, f_{max} is 12Hz. Figure 4 compares data bandwidth of 8- to 14-bit systems with and without S&H. The economic effect of adding an S&H module ahead of each ADC in a parallel-conversion DAU is obvious (possibly doubling the cost per channel of an 8-bit system) as is the cost of significantly increasing conversion speed except by use of tracking converters (advantageous only in parallel-conversion systems).

The conventional random-addressed DAU can serve any part of the data acquisition market where the task of the computer is light enough that the system can afford to enter a wait mode at data request. This wait period can be as low as 10-20μs if sufficient money is available for fast S&H circuits and fast ADCs, as high-speed components are traditionally quite expensive. Lower cost systems may require a wait period of 100-200μs before data is available. At the expense of more complex software, the computer could remain busy during the period of data preparation, and would return for the data when it was made ready. The data bandwidth may be deter-

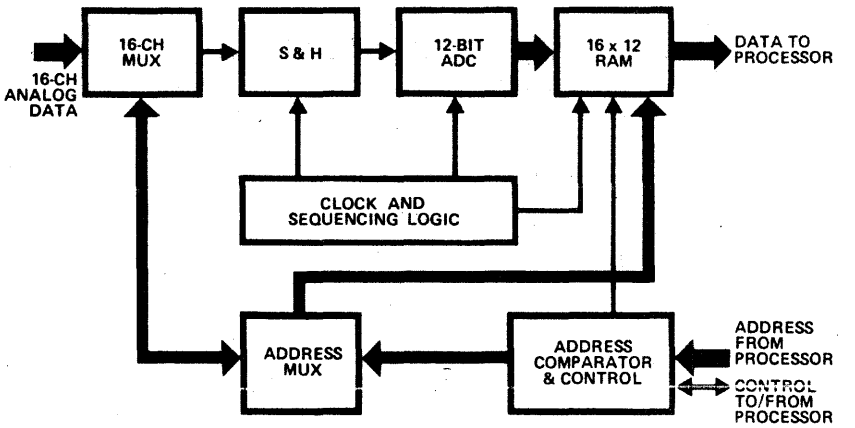


FIGURE 3. Multiplexed Immediate-Data-Access DAU

mined from Figure 4. Sixteen channels of 10Hz data could be available if each channel were sampled once every 20ms. This is a data throughput rate of 16ch x 1/20ms = 800Hz. The higher cost DAUs of this type have capability of 50-100kHz throughput rates. However, if the computer waits while data is made ready, it will be completely occupied with gathering data when the maximum throughput rate is utilized.

The parallel conversion DAU without S&H circuits is destined to operate on low-bandwidth data as indicated in Figure 4. To be economically feasible the ADCs must be of low cost. This means an 8- or 10-bit successive approximation register (SAR) or a 12-bit integrating monolithic ADC must be used. New ADC designs using tracking counters could increase data bandwidth capability over that possible with SAR counters. For purely economic reasons, then, use of parallel-conversion DAU systems will be limited to low bandwidth data – 10-30Hz on 8-bit, 2-5Hz on 10-bit, and less than 1Hz on 12-bit systems. These bandwidth figures for 8- to 10-bit systems could be considerably improved, say by 8-10 times, if tracking converters were used in place of SAR converters. This definitely suggests that there is a need for low-cost tracking converters. Note that S&H circuits are not needed in the parallel-conversion systems.

The multiplexed DAU with memory can serve any segment of the data market. It is limited in bandwidth

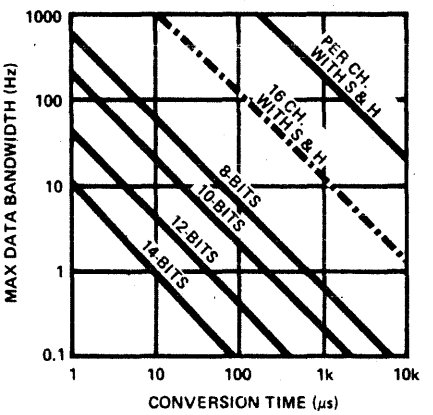


FIGURE 4. Data Bandwidth vs. Conversion Time

or data throughput rate principally by the S&H and ADC operating times, its cost per channel is only slightly higher than that of the conventional DAU, and it allows the computer to operate in the most efficient manner.

A comparison of system costs must include the following for a 16-channel system.

Parallel Conversion	Random Addressed Multiplexed	Multiplexed with Memory
16 A/D Converters	1 A/D Converter	1 A/D Converter
16 Anti-Aliasing Filters	1 S&H Module	1 S&H Module
Control Circuits	1 16-Channel Multiplexer	1 16-Channel Multiplexer
Additional power for extra converters	16 Anti-Aliasing Filters	16 Anti-Aliasing Filters
Lower data bandwidth	More complex control circuits	1 16x12 RAM
Simple software	Longer data access time	More complex control circuits
	Possibly more complex software	High-speed data access
		Simple Software

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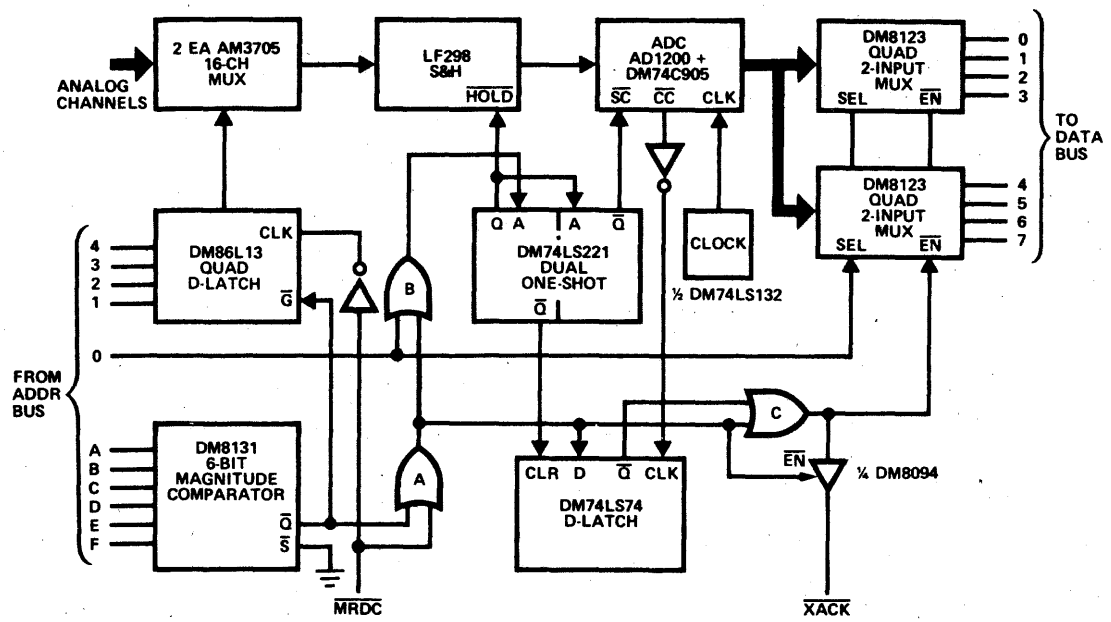


FIGURE 5. Conventional DAU for 8080

The future trends in DAU designs will include an increasing number of parallel-conversion DAUs, especially as cost reductions appear on monolithic ADCs with TRI-STATE output circuits (or latches). We should also start to see some tracking converters in the low-cost monolithics with TRI-STATE output data latches. Expect to see multiplexed DAUs with memory appearing in the near future. Its simplicity from a circuit and software standpoint cannot long go unnoticed.

RANDOM ADDRESSED DATA ACQUISITION UNIT

A conventional, random-addressed, 16-channel, 12-bit DAU is diagrammed in Figure 5. The analog section contains a 16-channel analog multiplexer, a sample-and-hold block, and a 12-bit ADC. A more complete system might contain a differential multiplexer and/or a differential (or instrumentation) amplifier preceding the S&H block. The data output circuits are arranged to interface an 8-bit data bus as found on an 8080 or 6800 microcomputer (μC). Since the data word is 12 bits, the μC must accept it in two 8-bit bytes. Normally the μC would address the DAU with two consecutive address locations corresponding to a 0 and a 1 at the address LSB to load the two bytes of data. The DM8123 multiplexers are ideally suited to this use. They have TRI-STATE output circuits, and the channel-select input may be directly driven from the address LSB. If a 16-bit address bus were being interfaced, such as in the PACE μC, the output multiplexers would be replaced with DM8097 or equivalent TRI-STATE output buffers (see Figure 11). In both instances, low-power versions of these parts, the DM81L23 and DM80L97, could be used to drive a lightly loaded data bus.

The address decoding is accomplished with a DM8161 6-bit magnitude comparator looking at the six most significant address bits. These 6 bits are compared with an address code hard wired into a DIP header which can be different for each DAU card in a system. Comparing only 6 address bits allows a possible 64 cards in a single system and uses up to 64 pages of memory position. If this is not satisfactory, two address comparators ORed together (DM8163) could select from 12 bits of address. The magnitude comparator(s) plus the four address lines to the 16-ch MUX make up the complete address decoding. The output of the magnitude comparator(s) indicates when this DAU has been addressed, and the four address lines to the MUX select the 1-of-16 channels of this DAU.

This circuit is designed to interface the 8080 μC. Thus, a memory read command $\overline{\text{MRDC}}$ must be received, and an acknowledgement $\overline{\text{XACK}}$ must be issued to indicate when data is ready. Operation is as follows: A valid address on address lines A-F causes comparator output $\overline{Q}$ to go low. This gates the inputs of the quad D latch to accept the 1-of-16 address word from address lines 1-4. At the occurrence of $\overline{\text{MRDC}}$ the address is clocked into the quad D latch and presented to the 16-ch MUX which selects the addressed channel. When $\overline{Q}$ and $\overline{\text{MRDC}}$ are both low, the output of OR gate A goes low, which enables the XACK signal buffer. If the address LSB is 0 (byte 1 of a 2-byte data request), OR gate B output goes low to trigger a one-shot.

The one-shot circuits are a simple means of timing the sample period and the converter start commands. There are other methods (see Figure 15) of accomplishing this timing without the hazards associated with one-shot circuits; however, the simplicity of this scheme lends itself to easy understanding of the timing required. The first one-shot generates a sample pulse of 5-30μs as required for the S&H to acquire and settle to 0.01% of value. Its $\overline{Q}$ output presets the single D latch ($\overline{Q}$ = 1). The trailing edge of this pulse returns the S&H to HOLD condition and triggers the next one-shot to generate a start conversion command of about 3μs. When the ADC completes conversion, its $\overline{\text{CC}}$ output goes low, thus clocking a 0 into the single D latch to reset its Q output low. Both inputs to OR gate C now being low will enable the output MUX and return a low on the XACK

line indicating to the μC that data is ready. Address LSB = 0 selects the 8 LSB of the data word for presentation to the data bus. A subsequent address with LSB = 1 selects the 8 MSB of the data word, but will not trigger the one-shot or preset the D latch because the output of OR gate B will remain high. Since the output of OR gates A and C will be low, $\overline{XACK}$ is returned and the output MUXs are enabled to present byte 2 of the data word on the data bus. When $\overline{MRDC}$ returns high, the output circuits are disabled. If the 6-bit comparator does not see a valid address, no action is taken by the DAU.

This represents the simplest possible DAU for interfacing to computers. The interface to the 8080 is one of the simplest. Only minor modifications are required to interface, for example, the 6800 or PACE μCs (see Figures 9 and 11). The only timing anomaly in the logic system shown is that when the $\overline{XACK}$ buffer is enabled there will be a 10-40ns pulse of 0 output. The computer, however, does not act on an XACK signal at this time and so will enter a wait mode until $\overline{XACK}$ is returned later on.

The analog signal section has purposely been omitted from this discussion of interfacing to processors because its details will depend upon analog signal levels, the possible requirement for differential channels, the possible need of an instrumentation amplifier following the multiplexer, and S&H timing requirements. The analog section of the DAU may be made up of various components, depending upon the required performance and operating conditions. A pair of 8-channel multiplexers will give the flexibility of connecting as differential 8-channel or as single ended 16-channel whereas a single 16-channel MUX with space and wiring on the board for another 16-channel MUX would allow for either 32 channels or 16 differential channels. A pair of AM3705s could be used for lowest cost where analog signals are no greater than ±5V. The S&H circuit could be monolithic LF198, hybrid LH0023, LH0043 or LH0053, made up of individual discrete and integrated circuits, or it could be any of several available modules.

The ADC used in this system may be of a conventional design with speed and accuracy being the only important technical considerations. No special TRI-STATE output or output data latches are needed as the data is latched in the register until a new start conversion (SC) command is given. The ADC could be made up of an AD1200 ADC building block plus DM2504 or MM74C905 successive-approximation register, it could be an AD1210 plus LH0071 reference and appropriate MOS-TTL and TTL-MOS buffers, or it could be any one of a number of other ADCs on the market.

Total power is about 2.8 watts and cost is about $9.50 per channel for components as indicated in Table 1. Note that output drivers are standard TTL circuits whereas low power TTL may be used for lower power dissipation where a lightly loaded data bus is to be driven.

PARALLEL-CONVERSION DATA ACQUISITION UNIT

Parallel data conversion is likely the simplest possible μC data system concept which will effect immediate access to latest input data as if it were main memory. It may be treated as main memory by the processor and is only slightly more complex than the simplified system of Figure 2. The individual ADCs in Figure 2 include TRI-STATE output for direct wire ORing on the data bus. However, to make each capable of driving a heavily loaded system bus would require significant and unnecessary power dissipation in each ADC. Accordingly, except in minimally loaded systems, a separate set of TRI-STATE TTL output data buffers would be added to Figure 2. Small differences in the address decoder and control circuits will exist, depending upon which μC system will be used.

The control circuits are exceptionally simple, being required primarily to accept the memory read command and to return a memory ready signal. The most complex part of the control circuits is that required of μC systems which accept data in two 8-bit bytes rather than in one 16-bit byte, yet even this added complexity is minimal.

Table 1. Conventional DAU Power & Cost

		P_D (mW)	$ (100s)
1 –	16-Channel MUX	300	19.55
1 –	S&H	500	74.50
1 –	ADC	600	40.00
2 – DM8123	Quad 2-Input MUX	800	2.56
1 – DM8161	Hex Comparator	250	2.56
1 – DM86L13	Quad D-Latch	30	1.28
1 – DM74LS221	Dual One-Shot	30	3.00
1 – DM74LS132	Quad Schmidt NAND	60	2.00
1 – DM7432	Quad OR Gate	100	.49
1 – DM74LS74	Dual D F-F	20	3.00
1 – DM8094	TRI-STATE 4 x Buffer	144	.71
		2834	150.05
			$9.38/Channel

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Table 2. Microprocessor System Characteristics

	8080	PACE	6800	SC/MP
Address Word Length	16-bit	16-bit data/address bus	16-bit	12- or 16-bit
Data Word Length	8-bit		8-bit	8-bit
Address & Data Polarity	All chips are 1 = true; however, if Intel system bus drivers and receivers are used, 8080 system data and address bits are 0 = true.			
Address Strobe	None	NADS = 0 to set memory address latches	VMA = 1 (concurrent with)	NADS = 0
Memory Read Strobe	MRDC = 0 to read data	IDS = 1 to input data	R/W = 1 to read data	NRDS = 0 to read data
Maximum Clock Rate	2MHz	2MHz	1MHz	1MHz

Since μC systems differ somewhat from one another, it is worth our effort to look at the hardware and software details and the system timing requirements of several of them when considering a DAU interface. From this consideration we can establish the desired function and characteristics of the ADCs, DACs, address decoders, control components, and μC interface signals. The following exercises include interfacing parallel conversion DAUs of 8- and 12 bits to the Intel 8080, the National PACE, and the Motorola 6800 microcomputer systems. Interface to other systems such as National's SC/MP will be similar. All request, control, and answer signals are considered along with the required signal polarities and timing relationships. Table 2 summarizes the important characteristics of these three systems.

8080 Interface

The 16-channel, 8-bit parallel-conversion DAU shown in Figure 6 will interface with an 8080 μC system without a wait period in the memory-read cycle. This system can be built with existing components for about $10 per channel. It is a minimal system, capable of driving only a lightly loaded data bus, as the MM5357 ADCs can drive but a single TTL load. When heavier loads must be driven, two quad TRI-STATE output buffers will be needed. The address decoding uses a 4-line to 16-line decoder which selects the addressed channel from the four least significant (LSB) of address bits. A 6-bit address comparator compares the six most significant (MSB) address bits with a code hard-wired into the code-select-header. The comparator output gates the 4:16 decoder only if the proper memory page (1 of 64) is addressed. The comparator output, gated by the memory read command $\overline{\text{MRDC}}$, inhibits the clock to prevent data change in the output latches during the data access period. Concurrence of the correct address and $\overline{\text{MRDC}}$ also returns a data-ready acknowledgement to the μC via the TRI-STATE output of a buffer. No other logic is required; however, inverters are necessary in the ADC enable lines due to a sense mismatch in the 4:16 decoder output and the ADC enable inputs. The system is truly as uncomplicated as indicated in Figure 2.

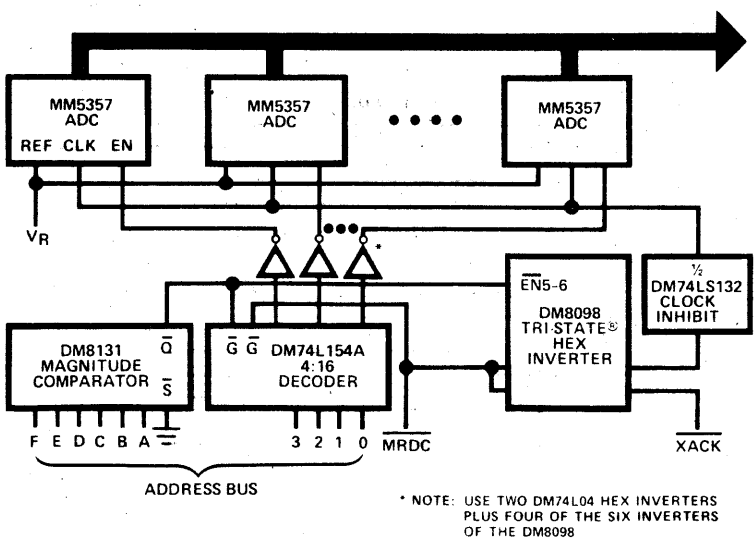


FIGURE 6. 16-Ch, 8-Bit Parallel-Conversion DAU for 8080

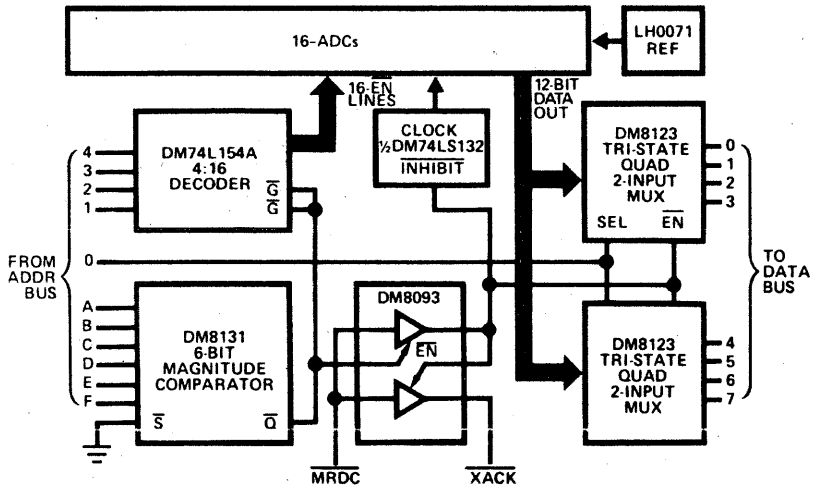


FIGURE 7. 16-Ch, 12-Bit Parallel-Conversion DAU for 8080

As 12-bit data is likely of greater interest in the market, the remainder of the discussion will consider the logic necessary to handle 12-bit data. Accordingly, Figure 7 shows a 16-channel, 12-bit parallel-conversion DAU for the 8080. No part number designation appears on the ADCs because they are hypothetical units possessing the characteristics considered desirable in this application. The converters contain the DAC switches, ladder network, comparator, up/down counter (for tracking conversion), control logic, and TRI-STATE buffered outputs. They operate continuously with the output data buffer updated at the end of each conversion. Such a converter containing CMOS logic could settle in less than 1-4 μs (after an initial but longer acquisition period) without being costly to construct, and would thus provide 12-bit accuracy to ±½ LSB at a data bandwidth of 10-20 Hz. A single external buffered reference could suffice for all converter channels. An external gated clock could drive all converters. Address decoding is the same as outlined for the 8-bit system. The LSB address bit is used to select byte 1 or byte 2 of the 12-bit output data word by means of the two DM8123 quad, TRI-STATE, 2-input multiplexers. Address bits 1-4 are decoded into 1-of-16 select bits to enable the TRI-STATE output of the selected ADC. Since the 1-of-16 output select of the DM75L154A decoder is 0 true, it is desirable that the ADC enable input be 0 true. Otherwise, 16 inverters would be required. The control timing may be considered in reference to the 8080 timing requirements shown in Figure 8.

The DM8131 address comparator provides an output to gate the 4:16 decoder and to enable the DM8093 quad TRI-STATE line driver. This occurs (+30 ns) only if the address is valid for this data card. If the address is valid, the 4:16 decoder accepts the address and the DM8093 is set to accept the MRDC command at inputs 5 and 6 (+250 ns). The decoder output to the ADC enable lines is available (+180 ns), and valid data is available from the selected ADC (+330 ns). As the data card must return a data ready signal (+440 ns) to prevent extending the memory access cycle, the DM8093 transmits the $\overline{\text{MRDC}}$

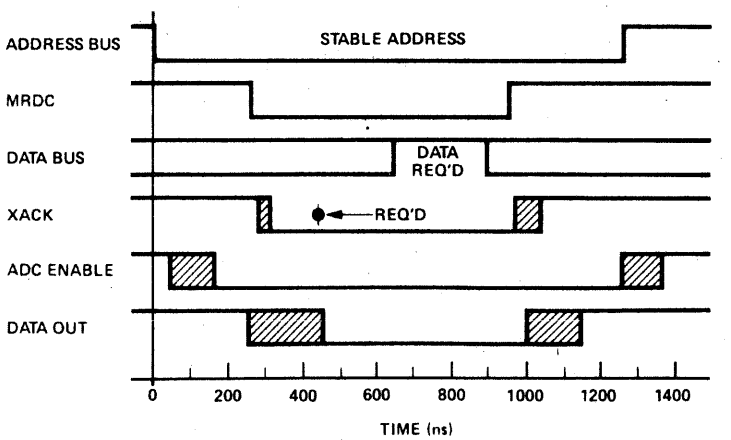


FIGURE 8. Timing and Control for 8080

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back out to the μC on the XACK line (+300ns) in advance of the time required. A 0 is placed on the XACK line for the duration of the MRDC command. The MRDC signal also enables the output multiplexer enable lines (+300ns) via the DM8093. This signal also interrupts the clock drive to the ADCs to prevent a change in data output during the remainder of the memory read cycle. A desirable built-in design feature of the ADC for this application might be a clock inhibit or data transfer inhibit operating from the $\overline{EN}$ input. Valid data is present on the data bus (+460ns) at least 200ns before it is required. Valid data remains stable until the end of the MRDC command when XACK and data output lines return to their normal high-impedance states.

Data is placed on the data bus in two 8-bit bytes as controlled by the LSB address code. A 0 selects the 8 LSB data, and a 1 selects the MSB data. Two consecutive memory addresses will then read the entire data word in two bytes. As there are only 12 data bits, zeros are placed on the remaining data lines. For 2s complement binary data coding of ± input analog signals, the 12th bit would be inverted and extended to the remaining data lines so that signals would appear as valid data to the microprocessor.

Total address decode, control, clock, and output drive logic circuitry is contained in six DIP circuits (only one of 24 pins). To this must be added a code-select header, a reference, and 16 converters. Total power required is 4.2 watts for 16 channels of 12-bit data from ±5V analog signals of 10Hz bandwidth (see Table 3). Low Power TTL output drive capability would reduce power drain by 370mW. Total cost of parts (assuming a future price of $25/ADC) would run to about $26 per channel (see Table 4).

Table 3. Power Required, 16-Channel, 12-Bit

		P_D (mW)		
		8080	6800	PACE
16 –	ADC		3200	
1 – LH0071	Reference		45	
1 – DM74LS132	4 x 2-Input NAND Schmidt		60	
1 – DM74L154A	4:16 Decoder		24	
1 – DM8131	6-Bit Comparator		250	
1 – DM8093	4 x Buffer	170		
or 1 – DM8099	6 x NAND Buffer		175	
or 3 – DM8097	6 x Buffer			975
2 – DM8123	4 x 2-Input MUX	400	400	
or 1 – DM86L13	4 x D-Latch			30
		4199	4154	4584

Table 4. Cost of Components, 16-Channel, 12-Bit

		$ (100s)		
		8080	6800	PACE
16 –	ADC		400.00	
1 – LH0071	Reference		5.00	
1 – DM74LS132	4 x 2-Input NAND Schmidt		2.00	
1 – DM74L154A	4:16 Decoder		2.46	
1 – DM8131	6-Bit Comparator		2.56	
1 – DM8098	6 x Inverter	1.65		
or 1 – DM8099	6 x NAND Buffer		1.70	
or 3 – DM8097	6 x Buffer			5.55
2 – DM8123	4 x 2-Input MUX	2.56	2.56	
or 1 – DM86L13	4 x D-Latch			1.28
		416.23	416.28	418.85
			≈ $26/Channel	

6800 Interface

For other μC systems, the logic will change slightly. Figure 9 shows the logic section of the DAU of Figure 7 modified as necessary to interface with the 6800 μC. The 6800 timing and control signals are shown in Figure 10. With the 6800, the address information, the valid memory address VMA signal, and the read/write W/R signal all come up approximately simultaneously and remain for about one clock period of 1μs (min.). The data need not appear on the data bus until 100ns thereafter. The valid address decoding is accomplished by ANDing the VMA and R/W signals together in a TRI-STATE 2-input AND gate. When enabled by the comparator output, this gate returns a READY signal to the μC and enables the output multiplexers. The appropriate data byte is selected by the LSB address bit as with the 8080 system. The necessary 10ns data hold time is provided by the ADC and output multiplexer disable delays. The remainder of the DAU is identical to that of Figure 7. Cost and power required are also similar to those of the 8080 system interface.

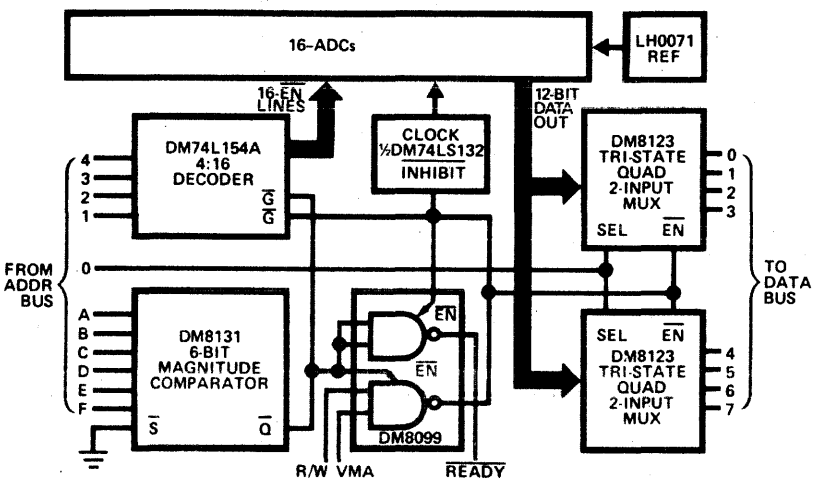


FIGURE 9. 16-Ch, 12-Bit Parallel-Conversion DAU for 6800

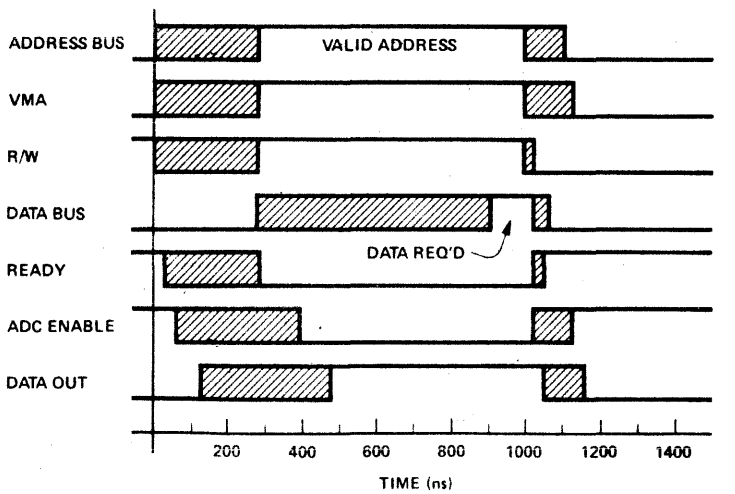


FIGURE 10. Timing and Control for 6800

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PACE Interface

Figure 11 shows the logic section of the DAU of Figure 7 modified to interface with a PACE μC. The PACE timing is shown in Figure 12. Since the PACE μC has but a single address/data bus, address latches are required for address decoding. The DM8131 address comparator contains output latches, but the DM74L154A 4:16 decoder does not, so a quad latch is inserted ahead of the 4:16 decoder. The latches all set on the rising edge of the NADS signal provided by PACE during the time that address information is on the bus, and drop out on the next NADS signal. Comparator output applied to gate the 4:16 decoder provides an enable ADC signal lasting until the falling edge of the next NADS pulse. The IDS signal ANDed with the comparator output enables the TRI-STATE output buffers and inhibits the clock. An additional MSB inverter would be needed for ± analog signals in order to provide the 2s complement code. Total address decode, control, clock, and output drive circuitry is contained in seven DIP packages, one more than required for the 8080 system interface. Total power and cost are comparable to those given for the 8080 system interface.

ADC CHARACTERISTICS

The ADC for use on a parallel-conversion DAU must contain TRI-STATE output data latches. Otherwise it may be conventional. The MM5357 was designed for direct connection to a data bus, therefore it contains the necessary output latches. At this writing there are other ADCs with the TRI-STATE output latches appearing on the market, and more can be expected. The MM5357 is nearly ideal for use in an 8-bit parallel-conversion DAU. It would be even more suitable to this use if it were a tracking converter, and the polarity of its enable input and of its data output were of opposite polarity. The data polarity is of lesser importance as the bus drivers probably needed may as well be inverting as non-inverting except for common usage. The enable polarity should match the decoder output to obviate the need for 16 inverters (3 logic packages, though of little cost). See the later discussion of ADC hardware for additional thoughts on this subject.

This parallel-conversion data system has data bandwidth limited to about 10 Hz for 8-bit SAR converters, but may be increased to 150-300 Hz with 8-bit tracking

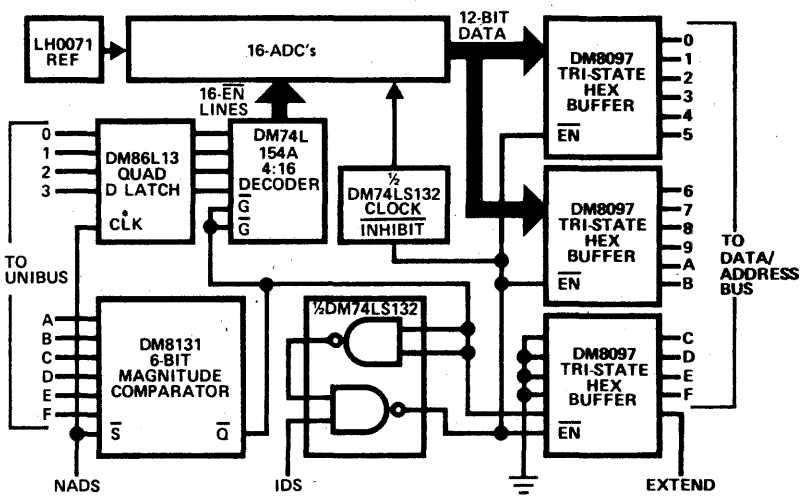


FIGURE 11. 16-Ch, 12-Bit Parallel-Conversion DAU for PACE

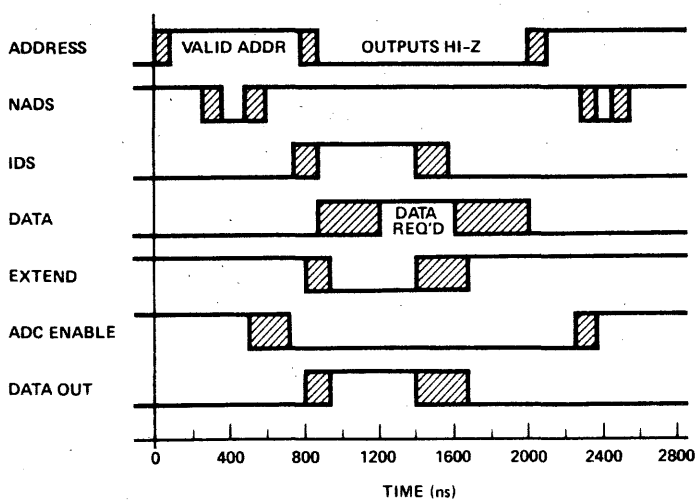


FIGURE 12. Timing and Control for PACE

converters. 12-bit data bandwidth will be 1/16 that of the 8-bit systems. On the other hand, no S&H module is required. Data rates could be considerably increased if S&H modules were added to each channel; however, costs per channel would more than double. For use with S&H modules, SAR logic converters would be faster than tracking types, allowing data bandwidths of over 600 Hz/channel for 12-bit data.

MULTIPLEXED DATA ACQUISITION UNIT WITH MEMORY

A multiplexed data acquisition system containing memory is probably the most cost-effective way of providing an immediate data-access interface to processors. The processor may address the peripheral data-acquisition unit to obtain immediate data without entering a wait mode, just as if it were accessing main memory. Latest valid data is always present within the DAU memory which is updated at a rate determined by the channel multiplexer rate and ADC conversion speed. There is no need to write subroutines into processor software or firmware to address and request data from the peripheral, resume its assigned processing task while watching for a flag set by the peripheral indicating that data is ready, and returning to accept data from the peripheral.

The multiplexed DAU with memory shown in Figure 3 takes care of routinely updating its memory by sequentially sampling each data channel, digitizing the channel signals, and writing data into its self-contained memory. When the DAU is interrogated, the sequential process is momentarily interrupted, the RAMs are addressed by the processor, and data is read out to the data bus. The memory can be three each DM8599 16x4-bit RAMs. These have TRI-STATE outputs, so can connect directly to the data bus. Note that the RAM inverts the data bits from the ADC. The RAMs are available in low-power TTL to drive a lightly loaded data bus, or they are available in Schottky versions for driving higher speed systems. In fact, almost the entire logic system could be realized in Schottky circuits, which should allow interfacing even the new fast bipolar μCs without a wait cycle.

The MUX sequencing circuits are shown in Figure 13. When the μC is not accessing memory on the DAU, the 16 data channels are scanned in continuous sequence.

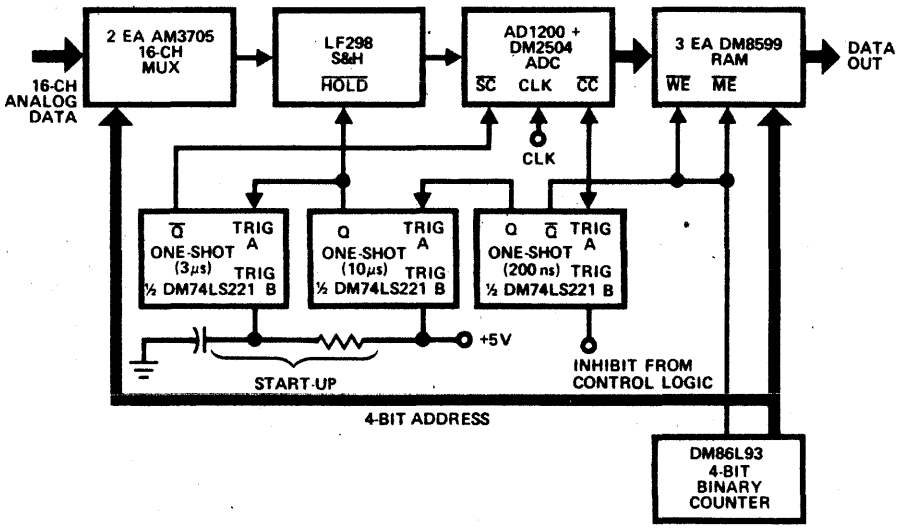


FIGURE 13. Sequencing Logic with OS

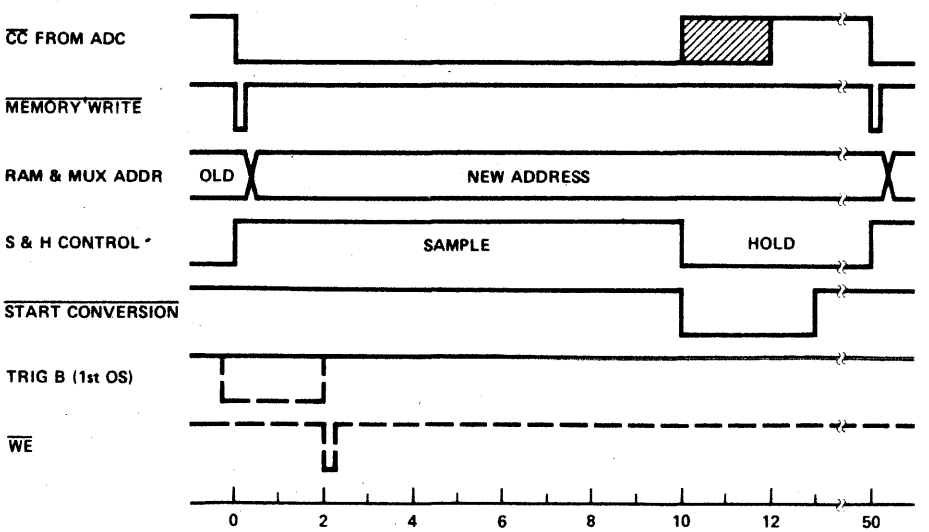


FIGURE 14. Timing for One-Shot Sequencing

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Data on each channel is sampled and held in the S&H module while the ADC converts the analog data to digital. At the completion of conversion, the digital output of the ADC is written into the RAMs before the multiplexer selects the next channel. The timing and sequencing of channels is accomplished with a 4-bit binary (÷ 16) counter and three one-shot pulse generators. Where one-shots are undesirable, an alternate approach using shift register timing could provide the same function. A valid address output from the address comparator switches the RAM address input from the ÷16 counter to the address bus input, thereby addressing the RAM to the desired channel for data readout. If the data conversion sequence is in the memory write condition, the gate applied to WE prevents switching the MUX to the address bus or returning an XACK signal until the memory has been loaded. Thereupon, the sequence is interrupted as outlined above. The interruption of the sequence lasts for about 1300ns (8080 system) while the address is valid.

The sequential data conversion cycle is shown in the timing signals of Figure 14. The conversion-complete $\overline{CC}$ output of the ADC triggers a one-shot to generate a 200ns memory write pulse. The trailing edge of this pulse advances the address ÷ 16 counter to the next channel and triggers a second one-shot to produce a 10μs sample period. At the completion of the sample period, the S&H goes into hold mode and a third one-shot generates a 3μs start conversion $\overline{SC}$ pulse. When the DAU is in the command read mode, a 0 appears at B trigger input to the first one-shot. If a $\overline{CC}$ signal occurs during the time the 0 is present on the B input, the one-shot will not be triggered until the B input returns to a 1.

An alternate sequencing circuit without one-shot circuits is shown in Figure 15 with timing relationships in Figure 16. It makes use of a shift register and exclusive-OR gates to generate the gates needed to write into memory, sample and hold, and start conversion. The ADC clock is generated at twice the desired clock frequency and divided by 2 in a D flip-flop. In this manner, the minimum gate width is 1/4 of the ADC clock period (620ns in this example). The $\overline{CC}$ signal is clocked into a D flip-flop with a delay of 620ns. The delayed output clears the shift register (SR) and is clocked into the SR after an additional 620ns delay. An exclusive-OR of the SR input and Q1 output generates a 620ns gate to write data into the RAMs. The trailing edge of this $\overline{WE}$ gate clocks the ÷ 16 counter to advance the MUX and RAM address to the next channel. Exclusive-ORing of SR Q1 and Q7 produces an 8.75μs sample gate. (If the acquisition and settling time of the S&H is greater than 8.75μs, additional circuit complexity is required.) Exclusive-ORing of Q7 and Q8 produces a synchronized 1.25μs gate to start the ADC. This circuit may not be the most versatile or elegant for the purpose. For those applications with longer S&H acquisition times or other requirements, some alternate circuit may be designed if that of Figure 15 is unacceptable.

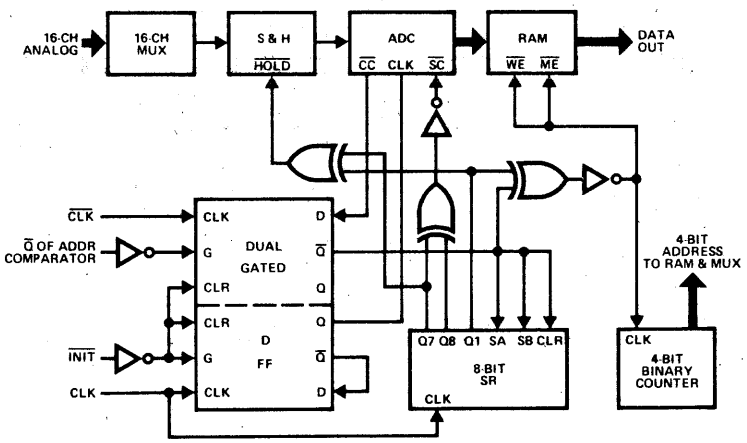


FIGURE 15. Sequencing Logic with SR

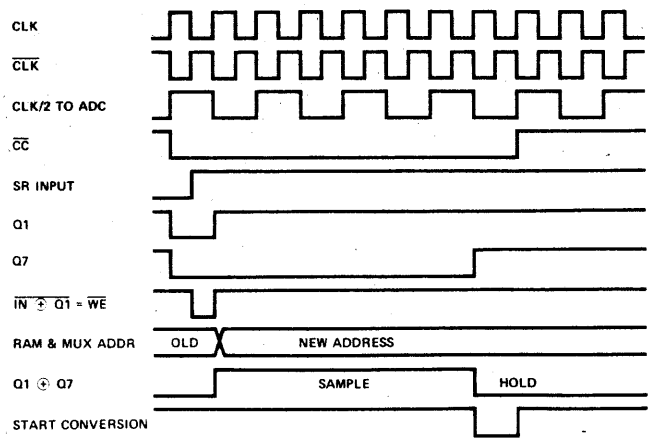


FIGURE 16. Timing for S-R Sequencing

The μ-computer interfaces shown in Figures 17 and 18 are similar to that of Figure 5. The PACE interface is seen to be slightly less complex than that of Figure 17 for 8-bit data-bus machines. A single DAU card with plug-in or strap options could be built to interface any of the three μCs considered. Such a universal circuit is shown in Figure 19. This circuit also includes an option to provide binary output for unipolar analog signals or complementary binary output for ± signals. In the case of binary output, the 13-16th data bits are set to 0. In the case of complementary binary, the sign bit is extended to the 13-16th data bits for valid recognition by the μC.

The total dissipation is 3.5 watts and cost is $11 per channel as shown in Table 5. Both are only slightly greater than those for the conventional DAU.

The ADC desired for this application is similar to the conventional ADC except that the ADC data output should be complementary to compensate for the data inversion within the RAMs. The AD1210 or AD1200 are thus ideal choices for an ADC in the multiplexed DAU with memory.

CONVERTER CHARACTERISTICS

Each approach to the DAU requires different characteristics of the ADC. Table 6 summarizes the requirements for each of the three DAU types. The sequential or addressed DAU types require similar ADCs. If the conventional addressed DAU must utilize bus drivers, the desired ADC characteristics are identical to those for the sequential DAU with memory. Only the parallel-conversion DAU is seen to require buffered TRI-STATE output latches.

By far the most important characteristic of an ADC for use in a parallel-conversion DAU is that it have buffered TRI-STATE output latches. It is desirable that it also have the other characteristics checked in Table 6. Items 1 and 2 are by far the most important of the desired characteristics. The need for item 1 has been discussed. TTL compatible control and data signals are desirable so that TTL-MOS and MOS-TTL interface buffers are not required between the ADC and the rest of the system. Dual output strobing makes it possible to wire-OR interface directly to an 8-bit data bus or to use only an 8-line buffer without the need for the output multi-

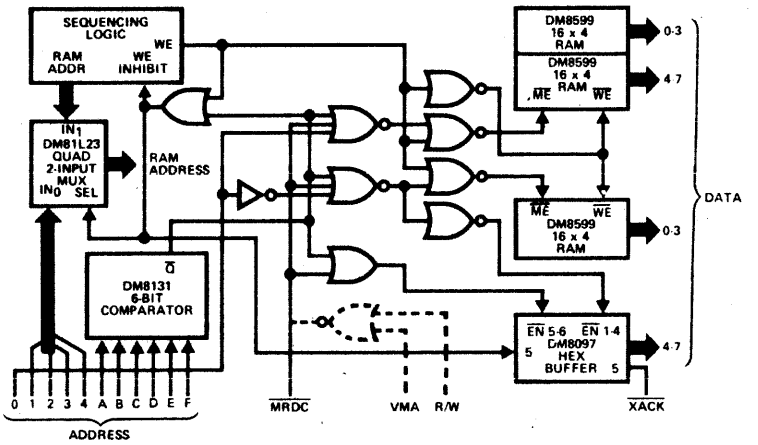


FIGURE 17. Address Comparator and Control for 8080 (6800)

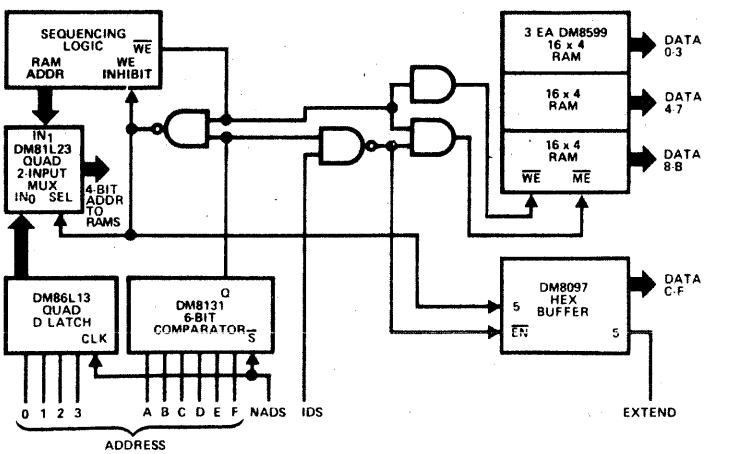


FIGURE 18. Address Comparator & Control for PACE

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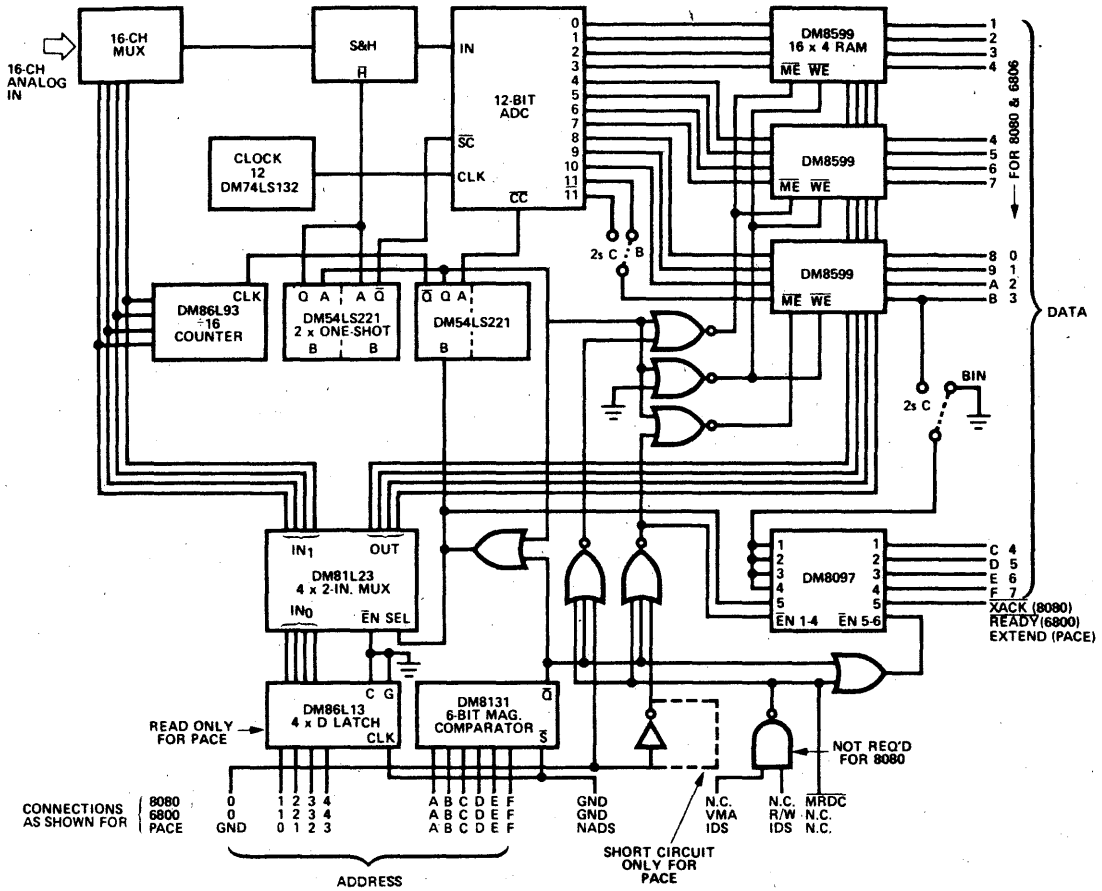


FIGURE 19. Multiplexed Immediate-Data-Access DAU

Table 5. Power & Cost, 16-Channel, 12-Bit Sequential with Memory

		P_D (mW)	$ (100s)
1 –	16-Channel MUX	300	19.55
1 –	S&H	500	74.50
1 –	ADC	600	40.00
1 – LH0070	Reference	45	5.00
3 – DM8599	256-Bit RAM	1200	15.36
1 – DM8097	6 x Buffer	325	1.65
1 – DM8131	6-Bit Comparator	250	2.56
1 – DM81L23	4 x 2-Input MUX	20	2.00
1 – DM74LS27	3 x 3-Input NOR	17	3.00
1 – DM7402	4 x 2-Input NOR	55	.35
1 – DM74L32	4 x 2-Input OR	12	.64
1 – DM86L93	÷16 Counter	25	2.11
2 – DM74LS221	2 x One-Shot	60	6.00
1 – DM74LS132	4 x NAND Schmidt	60	2.00
1 – DM86L13	4 x D-Latch	30	1.28
		3500	176.00
			$11/Channel

plexers shown in Figure 5 et. al., although a separate buffer is required in most systems. Tracking operation provides the higher speed useful in a conversion circuit without an S&H. Inhibiting data transfer to output data latches when the output is enabled prevents changing the output code while data is being read from the data bus. This function can be accomplished with an external gate, but could be convenient if handled within the ADC logic. Straight binary (not complemented) output is desired for all μC interfaces (except the 8080 when operating with Intel system bus drivers and receivers). As it may be necessary to add TRI-STATE line drivers to drive the data bus, data inversion can be handled by inverting buffers when required. The availability of both Q and $\overline{Q}$ outputs on the MSB simplifies data readout as binary or 2s complement without adding an external inverter. Table 6 has been arranged in the approximate order of preference for parallel-conversion DAU use; the preference will be different for multiplexed data.

The National MM5357 is the choice for an 8-bit ADC having buffered TRI-STATE output latches and TTL compatibility when converting ±5 or 0-5V analog inputs. If converting 0-10V inputs, it becomes 10V CMOS compatible. Several monolithic ADCs of 8 to 12 bits have been announced. These monolithic converters and future versions of them promise to bring converter prices down to a level which will make parallel-conversion economically feasible. Several hybrid converters have also been announced with attractive prices; however, it is the monolithics which promise the lowest ultimate cost. Features of several of these new products are compared in Table 7. Although only the MM5357 and the AD7550 are suitable in present form, their prices and characteristics show that the desired attributes are and will be possible at the needed prices.

The future ADC most suited for use in a parallel-conversion DAU might appear as in Figure 20. This

Table 6. Desired A/D Converter Characteristics

	Parallel Conversion	Sequential w/ Memory	Addressed w/o Memory
Buffered TRI-STATE Output Data Latches	x		?
TTL-Compatible Control & Data Signals	x	x	x
Dual Output-Enable (Bits 0-7 & Bits 8-11)	x		x
Counter Logic	UP/DN	SAR	SAR
Internal Comparator	x	x	x
Both Q & $\overline{Q}$ Outputs on MSB	x	x	x
Binary Output Polarity	Data*	$\overline{\text{Data}}$	Data*
Busy Output (TRI-STATE w/ Enable)	?		x
Internal Clock		x	x
Continuous Recycle when CC = SC	x		
Inhibit Data XFR to Latches when Enabled	x		

* Unimportant if Buss drivers used.

Table 7. Low-Cost Monolithic and Hybrid ADCs

	National MM5357	Analog Devices AD7570L	Teledyne 8702	National AD1210 (Hybrid)	Analog Devices AD7550
Number of Bits	8	10	12	12	13
Cost (in 100s)	$7.95	$69.00 (1-49)	$29.50	$24.95	$25.00
Conversion Method	Potentiometric	R-2R	Differential Charge Balancing	R-2R	Integrating
Logic Type	PMOS SAR	CMOS SAR	CMOS Integrating	CMOS SAR	CMOS Quad Slope
Conversion Time	25μs	20μs + Comp. Settling	20ms	130μs	40ms
Logic Interface at 5V Analog Sig. 0-10V	TTL CMOS	TTL TTL/CMOS	TTL TTL	TTL CMOS	TTL TTL/CMOS
External Circuits Required	Ref + Clock	Ref + Comparator	Ref	Ref + Clock	Ref
Output Buffered Latch?	Yes	No	Yes	No	Yes
TRI-STATE Output?	Yes	Yes	No	No	Yes
Separate Output Enables?	NA	Yes	Not Strobed	No	Yes
Output Code	Inverted	Normal	Normal	Inverted	2s Complement
Power Dissipation	170mW Dynamic	10mW Standby + Dynamic + Comparator	20mW Dynamic	140mW Dynamic	10mW Dynamic

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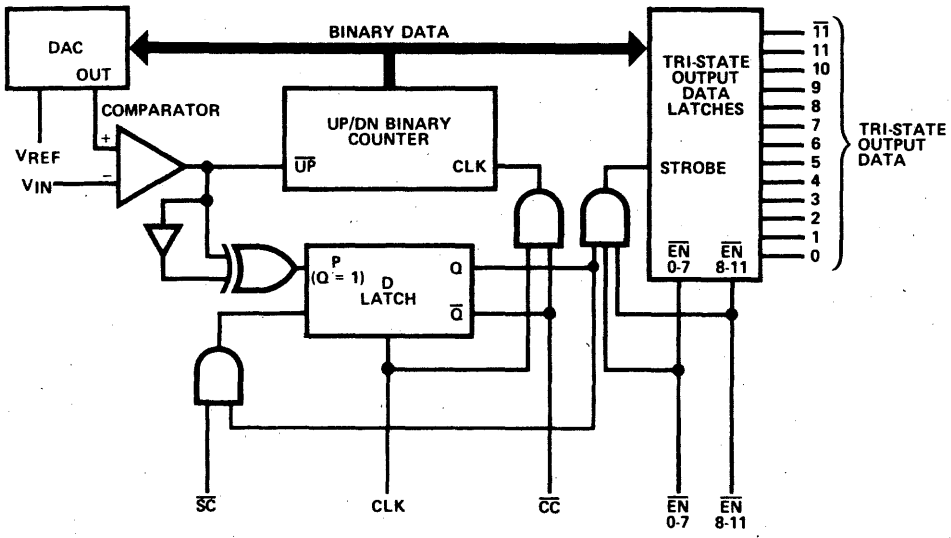


FIGURE 20. Tracking ADC for Parallel-Conversion DAU

design meets all the goals of Table 6. It could run at a clock rate of 0.25-1MHz (1-4μs conversion time) because it is a tracking converter, it contains TRI-STATE buffered output data latches, the separate high and low bit-enable lines allow two-byte operation of an 8-bit data bus, the output latches will not change state when the output is enabled, and the $\overline{CC}$ and $\overline{SC}$ terminals may be strapped for continuous conversion without missing a clock period. An 8- or 10-bit converter and possibly a 12-bit converter of this type could be built on a single chip without much difficulty. If not, a hybrid or two-chip design is practical. Where speed is not of importance, monolithic 10- or 12-bit converters can be built with integrating or voltage-to-frequency conversion techniques. The integrating technique possibly allows the greatest accuracy with the least circuitry, and is a prime contender for the application. As the integrating ADC utilizes both linear and digital circuits, it is normally of multi-chip design. However, as technology advances, it will become increasingly practical to produce the low-drift, low-offset amplifiers, integrators, and current sources required of a 12-bit ADC on a single reasonably small chip along with the necessary logic. A two-chip approach would likely be the choice today. We will certainly see some of these desired design features appearing on ADCs in the near future.

As far as ADCs and DACs are concerned, the entire makeup of their internal logic sections is different from that of conventional converters of today (except for the MM5357 and AD7550). Tables 6 and 8 outline the desired characteristics of ADCs and DACs for parallel-conversion and multiplexed systems. Figures 20 and 21 indicate the logic required. The ADC of Figure 20 is suitable for relatively high speed data acquisition without S&H circuits, while that of Figure 21 is suitable for slowly varying data only.

DATA DISTRIBUTION SYSTEMS

Until now, the discussion has centered entirely around the data acquisition end of the system. At first thought, the data distribution may seem almost trivial. However, there is still the address recognition and decoding plus the control functions. The conventional data distribution unit (DDU) has used a single DAC, a multi-channel analog demultiplexer, low-pass filters and possibly S&H

Table 8. Desired D/A Converter Characteristics

	Parallel Conversion	Multiplexed System
Hi-Z Digital Input Circuits	x	x
Strobed Data Input Latches	x	x
Dual Input Data Strobes (Bits 0-7 & Bits 8-11)	x	x
Optional Internal Inversion of MSB	x	x
Internal Output Amp & FB Resistors	x	?
Internal Reference	?	x

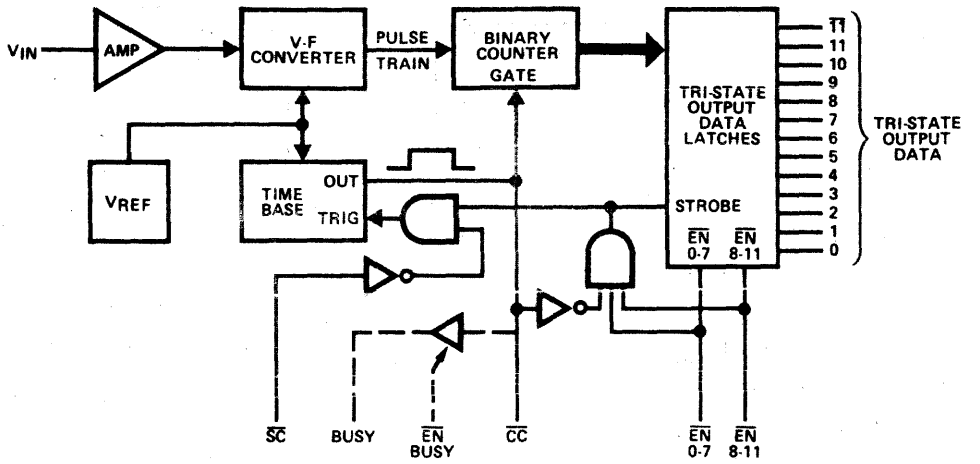


FIGURE 21. V-F ADC for Parallel-Conversion DAU

circuits on each channel reconverted to analog form. Such a system could benefit from a DAC with input data latches and separate (double-byte) input gating or strobing controls while a parallel-conversion DDU has even more need of these input characteristics.

The parallel-conversion DDU shown in Figure 22 would, if constructed with available DACs, require 12-bit input data latches ahead of each DAC. The characteristics desired of a DAC for this use are listed in Table 8. High impedance digital inputs prevent loading the data bus while a strobed input data latch allows entering data only in the addressed DAC and holding it until updated (thus performing the function of DAC and S&H). Separate input data strobes for low and high bits are used for the same reason as with the ADC, for alternate enabling on successive input data bytes. Figure 23 outlines the desired DAC for use in a parallel-conversion DDU.

The DDU address decoding and complexity is similar to that of the DAU. Input data strobing separated as 8 LSB and the remaining MSB is an advantage when used on 8-bit data bus systems. The cost per channel is essentially that of the DAC used. Likewise, for power dissipation. Practicality will be entirely dependent on ultimate cost of the converters. Advantages over a demultiplexed system are that only minimal output filters are required and that an output amplifier per channel is not required (already exists in each DAC).

CONCLUSION

Each type of DAU described exhibits unique advantages as indicated in the comparisons of Table 9.

Further reduction in the costs of monolithic converters will make the parallel-conversion type of DAU attractive where low-speed data is handled. For 8-bit data, this type of DAU is extremely attractive at this time because the DAU cost per channel is essentially that of an ADC which is as low as $8 in lots of 100.

It would seem that the multiplexed DAU with memory exhibits all of the advantages of the conventional random-addressed DAU plus all those of the parallel data conversion DAU except that the data in any specific channel may be older. Offsetting this single comparative disadvantage are significantly lower cost per channel, lower power requirements, and no requirement for special ADCs with buffered output latches. The multiplexed approach with memory is only slightly more complex or costly than a standard DAU, yet it brings the great advantage of high-speed immediate data access with significant cost savings over the parallel conversion technique.

Although the character of an ADC or DAC used in a parallel-conversion data system differs markedly from those used in the usual multiplexed data system, the processor interface requirements are similar or identical. The sense of μC bus control signals is of relatively minor importance so long as they are standardized among the several μC units available. Positive-true data and address signals are possibly a slight advantage over zero-true signals when TRI-STATE circuits are used. For the multiplexed system described, data inversion through the RAM would suggest the advantage of complementary binary output data from an ADC.

Conventional ADCs and DACs available today (except the MM5357 and AD7550) do not have the characteristics needed for parallel-conversion systems. However, this picture is changing as more units are designed for direct data bus interface. Fortunately, however, the multiplexed DAU with memory does not require the bus oriented type of ADC. There is at least one available DAC which includes the dual-strobed input data latches suggested for direct data bus interface; I would expect to see others appearing in future designs, both monolithic and hybrid.

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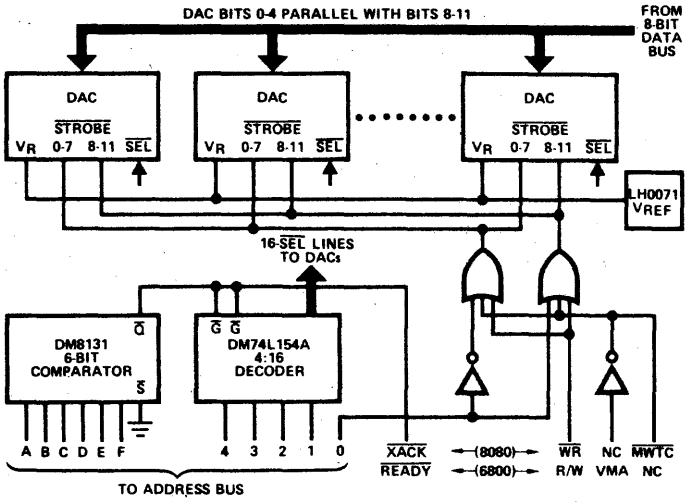


FIGURE 22. Parallel-Conversion DDU for 6800 or 8080

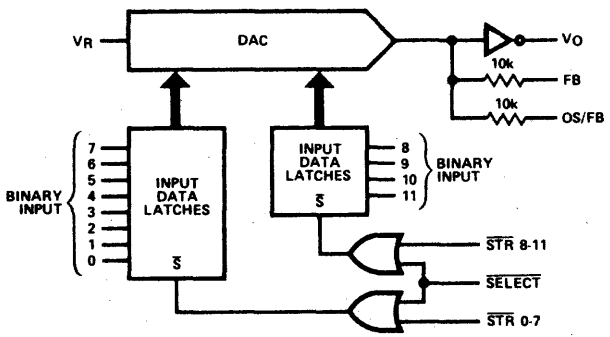


FIGURE 23. DAC for Parallel-Conversion DAU

Table 9. Comparison of Three Types of DAU

Features of DAU 16-Channel, 12-Bit	Conventional Random-Addressed	Parallel-Conversion Without S&H	Multiplexed With Memory
Approx. Component Cost (100s) (based on a $25 ADC)	$9.38	$26	$11
Approx. Power Dissipation	2.8W	4.3W	3.5W
Data Bandwidth/Channel $t_{conv} = 50\mu s$ t_{acq} (S&H) $= 10\mu s$	200Hz	10Hz (tracking: $t_{conv} = 4\mu s$)	200Hz
Data Access Time	$60\mu s$	$< 0.5\mu s$	$< 0.5\mu s$
Software	$60\mu s$ delay or subroutine and return on flag	as memory access	as memory access
Logic Interface Complexity	9 DIP	6 DIP	13 DIP
No. of IC Packages			
ADC Requirement		TRI-STATE buffered output data latches	

Manufactured under one or more of the following U.S. patents: 3083262, 3189758, 3231797, 3303356, 3317671, 3323071, 3381071, 3408542, 3421025, 3426423, 3440498, 3518750, 3519897, 3557431, 3560765, 3566218, 3571630, 3575609, 3579059, 3593069, 3597640, 3607469, 3617859, 3631312, 3633052, 3638131, 3648071, 3651565, 3693288.

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A Low Component Count Video Data Terminal Using the DP8350 CRT Controller and the INS8080 CPU

National Semiconductor
Application Note 199
Al Brilliott
August 1978

INTRODUCTION

The DP8350 is an I^2L – LS technology integrated circuit, designed to provide all control signals for a cathode ray tube (CRT) display system. This application note explains a system using the DP8350 and the INS8080 microprocessor. The design philosophy shows how the DP8350 interfaces to the INS8080, completing the function of a video data terminal with a minimum component count. After reading and understanding this application note the reader will realize the ease and flexibility of designing video terminals with the DP8350*. To thoroughly understand this application note the reader must be familiar with the DP8350 and the INS8080 microprocessor.

The video data terminal described is divided into the following sections, *(Figure 1).*

The DP8350 CRT controller (CRTC).

The 8080 μP system which includes ROM, RAM, interrupt instruction port, oscillator, and control support chips.

The character generator.

The communication element.

The keyboard and baud rate select ports.

THE CRTC

The DP8350 generates all the required control and timing signals for displaying video information on the video monitor. Here is a summary of the controller's functions:

Dot clock, control, and counter outputs for the character generator.

Bidirectional RAM address refresh counter for refreshing the video RAM and allowing microprocessor loading to the internal DP8350 registers.

Direct drive horizontal and vertical sync signal outputs.

Direct cursor address location output. The cursor is internally delayed or pipelined, allowing for the access time of video RAM and the character generator ROM, *(Figure 1).*

THE CPU

The microprocessor provides CRTC, operator, and external machine control for the system. When the CRT controller is not actively refreshing the video RAM, (i.e., during vertical retrace or blank scan lines), the microprocessor is enabled for system housekeeping, *(Figure 2).* This method of multiplexing the RAM with the CPU and the CRTC eliminates the need for line buffers.

*The DP8350 is equivalent to the INS8276

THE CHARACTER GENERATOR

The character generator consists of 3 elements: an address latch to hold the input address to the character ROM allowing for the access time of the ROM; the character ROM that stores the ASCII character in a form for parallel to serial conversion by the shift register; the shift register converts the character ROMs parallel output to serial form. The serial output from the shift register is the true video output, modulating the video monitors electron beam which writes characters on the screen. All of the 3 elements of the character generator are combined in the DM8678, *(Figure 3).* The DP8350 CRTC provides all the control signals for the DM8678.

THE COMMUNICATION ELEMENT

The INS8250 is the asynchronous communication element (ACE) for the data terminal. The ACE allows the CPU portion of the data terminal communication with peripherals or host computers at the correct baud rate, *(Figure 1).* The ACE is programmed by the CPU to send and receive serial data at the standard baud rates from 110 to 4800 baud. The ACE, in conjunction with the DS1488 and DS1489 line drivers and receivers, also provides full RS232C synchronous communication if higher baud rates are desired. System communication speed must always be considered to insure the baud rate does not exceed the time required for the CPU to process a data byte. Asynchronous communication at baud rates higher than 4800 are possible by adding a line buffer.

SYSTEM INITIALIZATION

Application of the terminal's power supply resets the microprocessor, the communication element, and the CRT controller. Resetting the ACE is necessary to clear the interrupt. Resetting the CRTC is not absolutely necessary since the microprocessor loads the cursor and top of page registers in the initialization routine.

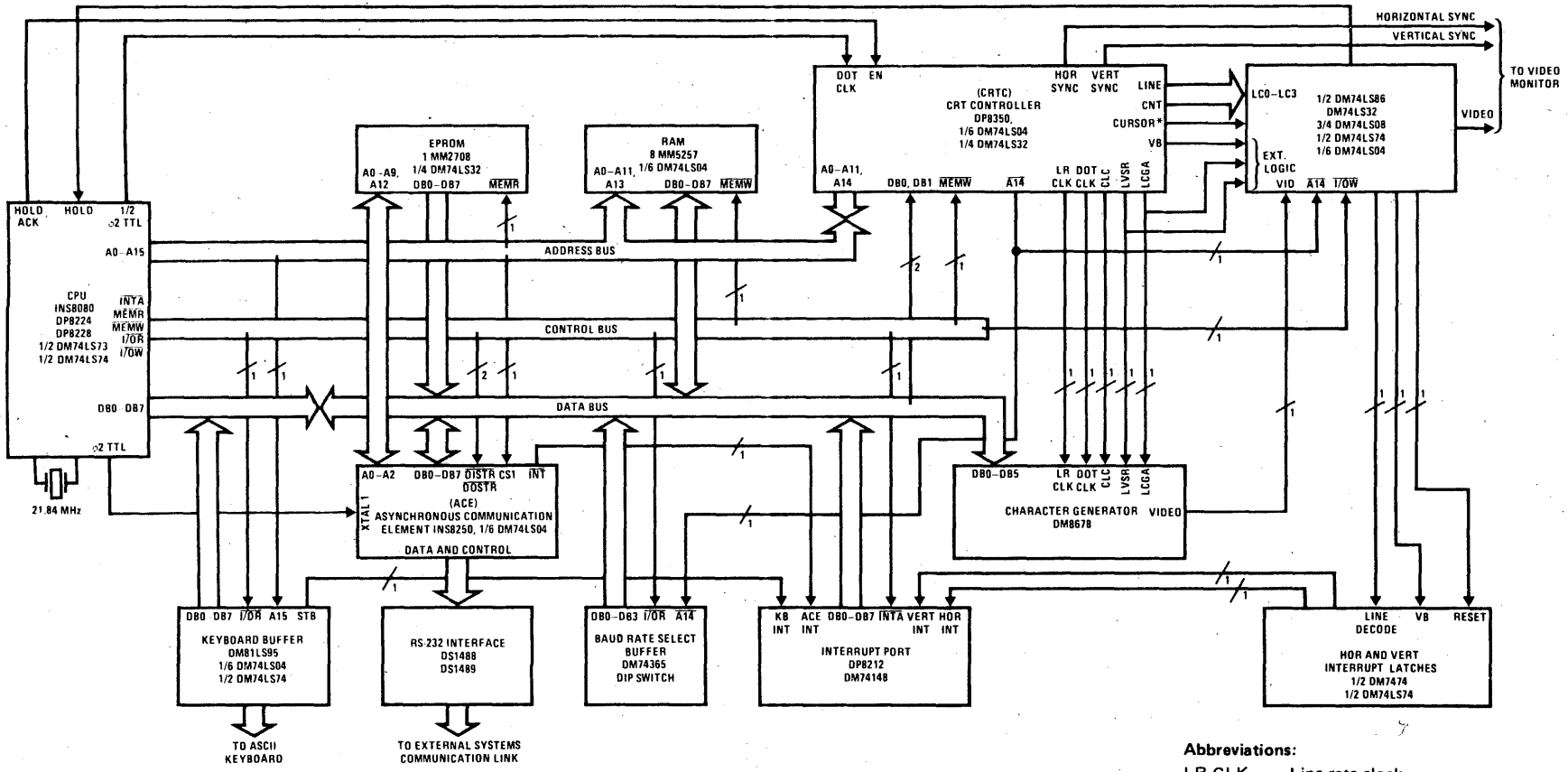
Following the reset all interrupts are disabled to avoid unwanted interrupts from the CRTC, ACE, or I/O ports. Refer to the initialization routine in the flowchart.

The stack pointer is loaded to the bottom of scratch pad RAM (3FFFH) for use as the register save pointer, *(Figure 4).*

The entire RAM is written with ASCII spaces generating a cleared screen. After completion of the screen clear loop the CPU writes 000H to the cursor and the top of page registers in the DP8350 CRTC. The routine homes the cursor to the upper left corner of the screen. The top of page register was loaded with 000H, therefore, the video RAM is refreshed by the CRTC from that starting address to the last address on the screen of video RAM (1920 characters).

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*The cursor is internally pipelined by the CRTC to allow for access time of the RAM and the character generator.

Abbreviations:

LR CLK	Line rate clock
CLC	Clear line counter
LVSR	Load video shift register
LCGA	Latch character generator address
Line CNT	Line counter
EN	Enable
VID	Video
KB INT	Keyboard interrupt
VB	Vertical blanking

FIGURE 1. Video Data Terminal Detailed Block Diagram

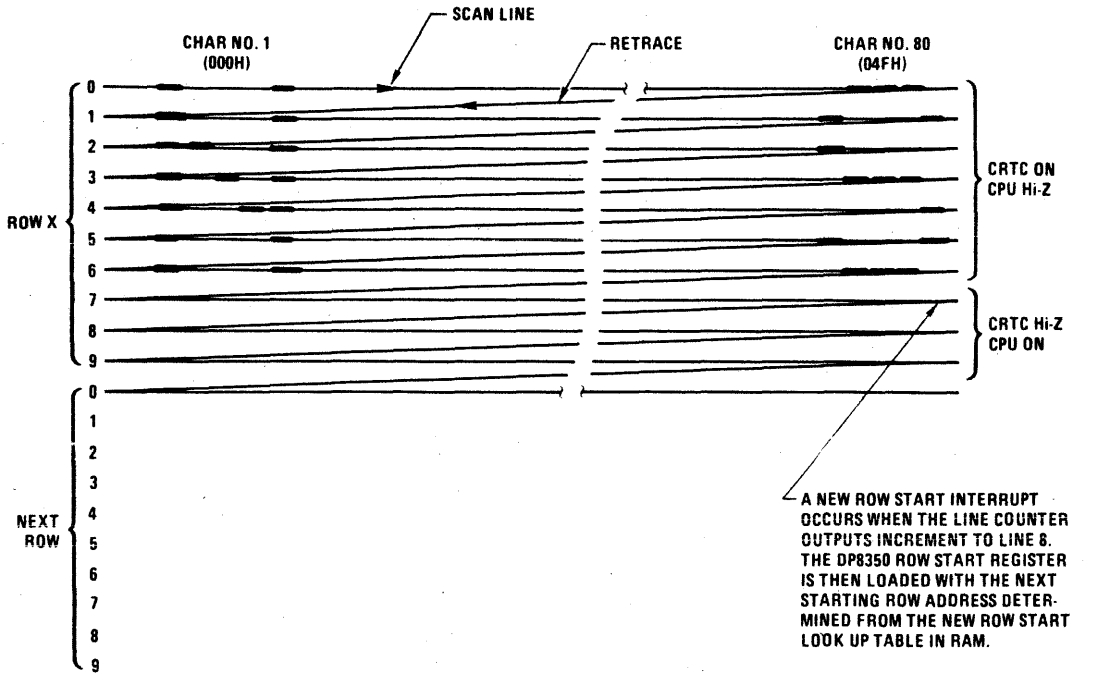


FIGURE 2. Row Start Interrupting and Multiplexing the INS8080 with the DP8350

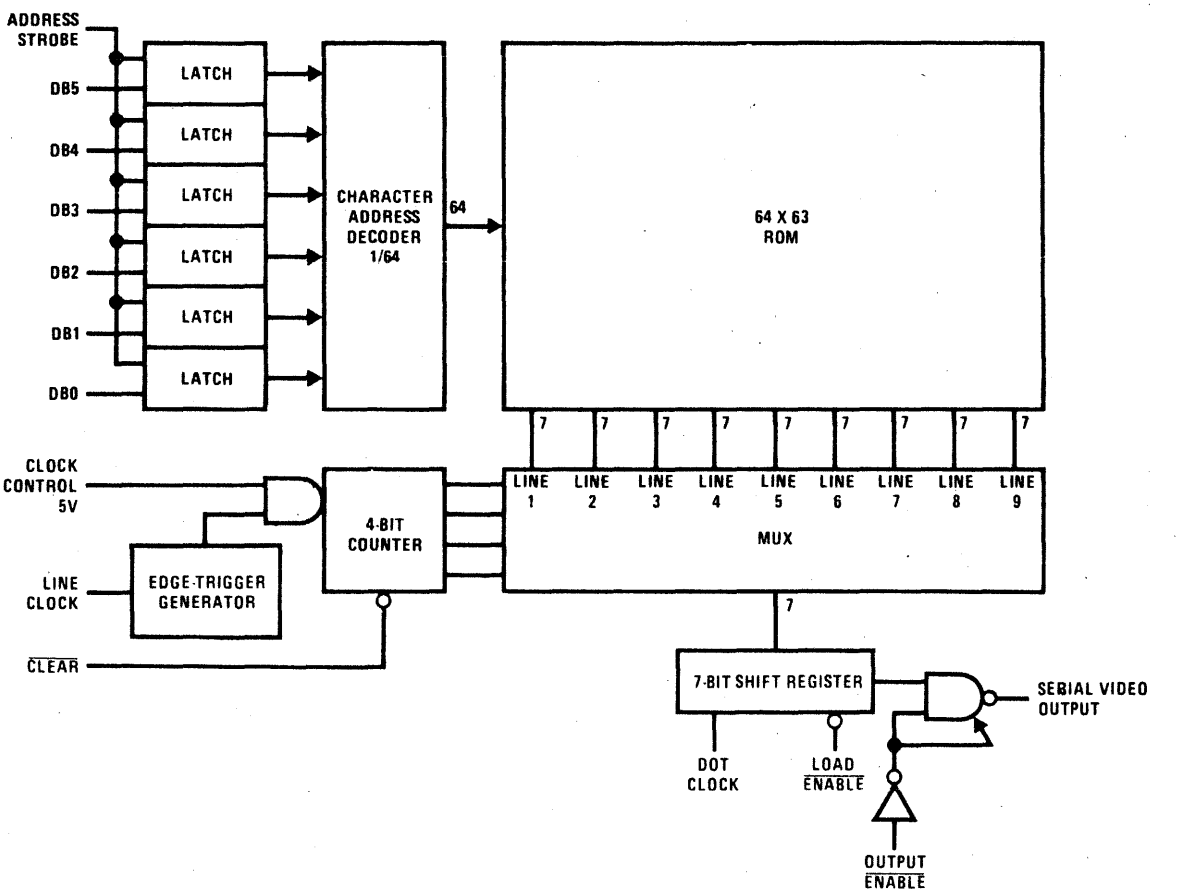


FIGURE 3. DM8678 Character Generator Block Diagram

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The CPU is ready to perform the communication element (ACE) load routine. First, the baud rate divisor for the ACE must be determined. The baud rate select switch is read providing a code which corresponds to the appropriate 16-bit divisor for the ACE. This divisor determines the baud rate at which the ACE will communicate. Any additional programming requirements needed for the ACE to communicate with host computer systems could also be done at this time. The software in this system does not contain any additional programming for the ACE. There are many programming modes related to the ACE. Details of these modes are beyond the scope of this application note.

The row start look-up table, *(Figure 5)*, is loaded up by a simple algorithm that loads and adds the data for referencing a row number to that row's starting address. The reference table, *(Figure 6)*, is initialized next by direct loading. This table provides the CPU with top of page, bottom of page, next row load, cursor row, and scratch row numbers for system housekeeping.

Finally, the new row start and vertical interrupt latches are cleared, *(Figure 7)*. The register pointers are loaded and the CPU is forced in a wait loop with interrupts enabled.

NON-SEQUENTIAL ADDRESSING

The data terminal described here was designed for non-sequential starting row addressing. In many systems sequential row addressing is used. If a character row consists of 10 scan lines the RAM is addressed 10 repetitive times from 000H through 04FH, *(Figure 2)*. The next row is refreshed in the same manner from 050H to 09FH. The starting row address is sequential 000H, 050H, 0A0H–EB0H for row numbers 0H, 1H, 2H,–2FH, respectively. Non-sequential row addressing would be equivalent to 050H, 000H, 0A0H–EB0H for row numbers 1H, 0H,–2FH, respectively, *(Figure 4)*.

In conjunction with the CPU, non-sequential row addressing is quite easily accomplished with the DP8350 since this is one of the features designed into the part. Accomplishing this task basically requires the following sequence of events. Assume the CRTC has finished writing a video row in the middle of the monitor's screen. This system has a 5 x 7 character font in a 7 x 10 field, *(Figure 2)*. At the completion of the last video scan line 7 the CRTC line counters continue to count the last 3 lines. Video is not present since the character is only 7 scan lines high. The blank scan lines are 7, 8, and 9 permitting the CRTC address outputs to be TRI-STATED®, allowing the CPU to run. When the line counter outputs increment to scan line 8 an interrupt signals the CPU. The interrupt occurring is the new row start interrupt. The interrupt routine fetches the next CRTC row number from the reference table *(Figure 6)*. This number is converted to the new starting row address, explained later, and loaded to the CRTC row start register. The CPU finishes the routine by clearing the interrupt, readying itself for the next new row start interrupt. The entire routine takes 1 scan line of time, approximately 64 μs. The CRTC continues to scan the video RAM from that new starting address on for the next 7 repetitive scan lines of the next row. Many advantages become apparent using the non-sequential addressing scheme. Scrolling up or down with the cursor always on the screen may be done faster and easier from a hardware/software standpoint. Exchanging one row with another row is fast since it is not necessary to rewrite the video RAM. Row swapping is useful for higher end terminals requiring row editing functions.

ADDRESS MAP

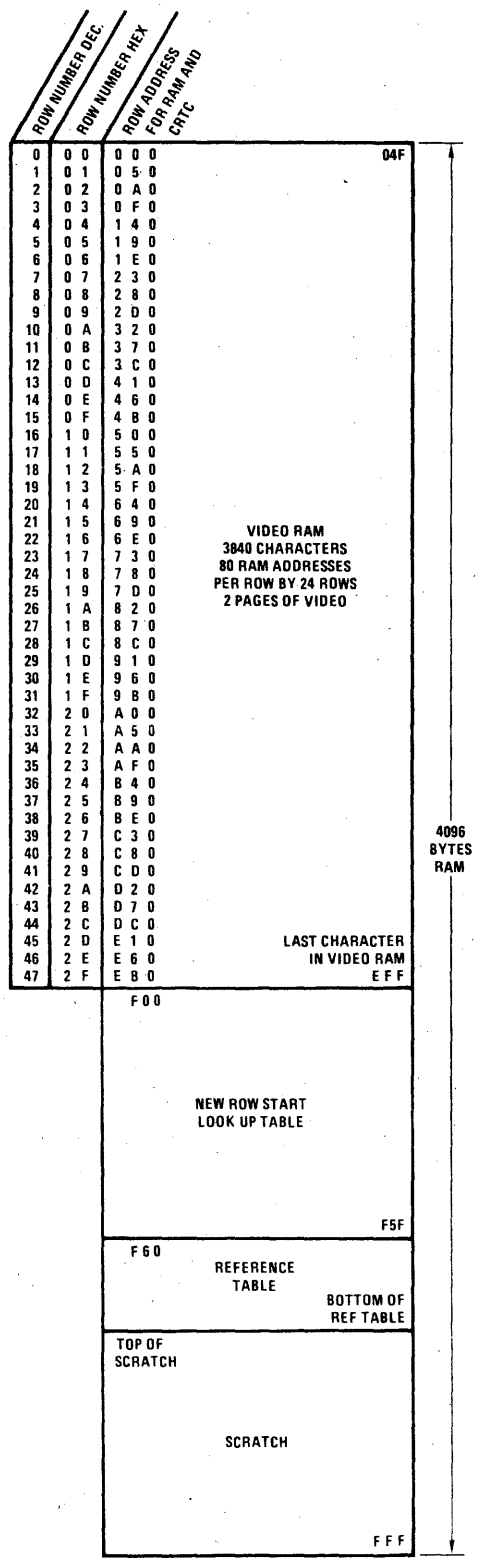


FIGURE 4. RAM Organization

MEMORY REFERENCE TABLES

Page 1

ROW NUMBER DEC	ROW NUMBER HEX	NRS HIGH ADDRESS	NRS HIGH ROW DATA	NRS LOW ADDRESS	NRS LOW ROW DATA
0	0 0	3 F 0 0	3 0	3 F 3 0	0 0
1	0 1	3 F 0 1	3 0	3 F 3 1	5 0
2	0 2	3 F 0 2	3 0	3 F 3 2	A 0
3	0 3	3 F 0 3	3 0	3 F 3 3	F 0
4	0 4	3 F 0 4	3 1	3 F 3 4	4 0
5	0 5	3 F 0 5	3 1	3 F 3 5	9 0
6	0 6	3 F 0 6	3 1	3 F 3 6	E 0
7	0 7	3 F 0 7	3 2	3 F 3 7	3 0
8	0 8	3 F 0 8	3 2	3 F 3 8	8 0
9	0 9	3 F 0 9	3 2	3 F 3 9	D 0
10	0 A	3 F 0 A	3 3	3 F 3 A	2 0
11	0 B	3 F 0 B	3 3	3 F 3 B	7 0
12	0 C	3 F 0 C	3 3	3 F 3 C	C 0
13	0 D	3 F 0 D	3 4	3 F 3 D	1 0
14	0 E	3 F 0 E	3 4	3 F 3 E	6 0
15	0 F	3 F 0 F	3 4	3 F 3 F	B 0
16	1 0	3 F 1 0	3 5	3 F 4 0	0 0
17	1 1	3 F 1 1	3 5	3 F 4 1	5 0
18	1 2	3 F 1 2	3 5	3 F 4 2	A 0
19	1 3	3 F 1 3	3 5	3 F 4 3	F 0
20	1 4	3 F 1 4	3 6	3 F 4 4	4 0
21	1 5	3 F 1 5	3 6	3 F 4 5	9 0
22	1 6	3 F 1 6	3 6	3 F 4 6	E 0
23	1 7	3 F 1 7	3 7	3 F 4 7	3 0

Page 2

ROW NUMBER DEC	ROW NUMBER HEX	NRS HIGH ADDRESS	NRS HIGH ROW DATA	NRS LOW ADDRESS	NRS LOW ROW DATA
24	1 8	3 F 1 8	3 7	3 F 4 8	8 0
25	1 9	3 F 1 9	3 7	3 F 4 9	D 0
26	1 A	3 F 1 A	3 8	3 F 4 A	2 0
27	1 B	3 F 1 B	3 8	3 F 4 B	7 0
28	1 C	3 F 1 C	3 8	3 F 4 C	C 0
29	1 D	3 F 1 D	3 9	3 F 4 D	1 0
30	1 E	3 F 1 E	3 9	3 F 4 E	6 0
31	1 F	3 F 1 F	3 9	3 F 4 F	B 0
32	2 0	3 F 2 0	3 A	3 F 5 0	0 0
33	2 1	3 F 2 1	3 A	3 F 5 1	5 0
34	2 2	3 F 2 2	3 A	3 F 5 2	A 0
35	2 3	3 F 2 3	3 A	3 F 5 3	F 0
36	2 4	3 F 2 4	3 B	3 F 5 4	4 0
37	2 5	3 F 2 5	3 B	3 F 5 5	9 0
38	2 6	3 F 2 6	3 B	3 F 5 6	E 0
39	2 7	3 F 2 7	3 C	3 F 5 7	3 0
40	2 8	3 F 2 8	3 C	3 F 5 8	8 0
41	2 9	3 F 2 9	3 C	3 F 5 9	D 0
42	2 A	3 F 2 A	3 D	3 F 5 A	2 0
43	2 B	3 F 2 B	3 D	3 F 5 B	7 0
44	2 C	3 F 2 C	3 D	3 F 5 C	C 0
45	2 D	3 F 2 D	3 E	3 F 5 D	1 0
46	2 E	3 F 2 E	3 E	3 F 5 E	6 0
47	2 F	3 F 2 F	3 E	3 F 5 F	B 0

FIGURE 5. New Row Start Look Up Table

FUNCTION	ADDRESS	DATA	INITIALIZED DATA
Last Row #	3F60	XY	17
8080 Row #	3F61	XY	00
First Row #	3F62	XY	00
Character #	3F63	XY	00
CRTC Row #	3F64	XY	00
Row Save #	3F65	XY	00
Temp. 1	3F66	XY	00
Temp. 2	3F67	XY	00

FIGURE 6. Reference Table

COMMAND		FUNCTION
OUT	40	Clear new row start and vertical interrupt latches
IN	80	Read keyboard
IN	40	Read baud rate select switch

FIGURE 7. Input/Output Space

DEVICE	ADDRESS*
ROM	0000 to 0FFF
RAM	3000 to 3FFF
CRTC	5000 to 5FFF
ACE	9000 to 9007

*Direct device selecting was used to minimize the system component count

FIGURE 8. CPU Addressing Space

ROW NUMBER DEC	ROW NUMBER HEX	NRS HIGH ADDRESS	NRS HIGH ROW DATA	NRS LOW ADDRESS	NRS LOW ROW DATA
32	2 0	3 F 2 0	3 A	3 F 5 0	0 0

Row Start Address for Row 20H.

3XXX Selects RAM.

5XXX Selects CRTC.

FIGURE 9. Example From the New Row Start Look Up Table

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ROW LOADING DETAILS

Obtaining the next starting row address for the CRT controller is accomplished by an addressing and adding scheme from the new row start look-up table. The same scheme is used to determine any needed address, given the row number.

Figure 9 shows a row number and address taken from the new row start look-up table.

The row number is loaded from the reference table in RAM to a register. The CPU determines the starting address from the row number and stores it in a 16-bit pointer register. The higher order 4 bits contain address for the RAM or the CRT controller, *(Figure 8)*.

Here are the details of how this is accomplished. Refer to the new row start interrupt in the software listing and *Figure 9.*

The CPU D-E registers are loaded to point to a row number in the reference table. The number is put in the accumulator and moved into the E register. The D-E register in this example now contains 3F20 which points to NRS HIGH ROW DATA (3A). The addressed data is moved to the accumulator and then to the H register. If it was desired to point to the CRTC then 20H would have been added to it first. The D-E register still contains 3F20H. To obtain the NRS LOW ROW DATA the E register is moved to the accumulator and 30H is added to it. Now the D-E register contains 3F50H and points to NRS LOW ROW DATA (00H). The data is loaded to the accumulator and then to the L register. The H-L registers contain 3A00H which is the starting row address for row number 20H. The method just described is used throughout the terminals program to move the cursor, load the top of page, and load the new starting row address in the CRTC.

VERTICAL INTERRUPT

The vertical interrupt occurs when the CRTC has completed refreshing a video page (1920 characters) of information. Vertical blanking identifies that condition and interrupts the CPU forcing it to the vertical interrupt routine. Refer to the vertical interrupt in the flow chart. The routine moves the first row number to the CRTC row number, updating it so the next new row start load occurs with the top of the page address or the first row of the video screen.

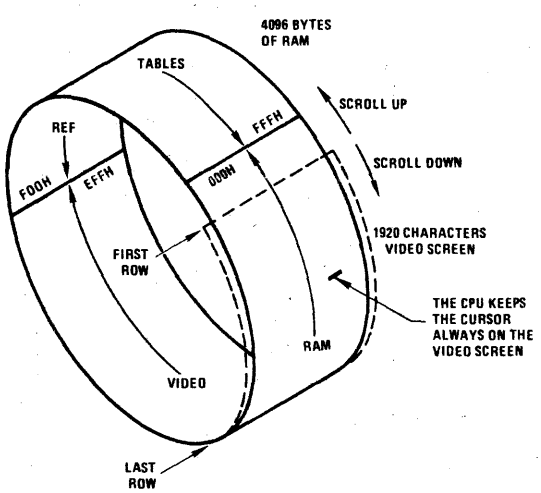
KEYBOARD INTERRUPT

The external keyboard requirements are ASCII outputs with a suitable strobe to interrupt the CPU for keyboard servicing. Refer to the keyboard interrupt in the flow chart. After the keyboard buffer is read the data byte is tested for a (CNTL E), new baud rate command. If the test fails the CPU writes the data byte to the ACE. Passing the test forces the CPU to read the baud switch and load the ACE with the new baud rate.

ACE INTERRUPT

As mentioned above, a data byte read from the keyboard that is not a baud rate command enters the accumulator. The CPU writes the data byte from the accumulator to the transmitter holding register in the ACE. The ACE proceeds to shift out the data byte, with the appropriate start and stop bits, serially from the (SOUT) output. The data is shifted to the serial input (SIN) of the ACE and loaded into the receiver holding register. When the register is full the ACE interrupts the CPU, initializating the ACE service routine. Refer to the ACE interrupt in the flow chart.

The CPU reads the receiver holding register in the ACE. Reading the ACE resets the interrupt. The data byte now resides in the accumulator. The CPU tests for a control or an escape function. The function is executed if test conditions are met. Refer to the keyboard interrupt routine in the software listing. The data byte is written to the video RAM at the cursor address which appears on the monitor screen. The cursor and character numbers are incremented as long as it is not at the end of a row. A character at the end of a row requires further testing to recognize the following situations. Is it the last row on the monitor's screen? Or is it on the maximum row of the video RAM? Essentially, the cursor is forced to stay visible on the video monitor's screen and video RAM is always kept out of scratch pad RAM, *(Figure 10).*



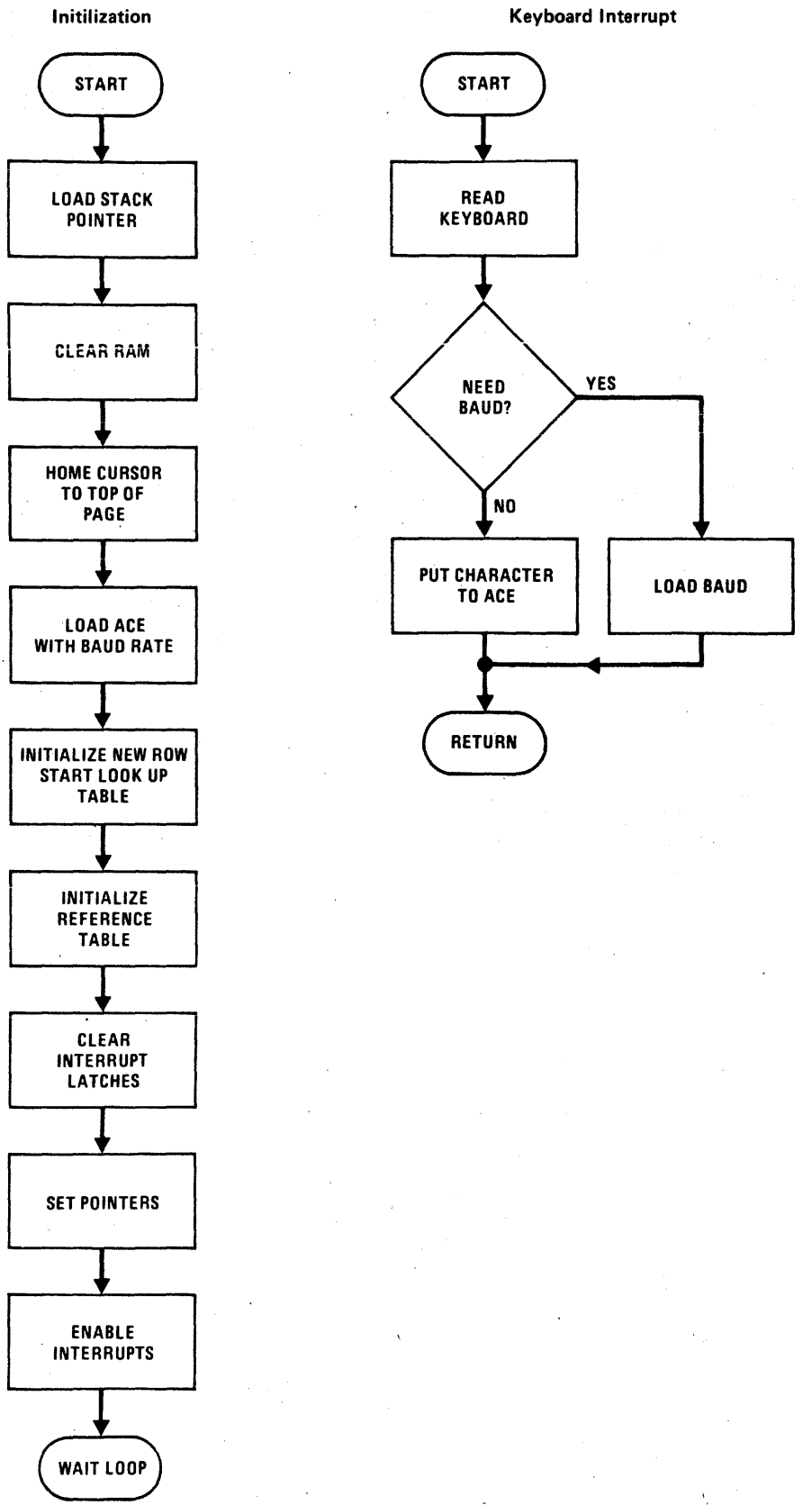
The video screen is allowed to scroll only through the video RAM (000H to EFFH). The CPU keeps the video screen within these bounds by loading the new row start register with that address range only (row 00H to 2FH).

FIGURE 10. Drum Analogy for the RAM

FULL/HALF DUPLEX OPERATION

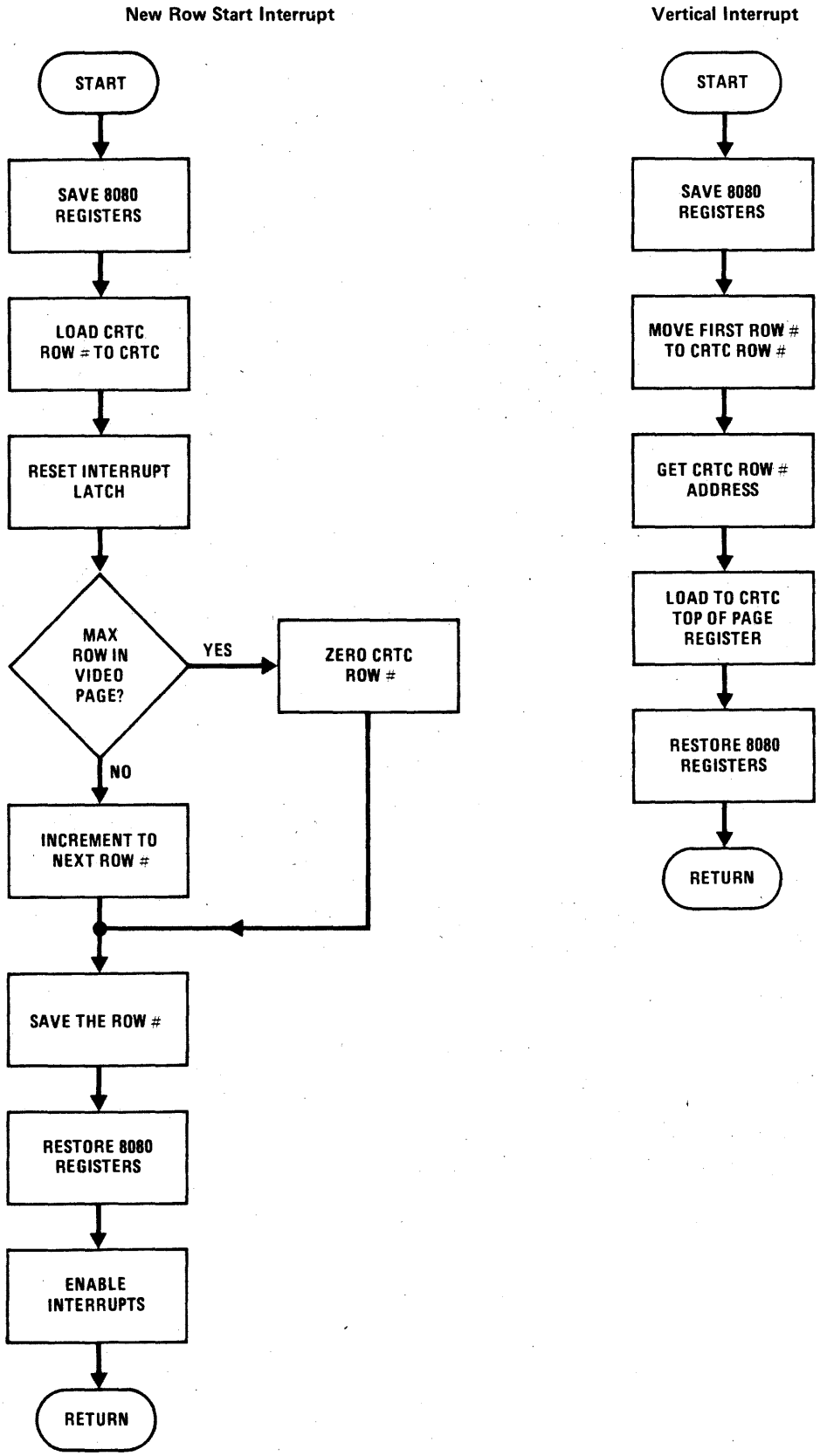
The data terminal and a host computer in the full duplex mode of operation would receive the serial information, process it, and send it back to the SIN input of ACE. Using the terminal in a stand-alone mode for testing, the serial out SOUT is tied to the serial in SIN of the ACE. In the half duplex mode a data byte is sent to the host computer at the same time it is sent to the terminal. When the data terminal is set up to communicate with a host computer the full duplex mode of operation is desirable.

DP8350/INS8080 VIDEO DATA TERMINAL BASIC SOFTWARE FLOW CHART



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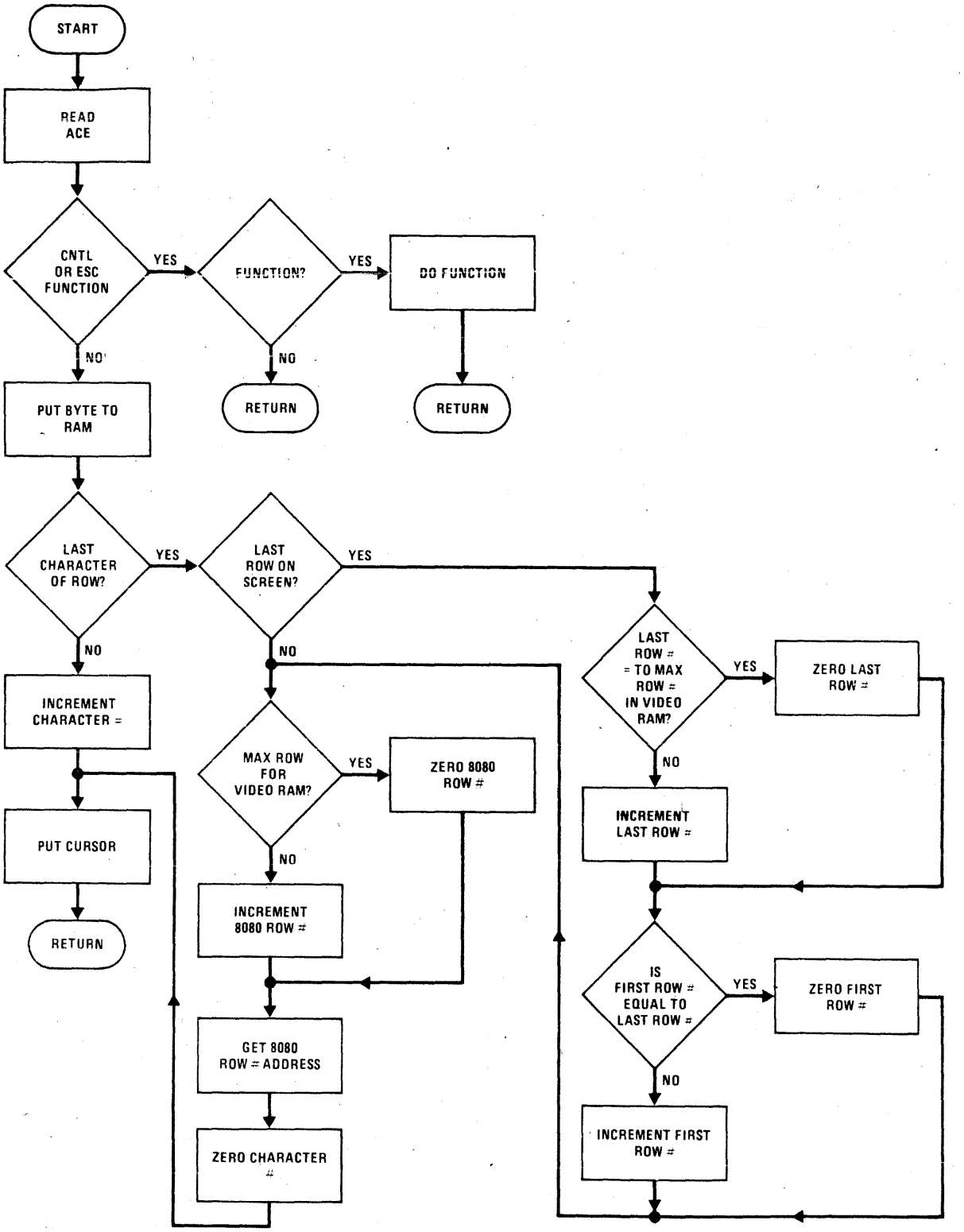
DP8350/INS8080 VIDEO DATA TERMINAL BASIC SOFTWARE FLOW CHART (Continued)



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DP8350/INS8080 VIDEO DATA TERMINAL BASIC SOFTWARE FLOW CHART (Continued)

ACE Interrupt



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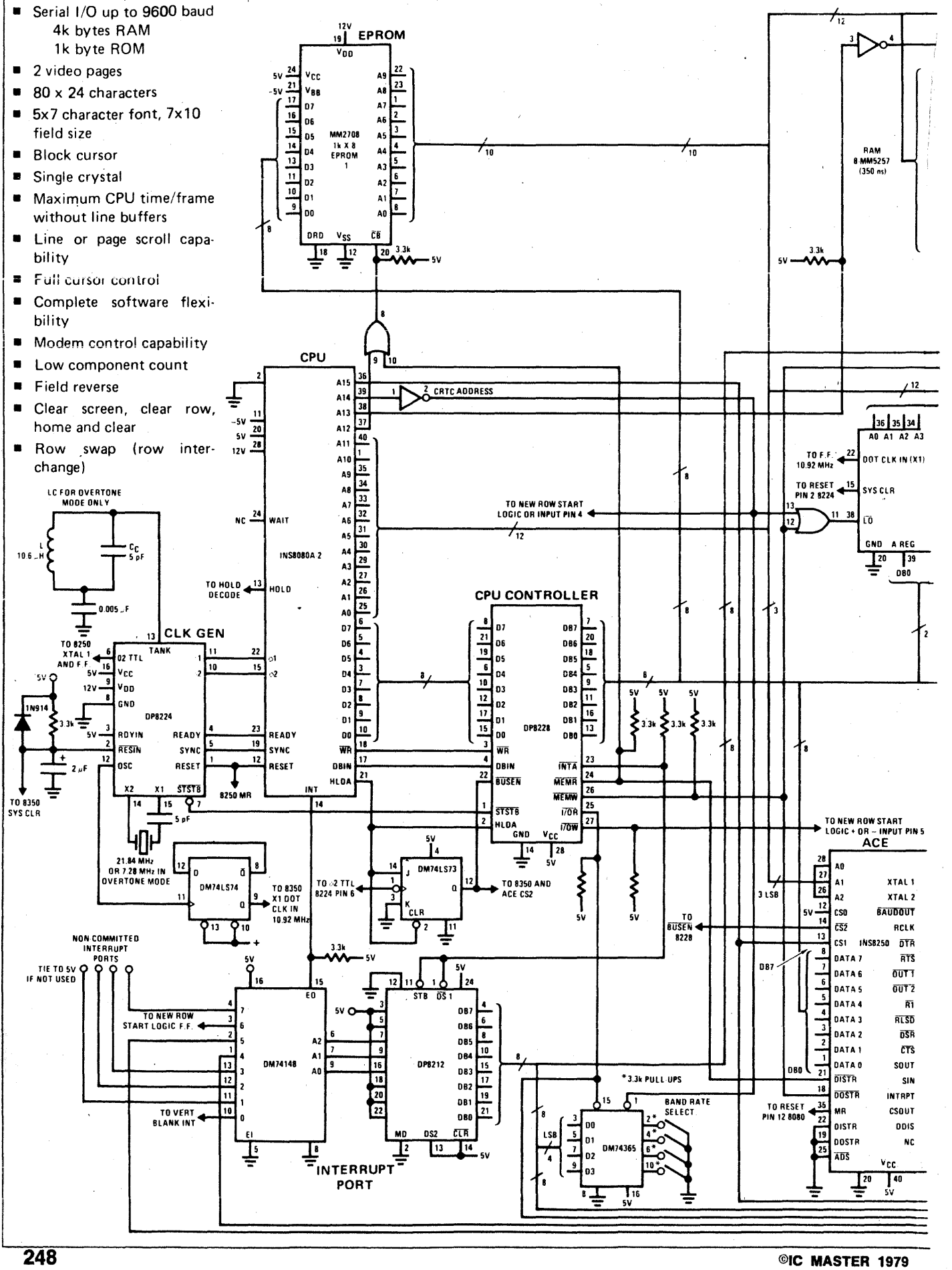
```
                        TITLE CRTC , 8080A 02/15/78
                ;** NATIONAL SEMICONDUCTOR'S
                ;   SERIES PROGRAMMABLE CRT CONTROLLER BOARD **
                ;AL BRILLIOTT-JIM TROUTNER
      0060      LASTROW =       060
      0061      ROW8080 =       061
      0062      FIRSTRO =       062
      0063      CHARNUM =       063
      0064      CRTCROW =       064
      0065      ROWSAVE =       065
      0066      TEMP1   =       066
      0067      TEMP2   =       067
      0068      IMASK   =       068
0000                    =0000
0000 F3     START:  DI              ;DISABLE INTERRUPTS
0001 31FF3F         LXI     SP,03FFF        ;LOAD STACK POINTER
0004 C33B00         JMP     INIT            ;JUMP TO INITILIZE ROUTINE
0007                    =0008
0008 C32502         JMP     NEWRO           ;NEW ROW START INTERRUPT
000B                    =0010
0010 C34A01         JMP     INTACE          ;ACE INTERUPT
0013                    =0018
0018 C33601         JMP     INTKB           ;KEYBOARD INTERUPT
001B                    =0038
0038 C34F02         JMP     VERTI           ;VERTICAL INTERUPT
003B 210030 INIT:   LXI     H,03000         ;1ST RAM ADDRESS
003E 0E20           MVI     C,020           ;ASCII SPACE INTO C REG.
0040 3E3F           MVI     A,03F           ;MAX RAM ADDRESS
0042 71     CLRAM:  MOV     M,C             ;ASCII SPACE INTO MEM
0043 23             INX     H               ;NEXT RAM ADDRESS
0044 BC             CMP     H               ;MAX RAM ADDRESS?
0045 C24200         JNZ     CLRAM           ;IF NO THEN NEXT ADD.
0048 0E00           MVI     C,000
004A 3E40           MVI     A,040
004C 71     CLRAM1: MOV     M,C
004D 23             INX     H
004E BC             CMP     H
004F C24C00         JNZ     CLRAM1
0052 CD8700         CALL    HMCUR           ;GO TO CUR HOME ROUTINE
0055 CD9300         CALL    BAUD            ;GO TO BAUD LOAD ROUTINE
                ;NEW ROW START LOOK UP TABLE GENERATION
0058 21003F         LXI     H,03F00         ;N.R.S. HIGH ADDRESS
005B 11303F         LXI     D,03F30         ;N.R.S. LOW ADDRESS
005E 010030         LXI     B,03000         ;N.R.S. ADDRESS DATA
0061 70     NRS:    MOV     M,B             ;STORE TO N.R.S. DATA TABLE
0062 79             MOV     A,C             ;N.R.S. DATA LOW TO ACC
0063 12             STAX    D               ;STORE TO N.R.S. DATA TABLE L
0064 C650           ADI     050             ;ACC READY FOR NEXT LOAD
0066 4F             MOV     C,A             ;ACC TO N.R.S. DATA HIGH
0067 78             MOV     A,B             ;N.R.S. DATA TO ACC
0068 CE00           ACI     000             ;ADD CARRY BIT TO DATA HIGH
006A 47             MOV     B,A             ;MOVE RESULT TO N.R.S. DATA H
006B 2C             INR     L               ;INCREMENT N.R.S. HIGH ADD
006C 1C             INR     E               ;INCREMENT N.R.S. LOW ADD
006D 7B             MOV     A,E             ;N.R.S. ADD LOW TO ACC
006E FE60           CPI     LASTROW         ;MAX TABLE ADDRESS
0070 C26100         JNZ     NRS             ;IF FALSE JUMP
                ;REFERENCE TABLE INITILIZE
0073 3E17           MVI     A,017           ;LAST ROW NUMBER TO ACC
0075 12             STAX    D               ;STORE TO REFERENCE TABLE
                ;CLEAR PERIPHERAL INTERRUPT FLOPS
0076 D340           OUT     040             ;N.R.S. INTERRUPT CLEAR
0078 DB80           IN      080             ;KEYBOARD INTERRUPT CLEAR
                ;SET UP POINTERS
007A 11603F         LXI     D,03F60         ;POINT D-E TO REFERENCE TABLE
007D 210030         LXI     H,03000         ;POINT H-L TO 1ST RAM LOCATI
0080 010090         LXI     B,09000         ;POINT B-C TO ACE
                ;WAIT LOOP FOR INTERUPTS
0083 FB     BACK:   EI                      ;ENABLE INTERRUPTS
0084 C38300         JMP     BACK            ;LOOP UNTIL INTERRUPTED
                ;HOME UP CURSOR
0087 210050 HMCUR   LXI     H,05000         ;POINT B-C TO CRTC
008A 3E02           MVI     A,002           ;T.O.P. REGISTER SELECT
008C 77             MOV     M,A             ;T.O.P. LOAD
008D 3C             INR     A               ;CURSOR REGISTER SELECT
008E 77             MOV     M,A             ;CURSOR LOADS TO T.O.P.
008F 210030         LXI     H,03000         ;POINT H-L TO 1ST RAM ADD
0092 C9             RET                     ;RETURN
                ;BAUD RATE SELECT
0093 D5     BAUD    PUSH    D               ;SAVE D-E REGISTERS
0094 DB40           IN      040             ;READ BAUD SELECT CODE
0096 E60F           ANI     00F             ;ZERO THE HIGH ORDER 4 BITS
0098 FE00           CPI     000
009A CAD400         JZ      B110            ;110 BAUD ROUTINE
009D FE01           CPI     001
009F CADA00         JZ      B150            ;150 BAUD ROUTINE
00A2 FE02           CPI     002
00A4 CAE000         JZ      B300            ;300 BAUD ROUTINE
00A7 FE03           CPI     003
00A9 CAE600         JZ      B600            ;600 BAUD ROUTINE
00AC FE04           CPI     004
00AE CAEC00         JZ      B1200           ;1200 BAUD ROUTINE
00B1 FE05           CPI     005
00B3 CAF200         JZ      B1800           ;1800 BAUD ROUTINE
00B6 FE06           CPI     006
00B8 CAF800         JZ      B2000           ;2000 BAUD ROUTINE
00BB FE07           CPI     007
00BD CAFE00         JZ      B2400           ;2400 BAUD ROUTINE
00C0 FE08           CPI     008
00C2 CA0401         JZ      B3600           ;3600 BAUD ROUTINE
00C5 FE09           CPI     009
00C7 CA0A01         JZ      B4800           ;4800 BAUD ROUTINE
00CA FE0A           CPI     00A
00CC CA1001         JZ      B7200           ;7200 BAUD ROUTINE
00CF FE0B           CPI     00B
00D1 CA1601         JZ      B9600           ;9600 BAUD ROUTINE
                ;BAUD RATE SET UP ROUTINES
00D4 110305 B110    LXI     D,00563         ;110 BAUD DIVISOR
00D7 C31C01         JMP     ACELD           ;GO TO ACE LOAD ROUTINE
00DA 11F303 B150    LXI     D,003F3         ;150 BAUD DIVISOR
00DD C31C01         JMP     ACELD
00E0 11F901 B300    LXI     D,001F9         ;300 BAUD DIVISOR
00E3 C31C01         JMP     ACELD
00E6 11FC00 B600    LXI     D,000FC         ;600 BAUD DIVISOR
00E9 C31C01         JMP     ACELD
00EC 117E00 B1200:  LXI     D,0007E         ;1200 BAUD DIVISOR
00EF C31C01         JMP     ACELD
00F2 115400 B1800:  LXI     D,00054         ;1800 BAUD DIVISOR
00F5 C31C01         JMP     ACELD
00F8 114C00 B2000:  LXI     D,0004C         ;2000 BAUD DIVISOR
00FB C31C01         JMP     ACELD
00FE 113F00 B2400:  LXI     D,0003F         ;2400 BAUD DIVISOR
0101 C31C01         JMP     ACELD
0104 112A00 B3600:  LXI     D,0002A         ;3600 BAUD DIVISOR
0107 C31C01         JMP     ACELD
010A 112000 B4800:  LXI     D,00020         ;4800 BAUD DIVISOR
010D C31C01         JMP     ACELD
0110 111500 B7200   LXI     D,00015         ;7200 BAUD DIVISOR
0113 C31C01         JMP     ACELD
0116 111000 B9600   LXI     D,00010         ;9600 BAUD DIVISOR
0119 C31C01         JMP     ACELD
                ;ACE LOAD ROUTINE
011C 010390 ACELD:  LXI     B,09003         ;POINT B C TO ACE
011F 3E83           MVI     A,083           ;INIT BAUD LOAD - 8 BITS
0121 02             STAX    B               ;DO INIT BAUD LOAD
0122 0E01           MVI     C,001           ;POINT TO BAUD HIGH
0124 7A             MOV     A,D             ;GET BAUD HIGH
0125 02             STAX    B               ;STORE BAUD HIGH TO ACE
0126 0E00           MVI     C,000           ;POINT ACE TO BAUD LOW
0128 7B             MOV     A,E             ;GET BAUD LOW
0129 02             STAX    B               ;STORE BAUD LOW TO ACE
012A 0E03           MVI     C,003           ;RESET DLAB TO ZERO
012C 79             MOV     A,C             ;INIT ACE T/R
012D 02             STAX    B               ;PUT TO ACE
012E 0E01           MVI     C,001           ;INTERRUPT ENABLE REG
0130 79             MOV     A,C             ;SELECT RECEIVED DATA INTERR
0131 02             STAX    B               ;LOAD IT
0132 0E00           MVI     C,000           ;RESTORE B-C ACE POINTER
0134 D1             POP     D               ;RESTORE D-E REGISTERS
0135 C9             RET                     ;RETURN
                ;KEYBOARD INTERRUPT ROUTINE
0136 DB80   INTKB:  IN      080             ;READ KEYBOARD
0138 FB             EI                      ;ENABLE INTERRUPTS
0139 FE05           CPI     005             ;NEED BAUD RATE? (CNTL E)
013B CA9300         JZ      BAUD            ;IF YES GO TO BAUD ROUTINE
013E FE12           CPI     012             ;INVERT NEXT CNTL R
0140 CA4803         JZ      IVERTN
0143 FE13           CPI     013             ;INVERT ROW CNTL S
0145 CA5403         JZ      IVERTR
0148 02             STAX    B               ;STORE BYTE TO ACE
0149 C9             RET                     ;RETURN
                ;ACE INTERUPT ROUTINE
014A 0A     INTACE: LDAX    B               ;LOAD ACE DATA BYTE TO ACC.
014B FB             EI                      ;ENABLE INTERRUPTS
014C FE7E           CPI     07E
014E CA7001         JZ      FUNC            ;TEST FOR ESC COMAMD
0151 FE7F           CPI     07F             ;TEST FOR DEL COMAND
0153 CA7001         JZ      FUNC
0156 5F             MOV     E,A             ;SAVE CHAR IN REG E
0157 E660           ANI     060             ;MASK OUT BITS FOR CNTL TEST
0159 CA7001         JZ      FUNC            ;IF ZERO JMP TO CNTL FUNC
015C 3A683F         LDA     03F68           ;LOAD INVERT MASK
015F B3             ORA     E               ;OR MASK AND CHAR
0160 77             MOV     M,A             ;STORE DATA BYTE TO RAM
                ;ADVANCE CURSOR
0161 1E63   ADCUR:  MVI     E,CHARNUM       ;POINT B-C TO CHAR #
0163 1A             LDAX    D               ;LOAD CHAR # TO ACC
0164 23             INX     H               ;NEXT CHAR LOCATION
0165 FE4F           CPI     04F             ;LAST CHAR OF ROW?
0167 CABE01         JZ      NXRO            ;IF TRUE JUMP TO NEXT ROW
016A C601           ADI     001             ;INCREMENT CHAR #
016C 12             STAX    D               ;STORE CHAR # TO RAM REF.
016D C3B301         JMP     PCUR            ;PUT CURSOR
                ;TEST FOR FUNCTION
0170 7B     FUNC:   MOV     A,E
0171 FE01           CPI     001             ;HOME AND CLEAR CNTL A (SOH)
0173 CA0000         JZ      START
0176 FE0D           CPI     00D             ;CARRAGE RETURN
0178 CA6E02         JZ      CR
017B FE11           CPI     011             ;SAVE ROW # CNTL Q (DC1)
017D CA7B02         JZ      SAVRO
0180 FE0C           CPI     00C             ;ADVANCE CURSOR CNTL L (FF)
0182 CA6101         JZ      ADCUR
0185 FE02           CPI     002             ;HOME UP CNTL B (STX)
0187 CAA402         JZ      HOME
018A FE1A           CPI     01A             ;SWAP   CNTL Z (SUB)
018C CAB502         JZ      SWAP
018F FE0A           CPI     00A             ;LINEFEED
0191 CA8D02         JZ      LF
0194 FE08           CPI     008             ;BACKSPACE CNTL H (BS)
0196 CAE002         JZ      BS
0199 FE0B           CPI     00B             ;UP CURSOR CNTL K (VT)
019B CAF102         JZ      UPCUR
019E FE18           CPI     018             ;CLEAR ROW CNTL X (CAN)
01A0 CA3003         JZ      CLROW
01A3 FE07           CPI     007             ;RING BELL CNTL G (BEL)
01A5 CA4503         JZ      BELL
01A8 FE12           CPI     012             ;INVERT NEXT CNTL R (DC2)
01AA CA4803         JZ      IVERTN
01AD FE13           CPI     013             ;INVERT ROW CNTL S (DC3)
01AF CA5403         JZ      IVERTR
01B2 C9             RET                     ;RETURN
                ;STORE CURSOR TO CRTC FROM H-L REGISTERS
01B3 7C     PCUR    MOV     A,H             ;H REG TO ACC
01B4 C620           ADI     020             ;SET H-L REG TO CRTC ADD.
01B6 67             MOV     H,A             ;H IS CRTC ADD.
01B7 3603           MVI     M,003           ;CURSOR REGISTER SELECT
01B9 7C             MOV     A,H             ;H REG SET BACK TO VIDIO RAM
01BA D620           SUI     020             ;ADDRESS
01BC 67             MOV     H,A
01BD C9             RET                     ;RETURN
                ;LAST ROW ON SCREEN
01BE CDDC01 NXRO    CALL    NXRO1           ;GO TO NEXT ROW SUBROUTINE
01C1 CDF301         CALL    ZCHAR           ;ZERO CHARACTER
01C4 E5     CLROW3  PUSH    H               ;SAVE H,L
01C5 1E60           MVI     E,LASTROW       ;POINT D,E TO LASTROW
01C7 1A             LDAX    D
01C8 C601           ADI     001             ;POINT AC TO FIRST ROW OFF SC
01CA FE30           CPI     030             ;CK IF LAST ROW IN RAM
01CC CAD701         JZ      ROZERO
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(Continued on page 13)

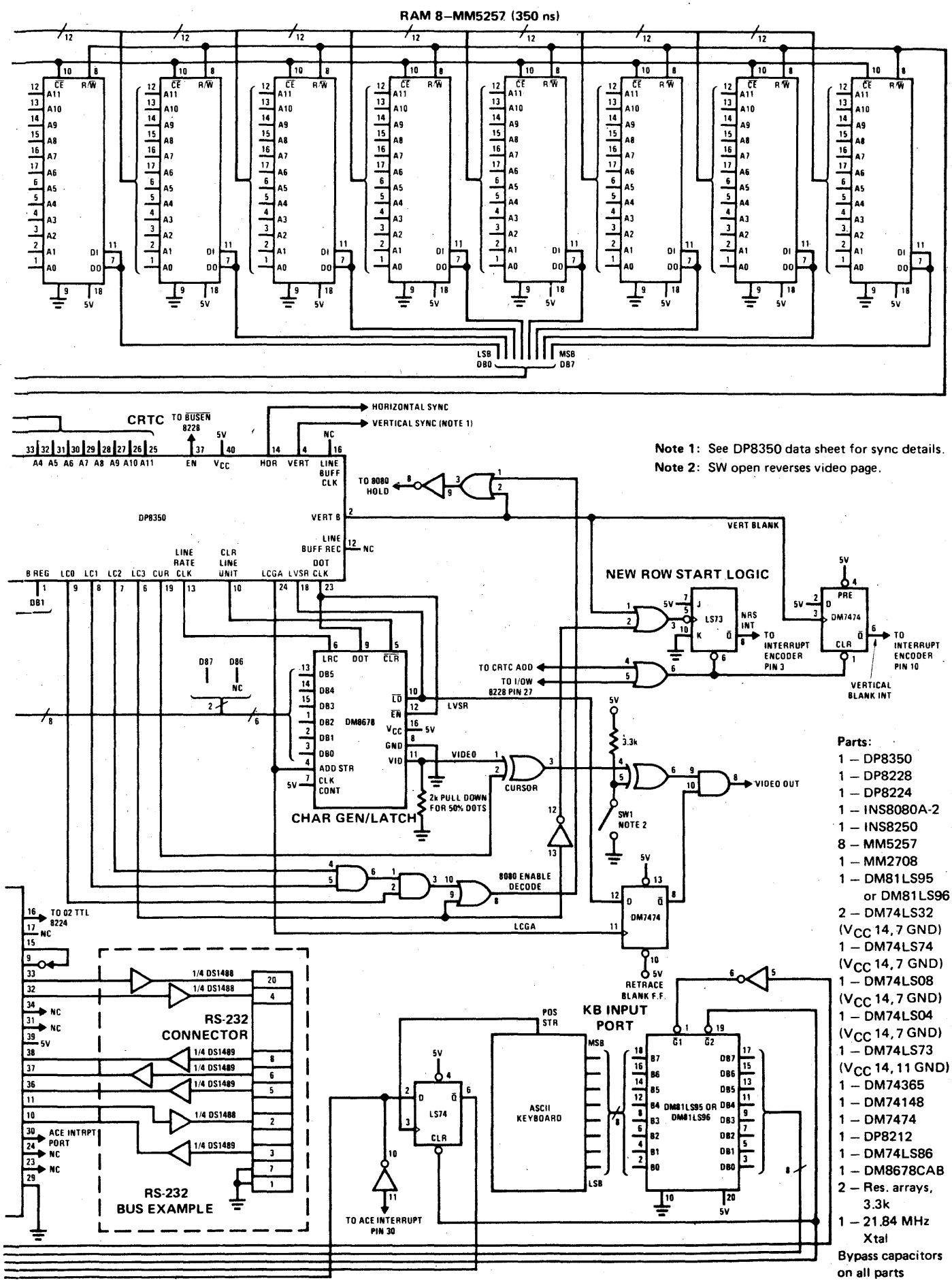
FEATURES

- Keyboard input port
- Serial I/O up to 9600 baud
  - 4k bytes RAM
  - 1k byte ROM
- 2 video pages
- 80 x 24 characters
- 5x7 character font, 7x10 field size
- Block cursor
- Single crystal
- Maximum CPU time/frame without line buffers
- Line or page scroll capability
- Full cursor control
- Complete software flexibility
- Modem control capability
- Low component count
- Field reverse
- Clear screen, clear row, home and clear
- Row swap (row interchange)

VIDEO DATA TERMINAL SYSTEM SCHEMATIC



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Note 1: See DP8350 data sheet for sync details.

Note 2: SW open reverses video page.

Parts:

- 1 – DP8350
- 1 – DP8228
- 1 – DP8224
- 1 – INS8080A-2
- 1 – INS8250
- 8 – MM5257
- 1 – MM2708
- 1 – DM81LS95 or DM81LS96
- 2 – DM74LS32 (V_{CC} 14, 7 GND)
- 1 – DM74LS74 (V_{CC} 14, 7 GND)
- 1 – DM74LS08 (V_{CC} 14, 7 GND)
- 1 – DM74LS04 (V_{CC} 14, 7 GND)
- 1 – DM74LS73 (V_{CC} 14, 11 GND)
- 1 – DM74365
- 1 – DM74148
- 1 – DM7474
- 1 – DP8212
- 1 – DM74LS86
- 1 – DM8678CAB
- 2 – Res. arrays, 3.3k
- 1 – 21.84 MHz Xtal

Bypass capacitors on all parts

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01CF CD8302 LOOP5:  CALL    LDHL1           ;LOAD H,L WITH ADD  OF LASTRO
01D2 CD3B03         CALL    CLROW2
01D5 E1             POP     H               ;RESTORE H,L
01D6 C9             RET
01D7 3E00   ROZERO: MVI     A,000           ;LOAD ROW ZERO
01D9 C3CF01         JMP     LOOP5
                    ;NEXT ROW
01DC 1E60   NXRO1:  MVI     E,LASTROW       ;POINT D-E REG TO LAST ROW
01DE 1A             LDAX    D               ;PUT LAST ROW # TO ACC
01DF EB             XCHG                    ;EXCHANGE H-L WITH D-E
01E0 23             INX     H               ;H-L IS NOW AT 8080 ROW #
01E1 BE             CMP     M               ;COMPARE LAST ROW # WITH
01E2 CA0502         JZ      SCROLL          ;8080 ROW # IF TRUE SCROLL
                    ;INCREMENT 8080 ROW #
01E5 3E2F   INCRO:  MVI     A,02F           ;TEST FOR MAX ROW AND
01E7 BE             CMP     M               ;JUMP TO ZERO ROW IF TRUE
01E8 CAFB01         JZ      ZROW            ;ZERO ROW
01EB 34             INR     M               ;INCREMENT THE 8080 ROW #
01EC EB             XCHG                    ;POINT H-L TO CHAR #
01ED 1E61           MVI     E,ROW8080
01EF CD8202         CALL    LDHL
01F2 C9             RET                     ;RETURN
                    ;ZERO CHARACTER
01F3 3E00   ZCHAR:  MVI     A,000           ;PUT CHAR # TO ZERO
01F5 32633F         STA     03F63           ;AND STORE
01F8 C3B301         JMP     PCUR            ;GO TO PUT CURSOR ROUTINE
                    ;ZERO 8080 ROW #
01FB 3600   ZROW:   MVI     M,000           ;8080 ROW # TO ZERO
01FD 2E00           MVI     L,000           ;N.R.S.  ADDRESS HIGH
01FF 56             MOV     D,M             ;N.R.S.  DATA HIGH TO D REG
0200 2E30           MVI     L,030           ;N.R.S.  ADDRESS LOW
0202 5E             MOV     E,M             ;N.R.S.  DATA LOW TO E REG
0203 EB             XCHG                    ;EXCHANGE H-L WITH D-E
0204 C9             RET                     ;RETURN
                     ROW SCROLL
0205 2B     SCROLL: DCX     H               ;POINT H-L TO LAST ROW#
0206 3E2F           MVI     A,02F           ;BEFORE SCRATCH TABLES
0208 BE             CMP     M               ;TEST FOR THE LAST ROW
0209 CA1902         JZ      ZLRO            ;JUMP TO ZERO LAST ROW IF TR
020C 34             INR     M               ;INCREMENT TO NEXT ROW
020D 2E62   ROLO:   MVI     L,FIRSTRO       ;POINT H-L TO FIRST ROW#
020F BE             CMP     M               ;IS FIRST LOW = TO LAST ROW.
0210 CA1E02         JZ      ZFRO            ;JUMP TO ZERO FIRST R
0213 34             INR     M               ;INCREMENT TO NEXT ROW
0214 2E61           MVI     L,ROW8080       ;POINT H-L TO 8080 ROW
0216 C3E501         JMP     INCRO           ;GO TO INCREMENT ROW ROUTINE
0219 3600   ZLRO:   MVI     M,000           ;PUT LAST ROW# TO ZERO
021B C30D02         JMP     ROLO            ;GO TO ROUTINE FOR FIRST ROW
021E 3600   ZFRO:   MVI     M,000           ;PUT FIRST ROW# TO ZERO
0220 2E61           MVI     L,ROW8080       ;POINT H-L TO 8080 ROW
0222 C3E501         JMP     INCRO           ;GO TO INCREMENT ROW ROUTINE
                    ;NEW ROW START INTERRUPT
0225 F5     NEWRO:  PUSH    PSW             ;SAVE ACC AND FLAGS
0226 E5             PUSH    H               ;SAVE H-L REG
0227 D5             PUSH    D
0228 11643F         LXI     D,03F64         ;POINT D-E TO CRTCROW #
022B 1A             LDAX    D               ;LOAD ACC WITH CRTC ROW #
022C 5F             MOV     E,A             ;N.R.S.  DATA ADD HIGH TO E
022D 1A             LDAX    D               ;ROW DATA HIGH INTO ACC
022E C620           ADI     020
0230 67             MOV     H,A             ;N.R.S.  DATA ADD HIGH INTO H
0231 7B             MOV     A,E
0232 C630           ADI     030             ;ACC TO N.R.S.  DATA LOW
0234 5F             MOV     E,A             ;N.R.S.  DATA ADD LOW TO E REG
0235 1A             LDAX    D               ;ROW DATA LOW TO ACC
0236 6F             MOV     L,A             ;N.R.S DATA ADD LOW INTO L
0237 3601           MVI     M,001           ;STORE N.R.S.  TO CRTC
0239 D340           OUT     040             ;RESET N.R.S.  AND VERT INTER
023B 1E64           MVI     E,CRTCROW
023D 1A             LDAX    D
023E FE2F           CPI     02F             ;TEST FOR CRTC MAX ROW
0240 CA4A02         JZ      ZCRTC           ;IF TRUE ZERO ACC
0243 3C             INR     A               ;INCREMENT TO NEXT ROW
0244 12     LOOP:   STAX    D               ;STORE NEXT ROW NUMBER
0245 D1             POP     D
0246 E1             POP     H               ;RESTORE H-L REG
0247 F1             POP     PSW             ;RESTORE ACC AND FLAGS
0248 FB             EI
0249 C9             RET                     ;RETURN
                    ;ZERO CRTCROW
024A 3E00   ZCRTC:  MVI     A,000           ;ZERO ACC
024C C34402         JMP     LOOP
                    ;VERTICAL INTERRUPT
024F F5     VERTI:  PUSH    PSW             ;SAVE ACC AND FLAGS
0250 E5             PUSH    H               ;SAVE H REG
0251 D5             PUSH    D
0252 1E62           MVI     E,FIRSTRO       ;POINT D-E TO FIRST ROW #
0254 1A             LDAX    D               ;LOAD 1ST ROW # INTO ACC
0255 1E64           MVI     E,CRTCROW       ;POINT D-E TO CRTCROW #
0257 12             STAX    D               ;UPDATE CRTCROW #
0258 E63F           ANI     03F             ;REMOVE MARKER
025A 5F             MOV     E,A             ;POINT H-L TO CRTC FIRST ROW
025B 1A             LDAX    D
025C C620           ADI     020
025E 67             MOV     H,A
025F 7B             MOV     A,E
0260 C630           ADI     030
0262 5F             MOV     E,A
0263 1A             LDAX    D
0264 6F             MOV     L,A
0265 3602           MVI     M,002           ;STORE TOP OF PAGE
0267 D340           OUT     040
0269 D1             POP     D
026A E1             POP     H
026B F1             POP     PSW             ;RESTORE ACC AND FLAGS
026C FB             EI
026D C9             RET                     ;RETURN

                    ;CARRAGE RETURN
026E 1E63   CR:     MVI     E,CHARNUM       ;POINT D-E TO CHAR #
0270 3E00           MVI     A,000
0272 12             STAX    D
0273 1E61           MVI     E,ROW8080
0275 CD8202         CALL    LDHL
0278 C3B301         JMP     PCUR            ;CURSOR TO THE BEGINNING OF R
                    ;SAVE ROW
027B 1E61   SAVRO:  MVI     E,ROW8080       ;POINT D-E TO 8080 ROW#
027D 1A             LDAX    D               ;PUT 8080 ROW # TO ACC
027E 1E65           MVI     E,ROWSAVE       ;POINT D-E TO ROW SAVE
0280 12             STAX    D               ;STORE ROW SAVE # IN REF TAB
0281 C9             RET                     ;RETURN
                    H-L ROW DATA LOAD ROUTINE
0282 1A     LDHL:   LDAX    D               ;LOAD ACC WITH D-E DATA
0283 5F     LDHL1:  MOV     E,A             ;POINT D-E TO N.R.S.  DATA HI
0284 1A             LDAX    D               ;ROW # TO N.R.S.  DATA HIGH
0285 67             MOV     H,A             ;ROW # TO H REG
0286 7B             MOV     A,E             ;PUT 1ST ROW # TO ACC
0287 C630           ADI     030             ;ACC TO N.R.S.  ADD LOW
0289 5F             MOV     E,A             ;POINT D-E TO N.R.S.  DATA LOW
028A 1A             LDAX    D               ;ROW # TO N.R.S DATA LOW
028B 6F             MOV     L,A             ;ROW # TO L REG
028C C9             RET                     ;RETURN
                    ;LINEFEED
028D CDDC01 LF:     CALL    NXRO1           ;DO NEXT ROW SUBROUTINE
0290 CDC401         CALL    CLROW2          ;OFF SCREEN CLEAR ROW ROUTINE
0293 1E61           MVI     E,ROW8080       ;MOVE REFERENCE ROW # TO H-L
0295 CD8202         CALL    LDHL            ;LOAD H-L
0298 3A633F ADDCH:  LDA     03F63           ;CHAR # TO ACC
029B 85             ADD     L               ;ADD THE CHAR # TO THE
029C 6F             MOV     L,A             ;FIRST ROW ADDRESS
029D 7C             MOV     A,H             ;IF A CARRY OCCURED ADD TO
029E CE00           ACI     000             ;THE DATA HIGH
02A0 67             MOV     H,A             ;H-L POINTS TO LINE FED ROW
02A1 C3B301         JMP     PCUR            ;PUT CURSOR TO LINE FED ROW
                    ;HOME CURSOR TO T O P
02A4 1E62   HOME:   MVI     E,FIRSTRO       ;POINT D-E TO 1ST ROW
02A6 1A             LDAX    D               ;STORE FIRSTROW TO ROW8080
02A7 1E61           MVI     E,ROW8080
02A9 12             STAX    D
02AA CD8302         CALL    LDHL1           ;MOVE REFERENCE ROW TO H-L
02AD 3E00           MVI     A,000           ;PUT CHAR # BACK
02AF 32633F         STA     03F63           ;TO ZERO
02B2 C3B301         JMP     PCUR            ;PUT CURSOR HOME
                    ;SWAP ROWS
02B5 1E65   SWAP:   MVI     E,ROWSAVE       ;POINT D-E TO ROW SAVE # AND
02B7 CD8202         CALL    LDHL            ;PUT IN H-L REG
02BA 22663F         SHLD    03F66           ;STORE ROW SAVE # TO TEMP 1 *
02BD 1E61           MVI     E,ROW8080       ;POINT D-E TO 8080 ROW # AND
02BF CD8202         CALL    LDHL            ;PUT ADDRESS IN H-L REG
02C2 1E65           MVI     E,ROWSAVE       ;POINT D-E TO ROW SAVE # AND
02C4 1A             LDAX    D               ;PUT IN ACC
02C5 5F             MOV     E,A             ;8080 ROW # TO ADD HIGH
02C6 7C             MOV     A,H             ;STORE 8080 ROW # TO N.R.S
02C7 12             STAX    D               ;DATA HIGH
02C8 7B             MOV     A,E
02C9 C630           ADI     030
02CB 5F             MOV     E,A             ;PUT 8080 ROW # TO
02CC 7D             MOV     A,L             ;N.R.S  DATA LOW
02CD 12             STAX    D               ;8080 ROW # IS NOW IN ROW SA
02CE 2A663F         LHLD    03F66           ;PUT ROW SAVE # BACK TO H-L
02D1 1E61           MVI     E,ROW8080       ;COMENT SAME AS ABOVE
02D3 1A             LDAX    D
02D4 5F             MOV     E,A
02D5 7C             MOV     A,H
02D6 12             STAX    D
02D7 7B             MOV     A,E
02D8 C630           ADI     030
02DA 5F             MOV     E,A
02DB 7D             MOV     A,L
02DC 12             STAX    D
02DD C39802         JMP     ADDCH           ;JUMP TO ADD CHAR
                    ;BACK SPACE
02E0 1E63   BS:     MVI     E,CHARNUM       ;POINT THE D-E REG TO CHAR #
02E2 1A             LDAX    D               ;AND PUT IN ACC
02E3 FE00           CPI     000             ;TEST FOR THE CHAR # =
02E5 CAEE02         JZ      UPROW           ;TO ZERO  JUMP IF TRUE
02E8 3D             DCR     A               ;DECREMENT CHAR #
02E9 12             STAX    D               ;STORE DECREMENTED CHAR #
02EA 2B             DCX     H               ;DEC H-L FOR NEW CURSOR LOCA
02EB C3B301         JMP     PCUR            ;PUT CURSOR IN DECREMENTED LO
                    ;NEXT ROW UP
02EE 3E4F   UPROW:  MVI     A,04F           ;MOVE THE CHAR #
02F0 12             STAX    D               ;TO 50H AND STORE IT
                    ;MOVE CURSOR UP
02F1 EB     UPCUR:  XCHG                    ;POINT H-L TO 8080 ROW AND D-
02F2 2E61           MVI     L,ROW8080       ;TO NEW CURSOR LOCATION
02F4 7E             MOV     A,M             ;TEST IF NEXT UP CURSOR WILL
02F5 23             INX     H               ;BE ON THE FIRST ROW
02F6 BE             CMP     M               ;IF TRUE JUMP TO
02F7 CA0803         JZ      UPSCL           ;UP SCROLL ROUTINE
02FA 2B             DCX     H               ;POINT H-L BACK TO 8080 ROW #
02FB FE00   BACK1:  CPI     000             ;IF 8080 ROW # IS EQUAL TO
02FD CA1E03         JZ      RO48            ;ZERO JUMP TO ROW 48 ROUTINE
0300 35             DCR     M               ;DECREMENT 8080 ROW #
0301 EB     LOOP1:  XCHG                    ;POINT H-L TO NEW CURSOR LOCA
0302 CD8202         CALL    LDHL            ;AND D-E TO 8080 ROW #  JUMP
0305 C39802         JMP     ADDCH           ;TO ADD CHARACTER ROUTINE
0308 7E     UPSCL:  MOV     A,M             ;PUT FIRST ROW # INTO ACC
0309 FE00           CPI     000             ;TEST IF FIRST ROW # IS = TO
030B CA2403         JZ      FRO48           ;ZERO  IF TRUE JUMP TO ROW
030E 35             DCR     M               ;48 ROUTINE
030F 2E60   LOOP2:  MVI     L,LASTROW
0311 7E             MOV     A,M
0312 FE00           CPI     000
0314 CA2A03         JZ      LRO48
0317 35             DCR     M
0318 2E61   LOOP3:  MVI     L,ROW8080       ;POINT H-L TO 8080 ROW #
031A 7E             MOV     A,M             ;AND LOAD TO ACC
031B C3FB02         JMP     BACK1
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534 031E 3E2F   R048    MVI     A,02F           ;CHANGE 8080 ROW #
535 0320 77             MOV     M,A             ;TO 23D AND STORE
536 0321 C30103         JMP     LOOP1           ;JUMP TO POINTER EXCHANGE ROU
537
538 0324 3E2F   FR048   MVI     A,02F
539 0326 77             MOV     M,A
540 0327 C30F03         JMP     LOOP2
541
542 032A 3E2F   LR048   MVI     A,02F           ;PUT THE 1ST ROW TO
543 032C 77             MOV     M,A             ;17H
544 032D C31803         JMP     LOOP3           ;JUMP TO 8080 ROW # STORE
545
546                      CLEAR ROW ROUTINE
547
548 0330 CD3603 CLROW   CALL    CLROW1
549 0333 C36E02         JMP     CR
550
551 0336 1E61   CLROW1  MVI     E,ROW8080
552 0338 CD8202         CALL    LDHL            ;PUT ROW DATA IN H-L REG
553 033B 3E50   CLROW2  MVI     A,050           ;INTILIZE LOOP COUNTER
554 033D 3620   LOOP4   MVI     M,020           ;STORE ASCII SPACE IN MEM
555 033F 3D             DCR     A               ;DECREMENT LOOP COUNTER.
556 0340 C8             RZ                      ;RETURN IF ZERO BIT IS SET
557 0341 23             INX     H               ;NEXT LOCATION
558 0342 C33D03         JMP     LOOP4           ;CLEAR NEXT LOCATION
559
560 0345 D301   BELL    OUT     001             ;RING BELL
561 0347 C9             RET
562
563 0348 AF     IVERTN  XRA     A
564 0349 1E68           MVI     E,IMASK         ;POINT D/E TO MASK
565 034B 1A             LDAX    D
566 034C 17             RAL                     ;CK BIT 8 STATUS
567 034D DA5203         JC      RSSET
568 0350 3E80           MVI     A,080           ;INVERT BIT 8
569 0352 12     RESET   STAX    D               ;STORE OUT NEW MASK
570 0353 C9             RET
571
572 0354 E5     IVERTR  PUSH    H
573 0355 1E61           MVI     E,ROW8080
574 0357 CD8202         CALL    LDHL            ;LOAD 1ST ADD  OF 8080ROW TO
575 035A 1E50           MVI     E,050           ;SET COUNTER
576 035C 7E     LOOP6   MOV     A,M             ;GET CHAR
577 035D 17             RAL                     ;CK BIT 8 STATUS AND INVERT
578 035E DA7003         JC      RESET1
579 0361 1F             RAR
580 0362 F680           ORI     080             ;MASK BIT 8 HIGH
581 0364 77     BACK2   MOV     M,A             ;STORE MOD  CHAR TO MEM
582 0365 23             INX     H               ;POINT TO NEXT MEM
583 0366 7B             MOV     A,E
584 0367 FE01           CPI     001
585 0369 CA7603         JZ      DONE            ;RETURN IF COUNT = ZERO
586 036C 1D             DCR     E               ;DEC  COUNTER
587 036D C35C03         JMP     LOOP6
588
589 0370 1F     RESET1  RAR
590 0371 E67F           ANI     07F             ;RESET BIT 8
591 0373 C36403         JMP     BACK2
592
593 0376 E1     DONE    POP     H
594 0377 C9             RET
595      0000            END     START
```

```
A       0007    ACELD   011C    ADCUR   0161    ADDCH   0298
B       0000    B110    00D4    B1200   00EC    B150    00DA
B1800   00F2    B2000   00F8    B2400   00FE    B300    00E0
B3600   0104    B4800   010A    B600    00E6    B7200   0110
B9600   0116    BACK    0083    BACK1   02FB    BACK2   0364
BAUD    0093    BELL    0345    BS      02E0    C       0001
CHARNU  0063    CLRAM   0042    CLRAM1  004C    CLROW   0330
CLROW1  0336    CLROW2  033B    CLROW3  01C4    CR      026E
CRTCRO  0064    D       0002    DONE    0376    E       0003
FIRSTR  0062    FR048   0324    FUNC    0170    H       0004
HMCUR   0087    HOME    02A4    IMASK   0068    INCRO   01E5
INIT    003B    INTACE  014A    INTRB   0136    IVERTN  0348
IVERTR  0354    L       0005    LASTRO  0060    LDHL    0282
LDHL1   0283    LF      028D    LOOP    0244    LOOP1   0301
LOOP2   030F    LOOP3   0318    LOOP4   033D    LOOP5   01CF
LOOP6   035C    LR048   032A    M       0006    NEWRO   0225
NRS     0061    NXRO    01BE    NXR01   01DC    PCUR    01B3
PSW     0006    RESET   0352    RESET1  0370    R048    031E
ROLO    020D    ROW808  0061    ROWSAV  0065    ROZERO  01D7
SAVRO   027B    SCROLL  0205    SP      0006    START   0000
SWAP    02B5    TEMP1   0066 *  TEMP2   0067 *  UPCUR   02F1
UPROW   02EE    UPSCL   0308    VERTI   024F    ZCHAR   01F3
ZCRTC   024A    ZERO    021E    ZLRO    0219    ZROW    01FB

 NO ERROR LINES
SOURCE CHECKSUM = 403F
OBJECT CHECKSUM = 0F51
INPUT FILE    1 CRT80A.SRC ON JIMFM
OBJECT FILE   1 CRT80A.LM ON JIMFM
```

DEFINITIONS

ACE – Asynchronous communication element
CRTC – Cathode ray tube controller
Video Page – Visible screen data
Video RAM – Entire portion of RAM used only for display
First Row # – Address for top row of video page
Last Row # – Address for bottom row of video page
CRTC Row # – Address for next row load
8080 Row # – Address for cursor row
Character # – Character location in a row
XXXH are hexidecimal numbers

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DM8678 Bipolar Character Generator
INS8080 Assembly and Reference Manuals

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Simplify CRT Terminal Design with the DP8350, AN-198

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Hardware Reference Manual BLC 80/10 Board Level Computer. National Semiconductor Microcomputer Systems Chapter 6 – System Interfacing.

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CMOS A/D Converter Chips Easily Interface to 8080A Microprocessor Systems

National Semiconductor
Application Note 200
Jake Buurma

SUMMARY

This paper describes techniques for interfacing National Semiconductor's new ADC3511 and ADC3711 microprocessor compatible analog-to-digital converter chips to 8080A microprocessor systems. The hardware interface and the software interrupt service routine will be described for single and multiple A/D converter data acquisition systems.

INTRODUCTION

The recent introduction of monolithic digital voltmeter chips has encouraged designers to consider their use as analog-to-digital converters in data acquisition systems. While the high accuracy afforded at low cost was attractive, certain difficulties in applying these devices in digital systems were encountered. Most of these difficulties were due to the DVM chip's output structure being oriented towards driving 7-segment displays with internally generated digit scanning rates. National Semiconductor has recently introduced a family of monolithic CMOS A/D converters -- two of these devices are directed towards LED display DPM and DVM applications (ADD3501 3 1/2-digit DPM and ADD3701 3 3/4-digit DPM) while the other two (ADC3511 3 1/2-digit A/D and ADC3711 3 3/4-digit A/D) have addressable BCD outputs. These last two devices allow easy interface to microprocessor and calculator-oriented (COPS) systems.

Single or multiple channel monitoring of physical variables can be achieved with high accuracy despite the lack of complexity and low overall cost.

A/D CONVERSION

All A/D converters in this family operate from a single 5V supply and convert inputs from 0 to ±2V. The converters use a pulse-width modulation technique which requires no precision components and exhibits low offset, low drift, high linearity and no rollover error. An additional advantage is that the voltage reference is of the same polarity as the supply.

Two resolutions are offered: the 3 1/2-digit types divide the input into 2,000 counts plus sign, while the 3 3/4-digit types provide 4,000 counts plus sign which is roughly equivalent to the resolution of a 12-bit plus sign binary converter. The 3 1/2-digit converters require 200 ms per conversion; 3 3/4-digit types require 400 ms.

The converters handle negative inputs by internally switching the inputs and forcing the sign bit low. While this technique allows conversion of positive and negative inputs with only a single supply, the inputs must be floating with respect to the supply return. Without a floating supply, only positive voltages may be converted.

The basic converter is shown in *Figure 1*. The actual conversion technique is described in Appendix A.

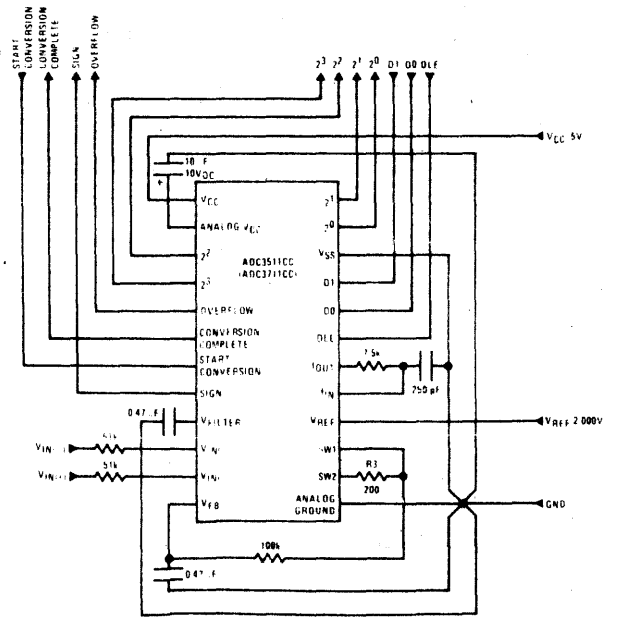


FIGURE 1. Basic A/D Converter

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BCD OUTPUT DESCRIPTION

The ADC3511 and ADC3711 present the output data in BCD form on a single 4-line output port, plus a separate sign output. The desired digit is selected by a 2-bit address which is latched by a high level at the Digit Latch Enable input (DLE); a low level at DLE allows flow thru operation. Since the output is BCD, it is compatible with many standard instruments and can easily be converted into binary by the processor if this format should be desired. Overrange inputs are indicated by a hexidecimal "EEEE" plus an Overflow output.

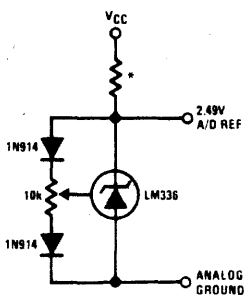
A new conversion is begun by a positive pulse or high level at the Start Conversion (SC) input. The analog section of the converter continuously tracks the analog input. The Start Conversion command controls only the transfer of new data to the output latches, consequently the delay from the SC pulse to the Conversion Complete (CC) signal may vary from several milliseconds to several hundred milliseconds. In interrupt driven systems the delay is no problem, since the processor does not execute delay instructions while waiting for the data. However, if in-line or program I/O is used where the program waits for the data to be ready, the maximum delay between SC and CC must be programmed into the wait routine. This type of I/O is therefore not as efficient as interrupt I/O.

The CC output goes low immediately after the SC pulse. At the end of a conversion, CC goes high and remains high until a new conversion is initiated. Continuous conversion operation is obtained by tying the SC input to V_{CC}.

REFERENCE VOLTAGE

The 2.000V reference is derived from the LM336, a recently announced monolithic reference which provides 2.5V with low drift at low cost. This active reference is adjusted for minimum thermal drift of about 20 ppm/°C by using a third terminal on the device to adjust its output to 2.490V.

Total reference current consumption is low, as the LM336 requires only 1 mA of bias current, and the resistor divider about 2 mA. The reference circuit is shown in *Figure 2*. One reference can be used for many A/D's. The value of the upper series resistor R1 depends on the number of converters used.



$$*R1 = \frac{2.49V}{(2N+1)\ mA} \quad N = 1, 2 \ldots 8$$

FIGURE 2. A/D Converter Reference. The 10k Pot is Adjusted to a Voltage of 2.49V on the Output; at this Voltage Minimum Drift Occurs. The Reference can Supply up to 8 A/D Converters.

A SINGLE CHANNEL CONVERTER

A complete A/D port is seen in *Figures 3 and 4*. *Figure 3* shows a Dual Polarity converter and *Figure 4* a Positive Only Polarity converter. Each port contains an A/D converter, TRI-STATE® bus driver, and 2 gates to control I/O. This A/D port is easily used in single or multichannel systems. In multichannel systems a converter is used on every channel allowing digital multiplexing of the outputs.

Data from the A/D converter in a single channel system is easily processed using an OUT command to start a conversion and IN commands to read the data after the microprocessor has been interrupted by a Conversion Complete.

As seen in *Figure 5*, a single channel A/D port uses a 6-bit bus comparator to decode its assigned peripheral address from the lower address bits of the 8080A address bus.

When an interrupt is received, the present status of the processor is stored on the stack memory by a series of push commands. The interrupt is serviced by reading digit 4 (MSD) into the processor and checking the overflow bit. If the overflow bit is high, the converter input has exceeded its range and an error signal is generated, indicating that scaling must be done to attenuate the input signal. If the OFL is low, the sign bit is then checked to determine the polarity of the conversion. If the sign bit is low, a "1" is added to the MSB of digit 4. Since this bit would normally be low, (maximum converter range allows MSB $\leq$ 3 or 0011) a "1" in this position is used to denote a negative input voltage. The 4 bits of digit 4 which now include the sign are shifted into the upper half of the first byte and the 4 bits of digit 3 are packed into the lower half. Similarly, digits 2 and 1 are packed into the second byte and both bytes stored in memory.

Figure 6 and routine 1 are the flow chart and assembly language routine used to implement this action.

8-CHANNEL A/D WITH SOFTWARE PRIORITY

The basic A/D port can easily be expanded to multiple channel systems. An 8-channel system is seen in *Figure 7*. This system interrupts the processor when one of the Conversion Complete outputs goes high. The processor saves the current status and reads the status word of the A/D system. The status word is then compared to a priority table. Each level in the table corresponds to a priority level with high priority converters which are first in the table. If 2 or more converters have the same priority and are ready at the same time, the converter with the highest number gets serviced first.

The program determines which service routine to use by the bit position of "1's" in the status word. The routine loads the address pointer to digit 4 of the selected converter. The program then calls a subroutine which

goes through the process of checking overflow, sign and packs 4 BCD digits into 2 bytes. These 2 bytes are then stored in a table in the memory directly above the converter addresses. After a channel is serviced, the original processor status is restored and the interrupt enabled. If additional channels need service, they immediately interrupt so the new status word is then read and a new priority established.

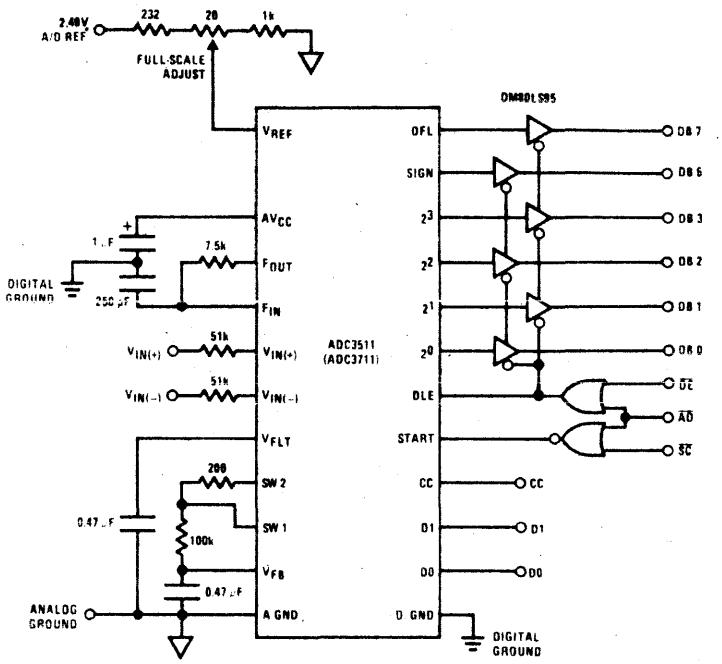


FIGURE 3. Dual Polarity A/D Requires that Inputs are Floating with Respect to the Supply. Input Range is ±1.999V.

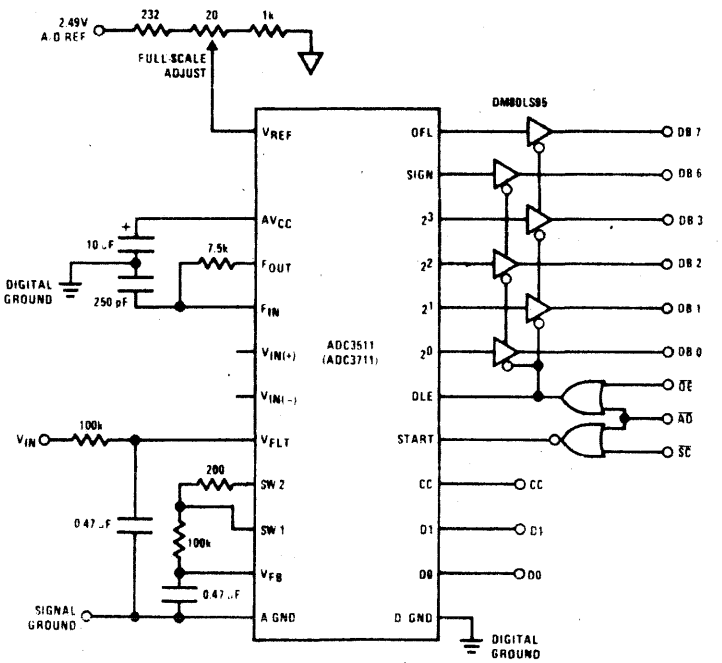


FIGURE 4. Positive Polarity A/D Operating from 5V Supply. Input Range is +1.999V.

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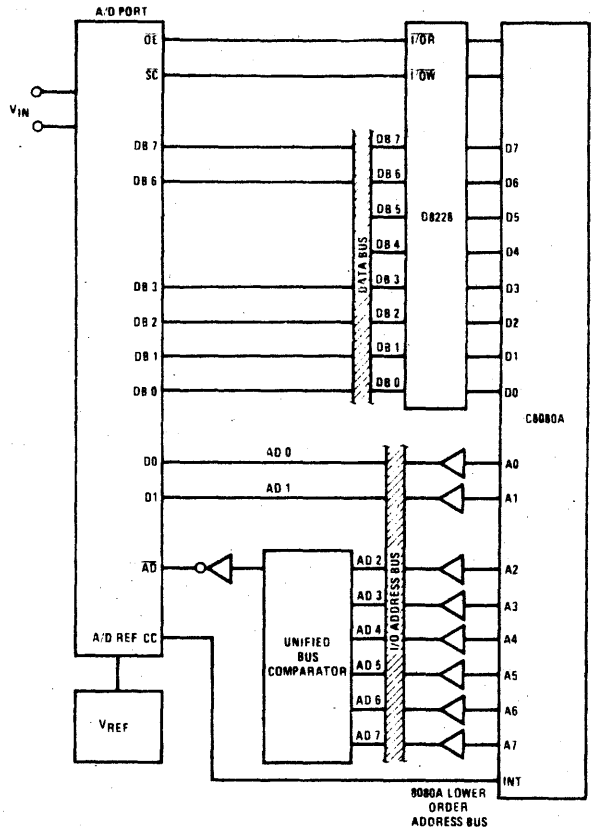


FIGURE 5. Single Channel A/D Interface with Peripheral Mapped I/O

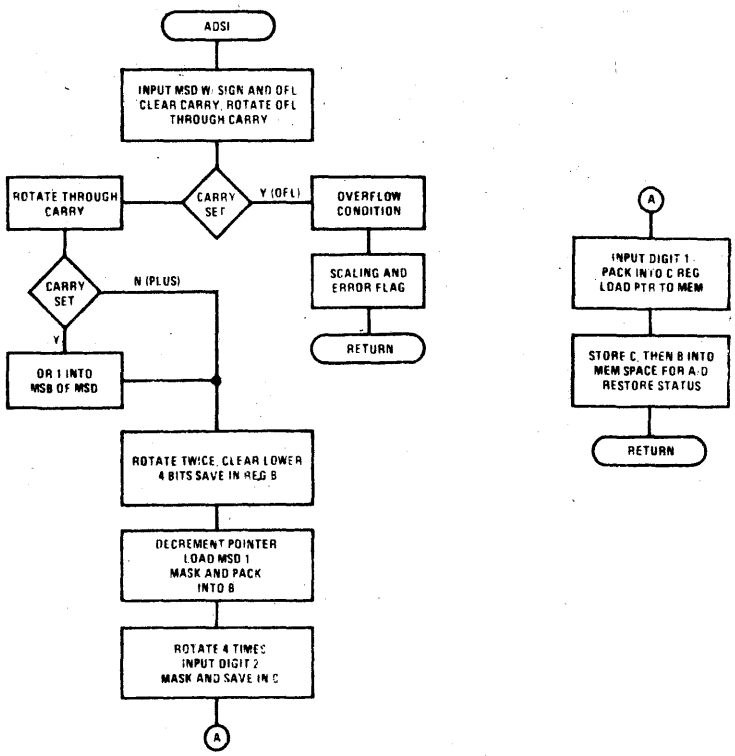


FIGURE 6. Flow Chart for Single Channel A/D Converter

```
LABEL   OPCODE   OPERAND   COMMENT
ADIS:   PUSH     PSW       ; A/D interrupt
                           service
        PUSH     H         ; save
        PUSH     B         ; current status
        IN       ADD 4     ; input A/D digit 4
        IN       ADD 4     ; delay
        ORA                ; reset carry
        RAL                ; rotate OFL thru
                           carry
        JC       OFL       ; overflow condition
        RAL                ; rotate sign thru
                           carry
        JC       PLUS      ; positive input
        ORI      20H       ; OR 1 into MSB,
                           neg input
PLUS:   RAL                ; shift
        RAL                ; into position
        ANI      FO        ; mask lower bits
        MOV      BA        ; save in B
        IN       ADD 3     ; input digit 3
        IN       ADD 3     ; delay
        ANI      OF        ; mask higher bits
        OR       B         ; pack into B
        MOV      B, A      ; save in B
        IN       ADD 2     ; input digit 2
        IN       ADD 2     ; delay
        RAL                ; rotate
        RAL                ; into
        RAL                ; upper
        RAL                ; 4 bits
        ANI      FO        ; mask lower bits
        MOV      C, A      ; save in C
        IN       ADD 1     ; in digit 1
        IN       ADD 1     ; delay
        ANI      OF        ; mask upper bits
        OR       C         ; pack
        MOV      C, A      ; save in C
        LXI      H, ADMS   ; load ptr to A/D
                           Mem, space
        MOV      M, C      ; save C in memory
        INX      H         ; point next
        MOV      M, B      ; save B in memory
        OUT      ADD 1     ; start new conver-
                           sion
        POP      B         ; restore
        POP      H         ; previous
        POP      PSW       ; status
        EI                 ; enable interrupts
        RET                ; return to main
                           program
```

Routine 1. Single Channel Interrupt Service Routine

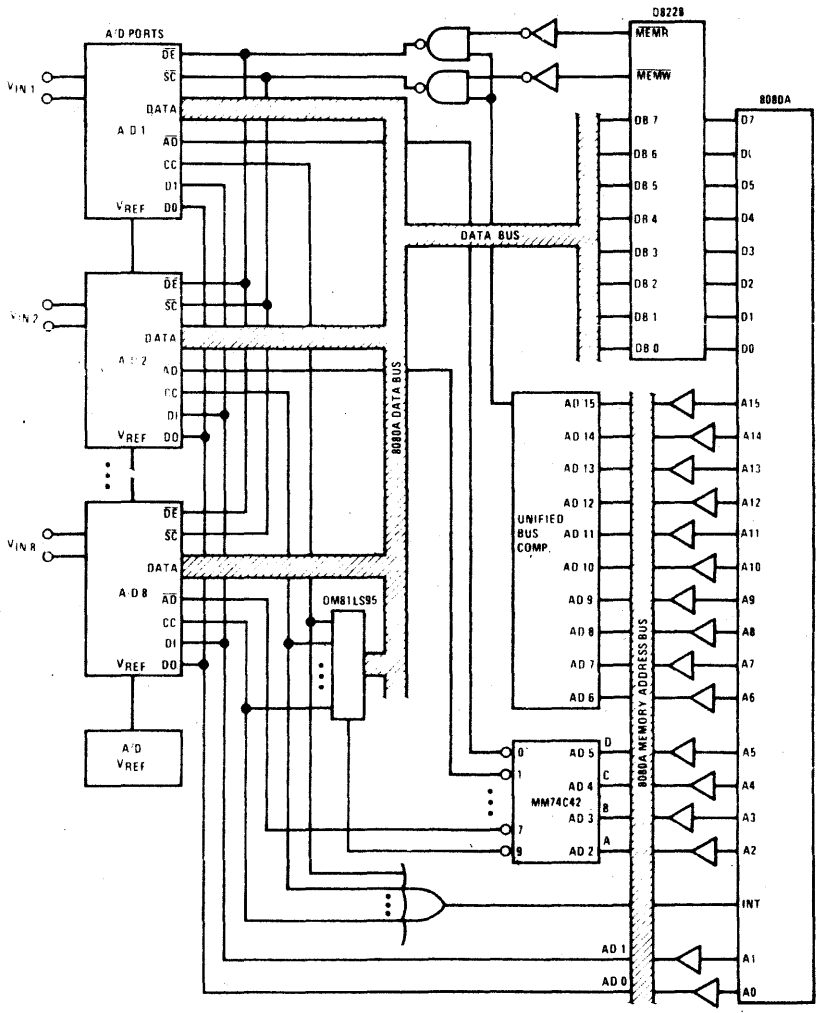


FIGURE 7. 8-Channel A/D System with Maskable Priority Interrupt Using Memory Mapped I/O

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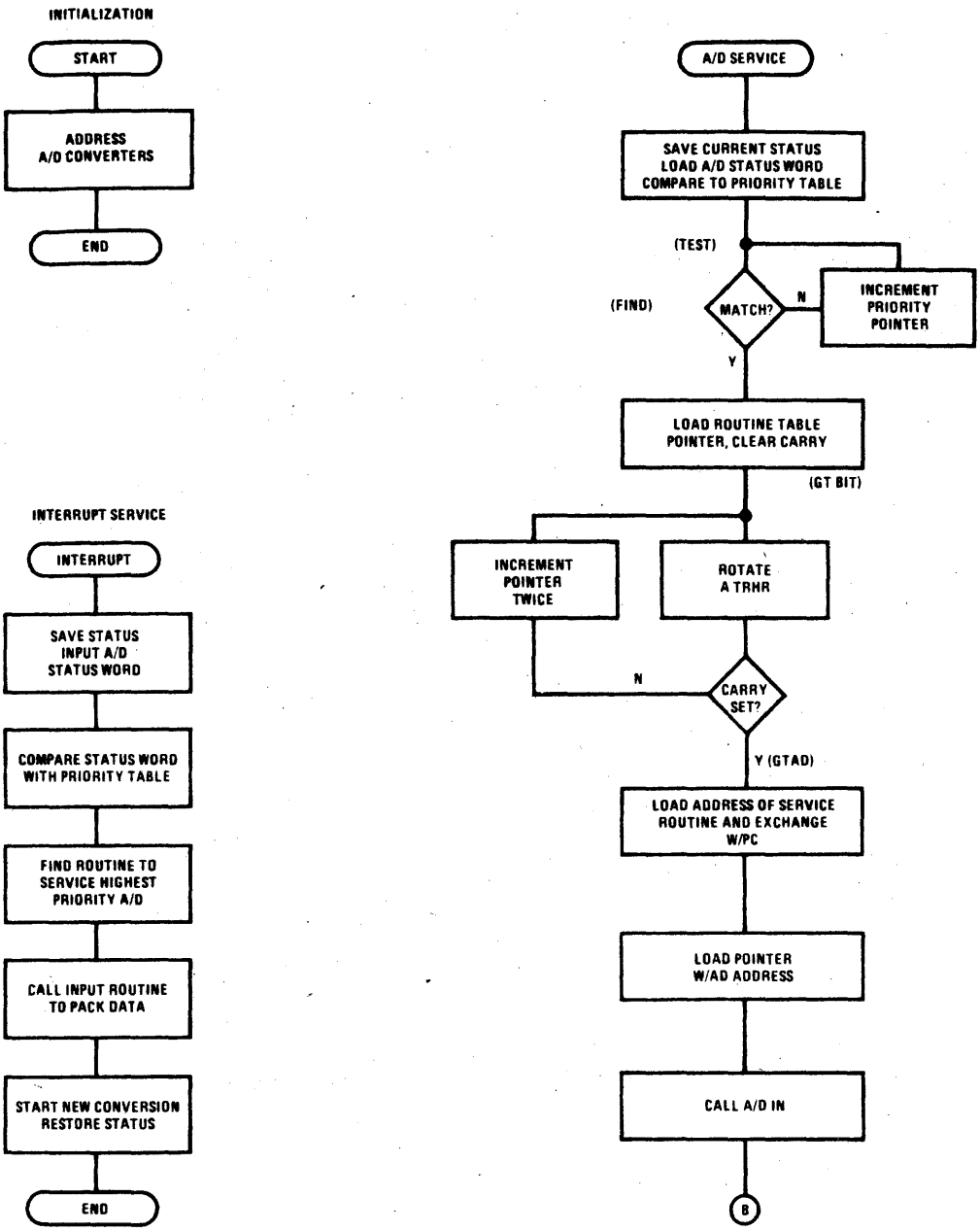


FIGURE 8. Flow Charts of A/D Routines

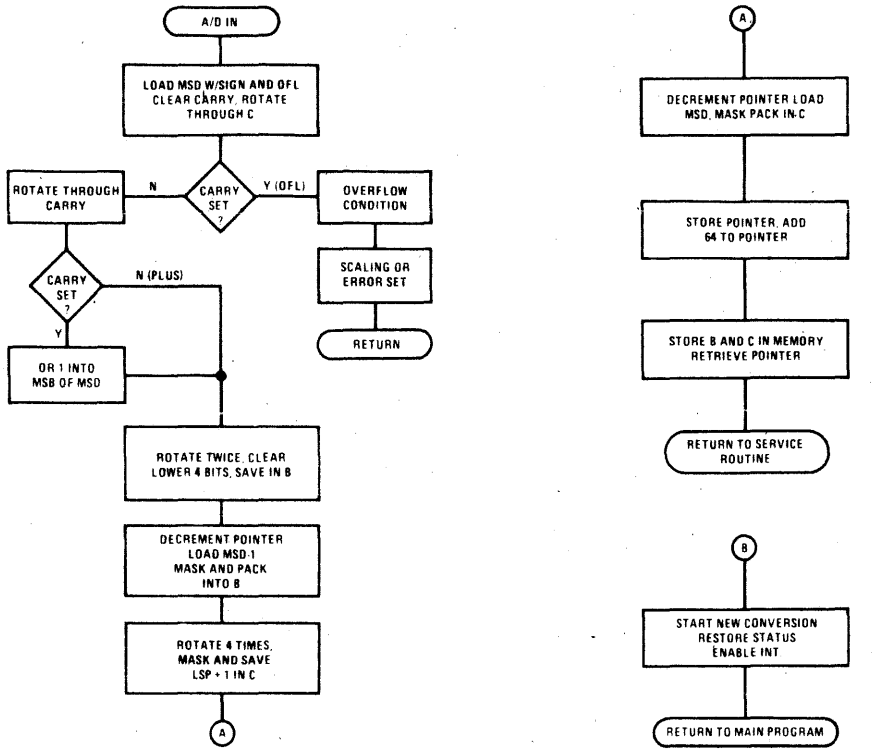


FIGURE 8. Flow Charts of A/D Routines (Continued)

LABEL	OPCODE	OPERAND	COMMENT
IAD:	PUSH	PSW	; interrupt from A/D
	PUSH	H	; save H & L on stack
	PUSH	B	; save B & C on stack
	PUSH	D	; save D & E on stack
	LXI	H, ADWD	; pickup A/D status word
	MOV	6, M	; move word into B
	LXI	H, PRTBL	; pickup priority tbl pointer
TEST:	MOV	A, B	; place status word in accum.
	ANA	M	; mask with priority table
	JNZ	FIND	; match jump to Find
	INX	H	; point to lower priority
	JMP	TEST	; try again
FIND:	LXI	H, RTBL	; pickup routine tbl pointer
	ORA	A	; reset carry
GTBIT:	RAR		; rotate thru carry
	JC	GTAD	; bit was found
	INX	H	; point to
	INX	H	; next routine
	JMP	GTBIT	; try again
GTAD:	MOV	E, M	; move first byte into E
	INX	H	; point to next byte
	MOV	D, M	; move second byte into D
	XCGH		; exchange DE, HL
	PCHL		; jump to input routine
INAD1:	LXI	H, AD1	; pickup pointer to A/D 1
	CALL	ADIN	; call common input routine
	MOV	M, A	; start new conversion
	JMP	DONE	; all done
INAD2:	LXI	H, AD2	; pickup pointer to A/D 2
	CALL	ADIN	; call input routine
	MOV	M, A	; start new conversion
	JMP	DONE	; all done
DONE:	POP	D	; restore D
	POP	B	; restore B
	POP	H	; restore H
	POP	PSW	; restore PSW
	EI		; enable-interrupts
	RET		; return to main program
PRTBL:	DB	04H	; 0000C100 AD3 highest priority
	DB	03H	; 00000011 AD2 & AD1 next priority

Routine 2. 8-Channel Interrupt Service Routine with Software Priority

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```
LABEL   OPCODE  OPERAND   COMMENT
PRTBL:  DB      10H       ;00010000 AD5 lowest priority
RTBL:   DW      1000H     ;routine for A/D 1
        DW      100CH     ;routine for A/D 2
        .
        .
        .
        DW      1060H     ;routine for A/D 8
ADIN:   MOV     A, M      ;input MSD plus OFL & SIGN
        MOV     A, M      ;delay
        ORA     A         ;reset carry
        RAL               ;rotate left thru carry, OFL
        JC      OFL       ;jump to overflow if set
        RAL               ;rotate left thru carry, sign
        JC      PLUS      ;jump to plus if set
        OR1     20H       ;OR1 into BCD, MSB for minus
PLUS:   RAL
        RAL
        ANI     FO        ;mask lower order bits
        MOV     B, A      ;save in B
        DCR     H         ;point to MSD-1
        MOV     A, M      ;input MSD-1
        MOV     A, M      ;delay
        ANI     OF        ;mask higher 4 bits
        OR      B         ;pack MSD and MSD-1
        MOV     B, A      ;save in B
        DCR     H         ;point to LSD + 1
        MOV     A, M      ;input LSD + 1
        MOV     A, M      ;delay
        RAL               ;rotate
        RAL               ;into
        RAL               ;upper
        RAL               ;4 bits
        ANI     FO        ;mask lower bits
        MOV     C, A      ;save in C
        DCR     H         ;point to LSD
        MOV     A, M      ;input LSD
        MOV     A, M      ;delay
        ANI     OF        ;mask upper bits
        OR      C         ;pack
        MOV     C, A      ;save in C
        SHLD    TEMP      ;store HL in temp
        MOV     A, L      ;move L in accum.
        ACI     64        ;generate lower address
        MOV     L, A      ;above memory mapped
        MOV     A, H      ;converter addresses
        ACI     0         ;include carry
        MOV     H, A      ;to upper bits
        MOV     M, C      ;store C
        INX     H         ;then
        MOV     M, B      ;store B
        LHLD    TEMP      ;retrieve HL
        RET               ;return
```

Routine 2. 8-Channel Interrupt Service Routine with Software Priority (Continued)

ADJUSTMENT AND TESTING

Adjustment and testing of a single channel A/D is done by monitoring the memory space where the interrupt routine stores the data word. The microprocessor is forced to loop around a section of program with interrupts enabled. As the input voltage of the converter is changed, this data word should also change as the converter updates it. A precision voltage reference is connected to the input of the A/D and incremental voltage steps are applied. The A/D data word should also change according to the voltage steps.

At full-scale input voltage, the data word should be at its maximum value. If not, check the full-scale adjust on the A/D by adjusting it so the OFL bit goes high when the input is exactly 2.000V.

Multichannel systems are more difficult to check. Start by individually checking the full-scale adjustments so the converters overflow at 2.000V. Check the software priority routine by forcing all status bits of the status word high. This corresponds to all converters being ready at the same time, a very unlikely worst-case condition. The microprocessor should respond by outputting the address of all 4 digits of the A/D port with the highest priority along with the $\overline{\text{memR}}$ strobes, then with a $\overline{\text{memW}}$ strobe to start a new conversion. The next highest priority converter should then receive its addresses and $\overline{\text{memR}}$ strobes and so on down the line.

Once the priority routine has been debugged, each data word is monitored as the input to its converter is adjusted. Since a common input routine is used, once 1 channel operates, all the other channels should also.

Debugging may most easily be done by single stepping through the program at these critical areas. No timing problems should be encountered since the A/D port appears to be a standard peripheral or memory. In the ADC3511 and ADC3711 the desired output is merely addressed the same as a memory location.

The memory requirements of the interface depends, of course, on the complexity of the system. The single channel converter requires approximately 60 bytes of program storage plus 2 bytes for data storage and 4 peripheral addresses.

The multichannel system requires about 40 bytes for the priority routine and 10 bytes of program for each converter routine. The common input routine requires about 50 bytes of program and is used by all the converter routines in the form of a subroutine.

Memory mapped I/O causes 64 memory locations to be used to input an 8-channel system. The data space is located directly above the address space for the converters and 16 memory locations are used to store the data for 8 converters.

CONCLUSION

The ADC3511 and ADC3711 microprocessor compatible A/D converters eliminate the difficulties previously encountered in applying DPM chips to microprocessor systems. The low parts count and low cost per channel make distributed or remote A/D conversion practical for a variety of data acquisition applications.

APPENDIX A

THEORY OF OPERATION

A schematic for the analog loop is shown in *Figure A1*. The output of SW 1 is either at V_{REF} or 0V, depending on the state of the D flip-flop. If Q is at a high level, $V_{OUT} = V_{REF}$ and if Q is at a low level $V_{OUT} = 0V$. This voltage is then applied to the low pass filter comprised of R1 and C1. The output of this filter, V_{FB}, is connected to the negative input of the comparator, where it is compared to the analog input voltage, V_{IN}. The output of the comparator is connected to the D input of the D flip-flop. Information is then transferred from the D input to the Q and $\overline{Q}$ outputs on the positive edge of clock. This loop forms an oscillator whose duty cycle is precisely related to the analog input voltage, V_{IN}.

An example will demonstrate this relationship. Assume the input voltage is equal to 0.500V. If the Q output of the D flip-flop is high, then V_{OUT} will equal V_{REF} (2.000V) and V_{FB} will charge toward 2V with a time constant equal to R1C1. At some time V_{FB} will exceed 0.500V and the comparator output will switch to 0V. At the next clock rising edge, the Q output of the D flip-flop will switch to ground, causing V_{OUT} to switch to 0V. At this time, V_{FB} will start discharging toward 0V with a time constant R1C1. When V_{FB} is less than 0.5V, the comparator output will switch high. On the rising edge of the next clock, the Q output of the D flip-flop will switch high and the process will repeat. There exists at the output of SW 1 a square wave pulse train with positive amplitude V_{REF} and negative amplitude 0V.

The DC value of this pulse train is:

$$V_{OUT} = V_{REF} \frac{t_{ON}}{t_{ON} + t_{OFF}} = V_{REF} \text{ (duty cycle)}$$

The low pass filter will pass the DC value and then:

$$V_{FB} = V_{REF} \text{ (duty cycle)}$$

Since the closed loop system will always force V_{FB} to equal V_{IN}, we can then say that:

$$V_{IN} = V_{FB} = V_{REF} \text{ (duty cycle)}$$

or

$$\frac{V_{IN}}{V_{REF}} = \text{(duty cycle)}$$

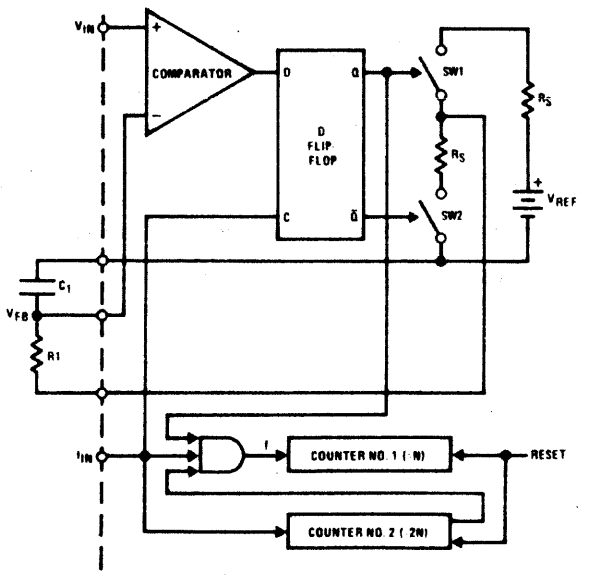
The duty cycle is logically ANDed with the input frequency f_{IN}. The resultant frequency f equals:

$$f = \text{(duty cycle)} \times (f_{IN})$$

Frequency f is accumulated by counter no. 1 for a time determined by counter no. 2. The count contained in counter no. 1 is then:

$$\text{count} = \frac{f}{(f_{IN})/N} = \frac{\text{(duty cycle)} \times (f_{IN})}{(f_{IN})/N} = \frac{V_{IN}}{V_{REF}} \times N$$

For the ADC3511 N = 2000.
For the ADC3711 N = 4000.



$V_{IN} = V_{FB} = V_{REF} \times \text{(duty cycle)}$

$f = \text{(duty cycle)} \times f_{IN}$

$$\text{Count in Counter No. 1} = \frac{f}{f_{IN}/N} = \frac{\text{(duty cycle)} \times f_{IN}}{f_{IN}/N} = \frac{V_{IN}}{V_{REF}} \times N$$

FIGURE A1. Analog Loop Schematic Pulse Modulation A/D Converter

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ELECTRICAL CHARACTERISTICS

ADC3511CC, ADC3711CC $4.75 \leq V_{CC} \leq 5.25V$; $-40°C \leq T_A + 85°C$, f_c = 5 conv./sec (ADC3511CC): 2.5 conv./sec (ADC3711CC); unless otherwise specified.

PARAMETER		CONDITIONS	MIN	TYP (Note 2)	MAX	UNITS
	Non-Linearity	(Note 3)				
		V_{IN} = 0–2V Full-Scale	−0.05	±0.025	0.05	% of Full-Scale
		V_{IN} = 0–200 mV Full-Scale				
	Organization Error		−1		0	Counts
	Offset Error	V_{IN} = 0V, (Note 4)	−0.5	1.0	3.0	mV
	Rollover Error		−0		0	Counts
V_{IN+}, V_{IN-}	Analog Input Current	T_A = 25°C	−5	1	5	nA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: All typicals are given for T_A = 25°C.

Note 3: For the ADC3511CC: full-scale = 1999 counts; therefore, 0.025% of full-scale = 1/2 counts and 0.05% of full-scale = 1 count. For the ADC3711CC: full-scale = 3999 counts; therefore, 0.025% of full-scale = 1 count and 0.05% of full-scale = 2 counts.

Note 4: For full-scale = 2.000V: 1 mV = 1 count for the ADC3511CC; 1 mV = 2 counts for the ADC3711CC.

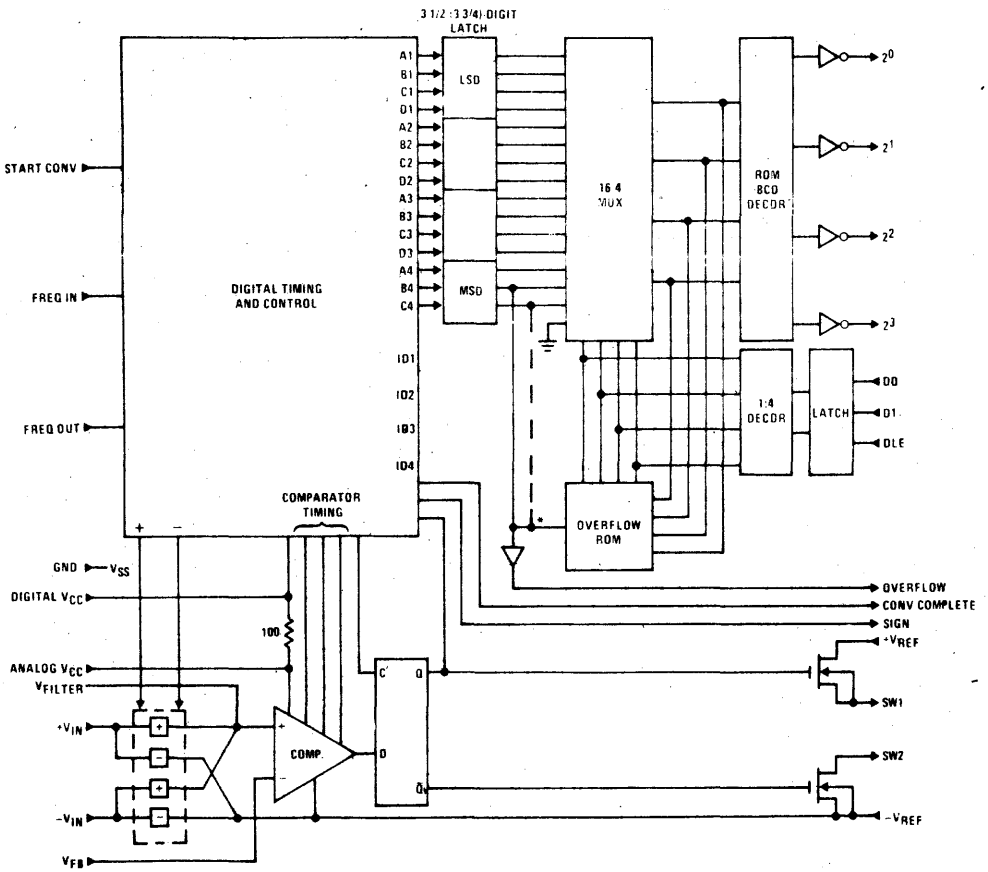


FIGURE A2. ADC3511 3 1/2-Digit A/D (*ADC3711 3 3/4-Digit A/D) Block Diagram

CMOS Schmitt Trigger —a Uniquely Versatile Design Component

National Semiconductor
Application Note 140
Gerald Buurma

INTRODUCTION

The Schmitt trigger has found many applications in numerous circuits, both analog and digital. The versatility of a TTL Schmitt is hampered by its narrow supply range, limited interface capability, low input impedance and unbalanced output characteristics. The Schmitt trigger could be built from discrete devices to satisfy a particular parameter, but this is a careful and sometimes time-consuming design.

The CMOS Schmitt trigger, which comes six to a package, uses CMOS characteristics to optimize design and advance into areas where TTL could not go. These areas include: interfacing with op amps and transmission lines, which operate from large split supplies, logic level conversion, linear operation, and special designs relying on a CMOS characteristic. The CMOS Schmitt trigger has the following advantages:

- High impedance input ($10^{12}\Omega$ typical)
- Balanced input and output characteristics
  - Thresholds are typically symmetrical to 1/2 V_{CC}
  - Outputs source and sink equal currents
  - Outputs drive to supply rails
- Positive and negative-going thresholds show low variation with respect to temperature
- Wide supply range (3–15V), split supplies possible
- Low power consumption, even during transitions
- High noise immunity, 0.70 V_{CC} typical

Applications demonstrating how each of these characteristics can become a design advantage will be given later in the application note.

ANALYZING THE CMOS SCHMITT

The input of the Schmitt trigger goes through a standard input protection and is tied to the gates of four stacked devices. The upper two are P-channel and the lower two are N-channel. Transistors P3 and N3 are operating in the source follower mode and introduce hysteresis by feeding back the output voltage, out', to two different points in the stack.

When the input is at 0V, transistors P1 and P2 are ON, and N1, N2 and P3 are OFF. Since out' is high, N3 is ON and acting as a source follower, the drain of N1, which is the source of N2, is at $V_{CC}-V_{TH}$. If the input voltage is ramped up to one threshold above ground transistor N1 begins to turn ON, N1 and N3 both being ON form a voltage divider network biasing the source of N2 at roughly half the supply. When the input is a threshold above 1/2 V_{CC}, N2 begins to turn ON and regenerative switching is about to take over. Any more voltage on the input causes out' to drop. When out' drops, the source of N3 follows its gate, which is out', the influence of N3 in the voltage divider with N1 rapidly diminishes, bringing out' down further yet. Meanwhile P3 has started to turn ON, its gate being brought low by the rapidly dropping out'. P3 turning ON brings the source of P2 low and turns P2 OFF. With P2 OFF, out' crashes down. The snapping action is due to greater than unity loop gain through the stack caused by positive feedback through the source follower transistors. When the input is brought low again an identical process occurs in the upper portion of the stack and the snapping action takes place when the lower threshold is reached.

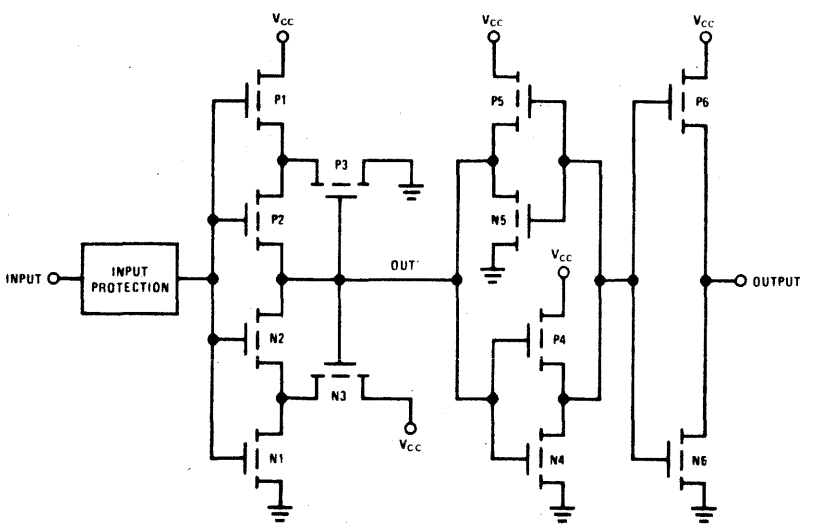


FIGURE 1. CMOS Schmitt Trigger

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Out' is fed into the inverter formed by P4 and N4; another inverter built with very small devices, P5 and N5, forms a latch which stabilizes out'. The output is an inverting buffer capable of sinking 360μA or two LPTTL loads.

The typical transfer characteristics are shown in *Figure 2*; the guaranteed trip point range is shown in *Figure 3*.

WHAT HYSTERESIS CAN DO FOR YOUR

Hysteresis is the difference in response due to the direction of input change. A noisy signal that traverses the threshold of a comparator can cause multiple transitions at the output, if the response time of the comparator is less than the time between spurious effects. A Schmitt trigger has two thresholds: any spurious effects must be greater than the threshold difference to cause multiple transitions. With a CMOS Schmitt at V_{CC} = 10V there is typically 3.6V of threshold difference, enough hysteresis to overcome almost any spurious signal on the input.

A comparator is often used to recover information sent down an unbalanced transmission line. The threshold of the comparator is placed at one half the signal amplitude (See *Figure 4b*). This is doen to prevent slicing level distortion. If a 4μs wide signal is sent down a transmission line a 4μs wide signal should be received or signal distortion occurs. If the comparator has a threshold above half the signal amplitude, then positive pulses sent are shorter and negative pulses are lengthened (See *Figure 4c*). This is called slicing level distortion. The Schmitt trigger does have a positive offset, V_{T+}, but it also has a negative offset V_{T-}. In CMOS these offsets are approximately symmetrical to half the signal level so a 4μs wide pulse sent is also recovered (see *Figure 4d*). The recovered pulse is delayed in time but the length is not changed, so noise immunity is achieved and signal distortion is not introduced because of threshold offsets.

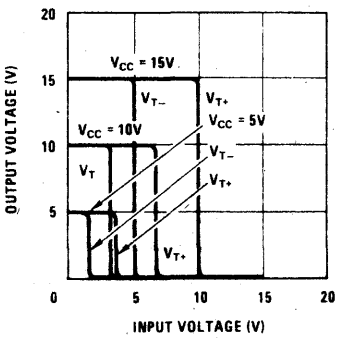


FIGURE 2. Typical CMOS Transfer Characteristics for Three Different Supply Voltages.

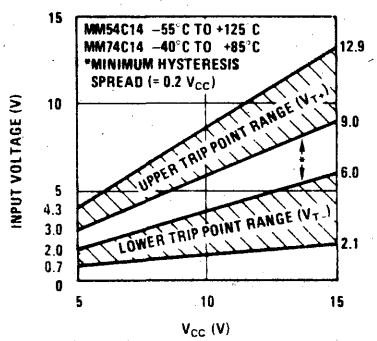


FIGURE 3. Guaranteed Trip Point Range.

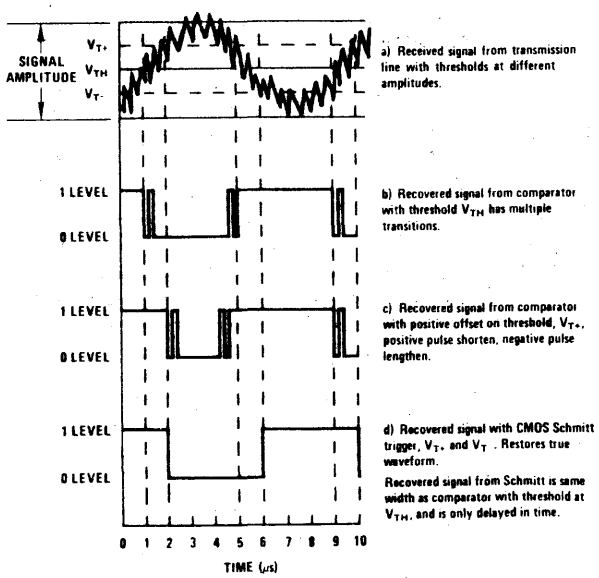


FIGURE 4. CMOS Schmitt Trigger Ignores Noise

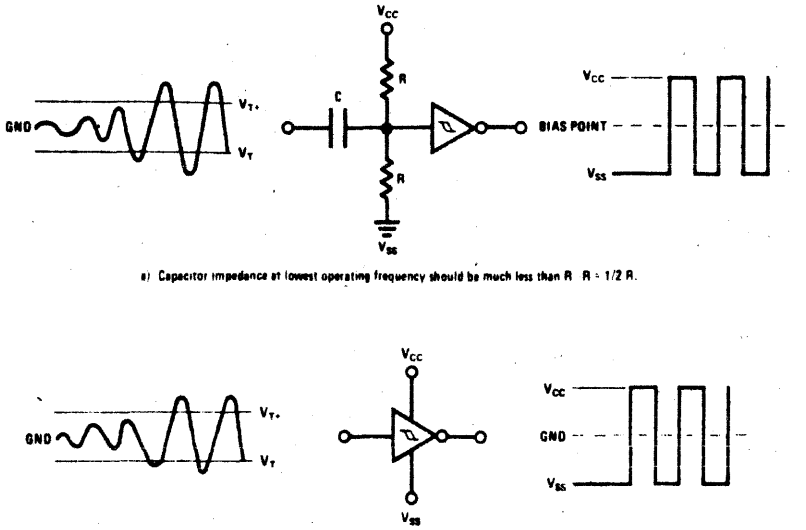


FIGURE 5. Sine to Square Wave Converter with Symmetrical Level Detection.

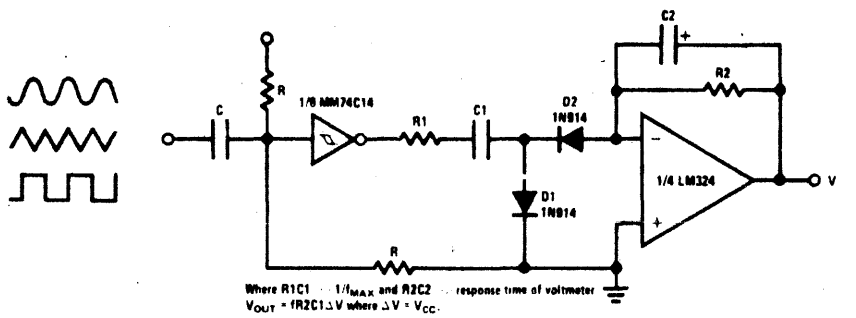


FIGURE 6. Diode Dump Tach Accepts any Input Waveform.

APPLICATIONS OF THE CMOS SCHMITT

Most of the following applications use a CMOS Schmitt characteristic to either simplify design or increase performance. Some of the applications could not be done at all with another logic family.

The circuit in *Figure 5a* is the familiar sine to square wave converter. Because of input symmetry the Schmitt trigger is easily biased to achieve a 50% duty cycle. The high input impedance simplifies the selection of the biasing resistors and coupling capacitor. Since CMOS has a wide supply range the Schmitt trigger could be powered from split supplies (see *Figure 5b*). This biases the mean threshold value around zero and makes direct coupling from an op amp output possible.

In *Figure 4*, we see a frequency to voltage converter that accepts many waveforms with no change in output voltage. Although the energy in the waveforms are quite different, it is only the frequency that determines the output voltage. Since the output of the CMOS Schmitt pulls completely to the supply rails, a constant voltage swing across capacitor C1 causes a current to flow through the capacitor, dependent only on frequency. On positive output swings, the current is dumped to ground through D1. On negative output swings, current is pulled from the inverting op amp node through D2 and transformed into an average voltage by R2 and C2.

Since the CMOS Schmitt pulls completely to the supply rails the voltage change across the capacitor is just the supply voltage.

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Schmitt triggers are often used to generate fast transitions when a slowly varying function exceeds a predetermined level. In *Figure 7*, we see a typical circuit, a light activated switch. The high impedance input of the CMOS Schmitt trigger makes biasing very easy. Most photo cells are several kΩ brightly illuminated and a couple MΩ dark. Since CMOS has a $10^{12}\Omega$ typical input impedance, no effects are felt on the input when the output changes. The selection of the biasing resistor is just the solution of a voltage divider equation.

A CMOS application note wouldn't be complete without a low power application. *Figure 8* shows a simple RC oscillator. With only six R's and C's and one Hex CMOS trigger, six low power oscillators can be built. The square wave output is approximately 50% duty cycle because of the balanced input and output characteristics of CMOS. The output frequency equation assumes that $t_1 = t_2 >> t_{pd0} + t_{pd1}$.

We earlier saw how the CMOS Schmitt increased noise immunity on an unbalanced transmission line. *Figure 9* shows an application for a balanced or differential transmission line. The circuit in *Figure 7a* is CMOS EXCLUSIVE OR, the MM74C86, which could also be built from inverters, and NAND gates. If unbalanced information is generated on the line by signal crosstalk or external noise sources, it is recognized as an error.

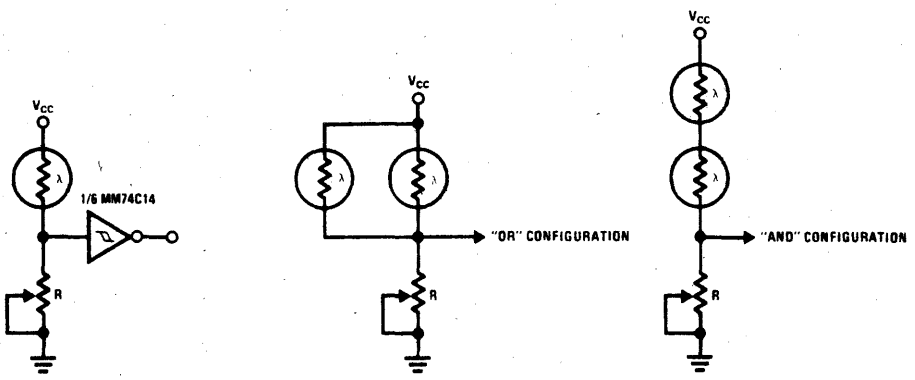


FIGURE 7. Light Activated Switch couldn't be Simpler. The Input Voltage Rises as Light Intensity Increases, when V_{T+} is Reached, the Output will go Low and Remain Low until the Intensity is Reduced Significantly.

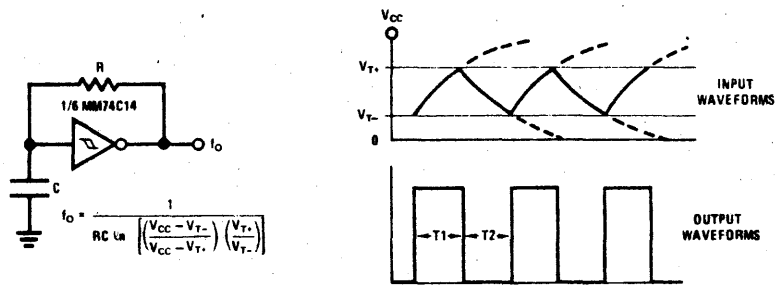


FIGURE 8. Simplest RC Oscillator? Six R's and C's make the CMOS Schmitt into Six Low Power Oscillators. Balanced Input and Output Characteristics give the Output Frequency a Typically 50% Duty Cycle.

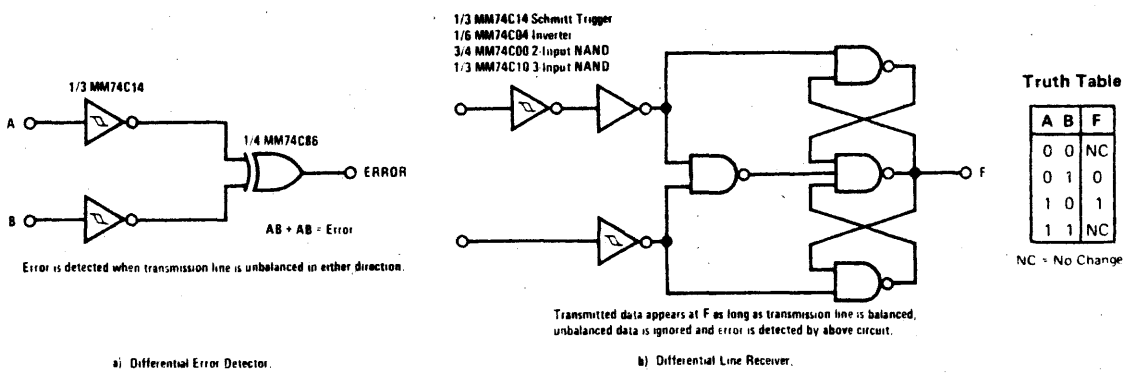


FIGURE 9. Increase Noise Immunity by using the CMOS Schmitt Trigger to Demodulate a Balanced Transmission Line.

The circuit in *Figure 9b* is a differential line receiver that recovers balanced transmitted data but ignores unbalanced signals by latching up. If both circuits of *Figure 9* were used together, the error detector could signal the transmitter to stop transmission and the line receiver would remember the last valid information bit when unbalanced signals persisted on the line. When balanced signals are restored, the receiver can pick up where it left off.

The standard voltage range for CMOS inputs is V_{CC} +0.3V and ground −0.3V. This is because the input protection network is diode clamped to the supply rails. Any input exceeding the supply rails either sources or sinks a large amount of current through these diodes. Many times an input voltage range exceeding this is desirable; for example, transmission lines often operate from ±12V and op amps from ±15V. A solution to this problem is found in the MM74C914. This new device has an uncommon input protection that allows the input signal to go to 25V above ground, and 25V below V_{CC}. This means that the Schmitt trigger in the sine to square wave converter, in *Figure 5b*, could be powered by ±1.5V supplies and still be directly compatible with an op amp powered by ±15V supplies.

A standard input protection circuit and the new input protection are shown in *Figure 10*. The diodes shown have a 35V breakdown. The input voltage can go positive until reverse biased D2 breaks down through forward bias D3, which is 35V above ground. The input voltage can go negative until reverse biased D1 breaks down through forward bias D2, which is 35V below V_{CC}. Adequate input protection against static charge is still maintained.

CMOS can be linear over a wide voltage range if proper consideration is paid to the biasing of the inputs. *Figure 11* shows a simple VCO made with a CMOS inverter, acting as an integrator, and a CMOS Schmitt, acting as a comparator with hysteresis. The inverter integrates the positive difference between its threshold and the input voltage V_{IN}. The inverter output ramps up until the positive threshold of the Schmitt trigger is reached. At that time, the Schmitt trigger output goes low, turning on the transistor through R_s and speeding up capacitor C_s. Hysteresis keeps the output low until the integrating capacitor C is discharged through R_D. Resistor R_D should be kept much smaller than RC to keep reset time negligible. The output frequency is given by

$$f_O = \frac{V_{TH} - V_{IN}}{(V_{T+} - V_{T-})\, R_{CC}}.$$

The frequency dependence with control voltage is given by the derivative with respect to V_{IN} So,

$$\frac{d\, f_O}{d\, V_{IN}} = \frac{-1}{(V_{T+} - V_{T-})\, RC},$$

where the minus sign indicates that the output frequency increases as the input is brought further below the inverter threshold. The maximum output frequency occurs when V_{IN} is at ground and the frequency will decrease as V_{IN} is raised up and will finally stop oscillating at the inverter threshold, approximately 0.55 V_{CC}.

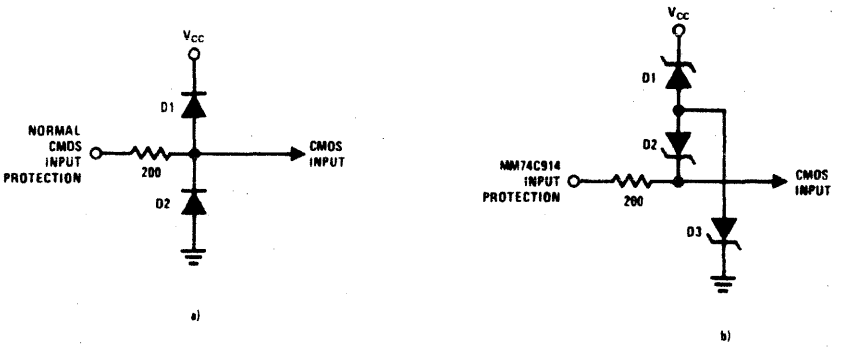


FIGURE 10. Input Protection Diodes, in a) Normally Limit the Input Voltage Swing to 0.3V above V_{CC} and 0.3V below Ground. In b) D2 or D1 is Reverse Biased Allowing Input Swings of 25V above Ground or 25V below V_{CC}.

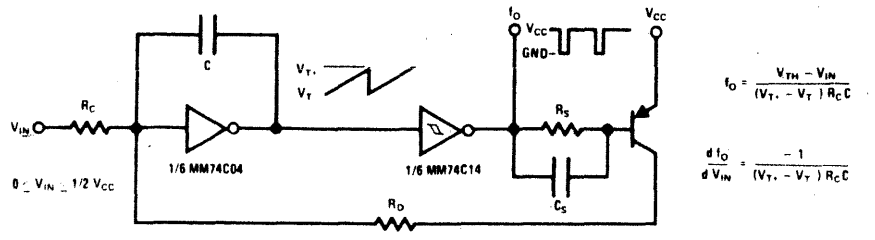


FIGURE 11. Linear CMOS (Voltage Controlled Oscillator)

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The pulses from the VCO output are quite narrow because the reset time is much smaller than the integration time. Pulse stretching comes quite naturally to a Schmitt trigger. A one-shot or pulse stretcher made with an inverter and Schmitt trigger is shown in *Figure 12*. A positive pulse coming into the inverter causes its output to go low, discharging the capacitor through the diode D1. The capacitor is rapidly discharged, so the Schmitt input is brought low and the output goes positive. Check the size of the capacitor to make sure that inverter can fully discharge the capacitor in the input pulse time, or

$$I_{SINK\ INVERTER} > \frac{C\,\Delta V}{\Delta T} + \frac{\Delta V}{R}$$

where $\Delta V = V_{CC}$ for CMOS, and ΔT is the input pulse width.

For very narrow pulses, under 100 ns, the capacitor can be omitted and a large resistor will charge up the CMOS gate capacitance just like a capacitor.

When the inverter input returns to zero, the blocking diode prevents the inverter from charging the capacitor and the resistor must charge it from its supply. When the input voltage of the Schmitt reaches V_{T+}, the Schmitt output will go low sometime after the input pulse has gone low.

THE SCHMITT SOLUTION

The Schmitt trigger, built from discrete parts, is a careful and sometimes time-consuming design. When introduced in integrated TTL, a few years ago, many circuit designers had renewed interest because it was a building block part. The input characteristics of TTL often make biasing of the trigger input difficult. The outputs don't source as much as they sink, so multivibrators don't have 50% duty cycle, and a limited supply range hampers interfacing with non 5V parts.

The CMOS Schmitt has a very high input impedance with thresholds approximately symmetrical to one half the supply. A high voltage input is available. The outputs sink and source equal currents and pull directly to the supply rails.

A wide threshold range, wide supply range, high noise immunity, low power consumption, and low board space make the CMOS Schmitt a uniquely versatile part.

Use the Schmitt trigger for signal conditioning, restoration of levels, discriminating noisy signals, level detecting with hysteresis, level conversion between logic families, and many other useful functions.

The CMOS Schmitt is one step closer to making design limited only by the imagination of the designer.

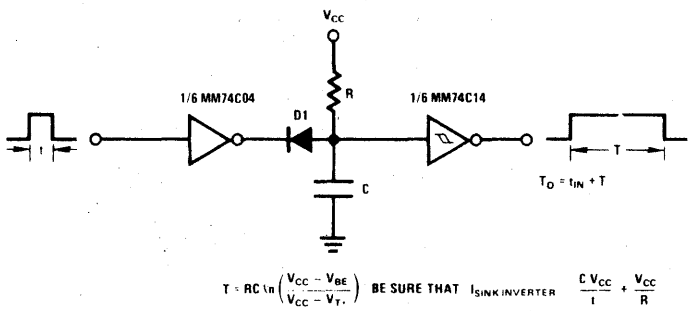


FIGURE 12. Pulse Stretcher. A CMOS Inverter Discharges a Capacitor, a Blocking Diode allows Charging through R only. Schmitt Trigger Output goes Low after the RC Delay.

Digital Weight Scales

National Semiconductor
Carson Chen
March 1978

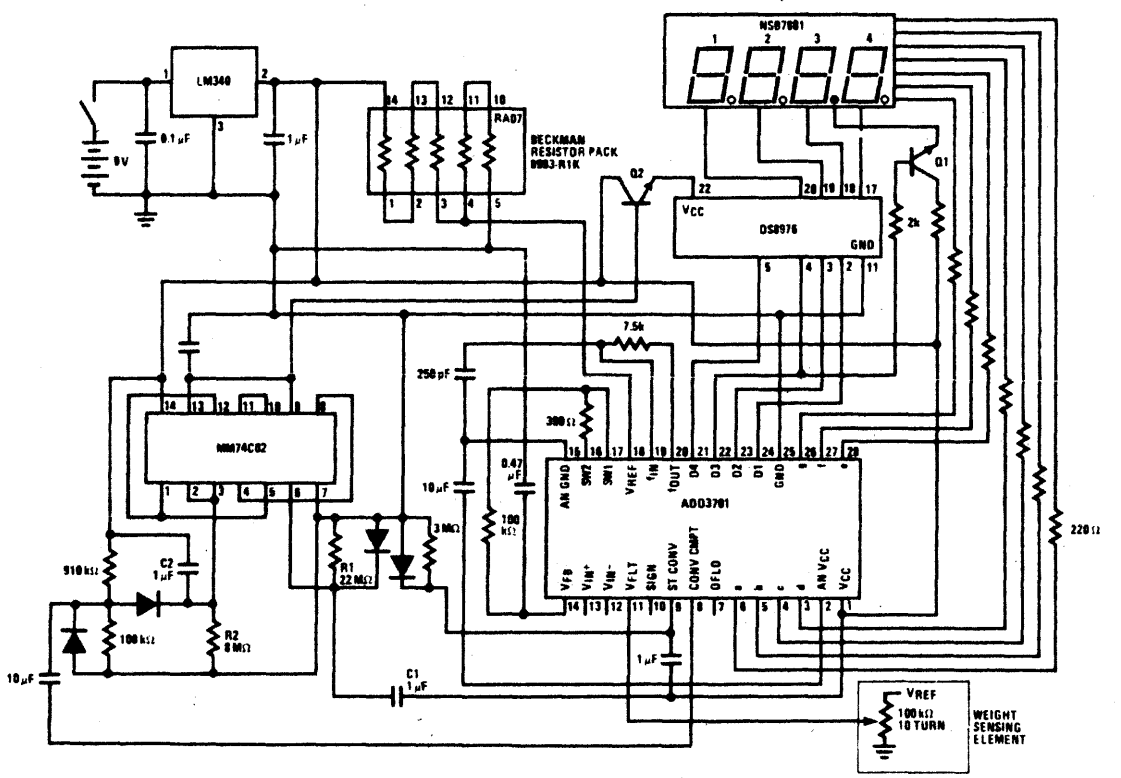
The application of digital systems to detect weight provides for low cost, accurate weight scales.

A developed system using the 3¾-digit DVM IC, ADD3701,* shown in figure 1, allows for conversion of an analog voltage to digital information linearly related to the weight being sensed.

Support circuitry for the DVM IC consists of a voltage regulator, a reference voltage, a weight sensing element, display drivers, and an LED display. Additional circuitry may be implemented for added features.

The weight scale circuit of figure 1 employs a potentiometer as the weight sensing element and functions as a variable voltage divider from ground to V_{REF}, 2 volts. An object placed upon the scale displaces the potentiometer wiper, which is connected to the scale mechanics, an amount proportional to its weight. Conversion of the wiper voltage to digital information is performed, decoded, and interfaced to the numeric display by the ADD3701. The LM340 regulates the V_{CC} supply voltage and the RA07 resistor array is connected as a voltage divider to generate the ADD3701 2V reference voltage. The NSB7881 is driven by the ADD3701 segment drivers and the DS8976 digit drivers.

*See ADD3701 data sheet for details of DVM operation.



Notes:

1. R1, C1 defines POWER ON display blanking interval. R2, C2 defines display ON time.
2. All V_{CC} connections should use a single V_{CC} point and all ground/analog ground connections should use a single ground/analog ground point.
3. Display sequence for Rev A ckt implementation:
   - t = 0 sec • power ON
   - t = 0 → 5 sec • display blanked • system converging
   - t = 5 → 10 sec • conversion complete • display ENABLE
   - t > 10 sec • display blanked • wait for new POWER UP cycle

Figure 1

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Q2, the MM74C02 and surrounding circuitry generate the display sequence explained in Note 3 of figure 1.

The ADD3701 3¾-digit DVM displays a maximum of 3999 counts, full scale, having a resolution of 500 μV per LSD.

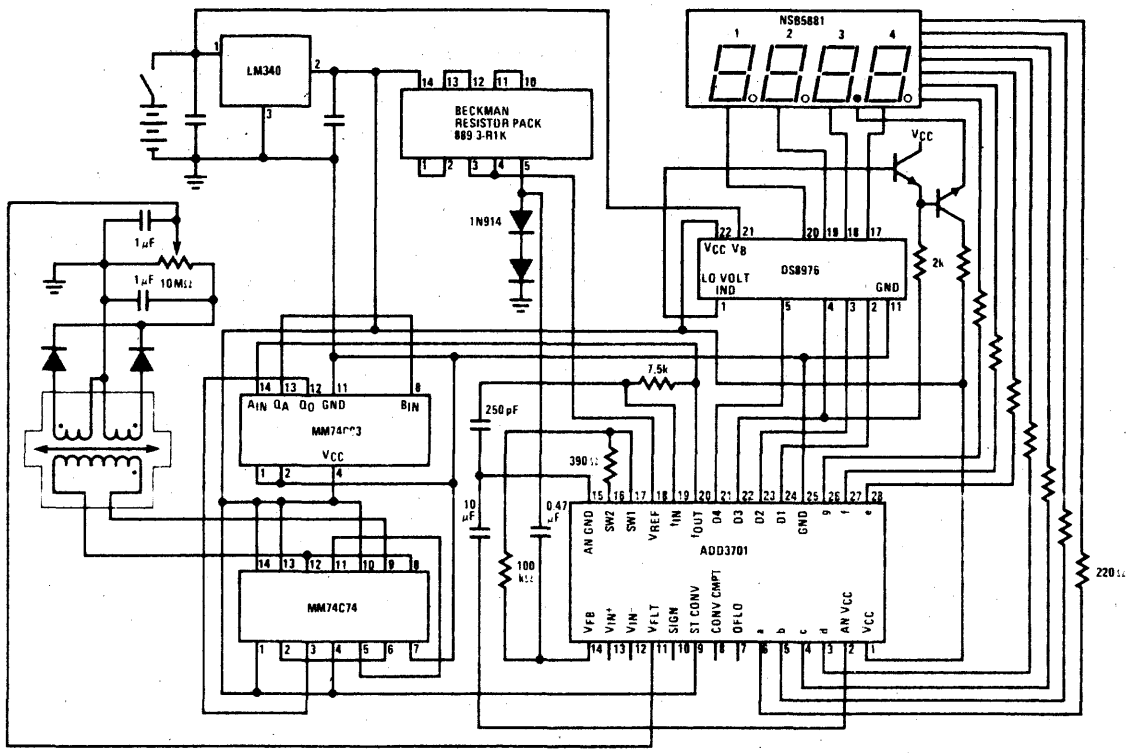
With the decimal point of digit 3 forced "ON" by Q1 the maximum displayed reading of figure 1 would equate to 399.9 units of weight.

Figure 2 is a weight scale sensor similar to that in figure 1, differing only in the weight sensing element and its related support circuitry.

The transformer of figure 2 is rectified to a DC voltage, proportional to a weight displacement, and then converted to its digital equivalent with the ADD3701.

The purpose of setting analog ground two diode drops above digital ground is to help cancel the inherent air coupling offset voltage generated by the transformer.

Figure 2 is also connected to display a maximum of 399.9 units of weight. The accuracy of both systems without the transducer elements is ±1 LSD at 25°C ± 15°C.



Notes:

1. Excitation to the LVDT (i.e., outputs of the MM74C93 and MM74C74) may be altered to compensate for the varying frequency ranges of LVDTs.
2. All V_{CC} connections should use a single V_{CC} point and all ground/analog ground connections should use a single ground/analog ground point.

Figure 2

Dynamic RAM Board Design Made Easy

National Semiconductor
Memory Application
Stephen Calebotta*
November 1977

INTRODUCTION

Many new memory system designs are being done with dynamic RAMs. This is especially true as the new 16k RAM chips become more readily available. This application note is aimed at those engineers who are doing their first dynamic RAM designs. Its intent is to give some direction in how to design a RAM board so that it will give the greatest production yield with the least amount of difficulty.

We shall not talk about specific RAMs or interface to a specific processor. Most engineers can design control and interface logic for RAMs and most board designers can lay out a PC board for that design. However, the quality of that design will become apparent only after the RAM board is built and phased into production. Does it come up easily? Does it go through testing with little or no RAM chip fallout? Is it reliable in the field?

The key to success in a dynamic RAM system, or any other system for that matter, is margin. A system designed to maximize power supply and timing margins will be reliable and easy to manufacture. One that doesn't will be a manufacturing and field service nightmare.

In this application note we shall discuss RAM chip characteristics, power supply and control signal distribution on PC boards, and control logic implementation suggestions. As successful examples, in the appendix we shall provide the schematics and foils for some memory boards that are in production.

RAM CHIP CHARACTERISTICS

For reference we shall compare dynamic and static RAMs at the chip level. Then we shall describe the unique characteristics of dynamic RAMs which must be considered in a memory system design.

Dynamic RAMs versus Static RAMs

The basic difference between dynamic and static RAMs is the way they store data. The static RAM uses a flip-flop to store a bit, while the dynamic RAM uses a capacitor to store a bit. (See figure 1.)

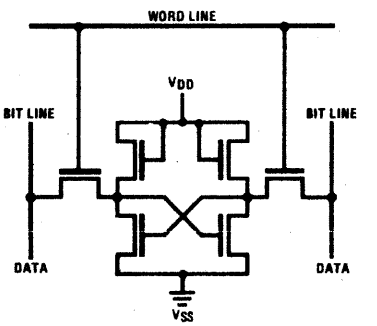
It is their respective cell designs that give each RAM its advantages over the other. Let's compare the RAMs for ease of use, power dissipation, die size, and price.

Ease of Use: The static RAM is easier to use because no refresh logic is required. In addition, static RAM control signals tend to be easier to generate because cycling is usually unnecessary.

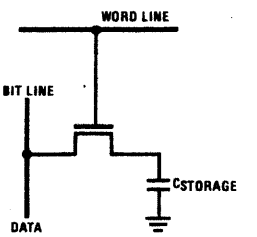
Power Dissipation: The dynamic RAM draws less power. The static RAM draws power continuously to sustain its flip-flops, while the dynamic RAM draws minimal power (1 to 2 mA) between cycles. With continuous cycling, the dynamic RAM draws about as much power as the static. However, in a large memory system, dynamic RAMs save total system power since only one bank of RAMs is ever accessed during a memory cycle. All other banks draw minimal current except during refresh cycles. The duty cycle for refresh is approximately 1½ to 3%.

Die Size: Dynamic RAMs tend to be smaller. Due to the difference in cell designs, the die size of the dynamic RAM is often at least 20% smaller than that of a comparable static RAM from the same manufacturer.

Price: Because of smaller die sizes and much larger production runs, dynamic RAMs should always remain considerably cheaper than comparable static RAMs. In addition, dynamic RAMs save money in larger systems. Less chip power means smaller and cheaper power supplies. Smaller supplies mean a further saving in reduced cooling requirements. In general, the larger the memory system, the greater the savings by using dynamics.



Static RAM Cell



Dynamic RAM Cell

Figure 1.

Dynamic RAMs

Refresh: Since charge leaks off the storage capacitors, it must be replenished periodically in order for a dynamic RAM chip to retain its data. The charge in any one cell is replenished, or refreshed, every time that cell is accessed for a read or a write. At the same time, all the other cells in the same row are also refreshed. For that reason the entire RAM chip can be refreshed by doing only 64 cycles (for 4k RAM; a 16k RAM needs 128

*Refer to Introduction.

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cycles) in 2 ms while sequencing through all the row addresses. The bit pattern presented to the column addresses does not matter. However, the setup and hold times must still be met. Unstable column addresses during refresh will cause data loss.

The hardware required for refresh amounts to a 6- or 7-bit counter for the refresh addresses, some way to multiplex the counter onto the RAM row address lines, a timer to signal when a refresh should be done, and the miscellaneous gating needed to couple into the usual read/write logic.

In some systems no extra refresh logic is needed. For example, in CRT systems normal operation sequences through all the row addresses in less than a 2 ms refresh period. This will be true only if the row address bits on the RAM chip are driven from the least significant address bits of the system. As a rule, this is good practice in all systems. By placing the most active system address bits on the RAM row addresses, normal system operation will automatically refresh the bulk of the RAM.

Cycling: One of the key functional differences between static and dynamic RAMs is the fact that dynamic RAMs must run through a cycle in order to read or write. Aborting the cycle by removing the chip enable too early or by trying to start a second cycle too soon after the first will probably cause data loss. Minimum chip enable on and off times must be observed.

Summary

Static RAMs are easier to use. Dynamic RAMs are cheaper, use less power, must be refreshed, and must be cycled.

MEMORY SUBSYSTEM DESIGN CONSIDERATIONS

Some memory board designs are easy to manufacture, while others, functionally identical, have low manufacturing yields seemingly due to the many "bad" chips. The difference between them is usually the amount of margin designed into each system. Power supply and timing margins are both critical, and as the margins go to zero or negative, the amount of "soft" errors goes up. (A chip has a "hard" error if a location consistently cannot be written and read back properly. It has a "soft" error if it only occasionally fails.)

On careful analysis, "soft" errors usually occur during a memory cycle in which some system parameter has gone out of spec. Since the RAM chips themselves have variations in their margins, replacing the offending RAM with one that has a greater margin in the out-of-spec parameter seems to cure the problem. This results in a large pile of "bad" RAMs. However, the real solution to this type of problem is in a careful system design and board layout in the beginning.

Power Distribution

By far the single most important aspect of a successful RAM system is good power distribution consisting of carefully designed decoupling and power gridding. The importance of good power distribution cannot be overemphasized.

Let's examine the problem. All dynamic RAMs have at least two supplies (V_{DD} and V_{BB}; V_{SS} is the RAM internal ground). Most also have a third called V_{CC}. We will discuss only V_{DD} since the other supplies have similar characteristics. Figure 2 shows the I_{DD} current waveform for a typical dynamic RAM chip during a memory cycle.

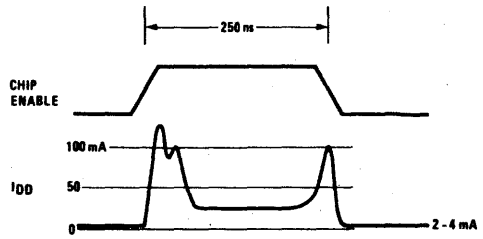


Figure 2.

At the beginning and end of chip enable, each RAM chip draws 50 to 100 mA current spikes with rise times of 20 ns. In addition, each RAM package draws a 20 to 40 mA DC current lasting for the duration of chip enable. The power distribution system must supply these currents while the voltages at the RAMs remain constant. Figure 3 is a schematic of the V_{DD} supply for a row of eight RAMs. The inductors are due to PC trace inductance which is about 10 nH per inch for a 13 mil trace. If the RAMs are on ½-inch centers there is 10 nH total between RAMs.

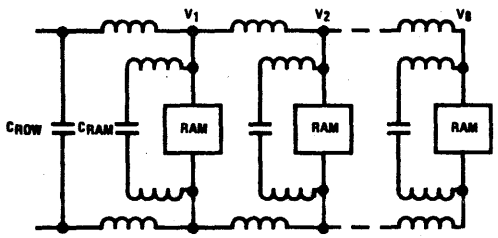


Figure 3.

If there is only one capacitor per row, and if that row capacitor, C_{row}, were infinite, the voltage spikes at the first, second, and last RAMs would be:

$$V_1 \text{ spike} = L \times 8\frac{di}{dt} = 10\,nH \times 8 \times \frac{100\,mA}{20\,ns}$$

$$= 400\,mV$$

$$V_2 \text{ spike} = L \times 15\frac{di}{dt} = 750\,mV$$

$$V_8 \text{ spike} = L \times 36\frac{di}{dt} = 1800\,mV$$

These spikes, especially the last two, are unacceptable.

If each RAM had its own decoupling capacitor, C_{RAM}, in series with 10 nH of trace inductance, the voltage spikes would be:

$$V_{spike} = L\frac{di}{dt} = 10\,nH \times \frac{100\,mA}{20\,ns} = 50\,mV$$

which is very good. Local decoupling should be used to overcome the spiking problem.

The ability of the power distribution system to supply the 20 to 40 mA per chip during a RAM cycle is also a function of the series inductance. For example, see figure 4.

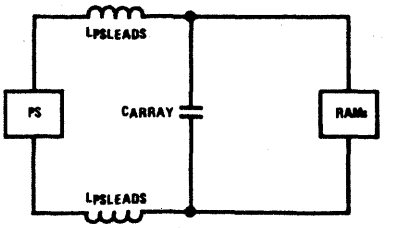


Figure 4.

Let the total power supply lead inductance be 50 nH. (We are ignoring the PC trace inductance within the RAM array itself.) What would the voltage step have to be at the RAMs to get 40 mA x 8 flowing in 20 ns? The equation is:

$$E = L\frac{di}{dt} = 50\,nH \times 8 \times \frac{40\,mA}{20\,ns} = 800\,mV$$

which is a large step which should not occur with adequately designed decoupling. Therefore, the bulk of the DC current for cycling the RAMs comes from decoupling caps themselves, and therefore they should be large enough to supply these currents with little droop. They should also be close enough to the RAMs to minimize the effect of the spikes. If we use a 0.1 μF cap, the droop for a 250 ns cycle would be:

$$V_{droop} = V = \frac{I}{C}t = \frac{40\,mA}{0.1\,\mu F} \times 250\,ns = 100\,mV$$

which is acceptable. Obviously, a larger capacitor will do an even better job of handling the droop. In addition, to help keep the droop to a minimum, the board should have about 50 to 200 μF of bulk decoupling on the +12 V supply. The other supplies can have less. Half should be placed near the point where the supplies enter the board. The other half should be placed at the far side of the RAMs so that the array lies between the bulk decoupling capacitors.

Alternatively, half of the bulk capacitors can be spread throughout the array. If this is done, use approximately 5 to 10 μF per eight RAM chips for V_{DD} and V_{BB}. For V_{CC}, 5 to 10 μF for 32 chips should be adequate.

Intuitively, this second approach seems better. However, the first technique works fine and is probably more cost effective.

The choice of capacitor types is very important. In all of the above decoupling calculations we have ignored the effective series resistance (ESR) of the capacitors. The effect of the ESR of real capacitors is probably at least as large as the effect of PC trace inductance and is a function of the capacitor type.

For best results, use ceramic capacitors for the local decoupling. The Memory Systems Group at National Semiconductor has had good results with ceramic capacitors of Z5U material from AVX and Sprague. To illustrate how important the Memory Systems Group feels these capacitors are to good memory board performance, every lot is subjected to an incoming inspection which includes, among other things, a transient response test.

For bulk decoupling, solid tantalum capacitors are recommended. They have better transient response than most other large value capacitors and they put a lot of capacitance into a small package which simplifies board layout.

A word about power gridding. If there are a number of rows of RAMs, all power supply traces to all RAMs should be run both vertically and horizontally throughout the array. Providing multiple paths through the array reduces the effective inductance of the power distribution system.

To summarize power distribution, we can say the following:

1. It is the single most important aspect of a good RAM board layout.
2. Use plenty of decoupling. The decoupling caps not only reduce voltage spikes, but also provide most of the RAM power during the cycling. Lay out the board for a 0.1 μF capacitor per power supply per RAM chip (up to three capacitors per chip). As production history accumulates, it may be possible to omit half the capacitors. However, lay out the board for one per supply per chip. Use 50 to 200 μF of bulk decoupling on +12 V. On +5 V and -5 V use 25 to 100 μF.
3. The decoupling capacitors should have the shortest possible traces back to their respective RAM power supply and ground pins. To reduce inductance further, these traces should be as wide as room will allow.
4. Traces running the power supply voltages throughout the array should be as wide as possible. However, with good decoupling design, even minimum trace widths will probably be acceptable. If some power supply traces can be wider than others, make V_{SS} (Ground) wider first, V_{DD} next, V_{BB} next, and finally V_{CC}. Ground is the key. Grid the supplies even if the traces are heavy in one direction and light in the other.
5. We have purposely omitted any discussion of multilayer boards. They tend to simplify power distribution problems, but the types of problems that must be solved are the same. Only the magnitudes have been somewhat reduced. Almost everything that has been said up to now is still applicable to multilayer boards.

Data and Control Signal Distribution

The second most important aspect of the successful RAM system is address, data, and control signal distribution.

Let's discuss the chip enables first. This is the most important signal to the RAM and all timing is referenced to it. There are two types of chip enables in common use today: 12 volt and TTL level swings. Running chip enable lines through an array tends to be less of a problem than one would think. There are only two things to keep in mind. First, place the actual driver chip near the RAM array it is driving, making the chip enable run short and direct. Second, put a damping resistor near the driver. Do this for either TTL level or 12 volt chip enables. Select the value of this resistor to

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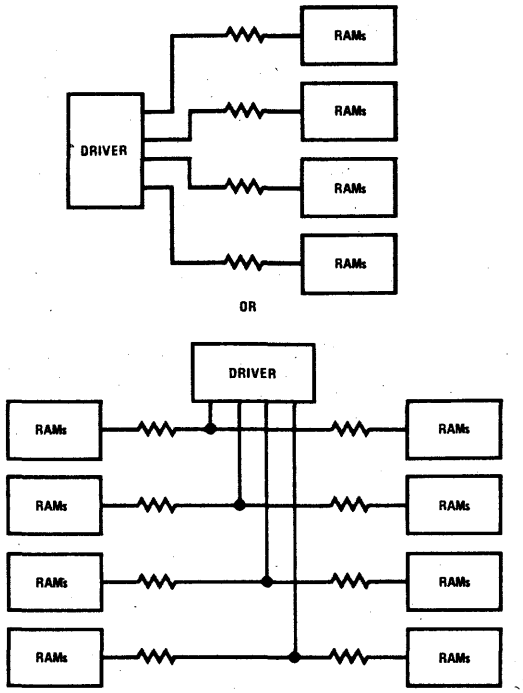


Figure 5.

give the best clock waveform at the RAM chips. Its value will probably be between 10 and 51 Ω. Figure 5 shows the commonly used arrangements.

The reasons for these two recommendations stem from the fact that, at the frequencies encountered here, the clock lines are, in fact, transmission lines. The impedance of the line is determined by:

$$Z_0 = \sqrt{L/C}$$

where the impedance of the clock line within the array of chips is in the range of 10 to 15 Ω while the unloaded line between the clock driver and the chip array is in the range of 30 to 50 Ω.

In order to drive the clock line cleanly, some attempt must be made to match the clock driver's output impedance to that of the line. The actual output impedance of most monolithic clock drivers varies as much as 3 to 1 and so we choose a fast clock driver with low output impedance and put a damping resistor in series to empirically set the effective output impedance to match the line (with only about 10% variation).

Long clock lines or long lengths of unloaded clock lines can cause problems. In the case of the long clock line, the open circuit at the far end of the line causes the reflection from the end of the line to return to the driver after the end of the rise time, resulting in ringing. In the case of the long unloaded length of line, the reflection from the junction of the unloaded and loaded sections of the line (due to the mismatch) causes glitches in the clock transitions.

To minimize crosstalk from chip enable to other signals, try to run chip enable at 90° to other signals. This is usually hard to do in an actual layout. As an alternative, leave as much room as possible between chip enable and adjacent traces as it runs through the array. Typically, signals in the array are on 50 mil centers. Moving the two adjacent signals more than 50 mils away from chip enable will help some in reducing crosstalk. However, as stated earlier, there seem to be very few problems associated with chip enable. Neither CE itself nor crosstalk to other signals will be troublesome if the above guidelines are observed.

Address, data, and control signals such as read/write (or equivalent) should be run as directly as possible. Their layouts tend to be non-critical. The critical thing is timing. The control logic should be designed to maximize setup and hold times with respect to chip enable. Again, high production yield is related to margins. As an example, consider a RAM board that was built for an 8080 system. The chip used was MM5271 4k RAM which has a low true TTL level clock input. The signal that controls read, write, and refresh is called TSP. The MM5271 data sheet says that the setup time for TSP is zero ns with respect to the leading edge of chip enable. When doing a refresh, TSP must be low at the beginning of chip enable. The original timing brought TSP down at the same time as chip enable. The system seemed to work. However, it would make an error once every half hour or so. With an oscilloscope everything appeared to be within specification. When TSP and chip enable were superimposed on the scope, their leading edges were absolutely coincident in both time and waveshape. The TSP/chip enable relationship was examined very, very carefully and pronounced okay. Finally, in an attempt to cure the problem, the TSP timing was changed to give about 50 ns of setup time and the problem disappeared.

The point was that the original design was done to the limit of the memory data sheet even though there was no need to do so. The success of the operation depended on the shape of the two waveforms to keep the system in spec. Once margin was designed in, with no hardship at all in the design, the system operated flawlessly.

In high-speed systems where it is hard to design in extra margin, use damping resistors in address, data, and control lines to help control their waveshapes. A resistor in every address, data, and control line allows these waveforms to be optimized, which gives the system improved margin over an undamped design. Use damping resistors only where necessary. Leave them out of signals that have time to settle down before they are needed.

Summarizing the use of damping resistors: always put them in chip enable lines, whether they are TTL levels or 12 V levels. Use them as necessary in those address, data, and control lines whose timings are approaching the limits of the RAM chip data sheet. Design in margin first. Tune it in when it can't be designed in.

LOGIC CONSIDERATIONS

These also affect yield. For example, a RAM cycle must never be aborted before its normal completion. The control logic must be designed to never permit a shortened cycle. At this point we shall briefly discuss some techniques for timing and control.

Timing Generation

The actual phasing of control signals can be done a number of ways. Existing system level control signals can be used. This is easy in some 8080 and PACE systems. When the available system control signals aren't quite up to the job, another technique that works

quite well is to use a high frequency oscillator and a shift register connected as a Johnson counter. Any timing signal that is necessary can be generated from a Johnson counter using a 2 input gate. This technique has a minor drawback if the high frequency oscillator is asynchronous with respect to the main system timing. The RAM cycle timing will always have a finite uncertainty with respect to the system cycle timing. This uncertainty is equal to the clock period of the high frequency oscillator. To apply the same technique but to avoid the timing uncertainty, use a gated delay line oscillator instead of a crystal or RC oscillator. Delay line oscillators can be started and stopped reliably. Crystal and RC oscillators take a few cycles to settle down and therefore are not reliable in a start-stop mode. How about one-shots? Do not, under any circumstances, use one-shots in critical timing applications!

Refresh Timeouts

A counter and oscillator are best. An astable oscillator is acceptable but must be carefully designed for worst case minimum frequency with respect to temperature to ensure the RAM gets refreshed often enough. At the end of the timeout a flip-flop should be set. When the refresh cycle is finally completed, that flip-flop should be reset. The timing should be such that it doesn't matter when the RAM gets refreshed within the refresh timer period.

Transparent versus Non-Transparent Refresh

Most microprocessors have predictable periods of time when they will not access the RAM board. Usually it takes little effort to insert refresh cycles in these times, thereby making refresh transparent to the CPU. When the CPU is very fast and is using the bus almost continuously, the refresh will have to hold up the processor. Even then, some clever design will minimize the time spent doing non-transparent refresh.

Single Step

Some systems need the capability of single stepping through programs. Since dynamic RAMs must be refreshed continuously, the output data from RAM should be latched. This permits single stepping because every time the address changes, the RAM is read and the data is latched. Then the refresh proceeds behind the latches, never disturbing the data. The RAM appears static.

DMA

DMA should be little different from normal cycles. One thing that must be considered is how to handle refresh. Three techniques immediately come to mind. First, have the DMAing device permit refresh periodically. Second, limit the DMA frequency. Make the period between DMA cycles equal to a normal RAM cycle plus a refresh cycle. This way the refresh can be handled transparently to the DMA. The third technique would be to limit the DMA time to something under 2 ms and at the end of the DMA do a burst refresh of the entire memory. There are a number of other ways to handle refresh and DMA. Performance of the system will determine which technique is most appropriate.

From a system standpoint, the most important aspect of DMA and dynamic RAMs is the polarity of the system level control signals. In a TTL system where bus control can change hands, the control signals must be *low true*. The reason for this is that, as control transfers from the CPU to the DMA device and back again, there will be short periods of time when the control lines are floating since neither device is driving the lines. In a TTL system, floating lines look high. If control signals have been defined as high true, then as the lines momentarily float, devices such as our RAM board will think that a command has been issued and will start an unintended cycle. Then the problem gets compounded. During the unintended cycle comes the command for a real cycle. Either the unintended cycle will be aborted, which destroys some RAM contents, or the intended cycle will start too late, causing other problems in the external system. An example of a bus with this problem is the S100, or hobby standard bus. It mixes signal polarities and, therefore, makes dynamic RAM control logic unnecessarily complex. If there is only one controlling device, signal polarities are academic. But if control can transfer, make the control lines low true.

SUMMARY

Refresh requirements make dynamic RAMs slightly harder to use than static RAMs. However, they pay the designer back for his efforts by reducing overall system cost in three ways. First, dynamic RAMs tend to be cheaper than static RAMs of the same size. This is primarily due to smaller chip sizes and higher production volumes than comparable static RAMs. Second, dynamic RAMs use less power. When a dynamic RAM is not being accessed it draws much less current than a static RAM. During access, dynamic and static RAMs draw similar amounts of power. However, in a large array, only that bank being accessed draws full power. All others still draw standby currents so that the total system power is lower than for a comparable static system. Because of the reduced power requirements, power supplies are cheaper. And, third, due to lower power dissipation, cooling requirements are reduced, allowing a further saving.

There are three things the system designer can do to maximize RAM board yields during manufacture. First, design proper power supply decoupling. This is probably the single most important consideration for the designer. A good high frequency 0.1 μF capacitor per supply per memory chip is recommended. A capacitor per supply per two chips is probably okay, but the board should be laid out for one capacitor per supply per chip and then capacitors can be left out as yield data becomes available. For bulk decoupling use about 50 to 200 μF per board on +12 V, less on +5 V and -5 V.

Second, design in as much margin as possible in all control signal timing. Use damping resistors where necessary. If timing is designed right to the minimum specs, periodically the right combination of data pattern, power supply noise, temperature, cosmic radiation, etc., causes the system to fail. The combined worst case parameters push a signal beyond specification and the memory fails.

Third, never allow spurious, shortened memory cycles to occur. Shortened or aborted memory cycles are guaranteed to destroy data in the row that was addressed during the aborted cycle.

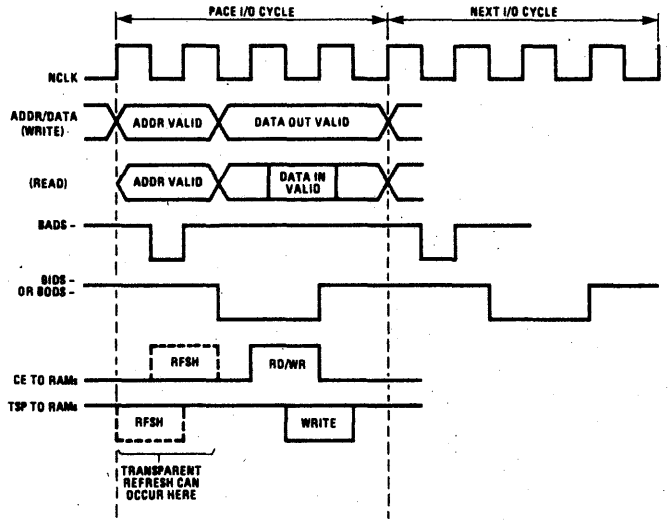
Any designer who uses reasonable care can successfully design dynamic memory systems which will be easy to manufacture and very reliable in the field.

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APPENDIX A

Appendix A shows a simplified timing diagram and schematics for a 16kx8 RAM board used by a PACE microprocessor for byte mode data storage.

RAMs are MM5270 4k RAMs with 12 V chip enables. All timing is generated from existing system signals. DMA is not now in use, but is possible in the future. Control signals from the bus are low true. Refresh is transparent, done at any time in the absence of any address, data in, or data out strobes, coincident with the rising edge of clock.



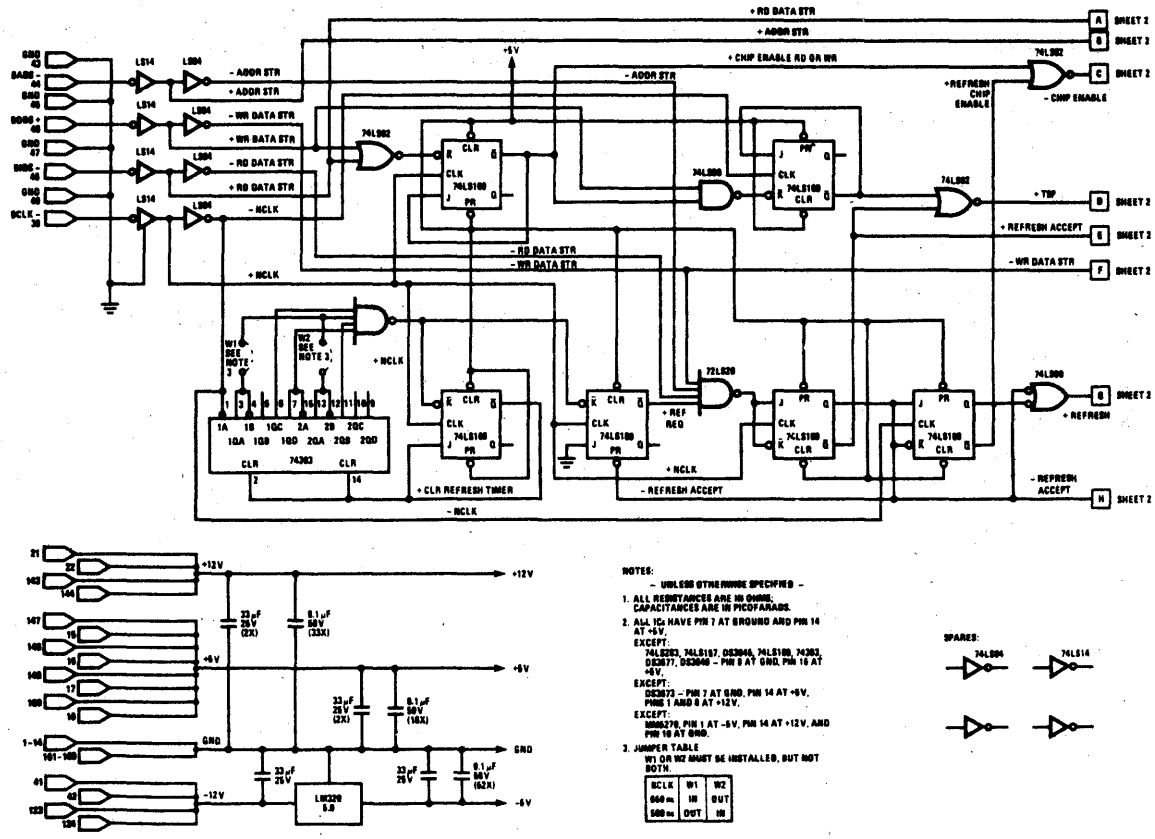


Figure 6. Control Logic, 16 x 8 R/W Memory Board

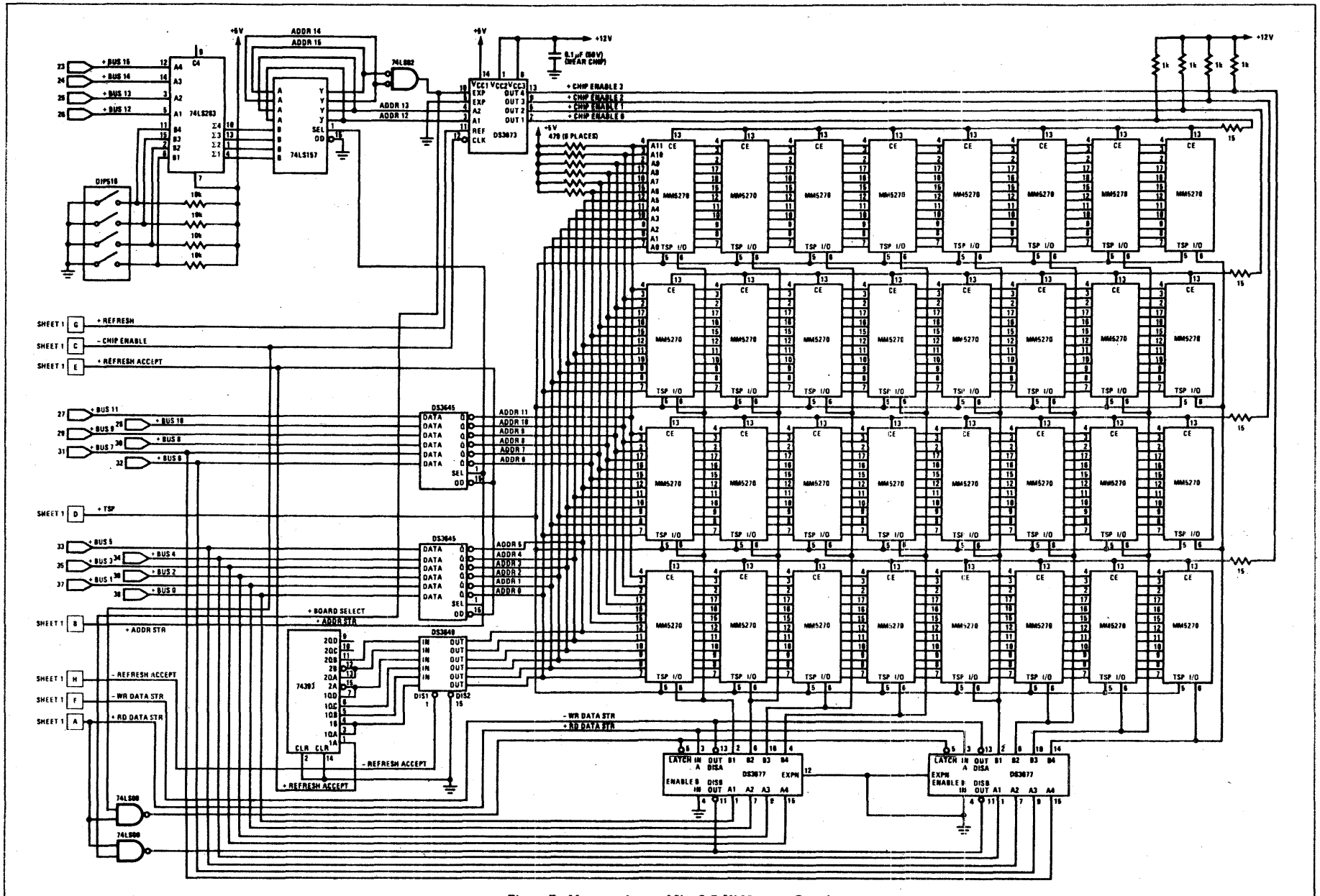
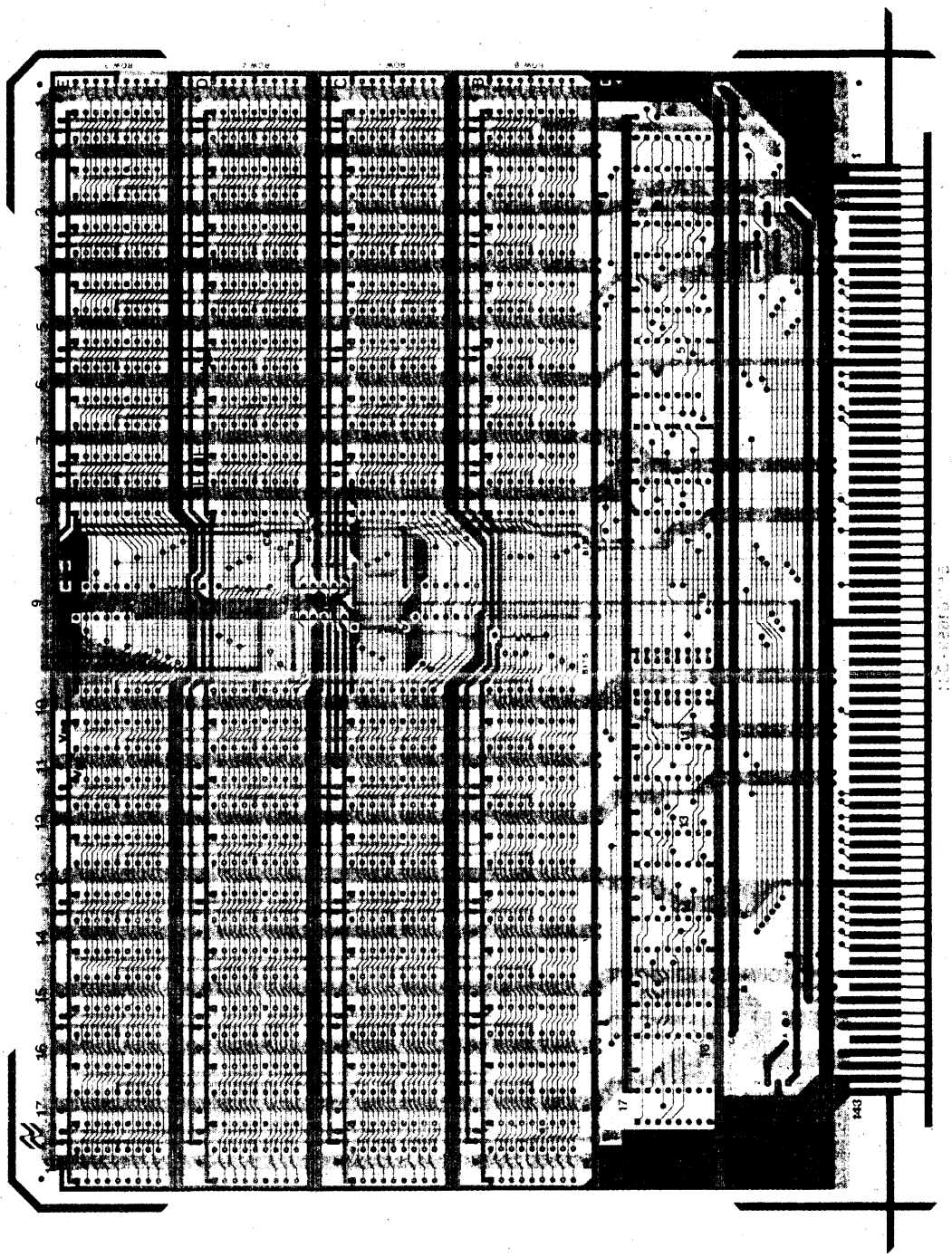


Figure 7. Memory Array, 16k x 8 R/W Memory Board

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APPENDIX B

In Appendix B we show the printed circuit board layout for a 16k x 16 RAM board which uses MM5270 18-pin 4k RAMs. It is an excellent example of the proper way to grid and decouple the power supplies on a two-sided board. Also shown are the centrally located chip enable drivers with their series damping resistors.



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MM5290 16K RAM Functional Description

National Semiconductor
B. Johnston

INTRODUCTION

This functional description covers the operation of the MM5290 16k dynamic RAM currently manufactured by National Semiconductor. This device is directly interchangeable with the MK4116. The National design has some internal differences, but these are transparent to the user, making the MM5290 a direct replacement for the MK4116.

Block Diagram

The block diagram shown in *Figure 1* shows the functional relationship between major blocks of circuitry in the MM5290. The multiplexed address, unlatched output and gated $\overline{CAS}$ features are shown. The row decoder column decoders and two 64 x 128 memory arrays with sense amplifiers between them are drawn in blocks that indicate their actual physical relationship on the die. This arrangement, with sense amplifiers in the middle and column decoders duplicated along each side, reduces cross talk (coupled noise) between address and column lines. Noise margin is improved because column line length is minimized.

Clock Generation

The MM5290 has multiplexed addressing necessitating separate row (Row Address Strobe, $\overline{RAS}$) and column (Column Address Strobe, $\overline{CAS}$) strobes. The timing relationship between these two strobes is made non-critical by gating $\overline{CAS}$ with the internal $\overline{RAS}$ clock. This is shown in *Figure 1*, along with the fact that $\overline{CAS}$ gates the write enable ($\overline{WE}$) control. These three signals are the source of the internal clocks (row, column and write clocks). Another way to describe this is: 1) the row clocks are referenced to $\overline{RAS}$; 2) the column clocks are referenced to either $\overline{RAS}$ or $\overline{CAS}$, depending on the $\overline{RAS}$ to $\overline{CAS}$ delay; and 3) the write clocks are referenced to $\overline{CAS}$ or $\overline{WE}$, depending on which occurs later. The block diagram in *Figure 1* indicates which blocks of circuitry the internal clocks control.

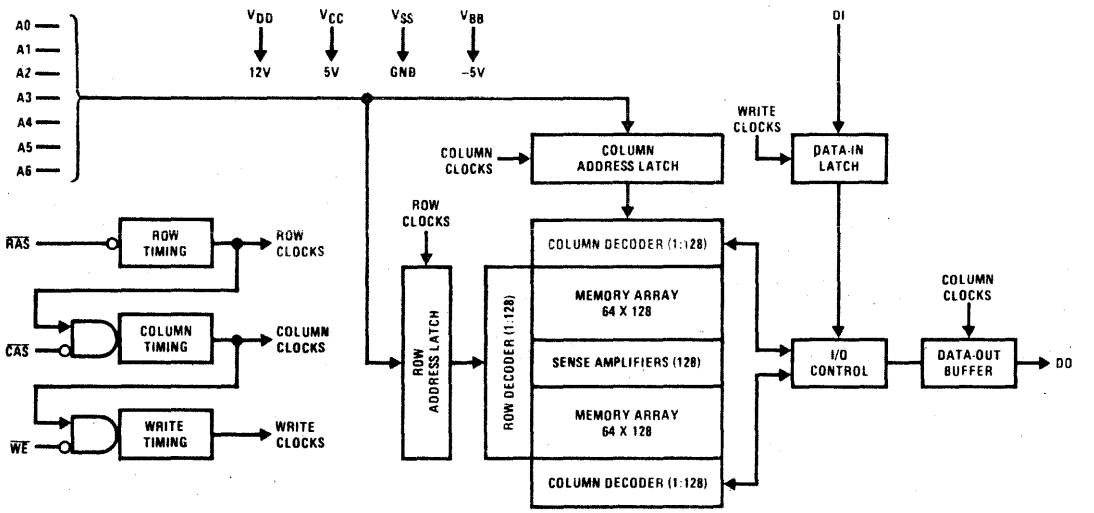


FIGURE 1. MM5290 Block Diagram

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Memory Cell

The basic memory cell consists of a transistor and capacitor as shown in *Figure 2*. Data is stored by selecting a cell and charging or discharging the storage capacitor C_S through transistor Q1. Q1 is then turned OFF (cell deselected) and data is retained until charge is lost through leakage current or the cell is refreshed. Each memory cell must be refreshed every 2 ms to guarantee data retention.

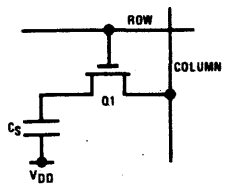


FIGURE 2. Basic Memory Cell

Cell Selection

Figure 3 shows a block diagram indicating how an individual memory cell is selected (addressed). First, the row address is latched in by $\overline{RAS}$. This is decoded to select 1 out of the 128 rows. Actually, there are 128 cells tied to each row so that 128 cell transistors (Q1 in *Figure 3*) are turned ON. Second, the column address is latched in. This is decoded to select 1 of the 128 columns. The row and column coincidence selects an individual cell for either reading or writing data.

Read Operation

Figure 4 shows a simplified version of the array of cells with the read/write circuitry. The array consists of 16,384 memory cells plus 2 rows of 128 reference cells. These are separated into 2 arrays by 128 sense amplifiers as shown. If row address AX5 is a logic "0", a row in the top half of the memory is being selected while the reference cells on the other side of the sense amplifier are also selected. Data is stored in complementary form in this half (top) of the array. The other half (bottom) of the array stores the data in true form when row address AX5 is a logic "1". A logic "0" in the array is defined as 0V stored in the cell and a logic "1" as +V.

Although the usual time reference in a cycle of operation is the high-to-low transition of $\overline{RAS}$, the prior events of discharging all row lines (to 0V) and precharging all column lines (to V_{DD}) must occur before a cycle of operation can be successfully completed. The starting point then is all row lines discharged and all column lines precharged. Then a row address is latched and the 128 cells connected to the selected row line are "read" by the 128 sense amplifiers. This also refreshes them. When a column address is latched, 1 of the 128 columns is connected to the I/O bus and the data of the selected cell becomes available on the DO pin.

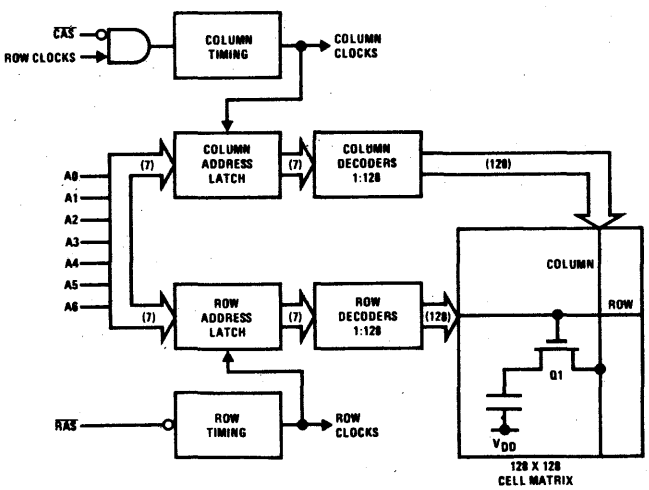


FIGURE 3. Block Diagram of Cell Selection

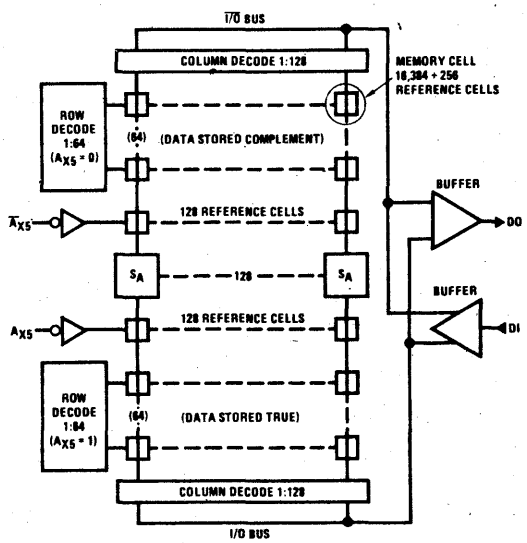


FIGURE 4. Simplified Read-Write Circuitry

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Sense Amplifier Operation

Figure 5 shows a simplified version of a sense amplifier together with a selected memory cell and the reference cell associated with "reading" the cell. When the cell is selected by the row address, a reference cell on the opposite side of the differential sense amplifier is also selected. (In fact, the entire row of 128 reference cells is selected.) If the selected memory cell contains a "1", then the storage capacitor C_S has the same potential as the left column line and no charge is transferred through Q1. If the selected cell contains a "0", then charge will be transferred through Q1 and shared between C_S and C_{CL}. The voltage of the column line will be reduced by ΔV where ΔV is a function of the ratio of C_S to C_{CL}.

Simultaneousiy with the events happening with the memory cell and the left column line, the right column line will always be reduced by 1/2 ΔV because charge will be transferred through Q2 between the capacitor of the reference cell labeled 1/2 C_S and C_{CL}. (All reference cells begin the cycle with a "0" stored on the storage capacitor.) This means that the sense amplifier will have a voltage difference of $\pm 1/2\ \Delta V$ across it with the polarity depending on the data stored in the memory cell. The sense amplifier regeneratively amplifies the difference and restores the data in the memory cell. This signal is also amplified by the output buffer and made available at the output pin (DO).

Write Operation

Figure 6 shows a block diagram of the write circuitry. The Data In buffer drives the column line of the selected cell either low (to ground) or high (to V_{DD}) depending on the logic level of DI. Transistor Q1 is ON because the cell has been selected and the storage capacitor C_S is written to the voltage of the column line. Then Q1 is turned OFF and C_S retains the data.

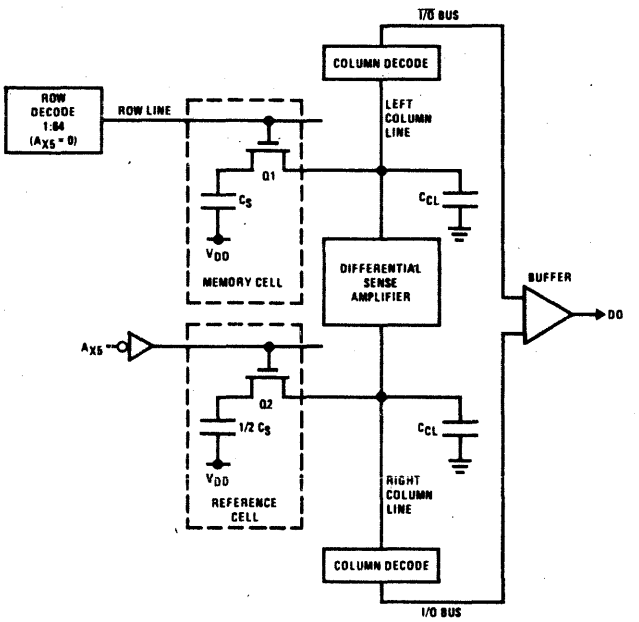


FIGURE 5. Simplified Read Circuitry

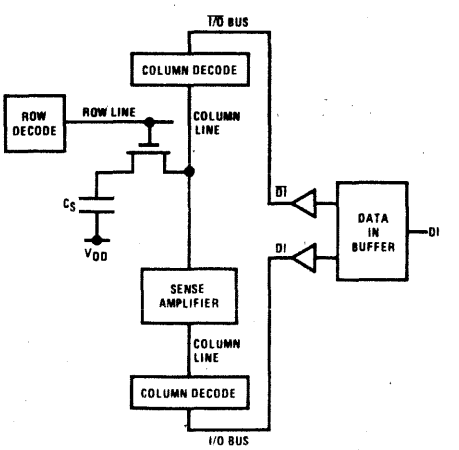


FIGURE 6. Simplified Write Circuitry

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Refresh

One side of the storage capacitor of the memory cell is a polysilicon V_{DD} line. The other side is a diffused junction (the drain of a transistor). The leakage of this junction normally increases with temperature and limits the data retention. This "dynamic" nature of the data storage requires that the cells be refreshed periodically (every 2 ms with today's technology) to retain data. A row of cells (128) is refreshed whenever any valid $\overline{RAS}$ cycle occurs. This means it takes 128 cycles to refresh the MM5290. Operating power is reduced and the output kept in the high impedance state when $\overline{CAS}$ is kept high and $\overline{RAS}$ is cycled for each of the 128 row addresses ($\overline{RAS}$ Only Refresh) to refresh the memory.

Most of the circuitry used in the MM5290 is dynamic and must also be "refreshed" for the memory to function properly. This is accomplished automatically when the dynamic cells are refreshed. This dynamic circuitry requires several cycles after power-up or after the refresh limit has been exceeded before proper device operation can be assured.

Read Timing

The read cycle timing is indicated in *Figure 7*. The cycle begins with $\overline{RAS}$ going low. This latches the row address. The address bus must be stable at this time: $\overline{CAS}$ then switches low sometime later. Again the address bus must be stable at the time $\overline{CAS}$ goes low because the column address is latched at that time. $\overline{WE}$ must be high coincidentally with $\overline{CAS}$ low during the read cycle. Data Out (DO) will be valid before t_{CAC} (access time from $\overline{CAS}$) or t_{RAC} (access time from $\overline{RAS}$) whichever is limiting. The output will return to TRI-STATE® in t_{OFF} time when $\overline{CAS}$ switches high. The valid data can be maintained to the end of the cycle (in fact, into the next cycle) because t_{CRP} minimum ($\overline{CAS}$ to $\overline{RAS}$ precharge time) is specified as a negative quantity in the data sheet.

Write Timing

There are 3 types of write cycles specified in the data sheet. These are called an Early Write, a Read-Write and a Read-Modify-Write cycle.

The Early Write cycle is characterized by $\overline{WE}$ going low no later than t_{WCS} minimum ($\overline{WE}$ to $\overline{CAS}$ set-up time) before $\overline{CAS}$. This could be called a "write only" cycle. The output remains in the high impedance state throughout the cycle while data is written into the desired location *(Figure 8a)*. D_{IN} is latched when $\overline{CAS}$ goes low and must be stable then rather than being referenced to $\overline{WE}$. The $\overline{WE}$ pulse width must be a minimum of t_{WP} and both the leading and trailing edges of $\overline{WE}$ have several timing constraints with respect to $\overline{RAS}$ and $\overline{CAS}$. Refer to the data sheet for these specifications.

The Read-Write cycle *(Figure 8b)* occurs when $\overline{WE}$ is delayed for at least t_{RWD} minimum ($\overline{RAS}$ to $\overline{WE}$ Delay) from $\overline{RAS}$ and the t_{CWD} minimum ($\overline{CAS}$ to $\overline{WE}$ Delay) from $\overline{CAS}$. The data in the selected location is first read; then new data is written into the location. The read portion of the cycle is explained in the section on Read Cycle Timing. The write portion of the cycle begins with data being latched in when $\overline{WE}$ falls and ends with the end of the cycle. The detailed timing is shown in the data sheet.

The Read-Modify-Write cycle *(Figure 8c)* is the Read-Write cycle extended in time so that the data in a particular location can be read, modified if necessary, and then written back into the same location. This requires that the $\overline{WE}$ pulse be delayed the minimum time of t_{RWD} from $\overline{RAS}$ and t_{CWD} from $\overline{CAS}$ plus an additional time shown as t_{MOD}. The additional time is the time required by the system to check the data, modify it as necessary and place it on the input data bus consistent with the required set-up time before $\overline{WE}$ goes low. Note that t_{MOD} is a system parameter. Detailed timing is given in the data sheet.

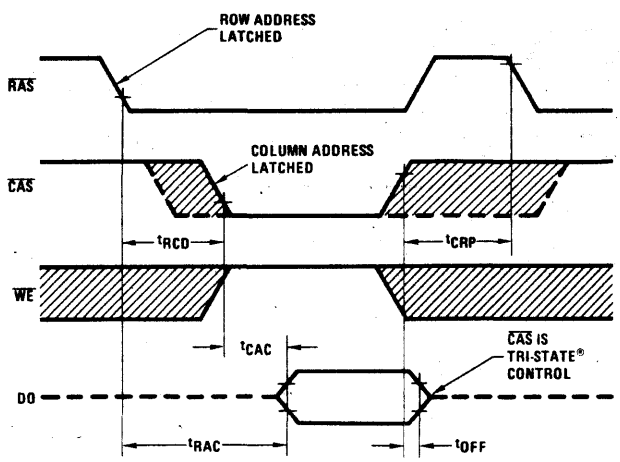


FIGURE 7. Read Cycle

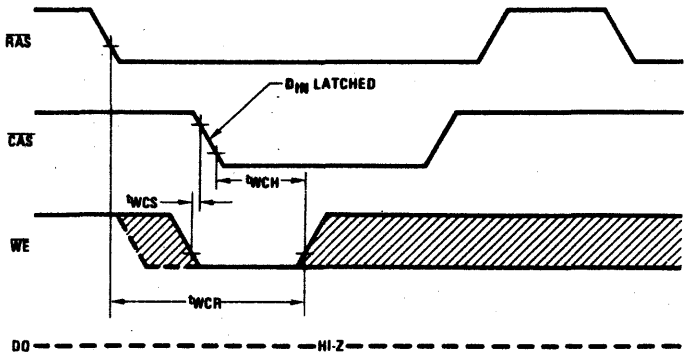


FIGURE 8a. Early Write

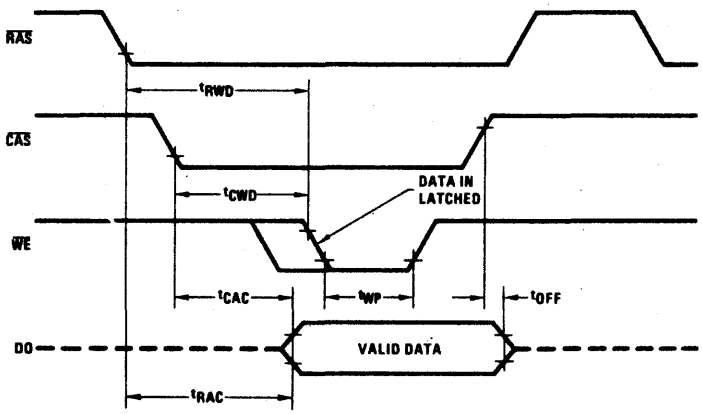


FIGURE 8b. Read-Write

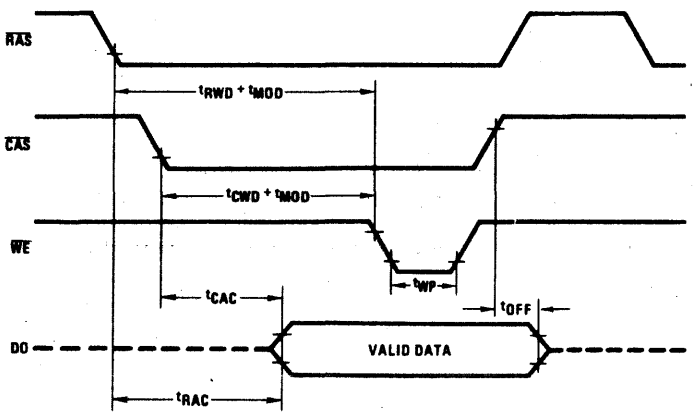


FIGURE 8c. Read-Modify-Write

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Page Mode Timing

The MM5290 functions in a page mode operation with up to 128 bits (1 row) per page. Data may be read or written in this mode of operation.

Figure 9 shows the timing for a page mode Read cycle. The cycle starts like a normal read cycle with the access time of the first bit (bit 0) either t_{RAC} or t_{CAC} whichever is limiting. The rest of the page mode read is accomplished by keeping $\overline{RAS}$ low and cycling $\overline{CAS}$ an additional 127 times while changing to a new column address each time. $\overline{WE}$ may be held high continuously or cycled. If $\overline{WE}$ is cycled, it must meet the timing constraints shown in the data sheet. $\overline{RAS}$ cannot be held low for more than 32 μs so that the maximum $\overline{CAS}$ cycle time is approximately 250 ns to read the full 128 bits of data in a page (row).

Figure 10a shows the timing for a page mode Early Write cycle. The cycle begins as a normal early write cycle. The rest of this mode of operation is accomplished by keeping $\overline{RAS}$ low and cycling $\overline{CAS}$ an additional 127 times while changing to a new column address each time. The input data (D_{IN}) must be referenced to the falling edge of $\overline{CAS}$ and not $\overline{WE}$. $\overline{WE}$ may be held low or pulsed. The output will remain in the high impedance state throughout the cycle.

Figure 10b shows the timing for a page mode Read-Write cycle. The cycle begins as a normal read-write cycle. Then $\overline{RAS}$ is held low and $\overline{CAS}$ is cycled an additional 127 times while a new column address is selected each time. $\overline{WE}$ must be kept high for the t_{CWD} time (to guarantee the data is read) and then switched low for t_{WP} time to accomplish writing the new data. The data to be entered (D_{IN}) must be referenced to $\overline{WE}$ with the appropriate set-up and hold times shown in the data sheet. Extending the t_{CWD} time to allow for modifying data and then writing it back into the same location would make this a Read-Modify-Write page mode cycle.

Refresh Timing

The MM5290 must be refreshed every 2 ms. Any valid cycle of $\overline{RAS}$ will refresh a row of 128 bits. It requires 128 cycles, (1 for each row of the matrix) to refresh the entire memory. *Figure 11* shows $\overline{RAS}$ only refresh. Only $\overline{RAS}$ switches. $\overline{CAS}$ is held high which reduces I_{DD} and TRI-STATES the output.

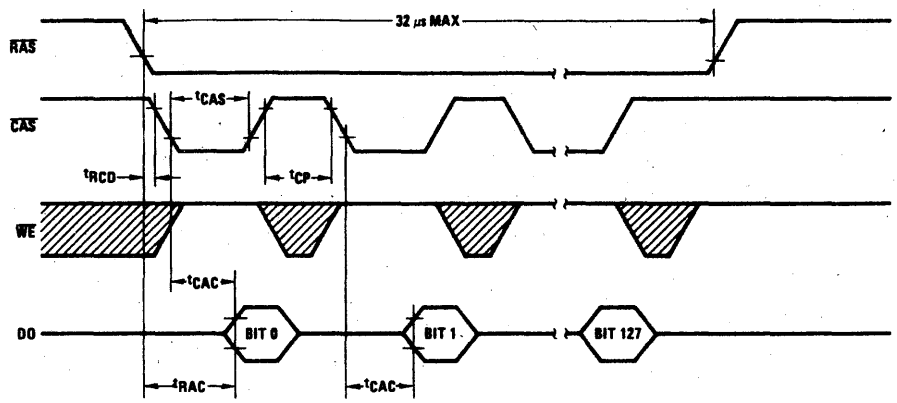


FIGURE 9. Page Mode Read Cycle

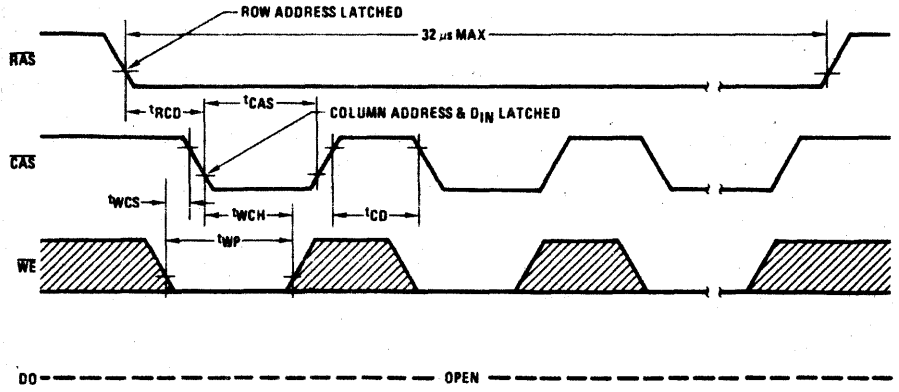


FIGURE 10a. Page Mode Early Write Cycle

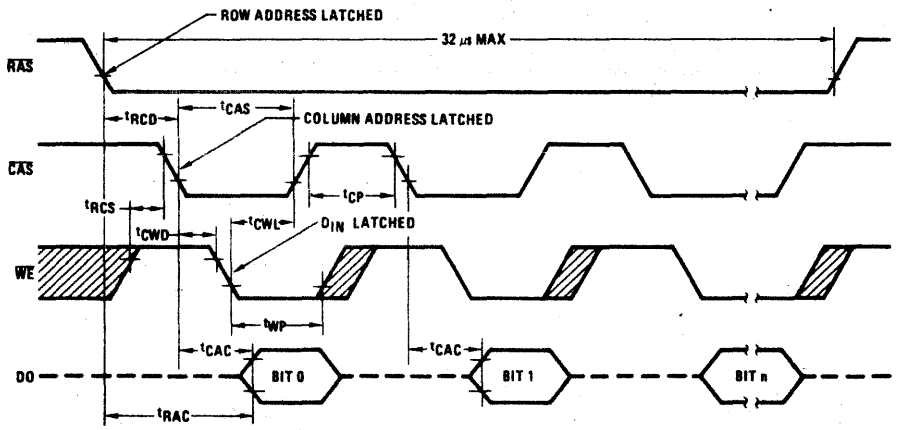


FIGURE 10b. Page Mode Read-Write Cycle

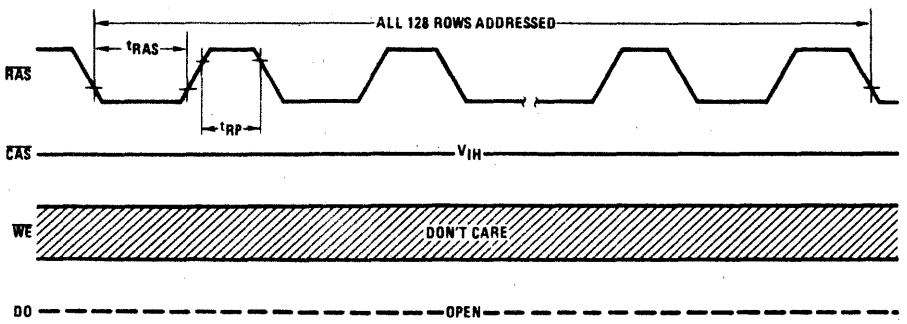
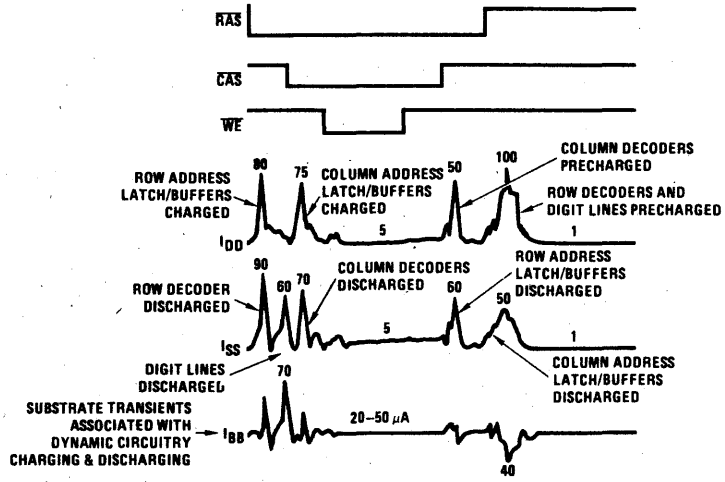


FIGURE 11. $\overline{RAS}$ Only Refresh Cycle

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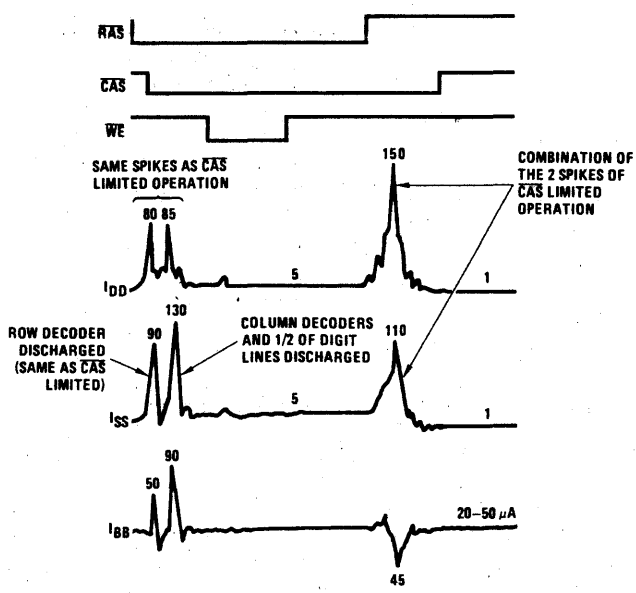
Current Transients

Figures 12 and 13 show the current waveforms for I_{DD}, I_{SS} and I_{BB}. When the MM5290 is operated with $\overline{CAS}$ limited timing, the transients associated with the row and column clocks are separated in time. The major events causing the transients are indicated in *Figure 12*. When the operation is $\overline{RAS}$ limited, some of the transients overlap. This is shown in *Figure 13*. The transients are then additive and maximum transient peaks occur. Adequate capacitive decoupling* at the board level is necessary to maintain power supply voltage transients within the data sheet specification of ±10%.



Note. All values in mA unless shown otherwise.

FIGURE 12. $\overline{CAS}$ Limited Timing Transients



Note. All values in mA unless shown otherwise.

FIGURE 13. $\overline{RAS}$ Limited Timing Transients

*Refer to "Dynamic RAM Board Design Made Easy"

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Bit-Slice Microprocessor Design Takes a Giant Step Forward with "Schottky-Coupled-Logic" Circuits

National Semiconductor
Application Note 203
Dale Mrazek
July 1978

A new four-bit slice "Schottky-coupled-logic" design combines the flexibility of the industry standard 2900 microprocessor architecture with advanced LSI processing. It implements low-power Schottky TTL circuitry on the same devices as a proprietary TRI-STATE™* emitter coupled logic design to achieve a 30 to 50 percent improvement in speed with no increase in power dissipation. It also allows the use of advanced "pipeline prediction" techniques in microprogram control design to significantly reduce microcycle times.

In most computer applications, cost, speed, power consumption and utility are the key factors. In some applications cost is the dominant consideration. In others it is speed or power consumption.

In bipolar four-bit slice microprocessor-based systems, this is particularly true. To date, however, designers have had to make a choice between the high speed of emitter coupled logic or the low power consumption and low cost of low power Schottky TTL four-bit designs such as the industry standard 2900 series.

But with current approaches it has not been very practical to have both.

If the designer chose an ECL design, he paid a price for the high speed with higher power consumption and loss of board design flexibility. If one of the LS bipolar 2900 designs currently available was chosen, low power could be achieved, but only at the price of considerably reduced system throughput.

Now, however, computer system designers can have both ECL-type speeds and LS bipolar power consumption. Using a new advanced "Schottky-coupled-logic" technique that combines low power Schottky circuitry on the same die as proprietary low power TRI-STATE ECL circuitry, the IDM2900 series of four-bit slice microprocessor components has been developed by National Semiconductor Corporation.

With this patented "SCL" technique, devices have been fabricated which are 30 to 50 percent faster than comparable 2900 designs now available. At the same time power consumption is slightly less than that for present LS bipolar designs and one third of that required for ECL-based designs.

The substantially increased system throughput made possible by this new series of SCL implemented IDM2900 parts means a number of advanced computer designs can be considered which were not possible before. For example, advanced "pipeline prediction" techniques in microprogram control design can be used to significantly reduce microcycle times.

An interesting byproduct of this approach is that this is the first ECL-based four-bit slice family to meet the military requirements over the military temperature range. Indeed, the new series shows even less performance degradation over the military temperature range than some of the standard LS bipolar parts now available.

A 60 Nanosecond Slice

The process and circuit improvement that have been achieved are the most apparent in the IDM2901A, which boasts an average microcycle time of only 60 to 70 nanoseconds, a 100% improvement over existing LS bipolar designs. Power consumption, however, is about the same, only 800 milliwatts for the entire device. Also available is an even faster version — the IDM2901A-1 — with a microcycle time of only 50 to 60 ns, and no increase in power consumption.

As with other implementations of the 2900 architecture, the IDM2901A is the key element in this high speed family of four-bit slice components. Designed as a high speed cascadable element intended for use in CPUs, peripheral controllers, programmable microprocessors and numerous other applications, the IDM2901A consists of a 16-word by 4-bit two-port random access memory, a high speed arithmetic logic unit and the associated shifting, decoding, and multiplexing circuitry. (See figure 1.)

Indeed, except for that most important parameter — speed — the IDM2901A is plug compatible with any LS bipolar implementation of the same architecture now on the market. But plug in replacement and raw speed improvements are just part of the story. As can be seen from tables 1 and 2, the IDM2901A, for example, has improved significantly almost every timing parameter possible. The read/modify/write cycle is 42 percent less, the maximum clock frequency 68 percent greater. Execution time for a typical operation, such as an add and shift (multiply) is 95ns maximum and 60ns typical, a significant gain over previous 2900 implementations. (See table 3.) Used in a typical design, system microcycle time is in the 100 to 150ns range, about one half to two thirds that of previous LS bit slice implementations.

These circuit and process improvements have been implemented in many of the standard components needed to build a system based on the 2900 bit slice architecture. In addition to the IDM2901A, 18 other standard parts have already been introduced. These will allow system designers to take advantage of the increased speed. (See table 4.)

*A trademark of National Semiconductor Corporation.

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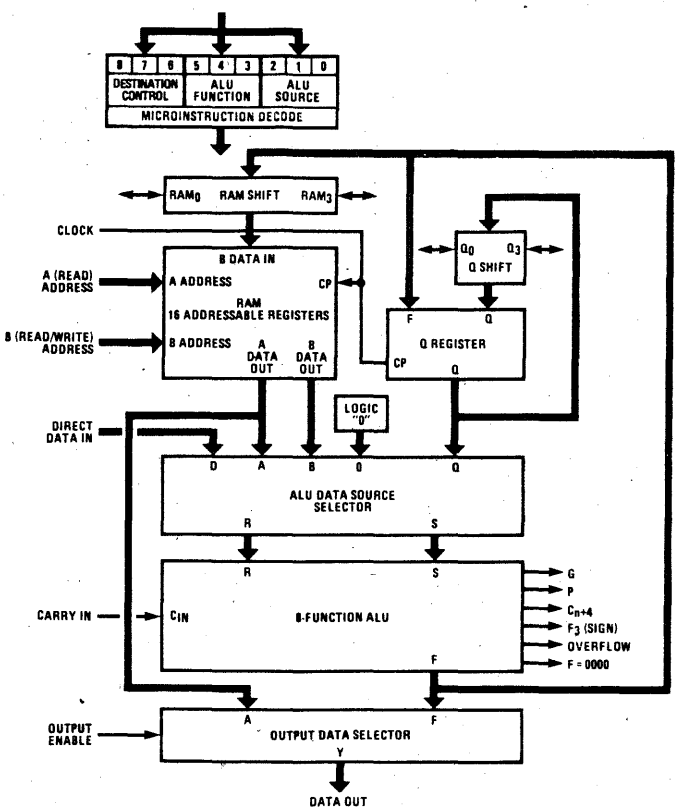


Figure 1. Block Diagram

Using some of the standard parts in the IDM2900 family, a typical 16-bit controller function can be implemented with a system microcycle time of about 140ns. This represents about a 30 percent improvement over that achieved with LS bipolar devices. Using the high speed IDM2901A-1, system throughput can be reduced to about 120ns. Using the proprietary parts added to the family, the same functions can be done in even less time, about 120 and 100ns, respectively.

Figure 2 shows a very simple, very fast state sequencing controller designed using IDM2900 family parts. It has no arithmetic capability, but 80ns clock intervals can be used. A less complex controller is shown in figure 3. It utilizes the IDM2901A for its data storage and arithmetic or logic generation. The IDM2911A is used as the state sequencer for this controller since its speed and subroutine stack can be used to advantage in the application.

LS + ECL = SCL

To achieve this combination of ECL speeds and LS bipolar power consumption, several techniques are used. One is to use low power Schottky circuitry in the periphery of the chip for input/output and interfacing to external TTL levels and the ECL internally — a technique commonly used in some bipolar memories. (See figure 4.)

Traditionally, ECL to TTL translators are slow unless considerable power is applied. In the IDM2900 family, however, the ECL speeds are retained, but at no cost in additional power, thanks to a TRI-STATE translator circuit technique that transforms the 0.7 volt ECL levels to 5 volt Schottky levels. This technique eliminates the slow and power consuming buffer transistors that usually do the job, and the translators can drop off to one third their active power with no loss in speed. Using this TRI-STATE translator technique, the extra 60 to 65 percent in power that would have been consumed is pumped instead into the portions of the device that require it; specifically, the ECL core circuitry.

Table 1. Percentage Improvement in Cycle Time and Clock Characteristics

Time	IDM2901A	IDM2901A-1
Read-Modify-Write Cycle	40% less	40%
Maximum Clock Frequency	6%	6%
Minimum Clock Low Time	same	same
Minimum Clock High Time	same	same
Minimum Clock Period	40% less	40%

Table 2.
Percentage Improvement
In Maximum Combinational Propagation Delays for IDM2901A and IDM2901A-1*

to Output / from Input	Y	F_3	C_{n+4}	$\overline{G}/\overline{P}$	F = 0 R_L = 470	OVR	Shift Output RAM_0 RAM_3	Shift Output O_0 O_3
A, B	19 (38)	19 (38)	13 (33)	8 (31)	22 (50)	24 (30)	26 (42)	
D (arith mode)	11 (29)	11 (29)	11 (29)	0 (14)	8 (47)	16 (27)	23 (46)	
D (I = x37)	0 (20)	0 (20)			0 (42)		17 (36)	
C_n	0 (17)	0 (27)	0 (20)		20 (42)	0 (17)	30 (30)	
$I_{2,1,0}$	0 (27)	9 (55)	0 (30)	0 (33)	14 (43)	23 (62)	20 (40)	
$I_{5,4,3}$	9 (30)	9 (30)	9 (30)	10 (36)	21 (43)	23 (31)	33 (40)	
$I_{8,7,6}$	0 (17)						0 (0)	0 (0)
$\overline{OE}$ Enable/Disable	14/0 (43/20)							
A Bypassing ALU (I = 2xx)	11 (11)							
Clock ↗	0 (17)	0 (25)	0 (25)	0 (20)	20 (33)	27 (27)	25 (31)	0 (0)

*2901A-1 in parentheses.

The output translators use both linear and digital techniques. Differential ECL signals are translated using a differential current amplifier where the differential output voltage is changed to a differential current and then back to an output voltage. This drives a phase splitting transistor used to, in turn, drive the output circuitry in the periphery. Key to the operation of these translators is the use of an improved TRI-STATE logic buffer circuit characterized by a current mirror transistor having its base and emitter, respectively, connected to the base and emitter of the phase splitter transistor, and its collector connected to the voltage supply terminal. (See figure 5.) The emitter size on the current mirror transistor is about twice that of the emitter size of the phase splitter transistor.

The current mirror transistor supplements the drive current that is provided by the phase splitter transistor to the pull-down output transistor. This permits a higher resistance to be connected between the voltage supply terminal and the collector of the phase splitter transistor without diminishing the drive current to the pull-down output transistor. By connecting a higher resistance, the power for the circuit is reduced when the output is in its disabled state.

An additional advantage realized as a result of the current mirror transistor base and emitter connected, respectively, to the base and emitter of the phase splitter, and its collector to the supply voltage terminal, is a faster dynamic response in the conduction state of the pull-down output transistor to a change in the level of the digital data input signal. This occurs due to the selective use of the Miller feedback effect to cause a beneficial ratio change in the current mirror pair during a dynamic transition. Miller feedback occurs on the phase splitter transistor because its collector is coupled to the voltage supply through a resistance, and is absent on the current mirror transistor because its collector is directly connected to the voltage supply terminal. As a result, with the onset of the transition in the digital data input signal, as received from the collector of the input transistor, the current ratio between the current mirror and phase splitter transistors is even greater than the ratio of the respective emitter sizes.

Internally, the ECL logic has level translators on each input. This necessary circuitry achieves not only the level translation, but also has a very desirable input level sensitivity. As can be seen in figure 6, the translator is similar to a differential amplifier whose internal reference is stable. The result is very abrupt transfer characteristics on all input signals, and, thus, very fast switching speeds.

Improved Computer Design

The substantially increased system throughput made possible by this new series of SCL-implemented IDM2900 components means a number of improved bit slice processor designs can be considered which were not possible before.

Compared to simple control applications, there are a number of other factors to be considered when using IDM2900 series devices in more complex processor systems. The general changes which take place relate to special handling of data and address outputs and data inputs. The IDM2901A's register and ALU elements are no longer sufficient, especially when data and address word lengths grow from 8 to 16 bits or greater. Special functional elements are generally added, and include: input and output data or addressing registers, sign extend of

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Table 3.
Maximum Throughput Comparisons for Add and Shift

Function	IDM 2901A-1	IDM 2901A	AMD 2901A	AMD 2901
A or B → $\overline{G}$ or $\overline{P}$	45	60	65	80
74S182 Delay	10.5	10.5	10.5	10.5
C_{IN} → RAM_0	35	35	50	55
RAM Setup Time	15	20	25	55
Total	105.5	125.5	150.5	200.5
Percent Change	47.4%	37.5%	25%	0%

data, and instruction decode, as well as shift and rotate control, and multiply functions. Also, special processor status registers are quite often added, as well as the unique controls for these elements.

Some special thought applied to these areas can reduce the parts count considerably and improve processor performance when using IDM2900 components.

The sign extend function is a good example of what can be done. Sign extension of a data word can be accomplished in a number of ways. But what the designer of the processor would prefer is to implement the function with the fewest possible parts and at the fastest data inputs. The first solution that comes to mind is the use of multiplexers, as shown in figure 7, which allows data to be fed through the multiplexer to D inputs of the IDM2901As. The control function which steers the data to the D input representing the bit which needs to be extended normally comes from the microprogram store. The added delay using this path is 12ns or more if parts slower than the DM74S157 are used. For each 4 bits of data to be modified an additional component is required; 2 parts for 8 bits, 3 parts for 12 bits and 4 parts for 16 bits.

The IDM2900 family, however, allows consideration of a number of other ways to do sign extension that require fewer parts and are less expensive and faster.

One is to use the carry input to accomplish a sign extend. But to use this input one must subtract "1" from "0" conditionally if the sign bit is a "1" and the opposite if it is a "0." But the problem arises as to how to obtain a value "0" in a register, an impossibility.

But the same effect can be achieved if the same address location is placed upon both the A and B address inputs. The source code is then used to select A and B and the function code for subtract. Now, if a carry input is a "1" the result is a "0" and if the carry input is a "0" the result is an all "1s" sign extend result. This technique can propagate for as many packages as necessary since the carry logic is necessary for other functions and is already included.

An easy method of inserting the conditional carry with the IDM2901A is to use the IDM2902 in a manner that is different from standard LS bipolar designs. Instead of connecting the carry input of the 2902 to the microcontrol carry from ROM, it is connected to the carry out of the least significant IDM2901A package. Note that this is just as fast as the previously suggested connections since the G and P are only slightly faster than the carry out of the least significant IDM2901A. Doing this allows one free G and P input to be available at the second level, as indicated in figure 8.

It is only necessary to connect an AND gate to the input and sign extend is accomplished. The lower bits which want to be entered without modification need only be applied to the D inputs and a source code selected to perform a D minus 0 transferred to B. The most significant package group produces A minus B where A and B are as described before. An all-1s or all-0s result is obtained dependent upon the value of the data bit to be extended. The result is a sign extension with three fourths of a package for any sign extend, achieved at no loss in normal cycle time. This is because a carry input change can occur later in a cycle than a change of D.

Performing a Multiply

Most of the time the name of the game in computer processor design is speed. Nowhere is this more true than when it is necessary to perform a multiply. This is because the multiply determines the longest cycle time if performed in the normal manner. This is because more than one path through the 2901A is utilized. Passage through several external components is usually required and this must also be added to the solution time. However, with the use of high speed components in the IDM2900 family it is possible to circumvent and shorten this path, and thus shorten the multiply cycle time.

How this is done is clearly understood only by referring to a specific example. Let's assume the problem is to perform a multiply of two signed 16-bit values.

Table 4. The 2900 Family

IDM2901A	4-Bit Microprocessor Slice
IDM2901A-1	4-Bit Microprocessor Slice
IDM2902	Carry Look-Ahead Generator
IDM2909A	Microsequencer
IDM2911A	Microsequencer
IDM29702	16x4 Bit RAM (open collector)
IDM29703	16x4 Bit RAM (TRI-STATE)
IDM29704A	16x4 Bit Dual Port (Open Collector)
IDM29705A	16x4 Bit Dual Port (TRI-STATE)
IDM29750	32x8 Bit PROM (open collector)
IDM29751	32x8 Bit PROM (TRI-STATE)
IDM29760	256x4 Bit PROM (open collector)
IDM29761	256x4 Bit PROM (TRI-STATE)
IDM29803	16-Way Branch Controller
IDM29811	Next Address Controller
IDM29901	Octal D Register (TRI-STATE)
IDM29902	Priority Encoder
IDM29903	16x4 Edge-Triggered Register (TRI-STATE)
IDM29908	Quad Gated Flip-Flop (flag control)

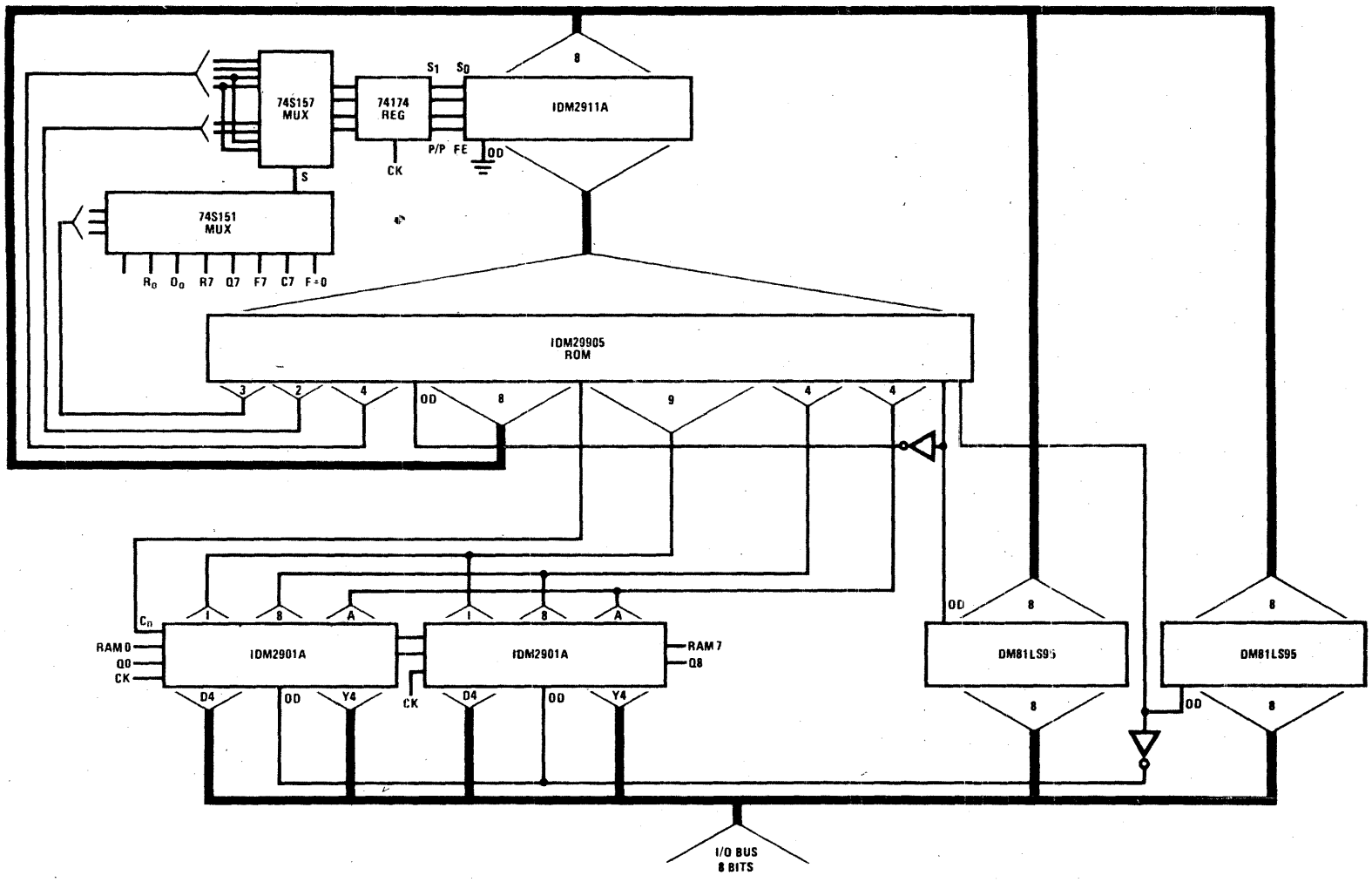


Figure 2. Very Fast State Sequencing Controller

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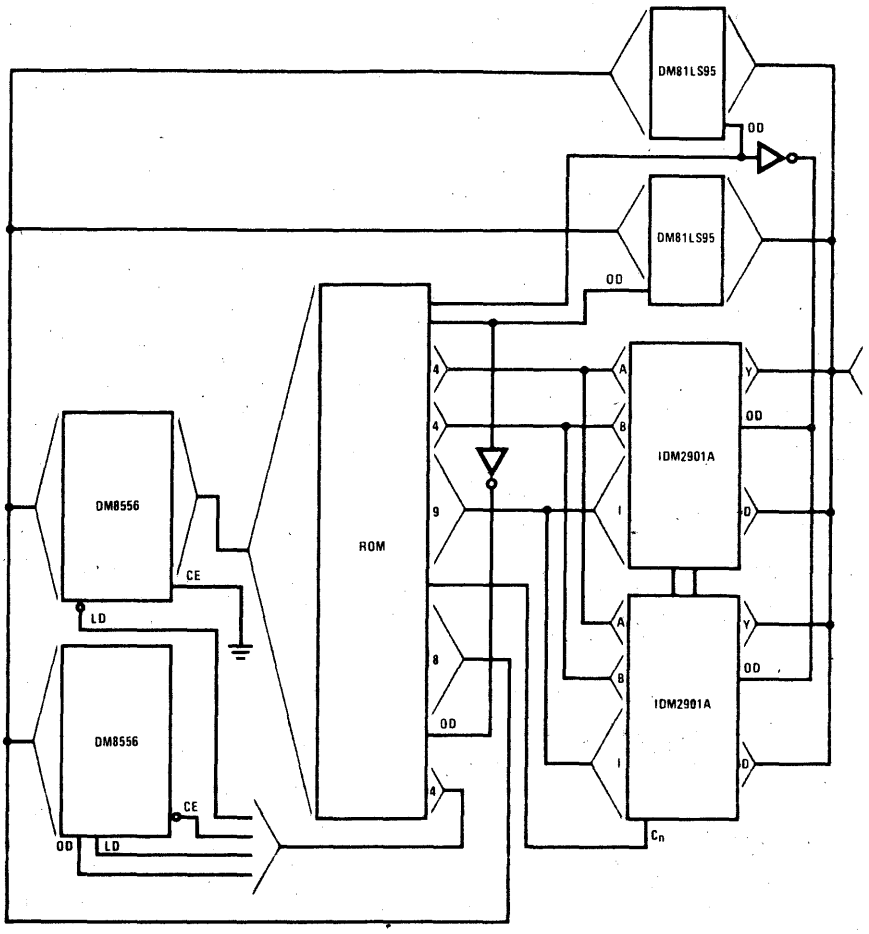


Figure 3. Small High Speed 8-Bit Controller with One Level of Subroutine Capability. This solution can run at 100ns cycles.

Figure 8 is the circuit as implemented using IDM2900 devices with the two multiplexers (74S253) and a D flip-flop (74S74). Using IDM2900 components and this technique, the multiply is performed 30 to 70 nanoseconds faster per cycle than with standard LS bipolar bit slice parts. This is a total speed improvement of 480 to 1,120ns.

An additional significance to the design is that special multiply cycle time intervals are not required. This operation, therefore, makes possible a processor or controller with a less complicated clock control circuit.

Note that in figure 8 there is an extra stage of register storage in the Q register (D type flip-flop), compared to traditional designs. It is therefore necessary to shift Q one time without shifting the file register.

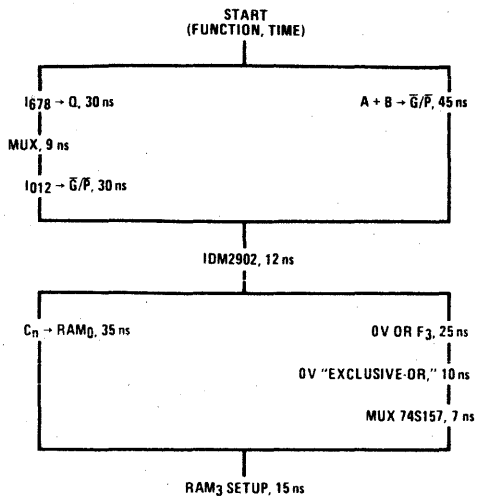
Since it is necessary to clear the partial product register, the Q register is shifted the first time so as to get the least significant bit into the extra storage location.

After this, the A and B register file addresses do not change and therefore do not enter into the timing equations. The much faster response time of an added D flip-flop saves a great deal of time in each microcycle of the multiply add and shift operation.

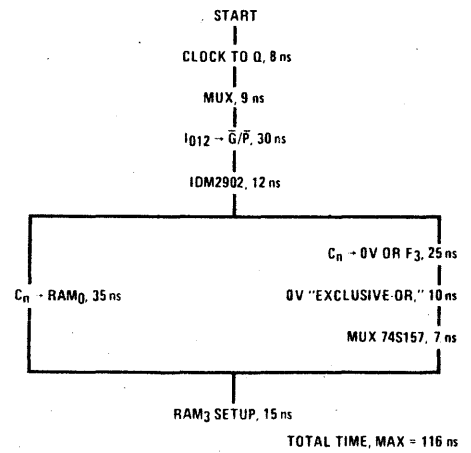
Since the A and B inputs do not change the critical path is from the D register output into the I_{O12} inputs and through the IDM2901As in a normal add and shift operation. Using the Q flip-flop, 20ns is saved, and using the I_{O12} input, 10ns is saved in each of the 16 cycles of the 16-by-16 multiply. This is all that is necessary for a positive signed multiplicand. But if a negative result is required, an additional path must be added.

The two possible paths in the most significant IDM2901A package are from C_n to RAM_0 output or from C_n to Overflow or F_3 and through the additional exclusive-OR gate and multiplexer input to the RAM_3 input. The maximum time delay path is 20ns from overflow and F_3 outputs back to the RAM_3 input for the most significant 2901A package.

Using standard techniques common to previous 2900 designs, only 15 conditional adds, followed by a shift and one conditional subtract and then a shift, are required to do a signed multiply in 2s complement notation. The resultant data paths required for this solution are as follows:



But if the circuit described in figure 8 is used, and the A and B address lines are set up one cycle ahead of the multiply sequence, the following timing comparison, using IDM2901A-1s instead of IDM2901As, prevails:



A net savings of 22ns per microcycle is thus achieved with this change. It can now be seen that sometimes it pays to add a flip-flop in certain locations to achieve higher performance so as to achieve a simpler solution in other areas. Here, a 20 percent reduction in cycle time was achieved.

Improving Microcycle Times with Pipeline Prediction

Perhaps the most important aspect of National's IDM2900 family of high speed, low power SCL components is the impact on how microprogram state sequencing is implemented in bit slice designs. The ultimate result will be further improvements in microcycle times beyond anything now possible with present 2900 bit slice families.

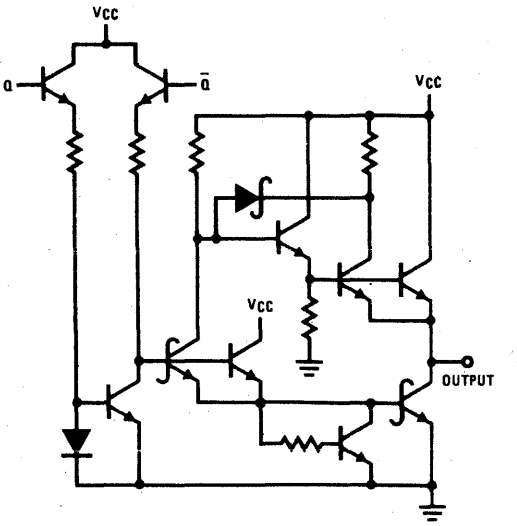


Figure 4.

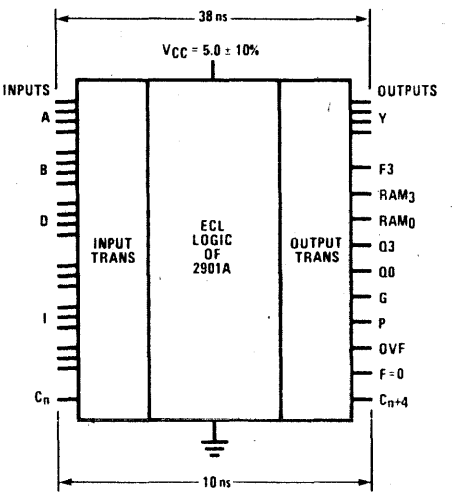


Figure 5.

In the very earliest use of state sequencing — in minicomputers and larger systems — operations were performed in series, one after the other, and the microcycle was defined as the sum of the operations. (See figure 9.) Still in use in some designs today, in this approach a state sequencer increments to the next state or branches to a next state depending on the logic level of the test input. In this solution the controller timing is from the clock edge of the controller register/counter through microcontrol storage (ROM) and the processing elements (2901s), then back through the next state decision tree to the controller-register counter.

The second approach is called "pipeline microcoding," and is an approach commonly used in bit slice systems such as the standard LS bipolar 2900 family. (See figure 10.) In this solution the microcontroller loop timing is operating in parallel with the execution of the processing component section.

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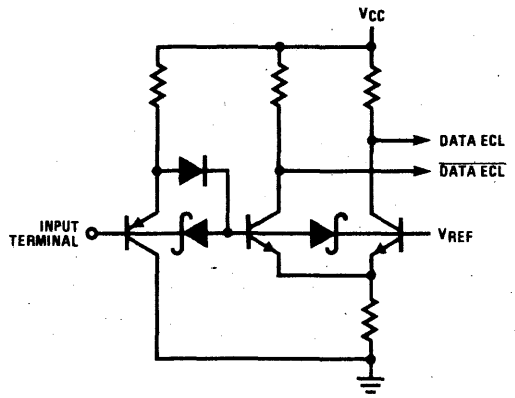


Figure 6.

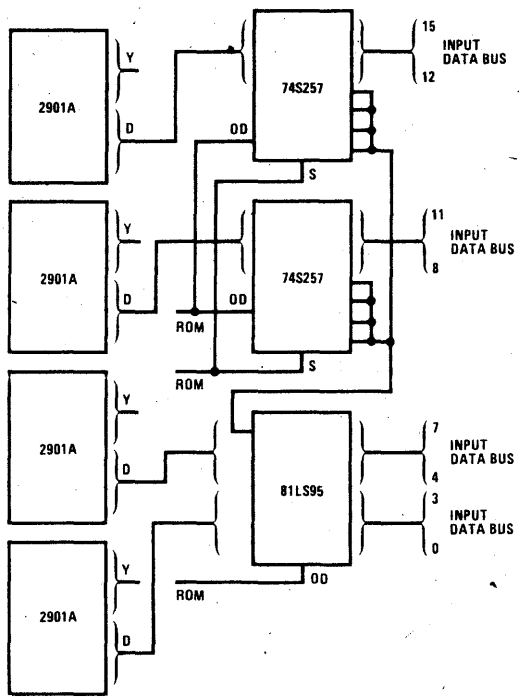


Figure 7. Sign Extend Using Multiplexers

During the time an arithmetic operation is being performed, the next microcontrol word is being set up for use by the microcode. The microcode for the present register/ALU operation occurs during the previous operation. The use of the register between the output of the microcontrol store and the 2901s allows the two sections to function with overlapped timing. The result of this type of micro-sequence control is a faster machine cycle time than used in the totally serial mode of operation.

Also required in this mode of operation is the absolute knowledge of the next state control one cycle before the execution of the 2901A cycle. It is therefore difficult to implement a number of successive conditional next state decisions. This type of microcontroller is said to be operating in a "pipeline" mode in that the next state microcontrol is being obtained during the time the previous one is being executed.

Using SCL-implemented IDM2900 components instead of LS bipolar bit slice devices in this approach results in a 65 to 75 percent reduction in the register/ALU portion of the microcycle. In spite of this, total microcycle time may be reduced only 40 to 50 percent. This is because the microcycle time is determined by the length of the longest operation, which in this case can be the delay in the microcode portion.

To get the full benefit of the high speeds inherent in National's SCL family therefore means abandoning the traditional approach to pipelining used in previous 2900 bit slice designs. What can be used instead is a different technique — pipeline prediction — which allows a reduction in the microcode portion of the microcycle so that it is equal to or less than the register/ALU setup time. The relative timing comparisons between these four approaches are shown in figures 11A through 11D.

The "pipeline prediction" controller functions in much the same way as the standard pipeline configuration except that it can also accept any number of successive conditional next state decisions in a row. This microcontroller "pipelines" microcontrol sequences in much the same manner as the previous design and for the same reasons. But shorter microcycles can be obtained due to the fact that during any microcycle the most predictable next cycle is being set up. But should the test of the next state decision be different from the one predicted, then the alternate state is conditioned and the microcontroller and the data system pass through a correction interval.

This design makes next state decisions within the same cycle as microcontrol of the IDM2901A. Figure 12 shows a "pipeline prediction" technique where the next state is a choice between two states. This means one state is predicted, and if incorrect the second choice is used. The microcycle is either delayed or an additional cycle is inserted.

There is no real reason why the design must be limited only to two next state conditons. Any number may exist. It is only necessary to predict the most probable next state and correct it if necessary. Most next state decisions are known to a high probability of occurrence. The additional cycle time added for the few times an incorrect prediction is made is extremely small compared to the total microcycle time saved. Additional speed is obtained with this technique since it minimizes the number of states through a control sequence.

Finally, pipeline prediction requires no increase in the number of components to achieve these increases.

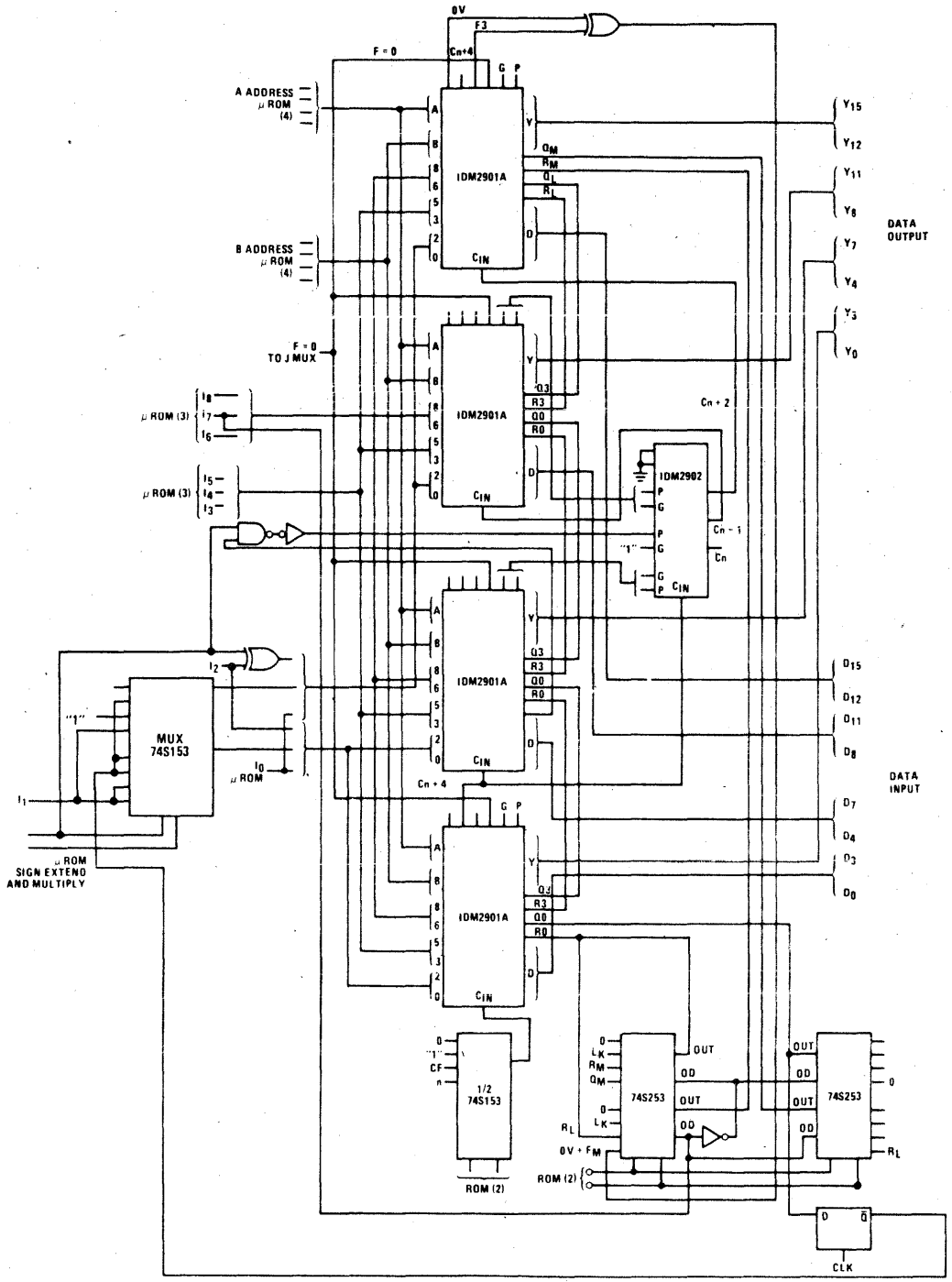


Figure 8. 16-Bit Register/ALU Design

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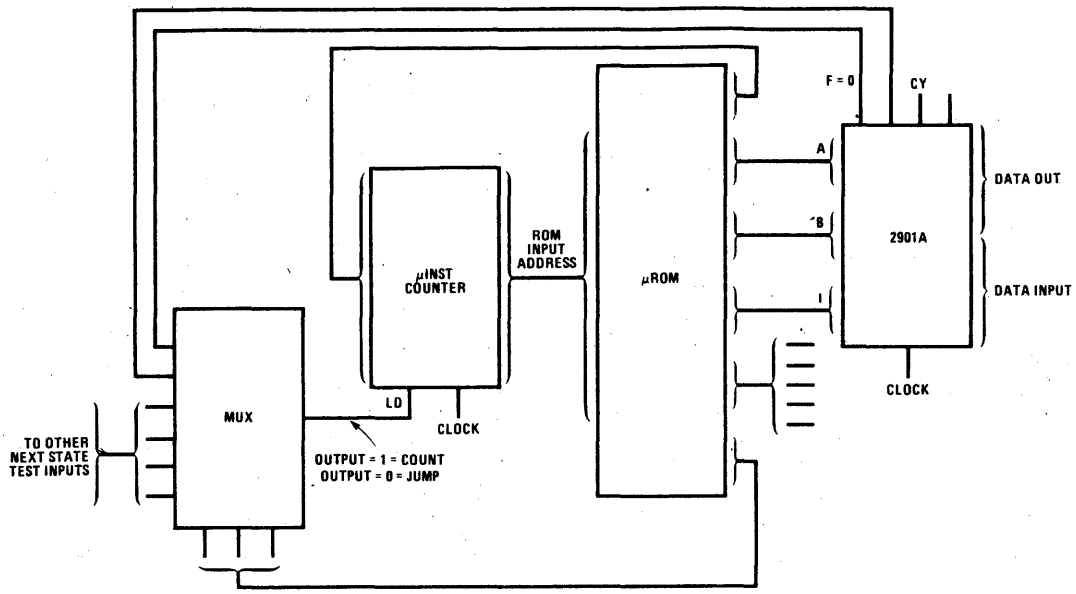


Figure 9. The Simple Microcontroller

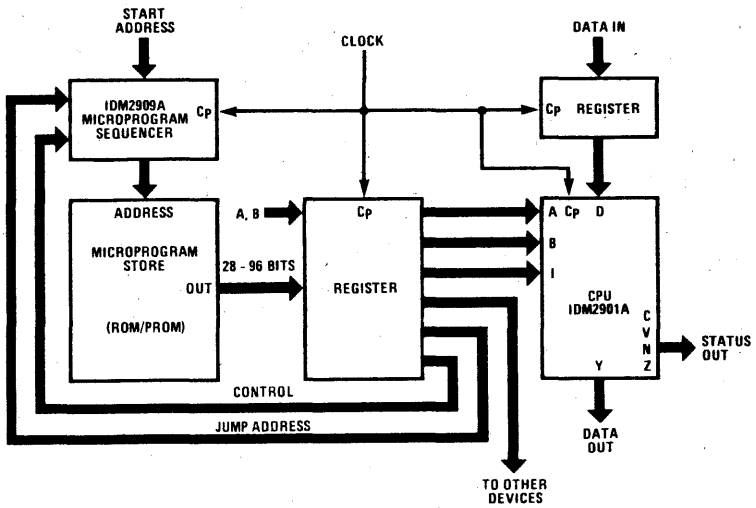


Figure 10. Microprogrammed Architecture Around IDM2901s

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Bit-Slice Microprocessor Design Takes a Giant Step Forward with "Schottky-Coupled-Logic" Circuits

Figure 12. Microsequencer Controller for Pipeline Prediction

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Simplify CRT Terminal Design with the DP8350

National Semiconductor
Application Note 198
Helge H. Mortensen
March 1978



INTRODUCTION

This application note is a description of a "low cost" CRT data terminal card design, based upon National's CRT Controller (DP8350) and 8-bit N-channel microprocessor (SC/MP). The terminal has a minimum parts count and implements all TTY functions. Even with this minimum number of parts, the terminal provides some "smart" features by efficiently utilizing the available hardware. Screen scroll, RS-232C interface and adjustable baud-rate (up to 1200-baud) are featured on the card. Higher baud-rates are available on a word-by-word basis if the RS-232-handshake signal is used. The design also demonstrates use of 2 new microprocessor-interface parts: the Asynchronous Communications Element (ACE), for serial I/O; and the RAM Input/Output (RAM I/O), for keyboard scanning and scratch pad memory. A 2-kilobyte video RAM is implemented with four 1024 x 4-bit, static RAM chips (MM2114), and dot generation uses the DM8678 5 x 7 Character Generator.

The card is self-contained except for the CRT monitor and power supply. It holds a keyboard and monitor-interface circuitry. Monitors requiring separate video and sync signals (Ball Brothers), and those requiring composite video (Motorola) are accommodated.

System Architecture

Since system cost is typically somewhat proportional to parts count, arriving at a minimum parts count solution has been a goal throughout this design effort.

A full-blown CRT terminal is shown in *Figure 1* and its low cost counterpart in *Figure 2*. Address decoding details are omitted in both cases.

Removing overhead circuitry shown in *Figure 1*, and making use of the TRI-STATE® concept greatly facilitated the parts reduction effort.

Obviously, extreme time conflicts for communicating on the system busses are created because all essential parts require access. Let us investigate this problem a little further.

Because the CRT Controller does the CRT display refresh function, it must have access to a memory containing current data for display. This memory may be a shift register (octal, 80-bit line buffer in *Figure 1*) which is loaded at the first video line in a character row and then recirculated for the number of video lines in that character row. Using such a line buffer allows the microprocessor access to the system busses for more than 90% of the video time (screen time). On the other hand, by removing the buffer, the refresh circuit needs direct memory access (DMA) during video display time.

However, with the bidirectional data buffer and the TRI-STATE address buffer in the system, the situation is not yet too serious. (We are only preventing the SC/MP microprocessor from updating video RAM data or using the scratch pad during character display time.) Instruction fetch (ROM) and keyboard scanning are still not affected. However, with the saving of the data buffer and the address buffer, a well-organized "time share" of the busses is required. How does this limited bus access affect the time-critical features such as scroll and high baud rate?

Scroll

Several scrolling methods may be implemented with the CRT Controller. The most straightforward is a rewrite of memory. This requires long processing time and bus access and is not feasible with the minimum hardware indicated in *Figure 2*. Sensing when the CRT is scanning character-row 24 and then loading a new "row start" requires additional overhead circuitry. An alternative approach is to load a new "top of page" address for each scroll and have the video RAM "wrapped-around" when it is accessed by the CRT!

In the latter approach, the processor only has to clear a row in video RAM and load a register in the CRT Controller to perform a total-screen scroll. The only problem remaining is handling the location of the scratch pad in the video RAM address space. By using the RAM I/O chip for a keyboard scanning and scratch pad RAM, the problem is solved. An additional feature for the software programmer is that the keyboard and RAM are addressable within the reach of one 8-bit index register.

Maximizing Communication Baud Rate

Assuming that the processor has bus access only during the vertical blanking period and the ACE interrupt service subroutine is executed in less than this time, only one received data word could be processed per frame! The processor's task is to transfer the word from ACE to scratch pad memory, check for terminal or system control functions, write into the proper locations in video RAM and check the keyboard for "Break" (BRK). A quick calculation reveals 60 bits/second as the maximum baud rate! To improve communication speed, the processor must have bus access during the video frame scan time. Three of the 10 scan lines making up a character row are blanked except during cursor time. Using these three lines (minimum decoding required) for processor bus access during video time allows us to communicate at 1200 baud.

Note that the baud rate is limited by the frame rate in the first approach; in the second approach, the limitation is the real time required to execute the service routine. The calculation is performed as follows. Estimated execution time for service routine with 100% availability of the bus is 2 ms. However, bus access is only granted during 3 video lines in each character row which is worth 192 μs. In terms of video time, we need 10 character rows to finish the routine and be ready for the next interrupt. Display time for 10 character rows is 6.4 ms, which in turn is the time interval for one 10-bit word. This translates into a 1600-baud maximum capability if scroll is not included in the service routine.

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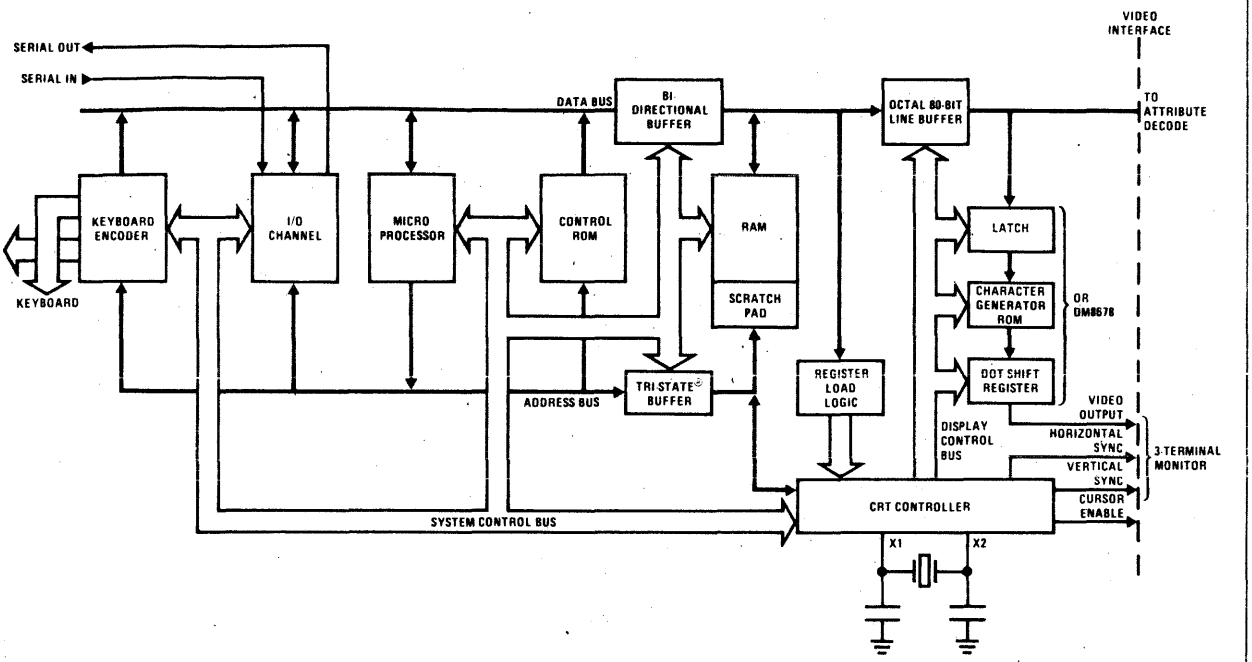


FIGURE 1. System Block Schematic Using Line Buffer, Address and Data Buffer

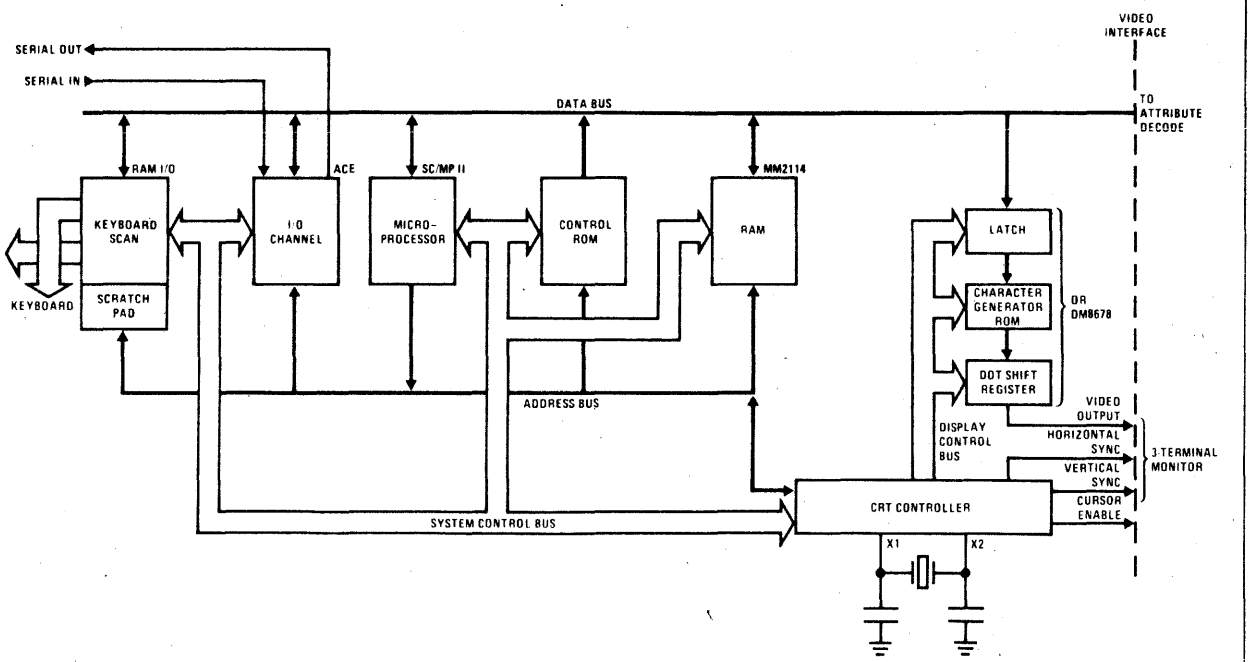


FIGURE 2. System Block Schematic for the Low Cost Terminal

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Address Decoding

Holding parts to a minimum leads to a one ROM address decoding scheme. However, this does not coincide with minimum cost. Instead, 2 low-power Schottky MSI devices replace the ROM in the final design.

Memory Address Space Utilization

A very simple decoding scheme is facilitated by partitioning the processor memory space into 500-byte pages. The detailed memory map is shown in *Figure 3*. In addition, address bits 12 and 13 (multiplexed on the data bus), are used to map four 4-kilobyte pages, with the first page dedicated to processor peripherals and the following 3 pages dedicated to register loading of the CRT Controller. The 3 CRT Controller registers to be loaded are "top of page", "row start" and "cursor".

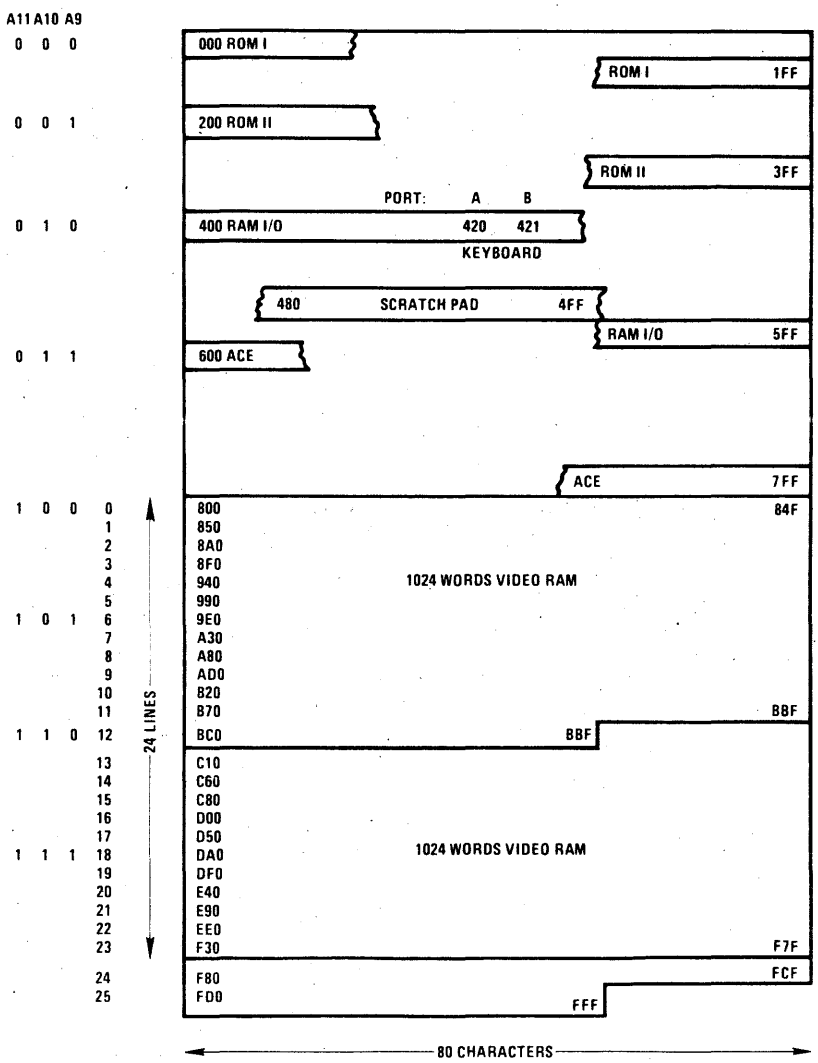


FIGURE 3. Memory Map

DISCUSSION OF SPECIFICATIONS

A device used to communicate with a computer is called interactive if it has the following properties:

a. Data may be entered on a keyboard and sent to the computer, which in turn echoes it back to the display.

b. Data may be received from the computer and displayed; keyboard is scanned for "Break" (BRK) entry by the operator of the system.

The concept of an interactive terminal is illustrated by the block diagram shown in *Figure 4*. To understand this, follow the data from the keyboard to the display and list the specifications for each block. An overall terminal specification is depicted in Table I.

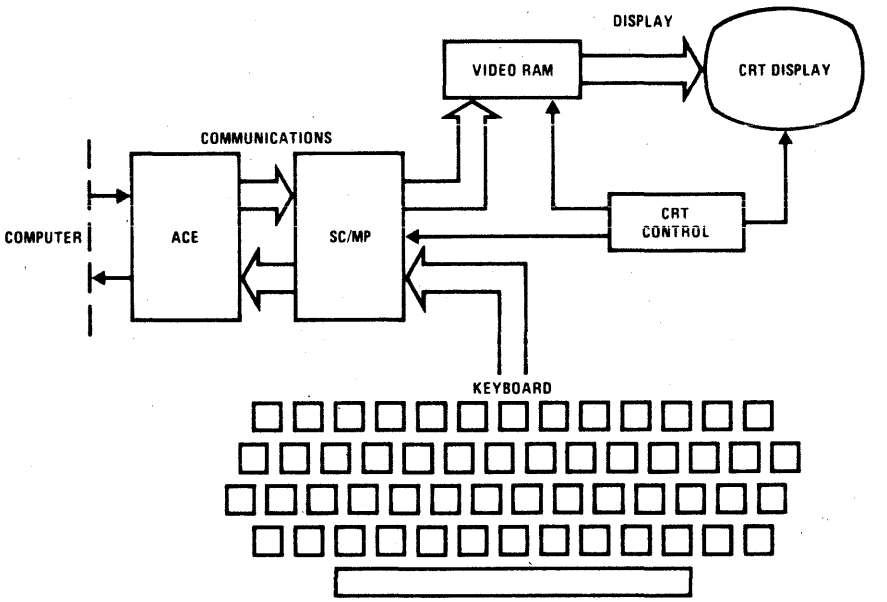


FIGURE 4. Block Diagram of an Interactive Terminal

TABLE I. TERMINAL SPECIFICATIONS

Keyboard	
Style	Typewriter
Characters/code set	64/ASC II
Cursor controls	6
Keyboard encoder	Software
Communication	
Mode	Full duplex, half duplex option
Technique	Asynchronous
Communications protocol	ASC II
Code	ASC II
Bits/character	10/11
Speed, bits/second	110 to 1200 (19,200 word-by-word)
Operator selectable speeds	4
Format	Character
Terminal interface	RS-232, 20 mA current loop
Display	
Display positions, characters/display	1920
Display arrangement (line x characters)	24 x 80
Total display symbols	64
Symbol formation	5 x 7 dot matrix
Reverse video	Cursor and whole screen
Scrolling	Yes
Cursor type	Block, reverse video
Cursor position	Down, left, right, home and return, back space.

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Keyboard

The keyboard is a copy of a standard teletypewriter with two-key rollover. The 54 keys can be broken into alphanumeric, punctuation, symbols, cursor control, and system control keys. The processor scans the keys at all times and translates any key closure into a unique code (ASC II), which is sent to the input/output channel for serial transmission to the computer. It should be noted that the RAM I/O chip has the capability of scanning 64 keys (8 x 8).

Communications

The input/output channel is based upon the Asynchronous Communication Element (ACE). This integrated circuit performs parallel-to-serial conversion of the data received from the keyboard, and serial-to-parallel conversion of data sent from the computer for display on the screen. When the system is initiated (power-up), the on-chip programmable baud generator is loaded with the desired baud rate (switch selectable). Start, stop, and parity bits are appended or deleted in this block of the system, depending on the direction of data flow. All control signals for the standard RS-232C interface are likewise generated here. Standard electrical specifications for RS-232C and 20 mA current loop are met by adding dedicated interface parts.

Display

After the data is received from the computer, it is stored in the video RAM. The CRT Controller chip refreshes the display at 60 Hz by sequentially addressing the video RAM; 1920 addresses are generated to fetch data for 24 lines of 80 characters. The standard 64-character ASC II set is displayed using a 5 x 7 dot-matrix block for each character. Data is entered from left to right and from top to bottom, until the screen is full. After that, upward scrolling with top-line overflow and newly cleared bottom line takes place automatically with line feed.

Software

A detailed flow chart of the software is shown in *Figure 5*. It is set up to service 3 major functions: a) initialize the system; b) scan the keyboard and c) service the ACE upon interrupt request.

a. Initialization
   The video RAM is cleared and the cursor is loaded at the upper left corner of the screen. ACE is set up with the desired baud rate and the interrupt enable flag is armed.

b. Keyboard Scan
   The keyboard is first checked for "Any Key Down" status. If positive, the keyboard is scanned and the binary code (ASC II) is computed by the program and read to ACE.

c. ACE Interrupt Service Routine
   When its receiver buffer is full, the ACE puts out an interrupt request. The SC/MP immediately suspends keyboard scanning and reads the buffer register. The main portion of this routine is checking incoming data for control functions and updating the video RAM and the CRT Controller registers. It should be noted that the need for executing this routine is the limiting factor for high baud rate communications.

Hardware

The detailed hardware implementation is shown in *Figure 6*. The CRT Controller grants the SC/MP microprocessor bus access during blanked scanlines and vertical blanking interval by logically OR-ing line counter outputs with the vertical blanking pulse and using this signal as a bus-available signal. The CRT Controller is held off the bus by disabling the TRI-STATE address output. This is done by applying logical "0" to the RAM address enable pin of the CRT Controller, the SC/MP then takes the bus as needed.

Sense-A of SC/MP is used as an interrupt request input whenever received data is available in the receiver buffer register of the ACE. The interrupt service routine is executed during vertical blanking and "inactive" video time as indicated above.

The keyboard is sensed for "Any Key Down" (under program control) by reading Port-B of the RAM I/O chip. Upon a positive result, the keys are scanned by a special sequence for key identification and encoding.

Mechanical

A PC board layout and its assembly is shown in *Figure 7*. Note that the keyboard is mounted directly on the card.

Acknowledgment

The development of the terminal involved significant contribution by a large number of people. The author would particularly like to express his appreciation to Len Bryson for software development and Dana Knight for invaluable suggestions and ideas during the hardware design phase.

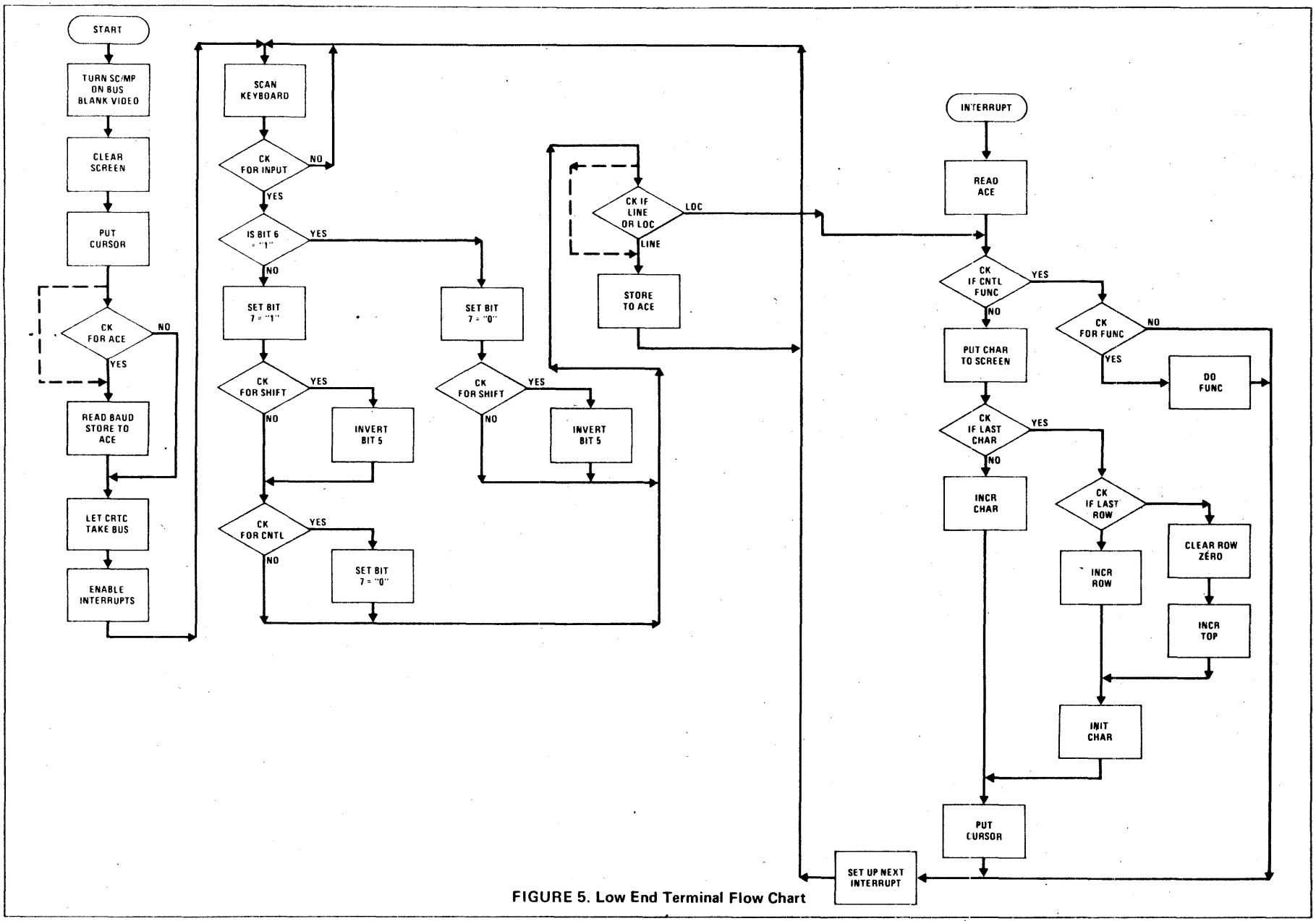


FIGURE 5. Low End Terminal Flow Chart

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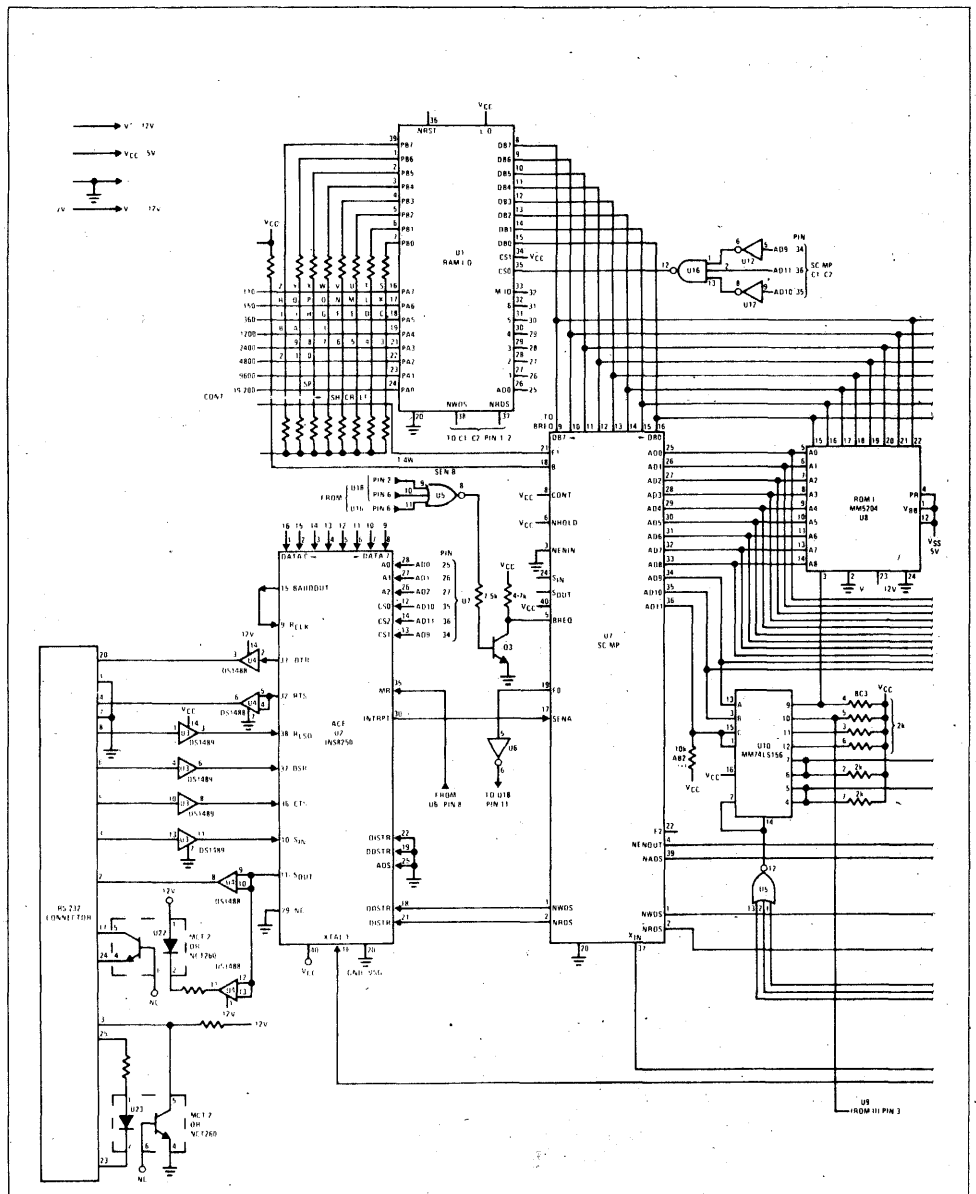


FIGURE 6. Low Cost CRT Terminal

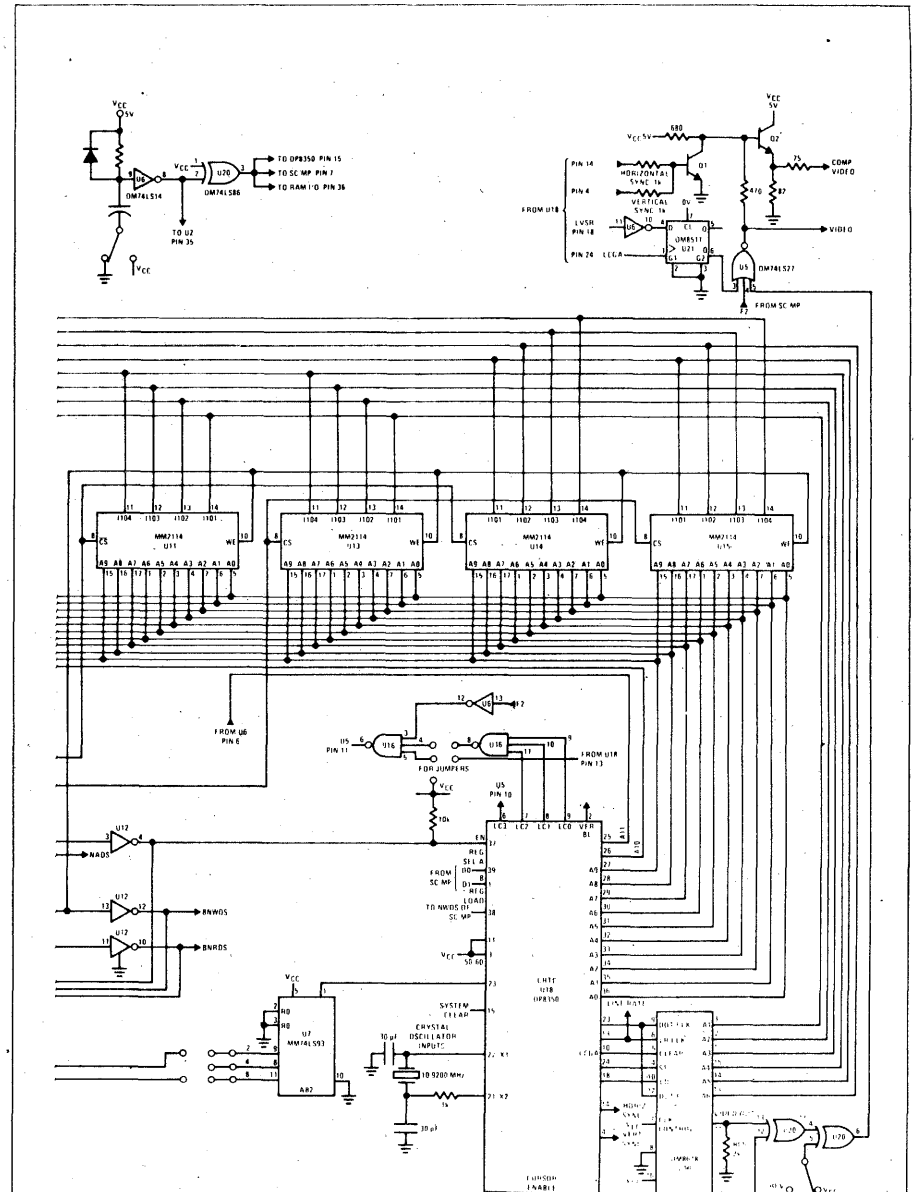


FIGURE 6. Low Cost CRT Terminal (Continued)

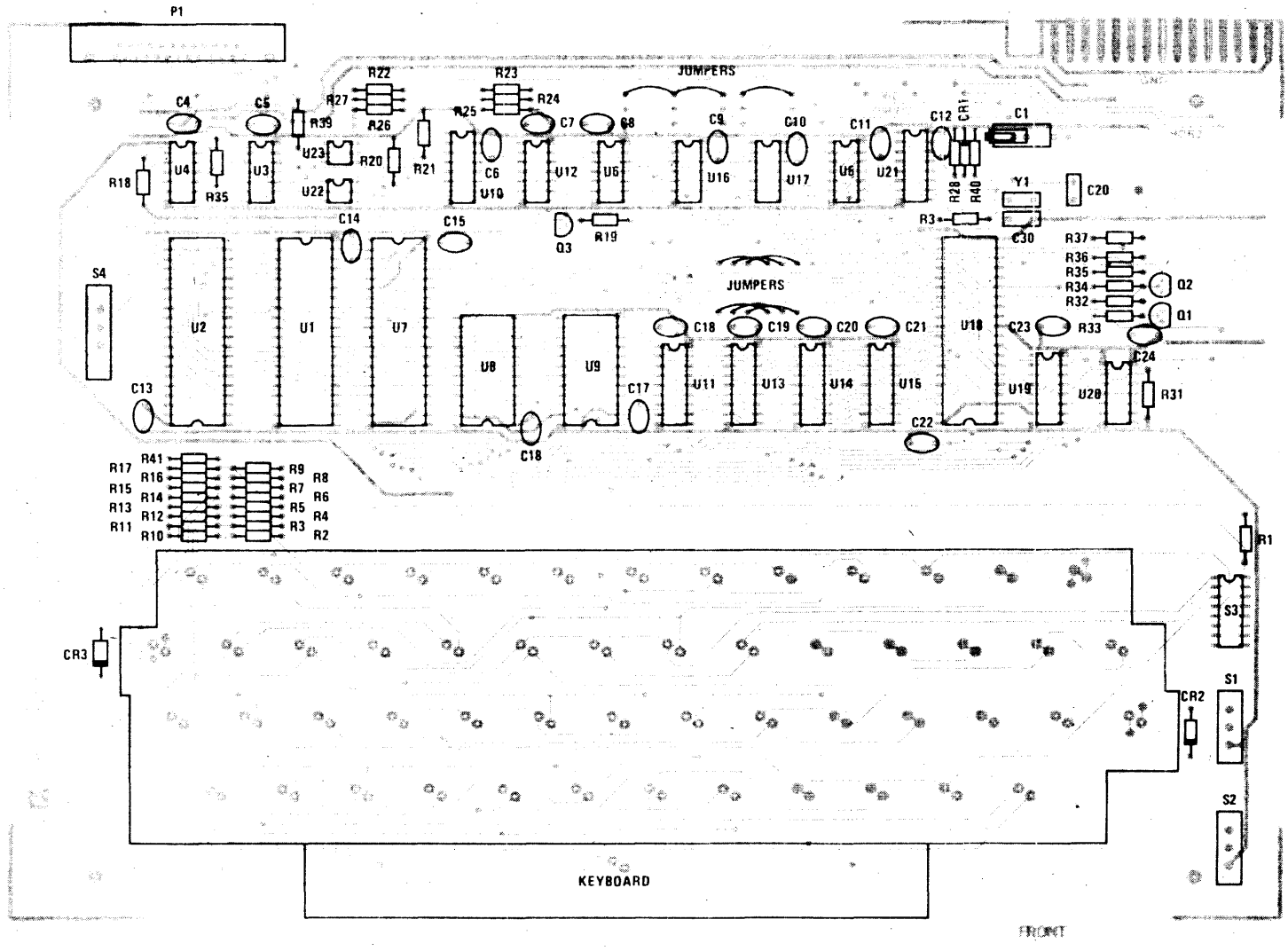


FIGURE 7A. PC Board Layout Assembly (Shown Half Size)

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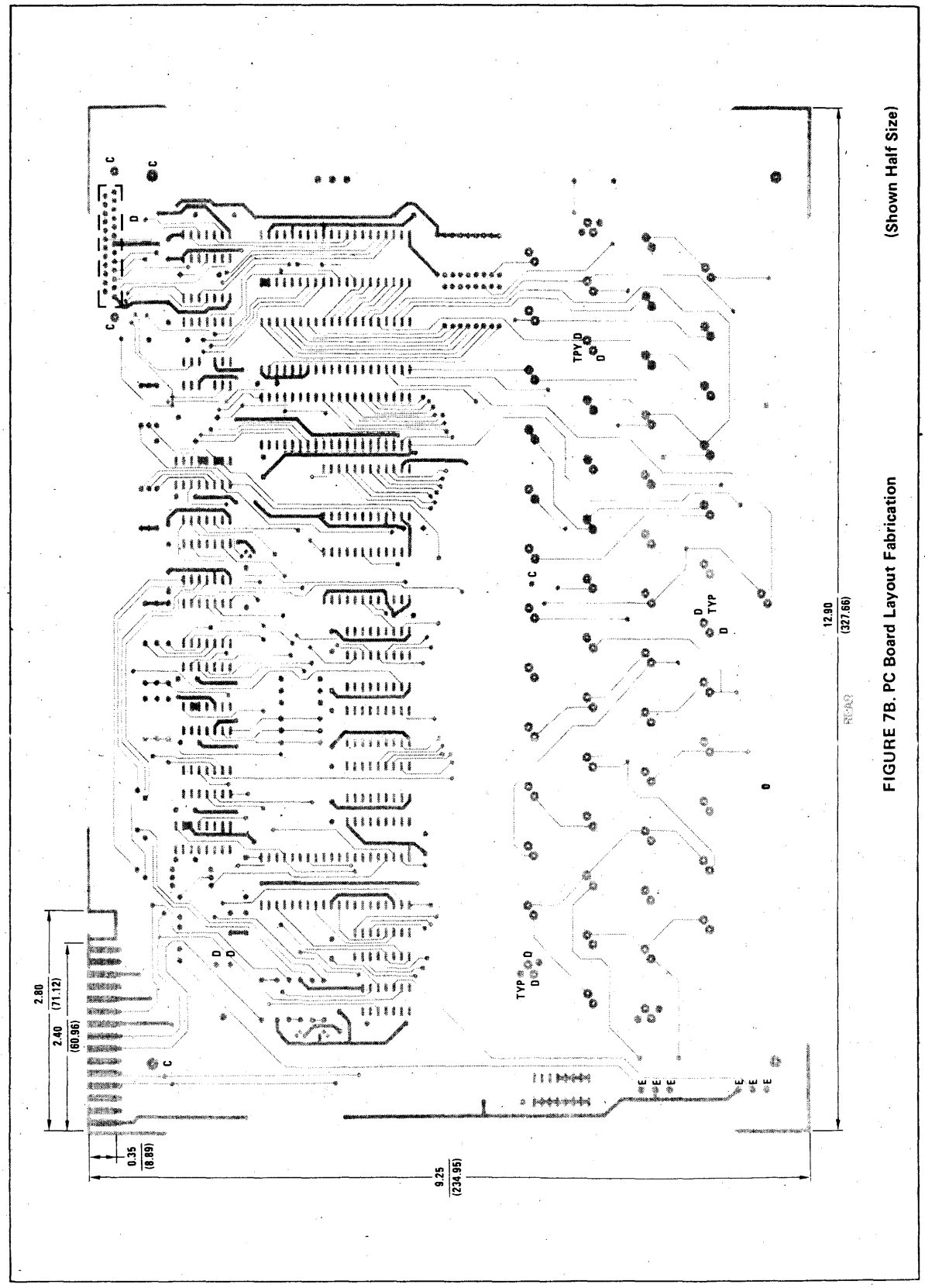


FIGURE 7B. PC Board Layout Fabrication (Shown Half Size)

National Semiconductor Corporation
2900 Semiconductor Drive
Santa Clara, California 95051
Tel: (408) 737-5000
TWX: (910) 339-9240

National Semiconductor GmbH
8000 München 21
61-2 Feldkirchenerstrasse
West Germany
Tel: 089-9 1502
Telex: 05-22772

NS International Inc., Japan
Miyake Building
1—9 Yotsuya, Shinjuku-ku, 160
Tokyo, Japan
Tel: (03) 355-3711
TWX: 232-2015 NSCJ J

NS Electronics (Hong Kong) Ltd.
8th Floor
Cheung Kong Electronic Bldg.
4 Hing Yip Street
Kwun Tong
Kowloon, Hong Kong
Tel: 3-411241-8
Telex: 73866 NSEHK HX
Cable: NATSEMI

NS Electronics Do Brasil
Avda Brigadeiro Faria Lima 844
11 Andar Conjunto 1104
Jardim Paulistano
Sao Paulo, Brasil
Telex: 1121008 CABINE SAO PAULO

NS Electronics Pty. Ltd
Cnr. Stud Rd. & Mtn. Highway
Bayswater, Victoria 3153
Australia
Tel: 03 729 6333
Telex: 32096

National does not assume any responsibility for use of any circuitry described, no circuit patent licenses are implied, and National reserves the right, at any time without notice, to change said circuitry.

"LAST PAGE THIS SECTION, NEXT PAGE 401"

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ABBREVIATIONS OF COMPANY NAMES

AD	Analog Devices
AMD	Advanced Micro Devices
AMI	American Microsystems, Inc.
Amperex	Amperex Electronics Corp.
Analogic	Analogic Corp.
Beckman	Beckman Instruments, Helipot Division
BEI	BEI Electronics
Burr-Brown	Burr-Brown Research
Cermetek	Cermetek
Cherry	Cherry Semiconductor
CMA	Consumer Microcircuits of America
Cybernetic	Cybernetic Micro Systems
Data General	Data General
Datel	Datel Systems
DDC	Data Devices Corp.
Delco	Delco Electronics
Dionics	Dionics Inc.
EA	Electronic Arrays
EMM/Semi	EMM Semi, Div. of Electronic Memories & Magnetics
Essex	Essex International
Exar	Exar Integrated Systems
Fairchild	Fairchild
Ferranti	Ferranti Electric
Fujitsu	Fujitsu
GI	General Instrument
Harris	Harris Semiconductor
Hitachi	Hitachi America Ltd.
Holt	Holt Inc.
Hughes	Hughes Aircraft Solid State Products
Hybrid Sys	Hybrid Systems
HyComp	HyComp
IMI	International Microcircuits, Inc.
Intech/FMI	Intech/Function Modules Inc.
Intel	Intel
Interdesign	Interdesign
Intersil	Intersil
IPI	Integrated Photomatrix, Inc.
Lambda	Lambda Electronics
LSI	LSI Computer Systems
Maruman	Maruman Integrated Circuits
Master Logic	Master Logic
Matrox	Matrox Electronics Systems
Micro Net	Micro Networks
Micropac	Micropac Industries
Micro Power	Micro Power Systems
Micro Tech	Microcircuits Technology
Mitel	Mitel Semiconductor
Mitsubishi	Mitsubishi Electric Co.
MMI	Monolithic Memories, Inc.
Monosil	Monosil
MOS	MOS Technology
Mostek	Mostek
Motorola	Motorola Semiconductor
National	National Semiconductor
NCR	NCR Corp., Microelectronics Division
NEC America	NEC America
NEC Micro	NEC Microcomputers
Nitron	Nitron
Nortec	Nortec Electronics
Novonics	Novonics
NPC	Nucleonic Products Co.
OEI	Optical Electronics, Inc.
OKI	OKI Semiconductor
Panasonic	Panasonic, Matsushita Electric Corp.
Photo Therm	Photo Therm
Plessey	Plessey Semiconductors
PMI	Precision Monolithics, Inc.
Raytheon	Raytheon Semiconductor
RCA	RCA Solid State Division
Reticon	Reticon
RIFA	RIFA
Rockwell	Rockwell Microelectronic Devices
RTC	Real Time Corp.
Sanken	Sanken Electric
Sanyo	Sanyo Electric
SGS	SGS-Ates Semiconductor
Siemens	Siemens
Signetics	Signetics (Philips)
Silicon G	Silicon General
Siliconix	Siliconix
Silicon Sys.	Silicon Systems, Inc.
Silitronics	Silitronics
SMC	Standard Microsystems
Solitron	Solitron Devices
Sprague	Sprague Electric Company
Supertex	Supertex, Inc.
SSM	Solid State Microtechnology for Music
SSS	Solid State Scientific
Synertek	Synertek
Telaris	Telaris
Teledyne C	Teledyne Crystalonics
Teledyne P	Teledyne Philbrick
Teledyne S	Teledyne Semiconductor
Telefunken	AEG-Telefunken
TI	Texas Instruments
TMX	TMX
Toshiba	Toshiba
Trans-Data	Trans-Data
TRW	TRW
Unitrode	Unitrode
Western	Western Digital
Zilog	Zilog

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INTRODUCTION TO DIGITAL

The Master Selection Guide provides sufficient information to make initial product selections. It enables you to find the products which are most appropriate to fulfill your major requirements and then provides data for many of the more important products.

All devices that appear in this section, both in the initial selection guide and in the data pages, are included in all other indexes.

The first two pages of the digital section present comparisons of the performance of the major digital families to help you choose between families. These are followed by lists of the devices in each family arranged into functional groups (arithmetic, buffers/inverters, etc.). The initial selection lists are followed by the device data pages which have been provided for you by the manufacturers. When such data is in the book, the page numbers are given with the initial selection listings.

Some digital circuits — calculator, watch chips, and electronic organ circuits — are not included in this section, but are covered in detail in the Linear-Consumer section. Digital circuits which do not fall into one of the major logic families are listed at the end of the selection information under the heading Digital-Other Devices.

This section is not complicated by reference to package styles; the package style suffixes are usually deleted. For more information on each companies' suffixes, see the Part Number Guide. Throughout the Master Selection Guide, each full military temperature range (−55°C to 125°C) device is indicated by a dagger (†) before the manufacturer's name. Manufacturers' names are normally spelled out; however, a few are abbreviated and the abbreviations are explained on page 306.

Page Number Index — Digital Devices

	CMOS	ECL10K	ECL95K	ECL100K	ECL III	HNIL/	TTL
Arithmetic Functions	404	418		421		423	425
Buffers/Inverters	404	418				423	427
Counters							
Binary	405	418	420		421	423	429
Decade	406	418	420		421	423	431
Miscellaneous	407			421	421		433
Decoders	408	418		421		423	433
Drivers	408	418		421		423	435
Flip-Flops	409	418	420	421	421	423	436
Gates	409	418					
AND/NAND	409	418				423	440
AND-OR/AND-OR-Invert	410			421		423	444
Exclusive OR/NOR	411	418	420	421	421	424	445
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Miscellaneous	412					424	447
Latches	412	419	420	421	421	424	447
Memories	413	419		421			448
Multiplexers (Digital)	414	420		421		424	449
Multivibrators	414	420			421	424	452
Oscillators/Dividers	414						
Shift Registers	415	420	420	421	421	424	453
Translators	416	420	420			424	455
Miscellaneous	416	420	420	421	421	424	455
Digital-Special (PMOS, Low voltage CMOS, etc.)							

Detailed Product Information provided by:

American Microsystems Inc.	466	Plessey Semiconductors	512
Fairchild Semiconductor	472	Raytheon Semiconductor	521
LSI Computer Systems	494	Signetics	561
Monolithic Memories, Inc.	495	Solid State Microtechnology for Music	564

The manufacturers listed above are providing detailed information on their latest and most significant products.

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WHICH DIGITAL FAMILY?

Edited from material published in Fairchild Progress magazine, Peter Alfke, author.

With several digital families available, the logical question is — which are the best ICs for my particular application?

To answer the question, you need to evaluate the pros and cons of the various logic families. These tradeoffs are listed in Tables I-IV. You will need to establish your speed requirements. Since speeds are characterized by the clock rate of registers and counters, this discussion is divided into four groups based on clock rates.

Very High Speed	Clock Rate	> 100 MHz	ECL
High Speed	Clock Rate	30 to 100 MHz	ECL, S-TTL
Medium Speed	Clock Rate	5 to 50 MHz	LS-TTL, TTL
Low Speed	Clock Rate	< 5 MHz	LS-TTL, CMOS

VERY HIGH SPEED SYSTEMS — Clock Rate > 100 MHz

There is only one reasonable IC logic family for use in very high speed systems — Emitter Coupled Logic, ECL. Originally, this technology presented considerable electrical problems such as voltage and temperature sensitivity and fast edge rates that caused reflection and cross-talk problems. In recent years, however, ECL development has become more user-oriented and there is better compatibility between circuit characteristics and interconnection techniques.

The modern popular ECL line is the 10,000 Series, manufactured in uncompensated, in voltage-compensated, or in both voltage and temperature-compensated forms. The latter form of compensation assures that significant parameters such as logic levels, noise margins and speed remain constant over a wide range of temperature and power supply voltage. These 10K and 95K logic circuits have deliberately slowed-down edge rates to make them easier to use and they can also drive terminated transmission lines whenever required by the interconnection length.

HIGH SPEED SYSTEMS — Clock Rate 30 to 100 MHz (Table II)

Here, you have a choice between ECL and Schottky TTL. H-TTL is really obsolete since it consumes more power than Schottky TTL, has similar interconnection problems and offers only half the speed. Also, it is not significantly faster than the best Low Power Schottky TTL. So, this narrows down your choice to ECL and Schottky TTL.

MEDIUM SPEED SYSTEMS — Clock Rate 5 to 50 MHz (Table III)

Standard TTL has been the obvious choice for medium speed systems for many years. Many designs will increasingly use Low Power Schottky TTL as it becomes more available, multiple sourced, and as the price premium decreases. You can mix standard and LS-TTL to solve most fan-out problems.

SLOW SPEED SYSTEMS — Clock Rate < 5 MHz (Table IV)

If you design slow speed systems you are faced with the largest number of attractive alternatives. Traditionally, TTL and DTL has been used. Now you can save power, cost and avoid heat and reliability problems by changing to LS-TTL, without affecting the logic design and perhaps not even changing the PC board layout.

If the system speed permits, you can switch to CMOS and save even more power and simplify the power supply, but now you must cope with a family of different logic elements and a hodgepodge of MSI elements, far less systems oriented than the better TTL circuits. Also you will notice wide parameter differences between the "same" products from different vendors.

The greatest challenge, however, is to examine the traditional hard-wired system design and decide whether or not it can be implemented with a microprocessor. If the requirements are both complicated and slow enough, this approach might save manufacturing cost, design time, and service time, as well as improve reliability, provide additional flexibility, and perhaps allow additional features at no extra cost.

MOS (p-channel, n-channel, either metal or silicon gate, also silicon on sapphire) does not compete directly with LS-TTL and CMOS. The MOS logic elements (gates and flip-flops) are very small but the input and output buffers are so large and relatively slow that MOS cannot be cost/performance competitive at MSI complexity (below 200 gates). MOS is therefore meaningful only in LSI circuits, where it has proven to be not only competitive, but dominating. These areas are:

- LSI memories, RAMs, ROMs, and shift registers of 500 to 4096 bits at clock rates below 5 MHz.
- Specialized, inherently slow LSI functions produced in very large volume (calculators, clocks, some instrument circuits like DVMs).
- Custom LSI circuits where the manufacturing volume is high enough or the weight/space saving valuable enough to absorb the development cost.
- Microprocessors, where a very carefully designed, standard circuit performs specialized tasks through ROM-stored programming.

SUMMARY

The proliferation of digital circuits and technologies gives you a new degree of freedom, but it also challenges your judgement and imagination. You are faced with an almost overwhelming number of competing technologies, each with its strong and weak points. The basic component speed requirement and the available power will quickly narrow your choice down to two or three different logic families; the tables presented here will make your final decision easier.

You should not forget, however, that the component speed requirement is also affected by your choice of architecture. A parallel approach requires more, but slower components, while a serial architecture requires fewer but faster components. The vesatility of modern MSI circuits makes it easy to explore these alternatives. It is very important to choose the IC logic family at an early stage in the system design, since the full cost, speed and reliability advantages can only be gained by designing in accordance with the device features, taking advantage of their logic and organization.

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TABLE I: COMPARISON OF ELECTRICAL CHARACTERISTICS

	CMOS 5 V SUPPLY	CMOS 10 V SUPPLY	STANDARD TTL	74LS LOW POWER SCHOTTKY	9LS LOW POWER SCHOTTKY	SCHOTTKY TTL	10K ECL
PROPAGATION DELAY	35 ns	25 ns	10 ns	10 ns	5 ns	3 ns	2 ns
FLIP-FLOP TOGGLE FREQUENCY	5 MHz	10 MHz	35 MHz	40 MHz	80 MHz	100 MHz	200 MHz
QUIESCENT POWER[1]	10 nW	10 nW	10 mW	2 mW	2 mW	25 mW	25 mW
NOISE IMMUNITY	2 V	4 V	1 V	0.8 V	0.8 V	0.9 V	0.2 V
FAN OUT (within family)	$> 50^2$	$> 50^2$	10	20	20	10	> 50

[1]Note the change from nanowatts to milliwatts.
[2]Or as determined by allowable propagation delay.

TABLE II. COMPARISON OF DIGITAL LOGIC FAMILY CHARACTERISTICS FOR HIGH SPEED SYSTEMS (CLOCK RATE 30 TO 100 MHz)

10K AND 95K SERIES ECL	SCHOTTKY TTL
Advantages	**Disadvantages**
Short delays allow propagation through more logic levels in a clock cycle. Compatibility with even faster families currently in development makes future system upgrading easy.	Component delays are about twice as long as with ECL and will not be improved in the foreseeable future.
Low output impedance drives all types of interconnections including terminated transmission lines.	Outputs are not capable of driving terminated transmission lines without causing severe fan-out compromises.
High output drive capability and complementary outputs accommodate differential transmission over tested pairs.	
Slow edge rate minimizes reflection problems.	Has the fastest output transitions of any logic family, causing reflection problems even with relatively short interconnection lengths, and causing cross-talk problems.
Complementary outputs on many elements add design flexibility.	
Wired-OR capability simplifies logic design.	
Compensated circuits simplify power supply and temperature regulation.	Generates fast power supply load changes, requires good decoupling.
High input impedance minimizes loading, allows high fan-out.	Input thresholds and output low levels are slightly offset from conventional TTL, causing some loss of noise immunity.
Disadvantages	**Advantages**
Unfamiliar type of circuitry, logic, nomenclature, and pinouts.	Compatible with popular TTL, same supply voltage, almost identical signal levels, same SSI and MSI logic, nomenclature, pinouts. Ideal to speed up critical paths in standard TTL systems.
Not level-compatible with TTL and CMOS, requires additional interface elements.	
Requires external pull-down resistors on all used outputs.	Outputs require no pull-up (or down) resistors.
Has less absolute noise margin.	Large signal swing and large absolute noise immunity cause less problems with temperature or supply voltage variations and gradients, resistive drops along supply lines, and outside noise.
Higher ground current requires heavier distribution busses.	
Has one less logic pin per package due to double ground.	
Has higher power consumption at low frequencies than equivalent S-TTL circuits.	Has lower system power consumption at moderate speed.

TABLE III. COMPARISON OF DIGITAL LOGIC FAMILY CHARACTERISTICS FOR MEDIUM SPEED SYSTEMS (CLOCK RATE 5 TO 50 MHz)

STANDARD TTL	LOW POWER SCHOTTKY TTL
Advantages	**Disadvantages**
Large number of SSI and MSI functions.	Somewhat fewer devices but this is changing.
Low prices.	Presently higher priced than standard TTL.
Specifications standardized.	Electrical characteristics differ between suppliers.
Disadvantages	**Advantages**
High power consumption (10 mW per gate, 200 to 500 mW per MSI package.)	Saves 75% of the power of equivalent standard TTL.
Large, heavy, expensive, hot power supply and regulator.	Smaller, lighter, cheaper, cooler power supply and regulator.
Heat density problems when using predominantly MSI.	No heat density problem. Cooler, therefore more reliable.
	May eliminate the need for fans and filters.
Not fully compatible with most CMOS and MOS.	Compatible with CMOS and MOS.
	Generates less noise than standard TTL.

TABLE IV. COMPARISON OF DIGITAL LOGIC FAMILY CHARACTERISTICS FOR LOW SPEED SYSTEMS (CLOCK RATE 5 MHz)

STANDARD OR LOW POWER SCHOTTKY TTL	CMOS
Advantages	**Disadvantages**
Well designed, system-oriented MSI.	Some of the original CMOS circuits are poorly defined and not systems oriented.
Adequate speed, tight tolerances.	Low speed, delays depend on supply voltage and capacitive loading.
Low impedance outputs give good immunity against capacitively coupled noise.	Poor current noise immunity (capacitively coupled noise.)
Familiar functions, logic, pinouts.	New functions, logic pinouts.
Standard TTL available from many suppliers, low cost.	Large parameter variations between different vendors.
Disadvantages	**Advantages**
Relatively high static consumption and heat generation.	Extremely low static power consumption, very little heat generated at moderate speed.
Tight power supply voltage requirements (5 V ±5% commercial, ±10% military grade).	Very wide range of supply voltages (theoretically 3 . . . 20 V, practically 5 . . . 12 V).
Not well-suited for portable battery operation.	Ideally suited for battery operation.
More expensive power supply.	Low cost power supply. Less cost, weight, heat, size than for any other family.
Lower voltage noise immunity.	High voltage noise immunity, an advantage with inductively coupled noise.
LS-TTL available from only a few suppliers.	Available from many suppliers.

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DIGITAL–CMOS

Arithmetic Functions

Function	Device	Source	Line
2 x 2 Bit (Parallel) Binary Multiplier	MC14554BA	† Motorola	
	MC14554BC	Motorola	
4-Bit Full Adder	F4008BC	Fairchild	
	F4008BM	† Fairchild	
	MC14008BA	† Motorola	
	MC14008BC	Motorola	
	MM54C83	† National	
	MM74C83	National	10
	CD4008BC	National	
	CD4008BM	† National	
	MSM4008	OKI	
	CD4008A	† RCA	
	CD4008AE	RCA	
	CD4008B	† RCA	
	CD4008BE	RCA	
	HBF4008AE	SGS	
	SCL4008B	† SSS	
	SCL4008BE	SSS	20
	CM4008A	† Solitron	
	CM4008AE	Solitron	
	TP4008A/B	TI	
	TC4008B	Toshiba	
Dual Full Adder	MSM580	OKI	
Triple Serial Adder (Positive Logic) with Internal Carry	MC14032BA	† Motorola	
	MC14032BC	Motorola	
	MSM4032	OKI	30
	CD4032A	† RCA	
	CD4032AE	RCA	
	CD4032B	† RCA	
	CD4032BE	RCA	
	CM4032A	† Solitron	
	CM4032AE	Solitron	
	TC4032B	Toshiba	
Triple Serial Adder (Negative Logic) with Internal Carry	MC14038BA	† Motorola	
	MC14038BC	Motorola	40
	MSM4038	OKI	
	CD4038A	† RCA	
	CD4038AE	RCA	
	CD4038B	† RCA	
	CD4038BE	RCA	
	CM4038A	† Solitron	
	CM4038AE	Solitron	
	TC4038B	Toshiba	
4-Bit Arithmetic Array	CD4057A	† RCA	50
4-Bit Arithmetic Logic Unit	MC14581BA	† Motorola	
	MC14581BC	Motorola	
	CD40181B	† RCA	
	CD40181BE	RCA	
	SCL4581B	† SSS	
	SCL4581BE	SSS	
	TP4581A	TI	
Look-Ahead Carry Block	F4582BC	Fairchild	60
	F4582BM	† Fairchild	
	MC14582BA	† Motorola	
	MC14582BC	Motorola	
	CD40182B	† RCA	
	CD40182BE	RCA	
	SCL4582B	SSS	
	TP4582A	TI	

Arithmetic Functions (Cont'd.)

Function	Device	Source	Line
4-Bit Magnitude Comparator	F40085BC	Fairchild	
	F40085BM	† Fairchild	70
	MC14585BA	† Motorola	
	MC14585BC	Motorola	
	MM54C85	† National	
	MM74C85	National	
	μPD4063B	NEC America	
	MSM582	OKI	
	MSM4063	OKI	
	MSM4585	OKI	
	CD4063B	† RCA	
	CD4063BE	RCA	80
	SCL4585B	† SSS	
	SCL4585BE	SSS	
	TC4063B	Toshiba	
	TC4585B	Toshiba	
NBCD Adder (Natural Binary Coded Decimal)	MC14560BA	† Motorola	
	MC14560BC	Motorola	
	μPD4560B	NEC America	
	TC4560B	Toshiba	
Nines Complementer	MC14561BA	† Motorola	90
	MC14561BC	Motorola	
	μPD4561B	NEC America	
	TC4561B	Toshiba	
Data Path Switch	F4704BC	Fairchild	
	F4704BM	† Fairchild	
Arithmetic Logic Register Stack	F4705BC	Fairchild	
	F4705BM	† Fairchild	100
Data Access Register (for memory address arithmetic)	F4707BC	Fairchild	
	F4707BM	† Fairchild	

Buffers/Inverters

Function	Device	Source	Line
Quad Low Impedance Buffer	SCL4441UB	† SSS	
	SCL4441UBE	SSS	
Quad Buffer, Three-State (Non-Inverting)	TC5024	Toshiba	
	TC5025	Toshiba	
Hex Buffer	MSM509	OKI	110
Hex Buffer/Converter (Non-Inverting)	SIL4010B	† Mitel	
	SIL4010BE	Mitel	
	CD4010AC	National	
	CD4010AM	† National	
	CD4010A	† RCA	
	CD4010AE	RCA	
	CD4010B	† RCA	
	CD4010BE	RCA	120
	HBF4010BE	SGS	
	SCL4010B	† SSS	
	SCL4010BE	SSS	
	CM4010A	† Solitron	
	CM4010AE	Solitron	
	TP4010A/B	† TI	
	TC4010B	Toshiba	
Hex Buffer/Converter (Non-Inverting)-Improved	F4050BC	Fairchild	
	F4050BM	† Fairchild	130
	SIL4050B	† Mitel	

(Continued)

Buffers/Inverters (Cont'd.)

Function	Device	Source	Line
Hex Buffer/Converter (Non-Inverting)-Improved (Cont'd.)	SIL4050BE	Mitel	
	MC14050BA	† Motorola	
	MC14050BC	Motorola	
	CD4050BC	National	
	CD4050BM	National	
	μPD4050B	NEC America	
	MSM4050	OKI	
	CD4050A	† RCA	140
	CD4050AE	RCA	
	CD4050B	† RCA	
	CD4050BE	RCA	
	HBF4050AE	SGS	
	SCL4050B	† SSS	
	SCL4050BE	SSS	
	CM4050A	† Solitron	
	CM4050AE	Solitron	
	TP4050A/B	TI	
	TC4050B	Toshiba	150
Hex Buffer, Open Drain (Active pull down)	MM54C906	† National	
	MM74C906	National	
Hex Buffer, Open Drain (Active pull up)	MM54C907	† National	
	MM74C907	National	
Hex Buffer, Three-State	F40097BC	Fairchild	
	F40097BM	† Fairchild	
	MC14503BA	† Motorola	160
	MC14503BC	Motorola	
	CD4503BC	National	
	CD4503BM	† National	
	MM70C95	† National	
	MM70C97	† National	
	MM80C95	National	
	MM80C97	National	
	μPD4503B	NEC America	
	TC5012B	Toshiba	
Hex TTL Buffer (Non-Inverting)(CMOS to TTL)	MM54C902	† National	170
	MM74C902	National	
Hex PMOS Buffer (Non-Inverting) (PMOS to CMOS or TTL)	MM54C904	† National	
	MM74C904	National	
Hex High Voltage Buffer	TC5064	Toshiba	
	TC5065	Toshiba	
Hex Buffer/Converter (Inverting)	SIL4009B	† Mitel	180
	SIL4009BE	Mitel	
	CD4009AC	National	
	CD4009AM	† National	
	CD4009A	† RCA	
	CD4009AE	RCA	
	CD4009UB	† RCA	
	CD4009UBE	RCA	
	HBF4009AE	SGS	
	SCL4009UB	† SSS	190
	SCL4009UBE	SSS	
	CM4009A	† Solitron	
	CM4009AE	Solitron	
	TP4009A/UB	TI	
	TC4009UB	Toshiba	
Hex Buffer/Converter (Inverting)-Improved	F4049BC	Fairchild	

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Values

Bold face indicates additional data is provided on the page noted.

DIGITAL–CMOS (Cont'd)

Buffers/Inverters (Cont'd.)

Function	Device	Source	Line
Hex Buffer/Converter (Inverting)-Improved (Cont'd.)			
	F4049BM	† Fairchild	
	SIL4049B	† Mitel	
	SIL4049BE	Mitel	
	MC14049UBA	† Motorola	
	MC14049UBC	Motorola	
	CD4049UBC	National	
	CD4049UBM	† National	
	µPD4049B	NEC America	
	MSM4049	OKI	10
	CD4049A	† RCA	
	CD4049AE	RCA	
	CD4049UB	† RCA	
	CD4049UBE	RCA	
	HBF4049AE	SGS	
	SCL4049UB	† SSS	
	SCL4049UBE	SSS	
	CM4049A	† Solitron	
	CM4049AE	Solitron	
	TP4049A/UB	TI	20
	TC4049B	Toshiba	
Hex Inverter			
	F4069UBC	Fairchild	
	F4069UBM	† Fairchild	
	SIL4069B	† Mitel	
	SIL4069BE	Mitel	
	MC14069UBA	† Motorola	
	MC14069UBC	Motorola	
	CD4069C	National	
	CD4069M	† National	30
	MM54C04	† National	
	MM74C04	† National	
	µPD4069B	NEC America	
	MSM508	OKI	
	MSM4069	OKI	
	CD4069UB	† RCA	
	CD4069UBE	RCA	
	SCL4069UB	† SSS	
	SCL4069UBE	SSS	
	SCL4449UB	† SSS	40
	SCL4449UBE	SSS	
	CM4069A	† Solitron	
	CM4069AE	Solitron	
	TP4069A/UB	TI	
	TP4315A	TI	
	TC4069UB	Toshiba	
Hex Inverter, Three-State			
	F40098BC	Fairchild	
	F40098BM	† Fairchild	
	MM70C96	† National	50
	MM80C96	National	
	MM70C98	† National	
	MM80C98	National	
Hex Inverter/Buffer, Three-State, Strobed			
	SIL4502B	† Mitel	
	SIL4502BE	Mitel	
	MC14502BA	† Motorola	
	MC14502BC	Motorola	
	MSM4502	OKI	
	CD4502B	† RCA	60
	CD4502BE	RCA	
	SCL4502B	† SSS	
	SCL4502BF	SSS	
Hex TTL Buffer (Inverting)(CMOS to TTL)			
	MM54C901	† National	
	MM74C901	National	

Buffers/Inverters (Cont'd.)

Function	Device	Source	Line
Hex PMOS Buffer (Inverting)(PMOS to CMOS or TTL)			
	MM54C903	† National	
	MM74C903	National	
Hex CMOS Compatible Buffer			70
	DS1630	† National	
	DS3630	National	
Dual Complementary Pair plus Inverter			
	F4007UBC	Fairchild	
	F4007UBM	† Fairchild	
	SIL4007B	† Mitel	
	SIL4007BE	† Mitel	
	MC14007UBA	† Motorola	
	MC14007UBC	Motorola	
	CD4007C	National	80
	CD4007M	† National	
	MSM4007	OKI	
	CD4007A	† RCA	
	CD4007AE	RCA	
	CD4007UB	† RCA	
	CD4007UBE	RCA	
	HBF4007AE	SGS	
	SCL4007UB	† SSS	
	SCL4007UBE	SSS	
	CM4007A	† Solitron	90
	CM4007AE	Solitron	
	TP4007A/UB	TI	
	TC4007UB	Toshiba	
Quad True/Complement Buffer			
	F4041BC	Fairchild	
	F4041BM	† Fairchild	
	CD4041C	National	
	CD4041M	National	
	CD4041A	† RCA	
	CD4041AE	RCA	100
	CD4041UB	† RCA	
	CD4041UBE	RCA	
	SCL4041UB	† SSS	
	SCL4041UBE	SSS	
	CM4041A	† Solitron	
	CM4041AE	Solitron	
7-Line High Voltage Buffer			
	TC5066B	Toshiba	
	TC5067B	Toshiba	

Counters, Binary

Function	Device	Source	Line
Divide by 2, 8 or 16 Counter			110
	MM54C93	† National	
	MM74C93	National	
5, 6, 7, 8, 9-Stage Binary Counter			
	MSM5577	OKI	
	TC5048	Toshiba	
7-Stage Binary Counter			
	F4024BC	Fairchild	
	F4024BM	† Fairchild	
	SIL4024B	† Mitel	
	SIL4024BE	Mitel	120
	MC14024BA	† Motorola	
	MC14024BC	Motorola	
	CD4024BC	National	
	CD4024BM	† National	
	µPD4024B	NEC America	
	MSM4024	OKI	
	CD4024A	† RCA	
	CD4024AE	RCA	
	CD4024B	† RCA	
	CD4024BE	RCA	130
	HBF4024AE	SGS	

(Continued)

Counters, Binary (Cont'd.)

Function	Device	Source	Line
7-Stage Binary Counter (Cont'd.)			
	SCL4024B	† SSS	
	SCL4024BE	SSS	
	CM4024A	† Solitron	
	CM4024AE	Solitron	
	TP4024A/B	TI	
	TC4024B	Toshiba	
8-Stage Synchronous Binary Counter			
	SCL4404B	† SSS	140
	SCL4404BE	SSS	
10, 11, 12, 13, 14-Stage Binary Counter			
	MSM5576	OKI	
12-Stage Binary Counter			
	F4040BC	Fairchild	
	F4040BM	† Fairchild	
	SIL4040B	† Mitel	
	SIL4040BE	Mitel	
	MC14040BA	† Motorola	
	MC14040BC	Motorola	150
	CD4040BC	National	
	CD4040BM	† National	
	µPD4040B	NEC America	
	MSM4040	OKI	
	MSM5507	OKI	
	CD4040A	† RCA	
	CD4040AE	RCA	
	CD4040B	† RCA	
	CD4040BE	RCA	
	SCL4040B	† SSS	160
	SCL4040BE	SSS	
	CM4040A	† Solitron	
	CM4040AE	Solitron	
	TP4040A/B	TI	
	TC4040B	Toshiba	
14-Stage Binary Counter			
	F4020BC	Fairchild	
	F4020BM	† Fairchild	
	MC14020BA	† Motorola	
	MC14020BC	Motorola	170
	SIL4020B	† Mitel	
	SIL4020BE	Mitel	
	CD4020BC	National	
	CD4020BM	† National	
	µPD4020B	NEC America	
	MSM4020	OKI	
	MSM5508	OKI	
	CD4020A	† RCA	
	CD4020AE	RCA	
	CD4020B	† RCA	180
	CD4020BE	RCA	
	HBF4020AE	SGS	
	SCL4020B	† SSS	
	SCL4020BE	SSS	
	CM4020A	† Solitron	
	CM4020AE	Solitron	
	TP4020A/B	TI	
	TC4020B	Toshiba	
14-Stage Binary Counter and Oscillator			
	SIL4060B	† Mitel	190
	SIL4060BE	Mitel	
	CD4060BC	National	
	CD4060BM	† National	
	CD4060A	† RCA	
	CD4060AE	RCA	
	CD4060B	† RCA	
	CD4060BE	RCA	
	SCL4060B	† SSS	

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Values

DIGITAL–CMOS (Cont'd)

Counters, Binary (Cont'd.)

Function	Device	Source	Line
14-Stage Binary Counter and Oscillator (Cont'd.)			
	SCL4060BE	SSS	
14, 15, 16-Stage Binary Counter (with reset)			
	MSM5562	OKI	
	TC5036	Toshiba	
16, 17, 18-Stage Binary Counter			
	MSM5580	OKI	
16, 17, 18-Stage Binary Counter (with reset)			
	MSM5564	OKI	
16, 17, 19-Stage Binary Counter (with reset)			10
	MSM5563	OKI	
19-Stage Binary Counter			
	MSM5583	OKI	
Presettable 4-Stage Binary Counter			
	MSM5536	OKI	
Presettable Synchronous Binary Counter, Asynchronous Clear			
	F40161BC	Fairchild	
	F40161BM	† Fairchild	
	MC14161BA	† Motorola	20
	MC14161BC	Motorola	
	CD40161BC	National	
	CD40161BM	† National	
	MM54C161	† National	
	MM74C161	National	
	CD40161B	† RCA	
	CD40161BE	RCA	
	SCL4161B	† SSS	
	SCL4161BE	SSS	
	TP4361A	TI	30
	TC49161B	Toshiba	
Presettable Fully Synchronous Binary Counter, Synchronous Clear			
	F40163BC	Fairchild	
	F40163BM	† Fairchild	
	MC14163BA	† Motorola	
	MC14163BC	Motorola	
	CD40163BC	National	
	CD40163BM	† National	
	MM54C163	† National	40
	MM74C163	National	
	CD40163B	† RCA	
	CD40163BE	RCA	
	SCL4163B	† SSS	
	SCL4163BE	SSS	
	TP4363A	TI	
	TC40163B	Toshiba	
Dual Synchronous Binary Counter			
	F4520BC	Fairchild	
	F4520BM	† Fairchild	50
	HD14502B	Hitachi	
	SIL4520B	† Mitel	
	SIL4520BE	Mitel	
	MC14520BA	† Motorola	
	MC14520BC	Motorola	
	CD4520BC	National	
	CD4520BM	† National	
	µPD4520B	NEC America	
	MSM4520	OKI	
	CD4520B	† RCA	60
	CD4520BE	RCA	
	SCL4520B	† SSS	
	SCL4520BE	SSS	
	CM4520B	† Solitron	
	CM4520BE	Solitron	
	TP4520A	TI	

(Continued)

Counters, Binary (Cont'd.)

Function	Device	Source	Line
Dual Synchronous Binary Counter (Cont'd.)			
	TC4520B	Toshiba	
Presettable Binary Up/Down Counter			
	F40193BC	Fairchild	70
	F40193BM	† Fairchild	
	F4516BC	Fairchild	
	F4516BM	† Fairchild	
	HD14516B	Hitachi	
	SIL4516B	† Mitel	
	SIL4516BE	Mitel	
	MC14516BA	† Motorola	
	MC14516BC	Motorola	
	CD40193BC	National	
	CD40193BM	† National	80
	CD4516BC	National	
	CD4516BM	† National	
	MM54C193	† National	
	MM74C193	National	
	µPD4516B	NEC America	
	MSM4516	OKI	
	MSM5504	OKI	
	MSM40193	OKI	
	CD40193B	† RCA	
	CD40193BE	RCA	90
	CD4516B	† RCA	
	CD4516BE	RCA	
	SCL4193B	† SSS	
	SCL4193BE	SSS	
	SCL4516B	† SSS	
	SCL4516BE	SSS	
	TC4516B	Toshiba	
Presettable 8-bit Binary Down Counter			
	CD40103B	† RCA	
	CD40103BE	RCA	100
Programmable Binary Divide-by-N 4-Bit Counter			
	F4526BC	Fairchild	
	F4526BM	† Fairchild	
	MC14526BA	† Motorola	
	MC14526BC	Motorola	
	CD4526BC	National	
	CD4526BM	† National	
	µPD4526B	NEC America	
	SCL4526B	† SSS	
	SCL4526BE	SSS	110
	TP4526A	TI	
4-Bit Binary Counter/Clock Generator			
	TC5018B	Toshiba	
4-Bit Binary Counter/Divider			
	MSM5538	OKI	
	TC5027B	Toshiba	

Counters, Decade

Function	Device	Source	Line
Presettable Decade Counter			
	MSM5530	OKI	
Presettable Decade Counter (Sets to 0 or 9, divides by 2, 5 or 10)			120
	MM54C90	† National	
	MM74C90	National	
Presettable Synchronous Decade Counter, Asynchronous Clear			
	F40160BC	Fairchild	
	F40160BM	† Fairchild	
	MC14160BA	† Motorola	
	MC14160BC	Motorola	
	CD40160BC	National	

(Continued)

Counters, Decade (Cont'd.)

Function	Device	Source	Line
Presettable Synchronous Decade Counter, Asynchronous Clear (Cont'd.)			130
	CD40160BM	† National	
	MM54C160	† National	
	MM74C160	National	
	CD40160B	† RCA	
	CD40160BE	RCA	
	SCL4160B	† SSS	
	SCL4160BE	SSS	
	TP4360A	TI	
	TC40160B	Toshiba	140
Presettable Fully Synchronous Decade Counter, Synchronous Clear			
	F40162BC	Fairchild	
	F40162BM	† Fairchild	
	MC14162BA	† Motorola	
	MC14162BC	Motorola	
	CD40162BC	National	
	CD40162BM	† National	
	MM54C162	† National	
	MM74C162	National	150
	CD40162B	† RCA	
	CD40162BE	RCA	
	SCL4162B	† SSS	
	SCL4162BE	SSS	
	TP4362A	TI	
	TC40162B	Toshiba	
Dual Synchronous Decade Counter			
	F4518BC	Fairchild	
	F4518BM	† Fairchild	
	SIL4518B	† Mitel	160
	SIL4518BE	Mitel	
	MC14518BA	† Motorola	
	MC14518BC	Motorola	
	CD4518BC	National	
	CD4518BM	† National	
	µPD4518B	NEC America	
	MSM4518	OKI	
	CD4518B	† RCA	
	CD4518BE	RCA	
	SCL4518B	† SSS	170
	SCL4518BE	SSS	
	CM4518B	† Solitron	
	CM4518BE	Solitron	
	TP4518A/B	TI	
	TC4518B	Toshiba	
Decade Counter/Divider, 10 line output			
	F4017BC	Fairchild	
	F4017BM	† Fairchild	
	HD14017B	Hitachi	
	SIL4017B	† Mitel	180
	SIL4017BE	Mitel	
	MC14017BA	† Motorola	
	MC14017BC	Motorola	
	CD4017BC	National	
	CD4017BM	† National	
	µPD4017B	NEC America	
	MSM4017	OKI	
	CD4017A	† RCA	
	CD4017AE	RCA	
	CD4017B	† RCA	190
	CD4017BE	RCA	
	HBF4017AE	SGS	
	SCL4017B	† SSS	
	SCL4017BE	SSS	
	CM4017A	† Solitron	
	CM4017AE	Solitron	
	TP4017A	TI	
	TC4017B	Toshiba	

† Military Temperature Range (−55° to 125°C)

* Typical Values

Bold face indicates additional data is provided on the page noted.

DIGITAL–CMOS (Cont'd)

Counters, Decade (Cont'd.)

Function	Device	Source	Line
Presettable Decade Up/Down Counter			
	F40192BC	Fairchild	
	F40192BM	† Fairchild	
	F4510BC	Fairchild	
	F4510BM	† Fairchild	
	HCTR0200	Hughes	
	SIL4510B	† Mitel	
	SIL4510BC	Mitel	
	MC14510BA	† Motorola	
	MC14510BC	Motorola	
	CD40192BC	National	10
	CD40192BM	† National	
	CD4510BC	National	
	CD4510BM	† National	
	MM54C192	† National	
	MM74C192	National	
	µPD4510B	NEC America	
	MSM4510	OKI	
	MSM5503	OKI	
	MSM5505	OKI	
	MSM40192	OKI	20
	CD40192B	† RCA	
	CD40192BE	RCA	
	CD4510B	† RCA	
	CD4510BE	RCA	
	SCL4192B	† SSS	
	SCL4192BE	SSS	
	SCL4510B	† SSS	
	SCL4510BE	SSS	
	TC4510B	Toshiba	
Presettable 2-Decade Down Counter			30
	CD40102B	† RCA	
	CD40102BE	RCA	
Programmable Decade Divide-By-N 4-Bit Counter			
	F4522BC	Fairchild	
	F4522BM	† Fairchild	
	MC14522BA	† Motorola	
	MC14522BC	Motorola	
	CD4522BC	National	
	CD4522BM	† National	
	µPD4522B	NEC America	40
	SCL4522B	† SSS	
	SCL4522BE	SSS	
	TP4522A	TI	
Presettable Decade Counter/Decoder/Driver			
	TC5034	Toshiba	
4-Decade Divide-by-N Counter			
	CD4059A	† RCA	
	MSM4059	OKI	
	CD4059AE	RCA	
Presettable Up/Down Decade Counter-7 Segment Display and BCD Output			50
	HCTR0200	Hughes	
Decade Counter/Divider-7 Segment Display Output and Display Enable			
	CD4026A	† RCA	
	CD4026AE	RCA	
	CD4026B	† RCA	
	CD4026BE	RCA	
	SCL4026B	† SSS	
	SCL4026BE	SSS	60
	SCL4426B	† SSS	
	SCL4426BE	SSS	
	CM4026A	† Solitron	
	CM4026AE	Solitron	

Counters, Decade (Cont'd.)

Function	Device	Source	Line
Decade Counter/Divider-7 Segment Display Output and Ripple Blanking			
	CD4033A	† RCA	
	CD4033AE	RCA	
	CD4033B	† RCA	
	CD4033BE	RCA	70
	HBF4033AE	SGS	
	SCL4033B	† SSS	
	SCL4033BE	SSS	
	SCL4433B	† SSS	
	SCL4433BE	SSS	
	CM4033A	† Solitron	
	CM4033AE	Solitron	
Decade Up/Down Counter/Decoder/Latch/Driver (direct 7-Segment driver)			
	CD40110B	† RCA	80
	CD40110BE	RCA	
Decade Counter/Latch/Decoder/Driver			
	MSM552	OKI	
	MSM5521	OKI	
	MSM5522	OKI	
Decade Up/Down Counter, Latch, Decoder, 7-Segment Display Output			
	CD40110B	RCA	
3-1/2 Digit Counter to BCD Driver			
	HCTR4010	Hughes	90
	HCTR6010	Hughes	
	CM4102	† Solitron	
	CM4102	Solitron	
3½ Digit Counter			
	MSM5500	OKI	
3-½ Digit Counter, Programmable			
	TC9122	Toshiba	
3 Decade Counter, Decoder, Driver			
	LC7960	Sanyo	
3 Decade Counter, Multiplexed Output			100
	F4553BC	Fairchild	
	F4553BM	† Fairchild	
	MC14553BA	† Motorola	
	MC14553BC	Motorola	
4 Decade Counter			
	TC5001B	Toshiba	
	MSM5501	OKI	
	MSM5502	OKI	
	TC5037B	Toshiba	
	TC5051B	Toshiba	110
	TC5052B	Toshiba	
4-Digit Up/Down Counter			
	MSM5512	Toshiba	
4 Decade Up/Down Counter With Timer			
	TC5010	Toshiba	
4 Decade Counter, Multiplexed Output (The 926 gives carry at 6000.)			
	MM74C925	National	
	MM74C926	National	
4 Digit Counter, Multiplexed Output, Second digit counts to 6 (Maximum count 9599.)			120
	MM74C927	National	
4 Digit Counter, Multiplexed Output, Left digit counts to 2 (Maximum count 1999.)			
	MM74C928	National	

Counters, Decade (Cont'd.)

Function	Device	Source	Line
4 Digit Up/Down Counter/Latch/Display Driver; Cascadable, Synchronous, Presettable, BCD output (versions have either common anode or cathode LED direct 7 segment and digit drivers; 9999 or 5959 count; hard wire control: 7217; processor control:7227; 5 V supply)			130
	ICM7217	Intersil	
	ICM7217A	Intersil	
	ICM7217B	Intersil	
	ICM7217C	Intersil	
	ICM7227	Intersil	
	ICM7227A	Intersil	
	ICM7227B	Intersil	
	ICM7227C	Intersil	
4-½ Digit Up Counter; direct 7 segment drivers, latched, decoder, count 1999 (7224-LCD; 7225-LED; "A" versions; count 15959)			140
	ICM7224	Intersil	
	ICM7224A	Intersil	
	ICM7225	Intersil	
	ICM7225A	Intersil	
4-1/2 Digit Up-Down Counter Oscillator (Maximum count 19999)			
	HCTR4010	Hughes	
	HCTR6010	Hughes	150
5 Channel, 4-Digit Dynamic Counter			
	MSM5511	OKI	
5 Decade Counter, Multiplexed Output			
	MC14534BA	† Motorola	
	MC14534BC	Motorola	
6-Digit Counter			
	TC5032	Toshiba	
Counter/Latch/Display Driver; direct 7 segment and digit drivers for common cathode LEDs; count 9,999,999; 2MHZ, 2-6 V supply			160
	ICM7208	Intersil	

Counters, Miscellaneous

See also CMOS Oscillators/Dividers; Digital-Special

Function	Device	Source	Line
Decade Counter/Divider			
	MSM551	OKI	
	TC5026B	Toshiba	
Presettable Up/Down Binary or Decade Counter			
	F4029BC	Fairchild	
	F4029BM	† Fairchild	
	SIL4029B	† Mitel	
	SIL4029BE	Mitel	170
	MC14029BA	† Motorola	
	MC14029BC	Motorola	
	CD4029BC	National	
	CD4029BM	† National	
	µPD4029B	NEC America	
	MSM4029	OKI	
	CD4029A	† RCA	
	CD4029AE	RCA	
	CD4029B	† RCA	
	CD4029BE	RCA	180
	HBF4029AE	SGS	
	SCL4029B	† SSS	
	SCL4029BE	SSS	
	CM4029A	† Solitron	
	CM4029AE	Solitron	
	TP4029A	TI	
	TC4029B	Toshiba	

† Military Temperature Range (−55° to 125°C)

* Typical Values

DIGITAL–CMOS (Cont'd)

Counters, Miscellaneous (Cont'd.)

Function	Device	Source	Line
Dual Programmable Divide-by-N Binary/Decade Counter			
	MC14569BA	**† Motorola (778)**	
	MC14569BC	**Motorola (778)**	
Divide-by-12 Counter			
	MSM5536	OKI	
Presettable Divide-by-12 Counter			
	MSM5531	OKI	
Divide-by-8-Counter/Divider, Decoded Output			
	F4022BC	Fairchild	
	F4022BM	† Fairchild	
	SIL4022B	† Mitel	10
	SIL4022BE	Mitel	
	MC14022BA	† Motorola	
	MC14022BC	Motorola	
	CD4022BC	National	
	CD4022BM	† National	
	MSM4022	OKI	
	CD4022A	† RCA	
	CD4022AE	RCA	
	CD4022B	† RCA	
	CD4022BE	RCA	20
	HBF4022AE	SGS	
	SCL4022B	† SSS	
	SCL4022BE	SSS	
	CM4022A	† Solitron	
	CM4022AE	Solitron	
	TP4022A	TI	
	TC4022B	Toshiba	
Divide-by-60-Counter, BCD Output (Industrial Time Base Generator)			
	MC14566BA	† Motorola	30
	MC14566BC	Motorola	
Presettable Divide-by-N Counter			
	F4018BC	Fairchild	
	F4018BM	† Fairchild	
	SIL4018B	† Mitel	
	SIL4018BE	Mitel	
	MC14018BA	† Motorola	
	MC14018BC	Motorola	
	CD4018BC	National	
	CD4018BM	† National	40
	CD4018A	† RCA	
	CD4018AE	RCA	
	CD4018B	† RCA	
	CD4018BE	RCA	
	HBF4018AE	SGS	
	SCL4018B	† SSS	
	SCL4018BE	SSS	
	CM4018A	† Solitron	
	CM4018AE	Solitron	
	TP4018A/B	TI	50
	TC4018B	Toshiba	
Programmable Divide-by-N Counter			
	TC5080	Toshiba	
Phase Comparator and Programmable Counters			
	MC14568BA	† Motorola	
	MC14568BC	Motorola	

Decoders

Function	Device	Source	Line
BCD-to-Decimal Decoder			
	F4028BC	Fairchild	
	F4028BM	† Fairchild	
	HD14028B	Hitachi	60
	SIL4028B	† Mitel	
	SIL4028BE	Mitel	

(Continued)

Decoders (Cont'd.)

Function	Device	Source	Line
BCD-to-Decimal Decoder (Cont'd.)			
	MC14028BA	† Motorola	
	MC14028BC	Motorola	
	CD4028BC	National	
	CD4028BM	† National	
	MM54C42	† National	
	MM74C42	National	
	µPD4028B	NEC America	70
	MSM564	OKI	
	CD4028A	† RCA	
	CD4028AE	RCA	
	MSM4028	OKI	
	CD4028B	† RCA	
	CD4028BE	RCA	
	HBF4028AE	SGS	
	SCL4028B	† SSS	
	SCL4028BE	SSS	
	CM4028A	† Solitron	80
	CM4028AE	Solitron	
	TP4028A/B	TI	
	TC4028B	Toshiba	
BCD-to-7-Segment Decoder			
	MC14558BA	† Motorola	
	MC14558BC	Motorola	
	MM54C48	† National	
	MM74C48	National	
	UCN-4102A	Sprague	
	TC5002B	Toshiba	90
BCD-to-7 Segment Decoder/Driver			
	MC14547BA	† Motorola	
	MC14547BC	Motorola	
4-bit Latch/4-to-16-Line Decoder (High)			
	F4514BC	Fairchild	
	F4514BM	† Fairchild	
	SIL4514BE	Mitel	
	SIL4514B	† Mitel	
	MC14514BA	† Motorola	
	MC14514BC	Motorola	100
	CD4514BC	National	
	CD4514BM	† National	
	µPD4514B	NEC America	
	MSM4514	OKI	
	CD4514B	† RCA	
	CD4514BE	RCA	
	SCL4514B	† SSS	
	SCL4514BE	SSS	
	CM4514B	† Solitron	
	CM4514BE	Solitron	110
	TC4514B	Toshiba	
4-bit Latch/4-to-16-Line Decoder (Low)			
	F4515BC	Fairchild	
	F4515BM	† Fairchild	
	HD14515B	Hitachi	
	SIL4515B	† Mitel	
	SIL4515BE	Mitel	
	MC14515BA	† Motorola	
	MC14515BC	Motorola	
	CD4515BC	National	120
	CD4515BM	† National	
	µPD4515B	NEC America	
	MSM4515	OKI	
	CD4515B	† RCA	
	CD4515BE	RCA	
	SCL4515B	† SSS	
	SCL4515BE	SSS	
	CM4515B	† Solitron	
	CM4515BE	Solitron	
	TC4515B	Toshiba	130

Decoders (Cont'd.)

Function	Device	Source	Line
Dual Binary to 1 of 4 Decoder/Demultiplexer (High)			
	F4555BC	Fairchild	
	F4555BM	† Fairchild	
	HD14555B	Hitachi	
	MC14555BA	† Motorola	
	MC14555BC	Motorola	
	µPD4555B	NEC America	
	MSM4555	OKI	
	CD4555B	† RCA	
	CD4555BE	RCA	140
	SCL4555B	† SSS	
	TC4555B	Toshiba	
Dual Binary to 1 of 4 Decoder/Demultiplexer (Low)			
	F4556BC	Fairchild	
	F4556BM	† Fairchild	
	MC14556BA	† Motorola	
	MC14556BC	Motorola	
	µPD4556B	NEC America	
	MSM4556	OKI	
	CD4556B	† RCA	150
	CD4556BE	RCA	
	SCL4556B	† SSS	
	SCL4556BE	SSS	
	TC4556B	Toshiba	
4-Line-to-16-Line Decoder/Demultiplexer			
	MM54C154	† National	
	MM74C154	National	
	MSM563	OKI	
1 of 8 Strobed Decoder			
	SCL4428B	† SSS	160
	SCL4428BE	SSS	
N-bit Decoder (for I/O Interface)			
	HCMP1853	† Hughes	
	CDP1853	† RCA	
	SCP1853	† SSS	

Drivers

Function	Device	Source	Line
BCD-to-7-Segment Latch/Decoder/Driver			
	F4511BC	Fairchild	
	F4511BM	† Fairchild	
	F4734BC	† Fairchild	
	F4734BM	Fairchild	170
	HD14511B	Hitachi	
	MC14511BA	† Motorola	
	MC14511BC	Motorola	
	MC14513BA	† Motorola	
	MC14513BC	Motorola	
	SIL4511B	† Mitel	
	SIL4511BE	Mitel	
	CD4511BC	National	
	CD4511BM	† National	
	µPD4511B	NEC America	180
	MSM561	OKI	
	MSM4511	OKI	
	CD4511B	† RCA	
	CD4511BE	RCA	
	SCL4511B	† SSS	
	SCL4511BE	SSS	
	CM4511B	† Solitron	
	CM4511BE	Solitron	
	TP4511B	TI	
	TC4511B	Toshiba	190
	TC5002B	Toshiba	
	TC5022B	Toshiba	
	TC5042B	Toshiba	

† Military Temperature Range (−55° to 125°C)

* Typical Values

Bold face indicates additional data is provided on the page noted.

DIGITAL–CMOS (Cont'd)

Function	Device	Source	Line
Drivers (Cont'd.)			
BCD(Hexadecimal) to 7-Segment Latch/Decoder/Driver			
	MD4311B	† Mitel	
	MD4311BE	Mitel	
	MD4568B	† Mitel	
	MD4568BE	Mitel	
	MC14495	**Motorola (786)**	
BCD-to-7-Segment Latch/Decoder/Driver (for Liquid Crystal Displays)			
	MC14543BA	† Motorola	
	MC14543BC	Motorola	
	CD4543BC	National	10
	CD4543BM	† National	
	MSM5621	OKI	
	SCL4543B	SSS	
	TC4543B	Toshiba	
BCD-to-7-Segment Liquid Crystal Decoder/Driver with "Display Frequency Output"			
	MD4055B	† Mitel	
	MD4055BE	Mitel	
	CD4055B	† RCA	
	CD4055BE	RCA	20
	TC4055B	Toshiba	
BCD-to-7-Segment Liquid Crystal Decoder/Driver with Strobed-Latch Function			
	MD4056B	† Mitel	
	MD4056BE	Mitel	
	CD4056B	† RCA	
	CD4056BE	RCA	
	TC4056B	Toshiba	
7-Segment to BCD Converter/Driver			
	MM54C915	† National	30
	MM74C915	National	
Display Driver, 4-Digit (stores segment and address data, drives 7-8 segment digits)			
	MM74C911	National	
4-Digit LED Driver, Multiplexed BCD or Binary to 7-Segment Decoder/Driver			
	ICM7212	Intersil	
	ICM7212A	Intersil	
4-Digit LED Driver, BCD or Binary to 7-Segment Decoder/Driver, data and digit select input latches for µP interface			40
	ICM7212M	Intersil	
	ICM7212AM	Intersil	
Display Driver, 6-Digit BCD (stores segment and address data, drives 7-8 segment digits)			
	MM74C912	National	
Display Driver, 6 Digit Hex (stores segment and address data, drives 7-segment digits)			
	MM74C917	National	
4-Line Liquid Crystal Display Driver			50
	MSM4054	OKI	
	CD4054B	† RCA	
	CD4054BE	RCA	
	TC4054B	Toshiba	
30-Bit Liquid Crystal Display with Register			
	MD4330B	† Mitel	
	MD4330BE	Mitel	
	MD4331B	† Mitel	
	MD4331BE	Mitel	
32-Bit LCD Driver with Register			60
	MD4332B	† Mitel	
	MD4332BE	Mitel	

Function	Device	Source	Line
Drivers (Cont'd.)			
4-Digit LCD Driver, Multiplexed BCD to LCD Decoder/Driver, AC Drive			
	ICM7211	Intersil	
	ICM7211A	Intersil	
	DF411	Siliconix	
	DF414	Siliconix	
4-Digit Multiplex Input LCD Driver			
	HLCD0437	Hughes	70
4-Digit Serial Input LCD Driver			
	HLCD0438	Hughes	
Dual High Voltage Driver, Source 250 ma			
	MM74C908	National	
	MM74C918	National	
Dual and Quad Line Drivers-See Miscellaneous			
Also See: Interface—Display Drivers, Memory and Peripheral Drivers			
Flip-Flops			
Dual "D" Flip-Flop			
	F4013BC	Fairchild	80
	F4013BM	† Fairchild	
	HD14013B	Hitachi	
	SIL4013B	† Mitel	
	SIL4013BE	Mitel	
	MC14013BA	† Motorola	
	MC14013BC	Motorola	
	CD4013BC	National	
	CD4013BM	† National	
	MM54C74	† National	
	MM74C74	National	90
	µPD4013B	NEC America	
	MSM530	OKI	
	CD4013A	† RCA	
	CD4013AE	RCA	
	MSM4013	OKI	
	CD4013B	† RCA	
	CD4013BE	RCA	
	HBF4013AE	SGS	
	SCL4013B	† SSS	
	SCL4013BE	SSS	100
	CM4013A	† Solitron	
	CM4013AE	Solitron	
	TP4013A/B	TI	
	TC4013B	Toshiba	
Quad "D" Flip-Flop			
	F40175BC	Fairchild	
	F40175BM	† Fairchild	
	HD14175B	Hitachi	
	MC14175BA	† Motorola	
	MC14175BC	Motorola	110
	MM54C175	† National	
	MM74C175	National	
	CD40175B	National	
	µPD4175B	NEC America	
	TC40175B	Toshiba	
Quad "D" Flip-Flop, Three-State			
	F4076BC	Fairchild	
	F4076BM	† Fairchild	
	SIL4076B	† Mitel	
	SIL4076BE	Mitel	120
	MC14076BA	Motorola	
	MC14076BC	Motorola	
	MM54C173	† National	
	MM74C173	National	
	CD4076BC	National	
	CD4076BM	† National	

(Continued)

Function	Device	Source	Line
Flip-Flops (Cont'd.)			
Quad "D" Flip-Flop, Three-State (Cont'd.)			
	CD4076B	† RCA	
	CD4076BE	RCA	
	SCL4076B	† SSS	130
	SCL4076BE	SSS	
	CM4076A	† Solitron	
	CM4076AE	Solitron	
	TC4076B	Toshiba	
Hex "D" Flip-Flop			
	F40174BC	Fairchild	
	F40174BM	† Fairchild	
	HD14174B	Hitachi	
	MC14174BA	† Motorola	
	MC14174BC	Motorola	140
	CD40174BC	National	
	CD40174BM	† National	
	MM54C174	† National	
	MM74C174	National	
	CD40174B	† RCA	
	CD40174BE	RCA	
	SCL4174B	† SSS	
	TP4370A	TI	
	TC40174B	Toshiba	
Octal "D" Flip-Flop			150
	MM54C374	† National	
	MM74C374	National	
Dual "J-K" Flip-Flop			
	F4027BC	Fairchild	
	F4027BM	† Fairchild	
	HD14027B	Hitachi	
	SIL4027B	† Mitel	
	SIL4027BE	Mitel	
	MC14027BA	† Motorola	
	MC14027BC	Motorola	160
	CD4027BC	National	
	CD4027BM	† National	
	MM54C76	† National	
	MM74C76	National	
	µPD4027B	NEC America	
	MSM531	OKI	
	CD4027A	† RCA	
	CD4027AE	RCA	
	MSM4027	OKI	
	CD4027B	† RCA	170
	CD4027BE	RCA	
	HBF4027AE	SGS	
	SCL4027B	† SSS	
	SCL4027BE	SSS	
	CM4027A	† Solitron	
	CM4027AE	Solitron	
	TP4027A/B	TI	
	TC4027B	Toshiba	
	TC7476B	Toshiba	
Dual "J-K" Flip-Flop w/o Preset			180
	MM54C73	† National	
	MM74C73	National	
	MM54C107	† National	
	MM74C107	National	
Gates, AND/NAND			
AND Gated "J-K" Flip-Flop			
	CD4095B	† RCA	
	CD4095BE	RCA	
	CD4096B	† RCA	
	CD4096BE	RCA	

† Military Temperature Range (−55° to 125°C)

* Typical Values

DIGITAL–CMOS (Cont'd)

Function	Device	Source	Line
Gates, AND/NAND (Cont'd.)			
8-Input AND Gate			
	SIL4968B	† Mitel	
	SIL4968BE	Mitel	
Dual 4-Input AND Gate			
	F4082BC	Fairchild	
	F4082BM	† Fairchild	
	HD14082B	Hitachi	
	SIL4082B	† Mitel	
	SIL4082BE	Mitel	
	MC14082BA	† Motorola	
	MC14082BC	Motorola	10
	μPD4082B	NEC America	
	MSM4082	OKI	
	CD4082B	† RCA	
	CD4082BE	RCA	
	SCL4082B	SSS	
	SCL4082BE	† SSS	
	TP4082B	TI	
	TC4082B	Toshiba	
Triple 3-Input AND Gate			
	F4073BC	Fairchild	20
	F4073BM	† Fairchild	
	HD14073B	Hitachi	
	SIL4073B	† Mitel	
	SIL4073BE	Mitel	
	MC14073BA	† Motorola	
	MC14073BC	Motorola	
	CD4073BC	National	
	CD4073BM	† National	
	μPD4073B	NEC America	
	MSM4073	OKI	30
	CD4073B	† RCA	
	CD4073BE	RCA	
	SCL4073B	† SSS	
	SCL4073BE	SSS	
	CM4073A	† Solitron	
	CM4073AE	Solitron	
	TP4073B	TI	
	TC4073	Toshiba	
Quad 2-Input AND Gate			
	F4081BC	Fairchild	40
	F4081BM	† Fairchild	
	HD14081B	Hitachi	
	SIL4081B	† Mitel	
	SIL4081BE	Mitel	
	MC14081BA	† Motorola	
	MC14081BC	Motorola	
	CD4081BC	National	
	CD4081BM	† National	
	MM54C08	† National	
	MM74C08	National	50
	μPD4081B	NEC America	
	MSM501	OKI	
	MSM4081	OKI	
	CD4081B	† RCA	
	CD4081BE	RCA	
	SCL4081B	† SSS	
	SCL4081BE	SSS	
	CM4081A	† Solitron	
	CM4081AE	Solitron	
	TP4081B	TI	60
	TC4081B	Toshiba	
8-Input NAND Gate			
	F4068BC	Fairchild	
	F4068BM	† Fairchild	
	HD14068B	Hitachi	
	SIL4068B	† Mitel	
	SIL4068BE	Mitel	
	MC14068BA	† Motorola	
		(Continued)	

Function	Device	Source	Line
Gates, AND/NAND (Cont'd.)			
8-Input NAND Gate		(Cont'd.)	
	MC14068BC	Motorola	70
	MM54C30	† National	
	MM74C30	National	
	μPD4068B	NEC America	
	MSM504	OKI	
	MSM4068	OKI	
	CD4068B	† RCA	
	CD4068BE	RCA	
	SCL4068B	† SSS	
	SCL4068BE	SSS	
	SCL4412B	† SSS	80
	SCL4412BE	SSS	
	CM4068A	† Solitron	
	CM4068AE	Solitron	
	TP4068B	TI	
	TC4068B	Toshiba	
Dual 4-Input NAND Gate			
	F4012BC	Fairchild	
	F4012BM	† Fairchild	
	HD14012B	Hitachi	
	SIL4012UB	† Mitel	90
	SIL4012UBE	Mitel	
	SIL4012B	† Mitel	
	SIL4012BE	Mitel	
	MC14012BA	† Motorola	
	MC14012BC	Motorola	
	MC14012UBA	† Motorola	
	MC14012UBC	Motorola	
	CD4012AC	National	
	CD4012AM	† National	
	MM54C20	† National	100
	MM74C20	National	
	μPD4012B	NEC America	
	MSM503	OKI	
	MSM4012	OKI	
	CD4012A	† RCA	
	CD4012AE	RCA	
	CD4012B	† RCA	
	CD4012BE	RCA	
	CD4012UB	† RCA	
	CD4012UBE	RCA	110
	HBF4012AE	SGS	
	SCL4012B	† SSS	
	SCL4012BE	SSS	
	CM4012A	† Solitron	
	CM4012AE	Solitron	
	TP4012A	TI	
	TC4012B	Toshiba	
	TC7420B	Toshiba	
Dual 2-Input NAND Gate (Driver)			
	CD40107B	† RCA	120
	CD40107BE	RCA	
Dual 4-Input Expandable NAND Gate			
	SCL4412B	† SSS	
	SCL4412BE	SSS	
Triple 3-Input NAND Gate			
	F4023BC	Fairchild	
	F4023BM	† Fairchild	
	HD14023B	Hitachi	
	SIL4023UB	† Mitel	
	SIL4023UBE	Mitel	130
	SIL4023B	† Mitel	
	SIL4023BE	Mitel	
	MC14023BA	† Motorola	
	MC14023BC	Motorola	
	MC14023UBA	† Motorola	
	MC14023UBC	Motorola	
		(Continued)	

Function	Device	Source	Line
Gates, AND/NAND (Cont'd.)			
Triple 3-Input NAND Gate		(Cont'd.)	
	μPD4023B	NEC America	
	MSM4023	OKI	
	CD4023BC	National	140
	CD4023BM	† National	
	MM54C10	† National	
	MM74C10	National	
	CD4023A	† RCA	
	CD4023AE	RCA	
	CD4023B	† RCA	
	CD4023BE	RCA	
	CD4023UB	† RCA	
	CD4023UBE	RCA	
	HBF4023AE	SGS	150
	SCL4023B	† SSS	
	SCL4023BE	SSS	
	CM4023A	† Solitron	
	CM4023AE	Solitron	
	TP4023A	TI	
	TC4023B	Toshiba	
	TC7410B	Toshiba	
Quad 2-Input NAND Gate			
	F4011BC	Fairchild	
	F4011BM	† Fairchild	160
	HD14011B	Hitachi	
	SIL4011UB	† Mitel	
	SIL4011UBE	Mitel	
	SIL4011B	† Mitel	
	SIL4011BE	Mitel	
	MC14011BA	† Motorola	
	MC14011BC	Motorola	
	MC14011UBA	† Motorola	
	MC14011UBC	Motorola	
	CD4011AC	National	170
	CD4011AM	† National	
	CD4011BC	National	
	CD4011BM	† National	
	MM54C00	† National	
	MM74C00	National	
	μPD4011B	NEC America	
	MSM4011	OKI	
	CD4011A	RCA	
	CD4011AE	RCA	
	CD4011B	† RCA	180
	CD4011BE	RCA	
	CD4011UB	† RCA	
	CD4011UBE	RCA	
	HBF4011AE	SGS	
	SCL4011B	† SSS	
	SCL4011BE	SSS	
	SCL4011UB	† SSS	
	SCL4011UBE	SSS	
	CM4011	† Solitron	
	CM4011	Solitron	190
	TP4011A/B	TI	
	TP4311A	TI	
	TC4011B	Toshiba	
	TC4011UB	Toshiba	
	TC7400B	Toshiba	
Quad 2-Input NAND Gate (Open Drain)			
	TC5029	Toshiba	
	TC5030	Toshiba	
Gates, AND-OR/AND-OR-Invert			
Triple AND-OR Bi-Phase Pairs			
	CD4037A	† RCA	200
	CD4037AE	RCA	
		(Continued)	

† Military Temperature Range (−55° to 125°C)

* Typical Values

Bold face indicates additional data is provided on the page noted.

DIGITAL–CMOS (Cont'd)

Gates, AND-OR/AND-OR-Invert (Cont'd.)

Function	Device	Source	Line
Triple AND-OR Bi-Phase Pairs (Cont'd.)			
	CD4037B	†RCA	
	CD4037BE	RCA	
	CM4037A	†Solitron	
	CM4037AE	Solitron	
Quad AND-OR Select Gate			
	F4019BC	Fairchild	
	F4019BM	†Fairchild	
	F4519BC	Fairchild	
	F4519BM	†Fairchild	10
	SIL4019B	†Mitel	
	SIL4019BE	Mitel	
	MC14519BA	†Motorola	
	MC14519BC	Motorola	
	CD4019BC	National	
	CD4019BM	†National	
	CD4519BC	National	
	CD4519BM	†National	
	µPD4019B	NEC America	
	MSM4019	OKI	20
	CD4019A	†RCA	
	CD4019AE	RCA	
	CD4019B	†RCA	
	CD4019BE	RCA	
	HBF4019AE	SGS	
	SCL4019B	†SSS	
	SCL4019BE	SSS	
	CM4019A	†Solitron	
	CM4019AE	Solitron	
	TP4019A/B	TI	30
	TP4519A/B	TI	
	TC4019B	Toshiba	
Quad AND-OR Select Gate, Three-State			
	CD40257B	†RCA	
	CD40257BE	RCA	
Dual 2-Wide 2-Input AND-OR-Invert Gate			
	F4085BC	Fairchild	
	F4085BM	Fairchild	
	SIL4085B	†Mitel	
	SIL4085BE	Mitel	40
	MC14506BA	†Motorola	
	MC14506BC	Motorola	
	MSM510	OKI	
	MSM4085	OKI	
	CD4085B	†RCA	
	CD4085BE	RCA	
	SCL4085B	†SSS	
	SCL4085BE	SSS	
	TC4085B	Toshiba	
2-Wide 4-Input AND-OR Gate			50
	MSM514	OKI	
4 Wide 2-Input Expandable AND-OR-Invert Gate			
	F4086BC	Fairchild	
	F4086BM	†Fairchild	
	MSM512	OKI	
	MSM4086	OKI	
	CD4086B	†RCA	
	CD4086BE	RCA	
	SCL4086B	†SSS	
	SCL4086BE	SSS	60
	TC4086B	Toshiba	
Quad 4-2-2-1-Input AND-OR-Invert Gate			
	TP4302A	TI	
Quad 2-4-4-1-Input AND-OR-Invert Gate			
	TP4303A	TI	

Gates, Exclusive OR/NOR

Function	Device	Source	Line
Quad Exclusive OR Gate			
	F4030BC	Fairchild	
	F4030BM	†Fairchild	
	F4070BC	Fairchild	
	F4070BM	†Fairchild	70
	HD14070B	Hitachi	
	SIL4030B	†Mitel	
	SIL4030BE	Mitel	
	SIL4070B	†Mitel	
	SIL4070BE	Mitel	
	MC14070BA	†Motorola	
	MC14070BC	Motorola	
	CD4030AC	National	
	CD4030AM	†National	
	CD4070BC	National	80
	CD4070BM	†National	
	CD4507BC	National	
	CD4507BM	†National	
	MM54C86	†National	
	MM74C86	National	
	µPD4030B	NEC America	
	MSM581	OKI	
	CD4030A	†RCA	
	CD4030AE	RCA	
	MSM4030	OKI	90
	CD4030B	†RCA	
	CD4030BE	RCA	
	CD4070B	†RCA	
	CD4070BE	RCA	
	HBF4030AE	SGS	
	SCL4030B	†SSS	
	SCL4030BE	SSS	
	SCL4070B	†SSS	
	SCL4070BE	SSS	
	CM4030A	†Solitron	100
	CM4030AE	Solitron	
	CM4070A	†Solitron	
	CM4070AE	Solitron	
	TP4030A	TI	
	TP4507A/B	TI	
	TC4030B	Toshiba	
Quad Exclusive NOR Gate			
	F4077BC	Fairchild	
	F4077BM	†Fairchild	
	F4519BC	Fairchild	110
	F4519BM	†Fairchild	
	HD14077B	Hitachi	
	SIL4077B	†Mitel	
	SIL4077BE	Mitel	
	MC14077BA	†Motorola	
	MC14077BC	Motorola	
	CD4519BC	National	
	CD4519BM	†National	
	CD4077B	†RCA	
	CD4077BE	RCA	120
	CM4077A	†Solitron	
	CM4077AE	Solitron	
	SCL4077B	†SSS	
	SCL4077BE	SSS	

Gates, OR/NOR

Function	Device	Source	Line
8-Input OR Gate			
	SIL4978B	†Mitel	
	SIL4978BE	Mitel	
Dual 4-Input OR Gate			
	F4072BC	Fairchild	
	F4072BM	†Fairchild	130
	HD14072B	Hitachi	

(Continued)

Gates, OR/NOR (Cont'd.)

Function	Device	Source	Line
Dual 4-Input OR Gate (Cont'd.)			
	SIL4072B	†Mitel	
	SIL4072BC	Mitel	
	MC14072BA	†Motorola	
	MC14072BC	Motorola	
	µPD4072B	NEC America	
	MSM4072	OKI	
	CD4072B	†RCA	
	CD4072BE	RCA	140
	SCL4072B	†SSS	
	SCL4072BE	SSS	
	TP4072B	TI	
	TC4072B	Toshiba	
Triple 3-Input OR Gate			
	F4075BC	Fairchild	
	F4075BM	†Fairchild	
	HD14075B	Hitachi	
	SIL4075B	†Mitel	
	SIL4075BE	Mitel	150
	MC14075BA	†Motorola	
	MC14075BC	Motorola	
	CD4075BC	National	
	CD4075BM	†National	
	µPD4075B	NEC America	
	MSM4075	OKI	
	CD4075B	†RCA	
	CD4075BE	RCA	
	SCL4075B	†SSS	
	SCL4075BE	SSS	160
	TP4075B	TI	
	TC4075B	Toshiba	
Quad 2-Input OR Gate			
	F4071BC	Fairchild	
	F4071BM	†Fairchild	
	HD14071B	Hitachi	
	SIL4071B	†Mitel	
	SIL4071BE	Mitel	
	MC14071BA	†Motorola	
	MC14071BC	Motorola	170
	CD4071BC	National	
	CD4071BM	†National	
	MM54C32	†National	
	MM74C32	National	
	µPD4071B	NEC America	
	MSM4071	OKI	
	CD4071B	†RCA	
	CD4071BE	RCA	
	SCL4071B	†SSS	
	SCL4071BE	SSS	180
	CM4071A	†Solitron	
	CM4071AE	Solitron	
	TP4071B	TI	
	TC4071B	Toshiba	
8-Input NOR Gate			
	F4078BC	Fairchild	
	F4078BM	†Fairchild	
	HD14078B	Hitachi	
	SIL4078B	†Mitel	
	SIL4078BE	Mitel	190
	MC14078BA	†Motorola	
	MC14078BC	Motorola	
	µPD4078B	NEC America	
	MSM507	OKI	
	MSM4078	OKI	
	CD4078B	†RCA	
	CD4078BE	RCA	
	SCL4078B	†SSS	
	SCL4078BE	SSS	

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Values

DIGITAL–CMOS (Cont'd)

Gates, OR/NOR (Cont'd.)

Function	Device	Source	Line
8-Input NOR Gate (Cont'd.)			
	SCL4402B	†SSS	
	SCL4402BE	SSS	
	CM4078A	† Solitron	
	CM4078AE	Solitron	
	TC4078B	Toshiba	
Dual 3-Input NOR Gate plus Inverter			
	SIL4000UB	† Mitel	
	SIL4000UBE	Mitel	
	MC14000UBA	† Motorola	10
	MC14000UBC	Motorola	
	CD4000C	National	
	CD4000M	† National	
	CD4000A	† RCA	
	CD4000AE	RCA	
	CD4000B	† RCA	
	CD4000BE	RCA	
	CD4000UB	† RCA	
	CD4000UBE	RCA	
	SCL4000B	†SSS	20
	SCL4000BE	SSS	
	CM4000A	Solitron	
	CM4000AE	Solitron	
	TP4000A	TI	
Dual 4-Input NOR Gate			
	F4002BC	Fairchild	
	F4002BM	† Fairchild	
	HD14002B	Hitachi	
	SIL4002UB	† Mitel	
	SIL4002UBE	Mitel	30
	SIL4002B	† Mitel	
	SIL4002BC	Mitel	
	MC14002BA	† Motorola	
	MC14002BC	Motorola	
	MC14002UBA	† Motorola	
	MC14002UBC	Motorola	
	CD4002AC	National	
	CD4002AM	† National	
	µPD4002B	NEC America	
	MSM506	OKI	40
	CD4002A	† RCA	
	CD4002AE	RCA	
	MSM4002	OKI	
	CD4002B	† RCA	
	CD4002BE	RCA	
	CD4002UB	† RCA	
	CD4002UBE	RCA	
	HBF4002AE	SGS	
	SCL4002B	†SSS	
	SCL4002BE	SSS	50
	CM4002A	† Solitron	
	CM4002AE	Solitron	
	TP4002A	TI	
	TC4002B	Toshiba	
Dual 4-Input Expandable NOR Gate			
	SCL4402B	†SSS	
	SCL4402BE	SSS	
Triple 3-Input NOR Gate			
	F4025BC	Fairchild	
	F4025BM	† Fairchild	60
	HD14025B	Hitachi	
	SIL4025UB	† Mitel	
	SIL4025UBE	Mitel	
	SIL4025B	† Mitel	
	SIL4025BE	Mitel	
	MC14025BA	† Motorola	
	MC14025BC	Motorola	
	MC14025UBA	† Motorola	

(Continued)

Gates, OR/NOR (Cont'd.)

Function	Device	Source	Line
Triple 3-Input NOR Gate (Cont'd.)			
	MC14025UBC	Motorola	70
	CD4025AC	National	
	CD4025AM	† National	
	CD4025BC	National	
	CD4025BM	† National	
	µPD4025B	NEC America	
	MSM4025	OKI	
	CD4025A	† RCA	
	CD4025AE	RCA	
	CD4025B	† RCA	
	CD4025BE	RCA	80
	CD4025UB	† RCA	
	CD4025UBE	RCA	
	HBF4025AE	SGS	
	SCL4025B	SSS	
	SCL4025BE	SSS	
	CM4025A	Solitron	
	CM4025AE	Solitron	
	TP4025A	TI	
	TC4025B	Toshiba	
Quad 2-Input NOR Gate			90
	F4001BC	Fairchild	
	F4001BM	† Fairchild	
	HD14001B	Hitachi	
	SIL4001UB	† Mitel	
	SIL4001UBE	Mitel	
	SIL4001B	† Mitel	
	SIL4001BE	Mitel	
	MC14001BA	† Motorola	
	MC14001BC	Motorola	
	MC14001UBA	† Motorola	100
	MC14001UBC	Motorola	
	CD4001AC	National	
	CD4001AM	† National	
	CD4001BC	National	
	CD4001BM	† National	
	MM54C02	† National	
	MM74C02	National	
	µPD4001B	NEC America	
	MSM505	OKI	
	MSM4001	OKI	110
	CD4001A	† RCA	
	CD4001AE	RCA	
	CD4001B	† RCA	
	CD4001BE	RCA	
	CD4001UB	† RCA	
	CD4001UBE	RCA	
	HBF4001AE	SGS	
	SCL4001UB	†SSS	
	SCL4001UBE	SSS	
	CM4001A	† Solitron	120
	CM4001AE	Solitron	
	TP4001A/B	TI	
	TP4301A/UB	TI	
	TC4001B	Toshiba	
	TC4001UB	Toshiba	

Gates, Miscellaneous

Function	Device	Source	Line
8-Input Expandable Multifunction Gate			
	CD4048BC	National	
	CD4048BM	† National	
	CD4048A	† RCA	
	CD4048AE	RCA	130
	CD4048B	† RCA	
	CD4048BE	RCA	
	SCL4048B	†SSS	
	SCL4402B	†SSS	

(Continued)

Gates, Miscellaneous (Cont'd.)

Function	Device	Source	Line
8-Input Expandable Multifunction Gate (Cont'd.)			
	SCL4402BE	SSS	
	CM4048A	† Solitron	
	CM4048AE	Solitron	
Triple Gate (dual 4-input NAND and 2-input OR/NOR)			
	HD14501	Hitachi	140
	MC14501UBA	† Motorola	
	MC14501UBC	Motorola	
	µPD4501B	NEC America	
Hex Function Gate			
	HD14572	Hitachi	
	MC14572A	† Motorola	
	MC14572C	Motorola	
Dual 5-Input Majority Logic Gate			
	MC14530BA	† Motorola	
	MC14530BC	Motorola	150
	µPD4530B	NEC America	

Latches

Function	Device	Source	Line
8-Bit Latch			
	MM54C373	† National	
	MM74C373	National	
8-bit Addressable Latch (Serial In, Parallel Out)			
	F4724BC	Fairchild	
	F4724BM	† Fairchild	
	MC14099BA	† Motorola	
	MC14099BC	Motorola	
	CD4099BC	National	160
	CD4099BM	† National	
	CD4724BC	National	
	CD4724BM	† National	
	µPD4099	NEC America	
	CD4099B	† RCA	
	CD4099BE	RCA	
	SCL4099B	†SSS	
	SCL40999BE	SSS	
	TC4099B	Toshiba	
8-bit Addressable Input, Parallel Output Latch, Three-State			170
	MC14598BA	† Motorola	
	MC14598BC	Motorola	
8-bit Addressable Latch, Bidirectional Data Port (Serial In/Out and Parallel Out)			
	MC14599BA	† Motorola	
	MC14599BC	Motorola	
8-bit Latch, Counter, Incremented Input, Parallel Output, Three-State			
	MC14597BA	† Motorola	180
	MC14597BC	Motorola	
Quad Clocked "D" Latch			
	F4042BC	Fairchild	
	F4042BM	† Fairchild	
	HD14042B	Hitachi	
	SIL4042B	† Mitel	
	SIL4042BE	Mitel	
	MC14042BA	† Motorola	
	MC14042BC	Motorola	
	CD4042BC	National	190
	CD4042BM	† National	
	µPD4042B	NEC America	
	MSM4042	OKI	
	CD4042A	† RCA	
	CD4042AE	RCA	
	CD4042B	† RCA	
	CD4042BE	RCA	

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Values

Bold face indicates additional data is provided on the page noted.

DIGITAL–CMOS (Cont'd)

Latches (Cont'd.)

Function	Device	Source	Line
Quad Clocked "D" Latch (Cont'd.)			
	HBF4042AE	SGS	
	SCL4042B	† SSS	
	SCL4042BE	SSS	
	CM4042A	† Solitron	
	CM4042AE	Solitron	
	TP4042A/B	TI	
	TC4042B	Toshiba	
Quad NAND R/S Latch			
	F4044BC	Fairchild	10
	F4044BM	† Fairchild	
	HD14044B	Hitachi	
	SIL4044B	† Mitel	
	SIL4044BE	Mitel	
	MC14044BA	† Motorola	
	MC14044BC	Motorola	
	CD4044AC	National	
	CD4044AM	† National	
	μPD4044B	NEC America	
	MSM4044	OKI	20
	CD4044A	† RCA	
	CD4044AE	RCA	
	CD4044A/B	† RCA	
	CD4044A/BE	RCA	
	SCL4044B	† SSS	
	SCL4044BE	SSS	
	CM4044A	† Solitron	
	TP4044A/B	TI	
	TC4044B	Toshiba	
Quad NAND Latch			30
	TP4376A	TI	
Quad NOR R/S Latch			
	F4043BC	Fairchild	
	F4043BM	† Fairchild	
	HD14043B	Hitachi	
	SIL4043B	† Mitel	
	SIL4043BE	Mitel	
	MC14043BA	† Motorola	
	MC14043BC	Motorola	
	CD4043AC	National	40
	CD4043AM	† National	
	μPD4043B	NEC America	
	MSM4043	OKI	
	CD4043A	† RCA	
	CD4043AE	RCA	
	CD4043B	† RCA	
	CD4043BE	RCA	
	SCL4043B	† SSS	
	SCL4043BE	SSS	
	CM4043A	† Solitron	50
	CM4043AE	Solitron	
	TP4043A/B	TI	
	TP4078B	TI	
	TC4043B	Toshiba	
Quad NOR Latch			
	TP4377A	TI	
Dual 4-bit Latch			
	HD14508B	Hitachi	
	SIL4508B	† Mitel	
	SIL4508BE	Mitel	60
	MC14508BA	† Motorola	
	MC14508BC	Motorola	
	μPD4508B	NEC America	
	MSM4508	OKI	
	CD4508B	† RCA	
	CD4508BE	RCA	
	SCL4508B	† SSS	

(Continued)

Latches (Cont'd.)

Function	Device	Source	Line
Dual 4-bit Latch (Cont'd.)			
	SCL4508BE	SSS	
	CM4508	Solitron	70
	TC4508B	Toshiba	
Dual 4-bit Addressable Latch			
	F4723BC	Fairchild	
	F4723BM	† Fairchild	
	CD4723BC	National	
	CD4723BM	National	

Memories

For additional information see Master Selection Guide-Memory Sections.

Function	Device	Source	Line
16-bit FIFO (4x4)			
	CD40105B	† RCA	80
	CD40105BE	RCA	
64-bit FIFO (16x4)			
	F4703BC	Fairchild	
	F4703BM	† Fairchild	
64-bit Program Stack (16x4 LIFO)			
	F4706BC	Fairchild	
	F4706BM	† Fairchild	
16-bit Multiport Register File (4x4 Read While Write RAM)			
	MC14580BA	† Motorola	90
	MC14580BC	Motorola	
	CD40108B	† RCA	
	CD40108BE	RCA	
	CD40208B	† RCA	
	CD40208BE	RCA	
1,024-bit PROM (256x4)			
	HM6611	**† Harris (1401)**	
32-bit RAM (Direct Word Line Addressing)			
	CD4039A	† RCA	
	CD4039AE	RCA	100
	CM4039A	† Solitron	
	CM4039AE	Solitron	
	TC4039B	Toshiba	
32-bit RAM (Binary Addressing)			
	CD4036A	† RCA	
	CD4036AE	RCA	
	CM4036A	† Solitron	
	CM4036AE	† Solitron	
	TC4036B	Toshiba	
64-bit RAM (64x1)			110
	MCM14505A	† Motorola	
	MCM14505C	Motorola	
64-bit RAM (16x4)			
	F4725BC	Fairchild	
	F4725BM	† Fairchild	
	MM54C89	† National	
	MM74C89	National	
	CD40114B	† RCA	
	CD40114BE	RCA	
64-bit RAM (16x4 clocked RAM, three state output register)			120
	F4710BC	Fairchild	
	F4710BM	† Fairchild	
256-bit RAM (256x1)			
	F4720C	Fairchild	
	F4720M	† Fairchild	
	F4720AC	Fairchild	
	F4720AM	† Fairchild	

(Continued)

Memories (Cont'd.)

Function	Device	Source	Line
256-bit RAM (256x1) (Cont'd.)			
	IM6523	† Intersil	130
	MCM14537A	† Motorola	
	MCM14537C	Motorola	
	MM54C200	† National	
	MM74C200	National	
	MSM4061	OKI	
	CD4061A	† RCA	
	CD40061	RCA	
	CD40061A	† RCA	
256-bit RAM (64x4)			
	MCM14552A	† Motorola	140
	MCM14552C	Motorola	
	MM54C910	† National	
	MM74C910	National	
	SCM5555	SSS	
256-bit RAM (32x8)			
	HCMP1824	† Hughes	
	CDP1824	† RCA	
	SCP1824	† SSS	
512-bit RAM (512x1)			
	S2222	AMI	150
	S2222A	AMI	
	2222	Nortec	
	2222A	Nortec	
	SCM5522	SSS	
768-bit RAM (64x12)			
	IM6512	Intersil	
	IM6512M	† Intersil	
1,024-bit RAM (128x8)			
	CDP1823	RCA	
1,024-bit RAM (256x4)			160
	S5101	**AMI (1206)**	
	S5101L	**AMI (1206)**	
	F4721BC	Fairchild	
	F4721BM	Fairchild	
	HM6501	**Harris (1356)**	
	HM6551	**Harris (1389)**	
	HM6561	**Harris (1389)**	
	HM6562	**Harris (1397)**	
	HM435101	Hitachi	
	HCMP1822	† Hughes	170
	5101	Intel	
	M5101	† Intel	
	IM6551	Intersil	
	IM6551M	† Intersil	
	IM6561	Intersil	
	IM6561M	† Intersil	
	MCM145101	**Motorola (1536)**	
	MM54C920	† National	
	MM74C920	National	
	MM54C921	† National	180
	MM74C921	National	
	μPD5101L	**NEC Micro (1562)**	
	CDP1822	RCA	
	SCM5101	† SSS	
	SCP1822	† SSS	
	SY5101	Synertek	
	TG5501	Toshiba	
1,024-bit RAM (1024x1)			
	S6508	**AMI (1207)**	
	S6508A	**AMI (1207)**	190
	F4736BC	Fairchild	
	F4736BM	† Fairchild	
	HM6508	**Harris (1366)**	
	HM6518	**Harris (1379)**	

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Values

DIGITAL–CMOS (Cont'd)

Memories (Cont'd.)

Function	Device	Source
1,024-bit RAM (1024x1)		(Cont'd.)
	IM6508	† Intersil
	IM6518	† Intersil
	SIL1902A	† Mitel
	SIL1902AE	Mitel
	MCM146508	**Motorola (1534)**
	MCM146518	**Motorola (1534)**
	MM54C929	† National
	MM74C929	National
	MM54C930	† National
	μPD6508	**NEC Micro (1562)**
	MM74C930	National
	CDP1821	RCA
	SCM5102	SSS
	TC5508	Toshiba
1,024-bit ROM (256x4)		
	MCM14524A	† Motorola
	MCM14524C	Motorola
4096-bit RAM (1024x4)		
	HM4334	Hitachi
	μPD444	**NEC Micro (1580)**
	μPD445L	**NEC Micro (1581)**
	CDP1825	RCA
	TC5047	Toshiba
4096-bit RAM (4096x1)		
	HM4315	Hitachi
	HM6147	Hitachi
	TC5504	Toshiba
2,048-bit ROM (256x8)		
	F4735BC	Fairchild
	F4735BM	† Fairchild
4,096-bit ROM (512x8)		
	HCMP1831	† Hughes
	HCMP1832	† Hughes
	CDP1831	† RCA
	CDP1832	† RCA
	SCP1831	† SSS
	SCP1832	† SSS
8,192-bit ROM (1024x8)		
	HCMP1833	† Hughes
	HCMP1834	† Hughes
	CDP1833	† RCA
	CDP1834	† RCA
	SCP1833	† SSS
	SCP1834	† SSS
12,228-bit ROM(1024x12)		
	HM6312	**Harris (1348)**
	IM6312	Intersil
16,384-Bit ROM (2048 x 8)		
	HCMP1835	Hughes
	SCM5316	SSS

Multiplexers, Digital

See also Interface—Analog Switches, Multiplexers

Quad 2-Input Multiplexer		
	F4519BC	Fairchild
	F4519BM	† Fairchild
	HD14519	Hitachi
	MC14519BA	† Motorola
	MC14519BC	Motorola
	CD4519BC	National
	CD4519BM	† National
	MM54C157	† National
	MM74C157	National
	μPD4519B	NEC America

(Continued)

Multiplexers, Digital (Cont'd.)

Quad 2-Input Multiplexer		(Cont'd.)
	TP4519A/B	TI
Dual 4-Channel Digital Multiplexer		
	F4539BC	Fairchild
	F4539BM	† Fairchild
	MC14539BA	† Motorola
	MC14539BC	Motorola
	μPD4539B	NEC America
	MSM4539	OKI
	TC4539B	Toshiba
8-Channel Data Selector		
	F4512BC	Fairchild
	F4512BM	† Fairchild
	HD14512	Hitachi
	SIL4512B	† Mitel
	SIL4512BE	Mitel
	MC14512A	† Motorola
	MC14512C	Motorola
	CD4512BC	National
	CD4512DM	† National
	μPD4512B	NEC America
	MSM4512	OKI
	CD4512B	† RCA
	CD4512BE	RCA
	SCL4512B	† SSS
	SCL4512BE	SSS
	TP4512A/B	TI
	TC4512B	Toshiba
8-Channel Digital Multiplexer		
	MM54C151	† National
	MM74C151	National
Dual 8-Channel Digital Multiplexer		
	TP4321A	TI
16-Channel Digital Multiplexer		
	MM54C150	† National
	MM74C150	National
	TP4320A	TI
16-Channel Digital Multiplexer, Three-State		
	MM72C19	† National
	MM82C19	National

Multivibrators

Monostable/Astable Multivibrator, retriggerable		
	F4047BC	Fairchild
	F4047BM	† Fairchild
	CD4047BC	National
	CD4047BM	† National
	CD4047A	† RCA
	CD4047AE	RCA
	CD4047B	† RCA
	CD4047BE	RCA
	CM4047A	† Solitron
	CM4047AE	Solitron
	SCL4047B	† SSS
	SCL4047BE	SSS
	TC4047B	Toshiba
Dual Monostable Multivibrator		
	MC14538BA	† Motorola
	MC14538BC	Motorola
	MM54C221	† National
	MM74C221	National
	MSM4538	OKI
	SCL4538B	† SSS
	SCL4538BE	SSS

Multivibrators (Cont'd.)

Dual Monostable Multivibrator, retriggerable		
	F4528BC	Fairchild
	F4528BM	† Fairchild
	HD14528B	Hitachi
	SIL4098B	† Mitel
	SIL4098BE	Mitel
	SIL4528B	† Mitel
	SIL4528BE	Mitel
	MC14528BA	† Motorola
	MC14528BC	Motorola
	CD4528BC	National
	CD4528BM	† National
	μPD4528B	NEC America
	CD4098B	† RCA
	CD4098BE	RCA
	SCL4528B	† SSS
	SCL4528BE	SSS
	TC4528B	Toshiba

Oscillators/Dividers

See also CMOS-Counters

Oscillator/Divider (Programmable Timer)		
	MC14541BA	† Motorola
	MC14541BC	Motorola
Oscillator/2^8 Divider (2-5v supplies)		
	ICM7209	Intersil
Oscillator/2^8, 2^{10}, 2^{11}, and 2^{12} Divider (10 V supply)		
	TC5082	Toshiba
Oscillator/2^9 Divider		
	5016	Nortec
Oscillator/2^{11} to 2^{19} Divider, with duty cycle control		
	MC14451	Motorola
Oscillator/2^{13} to 2^{15} Divider (2-5v supplies)		
	UCN-4105	Sprague
Oscillator/Divider, Mask Programmable for division by 10,000 to 98,000 (Standard divides 3.579 MHz TV crystal to 60 Hz)		
	MM5369	National
Oscillator/49,152 Divider		
	UCN-4103	Sprague
	UCN-4104	Sprague
Oscillator/2^{16} Divider/Buffer		
	MC14450	Motorola
	HBC4700	† SGS
	HBF4700	SGS
	UCN-4112	Sprague
	UCN-4116	Sprague
	SCL5411	SSS
Oscillator/2^{16} Divider with 2^{13} Output (Supply 1-2v 7038B, 2-5v 7038A)		
	ICM7038A	Intersil
	ICM7038B	Intersil
Oscillator/2^{12} and 2^{17} Divider, also 2^{17} x 10 (0.01 and 0.1 output, 6.5 MHz crystal, 3-5V supply)		
	ICM7207	Intersil
Oscillator/2^{13} and 2^{17} Divider (2-3v supplies)		
	UCN-4111	Sprague
Oscillator/2^{17} Divider		
	M58478	Mitsubishi
Oscillator/2^{17} Divider (2.5-6v supplies)		
	MM53107	National

† Military Temperature Range (−55° to 125°C)

* Typical Values

Bold face indicates additional data is provided on the page noted.

DIGITAL–CMOS (Cont'd)

Oscillators/Dividers (Cont'd.)

Function	Device	Source
Oscillator/2^{17} Divider with 2^{13} output (supply 1-2 V 7038D, 2-5 V 7038C)	ICM7038C	Intersil
	ICM7038D	Intersil
Oscillator/2^{18} Divider with 2^{13} output (supply 1-2 V 7038E, 2-5V 7038F)	ICM7038E	Intersil
	ICM7038F	Intersil
Oscillator/2^{19} Divider with 2^{13} output (supply 1-2V 7038G, 2-5 V 7038H)	ICM7038H	Intersil
Oscillator/2^{12} and 2^{20} Divider, also 2^{20}x10 (0.1 and 1 second output with 5.2 MHz crystal, 5v supply)	ICM7207A	Intersil
Oscillator/2^{12}, 2^{18}, 2^{21}, and 2^{17} Divider (Also 2^{21} x 60, 2-5v supplies)	ICM7213	Intersil
Oscillator/2^{21} Divider/Buffer	CD4045A	†RCA
	CD4045AE	RCA
	CD4045B	†RCA
	CD4045BE	RCA
	HBF4045AE	SGS
	SCL4445B	†SSS
	SCL4445BE	SSS
	CM4045A	† Solitron
	CM4045AE	Solitron
Oscillator/2 ^{22} Divider	SCL5421	SSS
Oscillator/2^{23} Divider	SCL5419	SSS
Oscillator/2^{24} Divider	MC14521BA	† Motorola
	MC14521BC	Motorola
	TC4521B	Toshiba
Oscillator/2^{0} to 2^{24} Divider (Programmable Timer)	MC14536BA	† Motorola
	MC14536BC	Motorola
Divider, divide by 5/6	**RED5/6**	**LSI Comp (494)**
Divider, divide by 6	D6	LSI Comp
Divider, divide by 50/60	**RED50/60**	**LSI Comp (494)**
Divider, divide by 60	D60	LSI Comp
Divider, divide by 3000/3600	**RED3000/3600**	**LSI Comp (494)**
Divider, divide by 3600	D3600	LSI Comp

Shift Registers

Function	Device	Source
4-bit Parallel In/Parallel Out Shift Register	F4035BC	Fairchild
	F4035BM	† Fairchild
	HD14305B	Hitachi
	SIL4035B	† Mitel
	SIL4035BE	Mitel
	MC14035BA	† Motorola
	MC14035BC	Motorola
	CD4035BC	National
	CD4035BM	† National
	μPD4035B	NEC America

(Continued)

Shift Registers (Cont'd.)

Function	Device	Source
4-bit Parallel In/Parallel Out Shift Register (Cont'd.)	MSM4035	OKI
	CD4035A	†RCA
	CD4035AE	RCA
	CD4035B	†RCA
	CD4035BE	RCA
	HBF4035AE	SGS
	SCL4035B	†SSS
	SCL4035BE	SSS
	CM4035A	† Solitron
	CM4035AE	Solitron
	TP4035B	TI
	TC4035B	Toshiba
4-bit Parallel Shift Register	F40195BC	Fairchild
	F40195BM	† Fairchild
	CD40195BC	National
	CD40195BM	† National
	MM54C195	† National
	MM74C195	National
4-bit Bidirectional Shift Register	F40194BC	Fairchild
	F40194BM	† Fairchild
	HD14194B	Hitachi
	MC14194BA	† Motorola
	MC14194BC	Motorola
	MM54C95	National
	MM74C95	† National
	μPD4194B	NEC America
	MSM40194	OKI
	MSM10104	OKI
Dual 4-bit Serial In/Parallel Out Shift Register	F4015BC	Fairchild
	F4015BM	† Fairchild
	HD14501B	Hitachi
	SIL4015B	† Mitel
	SIL4015BE	Mitel
	MC14015BA	† Motorola
	MC14015BC	Motorola
	CD4015AC	National
	CD4015AM	† National
	μPD4015B	NEC America
	MSM4015	OKI
	CD4015A	†RCA
	CD4015AE	RCA
	CD4015B	†RCA
	CD4015BE	RCA
	HBF4015AE	SGS
	SCL4015B	†SSS
	SCL4015BE	SSS
	CM4015A	† Solitron
	CM4015AE	Solitron
	TP4015A/B	TI
	TC4015B	Toshiba
5-bit Parallel In/Serial Out Shift Register	MSM543	OKI
8-bit Synchronous Parallel In/Serial Out Shift Register	F4014BC	Fairchild
	F4014BM	† Fairchild
	HD14014B	Hitachi
	SIL4014B	† Mitel
	SIL4014BE	Mitel
	MC14014BA	† Motorola
	MC14014BC	Motorola
	CD4014AC	National
	CD4014AM	† National
	μPD4014B	NEC America

(Continued)

Shift Registers (Cont'd.)

Function	Device	Source
8-bit Synchronous Parallel In/Serial Out Shift Register (Cont'd.)	MSM4014	OKI
	CD4014A	†RCA
	CD4014AE	RCA
	CD4014B	†RCA
	CD4014BE	RCA
	HBF4014AE	SGS
	SCL4014B	†SSS
	SCL4014BE	SSS
	CM4014A	† Solitron
	CM4014AE	Solitron
	TP4014A	TI
	TC4014B	Toshiba
8-bit (Asynchronous parallel or synchronous serial operation) Parallel In/Serial Out Shift Register	F4021BC	Fairchild
	F4021BM	† Fairchild
	HD14021B	Hitachi
	SIL4021B	† Mitel
	SIL4021BE	Mitel
	MC14021BA	† Motorola
	MC14021BC	Motorola
	CD4021AC	National
	CD4021AM	† National
	μPD4021B	NEC America
	MSM4021	OKI
	CD4021A	†RCA
	CD4021AE	RCA
	CD4021B	†RCA
	CD4021BE	RCA
	SCL4021B	†SSS
	SCL4021BE	SSS
	CM4021A	† Solitron
	CM4021AE	Solitron
	TP4021A	TI
	TC4021B	Toshiba
8-bit Serial In/Parallel Out Shift Register	MM54C164	† National
	MM74C164	National
	MSM541	OKI
8-bit Parallel In/Serial Out Shift Register	MM54C165	† National
	MM74C165	National
	MSM542	OKI
8-bit Bidirectional Parallel/Serial Input/Output Bus Register	F4034BC	Fairchild
	F4034BM	† Fairchild
	HD14034B	Hitachi
	MC14034BA	† Motorola
	MC14034BC	Motorola
	CD4034BC	National
	CD4034BM	† National
	μPD4034B	NEC America
	MSM4034	OKI
	CD4034A	†RCA
	CD4034AE	RCA
	CD4034B	†RCA
	CD4034BE	RCA
	SCL4034B	†SSS
	SCL4034BE	SSS
	CM4034A	† Solitron
	CM4034AE	Solitron
	TC4034B	Toshiba
8-bit Bus Register, Shift and Store	MC14094BA	† Motorola
	MC14094BC	Motorola

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Values

DIGITAL–CMOS (Cont'd)

Function	Device	Source	Line
Shift Registers (Cont'd.)			
8-bit Bus Register, Shift and Store (Cont'd.)			
	μPD4094B	NEC America	
	MSM4094	OKI	
	CD4094B	† RCA	
	CD4094BE	RCA	
	SCL4094B	† SSS	
	SCL4094BE	SSS	
18-bit Static Shift Register (4, 5, 8, 9, 10, 12, 13, 14, 16, 17, 18-bits)			
	F4006BC	Fairchild	10
	F4006BM	† Fairchild	
	MC14006BA	† Motorola	
	MC14006BC	Motorola	
	CD4006AC	National	
	CD4006AM	† National	
	μPD4006B	NEC America	
	CD006A	† RCA	
	CD4006AE	RCA	
	CD4006B	† RCA	
	CD4006BE	RCA	20
	SCL4006B	† SSS	
	SCL4006BE	SSS	
	CM4006A	† Solitron	
	CM4006AD	Solitron	
	CM4006AE	Solitron	
	TC4006B	Toshiba	
30-bit Static Shift Register			
	MD4330B	† Mitel	
	MD4330BE	Mitel	
	MD4331B	† Mitel	30
	MD4331BE	Mitel	
32-Bit Serial In/Parallel Out Shift Register			
	MD4332B	† Mitel	
	MD4332BE	Mitel	
Dual 16-bit Static Shift Register			
	HSSR0321	† Hughes	
	HSSR0351	† Hughes	
32-bit Bidirectional Serial In/Serial Out Shift Register			
	CD40100B	† RCA	
	CD40100BE	RCA	40
64-bit Static Shift Register			
	F4031BC	Fairchild	
	F4031BM	† Fairchild	
	CD4031BC	National	
	CD4031BM	† National	
	CD4031A	† RCA	
	CD4031AE	RCA	
	CD4031B	† RCA	
	CD4031BE	RCA	
	MS612	RTC	50
Dual 50-bit Dynamic Shift Register			
	MSM540	OKI	
Dual 64-bit Static Shift Register			
	MC14517BA	† Motorola	
	MC14517BC	Motorola	
	μPD4517B	NEC America	
	SCL4517B	SSS	
	TC5050	Toshiba	
Dual 50/64-bit Static Shift Register			
	TC5000	Toshiba	60
128-bit Static Shift Register (16-bit increments)			
	MC14562BA	† Motorola	
	MC14562BC	Motorola	
Quad 32-bit Static Shift Register			
	MSM544	OKI	

Function	Device	Source	Line
Shift Registers (Cont'd.)			
200-bit Dynamic Shift Register			
	CD4062A	† RCA	
Quad 64-bit Static Shift Register, Separate Clock			
	F4731BC	Fairchild	
	F4731BM	† Fairchild	70
64-bit Variable Length Shift Register			
	F4557BC	† Fairchild	
	F4557BM	Fairchild	
	MC14557BA	† Motorola	
	MC14557BC	Motorola	
96-bit Variable Length Elastic Shift Register			
	MS618	† RTC	
128-bit Static Shift Register, W/Control Logic			
	MS625	† RTC	
Dual 512-bit Dynamic Shift Register			80
	MSM545	OKI	
	TC5004	Toshiba	
Translators			
Quad Voltage Up Level Translator			
	F4104BE	Fairchild	
	F4104BM	† Fairchild	
	MD4104B	† Mitel	
	MD4104BE	Mitel	
Quad Level Shifter (low to high voltage)			
	CD40109B	† RCA	
	CD40109BE	RCA	90
Hex Level Shifter (CMOS or TTL to CMOS)			
	MC14504BA	† Motorola	
	MC14504BC	Motorola	
Hex Level Shifter (low-to-high voltage)			
	TC5020B	Toshiba	
Hex TTL Buffer (Inverting) (CMOS To TTL)			
	MM54C901	† National	
	MM74C901	National	
Hex TTL Buffer (Non-Inverting) (CMOS To TTL)			
	MM54C902	† National	100
	MM74C902	National	
Hex PMOS Buffer (Inverting) (PMOS To CMOS or TTL)			
	MM54C903	† National	
	MM74C903	National	
Hex PMOS Buffer (Non-Inverting) (PMOS To CMOS or TTL)			
	MM54C904	† National	
	MM74C904	National	
HNIL/HTL is suitable for translation/input protection. See HNIL/HTL section			110
Miscellaneous			
Microprocessor, 1-bit, Industrial Control Unit			
	MC14500B	**Motorola (2009)**	
Phase-Locked Loop			
	F4046BC	Fairchild	
	F4046BM	† Fairchild	
	SIL4046B	† Mitel	
	SIL4046BE	Mitel	
	MC14046BA	† Motorola	
	MC14046BC	Motorola	120
	CD4046BC	National	
	CD4046BM	† National	
	CD4046B	† RCA	

(Continued)

Function	Device	Source	Line
Miscellaneous (Cont'd.)			
Phase-Locked Loop (Cont'd.)			
	CD4046BE	RCA	
	SCL4446B	† SSS	
	SCL4446BE	SSS	
CMOS Transistor Array (See also 4007 Dual Complementary Pair and Inverter-listed under Buffers/Inverters)			130
	CA3600	† RCA	
Hex Contact Bounce Eliminator			
	MC14490	Motorola	
	MC14490E	† Motorola	
8-bit I/O Port			
	HCMP1852	† Hughes	
	CDP1852	† RCA	
	SCP1852	† SSS	
5-Bit D/A Audio Generator			
	ICM7219	Intersil	140
8-bit Priority Encoder			
	F4532BC	Fairchild	
	F4532BM	† Fairchild	
	HD14532B	Hitachi	
	MC14532BA	† Motorola	
	MC14532BC	Motorola	
	μPD4532B	NEC America	
	MSM4532	OKI	
	CD4532B	† RCA	
	CD4532BE	RCA	150
	SCL4532B	† SSS	
	SCL4532BE	SSS	
	TC4532B	Toshiba	
10-Line to 4-Line DCD Priority Encoder			
	CD40147B	† RCA	
	CD40147BE	RCA	
Binary Rate Multiplier			
	CD4089BC	National	
	CD4089BM	† National	
	CD4089B	† RCA	160
	CD4089BE	RCA	
BCD Rate Multiplier			
	MC14527BA	† Motorola	
	MC14527BC	Motorola	
	CD4527BC	National	
	CD4527BM	† National	
	MSM5506	OKI	
	MSM5535	OKI	
	CD4527B	† RCA	
	CD4527BE	RCA	170
	SCL4527B	† SSS	
	SCL4527BE	SSS	
	TC4527B	Toshiba	
4-Bit Binary Counter/Clock Generator			
	TC5018B	Toshiba	
Bit Rate Generator			
	F4702BC	Fairchild	
	F4702BM	† Fairchild	
	HD4702-2	**† Harris (1926)**	
	HD4702-9	**Harris (1926)**	180
	HD6405-2	**† Harris (1926)**	
	HD6405-9	**Harris (1926)**	
	MC14411	Motorola	
Code Identification System; encodes/decodes serial Manchester code; 16-bits plus sync and parity			
	HD15530-2	**† Harris (753)**	
	HD15530-9	**Harris (753)**	

† Military Temperature Range (−55° to 125°C)

* Typical Values

Bold face indicates additional data is provided on the page noted.

DIGITAL–CMOS (Cont'd)

Miscellaneous (Cont'd.)

Function	Device	Source		Line
Code Identification System; encodes/decodes serial Manchester code; 2-28 data bits; even or odd parity on receiver or transmitter				
	HD15531-2	**† Harris**	**(760)**	
	HD15531-9	**Harris**	**(760)**	
Code Identification System; transmitter encodes up to 15 input lines to serial Manchester code; receiver decodes, presents serial output and compares to preset value to give an output if a match is found				
	ED-9	**Supertex**	**(834)**	
	ED-15	**Supertex**	**(834)**	
Code Identification System; transmitter encodes up to 11 input lines and 4 control lines to serial Manchester code, compares to preset value and presents serial control output if match is found				10
	ED-11	**Supertex**	**(834)**	
Comparator, Linear, Dual with Dual Op Amp				
	MC14574	Motorola		
Comparator, Linear, Dual with Quad Op Amp				
	MC14573	Motorola		
Comparator, Linear, Quad				
	MC14575	Motorola		
	MM54C909	† National		20
	MM74C909	National		
Dual Differential Line Driver				
	MM78C30	† National		
	MM88C30	National		
Quad Single Ended Line Driver				
	MM78C29	† National		
	MM88C29	National		
Successive Approximation Register				
	MC14559BA	† Motorola		
	MC14559BC	Motorola		30
	MM54C905	**† National**	**(1073)**	
	MM74C905	**National**	**(1073)**	
Successive Approximation Register, Cascadable				
	MC14549BA	† Motorola		
	MC14549BC	Motorola		
Digital Logic (for 3-1/2 digit A/D Systems)				
	MC14435	Motorola		
	MC14435E	† Motorola		
Phase Comparator				
	TC5081	Toshiba		40
Phase Comparator and Programmable Counters				
	MC14568BA	† Motorola		
	MC14568BC	Motorola		
Synthesizers, see Linear-Phase Locked Loop Circuits				
9-bit Parity Generator and Checker				
	CD40101B	† RCA		
	CD40101BE	RCA		
Addressable Asynchronous Receiver/Transmitter				
	MC14469	**Motorola**	**(788)**	
12-bit Parity Tree				
	F4531BC	Fairchild		
	F4531BM	† Fairchild		
	TC4531B	Toshiba		
	MC14531BA	† Motorola		50
	MC14531BC	Motorola		
	SCL4531B	SSS		
	TP4531B	TI		
Dual Schmitt Trigger				
	F4583BC	Fairchild		
	F4583BM	† Fairchild		60

(Continued)

Miscellaneous (Cont'd.)

Function	Device	Source		Line
Dual Schmitt Trigger			(Cont'd.)	
	HD14583B	Hitachi		
	MC14583BA	† Motorola		
	MC14583BC	Motorola		
	MSM4583	OKI		
	TC4583B	Toshiba		
Hex Schmitt Trigger				
	F40014BC	Fairchild		
	F40014AM	† Fairchild		
	HD14584B	Hitachi		70
	MC14584BA	† Motorola		
	MC14584BC	Motorola		
	CD40106BC	National		
	CD40106BM	† National		
	CD4584BC	National		
	CD4584BM	† National		
	MM54C14	**† National**	**(262)**	
	MM74C14	**National**	**(262)**	
	MM54C914	† National		
	MM74C914	National		80
	µPD4584B	NEC America		
	MSM4584	OKI		
	CD40106B	† RCA		
	CD40106BE	RCA		
	SCL4584B	SSS		
	TP4304A	TI		
Quad 2-input NAND Schmitt Trigger				
	F4093BC	† Fairchild		
	F4093BM	Fairchild		
	MC14093BA	† Motorola		90
	MC14093BC	Motorola		
	CD4093BC	National		
	CD4093BM	† National		
	µPD4093B	NEC America		
	MSM4093	OKI		
	CD4093B	† RCA		
	CD4093BE	RCA		
	SCL4093B	† SSS		
	SCL4093BE	SSS		
	TC4093B	Toshiba		100
Binary-to-phone Pulse Converter (See also Linear-Telecommunication Circuits)				
	MC14408	Motorola		
	MC14409	Motorola		
Modem (0-600 bps)				
	MC14412	Motorola		
Remote Control Transmitter (see also Linear-Consumer Circuits, TV Remote Control)				
	MC14422	Motorola		
2 of 8 Keyboard to Binary Encoder				110
	MC14419	Motorola		
Programmable Timer				
	MC14536BA	† Motorola		
	MC14536BC	Motorola		
	MC14541BA	† Motorola		
	MC14541BC	Motorola		
Timer, Detector, Driver				
	MD4301A	Mitel		
	MD4302A	Mitel		
	MD4303A	Mitel		120
	MD4304A	Mitel		
Quad Precision Timer/Driver (Inputs cause outputs to switch state for 100 clock pulses)				
	MC14415	Motorola		
	MC14415E	† Motorola		

Miscellaneous (Cont'd.)

Function	Device	Source	Line
Standardized Celled CMOS, for custom circuits			
	HI-1000	Holt	
Standardized CMOS Array, to build custom circuits by changing final metalization			
	MASTERMOS	IMI	130
	MM50	IMI	
	MM100	IMI	
	MM150	IMI	
	MM200	IMI	
	MM250	IMI	
	MM300	IMI	
	MM350	IMI	
	MM400	IMI	
	MM450	IMI	
	MM500	IMI	140
	MM550	IMI	
	MonochipM	Interdesign	
	MCA	Interdesign	
	MCB	Interdesign	
	MCC	Interdesign	
	MCD	Interdesign	
	ML50	Master Logic	
	ML75	Master Logic	
	ML100	Master Logic	
	ML150	Master Logic	150
	ML200	Master Logic	
	ML350	Master Logic	
	MCA	Master Logic	
	MCB	Master Logic	
	MCC	Master Logic	
	MCD	Master Logic	
	MC606	Micro Tech	
	MC616	Micro Tech	
	MC626	Micro Tech	
	MC636	Micro Tech	160
	MASTERMOS	Monosil	
Quad Bilateral Switch			
	MSM591	OKI	
UART			
	HCMP1854	† Hughes	
	CDP1854	† RCA	
	SCP1854	† SSS	
Low voltage CMOS devices (Counters, Display Drivers, Counter-Timers) not usually mixed with 5-20v CMOS logic are listed under Digital-Special or CMOS-Oscillators/Dividers			170

† Military Temperature Range (−55° to 125°C)

* Typical Values

IC MASTER

DIGITAL–ECL

Function	Device	Source	Line
The ECL-10000, 95000, 100K and III-Other Series are presented as separate groups in that sequence.			
ECL-10000 Series			
Arithmetic Functions			
Dual High Speed Adder/Subtractor			
	F10180	Fairchild	
	F10580	† Fairchild	
	HD10180	Hitachi	
	MC10180	Motorola	
	MC10580	† Motorola	
	μPB10180	NEC America	
	10180	Signetics	10
2-bit Arithmetic Logic Unit/Function Generator			
	MC10182	Motorola	
4-bit Arithmetic Logic Unit/Function Generator			
	F10181	Fairchild	
	F10581	† Fairchild	
	HD10181	Hitachi	
	MC10181	Motorola	
	MC10581	† Motorola	
	μPB10181	NEC America	
	10181	Signetics	20
4-bit ALU Slice (Microprocessor)			
	MC10800	Motorola	
2-bit Multiplier, High Speed			
	MC10287	Motorola	
	MC10687	Motorola	
4x2-bit Multiplier			
	MC10183	Motorola	
Look-ahead Carry Circuit			
	F10179	Fairchild	
	F10579	† Fairchild	30
	HD10179	Hitachi	
	MC10179	Motorola	
	MC10579	† Motorola	
	10179	Signetics	
5-bit Comparator			
	F10166	Fairchild	
	F10566	† Fairchild	
	MC10166	Motorola	
Buffers			
Hex Buffer			
	10188	Signetics	40
Hex Inverter			
	MC10189	Motorola	
	10189	Signetics	
Hex Inverter/Buffer			
	MC10195	Motorola	
Counters, Binary			
4-bit Binary Counter			
	F10016C	Fairchild	
	F10016M	† Fairchild	
	MC10178	Motorola	
4-bit Universal Binary Counter			50
	F10136	Fairchild	
	F10536	† Fairchild	
	HD10136	Hitachi	
	MC10136	Motorola	
	MC10536	† Motorola	
	μPB10136	NEC America	
	10136	Signetics	
Counters, Decade			
Bi-Quinary Counter			
	MC10138	Motorola	
Decade Counter			60
	F10010C	Fairchild	
	F10010M	† Fairchild	
Universal Decade Counter			
	F10137	Fairchild	
	MC10137	Motorola	
	MC10537	† Motorola	
	10137	Signetics	
Decoders			
Binary to 1-8 Decoder (High)			
	F10162	Fairchild	
	F10562	† Fairchild	70
	HD10162	Hitachi	
	MC10162	Motorola	
	MC10562	† Motorola	
	μPB10162	NEC America	
	10162	Signetics	
Binary to 1-8 Decoder (Low)			
	F10161	Fairchild	
	F10561	† Fairchild	
	HD10161	Hitachi	
	MC10161	Motorola	80
	MC10561	† Motorola	
	μPB10161	NEC America	
	10161	Signetics	
Dual Binary to 1-4 Decoder (High)			
	F10172	Fairchild	
	F10572	† Fairchild	
	MC10172	Motorola	
	MC10572	† Motorola	
	10172	Signetics	
Dual Binary to 1-4 Decoder (Low)			90
	F10171	Fairchild	
	F10571	† Fairchild	
	MC10171	Motorola	
	MC10571	† Motorola	
	10171	Signetics	
Drivers			
Dual TTL/MST Bus Driver			
	MC10128	Motorola	
Triple 4-3-3 Input Bus Driver			
	F10123	Fairchild	
	F10523	† Fairchild	100
	MC10123	Motorola	
	10123	Signetics	
Quad Bus Driver			
	F10192	Fairchild	
	10192	Signetics	
Flip-Flops			
Dual "D" Master-Slave Flip-Flop			
	F10131	Fairchild	
	F10231	Fairchild	
	F10531	† Fairchild	
	F10631	† Fairchild	110
	HD10131	Hitachi	
	MC10131	Motorola	
	MC10231	Motorola	
	MC10531	† Motorola	
	MC10631	† Motorola	
		(Continued)	

Function	Device	Source	Line
Flip-Flops (Cont'd.)			
Dual "D" Master-Slave Flip-Flop (Cont'd.)			
	μPB10131	NEC America	
	10131	Signetics	
	10231	Signetics	
Hex "D" Master-Slave Flip-Flop			120
	F10176	Fairchild	
	F10576	† Fairchild	
	MC10176	Motorola	
	MC10576	† Motorola	
	μPB10176	NEC America	
	10176	Signetics	
Hex "D" Master-Slave Flip-Flop (With Common Reset)			
	F10186	Fairchild	
	F10586	† Fairchild	
	MC10186	Motorola	130
Dual "J-$\bar{K}$" Master-Slave Flip-Flop			
	F10135	Fairchild	
	F10535	† Fairchild	
	MC10135	Motorola	
	MC10535	† Motorola	
	μPB10135	NEC America	
	10135	Signetics	
Gates, AND/NAND			
Hex AND Gate			
	MC10197	Motorola	
Dual 4-Input AND/NAND Gate			140
	10108	Signetics	
Quad 2-Input Gate (3 AND, 1 AND/NAND)			
	F10104	Fairchild	
	F10504	† Fairchild	
	HD10104	Hitachi	
	MC10104	Motorola	
	MC10504	† Motorola	
	10104	Signetics	
Gates, Exclusive OR/NOR			
Quad Exclusive OR Gate			
	F10113	Fairchild	150
	F10513	† Fairchild	
	MC10113	Motorola	
	10113	Signetics	
Triple 2-Input Exclusive OR/NOR Gate			
	F10107	Fairchild	
	F10507	† Fairchild	
	HD10107	Hitachi	
	MC10107	Motorola	
	MC10507	† Motorola	
	μPB10107	NEC America	160
	10107	Signetics	
Gates, OR/NOR			
Dual 3-Input 3-Output OR Gate (Line Driver)			
	F10110	Fairchild	
	F10210	Fairchild	
	F10510	† Fairchild	
	F10610	† Fairchild	
	HD10110	Hitachi	
	MC10110	Motorola	
	MC10210	Motorola	170
	μPB10110	NEC America	
	10110	Signetics	

† Military Temperature Range (−55° to 125°C)

* Typical Values

Bold face indicates additional data is provided on the page noted.

DIGITAL–ECL (Cont'd)

Gates, OR/NOR (Cont'd.)

Function	Device	Source	Line
Dual 3-Input 3-Output NOR Gate (Line Driver)	F10111	Fairchild	
	F10211	Fairchild	
	F10511	† Fairchild	
	F10611	† Fairchild	
	HD10111	Hitachi	
	MC10111	Motorola	
	DM10111	National	
	μPB10111	NEC America	
	10111	Signetics	
	10211	Signetics	10
Triple 4-3-3 Input NOR Gate	F10106	Fairchild	
	F10506	† Fairchild	
	HD10106	Hitachi	
	MC10106	Motorola	
	MC10506	† Motorola	
	DM10106	National	
	μPB10106	NEC America	
	10106	Signetics	
Quad 3-Input NOR Gate (One Input Common)	F10100	Fairchild	20
	MC10100	Motorola	
	μPB10100	NEC America	
	10100	Signetics	
Dual 3-Input 3-Output (1 OR, 2 NOR) Gate (Line Driver)	F10212	Fairchild	
	F10612	† Fairchild	
	MC10212	Motorola	
	DM10112	National	30
	10112	Signetics	
Dual 4-5 Input OR/NOR Gate	F10109	Fairchild	
	F10509	† Fairchild	
	HD10109	Hitachi	
	HD10209	Hitachi	
	MC10109	Motorola	
	MC10509	† Motorola	
	DM10109	National	
	μPB10109	NEC America	40
	10109	Signetics	
Triple 2-3-2 Input OR/NOR Gate	F10105	Fairchild	
	F10505	† Fairchild	
	HD10105	Hitachi	
	MC10105	Motorola	
	MC10505	† Motorola	
	DM10105	National	
	μPB10105	NEC America	
	10105	Signetics	50
Quad 2-Input OR/NOR Gate (One Input Common)	F10101	Fairchild	
	F10501	† Fairchild	
	HD10101	Hitachi	
	MC10101	Motorola	
	MC10501	† Motorola	
	μPB10101	NEC America	
	10101	Signetics	
Quad 2-Input Gate (3 OR, 1 OR/NOR)	F10103	Fairchild	
	F10503	† Fairchild	
	MC10103	Motorola	
	μPB10103	NEC America	
	10103	Signetics	60
Quad 2-Input Gate (3 NOR, 1 OR/NOR)	F10102	Fairchild	

(Continued)

Gates, OR/NOR (Cont'd.)

Function	Device	Source	Line
Quad 2-Input Gate (3 NOR, 1 OR/NOR) (Cont'd.)	F10502	† Fairchild	
	HD10102	Hitachi	
	MC10102	Motorola	70
	MC10502	† Motorola	
	μPB10105	NEC America	
	10102	Signetics	

Gates, OR-AND/OR-AND-Invert

Function	Device	Source	Line
4-Wide 4-3-3-3 Input OR-AND Gate	F10119	Fairchild	
	F10519	† Fairchild	
	HD10119	Hitachi	
	MC10119	Motorola	
	MC10519	† Motorola	
	DM10119	National	80
	10119	Signetics	
Dual 2-Wide 3-Input OR-AND Gate	F10118	Fairchild	
	F10518	† Fairchild	
	HD10118	Hitachi	
	MC10118	Motorola	
	MC10518	† Motorola	
	DM10118	National	
	μPB10118	NEC America	
	10118	Signetics	90
4-Wide 3-Input OR-AND/OR-AND-Invert Gate	F10121	Fairchild	
	F10521	† Fairchild	
	HD10121	Hitachi	
	MC10121	Motorola	
	MC10521	† Motorola	
	DM10121	National	
	10121	Signetics	
Dual 2-Wide 2-3 Input OR-AND/OR-AND-Invert Gate	F10117	Fairchild	100
	F10517	† Fairchild	
	HD10117	Hitachi	
	MC10117	Motorola	
	MC10517	† Motorola	
	DM10117	National	
	μPB10117	NEC America	
	10117	Signetics	

Latches

Function	Device	Source	Line
Dual "D" Clocked Latch	F10130	Fairchild	
	F10530	† Fairchild	110
	HD10130	Hitachi	
	HD10230	Hitachi	
	MC10130	Motorola	
	MC10530	† Motorola	
	10130	Signetics	
Quad "D" Latch, Gated Output; Active High Enable	F10133	Fairchild	
	F10533	† Fairchild	
	HD10133	Hitachi	
	MC10133	Motorola	120
	MC10533	† Motorola	
	μPB10133	NEC America	
	10133	Signetics	
Quad "D" Latch, Gated Output; Active Low Enable	F10153	Fairchild	
	F10553	† Fairchild	
	MC10153	Motorola	

Latches (Cont'd.)

Function	Device	Source	Line
Quad Latch, Common Clock, Separate Output Enable	F10168	Fairchild	
	F10568	† Fairchild	130
	MC10168	Motorola	
Quint Latch	F10175	Fairchild	
	F10575	† Fairchild	
	HD10175	Hitachi	
	MC10175	Motorola	
	MC10575	† Motorola	
	μPB10175	NEC America	
	10175	Signetics	
Dual 2 to 1 Multiplexer-Latch, Common Reset	F10132	Fairchild	140
	F10532	† Fairchild	
	HD10132	Hitachi	
	MC10132	Motorola	
	10132	Signetics	
Dual 2 to 1 Multiplexer-Latch	F10134	Fairchild	
	F10534	† Fairchild	
	HD10134	Hitachi	
	MC10134	Motorola	150
	10134	Signetics	
Quad 2-Input Multiplexer-Latch	F10173	Fairchild	
	F10573	† Fairchild	
	MC10173	Motorola	
	10173	Signetics	

Memories

For additional information, see Master Selection Guide-Memory sections

Function	Device	Source	Line
CAM (16-bit Content Addressable Memory)	10155	Signetics	160
RAM (8x2) Simultaneous Read-Write	MCM10143	Motorola	
RAM (16x4)	F10145AC	Fairchild	
	HD10145	Hitachi	
	MCM10145	Motorola	
	10145	Signetics	
RAM (64x1)	μPB10142	NEC America	
	10142	Signetics	170
	SN10142	TI	
RAM (64x1) 50 Ohm Drive	HD10148	Hitachi	
	MC10148	Motorola	
	μPB10148	NEC America	
	10148	Signetics	
	SN10148	TI	
RAM (64x1) 90 Ohm Drive	10140	Signetics	
	SN10140	TI	180
RAM (64x1) Read-while-Write	10151	Signetics	
RAM (128x1)	F10405C	Fairchild	
	MB7047	Fujitsu	
	HD10147	Hitachi	
	MCM10147	Motorola	
	SN10147	TI	

† Military Temperature Range (−55° to 125°C)

* Typical Values

IC MASTER

DIGITAL–ECL (Cont'd)

Memories (Cont'd.)

Function	Device	Source	Line
RAM (256x1)			
	F10410C	Fairchild	
	F10411C	Fairchild	
	MBM10410	Fujitsu	
	MB7042	Fujitsu	
	HM2105	Hitachi	
	HM2106	Hitachi	
	MCM10144	Motorola	
	MCM10152	Motorola	
	μPB10144	NEC America	
	10144	Signetics	10
	RI10144	Raytheon	
	SN10144	TI	
RAM (1024x1)			
	F10415	**Fairchild (1246)**	
	F10415A	**Fairchild (1246)**	
	F100415A	**Fairchild (1246)**	
	HM2110	Hitachi	
	MCM10146	Motorola	
	MCM10415A	Motorola	
	MBM10415A	Fujitsu	20
PROM (32x8)			
	MCM10139	Motorola	
	10139	Signetics	
PROM (256x4)			
	F10416	Fairchild	
	MCM10149	Motorola	
	GXB10149	Siemens	
	10149	Signetics	

Multivibrators

Function	Device	Source	Line
Monostable Multivibrator			
	MC10198	Motorola	30

Multiplexers

Function	Device	Source	Line
8 to 1 Multiplexer			
	F10164	Fairchild	
	F10564	† Fairchild	
	HD10164	Hitachi	
	MC10164	Motorola	
	MC10564	† Motorola	
	μPB10164	NEC America	
	10164	Signetics	
	SN10164	TI	
Dual 4 to 1 Multiplexer			40
	F10174	Fairchild	
	F10574	† Fairchild	
	HD10174	Hitachi	
	MC10174	Motorola	
	μPB10174	NEC America	
	10174	Signetics	
	SN10174	TI	
	MC10574	† Motorola	
Quad 2 to 1 Multiplexer (Non-Inverting)			
	F10158	Fairchild	50
	F10558	† Fairchild	
	MC10158	Motorola	
	μPB10158	NEC America	
	10158	Signetics	
Quad 2 to 1 Multiplexer (Inverting With Enable)			
	F10159	Fairchild	
	F10559	† Fairchild	
	MC10159	Motorola	
	10159	Signetics	

Shift Registers

Function	Device	Source	Line
4-bit Shift Register			60
	F10000C	Fairchild	
4-bit Universal Shift Register			
	F10141	Fairchild	
	MC10141	Motorola	
	MC10541	† Motorola	
	10141	Signetics	

Translators

Function	Device	Source	Line
Dual ECL to MOS/TTL Translator			
	MC75358	Motorola	
	MC75368	Motorola	
Triple ECL to NMOS Translator			70
	MC10177	Motorola	
	F10177	Fairchild	
Hex ECL to MST Translator			
	MC10191	Motorola	
	10191	Signetics	
Quad ECL to TTL Translator (Differential Input)			
	F10125	Fairchild	
	F10525	† Fairchild	
	HD10125	Hitachi	
	MC10125	Motorola	80
	MC10525	† Motorola	
	μPB10125	NEC America	
	10125	Signetics	
Quad Differential Receiver/MST to ECL Translator			
	MC10190	Motorola	
	10190	Signetics	
Quad TTL to ECL OR/NOR Translator			
	F10124	Fairchild	
	F10524	† Fairchild	
	HD10124	Hitachi	90
	MC10124	Motorola	
	MC10524	† Motorola	
	DM10124	National	
	μPB10124	NEC America	
	10124	Signetics	

Miscellaneous

Function	Device	Source	Line
Triple Differential Line Receiver			
	F10114	Fairchild	
	F10116	Fairchild	
	F10514	† Fairchild	
	F10516	† Fairchild	100
	HD10116	Hitachi	
	MC10114	Motorola	
	MC10116	Motorola	
	MC10216	Motorola	
	MC10514	† Motorola	
	MC10516	† Motorola	
	MC10616	† Motorola	
	DM10116	National	
	10114	Signetics	
	10116	Signetics	110
	10216	Signetics	
Quad Differential Line Receiver			
	F10115	Fairchild	
	F10515	† Fairchild	
	MC10115	Motorola	
	MC10515	† Motorola	
	DM10115	National	
	μPB10115	NEC America	
	10115	Signetics	

Miscellaneous (Cont'd.)

Function	Device	Source	Line
Quad Bus Receiver			120
	MC10129	Motorola	
	10129	Signetics	
Dual Simultaneous Bus Transceiver			
	MC10194	Motorola	
8-Input Priority Encoder			
	F10165	Fairchild	
	F10565	† Fairchild	
	HD10165	Hitachi	
	MC10165	Motorola	
	10165	Signetics	130
9-bit Parity Circuit (2 Carry Inputs)			
	F10170	Fairchild	
	F10570	† Fairchild	
	MC10170	Motorola	
	μPB10170	NEC America	
	10170	Signetics	
12-bit Parity Generator/Checker			
	F10160	Fairchild	
	F10560	† Fairchild	
	HD10160	Hitachi	140
	MC10160	Motorola	
	MC10560	† Motorola	
	μPB10160	NEC America	
	10160	Signetics	
Error Detection/Correction Circuit			
	MC10163	Motorola	
	MC10193	Motorola	
Active Terminator			
	F10014C	Fairchild	
	F10014M	† Fairchild	150

ECL-95000 Series

Counters

Function	Device	Source	Line
Binary Counter			
	F95016	Fairchild	
Decade Counter			
	F95010	Fairchild	

Flip-Flops

Function	Device	Source	Line
"J-K" Flip-Flop			
	F95029	Fairchild	
Dual "D" Master-Slave Flip-Flop			
	F95231	Fairchild	

Gates, Exclusive OR/NOR

Function	Device	Source	Line
Triple 2-Input Exclusive OR/NOR Gate			
	F95107	Fairchild	160

Gates, OR/NOR

Function	Device	Source	Line
Dual 3-Input 3-Output OR Gate (Line Driver)			
	F95110	Fairchild	
Dual 3-Input 3-Output NOR Gate (Line Driver)			
	F95111	Fairchild	
Triple 4-3-3 Input NOR Gate			
	F95106	Fairchild	
Quad 2-Input NOR (with Enable)			
	F95004	Fairchild	

† Military Temperature Range (−55° to 125°C)

* Typical Values

Bold face indicates additional data is provided on the page noted.

DIGITAL–ECL (Cont'd)

Function	Device	Source	Line
Gates, OR/NOR (Cont'd.)			
Dual 4-5 Input OR/NOR Gate	F95109	Fairchild	
Dual 4-Input OR/NOR Gate (with Enable)	F95002	Fairchild	
Triple 2-3-2 Input OR/NOR Gate	F95105	Fairchild	
Triple 2-Input OR/NOR Gate (with Enable)	F95003	Fairchild	
Quad 2-Input Gate (3 OR, 1 OR/NOR)	F95103	Fairchild	
Quad 2-Input Gate (3 NOR, 1 OR/NOR)	F95102	Fairchild	10
Quad 2-Input OR/NOR Gate (One Input Common)	F95101	Fairchild	
Latches			
Dual "D" Clocked Latch	F95130	Fairchild	
Shift Registers			
4-bit Shift Register	F95H00C	Fairchild	
	F95000	Fairchild	
Translators			
Quad TTL to ECL OR/NOR Translator	F95124	Fairchild	20
Miscellaneous			
Triple Differential Line Receiver	F95116	Fairchild	
Quad Differential Line Receiver	F95115	Fairchild	
ECL-100K Series			
Arithmetic Functions			
6-bit Adder	F10080	Fairchild	
4-bit Binary/Decade Arithmetic Logic Unit	F100181	Fairchild	
Look Ahead Carry Circuit	F100179	Fairchild	30
9-bit Comparator	F100166	Fairchild	
9-bit Wallace Tree Adder	F100182	Fairchild	
2x8-bit Recode Multiplier	F100183	Fairchild	
Counters			
Multipurpose Counting Register	F100136	Fairchild	
Decoders			
Universal Decoder	F100170	Fairchild	40
Drivers			
Quad Driver	F100112	Fairchild	
Hex Bus Driver	F100123	Fairchild	
Flip-Flops			
Triple D Type	F100131	Fairchild	
Hex D Type	F100151	Fairchild	
Gates, AND-OR-Invert			
Triple AND-OR-Invert Gate	F100117	Fairchild	50
5-Wide AND-OR-Invert Gate	F100118	Fairchild	
Gates, Exclusive OR/NOR			
Quintuple Exclusive OR/NOR Gate	F100107	Fairchild	
Gates, OR/NOR			
Triple 5-Input OR/NOR Gate	F100101	Fairchild	
Quintuple 2-Input OR/NOR Gate	F100102	Fairchild	
Latches			
Triple D Latch	F100130	Fairchild	60
Hex D Latch	F100150	Fairchild	
Memories			
CAM (4x4)	F100142	Fairchild	
RAM (16x4 Register File)	F100145	Fairchild	
RAM (256x1)	F10014	Fairchild	
RAM (1024x1)	**F100415**	**Fairchild (1246)**	70
Multiplexers			
Dual 8-Input Multiplexer	F100163	Fairchild	
16-Input Multiplexer	F100164	Fairchild	
Triple 4-Input Multiplexer	F100171	Fairchild	
Quad 2-Input Multiplexer with Latch	F100155	Fairchild	
Shift Registers			
8-bit Universal Shift Register	F100141	Fairchild	80
Shift Registers (Cont'd.)			
8-bit Shift Matrix	F100158	Fairchild	
Mask-Merge	F100156	Fairchild	
Miscellaneous			
Quintuple Line Receiver	F100114	Fairchild	
Quintuple Transceiver	F100194	Fairchild	
Dual 9-bit Parity Generator/Checker	F100160	Fairchild	90
Universal Priority Encoder	F100165	Fairchild	
Gate Array (Customized in final metalizations)	ECL-Array	Fairchild	
	ECL-ARRAY	NEC America	
ECL-III and Other Series			
Counters			
Binary Counter	MC1654	Motorola	
Divide by 4 Counter (1 GHz)	11C05C	Fairchild	
	11C05M	Fairchild	100
	MC1699	Motorola	
	SP8610	Plessey	
	SP8611B	Plessey	
	SP8611M	Plessey	
	SP8617B	Plessey	
	SP8619B	Plessey	
Divide by 4 Prescaler (1 GHz)	MC1697	Motorola	
	MC1699	Motorola	
Bi-Quinary Counter	MC1678	Motorola	110
Divide by 5/6 Prescaler, 650 MHz	11C91C	Fairchild	
	11C91M	† Fairchild	
Divide by 10/11 Prescaler, 650 MHz	11C90C	Fairchild	
	11C90M	† Fairchild	
	SP8680	Plessey	
Divide-by-6, 20/22 Prescaler (to 1.3 GHz)	SP8785	Plessey	120
	SP8786	Plessey	
Divide by 248/256 Prescaler, 950 MHz	11C83	Fairchild	
Flip-Flops			
Master-Slave "D" Flip-Flop	11C70C	Fairchild	
	MC1670	Motorola	
	μPB606B	NEC America	
	μPB636B	NEC America	
	SP1670B	Plessey	
	SP1671B	Plessey	130
Master-Slave "D" Flip-Flop (UHF Prescaler)	11C06C	Fairchild	
	MC1690	Motorola	

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Values

IC MASTER

DIGITAL–ECL (Cont'd)

Function	Device	Source	Line
Flip-Flops (Cont'd.)			
Master-Slave "D" Flip-Flop (UHF Prescaler) (Cont'd.)			
	SP1690B	Plessey	
Dual, Clocked "R-S" Flip-Flop			
	MC1666	Motorola	
	μPB604B	NEC America	
	SP1666	Plessey	
	SP1667B	Plessey	
Gates, Exclusive OR/NOR			
Triple 2-Input Exclusive OR Gate			
	MC1672	Motorola	
	μPB607B	NEC America	10
	SP1672B	Plessey	
	SP1673B	Plessey	
Triple 2-Input Exclusive NOR Gate			
	MC1674	Motorola	
	SP1674B	Plessey	
	SP1675B	Plessey	
Gates, OR/NOR			
Quad 2-Input OR Gate			
	MC1664	Motorola	
	μPB603B	NEC America	
	SP1664B	Plessey	20
	SP1665B	Plessey	
Quad 2-Input NOR Gate			
	MC1662	Motorola	
	μPB602B	NEC America	
	SP1662B	Plessey	
	SP1663B	Plessey	
Dual 4-Input OR/NOR Gate			
	MC1660	Motorola	
	μPB601B	NEC America	
	μPB631B	NEC America	30
	SP16F60	Plessey	
	SP1660B	Plessey	
	SP1661B	Plessey	
Dual 4-5 Input OR/NOR Gate			
	11C01C	Fairchild	
	MC1688	Motorola	
Latches			
Dual Clocked Latch			
	MC1668	Motorola	
	μPB605B	NEC America	
	SP1668	Plessey	40
	SP1669	Plessey	
Multivibrators			
Voltage Controlled Multivibrator			
	11C58C	Fairchild	
	MC1658	Motorola	
	SP1658	Plessey	
Shift Registers			
4-bit Shift Register			
	MC1694	Motorola	
Miscellaneous			
Dual Analog/Digital Comparator			
	MC1650	Motorola	

(Continued)

Function	Device	Source	Line
Miscellaneous (Cont'd.)			
Dual Analog/Digital Comparator (Cont'd.)			50
	MC1651	Motorola	
	SP1650B	Plessey	
	SP1651B	Plessey	
Quad Line Receiver			
	MC1692	Motorola	
	SP1692B	Plessey	
Voltage Controlled Oscillator			
	MC1648	† Motorola	
	SP1648	Plessey	

Function	Device	Source	Line

† Military Temperature Range (−55° to 125°C)

* Typical Values

Bold face indicates additional data is provided on the page noted.

DIGITAL–HNIL/HTL

Function	Device	Source	Line
Arithmetic Functions			
4-bit Comparator			
	343A/C	Teledyne S	
	343B/M	† Teledyne S	
Buffers/Inverters			
See also: Gates, Miscellaneous			
Hex Inverter			
	MC680	Motorola	
	MC690	Motorola	
	MC697	Motorola	
	H118	SGS	
	332A/C	Teledyne S	10
	332B/M	† Teledyne S	
Hex Inverter, Open Collector			
	MC681	Motorola	
	MC689	Motorola	
	H112	SGS	
Hex Inverter, Strobed			
	MC677	Motorola	
	H119	SGS	
	335A/C	Teledyne S	
	335B/M	† Teledyne S	20
Hex Inverter, Strobed, Open Collector			
	MC678	Motorola	
	H115	SGS	
	334A/C	Teledyne S	
	334B/M	† Teledyne S	
Counters			
Binary Counter			
	MC685	Motorola	
	H156	SGS	
	372A/C	Teledyne S	
	372B/M	† Teledyne S	30
Binary Up/Down Counter			
	374A/C	Teledyne S	
	374B/M	† Teledyne S	
Decade Counter			
	MC684	Motorola	
	H157	SGS	
	371A/C	Teledyne S	
	371B/M	† Teledyne S	
Decade Up/Down Counter			
	373A/C	Teledyne S	40
	373B/M	† Teledyne S	
Decoders/Drivers			
BCD to Seven Segment Decoder/Driver			
	383A/C	Teledyne S	
	383B/M	† Teledyne S	
BCD to Decimal Decoder, Open Collector			
	381A/C	Teledyne S	
	381B/M	† Teledyne S	
BCD to Seven Segment Driver, Gas Discharge Driver			
	384A/C	Teledyne S	
	384B/M	† Teledyne S	50
BCD to Decimal Decoder/Lamp Driver, Open Collector			
	380A/C	Teledyne S	
	380B/M	† Teledyne S	
BCD to Decimal Decoder/Driver (for Gas Discharge Display Tubes)			
	MC676	Motorola	
		(Continued)	

Function	Device	Source	Line
Decoders/Drivers (Cont'd.)			
BCD to Decimal Decoder/Driver (for Gas Discharge Display Tubes) (Cont'd.)			
	H158	SGS	60
	382A/C	Teledyne S	
	382B/M	† Teledyne S	
Dual Lamp/Line Driver			
	MC679	Motorola	
Dual Power AND Driver, Open Collector and Open Emitter (Schmitt Trigger)			
	MC699	Motorola	
Dual 4-Input AND Driver, Expandable			
	H109	SGS	
Dual 4-Input NAND Line Driver, Expandable			70
	MC662	Motorola	
Dual 5-Input Power NAND Driver			
	301A/C	Teledyne S	
	301B/M	† Teledyne S	
Dual 4-Input NAND Lamp/Relay Driver, Open Collector (to 30 v)			
	MC679	Motorola	
Quad 2-Input Power NAND Driver, Open Collector			
	302A/C	Teledyne S	
	302B/M	† Teledyne S	80
Flip-Flops			
Quad "D" Flip-Flop			
	370A/C	Teledyne S	
	370B/M	† Teledyne S	
Master-Slave "R-S" Flip-Flop			
	MC664	Motorola	
Master-Slave "J-K" or Set-Reset Flip-Flop			
	311A/C	Teledyne S	
	311B/M	† Teledyne S	
Dual "J-K" Flip-Flop with Preset			
	H110	SGS	90
Dual "J-K" Flip-Flop with Preset and Clear			
	H111	SGS	
Dual "J-K" Flip-Flop with Reset			
	MC663	Motorola	
Dual "J-K" or Set-Reset Flip-Flop			
	MC688	Motorola	
	312A/C	Teledyne S	
	312B/M	† Teledyne S	
	313A/C	Teledyne S	
	313B/M	† Teledyne S	100
Gates, AND/NAND			
Dual 2-Input AND Interface Buffer			
	391	Teledyne S	
Dual 4-Input AND Interface Buffer			
	390	Teledyne S	
Dual 4-Input NAND Gate			
	MC660	Motorola	
	MC661	Motorola	
Dual 2-Input NAND Interface Buffer			
	392	Teledyne S	
Dual 4-Input NAND Interface Buffer			110
	395	Teledyne S	
Dual 4-Input NAND Gate, Expandable			
	H104	SGS	
	H124	SGS	
		(Continued)	

Function	Device	Source	Line
Gates, AND/NAND (Cont'd.)			
Dual 4-Input NAND Gate, Expandable (Cont'd.)			
	396	Teledyne S	
Dual 5-Input NAND Gate			
	301A/C	Teledyne S	
	301B/M	† Teledyne S	
	322A/C	Teledyne S	120
	322B/M	† Teledyne S	
Triple 3-Input NAND Gate			
	MC670	Motorola	
	MC671	Motorola	
	H103	SGS	
4, 3, 4-Input NAND Gate			
	304A/C	Teledyne S	
	304B/M	† Teledyne S	
Quad 2-Input NAND Gate			
	MC668	Motorola	130
	MC672	Motorola	
	H102	SGS	
	H122	SGS	
	303A/C	Teledyne S	
	303B/M	† Teledyne S	
	321A/C	Teledyne S	
	321B/M	† Teledyne S	
	324A/C	Teledyne S	
	324B/M	† Teledyne S	
Quad 2-Input NAND Gate, Open Collector			140
	302A/C	Teledyne S	
	302B/M	† Teledyne S	
	323A/C	Teledyne S	
	323B/M	† Teledyne S	
Quad 2-Input NAND Gate (Schmitt Trigger)			
	MC693	Motorola	
2,2,3,3-Input NAND Gate			
	325A/C	Teledyne S	
	325B/M	† Teledyne S	
	326A/C	Teledyne S	150
	326B/M	Teledyne S	
Gates, OR/NOR			
Dual 2-Input OR Interface Buffer			
	393	Teledyne S	
Dual 2-Input NOR Interface Buffer			
	394	Teledyne S	
Quad 2-Input NOR Gate			
	306A/C	Teledyne S	
	306B/M	† Teledyne S	
Quad 2-Input NOR Gate, Open Collector			
	307A/C	Teledyne S	160
	307B/M	† Teledyne S	
GATES, AND-OR-Invert			
Expandable AND-OR-Invert			
	344A/C	Teledyne S	
	344B/M	† Teledyne S	
Dual 2-Wide, 2-Input AND-OR-Invert Gate			
	MC673	Motorola	
	MC674	Motorola	
	341A/C	Teledyne S	
	341B/M	† Teledyne S	
Dual 2-Wide, 2-Input AND-OR-Invert Gate, Expandable			170
	H105	SGS	

† Military Temperature Range (−55° to 125°C)

* Typical Values

IC MASTER

DIGITAL–HNIL/HTL (Cont'd)

Function	Device	Source	Line
Gates, Exclusive OR			
Quad 2-Input Exclusive OR Gate			
	MC683	Motorola	
Gates, Miscellaneous			
Hex Inverter/Gate (Quad Inverter, Dual NAND Gate)			
	333A/C	Teledyne S	
	333B/M	† Teledyne S	
Hex Inverter/Gate (Quad Inverter, Dual NAND Gate) Open Collector			
	332A/C	Teledyne S	
	332B/M	† Teledyne S	
Dual 4-Input Gate Expander (for 600 Series)			
	MC669	Motorola	10
Dual 5-Input Gate Expander (for 300 Series)			
	331A/C	Teledyne S	
	331B/M	†.Teledyne S	
	CA3094	†RCA	
	CA3094A	†RCA	
	CA3094B	†RCA	
Latches			
Quad Latch			
	MC682	Motorola	
Multiplexers			
8-Bit Multiplexer			
	350A/C	Teledyne S	20
	350B/M	† Teledyne S	
Dual 4-Bit Multiplexer			
	351A/C	Teledyne S	
	351B/M	† Teledyne S	
Multivibrators			
Monostable Multivibrator			
	H117	SGS	
	346	Teledyne S	
Dual Monostable Multivibrator			
	MC667	Motorola	
	342A/C	Teledyne S	30
	342B/M	† Teledyne S	
Dual Retriggerable Monostable Multivibrator			
	347A/C	Teledyne S	
	347B/M	† Teledyne S	
Shift Registers			
4-bit Parallel In Parallel Out Shift Register			
	MC686	Motorola	
	375A/C	Teledyne S	
	375B/M	† Teledyne S	
Translators			
Dual Low to High Interface (TTL to HNIL)			
	362A/C	Teledyne S	40
	362B/M	† Teledyne S	
Triple Low to High Translator (TTL to HTL)			
	MC666	Motorola	
Quad Low to High Interface (TTL to HNIL)			
	H114	SGS	
	363A/C	Teledyne S	
	363B/M	† Teledyne S	

Function	Device	Source	Line
Translators (Cont'd.)			
Dual High to Low Interface (HNIL to DTL, TTL)			
	361A/C	Teledyne S	
	361B/M	† Teledyne S	50
Dual Interface Element, (Line Driver, Receiver, ECL to TTL, MOS to TTL, Schmitt Trigger)			
	MC696	Motorola	
Triple High to Low Translator (HTL to TTL)			
	MC665	Motorola	
Quad High to Low Converter (Open Collector)			
	H113	SGS	
Hex Inverter/Interface (Low to High: TTL, CMOS to HTL, CMOS)			
	MC691	Motorola	60
Miscellaneous			
Pulse Stretcher			
	348	Teledyne S	
Dual Pulse Stretcher			
	MC675	Motorola	
	349A/C	Teledyne S	
	349B/M	† Teledyne S	
Quad Schmitt Trigger/Line Receiver			
	367A/C	Teledyne S	
	367B/M	† Teledyne S	
Quad Schmitt Trigger/Line Receiver, Open Collector			70
	MC693	Motorola	
	368A/C	Teledyne S	
	368B/M	† Teledyne S	
Timer (See also Linear-Timers)			
	355A/C	Teledyne S	
	355B/M	Teledyne S	

Function	Device	Source	Line

† Military Temperature Range (−55° to 125°C)

* Typical Values

Bold face indicates additional data is provided on the page noted.

DIGITAL–TTL

Arithmetic Functions

Function	Device	Source	Line
Gated Full Adder			
TTL	5480	† Fairchild	
	7480	Fairchild	
	M53280	Mitsubishi	
	MC5480	† Motorola	
	MC7480	Motorola	
	μPB7480	NEC America	
	5480	† Signetics	
	7480	Signetics	
	N8268	Signetics	10
	SN5480	† TI	
	SN7480	TI	
	TC3480	Toshiba	
2-bit Binary Full Adder			
TTL	5482	† Fairchild	
	7482	Fairchild	
	ZN5482	† Ferranti	
	ZN7482	Ferranti	
	HD2513	Hitachi	
	MC7482	Motorola	20
	SN5482	† TI	
	SN7482	TI	
4-bit Binary Full Adder, Look-Ahead Carry			
TTL	5483	† Fairchild	
	7483	Fairchild	
	54283	† Fairchild	
	74283	Fairchild	
	ZN5483A	† Ferranti	
	ZN7483A	Ferranti	
	HD7483A	Hitachi	30
	HD74283	Hitachi	
	M53283	Mitsubishi	
	M53483	Mitsubishi	
	MC5483	† Motorola	
	MC7483	Motorola	
	DM5483	† National	
	DM7483	National	
	μPB74283	NEC America	
	5483	† Signetics	
	7483	Signetics	40
	SN5483A	† TI	
	SN7483A	TI	
	SN54283	† TI	
	SN74283	TI	
TTL-LS	9LS83C	Fairchild	
	9LS83M	† Fairchild	
	9LS283C	Fairchild	
	9LS283M	† Fairchild	
	54LS83	† Fairchild	
	74LS83	Fairchild	50
	54LS283	† Fairchild	
	74LS283	Fairchild	
	HD74LS83A	Hitachi	
	HD74LS283A	Hitachi	
	54LS283	† MMI	
	74LS283	MMI	
	SN54LS83A	† Motorola	
	SN74LS83A	Motorola	
	SN54LS283	† Motorola	
	SN74LS283	Motorola	60
	DM54LS83A	† National	
	DM74LS83A	National	
	DM54LS283	† National	
	DM74LS283	National	
	9LS83AC	Raytheon	
	9LS83AM	† Raytheon	
	54LS83A	† Raytheon	
	74LS83A	Raytheon	
	9LS283C	Raytheon	

(Continued)

Arithmetic Functions (Cont'd.)

Function	Device	Source	Line
TTL-LS		(Cont'd.)	70
	9LS283M	† Raytheon	
	54LS283	† Raytheon	
	74LS283	Raytheon	
	54LS83A	† Signetics	
	74LS83A	Signetics	
	54LS283	† Signetics	
	74LS283	Signetics	
	SN54LS83A	† TI	
	SN74LS83A	TI	
	SN54LS283	† TI	80
	SN74LS283	TI	
TTL-S	54S283	† MMI	
	74S283	MMI	
	SN54S283	† TI	
	SN74S283	TI	
4-bit Full Adder with Output Latch			
TTL	AM2506C	AMD	
	AM2506M	† AMD	
	RC2506	Raytheon	
	RM2506	† Raytheon	90
NBCD Adder (Natural Binary Coded Decimal)			
TTL	MC4056	Motorola	
	MC4356	† Motorola	
	MC54456	† Motorola	
	MC74456	Motorola	
4-bit BCD Adder			
TTL-S	N82S83	Signetics	
Dual Full Adder			
TTL	9304C	AMD	
	9304M	† AMD	100
	9304C	Fairchild	
	9304M	† Fairchild	
	M54304	Mitsubishi	
	MC8304	Motorola	
	MC9304	Motorola	
	RC9304	Raytheon	
	RM9304	† Raytheon	
	9304	Signetics	
TTL-LS	SN54LS183	† TI	
	SN74LS183	TI	110
TTL-H	54H183	† Fairchild	
	74H183	Fairchild	
	HD74H183	Hitachi	
	SN54H183	† TI	
	SN74H183	TI	
Dual Full Adder/Full Subtractor			
TTL	M54401	Mitsubishi	
Quad Serial Adder/Subtractor			
TTL-LS	AM25LS15C	AMD	
	AM25LS15M	† AMD	120
	SN54LS385	† AMD	
	SN74LS385	AMD	
	SN54LS385	† Motorola	
	SN74LS385	Motorola	
	25LS15C	Raytheon	
	25LS15M	† Raytheon	
	9LS385C	**Raytheon (554)**	
	9LS385M	**† Raytheon (554)**	
	54LS385	**† Raytheon (554)**	
	74LS385	**Raytheon (554)**	130
	SN54LS385	† TI	
	SN74LS385	TI	
4-bit BCD Arithmetic Unit (add, subtract, compare)			
TTL-S	N82S82	Signetics	

Arithmetic Functions (Cont'd.)

Function	Device	Source	Line
Binary Multiplier (2x4) Parallel, Serial Output			
TTL-LS	9LS261C	Raytheon	
	9LS261M	† Raytheon	
	54LS261	† Raytheon	
	74LS261	Raytheon	
	54LS261	† Signetics	140
	74LS261	Signetics	
	SN54LS261	† TI	
	SN74LS261	TI	
Binary Multiplier (4x2)			
TTL	9344C	Fairchild	
	9344M	† Fairchild	
Binary Multiplier (4x4) Three-State			
TTL-S	SN74S274	TI	
4-bit Multiplier, Three-State (two ICs to a set, 7875A and 7875B)			150
TTL	DM7875	† National	
	DM8875	National	
Binary Multiplier (4x4) Parallel (used with 54/74285)			
TTL	DM54284	† National	
	SN54284	† TI	
	SN74284	TI	
Binary Multiplier (4x4) Parallel (used with 54/74284)			
TTL	SN54285	† TI	
	SN74285	TI	
Multiplier (8x1) Serial/Parallel 2's Complement			160
TTL-LS	AM25LS14C	AMD	
	AM25LS14M	† AMD	
	SN54LS384	† AMD	
	SN74LS384	AMD	
	SN54LS384	† Motorola	
	SN74LS384	Motorola	
	25LS14C	Raytheon	
	25LS14M	† Raytheon	
	9LS384C	**Raytheon (551)**	
	9LS384M	**† Raytheon (551)**	170
	54LS384	**† Raytheon (551)**	
	74LS384	**Raytheon (551)**	
8-bit Parallel Byte Multiplier			
TTL	SBP9708C	TI	
	SBP9708M	† TI	
TTL-LS	SN54LS384	† TI	
	SN74LS384	TI	
8-Bit Serial/Parallel Register (for use with 25LS14/74LS384)			
TTL-LS	AM25LS22C	AMD	180
	AM25LS22M	† AMD	
	SN54LS322	† AMD	
	SN74LS322	AMD	
	54LS322	† MMI	
	74LS322	MMI	
	SN54LS322	† Motorola	
	SN74LS322	Motorola	
	25LS22C	Raytheon	
	25LS22M	† Raytheon	
	SN54LS322A	TI	190
	SN74LS322A	TI	
2's Complement Multiplier (4x2)			
TTL	AM2505C	AMD	
	AM2505M	† AMD	
	RC2505	Raytheon	
	RM2505	† Raytheon	
TTL-S	AM25S05C	AMD	
	AM25S05M	† AMD	
	93S43C	Fairchild	
	93S43M	† Fairchild	200

† Military Temperature Range (−55° to 125°C)

* Typical Values

DIGITAL–TTL (Cont'd)

Arithmetic Functions (Cont'd.)

Function	Device	Source	Line
2's Complement Multiplier (8x8)			
TTL-LS	AM25LS2516C	AMD	
	AM25LS2516M	† AMD	
TTL	**57558**	**† MMI**	**(495)**
	67558	**MMI**	**(495)**
	57558-1	**† MMI**	**(495)**
	67558-1	**MMI**	**(495)**
	MPY8AJ	TRW	
	MPY8AJM	† TRW	
	MPY8HJ	TRW	
	MPY8HJM	† TRW	10
2's Complement Multiplier/Accumulator/Divider (8x8)			
TTL	**57508**	**† MMI**	**(498)**
	67508	**MMI**	**(498)**
2's Complement Multiplier (8x8), Pipelined			
TTL	57559	† MMI	
	67559	MMI	
2's Complement Multiplier (8x8) with Accumulator			
TTL	TDC1008J	TRW	
	TDC1008JM	† TRW	
2's Complement Multiplier (12x12. 'H' version allows unsigned magnitude inputs as well)			20
TTL	MPY12AJ	TRW	
	MPY12AJM	† TRW	
	MPY12HJ	TRW	
	MPY12HJM	† TRW	
2's Complement Multiplier (12x12) with Accumulator			
TTL	TDC1003J	TRW	
	TDC1003JM	† TRW	
	TDC1009J	TRW	
	TDC1009JM	† TRW	30
2'S Complement Multipler (16x16. "H" version allows unsigned magnitude inputs as well)			
TTL	MPY16	MMI	
	MPY16AJ	TRW	
	MPY16AJM	† TRW	
	MPY16HJ	TRW	
	MPY16HJM	† TRW	
2's Complement Multiplier (16x16) with Accumulator			
TTL	TDC1010J	TRW	
	TDC1010JM	† TRW	40
2's Complement Multiplier/Accumulator/Divider (16x16)			
TTL	**57516**	**† MMI**	**(498)**
	67516	**MMI**	**(498)**
	57518	**† MMI**	**(498)**
	67518	**MMI**	**(498)**
2's Complement Multiplier (24x24. Allows unsigned magnitude inputs also)			
TTL	MPY24HJ	TRW	
	MPY24HJM	† TRW	50
TTL-S	MPY24AJ	TRW	
7-bit Slice Wallace Tree (to build multipliers)			
TTL-LS	SN54LS275	† TI	
	SN74LS275	TI	
TTL-S	SN54S275	† TI	
	SN74S275	TI	
4-bit ALU with Look-ahead Carry			
TTL	9340C	AMD	
	9340M	† AMD	
	9340C	Fairchild	60
	9340M	† Fairchild	
Register/Arithmetic Logic Unit			
TTL-LS	SN54LS681	† TI	

(Continued)

Arithmetic Functions (Cont'd.)

Function	Device	Source	Line
TTL-LS			(Cont'd.)
	SN74LS681	TI	
Arithmetic Logic Unit/Function Generator			
TTL	9341C	AMD	
	9341M	† AMD	
	AM2506C	AMD	
	AM2506M	† AMD	70
	SN54181	† AMD	
	SN74181	AMD	
	9341C	Fairchild	
	9341M	† Fairchild	
	54181	† Fairchild	
	74181	† Fairchild	
	ZN54181	† Ferranti	
	ZN74181	Ferranti	
	HD2547	Hitachi	
	M53381	Mitsubishi	80
	MC54181	Motorola	
	MC74181	Motorola	
	DM54181	† National	
	DM74181	National	
	μPB74181	NEC America	
	RC2506	Raytheon	
	RM2506	† Raytheon	
	RC9341	Raytheon	
	RM9341	† Raytheon	
	54181	† Signetics	90
	74181	Signetics	
	SN54181	† TI	
	SN74181	TI	
TTL-LS	AM25LS181C	AMD	
	AM25LS181M	† AMD	
	SN54LS181	† AMD	
	SN74LS181	AMD	
	9LS181C	Fairchild	
	9LS181M	† Fairchild	
	54LS181	† Fairchild	100
	74LS181	Fairchild	
	SN54LS181	† Motorola	
	SN74LS181	Motorola	
	9LS181C	Raytheon	
	9LS181M	† Raytheon	
	54LS181	† Raytheon	
	74LS181	Raytheon	
	25LS181C	Raytheon	
	25LS181M	† Raytheon	
	54LS181	† Signetics	110
	74LS181	Signetics	
	SN54LS181	† TI	
	SN74LS181	TI	
TTL-S	SN54S181	† AMD	
	SN74S181	AMD	
	93S41C	Fairchild	
	93S41M	† Fairchild	
	HD74S181	Hitachi	
	M5S181	Mitsubishi	
	54S181	† Signetics	120
	74S181	Signetics	
	SN54S181	† TI	
	SN74S181	TI	
Arithmetic Logic Unit/Function Generator			
TTL-LS	AM25LS2517C	AMD	
	AM25LS2517M	AMD	
	AM25LS381C	AMD	
	AM25LS381M	† AMD	
	SN54LS381	† AMD	
	SN74LS381	AMD	130
	SN54LS381	† TI	

(Continued)

Arithmetic Functions (Cont'd.)

Function	Device	Source	Line
TTL-LS			(Cont'd.)
	SN74LS381	TI	
	SN54LS382	† TI	
	SN74LS382	TI	
TTL-S	54S381	† MMI	
	74S381	MMI	
	57S581	† MMI	
	67S581	MMI	
	57S582	† MMI	140
	67S582	MMI	
	SN54S381	† TI	
	SN74S381	TI	
Look-ahead Carry Generator			
TTL	9342C	AMD	
	9342M	† AMD	
	SN54182	† AMD	
	SN74182	AMD	
	9342C	Fairchild	
	9342M	† Fairchild	150
	54182	† Fairchild	
	74182	Fairchild	
	HD74182	Hitachi	
	M53382	Mitsubishi	
	MC54182	† Motorola	
	MC74182	Motorola	
	μPB74182	NEC America	
	DM54182	† National	
	DM74182	National	
	RC9342	Raytheon	160
	RM9342	† Raytheon	
	54182	† Signetics	
	74182	Signetics	
	SN54182	† TI	
	SN74182	TI	
TTL-S	93S42C	Fairchild	
	93S42M	† Fairchild	
	HD74S182	Hitachi	
	M5S182	Mitsubishi	
	54S182	† MMI	170
	74S182	MMI	
	DM74S182	National	
	54S182	† Signetics	
	74S182	Signetics	
	SN54S182	† TI	
	SN74S182	TI	
Look Ahead Carry Generator (8-Group)			
TTL-S	57S583	† MMI	
	67S583	MMI	
	57S584	† MMI	180
	67S584	MMI	
	57S585	† MMI	
	67S585	MMI	
Register/Arithmetic Logic Unit			
TTL-LS	AM25LS281C	AMD	
	AM25LS281M	† AMD	
	SN54LS281	† AMD	
	SN74LS281	AMD	
	SN54LS681	† TI	
	SN74LS681	TI	190
TTL-S	DM74S281	National	
	SN54S281	† TI	
	SN74S281	TI	
Arithmetic Logic Element			
TTL	MC7260	Motorola	
	MC8260	† Motorola	
	RC8260	Raytheon	

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† Military Temperature Range (−55° to 125°C)

* Typical Values

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DIGITAL–TTL (Cont'd)

Arithmetic Functions (Cont'd.)

Function	Device	Source	Line
TTL		(Cont'd.)	
	RM8260	† Raytheon	
	N8260	Signetics	
	S8260	† Signetics	
Fast Carry Extender (for 8260)			
TTL	MC7261	Motorola	
	MC8261	† Motorola	
	RC8261	Raytheon	
	RM8261	† Raytheon	
	N8261	Signetics	10
	S8261	† Signetics	
Arithmetic and Logic Shift Matrix, Bit and Byte Masking			
TTL-S	**9405AC**	**Fairchild (1893)**	
	9405AM	**† Fairchild (1893)**	
4-bit Microprocessor Slice (ALU)			
TTL-LS	SN54LS481	† TI	
	SN74LS481	TI	
TTL-S	AM2901C	AMD	
	AM2901M	† AMD	
	AM2901AC	AMD	20
	AM2901AM	† AMD	
	AM2903C	AMD	
	AM2903M	† AMD	
	F2901AC	**Fairchild (1893)**	
	F2901AM	**† Fairchild (1893)**	
	F2903C	Fairchild	
	F2903M	† Fairchild	
	9409AC	Fairchild	
	9409AM	† Fairchild	
	9413	Fairchild	30
	3002	Intel	
	M3002	† Intel	
	2901AC	MMI	
	2901AM	† MMI	
	5701	† MMI	
	6701	MMI	
	MC2901	Motorola	
	MC2901AC	Motorola	
	MC2901AM	† Motorola	
	MC2903C	Motorola	40
	MC2903M	† Motorola	
	IDM2901AC	**National (286)**	
	IDM2901AM	**† National (286)**	
	µPB2901A	NEC Micro	
	AM2901C	Raytheon	
	AM2901M	† Raytheon	
	AM2901AC	Raytheon	
	AM2901AM	† Raytheon	
	N2901-1	Signetics	
	N3002	Signetics	50
	S3002	† Signetics	
	SN74S481	TI	
4-bit Magnitude Comparator			
TTL	DM7200	† National	
	DM8200	National	
	N8269	Signetics	
	S8269	† Signetics	
	TD3502A	Toshiba	
4-bit Magnitude Comparator, Separate A=B Output			
TTL	9324C	AMD	60
	9324M	† AMD	
	5485	† Fairchild	
	7485	Fairchild	
	9324C	Fairchild	
	9324M	† Fairchild	
	ZN5485	† Ferranti	
	ZN7485	Ferranti	

(Continued)

Arithmetic Functions (Cont'd.)

Function	Device	Source	Line
TTL		(Cont'd.)	
	HD7485	Hitachi	
	M53285	Mitsubishi	70
	MC5485	† Motorola	
	MC7485	Motorola	
	MC8324	Motorola	
	MC9324	† Motorola	
	DM5485	† National	
	DM7485	National	
	µPB7485	NEC America	
	5485	† Signetics	
	7485	Signetics	
	N9324	Signetics	80
	S9324	† Signetics	
	SN5485	† TI	
	SN7485	TI	
TTL-LS	9LS85C	Fairchild	
	54LS85	† Fairchild	
	74LS85	Fairchild	
	SN54LS85	† Motorola	
	SN74LS85	Motorola	
	DM54LS85	† National	
	DM74LS85	National	90
	9LS85C	Raytheon	
	9LS85M	† Raytheon	
	54LS85	† Raytheon	
	74LS85	Raytheon	
	54LS85	† Signetics	
	74LS85	Signetics	
	SN54LS85	† TI	
	SN74LS85	TI	
TTL-S	M5S085	Mitsubishi	
	54S85	† Signetics	100
	74S85	Signetics	
	SN54S85	† TI	
	SN74S85	TI	
Dual 4-bit Magnitude Comparator			
TTL	MC4021	Motorola	
	MC4022	Motorola	
	MC4321	† Motorola	
	MC4322	† Motorola	
6-bit, Unified Bus Comparator, Active Pull Up			
TTL	DM7131	† National	110
	DM8131	National	
6-bit Unified Bus Comparator, Open Collector			
TTL	DM7136	† National	
	DM8136	National	
6-bit Identity Comparator			
TTL	DM7160	† National	
	DM8160	National	
TTL-S	93S46C	Fairchild	
	93546M	† Fairchild	
6-bit Identity Comparator, Open Collector			120
TTL-S	93S47C	Fairchild	
	93S47M	† Fairchild	
8-bit Comparator			
TTL-LS	AM25LS2521C	AMD	
	AM25LS2521M	† AMD	
8-Bit 2's Complementor			
TTL-S	57S587	† MMI	
	67S587	MMI	
8-Bit Incrementor			
TTL-S	57S586	† MMI	130
	67S586	MMI	

Arithmetic Functions (Cont'd.)

Function	Device	Source	Line
8-Bit Double Incrementor			
TTL-S	57S588	† MMI	
	67S588	MMI	
8-Bit Incrementor, Decrementor, and 2's Complementor			
TTL-S	57S589	† MMI	
	67S589	MMI	
10-bit Identity Comparator			
TTL	DM7130	† National	140
	DM8130	National	

Buffers/Inverters

Function	Device	Source	Line
Quad Gated Buffer, Three-State			
TTL	54125	† Fairchild	
	74125	Fairchild	
	HD74125	Hitachi	
	M53325	Mitsubishi	
	DM7093	† National	
	DM8093	National	
	DM54125	† National	
	DM74125	National	150
	54125	† Signetics	
	74125	Signetics	
	SN54125	† TI	
	SN74125	TI	
	SN54425	† TI	
	SN74425	TI	
TTL-LS	9LS125C	Fairchild	
	9LS125M	Fairchild	
	54LS125	† Fairchild	
	74LS125	Fairchild	160
	SN54LS125A	† Motorola	
	SN74LS125A	Motorola	
	DM54LS125	† National	
	DM74LS125	National	
	9LS125C	Raytheon	
	9LS125M	† Raytheon	
	54LS125	† Raytheon	
	74LS125	Raytheon	
	54LS125A	† Signetics	
	74LS125A	Signetics	170
	SN54LS125A	† TI	
	SN74LS125A	TI	
Quad Gated Buffer, Three-State (Inverted Control)			
TTL	54126	† Fairchild	
	74126	Fairchild	
	HD74126	Hitachi	
	M53326	Mitsubishi	
	DM7094	† National	
	DM8094	National	
	DM54126	† National	180
	DM74126	National	
	54126	† Signetics	
	74126	Signetics	
	SN54126	† TI	
	SN74126	TI	
	SN54426	† TI	
	SN74426	TI	
TTL-LS	9LS126C	Fairchild	
	9LS126M	† Fairchild	
	54LS126	† Fairchild	190
	74LS126	Fairchild	
	SN54LS126A	† Motorola	
	SN74LS126A	Motorola	
	DM54LS126	† National	
	DM74LS126	National	
	9LS126C	Raytheon	

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Values

IC MASTER

DIGITAL–TTL (Cont'd)

Buffers/Inverters (Cont'd.)

Function	Device	Source	Line
TTL-LS		(Cont'd.)	
	9LS126M	† Raytheon	
	54LS126	† Raytheon	
	74LS126	Raytheon	
	54LS126A	† Signetics	
	74LS126A	Signetics	
	SN54LS126A	† TI	
	SN74LS126A	TI	
Hex Buffer, Three-State			
TTL	DM7095	† National	10
	DM7097	† National	
	DM8097	National	
	DM8095	National	
	DM54365	† National	
	DM74365	National	
	DM54367	† National	
	DM74367	National	
	54365A	† Signetics	
	74365A	Signetics	
	54367A	† Signetics	20
	74367A	Signetics	
	SN54365	† TI	
	SN74365	TI	
	SN54367	† TI	
	SN74367	TI	
TTL-LS	9LS365C	Fairchild	
	9LS365M	† Fairchild	
	9LS367C	Fairchild	
	9LS367M	† Fairchild	
	54LS365	† Fairchild	30
	74LS365	Fairchild	
	54LS367	† Fairchild	
	74LS367	Fairchild	
	HD74LS367	Hitachi	
	SN54LS365A	† Motorola	
	SN74LS365A	Motorola	
	SN54LS367A	† Motorola	
	SN74LS367A	Motorola	
	DM54LS365	† National	
	DM74LS365	National	40
	DM54LS367	† National	
	DM74LS367	National	
	µPB74LS365	NEC America	
	µPB74LS367	NEC America	
	9LS365C	Raytheon	
	9LS365M	† Raytheon	
	54LS365	† Raytheon	
	74LS365	Raytheon	
	9LS367C	Raytheon	
	9LS367M	† Raytheon	50
	54LS367	† Raytheon	
	74LS367	Raytheon	
	54LS365A	† Signetics	
	74LS365A	Signetics	
	54LS367A	† Signetics	
	74LS367A	Signetics	
	SN54LS365A	† TI	
	SN74LS365A	TI	
	SN54LS367A	† TI	
	SN74LS367A	TI	60
TTL-S	MB485	Fujitsu	
	MB487	Fujitsu	
	MC8T95	Motorola	
	MC8T97	Motorola	
	N8T95	**Signetics (2295)**	
	S8T95	**† Signetics (2295)**	
	N8T97	**Signetics (2295)**	
	S8T97	**† Signetics (2295)**	

(Continued)

Buffers/Inverters (Cont'd.)

Function	Device	Source	Line
TTL-S		(Cont'd.)	
	74S365	Signetics	70
	74S367	Signetics	
Octal Buffer, Three-State			
TTL-LS	DM71LS95	† AMD	
	DM81LS95	AMD	
	DM71LS97	† AMD	
	DM81LS97	AMD	
	DM71LS95	† National	
	DM81LS95	National	
	DM71LS97	† National	
	DM81LS97	National	80
Octal (Dual Quad), Buffer (Driver), Hysteresis, Three-State. See Octal Bus Drivers under Miscellaneous			
Hex Inverter			
TTL	5404	† Fairchild	
	7404	Fairchild	
	9016C	Fairchild	
	9016M	† Fairchild	
	ZN5404	† Ferranti	
	ZN7404	Ferranti	90
	HD7404	Hitachi	
	M53204	Mitsubishi	
	MC5404	† Motorola	
	MC7404	Motorola	
	DM5404	† National	
	DM7404	National	
	DM9016C	National	
	µPB7404	NEC America	
	7404	Signetics	
	5404	† Signetics	100
	SN5404	† TI	
	SN7404	TI	
	TD3404	Toshiba	
TTL-LS	9LS04C	Fairchild	
	9LS04M	† Fairchild	
	54LS04	† Fairchild	
	74LS04	Fairchild	
	HD74LS04	Hitachi	
	SN54LS04	† Motorola	
	SN74LS04	Motorola	110
	DM54LS04	† National	
	DM74LS04	National	
	µPB74LS04	NEC America	
	9LS04C	Raytheon	
	9LS04M	† Raytheon	
	54LS04	† Raytheon	
	74LS04	Raytheon	
	54LS04	† Signetics	
	74LS04	Signetics	
	SN54LS04	† TI	120
	SN74LS04	TI	
TTL-H	54H04	† Fairchild	
	74H04	Fairchild	
	HD2563	Hitachi	
	MC3008	Motorola	
	MC3108	† Motorola	
	DM54H04	† National	
	DM74H04	National	
	µPB74H04	NEC America	
	54H04	† Signetics	130
	74H04	Signetics	
	SN54H04	† TI	
	SN74H04	TI	
TTL-S	54S04	† Fairchild	
	74S04	Fairchild	

(Continued)

Buffers/Inverters (Cont'd.)

Function	Device	Source	Line
TTL-S		(Cont'd.)	
	9S04AC	Fairchild	
	9S04AM	† Fairchild	
	HD74S04	Hitachi	
	M5S004	Mitsubishi	140
	DM74S04	National	
	54S04	† Signetics	
	74S04	Signetics	
	N8T93	Signetics	
	SN54S04	† TI	
	SN74S04	TI	
Hex Inverter, Open Collector			
TTL	5405	† Fairchild	
	7405	Fairchild	
	9017C	Fairchild	150
	9017M	† Fairchild	
	ZN5405	Ferranti	
	ZN7405	Ferranti	
	HD7405	Hitachi	
	M53205	Mitsubishi	
	MC5405	† Motorola	
	MC7405	Motorola	
	DM5405	† National	
	DM7405	National	
	µPB7405	NEC America	160
	5405	† Signetics	
	N8T90	Signetics	
	S8T90	† Signetics	
	7405	Signetics	
	SN5405	† TI	
	SN7405	TI	
	TD3405	Toshiba	
	7405	TRW	
TTL-LS	9LS05C	Fairchild	
	9LS05M	† Fairchild	170
	54LS05	† Fairchild	
	74LS05	Fairchild	
	HD74LS05	Hitachi	
	SN54LS05	† Motorola	
	SN74LS05	Motorola	
	DM54LS05	† National	
	DM74LS05	National	
	µPB74LS05	NEC America	
	9LS05C	Raytheon	
	9LS05M	† Raytheon	180
	54LS05	† Raytheon	
	74LS05	Raytheon	
	54LS05	† Signetics	
	74LS05	Signetics	
	SN54LS05	† TI	
	SN74LS05	TI	
TTL-H	54H05	† Fairchild	
	74H05	Fairchild	
	MC3009	Motorola	
	MC3109	† Motorola	190
	DM54H05	† National	
	DM74H05	National	
	54H05	† Signetics	
	74H05	Signetics	
	SN54H05	† TI	
	SN74H05	TI	
TTL-S	54S05	† Fairchild	
	74S05	Fairchild	
	9S05AC	Fairchild	
	9S05AM	† Fairchild	200
	HD74S05	Hitachi	
	M5S005	Mitsubishi	
	DM74S05	National	

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Values

Bold face indicates additional data is provided on the page noted.

DIGITAL–TTL (Cont'd)

Buffers/Inverters (Cont'd.)

Function	Device	Source	Line
TTL-S		(Cont'd.)	
	54S05	† Signetics	
	74S05	Signetics	
	N8T94	Signetics	
	SN54S05	† TI	
	SN74S05	TI	
Hex Inverter, Three-State			
TTL	DM7096	† National	
	DM8096	National	
	DM7098	† National	10
	DM8098	National	
	DM54366	† National	
	DM74366	National	
	DM54368	† National	
	DM74368	National	
	54366A	† Signetics	
	74366A	Signetics	
	54368A	† Signetics	
	74368A	Signetics	
	SN54366	† TI	20
	SN54368	† TI	
	SN74366	TI	
	SN74368	TI	
TTL-LS	9LS366C	Fairchild	
	9LS366M	† Fairchild	
	9LS368C	Fairchild	
	9LS368M	† Fairchild	
	54LS366	† Fairchild	
	74LS366	Fairchild	
	54LS368	† Fairchild	30
	74LS368	Fairchild	
	HD74LS368	Hitachi	
	SN54LS366A	† Motorola	
	SN74LS366A	Motorola	
	SN54LS368A	† Motorola	
	SN74LS368A	Motorola	
	DM54LS366	† National	
	DM74LS366	National	
	DM54LS368	† National	
	DM74LS368	National	40
	μPB74LS366	NEC America	
	μPB74LS368	NEC America	
	9LS366C	Raytheon	
	9LS366M	† Raytheon	
	54LS366	† Raytheon	
	74LS366	Raytheon	
	9LS368C	Raytheon	
	9LS368M	† Raytheon	
	54LS368	† Raytheon	
	74LS368	Raytheon	50
	54LS366A	† Signetics	
	74LS366A	Signetics	
	54LS368A	† Signetics	
	74LS368A	Signetics	
	SN54LS366A	† TI	
	SN74LS366A	TI	
	SN54LS368A	† TI	
	SN74LS368A	TI	
TTL-S	MB486	Fujitsu	
	MB488	Fujitsu	60
	MC8T96	Motorola	
	MC8T98	Motorola	
	N8T96	**Signetics (2295)**	
	S8T96	**† Signetics (2295)**	
	N8T98	**Signetics (2295)**	
	S8T98	**† Signetics (2295)**	
	74S366	Signetics	
	74S368	Signetics	

Buffers/Inverters (Cont'd.)

Function	Device	Source	Line
Octal Inverter, Three-State			
TTL-LS	DM71LS96	† AMD	70
	DM81LS96	AMD	
	DM71LS98	† AMD	
	DM81LS98	AMD	
	DM71LS96	† National	
	DM81LS96	National	
	DM71LS98	† National	
	DM81LS98	National	
Octal (Dual Quad) Inverter (Driver) Hysteresis, Three-State. See Octal Bus Drivers under Miscellaneous			80

Counters, Binary Count Up

Function	Device	Source	Line
4-bit Binary Counter, Ripple			
TTL	5493	† Fairchild	
	7493	Fairchild	
	9305C	Fairchild	
	9305M	† Fairchild	
	54293	† Fairchild	
	74293	Fairchild	
	ZN5493	† Ferranti	
	ZN7493	Ferranti	
	HD7493A	Hitachi	90
	HD74293	Hitachi	
	M5393	Mitsubishi	
	M53293	Mitsubishi	
	M53493	Mitsubishi	
	MC5493	† Motorola	
	MC7493	Motorola	
	MC54293	† Motorola	
	MC74293	Motorola	
	DM5493	† National	
	DM7493	National	100
	5493	† Signetics	
	7493	Signetics	
	SN5493A	† TI	
	SN7493A	TI	
	SN54293	† TI	
	SN74293	TI	
	TD3505A	Toshiba	
	TD3493	Toshiba	
TTL-LS	9LS93C	Fairchild	
	9LS93M	† Fairchild	110
	9LS293C	Fairchild	
	9LS293M	† Fairchild	
	54LS93	† Fairchild	
	74LS93	Fairchild	
	54LS293	† Fairchild	
	74LS293	Fairchild	
	SN54LS93	† Motorola	
	SN74LS93	Motorola	
	SN54LS293	† Motorola	
	SN74LS293	Motorola	120
	DM54LS93	† National	
	DM74LS93	National	
	DM54LS293	† National	
	DM74LS293	National	
	9LS93C	Raytheon	
	9LS93M	† Raytheon	
	54LS93	† Raytheon	
	74LS93	Raytheon	
	54LS93	† Signetics	
	74LS93	Signetics	130
	54LS293	† Signetics	
	74LS293	Signetics	
	SN54LS93	† TI	
	SN74LS93	TI	

(Continued)

Counters, Binary Count Up (Cont'd.)

Function	Device	Source	Line
TTL-LS		(Cont'd.)	
	SN54LS293	† TI	
	SN74LS293	TI	
Dual 4-bit Binary Counter, Ripple (Dual 54/7493A)			
TTL	SN54393	† TI	
	SN74393	TI	140
TTL-LS	9LS393C	Fairchild	
	9LS393M	† Fairchild	
	54LS393	† Fairchild	
	74LS393	Fairchild	
	SN54LS393	† Motorola	
	SN74LS393	Motorola	
	74LS393	Signetics	
	SN54LS393	† TI	
	SN74LS393	TI	
Binary Counter/Latch (Divide-by-2, 4, 8, 16), Preset Input			150
TTL	54177	† Fairchild	
	74177	Fairchild	
	54197	Fairchild	
	74197	Fairchild	
	ZN54197	† Ferranti	
	ZN74197	Ferranti	
	HD74177	Hitachi	
	HD74197	Hitachi	
	M53377	Mitsubishi	160
	MC7281	Motorola	
	MC8281	Motorola	
	MC54177	† Motorola	
	MC74177	Motorola	
	MC54197	† Motorola	
	MC74197	Motorola	
	DM7281	† National	
	DM8281	National	
	DM7291	† National	
	DM8291	National	170
	DM54197	† National	
	DM74197	National	
	DM54177	† National	
	DM74177	National	
	RC8281	Raytheon	
	RC8291	Raytheon	
	RM8281	† Raytheon	
	RM8291	† Raytheon	
	N8281	Signetics	
	S8281	† Signetics	180
	N8291	Signetics	
	S8291	† Signetics	
	74177	Signetics	
	74197	Signetics	
	SN54177	† TI	
	SN74177	TI	
	SN54197	† TI	
	SN74197	TI	
TTL-LS	9LS197C	Fairchild	
	9LS197M	† Fairchild	190
	54LS197	† Fairchild	
	74LS197	Fairchild	
	SN54LS197	† Motorola	
	SN74LS197	Motorola	
	DM54LS197	† National	
	DM74LS197	National	
	9LS197C	Raytheon	
	9LS197M	† Raytheon	
	54LS197	† Raytheon	
	74LS197	Raytheon	200
	74LS197	Signetics	
	SN54LS197	† TI	

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Values

DIGITAL–TTL (Cont'd)

Counters, Binary Count Up (Cont'd.)

Function	Device	Source	Line
TTL-LS		(Cont'd.)	
	SN74LS197	TI	
TTL-S	74S197	Signetics	
	N82S91	Signetics	
	SN54S197	† TI	
	SN74S197	TI	
Dual Binary Counter, Synchronous			
TTL	MC4053	Motorola	
	MC4353	† Motorola	10
	MC54453	† Motorola	
	MC74453	Motorola	
Binary Counter, Synchronous, Preset Input (Synchronous Clear)			
TTL	SN54163	† AMD	
	SN74163	AMD	
	54163	† Fairchild	
	74163	Fairchild	
	ZN54163	† Ferranti	
	ZN74163	Ferranti	20
	HD74163	Hitachi	
	M53363	Mitsubishi	
	MC54163	† Motorola	
	MC74163	Motorola	
	DM54163	† National	
	DM74163	National	
	54163	Signetics	
	74163	Signetics	
	SN54163	† TI	
	SN74163	TI	30
TTL-LS	AM25LS163C	AMD	
	AM25LS163M	† AMD	
	SN54LS163	† AMD	
	SN74LS163	AMD	
	9LS163C	Fairchild	
	9LS163M	† Fairchild	
	54LS163	† Fairchild	
	74LS163	Fairchild	
	HD74LS163A	Hitachi	
	SN54LS163A	† Motorola	40
	SN74LS163A	Motorola	
	DM54LS163	† National	
	DM74LS163	National	
	9LS163C	Raytheon	
	9LS163M	† Raytheon	
	25LS163C	Raytheon	
	25LS163M	† Raytheon	
	54LS163	† Raytheon	
	74LS163	Raytheon	
	54LS163A	† Signetics	50
	74LS163A	Signetics	
	SN54LS163A	† TI	
	SN74LS163A	TI	
TTL-S	SN54S163	† TI	
	SN74S163	TI	
Binary Counter, Synchronous, Preset Input (Asynchronous Clear)			
TTL	SN54161	† AMD	
	SN74161	AMD	
	9316C	AMD	60
	9316M	† AMD	
	9316C	Fairchild	
	9316M	† Fairchild	
	54161	† Fairchild	
	74161	Fairchild	
	ZN54161	† Ferranti	
	ZN74161	Ferranti	
	HD74161	Hitachi	

(Continued)

Counters, Binary Count Up (Cont'd.)

Function	Device	Source	Line
TTL		(Cont'd.)	70
	M53361	Mitsubishi	
	MC8316	Motorola	
	MC9316	† Motorola	
	MC54161	† Motorola	
	MC74161	Motorola	
	DM54161	† National	
	DM74161	National	
	DM8316	† National	
	DM9316	National	
	μPB74161	NEC America	80
	RC9316	Raytheon	
	RM9316	† Raytheon	
	54161	† Signetics	
	74161	Signetics	
	9316	Signetics	
	SN29316	TI	
	SN39316	† TI	
	SN54161	† TI	
	SN74161	TI	
TTL-LS	AM25LS161C	AMD	90
	AM25LS161M	† AMD	
	SN54LS161	† AMD	
	SN74LS161	AMD	
	9LS161C	Fairchild	
	9LS161M	† Fairchild	
	54LS161	† Fairchild	
	74LS161	Fairchild	
	HD74LS161A	Hitachi	
	SN54LS161A	† Motorola	
	SN74LS161A	Motorola	100
	μPB74LS161	NEC America	
	DM54LS161	† National	
	DM74LS161	National	
	9LS161C	Raytheon	
	9LS161M	† Raytheon	
	25LS161C	Raytheon	
	25LS161M	† Raytheon	
	54LS161	† Raytheon	
	74LS161	Raytheon	
	54LS161A	† Signetics	110
	74LS161A	Signetics	
	SN54LS161A	† TI	
	SN74LS161A	TI	
TTL-S	SN54S161	† AMD	
	SN74S161	AMD	
	93S16C	AMD	
	93S16M	† AMD	
	93S16C	Fairchild	
	93S16M	† Fairchild	
Binary Counter/Register with multiplexed output, three-state			120
TTL-LS	SN54LS691	† TI	
	SN74LS691	TI	
	SN54LS693	† TI	
	SN74LS693	TI	
Binary Counter, Synchronous, Preset Input, Low-Power			
TTL	N8293	Signetics	
	S8293	† Signetics	
Binary Counter, Synchronous (both conventional and three state outputs) Preset Input			130
TTL	DM7556	† National	
	DM8556	National	

Counters, Binary, Count Up/Down

Function	Device	Source	Line
Binary Up/Down Counter, Synchronous with mode control			
TTL	N8284	AMD	
	S8284	† AMD	
	AM2501C	AMD	
	AM2501M	† AMD	
	RC8284	Raytheon	
	RM8284	† Raytheon	140
	N8284	Signetics	
	S8284	† Signetics	
Binary Up/Down, Synchronous, Preset Input with mode control			
TTL	54191	† Fairchild	
	74191	Fairchild	
	ZN54191	† Ferranti	
	ZN74191	Ferranti	
	HD74191	Hitachi	
	M53391	Mitsubishi	150
	MC54191	† Motorola	
	MC74191	Motorola	
	DM54191	† National	
	DM74191	National	
	54191	† Signetics	
	74191	Signetics	
	SN54191	† TI	
	SN74191	TI	
TTL-LS	AM25LS191C	AMD	
	AM25LS191M	† AMD	160
	SN54LS191	† AMD	
	SN74LS191	AMD	
	9LS191C	Fairchild	
	9LS191M	† Fairchild	
	54LS191	† Fairchild	
	74LS191	Fairchild	
	SN54LS191	† Motorola	
	SN74LS191	Motorola	
	DM54LS191	† National	
	DM74LS191	National	170
	9LS191C	Raytheon	
	9LS191M	† Raytheon	
	25LS191C	Raytheon	
	25LS191M	† Raytheon	
	54LS191	† Raytheon	
	74LS191	Raytheon	
	54LS191	† Signetics	
	74LS191	Signetics	
	SN54LS191	† TI	
	SN74LS191	TI	180
Binary Up/Down, Synchronous, Preset Input (2 Clocks)			
TTL	9366C	AMD	
	9366M	† AMD	
	SN54193	† AMD	
	SN74193	AMD	
	54193	† Fairchild	
	74193	Fairchild	
	ZN54193	† Ferranti	
	ZN74193	Ferranti	190
	HD74193	Hitachi	
	M53393	Mitsubishi	
	MC54193	† Motorola	
	MC74193	Motorola	
	DM7563	† National	
	DM8563	National	
	DM54193	† National	
	DM74193	National	
	μPB74193	NEC America	
	RC9366	Raytheon	200
	RM9366	† Raytheon	

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Values

Bold face indicates additional data is provided on the page noted.

DIGITAL–TTL (Cont'd)

Counters, Binary, Count Up/Down (Cont'd.)

Function	Device	Source	Line
TTL		(Cont'd.)	
	54193	† Signetics	
	74193	Signetics	
	SN54193	† TI	
	SN74193	TI	
	TD34193	Toshiba	
TTL-LS	AM25LS193C	AMD	
	AM25LS193M	† AMD	
	SN54LS193	† AMD	10
	SN74LS193	AMD	
	9LS193C	Fairchild	
	9LS193M	† Fairchild	
	54LS193	† Fairchild	
	74LS193	Fairchild	
	SN54LS193	† Motorola	
	SN74LS193	Motorola	
	DM54LS193	† National	
	DM74LS193	National	
	µPB74LS193	NEC America	20
	9LS193C	Raytheon	
	9LS193M	† Raytheon	
	25LS193C	Raytheon	
	25LS193M	† Raytheon	
	54LS193	† Raytheon	
	74LS193	Raytheon	
	54LS193	Signetics	
	74LS193	Signetics	
	SN54LS193	† TI	
	SN74LS193	TI	30
Binary Up/Down Counter, Synchronous, Preset Input, Mode Control, Look-ahead Carry			
TTL-LS	AM25LS169AC	AMD	
	AM25LS169AM	† AMD	
	SN54LS169A	† AMD	
	SN74LS169A	AMD	
	9LS169C	Fairchild	
	54LS169	† Fairchild	
	74LS169	Fairchild	
	SN54LS169	† Motorola	40
	SN74LS169	Motorola	
	DM54LS169	† National	
	DM74LS169	National	
	SN54LS169	† TI	
	SN74LS169	TI	
	SN54LS669	**† TI** **(1718)**	
	SN74LS669	**TI** **(1718)**	
TTL-S	SN54S169	† TI	
	SN74S169	TI	
Binary Up/Down Counter, Synchronous, Preset Input, Three-State			50
TTL-LS	AM25LS2569C	AMD	
	AM25LS2569M	† AMD	
	SN54LS569	† Motorola	
	SN74LS569	Motorola	
Binary Up/Down Counter/Register with multiplexed three-state output			
TTL-LS	SN54LS697	† TI	
	SN74LS697	TI	
	SN54LS699	† TI	
	SN74LS699	TI	60
Dual Binary Up/Down Counter, Synchronous, Preset Input			
TTL	MC4055	Motorola	
	MC4355	† Motorola	
	MC54455	† Motorola	
	MC74455	Motorola	

Counters, Binary, Count Up/Down (Cont'd.)

Function	Device	Source	Line
4-bit Universal Shift Register, Binary Up/Down Counter, Synchronous			
TTL-S	SN74S291	TI	70

Counters, Decade, Count Up

Function	Device	Source	Line
Decade Counter, Divide-by-2 and by-5			
TTL	5490	† Fairchild	
	7490	Fairchild	
	54290	† Fairchild	
	74290	Fairchild	
	ZN5490	† Ferranti	
	ZN7490	Ferranti	
	HD7490A	Hitachi	
	HD74290	Hitachi	
	M53290	Mitsubishi	80
	M53490	Mitsubishi	
	MC5490	† Motorola	
	MC7490	Motorola	
	MC54290	† Motorola	
	MC74290	Motorola	
	DM5490	† National	
	DM7490	National	
	5490	† Signetics	
	7490	Signetics	
	SN5490A	† TI	90
	SN7490A	TI	
	SN54290	† TI	
	SN74290	TI	
	TD3501A	Toshiba	
	TD3490	Toshiba	
TTL-LS	9LS90C	Fairchild	
	9LS90M	† Fairchild	
	9LS290C	Fairchild	
	9LS290M	† Fairchild	
	54LS90	† Fairchild	100
	74LS90	Fairchild	
	54LS290	† Fairchild	
	74LS290	Fairchild	
	SN54LS90	† Motorola	
	SN74LS90	Motorola	
	SN54LS290	† Motorola	
	SN74LS290	Motorola	
	DM54LS90	† National	
	DM74LS90	National	
	DM54LS290	† National	110
	DM74LS290	National	
	9LS90C	Raytheon	
	9LS90M	† Raytheon	
	54LS90	† Raytheon	
	74LS90	Raytheon	
	54LS90	† Signetics	
	74LS90	Signetics	
	54LS290	† Signetics	
	74LS290	Signetics	
	SN54LS90	† TI	120
	SN74LS90	TI	
	SN54LS290	† TI	
	SN74LS290	TI	
Decade (Divide-by-2 and Divide-by-5) Counter/Latch, Ripple, Preset Input			
TTL	54176	† Fairchild	
	74176	Fairchild	
	54196	† Fairchild	
	74196	Fairchild	
	HD74176	Hitachi	130
	HD74196	Hitachi	
	M53376	Mitsubishi	
	MC7280	† Motorola	

(Continued)

Counters, Decade, Count Up (Cont'd.)

Function	Device	Source	Line
TTL		(Cont'd.)	
	MC54176	† Motorola	
	MC74176	Motorola	
	MC54196	† Motorola	
	MC74196	Motorola	
	DM7280	† National	140
	DM8280	National	
	DM7290	† National	
	DM8290	National	
	DM54176	† National	
	DM74176	National	
	DM54196	† National	
	DM74196	National	
	RC8280	Raytheon	
	RC8290	Raytheon	
	RM8280	† Raytheon	150
	RM8290	† Raytheon	
	N8280	Signetics	
	N8290	Signetics	
	74176	Signetics	
	74196	Signetics	
	S8280	† Signetics	
	S8290	† Signetics	
	SN54176	† TI	
	SN74176	TI	
	SN54196	† TI	160
	SN74196	TI	
TTL-LS	9LS196C	Fairchild	
	9LS196M	† Fairchild	
	54LS196	† Fairchild	
	74LS196	Fairchild	
	SN54LS196	† Motorola	
	SN74LS196	Motorola	
	DM54LS196	† National	
	DM74LS196	National	
	9LS196C	Raytheon	170
	9LS196M	† Raytheon	
	54LS196	† Raytheon	
	74LS196	Raytheon	
	74LS196	† Signetics	
	SN54LS196	† TI	
	SN74LS196	TI	
TTL-S	N82S90	Signetics	
	SN54S196	† TI	
	SN74S196	TI	
Decade Counter, Synchronous, Preset Input (Asynchronous Clear)			180
TTL	9310C	AMD	
	9310M	† AMD	
	SN54160	† AMD	
	SN74160	AMD	
	9310C	Fairchild	
	9310M	† Fairchild	
	54160	† Fairchild	
	74160	Fairchild	
	HD74160	Hitachi	190
	M53360	Mitsubishi	
	MC8310	Motorola	
	MC9310	Motorola	
	MC54160	† Motorola	
	MC74160	Motorola	
	DM54160	† National	
	DM74160	National	
	DM8310	National	
	DM9310	† National	
	RC9310	Raytheon	200
	RM9310	† Raytheon	
	54160	† Signetics	

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Values

DIGITAL–TTL (Cont'd)

Counters, Decade, Count Up (Cont'd.)

Function	Device	Source	Line
TTL		(Cont'd.)	
	74160	Signetics	
	9310	Signetics	
	SN29310	TI	
	SN39310	TI	
	SN54160	† TI	
	SN74160	TI	
TTL-LS	AM25LS160C	AMD	
	AM25LS160M	† AMD	10
	SN54LS160	† AMD	
	SN74LS160	AMD	
	9LS160C	Fairchild	
	9LS160M	† Fairchild	
	54LS160	† Fairchild	
	74LS160	Fairchild	
	HD74LS160A	Hitachi	
	SN54LS160A	† Motorola	
	SN74LS160A	Motorola	
	DM54LS160	† National	20
	DM74LS160	National	
	9LS160C	Raytheon	
	9LS160M	† Raytheon	
	25LS160C	Raytheon	
	25LS160M	† Raytheon	
	54LS160	† Raytheon	
	74LS160	Raytheon	
	74LS160A	Signetics	
	SN54LS160A	† TI	
	SN74LS160A	TI	30
TTL-S	SN54S160	† AMD	
	SN74S160	AMD	
	93S10C	AMD	
	93S10M	† AMD	
	93S10C	Fairchild	
	93S10M	† Fairchild	
Decade Counter, Synchronous, Preset Input (Synchronous Clear)			
TTL	SN54162	† AMD	
	SN74162	AMD	40
	54162	† Fairchild	
	74162	Fairchild	
	HD74162	Hitachi	
	M53362	Mitsubishi	
	MC54162	† Motorola	
	MC74162	Motorola	
	DM54162	† National	
	DM74162	National	
	54162	† Signetics	
	74162	Signetics	50
	SN54162	† TI	
	SN74162	TI	
TTL-LS	AM25LS162C	AMD	
	AM25LS162M	† AMD	
	SN54LS162	† AMD	
	SN74LS162	AMD	
	9LS162C	Fairchild	
	9LS162M	† Fairchild	
	54LS162	† Fairchild	
	74LS162	Fairchild	60
	HM74LS162A	Hitachi	
	SN54LS162A	† Motorola	
	SN74LS162A	Motorola	
	DM54LS162	† National	
	DM74LS162	National	
	9LS162C	Raytheon	
	9LS162M	† Raytheon	
	25LS162C	Raytheon	
	25LS162M	† Raytheon	

(Continued)

Counters, Decade, Count Up (Cont'd.)

Function	Device	Source	Line
TTL-LS		(Cont'd.)	
	54LS162	† Raytheon	
	74LS162	Raytheon	
	74LS162A	Signetics	
	SN54LS162A	† TI	
	SN74LS162A	TI	
TTL-S	SN54S162	† TI	
	SN74S162	TI	
Decade Counter/Register with multiplexed output			
TTL-LS	SN54LS690	† TI	80
	SN74LS690	TI	
	SN54LS692	† TI	
	SN74LS692	TI	
Decade Counter, Synchronous, Preset Input Low-Power			
TTL	N8292	Signetics	
	S8292	† Signetics	
Decade Counter, Synchronous (both conventional and three-state outputs), Preset Inputs			
TTL	DM7555	† National	90
	DM8555	National	
Decade Counter, 10-line Output (resettable 2-10)			
TTL	9319C	Fairchild	
	9319M	† Fairchild	
	9320C	Fairchild	
	9320M	† Fairchild	
Decade Counter			
TTL	TC3504A	Toshiba	
Dual Decade Counter, Synchronous			
TTL	MC54452	† Motorola	100
	MC74452	Motorola	
Dual Decade Counter, Ripple (Dual 54/7490A)			
TTL	MC4052	Motorola	
	MC4352	† Motorola	
	SN54390	† TI	
	SN54490	† TI	
	SN74390	TI	
	SN74490	TI	
TTL-LS	9LS390C	Fairchild	
	54LS390	† Fairchild	110
	74LS390	Fairchild	
	9LS490C	Fairchild	
	54LS490	† Fairchild	
	74LS490	Fairchild	
	SN54LS390	† Motorola	
	SN74LS390	Motorola	
	SN54LS490	† Motorola	
	SN74LS490	Motorola	
	74LS390	Signetics	
	74LS490	Signetics	120
	SN54LS390	† TI	
	SN74LS390	TI	
	SN54LS490	† TI	
	SN74LS490	TI	

Counters, Decade, Count Up/Down

Function	Device	Source	Line
Decade Up/Down Counter, Synchronous			
TTL	N8285	AMD	
	S8285	† AMD	
	RC8285	Raytheon	
	RM8285	† Raytheon	
	N8285	Signetics	130
	S8285	† Signetics	

Counters, Decade, Count Up/Down (Cont'd.)

Function	Device	Source	Line
Decade Up/Down Counter, Synchronous, Preset, with Mode Control			
TTL	9306C	AMD	
	9306M	† AMD	
	54190	† Fairchild	
	74190	Fairchild	
	HD74190	Hitachi	
	M53390	Mitsubishi	
	MC54190	† Motorola	140
	MC74190	Motorola	
	DM54190	† National	
	DM74190	National	
	54190	† Signetics	
	74190	Signetics	
	SN54190	† TI	
	SN74190	TI	
TTL-LS	AM25LS190C	AMD	
	AM25LS190M	† AMD	
	SN54LS190	† AMD	150
	SN74LS190	AMD	
	9LS190C	Fairchild	
	9LS190M	† Fairchild	
	54LS190	† Fairchild	
	74LS190	Fairchild	
	SN54LS190	† Motorola	
	SN74LS190	Motorola	
	DM54LS190	† National	
	DM74LS190	National	
	9LS190C	Raytheon	160
	9LS190M	† Raytheon	
	25LS190C	Raytheon	
	25LS190M	† Raytheon	
	54LS190	† Raytheon	
	74LS190	Raytheon	
	54LS190	† Signetics	
	74LS190	Signetics	
	SN54LS190	† TI	
	SN74LS190	TI	
Decade Up/Down Counter, Synchronous, Preset Input (2 clocks)			170
TTL	9360C	AMD	
	9360M	† AMD	
	SN54192	† AMD	
	SN74192	AMD	
	54192	† Fairchild	
	74192	Fairchild	
	ZN54192	† Ferranti	
	ZN74192	Ferranti	
	HM74192	Hitachi	180
	M53392	Mitsubishi	
	MC54192	† Motorola	
	MC74192	Motorola	
	DM7560	† National	
	DM8560	National	
	DM54192	† National	
	DM74192	National	
	μPB74192	NEC America	
	RC9360	Raytheon	
	RM9360	† Raytheon	190
	54192	Signetics	
	74192	† Signetics	
	SN54192	† TI	
	SN74192	TI	
	TD34192	Toshiba	
TTL-LS	AM25LS192C	AMD	
	AM25LS192M	† AMD	
	SN54LS192	† AMD	
	SN74LS192	AMD	
	9LS192C	Fairchild	200

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Values

Bold face indicates additional data is provided on the page noted.

DIGITAL–TTL (Cont'd)

Counters, Decade, Count Up/Down (Cont'd.)

Function	Device	Source	Line
TTL-LS		(Cont'd.)	
	9LS192M	† Fairchild	
	54LS192	† Fairchild	
	74LS192	Fairchild	
	SN54LS192	† Motorola	
	SN74LS192	Motorola	
	DM54LS192	† National	
	DM74LS192	National	
	μPB74LS192	NEC America	10
	9LS192C	Raytheon	
	9LS192M	† Raytheon	
	25LS192C	Raytheon	
	25LS192M	† Raytheon	
	54LS192	† Raytheon	
	74LS192	Raytheon	
	54LS192	† Signetics	
	74LS192	Signetics	
	SN54LS192	† TI	
	SN74LS192	TI	20
Decade Up/Down Counter, Synchronous, Preset Input, Three-State			
TTL-LS	AM25LS2568C	AMD	
	AM25LS2568M	† AMD	
	SN54LS568	† Motorola	
	SN74LS568	Motorola	
Decade Up/Down Counter, Counter, Synchronous, Preset Input, Mode Control, Look-ahead Carry			
TTL-LS	AM25LS168AC	AMD	
	AM25LS168AM	† AMD	30
	SN54LS168A	† AMD	
	SN74LS168A	AMD	
	9LS168C	Fairchild	
	54LS168	† Fairchild	
	74LS168	Fairchild	
	SN54LS168	† Motorola	
	SN74LS168	Motorola	
	DM54LS168	National	
	DM74LS168	National	
	SN54LS168	† TI	40
	SN74LS168	TI	
	SN54LS668	**† TI**	**(1718)**
	SN74LS668	**TI**	**(1718)**
TTL-S	SN54S168	† TI	
	SN74S168	TI	
Decade Up/Down Counter/Register with Multiplexed Three-State Output			
TTL-LS	SN54LS696	† TI	
	SN74LS696	TI	
	SN54LS698	† TI	50
	SN74LS698	TI	
Dual Decade Up/Down Counter, Synchronous, Preset Input			
TTL	MC4054	Motorola	
	MC4354	† Motorola	
	MC54454	Motorola	
	MC74454	Motorola	
Four Decade Up/Down Counter/Latch/Display Driver (Synchronous, BCD and segment drives)			
TTL	ZN1040E	Ferranti	60

Counters, Miscellaneous

Function	Device	Source	Line
4-bit Universal Counter			
TTL	MC4023	Motorola	
6-bit Universal Counter			
TTL-S	DM75S50	National	

Counters, Miscellaneous (Cont'd.)

Function	Device	Source	Line
Divide-by-4 Counter			
TTL	TD6100	Toshiba	
Divide-By-12 Counter (Divide by 2 and 6), Ripple			
TTL	5492	† Fairchild	
	7492	Fairchild	
	ZN5492	† Ferranti	70
	ZN7492	Ferranti	
	HD7492A	Hitachi	
	M53292	Mitsubishi	
	M53492	Mitsubishi	
	MC5492	† Motorola	
	MC7492	Motorola	
	DM5492	† National	
	DM7492	National	
	5492	† Signetics	
	7492	Signetics	80
	SN5492A	† TI	
	SN7492A	TI	
	TD3492	Toshiba	
TTL-LS	9LS92C	Fairchild	
	9LS92M	† Fairchild	
	54LS92	† Fairchild	
	74LS92	Fairchild	
	HD74LS92	Hitachi	
	SN54LS92	† Motorola	
	SN74LS92	Motorola	90
	DM54LS92	† National	
	DM74LS92	National	
	9LS92C	Raytheon	
	9LS92M	† Raytheon	
	54LS92	† Raytheon	
	74LS92	Raytheon	
	54LS92	† Signetics	
	74LS92	Signetics	
	SN54LS92	† TI	
	SN74LS92	TI	100
Divide-By-12 Counter (Divide by 2 and 6), Preset Input			
TTL	DM7288	† National	
	DM8288	National	
	N8288	Signetics	
	S8288	† Signetics	
Programmable Modulo-N Binary Counter			
TTL	MC4018	Motorola	
	MC4318	† Motorola	
	MC4019	Motorola	
	MC4319	† Motorola	110
Programmable Modulo-N Decade Counter			
TTL	MC4016	Motorola	
	MC4316	† Motorola	
	MC4017	Motorola	
	MC4317	† Motorola	
Binary Counter/Latch, Three-State			
TTL	DM7554	† National	
	DM8554	National	
Decade Counter/Latch, Three-State			
TTL	DM7552	† National	120
	DM8552	National	
Programmable Modulo-N Divider (Divide by 2 to 15, Cascadable)			
TTL	DM7520	† National	
	DM8520	National	
4-bit Variable Modulo Counter (2 and 5, 6, 7, 8, or 10, 12, 14, 16)			
TTL	9305C	Fairchild	
	9305M	† Fairchild	
TTL-S	93S05C	Fairchild	130

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Counters, Miscellaneous (Cont'd.)

Function	Device	Source	Line
TTL-S		(Cont'd.)	
	93S05M	† Fairchild	
Decade Counter/Latch/7 Segment Decoder			
TTL	MC4050	Motorola	
	MC4350	† Motorola	
	MC4051	Motorola	
Decade Counter/Latch/Decoder (Nixie Driver)			
TTL	SN74142	TI	
Decade Counter/Latch LED/Lamp Driver (High Current Output)			140
TTL	SN54144	† TI	
	SN74144	TI	
Decade Counter/Latch, LED/Lamp Driver (Constant Current Output)			
TTL	SN54143	† TI	
	SN74143	TI	

Decoders

Function	Device	Source	Line
Excess 3-to-Decimal (1 of 10) Decoder			
TTL	5443	† Fairchild	
	7443	Fairchild	150
	HD7443A	Hitachi	
	M53243	Mitsubishi	
	MC5443	† Motorola	
	MC7443	Motorola	
	5443	† Signetics	
	7443	Signetics	
	SN5443A	† TI	
	SN7443A	TI	
TTL-LS	9LS43C	Raytheon	
	9LS43M	† Raytheon	160
	54LS43	† Raytheon	
	74LS43	Raytheon	
Excess 3 Gray-to-Decimal (1 of 10) Decoder			
TTL	5444	† Fairchild	
	7444	Fairchild	
	HD7444A	Hitachi	
	M53244	Mitsubishi	
	MC5444	† Motorola	
	MC7444	Motorola	
	5444	† Signetics	170
	7444	Signetics	
	SN5444A	† TI	
	SN7444A	TI	
TTL-LS	9LS44C	Raytheon	
	9LS44M	† Raytheon	
	54LS44	† Raytheon	
	74LS44	Raytheon	
BCD-to-Decimal (1 of 10) Decoder			
TTL	9301M	† AMD	
	9301C	AMD	180
	5442	† Fairchild	
	7442	Fairchild	
	9301C	Fairchild	
	9301M	† Fairchild	
	9302C	Fairchild	
	9302M	† Fairchild	
	ZN5442	† Ferranti	
	ZN7442	Ferranti	
	HD7442A	Hitachi	
	M53262	Mitsubishi	190
	M53242	Mitsubishi	
	MC5442	† Motorola	
	MC7442	Motorola	
	MC8301	Motorola	

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Values

DIGITAL–TTL (Cont'd)

Decoders (Cont'd.)

Function	Device	Source	Line
TTL		(Cont'd.)	
	MC9301	† Motorola	
	DM5442	† National	
	DM7442	National	
	DM8301	National	
	DM9301	† National	
	µPB7442	NEC America	
	RC8251	Raytheon	
	RC8252	Raytheon	
	RM8251	† Raytheon	10
	RM8252	† Raytheon	
	5442	† Signetics	
	7442	Signetics	
	N8251	Signetics	
	N8252	Signetics	
	S8251	† Signetics	
	S8252	† Signetics	
	SN29301	TI	
	SN39301	† TI	
	SN5442A	† TI	20
	SN7442A	TI	
	TD3441	Toshiba	
	TD3442	Toshiba	
TTL-LS	9LS42C	Fairchild	
	9LS42M	† Fairchild	
	54LS42	† Fairchild	
	74LS42	Fairchild	
	HD74LS42	Hitachi	
	SN54LS42	† Motorola	
	SN74LS42	Motorola	30
	DM54LS42	† National	
	DM74LS42	National	
	µPB74LS42	NEC America	
	9LS42C	Raytheon	
	9LS42M	† Raytheon	
	54LS42	† Raytheon	
	74LS42	Raytheon	
	54LS42	† Signetics	
	74LS42	Signetics	
	SN54LS42	† TI	40
	SN74LS42	TI	
TTL-S	N82S52	Signetics	
BCD-to-Decimal (1 of 10) Decoder, Three-State			
TTL-LS	AM25LS2537C	AMD	
	AM25LS2537M	† AMD	
BCD-to-Binary and Binary-to-BCD Converter, Open Collector			
TTL	MC4001	Motorola	
BCD to Decimal Decoder/Driver, Open Collector			
TTL-LS	74LS445	Signetics	50
	SN54LS445	† TI	
	SN74LS445	TI	
BCD-to-Decimal Decoder/Driver, Open Collector, 15v			
TTL	54145	† Fairchild	
	74145	Fairchild	
	HD74145	† Hitachi	
	M53345	Mitsubishi	
	MC54145	† Motorola	
	MC74145	Motorola	
	DM54145	† National	60
	DM74145	National	
	54145	† Signetics	
	74145	Signetics	
	SN54145	† TI	
	SN74145	TI	
TTL-LS	54LS145	† Fairchild	

(Continued)

Decoders (Cont'd.)

Function	Device	Source	Line
TTL-LS		(Cont'd.)	
	74LS145	Fairchild	
	SN54LS145	† TI	
	SN74LS145	TI	70
BCD-to-Decimal/Decoder Driver, Open Collector to 30v Output			
TTL	5445	† Fairchild	
	7445	Fairchild	
	HD7445	Hitachi	
	M53245	Mitsubishi	
	MC5445	† Motorola	
	MC7445	Motorola	
	DM5445	† National	
	DM7445	National	80
	µPB7445	NEC America	
	5445	† Signetics	
	7445	Signetics	
	SN5445	† TI	
	SN7445	TI	
Dual 1-of-4 Decoder/Demultiplexer (Independent Address)			
TTL	9321C	AMD	
	9321M	† AMD	
	9321C	Fairchild	90
	9321M	† Fairchild	
Dual Binary to One-Of-Four Line Gated Decoder			
TTL	MC4007	Motorola	
	MC4307	† Motorola	
Demultiplexer, (2-Lines In-2 of 4 Out) Three-State			
TTL	DM7230	† National	
	DM8230	National	
Dual 2-Line To 4-Line Decoder/Demultiplexer, Totem Pole Output (or 3-Line to 8-Line Decoder/Demultiplexer)			
TTL	54155	† Fairchild	100
	74155	Fairchild	
	ZN54155	† Ferranti	
	ZN74155	Ferranti	
	HD74155	Hitachi	
	M53355	Mitsubishi	
	MC54155	† Motorola	
	MC74155	Motorola	
	DM54155	† National	
	DM74155	National	110
	µPB74185	NEC America	
	54155	† Signetics	
	74155	Signetics	
	SN54155	† TI	
	SN74155	TI	
TTL-LS	9LS155C	Fairchild	
	9LS155M	† Fairchild	
	54LS155	† Fairchild	
	74LS155	Fairchild	
	HD74LS155	Hitachi	120
	SN54LS155	† Motorola	
	SN74LS155	Motorola	
	DM54LS155	† National	
	DM74LS155	National	
	µPB74LS155	NEC America	
	9LS155C	Raytheon	
	9LS155M	† Raytheon	
	54LS155	† Raytheon	
	74LS155	Raytheon	
	74LS155	Signetics	130
	SN54LS155	† TI	
	SN74LS155	TI	

Decoders (Cont'd.)

Function	Device	Source	Line
Dual 2-Line to 4-Line Decoder/Demultiplexer, Open Collector (or 3-Line to 8-Line Decoder/Demultiplexer)			
TTL	54156	† Fairchild	
	74156	Fairchild	
	HD74156	Hitachi	
	M53356	Mitsubishi	
	MC54156	† Motorola	
	MC74156	Motorola	140
	DM54156	† National	
	DM74156	National	
	µPB74156	NEC America	
	54156	† Signetics	
	74156	Signetics	
	SN54156	† TI	
	SN74156	TI	
TTL-LS	9LS156C	Fairchild	
	9LS156M	† Fairchild	
	54LS156	† Fairchild	150
	74LS156	Fairchild	
	HD74LS156	Hitachi	
	SN54LS156	† Motorola	
	SN74LS156	Motorola	
	DM54LS156	† National	
	DM74LS156	National	
	9LS156C	Raytheon	
	9LS156M	† Raytheon	
	54LS156	† Raytheon	
	74LS156	Raytheon	160
	74LS156	Signetics	
	SN54LS156	† TI	
	SN74LS156	TI	
Dual 2-Line to 4-Line Decoder/Demultiplexer (or 3-Line to 8-Line Decoder/Demultiplexer) Three-State			
TTL-LS	9LS255C	Raytheon	
	9LS255M	† Raytheon	
	54LS255	† Raytheon	
	74LS255	Raytheon	
Dual 2-Line to 4-Line Decoder/Demultiplexer			170
TTL-LS	AM25LS139C	AMD	
	AM25LS139M	AMD	
	SN54LS139	† AMD	
	SN74LS139	AMD	
	9LS139C	Fairchild	
	9LS139M	† Fairchild	
	54LS139	† Fairchild	
	74LS139	Fairchild	
	HD74LS139	Hitachi	
	SN54LS139	† Motorola	180
	SN74LS139	Motorola	
	DM54LS139	† National	
	DM74LS139	National	
	µPB74LS139	NEC America	
	9LS139C	Raytheon	
	9LS139M	† Raytheon	
	25LS139C	Raytheon	
	25LS139M	† Raytheon	
	54LS139	† Raytheon	
	74LS139	Raytheon	190
	54LS139	† Signetics	
	74LS139	Signetics	
	SN54LS139	† TI	
	SN74LS139	TI	
TTL-S	93S21C	AMD	
	93S21M	† AMD	
	SN54S139	† AMD	
	SN74S139	AMD	
	54S139	† Fairchild	
	74S139	Fairchild	200
	DM74S139	National	

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† Military Temperature Range (−55° to 125°C)

* Typical Values

Bold face indicates additional data is provided on the page noted.

DIGITAL–TTL (Cont'd)

Decoders (Cont'd.)

Function	Device	Source	Line
TTL-S		(Cont'd.)	
	54S139	† Signetics	
	74S139	Signetics	
	SN54S139	† TI	
	SN74S139	TI	
Dual 2-Line to 4-Line Decoder/Demultiplexer, Three-State			
TTL-LS	AM25LS2539C	AMD	
	AM25LS2539M	† AMD	
3-Line to 8-Line Decoder/Demultiplexer			10
TTL-LS	AM25LS138C	AMD	
	AM25LS138M	AMD	
	SN54LS138	† AMD	
	SN74LS138	AMD	
	9LS138C	Fairchild	
	9LS138M	† Fairchild	
	54LS138	† Fairchild	
	74LS138	Fairchild	
	HD74LS138	Hitachi	
	SN54LS138	† Motorola	20
	SN74LS138	Motorola	
	DM54LS138	† National	
	DM74LS138	National	
	μPB74LS138	NEC America	
	9LS138C	Raytheon	
	9LS138M	† Raytheon	
	25LS138C	Raytheon	
	25LS138M	† Raytheon	
	54LS138	† Raytheon	
	74LS138	Raytheon	30
	54LS138	† Signetics	
	74LS138	Signetics	
	SN54LS138	† TI	
	SN74LS138	TI	
TTL-S	SN54S138	† AMD	
	SN74S138	AMD	
	54S138	† Fairchild	
	74S138	Fairchild	
	3205	Intel	
	M5S138	Mitsubishi	40
	DM74S138	National	
	74S138	† Signetics	
	SN54S138	† TI	
	SN74S138	TI	
3-Line to 8-Line Decoder/Demultiplexer, Inverting/Non-Inverting, Three-State			
TTL-LS	AM25LS2538C	AMD	
	AM25LS2538M	† AMD	
3-Line to 8-Line Decoder/Demultiplexer, Inverting/Non-Inverting, Input Latches			50
TTL-LS	AM25LS2536C	AMD	
	AM25LS2536M	† AMD	
3-Line to 8-Line Decoder/Demultiplexer with Input Latches			
TTL-LS	SN54LS137	† TI	
	SN74LS137	TI	
TTL-S	93S137C	Fairchild	
	93S137M	† Fairchild	
Binary to Octal (1 of 8) Decoder			
TTL	9301C	Fairchild	60
	9301M	† Fairchild	
	M54402	Mitsubishi	
	MC4006	Motorola	
	MC4306	† Motorola	
	MC7250	Motorola	
	MC8250	† Motorola	

(Continued)

Decoders (Cont'd.)

Function	Device	Source	Line
TTL		(Cont'd.)	
	AN852	Panasonic	
	RC8250	Raytheon	
	RM8250	† Raytheon	70
	N8250	Signetics	
	S8250	† Signetics	
	9301	Signetics	
TTL-S	N82S50	Signetics	
Binary to Octal Decoder, Non-Inverting			
TTL	MC4048	Motorola	
Binary to Octal Decoder, Inverting/Non-Inverting, Open Collector			
TTL	MC4038	Motorola	
Binary to Octal (1 of 8) Decoder, Polarity Control, Three-State			80
TTL-LS	AM2921C	AMD	
	AM2921M	† AMD	
1-Line to 8-Line Demultiplexer			
TTL	DM7223	† National	
	DM8223	National	
Binary to 2-of-8 Decoder, Open Collector			
TTL	MC4040	Motorola	
4-Line to 16-Line Decoder/Demultiplexer			
TTL	9311C	AMD	90
	9311M	† AMD	
	SN54154	† AMD	
	SN74154	AMD	
	9311C	Fairchild	
	9311M	† Fairchild	
	54154	† Fairchild	
	74154	Fairchild	
	ZN54154	† Ferranti	
	ZN74154	Ferranti	
	HD74154	Hitachi	100
	M53354	Mitsubishi	
	MC8311	Motorola	
	MC9311	† Motorola	
	MC54154	† Motorola	
	MC74154	Motorola	
	DM54154	† National	
	DM74154	National	
	DM8311	National	
	DM9311	† National	
	μPB74154	NEC America	110
	RC9311	Raytheon	
	RM9311	† Raytheon	
	54154	† Signetics	
	74154	Signetics	
	SN29311	TI	
	SN39311	† TI	
	SN54154	† TI	
	SN74154	TI	
TTL-LS	DM54LS154	† National	
	DM74LS154	National	120
	54LS154	† Signetics	
	74LS154	Signetics	
4-Line to 16-Line Decoder/Demultiplexer, Open Collector Output			
TTL-LS	HD74159	Hitachi	
TTL	SN54159	† TI	
	SN74159	TI	

Drivers

Function	Device	Source	Line
Quad Predriver, Open Collector			
TTL	MC4042	Motorola	
Quad 2-Input AND Buffer, Open Collector, to 15v Output (High Voltage 54/74109)			130
TTL	DS7819	† National	
	DS8819	National	
Hex Buffer/Driver, Open Collector High Voltage Output, to 15v			
TTL	5417	† Fairchild	
	7417	Fairchild	
	HD7417	Hitachi	
	M53217	Mitsubishi	
	MC5417	† Motorola	140
	MC7417	Motorola	
	DM5417	† National	
	DM7417	National	
	5417	† Signetics	
	7417	Signetics	
	SN5417	† TI	
	SN7417	TI	
	TD3417	Toshiba	
Hex Buffer/Driver, Open Collector High Voltage Output, to 30v			150
TTL	5407	† Fairchild	
	7407	Fairchild	
	HD7407	Hitachi	
	M53207	Mitsubishi	
	MC5407	† Motorola	
	MC7407	Motorola	
	DM5407	† National	
	DM7407	National	
	5407	† Signetics	
	7407	Signetics	160
	SN5407	† TI	
	SN7407	TI	
	TD3407	Toshiba	
Hex Inverter Buffer/Driver Open Collector High Voltage Output, to 15v			
TTL	5416	† Fairchild	
	7416	Fairchild	
	HD7416	Hitachi	
	M53216	Mitsubishi	
	MC5416	† Motorola	170
	MC7416	Motorola	
	DM5416	† National	
	DM7416	National	
	DS7812	† National	
	DS8812	National	
	5416	† Signetics	
	7416	Signetics	
	SN5416	† TI	
	SN7416	TI	
	TD3416	Toshiba	180
Hex Inverter Buffer/Driver, Open Collector High Voltage Output, to 30v			
TTL	5406	† Fairchild	
	7406	Fairchild	
	HD7406	Hitachi	
	M53206	Mitsubishi	
	MC5406	† Motorola	
	MC7406	Motorola	
	DM5406	† National	
	DM7406	National	190
	5406	† Signetics	
	7406	Signetics	
	SN5406	† TI	
	SN7406	TI	
	TD3406	Toshiba	

† Military Temperature Range (−55° to 125°C)

* Typical Values

DIGITAL–TTL (Cont'd)

Drivers (Cont'd.)

Function	Device	Source
Hex High Voltage Interface Driver, Open Collector, to 35v		
TTL	HD235	† Harris
	HD535	Harris
Quad 2-Input NAND Buffer, Open Collector, to 15v Output		
TTL	5426	† Fairchild
	7426	Fairchild
	HD7426	Hitachi
	MC5426	† Motorola
	MC7426	Motorola
	DM5426	† National
	DM7426	National
	DS7810	† National
	DS8810	National
	DS7811	† National
	DS8811	National
	5426	† Signetics
	7426	Signetics
	SN5426	† TI
	SN7426	TI
	TD3426	Toshiba
Quad 2-Input NAND Buffer, Open Collector, to 30v Output		
TTL	N8T80	Signetics
	S8T80	† Signetics
4-Input NAND High Voltage, High Current Driver (40 to 50v, sinks 150 to 500ma)		
TTL	SH2001C	Fairchild
	SH2001M	† Fairchild
	SH2002C	Fairchild
	SH2002M	† Fairchild
	SH2200C	Fairchild
	SH2200M	† Fairchild
Quad 2-Input AND Power Driver (to 70v, sinks 300ma)		
TTL	MN204	Micro Net
	MN304	Micro Net
	MN304H	† Micro Net
	UDN-5706A	Sprague
	UDS-5706H	† Sprague
Quad 2-Input AND Power Driver, Open Collector (to 100v, sinks 500ma)		
TTL	UHC/D-400	† Sprague
	UHC/D-406	† Sprague
	UHC/D-500	† Sprague
	UHC/D-506	† Sprague
	UHP-400	Sprague
	UHP-406	Sprague
	UHP-500	Sprague
	UHP-506	Sprague
Quad 2-Input NAND Power Driver, Open Collector (to 100v, sinks 500ma)		
TTL	UHC/D-407	† Sprague
	UHC/D-408	† Sprague
	UHC/D-507	† Sprague
	UHC/D-508	† Sprague
	UHP-407	Sprague
	UHP-408	Sprague
	UHP-507	Sprague
	UHP-508	Sprague
Quad 2-Input NAND Bus Driver, Open Collector, 80ma		
TTL	96101	Fairchild
Quad 2-Input OR Power Driver, Open Collector (to 100v, sinks 500ma)		
TTL	UHC/D-402	† Sprague
	UHC/D-403	† Sprague
	UHC/D-502	† Sprague

(Continued)

Drivers (Cont'd.)

Function	Device	Source
TTL		(Cont'd.)
	UHC/D-503	† Sprague
	UHP-402	Sprague
	UHP-403	Sprague
	UHP-502	Sprague
	UHP-503	Sprague
Quad 2-Input NOR Power Driver, Open Collector (to 100v, sinks 500ma)		
TTL	UHC/D-432	† Sprague
	UHC/D-433	† Sprague
	UHC/D-532	† Sprague
	UHC/D-533	† Sprague
	UHP-432	Sprague
	UHP-433	Sprague
	UHP-532	Sprague
	UHP-533	Sprague
Quad 2-Input NOR 75-Ohm/50-Ohm Line Driver		
TTL	74128	Signetics
	SN54128	† TI
	SN74128	TI
Hex Interface Inverter, Open Collector, to 30v		
TTL	N8T90	Signetics
	S8T90	† Signetics
Hex Interface Inverter, Open Collector, to 50v or to 50ma)		
TTL	HD534	Harris
Quad Bus Driver, Three-State		
TTL	RC8T09	Raytheon
	RM8T09	† Raytheon
	N8T09	Signetics
	S8T09	† Signetics
Hex Bus Driver, Gated Enable, Three-State		
TTL	DM54365	† National
	DM74365	National
	54365A	† Signetics
	74365A	Signetics
	SN54365	† TI
	SN74365	TI
Hex Bus Driver, Gated Enable, Inverted Three-State Output		
TTL	DM54366	† National
	DM74366	National
	54366A	† Signetics
	74366A	Signetics
	SN54366	† TI
	SN74366	TI
Hex Bus Driver, 2-Line and 4-Line Enable, Three-State		
TTL	DM54367	† National
	DM74367	National
	54367A	† Signetics
	74367A	Signetics
	SN54367	† TI
	SN74367	TI
Hex Bus Driver, 2-Line and 4-Line Enable, Inverted Three-State Output		
TTL	DM54368	† National
	DM74368	National
	54368A	† Signetics
	74368A	Signetics
	SN54368	† TI
	SN74368	TI
Dual 3-Input 3-Output AND Series Terminated Line Driver		
TTL-H	MC3028	Motorola
	MC3128	† Motorola

Drivers (Cont'd.)

Function	Device	Source
Dual 3-Input 3-Output NAND Series Terminated Line Driver		
TTL-H	MC3029	Motorola
	MC3129	† Motorola
Dual 4-Input Positive NAND 50 Ohm Line Driver		
TTL-S	54S140	† Fairchild
	74S140	† Fairchild
	HD74S140	Hitachi
	DM74S140	National
	54S140	† Signetics
	74S140	Signetics
	SN54S140	† TI
	SN74S140	TI

See Also Interface-Memory and Peripheral Drivers

Flip-Flops

Function	Device	Source
"J-K" Master-Slave Flip-Flop		
TTL	9000C	Fairchild
	9000M	† Fairchild
	9001C	Fairchild
	9001M	† Fairchild
	54104	† Fairchild
	74104	Fairchild
	54105	† Fairchild
	74105	Fairchild
	μPB74105	NEC America
AND Gated "J-K" Master-Slave Flip-Flop with Preset and Clear		
TTL	5472	† Fairchild
	7472	Fairchild
	ZN5472	† Ferranti
	ZN7472	Ferranti
	HD7472	Hitachi
	M5375	Mitsubishi
	M53272	Mitsubishi
	MC5472	† Motorola
	MC7472	Motorola
	DM5472	† National
	DM7472	National
	7472	Signetics
	5472	† Signetics
	SN5472	† TI
	SN7472	TI
	TD3472	Toshiba
TTL-H	54H72	† Fairchild
	74H72	Fairchild
	MC3051	Motorola
	MC3151	† Motorola
	DM54H72	† National
	DM74H72	National
	54H72	† Signetics
	74H72	Signetics
	SN54H72	† TI
	SN74H72	TI
AND Gated "J-K" Master-Slave Flip-Flop with Data Lockout		
TTL	SN54110	† TI
	SN74110	TI
AND Gated, Edge-Triggered "J-K" Flip-Flop with Preset and Clear		
TTL	5470	† Fairchild
	7470	Fairchild
	ZN5470	† Ferranti
	ZN7470	Ferranti
	M53270	Mitsubishi
	MC5470	† Motorola
	MC7470	Motorola

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† Military Temperature Range (−55° to 125°C)

* Typical Values

Bold face indicates additional data is provided on the page noted.

DIGITAL–TTL (Cont'd)

Flip-Flops (Cont'd.)

Function	Device	Source	Line
TTL (Cont'd.)			
	DM5470	† National	
	DM7470	National	
	5470	† Signetics	
	7470	Signetics	
	N8270	Signetics	
	S8270	† Signetics	
	SN5470	† TI	
	SN7470	TI	10
"J-K" Negative Edge-Triggered Flip-Flop, AND Input			
TTL-H	54H102	† Fairchild	
	74H102	Fairchild	
	54H102	† Signetics	
	74H102	Signetics	
	SN54H102	† TI	
	SN74H102	TI	
"J-K" Master-Slave Flip-Flop, AND-OR Input			
TTL-H	54H71	† Fairchild	
	74H71	Fairchild	20
	DM54H71	† National	
	DM74H71	National	
	54H71	† Signetics	
	74H71	Signetics	
	SN54H71	† TI	
	SN74H71	TI	
"J-K" Negative Edge-Triggered Flip-Flop, AND-OR Input			
TTL-H	54H101	† Fairchild	
	74H101	Fairchild	30
	54H101	† Signetics	
	74H101	Signetics	
	SN54H101	† TI	
	SN74H101	TI	
Dual "J-K" Negative Edge-Triggered Flip-Flop, with Clear			
TTL-H	54H103	† Fairchild	
	74H103	Fairchild	
	DM54H103	† National	
	DM74H103	National	40
	54H103	† Signetics	
	74H103	Signetics	
	SN54H103	† TI	
	SN74H103	TI	
Dual "J-K" Negative Edge-Triggered Flip-Flop, Preset, Common Clear, Common Clock			
TTL-H	54H108	† Fairchild	
	74H108	Fairchild	
	DM54H108	† National	
	DM74H108	National	50
	54H108	† Signetics	
	74H108	Signetics	
	SN54H108	† TI	
	SN74H108	TI	
AND Input "JJ-$\overline{KK}$" Flip-Flop			
TTL-H	MC3052	Motorola	
	MC3152	† Motorola	
Dual "J-$\overline{K}$" Flip-Flop with Preset, Common Clock and Common Clear			
TTL-LS	54LS78	† Fairchild	
	74LS78	Fairchild	60
	HD74LS78	Hitachi	
	SN54LS78A	† Motorola	
	SN74LS78A	Motorola	
	DM54LS78	† National	
	DM74LS78	National	
	9LS78C	Raytheon	
		(Continued)	

Flip-Flops (Cont'd.)

Function	Device	Source	Line
TTL-LS (Cont'd.)			
	9LS78M	† Raytheon	70
	54LS78	Raytheon	
	74LS78	Raytheon	
	54LS78	† Signetics	
	74LS78	Signetics	
	SN54LS78A	† TI	
	SN74LS78A	TI	
TTL-H	54H78	† Fairchild	
	74H78	Fairchild	
	DM54H78	† National	
	DM74H78	National	80
	SN54H78	† TI	
	SN74H78	TI	
Dual "J-$\overline{K}$" Positive Edge-Triggered Flip-Flop, Preset and Clear			
TTL	9024C	Fairchild	
	9024M	† Fairchild	
	DM54109	† National	
	DM74109	National	
	54109	† Signetics	
	74109	Signetics	90
	SN54109	† TI	
	SN74109	TI	
TTL-LS	9LS109C	Fairchild	
	9LS109M	† Fairchild	
	54LS109	† Fairchild	
	74LS109	Fairchild	
	SN54LS109A	† Motorola	
	SN74LS109A	Motorola	
	DM54LS109	† National	
	DM74LS109	National	100
	µPB74LS109	NEC America	
	9LS109C	Raytheon	
	9LS109M	† Raytheon	
	54LS109	† Raytheon	
	74LS109	Raytheon	
	54LS109	† Signetics	
	74LS109	Signetics	
	SN54LS109A	† TI	
	SN74LS109A	TI	
TTL-S	54S109	† Fairchild	110
	74S109	Fairchild	
Dual "J-K" Negative Edge-Triggered Flip-Flop, Separate Preset and Clock, (no Clear)			
TTL-LS	9LS113C	Fairchild	
	9LS113M	† Fairchild	
	54LS113	† Fairchild	
	74LS113	Fairchild	
	HD74LS113	Hitachi	
	SN54LS113A	† Motorola	
	SN74LS113A	Motorola	120
	DM54LS113	† National	
	DM74LS113	National	
	µPB74LS113	NEC America	
	9LS113C	Raytheon	
	9LS113M	† Raytheon	
	54LS113	† Raytheon	
	74LS113	Raytheon	
	54LS113	† Signetics	
	74LS113	Signetics	
	SN54LS113A	† TI	130
	SN74LS113A	TI	
TTL-S	54S113	† Fairchild	
	74S113	Fairchild	
	HD74S113	Hitachi	
	M5S113	Mitsubishi	
		(Continued)	

Flip-Flops (Cont'd.)

Function	Device	Source	Line
TTL-S (Cont'd.)			
	DM74S113	National	
	54S113	† Signetics	
	74S113	Signetics	140
	SN54S113	† TI	
	SN74S113	TI	
Dual "J-K" Negative Edge-Triggered Flip-Flop with Preset, Common Clock and Common Clear			
TTL-LS	9LS114C	Fairchild	
	9LS114M	† Fairchild	
	54LS114	† Fairchild	
	74LS114	Fairchild	
	HD74LS114	Hitachi	
	SN54LS114A	† Motorola	150
	SN74LS114A	Motorola	
	DM54LS114	† National	
	DM74LS114	National	
	9LS114C	Raytheon	
	9LS114M	† Raytheon	
	54LS114	† Raytheon	
	74LS114	Raytheon	
	54LS114	† Signetics	
	74LS114	Signetics	
	SN54LS114A	† TI	160
	SN74LS114A	TI	
TTL-S	54S114	† Fairchild	
	74S114	Fairchild	
	HD74S114	Hitachi	
	M5S114	Mitsubishi	
	DM74S114	National	
	54S114	† Signetics	
	74S114	Signetics	
	SN54S114	† TI	
	SN74S114	TI	170
Dual "J-K" Negative Edge-Triggered Flip-Flop with Preset and Clear			
TTL-LS	9LS112C	Fairchild	
	9LS112M	† Fairchild	
	54LS112	† Fairchild	
	74LS112	Fairchild	
	HD74LS112	Hitachi	
	SN54LS112A	† Motorola	
	SN74LS112A	Motorola	
	DM54LS112	† National	180
	DM74LS112	National	
	µPB74LS122	NEC America	
	9LS112C	Raytheon	
	9LS112M	† Raytheon	
	54LS112	† Raytheon	
	74LS112	Raytheon	
	54LS112	Signetics	
	74LS112	Signetics	
	SN54LS112A	† TI	
	SN74LS112A	TI	190
TTL-S	54S112	† Fairchild	
	74S112	Fairchild	
	HD74S112	Hitachi	
	M5S112	Mitsubishi	
	DM74S112	National	
	54S112	† Signetics	
	74S112	Signetics	
	SN54S112	† TI	
	SN74S112	TI	
TTL-H	54H106	† Fairchild	200
	74H106	Fairchild	
	DM54H106	† National	
	DM74H106	National	
		(Continued)	

† Military Temperature Range (−55° to 125°C)

* Typical Values

DIGITAL–TTL (Cont'd)

Function	Device	Source	Line
Flip-Flops (Cont'd.)			
TTL-H		(Cont'd.)	
	54H106	† Signetics	
	74H106	Signetics	
	SN54H106	† TI	
	SN74H106	TI	
Dual "J-K" Master-Slave Flip-Flop			
TTL	9020C	Fairchild	
	9020M	† Fairchild	
Dual "J-K" Master-Slave Flip-Flop with Clear			10
TTL	5473	† Fairchild	
	7473	Fairchild	
	54107	† Fairchild	
	74107	Fairchild	
	ZN5473	† Ferranti	
	ZN7473	Ferranti	
	ZN54107	† Ferranti	
	ZN74107	Ferranti	
	HD7473	Hitachi	
	HD74107	Hitachi	20
	M5373	Mitsubishi	
	M53273	Mitsubishi	
	M53307	Mitsubishi	
	MC5473	† Motorola	
	MC7473	Motorola	
	MC54107	† Motorola	
	MC74107	Motorola	
	DM5473	† National	
	DM7473	National	
	DM54107	† National	30
	DM74107	National	
	μPB7473	NEC America	
	μPB74107	NEC America	
	5473	† Signetics	
	7473	Signetics	
	54107	† Signetics	
	74107	Signetics	
	SN5473	† TI	
	SN7473	† TI	
	SN54107	† TI	40
	SN74107	TI	
	TD3473	Toshiba	
	TD34107	Toshiba	
TTL-LS	9LS73C	Fairchild	
	9LS73M	† Fairchild	
	54LS73	† Fairchild	
	74LS73	Fairchild	
	54LS107	† Fairchild	
	74LS107	Fairchild	
	HD74LS73	Hitachi	50
	HD74LS107	Hitachi	
	SN54LS73A	† Motorola	
	SN74LS73A	Motorola	
	SN54LS107A	† Motorola	
	SN74LS107A	Motorola	
	DM54LS73	† National	
	DM74LS73	National	
	DM54LS107	† National	
	DM74LS107	National	
	9LS73C	Raytheon	60
	9LS73M	† Raytheon	
	54LS73	† Raytheon	
	74LS73	Raytheon	
	9LS107C	Raytheon	
	9LS107M	† Raytheon	
	54LS107	† Raytheon	
	74LS107	Raytheon	
	54LS73	† Signetics	
	74LS73	Signetics	

(Continued)

Function	Device	Source	Line
Flip-Flops (Cont'd.)			
TTL-LS		(Cont'd.)	70
	54LS107	† Signetics	
	74LS107	Signetics	
	SN54LS73A	† TI	
	SN74LS73A	TI	
	SN54LS107A	† TI	
	SN74LS107A	TI	
TTL-H	54H73	† Fairchild	
	74H73	Fairchild	
	MC3061	Motorola	
	MC3062	Motorola	80
	MC3161	† Motorola	
	MC3162	† Motorola	
	DM54H73	† National	
	DM74H73	National	
	54H73	† Signetics	
	74H73	Signetics	
	SN54H73	† TI	
	SN74H73	TI	
Dual "J-K" Master-Slave Flip-Flop with Preset and Clear			90
TTL	5476	† Fairchild	
	7476	Fairchild	
	9022C	Fairchild	
	9022M	† Fairchild	
	ZN5476	† Ferranti	
	ZN7476	Ferranti	
	HD7476	Hitachi	
	M5376	Mitsubishi	
	M53276	Mitsubishi	
	MC5476	† Motorola	100
	MC7476	Motorola	
	DM5476	† National	
	DM7476	National	
	μPB7476	NEC America	
	7476	Signetics	
	5476	† Signetics	
	SN5476	† TI	
	SN7476	TI	
	TD3476	Toshiba	
TTL-LS	54LS76	† Fairchild	110
	74LS76	Fairchild	
	HD74LS76	Hitachi	
	SN54LS76A	† Motorola	
	SN74LS76A	Motorola	
	DM54LS76	† National	
	DM74LS76	National	
	9LS76C	Raytheon	
	9LS76M	† Raytheon	
	54LS76	† Raytheon	
	74LS76	Raytheon	120
	54LS76	† Signetics	
	74LS76	Signetics	
	SN54LS76A	† TI	
	SN74LS76A	TI	
TTL-H	54H76	† Fairchild	
	74H76	Fairchild	
	DM54H76	† National	
	DM74H76	National	
	54H76	† Signetics	
	74H76	Signetics	130
	SN54H76	† TI	
	SN74H76	TI	
Dual "J-K" Master-Slave Flip-Flop with Data Lockout			
TTL	SN74111	TI	
Dual Gated Master-Slave "J-K/D" Flip-Flop			
TTL	DM7512	† National	

(Continued)

Function	Device	Source	Line
Flip-Flops (Cont'd.)			
TTL		(Cont'd.)	
	DM8512	National	
Quad "J-$\bar{K}$" Edge-Triggered Flip-Flop with Clear			
TTL	SN54376	† TI	140
	SN74376	TI	
Quad "J-$\bar{K}$" Edge-Triggered Flip-Flop with Preset and Clear			
TTL	SN74276	TI	
Dual D-Type Flip-Flop			
TTL	MC5479	† Motorola	
	MC7479	Motorola	
Dual D-Type Positive Edge-Triggered Flip-Flop with Preset and Clear			
TTL	5474	† Fairchild	150
	7474	Fairchild	
	ZN5474	† Ferranti	
	ZN7474	Ferranti	
	HD7474	Hitachi	
	M5374	Mitsubishi	
	M53274	Mitsubishi	
	MC5474	† Motorola	
	MC7474	Motorola	
	DM5474	† National	
	DM7474	National	160
	μPB7474	NEC America	
	5474	† Signetics	
	7474	Signetics	
	SN5474	† TI	
	SN7474	TI	
	TD3474	Toshiba	
TTL-LS	9LS74C	Fairchild	
	9LS74M	† Fairchild	
	54LS74	† Fairchild	
	74LS74	Fairchild	170
	HD74LS74A	Hitachi	
	SN54LS74A	† Motorola	
	SN74LS74A	Motorola	
	DM54LS74	† National	
	DM74LS74	National	
	μPB74LS74	NEC America	
	9LS74C	Raytheon	
	9LS74M	† Raytheon	
	54LS74	† Raytheon	
	74LS74	Raytheon	180
	54LS74A	† Signetics	
	74LS74A	Signetics	
	SN54LS74A	† TI	
	SN74LS74A	TI	
TTL-H	54H74	† Fairchild	
	74H74	Fairchild	
	MC3060	Motorola	
	MC3160	† Motorola	
	DM54H74	† National	
	DM74H74	National	190
	54H74	† Signetics	
	74H74	Signetics	
	SN54H74	† TI	
	SN74H74	TI	
TTL-S	54S74	† Fairchild	
	74S74	Fairchild	
	HD74S74	Hitachi	
	M5S074	Mitsubishi	
	DM74S74	National	
	54S74	† Signetics	200
	74S74	Signetics	
	SN54S74	† TI	

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† Military Temperature Range (−55° to 125°C)

* Typical Values

Bold face indicates additional data is provided on the page noted.

DIGITAL–TTL (Cont'd)

Flip-Flops (Cont'd.)

Function	Device	Source	Line
TTL-S (Cont'd.)	SN74S74	TI	
Dual Gated D Flip-Flop			
TTL	DM7511	† National	
	DM8511	National	
Quad Gated D Flip-Flop			
TTL	DM7613	† National	
	DM8613	National	
Quad D-Type Flip-Flop, Common Clock			10
TTL	MC4015	Motorola	
Quad D-Type Flip-Flop, Three-State			
TTL	54173	† Fairchild	
	74173	Fairchild	
	HD74173	Hitachi	
	DM54173	† National	
	DM74173	National	
	DM7551	† National	
	DM8551	National	
	RC8T10	Raytheon	20
	RM8T10	† Raytheon	
	N8T10	Signetics	
	S8T10	† Signetics	
	74173	Signetics	
	SN54173	† TI	
	SN74173	TI	
TTL-LS	9LS173C	Fairchild	
	9LS173M	† Fairchild	
	54LS173A	† Fairchild	
	74LS173A	Fairchild	30
	SN54LS173A	† Motorola	
	SN74LS173A	Motorola	
	DM54LS173	† National	
	DM74LS173	National	
	54LS173	† Signetics	
	74LS173	Signetics	
	SN54LS173	† TI	
	SN74LS173	TI	
Quad D-Type Edge-Triggered Flip-Flop with Clear, Complementary Output			
TTL	SN54175	† AMD	
	SN74175	AMD	40
	54175	† Fairchild	
	74175	Fairchild	
	ZN54175	† Ferranti	
	ZN74175	Ferranti	
	HD74175	Hitachi	
	M53375	Mitsubishi	
	MC54175	† Motorola	
	MC74175	Motorola	
	DM54175	† National	50
	DM74175	National	
	μPB74175	NEC America	
	54175	† Signetics	
	74175	Signetics	
	SN54175	† TI	
	SN74175	TI	
TTL-LS	AM25LS175C	AMD	
	AM25LS175M	AMD	
	SN54LS175	† AMD	
	SN74LS175	AMD	60
	9LS175C	Fairchild	
	9LS175M	† Fairchild	
	54LS175	† Fairchild	
	74LS175	Fairchild	
	HD74LS175	Hitachi	
	SN54LS175	† Motorola	

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Flip-Flops (Cont'd.)

Function	Device	Source	Line
TTL-LS (Cont'd.)	SN74LS175	Motorola	70
	DM54LS175	† National	
	DM74LS175	National	
	μPB74LS175	NEC America	
	9LS175M	† Raytheon	
	9LS175C	Raytheon	
	25LS175C	Raytheon	
	25LS175M	† Raytheon	
	54LS175	† Raytheon	
	74LS175	Raytheon	
	54LS175	† Signetics	80
	74LS175	Signetics	
	SN54LS175	† TI	
	SN74LS175	TI	
TTL-S	SN54S175	† AMD	
	SN74S175	AMD	
	54S175	† Fairchild	
	74S175	Fairchild	
	HD74S175	Hitachi	
	M5S175	Mitsubishi	
	DM74S175	National	90
	74S175	Signetics	
	SN74S175	TI	
	SN54S175	† TI	
Quad D-Type Flip-Flop with Common Clock Enable			
TTL-LS	AM25LS08C	AMD	
	AM25LS08M	† AMD	
	AM25LS379C	AMD	
	AM25LS379M	† AMD	
	SN54LS379	† AMD	
	SN74LS379	AMD	100
	54LS379	† Fairchild	
	74LS379	Fairchild	
	SN54LS379	† Motorola	
	SN74LS379	Motorola	
	SN54LS379	† TI	
	SN74LS379	TI	
TTL-S	AM25S08C	AMD	
	AM25S08M	† AMD	
	SN54S379	† AMD	
	SN74S379	AMD	110
Quad D-Type Flip-Flop, Standard TTL and Three-State Outputs			
TTL	AM2918C	AMD	
	AM2918M	† AMD	
	μPB2918A	NEC Micro	
	AM2918C	Raytheon	
	AM2918M	† Raytheon	
TTL-LS	AM25LS2518C	AMD	
	AM25LS2518M	† AMD	
	AM29LS18C	AMD	120
	AM29LS18M	† AMD	
	SN54LS388	† AMD	
	SN74LS388	AMD	
TTL-S	AM25S18C	AMD	
	AM25S18M	† AMD	
	SN54S388	† AMD	
	SN74S388	AMD	
Quad D-type Flip-Flop, Dual Three-State Outputs			
TTL-LS	AM25LS2519C	AMD	
	AM25LS2519M	† AMD	130
Quad D-Type Flip-Flop with Multiplexed Dual Inputs			
TTL	54298	† Fairchild	
	74298	Fairchild	
	MC54298	† Motorola	

(Continued)

Flip-Flops (Cont'd.)

Function	Device	Source	Line
TTL (Cont'd.)	MC74298	Motorola	
	54298	† Signetics	
	74298	Signetics	
	SN54298	† TI	
	SN74298	TI	140
TTL-LS	AM25LS09C	AMD	
	AM25LS09M	† AMD	
	AM25LS399C	AMD	
	AM25LS399M	† AMD	
	SN54LS399	† AMD	
	SN74LS399	AMD	
	9LS298C	Fairchild	
	9LS298M	† Fairchild	
	54LS298	† Fairchild	
	74LS298	Fairchild	150
	SN54LS298	† Motorola	
	SN74LS298	Motorola	
	SN54LS398	† Motorola	
	SN74LS398	Motorola	
	SN54LS399	† Motorola	
	SN74LS399	Motorola	
	9LS298C	Raytheon	
	9LS298M	† Raytheon	
	54LS298	† Raytheon	
	74LS298	Raytheon	160
	74LS298	Signetics	
	SN54LS298	† TI	
	SN74LS298	TI	
	SN54LS398	† TI	
	SN74LS398	TI	
	SN54LS399	† TI	
	SN74LS399	TI	
TTL-S	AM25S09C	AMD	
	AM25S09M	† AMD	
	SN54S399	† AMD	170
	SN74S399	AMD	
Hex D-Type Flip-Flop with Common Enable			
TTL-LS	AM25LS07C	AMD	
	AM25LS07M	† AMD	
	AM25LS378C	AMD	
	AM25LS378M	† AMD	
	SN54LS378	† AMD	
	SN74LS378	AMD	
	54LS378	† Fairchild	
	74LS378	Fairchild	180
	SN54LS378	† Motorola	
	SN74LS378	Motorola	
	74LS378	Signetics	
	SN54LS378	† TI	
	SN74LS378	TI	
TTL-S	AM25S07C	AMD	
	AM25S07M	† AMD	
	SN54S378	† AMD	
	SN74S378	AMD	
Hex D-Type Edge-Triggered Flip-Flop with Clear			190
TTL	SN54174	† AMD	
	SN74174	AMD	
	54174	† Fairchild	
	74174	Fairchild	
	93174C	Fairchild	
	ZN54174	† Ferranti	
	ZN74174	Ferranti	
	HD74174	Hitachi	
	M53374	Mitsubishi	
	MC54174	† Motorola	200
	MC74174	Motorola	

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Values

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DIGITAL–TTL (Cont'd)

Flip-Flops (Cont'd.)

Function	Device	Source	Line
TTL		(Cont'd.)	
	DM54174	† National	
	DM74174	National	
	54174	† Signetics	
	74174	Signetics	
	SN54174	† TI	
	SN74174	TI	
TTL-LS	AM25LS174C	AMD	
	AM25LS174M	† AMD	
	SN54LS174	† AMD	10
	SN74LS174	AMD	
	9LS174C	Fairchild	
	9LS174M	† Fairchild	
	54LS174	† Fairchild	
	74LS174	Fairchild	
	HD74LS174	Hitachi	
	SN74LS174	Motorola	
	DM54LS174	† National	
	DM74LS174	National	
	9LS174C	Raytheon	20
	9LS174M	† Raytheon	
	25LS174C	Raytheon	
	25LS174M	† Raytheon	
	54LS174	† Raytheon	
	74LS174	Raytheon	
	54LS174	† Signetics	
	74LS174	Signetics	
	SN54LS174	† TI	
	SN74LS174	TI	
TTL-S	SN54S174	† AMD	30
	SN74S174	AMD	
	54S174	† Fairchild	
	74S174	Fairchild	
	HD74S174	Hitachi	
	M5S174	Mitsubishi	
	DM74S174	National	
	54S174	† Signetics	
	74S174	Signetics	
	SN54S174	† TI	
	SN74S174	TI	40
Octal D-Type, Edge-Triggered Flip-Flop, with Clear			
TTL	SN74273	TI	
TTL-LS	AM25LS273C	AMD	
	AM25LS273M	† AMD	
	SN54LS273	† AMD	
	SN74LS273	AMD	
	54LS273	† Fairchild	
	74LS273	Fairchild	
	54LS273	**† MMI (509)**	
	74LS273	**MMI (509)**	50
	57LS313	**† MMI (509)**	
	67LS313	**MMI (509)**	
	SN54LS273	† Motorola	
	SN74LS273	Motorola	
	9LS273C	**Raytheon (531)**	
	9LS273M	**† Raytheon (531)**	
	25LS273C	**Raytheon (531)**	
	25LS273M	**† Raytheon (531)**	
	54LS273	**† Raytheon (531)**	
	74LS273	**Raytheon (531)**	60
	74LS273	Signetics	
	SN54LS273	† TI	
	SN74LS273	TI	
Octal D-Type Edge-Triggered Flip-Flop, Three-State			
TTL-LS	AM25LS374C	AMD	
	AM25LS374M	† AMD	
	SN54LS374	† AMD	

(Continued)

Flip-Flops (Cont'd.)

Function	Device	Source	Line
TTL-LS		(Cont'd.)	
	SN74LS374	AMD	
	54LS374	† Fairchild	70
	74LS374	Fairchild	
	54LS374	**MMI (505)**	
	74LS374	**MMI (505)**	
	SN54LS374	† Motorola	
	SN74LS374	Motorola	
	SN54LS574	† Motorola	
	SN74LS574	Motorola	
	DM54LS374	† National	
	DM74LS374	National	
	9LS374C	**Raytheon (543)**	80
	9LS374M	**† Raytheon (543)**	
	25LS374C	**Raytheon (543)**	
	25LS374M	**† Raytheon (543)**	
	54LS374	**† Raytheon (543)**	
	74LS374	**Raytheon (543)**	
	74LS364	Signetics	
	74LS374	Signetics	
	SN54LS364	† TI	
	SN74LS364	TI	
	SN54LS374	† TI	90
	SN74LS374	TI	
TTL-S	SN54S374	† AMD	
	SN74S374	AMD	
	54S374	**† MMI (505)**	
	74S374	**MMI (505)**	
	57S374	**† MMI (505)**	
	67S374	**MMI (505)**	
	SN54S374	† TI	
	SN74S374	TI	
Octal, D-Type Edge-Triggered Flip-Flop, Inverting, Three-State			100
TTL-LS	SN54LS534	† AMD	
	SN74LS534	AMD	
	57LS376	**† MMI (505)**	
	67LS376	**MMI (505)**	
TTL-S	SN54S534	† AMD	
	SN74S534	AMD	
	57S376	**† MMI (505)**	
	67S376	**MMI (505)**	
	57S378	**† MMI (505)**	110
	67S378	**MMI (505)**	
Octal D-Type Flip-Flop with Enable			
TTL-LS	AM25LS377C	AMD	
	AM25LS377M	† AMD	
	SN54LS377	† AMD	
	SN74LS377	AMD	
	54LS377	† Fairchild	
	74LS377	Fairchild	
	57LS314	**† MMI (509)**	
	67LS314	**MMI (509)**	120
	54LS377	**MMI (509)**	
	74LS377	**MMI (509)**	
	SN54LS377	† Motorola	
	SN74LS377	Motorola	
	9LS377C	**Raytheon (549)**	
	9LS377M	**† Raytheon (549)**	
	25LS377C	**Raytheon (549)**	
	25LS377M	**† Raytheon (549)**	
	54LS377	**† Raytheon (549)**	
	74LS377	**Raytheon (549)**	130
	74LS377	Signetics	
	SN54LS377	† TI	
	SN74LS377	TI	

Flip-Flops (Cont'd.)

Function	Device	Source	Line
Octal D-type Flip-Flop, Common Clear and Enable, Three-State			
TTL-LS	AM25LS2520C	AMD	
	AM25LS2520M	† AMD	
	AM2920C	AMD	
	AM2920M	† AMD	
Octal I/O Register, Three-State			140
TTL-LS	57LS315	† MMI	
	67LS315	MMI	
Quad I/O Register, Three-State (two terminals per flip-flop can be used as input or output)			
TTL	DM7542	† National	
	DM8542	National	

Gates, AND/NAND

Dual 4-Input AND Gate			
TTL	5421	† Fairchild	
	7421	Fairchild	
	5421	† Signetics	150
	7421	Signetics	
	TD3421	Toshiba	
TTL-LS	9LS21C	Fairchild	
	9LS21M	† Fairchild	
	54LS21	† Fairchild	
	74LS21	Fairchild	
	HD74LS21	Hitachi	
	SN54LS21	† Motorola	
	SN74LS21	Motorola	
	DM54LS21	† National	160
	DM74LS21	National	
	μPB74LS21	NEC America	
	9LS21C	Raytheon	
	9LS21M	† Raytheon	
	54LS21	† Raytheon	
	74LS21	Raytheon	
	54LS21	† Signetics	
	74LS21	Signetics	
	SN54LS21	† TI	
	SN74LS21	TI	170
TTL-H	54H21	† Fairchild	
	74H21	Fairchild	
	MC3011	Motorola	
	MC3111	† Motorola	
	DM54H21	† National	
	DM74H21	National	
	54H21	† Signetics	
	74H21	Signetics	
	SN74H21	† TI	
	SN74H21	TI	180
Dual 4-Input AND Power Gate			
TTL-H	MC3026	Motorola	
	MC3126	† Motorola	
Triple 3-Input AND Gate			
TTL	5411	† Fairchild	
	7411	Fairchild	
	HD74LS11	Hitachi	
	DM5411	† National	
	DM7411	National	
	5411	† Signetics	190
	7411	Signetics	
TTL-LS	9LS11C	Fairchild	
	9LS11M	† Fairchild	
	54LS11	† Fairchild	
	74LS11	Fairchild	
	SN54LS11	† Motorola	
	SN74LS11	Motorola	

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† Military Temperature Range (−55° to 125°C)

* Typical Values

Bold face indicates additional data is provided on the page noted.

DIGITAL–TTL (Cont'd)

Gates, AND/NAND (Cont'd.)

Function	Device	Source	Line
TTL-LS		(Cont'd.)	
	DM54LS11	† National	
	DM74LS11	National	
	μPB74LS11	NEC America	
	9LS11C	Raytheon	
	9LS11M	† Raytheon	
	54LS11	† Raytheon	
	74LS11	Raytheon	
	54LS11	† Signetics	
	74LS11	Signetics	10
	SN54LS11	TI	
	SN74LS11	† TI	
TTL-H	54H11	† Fairchild	
	74H11	Fairchild	
	MC3006	Motorola	
	MC3106	† Motorola	
	DM54H11	† National	
	DM74H11	National	
	54H11	† Signetics	
	74H11	Signetics	20
	SN54H11	† TI	
	SN74H11	TI	
TTL-S	54S11	† Fairchild	
	74S11	Fairchild	
	HD74S11	Hitachi	
	M5S011	Mitsubishi	
	DM74S11	National	
	54S11	† Signetics	
	74S11	Signetics	
	SN54S11	† TI	30
	SN74S11	TI	
Triple 3-Input AND Gate, Open Collector			
TTL-LS	9LS15C	Fairchild	
	9LS15M	† Fairchild	
	54LS15	† Fairchild	
	74LS15	Fairchild	
	HD74LS15	Hitachi	
	SN54LS15	† Motorola	
	SN74LS15	Motorola	
	DM54LS15	† National	40
	DM74LS15	National	
	9LS15C	Raytheon	
	9LS15M	† Raytheon	
	54LS15	† Raytheon	
	74LS15	Raytheon	
	54LS15	† Signetics	
	74LS15	Signetics	
	SN54LS15	† TI	
	SN74LS15	TI	
TTL-H	54H15	† Fairchild	50
	74H15	Fairchild	
	SN54H15	† TI	
	SN74H15	TI	
TTL-S	54S15	† Fairchild	
	74S15	Fairchild	
	HD74S15	Hitachi	
	M5S015	Mitsubishi	
	DM74S15	National	
	54S15	† Signetics	
	74S15	Signetics	60
	SN54S15	† TI	
	SN74S15	TI	
Quad 2-Input AND Gate			
TTL	5408	† Fairchild	
	7408	Fairchild	
	ZN5408	† Ferranti	
	ZN7408	Ferranti	

(Continued)

Gates, AND/NAND (Cont'd.)

Function	Device	Source	Line
TTL		(Cont'd.)	
	HD7408	Hitachi	
	M53208	Mitsubishi	70
	MC5408	† Motorola	
	MC7408	Motorola	
	DM5408	† National	
	DM7408	National	
	5408	† Signetics	
	7408	Signetics	
	SN5408	† TI	
	SN7408	TI	
	TD3408	Toshiba	
TTL-LS	9LS08C	Fairchild	80
	9LS08M	† Fairchild	
	54LS08	† Fairchild	
	74LS08	Fairchild	
	HD74LS08	Hitachi	
	SN54LS08	† Motorola	
	SN74LS08	Motorola	
	DM54LS08	† National	
	DM74LS08	National	
	μPB74LS08	NEC America	
	9LS08C	Raytheon	90
	9LS08M	† Raytheon	
	54LS08	† Raytheon	
	74LS08	Raytheon	
	54LS08	† Signetics	
	74LS08	Signetics	
	SN54LS08	† TI	
	SN74LS08	TI	
TTL-H	54H08	† Fairchild	
	74H08	Fairchild	
	MC3001	Motorola	100
	MC3101	† Motorola	
	DM54H08	† National	
	DM74H08	National	
	54H08	† Signetics	
	74H08	Signetics	
TTL-S	54S08	† Fairchild	
	74S08	Fairchild	
	54S08	† Signetics	
	74S08	Signetics	
	SN54S08	† TI	110
	SN74S08	TI	
Quad 2-Input AND Gate, Open Collector			
TTL	5409	† Fairchild	
	7409	Fairchild	
	ZN5409	Ferranti	
	ZN7409	Ferranti	
	HD7409	Hitachi	
	M53209	Mitsubishi	
	MC5409	† Motorola	
	MC7409	Motorola	120
	DM5409	† National	
	DM7409	National	
	5409	† Signetics	
	7409	Signetics	
	SN5409	† TI	
	SN7409	TI	
	TD3409	Toshiba	
TTL-LS	9LS09C	Fairchild	
	9LS09M	† Fairchild	
	54LS09	† Fairchild	130
	74LS09	Fairchild	
	HD74LS09	Hitachi	
	SN54LS09	† Motorola	
	SN74LS09	Motorola	

(Continued)

Gates, AND/NAND (Cont'd.)

Function	Device	Source	Line
TTL-LS		(Cont'd.)	
	DM54LS09	† National	
	DM74LS09	National	
	9LS09C	Raytheon	
	9LS09M	† Raytheon	
	54LS09	† Raytheon	140
	74LS09	Raytheon	
	54LS09	† Signetics	
	74LS09	Signetics	
	SN54LS09	† TI	
	SN74LS09	† TI	
TTL-H	54H09	† Fairchild	
	74H09	Fairchild	
TTL-S	54S09	† Fairchild	
	74S09	Fairchild	
	54S09	† Signetics	150
	74S09	Signetics	
	SN54S09	† TI	
	SN74S09	TI	
2-2-3-3 Input AND Gate			
TTL-S	9S41C	Fairchild	
	9S41M	† Fairchild	
8-Input NAND Gate			
TTL	5430	† Fairchild	
	7430	Fairchild	
	9007C	Fairchild	160
	9007M	† Fairchild	
	ZN5430	† Ferranti	
	ZN7430	Ferranti	
	HD7430	Hitachi	
	M53230	Mitsubishi	
	MC5430	† Motorola	
	MC7430	Motorola	
	DM5430	† National	
	DM7430	National	
	μPB7430	NEC America	170
	5430	† Signetics	
	7430	Signetics	
	SN5430	† TI	
	SN7430	TI	
	TD3430	Toshiba	
TTL-LS	9LS30C	Fairchild	
	9LS30M	† Fairchild	
	54LS30	† Fairchild	
	74LS30	Fairchild	
	HD74LS30	Hitachi	180
	SN54LS30	† Motorola	
	SN74LS30	Motorola	
	DM54LS30	† National	
	DM74LS30	National	
	μPB74LS30	NEC America	
	9LS30C	Raytheon	
	9LS30M	† Raytheon	
	54LS30	† Raytheon	
	74LS30	Raytheon	
	54LS30	† Signetics	190
	74LS30	Signetics	
	SN54LS30	† TI	
	SN74LS30	TI	
TTL-H	54H30	† Fairchild	
	74H30	Fairchild	
	MC3015	Motorola	
	MC3016	Motorola	
	MC3115	† Motorola	
	MC3116	† Motorola	
	DM54H30	† National	200
	DM74H30	National	

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Values

DIGITAL–TTL (Cont'd)

Gates, AND/NAND (Cont'd.)

Function	Device	Source	Line
TTL-H		(Cont'd.)	
	μPB74H30	NEC America	
	54H30	† Signetics	
	74H30	Signetics	
	SN54H30	† TI	
	SN74H30	TI	
TTL-S	54S30	† Fairchild	
	74S30	Fairchild	
	M5S030	Mitsubishi	
	DM74S30	National	10
	SN54S30	† TI	
	SN74S30	TI	
12-Input NAND Gate, Three-State			
TTL-S	54S134	† Fairchild	
	74S134	Fairchild	
	HD74S134	Hitachi	
	DM74S134	National	
	54S134	† Signetics	
	74S134	Signetics	
	SN54S134	† TI	20
	SN74S134	TI	
13-Input NAND Gate			
TTL-LS	9LS133C	Fairchild	
	9LS133M	† Fairchild	
	54LS133	† Fairchild	
	74LS133	Fairchild	
	SN54LS133	† Motorola	
	SN74LS133	Motorola	
TTL-S	54S133	† Fairchild	
	HD74S133	Hitachi	30
	74S133	Fairchild	
	M5S133	Mitsubishi	
	DM74S133	National	
	54S133	† Signetics	
	74S133	Signetics	
	SN54S133	† TI	
	SN74S133	TI	
Dual 4-Input NAND Gate			
TTL	5420	† Fairchild	
	7420	Fairchild	40
	9004C	Fairchild	
	9004M	† Fairchild	
	ZN7420	Ferranti	
	ZN5420	† Ferranti	
	HD7420	Hitachi	
	M53220	Mitsubishi	
	MC5420	† Motorola	
	MC7420	Motorola	
	DM5420	† National	
	DM7420	National	50
	DM9004C	National	
	μPB7420	NEC America	
	5420	† Signetics	
	7420	Signetics	
	SN5420	† TI	
	SN7420	TI	
	TD3420	Toshiba	
TTL-LS	9LS20C	Fairchild	
	9LS20M	† Fairchild	
	54LS20	† Fairchild	60
	74LS20	Fairchild	
	HD74LS20	Hitachi	
	SN54LS20	† Motorola	
	SN74LS20	Motorola	
	DM54LS20	† National	
	DM74LS20	National	
	μPB74LS20	NEC America	

(Continued)

Gates, AND/NAND (Cont'd.)

Function	Device	Source	Line
TTL-LS		(Cont'd.)	
	9LS20C	Raytheon	
	9LS20M	† Raytheon	70
	54LS20	† Raytheon	
	74LS20	Raytheon	
	54LS20	† Signetics	
	74LS20	Signetics	
	SN54LS20	† TI	
	SN74LS20	TI	
TTL-H	54H20	† Fairchild	
	74H20	Fairchild	
	MC3010	Motorola	
	MC3110	† Motorola	80
	DM54H20	† National	
	DM74H20	National	
	μPB74H20	NEC America	
	54H20	† Signetics	
	74H20	Signetics	
	SN54H20	† TI	
	SN74H20	TI	
TTL-S	54S20	† Fairchild	
	74S20	Fairchild	
	ZN54S20	† Ferranti	90
	ZN74S20	Ferranti	
	HD74S20	Hitachi	
	M5S020	Mitsubishi	
	DM74S20	National	
	54S20	† Signetics	
	74S20	Signetics	
	SN54S20	† TI	
	SN74S20	TI	
Dual 4-Input NAND Buffer			
TTL	5440	† Fairchild	100
	7440	Fairchild	
	9009C	Fairchild	
	9009M	† Fairchild	
	ZN5440	† Ferranti	
	ZN7440	Ferranti	
	HD7440	Hitachi	
	M53240	Mitsubishi	
	MC5440	† Motorola	
	MC7440	Motorola	
	DM5440	† National	110
	DM7440	National	
	DM9009C	National	
	μPB7440	NEC America	
	5440	† Signetics	
	7440	Signetics	
	SN5440	† TI	
	SN7440	TI	
	TD3440	Toshiba	
TTL-LS	9LS40C	Fairchild	
	9LS40M	† Fairchild	120
	54LS40	† Fairchild	
	74LS40	Fairchild	
	HD74LS40	Hitachi	
	SN54LS40	† Motorola	
	SN74LS40	Motorola	
	DM54LS40	† National	
	DM74LS40	National	
	μPB74LS40	NEC America	
	9LS40C	Raytheon	
	9LS40M	† Raytheon	130
	54LS40	† Raytheon	
	74LS40	Raytheon	
	54LS40	Signetics	
	74LS40	Signetics	
	SN54LS40	† TI	

(Continued)

Gates, AND/NAND (Cont'd.)

Function	Device	Source	Line
TTL-LS		(Cont'd.)	
	SN74LS40	TI	
TTL-H	54H40	† Fairchild	
	74H40	Fairchild	
	MC3024	Motorola	140
	MC3025	Motorola	
	MC3124	† Motorola	
	MC3125	† Motorola	
	DM54H40	† National	
	DM74H40	National	
	μPB74H40	NEC America	
	54H40	† Signetics	
	74H40	Signetics	
	SN54H40	† TI	
	SN74H40	TI	150
TTL-S	54S40	† Fairchild	
	74S40	Fairchild	
	HD74S40	Hitachi	
	M5S040	Mitsubishi	
	DM74S40	National	
	54S40	† Signetics	
	74S40	Signetics	
	SN54S40	† TI	
	SN74S40	TI	
Dual 4-Input NAND Gate, Open Collector			160
TTL	5422	† Fairchild	
	7422	Fairchild	
	HD7422	Hitachi	
	SN5422	† TI	
	SN7422	TI	
TTL-LS	9LS22C	Fairchild	
	9LS22M	† Fairchild	
	54LS22	† Fairchild	
	74LS22	Fairchild	
	HD74LS22	Hitachi	170
	SN54LS22	† Motorola	
	SN74LS22	Motorola	
	DM54LS22	† National	
	DM74LS22	National	
	9LS22C	Raytheon	
	9LS22M	† Raytheon	
	54LS22	† Raytheon	
	74LS22	Raytheon	
	54LS22	† Signetics	
	74LS22	Signetics	180
	SN54LS22	† TI	
	SN74LS22	TI	
TTL-H	54H22	† Fairchild	
	74H22	Fairchild	
	MC3012	Motorola	
	MC3112	† Motorola	
	DM54H22	† National	
	DM74H22	National	
	54H22	† Signetics	
	74H22	Signetics	190
	SN54H22	† TI	
	SN74H22	TI	
TTL-S	54S22	† Fairchild	
	74S22	Fairchild	
	ZN54S22	† Ferranti	
	ZN74S22	Ferranti	
	HD74S22	Hitachi	
	M5S022	Mitsubishi	
	DM74S22	National	
	54S22	† Signetics	200
	74S22	Signetics	
	SN54S22	† TI	

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Values

Bold face indicates additional data is provided on the page noted.

DIGITAL–TTL (Cont'd)

Gates, AND/NAND (Cont'd.)

Function	Device	Source	Line
TTL-S		(Cont'd.)	
	SN74S22	TI	
Dual 5-Input NAND Gate			
TTL	DM7092	† National	
	DM8092	National	
Triple 3-Input NAND Gate			
TTL	5410	† Fairchild	
	7410	Fairchild	
	9003C	Fairchild	
	9003M	† Fairchild	10
	ZN5410	† Ferranti	
	ZN7410	Ferranti	
	HD7410	Hitachi	
	M5330	Mitsubishi	
	M53210	Mitsubishi	
	MC5410	† Motorola	
	MC7410	Motorola	
	DM5410	† National	
	DM7410	National	
	DM9003C	National	20
	µPB7410	NEC America	
	5410	† Signetics	
	7410	Signetics	
	SN5410	† TI	
	SN7410	TI	
	TD3410	Toshiba	
TTL-LS	9LS10C	Fairchild	
	9LS10M	† Fairchild	
	54LS10	† Fairchild	
	74LS10	Fairchild	30
	HD74LS10	Hitachi	
	SN54LS10	† Motorola	
	SN74LS10	Motorola	
	DM54LS10	† National	
	DM74LS10	National	
	µPB74LS10	NEC America	
	9LS10C	Raytheon	
	9LS10M	† Raytheon	
	54LS10	† Raytheon	
	74LS10	Raytheon	40
	54LS10	† Signetics	
	74LS10	Signetics	
	SN54LS10	† TI	
	SN74LS10	TI	
TTL-H	54H10	† Fairchild	
	74H10	Fairchild	
	MC3005	Motorola	
	MC3105	† Motorola	
	DM54H10	† National	
	DM74H10	National	50
	µPB74H10	NEC America	
	54H10	† Signetics	
	74H10	Signetics	
	SN54H10	† TI	
	SN74H10	TI	
TTL-S	54S10	† Fairchild	
	74S10	Fairchild	
	HD74S10	Hitachi	
	M5S010	Mitsubishi	
	DM74S10	National	60
	54S10	† Signetics	
	74S10	Signetics	
	SN54S10	† TI	
	SN74S10	TI	
Triple 3-Input NAND Gate, Open Collector			
TTL	5412	† Fairchild	
	7412	Fairchild	

(Continued)

Gates, AND/NAND (Cont'd.)

Function	Device	Source	Line
TTL		(Cont'd.)	
	ZN5412	† Ferranti	
	ZN7412	Ferranti	70
	HD7412	Hitachi	
	5412	† Signetics	
	7412	Signetics	
	SN5412	† TI	
	SN7412	TI	
TTL-LS	54LS12	† Fairchild	
	74LS12	Fairchild	
	HD74LS12	Hitachi	
	SN54LS12	† Motorola	
	SN74LS12	Motorola	80
	DM54LS12	† National	
	DM74LS12	National	
	9LS12C	Raytheon	
	9LS12M	† Raytheon	
	54LS12	† Raytheon	
	74LS12	Raytheon	
	54LS12	† Signetics	
	74LS12	Signetics	
	SN54LS12	† TI	
	SN74LS12	TI	90
TTL-S	HD74S12	Hitachi	
TTL-H	MC3007	Motorola	
	MC3107	† Motorola	
Quad 2-Input NAND Gate			
TTL	5400	† Fairchild	
	7400	Fairchild	
	9002C	Fairchild	
	9002M	† Fairchild	
	ZN5400	† Ferranti	
	ZN7400	Ferranti	100
	HD7400	Hitachi	
	M5340	Mitsubishi	
	M53200	Mitsubishi	
	MC5400	† Motorola	
	MC7400	Motorola	
	DM5400	† National	
	DM7400	National	
	DM9002C	National	
	µPB7400	NEC America	
	5400	† Signetics	110
	7400	Signetics	
	SN5400	† TI	
	SN7400	TI	
	TD3400	Toshiba	
TTL-LS	9LS00C	Fairchild	
	9LS00M	† Fairchild	
	54LS00	† Fairchild	
	74LS00	Fairchild	
	HD74LS00	Hitachi	
	SN54LS00	† Motorola	120
	SN74LS00	Motorola	
	DM54LS00	† National	
	DM74LS00	National	
	µPB74LS00	NEC America	
	9LS00C	Raytheon	
	9LS00M	† Raytheon	
	54LS00	† Raytheon	
	74LS00	Raytheon	
	54LS00	† Signetics	
	74LS00	Signetics	130
	SN54LS00	† TI	
	SN74LS00	TI	
TTL-H	54H00	† Fairchild	
	74H00	Fairchild	

(Continued)

Gates, AND/NAND (Cont'd.)

Function	Device	Source	Line
TTL-H		(Cont'd.)	
	MC3000	Motorola	
	MC3100	† Motorola	
	DM54H00	† National	
	DM74H00	National	
	µPB74H00	NEC America	140
	54H00	† Signetics	
	74H00	Signetics	
	SN54H00	† TI	
	SN74H00	TI	
TTL-S	54S00	† Fairchild	
	74S00	† Fairchild	
	ZN54S00	† Ferranti	
	ZN74S00	Ferranti	
	HD74S00	Hitachi	
	M5S000	Mitsubishi	150
	DM74S00	National	
	54S00	† Signetics	
	74S00	Signetics	
	SN54S00	† TI	
	SN74S00	TI	
Quad 2-Input NAND Buffer			
TTL	5437	† Fairchild	
	7437	Fairchild	
	ZN5437	† Ferranti	
	ZN7437	Ferranti	160
	HD7437	Hitachi	
	M53237	Mitsubishi	
	MC5437	† Motorola	
	MC7437	Motorola	
	DM5437	† National	
	DM7437	National	
	DM7091	† National	
	DM8091	National	
	µPB7437	NEC America	
	5437	† Signetics	170
	7437	Signetics	
	SN5437	† TI	
	SN7437	TI	
	TD3437	Toshiba	
TTL-LS	9LS37C	Fairchild	
	9LS37M	† Fairchild	
	54LS37	† Fairchild	
	74LS37	Fairchild	
	HD74LS37	Hitachi	
	SN54LS37	† Motorola	180
	SN74LS37	Motorola	
	DM54LS37	† National	
	DM74LS37	National	
	µPB74LS37	NEC America	
	9LS37C	Raytheon	
	9LS37M	† Raytheon	
	54LS37	† Raytheon	
	74LS37	Raytheon	
	54LS37	† Signetics	
	74LS37	Signetics	190
	SN54LS37	† TI	
	SN74LS37	TI	
TTL-S	74S37	Signetics	
	SN54S37	† TI	
	SN74S37	TI	
Quad 2-Input NAND Gate, Open Collector			
TTL	5401	† Fairchild	
	7401	Fairchild	
	5403	† Fairchild	
	7403	Fairchild	200
	9012C	Fairchild	

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Values

DIGITAL–TTL (Cont'd)

Gates, AND/NAND (Cont'd.)

Function	Device	Source	Line
TTL		(Cont'd.)	
	9012M	† Fairchild	
	ZN5401	† Ferranti	
	ZN7401	Ferranti	
	HD7401	Hitachi	
	HD7403	Hitachi	
	M53201	Mitsubishi	
	M53203	Mitsubishi	
	MC5401	† Motorola	
	MC7401	Motorola	10
	MC5403	† Motorola	
	MC7403	Motorola	
	DM5401	† National	
	DM7401	National	
	DM5403	† National	
	DM7403	National	
	DM9012C	National	
	5401	† Signetics	
	7401	Signetics	
	5403	† Signetics	20
	7403	Signetics	
	SN5401	† TI	
	SN7401	TI	
	SN5403	† TI	
	SN7403	TI	
	TD3401	Toshiba	
	TD3403	Toshiba	
TTL-LS	9LS03C	Fairchild	
	9LS03M	† Fairchild	
	54LS03	† Fairchild	30
	74LS03	Fairchild	
	HD74LS01	Hitachi	
	HD74LS03	Hitachi	
	SN54LS01	† Motorola	
	SN74LS01	Motorola	
	SN54LS03	† Motorola	
	SN74LS03	Motorola	
	DM54LS01	† National	
	DM74LS01	National	
	DM54LS03	† National	40
	DM74LS03	National	
	μPB74LS03	NEC America	
	9LS01C	Raytheon	
	9LS01M	† Raytheon	
	54LS01	† Raytheon	
	74LS01	Raytheon	
	9LS03C	Raytheon	
	9LS03M	† Raytheon	
	54LS03	† Raytheon	
	74LS03	Raytheon	50
	54LS01	† Signetics	
	74LS01	Signetics	
	54LS03	† Signetics	
	74LS03	Signetics	
	SN54LS01	† TI	
	SN74LS01	TI	
	SN54LS03	† TI	
	SN74LS03	TI	
TTL-H	54H01	† Fairchild	
	74H01	Fairchild	60
	MC3004	Motorola	
	MC3104	† Motorola	
	DM54H01	† National	
	DM74H01	National	
	μPB74H01	NEC America	
	54H01	† Signetics	
	74H01	Signetics	
	SN54H01	† TI	
	SN74H01	TI	

(Continued)

Gates, AND/NAND (Cont'd.)

Function	Device	Source	Line
Quad 2-Input NAND Gate, Open Collector (Cont'd.)			70
TTL-S	54S03	† Fairchild	
	74S03	Fairchild	
	ZN54S03	† Ferranti	
	ZN74S03	Ferranti	
	HD74S03	Hitachi	
	M5S003	Mitsubishi	
	DM74S03	National	
	54S03	† Signetics	
	74S03	Signetics	
	SN54S03	† TI	80
	SN74S03	TI	
Quad 2-Input NAND Buffer, Open Collector			
TTL	5438	† Fairchild	
	7438	Fairchild	
	7439	Fairchild	
	ZN5438	† Ferranti	
	ZN7438	Ferranti	
	HD7438	Hitachi	
	M53238	Mitsubishi	
	MC5438	† Motorola	90
	MC7438	Motorola	
	DM5438	† National	
	DM7438	National	
	μPB7438	NEC America	
	5438	† Signetics	
	7438	Signetics	
	5439	† Signetics	
	7439	Signetics	
	SN5438	† TI	
	SN7438	TI	100
	TD3438	Toshiba	
TTL-LS	9LS38C	Fairchild	
	9LS38M	† Fairchild	
	54LS38	† Fairchild	
	74LS38	Fairchild	
	HD74LS38	Hitachi	
	SN54LS38	† Motorola	
	SN74LS38	Motorola	
	9LS38C	Raytheon	
	9LS38M	† Raytheon	110
	54LS38	† Raytheon	
	74LS38	Raytheon	
	DM54LS38	† National	
	DM74LS38	National	
	μPB74LS38	NEC America	
	74LS38	Signetics	
	54LS38	† Signetics	
	SN54LS38	† TI	
	SN74LS38	TI	
TTL-S	74S38	Signetics	120
	SN54S38	† TI	
	SN74S38	TI	
Quad 2-Input NAND Buffer, Open Collector, to 15v			
TTL-LS	9LS26C	Fairchild	
	9LS26M	† Fairchild	
	54LS26	† Fairchild	
	74LS26	Fairchild	
	HD74LS26	Hitachi	
	SN54LS26	† Motorola	
	SN74LS26	Motorola	130
	DM54LS26	† National	
	DM74LS26	National	
	9LS26C	Raytheon	
	9LS26M	† Raytheon	
	54LS26	† Raytheon	
	74LS26	Raytheon	
	54LS26	† Signetics	

(Continued)

Gates, AND/NAND (Cont'd.)

Function	Device	Source	Line
TTL-LS		(Cont'd.)	
	74LS26	Signetics	
	SN54LS26	† TI	140
	SN74LS26	TI	
Quad 2-Input NAND Buffer, Three-State			
TTL	DM7099	† National	
	DM8099	National	

Gates, AND-OR/AND-OR-Invert

Dual 2-4 Input AND/OR Gate			
TTL-S	9S42C	Fairchild	
	9S42M	Fairchild	
2-2-2-3-Input AND-OR Gate, Expandable			
TTL-H	54H52	† Fairchild	
	74H52	Fairchild	150
	MC3031	Motorola	
	MC3131	† Motorola	
	DM54H52	† National	
	DM74H52	National	
	54H52	† Signetics	
	74H52	Signetics	
	SN54H52	† TI	
	SN74H52	TI	
2-2-2-3-Input AND-OR-Invert Gate, Expandable			
TTL	9008C	Fairchild	160
	9008M	† Fairchild	
	DM9008C	National	
4-Wide 2-Input AND-OR-Invert Gate			
TTL	5454	† Fairchild	
	7454	Fairchild	
	ZN5454	† Ferranti	
	ZN7454	Ferranti	
	HD7454	Hitachi	
	MC5454	† Motorola	
	MC7454	Motorola	170
	DM5454	† National	
	DM7454	National	
	μPB7454	NEC America	
	5454	† Signetics	
	7454	Signetics	
	SN5454	† TI	
	SN7454	TI	
4-Wide 2-2-3-3-Input AND-OR-Invert Gate			
TTL-LS	9LS54C	Fairchild	
	9LS54M	† Fairchild	180
	54LS54	† Fairchild	
	74LS54	Fairchild	
	HD74LS54	Hitachi	
	SN54LS54	† Motorola	
	SN74LS54	Motorola	
	DM54LS54	† National	
	DM74LS54	National	
	μPB74LS54	NEC America	
	9LS54C	Raytheon	
	9LS54M	† Raytheon	190
	54LS54	† Raytheon	
	74LS54	Raytheon	
	54LS54	† Signetics	
	74LS54	Signetics	
	SN54LS54	† TI	
	SN74LS54	TI	
2-2-2-3-Input AND-OR-Invert Gate			
TTL-H	54H54	† Fairchild	
	74H54	Fairchild	
	DM54H54	† National	200
	DM74H54	National	

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Values

Bold face indicates additional data is provided on the page noted.

DIGITAL–TTL (Cont'd)

Gates, AND-OR/AND-OR-Invert (Cont'd.)

Function	Device	Source	Line
TTL-H		(Cont'd.)	
	54H54	† Signetics	
	74H54	Signetics	
	SN54H54	† TI	
	SN74H54	TI	
4-Wide 2-Input AND-OR-Invert Gate, Expandable			
TTL	5453	† Fairchild	
	7453	Fairchild	
	ZN5453	† Ferranti	
	ZN7453	Ferranti	10
	HD7453	Hitachi	
	M53253	Mitsubishi	
	MC5453	† Motorola	
	MC7453	Motorola	
	DM5453	† National	
	DM7453	National	
	μPB7453	NEC America	
	5453	† Signetics	
	7453	Signetics	
	SN5453	† TI	20
	SN7453	TI	
2-2-2-3-Input AND-OR-Invert Gate, Expandable			
TTL-H	54H53	† Fairchild	
	74H53	Fairchild	
	MC3032	Motorola	
	MC3132	† Motorola	
	DM54H53	† National	
	DM74H53	National	
	54H53	† Signetics	
	74H53	Signetics	30
	SN54H53	† TI	
	SN74H53	TI	
4-2-3-2-Input AND-OR-Invert Gate			
TTL-S	54S64	† Fairchild	
	74S64	† Fairchild	
	HD74S64	Hitachi	
	DM74S64	National	
	54S64	† Signetics	
	74S64	† Signetics	
	SN54S64	TI	40
	SN74S64	TI	
4-2-3-2-Input AND-OR-Invert Gate, Open Collector			
TTL-S	54S65	† Fairchild	
	74S65	† Fairchild	
	HD74S65	Hitachi	
	DM74S65	National	
	54S65	† Signetics	
	74S65	Signetics	
	SN54S65	† TI	
	SN74S65	TI	50
Dual 2-Wide 2-Input AND-OR-Invert Gate			
TTL	5451	† Fairchild	
	7451	Fairchild	
	ZN7451	Ferranti	
	ZN5451	† Ferranti	
	HD7451	Hitachi	
	MC5451	† Motorola	
	MC7451	Motorola	
	DM5451	† National	
	DM7451	National	60
	μPB7451	NEC America	
	5451	† Signetics	
	7451	Signetics	
	SN5451	† TI	
	SN7451	TI	
	TD3451	Toshiba	
TTL-H	54H51	† Fairchild	

(Continued)

Gates, AND-OR/AND-OR-Invert (Cont'd.)

Function	Device	Source	Line
TTL-H		(Cont'd.)	
	74H51	Fairchild	
	MC3023	Motorola	70
	MC3123	† Motorola	
	DM54H51	† National	
	DM74H51	National	
	μPB74H51	NEC America	
	54H51	† Signetics	
	74H51	Signetics	
	SN54H51	† TI	
	SN74H51	TI	
TTL-S	54S51	† Fairchild	
	74S51	Fairchild	80
	HD74S51	Hitachi	
	M5S051	Mitsubishi	
	DM74S51	National	
	54S51	† Signetics	
	74S51	Signetics	
	SN54S51	† TI	
	SN74S51	TI	
TTL-LS	9LS51C	Fairchild	
	9LS51M	† Fairchild	
	54LS51	† Fairchild	90
	74LS51	Fairchild	
	HD74LS51	Hitachi	
	SN54LS51	† Motorola	
	SN74LS51	Motorola	
	DM54LS51	† National	
	DM74LS51	National	
	μPB74LS51	NEC America	
	9LS51C	Raytheon	
	9LS51M	† Raytheon	
	54LS51	† Raytheon	100
	74LS51	Raytheon	
	54LS51	† Signetics	
	74LS51	Signetics	
	SN54LS51	† TI	
	SN74LS51	TI	
2-Wide, 4-Input AND-OR-Invert Gate			
TTL-LS	9LS55C	Fairchild	
	9LS55M	† Fairchild	
	54LS55	† Fairchild	
	74LS55	Fairchild	110
	HD74LS55	Hitachi	
	SN54LS55	† Motorola	
	SN74LS55	Motorola	
	DM54LS55	† National	
	DM74LS55	National	
	μPB74LS55	NEC America	
	9LS55C	Raytheon	
	9LS55M	† Raytheon	
	54LS55	† Raytheon	
	74LS55	Raytheon	120
	54LS55	† Signetics	
	74LS55	Signetics	
	SN54LS55	† TI	
	SN74LS55	TI	
2-Wide, 4-Input AND-OR-Invert Gate, Expandable			
TTL-H	54H55	† Fairchild	
	74H55	Fairchild	
	DM54H55	† National	
	DM74H55	National	
	54H55	† Signetics	130
	74H55	Signetics	
	SN54H55	† TI	
	SN74H55	TI	

Gates, AND-OR/AND-OR-Invert (Cont'd.)

Function	Device	Source	Line
Dual 2-Wide 2-Input AND-OR-Invert Gate (one gate is expandable)			
TTL	5450	† Fairchild	
	7450	Fairchild	
	9005C	Fairchild	
	9005M	† Fairchild	
	ZN5450	† Ferranti	140
	ZN7450	Ferranti	
	HD7450	Hitachi	
	M5352	Mitsubishi	
	M53250	Mitsubishi	
	MC5450	† Motorola	
	MC7450	Motorola	
	DM5450	† National	
	DM7450	National	
	DM9005C	National	
	μPB7450	NEC America	150
	5450	† Signetics	
	7450	Signetics	
	SN5450	† TI	
	SN7450	TI	
	TD3450	Toshiba	
TTL-H	54H50	† Fairchild	
	74H50	Fairchild	
	MC3020	Motorola	
	MC3120	† Motorola	
	DM54H50	† National	160
	DM74H50	National	
	54H50	† Signetics	
	74H50	Signetics	
	SN54H50	† TI	
	SN74H50	TI	
Dual 4-Input Expander (for 54/7423, 54/7450, 54/7453)			
TTL	5460	† Fairchild	
	7460	Fairchild	
	ZN5460	† Ferranti	170
	ZN7460	Ferranti	
	HD7460	Hitachi	
	M5304	Mitsubishi	
	M53260	Mitsubishi	
	MC5460	† Motorola	
	MC7460	Motorola	
	DM5460	† National	
	DM7460	National	
	μPB7460	NEC America	
	5460	† Signetics	180
	7460	Signetics	
	SN5460	† TI	
	SN7460	TI	
	TD3460	Toshiba	
Dual 4-Input Extender (for 9005, 9008)			
TTL	9006C	Fairchild	
	9006M	† Fairchild	
	DM9006C	National	

Gates, Exclusive OR/NOR

Function	Device	Source	Line
Quad 2-Input Exclusive-OR Gate			
TTL	5486	† Fairchild	190
	7486	Fairchild	
	ZN5486	† Ferranti	
	ZN7486	Ferranti	
	HD7486	Hitachi	
	DM74LS386	National	
	M53286	Mitsubishi	
	MC5486	† Motorola	
	MC7486	Motorola	
	MC7241	Motorola	

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Values

DIGITAL–TTL (Cont'd)

Gates, Exclusive OR/NOR (Cont'd.)

Function	Device	Source	Line
TTL		(Cont'd.)	
	MC8241	† Motorola	
	DM5486	National	
	DM7486	National	
	μPB7486	NEC America	
	RC8241	Raytheon	
	RM8241	† Raytheon	
	5486	† Signetics	
	7486	Signetics	
	N8241	Signetics	10
	S8241	† Signetics	
	SN5486	† TI	
	SN7486	TI	
	TD3486	Toshiba	
TTL-LS	9LS86C	Fairchild	
	9LS86M	† Fairchild	
	54LS86	† Fairchild	
	74LS86	Fairchild	
	HD74LS86	Hitachi	
	HD74LS386	Hitachi	20
	SN54LS86	† Motorola	
	SN74LS86	Motorola	
	SN54LS386	† Motorola	
	SN74LS386	Motorola	
	DM54LS86	† National	
	DM74LS86	National	
	DM54LS386	† National	
	DM74LS386	National	
	μPB74LS86	NEC America	
	9LS86C	Raytheon	30
	9LS86M	† Raytheon	
	54LS86	† Raytheon	
	74LS86	Raytheon	
	9LS386C	Raytheon	
	9LS386M	† Raytheon	
	54LS386	† Raytheon	
	74LS386	Raytheon	
	54LS86	† Signetics	
	74LS86	Signetics	
	54LS386	† Signetics	40
	74LS386	Signetics	
	SN54LS86	† TI	
	SN74LS86	TI	
	SN54LS386	† TI	
	SN74LS386	TI	
TTL-H	MC3021	Motorola	
	MC3121	† Motorola	
TTL-S	54S86	† Fairchild	
	74S86	Fairchild	
	HD74S86	Hitachi	50
	DM74S86	National	
	N82S41	Signetics	
	54S86	† Signetics	
	74S86	Signetics	
	SN54S86	† TI	
	SN74S86	TI	
Quad 2-Input Exclusive OR Gate (two of the outputs are complemented)			
TTL	9014C	Fairchild	
	9014M	† Fairchild	60
Quad 2-Input Exclusive-OR Gate, Open Collector			
TTL	HD74136	Hitachi	
	MC54136	† Motorola	
	MC74136	Motorola	
	SN54136	† TI	
	SN74136	TI	
TTL-LS	9LS136C	Fairchild	

(Continued)

Gates, Exclusive OR/NOR (Cont'd.)

Function	Device	Source	Line
TTL-LS		(Cont'd.)	
	9LS136M	† Fairchild	
	54LS136	Fairchild	70
	74LS136	Fairchild	
	HD74LS136	Hitachi	
	SN54LS136	† Motorola	
	SN74LS136	Motorola	
	DM54LS136	† National	
	DM74LS136	National	
	9LS136C	Raytheon	
	9LS136M	† Raytheon	
	54LS136	† Raytheon	
	74LS136	Raytheon	80
	54LS136	† Signetics	
	74LS136	Signetics	
	SN54LS136	† TI	
	SN74LS136	TI	
TTL-S	DM74S136	National	
Quad 2-Input Exclusive NOR Gate			
TTL-H	MC3022	Motorola	
	MC3122	† Motorola	
Quad 2-Input Exclusive NOR Gate, Open Collector			
TTL	9386C	Fairchild	90
	9386M	† Fairchild	
	MC7242	Motorola	
	MC8242	† Motorola	
	RC8242	Raytheon	
	RM8242	† Raytheon	
	N8242	Signetics	
	S8242	† Signetics	
TTL-LS	9LS266C	Fairchild	
	9LS266M	† Fairchild	
	54LS266	† Fairchild	100
	74LS266	Fairchild	
	SN54LS266	† Motorola	
	SN74LS266	Motorola	
	DM54LS266	† National	
	DM74LS266	National	
	9LS266C	Raytheon	
	9LS266M	† Raytheon	
	54LS266	† Raytheon	
	74LS266	Raytheon	
	54LS266	† Signetics	110
	74LS266	Signetics	
	SN54LS266	† TI	
	SN74LS266	TI	
TTL-S	N82S42	Signetics	
Quad 2-Input OR/NOR Gate			
TTL-S	54S135	† Fairchild	
	74S135	Fairchild	
	HD74S135	Hitachi	
	DM74S135	National	
	74S135	Signetics	120
	SN54S135	† TI	
	SN74S135	TI	

Gates, OR/NOR

Function	Device	Source	Line
Quad 2-Input OR Gate			
TTL	5432	† Fairchild	
	7432	Fairchild	
	ZN5432	† Ferranti	
	ZN7432	Ferranti	
	HD7432	Hitachi	
	DM5432	† National	
	DM7432	National	130
	5432	† Signetics	

(Continued)

Gates, OR/NOR (Cont'd.)

Function	Device	Source	Line
TTL		(Cont'd.)	
	7432	Signetics	
	SN5432	† TI	
	SN7432	TI	
TTL-LS	9LS32C	Fairchild	
	9LS32M	† Fairchild	
	54LS32	† Fairchild	
	74LS32	Fairchild	
	HD74LS32	Hitachi	140
	SN54LS32	† Motorola	
	SN74LS32	Motorola	
	DM54LS32	† National	
	DM74LS32	National	
	μPB74LS32	NEC America	
	9LS32C	Raytheon	
	9LS32M	† Raytheon	
	54LS32	† Raytheon	
	74LS32	Raytheon	
	54LS32	† Signetics	150
	74LS32	Signetics	
	SN54LS32	† TI	
	SN74LS32	TI	
TTL-S	54S32	† Fairchild	
	74S32	Fairchild	
	54S32	† Signetics	
	74S32	Signetics	
	SN54S32	† TI	
	SN74S32	TI	
2-2-2-4 Input NOR Gate			160
TTL	9015C	Fairchild	
	9015M	† Fairchild	
Dual 4-Input NOR Gate, with Strobe			
TTL	5425	† Fairchild	
	7425	Fairchild	
	ZN5425	† Ferranti	
	HD7425	Hitachi	
	ZN7425	Ferranti	
	M53225	Mitsubishi	
	MC5425	† Motorola	170
	MC7425	Motorola	
	DM5425	† National	
	DM7425	National	
	7425	Signetics	
	SN5425	† TI	
	SN7425	TI	
Dual 4-Input NOR Gate, with Strobe, Expandable (see 54/7460 Expander)			
TTL	5423	† Fairchild	
	7423	Fairchild	180
	HD7423	Hitachi	
	MC5423	† Motorola	
	MC7423	Motorola	
	DM5423	† National	
	DM7423	National	
	7423	Signetics	
	SN5423	† TI	
	SN7423	TI	
Dual 5-Input NOR Gate			
TTL-LS	9LS260C	Fairchild	190
	9LS260M	† Fairchild	
	54LS260	† Fairchild	
	74LS260	Fairchild	
	SN54LS260	† Motorola	
	SN74LS260	Motorola	
	54LS260A	† Signetics	
	74LS260A	Signetics	

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† Military Temperature Range (−55° to 125°C)

* Typical Values

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DIGITAL–TTL (Cont'd)

Gates, OR/NOR (Cont'd.)

Function	Device	Source	Line
Dual 5-Input NOR Gate (Cont'd.)			
TTL-S	DM74S260	National	
	54S260	† Signetics	
	74S260	Signetics	
	SN54S260	† TI	
	SN74S260	TI	
Triple 3-Input NOR Gate			
TTL	5427	† Fairchild	
	7427	Fairchild	
	ZN5427	† Ferranti	10
	ZN7427	Ferranti	
	HD7427	Hitachi	
	M53227	Mitsubishi	
	MC5427	† Motorola	
	MC7427	Motorola	
	DM5427	† National	
	DM7427	National	
	5427	† Signetics	
	7427	Signetics	
	SN5427	† TI	20
	SN7427	TI	
TTL-LS	9LS27C	Fairchild	
	9LS27M	† Fairchild	
	54LS27	† Fairchild	
	74LS27	Fairchild	
	HD74LS27	Hitachi	
	SN54LS27	† Motorola	
	SN74LS27	Motorola	
	DM54LS27	† National	
	DM74LS27	National	30
	μPB74LS27	NEC America	
	9LS27C	Raytheon	
	9LS27M	† Raytheon	
	54LS27	† Raytheon	
	74LS27	Raytheon	
	54LS27	† Signetics	
	74LS27	Signetics	
	SN54LS27	† TI	
	SN74LS27	TI	
Quad 2-Input NOR Gate (54/7428 devices are also buffers)			40
TTL	5402	† Fairchild	
	7402	Fairchild	
	ZN5428	† Ferranti	
	ZN7428	Ferranti	
	HD7402	Hitachi	
	M53202	Mitsubishi	
	MC5402	† Motorola	
	MC7402	Motorola	
	DM5402	† National	50
	DM7402	National	
	μPB7402	NEC America	
	5402	† Signetics	
	7402	Signetics	
	5428	† Signetics	
	7428	Signetics	
	SN5402	† TI	
	SN7402	TI	
	SN5428	† TI	
	SN7428	TI	60
	TD3402	Toshiba	
TTL-LS	9LS02C	Fairchild	
	9LS02M	† Fairchild	
	54LS02	† Fairchild	
	74LS02	Fairchild	
	9LS28C	Fairchild	
	74LS28	Fairchild	
	HD74LS02	Hitachi	

(Continued)

Gates, OR/NOR (Cont'd.)

Function	Device	Source	Line
TTL-LS		(Cont'd.)	70
	SN54LS02	† Motorola	
	SN74LS02	Motorola	
	SN54LS28	† Motorola	
	SN74LS28	Motorola	
	DM54LS02	† National	
	DM74LS02	National	
	μPB74LS02	NEC America	
	9LS02C	Raytheon	
	9LS02M	† Raytheon	
	54LS02	† Raytheon	80
	74LS02	Raytheon	
	9LS28C	Raytheon	
	9LS28M	† Raytheon	
	54LS28	† Raytheon	
	74LS28	Raytheon	
	54LS02	† Signetics	
	74LS02	Signetics	
	54LS28	† Signetics	
	74LS28	Signetics	
	SN54LS02	† TI	90
	SN74LS02	TI	
	SN54LS28	† TI	
	SN74LS28	TI	
TTL-S	54S02	† Fairchild	
	74S02	Fairchild	
	HD74S02	Hitachi	
	DM74S02	National	
	54S02	† Signetics	
	74S02	Signetics	
	SN54S02	† TI	100
	SN74S02	TI	
Quad 2-Input NOR Buffer, Open Collector			
TTL	5433	† Signetics	
	7433	Signetics	
	SN5433	† TI	
	SN7433	TI	
TTL-LS	9LS33C	Fairchild	
	54LS33	† Fairchild	
	74LS33	Fairchild	
	SN54LS33	† Motorola	110
	SN74LS33	Motorola	
	9LS33C	Raytheon	
	9LS33M	† Raytheon	
	54LS33	† Raytheon	
	74LS33	Raytheon	
	54LS33	† Signetics	
	74LS33	Signetics	
	SN54LS33	† TI	
	SN74LS33	TI	
Quad 2-Input OR Gate			120
TTL-H	MC3003	Motorola	
	MC3103	† Motorola	
Quad 2-Input NOR Gate			
TTL-H	MC3002	Motorola	
	MC3102	† Motorola	

Gates, Miscellaneous

Function	Device	Source	Line
Quad Inverter and Dual 2-Input NAND Gate			
TTL	DM7090	† National	
	DM8090	National	
Dual Majority Logic Gate			
TTL	MC4062	Motorola	130

Latches

Function	Device	Source	Line
8-bit Addressable Latch, with Clear			
TTL	9334C	AMD	
	9334M	† AMD	
	SN54259	† AMD	
	SN74259	AMD	
	9334C	Fairchild	
	9334M	† Fairchild	
	DM8334	National	
	DM9334	† National	
	N9334	Signetics	140
	S9334	† Signetics	
	SN54259	† TI	
	SN74259	TI	
TTL-LS	9LS259C	Fairchild	
	9LS259M	† Fairchild	
	54LS259	† Fairchild	
	74LS259	Fairchild	
	SN54LS259	† Motorola	
	SN74LS259	Motorola	
	SN54LS259	† TI	150
	SN74LS259	TI	
Dual 4-bit Addressable Latch			
TTL-LS	54LS256	† Fairchild	
	74LS256	Fairchild	
	SN54LS256	† Motorola	
	SN74LS256	Motorola	
8-bit Latch, Three-State (input and output through the same pins)			
TTL	DM7553	† National	
	DM8553	National	160
8-bit Latch, Transparent, D Type, Three-State			
TTL-LS	AM25LS373C	AMD	
	AM25LS373M	† AMD	
	SN54LS373	† AMD	
	SN74LS373	AMD	
	54LS373	† Fairchild	
	74LS373	Fairchild	
	54LS373	**† MMI (505)**	
	74LS373	**MMI (505)**	
	SN54LS373	† Motorola	170
	SN74LS373	Motorola	
	SN54LS573	† Motorola	
	SN74LS573	Motorola	
	9LS373C	**Raytheon (543)**	
	9LS373M	**† Raytheon (543)**	
	25LS373C	**Raytheon (543)**	
	25LS373M	**† Raytheon (543)**	
	54LS373	**† Raytheon (543)**	
	74LS373	**Raytheon (543)**	
	74LS363	Signetics	180
	74LS373	Signetics	
	SN54LS363	† TI	
	SN74LS363	TI	
	SN54LS373	† TI	
	SN74LS373	TI	
TTL-S	SN54S373	† AMD	
	SN74S373	AMD	
	54S373	**† MMI (505)**	
	74S373	**MMI (505)**	
	57S373	**† MMI (505)**	190
	67S373	**MMI (505)**	
	SN54S373	† TI	
	SN74S373	TI	
	SN54S412	† TI	
	SN74S412	TI	
8-bit Latch, Transparent, D-Type, Inverting Three-State			
TTL-LS	SN54LS533	† AMD	
	SN74LS533	AMD	

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Values

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DIGITAL–TTL (Cont'd)

Latches (Cont'd.)

Function	Device	Source	Line
TTL-LS			(Cont'd.)
	57LS380	**† MMI**	**(505)**
	67LS380	**MMI**	**(505)**
TTL-S	SN54S533	† AMD	
	SN74S533	AMD	
	57S380	**† MMI**	**(505)**
	67S380	**MMI**	**(505)**
	57S382	**† MMI**	**(505)**
	67S382	**MMI**	**(505)**
6-bit Latch (Independent 2 and 4-bit)			
TTL-S	3404	Intel	10
Dual 4-bit Latch			
TTL	MC54100	† Motorola	
	MC74100	Motorola	
	54100	† Signetics	
	74100	Signetics	
	SN54100	† TI	
	SN74100	TI	
Dual 4-bit Latch with Clear			
TTL	9308C	AMD	20
	9308M	† AMD	
	9308C	Fairchild	
	9308M	† Fairchild	
	54116	† Fairchild	
	74116	Fairchild	
	MC8308	Motorola	
	MC9308	† Motorola	
	µPB9308	NEC America	
	RM9308	† Raytheon	
	RC9308	Raytheon	30
	54116	† Signetics	
	74116	Signetics	
	N9308	Signetics	
	S9308	† Signetics	
	SN29308	TI	
	SN39308	† TI	
	SN54116	† TI	
	SN74116	TI	
Quad Multifunction Latch			
TTL	9314C	AMD	40
	9314M	† AMD	
	9314C	Fairchild	
	9314M	† Fairchild	
	MC8314	Motorola	
	MC9314	† Motorola	
	N9314	Signetics	
	S9314	† Signetics	
Quad Bistable Latch, Single Output			
TTL	5477	† Fairchild	
	7477	Fairchild	50
	MC5477	† Motorola	
	MC7477	Motorola	
	5477	† Signetics	
	7477	Signetics	
	SN5477	† TI	
TTL-LS	54LS77	† Fairchild	
	74LS77	Fairchild	
	SN54LS377	† Motorola	
	SN74LS377	Motorola	
	DM74LS77	National	60
	9LS77C	Raytheon	
	9LS77M	† Raytheon	
	54LS77	† Raytheon	
	74LS77	Raytheon	
	SN54LS77	† TI	
	SN74LS77	TI	

Latches (Cont'd.)

Function	Device	Source	Line
Quad Bistable Latch, Complementary Outputs			
TTL	5474	† Fairchild	
	7474	Fairchild	
	5475	† Fairchild	70
	7475	Fairchild	
	ZN5474	† Ferranti	
	ZN7475	Ferranti	
	HD7475	Hitachi	
	M53275	Mitsubishi	
	MC5475	† Motorola	
	MC7475	Motorola	
	DM5475	† National	
	DM7475	National	
	5474	† Signetics	80
	7474	Signetics	
	5475	† Signetics	
	7475	Signetics	
	SN5474	† TI	
	SN7475	TI	
	TD3475	Toshiba	
TTL-LS	54LS75	† Fairchild	
	74LS75	Fairchild	
	54LS375	† Fairchild	
	74LS375	Fairchild	90
	SN54LS75	† Motorola	
	SN74LS75	Motorola	
	SN54LS375	† Motorola	
	SN74LS375	Motorola	
	DM54LS75	† National	
	DM74LS75	National	
	µPB74LS375	NEC America	
	9LS75C	Raytheon	
	9LS75M	† Raytheon	
	54LS75	† Raytheon	100
	74LS75	Raytheon	
	54LS75	† Signetics	
	74LS75	Signetics	
	54LS375	† Signetics	
	74LS375	Signetics	
	SN54LS75	† TI	
	SN74LS75	TI	
	SN54LS375	† TI	
	SN74LS375	TI	
Quad Set-Reset Latch			110
TTL	54279	† Fairchild	
	74279	Fairchild	
	HD74279	Hitachi	
	54279	† Signetics	
	74279	Signetics	
	SN54279	† TI	
	SN74279	TI	
TTL-LS	9LS279C	Fairchild	
	9LS279M	† Fairchild	
	54LS279	† Fairchild	120
	74LS279	Fairchild	
	SN54LS279	† Motorola	
	SN74LS279	Motorola	
	DM54LS279	† National	
	DM74LS279	National	
	µPB74LS279	NEC America	
	9LS279C	Raytheon	
	9LS279M	† Raytheon	
	54LS279	† Raytheon	
	74LS279	Raytheon	130
	54LS279	† Signetics	
	74LS279	Signetics	
	SN54LS279	† TI	
	SN74LS279	TI	

Latches (Cont'd.)

Function	Device	Source	Line
Hex Set-Reset Latch (Common Reset)			
TTL	ZN54118	† Ferranti	
	ZN74118	Ferranti	
	ZN54119	† Ferranti	
	ZN74119	Ferranti	

Memories

For additional information on these and larger TTL compatible memories, see the Master Selection Guide-Memory section — 140

8-bit Multiport Register (RAM with simultaneous Read/Write)			
TTL	9338C	AMD	
	9338M	† AMD	
	9338C	Fairchild	
	9338M	† Fairchild	
Octal Storage Register (two stage, 4-bit wide shift register)			150
TTL-LS	SN54LS396	† TI	
	SN74LS396	TI	
Dual Rank 8-bit Shift Register (8-Bit I/O Buffer, "D" Register, and Serial "B" Register)			
TTL-LS	DM76LS52	† National	
	DM86LS52	National	
	DM76LS62	† National	
	DM86LS62	National	
16-bit Active Element Memory			
TTL	93407C	Fairchild	160
	93407M	† Fairchild	
	MC4004	Motorola	
	MC4005	Motorola	
	MC4304	† Motorola	
	MC4305	† Motorola	
	SN5481A	† TI	
	SN7481A	TI	
16-bit Active Element Memory, Gated Write			
TTL	M53284	Mitsubishi	
	µPB7484	NEC America	170
	SN5484A	† TI	
	SN7484A	TI	
16-bit (4x4) Register File, Simultaneous Read/Write, Open Collector			
TTL	54170	† Fairchild	
	74170	Fairchild	
	ZN54170	† Ferranti	
	ZN74170	Ferranti	
	M53370	Mitsubishi	
	DM74170	National	180
	µPB74170	NEC America	
	54170	† Signetics	
	74170	Signetics	
	SN54170	† TI	
	SN74170	TI	
TTL-LS	9LS170C	Fairchild	
	9LS170M	† Fairchild	
	54LS170	† Fairchild	
	74LS170	Fairchild	
	SN54LS170	† Motorola	190
	SN74LS170	Motorola	
	DM54LS170	† National	
	DM74LS170	National	
	9LS170C	Raytheon	
	9LS170M	† Raytheon	
	54LS170	† Raytheon	
	74LS170	Raytheon	
	25LS170C	Raytheon	

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Values

Bold face indicates additional data is provided on the page noted.

DIGITAL–TTL (Cont'd)

Memories (Cont'd.)

Function	Device	Source	Line
TTL-LS		(Cont'd.)	
	25LS170M	† Raytheon	
	54LS170	† Signetics	
	74LS170	Signetics	
	SN54LS170	† TI	
	SN74LS170	TI	
16-bit (4x4) Register File, Simultaneous Read/Write, Three-State			
TTL-LS	9LS670C	Fairchild	10
	9LS670M	† Fairchild	
	54LS670	† Fairchild	
	74LS670	Fairchild	
	SN54LS670	† Motorola	
	SN74LS670	Motorola	
	DM54LS670	† National	
	DM74LS670	National	
	9LS670C	Raytheon	
	9LS670M	† Raytheon	
	25LS670C	Raytheon	20
	25LS670M	† Raytheon	
	54LS670	† Raytheon	
	74LS670	Raytheon	
	54LS670	† Signetics	
	74LS670	Signetics	
	SN54LS670	† TI	
	SN74LS670	TI	
16-bit (8x2) Multiport Register File, Simultaneous Read/Write, Three-State			
TTL	SN74172	TI	30
TTL-S	74S172	Signetics	
32-bit (8x4) Multiport RAM			
TTL-S	**N82S12**	**Signetics (1678)**	
	N82S112	**Signetics (1678)**	
64-Bit (16x4) Register File with Latch, Three-State			
TTL-S	85S68	MMI	
	DM85S68	National	
64-Bit (32x2) Simultaneous Read/Write RAM			
TTL-S	**N82S21**	**Signetics (1678)**	
64-Bit (16x4) Simultaneous Read/Write RAM with output register			40
TTL	**9410C**	**Fairchild (1893)**	
	9410M	**† Fairchild (1893)**	
64-Bit (16x4) RAM with two output ports			
TTL	AM29704C	AMD	
	AM29704M	† AMD	
	AM29705C	AMD	
	AM29705M	† AMD	
80-bit (16x5) First-In/First-Out Memory, Asynchronous, Three-State			50
TTL-S	SN74S225	TI	

Multiplexers

Function	Device	Source	Line
Quad 2-Input Multiplexer, Non-Inverting			
TTL	9322C	AMD	
	9322M	† AMD	
	SN54157	† AMD	
	SN74157	AMD	
	9322C	Fairchild	
	9322M	† Fairchild	
	54157	† Fairchild	
	74157	Fairchild	60
	ZN54157	† Ferranti	
	ZN74157	Ferranti	
	HD74157	Hitachi	
	M53357	Mitsubishi	

(Continued)

Multiplexers (Cont'd.)

Function	Device	Source	Line
TTL		(Cont'd.)	
	MC8322	Motorola	
	MC9322	† Motorola	
	MC54157	† Motorola	
	MC74157	Motorola	
	DM8322	National	70
	DM9322	† National	
	DM54157	† National	
	DM74157	National	
	μPB74157	NEC America	
	RC8233	Raytheon	
	RM8233	† Raytheon	
	RC9322	Raytheon	
	RM9322	† Raytheon	
	N8233	Signetics	
	S8233	† Signetics	80
	N9322	Signetics	
	54157	† Signetics	
	74157	Signetics	
	SN54157	† TI	
	SN74157	TI	
TTL-LS	AM25LS157C	AMD	
	AM25LS157M	AMD	
	SN54LS157	† AMD	
	SN74LS157	AMD	
	9LS157C	Fairchild	90
	9LS157M	† Fairchild	
	54LS157	† Fairchild	
	74LS157	Fairchild	
	HD74LS157	Hitachi	
	SN54LS157	† Motorola	
	SN74LS157	Motorola	
	DM54LS157	† National	
	DM74LS157	National	
	μPB74LS157	NEC America	
	9LS157C	Raytheon	100
	9LS157M	† Raytheon	
	25LS157C	Raytheon	
	25LS157M	† Raytheon	
	54LS157	† Raytheon	
	74LS157	Raytheon	
	54LS157	Signetics	
	74LS157	Signetics	
	SN54LS157	† TI	
	SN74LS157	TI	
TTL-S	SN54S157	† AMD	110
	SN74S157	AMD	
	93S22C	AMD	
	93S22M	† AMD	
	54S157	† Fairchild	
	74S157	Fairchild	
	HD74S157	Hitachi	
	M5S157	Mitsubishi	
	DM74S157	National	
	54S157	† Signetics	
	74S157	Signetics	120
	SN54S157	† TI	
	SN74S157	TI	
Quad 2-Input Multiplexer, (Three-State 54/74157)			
TTL	DM7123	National	
	DM8123	† National	
Quad 2-Input Multiplexer with Storage			
TTL	54298	† Fairchild	
	74298	Fairchild	
	MC54298	† Motorola	
	MC74298	Motorola	130
	54298	† Signetics	
	74298	Signetics	

(Continued)

Multiplexers (Cont'd.)

Function	Device	Source	Line
TTL		(Cont'd.)	
	SN54298	† TI	
	SN74298	TI	
TTL-LS	SN54LS298	† AMD	
	SN74LS298	AMD	
	54LS298	† Fairchild	
	74LS298	Fairchild	
	SN54LS298	† Motorola	140
	SN74LS298	Motorola	
	SN74LS398	Motorola	
	SN74LS399	Motorola	
	9LS298C	Raytheon	
	9LS298M	† Raytheon	
	54LS298	† Raytheon	
	74LS298	Raytheon	
	SN54LS298	† TI	
	SN74LS298	TI	
Quad 2-Input Digital Multiplexer (Suitable for Driving Adders, Registers)			150
TTL	MC7266	Motorola	
	MC8266	† Motorola	
	RC8266	Raytheon	
	RM8266	† Raytheon	
	N8266	Signetics	
	S8266	† Signetics	
TTL-S	N82S66	Signetics	
Quad 2-Input Multiplexer, Open Collector (for adder, register input)			160
TTL	MC7267	Motorola	
	MC8267	† Motorola	
	RC8267	Raytheon	
	RM8267	† Raytheon	
	N8267	Signetics	
	S8267	† Signetics	
TTL-S	N82S67	Signetics	
Quad 2-Input Multiplexer, Inverting			
TTL	M53358	Mitsubishi	
	54158	† Signetics	170
	74158	Signetics	
TTL-LS	AM25LS158C	AMD	
	AM25LS158M	† AMD	
	SN54LS158	† AMD	
	SN74LS158	AMD	
	9LS158C	Fairchild	
	9LS158M	† Fairchild	
	54LS158	† Fairchild	
	74LS158	Fairchild	
	HD74LS158	Hitachi	180
	SN54LS158	† Motorola	
	SN74LS158	Motorola	
	DM54LS158	† National	
	DM74LS158	National	
	9LS158C	Raytheon	
	25LS158C	Raytheon	
	25LS158M	† Raytheon	
	9LS158M	† Raytheon	
	54LS158	† Raytheon	
	74LS158	Raytheon	190
	54LS158	† Signetics	
	74LS158	Signetics	
	SN54LS158	† TI	
	SN74LS158	TI	
TTL-S	SN54S158	† AMD	
	SN74S158	AMD	
	54S158	† Fairchild	
	74S158	Fairchild	

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Values

DIGITAL–TTL (Cont'd)

Multiplexers (Cont'd.)

Function	Device	Source	Line
TTL-S		(Cont'd.)	
	HD74S158	Hitachi	
	M5S158	Mitsubishi	
	DM74S158	National	
	54S158	† Signetics	
	74S158	Signetics	
	N82S66	Signetics	
	SN54S158	† TI	
	SN74S158	TI	
Quad 2-Input Multiplexer, Inverting Three-State			10
TTL-LS	AM25LS258C	AMD	
	AM25LS258M	† AMD	
	SN54LS258	† AMD	
	SN74LS258	AMD	
	9LS258C	Fairchild	
	9LS258M	† Fairchild	
	54LS258	† Fairchild	
	74LS258	Fairchild	
	HD74LS258	Hitachi	
	SN54LS258A	† Motorola	20
	SN74LS258A	Motorola	
	DM54LS258	† National	
	DM74LS258	National	
	μPB74LS258	NEC America	
	9LS258C	Raytheon	
	9LS258M	† Raytheon	
	25LS258C	Raytheon	
	25LS258M	† Raytheon	
	54LS258	† Raytheon	
	74LS258	Raytheon	30
	74LS258	Signetics	
	SN54LS258A	† TI	
	SN74LS258A	TI	
TTL-S	SN54S258	† AMD	
	SN74S258	AMD	
	54S258	† Fairchild	
	74S258	Fairchild	
	M5S258	Mitsubishi	
	DM74S258	National	
	54S258	† Signetics	40
	74S258	Signetics	
	SN54S258	† TI	
	SN74S258	TI	
Quad 2-Input Multiplexer, Non-Inverting, Three-State			
TTL-LS	AM25LS257C	AMD	
	AM25LS257M	† AMD	
	SN54LS257	† AMD	
	SN74LS257	AMD	
	9LS257C	Fairchild	
	9LS257M	† Fairchild	50
	54LS257	† Fairchild	
	74LS257	Fairchild	
	HD74LS257	Hitachi	
	SN54LS257A	† Motorola	
	SN74LS257A	Motorola	
	DM54LS257	† National	
	DM74LS257	National	
	μPB74LS57	NEC America	
	9LS257C	Raytheon	
	9LS257M	† Raytheon	60
	25LS257C	Raytheon	
	25LS257M	† Raytheon	
	54LS257	† Raytheon	
	74LS257	Raytheon	
	54LS257	† Signetics	
	74LS257	Signetics	
	SN54LS257A	† TI	
	SN74LS257A	TI	

(Continued)

Multiplexers (Cont'd.)

Function	Device	Source	Line
Quad 2-Input Multiplexer, Non-Inverting, Three-State (Cont'd.)			
TTL-S	SN54S257	† AMD	70
	SN74S257	AMD	
	54S257	† Fairchild	
	74S257	Fairchild	
	HD74S257	Hitachi	
	M5S257	Mitsubishi	
	DM74S257	National	
	74S257	Signetics	
	SN54S257	† TI	
	SN74S257	TI	
Quad 2-Input Multiplexer, Inverting, Open Collector			80
TTL	RC8234	Raytheon	
	RM8234	† Raytheon	
	N8234	Signetics	
	S8234	† Signetics	
Quad 2-Input Multiplexer, Conditional Complementing, Open Collector			
TTL	RC8235	Raytheon	
	RM8235	† Raytheon	
	N8235	Signetics	
	S8235	† Signetics	90
Quad 3-Input Multiplexer, Conditional Complementing			
TTL	RC8263	Raytheon	
	RM8263	† Raytheon	
	N8263	Signetics	
	S8263	† Signetics	
Quad 3-Input Multiplexer, Open Collector, Conditional Complementing, Output Enable			
TTL	RC8264	Raytheon	
	RM8264	† Raytheon	
	N8264	Signetics	100
	S8264	Signetics	
Quad 2-Input Multiplexer with Storage			
TTL-LS	AM25LS09C	AMD	
	AM25LS09M	† AMD	
	AM25LS399C	AMD	
	AM25LS399M	† AMD	
	SN54LS399	† AMD	
	SN74LS399	AMD	
	9LS298C	Fairchild	
	9LS298M	† Fairchild	110
	54LS298	† Fairchild	
	74LS298	Fairchild	
	HD74LS298	Hitachi	
	SN54LS298	† Motorola	
	SN74LS298	Motorola	
	SN54LS398	† Motorola	
	SN74LS398	Motorola	
	SN54LS399	† Motorola	
	SN74LS399	Motorola	
	9LS298C	Raytheon	120
	9LS298M	† Raytheon	
	54LS298	† Raytheon	
	74LS298	Raytheon	
	74LS298	Signetics	
	SN54LS298	† TI	
	SN74LS298	TI	
	SN54LS398	† TI	
	SN74LS398	TI	
	SN54LS399	† TI	
	SN74LS399	TI	130
TTL-S	AM25S09C	AMD	
	AM25S09M	† AMD	
Dual 4-Input Multiplexer			
TTL	54153	† Fairchild	

(Continued)

Multiplexers (Cont'd.)

Function	Device	Source	Line
TTL		(Cont'd.)	
	74153	Fairchild	
	ZN54153	† Ferranti	
	ZN74153	Ferranti	
	HD74123	Hitachi	
	M53353	Mitsubishi	140
	MC4000	Motorola	
	MC4300	† Motorola	
	MC54153	† Motorola	
	MC74153	Motorola	
	DM54153	† National	
	DM74153	National	
	μPB74153	NEC America	
	54153	† Signetics	
	74153	Signetics	
	SN54153	† TI	150
	SN74153	TI	
TTL-LS	AM25LS153C	AMD	
	AM25LS153M	† AMD	
	SN54LS153	† AMD	
	SN74LS153	AMD	
	9LS153C	Fairchild	
	9LS153M	† Fairchild	
	54LS153	† Fairchild	
	74LS153	Fairchild	
	HD74LS153	Hitachi	160
	SN54LS153	† Motorola	
	SN74LS153	Motorola	
	DM54LS153	† National	
	DM74LS153	National	
	μPB74LS153	NEC America	
	9LS153C	Raytheon	
	9LS153M	† Raytheon	
	25LS153C	Raytheon	
	25LS153M	† Raytheon	
	54LS153	† Raytheon	170
	74LS153	Raytheon	
	54LS153	† Signetics	
	74LS153	Signetics	
	SN54LS153	† TI	
	SN74LS153	TI	
TTL-S	SN54S153	† AMD	
	SN74S153	AMD	
	54S153	† Fairchild	
	74S153	Fairchild	
	HD74S153	Hitachi	180
	DM74S153	National	
	M5S153	Mitsubishi	
	54S153	† Signetics	
	74S153	Signetics	
	SN54S153	† TI	
	SN74S153	TI	
Dual 4-Input Multiplexer (Three-State 54/75153)			
TTL	DM7214	† National	
	DM8214	National	
Dual 4-Input Multiplexer, Three-State			190
TTL-LS	AM25LS253C	AMD	
	AM25LS253M	† AMD	
	SN54LS253	† AMD	
	SN74LS253	AMD	
	9LS253C	Fairchild	
	9LS253M	† Fairchild	
	54LS253	† Fairchild	
	74LS253	Fairchild	
	HD74LS253	Hitachi	
	SN54LS253	† Motorola	200
	SN74LS253	Motorola	
	DM54LS253	† National	

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† Military Temperature Range (−55° to 125°C)

* Typical Values

Bold face indicates additional data is provided on the page noted.

DIGITAL–TTL (Cont'd)

Multiplexers (Cont'd.)

Function	Device	Source	Line
TTL-LS		(Cont'd.)	
	DM74LS253	National	
	μPB74LS253	NEC America	
	9LS253C	Raytheon	
	9LS253M	† Raytheon	
	25LS253C	Raytheon	
	25LS253M	† Raytheon	
	54LS253	† Raytheon	
	74LS253	Raytheon	
	54LS253	† Signetics	10
	74LS253	Signetics	
	SN54LS253	† TI	
	SN74LS253	TI	
TTL-S	SN54S253	† AMD	
	SN74S253	AMD	
	54S253	† Fairchild	
	74S253	Fairchild	
	DM74S253	National	
	54S253	† Signetics	
	74S253	Signetics	20
Dual 4-Input Multiplexer, Inverting			
TTL-LS	54LS352	† Fairchild	
	74LS352	Fairchild	
	SN54LS352	† Motorola	
	SN74LS352	Motorola	
	DM54LS352	† National	
	DM74LS352	National	
	SN54LS352	† TI	
	SN74LS352	TI	
Dual 3-Input Multiplexer, Inverting, Three-State			30
TTL-LS	54LS353	† Fairchild	
	74LS353	Fairchild	
	SN54LS353	† Motorola	
	SN74LS353	Motorola	
	DM54LS353	† National	
	DM74LS353	National	
	SN54LS353	† TI	
	SN74LS353	TI	
Dual 4-Input Multiplexer, Complementary Output			
TTL	9309C	AMD	40
	9309M	† AMD	
	9309C	Fairchild	
	9309M	† Fairchild	
	MC8309	Motorola	
	MC9309	† Motorola	
	DM8309	National	
	DM9309	National	
	μPB9309	NEC America	
	N9309	Signetics	
	S9309	† Signetics	50
	SN29309	TI	
	SN39309	† TI	
8-Input Multiplexer, Inverted Output			
TTL	54152	† Fairchild	
	74152	Fairchild	
	MC54152	† Motorola	
	MC74152	Motorola	
	DM7210	† National	
	DM7211	† National	
	DM8210	National	60
	DM8211	National	
	54152	† Signetics	
	SN54152A	† TI	
TTL-LS	9LS152C	Fairchild	
	9LS152M	† Fairchild	
	54LS152	† Fairchild	
	74LS152	Fairchild	

(Continued)

Multiplexers (Cont'd.)

Function	Device	Source	Line
TTL-LS		(Cont'd.)	
	HD74LS152	Hitachi	
	SN54LS152	† Motorola	70
	SN74LS152	Motorola	
	9LS152C	Raytheon	
	9LS152M	† Raytheon	
	54LS152	† Raytheon	
	74LS152	Raytheon	
	SN54LS152	† TI	
8-Input Multiplexer, Complementary Output			
TTL	9312C	AMD	
	9312M	† AMD	
	9312C	Fairchild	80
	9312M	† Fairchild	
	MC8312	Motorola	
	MC9312	† Motorola	
	DM8312	National	
	DM9312	† National	
	μPB9312	NEC America	
	RC8230	Raytheon	
	RC8232	Raytheon	
	RC9312	Raytheon	
	RM8230	† Raytheon	90
	RM8232	† Raytheon	
	RM9312	† Raytheon	
	N8230	Signetics	
	S8230	† Signetics	
	N8232	Signetics	
	S8232	† Signetics	
	N9312	Signetics	
	SN29312	TI	
	SN39312	† TI	
TTL-S	N82S30	Signetics	100
	S82S30	† Signetics	
	N82S31	Signetics	
	S82S31	† Signetics	
	N82S32	Signetics	
	S82S32	† Signetics	
8-Input Multiplexer, Complementary Output, Strobe			
TTL	54151	† Fairchild	
	74151	Fairchild	
	ZN54151	† Ferranti	
	ZN74151	Ferranti	110
	HD74151A	Hitachi	
	M53351	Mitsubishi	
	MC54151	† Motorola	
	MC74151	Motorola	
	DM54151A	† National	
	DM74151A	National	
	μPB74151	NEC America	
	54151	† Signetics	
	74151	Signetics	
	SN54151A	† TI	120
	SN74151A	TI	
TTL-LS	AM25LS151C	AMD	
	AM25LS151M	† AMD	
	SN54LS151	† AMD	
	SN74LS151	AMD	
	9LS151C	Fairchild	
	9LS151M	† Fairchild	
	54LS151	† Fairchild	
	74LS151	Fairchild	
	HD74LS151A	Hitachi	130
	SN54LS151	† Motorola	
	SN74LS151	Motorola	
	DM54LS151	† National	
	DM74LS151	National	
	μPB74LS151	NEC America	

(Continued)

Multiplexers (Cont'd.)

Function	Device	Source	Line
TTL-LS		(Cont'd.)	
	9LS151C	Raytheon	
	9LS151M	Raytheon	
	25LS151C	Raytheon	
	25LS151M	† Raytheon	140
	54LS151	† Raytheon	
	74LS151	Raytheon	
	54LS151	† Signetics	
	74LS151	Signetics	
	SN54LS151	† TI	
	SN74LS151	TI	
TTL-S	SN54S151	† AMD	
	SN74S151	AMD	
	54S151	† Fairchild	
	74S151	Fairchild	150
	93S12C	Fairchild	
	93S12M	† Fairchild	
	HD74S151	Hitachi	
	M5S151	Mitsubishi	
	DM74S151	National	
	54S151	† Signetics	
	74S151	Signetics	
	SN54S151	† TI	
	SN74S151	TI	
8-Input Multiplexer, Complementary Output (Three-State 54/74151)			160
TTL	DM7121	† National	
	DM8121	National	
8-Input Multiplexer, Complementary Output, Open Collector			
TTL	9313C	Fairchild	
	9313M	† Fairchild	
	RC8231	Raytheon	
	RM8231	† Raytheon	
	N8231	Signetics	170
	S8231	† Signetics	
	N9313	Signetics	
8-Input Multiplexer, Strobe, Complementary Output, Three-State			
TTL	HD74251	Hitachi	
	DM54251	† National	
	DM74251	National	
	SN54251	† TI	
	SN74251	TI	
TTL-LS	AM25LS251C	AMD	180
	AM25LS251M	† AMD	
	SN54LS251	† AMD	
	SN74LS251	AMD	
	9LS251C	Fairchild	
	9LS251M	† Fairchild	
	54LS251	† Fairchild	
	74LS251	Fairchild	
	HD74LS251	Hitachi	
	SN54LS251	† Motorola	
	SN74LS251	Motorola	190
	μPB74LS151	NEC America	
	9LS251C	Raytheon	
	9LS251M	† Raytheon	
	25LS251C	Raytheon	
	25LS251M	† Raytheon	
	54LS251	† Raytheon	
	74LS251	Raytheon	
	54LS251	† Signetics	
	SN54LS251	† TI	
	SN74LS251	TI	200
TTL-S	SN54S251	† AMD	
	SN74S251	AMD	

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Values

DIGITAL–TTL (Cont'd)

Multiplexers (Cont'd.)

Function	Device	Source
TTL-S		(Cont'd.)
	54S251	† Fairchild
	74S251	Fairchild
	HD74S251	Hitachi
	M5S251	Mitsubishi
	DM74S251	National
	54LS251	† Signetics
	74S251	Signetics
	SN54S251	† TI
	SN74S251	TI
8-Input Multiplexer, Inverting/Non Inverting, Control Storage		
TTL-LS	AM25LS2535C	AMD
	AM25LS2535M	† AMD
	AM2922C	AMD
	AM2922M	† AMD
Dual 8-Input Multiplexer (two 8-to-1 sections)		
TTL	SN74351	TI
16-Input Multiplexer, Inverted Output, Strobe		
TTL	54150	† Fairchild
	74150	Fairchild
	ZN54150	† Ferranti
	ZN74150	Ferranti
	HD74150	Hitachi
	M53350	Mitsubishi
	MC54150	† Motorola
	MC74150	Motorola
	DM54150	† National
	DM74150	National
	μPB74150	NEC America
	54150	† Signetics
	74150	Signetics
	SN54150	† TI
	SN74150	TI
16-Input Multiplexer (Three-State 54/74150)		
TTL	DM7219	† National
	DM8219	National
10-Input, Quad, 8-to-1 Programmable Multiplexer, Three-State.		
TTL	29693C	Raytheon
	29693M	† Raytheon

Multivibrators

Function	Device	Source
Monostable Multivibrator, Schmitt Trigger Input*		
TTL	54121	† Fairchild
	74121	Fairchild
	ZN54121	† Ferranti
	ZN74121	Ferranti
	HD74121	Hitachi
	M53321	Mitsubishi
	MC54121	† Motorola
	MC74121	Motorola
	DM54121	† National
	DM74121	National
	54121	† Signetics
	74121	Signetics
	SN54121	† TI
	SN74121	TI
	TD34121	Toshiba
Retriggerable Monostable Multivibrator		
TTL	9601C	AMD
	9601M	† AMD
	9601C	Fairchild
	9601M	† Fairchild
	MC8601	Motorola
	MC9601	† Motorola

(Continued)

Multivibrators (Cont'd.)

Function	Device	Source
TTL		(Cont'd.)
	DM8601	National
	DM9601	† National
	RF8601	Raytheon
	RF9601	† Raytheon
	N8T22	Signetics
	SN29601	TI
Retriggerable Monostable Multivibrator, with Reset		
TTL	9600C	AMD
	9600M	† AMD
	AM2600C	AMD
	AM2600M	† AMD
	9600C	Fairchild
	9600M	† Fairchild
Retriggerable Monostable Multivibrator with Clear		
TTL	54122	† Fairchild
	74122	Fairchild
	ZN54122	† Ferranti
	ZN74122	Ferranti
	M53322	Mitsubishi
	MC54122	† Motorola
	MC74122	Motorola
	74122	Signetics
	SN54122	† TI
	SN74122	TI
TTL-LS	SN54LS122	† Motorola
	SN74LS122	Motorola
	DM54LS122	† National
	DM74LS122	National
	9LS122C	Raytheon
	9LS122M	† Raytheon
	54LS122	† Raytheon
	74LS122	Raytheon
	SN54LS122	† TI
	SN74LS122	TI
Bidirectional Monostable Multivibrator (Low Level Input)		
TTL	RC8T20	Raytheon
	RM8T20	† Raytheon
	N8T20	Signetics
Dual Monostable Multivibrator, Schmitt-Trigger Input (Dual 54/74121)		
TTL	SN54221	† AMD
	SN74221	AMD
	HD74221	Hitachi
	74221	Signetics
	SN54221	† TI
	SN74221	TI
TTL-LS	SN54LS221	† Motorola
	SN74LS221	Motorola
	DM54LS221	† National
	DM74LS221	National
	9LS221C	Raytheon
	9LS221M	† Raytheon
	54LS221	† Raytheon
	74LS221	Raytheon
	54LS221	† Signetics
	74LS221	Signetics
	SN54LS221	TI
	SN74LS221	TI
Dual Retriggerable Monostable Multivibrator with Reset (OR Triggered)		
TTL	AM2602C	AMD
	AM2602M	† AMD
	9602C	AMD
	9602M	† AMD

(Continued)

Multivibrators (Cont'd.)

Function	Device	Source	
TTL			(Cont'd.)
	96L02C	Fairchild	
	96L02M	† Fairchild	
	9602C	Fairchild	
	9602M	† Fairchild	
	MC8602	Motorola	
	MC9602	† Motorola	
	DM8602	National	
	DM9602	† National	
	μPB9602	NEC America	
	RF8602	Raytheon	
	RF9602	† Raytheon	
	N9602	Signetics	
	S9602	† Signetics	
TTL-LS	**96LS02C**	**Fairchild**	**(472)**
	96LS02M	**† Fairchild**	**(472)**
TTL-S	AM26S02C	AMD	
	AM26S02M	† AMD	
	96S02C	**Fairchild**	**(472)**
	96S02M	**† Fairchild**	**(472)**
Dual Retriggerable Monostable Multivibrator with Clear (AND Triggered)			
TTL	AM26123C	AMD	
	AM26123M	† AMD	
	SN54123	† AMD	
	SN74123	AMD	
	54123	† Fairchild	
	74123	Fairchild	
	ZN54123	† Ferranti	
	ZN74123	Ferranti	
	HD74123	Hitachi	
	M53323	Mitsubishi	
	MC54123	† Motorola	
	MC74123	Motorola	
	DM54123	† National	
	DM74123	National	
	μPB74123	NEC America	
	54123	† Signetics	
	74123	Signetics	
	SN54123	† TI	
	SN74123	TI	
TTL-LS	AM25LS123C	AMD	
	AM25LS123M	† AMD	
	SN54LS123	† AMD	
	SN74LS123	AMD	
	HD74LS123	Hitachi	
	SN54LS123	† Motorola	
	SN74LS123	Motorola	
	DM54LS123	† National	
	DM74LS123	National	
	9LS123C	Raytheon	
	9LS123M	† Raytheon	
	54LS123	† Raytheon	
	74LS123	Raytheon	
	SN54LS123	† TI	
	SN74LS123	TI	
Dual Monostable Multivibrator (Double-Edge)			
TTL	DM7853	† National	
	DM8853	National	
Dual Voltage-Controlled Multivibrator *			
TTL	11C24C	Fairchild	
	MC4024	Motorola	
	MC4324	† Motorola	

† Military Temperature Range (−55° to 125°C)

* Typical Values

Bold face indicates additional data is provided on the page noted.

DIGITAL–TTL (Cont'd)

Shift Registers

4-Bit Parallel Input, Parallel Output Shift Register

Function	Device	Source	Line
TTL	9300C	AMD	
	9300M	† AMD	
	SN54195	† AMD	
	SN74195	AMD	
	9300C	Fairchild	
	9300M	† Fairchild	
	54195	† Fairchild	
	74195	Fairchild	
	HD74195	Hitachi	
	MC8300	Motorola	10
	MC9300	† Motorola	
	MC54195	† Motorola	
	MC74195	Motorola	
	DM8300	National	
	DM9300	† National	
	DM54195	† National	
	DM74195	National	
	µPB74195	NEC America	
	RC9300	Raytheon	
	RM9300	† Raytheon	20
	54195	† Signetics	
	74195	Signetics	
	N9300	Signetics	
	S9300	† Signetics	
	SN54195	† TI	
	SN74195	TI	
TTL-LS	AM25LS195AC	AMD	
	AM25LS195AM	† AMD	
	SN54LS195A	† AMD	
	SN74LS195A	AMD	30
	9LS195C	Fairchild	
	9LS195M	† Fairchild	
	54LS195	† Fairchild	
	74LS195	Fairchild	
	HD74LS195A	Hitachi	
	SN54LS195A	† Motorola	
	SN74LS195A	Motorola	
	µPB74LS195	NEC America	
	9LS195AC	Raytheon	
	9LS195AM	† Raytheon	40
	25LS195AC	Raytheon	
	25LS195AM	† Raytheon	
	54LS195A	† Raytheon	
	74LS195A	Raytheon	
	54LS195A	† Signetics	
	74LS195A	Signetics	
	SN54LS195A	† TI	
	SN74LS195A	TI	
TTL-S	SN54S195	† AMD	
	SN74S195	AMD	50
	93S00C	Fairchild	
	93S00M	† Fairchild	
	DM74S195	National	
	74S195	Signetics	
	SN54S195	† TI	
	SN74S195	TI	

4-bit Parallel-In, Parallel Out, Right/Left Shift Register

Function	Device	Source	Line
TTL	5495	† Fairchild	
	7495	Fairchild	
	ZN5495A	† Ferranti	60
	ZN7495A	Ferranti	
	HD2534	Hitachi	
	M5395	Mitsubishi	
	M53295	Mitsubishi	
	MC4012	Motorola	
	MC4312	† Motorola	
	MC5495A	† Motorola	
	MC7495A	Motorola	

(Continued)

Shift Registers (Cont'd.)

Function	Device	Source	Line
TTL			(Cont'd.)
	DM5495	† National	70
	DM7495	National	
	5495A	† Signetics	
	7495A	Signetics	
	SN5495A	† TI	
	SN7495A	TI	
	TD3495	Toshiba	
TTL-LS	9LS95C	Fairchild	
	9LS95M	† Fairchild	
	54LS95B	† Fairchild	
	74LS95B	Fairchild	80
	HD74LS95B	Hitachi	
	SN54LS95B	† Motorola	
	SN74LS95B	Motorola	
	9LS95BC	Raytheon	
	9LS95BM	† Raytheon	
	54LS95B	† Raytheon	
	74LS95B	Raytheon	
	74LS95B	Signetics	
	SN54LS95B	† TI	
	SN74LS95B	TI	90

4-bit Universal Bidirectional Shift Register

Function	Device	Source	Line
TTL	SN54194	† AMD	
	SN74194	AMD	
	54194	† Fairchild	
	74194	Fairchild	
	ZN54194	† Ferranti	
	ZN74194	Ferranti	
	HD74194	Hitachi	
	MC54194	† Motorola	
	MC74194	Motorola	100
	DM54194	† National	
	DM74194	National	
	54194	† Signetics	
	74194	Signetics	
	SN54194	† TI	
	SN74194	TI	
TTL-LS	AM25LS194AC	AMD	
	AM25LS194AM	† AMD	
	SN54LS194A	† AMD	
	SN74LS194A	AMD	110
	9LS194C	Fairchild	
	9LS194M	† Fairchild	
	54LS194A	† Fairchild	
	74LS194A	Fairchild	
	HD74LS194A	Hitachi	
	SN54LS194A	† Motorola	
	SN74LS194A	Motorola	
	µPB74LS194	NEC America	
	9LS194AC	Raytheon	
	9LS194AM	† Raytheon	120
	25LS194AC	Raytheon	
	25LS194AM	† Raytheon	
	54LS194A	† Raytheon	
	74LS194A	Raytheon	
	74LS194A	Signetics	
	SN54LS194A	† TI	
	SN74LS194A	TI	
TTL-S	SN54S194	† AMD	
	SN74S194	AMD	
	54S194	† Fairchild	130
	74S194	Fairchild	
	DM74S194	National	
	74S194	Signetics	
	SN54S194	† TI	
	SN74S194	TI	

Shift Registers (Cont'd.)

4-bit Parallel In, Parallel Out, Right/Left Shift Register, Three-State

Function	Device	Source	Line
TTL-LS	9LS295C	Fairchild	
	9LS295M	† Fairchild	
	54LS295	† Fairchild	140
	74LS295	Fairchild	
	SN54LS295A	† Motorola	
	SN74LS295A	Motorola	
	µPB74LS295	NEC America	
	9LS295AC	Raytheon	
	9LS295AM	† Raytheon	
	54LS295A	† Raytheon	
	74LS295A	Raytheon	
	74LS295B	Signetics	
	SN54LS295B	† TI	150
	SN74LS295B	TI	

4-bit Parallel-In, Parallel-Out, Cascadable Shift Register, Three-State

Function	Device	Source	Line
TTL-LS	9LS395C	Fairchild	
	54LS395	† Fairchild	
	74LS395	Fairchild	
	SN54LS395A	† Motorola	
	SN74LS395A	Motorola	
	µPB74LS395	NEC America	
	9LS395AC	**Raytheon (557)**	160
	9LS395AM	**† Raytheon (557)**	
	54LS395A	**† Raytheon (557)**	
	74LS395A	**Raytheon (557)**	
	54LS395	† Signetics	
	74LS395	Signetics	
	SN54LS395A	† TI	
	SN74LS395A	TI	

4-bit Parallel-In, Parallel Out, Shift Register, (with load, shift, hold control)

Function	Device	Source	Line
TTL	54178	† Fairchild	170
	74178	Fairchild	
	MC7270	Motorola	
	MC8270	† Motorola	
	RC8270	Raytheon	
	RM8270	† Raytheon	
	S8270	† Signetics	
	N8270	Signetics	
	SN54178	† TI	
	SN74178	TI	
TTL-S	74S178	Signetics	180
	N82S70	Signetics	

4-bit Parallel-In, Parallel Out, Shift Register, with Reset, Complementary Output for last bit

Function	Device	Source	Line
TTL	54179	† Fairchild	
	74179	Fairchild	
	MC7271	Motorola	
	MC8271	† Motorola	
	RC8271	Raytheon	
	RM8271	† Raytheon	
	N8271	Signetics	190
	S8271	† Signetics	
	SN54179	† TI	
	SN74179	TI	
TTL-S	74S179	Signetics	
	N82S71	Signetics	

4-bit Parallel-In, Serial-Out, Shift Register

Function	Device	Source	Line
TTL	5494	† Fairchild	
	7494	Fairchild	
	ZN5494	† Ferranti	
	ZN7494	Ferranti	200
	MC5494	† Motorola	
	MC7494	Motorola	
	5494	† Signetics	

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† Military Temperature Range (−55° to 125°C)

* Typical Values

DIGITAL–TTL (Cont'd)

Shift Registers (Cont'd.)

Function	Device	Source	Line
TTL		(Cont'd.)	
	7494	Signetics	
	SN5494	† TI	
	SN7494	TI	
5-bit Parallel-In, Parallel-Out, Shift Register			
TTL	5496	† Fairchild	
	7496	Fairchild	
	ZN5496	† Ferranti	
	ZN7496	Ferranti	
	HD7496	Hitachi	10
	M53296	Mitsubishi	
	MC5496	† Motorola	
	MC7496	Motorola	
	DM5496	† National	
	DM7496	National	
	5496	† Signetics	
	7496	Signetics	
	SN5496	† TI	
	SN7496	TI	
TTL-LS	54LS96	† Signetics	20
	74LS96	Signetics	
	SN54LS96	† TI	
	SN74LS96	TI	
5-bit Right/Left Shift Register with Clear			
TTL	M54403	Mitsubishi	
8-bit Parallel-In, Parallel-Out, Unidirectional Shift Register			
TTL	54199	† Fairchild	
	74199	Fairchild	
	HD74199	Hitachi	30
	M53399	Mitsubishi	
	DM54199	† National	
	DM74199	National	
	54199	† Signetics	
	74199	Signetics	
	SN54199	† TI	
	SN74199	TI	
8-bit Parallel-In, Parallel-Out, Right/Left Shift Register			
TTL	54198	† Fairchild	
	74198	Fairchild	40
	HD74198	Hitachi	
	M53398	Mitsubishi	
	DM54198	† National	
	DM74198	National	
	μPB74198	NEC America	
	54198	† Signetics	
	74198	Signetics	
	SN54198	† TI	
	SN74198	TI	
8-bit Universal Shift Register, Three-State			50
TTL	DM7546	† National	
	DM8546	National	
TTL-LS	AM25LS23C	AMD	
	AM25LS23M	† AMD	
	AM25LS299C	AMD	
	AM25LS299M	† AMD	
	SN54LS299	† AMD	
	SN74LS299	AMD	
	SN54LS323	† AMD	
	SN74LS323	AMD	60
	54LS299	† Fairchild	
	74LS299	Fairchild	
	54LS323	† Fairchild	
	74LS323	Fairchild	
	54LS299	† MMI	
	74LS299	MMI	

(Continued)

Shift Registers (Cont'd.)

Function	Device	Source	Line
TTL-LS		(Cont'd.)	
	54LS323	† MMI	
	74LS323	MMI	
	SN54LS299	† Motorola	70
	SN74LS299	Motorola	
	SN54LS323	† Motorola	
	SN74LS323	Motorola	
	9LS299C	**Raytheon (533)**	
	9LS299M	**† Raytheon (533)**	
	25LS23C	Raytheon	
	25LS23M	† Raytheon	
	25LS299C	**Raytheon (533)**	
	25LS299M	**† Raytheon (533)**	
	54LS299	**† Raytheon (533)**	80
	74LS299	**Raytheon (533)**	
	9LS323C	**Raytheon (540)**	
	9LS323M	**† Raytheon (540)**	
	54LS323	**† Raytheon (540)**	
	74LS323	**Raytheon (540)**	
	SN54LS299	† TI	
	SN74LS299	TI	
	SN54LS323	† TI	
	SN74LS323	TI	
TTL-S	SN54S299	† TI	90
	SN74S299	TI	
8-bit Parallel-In, Serial-Out Shift Register, Complementary Output			
TTL	54165	† Fairchild	
	74165	Fairchild	
	ZN54165	† Ferranti	
	ZN74165	Ferranti	
	M53365	Mitsubishi	
	MC54165	† Motorola	
	MC74165	Motorola	100
	DM54165	† National	
	DM74165	National	
	54165	† Signetics	
	74165	Signetics	
	SN54165	† TI	
	SN74165	TI	
TTL-LS	74LS165	Fairchild	
	SN54LS165	† Motorola	
	SN74LS165	Motorola	
	SN54LS165	† TI	110
	SN74LS165	TI	
8-bit Parallel-In, Serial-Out Shift Register with Clear			
TTL	54166	† Fairchild	
	74166	Fairchild	
	ZN54166	† Ferranti	
	ZN74166	Ferranti	
	HD74166	Hitachi	
	M53366	Mitsubishi	
	DM54166	† National	
	DM74166	National	120
	54166	† Signetics	
	74166	Signetics	
	SN54166	† TI	
	SN74166	TI	
TTL-LS	SN54LS166	† Motorola	
	SN74LS166	Motorola	
	SN54LS166	† TI	
	SN74LS166	TI	
8-bit Gated Serial-In, Parallel-Out Shift Register			
TTL	SN54164	† AMD	130
	SN74164	AMD	
	54164	† Fairchild	
	74164	Fairchild	

(Continued)

Shift Registers (Cont'd.)

Function	Device	Source	Line
TTL		(Cont'd.)	
	ZN54164	† Ferranti	
	ZN74164	Ferranti	
	HD74164	Hitachi	
	M53364	Mitsubishi	
	DM7570	† National	
	DM8570	National	140
	DM54164	† National	
	DM74164	National	
	μPB74164	NEC America	
	54164	† Signetics	
	74164	Signetics	
	SN54164	† TI	
	SN74164	TI	
	TD3503	Toshiba	
TTL-LS	AM25LS164C	AMD	
	AM25LS164M	AMD	150
	SN54LS164	† AMD	
	SN74LS164	AMD	
	54LS164	† Fairchild	
	74LS164	Fairchild	
	HD74LS164	Hitachi	
	SN54LS164	† Motorola	
	SN74LS164	Motorola	
	DM54LS164	† National	
	DM74LS164	National	
	μPB74LS164	NEC America	160
	9LS164C	Raytheon	
	9LS164M	† Raytheon	
	54LS164	† Raytheon	
	74LS164	Raytheon	
	54LS164	† Signetics	
	74LS164	Signetics	
	SN54LS164	† TI	
	SN74LS164	TI	
8-bit Serial-In, Serial-Out Shift Register			
TTL	5491	† Fairchild	170
	7491	Fairchild	
	ZN5491	† Ferranti	
	ZN7491	Ferranti	
	HD7491A	Hitachi	
	M5391	Mitsubishi	
	M53291	Mitsubishi	
	MC5491	† Motorola	
	MC7491	Motorola	
	DM5491A	† National	
	DM7491A	National	180
	μPB7491	NEC America	
	N8276	Signetics	
	5491	† Signetics	
	7491	Signetics	
	SN5491A	† TI	
	SN7491A	TI	
	* TD3491	Toshiba	
TTL-LS	9LS91C	Raytheon	
	9LS91M	† Raytheon	
	54LS91	† Raytheon	190
	74LS91	Raytheon	
	SN54LS91	† TI	
	SN74LS91	TI	
8-bit Serial/Parallel-In Register with Sign Extend (for use with 25LS14/74LS384 Multiplier)			
TTL-LS	AM25LS22C	AMD	
	AM25LS22M	† AMD	
	SN54LS322	† AMD	
	SN74LS322	AMD	
	25LS22C	Raytheon	200
	25LS22M	† Raytheon	

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Values

Bold face indicates additional data is provided on the page noted.

DIGITAL–TTL (Cont'd)

Shift Registers (Cont'd.)

Function	Device	Source		Line
TTL-LS			(Cont'd.)	
	54LS322	† MMI		
	74LS322	MMI		
	SN54LS322	† Motorola		
	SN74LS322	Motorola		
	9LS322C	**Raytheon**	**(537)**	
	9LS322M	**† Raytheon**	**(537)**	
	54LS322	**† Raytheon**	**(537)**	
	74LS322	**Raytheon**	**(537)**	10
	SN54LS322A	† TI		
	SN74LS322A	TI		
Octal Storage Register, two stage 4-bit wide shift register				
TTL-LS	SN54LS396	† TI		
	SN74LS396	TI		
Dual Rank 8-bit Shift Register (8-bit I/O buffer, "A" register, and serial "B" register)				
TTL-LS	DM76LS52	† National		
	DM86LS52	National		20
	DM76LS62	† National		
	DM86LS62	National		
10-bit Parallel-In, Parallel-Out Buffer Register, with Reset (clocked flip-flops)				
TTL	RC8202	Raytheon		
	RM8202	† Raytheon		
	N8202	Signetics		
	S8202	† Signetics		
10-bit Parallel-In, Parallel-Out Buffer Register, with Reset, Inverting Output (clocked flip-flops)				30
TTL	RC8203	Raytheon		
	RM8203	† Raytheon		
	N8203	Signetics		
	S8203	† Signetics		
10-bit Parallel-In, Serial-Out Shift Register				
TTL	RC8274	Raytheon		
	RM8274	† Raytheon		
	N8274	Signetics		
	S8274	Signetics		
10-bit Serial-In, Parallel-Out Shift Register				40
TTL	RC8273	Raytheon		
	RM8273	† Raytheon		
	N8273	Signetics		
	S8273	† Signetics		
Dual 5-bit Parallel-In, Parallel-Out Buffer Register, (clocked flip-flops)				
TTL	RC8200	Raytheon		
	RM8200	† Raytheon		
	N8200	Signetics		
	S8200	† Signetics		50
Dual 5-bit Parallel-In, Parallel-Out, Buffer Register, Inverting Output (clocked flip-flops)				
TTL	RC8201	Raytheon		
	RM8201	† Raytheon		
	N8201	Signetics		
	S8201	† Signetics		
Dual 8-bit Serial-In, Serial-Out, Shift Register				
TTL	9328C	AMD		
	9328M	† AMD		
	9328C	Fairchild		60
	9328M	† Fairchild		
	MC8328	Motorola		
	MC9328	† Motorola		
	RC8277	Raytheon		
	RM8277	† Raytheon		
	N8277	Signetics		

Shift Registers (Cont'd.)

Function	Device	Source	Line
16-bit Serial-In, Serial-Out Register plus Stored Parallel Output			
TTL-LS	SN54LS673	† TI	
	SN74LS673	TI	70
16-bit Parallel-In, Serial-Out Shift Register			
TTL-LS	SN54LS674	† TI	
	SN74LS674	TI	

Translators

Function	Device	Source	Line
Hex DTL to TTL Inverter			
TTL	9109C	Fairchild	
	9109M	† Fairchild	
Hex TTL to DTL Inverter			
TTL	9112C	Fairchild	
	9112M	† Fairchild	
Dual MOS to TTL Level Converter			80
TTL	9625C	Fairchild	
	9625M	† Fairchild	
Dual MOS to TTL Level Translator, Three-State			
TTL	MC4068	Motorola	
	MC4368	† Motorola	
	MC54468	† Motorola	
	MC74468	Motorola	
7-Unit MOS to TTL Level Converter			
TTL	SN75270	TI	
Dual 2-Input NAND Gate, High Voltage to TTL Interface, to 30v Input			90
TTL	N8T18	Signetics	
	S8T18	† Signetics	
Dual TTL to MOS Voltage Translator			
TTL	D130A	† Siliconix	
	D130B	Siliconix	
	D139A	† Siliconix	
	D139B	Siliconix	
Dual 2-Input NAND TTL to MOS Voltage Translator			
TTL	9624C	Fairchild	100
	9624M	† Fairchild	
	DH0034	† National	
	DH0034C	National	
	DS7800	† National	
	DS8800	National	
	SN55180	† TI	
	SN75180	TI	
Hex TTL to MOS Voltage Translator			
TTL	DS7812	† National	
	DS8812	National	110
	DS78L12	† National	
	DS88L12	National	
	D123A	† Siliconix	
	D123B	Siliconix	
	D125A	† Siliconix	
	D125B	Siliconix	
Quad 2-Input NAND TTL to MOS Voltage Translators			
TTL	DS7810	† National	
	DS8810	National	
	DS7811	† National	120
	DS8811	National	
Quad 2-Input AND TTL to MOS Voltage Translators			
TTL	DS7819	† National	
	DS8819	National	
Dual ECL to MOS Driver (also ECL to TTL)			
TTL	MC75358	Motorola	
	MC75368	Motorola	
	SN75368	TI	

Translators (Cont'd.)

Function	Device	Source	Line
Quad TTL to MOS Inverter/Driver, Three-State			
TTL	SN75357	TI	130
	SN75367	TI	

For other translators, see Interface-Sense Amplifiers and also Memory and Peripheral Drivers

Miscellaneous

Function	Device	Source		Line
Field Programmable Array Logic; AND-OR Gate Array				
TTL	**PAL10H8C**	**MMI**	**(1479)**	
	PAL10H8M	**† MMI**	**(1479)**	
	PAL12H6C	**MMI**	**(1479)**	
	PAL12H6M	**† MMI**	**(1479)**	
	PAL14H4C	**MMI**	**(1479)**	
	PAL14H4M	**† MMI**	**(1479)**	140
	PAL16C1C	**MMI**	**(1479)**	
	PAL16C1M	**† MMI**	**(1479)**	
	PAL16H2C	**MMI**	**(1479)**	
	PAL16H2M	**† MMI**	**(1479)**	
	PAL10H8C	Raytheon		
	PAL10H8M	† Raytheon		
	PAL12H6C	Raytheon		
	PAL12H6M	† Raytheon		
	PAL14H4C	Raytheon		
	PAL14H4M	† Raytheon		150
	PAL16C1C	Raytheon		
	PAL16C1M	† Raytheon		
	PAL16H2C	Raytheon		
	PAL16H2M	† Raytheon		
Field Programmable Array Logic; AND-OR INVERT Gate Array				
TTL	**PAL10L8C**	**MMI**	**(1479)**	
	PAL10L8M	**† MMI**	**(1479)**	
	PAL12L6C	**MMI**	**(1479)**	
	PAL12L6M	**† MMI**	**(1479)**	160
	PAL14L4C	**MMI**	**(1479)**	
	PAL14L4M	**† MMI**	**(1479)**	
	PAL16L2C	**MMI**	**(1479)**	
	PAL16L2M	**† MMI**	**(1479)**	
	PAL16L8C	**MMI**	**(1479)**	
	PAL16L8M	**† MMI**	**(1479)**	
	PAL10L8C	Raytheon		
	PAL10L8M	† Raytheon		
	PAL12L6C	Raytheon		
	PAL12L6M	† Raytheon		170
	PAL14L4C	Raytheon		
	PAL14L4M	† Raytheon		
	PAL16L2C	Raytheon		
	PAL16L2M	† Raytheon		
	PAL16L8C	Raytheon		
	PAL16L8M	† Raytheon		
Field Programmable Array Logic; AND-OR INVERT Gate Array with registers				
TTL	**PAL16R4C**	**MMI**	**(1479)**	
	PAL16R4M	**† MMI**	**(1479)**	180
	PAL16R6C	**MMI**	**(1479)**	
	PAL16R6M	**† MMI**	**(1479)**	
	PAL16R8C	**MMI**	**(1479)**	
	PAL16R8M	**† MMI**	**(1479)**	
	PAL16R4C	Raytheon		
	PAL16R4M	† Raytheon		
	PAL16R6C	Raytheon		
	PAL16R6M	† Raytheon		
	PAL16R8C	Raytheon		
	PAL16R8M	† Raytheon		190
Field Programmable Array Logic; AND-OR-XOR Gate Array with registers				
TTL	**PAL16X4C**	**MMI**	**(1479)**	
	PAL16X4M	**† MMI**	**(1479)**	

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Values

DIGITAL–TTL (Cont'd)

Miscellaneous (Cont'd.)

Function	Device	Source	Line
TTL		(Cont'd.)	
	PAL16X4C	Raytheon	
	PAL16x4M	† Raytheon	
Field Programmable Array Logic; AND-CARRY-OR-XOR-INVERT Gate Array with registers			
TTL	**PAL16A4C**	**MMI (1479)**	
	PAL16A4M	**† MMI (1479)**	
	PAL16A4C	Raytheon	10
	PAL16A4M	† Raytheon	
Programmable Logic Array, Mask Programmed (See also Memory-PLAs)			
TTL	DM7575	† National	
	DM7576	† National	
	DM8575	National	
	DM8576	National	
TTL-S	N82S200	Signetics	
	N82S201	Signetics	
Programmable Logic Arrays, Field Programmable (See also Memory-PLAs)			20
TTL	IM5200	Intersil	
TTL-S	82S100	MMI	
	82S101	MMI	
	N82S100	**Signetics (1684)**	
	S82S100	**† Signetics (1684)**	
	N82S101	**Signetics (1684)**	
	S82S101	**† Signetics (1684)**	
	SN54S330	† TI	
	SN74S330	TI	30
	SN54S331	† TI	
	SN74S331	TI	
Bubble Memory Controller (T-Bar)			
TTL-LS	SN54LS360	† TI	
	SN74LS360	TI	
Bubble Memory Controller (Chevron)			
TTL-LS	SN54LS361	† TI	
	SN74LS361	TI	
4-bit True/Complement Zero/One Element			
TTL-H	54H87	† Fairchild	40
	74H87	Fairchild	
	MC54H87	† Motorola	
	MC74H87	Motorola	
	SN54H87	† TI	
	SN74H87	TI	
Dual 4-Input Expander (for H50, H53, H55)			
TTL-H	54H60	† Fairchild	
	74H60	Fairchild	
	DM54H60	† National	
	DM74H60	National	50
	54H60	† Signetics	
	74H60	Signetics	
	SN54H60	† TI	
	SN74H60	TI	
Triple 3-Input Expander (for H52)			
TTL-H	54H61	† Fairchild	
	74H61	Fairchild	
	DM54H61	† National	
	DM74H61	National	
	54H61	† Signetics	60
	74H61	Signetics	
	SN54H61	† TI	
	SN74H61	TI	
3-2-2-3-Input AND-OR Expander (for H50, H53, H55)			
TTL-H	54H62	† Fairchild	
	74H62	Fairchild	

(Continued)

Miscellaneous (Cont'd.)

Function	Device	Source	Line
TTL-H		(Cont'd.)	
	DM54H62	† National	
	DM74H62	National	
	54H62	† Signetics	70
	74H62	Signetics	
	SN54H62	† TI	
	SN74H62	TI	
8-bit Successive Approximation Register			
TTL	AM2502C	AMD	
	AM2502M	† AMD	
	AM2503C	AMD	
	AM2503M	† AMD	
	AM2502	Intersil	
	AM2503	Intersil	80
	DM2502	**† National (1073)**	
	DM2502C	**National (1073)**	
	DM2503	**† National (1073)**	
	DM2503C	**National (1073)**	
TTL-LS	54LS502	† Fairchild	
	54LS503	**† Fairchild (488)**	
	74LS502	Fairchild	
	74LS503	**Fairchild (488)**	
	SN54LS502	† Motorola	
	SN74LS502	Motorola	90
	SN54LS503	† Motorola	
	SN74LS503	Motorola	
12-bit Successive Approximation Register			
TTL	AM2504C	AMD	
	AM2504M	† AMD	
	AM2504	Intersil	
	DM2504	**† National (1073)**	
	DM2504C	**National (1073)**	
TTL-LS	**54LS504**	**† Fairchild (488)**	
	74LS504	**Fairchild (488)**	100
	SN54LS504	† Motorola	
	SN74LS504	Motorola	
8-bit Position Scaler (The output is shifted with respect to the input up to 8 positions as determined by a 3-bit selector code.)			
TTL	RC8243	Raytheon	
	RM8243	† Raytheon	
	N8243	Signetics	
	S8243	† Signetics	
4-bit Shifter (shifts data 0, 1, 2, or 3 places as determined by 2-bit selector code)			110
TTL-S	SN54S350	† AMD	
	SN74S350	AMD	
	54S350	**† Signetics (561)**	
	74S350	**Signetics (561)**	
4-bit Shifter, Three-State (Shifts 0, 1, 2, or 3-bits under 2-Line Select Control)			
TTL-S	AM25S10C	AMD	
	AM25S10M	† AMD	
	N25S10	Signetics	120
6-bit Synchronous Binary Rate Multiplier			
TTL	5497	† Fairchild	
	7497	Fairchild	
	MC5497	† Motorola	
	MC7497	Motorola	
	SN5497	† TI	
	SN7497	TI	
Synchronous Decade Rate Multiplier			
TTL	54167	† Fairchild	
	74167	Fairchild	130
	MC54167	† Motorola	
	MC74167	Motorola	

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Miscellaneous (Cont'd.)

Function	Device	Source	Line
TTL		(Cont'd.)	
	SN54167	† TI	
	SN74167	TI	
TTL-S	54S167	† Fairchild	
	74S167	Fairchild	
4-bit Priority Register, Cascadable			
TTL	M53478	Mitsubishi	
	SN54278	† TI	140
	SN74278	TI	
8-Input Priority Encoder			
TTL	9318C	AMD	
	9318M	† AMD	
	9318C	Fairchild	
	9318M	† Fairchild	
	HD74148	Hitachi	
	M53348	Mitsubishi	
	MC8318	Motorola	
	MC9318	† Motorola	150
	DM8318	National	
	DM9318	† National	
	DM54148	† National	
	DM74148	National	
	μPB74148	NEC America	
	54148	† Signetics	
	74148	Signetics	
	SN29318	TI	
	SN39318	† TI	
	SN54148	† TI	160
	SN74148	TI	
TTL-LS	AM2913C	AMD	
	AM2913M	† AMD	
	AM25LS148C	AMD	
	AM25LS148M	† AMD	
	SN54LS148	† AMD	
	SN74LS148	AMD	
	AM25LS2513C	AMD	
	AM25LS2513M	† AMD	
	SN54LS148	† TI	170
	SN74LS148	TI	
	SN54LS348	† TI	
	SN74LS348	TI	
10-Input Priority Encoder			
TTL	HD74147	Hitachi	
	M53347	Mitsubishi	
	DM54147	† National	
	DM74147	National	
	μPB74147	NEC America	
	54147	† Signetics	180
	74147	Signetics	
	SN54147	† TI	
	SN74147	TI	
TTL-LS	SN54LS147	† TI	
	SN74LS147	TI	
8-bit Parity Tree			
TTL	MC4008	Motorola	
	MC4308	† Motorola	
	MC54408	† Motorola	
	MC74408	Motorola	190
Dual 4-bit Parity Tree			
TTL	MC4010	Motorola	
	MC4310	† Motorola	
9-bit Parity Generator/Checker			
TTL	DM7220	† National	
	DM8220	National	

† Military Temperature Range (−55° to 125°C)

* Typical Values

Bold face indicates additional data is provided on the page noted.

DIGITAL–TTL (Cont'd)

Miscellaneous (Cont'd.)

Function	Device	Source	Line
9-bit Odd/Even Parity Generator/Checker			
TTL	54180	† Fairchild	
	74180	Fairchild	
	ZN54180	† Ferranti	
	ZN74180	Ferranti	
	HD74180	Hitachi	
	M53380	Mitsubishi	
	MC54180	† Motorola	
	MC74180	Motorola	
	DM54180	† National	
	DM74180	National	10
	μPB8262	NEC America	
	μPB74180	NEC America	
	RC8262	Raytheon	
	RM8262	† Raytheon	
	N8262	Signetics	
	S8262	† Signetics	
	54180	† Signetics	
	74180	Signetics	
	SN54180	† TI	
	SN74180	TI	20
TTL-LS	54LS280	† Fairchild	
	74LS280	Fairchild	
	SN54LS280	† TI	
	SN74LS280	TI	
TTL-S	82S62C	AMD	
	82S62M	† AMD	
	93S62C	Fairchild	
	93S62M	† Fairchild	
	HD74S280	Hitachi	
	DM74S280	National	30
	74S280	Signetics	
	N82S62	Signetics	
	SN54S280	† TI	
	SN74S280	TI	
12-Input Odd/Even Parity Checker/Generator			
TTL	9348C	Fairchild	
	9348M	† Fairchild	
TTL-S	93S48C	AMD	
	93S48M	† AMD	
Clock Generator/Driver			
TTL-LS	AM25LS2525C	AMD	40
	AM25LS2525M	† AMD	
Cyclic Redundancy Checker			
TTL	**9401C**	**Fairchild (1893,1894)**	
	9401M	**† Fairchild (1893,1894)**	
	9411C	**Fairchild (1893,1894)**	
Phase Locked Loop			
TTL-LS	SN54LS297	† TI	50
	SN74LS297	TI	
4-bit Universal Presettable Polynomial Generator			
TTL	MC8504	Motorola	
Polynomial Generator			
TTL	MC8506	Motorola	
Single Error Hamming Code Detector and Generator			
TTL	MC4041	Motorola	
BCD-To-Binary/Binary-To-BCD Number Converter			
TTL	MC4001	Motorola	60
BCD-To-Binary Converter			
TTL	ZN54184	† Ferranti	
	ZN74184	Ferranti	
	DM54184	† National	

(Continued)

Miscellaneous (Cont'd.)

Function	Device	Source	Line
TTL		(Cont'd.)	
	DM74184	National	
	SN54184	† TI	
	SN74184	TI	
BCD-To-Binary Converter (Three-State 54/74184)			
TTL	DM8898	National	70
Binary-To-BCD Converter			
TTL	M53385	Mitsubishi	
	DM54185A	† National	
	DM74185A	National	
	DM8899	National	
	SN54185A	† TI	
	SN74185A	TI	
Dual Pulse Synchronizer/Driver			
TTL	MC54120	† Motorola	
	MC74120	Motorola	80
	SN54120	† TI	
	SN74120	TI	
Quad Power Strobe (Vcc strobe or digit driver)			
TTL	HD6600-2	† Harris	
	HD6600-5	Harris	
	HD6605-2	† Harris	
	HD6605-5	Harris	
	HD6600-2	† MMI	
	HD6600-5	MMI	
	HD6605-2	† MMI	90
	HD6605-5	MMI	
Phase-Frequency Detector			
TTL	11C44C	Fairchild	
	MC4044	Motorola	
	MC4344	† Motorola	
Contact Bounce Eliminator			
TTL	DM7544	† National	
	DM8544	National	
Quad Complementary-Output Elements (for symmetrical generation of complementary outputs)			100
TTL	SN54265	† TI	
	SN74265	TI	
Dual Zero Crossing Detector			
TTL	N8T363	Signetics	
MOS Dynamic Memory Refresh Logic Circuit			
TTL	MC8505	Motorola	
Data Encryption, 4 Device Set			
I^2L	9414-1	Fairchild	
	9414-2	Fairchild	
	9414-3	Fairchild	110
	9414-4	Fairchild	
Dual 4-Input NAND Schmitt-Trigger			
TTL	5413	† Fairchild	
	7413	Fairchild	
	ZN5413	† Ferranti	
	ZN7413	Ferranti	
	HD7413	Hitachi	
	M53213	Mitsubishi	
	MC5413	† Motorola	
	MC7413	Motorola	120
	DM5413	† National	
	DM7413	National	
	μPB7413	NEC America	
	5413	† Signetics	
	7413	Signetics	
	SN5413	† TI	
	SN7413	TI	
TTL-LS	9LS13C	Fairchild	

(Continued)

Miscellaneous (Cont'd.)

Function	Device	Source	Line
TTL-LS		(Cont'd.)	
	9LS13M	† Fairchild	130
	54LS13	† Fairchild	
	74LS13	Fairchild	
	HD74LS13	Hitachi	
	SN54LS13	† Motorola	
	SN74LS13	Motorola	
	DM54LS13	† National	
	DM74LS13	National	
	9LS13C	Raytheon	
	9LS13M	† Raytheon	
	54LS13	† Raytheon	140
	74LS13	Raytheon	
	54LS13	† Signetics	
	74LS13	Signetics	
	SN54LS13	† TI	
	SN74LS13	TI	
Quad 2-Input NAND Schmitt-Trigger			
TTL	54132	† Fairchild	
	74132	Fairchild	
	HD74132	Hitachi	
	M53332	Mitsubishi	150
	MC54132	† Motorola	
	MC74132	Motorola	
	DM54132	† National	
	DM74132	National	
	54132	† Signetics	
	74132	Signetics	
	SN54132	† TI	
	SN74132	TI	
TTL-LS	9LS132C	Fairchild	
	9LS132M	† Fairchild	160
	54LS132	† Fairchild	
	74LS132	Fairchild	
	HD74LS132	Hitachi	
	SN54LS132	† Motorola	
	SN74LS132	Motorola	
	DM54LS132	† National	
	DM74LS132	National	
	9LS132C	Raytheon	
	9LS132M	† Raytheon	
	54LS132	† Raytheon	170
	74LS132	Raytheon	
	74LS132	Signetics	
	54LS132	† Signetics	
	SN54LS132	† TI	
	SN74LS132	TI	
TTL-S	54S132	† Fairchild	
	74S132	Fairchild	
	SN54S132	† TI	
	SN74S132	TI	
Hex Schmitt Trigger, Inverting			180
TTL	5414	† Fairchild	
	7414	Fairchild	
	HD7414	Hitachi	
	M53214	Mitsubishi	
	MC5414	† Motorola	
	MC7414	Motorola	
	DM5414	† National	
	DM7414	National	
	5414	† Signetics	
	7414	Signetics	190
	SN5414	† TI	
	SN7414	TI	
TTL-LS	9LS14C	Fairchild	
	9LS14M	† Fairchild	
	54LS14	† Fairchild	

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Values

IC MASTER

DIGITAL–TTL (Cont'd)

Miscellaneous (Cont'd.)

Function	Device	Source	Line
TTL-LS		(Cont'd.)	
	74LS14	Fairchild	
	HD74LS14	Hitachi	
	SN54LS14	† Motorola	
	SN74LS14	Motorola	
	DM54LS14	† National	
	DM74LS14	National	
	9LS14C	Raytheon	
	9LS14M	† Raytheon	
	54LS14	† Raytheon	10
	74LS14	Raytheon	
	54LS14	† Signetics	
	74LS14	Signetics	
	SN54LS14	† TI	
	SN74LS14	TI	
Voltage Controlled Oscillator (or Crystal Controlled)			
TTL-LS	SN54LS324	† TI	
	SN74LS324	TI	
Oscillator Clock/Driver			
TTL-LS	SN54LS320	† TI	20
	SN74LS320	TI	
	SN54LS321	† TI	
	SN74LS321	TI	
Dual Voltage Controlled Oscillator (or Crystal Controlled)			
TTL-LS	SN54LS124	† TI	
	SN74LS124	TI	
	SN54LS325	† TI	
	SN74LS325	TI	
	SN54LS326	† TI	30
	SN74LS326	TI	
	SN54LS327	† TI	
	SN74LS327	TI	
TTL-S	SN54S124	† TI	
	SN74S124	TI	
	SN54LS328	† TI	
	SN74LS328	TI	
Voltage Comparator (Analog Input-Digital Output)			
TTL-S	686C	AMD	
	686M	† AMD	40
Decade Sequencer (sequential 1 of 10 Decoder), adjustable sequence length			
TTL	9319C	Fairchild	
	9319M	† Fairchild	
	9320C	Fairchild	
	9320M	† Fairchild	
Bus Transfer Switch (transmit-receive connections to 4 bus terminals)			
TTL	MC4060	Motorola	
	MC4363	† Motorola	50
	MC54460	† Motorola	
	MC74460	Motorola	
Triple Bidirectional Bus Switch, Three-State (Connects any 2 of 3 inputs together)			
TTL-S	MC6881	Motorola	
	MC3449	Motorola	
Quad Three Bus Transceiver, Three State			
TTL-LS	SN54LS442	† TI	
	SN74LS442	TI	
	SN54LS443	† TI	60
	SN74LS443	TI	
	SN54LS444	† TI	
	SN74LS444	TI	
Quad Bus Transceiver			
TTL-LS	AM25LS242C	AMD	

(Continued)

Miscellaneous (Cont'd.)

Function	Device	Source	Line
TTL-LS		(Cont'd.)	
	AM25LS242M	† AMD	
	SN54LS242	† AMD	
	SN74LS242	AMD	
	AM25LS243C	AMD	70
	AM25LS243M	† AMD	
	SN54LS243	† AMD	
	SN74LS243	AMD	
	54LS242	† Fairchild	
	74LS242	Fairchild	
	54LS243	† Fairchild	
	74LS243	Fairchild	
	SN54LS242	† Motorola	
	SN74LS242	Motorola	
	SN54LS243	† Motorola	80
	SN74LS243	Motorola	
	9LS242C	**Raytheon (528)**	
	9LS242M	**† Raytheon (528)**	
	25LS242C	**Raytheon (528)**	
	25LS242M	**† Raytheon (528)**	
	54LS242	**† Raytheon (528)**	
	74LS242	**Raytheon (528)**	
	9LS243C	**Raytheon (528)**	
	9LS243M	**† Raytheon (528)**	
	25LS243C	**Raytheon (528)**	90
	25LS243M	**† Raytheon (528)**	
	54LS243	**† Raytheon (528)**	
	74LS243	**Raytheon (528)**	
	74LS242	Signetics	
	74LS243	Signetics	
	SN54LS242	† TI	
	SN74LS242	TI	
	SN54LS243	† TI	
	SN74LS243	TI	
TTL-S	SN54S242	† AMD	100
	SN74S242	AMD	
	SN54S243	† AMD	
	SN74S243	AMD	
4-bit Parallel Bus Transceiver, Non-Inverting, Three-State			
TTL-S	N8T28	AMD	
	MC8T28	Motorola	
	MC6889	Motorola	
	DS8T28	National	
	DS8T28M	† National	110
	N8T28	Signetics	
	N8T128	**Signetics (2297)**	
	S8T128	**† Signetics (2297)**	
	N8T129	**Signetics (2297)**	
	S8T129	**† Signetics (2297)**	
4-bit Parallel Universal Bus Transceiver, Storage, Three-State			
TTL-S	SN54S226	† TI	
	SN74S226	TI	
4-bit Parallel Bus Transceiver, Inverting Three-State			120
TTL-S	N8T26	AMD	
	S8T26	† AMD	
	N8T26A	AMD	
	S8T26A	† AMD	
	MB424	Fujitsu	
	HD268T26	Hitachi	
	MC8T26A	Motorola	
	DS8T26A	National	
	DS8T26AM	† National	
	N8T26A	Signetics	130
	S8T126	**† Signetics (2297)**	
	N8T127	**Signetics (2297)**	
	S8T127	**† Signetics (2297)**	

(Continued)

Miscellaneous (Cont'd.)

Function	Device	Source	Line
TTL-S		(Cont'd.)	
	N8T26	TI	
	SN75136	TI	
4-bit Parallel Bus Transceiver, Open Collector Drivers			
TTL-S	AM26S10C	AMD	
	AM26S10M	† AMD	
	AM26S11C	AMD	140
	AM26S11M	† AMD	
	AM26S12C	AMD	
	AM26S12M	† AMD	
	AM26S12AC	AMD	
	AM26S12AM	† AMD	
	9640C	Fairchild	
	9640M	† Fairchild	
	9641C	Fairchild	
	9641M	† Fairchild	
	MC26S10	Motorola	150
	MC26S11	Motorola	
	DM26S10C	National	
	DM26S10M	† National	
	DM26S11C	National	
	DM26S11M	† National	
	26S10C	Raytheon	
	26S10M	Raytheon	
	26S11C	Raytheon	
	26S11M	Raytheon	
	AM26S10C	† TI	160
	AM26S10M	† TI	
	AM26S11C	TI	
	AM26S11M	† TI	
8-bit Bidirection I/O Port			
TTL-S	**N8T31**	**Signetics (2290)**	
8-bit Bidirectional I/O Port, Latched, Addressable			
TTL-S	**N8T32**	**Signetics (2291)**	
	S8T32	**† Signetics (2291)**	
	N8T33	**Signetics (2291)**	
	S8T33	**† Signetics (2291)**	170
	N8T35	**Signetics (2291)**	
	S8T35	**† Signetics (2291)**	
	N8T36	**Signetics (2291)**	
	S8T36	**† Signetics (2291)**	
	N8T39	**Signetics (2292)**	
	S8T39	**† Signetics (2292)**	
Octal Bus Driver (Schmitt Trigger), Inverting, Three-State			
TTL-LS	AM25LS240C	AMD	
	AM25LS240M	† AMD	180
	SN54LS240	† AMD	
	SN74LS240	AMD	
	54LS240	† Fairchild	
	74LS240	Fairchild	
	54LS540	† Fairchild	
	74LS540	Fairchild	
	54LS240	**† MMI (768)**	
	74LS240	**MMI (768)**	
	57LS300	**† MMI (768)**	
	67LS300	**MMI (768)**	190
	57LS306	**† MMI (768)**	
	67LS306	**MMI (768)**	
	57LS307	**† MMI (768)**	
	67LS307	**MMI (768)**	
	SN54LS240	† Motorola	
	SN74LS240	Motorola	
	SN54LS540	† Motorola	
	SN74LS540	Motorola	
	9LS240C	**Raytheon (522)**	
	9LS240M	**† Raytheon (522)**	200
	25LS240C	**Raytheon (522)**	

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Values

Bold face indicates additional data is provided on the page noted.

DIGITAL–TTL (Cont'd)

Miscellaneous (Cont'd.)

Function	Device	Source		Line
TTL-LS			(Cont'd.)	
	25LS240M	**† Raytheon**	**(522)**	
	54LS240	**† Raytheon**	**(522)**	
	74LS240	**Raytheon**	**(522)**	
	74LS240	Signetics		
	SN54LS240	† TI		
	SN74LS240	TI		
TTL-S	SN54S240	† AMD		
	SN74S240	AMD		10
	54S240	**† MMI**	**(768)**	
	74S240	**MMI**	**(768)**	
	57S300	**† MMI**	**(768)**	
	67S300	**MMI**	**(768)**	
	57S306	**† MMI**	**(768)**	
	67S306	**MMI**	**(768)**	
	57S307	**† MMI**	**(768)**	
	67S307	**MMI**	**(768)**	
	SN54S240	† TI		
	SN74S240	TI		20
Octal Bus Driver (Schmitt Trigger), Inverting, Three-State, Symmetrical Controls				
TTL-LS	**57LS306**	**† MMI**	**(768)**	
	67LS306	**MMI**	**(768)**	
	57LS307	**† MMI**	**(768)**	
	67LS307	**MMI**	**(768)**	
TTL-S	**57S306**	**† MMI**	**(768)**	
	67S306	**MMI**	**(768)**	
	57S307	**† MMI**	**(768)**	
	67S307	**MMI**	**(768)**	30
Octal Bus Driver (Schmitt Trigger), Non-Inverting, Three-State, Symmetrical Controls				
TTL-LS	AM25LS241C	AMD		
	AM25LS241M	† AMD		
	SN54LS241	† AMD		
	SN74LS241	AMD		
	9LS241C	**Raytheon**	**(525)**	
	9LS241M	**† Raytheon**	**(525)**	
	54LS241	† Fairchild		
	74LS241	Fairchild		40
	54LS541	† Fairchild		
	74LS541	Fairchild		
	54LS241	**† MMI**	**(768)**	
	74LS241	**MMI**	**(768)**	
	57LS301	**† MMI**	**(768)**	
	67LS301	**MMI**	**(768)**	
	SN54LS241	† Motorola		
	SN74LS241	Motorola		
	SN54LS541	† Motorola		
	SN74LS541	Motorola		50
	25LS241C	**Raytheon**	**(525)**	
	25LS241M	**† Raytheon**	**(525)**	
	54LS241	**† Raytheon**	**(525)**	
	74LS241	**Raytheon**	**(525)**	
	74LS241	Signetics		
	SN54LS241	† TI		
	SN74LS241	TI		
TTL-S	SN54S241	† AMD		
	SN74S241	AMD		
	54S241	**† MMI**	**(768)**	60
	74S241	**MMI**	**(768)**	
	57S301	**† MMI**	**(768)**	
	67S301	**MMI**	**(768)**	
	SN54S241	† TI		
	SN74S241	TI		
Octal Bus Driver (Schmitt Trigger), Non-Inverting, Three-State, Complementary Controls				
TTL-LS	AM25LS244C	AMD		

(Continued)

Miscellaneous (Cont'd.)

Function	Device	Source		Line
TTL-LS			(Cont'd.)	70
	AM25LS244M	† AMD		
	SN54LS244	† AMD		
	SN74LS244	AMD		
	54LS244	† Fairchild		
	74LS244	Fairchild		
	54LS244	**† MMI**	**(768)**	
	74LS244	**MMI**	**(768)**	
	57LS304	**† MMI**	**(768)**	
	67LS304	**MMI**	**(768)**	
	SN54LS244	† Motorola		80
	SN74LS244	Motorola		
	9LS244C	**Raytheon**	**(525)**	
	9LS244M	**† Raytheon**	**(525)**	
	25LS244C	**Raytheon**	**(525)**	
	25LS244M	**† Raytheon**	**(525)**	
	54LS244	**† Raytheon**	**(525)**	
	74LS244	**Raytheon**	**(525)**	
	74LS244	Signetics		
	SN54LS244	† TI		
	SN74LS244	TI		90
TTL-S	SN54S244	† AMD		
	SN74S244	AMD		
	54S244	**† MMI**	**(768)**	
	74S244	**MMI**	**(768)**	
	57S304	**† MMI**	**(768)**	
	67S304	**MMI**	**(768)**	
Octal Bus Transceiver, Open Collector				
TTL-LS	SN54LS641	† Motorola		
	SN74LS641	Motorola		
	SN54LS642	† Motorola		100
	SN74LS642	Motorola		
	SN54LS641	† TI		
	SN74LS641	TI		
	SN74LS641-1	TI		
	SN54LS642	† TI		
	SN74LS642	TI		
	SN74LS642-1	TI		
	SN54LS644	† TI		
	SN74LS644	TI		
	SN74LS644-1	TI		110
Octal Bus Transceiver, Three-State				
TTL-LS	8304	AMD		
	SN54LS245	† AMD		
	SN74LS245	AMD		
	54LS245	† Fairchild		
	74LS245	Fairchild		
	54LS245	**† MMI**	**(774)**	
	74LS245	**MMI**	**(774)**	
	57LS305	**† MMI**	**(774)**	
	67LS305	**MMI**	**(774)**	120
	57LS310	**† MMI**	**(774)**	
	67LS310	**MMI**	**(674)**	
	SN54LS245	† Motorola		
	SN74LS245	Motorola		
	SN54LS640	† Motorola		
	SN74LS640	Motorola		
	SN54LS645	† Motorola		
	SN74LS645	Motorola		
	74LS245	Signetics		
	N8T125	Signetics		130
	SN54LS245	† TI		
	SN74LS245	TI		
	SN54LS640	† TI		
	SN74LS640	TI		
	SN74LS640-1	TI		
	SN54LS643	† TI		
	SN74LS643	TI		

(Continued)

Miscellaneous (Cont'd.)

Function	Device	Source		Line
TTL-LS			(Cont'd.)	
	SN74LS643-1	TI		
	SN54LS645	† TI		140
	SN74LS645	TI		
	SN74LS645-1	TI		
Pipeline I/O Port				
TTL-LS	**N8T40**	**Signetics**	**(2293)**	
Hex Current Sensing Interface Gate				
TTL-LS	SN54LS63	† TI		
	SN74LS63	TI		
Microprogram Sequencer				
TTL-LS	AM2909C	AMD		
	AM2909M	† AMD		150
	AM2911C	AMD		
	AM2911M	† AMD		
	F2909C	Fairchild		
	F2909M	† Fairchild		
	9419	Fairchild		
	F2911C	Fairchild		
	F2911M	† Fairchild		
	9421	Fairchild		
	3001	Intel		
	M3001	Intel		160
	MC2909C	Motorola		
	MC2909M	† Motorola		
	MC2911C	Motorola		
	MC2911M	† Motorola		
	IDM2909AC	National		
	IDM2909AM	† National		
	IDM2911AC	National		
	IDM2911AM	† National		
	µPB2909A	NEC Micro		
	µPB2911A	NEC Micro		170
	AM2909C	Raytheon		
	AM2909M	† Raytheon		
	AM2911C	Raytheon		
	AM2911M	† Raytheon		
	N8X02	**Signetics**	**(2280)**	
	N3001	Signetics		
	S3001	† Signetics		
Micro-Address Generator (for bit slice microprocessor)				
TTL-S	SN54S482	† TI		
	SN74S482	TI		180

† Military Temperature Range (−55° to 125°C)

* Typical Values

DIGITAL–Special

Other Digital Devices

Function	Device	Source	Line
Arithmetic Processor (supply 5-12v)	9511	AMD	
	9511-4	AMD	
Arithmetic Processor, 4 functions, ASCII Floating Point Computations (Supply 5v)	CY-450	Cybernetic	
Baud Rate Generator/Programmable Divider (ROM controlled divider)	MM5307	National	10
	COM5016	SMC	
	COM5016T	SMC	
Baud Rate Generator/Programmable Divider, Dual (ROM controlled divider)	COM5036	SMC	
	COM5036T	SMC	
	BR1941	Western	
Correlator (Continually compares two independently clocked serial inputs and gives correlation output)	TDC1004J	TRW	20
Custom Arrays (Digital and Linear circuits customized in final metalization)	**A100**	**Exar (932)**	
	B100	**Exar (932)**	
	C100	**Exar (932)**	
	D100	**Exar (932)**	
	F100	**Exar (932)**	
	XR-I²L-CHIP	Exar	30
	XR-CHIP	Exar	
	XR300	**Exar (932)**	
	XR400	**Exar (932)**	
	XR500	**Exar (932)**	
	ECL-Array	Fairchild	
	ULA	Ferranti	
	MONOCHIP	Interdesign	
	MCA	Interdesign	
	MCB	Interdesign	
	MCC	Interdesign	40
	MCD	Interdesign	
	MOA	Interdesign	
	MOB	Interdesign	
	MOC	Interdesign	
	MOD	Interdesign	
	MOE	Interdesign	
	MOF	Interdesign	
	MOG	Interdesign	
	MDA	Interdesign	
	MUA	Interdesign	50
	MASTERMOS	IMI	
	MM50	IMI	
	MM100	IMI	
	MM150	IMI	
	MM200	IMI	
	MM250	IMI	
	MM300	IMI	
	MM350	IMI	
	MM400	IMI	
	MM450	IMI	60
	MM500	IMI	
	MM550	IMI	
	OMNICHIP1	IMI	
	OMNICHIP2	IMI	
	ML50	Master Logic	
	ML75	Master Logic	
	ML100	Master Logic	
	ML150	Master Logic	
	ML200	Master Logic	
	ML350	Master Logic	70
	MCA	Master Logic	

(Continued)

Other Digital Devices (Cont'd.)

Function	Device	Source	Line
Custom Arrays (Digital and Linear circuits customized in final metalization) (Cont'd.)	MCB	Master Logic	
	MCC	Master Logic	
	MCD	Master Logic	
	MONOCHIP	Master Logic	
	MC606	Micro Tech	
	MC616	Micro Tech	
	MC626	Micro Tech	80
	MC636	Micro Tech	
	MC707	Micro Tech	
	MC717	Micro Tech	
	MC727	Micro Tech	
	MC737	Micro Tech	
	MASTERMOS	Monosil	
	XC160	Motorola	
	XC177	Motorola	
	XC400	Motorola	
	ECL-ARRAY	NEC America	90
Calculators: See Linear-Consumer			
Counters-See also CMOS and TTL-Counters			
Comparator/Mux, 6 Decade, 7 level, latched and multiplexed output (use with 6 decade counter)	**LS7240**	**LSI Comp (494)**	
Counter, 16-Bit, Non-Volatile Storage, Parallel Input/Output, 500KHz (Supply -29,5v)	NCR2900	NCR	
Counter, 3½-Digit, Programmable	TC9122	Toshiba	100
Counter, 32-bit, multiplexed and latched outputs (5 V supply)	**LS7060**	**LSI Comp (494)**	
Counter, 32-bit, 8-bit prescalable, multiplexed and latched outputs (5 V supply)	**LS7061**	**LSI Comp (494)**	
Counter, 4 Decade (Counts and stores, BCD Output, 0.5 MHz; supply -12,5v)	AY5-4057	GI	
4 Decade Up/Down Counter/Latch/Display Driver, Cascadable, Synchronous, Presettable, BCD output (versions have direct 7 segment and digit drivers for either common anode or cathode LEDs; either 9999 or 5959 count; 7217: hardwire control; 7227: processor control. 5 V supply)	ICM7217	Intersil	120
	ICM7217A	Intersil	
	ICM7217B	Intersil	
	ICM7217C	Intersil	
	ICM7227	Intersil	
	ICM7227A	Intersil	
	ICM7227B	Intersil	130
	ICM7227C	Intersil	
Counter/Clock, 4 Decade (supply -12V)	SAJ341	Siemens	
Counter/Display Decoder, 4 Decade (7 Segment and BCD outputs, 0.25 MHz; supply 5v)	MK5002	Mostek	
	MK5005	Mostek	
	MK5007	Mostek	
4 Decade Quad Counter, Up/Down, non-volatile storage (supply 5,-12 V)	MN9105	Plessey	140
Counter, 5 Decade (includes storage, multiplexed BCD output, 0.6 MHz, supply -12,5v)	3815	Fairchild	

Other Digital Devices (Cont'd.)

Function	Device	Source	Line
Dual Counter (two 3-decade up/down counters with latch, BCD output. 0.5 MHz., supply 5-15 v)	**LS7040**	**LSI Comp (494)**	
Counter/Display Driver, 1 Decade Up/Down, Preset (7 segment and BCD output, 1 MHz)	HCTR0107	Hughes	150
Counter/Display Driver, 4 Decade Up/Down (7 segment output, 0.6 M Hz, supply -12, 5v; BCD; and serial output versions available)	AY5-4007	GI	
	AY5-4007A	GI	
	AY5-4007D	GI	
Counter 6 Decade Up/Down (predetermining, latched output, 2 presettable compare registers)	**LS7050**	**LSI Comp (494)**	
Counter/Display Driver, 6 Decade Up/Down (7 segment and BCD output, 1 MHz, presettable compare register, latched output, LED drive maximum count 999999, 995959, or 595999 versions, supply 10-15 v)	MK50395	Mostek	160
	MK50396	Mostek	
	MK50397	Mostek	
	MK50398	Mostek	
	MK50399	Mostek	
Counter, 6 Decade, BCD output, 5 MHz, 8 latches (supply 5-15v)	**LS7031**	**LSI Comp (494)**	170
6 Decade Up/Down Counter/Display Driver, non-volatile storage, presettable (supply -8, 12V)	NC7102	Nitron	
7 Decade Counter/Latch/Display Driver (7 segment and digit drivers for common cathode LEDs, count 9,999,999; 2 MHz, 2-6 V supply)	ICM7208	Intersil	
8 Decade Up/Down Counter/Display Driver, non-volatile storage, presettable (supply -8, 12V)	NC7101	Nitron	180
Counter, 8 Decade, BCD and 7 segment outputs, 5 MHz, latches (supply 5-15v)	**LS7030**	**LSI Comp (494)**	
8 Decade Universal Counter/Latch/Display Driver (Direct 7 segment and digit drivers for common anode LEDs: 'A' types; Common cathode LEDs: 'B' types; 7216 hardwire controlled; 7226 processor controlled; DC to 10 MHZ, 5 V supply)	ICM7216A	Intersil	190
	ICM7216B	Intersil	
	ICM7226A	Intersil	
	ICM7226B	Intersil	
8 Decade Frequency Counter/Latch/Display Driver (Direct 7 segment and digit drivers for common anode LEDs: 7216C; common cathode LEDs: 7216D. DC to 10 MHz, 5 V supply)	ICM7216C	Intersil	
	ICM7216D	Intersil	200
Counter, 9 Decade Up/Down (count 99959599 or 999999999, latched output)	**LS7090**	**LSI Comp (494)**	
Counter Time-Base (Oscillator, programmable divider, 10^1 to 10^8, $2x10^7$, $6x10^7$, $6x10^8$ and $36x10^8$, (supply -12,5v)	MK5009	Mostek	
Dual Counter/Timer	MM5865	National	

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† Military Temperature Range (−55° to 125°C)

* Typical Values

Bold face indicates additional data is provided on the page noted.

DIGITAL–Special (Cont'd)

Other Digital Devices (Cont'd.)

Function	Device	Source	Line
Dual Counter/Timer		(Cont'd.)	
	DF215	Siliconix	
Down/Up Timer (0.1 and 1 second, Keyboard Entry)			
	DF216	Siliconix	
Elapsed Time Counter, 6 Decade (7 segment and digit drivers for common cathode LEDs; 0.01 s to 1 hr; 2-5 V supply)			
	ICM7205	Intersil	
	ICM7215	Intersil	
Elapsed Time Counter, 8 Decade (7 segment and digit drivers for common cathode LED; 0.01 s to 24 hrs; 2.5-4.5 V supply)			10
	ICM7045	Intersil	
Elapsed Time Counter, Decimal (7 segment and digit driver for common cathode LEDs; 2.5-4.5 V supply; 0.1 s to 10 hrs; count 2399999)			
	ICM7045A	Intersil	
Programmable Diode Matrix, 5x5			
	HM074	† Harris	
	HM075	† Harris	20
	HM076	† Harris	
Programmable Diode Matrix, 5x8			
	HM010	† Harris	
	HM012	† Harris	
	HM013	† Harris	
Programmable Diode Matrix, 8x5			
	HM080	† Harris	
	HM081	† Harris	
	HM084	† Harris	
Programmable Diode Matrix, 4x10			30
	HM090	† Harris	
	HM091	† Harris	
	HM093	† Harris	
	HM0110	Harris	
	HM0410	**Harris** (1406)	
Programmable Diode Matrix,10x4			
	HM050	† Harris	
	HM051	† Harris	
	HM055	† Harris	
	HM0104	**Harris** (1406)	40
Programmable Diode Matrix,6x8			
	HM030	† Harris	
	HM031	† Harris	
	HM034	† Harris	
	HM0168	**Harris** (1406)	
Programmable Diode Matrix, 8x6			
	HM040	† Harris	
	HM041	† Harris	
	HM044	† Harris	
	HM0186	**Harris** (1406)	50
Programmable Diode Matrix, 9x8			
	HM0198	**Harris** (1406)	
Programmable Diode Matrix, 18x5			
	M54510	Mitsubishi	
Programmable Diode Matrix, 10x16			
	S353	Siemens	
Divider, divide by 2, 525, supply -12v			
	MN115	Panasonic	
Divider, divide by 2, 625, supply -12v			
	MN116	Panasonic	60

Other Digital Devices (Cont'd.)

Function	Device	Source	Line
Programmable Divider (any modulo from 3 to 262,145, supply -12,5)			
	3816	Fairchild	
Programmable Divider (divide by 2 to 8191)			
	S0437	Siemens	
Programmable Divider, 22-stage			
	M54814	Mitsubishi	
Divider, divide by 1/10/100, to 150 MHZ			
	MSL2316	OKI	
Divider, divide by 2, 0.2 to 1 GHz			70
	MC1690	Motorola	
	SP1690B	Plessey	
	SP8602A	† Plessey	
	SP8602B	Plessey	
	SP8602M	Plessey	
	SP8603A	† Plessey	
	SP8603B	Plessey	
	SP8603M	Plessey	
	SP8604A	† Plessey	
	SP8604B	Plessey	80
	SP8604M	Plessey	
	SP8607A	† Plessey	
	SP8607B	Plessey	
	SP8607M	Plessey	
	SP8608B	Plessey	
	SP8608M	Plessey	
Divider, divide-by-2, above 1 GHz			
	SP8609B	Plessey	
	SP8609M	Plessey	
Divider, divide by 3/4, 40 to 300 MHz			90
	SP8720	Plessey	
Divider, divide by 4, 0.15 to 1 GHz			
	MC1697	Motorola	
	MC1699	Motorola	
	SP8600A	† Plessey	
	SP8600B	Plessey	
	SP8600M	Plessey	
	SP8601A	† Plessey	
	SP8601B	Plessey	
	SP8601M	Plessey	100
	SP8613B	Plessey	
	SP8613M	Plessey	
	SP8614B	Plessey	
	SP8614M	Plessey	
	SP8615B	Plessey	
	SP8615M	Plessey	
	SP8616B	Plessey	
Divider, divide by 4, above 1 GHz			
	11C05C	Fairchild	
	11C05M	† Fairchild	110
	SP8610	Plessey	
	SP8611B	Plessey	
	SP8611M	Plessey	
	SP8616B	Plessey	
	SP8617B	Plessey	
	SP8619B	Plessey	
Divider, divide by 4/8/32, 0.5 MHZ			
	M54812	Mitsubishi	
Divider, divide by 4/16/32, 0.5 MHZ			
	M54813	Mitsubishi	120
Divider, divide by 4/40/400, 0.5 MHZ			
	M54815	Mitsubishi	
Divider, divide by 5, 0.2 to 1 GHz			
	SP8620A	† Plessey	
	SP8620B	Plessey	

(Continued)

Other Digital Devices (Cont'd.)

Function	Device	Source	Line
Divider, divide by 5, 0.2 to 1 GHz		(Cont'd.)	
	SP8620M	Plessey	
	SP8621A	† Plessey	
	SP8621B	Plessey	
	SP8621M	Plessey	130
	SP8622B	Plessey	
	SP8622M	Plessey	
Divider, divide by 5/6, 0.2 to 1 GHz			
	11C91C	Fairchild	
	11C91M	† Fairchild	
	95H91C	Fairchild	
	MC12009	Motorola	
	MC12509	† Motorola	
	SP8740A	† Plessey	
	SP8740B	Plessey	140
	SP8740M	Plessey	
	SP8745A	† Plessey	
	SP8745B	Plessey	
	SP8745M	Plessey	
Divider, divide by 6/7, 0.2 to 1 GHz			
	SP8741A	† Plessey	
	SP8741B	Plessey	
	SP8741M	Plessey	
	SP8746A	† Plessey	
	SP8746B	Plessey	150
	SP8746M	Plessey	
Divider, divide by 8, 0.25 to 1 GHz			
	SP8670A	† Plessey	
	SP8670B	Plessey	
	SP8670M	Plessey	
	SP8671A	† Plessey	
	SP8671B	Plessey	
	SP8671M	Plessey	
	SP8672A	† Plessey	
	SP8672B	Plessey	160
	SP8672M	Plessey	
	SP8735B	Plessey	
	SP8736B	Plessey	
Divider, divide by 8, above 1 GHz			
	SP8675B	Plessey	
	SP8675M	Plessey	
	SP8676B	Plessey	
	SP8676M	Plessey	
	SP8677B	Plessey	
	SP8677M	Plessey	170
Divider, divide by 8/9, 0.25 to 1 GHz			
	MC12011	Motorola	
	MC12511	† Motorola	
	SP8743B	Plessey	
	SP8743M	Plessey	
	SP8748B	Plessey	
	SP8748M	Plessey	
Divider, divide by 10, 0.2 to 1 GHz			
	SP8505	Plessey	
	SP8515	Plessey	180
	SP8630A	† Plessey	
	SP8630B	Plessey	
	SP8630M	Plessey	
	SP8631A	† Plessey	
	SP8631B	Plessey	
	SP8631M	† Plessey	
	SP8632A	Plessey	
	SP8632B	Plessey	
	SP8632M	Plessey	
	SP8634B	Plessey	190
	SP8635B	Plessey	
	SP8636B	Plessey	

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Values

DIGITAL–Special (Cont'd)

Other Digital Devices (Cont'd.)

Divider, divide by 10, 0.2 to 1 GHz (Cont'd.)

Device	Source	
SP8637B	Plessey	
SP8660A	† Plessey	
SP8660B	Plessey	
SP8660M	Plessey	

Divider, divide by 10, above 1 GHz

Device	Source	
SP8665B	Plessey	
SP8666B	Plessey	
SP8667B	Plessey	

Divider, divide by 10/11, 0.2 to 1 GHz

Device	Source	
11C90C	Fairchild	
11C90M	† Fairchild	
95H90C	Fairchild	
95H90M	† Fairchild	
MC12013	Motorola	
MC12513	† Motorola	
SP8640A	† Plessey	
SP8640B	Plessey	
SP8640M	Plessey	
SP8641A	† Plessey	
SP8641B	Plessey	
SP8641M	Plessey	
SP8642A	† Plessey	
SP8642B	Plessey	
SP8642M	Plessey	
SP8643B	Plessey	
SP8643M	Plessey	
SP8646A	† Plessey	
SP8646B	Plessey	
SP8646M	Plessey	
SP8647A	† Plessey	
SP8647B	Plessey	
SP8647M	Plessey	
SP8680A	**† Plessey**	**(514)**
SP8680B	**Plessey**	**(514)**
SP8685A	† Plessey	
SP8685B	Plessey	
SP8685M	Plessey	
SP8690A	† Plessey	
SP8690B	Plessey	
SP8690M	Plessey	
SP8695A	† Plessey	
SP8695B	Plessey	
SP8695M	Plessey	

Divider, divide by 16, 0.2 to 1 GHz

Device	Source	
SP8650A	† Plessey	
SP8650B	Plessey	
SP8650M	Plessey	
SP8651A	† Plessey	
SP8651B	Plessey	
SP8651M	Plessey	
SP8652A	† Plessey	
SP8652B	Plessey	
SP8652M	Plessey	
SP8659A	† Plessey	
SP8659B	Plessey	
SP8659M	Plessey	

Divider, divide by 20, 0.2 to 1 GHz

Device	Source	
SP8657A	† Plessey	
SP8657B	Plessey	
SP8657M	Plessey	

Divider, divide by 20/22, above 1 GHz

Device	Source	
SP8785B	**Plessey**	**(518)**
SP8785M	**Plessey**	**(518)**
SP8786B	**Plessey**	**(518)**
SP8786M	**Plessey**	**(518)**

Other Digital Devices (Cont'd.)

Divider, divide by 32, 0.2 to 1 GHz

Device	Source	
SP8655A	† Plessey	
SP8655B	Plessey	
SP8655M	Plessey	

Divider, divide by 50/60/3000/3600, 2 MHZ

Device	Source	
M54810	Mitsubishi	

Divider, divide by 64, 0.08 to 1 GHz

Device	Source	
S0436	Siemens	

Divider, divide by 64, 0.2 to 1 GHz

Device	Source	
SP4020	Plessey	

Divider, divide by 64, above 1 GHz

Device	Source	
SP8750B	Plessey	
SP8750M	Plessey	
SP8751B	Plessey	
SP8751M	Plessey	
SP8752B	Plessey	

Divider, divide-by-80, to 150 MHz

Device	Source	
SP8627	Plessey	

Divider, divide by 100, to 150 MHz

Device	Source	
DS8629	National	
SP8627	Plessey	
SP8628	Plessey	
SP8629	Plessey	

Divider, divide by 256, 0.2 to 1GHZ

Device	Source	
SP4040	Plessey	

Divider, divide by 256, above 1 GHz

Device	Source	
SP8770B	Plessey	
SP8771B	Plessey	
SP8772B	Plessey	

Divider, divide-by-1000, 0-25 KHz (supply -15v)

Device	Source	
SAJ131	Siemens	
SAJ135	Siemens	

Divider, divide-by-1, 10, 100, 1000; 0-1 MHZ (supply -5 to -16v)

Device	Source	
SAJ141	Siemens	

Divider Extender, divide by 4, to extend division ratios of two modulus counters while maintaining the difference (ie 5/6 to 20/21)

Device	Source	
SP8790A	† Plessey	
SP8790B	Plessey	
SP8790M	Plessey	

Divider Extender, divide by 8 (ie extends 5/6 to 40/41)

Device	Source	
SP8794A	† Plessey	
SP8794B	Plessey	
SP8794M	Plessey	

DVM Logic, 3-1/2 Decade (for dual ramp integration DVM, BCD or 7 Segment Output; supply -12 to -18 or -18 to -24v)

Device	Source	
AY5-3507	GI	
AY5-3510	GI	

DVM Logic 3-3/4 Digit (ramp integration BCD or 7 segment output, supply -7.5,-15)

Device	Source	
AY5-3500	GI	

DVM Logic, 4 Digits (supply -17v)

Device	Source	
MN6032	Panasonic	

DVM Logic, 4-1/2 Digit, (dual slope integration, supply -15,5)

Device	Source	
ADB4500	National	

DVM Logic, 4-1/2 Decade (Multiplexed BCD output; supply -12,5v)

Device	Source	
3814C	Fairchild	

Other Digital Devices (Cont'd.)

DVM Logic, 4-3/4 Digit, (dual ramp integration, BCD and 7 segment output, supply 5v)

Device	Source	
AY3-3550	GI	

DVM Logic: See also Interface-Analog to Digital Converters, Decimal Output

Electronic Organ Circuits: See Linear-Consumer

Flip-Flop, D-Type Master-Slave (ECL or TTL supplies)

Device	Source	
11C70C	Fairchild	

Frequency Synthesizers: See Linear-Phase Locked Loop Circuits

Frequency to Voltage: See Linear-Other Devices

Gate, Dual OR/NOR (4-Input, 0.5 ns delay, ECL supply)

Device	Source	
SP16F60	Plessey	

Hall Effect Switch (senses magnetic field)

Device	Source	
DN830	Panasonic	
DM831	Panasonic	
DN834	Panasonic	
DN835	Panasonic	
DN837	Panasonic	
DN838	Panasonic	
DN839	Panasonic	
SAS201	Siemens	
SAS211	Siemens	
UGN-3019	Sprague	
UGS-3019	† Sprague	
UGN-3020	Sprague	
UGS-3020	† Sprague	
UGN-3201	Sprague	
UGN-3203	Sprague	
UGN-3501	Sprague	
TL170	TI	
TL172	TI	
TL175	TI	

Inverter, Triple PMOS

Device	Source	
LM8942	Sanyo	

Latch, Quad with non-volatile memory

Device	Source	
MN9102	**Plessey**	**(512)**

Latch/Drivers-See Interface-Memory and Peripheral Drivers

LED Driver System, 8 Decade, 8x8 memory, Decoder (versions either hardwire or processor controlled; versions have either common anode or common cathode LED 7 segment and digit drivers; 2-6 V supply)

Device	Source	
ICM7218A	Intersil	
ICM7218B	Intersil	
ICM7218C	Intersil	
ICM7218D	Intersil	
ICM7218E	Intersil	

Multiplexer/Demultiplexer, 8-channel latched, binary addressable(Supply -5 to -70v)

Device	Source	
LS7110	**LSI Comp**	**(494)**

Multivibrator, astable (programmable pulse width, current controlled pulse rep. rate, supply 3-7v)

Device	Source	
MC3380	Motorola	

PIN Diode Drivers

Device	Source	
DH0035	† National	
DH0035C	National	
UDS-5790	† Sprague	
UDS-5791	Sprague	

† Military Temperature Range (−55° to 125°C)

* Typical Values

Bold face indicates additional data is provided on the page noted.

DIGITAL–Special (Cont'd)

Function	Device	Source	Line
Other Digital Devices (Cont'd.)			
Pulse Group Encoder (2141) and Decoder (2151) for pulse width code systems (25^5 codes programmed by RC networks)			
	TMX2141	TMX	
	TMX2151	TMX	
Regulators, Switching: See Linear-Other Devices			
Schmitt Trigger, Complementary Open Collector Output (supply 2.2 to 6v)			
	ULN-3303	Sprague	
Schmitt Trigger (Supply 8 to 16v)			
	LB8015	Sanyo	
Schmitt Trigger, Programmable			
	CA3098	†RCA	10
	CA3099	†RCA	
Schmitt Trigger, Zener Clamped Output (supply 2.2 to 6v)			
	CS102	Cherry	
	ULN-3304	Sprague	
Schmitt Trigger, Dual, Complementary Open Collector Outputs (supply 2.2 to 6v)			
	CS122	Cherry	
	ULN-3305	Sprague	
Schmitt Trigger, Dual one Open Collector Output, one Zener Clamped Output (supply 2.2 to 6v)			20
	ULN-3306	Sprague	
Schmitt Trigger, Dual, Low voltage; 3.5v			
	SN76811	TI	
Sequential Boolean Analyzer, microprogrammable			
	SBA	GI	
Serial to Parallel Converter, 33-bits (shift register with output latch)			
	MM5559	National	
Shift Registers: See Memory-Shift Registers			30
Shift Register, 8-bit with 8 corresponding analog switches			
	SD5350	Signetics	
Timers: See Linear-Timers			
Voltage to Frequency: See Linear-Other Devices			
Watch Circuits-See Linear-Consumer Circuits			

† Military Temperature Range (−55° to 125°C)

* Typical Values

ABBREVIATIONS OF COMPANY NAMES

AD	Analog Devices
AMD	Advanced Micro Devices
AMI	American Microsystems, Inc.
Amperex	Amperex Electronics Corp.
Analogic	Analogic Corp.
Beckman	Beckman Instruments, Helipot Division
BEI	BEI Electronics
Burr-Brown	Burr-Brown Research
Cermetek	Cermetek
Cherry	Cherry Semiconductor
CMA	Consumer Microcircuits of America
Cybernetic	Cybernetic Micro Systems
Data General	Data General
Datel	Datel Systems
DDC	Data Devices Corp.
Delco	Delco Electronics
Dionics	Dionics Inc.
EA	Electronic Arrays
EMM/Semi	EMM Semi, Div. of Electronic Memories & Magnetics
Essex	Essex International
Exar	Exar Integrated Systems
Fairchild	Fairchild
Ferranti	Ferranti Electric
Fujitsu	Fujitsu
GI	General Instrument
Harris	Harris Semiconductor
Hitachi	Hitachi America Ltd.
Holt	Holt Inc.
Hughes	Hughes Aircraft Solid State Products
Hybrid Sys	Hybrid Systems
HyComp	HyComp
IMI	International Microcircuits, Inc.
Intech/FMI	Intech/Function Modules Inc.
Intel	Intel
Interdesign	Interdesign
Intersil	Intersil
IPI	Integrated Photomatrix, Inc.
Lambda	Lambda Electronics
LSI	LSI Computer Systems
Maruman	Maruman Integrated Circuits
Master Logic	Master Logic
Matrox	Matrox Electronics Systems
Micro Net	Micro Networks
Micropac	Micropac Industries
Micro Power	Micro Power Systems
Micro Tech	Microcircuits Technology
Mitel	Mitel Semiconductor
Mitsubishi	Mitsubishi Electric Co.
MMI	Monolithic Memories, Inc.
Monosil	Monosil
MOS	MOS Technology
Mostek	Mostek
Motorola	Motorola Semiconductor
National	National Semiconductor
NCR	NCR Corp., Microelectronics Division
NEC America	NEC America
NEC Micro	NEC Microcomputers
Nitron	Nitron
Nortec	Nortec Electronics
Novonics	Novonics
NPC	Nucleonic Products Co.
OEI	Optical Electronics, Inc.
OKI	OKI Semiconductor
Panasonic	Panasonic, Matsushita Electric Corp.
Photo Therm	Photo Therm
Plessey	Plessey Semiconductors
PMI	Precision Monolithics, Inc.
Raytheon	Raytheon Semiconductor
RCA	RCA Solid State Division
Reticon	Reticon
RIFA	RIFA
Rockwell	Rockwell Microelectronic Devices
RTC	Real Time Corp.
Sanken	Sanken Electric
Sanyo	Sanyo Electric
SGS	SGS-Ates Semiconductor
Siemens	Siemens
Signetics	Signetics (Philips)
Silicon G	Silicon General
Siliconix	Siliconix
Silicon Sys.	Silicon Systems, Inc.
Silitronics	Silitronics
SMC	Standard Microsystems
Solitron	Solitron Devices
Sprague	Sprague Electric Company
Supertex	Supertex, Inc.
SSM	Solid State Microtechnology for Music
SSS	Solid State Scientific
Synertek	Synertek
Telaris	Telaris
Teledyne C	Teledyne Crystalonics
Teledyne P	Teledyne Philbrick
Teledyne S	Teledyne Semiconductor
Telefunken	AEG-Telefunken
TI	Texas Instruments
TMX	TMX
Toshiba	Toshiba
Trans-Data	Trans-Data
TRW	TRW
Unitrode	Unitrode
Western	Western Digital
Zilog	Zilog

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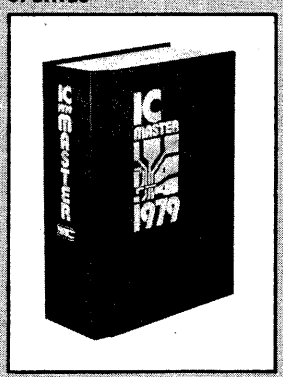
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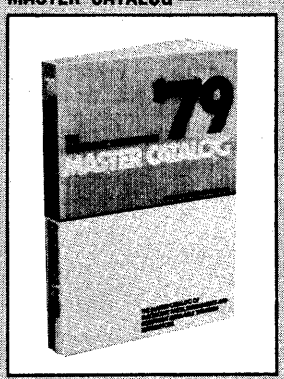
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Consumer Circuits

Part No.	Description	Digits	Power Supplies	Process	Packages
S1424A	Five Function LCD Watch with alternating time/date mode and voltage tripler display options	3½	+1.5V	CMOS	Die
S1424C	Five Function LCD Watch Circuit	3½	+1.5V	CMOS	Die
S1425A	Five Function LCD Watch Circuit	3½	+1.5V	CMOS	Chip Carrier
S1427A	Five Function LCD Watch Circuit	3½	+1.5V	CMOS	40 Pin DIP
S1856	Digital Clock Circuit — LED/Gas Discharge Auto Clock	3½	+6V to +16V	P-I^2	40 Pin DIP
S1998A	50/60Hz Line LED Clock Circuit	4	+8V to +26V	P-I^2	40 Pin DIP
S1998B	50/60Hz Line Clock — Gas Discharge	4	+8V to +33V	P-I^2	40 Pin DIP
S2709	Fluorescent Automotive Digital Clock	4	+12V	P-I^2	22 Pin Plastic
S2733	Six Function LCD Watch Circuit	4	+1.5V	CMOS	40 Pin Plastic

Organ Circuits

Part No.	Description	Process	Power Supplies	Power Dissipation	Packages
S10110	Analog Shift Register	P-I^2	-24V		8 Pin Plastic
S10111	Analog Shift Register	P-I^2	-24V		8 Pin Plastic
S10129	Six-Stage Frequency Divider	P-I^2	-14V, -27V	350mW	14 Pin Plastic
S10130	Six-Stage Frequency Divider	P-I^2	-14V, -27V	350mW	14 Pin Plastic
S10131	Six-Stage Frequency Divider	P-I^2	-14V, -27V	350mW	14 Pin Plastic
S10377	Analog Shift Register	P-I^2 MOS			8 Pin Package
S10430	Divider-Keyer	P-I^2 MOS			40 Pin Package
S2193	Seven-Stage Frequency Divider	P-I^2	-14V, -28V	300mW	14 Pin Plastic
S2567	Rhythm Counter	HI V_T	-15V, -27V	400mW	14 Pin Plastic
S8890	Rhythm Generator	P-I^2	-12V	400mW	40 Pin Plastic
S9660	Rhythm Generator	P-I^2	-12V	400mW	28 Pin Plastic
S50240	Top Octave Synthesizer	P-I^2	-11V, -16V	360mW	16 Pin Plastic
S50241	Top Octave Synthesizer	P-I^2	-11V, -16V	360mW	16 Pin Plastic
S50242	Top Octave Synthesizer	P-I^2	-11V, -16V	360mW	16 Pin Plastic
S50243	Top Octave Synthesizer	P-I^2	-11V, -16V	360mW	16 Pin Plastic
S50244	Top Octave Synthesizer	P-I^2	-11V, -16V	360mW	16 Pin Plastic
S50145	Top Octave Synthesizer	P-I^2	-11V, -16V	360mW	16 Pin Plastic

Remote Control Circuits

Part No.	Description	Process	Power Supplies	I/O Bits	Packages
S2600	Remote Control Transmitter	CMOS	+7V to +10V	11	16 Pin Plastic
S2601	Remote Control Receiver	P-I^2	+10V to +18V	5	22 Pin Plastic
S2742	Remote-Control Decoder	P-MOS	+9V		18 Pin Package
S2743	Remote-Control Encoder	P-MOS	+9V		16 Pin Package

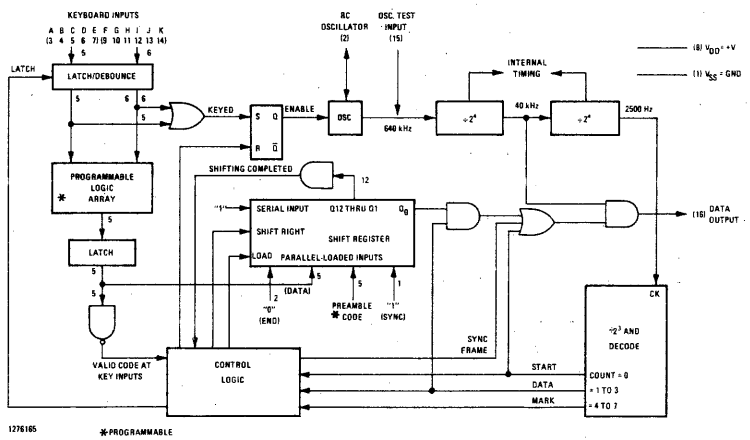
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ENCODER/DECODER REMOTE-CONTROL 2-CHIP SET

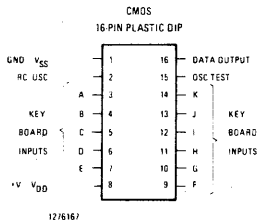
Features

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- ☐ Easily Used in LED, Ultrasonic, RF, or Hard-wire Transmission Schemes
- ☐ Very Low Reception Error
- ☐ Low Power Drain CMOS Transmitter for Portable and Battery Operation
- ☐ 31 Commands — 5-bit Output Bus with Data Valid
- ☐ 3 Analog (LP Filterable PWM) Outputs
- ☐ Muting (Analog Output Kill/Restore)
- ☐ Indexing Output — 2½ Hz Pulse Train
- ☐ Toggle Output (On/Off)
- ☐ Mask-Programmable Codes

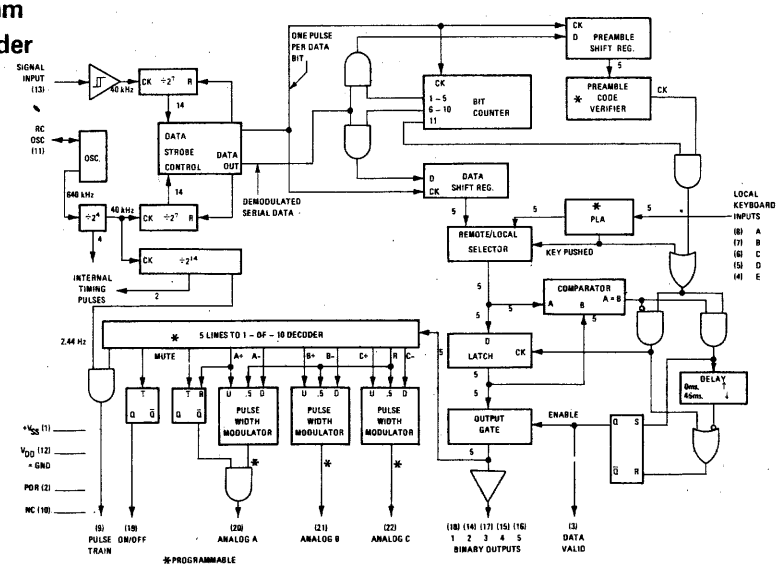
Block Diagram S2600 Encoder



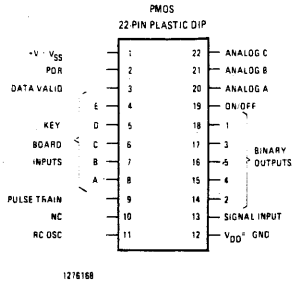
Pin Configuration S2600



Block Diagram S2601 Decoder



Pin Configuration S2601



Functional Description

The S2600/S2601 is a set of two LSI circuits which allows a complete system to be implemented for remote control of televisions, toys, security systems, industrial controls, etc. The choice of transmission medium is up to the user and can be ultrasonic, infrared radio frequency, or hardwire such as twisted pair or telephone.

The use of a synchronizing marker technique has eliminated the need for highly accurate frequencies generated by crystals. The S2600 Encoder typically generates a 40kHz carrier which it amplitude-modulates with a base-band message of 12 bits, each bit preceded by a synchronizing marker pulse.

Bits 1 and 12 denote sync and end-of-message, respectively, bits 2 thru 6 constitute a fixed preamble which must be received correctly for the command bits to be received, and bits 7 thru 11 contain the command data. The S2601 Decoder produces an output only after two complete, consecutive, identical, 12-bit transmissions. Marker pulses, preamble bits, and redundant transmissions, have given the S2600/S2601 system a very high immunity to noise, without a large number of discrete components.

S2600 Encoder

The S2600 is a CMOS device with an on-chip oscillator, 11 keyboard inputs, a keyboard encoder, a shift register, and some control logic. The oscillator requires only an external resistor and capacitor, and to conserve power, runs only during transmission. Keyboard inputs are active-low, and have internal pull-up resistors to V_{DD}. When one keyboard input from the group A thru E is activated with one from the group F thru K, the keyboard encoder generates a 5-bit code, as given in the table entitled ((S2600/S2601 CODING," below. This code is loaded into a shift register in parallel with the sync, preamble, and end bits, to form the 12-bit message.

The transmitter output is a 40 kHz square wave of 50% duty factor which has been pulse-code-modulated by (i.e., ANDed with) a signal having a recurring pattern, a bit frame of 3.2 millisecond duration. This bit frame is comprised of three signals: the Start signal which is 0.4 milliseconds of logic "1"; followed by the Data signal which is 1.2 milliseconds of the lowest-order shift register bit; followed by the Mark signal which is 1.6 milliseconds of logic "0" (except in the first bit frame where Mark = 1 to facilitate receiver synchronization).

The shift register is clocked once per bit frame, so that its 12-bit message is transmitted once in 38.4 milliseconds. The minimum number of tranmissions that can occur is two, but if the keyboard inputs are active after the first 3.6 milliseconds of any 12-bit transmission, one more 12-bit transmission will result. Transmissions are always complete, never truncated, regardless of the keyboard inputs.

The Test Input is used for functional testing of the device. A low level input will cause the oscillator frequency to be gated to the Data Output pin. This input has an internal pull-up resistor to V_{DD}.

S2601 Decoder

The S2601 is a PMOS LSI device with an on-chip oscillator, five keyboard inputs, a 40 kHz signal input, and 11 outputs. The oscillator requires only an external R and C. The five keyboard inputs are active-low with internal pull-up resistors to V_{SS}; activation of any two causes one of 10 possible 5-bit codes to be generated and fed to the outputs of the S2601, overriding any 40 kHz signal input.

Two counters, the signal counter and the local counter, are clocked respectively by the signal input and a 40 kHz signal from the local RC oscillator timing chain. A 40 kHz input lasting 3.2 milliseconds (i.e., an initial bit frame) causes the signal counter to overrun and reset both itself and the local counter. At specific intervals thereafter, the local counter generates pulses used to interrogate the contents of the signal counter. Resynchronization of the counters occurs every bit frame so that the interrogation yields valid data bits even if the transmitter oscillator frequency has deviated up to ± 24% with respect to the receiver oscillator frequency.

Decoded data bits from the next five bit frames following the initial synchronizing frame are compared with the fixed preamble code. The next five decoded bits, the command bits, are converted to a parallel format and are compared against the command bits saved from the prior transmission. If they match, and if the preamble bits are correct, the command bits are gated to the receiver outputs. However, a mismatch causes the receiver outputs to be immediately disabled, and the new command bits are saved for comparison against the command bits from the next 12-bit transmission. In the case where 2 identical, proper, 12-bit transmissions are immediately followed either by transmissions with erroneous preamble codes or by

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nothing, the receiver outputs will be activated during the end-frame of the second transmission, and will be disabled 45 milliseconds thereafter. In the rest (disabled) state the five Binary Outputs are at a "1" logic level; when not in the rest state, one or more of the open-sourced output transistors will conduct to V_{DD}. The Data Valid output is low during the rest state, and high whenever data is present at the Binary Outputs.

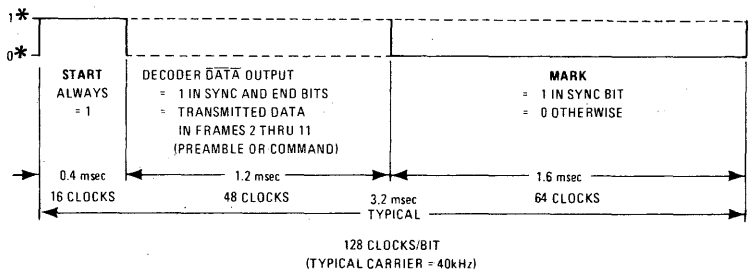
The S2601 has five other outputs: Pulse Train, On/Off, Analog A, Analog B, and Analog C. The states of these outputs are controlled by the 10 particular Binary Output codes which the receiver Keyboard Inputs can cause to be generated. The Pulse Train output provides a 2.44 Hz square wave (50% duty factor) whenever 11011 appears at the Binary Outputs, but otherwise it remains at a logic "0". This pulse train can be used for indexing, e.g., for stepping a TV channel selector.

The On/Off ("mains") output changes state each time 01111 appears at the Binary Outputs. In TV applications the On/Off output is most often used to kill and restore the main power supply.

Analog Outputs A, B, and C are 10 kHz pulse trains whose duty factors are independently controllable. With a simple low-pass filter each of these outputs can provide 64 distinct DC levels suitable for control of volume, color saturation, brightness, motor speed, etc. Each Analog Output increases its duty factor in response to a particular Binary Output code and decreases its duty factor in response to another code — 6 codes in all. The entire range of 0% to 100% duty factor can be traversed in 26 seconds or at a rate of the oscillator frequency divided by 262,144. All three Analog Outputs are set to 50% duty factor whenever 01011 appears at the Binary Outputs. Analog A is mutable; 01100 sets it to 0% duty factor. If 01100 then disappears and reappears, the original duty factor is restored. This of course implements the TV "sound killer" feature.

The S2601 has an on-chip power-on reset (POR) circuit which sets the Pulse Train and On/Off Outputs to "0," sets the Analog Outputs at 50% duty factor, and insures that Analog A is muted. No external components are required to implement POR, but a POR input has been provided for applications where externally controlled reset is desirable, e.g., where the power supply voltage rise time is extremely slow. The POR input has an internal resistor pull-up to V_{SS}; pulling it low causes a reset.

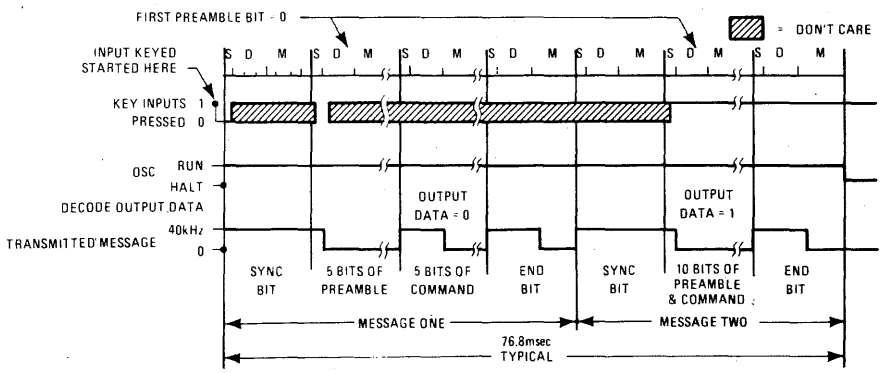
Message Bit Format



* "1" MEANS PRESENCE OF A 40kHz CARRIER (SQUARE WAVE); "0" MEANS ABSENCE OF A 40kHz CARRIER (SQUARE WAVE).

** IF MESSAGE BIT = "1" THEN DECODER DATA OUTPUT = ENCODER DATA INPUT = "0";
IF MESSAGE BIT = "0" THEN DECODER DATA OUTPUT = ENCODER DATA INPUT = "1".

Message Format



S2600/S2601 Coding

Transmitter Keyboard Input Pins Tied to V_{SS}	Receiver Keyboard Input Pins Tied to V_{DD} (See Note 1)	Resulting Receiver Binary Outputs 1	2	3	4	5	Receiver Dedicated Functions (Mask programmable except for rest state)
AB	–	0	0	0	0	0	
AF	–	0	0	0	0	1	
AG	–	0	0	0	1	0	
AH	–	0	0	0	1	1	
AI	BC	0	0	1	0	0	Increase Analog C pulse width
AJ	–	0	0	1	0	1	
AK	–	0	0	1	1	0	
BF	AE	0	0	1	1	1	Decrease Analog B pulse width
BG	–	0	1	0	0	0	
BH	–	0	1	0	0	1	
BI	–	0	1	0	1	0	
BJ	DE	0	1	0	1	1	RESET Analog (See Note 2)
BK	CE	0	1	1	0	0	MUTE (See Note 3)
CF	–	0	1	1	0	1	
CG	–	0	1	1	1	0	
CH	CD	0	1	1	1	1	Toggle On/Off Output
CI	–	1	0	0	0	0	
CJ	–	1	0	0	0	1	
CK	–	1	0	0	1	0	
DF	AD	1	0	0	1	1	Increase Analog B pulse width
DG	BD	1	0	1	0	0	Decrease Analog C pulse width
DH	–	1	0	1	0	1	
DI	–	1	0	1	1	0	
DJ	AB	1	0	1	1	1	Increase Analog A pulse width
DK	–	1	1	0	0	0	
EF	–	1	1	0	0	1	
EG	–	1	1	0	1	0	
EH	BE	1	1	0	1	1	Activate Pulse Train Output
EI	–	1	1	1	0	0	
EJ	–	1	1	1	0	1	
EK	AC	1	1	1	1	0	Decrease Analog A pulse width
–	–	1	1	1	1	1	Rest State

NOTES:
1. Receiver keyboard inputs override any remote signal input.
2. Sets Analog A, B, and C waveforms to 50% Duty Factor.
3. First operation sets Analog A to 0% Duty Factor; second operation restores former Analog A Duty Factor.

Electrical Specifications – 2600 Encoder

All voltages measured with respect to V_{SS}.

Absolute Maximum Ratings

Operating ambient temperature T_A ..... 0 to +70°C
Storage temperature ..... −65°C to +150°C
Positive voltage on any pin ..... +14V
Negative voltage on any pin ..... −0.3V

Electrical Characteristics

Unless otherwise noted, V_{DD} = 8.5 ± 1.5V and T_A = 0 to +70°C.

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
f0	Oscillator frequency	7	640	2000	kHz	R_{OSC} = 12K, C_{OSC} = 100pF
Δf0/f0	Frequency deviation	−10		+10	%	Fixed R_{OSC}, C_{OSC}, V_{DD} ± 10%
I_{DD}	Supply current			2	mA	During transmission, Data Output = 1mA
	Standby			10	μA	No transmission (25°C)
V_{IH}	Input "1" threshold	25	50		%V_{DD}	
V_{IL}	Input "0" threshold		50	75	%V_{DD}	
I_{IL}	Input source currrent	50		200	μA	V_I = 0V
I_{OH}	Output source current	1	1.5		mA	V_0 = V_{DD} − 3V
I_{OL}	Output sink current	−.2	−.5		mA	V_0 = +0.5V

Note: Circuit operates with V_{DD} from 3.0V to 12.0V.

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ENCODER/DECODER REMOTE-CONTROL 2-CHIP SET

Features

- ☐ **Lower System Costs**
  - **RC oscillator used on encoder (no crystal required)**
  - **Phase-locked-loop on decoder (no crystal required)**
  - **Single binary inputs allow inexpensive switches on pc board jumpers**
- ☐ **Flexibility of Application**
  - **512 user selectable address codes**
  - **Decoder signal valid output**
  - **Externally selectable one-shot tailors message reception**
  - **User has choice of transmission media: infrared, ultrasonic, RF, or hardware**
  - **Eight ROM programmable preamble codes**
  - **Encoder operates on a single 9V battery**
- ☐ **Reliable System Operation**
  - **Frequency shift keying scheme means low reception error**
  - **PLL allows frequency variation ± 15% between encoder and decoder**
  - **One-shot period allows adjustment for system noise**
  - **Triple message redundancy required**
  - **Preamble adds to message security**
  - **High noise immunity**

General Description

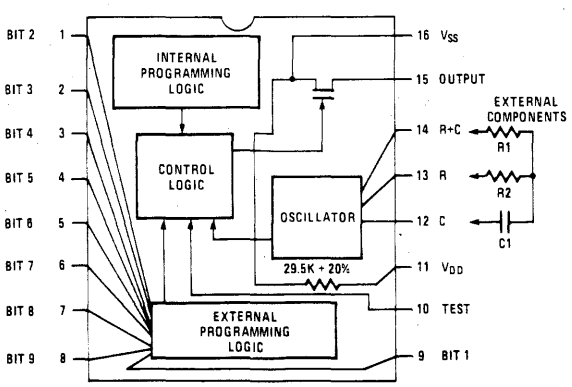
Encoder/Decoder

This two chip PMOS set includes a user programmable serial data encoder for use in a simple low power transmitter and a serial data decoder for use in a user addressable receiver. The user can select the transmission medium (RF, infrared ultrasonic, or hard wired). The externally selectable message allows up to 512 codes or addresses; this is done with the nine binary inputs on each device. An additional 3 bits of address can be programmed on chip as a fixed preamble.

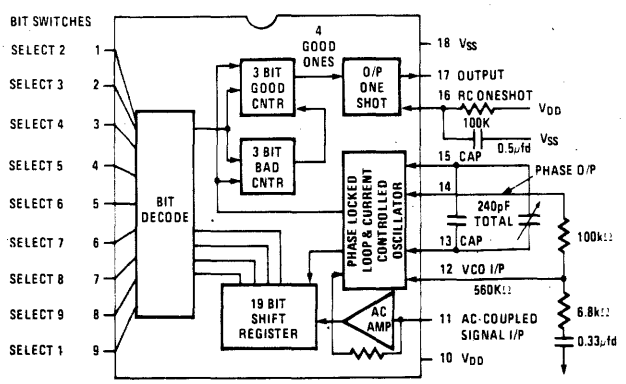
The serial data encoder encodes by means of a frequency-shift-keyed trinary data pattern composed of 16 data bits. Each data bit will have a length equivalent to 32 cycles of high frequency clock (20kHz typical). Each trinary data pattern will be 512 cycles of 1/2 the oscillator frequency length. The encoder frequency oscillator reference is controlled with an external RC network. The encoder transmitter can be powered by a single 9 volt battery so that a single momentary push button will activate the encoder and transmitter. In the off position there is no current flow.

The serial data decoder in conjunction with a receiver amplifier decodes the transmitted 16 bit coded signal. The on-chip phase-locked-loop locks in on the 20kHz signal even if the transmitted frequency differs from the receiver by up to ± 15%. The coded signal input is

S2743 Serial Data Encoder Block Diagram and Pin Configuration



S2742 Serial Data Decoder Block Diagram and Pin Configuration



ADVANCED PRODUCT DESCRIPTION

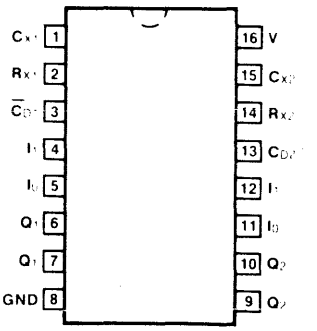
96S02
96LS02

DUAL RETRIGGERABLE RESETTABLE MONOSTABLE MULTIVIBRATOR

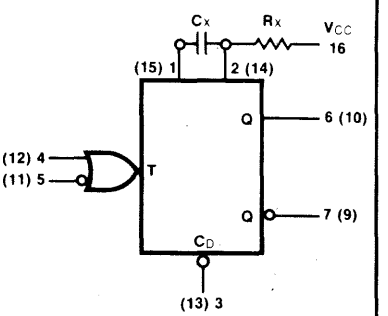
DESCRIPTION — The 96S02 and 96LS02 are dual retriggerable and resettable monostable multivibrators. These one-shots provide exceptionally wide delay range, pulse width stability, predictable accuracy and immunity to noise. The pulse width is set by an external resistor and capacitor. Resistor values up to 1.0 MΩ for the 96LS02 and 2.0 MΩ for the 96S02 reduce required capacitor values. Hysteresis is provided on both trigger inputs of the 96LS02 and on the positive trigger input of the 96S02 for increased noise immunity.

- **REQUIRED TIMING CAPACITANCE REDUCED BY FACTORS OF 10 TO 100 OVER CONVENTIONAL DESIGNS**
- **BROAD TIMING RESISTOR RANGE — 1.0 kΩ to 2.0 MΩ**
- **OUTPUT PULSE WIDTH IS VARIABLE OVER A 2000:1 RANGE BY RESISTOR CONTROL**
- **PROPAGATION DELAY OF 35 ns 96LS02, 12 ns 96S02**
- **0.3 V HYSTERESIS ON TRIGGER INPUTS**
- **OUTPUT PULSE WIDTH INDEPENDENT OF DUTY CYCLE**
- **35 ns TO ∞ OUTPUT PULSE WIDTH RANGE**

CONNECTION DIAGRAM
PINOUT A



LOGIC SYMBOL



VCC = Pin 16
GND = Pin 8

ORDERING CODE: See Section 9

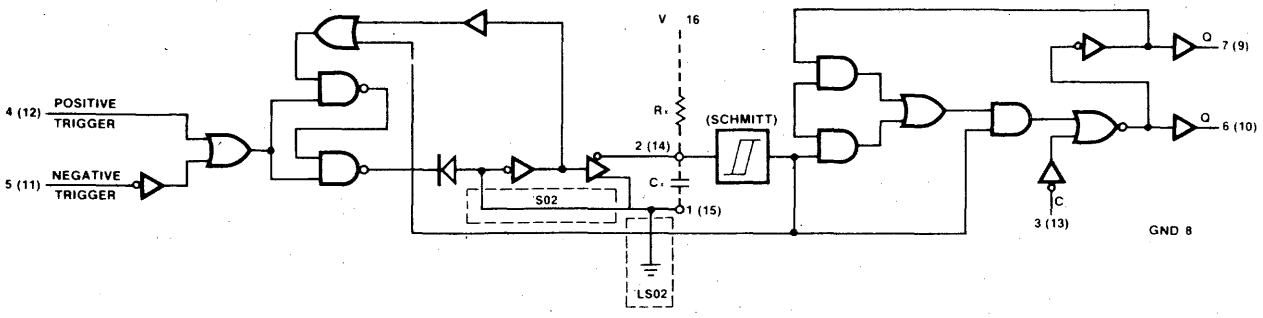
PKGS	PIN OUT	COMMERCIAL GRADE	MILITARY GRADE	PKG TYPE
		VCC = +5.0 V ±5%, TA = 0°C to +70°C	VCC = +5.0 V ±10%, TA = -55°C to +125°C	
Plastic DIP (P)	A	96S02PC, 96LS02PC		9B
Ceramic DIP (D)	A	96S02DC, 96LS02DC	96S02DM, 96LS02DM	6B
Flatpak (F)	A	96S02FC, 96LS02FC	96S02FM, 96LS02FM	4L

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	96S (U.L.) HIGH/LOW	96LS (U.L.) HIGH/LOW
$\overline{I}_0$	Trigger Input (Active Falling Edge)	0.5/0.625	
$\overline{I}_0$	Schmitt Trigger Input (Active Falling Edge)		0.5/0.25
I_1	Schmitt Trigger Input (Active Rising Edge)	0.5/0.625	0.5/0.25
$\overline{C}_D$	Direct Clear Input (Active LOW)	0.5/0.625	0.5/0.25
Q	True Pulse Output	25/12.5	10/5.0 (2.5)
$\overline{Q}$	Complementary Pulse Output	25/12.5	10/5.0 (2.5)

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LOGIC DIAGRAM

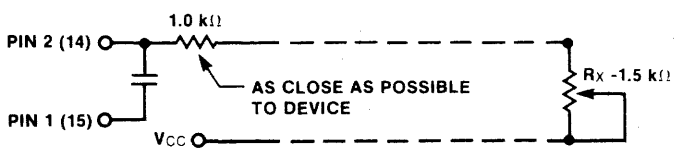


FUNCTIONAL DESCRIPTION — The 96S02 and 96LS02 dual retriggerable resettable monostable multivibrators have two dc coupled trigger inputs per function, one active LOW ($\overline{I_0}$) and one active HIGH (I_1). The I_1 input of both circuit types and the $\overline{I_0}$ input of the 96LS02 utilize an internal Schmitt trigger with hysteresis of 0.3 V to provide increased noise immunity. The use of active HIGH and LOW inputs allows either rising or falling edge triggering and optional non-retriggerable operation. The inputs are dc coupled making triggering independent of input transition times. When input conditions for triggering are met the Q output goes HIGH and the external capacitor is rapidly discharged and then allowed to recharge. An input trigger which occurs during the timing cycle will retrigger the circuit and result in Q remaining HIGH. The output pulse may be terminated (Q to the LOW state) at any time by setting the Direct Clear input LOW. Retriggering may be inhibited by tying the $\overline{Q}$ output to $\overline{I_0}$ or the Q output to I_1. Differential sensing techniques are used to obtain excellent stability over temperature and power supply variations and a feedback Darlington capacitor discharge circuit minimizes pulse width variation from unit to unit. Schottky TTL output stages provide high switching speeds and output compatibility with all TTL logic families.

Operation Notes

TIMING

1. An external resistor (R_X) and an external capacitor (C_X) are required as shown in the Logic Diagram. The value of R_X may vary from 1.0 kΩ to 1.0 MΩ (96LS02) or 2.0 MΩ (96S02).
2. The value of C_X may vary from 0 to any necessary value available. If, however, the capacitor has significant leakage relative to V_{CC}/R_X the timing equations may not represent the pulse width obtained.
3. Polarized capacitors may be used directly. The (+) terminal of a polarized capacitor is connected to pin 1 (15), the (-) terminal to pin 2 (14) and R_X. Pin 1 (15) will remain positive with respect to pin 2 (14) during the timing cycle. In the 96S02, however, during quiescent (non-triggered) conditions, pin 1 (15) may go negative with respect to pin 2 (14) depending on values of R_X and V_{CC}. For values of $R_X \geq 10$ kΩ the maximum amount of capacitor reverse polarity, pin 1 (15) negative with respect to pin 2 (14) is 500 mV. Most tantalum electrolytic capacitors are rated for safe reverse bias operation up to 5% of their working forward voltage rating; therefore, capacitors having a rating of 10 WVdc or higher should be used with the 96S02 when $R_X \geq 10$ kΩ.
4. The output pulse width t_w for $R_X \geq 10$ kΩ and $C_X \geq 1000$ pF is determined as follows:
   (96S02) $t_w = 0.55\ R_X C_X$
   (96LS02) $t_w = 0.43\ R_X C_X$
   Where R_X is in kΩ, C_X is in pF, t is in ns *or* R_X is in kΩ, C_X is in μF, t is in ms.
5. The output pulse width for $R_X < 10$ kΩ or $C_X < 1000$ pF should be determined from pulse width versus C_X or R_X graphs.
6. To obtain variable pulse width by remote trimming, the following circuit is recommended:



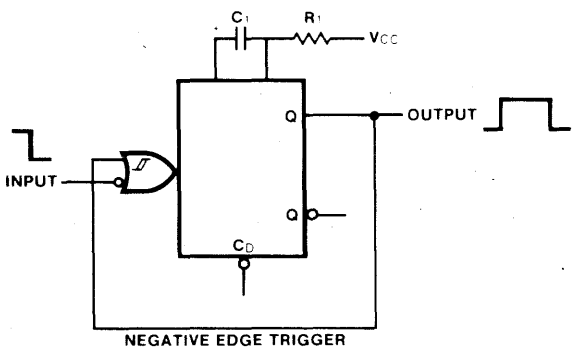
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Operation Notes (Cont'd)

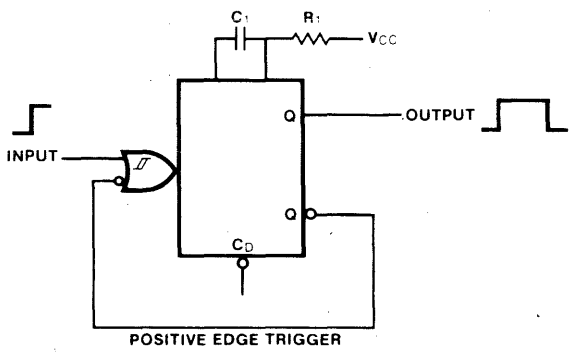
7. Under any operating condition, C_X and R_X (Min) must be kept as close to the circuit as possible to minimize stray capacitance and reduce noise pickup.
8. V_{CC} and ground wiring should conform to good high frequency standards so that switching transients on V_{CC} and ground leads do not cause interaction between one shots. Use of a 0.01 μF to 0.1 μF bypass capacitor between V_{CC} and ground located near the circuit is recommended.

TRIGGERING

1. The minimum negative pulse width into $\overline{I}_0$ is 8.0 ns; the minimum positive pulse width into I_1 is 12 ns.
2. Input signals to the 96S02 exhibiting slow or noisy transitions should use the positive trigger input I_1 which contains a Schmitt trigger. Input signals to the 96LS02 exhibiting slow or noisy transitions can use either trigger as both are Schmitt triggers.
3. When non-retriggerable operation is required, i.e., when input triggers are to be ignored during quasi-stable state, input latching is used to inhibit retriggering.



NEGATIVE EDGE TRIGGER



POSITIVE EDGE TRIGGER

4. An overriding active LOW level direct clear is provided on each multivibrator. By applying a LOW to the clear, any timing cycle can be terminated or any new cycle inhibited until the LOW reset input is removed. Trigger inputs will not produce spikes in the output when the reset is held LOW. A LOW-to-HIGH transition on $\overline{C}_D$ will not trigger the 96S02 or 96LS02. If the $\overline{C}_D$ input goes HIGH coincident with a trigger transition, the circuit will respond to the trigger.

TRIGGERING TRUTH TABLE

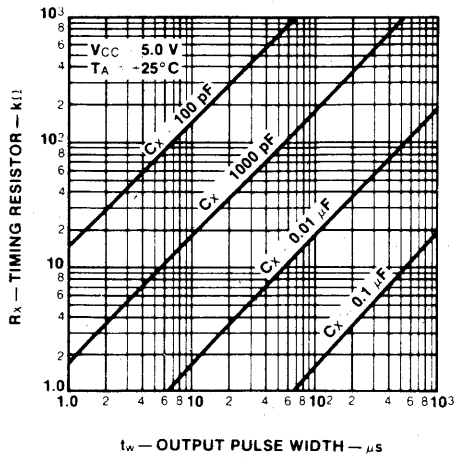
PIN NO'S. 5 (11)	4 (12)	3 (13)	OPERATION
H→L	L	H	Trigger
H	L→H	H	Trigger
X	X	L	Reset

H = HIGH Voltage Level ≥ V_{IH}
L = LOW Voltage Level ≤ V_{IL}
X = Immaterial (either H or L)
H→L = HIGH to LOW Voltage Level transition
L→H = LOW to HIGH Voltage Level transition

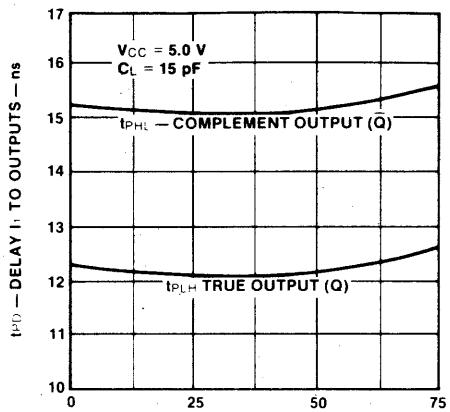
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TYPICAL CHARACTERISTICS
96S02

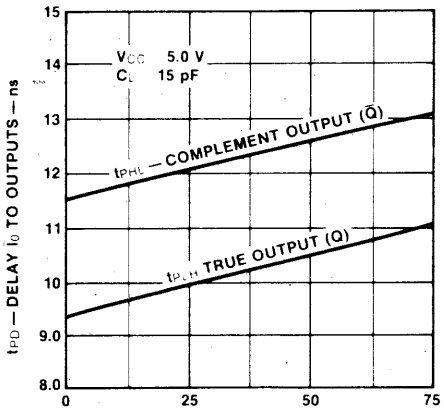
OUTPUT t_w vs R_X and C_X



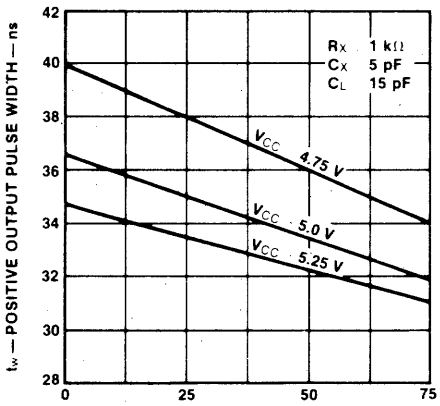
I_1 DELAY TIME vs T_A



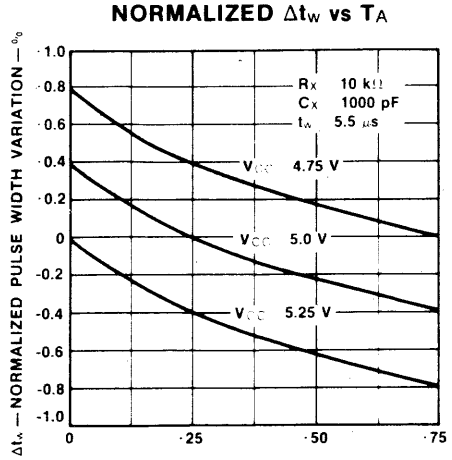
$\overline{I}_0$ DELAY TIME vs T_A



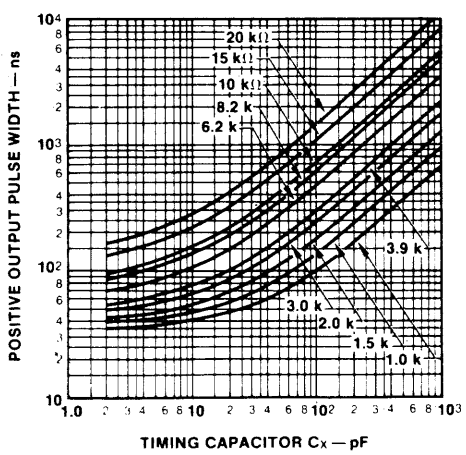
OUTPUT t_w vs T_A



NORMALIZED Δt_w vs T_A



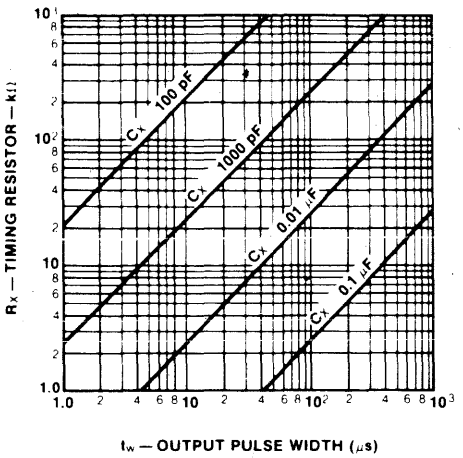
PULSE WIDTH vs R_XC_X



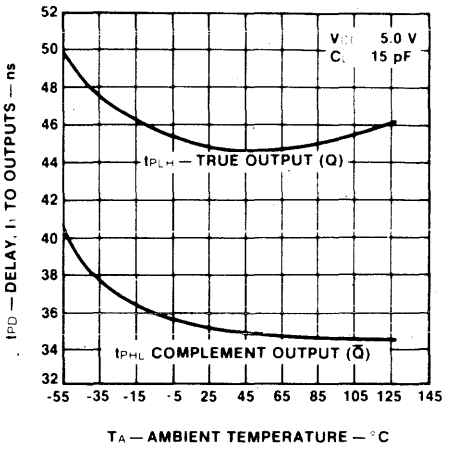
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TYPICAL CHARACTERISTICS
96LS02

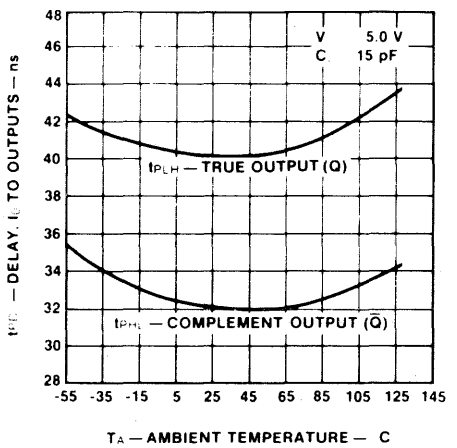
OUTPUT t_W vs R_X and C_X



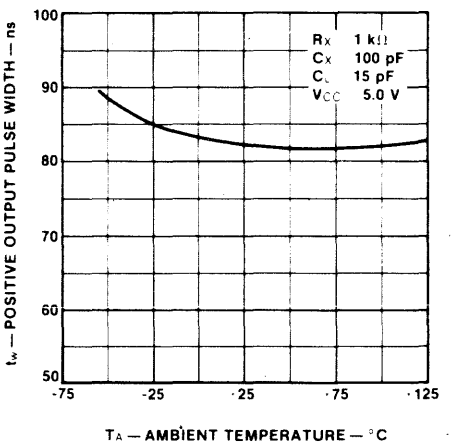
I_1 DELAY TIME vs T_A



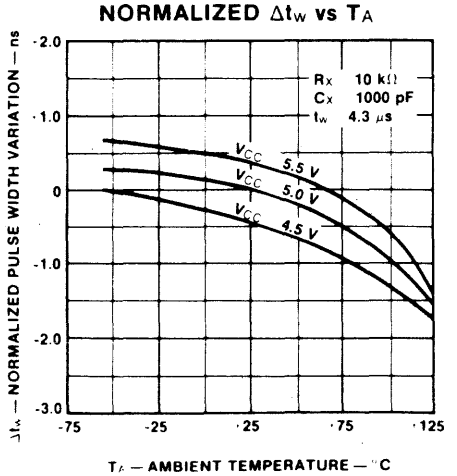
$\bar{I}_0$ DELAY TIME vs T_A



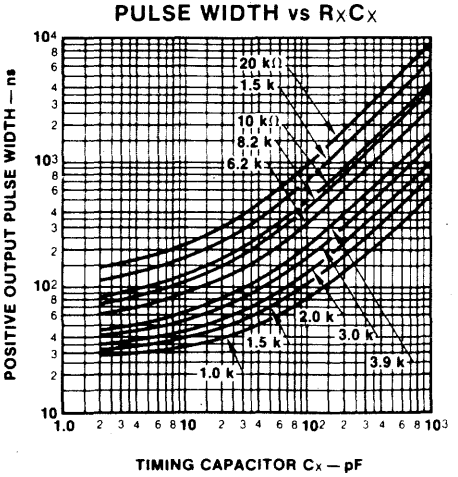
OUTPUT t_W vs T_A



NORMALIZED Δt_W vs T_A



PULSE WIDTH vs R_XC_X



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DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		96S Min	96S Max	96LS Min	96LS Max	UNITS	CONDITIONS
V_{T+}	Positive-going Threshold Voltage, $\overline{I_0}$, I_1 (96LS02) I_1 (96S02)			2.0		2.0	V	V_{CC} = 5.0 V
V_{T-}	Negative-going Threshold Voltage $\overline{I_0}$, I_1 (96LS02) I_1 (96S02)	XM XC	0.8 0.8		0.7 0.8		V	V_{CC} = 5.0 V
V_{OH}	Output HIGH Voltage	XM XC	2.7 2.7		2.5 2.7		V	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL} I_{OH} = -400 μA ('LS02) I_{OH} = -1.0 mA ('S02)
V_{OL}	Output LOW Voltage	XM XC		0.5 0.5		0.5 0.4	V	V_{CC} = Min, V_{IN} = V_{IH} or V_{IL}
V_{CX}	Capacitor Voltage Pin 1 (15) Referenced to Pin 2 (14)		-0.85 -0.5 -0.4	3.0 3.0 3.0	0 0 0	3.0 3.0 3.0	V	R_X = 1.0 kΩ R_X = > 10 kΩ R_X > 1.0 MΩ V_{CC} = 4.75 V to 5.25 V
I_{IH}	Input HIGH Current			20 0.1		20 0.1	μA mA	V_{IN} = 2.7 V V_{IN} = 5.5 V ('S02) V_{IN} = 10 V ('LS02) V_{CC} = Max
I_{IL}	Input LOW Current			-1.0		-0.4	mA	V_{IN} = 0.4 V, V_{CC} = Max
I_{OS}	Output Short Circuit Current		-40	-100	-20	-100	mA	V_{CC} = Max, V_{OUT} = 0 V
I_{CC}	Power Supply Current			75		36	mA	V_{IN} = Open, V_{CC} = Max

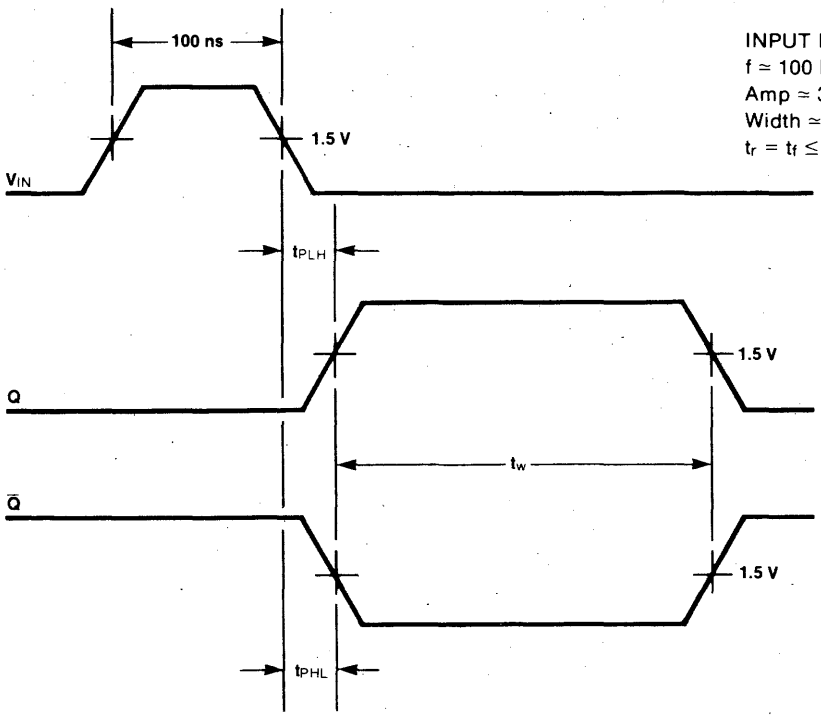


Fig. a

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FAIRCHILD • 96S02 • 96LS02

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25°C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER		96S C_L = 15 pF Min	96S C_L = 15 pF Max	96LS C_L = 15 pF Min	96LS C_L = 15 pF Max	UNITS	CONDITIONS
t_{PLH}	Propagation Delay $\overline{I_0}$ to Q			15		55	ns	Fig. a
t_{PHL}	Propagation Delay $\overline{I_0}$ to $\overline{Q}$			19		50	ns	
t_{PLH}	Propagation Delay I_1 to Q			19		60	ns	
t_{PHL}	Propagation Delay I_1 to $\overline{Q}$			20		55	ns	
t_{PHL}	Propagation Delay $\overline{C_D}$ to Q			20		30	ns	
t_{PLH}	Propagation Delay $\overline{C_D}$ to $\overline{Q}$			14		35	ns	
t_w (L)	$\overline{I_0}$ Pulse Width LOW		8.0		15		ns	
t_w (H)	I_1 Pulse Width HIGH		12		30		ns	
t_w (L)	$\overline{C_D}$ Pulse Width LOW		7.0		22		ns	
t_w (H)	Minimum Q Pulse Width HIGH		30	45	25	55	ns	R_X = 1.0 kΩ, C_X = 10 pF including jig and stray
t_w	Q Pulse Width		5.2	5.8	4.1	4.5	μs	R_X = 10 kΩ, C_X = 1000 pF
R_X	Timing Resistor Range		1.0	2000	1.0	1000	kΩ	T_A = -55°C to +125°C, V_{CC} = 4.5 V to 5.5 V
t	Change in Q Pulse Width over Temperature	XM				3.0	%	R_X = 10 kΩ, C_X = 1000 pF
		XC		1.0		1.0		
t	Change in Q Pulse Width over V_{CC} Range			1.0		0.8	%	T_A = 25°C, V_{CC} = 4.75 V to 5.25 V, R_X = 10 kΩ, C_X = 1000 pF
						1.5		T_A = 25°C, V_{CC} = 4.5 V to 5.5 V, R_X = 10 kΩ, C_X = 1000 pF

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96LS32

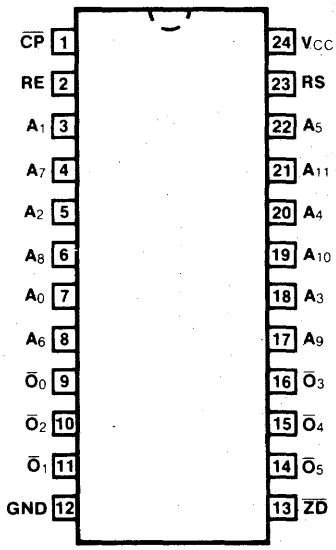
ADDRESS MULTIPLEXER/REFRESH COUNTER

(For 4K Dynamic RAMs)

DESCRIPTION — The 96LS32 is an address multiplexer and refresh counter for multiplexed address dynamic RAMs requiring refresh of up to six input addresses (or 4K bits for 64 x 64 organization). It multiplexes 12 bits of system applied address to six output address pins. The device also contains a 6-bit refresh counter which is externally clocked so that either distributed or burst refresh may be used. The high performance of the 96LS32 makes it especially suitable for use with high speed n-channel RAMs like the M4027. The 96LS32 operates from a single +5.0 V power supply and is specified for operation over a 0°C to +75°C ambient temperature range.

- **SIMPLIFIES SYSTEM DESIGN**
- **REDUCES PACKAGE COUNT**
- **DRIVES HIGH CAPACITANCE LOADS**
- **USE FOR DISTRIBUTED OR BURST REFRESH**
- **STANDARD 24-PIN DUAL IN-LINE PACKAGE**
- **LOW POWER SCHOTTKY DESIGN MINIMIZES POWER CONSUMPTION**

CONNECTION DIAGRAM
PINOUT A



ORDERING CODE: See Section 9

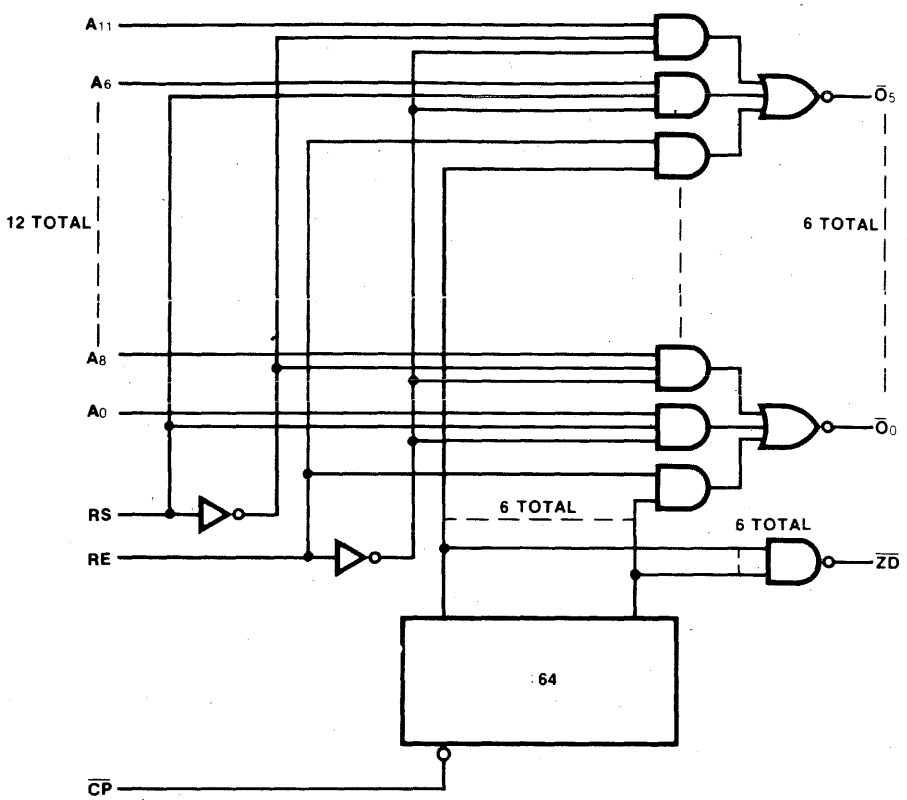
PKGS	PIN OUT	COMMERCIAL GRADE	MILITARY GRADE	PKG TYPE
		V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	
Plastic DIP (P)	A	96LS32PC		9N
Ceramic DIP (D)	A	96LS32DC	96LS32DM	6N
Flatpak (F)	A	96LS32FC	96LS32FM	4M

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

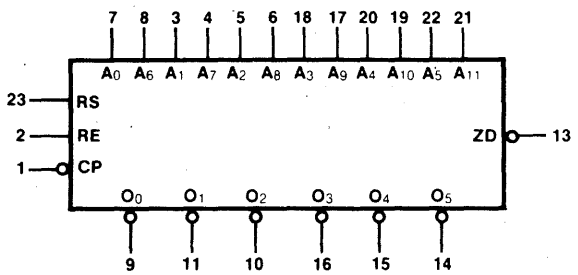
PIN NAMES	DESCRIPTION	96XX (U.L.) HIGH/LOW
$A_0 - A_5$	Row Address Inputs	0.5/0.13
$A_6 - A_{11}$	Column Address Inputs	0.5/0.13
$\overline{CP}$	Clock Pulse Input (Active Falling Edge)	0.5/0.13
RE	Refresh Enable Input (Active HIGH)	0.5/0.13
RS	Row Select Input (Active HIGH)	0.5/0.13
$\overline{ZD}$	Refresh Counter Zero Detect Output (Active LOW)	25/3.1
$\overline{O}_0 - \overline{O}_5$	Address Outputs	25/3.1

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LOGIC DIAGRAM



LOGIC SYMBOL



V_{CC} = Pin 24
GND = Pin 12

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FUNCTIONAL DESCRIPTION — The 96LS32 address multiplexer/refresh counter performs the following functions:

1. Row, Column and Refresh Address multiplexing
2. Address counting for burst or distributed refresh

These functions are controlled by two signals, Refresh Enable and Row Select, both of which are active HIGH TTL inputs. the Function Table shows the levels required to multiplex to the output:

1. Refresh address (from internal counter)
2. Row addresses (A_0 through A_5)
3. Column addresses (A_6 through A_{11})

BURST REFRESH MODE — When refresh is requested the Refresh Enable input is HIGH. This input is ANDed with the six outputs of the internal 6-bit counter. At each $\overline{CP}$ pulse the counter increments by one, sequencing the outputs ($\overline{O}_0 - \overline{O}_5$) through all 64 row addresses. When the counter sequences to all zeroes, the Zero Detect output goes LOW signaling the end of the refresh sequence. Due to counter decoding spikes, the Zero Detect output is valid only after t_{cz} following the LOW going edge of $\overline{CP}$.

DISTRIBUTED REFRESH MODE — In the distributed refresh mode, one row is selected for refresh each ($t_{refresh/n}$) time where n = number of rows in the device and refresh is the specified refresh rate for the device. For the M4027, $t_{refresh}$ = 2.0 ms and n = 64, therefore one row is refreshed each 31 μs. Following the refresh cycle at row n, the $\overline{CP}$ input is pulsed, advancing the refresh address by one row so that the next refresh cycle will be performed on row n + 1. The $\overline{CP}$ input may be pulsed following each refresh cycle or within the refresh cycle after the specified memory device address hold time.

ROW AND COLUMN ADDRESS — All twelve system address lines are applied to the inputs of the 96LS32. When Refresh Enable is LOW and Row Select is HIGH, the input addresses $A_0 - A_5$ are gated to the outputs and applied to the driven memories. Conversely, when Row Select is LOW (with Refresh Enable still LOW), input addresses $A_6 - A_{11}$ are gated to the outputs and applied to the driven memories. When memory devices are driven directly by the 96LS32, the address applied to the memory devices is the inverse of the address at the inputs due to the inverted outputs of the 96LS32. This should be remembered when checking out the memory system.

FUNCTION TABLE

Refresh Enable	Row Select	Outputs
H	X	Refresh Address (from internal counter)
L	H	Row Address (complement of $A_0 - A_5$)
L	L	Column Address (complement of $A_6 - A_{11}$)

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

96LS42

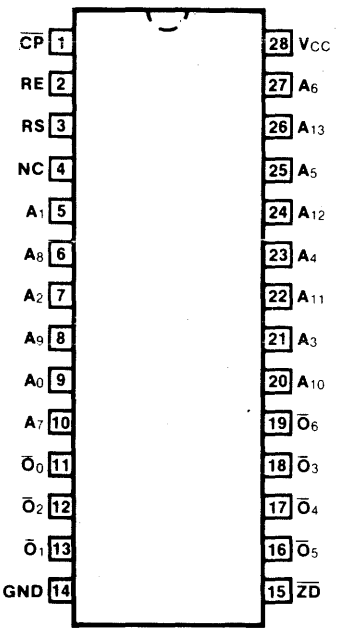
ADDRESS MULTIPLEXER/REFRESH COUNTER

(For 16K Dynamic RAMs)

DESCRIPTION — The 96LS42 is an address multiplexer and refresh counter for multiplexed address dynamic RAMs requiring refresh of 64 or 128 cycles. It multiplexes 14 bits of system supplied address to seven output address pins. The device also contains a 7-bit refresh counter which is externally controlled so that either distributed or burst refresh may be used. The high performance of the 96LS42 makes it especially suitable for use with high speed n-channel RAMs like the F16K. The 96LS42 is manufactured using Fairchild's advanced low power Schottky process.

- **SIMPLIFIES SYSTEM DESIGN**
- **REDUCES PACKAGE COUNT**
- **DRIVES HIGH CAPACITIVE LOADS**
- **EITHER BURST OR DISTRIBUTED REFRESH**
- **LOW POWER SCHOTTKY DESIGN**
- **STANDARD 28-PIN PACKAGE**

CONNECTION DIAGRAM
PINOUT A



ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE	MILITARY GRADE	PKG TYPE
		V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	
Plastic DIP (P)	A	96LS42PC		9Y
Ceramic DIP (D)	A	96LS42DC	96LS42DM	8E

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	96XX (U.L.) HIGH/LOW
A_0 — A_6	Row Address Inputs	0.5/0.13
A_7 — A_{13}	Column Address Inputs	0.5/0.13
$\overline{CP}$	Clock Pulse Input (Active Falling Edge)	0.5/0.13
RE	Refresh Enable Input	0.5/0.13
RS	Row Select Input	0.5/0.13
$\overline{ZD}$	Refresh Counter Zero Detect Output (Active LOW)	25/3.1
$\overline{O}_0$ — $\overline{O}_6$	Multiplexer Outputs (Active LOW)	25/3.1

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FUNCTIONAL DESCRIPTION — The 96LS42 address multiplexer/refresh counter performs the following functions:

1. Row, Column and Refresh Address multiplexing
2. Address counting for burst or distributed refresh

These functions are controlled by two signals, Refresh Enable and Row Select, both of which are active HIGH TTL inputs. The Function Table shows the levels required to multiplex to the output:

1. Refresh addresses (from internal counter)
2. Row addresses (A_0 through A_6)
3. Column addresses (A_7 through A_{13})

Burst Refresh Mode — When refresh is requested the Refresh Enable input is HIGH. This input is AND-ed with the seven outputs of the internal 7-bit counter. At each $\overline{CP}$ pulse the counter increments by one, sequencing the outputs ($\overline{O}_0 - \overline{O}_6$) through all 128 row addresses. When the counter sequences to all zeroes, the Zero Detect output goes LOW signaling the end of the refresh sequence. Due to counter decoding spikes, the Zero Detect output is valid only after t_{cz} following the LOW going edge of $\overline{CP}$.

Distributed Refresh Mode — In the distributed refresh mode, one row is selected for refresh each ($t_{refresh/n}$) time where n = number of rows in the device and refresh is the specified refresh rate for the device. For the F16 k, Refresh = 2.0 ms and n = 128, therefore one row is refreshed each 62 μS. Following the refresh cycle at row n, the $\overline{CP}$ input is pulsed, advancing the refresh address by one row so that the next refresh cycle will be performed on row n + 1. The $\overline{CP}$ input may be pulsed following each refresh cycle or within the refresh cycle after the specified memory device address hold time.

Row and Column Address — All 14 system address lines are applied to the inputs of the 96LS42. When Refresh Enable is LOW and Row Select is HIGH, the input Addresses $A_0 - A_6$ are gated to the outputs and applied to the driven memories. Conversely, when Row Select is LOW (with Refresh Enable still LOW). Input addresses $A_7 - A_{13}$ are gated to the outputs and applied to the driven memories. When memory devices are driven directly by the 96LS42, the address applied to the memory devices is the inverse of the address at the inputs due to the inverted outputs of the 96LS42. This should be remembered when checking out the memory system.

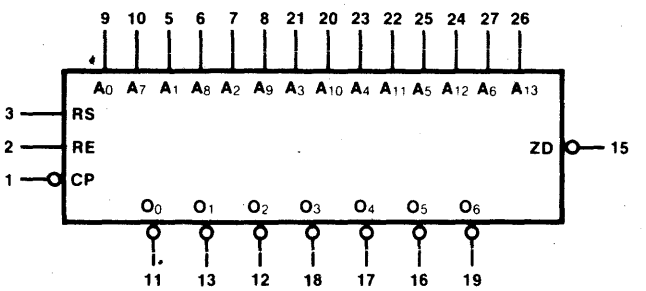
FUNCTION TABLE

Refresh Enable	Row Select	Outputs
H	X	Refresh Address (from internal counter)
L	H	Row Address (complement of $A_0 - A_6$)
L	L	Column Address (complement of $A_7 - A_{13}$)

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

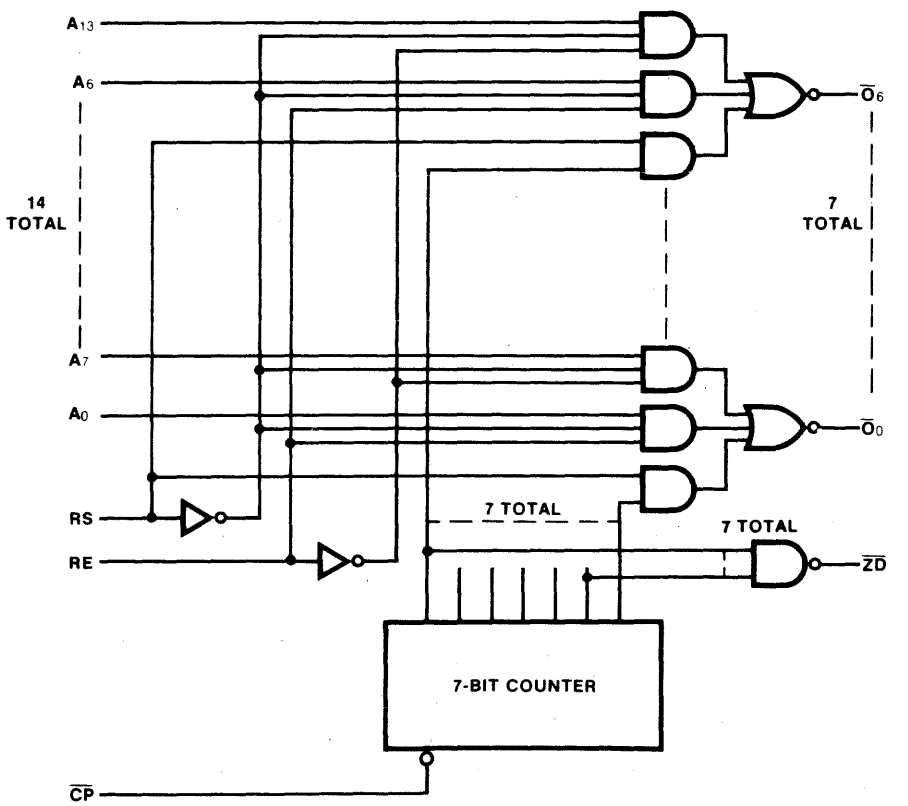
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LOGIC SYMBOL



V_{CC} = Pin 28
GND = Pin 14

LOGIC DIAGRAM



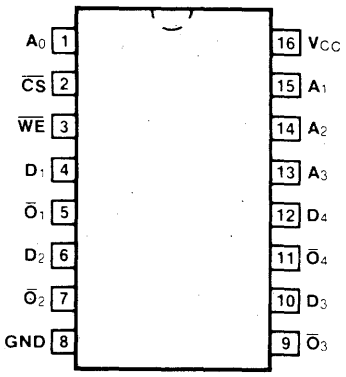
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54S/74S189
54LS/74LS189

64-BIT RANDOM ACCESS MEMORY

(With 3-State Outputs)

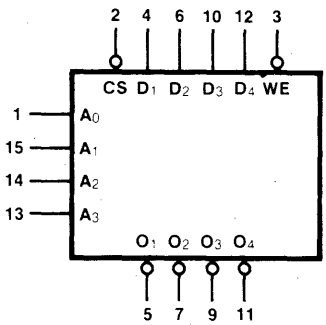
CONNECTION DIAGRAM
PINOUT A



DESCRIPTION — The '189 is a high speed 64-bit RAM organized as a 16-word by 4-bit array. Address inputs are buffered to minimize loading and are fully decoded on-chip. The outputs are 3-state and are in the high impedance state whenever the Chip Select ($\overline{CS}$) input is HIGH. The outputs are active only in the Read mode and the output data is the complement of the stored data.

- **3-STATE OUTPUTS FOR DATA BUS APPLICATIONS**
- **BUFFERED INPUTS MINIMIZE LOADING**
- **ADDRESS DECODING ON-CHIP**
- **DIODE CLAMPED INPUTS MINIMIZE RINGING**

LOGIC SYMBOL



VCC = Pin 16
GND = Pin 8

ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE VCC = +5.0 V ±5%, TA = 0°C to +70°C	MILITARY GRADE VCC = +5.0 V ±10%, TA = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	74S189PC, 74LS189PC		9B
Ceramic DIP (D)	A	74S189DC, 74LS189DC	54S189DM, 54LS189DM	6B
Flatpak (F)	A	74S189FC, 74LS189FC	54S189FM, 54LS189FM	4L

INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	54/74S (U.L.) HIGH/LOW	54/74LS (U.L.) HIGH/LOW
$A_0 - A_3$	Address Inputs	0.63/0.16	0.5/0.013
$\overline{CS}$	Chip Select Input (Active LOW)	0.63/0.16	0.5/0.013
$\overline{WE}$	Write Enable Input (Active LOW)	0.63/0.16	0.5/0.013
$D_1 - D_4$	Data Inputs	0.63/0.16	0.5/0.013
$\overline{O}_1 - \overline{O}_4$	Inverted Data Outputs	162/10 (50)	10/10 (5.0)

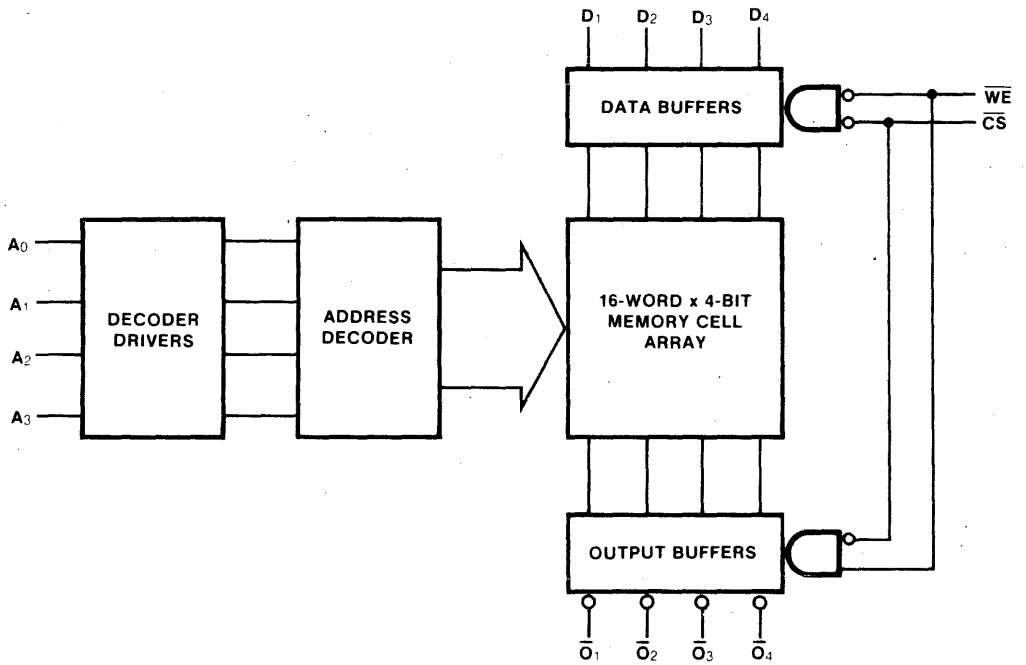
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FUNCTION TABLE

INPUTS $\overline{CS}$	INPUTS $\overline{WE}$	OPERATION	CONDITION OF OUTPUTS
L	L	Write	High Impedance
L	H	Read	Complement of Stored Data
H	X	Inhibit	High Impedance

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER		54/74S Min	54/74S Max	54/74LS Min	54/74LS Max	UNITS	CONDITIONS
V_{OL}	Output LOW Voltage	XM		0.5		0.4	V	V_{CC} = Min I_{OL} = 16 mA ('S189) I_{OL} = 8.0 mA (54LS189) I_{OL} = 16 mA (74LS189)
		XC		0.45		0.5		
V_{OH}	Output HIGH Voltage	XM		2.4		2.8	V	V_{CC} = Min I_{OH} = 2.0 mA (54S189) I_{OH} = 6.5 mA (74S189) I_{OH} = 0.4 mA ('LS189)
		XC		2.4		2.8		
I_{OS}	Output Short Circuit Current		-30	-100	-80*		mA	V_{CC} = Max
I_{CC}	Power Supply Current			110		40	mA	V_{CC} = Max; $\overline{WE}$, $\overline{CS}$, Gnd

*Typical Value

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AC CHARACTERISTICS OVER RECOMMENDED V_{CC} AND T_A RANGE (unless otherwise specified)

SYMBOL	PARAMETER		54/74S C_L = 30 pF, R_L = 300 Ω Min	54/74S Max	54/74LS C_L = 15 pF Min	54/74LS Max	UNITS	CONDITIONS
t_{PLH} t_{PHL}	Access Time, HIGH or LOW, A_n to $\overline{O}_n$	XM XC		50 35		37* 37*	ns	Figs. 3-1, 3-20
t_{PZH} t_{PZL}	Access Time, HIGH or LOW, $\overline{CS}$ to $\overline{O}_n$	XM XC		32 22		10* 10*	ns	Figs. 3-3, 3-11, 3-12 R_L = 2 kΩ ('LS189)
t_{PHZ}	Disable Time $\overline{CS}$ to $\overline{O}_n$	XM XC		35 25			ns	Figs. 3-3, 3-11, 3-12 R_L = 2 kΩ ('LS189) C_L = 5 pF
t_{PLZ}	Disable Time $\overline{CS}$ to $\overline{O}_n$	XM XC		25 17				
t_{PZH} t_{PZL}	Access Time, HIGH or LOW, $\overline{WE}$ to $\overline{O}_n$	XM XC		40 30			ns	Figs. 3-3, 3-11, 3-12 R_L = 2 kΩ ('LS189)
t_{PHZ}	Disable Time $\overline{WE}$ to $\overline{O}_n$	XM XC		30 20			ns	Figs. 3-3, 3-11, 3-12 R_L = 2 kΩ ('LS189) C_L = 5 pF
t_{PLZ}	Disable Time $\overline{WE}$ to $\overline{O}_n$	XM XC		32 20				

AC OPERATING REQUIREMENTS OVER RECOMMENDED V_{CC} AND T_A RANGE (unless otherwise specified)

SYMBOL	PARAMETER	54/74S Min	54/74S Max	54/74LS Min	54/74LS Max	UNITS	CONDITIONS
t_s (H) t_s (L)	Setup Time HIGH or LOW A_n to $\overline{WE}$	0 0		10* 10*		ns	Fig. 3-21
t_h (H) t_h (L)	Hold Time HIGH or LOW A_n to $\overline{WE}$	0 0		0* 0*		ns	
t_s (H) t_s (L)	Setup Time HIGH or LOW D_n to $\overline{WE}$	20 20		25* 25*		ns	Fig. 3-13
t_h (H) t_h (L)	Hold Time HIGH or LOW D_n to $\overline{WE}$	0 0		0* 0*		ns	
t_s (L)	Setup Time LOW $\overline{CS}$ to $\overline{WE}$	0				ns	Fig. 3-14
t_h (L)	Hold Time LOW $\overline{CS}$ to $\overline{WE}$	0				ns	Fig. 3-13
t_w (L)	$\overline{WE}$ Pulse Width LOW	20		25*		ns	Fig. 3-14

*Typical Value

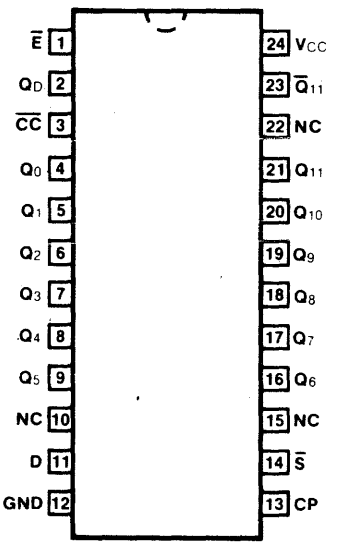
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54LS/74LS504

12-BIT SUCCESSIVE APPROXIMATION REGISTER

(With Expansion Control)

CONNECTION DIAGRAM
PINOUT A



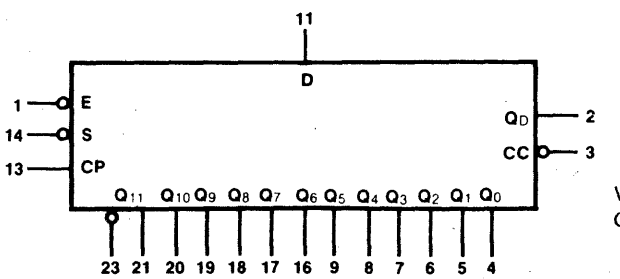
DESCRIPTION — The 'LS504 performs serial-to-parallel conversion and provides a Conversion Complete ($\overline{CC}$) signal. The 'LS504 is a 12-bit version of the 8-bit 'LS502 and has an active LOW Enable ($\overline{E}$) input for expansion, similar to the 'LS503. For detailed discussion of the various operations, please see the 'LS502 and 'LS503 data sheets.

- **PERFORMS SERIAL-TO-PARALLEL CONVERSION**
- **EXPANSION CONTROL FOR LONGER WORDS**
- **STORAGE AND CONTROL FOR SUCCESSIVE APPROXIMATION A TO D CONVERSION**
- **LOW POWER SCHOTTKY VERSION OF 2504**

ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE	MILITARY GRADE	PKG TYPE
		V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	
Plastic DIP (P)	A	74LS504PC		9N
Ceramic DIP (D)	A	74LS504DC	54LS504DM	6N
Flatpak (F)	A	74LS504FC	54LS504FM	4M

LOGIC SYMBOL



VCC = Pin 24
GND = Pin 12

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INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	54/74LS (U.L.) HIGH/LOW
D	Serial Data Input	0.5/0.25
$\overline{S}$	Start Input (Active LOW)	0.5/0.25
CP	Clock Pulse Input (Active Rising Edge)	0.5/0.25
$\overline{E}$	Conversion Enable Input (Active LOW)	0.5/0.25
Q_D	Synchronized Serial Data Output	10/5.0 (2.5)
$\overline{CC}$	Conversion Complete Output (Active LOW)	10/5.0 (2.5)
$Q_0 - Q_{11}$	Parallel Register Outputs	10/5.0 (2.5)
$\overline{Q}_{11}$	Complement of Q_{11} Output	10/5.0 (2.5)

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER	54/74LS		UNITS	CONDITIONS
		Min	Max		
I_{CC}	Power Supply Current		90	mA	V_{CC} = Max

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25° C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	54/74LS C_L = 15 pF		UNITS	CONDITIONS
		Min	Max		
f_{max}	Maximum Clock Frequency	15		MHz	Figs. 3-1, 3-8
t_{PLH} t_{PHL}	Propagation Delay CP to Q_n or $\overline{CC}$		38 28	ns	
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}$ to Q_7		19 24	ns	Figs. 3-1, 3-5 CP = 4.5, $\overline{S}$ = Gnd

AC OPERATING REQUIREMENTS: V_{CC} = +5.0 V, T_A = +25° C

SYMBOL	PARAMETER	54/74LS		UNITS	CONDITIONS
		Min	Max		
t_s (H) t_s (L)	Setup Time HIGH or LOW $\overline{S}$ to CP	16 16		ns	Fig. 3-6
t_h (H) t_h (L)	Hold Time HIGH or LOW $\overline{S}$ to CP	0 0		ns	
t_s (H) t_s (L)	Setup Time HIGH or LOW D to CP	8.0 8.0		ns	Fig. 3-6
t_h (H) t_h (L)	Hold Time HIGH or LOW D to CP	10 10		ns	
t_w (H) t_w (L)	CP Pulse Width HIGH or LOW	20 46		ns	Fig. 3-8

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54LS/74LS503

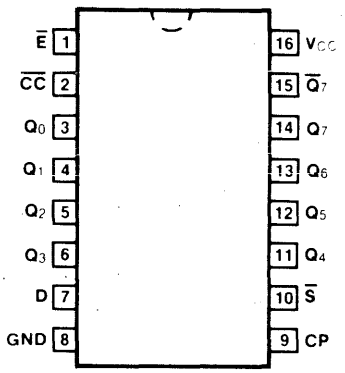
8-BIT SUCCESSIVE APPROXIMATION REGISTER

(With Expansion Control)

DESCRIPTION — The 'LS503 register is basically the same as the 'LS502 except that it has an active LOW Enable ($\overline{E}$) input that is used in cascading two or more packages for longer word lengths. A HIGH signal on $\overline{E}$, after a START operation, forces Q_7 HIGH and prevents the device from accepting serial data. With the $\overline{E}$ input of an 'LS503 connected to the $\overline{CC}$ output of a preceding (more significant) device, the 'LS503 will be inhibited until the preceding device is filled, causing its $\overline{CC}$ output to go LOW. This LOW signal then enables the 'LS503 to accept the serial data on subsequent clocks. For a description of the starting, shifting and conversion operations, please see the 'LS502 data sheet.

- **PERFORMS SERIAL-TO-PARALLEL CONVERSION**
- **EXPANSION CONTROL FOR LONGER WORDS**
- **STORAGE AND CONTROL FOR SUCCESSIVE APPROXIMATION A TO D CONVERSION**
- **LOW POWER SCHOTTKY VERSION OF 2503**

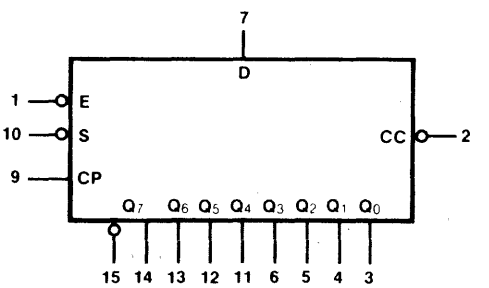
CONNECTION DIAGRAM
PINOUT A



ORDERING CODE: See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE V_{CC} = +5.0 V ±5%, T_A = 0°C to +70°C	MILITARY GRADE V_{CC} = +5.0 V ±10%, T_A = -55°C to +125°C	PKG TYPE
Plastic DIP (P)	A	74LS503PC		9B
Ceramic DIP (D)	A	74LS503DC	54LS503DM	6B
Flatpak (F)	A	74LS503FC	54LS503FM	4L

LOGIC SYMBOL

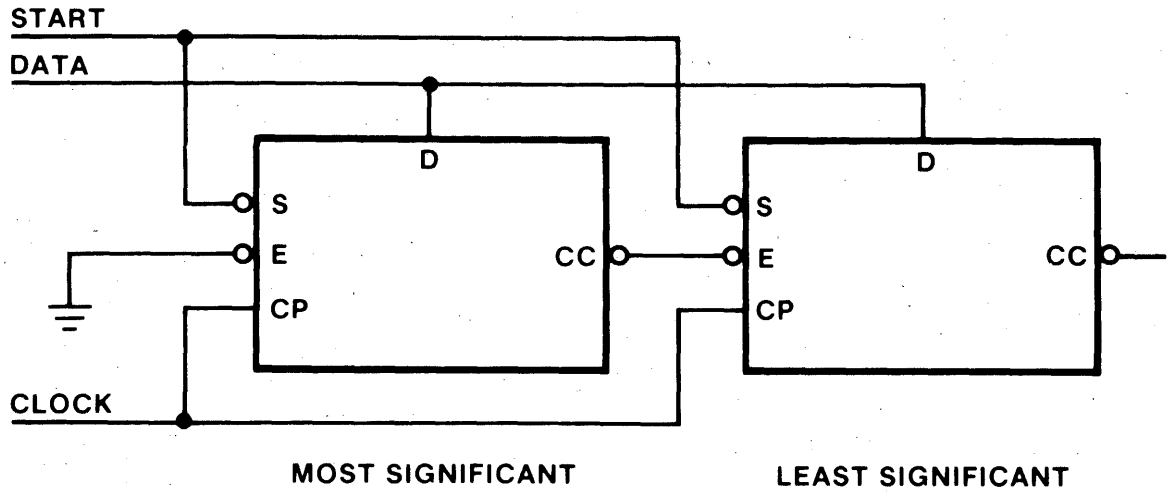


V_{CC} = Pin 16
GND = Pin 8

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CONNECTION FOR LONGER WORD LENGTHS



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE (unless otherwise specified)

SYMBOL	PARAMETER	54/74LS		UNITS	CONDITIONS
		Min	Max		
I_{CC}	Power Supply Current		65	mA	V_{CC} = Max

AC CHARACTERISTICS: V_{CC} = +5.0 V, T_A = +25°C (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	54/74LS C_L = 15 pF		UNITS	CONDITIONS
		Min	Max		
f_{max}	Maximum Clock Frequency	15		MHz	
t_{PLH} t_{PHL}	Propagation Delay CP to Q_n or $\overline{CC}$		38 28	ns	Figs. 3-1, 3-8
t_{PLH} t_{PHL}	Propagation Delay $\overline{E}$ to Q_7		19 24	ns	Figs. 3-1, 3-5 CP = 4.5 V, $\overline{S}$ = Gnd

AC OPERATING REQUIREMENTS: V_{CC} = +5.0 V, T_A = +25°C

SYMBOL	PARAMETER	54/74LS		UNITS	CONDITIONS
		Min	Max		
t_s (H) t_s (L)	Setup Time HIGH or LOW $\overline{S}$ to CP	16 16		ns	Fig. 3-6
t_h (H) t_h (L)	Hold Time HIGH or LOW $\overline{S}$ to CP	0 0		ns	
t_s (H) t_s (L)	Setup Time HIGH or LOW D to CP	8.0 8.0		ns	Fig. 3-6
t_h (H) t_h (L)	Hold Time HIGH or LOW D to CP	10 10		ns	
t_w (H) t_w (L)	CP Pulse Width HIGH or LOW	20 46		ns	Fig. 3-8

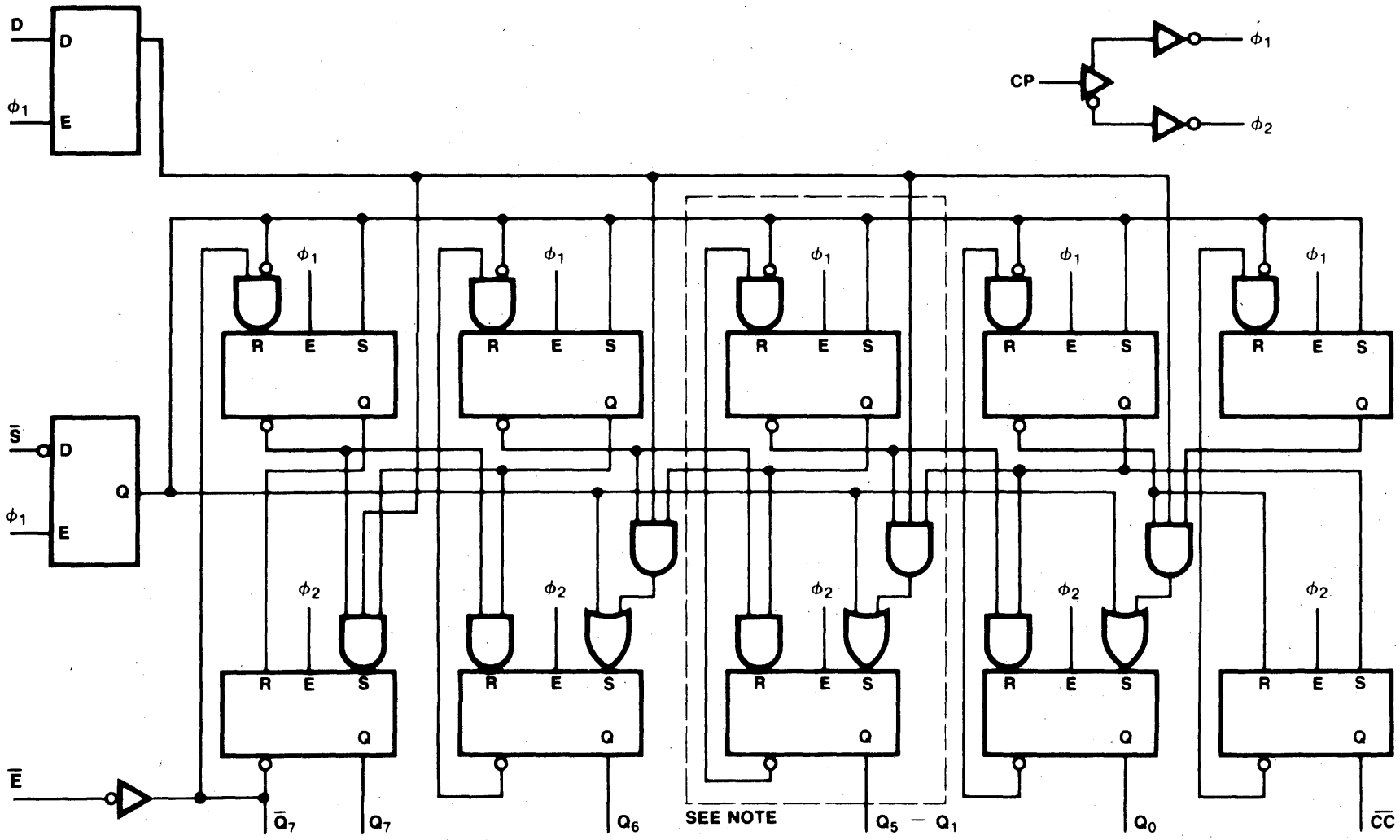
INPUT LOADING/FAN-OUT: See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	54/74LS (U.L.) HIGH/LOW
D	Serial Data Input	0.5/0.25
$\overline{S}$	Start Input (Active LOW)	0.5/0.25
CP	Clock Pulse Input (Active Rising Edge)	0.5/0.25
$\overline{E}$	Conversion Enable Input (Active LOW)	10/5.0 (2.5)
$\overline{CC}$	Conversion Complete Output (Active LOW)	10/5.0 (2.5)
$Q_0 - Q_7$	Parallel Register Outputs	10/5.0 (2.5)
$\overline{Q}_7$	Complement of Q_7 Output	10/5.0 (2.5)

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LOGIC DIAGRAM



Note: Cell logic is repeated for register stages Q_5 to Q_1.

HERE ARE 9 COMPELLING REASONS FOR HAVING US PRODUCE A CUSTOM LSI CIRCUIT FOR YOU:

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COUNTERS

For DC to 5MHz counting applications.

LS7030: DC to 5MHz eight decade MOS up counter with 8 decade latch and multiplexer.

Multiplexed BCD and 7 segment outputs. Single power supply +4.75 to +15 VDC (full frequency range over full voltage range). Compatible with CMOS logic. Counter output latches. Leading zero blanking. 40 pin DIP.

For 5MHz to 500MHz counting applications.

LS7031: DC to 5MHz six decade MOS up counter with 8 decade latch and multiplexer.

Multiplexed BCD outputs. Access to LSD latches allows attachment of prescalers for counting to 500 MHz. Leading zero blanking. Single power supply operation +4.75 to +15VDC (full frequency range over full voltage range). Compatible with CMOS logic. 40 pin DIP.

For multi-comparison applications where parallel outputs are required.

LS7040: Dual 3 decade up/down counter with parallel BCD outputs.

Selectable as 6 decade or dual 3 decade up/down counter. DC to 350KHz count frequency at +5 volts. Fully synchronous operation. Inputs CMOS, TTL, and DTL compatible at +5V operation. Reset. Count enable. Power-on-reset. 40 pin DIP.

For counting applications requiring presignalling and recycling.

LS 7050: DC to 50 KHz six decade up/down counter.

Counting down: 2 signals, optional recycling; counting up: 2 signals, optional recycling, zero detect output. Divide by 5 or 6 inputs. 7-segment output. Latches. Leading zero blanking. High noise immunity. All outputs CMOS compatible over entire power supply range (+5V to +15V) 40-pin DIP.

For DC to 10 MHz counting applications.

LS 7060: DC to 10 MHz 32-bit MOS binary counter with 32-bit latch and multiplexer.

8-bit tri-state multiplexed outputs. Single power supply +4.75 to +5.25 VDC. Bus compatible. 18-pin DIP.

For DC to 2.56 GHz counting applications.

LS 7061 DC to 10 Mhz 32-bit MOS up counter with 40 bit latch and multiplexer.

8-bit tri-state multiplexed outputs. Access to 8 LSB latches allows attachment of prescalers for counting to 2.56 GHz. Single power supply operation +4.75 to +5.25 VDC. Bus compatible. 24-pin DIP.

For timing applications requiring keyboard control.

LS7090: 9 decade keyboard controlled Up/Down timer or counter with memory providing 7 segment display, comparator and tone outputs.

Interfaces directly with key switches of standard keyboard. Automatic or keyboard-controlled reset. Divide by 5 or 6 inputs. Contents of memory counter can be displayed at any time. Schmitt trigger count input. Leading zero blanking. Single pin scan oscillator controls. CMOS type noise immunity. All inputs protected, and CMOS, TTL, and DTL compatible at 5V operation. 40-pin DIP.

COMPARATOR

For multicomparison applications; to be used with LS7040.

LS7240: 7 level comparator/multiplexer with parallel BCD inputs. Seven comparators can be loaded with one set of thumbwheel switches. Contents of any comparator constantly available for 7-segment display. Two or more 7240s can be used with one 7040, offering as many levels as needed. 24-pin DIP.

NUMERIC DISPLAY DRIVER

For liquid crystal or gas discharge displays requiring up to 60V

LS7100: BCD to 7 segment latch/decoder/driver.

Ion-implanted P Channel MOS circuit compatible with CMOS and TTL systems. Drive voltages up to 60V. 16 pin DIP.

MULTIPLEXER/ALPHA-NUMERIC DISPLAY DRIVER

For switching applications and alpha-numeric display applications requiring up to 60V.

LS7110: Binary addressable latched 8-channel multiplexer/demultiplexer/driver.

Ion-implanted P Channel MOS circuit compatible with CMOS and TTL systems. Drive voltages up to 60V. 16 pin DIP.

CLOCK CIRCUIT

For direct drive of large liquid crystal display clocks from 50/60Hz.

C1200: MOS digital clock circuit.

Directly drives liquid crystal displays (80V P-P across LCD), 50/60Hz AC input. 12 hour clock format (hours and minutes). Independent minute and hour set at 2Hz rate. Flashing 1 second indicator. 28 pin DIP.

DIVIDERS

For applications requiring 10 pulses per second from 50/60Hz input.

RED 5/6: CMOS divider.

Input shaping network. Resettable. Division select input 50/60Hz. Clock enable input. 8 pin* mini-DIP.

For applications requiring 1 pulse per second from 50/60Hz input.

RED 50/60: CMOS divider.

Input shaping network. Resettable. Division select input 50/60Hz. Clock enable input. 8 pin* mini-DIP.

For applications requiring 1 pulse per minute from 50/60Hz input.

RED 3000/3600: CMOS divider.

Input shaping network. Resettable. Division select input 50/60Hz. Clock enable input. 8 pin* mini-DIP.

* Inputs so arranged that circuit cannot be damaged if plugged in backwards.

LSI COMPUTER SYSTEMS INC.
1235 Walt Whitman Road, Melville, New York 11746.
(516) 271-0400. TWX: 510 226 7833.
Argentina Tel. 46-9549. Germany Tel. 089/69 65 66/67. U.K. Tel. 01 995-8495, Mr. Glyn Hall.
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8 x 8 Multiplier

67558/57558
67558-1/57558-1

Features/Benefits

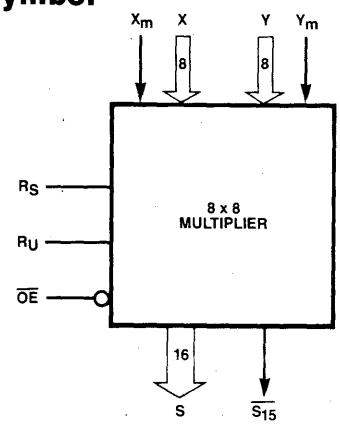
- **Unsigned, Signed, or Mixed Multiplication**
- **Rounding Inputs for Signed or Unsigned Operation**
- **Inverted Most Significant Output for Signed Expansion**
- **Three-State Outputs for Bus Operation**
- **High Speed—125 ns Max**

PART NUMBER	PACKAGE	TEMPERATURE RANGE
67558, 67558-1	D40	0°C TO +75°C
57558, 57558-1	D40	−55°C TO +125°C
57558, 57558-1	F42	−55°C TO +125°C

Description

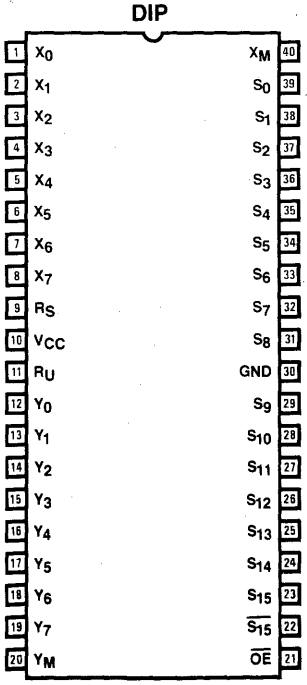
The 57558/67558 is a high speed 8 x 8 combinatorial Multiplier which can multiply two eight-bit unsigned or signed 2s complement numbers and generate the sixteen-bit unsigned or signed product. Each input operand X and Y has an associated Mode control line, X_M and Y_M respectively. When a Mode control line is at a Low logic level the operand is treated as an unsigned eight-bit number while if the Mode control is at a High logic level the operand is treated as an eight-bit signed 2s complement number. Two additional inputs R_S and R_U allow the addition of a bit in the multiplier array at the appropriate bit positions for rounding signed or unsigned fractional numbers. The most significant product bit is available in both True and Complement form to assist in expansion to larger signed multipliers. The product outputs are three-state, controlled by an active Low Output Enable which allows several Multipliers to be connected to a parallel bus or be used in a pipelined system. The device uses a single +5V power supply and is packaged in a standard 40-pin DIP.

Logic Symbol

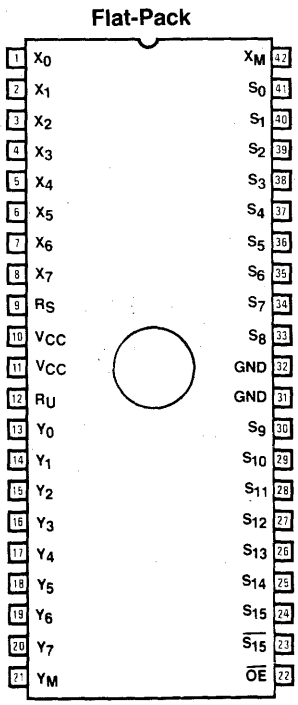


Pin Configuration

DIP



Flat-Pack



1165 East Arques Avenue, Sunnyvale, CA 94086 Tel: (408) 739-3535 TWX: 910-339-9229 Monolithic Memories

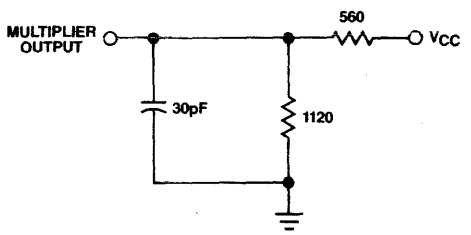
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AC Electrical Characteristics

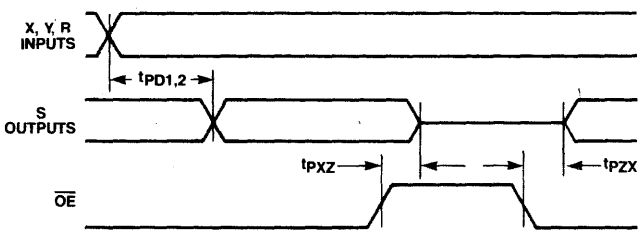
Over Recommended Operating V_{CC} and Temperature Range

SYMBOL	PARAMETER	DEVICE	MIN	TYP	MAX	UNIT
t_{PXZ}	Delay from OE to S High Impedance State	67558		30	40	ns
		57558		30	50	
		67558-1		30	40	
		57558-1		30	50	
t_{PZX}	Delay from OE to S Active State	67558		30	40	ns
		57558		30	50	
		67558-1		30	40	
		57558-1		30	50	
t_{PD1}	Delay from Y, X to S_{0-4}	67558		80	135	ns
		57558		80	140	
		67558-1		80	115	
		57558-1		80	125	
t_{PD2}	Delay from Y, X to S_{5-15}, $\overline{S_{15}}$	67558		100	150	ns
		57558		100	155	
		67558-1		100	125	
		57558-1		100	135	

Standard Test Load



Timing Waveform



Functional Description

The 57558/67558 Multiplier is an 8 x 8 combinatorial logic array capable of multiplying numbers in unsigned, signed 2s complement, or mixed notation. Each eight-bit input operand X and Y has associated with it a mode control which determines whether the array treats the number as signed or unsigned. If the mode control is at a High Logic level then the operand is treated as a 2s complement number with the most significant bit having a negative weight, while if the mode control is at a Low Logic level then the operand is treated as an unsigned number.

The multiplier provides all 16 product bits generated by the multiplication. For expansion during signed or mixed multiplication the most significant product bit has both true and complement available. This allows an adder to be used as a subtractor in many applications and eliminates the need for SSI circuits.

Two inputs, R_S and R_U, are additional inputs to the array which allow the addition of a bit at the appropriate positions in the array so as to provide rounding to the best signed or unsigned fractional eight-bit result. These inputs can also be used for rounding in larger multipliers.

The product outputs of the multiplier are controlled by an active Low Output Enable control. When this control is at a Low Logic level the multiplier outputs are active, while if the control is at a High Logic level then the outputs are placed in a high-impedance state. This three-state capability allows multipliers to be placed on a common bus and also allows pipelining of multiplications for higher speed systems.

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Absolute Maximum Ratings

Supply Voltage V_{CC} ..... −0.5V to +7.0V
Input Voltage ..... −1.5V to +5.5V
Input Current ..... −20 MA to +5 mA
Output Current ..... 100 mA
Storage Temperature Range ..... −65°C to +150°C

Recommended Operating Conditions

SYMBOL	PARAMETER	57558, 57558-1			67558, 67558-1			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply Voltage	4.5	5.0	5.5	4.75	5.0	5.25	V
T_A	Operating Free Air Temperature				0	25	75	°C
T_C	Operating Case Temperature	−55	25	125				°C
I_{OH}	High Level Output Current			−2.0			−2.0	mA
I_{OL}	Low Level Output Current			8			8	mA

DC Electrical Characteristics

Over Recommended Operating Free Air Temperature Range Unless Otherwise Noted

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP[1]	MAX	UNIT
V_{IH}	High Level Input Voltage		2.0			V
V_{IL}	Low Level Input Voltage				0.8	V
V_{IC}	Input Clamp Voltage	V_{CC} = Min, I_I = −18 mA		−1.0	−1.5	V
V_{OH}	High Level Output Voltage	V_{CC} = Min, I_{OH} = −2.0 mA	2.4	3.0		V
V_{OL}	Low Level Output Voltage	V_{CC} = Min, I_{OL} = 8 mA		0.3	0.5	V
I_{HZ}	High Level Off-State Output Current	V_{CC} = Max, V_O = 2.4V			100	μA
I_{LZ}	Low Level Off-State Output Current	V_{CC} = Max, V_O = 0.5V			−100	μA
I_I	Maximum Input Current	V_{CC} = Max, V_I = 5.5V			1.0	mA
I_{IH}	High Level Input Current	V_{CC} = Max, V_I = 2.4V			100	μA
I_{IL}	Low Level Input Current	V_{CC} = Max, V_I = 0.5V			−1.0	mA
I_{OS}	Output Short Circuit Current	V_{CC} = Max, V_O = 0V	−10		−90	mA
I_{CC}	Supply Current	V_{CC} = Max		180	280	mA

NOTE: 1. Typical values are at V_{CC} = 5.0V, T_A = 25°C

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67516/67518 16x16 Multiplier/Divider
67508 8x8 Multiplier/Divider

PRELIMINARY

Product Information

67516 16 x 16 (67508 8 x 8) Multiplier/Divider

The 67516 (67508) is a bus organized family of 16 x 16 and 8 x 8 Multiplier/Divider. The device provides both multiplication and division of 2s complement 16 (8) bit numbers at high speed. There are 16 different multiply options including positive and negative multiply, positive and negative accumulation, multiplication by a constant and both single and double length addition in conjunction with the multiplication. Seven different divide options allow single or double length division, division of a previously generated number, division by a constant, and continual division of a remainder or quotient. The 67516 (67508) is a time sequenced device requiring a single clock and loads operands and presents results to a bi-directional 16 (8) bit-bus. The loading of the operands, reading of the results and control of the device is performed by a 3-bit control field. The device has the additional feature that operands and results can be either integers or fractions and when dealing with fractions, automatic scaling occurs. Results can be rounded if required and an Overflow output indicates whenever a result is outside the normally accepted number range. For a simple multiplication of two operands and reading of the double length result the device takes n/2 clock periods, a worst case clock period of 100 ns gives a multiplication time of 800 ns worst case for 16 x 16 multiplication and 400 ns for 8 x 8. More complex multiplications will take additional clock periods for loading the additional operands. A simple divide operaton will take n + 4 clock periods for a worst case time of 2μs (32 bits/16 bits) and 1.2μs (16 bits/8 bits).

The device uses standard low-power Schottky technology to produce a single +5V supply TTL compatible device. Bus input and control and clock inputs require less than 1mA input current, and bus outputs are three-state sinking 8mA at the low logic level. These devices will be available both in a commercial and military temperature range and packaged in 24 pin (16 x 16) and 16 pin (8 x 8) dual-in-line packages. Power consumption will be approximately 1 watt and 0.75 watts respectively to give a worst case clock period over the military temperature range of 100 ns.

Device Operation

The Multiplier/Divider contains four working registers each of 16 (8) bits. These registers are Y the Multiplier register, X the Multiplicand and Divisor register, W which is the least significant half of a double length accumulator and holds the least significant half of the product after a multiplication or the quotient after a division operation. In addition to the registers, there is a high speed arithmetic unit which performs addition, subtraction and shifting operations in order to generate the required arithmetic functions, a loading sequencer and a PLA control network.

Operands are loaded into the working registers in time sequence at each clock period under the control of a sequencer. A load signal must be low in order for the clock to activate the loading process and continue to the next step in the loading operation. After all the operands are loaded, the device jumps to the multiply or to the divide routine and performs the required operation. After n/2 clock periods for a multiply (or n + 4 clock periods for a divide), the device is ready to place the result on the bus in time sequence.

Three control inputs $I_{0,1,2}$ select the required function and drive the sequencer from state to state. So the action of the Multiplier/Divider at any clock period is a function of the machine state and the state of the control inputs. Figure 1 shows the Multiply/Divide State Table and all possible operations. After a Read or Round operation the machine is driven back to State 0 and a new sequence of arithmetic operations is assumed. If a chain operation is being performed, such as accumulate products, then State 0 is bypassed and loading of an operand or jumping to the arithmetic operation occurs at the end of the previous arithmetic operation at State 32 for a Multiply, or State 33 for a Divide.

Register X is a dual rank register which allows the loading of operand X during the multiplication or division process. If the machine enters the loading sequence and a new X operand has not been loaded then the machine proceeds with the previously loaded X. This loading while processing allows a cycle to be saved during chain calculations and also allows multiplication and division by a constant.

Figures 2 and 3 show the codes and time taken for the 23 different arithmetic operations possible. These operations can be concatenated in strings to perform complex arithmetic 2s complement operations at high speed. Rounding and reading of results can be performed after any operation.

Figure 4 is a block diagram of the nxn Multiplier/Divider.

Multiplication

The 67516 (67508) provides 2s complement 16 (8) bit multiplication, and can also accumulate previously generated double products. No time penalty is incurred for accumulation since the machine accumulates while the multiplication operation is proceeding. In addition to accumulation the device can add in to a product either a single length or double length number. It can also use a previously loaded operand as a constant so that constant multiplication and accumulation is possible.

One key feature is the ability to perform both positive and negative multiplications again without any speed penalty. This feature allows complex multiplications to be programmed simply. Another important feature is the ability to work in fractions or integers.

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Division

The 67516 (67508) also provides a range of division operations. A double length number in Z,W is divided by X, and the result Q is stored in Z and the remainder R in W. Again all numbers are in the 2s complement number representation with the most significant bit of an operand, whether double or single length, having a negative weight. In order to facilitate repeated division and have a multiple length quotient keep the same sign, the remainder is always the same sign as the dividend. Fractional or integer operation is possible and division and multiplication operations can be concatenated. For example, the operations (A x B)/C, (A/B) x C can easily be performed. The dividend can be any previously generated result, product, quotient, remainder, or a double or single length signed operand.

Reading Results

Results of an arithmetic operation, or string of operations, can be read onto the 16 (8) bit bus if the machine is at the end of an operation or at the start of a new sequence. The read operation requires that the load signal is held Low whereby the information is read out onto the bi-directional bus when Code 7 is specified. (See Figure 5) Since there is a double length accumulator Z,W reading can take two time periods. First register Z is read out, this could be the most significant half of a product, or the quotient during a division operation. After a clock has been received and Code 7 is still present, the least significant half of the product from the W register is placed on the bus, or the remainder if a division operation was performed.

If the machine is asked to perform a read during the loading sequence then the sequence is broken and the machine is forced back to state 0 ready to start the sequence again. Continual read operations at state 0 just swap the contents of register Z and W.

Initialization of the 67516 Multiplier/Divider can easily be performed by continually calling out Code 7 which after a maximum of 21 (13) clock periods forces the machine back to State 0. The 67508/18 have a direct Reset line.

Integer and Fractional Arithmetic

The 67516 (67508) can work in either fractional or integral number representations. When working with integers all numbers are scaled from the least significant end and the least significant bit is assumed to have a weight of 2^0. For integer multiplication, accumulation, and division, all numbers are scaled from this least significant weight, and results are correct if interpreted in this manner. The double length register Z,W can therefore hold numbers in the range -2^{31} to $+2^{31}-1$ (-2^{15} to $+2^{15}-1$) and the operands X and Y and single length results are in the range -2^{15} to $+2^{15}-1$ (-2^7 to $+2^7-1$).

When working with fractions, the machine automatically performs scaling so that input operands and result have a consistent format. All numbers in the fractional representation are scaled from the most significant end which has a weight of 2^0 and is negative. The binary point is one place to the right of this most significant bit, so that the next bit has a weight of 2^{-1}. The double length register Z,W therefore holds numbers in the range -1 to $+1 - 2^{-31}$ (2^{-15}) and the operand X and Y and single length results are in the range -1 to $+1 - 2^{15}$ (2^7). Since automatic scaling occurs, the product of two numbers always has the least significant bit as a 0 unless an accumulation is performed with the least significant bit as a 1.

During a chain operation with the partial results not being read onto the bus, the machine will stay in either the fractional or integer mode. At the start of a sequence of operations, integer or fraction operation is designated by loading operands with Code 6 or Code 5 respectively.

Mixed fraction and integer working is possible by re-defining the weight of the least or most significant bit. Care, however, must be exercised due to the automatic scaling feature when fractional arithmetic is programmed.

Rounding

Rounding can be performed on the result of a multiplication or division. Generally rounding would only be called out during fractional operation but nothing in the machine precludes forming a rounded result during integer working.

Rounding for multiplication provides the best single length most significant half of the product. Rounding occurs at the end of a multiplication and is performed instead of a Load or Read operation. The machine looks at the most significant bit of the least significant half of the product (W_{15} or W_7) and adds 1 to the most significant half of the product at the least significant end if W_{15} (W_7) is a 1. After the operation the machine is in state 0 so that the rounded product can be read, and the W register is clear.

Division rounding is performed by forcing the least significant bit of the quotient in Z to a 1 unless the division is exact (remainder is zero). This method of rounding causes a slightly higher variance in the result than having an additional iterative division operation, but is considerably easier to perform. Again after rounding the machine goes to state 0 so that a read operation can be performed, and the W register is clear.

Overflow

The machine has an overflow output which is cleared prior to an operation and is set during an operation if the product or quotient goes outside the normally accepted range.

For multiplication, overflow can only occur if the most negative number in the operand range is used. $-1X\ -1 = +1$ which cannot be held in the machine. Overflow can more easily occur during accumulation of products either positively or negatively. For fractional working, if the product or accumulation goes outside the range of -1 to $+1\ -2^{-31}$ then the overflow flip-flop will be set.

Division overflow also occurs if the quotient goes outside the generally accepted number range of -1 to $+1\ -2^{-15}$ (2^{-7}) during fractional operation. This would occur if the divisor is less than the dividend or equal to the dividend if a positive quotient is being generated. For integer working the numbers must be scaled by 2^{15} (2^7).

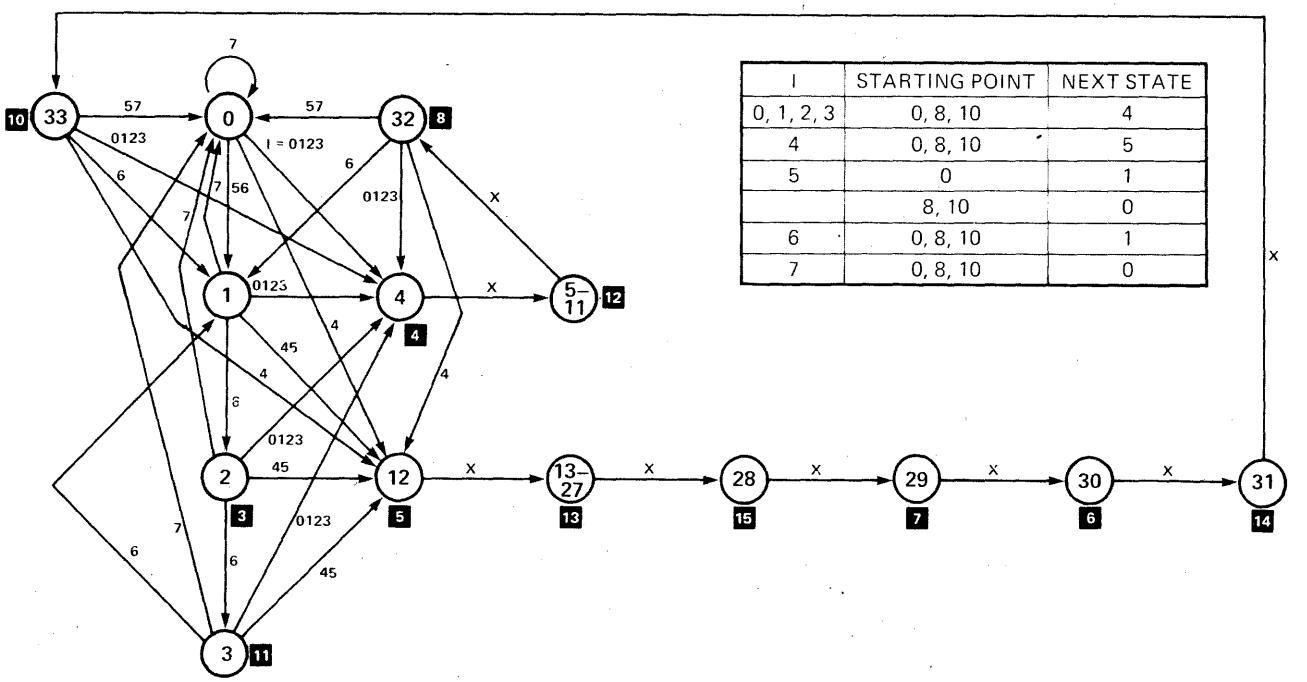
Timing

General timing waveforms are shown in Figure 6. Specific examples are shown in Figures 7 and 8.

CODE $I_2I_1I_0$	STATE 0	1	2	3	MULTIPLY	DIVIDE	END MULTIPLY	END DIVIDE
000 LOAD MULT CLR POS	X_1Y SM	XY SM	XY + Z SM	XY + Z, W SM	MULTIPLY	DIVIDE	X_1Y SM	X_1Y SM
001 LOAD MULT CLR NEG	$-X_1Y$ SM	-XY SM	-XY + Z SM	-XY + Z, W SM	MULTIPLY	DIVIDE	$-X_1Y$ SM	$-X_1Y$ SM
010 LOAD MULT POS	X, Y + KZ, KW SM	XY + KZ, KW SM	XY + K_Z2^{-15} SM	XY + Wsig. SM	MULTIPLY	DIVIDE	X_1Y + KZ, KW SM	X_1Y + KZ, KW SM
011 LOAD MULT NEG	-X, Y +KZ, KW SM	-XY + KZ, KW SM	-XY + K_Z2^{-15} SM	-XY + Wsig. SM	MULTIPLY	DIVIDE	$-X_1Y$ +KZ, KW SM	$-X_1Y$ + KZ, KW SM
100 LOAD DIVIDE	$\frac{KZ, KW}{X_1}$ SD	$\frac{KW}{X}$ SD	$\frac{Z, W}{X}$ SD	$\frac{Wuns.}{X}$ SD	MULTIPLE	DIVIDE	$\frac{KZ, KW}{X_1}$ SD	$\frac{KZ, KW}{X_1}$ SD
101 LOAD FR. & DIVIDE & RND.	LOAD FR S1	$\frac{KZ}{X}$ SD	$\frac{Z}{X}$ SD	$\frac{Wsig.}{X}$ SD	MULTIPLY	DIVIDE	ROUND MULTIPLY S0	ROUND DIVIDE S0
110 LOAD INT.	LOAD INT S1	LOAD S2	LOAD S3	LOAD S1	MULTIPLE	DIVIDE	LOAD S1	LOAD S1
111 READ	READ S0	READ S0	READ S0	READ S0	MULTIPLY	DIVIDE	READ S0	READ S0

KZ, KW PREVIOUSLY GENERATED Z, W
X_1 PREVIOUSLY LOADED X

Table 1 67516 (16 x 16) and 67508 (8 x 8) Multiply/Divide State Table & Operations



I	STARTING POINT	NEXT STATE
0, 1, 2, 3	0, 8, 10	4
4	0, 8, 10	5
5	0	1
	8, 10	0
6	0, 8, 10	1
7	0, 8, 10	0

Figure 1 Transition Table Multiplier/Divider

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OPERATION		TIME SLOT 1	2	3	4	5	6	7	8	9	10	11	12
X, Y	INS CODE	0	MULTIPLY										
	BUS	Y											
-X, Y	INS CODE	1	MULTIPLY										
	BUS	Y											
X, Y + K_Z, K_W	INS CODE	2	MULTIPLY										
	BUS	Y											
-X, Y + K_Z, K_W	INS CODE	3	MULTIPLY										
	BUS	Y											
XY	INS CODE	5/6	0	MULTIPLY									
	BUS	X	Y										
-XY	INS CODE	5/6	1	MULTIPLY									
	BUS	X	Y										
XY + K_Z, K_W	INS CODE	5/6	2	MULTIPLY									
	BUS	X	Y										
-XY + K_Z, K_W	INS CODE	5/6	3	MULTIPLY									
	BUS	X	Y										
XY + Z	INS CODE	5/6	6	0	MULTIPLY								
	BUS	X	Z	Y									
-XY + Z	INS CODE	5/6	6	1	MULTIPLY								
	BUS	X	Z	Y									
XY + $K_Z 2^{-(n-1)}$	INS CODE	5/6	6	2	MULTIPLY								
	BUS	X	–	Y									
-XY + $K_Z 2^{-(n-1)}$	INS CODE	5/6	6	3	MULTIPLY								
	BUS	X	–	Y									
XY + Z, W	INS CODE	5/6	6	6	0	MULTIPLY							
	BUS	X	Z	W	Y								
-XY + Z, W	INS CODE	5/6	6	6	1	MULTIPLY							
	BUS	X	Z	W	Y								
XY + Wsign	INS CODE	5/6	6	6	2	MULTIPLY							
	BUS	X	–	W	Y								
-XY + Wsign	INS CODE	5/6	6	6	3	MULTIPLY							
	BUS	X	–	W	Y								

NOTES: 1) X1 IS CONTENTS OF 1ST RANK OF X REGISTER (EITHER OLD X OR A NEW X).

2) $KZ2^{(n-1)}$ IS A SINGLE LENGTH SIGNED NUMBER THE MOST SIGNIFICANT HALF OF THE PREVIOUS PRODUCT ADDED IN AT THE LEAST SIGNIFICANT END.

3) W SIGN IS A SINGLE LENGTH SIGNED NUMBER.

4) INTEGER OR FRACTIONAL WORKING IS SPECIFIED BY HAVING THE LAST BUT ONE OPERAND LOADED WITH A 6 OR 5 RESPECTIVELY.

Figure 2 Multiplication Codes and Times for 16 x 16 (For 8 x 8 Timing is Reduced by 4 Cycles)

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OPERATION		1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24
K_Z, K_W/X_1	INS CODE	4																							
	BUS	–								DIVIDE												I	NOTE 2		
K_W/X	INS CODE	5/6	4																						
	BUS	X	–							DIVIDE													I		
K_Z/X	INS CODE	5/6	5																						
	BUS	X	–							DIVIDE													I		
Z, W/X	INS CODE	5/6	6	4																					
	BUS	X	Z	W						DIVIDE														I	
Z/X	INS CODE	5/6	6	5																					
	BUS	X	Z	–						DIVIDE														I	
W/X	INS CODE	5/6	6	6	4																				
	BUS	X	–	W	–					DIVIDE															I
W_S/X	INS CODE	5/6	6	6	5																				
	BUS	X	0	W	–					DIVIDE															I

NOTES: 1) X_1 IS CONTENTS OF 1ST RANK OF X REGISTER (EITHER OLD X OR A NEW X)

2) FRACTIONAL DIVISION DIVIDES A 31 BIT 2'S COMPLEMENT NUMBER IN 1 CLOCK PERIOD LESS THAN INTEGER DIVISION.

3) W_{sign} IS A SINGLE LENGTH SIGNED NUMBER.

4) DIVISION OPERATION W_S/X DEMANDS THAT Z REGISTER IS INITIALIZED WITH ALL 0'S AT LOADING INTERVAL FOR Z.

5) INTEGER OR FRACTIONAL WORKING IS SPECIFIED BY HAVING THE LAST BUT ONE OPERAND LOADED WITH A 6 OR 5 RESPECTIVELY.

Figure 3 Division Codes and Time for 32/16 (For 16/8 Timing is Reduced by 8 Cycles)

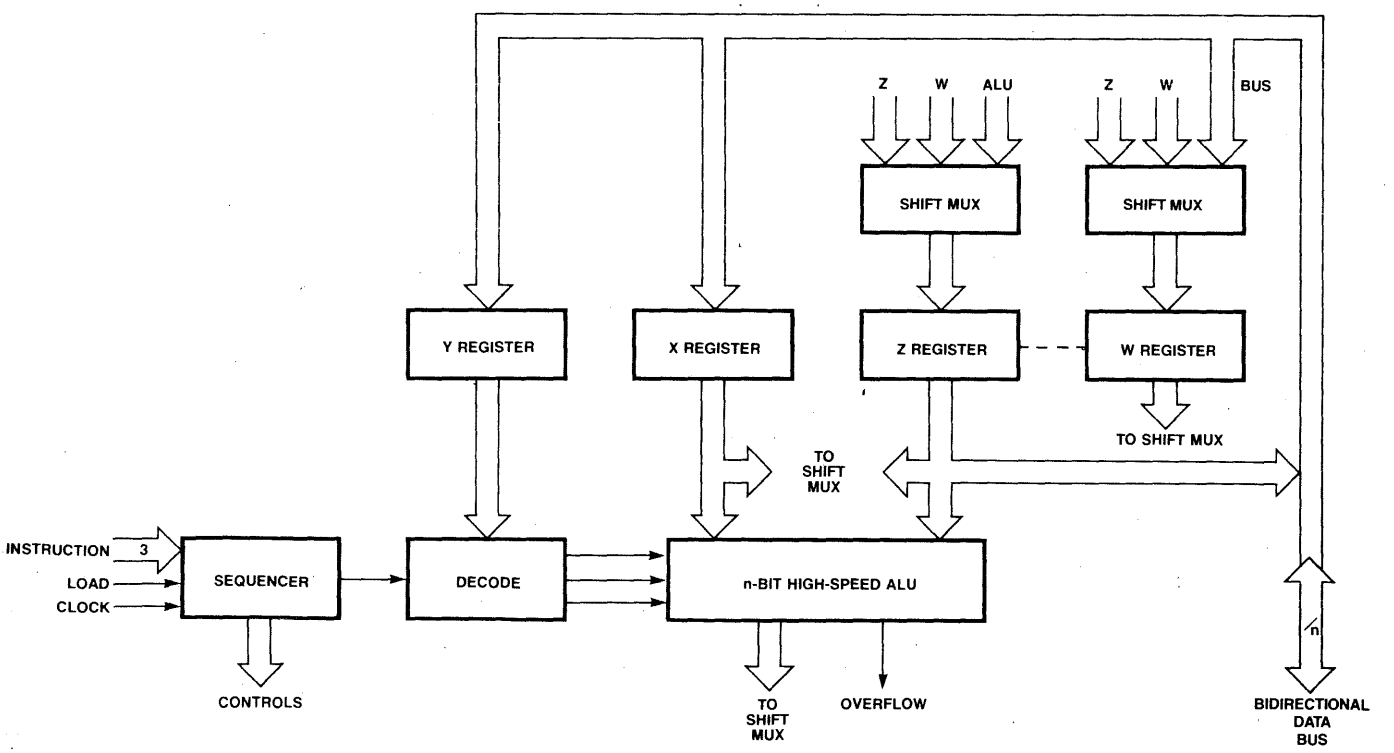
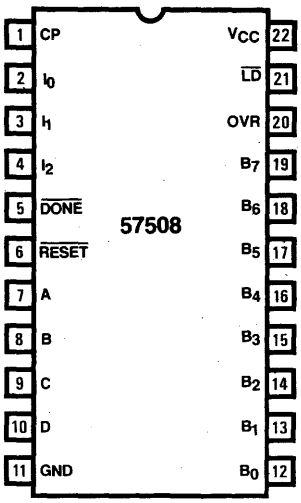


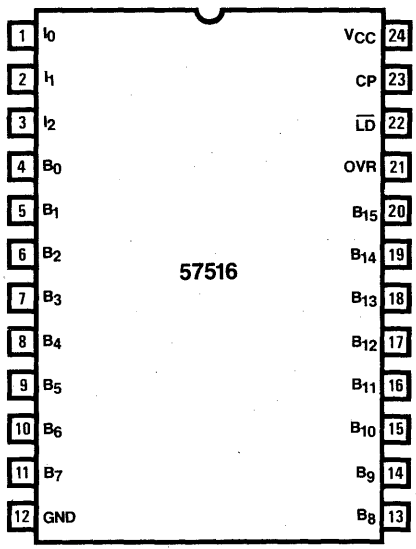
Figure 4 Multiply/Divide Processor Family

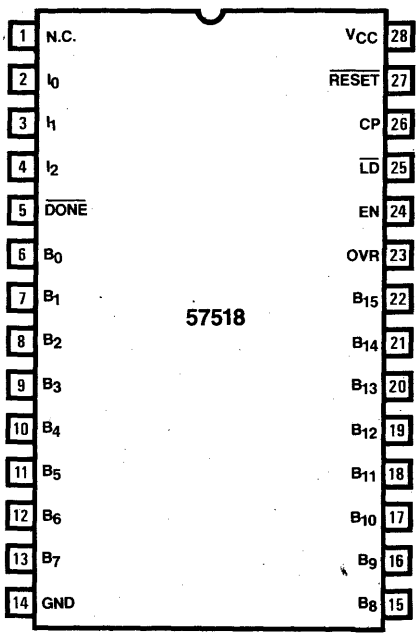
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8 x 8 Multiplier/Divider Pin-out



16 x 16 Multiplier/Divider Pin-out





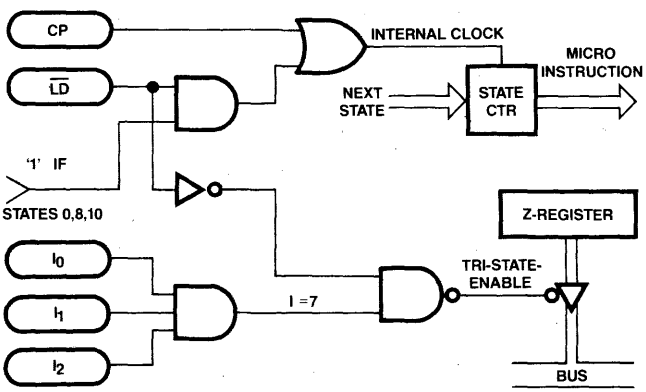


Figure 5. 67516/08 Internal Circuitry of "Load" Line and Tri-State-Enable.

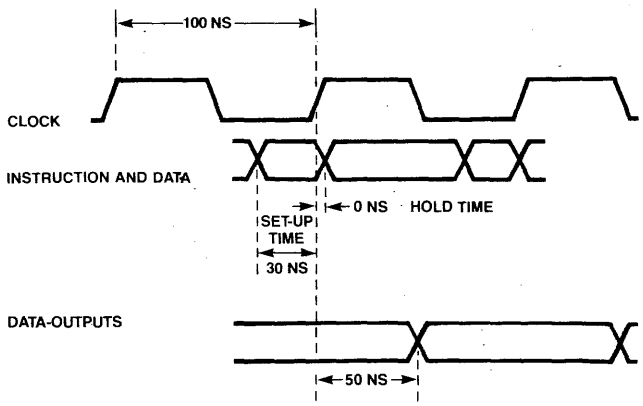


Figure 6. Timing Diagram 67516/67508 (Preliminary)

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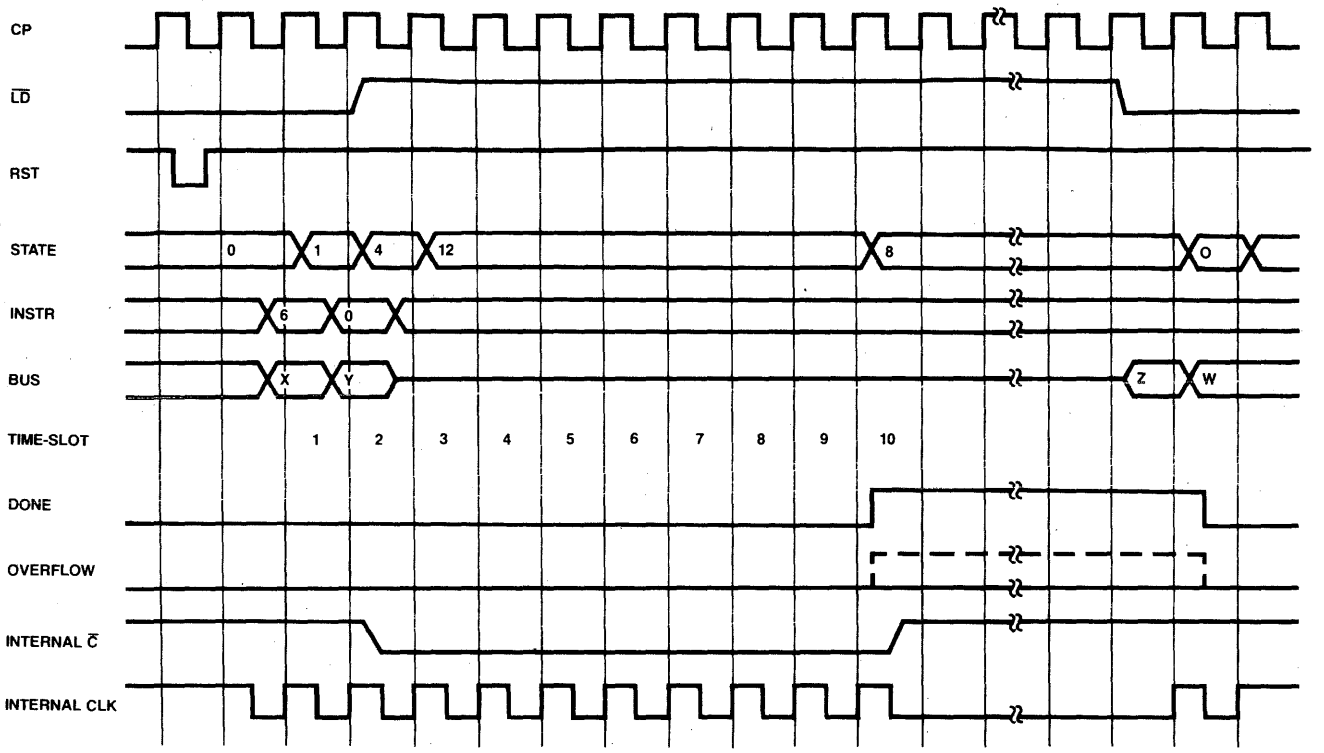


Figure 7. Example #1 Load X, Load Y, Multiply, Wait, Read Z, Read W.

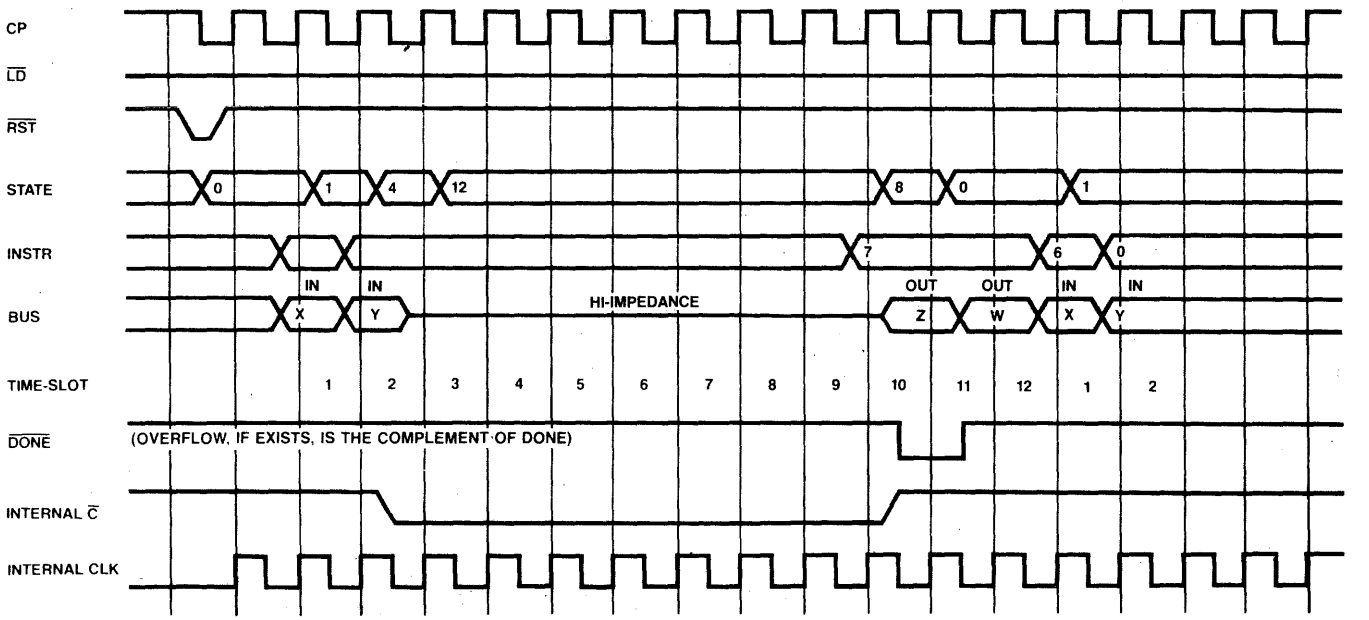


Figure 8. Example #2: Repeat: "Load X, Load Y, Multiply, Read Z, Read W".

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Octal Latches, Octal Registers With Three-State Outputs

Features/Benefits

- Inverting and Non-Inverting Outputs
- Up to 32 mA I_{OL}
- 3-State Outputs Drive Bus Lines
- 20 Pin Skinny DIP™ Saves Space
- 8 Bits Matches Byte Boundaries
- Hysteresis Improves Noise Margin
- Low Current PNP Inputs Reduce Loading
- Ideal for Microprocessor Interface

Latch Function Table

$\overline{OE}$	G	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

Register Function Table

$\overline{OE}$	CK	D	Q
L	↑	H	H
L	↑	L	L
L	L	X	Q_0
H	X	X	Z

Inverting Latch Function Table

$\overline{OE}$	G	D	$\overline{Q}$
L	H	H	L
L	H	L	H
L	L	X	Q_0
H	X	X	Z

Inverting Register Function Table

$\overline{OE}$	CK	D	$\overline{Q}$
L	↑	H	L
L	↑	L	H
L	L	X	Q_0
H	X	X	Z

PART NUMBER	PKG	TEMP	I_{OL}	POLARITY	TYPE	POWER
SN74LS373 SN54LS373	N,J J	com mil	24mA 12mA	Non-invert	Latch	LS
67LS380 57LS380	N,J J	com mil	24mA 12mA	Invert		
SN74LS374 SN54LS374	N,J J	com mil	24mA 12mA	Non-invert	Register	
67LS376 57LS376	N,J J	com mil	24mA 12mA	Invert		
SN74S373 SN54S373	N,J J	com mil	20mA	Non-invert	Latch	S
67S373 57S373	N,J J	com mil	32mA			
67S380 57S380	N,J J	com mil	20mA	Invert		
67S382 57S382	N,J J	com mil	32mA			
SN74S374 SN54S374	N,J J	com Mil	20mA	Non-invert	Register	
67S374 57S374	N,J J	com mil	32mA			
67S376 57S376	N,J J	com mil	20mA	Invert		
67S378 57S378	N,J J	com mil	32mA			

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Description

The latch passes eight (octal) bits of data from the inputs (D) to the outputs (Q) when the gate (G) is high. The data is "latched" when the gate (G) goes low. The register loads eight (octal) bits of input data and passes it to the output on the "rising edge" of the clock.

The three state outputs are active when OE is low, and high impedance when OE is high. Schmitt-trigger buffers at the gate/clock inputs improve system noise margin by providing typically 400 mV of hysteresis.

In addition to the standard S and LS latches and Registers, Monolithic Memories provides these enhancements:

1) Increased output sink current (I_{OL}) from the standard Schottky I_{OL} of 20 mA to an improved 32 mA.

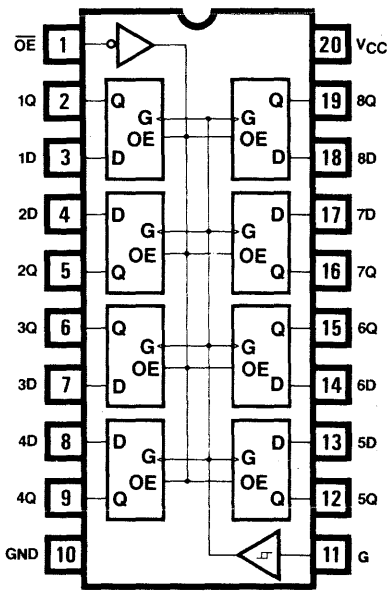
2) Inverting outputs instead of the standard non-inverting outputs.

The higher I_{OL} is intended for upgrading systems which presently satisfy 32 mA requirements with SN54/74365, 366, 367, 368, Hex Buffers. The inverting outputs are intended for bus applications that require inversion as in interfacing the Am2901A 4-Bit Slice to an active low bus.

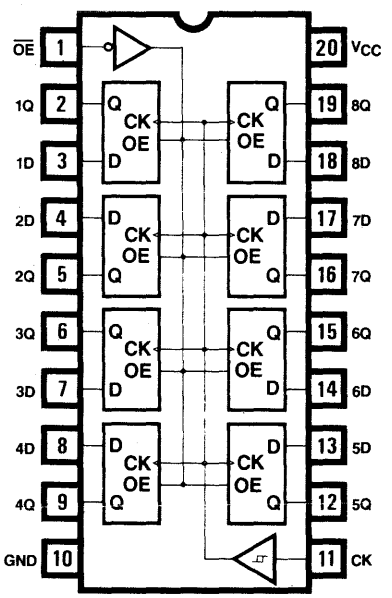
All of the octal devices are packaged in the popular 20 in. Skinny DIP.™

Logic Symbols

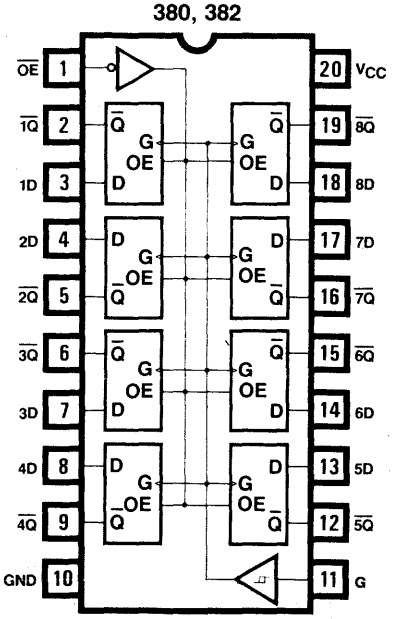
Octal Latch
373



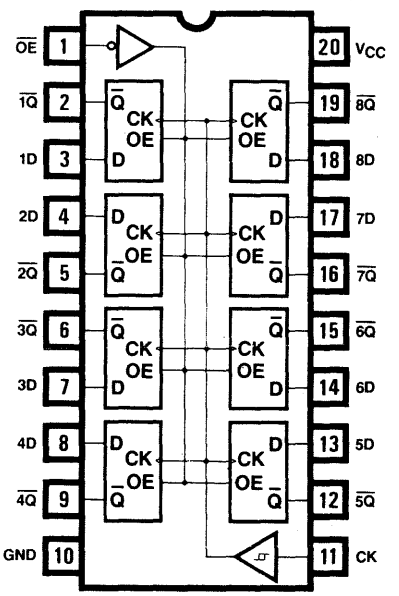
Octal Register
374



Octal Latch (Inverting)
380, 382



Octal Register (Inverting)
376, 378



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Absolute Maximum Ratings

Supply Voltage, V_{CC} 7V
Input Voltage 5.5V
Off-state ouptut voltage 5.5V
Storage temperature range ..... −65°C to +150°C

Recommended Operating Conditions

SYMBOL	PARAMETER	MILITARY MIN	MILITARY NOM	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL NOM	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
I_{OH}	High-level output current			−12			−15	mA
I_{OL}	Low-level output current			48			64	mA
T_A	Operating free-air temperature	−55		125*	0		70	°C

*The SN54S241/244J operating at free air temperature above 116°C requires a heat sink such that $R_{\theta CA}$ is not more than 40°C/W

Electrical Characteristics Over Recommended Operating Free Air Temperature Range

SYMBOL	PARAMETER			CONDITIONS		S240, S306 MIN	S240, S306 TYP	S240, S306 MAX	S241, S244 MIN	S241, S244 TYP	S241, S244 MAX	UNIT
V_{IH}	High-level input voltage					2			2			V
V_{IL}	Low-level input voltage							0.8			0.8	V
V_{IC}	Input clamp voltage			V_{CC} = MIN, I_I = −18mA				−1.2			−1.2	V
	Hystersis ($V_{T+} - V_{T-}$)			V_{CC} = MIN		0.2	0.4		0.2	0.4		V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2V	74S	V_{IL} = 0.8V, I_{OH} = −1mA		2.7			2.7			V
			54S 74S	V_{IL} = 0.8V, I_{OH} = −3mA		2.4	3.4		2.4	3.4		
			54S 74S	V_{IL} = 0.5V, I_{OH} = MAX		2			2			
V_{OL}	Low-level output voltage			V_{CC} = MIN, V_{IH} = 2V, V_{IL} = 0.8V, I_{OL} = MAX				0.55			0.55	V
I_{OZH}	Off-state output current			V_{CC} = MAX, V_{IH} = 2V, V_{IL} = 0.8V	V_O = 2.4V			50			50	μA
I_{OZL}					V_O = 0.5V			−50			−50	
I_I	Maximum input current			V_{CC} = MAX, V_I = 5.5V				1			1	mA
I_{IH}	High-level input current			V_{CC} = MAX, V_I = 2.7V				50			50	μA
I_{IL}	Low-level input current	Any A		V_{CC} = MAX, V_I = 0.5V				−400			−400	μA
		Any E						−2			−2	mA
I_{OS}	Short circuit output current[1]			V_{CC} = MAX		−50		−225	−50		−225	mA
I_{CC}	Supply current	Outputs high		V_{CC} = MAX, Outputs Open	Military		80	123		95	147	mA
					Commercial		80	135		95	160	
		Outputs low			Military		100	145		120	170	
					Commercial		100	150		120	180	
		Outputs disabled			Military		100	145		120	170	
					Commercial		100	150		120	180	

Switching Characteristics V_{CC} = 5 V, T_A = 25°C

SYMBOL	PARAMETER	TEST CONDITIONS	S240, S306 MIN	S240, S306 TYP	S240, S306 MAX	S241, S244 MIN	S241, S244 TYP	S241, S244 MAX	UNIT
t_{PLH}	Data to output delay	C_L = 50 pF, R_L = 90Ω, See Page 10-4		4.5	7		6	9	ns
t_{PHL}				4.5	7		6	9	ns
t_{PZL}	Output enable delay			10	15		10	15	ns
t_{PZH}				6.5	10		8	12	ns
t_{PLZ}	Output disable delay	C_L = 5 pF, R_L = 90Ω, See Page 10-4		10	15		10	15	ns
t_{PHZ}				6	9		6	9	ns

Absolute Maximum Ratings

Supply Voltage, V_{CC} 7V
Input Voltage 5.5V
Off-State Output Voltage 5.5V
Storage Temperature Range ..... −65°C to +150°C

Recommended Operating Conditions

SYMBOL	PARAMETER		MILITARY MIN	MILITARY NOM	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL NOM	COMMERCIAL MAX	UNIT
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{OH}	High Level Output Voltage				5.5			5.5	V
I_{OH}	High Level Output Current				−2			−6.5	mA
t_W	Width of Clock/Gate	High	6			6			ns
		Low	7.3			7.3			ns
t_{SU}	Set Up Time	Latch	0↓			0↓			ns
		Register	5↑			5↑			ns
t_H	Hold Time	Latch	10↓			10↓			ns
		Register	2↑			2↑			ns
T_A	Operating Free Air Temperature		−55		125	0		70	°C

Electrical Characteristics Over Recommended Operating Free Air Temperature Range

SYMBOL	PARAMETER		CONDITIONS		MIN	TYP	MAX	UNIT
V_{IH}	High Level Input Voltage				2			V
V_{IL}	Low Level Input Voltage						0.8	V
V_{IC}	Input Clamp Voltage		V_{CC} = MIN, I_I = −18 mA				−1.2	V
V_{OH}	High Level Output Voltage		V_{CC} = MIN, V_{IH} = 2V, I_{OH} = MAX V_{IL} = 0.8V		2.4	3.1		V
V_{OI}	Low Level Output Voltage	SN54/74S373 57/67S380 SN54/74S374 57/67S376	V_{CC} = MIN V_{IL} = 0.8V V_{IH} = 2V	I_{OL} = 20 mA			0.5	V
		57/67S373 57/67S382 57/67S374 57/67S378		I_{OL} = 32 mA				
I_{HZ}	High Level Off-State Output Current		V_{CC} = MAX, V_O = 2.4V, V_{IH} = 2V				50	μA
I_{LZ}	Low Level Off-State Output Current		V_{CC} = MAX, V_O = 0.5V, V_{IH} = 2V				−50	μA
I_I	Input Current at MAX V_I		V_{CC} = MAX, V_I = 5.5V				1	mA
I_{IH}	High Level Input Current		V_{CC} = MAX, V_I = 2.7V				50	μA
I_{IL}	Low Level Input Current		V_{CC} = MAX, V_I = 0.5V				−250	μA
I_{OS}	Output Short Circuit Current		V_{CC} = MAX		−40		−100	mA
I_{CC}	Supply Current	Latch	V_{CC} = MAX			105	160	mA
		Register	V_{CC} = MAX			90	140	mA

Switching Characteristics V_{CC} = 5V, T_A = 25°C

SYMBOL	PARAMETER	CONDITIONS	LATCH MIN	LATCH TYP	LATCH MAX	REGISTER MIN	REGISTER TYP	REGISTER MAX	UNIT
f_{MAX}	Maximum Clock Frequency	C_L = 15 pF R_L = 280Ω See Page 10-4				75	100		MHz
t_{PLH}	Data to Output Delay			5	9				ns
t_{PHL}				9	13				ns
t_{PLH}	Clock/Gate to Output Delay			7	14		8	15	ns
t_{PHL}				12	18		11	17	ns
t_{PZH}	Output Enable Delay			8	15		8	15	ns
t_{PZL}				11	18		11	18	ns
t_{PHZ}	Output Disable Delay	C_L = 5pF See R_L = 280Ω Page 10-4		6	9		5	9	ns
t_{PLZ}				8	12		7	12	ns

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Octal Registers With Clear and Clock Enable

Features

- **Inverting and non-inverting outputs**
- **Slim 20-pin Skinny DIP™ saves space**
- **8 bits matches byte boundaries**
- **Ideal for microprogram instruction register**
- **Ideal for microprocessor interface**

Description

These Octal registers contain 8 D-type flip-flops and feature very low I_{CC} (17 mA typ). The LS273 and LS313 registers are loaded on the rising edge of the clock (CK) and asynchronously cleared whenever the $\overline{\text{CLEAR}}$ line is low. The LS377 and LS314 are loaded on the rising edge of the clock provided the clock enable line, $\overline{\text{CK EN}}$ is low.

PART NUMBER	PKG	TEMP	POLARITY	CONTROL OPTION
SN74LS273 SN54LS273	N,J J	com mil	Non-invert	Clear
67LS313 57LS313	N,J J	com mil	Invert	Clear
SN74LS377 SN54LS377	N,J J	com mil	Non-invert	Clock Enable
67LS314 57LS314	N,J J	com mil	Invert	Clock Enable

Function Table LS273, LS313

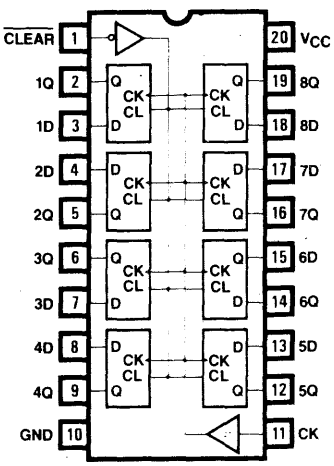
INPUTS			OUTPUT	
CLEAR	CLOCK	D	Q	$\overline{Q}$
L	X	X	L	H
H	↑	H	H	L
H	↑	L	L	H
H	L	X	Q_0	$\overline{Q}_0$

Function Table LS377, LS314

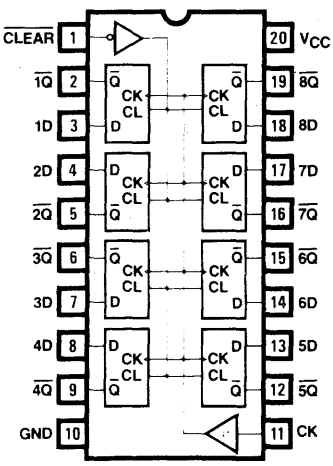
INPUTS			OUTPUTS	
$\overline{\text{CK EN}}$	CLOCK	DATA	Q	$\overline{Q}$
H	X	X	Q_0	$\overline{Q}_0$
L	↑	H	H	L
L	↑	L	L	H
X	L	X	Q_0	$\overline{Q}_0$

Logic Symbols

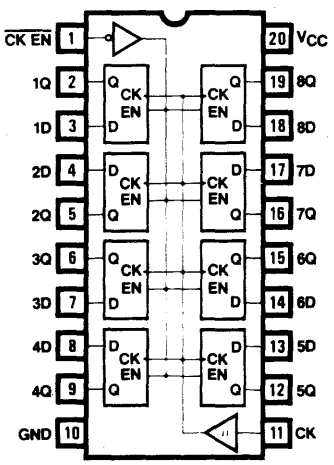
Octal Register with clear
LS273



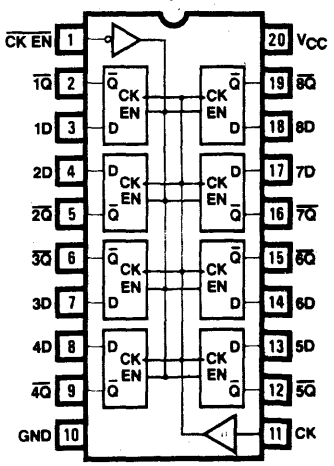
Octal Register with clear (inverting)
LS313



Octal Register with clock enable
LS377



Octal Register with clock enable (inverting)
LS314



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Absolute Maximum Ratings

Supply Voltage, V_{CC} 7V
Input Voltage 7V
Off-State Output Voltage 7V
Storage Temperature Range ..... −65°C to +150°C

Recommended Operating Conditions

SYMBOL	PARAMETER		MILITARY MIN	MILITARY NOM	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL NOM	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	4.75	5	5.25	V
I_{OH}	High-level output current				−400			−400	μA
I_{OL}	Low-level output current				4			8	mA
f_{clock}	Clock frequency		0		30	0		30	MHz
t_W	Width of clock or clear pulse		20			20			ns
t_{su}	Set-up time	Data input	20↑			20↑			ns
		Clear inactive state	25↑			25↑			
		Enable active state	25↑			25↑			
		Enable inactive state	10↑			10↑			
t_h	Data hold time		5↑			5↑			ns
T_A	Operating free-air temperature		−55		125	0		70	°C

Electrical Characteristics

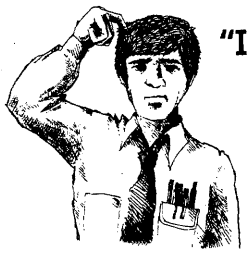
Over Recommended Operating Free-Air Temperature Range

SYMBOL	PARAMETER	TEST CONDITIONS		MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.8			0.8	V
V_{HC}	Input clamp voltage	V_{CC} = MIN, I_I = −18 mA				−1.5			−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL}MAX, I_{OH} = −400 μA		2.5	3.4		2.7	3.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL}MAX	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
			I_{OL} = 8 mA					0.35	0.5	
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7 V				0.1			0.1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7 V				20			20	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = −0.4 V				−0.4			−0.4	mA
I_{OS}	Short-Circuit output current	V_{CC} = MAX		−20		−100	−20		−100	mA
I_{CC}	Supply current	V_{CC} = MAX,	LS273 LS315		17	27		17	27	mA
			LS377 LS314		17	28		17	28	mA

Switching Characteristics, V_{CC} = 5 V, T_A = 25°C

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{MAX}	Maximum clock frequency	C_L = 15 pF, R_L = 2 kΩ, See Page 10-4	30	40		MHz
t_{PHL}	Propagation delay time, high-to-low-level output from clear			18	27	ns
t_{PLH}	Propagation delay time, low-to-high-level output from clock			17	27	ns
t_{PHL}	Propagation delay time, high-to-low-level outut from clock			18	27	ns

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- 1024x1
- CMOS
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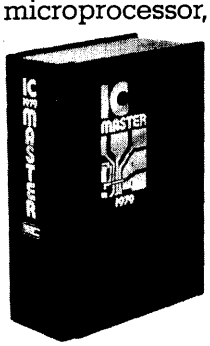
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UTP

PLESSEY SEMICONDUCTORS

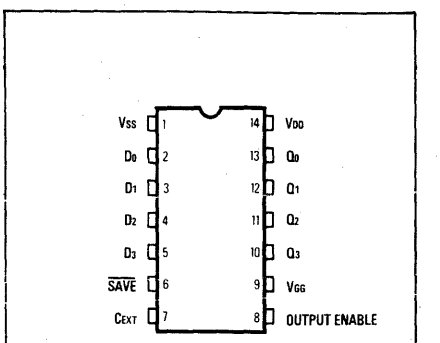
MN9102 NON-VOLATILE LOGIC

PROVISIONAL DATA
MN9102
NON-VOLATILE QUAD LATCH

The Plessey MN9102 is a non-volatile 4-bit data latch which uses MNOS transistors as memory elements to retain stored data in the absence of applied power. The data that is applied to the four inputs is written into the memory when the SAVE control is taken to a logic '0' level and the data subsequently appears on the four outputs. The stored data is also automatically restored to the outputs whenever power is re-applied to the device.

An OUTPUT ENABLE is also available, which when taken to logic '0' level presents a high impedance state on each data output line, permitting multiplexed operation.

The high voltage ususally associated with MNOS memory devices is generated internally, requiring only a single external capacitor to act as a charge reservoir for supplying current when writing into the memory. The device therefore operates from standard voltage rails and requires no additional drive circuitry.



DC14/DG14

Fig. 1. Pin connections (top)

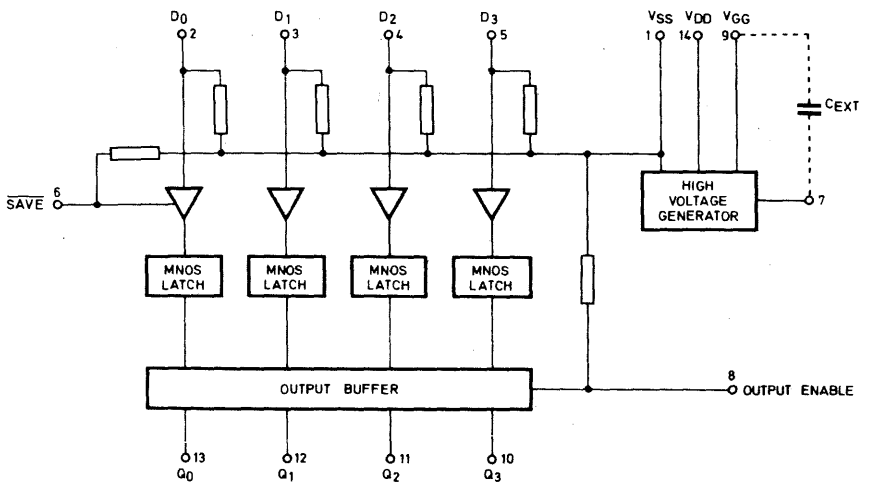


Fig. 2 Block diagram of MN9102

FEATURES

- Data Retention for One Year in the Absence of Applied Power
- Simple to Use
- Standard Power Supplies Only (+5V, −12V)
- CMOS/TTL Compatible
- 14-lead DIL Package
- Typically Ten Million SAVE Operations

APPLICATIONS

- Metering Systems
- Elapsed Time Indicators
- Security Code Storage
- Last Channel Memory for Digital Tuning

ELECTRICAL CHARACTERISTICS

Operating conditions (unless otherwise stated):
V_{SS} = +5V ± 5%
V_{DD} = 0V
V_{GG} = −12V ± 5%
Output loading = 1 TTL load
Ambient operating temperature range including data retention in the absence of applied power:
0°C to +70°C

Characteristic	Symbol	Value			Units	Conditions
		Min.	Typ.	Max.		
Logic '0' input voltage	V_{IL}			0.8	V	Nominal 20kohms internal pullup
Logic '1' input voltage	V_{IH}	V_{SS}−1			V	resistor to V_{SS} on all inputs
Logic '0' output voltage	V_{OL}			0.6	V	Output current = −1.6mA
Logic '1' output voltage	V_{OH}	V_{SS}−1			V	Output current = 100 µA
Output leakage current		−10		+10	µA	$V_{SS} \geqslant V_{OUT} \geqslant V_{DD}$ with OUTPUT ENABLE = V_{DD}
Output voltage on C_{EXT}			−38		V	Load on $C_{EXT} \geqslant$ 10Mohms
External reservoir capacitor	C_{EXT}	0.1		0.47	µF	See note 1
Data set-up time	t_s	1			µs	
Data hold time	t_h	1			µs	
Data settling time	t_d			7	µs	C_{LOAD} = 47pf
Output enable delay	t_o			2.5	µs	C_{LOAD} = 47pf
SAVE time	t_{SAVE}	10			ms	See note 2
SAVE duty cycle				50	%	See note 3
SAVE cycles		10^6	10^7			See note 5
SAVE rise and fall times	t_e			5	µs	
Data retention time		1			year	
Power dissipation			50	100	mW	See note 4

ABSOLUTE MAXIMUM RATINGS
(all voltages with respect to Vss)

Voltage on C_{EXT} −46 to + 0.3V
Voltage on V_{GG} −20 to + 0.3V
Voltage on any other pin −7 to + 0.3V
Storage temperature −55°C to + 125°C
Ambient operating temperature −40°C to + 80°C

The above limits are absolute limiting values beyond which the lifetime and performance of the device may be impaired. No guarantee is implied that the device will function at any condition other than specified under the operating conditions.

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OPERATING NOTES

1. When two or more devices are used, the C_{EXT} outputs may be tied together with a single external capacitor. The size of this capacitor should be increased in proportion to the number of devices.
2. Data can be entered into the latch with SAVE times much less than ten milliseconds, however the retention time is then significantly reduced. It is therefore important that spurious SAVE pulses do not occur, particularly when power is applied to the device.
3. Duty cycles in excess of 50% may be required in certain applications. An external supply (−37V ±5%) must then be used to maintain sufficient voltage on the C_{EXT} output.
4. The majority of the power dissipation arises from the current flow between V_{SS} and V_{GG}. The current level on V_{DD} is the sum of the logic "0" level current plus leakage currents.
5. Exceeding this number of SAVE cycles can cause permanent damage to the device. It should also be noted that rapid changes of data in excess of 10^5 may cause a reduction in the data retention time.

ANTI-STATIC PRECAUTIONS

All inputs have suitable protection devices to minimise the possibility of damage due to static discharge. Care should still be taken when handling the device and the leads should at all times be shorted together until actually incorporated in the circuit in which the device is being used. Care should be taken to avoid static charges occurring in the circuit before completion and soldering should be carried out with an earthed bit.

To ensure no damage occurs during transit, the devices are supplied packed in conducting foam or other suitable carriers.

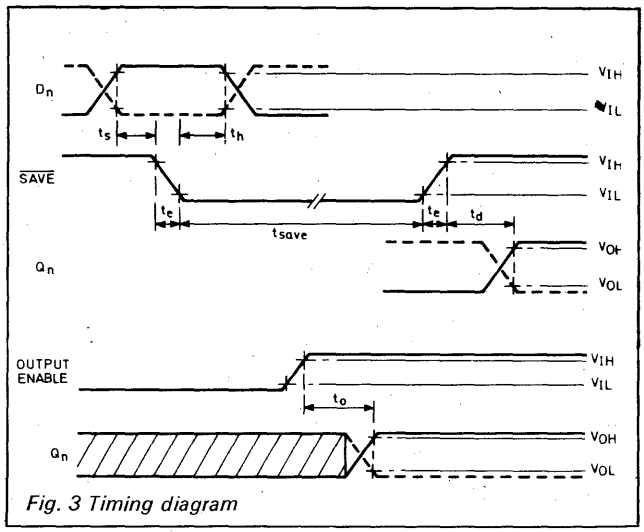
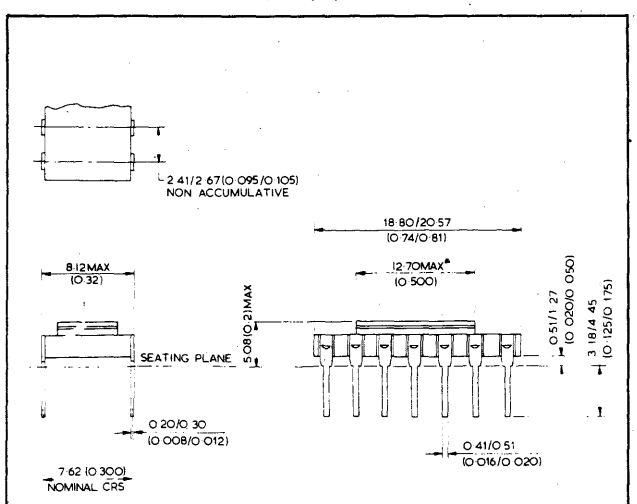


Fig. 3 Timing diagram

PACKAGE DETAILS

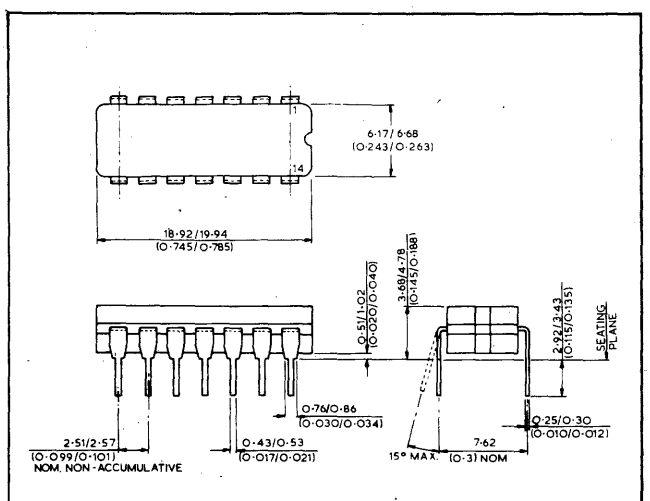
Dimensions are shown thus: mm (in)



14 LEAD DILMON

DC14

Fig. 4



14 LEAD CERAMIC D.I.L.

DG14

Fig. 5

PLESSEY SEMICONDUCTORS

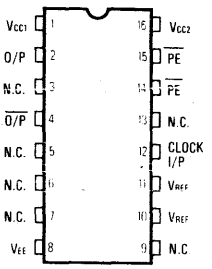
SP8000 SERIES HIGH SPEED DIVIDERS

SP8785B&M 1.0GHz ÷ 20/22
SP8786B&M 1.3GHz ÷ 20/22
UHF PROGRAMMABLE DIVIDERS

FEATURES
- DC to 1.3GHz operation
- 0°C to +70°C operation (B Grade)
- −40 to +85°C operation (M grade)
- Complementary outputs and control inputs are ECL 10K/ECL III compatible.
- AC coupled clock input with wide dynamic range.

QUICK REFERENCE DATA
- Supply voltage $V_{CC}-V_{EE}$ = 5.2V ± .25V
- Power Consumption 440 mW typ (no load)
- ECL compatible
- Maximum input frequency 1GHz (SP8785), 1.3GHz (SP8786)
- Control loop delay time 12 ns typ with 1.3GHz input.

Fig. 1 Pin connections (viewed from above)



DG16

The SP8785 B & M and SP8786 B & M are high speed programmable ÷20/22 counters which operate at input frequencies up to 1.0GHz and 1.3GHz respectively over the temperature ranges 0°C to +70°C (B grade) and −40°C to +85°C (M grade).

The clock input is biased internally and is coupled to the signal source by a capacitor. The input RF path is completed by two input reference decoupling capacitors which are connected to earth.

The division ratio is controlled by two PE inputs. The counter will divide by 20 when either input is in the high state and by 22 when both inputs are in the low state. These inputs are ECL III/10K compatible and have internal 4.3KΩ pulldown, unused inputs may therefore be left open. When using the device as a ÷20 prescaler the inverse output should be connected to a PE input.

In keeping with the device performance the complementary outputs are ECL 10K compatible.

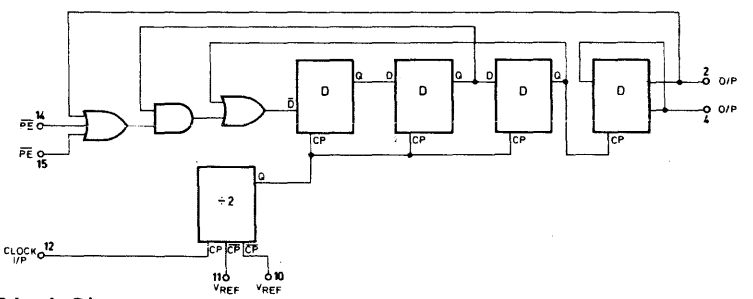


Fig. 2 Logic Diagram

Clock Pulse	Q1	Q2	Q3	Q4
2	L	H	H	H
4	L	L	H	H
6	L	L	L	H
8	H	L	L	H
10	H	H	L	H
12	L	H	H	L
14	L	L	H	L
16	L	L	L	L
18	H	L	L	L
20	H	H	L	L
22	H	H	H	H

$\overline{PE}$	PE	DIV RATIO
L	L	22
H	L	20
L	H	20
H	H	20

The maximum possible loop delay for control is obtained if the L → H transition from Q4 or the H → L transition from Q4 is used to clock the stage controlling the ÷20/22. The loop delay is 20 clock periods minus the internal delays of the ÷20/22 circuit.

ELECTRICAL CHARACTERISTICS

Test conditions (unless otherwise stated):
Tamb 0°C to +70°C (B Grade)
−40°C to + 85°C (M Grade)
Supply voltage V_{CC}=OV
V_{EE}=−5.2V*

Static characteristics

Characteristic	Value Min.	Typ.	Max.	Units	Conditions
PE input voltage V_{INH}	−.96		V_{CC}	V	Tamb = 25°C
V_{INL}	V_{EE}		−1.62	V	see note 2
PE input pulldown resistor		4.3		KΩ	
Output Voltage levels					
V_{OH}	−.93		−.78	V	Tamb = 25°C
V_{OL}	−1.85		−1.62	V	430Ω from o/p to V_{EE} see note 2
Power supply current		85	115	mA	No load

* The SP8785/6 may be operated with a +5.2V supply provided sufficient care is taken with supply decoupling and interfacing of input and outputs.

Dynamic characteristics

Characteristic	Value Min.	Typ.	Max.	Units	Conditions
Max. toggle frequency					
SP8786	1300			MHz	See Note 3
SP8785	1000			MHz	
Min. frequency sinewave drive			150	MHz	
Min. slew rate of square wave for correct operation to D.C.			200	V/μS	
Propagation delay clock input to output		2.5		μS	
Set up time		.5		nS	See note 4
Release time		.5		nS	See note 5

NOTES:
1. Correct operation is specified for $V_{CC} - V_{EE}$ = 5.2V ±.25V.
2. The input threshold and output voltage levels have the same temperature coefficient as ECL 111/10K.
3. The devices are dynamically tested using the circuit shown in Fig. 4 with input amplitudes of 400 and 1000 mVpp over the full temperature range.
4. Set up is defined as the minimum time that can elapse between a L → H transition of control input and the last L → H clock pulse transition to ensure the ÷20 mode is selected.
5. Release time is defined as the minimum time that can elapse between a H → L transition of the control input and the last L → H clock pulse transition to ensure the ÷22 mode is selected.

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SP8000 SERIES
HIGH SPEED DIVIDERS

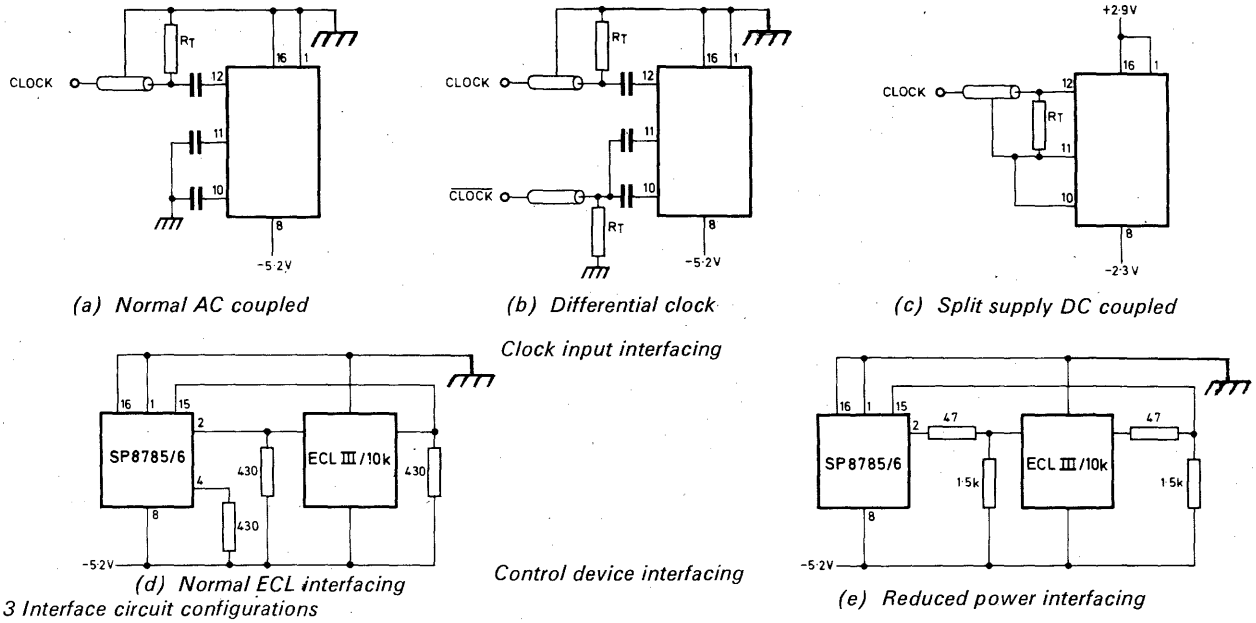


Fig. 3 Interface circuit configurations

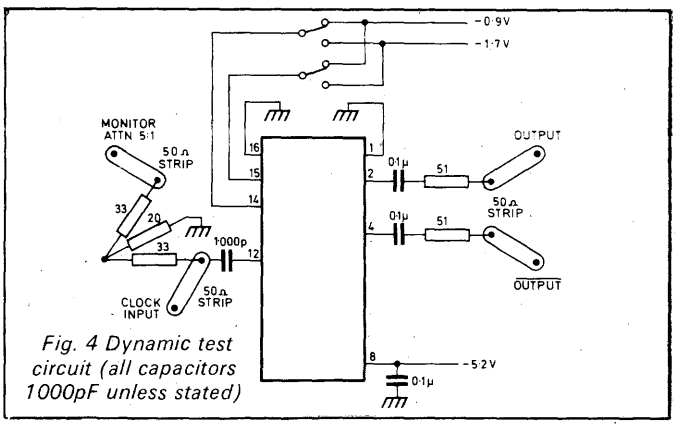


Fig. 4 Dynamic test circuit (all capacitors 1000pF unless stated)

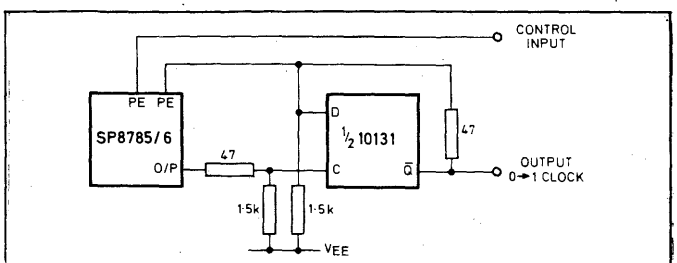


Fig. 5 40/42 control loop delay time 24ns typ

OPERATING NOTES

It is recommended that high frequency construction techniques are used with these devices with the positive rail connected to a ground plane. All components used in the circuit layout should be suitable for the frequencies involved.

The clock input to the device is normally capacitively coupled to the signal source as shown in Fig. 3a. The input is self biased by an internal 400Ω resistor to a bias voltage, and in order to complete the input path the two input reference pins must be decoupled to the earth plane with minimum of series inductance. Alternative connections which allow the use of complementary drive or DC coupling for added sensitivity are also shown in Fig. 3.

In the absence of an input signal, circuit will self oscillate with an output frequency of approximately 50MHz. This can be prevented by connecting a 10KΩ resistor between pin 11 and the negative rail. This offsets the input sensitivity by approximately 100mV.

The SP8785/6 will miscount with low frequency sinewave inputs or slow ramps. A slew of 200V/µs or greater is necessary for safe operation at low frequencies.

The input impedance of the SP8785/6 is a function of frequency and minimises at about the same frequency as the maximum input sensivity, so although it can load the signal source significantly there is generally enough signal to operate the device satisfactorily when the input impedance is at a minimum. The worst case occurs at the maximum frequency because this is where the input sensitivity is worst.

The modulus control inputs have been designed to interface directly to ECL III/ECL10k since on ECL counter such as the 10136 is required to directly control the device at the maximum input clock frequency. If the input frequency is reduced or the modulus extended as shown in the application notes, the device may be controlled by a TTL. or CMOS. counter provided the loop delay requirements are met and suitable interfacing is applied. Unused PE inputs should be left open circuit.

The SP8785/6 have outputs which are compatable with the ECL 10k logic family. The device will drive 100Ω lines and can be used with line impedances down to 50Ω with a small loss in noise immunity.

An equal load on the unused output will reduce waveform distortion.

APPLICATION NOTES

The SP8785/6 when used in a system operating at 1.3GHz may be controlled by a variable divider to give effective variable division at half the input frequency. The variable divider must produce a control signal within the period of the output of the SP8785/6 minus the delays within this device. The control loop delay time is typically 12 nsec.

Two methods may be used to achieve a satisfactory delay time within the control divider—

1. An extra divider may be inserted to increase the division ratio of the two modulus from 20/22 to 40/42, 80/82 or 100/102, hence reducing the control divider frequency and increasing the control loop delay time.
2. An ECL variable counter may be used to produce the control command. A device which is suitable is the 10136, in the ECL10k range.

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PLESSEY SEMICONDUCTORS

SP8000 SERIES HIGH SPEED DIVIDERS

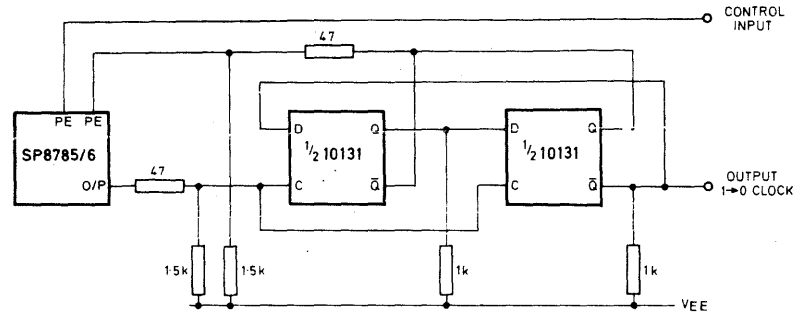


Fig. 6 ÷ 80/81 control loop delay time 55ns typ.

ABSOLUTE MAXIMUM RATINGS

Power supply voltage $V_{CC}-V_{EE}$	0V to +8V
Input voltage, PE inputs	V_{EE} to V_{CC}
Input voltage	2V peak to peak
Output current	40mA
Operating function temperature	+150°C
Storage temperature	−55°C to +150°C

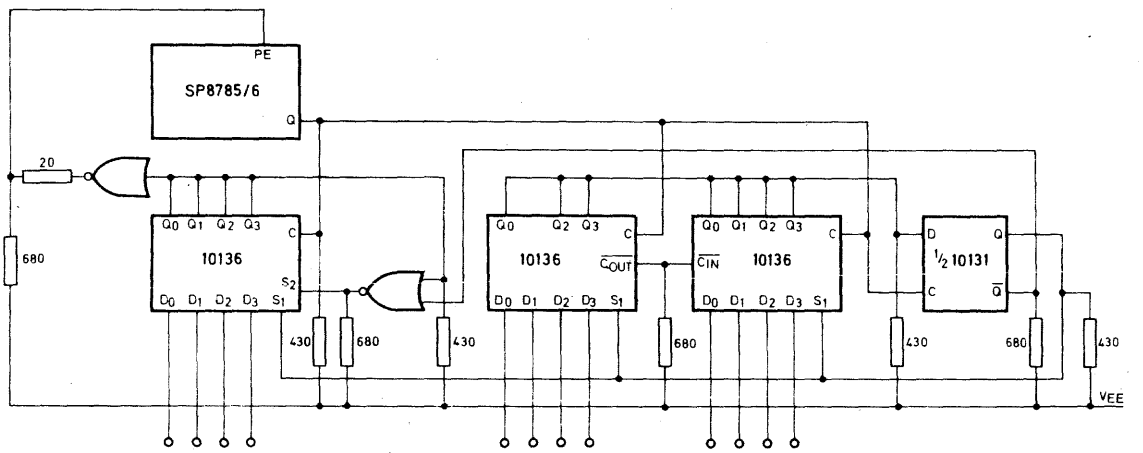
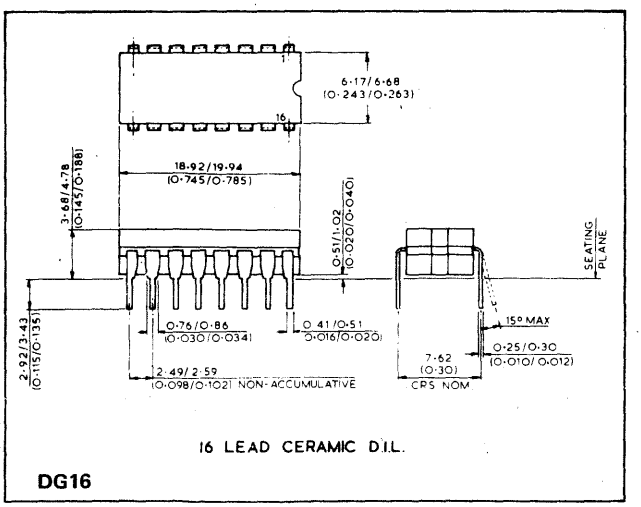


Fig. 7 1.3 GHz variable divider (200—2000 in steps of 2)

PACKAGE DETAILS

Dimensions are shown thus: mm (in)



16 LEAD CERAMIC D.I.L.

DG16

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SP8680A&B
HIGH SPEED DIVIDERS

SP8680 A & B
600 MHz–10/11
U.H.F. PROGRAMMABLE DIVIDERS

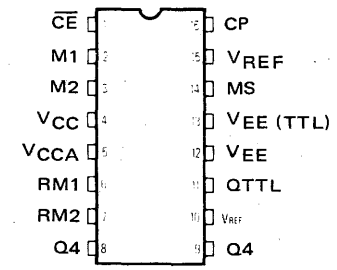
FEATURES

- D.C. to 600 MHz operation
- ECL and TTL compatible
- D.C. or A.C. clock input
- Clock enable
- Asynchronous master set

QUICK REFERENCE DATA

- Supply voltage ($V_{CC}-V_{EE}$) =5.0 V +0.5 V −0.25 V
- Power consumption 400 mW typ. (no load)
  T.T.L. output 20 mW typ.
- Maximum input frequency 600 MHz SP8680B
  550 MHz SP8680A
  Input amplitude (a.c. coupled)
  350 mV to 700 mV.

Fig. 1 Pin Connections (Top View)



The SP8680 A & B are high speed programmable–10/11 counters which operate at input frequencies up to 600 MHz over the temperature ranges −55°C to +125°C (A grade), −30°C to +70°C (B grade). The devices operate on a single +5 V or −5.2 V power supply and may be easily interfaced to E.C.L. or T.T.L. logic. The clock input may be directly coupled to E.C.L., or (by connecting the internal V_{REF}) capacitively coupled to the signal source. A clock enable, which is E.C.L. compatible, is provided.

The division ratio is controlled by two mode inputs which are also ECL compatible. The counter will divide by 10 when either input is in the high state and by 11 when both inputs are low. The counter may be set to the eleventh state by applying a high level to the M5 input. The set command is asynchronous and overrides the clock input. All inputs have internal 50 k Ω pull down resistors, so that unused inputs may be left open circuit.

Two complementary ECL outputs are provided. They are both capable of driving 50 Ω lines. A T.T.L. push pull output is also provided which may be powered up separately from the counter using the V_{EE} on pin 13.

Q1	Q2	Q3	Q4 (QTR)	
H	H	H	H	
L	H	H	H	
L	L	H	H	
L	L	L	H	
H	L	L	H	
H	H	L	H	
L	H	H	L	
L	L	H	L	
L	L	L	L	
H	L	L	L	
H	H	L	L	

÷10 ÷11

MS	CE	M1	M2	Response
H	X	X	X	Set
L	H	X	X	Hold
L	L	L	L	÷11
L	L	H	X	÷10
L	L	X	H	÷10

X = DON'T CARE

FOR USE AS ÷10 PRESCALER CONNECT M1 OR M2 to Q4

Fig. 3 Count Sequence & Control Input Truth Table

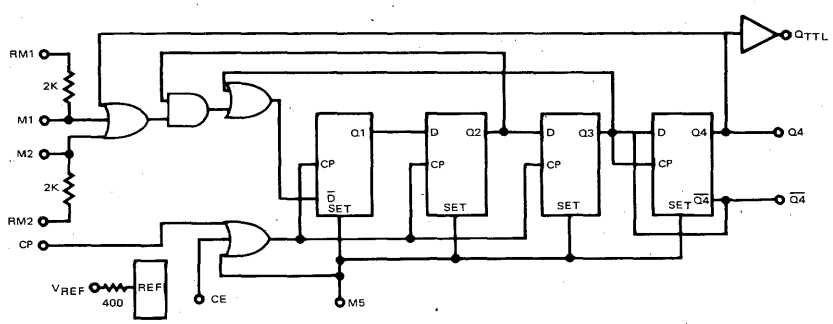


Fig. 2 Logic diagram

Absolute Maximum Ratings

Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The table of Electrical Characteristics provides conditions for actual device operation.

Power Supply Voltage	$[V_{CC}(V_{CCA})-V_{EE}]$ −0.5 to +7V
Input Voltage	V_{EE} to V_{CC}
ECL Output Source Current	−50 mA
TTL Output Sink Current	30 mA
Voltage applied to TTL Ouput High	V_{EE} to V_{CC}
Operating Ambient Temperature	−55°C to +125°C
Storage Temperature	−55°C to +150°C

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PLESSEY
SEMICONDUCTORS

SP8680A & B
HIGH SPEED DIVIDERS

Static Characteristics

Characteristics	Value Min.	Value Type	Value Max.	Units	Conditions
Guaranteed Input High Voltage V_{INH}	4.1		4.4	V	V_{CC} = +5.2V Tamb = 25°C
Guaranteed Input Low Voltage V_{INL}	3.35		3.7	V	(See Note 2)
Input High Current I_{INH}					V_{CC} = +5.2V
CP and MS inputs			400	μA	Tamb = 25°C
M1 and M2 inputs			250	μA	V_{INH} = 4.4V
Input Low Current I_{INL}	0.5			μA	V_{INL} = 3.35V
E.C.L. Output Low Voltage V_{OL}	3.38	3.49	3.58	V	V_{CC} = +5.2V Tamb = 25°C
E.C.L. Output High Voltage V_{OH}	4.22	4.30	4.38	V	load 100 Ω to +3.2V
T.T.L. Output High Voltage V_{OH}	2.7	3.3		V	V_{CC} = V_{CCA} = 4.75V I_{OH} = −1 mA Tamb = 25°C
T.T.L. Output Low Voltage V_{OL}		0.3	0.5	V	V_{CC} = V_{CCA} = 4.75V I_{OL} = 20 mA Tamb = 25°C
T.T.L. Output Short Circuit Current	−80	−40	−20	mA	V_{CC} = V_{CCA} = 5.5V V_{OUT} = 0V Pin 14 = V_{INH}
M1, M2 Input Low Current (using int. 2K Ω pull up)	−4.0	−2.5		V	V_{CC} = V_{CCA} = 5.5V V_{IN} = 0.4V Pins 6,7 = V_{CC}
Power Supply Current		75	105	mA	No load Pins 6,7,13 open circuit
T.T.L. Output Stage Supply Current		4		mA	Mean, Output High and Low

Dynamic Characteristics

Characteristics	Value Min.	Value Typ.	Value Max.	Units	Conditions
Max. Count Frequency					V_{CC} = +5.2v a.c. coupled input 350mV peak to peak
SP8680B	600			MHz	−30°C to +70°C
SP8680A	550			MHz	−55°C to +125°C
Min. Frequency with sinewave clock input			10	MHz	V_{CC} = +5.2V a.c. coupled input 600mV peak to peak Tamb = 25°C
Min. slew rate of square wave clock input			20	V/μsec	V_{CC} = +5.2v
Propagation Delay CP to Q4		2.2	3.0	nsec	Tamb = 25°C
Propagation Delay MS to Q4		4.5	6.0	nsec	Output Load
Min Set Up Time M to CP		2.0	4.0	nsec	100Ω to +3.2v
ECL Output Rise & Fall Times		1.3		nsec	
Propagation Delay CP to QTTL		8	14	nsec	V_{CC} = +5.0v Tamb = 25°C
TTL Ouput Rise Time		3		nsec	
TTL Output Fall Time		3		nsec	

NOTES:
1. The SP8680 may be used in a positive earth system with V_{CC} = 0V and V_{EE} = −4.75V to −5.5V
2. The input threshold has a temperature coefficient of 0.8mV/°C. This may be used to calculate V_{INH} and V_{INL} values at the temperature extremes.
3. The E.C.L. outputs are capable of driving a 50Ω load to +3.2V over a limited temperature range of 0°C to 70°C. The output high level will be reduced by typically 50mv.

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The output high level has a temperature coefficient of 1.2 mV/°C, whilst the output iow level has a coefficient of 0.2 mV/°C.

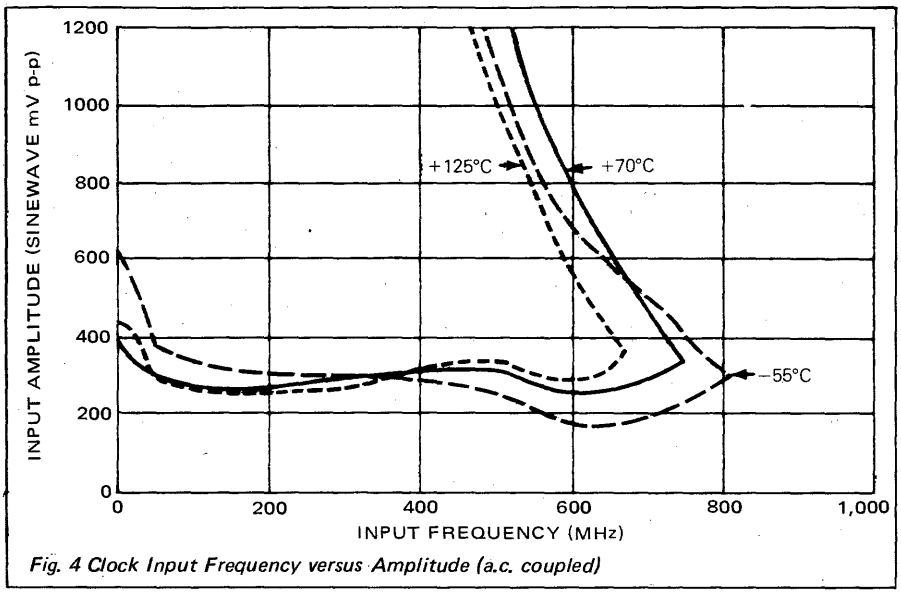


Fig. 4 Clock Input Frequency versus Amplitude (a.c. coupled)

N.B.
The graphs on the left are with the TTL output connected. Sensitivity in the 300 to 500MHz frequency range is improved by of the order of 100mV p-p when pin 13 is disconnected.

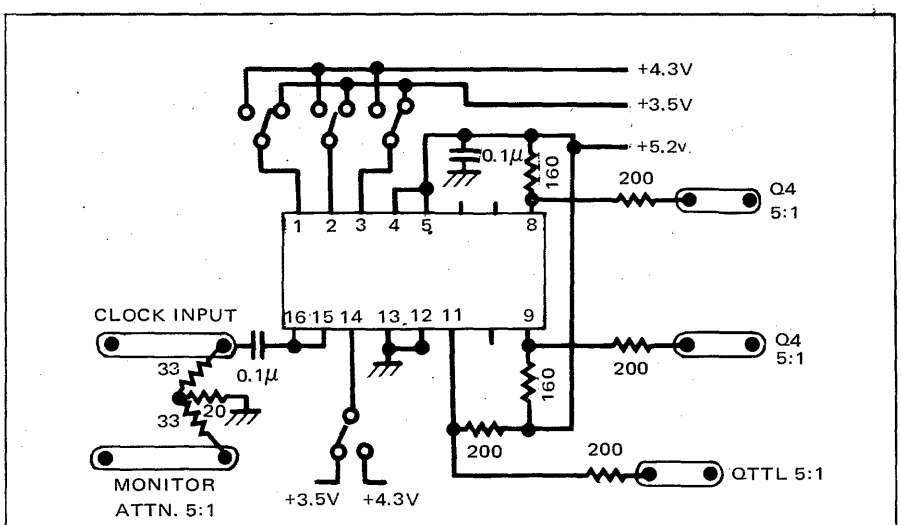


Fig. 5 Dynamic test circuit

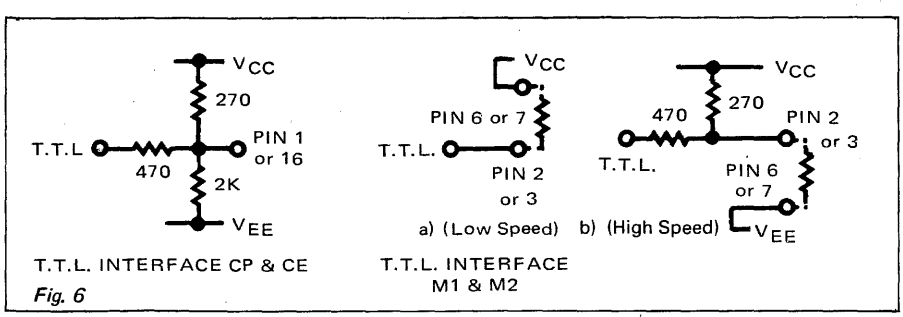


Fig. 6

OPERATING NOTES

The SP8680 is designed to operate in the UHF band and therefore PCB layouts should comply with norman UHF rules, e.g. short tracks, low inductance capacitors etc.

All clock and control inputs are compatible with ECL 10K throughout the temperature range. The clock input may be capacitively coupled by connecting pin 16 to pin 15. All inputs may be interfaced with T.T.L. logic as shown in Fig. 6.

PLESSEY
SEMICONDUCTORS

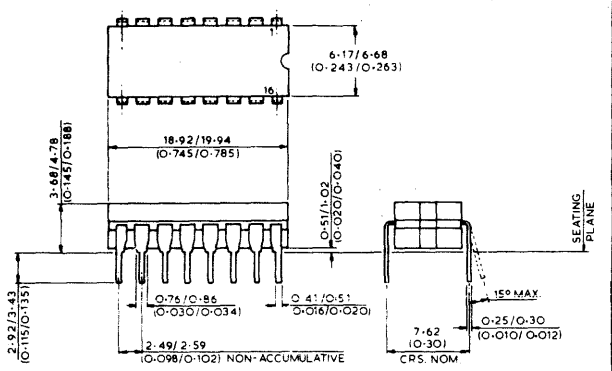
SP8680A&B
HIGH SPEED DIVIDERS

Two E.C.L. compatible outputs are available (true and inverse) both capable of driving a 100 Ω load (to +3.2V) over the full temperature range. These outputs have no internal pull down so an external resistor to V_{EE} is required when interfacing to other E.C.L. logic. A T.T.L. output is also provided which is powered up by connecting pin 13 to V_{EE}.

The SP8680 may be controlled by a following variable divider to produce effective variable division at up to 600 MHz. Some points to be noted when this technique is employed are as follows:—

1) The 0—1 edge of the Q4 or TTL outputs must be used to clock the following divider. This gives a maximum control loop delay time (equal to ten clock periods minus internal delays).
2) At 600 MHz the required control loop delay time is only 13 nsec (using ECL outputs) and hence only an E.C.L. variable divider can be used in the control loop. A suitable device is the 10136.
3) To overcome the above problem the modulus may be be extended from 10/11 to 20/21, 40/41, or 100/101. This will considerably increase the control loop delay time, so that a TTL variable divider may be used in the control loop.
4) The minimum division number of a 'two modulus' n/n + 1 when employed as a fully variable divider is n(n—1). Therefore for a 10/11 this will give 90. If the modulus has been extended to 100/101 the minimum divide will be 9,900 which may well be too large.
5) If the above two modulus approach does not give a satisfactory systems solution then a four modulus system may be required. An example of this would be a 100/101/110/111 followed by two control dividers. The two control dividers decide on the number of +1 and +10 counts required. The minimum division number of such a system is 900.

PACKAGE DETAILS



16 LEAD CERAMIC D.I.L.

DG16

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Raytheon . . .

The source for low power Schottky

Basic Type	Description	9LS	25LS	54LS	74LS
LS00	Quad 2-input NAND gate	X		X	X
LS01	Quad 2-input NAND gate. open collectors	X		X	X
LS02	Quad 2-input NOR gate. open collectors	X		X	X
LS03	Quad 2-input NAND gate. open collectors	X		X	X
LS04	Hex inverter	X		X	X
LS05	Hex inverter. open collectors	X		X	X
LS08	Quad 2-input AND gate	X		X	X
LS09	Quad 2-input AND gate. open collectors	X		X	X
LS10	Triple 3-input NAND gate	X		X	X
LS11	Triple 3-input AND gate	X		X	X
LS12	Triple 3-input NAND gate. open collectors	X		X	X
LS13	Dual 4-input Schmitt trigger	X		X	X
LS14	Hex Schmitt trigger	X	(1)	X	X
LS15	Triple 3-input AND gate. open collectors	X	(2)	X	X
LS20	Dual 4-input NAND gate	X		X	X
LS21	Dual 4-input AND gate	X		X	X
LS22	Dual 4-input NAND gate. open collectors	X	(3)	X	X
LS26	Quad 2-input NAND. open collectors 15V	X	(4)	X	X
LS27	Triple 3-input NOR gate	X		X	X
LS28	Quad 2-input NOR buffer	X		X	X
LS30	8-input NAND gate	X		X	X
LS32	Quad 2-input OR gate	X		X	X
LS33	Quad 2-input NOR buffer. open collectors	X		X	X
LS37	Quad 2-input NAND buffer	X		X	X
LS38	Quad 2-input NAND buffer. open collectors	X		X	X
LS40	Dual 4-input NAND buffer	X		X	X
LS42	1-of-10 decoder	X		X	X
LS43	Excess 3 to decimal decoder	X		X	X
LS44	Excess gray to decimal decoder	X		X	X
LS51	Dual AOI gate	X		X	X
LS54	2-3-3-2-input AOI gate	X		X	X
LS55	2-wide. 4-input AOI gate	X		X	X
LS73	Dual J-K flip-flop	X		X	X
LS74	Dual D flip-flop	X		X	X
LS75	Quad transparent latch	X		X	X
LS76	Dual J-K flip-flop	X		X	X
LS77	Quad transparent latch	X		X	X
LS78	Dual J-K flip-flop	X		X	X
LS83A	4-bit full adder	X		X	X
LS85	4-bit magnitude comparator	X		X	X
LS86	Quad exclusive OR gate	X		X	X
LS90	Decade counter	X		X	X
LS91	8-bit shift register	X		X	X
LS92	Divide by 12 counter	X		X	X
LS93	4-bit binary counter	X		X	X
LS95B	4-bit shift register	X		X	X
LS107	Dual J-K flip-flop	X		X	X
LS109	Dual J-K flip-flop	X		X	X
LS112	Dual J-K edge-triggered flip-flop	X		X	X
LS113	Dual J-K edge-triggered flip-flop	X		X	X
LS114	Dual J-K edge-triggered flip-flop	X		X	X
LS122	Retriggerable one-shot	X	X	X	X
LS123	Dual one-shot	X	X	X	X
LS132	Quad 2-input Schmitt trigger	X		X	X
LS136	Quad exclusive OR gate. open collectors	X		X	X
LS137	Decoder/demultiplexer				
LS138	3-to-8 decoder/demultiplexer	X	X	X	X
LS139	Dual 2-to-4 decoder/demultiplexer	X	X	X	X
LS151	8-to-1 line multiplexer	X	X	X	X

Basic Type	Description	9LS	25LS	54LS	74LS
LS152	8-to-1 line multiplexer	X		X	X
LS153	Dual 4-to-1 multiplexer	X	X	X	X
LS155	Dual 2-to-4 decoder/demultiplexer	X		X	X
LS156	LS155. open collectors	X		X	X
LS157	Quad 2-to-1 line multiplexer	X	X	X	X
LS158	LS157. inverting	X	X	X	X
LS160	Decoder counter. asynchronous clear	X	X	X	X
LS161	Binary counter. asynchronous clear	X	X	X	X
LS162	Decade counter. synchronous clear	X	X	X	X
LS163	Binary counter. synchronous clear	X	X	X	X
LS164	8-bit shift register (SIPO)	X	X	X	X
LS170	4 x 4 register file. open collectors	X	X	X	X
LS173	Quad bus buffer register				
LS174	Hex D-type flip-flop	X	X	X	X
LS175	Quad D-type flip-flop	X	X	X	X
LS181	4-bit arithmetic logic unit	X	X	X	X
LS190	BCD decade counter. mode control	X	X	X	X
LS191	4-bit binary counter. mode control	X	X	X	X
LS192	BCD decade counter. up/down	X	X	X	X
LS193	4-bit binary counter. up/down	X	X	X	X
LS194A	4-bit R shift register	X	X	X	X
LS195A	4-bit parallel shift register	X	X	X	X
LS196	4-bit presettable decade counter	X	X	X	X
LS197	4-bit presettble binary counter	X	X	X	X
LS221	Dual one-shot (very stable)	X		X	X
LS240	Octal inverting bus driver (20-pin)	X	X	X	X
LS241	Octal non-inverting bus driver (20-pin)	X	X	X	X
LS242	Quad transceiver	X	X	X	X
LS243	Quad transceiver	X	X	X	X
LS244	Octal 3-state driver	X	X	X	X
LS251	LS151 with tri-state outputs	X	X	X	X
LS253	LS153 with tri-state outputs	X	X	X	X
LS255	LS155 with tri-state outputs	X		X	X
LS257	LS157 with tri-state outputs	X	X	X	X
LS258	LS158 with tri-state outputs	X	X	X	X
LS261	2 x 4 binary multiplier	X		X	X
LS266	Quad exclusive NOR gate. open collectors	X		X	X
LS273	Octal D flip-flop with master reset (20-pin)	X	X	X	X
LS279	Quad set/reset latch	X		X	X
LS283	4-bit full adder. fast carry (rotated LS83)	X		X	X
LS295A	LS95B with tri-state outputs	X		X	X
LS298	Quad 2-multiplexer with output register	X		X	X
LS299	8-bit universal shift register (20-pin)	X	X	X	X
LS322	8-bit serial/parallel register	X		X	X
LS323	8-bit shift/storage register	X		X	X
LS365	Hex buffer. tri-state. common enable	X		X	X
LS366	Hex inverter. tri-state. common enable	X		X	X
LS367	Hex buffer. tri-state. 4-bit and 2-bit	X		X	X
LS368	Hex inverter. tri-state. 4-bit and 2-bit	X		X	X
LS373	Octal transparent latch (20-pin)	X	X	X	X
LS374	Octal D flip-flop (20-pin)	X	X	X	X
LS377	Octal D flip-flop with enable (20-pin)	X	X	X	X
LS384	8-bit serial/parallel multiplier	X		X	X
LS385	4-bit serial/parallel adder/subtractor	X		X	X
LS386	Quad exclusive OR gate	X		X	X
LS395	4-bit shift register. tri-state	X		X	X
LS670	4 x 4 register file. tri-state	X	X	X	X

25LS Descriptions

1. 8-bit serial/parallel two's complement multiplier
2. Quad serial adder/subtractor
3. 8-bit serial/parallel register with sign extender
4. 8-bit shift/storage register with synchronous clear

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LS240 Octal Three-State Inverting Drivers

Features

- Three-state outputs drive bus lines directly
- Hysteresis at inputs improve noise margin
- PNP inputs reduce D.C. loading on bus lines
- Data-to-output propagation delay times—18ns Max.
- Enable-to-output—30ns Max.
- 20 pin hermetic and molded DIP packages

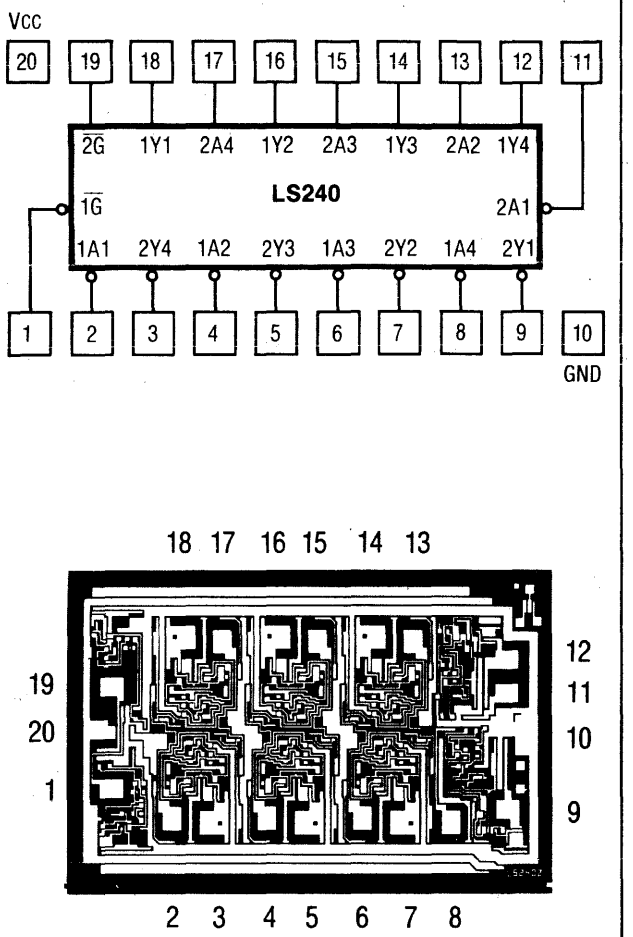
Description

The LS240 is an octal inverting line driver fabricated using advanced low-power Schottky technology.

Three-state outputs are provided to drive bus lines directly with an output sink current guaranteed at 12mA over the military range and 24mA over the commercial range. Four buffers are enabled from one common line and the other four from a second enable line.

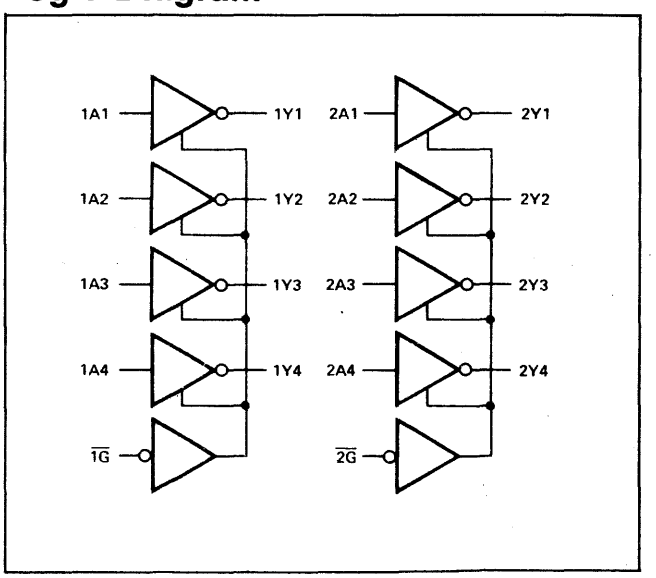
Improved noise rejection and high fan-out are provided by input hysteresis and low current PNP inputs.

Pinout Diagram



Die Size .102 x .067

Logic Diagram



Function Table

Inputs		Output
$\overline{G}$	A	Y
H	X	Z
L	H	L
L	L	H

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Electrical Characteristics

The following conditions apply unless otherwise specified:

Com'l $T_A = 0°C$ to $+70°C$ $V_{CC} = 5.0V \pm 5\%$ (Min. = 4.75V Max. = 5.25V)
Mil. $T_A = -55°C$ to $+125°C$ $V_{CC} = 5.0V \pm 10\%$ (Min. = 4.50V Max. = 5.50V)

Electrical Characteristics

Parameters	Test Conditions[1]		9LS/54LS Min.	9LS/54LS Typ.[2]	9LS/54LS Max.	9LS/74LS Min.	9LS/74LS Typ.[2]	9LS/74LS Max.	Units
V_{OH}	V_{CC} = Min., V_{IH} = 2.0V I_{OH} = -3.0mA, V_{IL} = V_{IL}Max.		2.4	3.4		2.4	3.4		Volts
	V_{CC} = Min., V_{IL} = 0.5V	I_{OH} = -12mA	2.0						
		I_{OH} = -15mA				2.0			
V_{OL}	V_{CC} = Min.	I_{OL} = 12mA		0.25	0.4		0.25	0.4	Volts
		I_{OL} = 24mA					0.35	0.5	
V_{IH}	Guaranteed input logical HIGH voltage for all inputs		2.0			2.0			Volts
V_{IL}					0.7			0.8	Volts
V_{IK}	V_{CC} = Min., I_I = -18mA				-1.5			-1.5	Volts
	V_{CC} = Min.		0.2	0.4		0.2	0.4		Volts
I_{OZH}	V_{CC} = Max. V_{IH} = 2.0V	V_O = 2.7V			20			20	uA
I_{OZL}	V_{IL} = V_{IL}Max.	V_O = 0.4V			-20			-20	
I_I	V_{CC} = Max., V_I = 7.0V				0.1			0.1	mA
I_{IH}	V_{CC} = Max., V_{IH} = 2.7V				20			20	uA
I_{IL}	V_{CC} = Max., V_{IL} = 0.4V				-200			-200	uA
I_{SC}[3]	V_{CC} = Max.		-50		-225	-50		-225	mA
I_{CC}	V_{CC} = Max. Outputs open	All Outputs HIGH		13	23		13	23	mA
		All Outputs LOW		26	44		26	44	
		Outputs at Hi-Z		29	50		29	50	

Notes: 1. For conditions shown as Min. or Max., use the appropriate value specified under recommended operating conditions.
2. All typical values are V_{CC} = 5.0V, T_A = 25°C.
3. Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

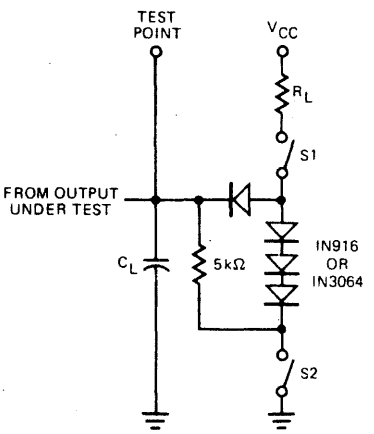
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Switching Characteristics (V_{CC} = 5.0V)

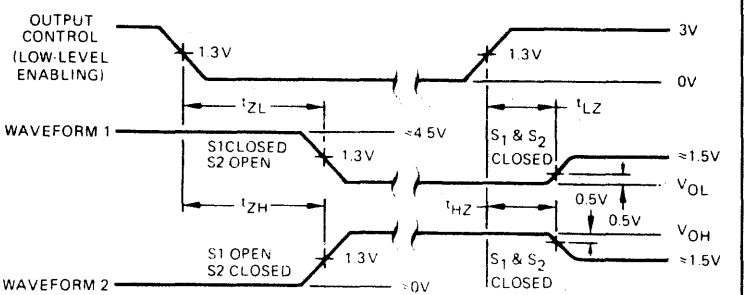
Parameters	-55° C			+25° C			+125° C			Units
	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Test Conditions: C_L = 45pF, R_L = 667 Ohms										
t_{PLH}					9.0	14				ns
t_{PHL}					12	18				ns
t_{PZL}					20	30				ns
t_{PZH}					15	23				ns
Test Conditions: C_L = 5.0pF, R_L = 667 Ohms										
t_{PLZ}					15	25				ns
t_{PHZ}					10	18				ns

Notes: 1. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
2. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
3. In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily. PRR ≤ 1.0MHz, $Z_{OUT} \approx 50\Omega$ and $t_r \leq 2.5$ns, $t_f \leq 2.5$ns.

LOAD CIRCUIT FOR THREE-STATE OUTPUTS



VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES, THREE-STATE OUTPUTS



Notes: 1. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
2. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
3. In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily. PRR ≤ 1.0MHz, $Z_{OUT} \approx 50\Omega$ and $t_r \leq 2.5$ns, $t_f \leq 2.5$ns.

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Octal Three-State Buffers

LS241 LS244

Features

- Three-state outputs drive bus lines directly
- Hysteresis at inputs improve noise margin
- PNP inputs reduce D.C. loading on bus lines
- Data-to-output propagation delay times—18ns Max.
- Enable-to-output—30ns Max.
- 20 pin hermetic and molded DIP packages

Description

The LS241 and LS244 are octal buffers fabricated using advanced low-power Schottky technology.

Three-state outputs are provided to drive bus lines directly with an output sink current guaranteed at 12mA over the military range and 24mA over the commercial range. Four buffers are enabled from one common line and the other four from a second enable line.

The LS241 has enable inputs of opposite polarity to allow use as a transceiver without overlap. The LS244 enables are of similar polarity for use as a unidirectional buffer in which both halves are enabled simultaneously.

Improved noise rejection and high fan-out are provided by input hysteresis and low current PNP inputs.

Function Tables

LS241

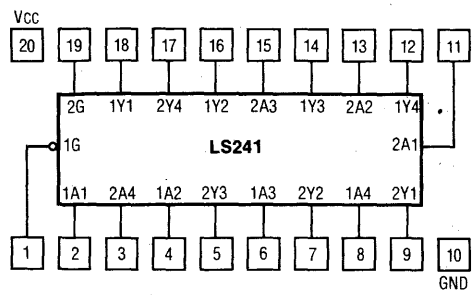
Inputs			Outputs
$\overline{1G}$	2G	A	Y
H	L	X	Z
L	H	H	H
L	H	L	L

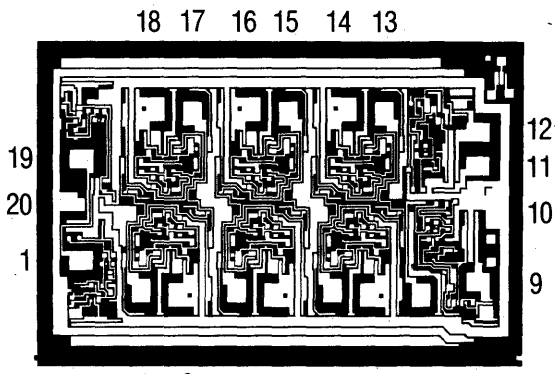
LS244

Inputs		Output
$\overline{G}$	A	Y
H	X	Z
L	H	H
L	L	L

Pinout Diagrams

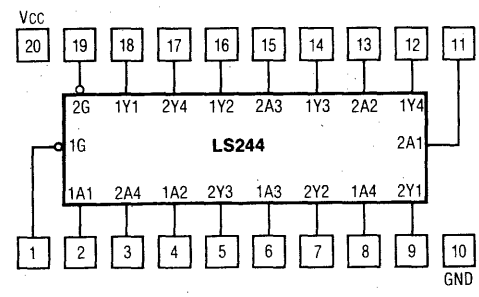
LS241

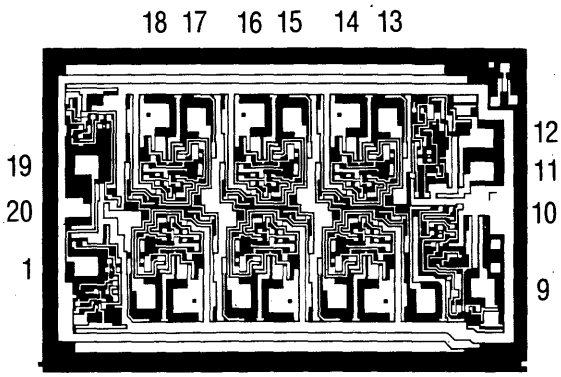




Die Size .102 x .067

LS244





Die Size .102 x .067

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Electrical Characteristics

The following conditions apply unless otherwise specified:

Com'l $T_A = 0°C$ to $+70°C$ $V_{CC} = 5.0V + 5\%$ (Min. = 4.75V Max. = 5.25V)
Mil. $T_A = -55°C$ to $+125°C$ $V_{CC} = 5.0V + 10\%$ (Min. = 4.50V Max. = 5.50V)

Electrical Characteristics

Parameters	Test Conditions[1]		9LS/54LS Min.	9LS/54LS Typ.[2]	9LS/54LS Max.	9LS/74LS Min.	9LS/74LS Typ.[2]	9LS/74LS Max.	Units
V_{OH}	V_{CC} = Min., V_{IH} = 2.0V I_{OH} = -3.0mA, V_{IL} = V_{IL}Max.		2.4	3.4		2.4	3.4		Volts
	V_{CC} = Min., V_{IL} = 0.5V	I_{OH} = -12mA	2.0						
		I_{OH} = -15mA				2.0			
V_{OL}	V_{CC} = Min.	I_{OL} = 12mA		0.25	0.4		0.25	0.4	Volts
		I_{OL} = 24mA					0.35	0.5	
V_{IH}	Guaranteed input logical HIGH voltage for all inputs		2.0			2.0			Volts
V_{IL}					0.7			0.8	Volts
V_{IK}	V_{CC} = Min., I_I = -18mA				-1.5			-1.5	Volts
	V_{CC} = Min.		0.2	0.4		0.2	0.4		Volts
I_{OZH}	V_{CC} = Max. V_{IH} = 2.0V	V_O = 2.7V			20			20	uA
I_{OZL}	V_{IL} = V_{IL}Max.	V_O = 0.4V			-20			-20	
I_I	V_{CC} = Max., V_I = 7.0V				0.1			0.1	mA
I_{IH}	V_{CC} = Max., V_{IH} = 2.7V				20			20	uA
I_{IL}	V_{CC} = Max., V_{IL} = 0.4V				-200			-200	uA
I_{SC}[3]	V_{CC} = Max.		-50		-225	-50		-225	mA
I_{CC}	V_{CC} = Max. Outputs open	All Outputs HIGH		13	23		13	23	mA
		All Outputs LOW		27	46		27	46	
		Outputs at Hi-Z		32	54		32	54	

Notes: 1. For conditions shown as Min. or Max., use the appropriate value specified under recommended operating conditions.
2. All typical values are V_{CC} = 5.0V, T_A = 25°C.
3. Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

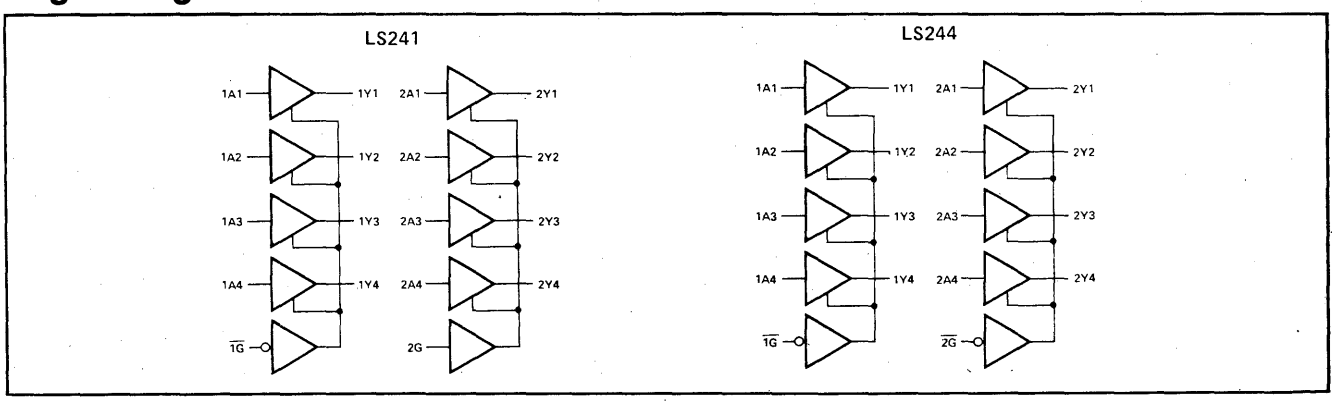
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Switching Characteristics (V_{CC} = 5.0V)

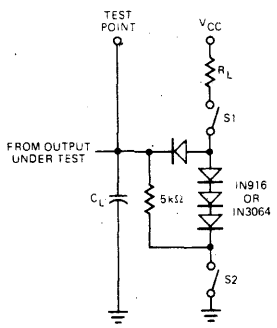
Parameters	-55° C			+25° C			+125° C			Units
	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Test Conditions: C_L = 45pF, R_L = 667 Ohms.										
t_{PLH}					12	18				ns
t_{PHL}					12	18				ns
t_{PZL}					20	30				ns
t_{PZH}					15	23				ns
Test Conditions: C_L = 5.0pF, R_L = 667 Ohms										
t_{PLZ}					15	25				ns
t_{PHZ}					10	18				ns

Notes: 1. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
2. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
3. In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily.
4. Pulse generator characteristics: PRR ≤ 1.0MHz, Z_{OUT} ≈ 50 Ohms, t_r ≤ 15ns, t_f ≤ 6ns.
5. When measuring t_{PLH}, switches S_1 and S_2 are closed.

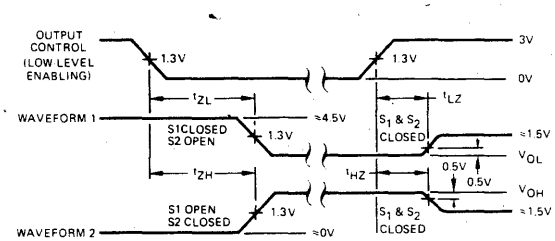
Logic Diagram



LOAD CIRCUIT FOR THREE-STATE OUTPUTS



VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES, THREE-STATE OUTPUTS



Notes: 1. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control.
2. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
3. In the examples above, the phase relationships between inputs and outputs have been chosen arbitrarily.
4. Pulse generator characteristics: PRR ≤ 1.0MHz, Z_{OUT} ≈ 50Ω, t_r ≤ 15ns, t_f ≤ 6ns.
5. When measuring t_{PLH} and t_{PHL}, switches S_1 and S_2 are closed.

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LS242 LS243

Quad Bus Transceivers with Three-State Outputs

Features

- Three-state outputs drive bus lines directly
- Hysteresis at inputs improve noise margin
- PNP inputs reduce D.C. loading on bus lines
- Data-to-output propagation delay times—18ns Max.
- Enable-to-output—30ns Max.
- LS242 and LS243 are specified at 48mA output current

Description

The LS242 and LS243 are quad bus transceivers designed for asynchronous two-way communications between data buses.

The LS242 and LS243 have the two 4-line data paths connected input-to-output on both sides to form an asynchronous transceiver/buffer with complementing enable inputs. The LS242 is inverting, while the LS243 presents non-inverting data at the outputs.

Three-state outputs are provided to drive bus lines directly with an output sink current guaranteed at 12mA over the military range and 24mA over the commercial range.

Improved noise rejection and high fan-out are provided by input hysteresis and low current PNP inputs.

Function Tables

LS242

CONTROL INPUTS		DATA OUTPUTS	
$\overline{G}AB$	GBA	A	B
H	H	$\overline{O}$	I
L	H	*	*
H	L	ISOLATED	
L	L	I	$\overline{O}$

I = Input
O = Output
$\overline{O}$ = Inverting Output

H = HIGH
L = LOW

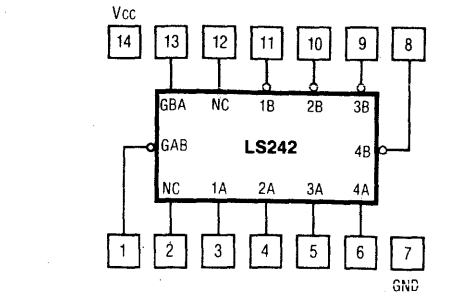
LS243

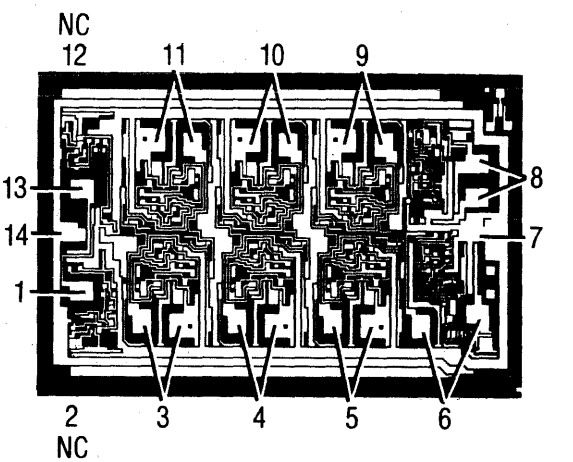
CONTROL INPUTS		DATA OUTPUTS	
$\overline{G}AB$	GBA	A	B
H	H	O	I
L	H	*	*
H	L	ISOLATED	
L	L	I	O

*Possible destructive oscillation may occur if the transceivers are enable in both directions at once

Pinout Diagram

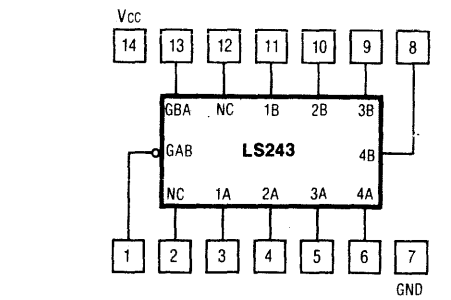
LS242

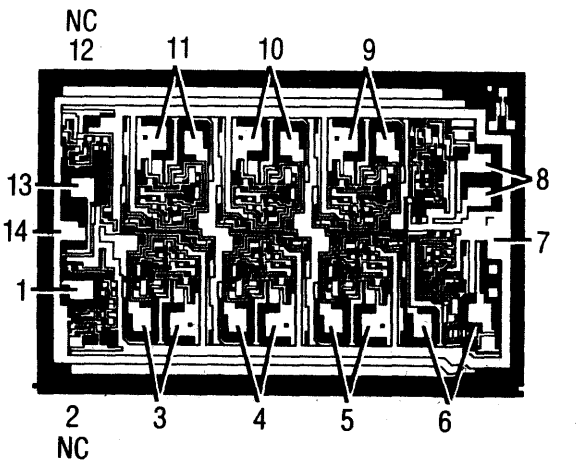




Die Size .102 x .067

LS243





Die Size .102 x .067

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Quad Bus Transceivers with Three-State Outputs

LS242 LS243

Electrical Characteristics

The following conditions apply unless otherwise specified:

Com'l $T_A = 0°C$ to $+70°C$ $V_{CC} = 5.0V + 5\%$ (Min. = 4.75V Max. = 5.25V)
Mil. $T_A = -55°C$ to $+125°C$ $V_{CC} = 5.0V + 10\%$ (Min. = 4.50V Max. = 5.50V)

Electrical Characteristics

Parameters	Test Conditions[1]		9LS/54LS Min.	9LS/54LS Typ.[2]	9LS/54LS Max.	9LS/74LS Min.	9LS/74LS Typ.[2]	9LS/74LS Max.	Units
V_{OH}	V_{CC} = Min., V_{IH} = 2.0V I_{OH} = -3.0mA, V_{IL} = V_{IL}Max.		2.4	3.4		2.4	3.4		Volts
	V_{CC} = Min., V_{IL} = 0.5V	I_{OH} = -12mA	2.0						
		I_{OH} = -15mA				2.0			
V_{OL}	V_{CC} = Min.	I_{OL} = 12mA		0.25	0.4		0.25	0.4	Volts
		I_{OL} = 24mA					0.35	0.5	
V_{IH}	Guaranteed input logical HIGH voltage for all inputs		2.0			2.0			Volts
V_{IL}					0.7			0.8	Volts
V_{IK}	V_{CC} = Min., I_I = -18mA				-1.5			-1.5	Volts
	V_{CC} = Min.		0.2	0.4		0.2	0.4		Volts
I_{OZH}	V_{CC} = Max. V_{IH} = 2.0V	V_O = 2.7V			20			20	uA
I_{OZL}	V_{IL} = V_{IL}Max.	V_O = 0.4V			-20			-20	
I_I	V_{CC} = Max., V_I = 7.0V				0.1			0.1	mA
I_{IH}	V_{CC} = Max., V_{IH} = 2.7V				20			20	uA
I_{IL}	V_{CC} = Max., V_{IL} = 0.4V				-200			-200	uA
I_{SC}[3]	V_{CC} = Max.		-50		-225	-50		-225	mA
I_{CC}[4]	All Outputs HIGH			22	38		22	38	mA
	All Outputs LOW			29	50		29	50	
	Outputs at Hi-Z (LS242)			29	50		29	50	
	Outputs at Hi-Z (LS243)			32	54		32	54	

Notes: 1. For conditions shown as Min. or Max., use the appropriate value specified under recommended operating conditions.
2. All typical values are V_{CC} = 5.0V, T_A = 25°C.
3. Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.
4. For LS242 and LS243 I_{CC} is measured with transceivers enabled in one direction only, or with all transceivers disabled.

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LS242 LS243 Quad Bus Transceivers with Three-State Outputs

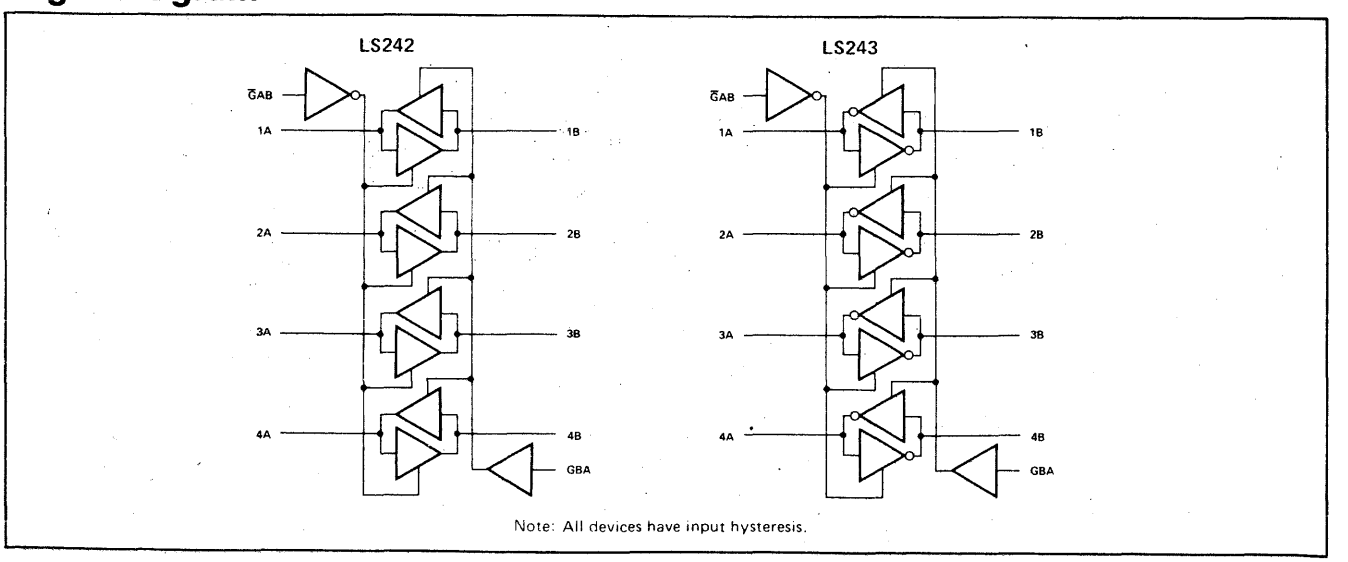
LS242 Switching Characteristics (Vcc = 5.0V)

Parameters	-55° C			+25° C			+125°			Units
	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Test Conditions: C_L = 45pF, R_L = 667 Ohms										
t_{PLH}					9.0	14				ns
t_{PHL}					12	18				ns
t_{PZL}					20	30				ns
t_{PZH}					15	23				ns
Test Conditions: C_L = 5.0pF, R_L = 667 Ohms										
t_{PLZ}					15	25				ns
t_{PHZ}					10	18				ns

LS243 Switching Characteristics (Vcc = 5.0V)

Parameters	-55° C			+25° C			+125° C			Units
	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Test Conditions C_L = 45pF, R_L = 667 Ohms										
t_{PLH}					12	18				ns
t_{PHL}					12	18				ns
t_{PZL}					20	30				ns
t_{PZH}					15	23				ns
Test Conditions: C_L =5.0pF, R_L = 667 Ohms										
t_{PLZ}					15	25				ns
t_{PHZ}					10	18				ns

Logic Diagram



Note: All devices have input hysteresis.

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Octal D-Type Flip-Flop with Clear LS273

Features

- Contains eight flip-flops with single-rail outputs
- Buffered clock and direct clear inputs
- Individual data input to each flip-flop

Description

These monolithic, positive-edge-triggered flip-flops utilize TTL circuitry to implement D-type flip-flop logic with a direct clear input.

Information at the D inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the high or low level, the D input signal has no effect at the output.

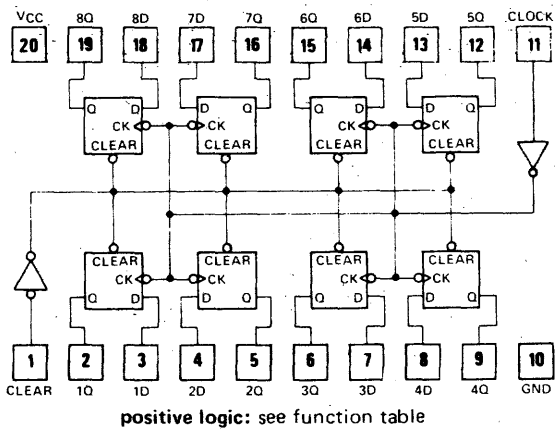
These flip-flops are guaranteed to respond to clock frequencies ranging from 0 to 30MHz while maximum clock frequency is typically 40MHz. Typical power dissipation is 10mW for the LS273.

Function Table

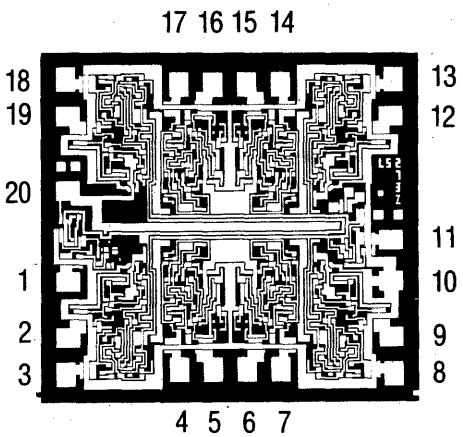
(Each Flip-Flop)

Inputs			Output
Clear	Clock	D	Q
L	X	X	L
H	↑	H	H
H	↑	L	L
H	L	X	Q_0

Pinout Diagram

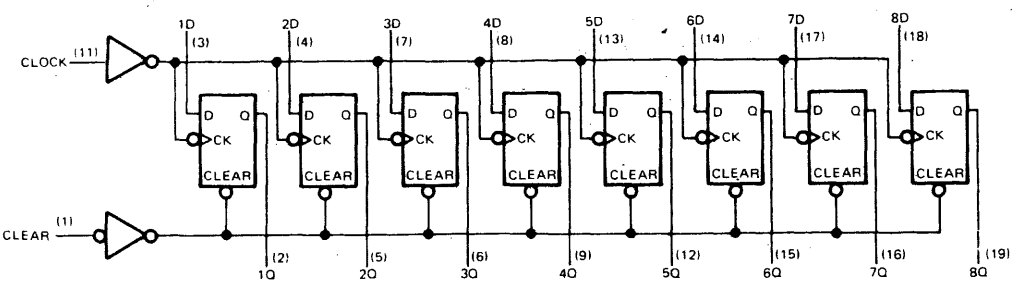


positive logic: see function table



Die Size .078 x .071

Logic Diagram



LS273 Octal D-Type Flip-Flop with Clear

Recommended Operating Conditions

		9LS/54LS273			9LS/74LS273			Unit
		Min.	Nom.	Max.	Min.	Nom.	Max.	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	Volts
High-Level Output Current, I_{OH}				-400			-400	uA
Low-Level Output Current, I_{OL}				4			8	mA
Clock Frequency, f_{clock}		0		30	0		30	MHz
Width of Clock or Clear Pulse, t_w		20			20			ns
Set-Up Time, t_{su}	Data input	20 ↑			20 ↑			ns
	Clear Inactive State	25 ↑			25 ↑			
Data Hold Time, t_h		5 ↑			5 ↑			ns
Operating Free-Air Temperature, T_A		-55		125	0		70	°C

↑ The arrow indicates that the rising edge of the clock pulse is used for reference.

Electrical Characteristics

Parameter	Test Conditions[1]		9LS/54LS273			9LS/74LS273			Unit
			Min.	Typ.[2]	Max.	Min.	Typ.[2]	Max.	
V_{IH}			2			2			Volts
V_{IL}					0.7			0.8	Volts
V_{IK}	V_{CC} = Min., I_I = -18mA				-1.5			-1.5	Volts
V_{OH}	V_{CC} = Min., V_{IH} = 2.0V V_{IL} = V_{IL}Max., I_{OH} = -400uA		2.5	3.4		2.7	3.4		Volts
V_{OL}	V_{CC} = Min., V_{IH} = 2.0V	I_{OL} = 4mA		0.25	0.4		0.25	0.4	Volts
	V_{IL} = V_{IL}Max.	I_{OL} = 8mA					0.35	0.5	
I_I	V_{CC} = Max., V_I = 7.0V				0.1			0.1	mA
I_{IH}	V_{CC} = Max., V_I = 2.7V				20			20	uA
I_{IL}	V_{CC} = Max., V_I = -0.4V				-0.4			-04	mA
I_{OS}[3]	V_{CC} = Max.		-20		-100	-20		-100	mA
I_{CC}[4]	V_{CC} = Max.			17	27		17	27	mA

Notes 1. For conditions shown as Min. or Max., use the appropriate value specified under recommended operating conditions.
2. All typical values are at V_{CC} = 5.0V, T_A = 25°C.
3. Not more than one output should be shorted at a time and duration of short circuit should not exceed one second.
4. With all outputs open and 4.5V applied to all data and clear inputs. I_{CC} is measured after a momentary ground, then 4.5V is applied to clock.

Switching Characteristics (V_{CC} = 5.0V)

Parameters	-55° C			+25° C			+125° C			Units
	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Test Conditions: C_L = 15pF, R_L = 7KOhms										
$f_{max.}$				30	40					MHz
t_{PHL}					18	27				ns
t_{PLH}					17	27				ns
t_{PHL}					18	27				ns

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8-Bit Universal Shift/Storage Registers LS299

Features

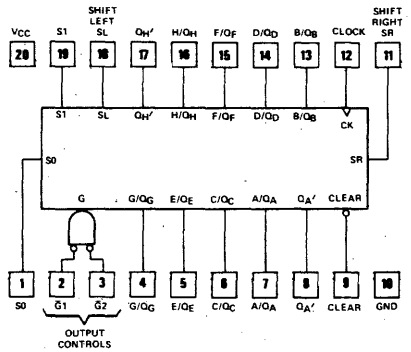
- Multiplexed inputs/outputs provide improved bit density
- Four modes of operation:
  Hold (store) Shift Left
  Shift Right Load Data
- Operates with outputs enabled or at high Z
- 3-state outputs drive bus lines directly
- Can be cascaded for n-bit word lengths
- 54LS299 and 74LS299 are similar but have synchronous clear
- Guaranteed shift (clock) frequency—35MHz
- Typical power dissipation—175mW

Description

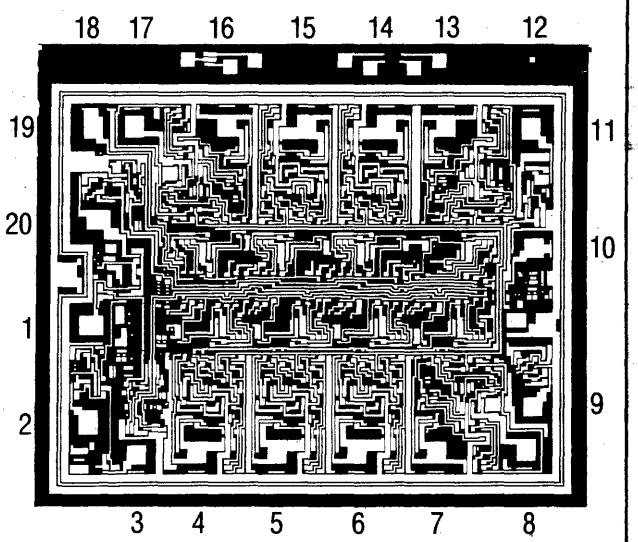
These Schottky TTL eight-bit universal registers feature multiplexed inputs/outputs to achieve full eight bit data handling in a single 20-pin package. Two function-select inputs and two output-control inputs can be used to choose the modes of operation listed in the function table.

Synchronous parallel loading is accomplished by taking both function-select lines, S0 and S1, high. This places the three-state outputs in a high-impedance state, which permits data that is applied on the input/output lines to be clocked into the register. Reading out of the register can be accomplished while the outputs are enabled in any mode. A direct overriding input is provided to clear the register whether the outputs are enabled or off.

Pinout Diagram



logic: see description and function table



Die Size .095 x .114

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LS299 8-Bit Universal Shift/Storage Registers

Function Table

Mode	Inputs								Inputs/Outputs								Outputs	
	Clear	Function Select		Output Control		Clock	Serial		A/Q_A	B/Q_B	C/Q_C	D/Q_D	E/Q_E	F/Q_F	G/Q_G	H/Q_H	Q_A'	Q_H'
		S1	S0	G1†	G2†		SL	SR										
Clear	L	X	L	L	L	X	X	X	L	L	L	L	L	L	L	L	L	L
	L	L	X	L	L	X	X	X	L	L	L	L	L	L	L	L	L	L
Hold	H	L	L	L	L	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	Q_{E0}	Q_{F0}	Q_{G0}	Q_{H0}	Q_{A0}	Q_{H0}
	H	X	X	L	L	L	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	Q_{E0}	Q_{F0}	Q_{G0}	Q_{H0}	Q_{A0}	Q_{H0}
Shift	H	L	H	L	L	↑	X	H	H	Q_{An}	Q_{Bn}	Q_{Cn}	Q_{Dn}	Q_{En}	Q_{Fn}	Q_{Gn}	H	Q_{Gn}
Right	H	L	H	L	L	↑	X	L	L	Q_{An}	Q_{Bn}	Q_{Cn}	Q_{Dn}	Q_{En}	Q_{Fn}	Q_{Gn}	L	Q_{Gn}
Shift	H	H	L	L	L	↑	H	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	Q_{En}	Q_{Fn}	Q_{Gn}	Q_{Hn}	H	Q_{Bn}	H
Left	H	H	L	L	L	↑	L	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	Q_{En}	Q_{Fn}	Q_{Gn}	Q_{Hn}	L	Q_{Bn}	L
Load	H	H	H	X	X	↑	X	X	a	b	c	d	e	f	g	h	a	h

†When one or both output controls are high the eight input/output terminals are disabled to the high-impedance state; however, sequential operation or clearing of the register is not affected.

a . . . h = the level of the steady-state input at inputs A through H, respectively. These data are loaded into the flip-flops while the flip-flop outputs are isolated from the input/output terminals.

Recommended Operating Conditions

		9LS/54LS299			9LS/74LS299			Units
		Min.	Nom.	Max.	Min.	Nom.	Max.	
Supply Voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	Volts
High-Level Output Current, I_{OH}	Q_A thru Q_H			-1			-2.6	mA
	Q_A' or Q_H'			-0.4			-0.4	
Low-Level Output Current, I_{OL}	Q_A thru Q_H			12			24	mA
	Q_A' or Q_H'			4			8	
Clock Frequency, f_{clock}		0		35	0		35	MHz
Width of Clock Pulse, $t_{w(clock)}$	Clock High	20			20			ns
	Clock Low	20			20			
Width of Clear Pulse, $t_{w(clear)}$	Clear Low	20			20			ns
Setup Time, T_{su}	Select	10 ↑			10 ↑			ns
	High-Level*	20 ↑			20 ↑			
	Low-Level*	20 ↑			20 ↑			
	Clear Inactive State	20 ↑			20 ↑			
Hold Time, t_h	Select	10 ↑			10 ↑			ns
	Data*	0 ↑			0 ↑			
Operating Free-Air Temperature, T_A		-55		125	0		70	°C

*Data includes the two serial inputs and the eight input/output data lines.

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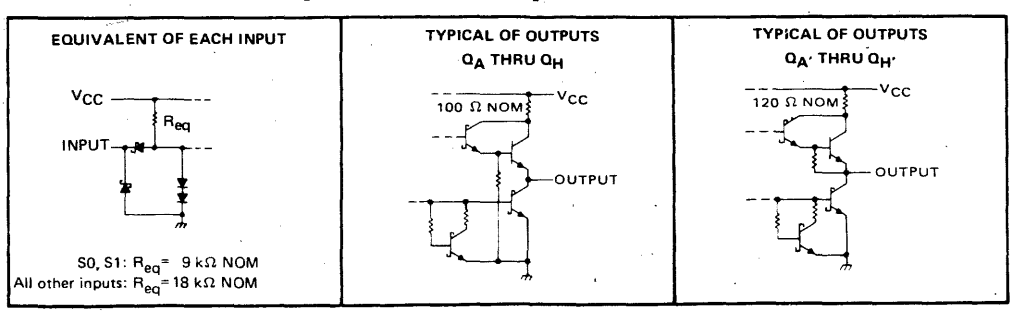
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Electrical Characteristics

Parameter		Test Conditions[1]		9LS/54LS299			9LS/74LS299			Units
				Min.	Typ.[2]	Max.	Min.	Typ.[2]	Max.	
V_{IH}				2			2			Volts
V_{IL}						0.7			0.8	Volts
V_{IK}		V_{CC} = Min., I_I = -18mA				-1.5			-1.5	Volts
V_{OH}	Q_A thru Q_H	V_{CC} = Min., V_{IH} = 2.0V		2.4	3.2		2.4	3.1		Volts
	Q_A' or Q_H'	V_{IL} = V_{IL}Max., I_{OH} = Max.		2.7	3.4		2.7	3.4		
V_{OL}	Q_A thru Q_H	V_{CC} = Min.,	I_{OL} = 12mA		0.25	0.4		0.25	0.4	Volts
		V_{IH} = 2.0V	I_{OL} = 24mA					0.35	0.5	
	Q_A' or Q_H'	V_{IL} = V_{IL}Max.	I_{OL} = 4mA		0.25	0.4		0.25	0.4	
			I_{OL} = 8mA					0.35	0.5	
I_{OZH}	Q_A thru Q_H	V_{CC} = Max., V_{IH} = 2.0V V_O = 2.7V				40			40	uA
I_{OZL}	Q_A thru Q_H	V_{CC} = Max., V_{IH} = 2.0V V_O = 0.4V				-400			-400	uA
I_I	S0, S1	V_{CC} = Max.	V_I = 7.0V			200			200	uA
	A thru H		V_I = 5.5V			100			100	
	Any other		V_I = 7.0V			100			100	
I_{IH}	A thru H, S0, S1	V_{CC} = Max., V_I = 2.7V				40			40	uA
	Any other					20			20	
I_{IL}	S0, S1	V_{CC} = Max., V_I = 0.4V				-0.8			-0.8	mA
	Any other					-0.4			-04	
I_{OS}[3]	Q_A thru Q_H	V_{CC} = Max.		-30		-130	-30		-130	mA
	Q_A' or Q_H'			-20		-100	-20		-100	
I_{CC}		V_{CC} = Max.			35	60		35	60	mA

Notes: 1. For conditions shown as Min. or Max., use the appropriate value specified under recommended operating conditions.
2. All typical values are at V_{CC} = 5.0V, T_A = 25° C.
3. Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.

Schematics of Inputs and Outputs



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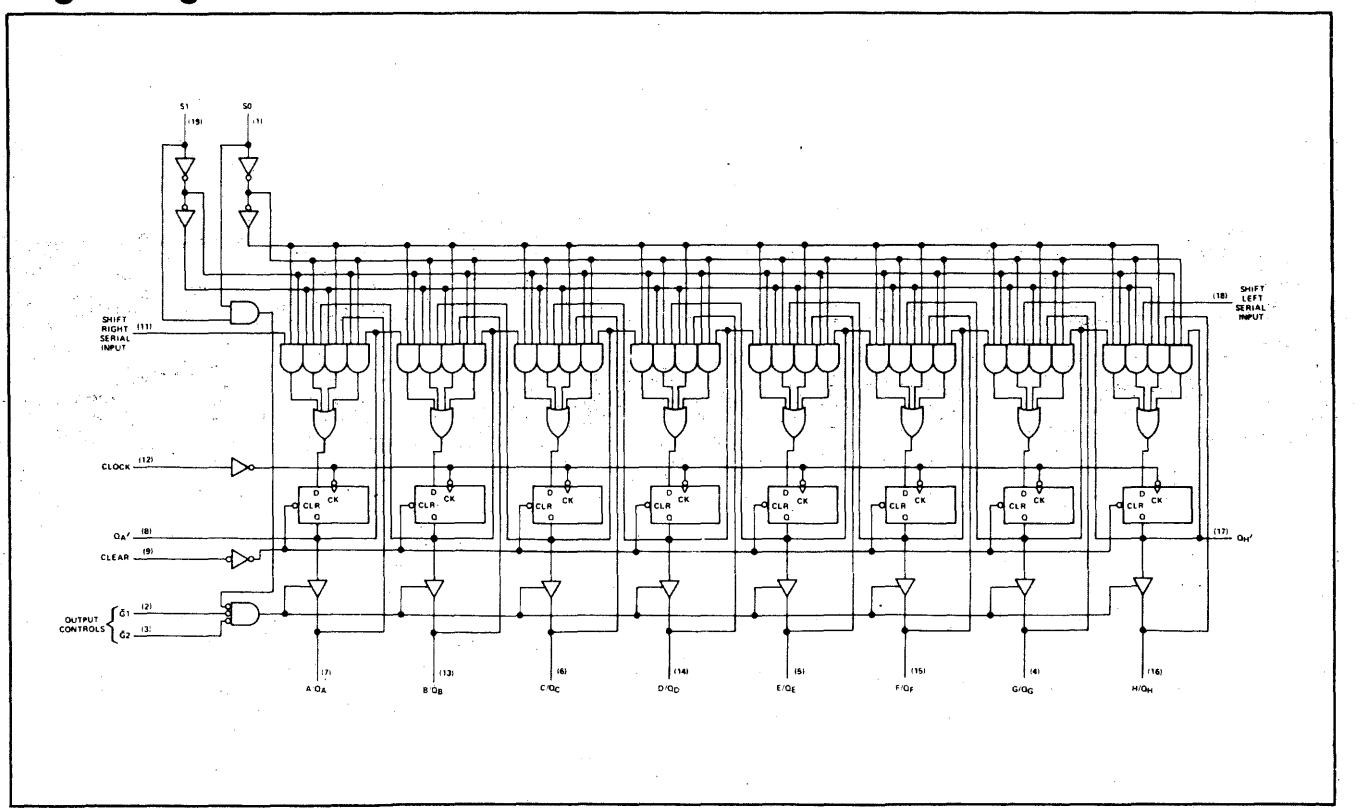
LS299 8-Bit Universal Shift/Storage Registers

Switching Characteristics (V_{CC} = 5V)

Parameter	From (Input)	To (Output)	-55° C			+25° C			+125° C			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Test Conditions: C_L = 15pF, R_L = 2kOhms												
f_{max} *						35	50					MHz
t_{PLH}	Clock	Q_A' or Q_H'					15	25				ns
t_{PHL}							15	25				
t_{PHL}	Clear	Q_A' or Q_H'					20	35				ns
Test Conditions: C_L = 45pF, R_L = 665 Ohms												
t_{PLH}	Clock	Q_A thru Q_H					15	25				ns
t_{PHL}							15	25				
t_{PHL}	Clear	Q_A thru Q_H					20	35				ns
t_{PZH}	$\overline{G}1$, $\overline{G}2$	Q_A thru Q_H					20	35				ns
t_{PZL}							20	35				
Test Conditions: C_L = 5pF, R_L = 665 Ohms												
t_{PHZ}	$\overline{G}1$, $\overline{G}2$	Q_A thru Q_H					15	25				ns
t_{PLZ}							15	25				

* For testing f_{max}, all outputs are loaded simultaneously, each with C_L and R_L as specified for the propagation times.

Logic Diagram



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8-Bit Shift/Storage Register with Synchronous Clear

LS322

Features

- Three-state outputs
- Multiplexed serial data input
- Sign extend function
- Advanced low-power Schottky processing

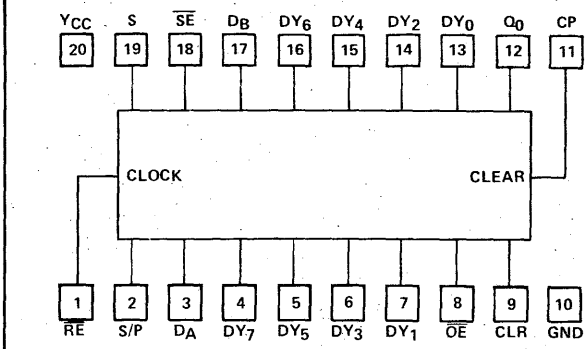
Description

The LS322 is an eight-bit serial/parallel register built using advanced Low-Power Schottky processing. The device features an eight-bit parallel multiplexed input/output port to provide improved bit density in a 20-pin package. Data may be loaded into the device in a serial manner from either input D_A or D_B. A serial output, Q_0, is also provided.

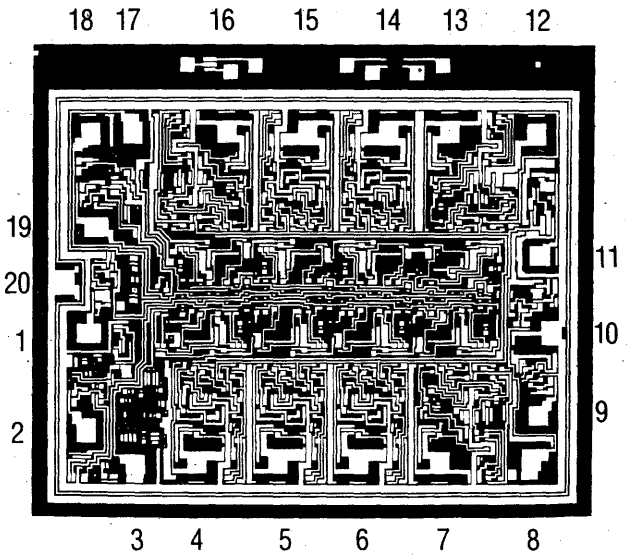
The LS322 is specifically designed for operation with the LS384 serial/parallel two's complement multiplier and provides the sign extend function required for this device.

When the Register Enable ($\overline{RE}$) input is HIGH, the register will retain its current contents. Synchronous parallel loading is accomplished by applying a LOW to $\overline{RE}$ and applying a LOW to the Serial/Parallel (S/P) input. This places the three-state outputs in the high-impedance state independent of $\overline{OE}$ and allows data that is applied on the input/output lines (DY_j) to be clocked into the register. When the S/P input is HIGH, the device will shift right. The Sign Extend ($\overline{SE}$) input is used to repeat the sign in the Q_7 flip-flop. This occurs whenever $\overline{SE}$ is LOW when the SHIFT mode is selected. When $\overline{SE}$ is HIGH, the serial two-input multiplexer is enabled. Thus, either D_A or D_B can be selected to load data serially. The register changes state on the LOW-to-HIGH transition of the clock. A clear input (CLR) is used to asynchronously reset all flip-flops when a LOW is applied.

Pinout Diagram



Note: Pin 1 is marked for orientation.



Die Size .095 x .114

Recommended Operating Conditions

		9LS/54LS			9LS/74LS			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Supply Voltage V_{CC}		4.5	5.0	5.5	4.75	5.0	5.25	Volts
High-Level Output Current I_{OH}	Q_0			-0.44			-0.44	mA
	DY_i			-1.0			-2.6	
Low-Level Output Current I_{OL}			4	8		4	8	mA
Operating Free Air Temperature		-55		125	0		70	°C

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LS322 — 8-Bit Shift/Storage Register with Synchronous Clear

Electrical Characteristics

Parameters	Test Conditions[1]		9LS/74LS Min.	9LS/74LS Typ.[2]	9LS/74LS Max.	9LS/54LS Min.	9LS/54LS Typ.[2]	9LS/54LS Max.	Units
V_{OH}	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	Q_0, I_{OH} = -440uA	2.7			2.5			Volts
		DY_i, I_{OH} = -1.0mA	2.4			2.4			
		DY_i, I_{OH} = -2.6mA	2.4			2.4			
V_{OL}	V_{CC} = Min. V_{IN} = V_{IH} or V_{IL}	I_{OL} = 4.0mA			0.4			0.4	Volts
		I_{OL} = 8.0mA			0.45			0.45	
V_{IH}	Guaranteed input logical HIGH voltage for all inputs		2.0			2.0			Volts
V_{IL}	Guaranteed input logical LOW voltage for all inputs				0.8			0.7	Volts
V_I	V_{CC} = Min., I_{IN} = -18mA				-1.5			-1.5	Volts
I_{IL}[3]	V_{CC} = Max., V_{IN} = 0.4V	$\overline{SE}$			-1.08			-1.08	mA
		S			-0.72			-0.72	
		Others			-0.36			-0.36	
I_{IH}[3]	V_{CC} = Max., V_{IN} 2.7V (Except DY_i)	$\overline{SE}$			60			60	uA
		S			40			40	
		Others			20			20	
I_I	V_{CC} = Max., V_{IN} = 5.5V (Except DY_i)	SE			0.3			0.3	mA
		S			0.2			0.2	
		Others			0.1			0.1	
I_O	V_{CC} = Max.	V_O = 2.4V			40			40	uA
		V_O = 0.4V			-100			-100	
I_{SC}[4]	V_{CC} = Max.		-30		-85	-30		-85	mA
I_{CC}	V_{CC} = Max.			40	65		40	65	mA

Notes:
1. For conditions shown as Min. or Max., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25° C ambient and maximum loading.
3. Actual input currents = Unit Load Current x Input Load Factor (See Loading Rules).
4. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.

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8-Bit Shift/Storage Register with Synchronous Clear

LS322

Switching Characteristics (V_{CC} = 5.0V)

Parameters	From (Input)	To (Output)	-55°C			+25°C			+125°C			Units
			Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Test Conditions: C_L = 50pF, R_L = 2.0kOhms												
t_{PLH}	Clock	DY_i					16.5	24				ns
t_{PHL}							18	26				
t_{PHL}	Clear	DY_i					23	30				ns
t_{PLH}	Clock	Q_0					16.5	24				ns
t_{PHL}							18	26				
t_{PHL}	Clear	Q_0					23	30				ns
Test Conditions: C_L = 5pF, R_L = 2.0kOhms												
t_{ZH}	$\overline{OE}$	DY_i					13	21				ns
t_{ZL}							18	26				
t_{HZ}							13	21				
t_{LZ}							18	26				
t_{ZH}	SER/PAR	DY_i					18	26				ns
t_{ZL}							23	32				
t_{HZ}							18	26				
t_{LZ}							23	32				
t_s	Set Up Time RE to Clock					20						ns
t_s	Set Up Time SE to Clock					10						
t_s	Set Up Time S to Clock					15						
t_s	Set Up Time D_A/D_B to Clock					15						
t_s	Set Up Time DY_i to Clock					15						
t_s	Clear Recovery to Clock					8.0						
t_s	Set Up Time S/P to Clock					15						ns
t_h	Hold Time Any Input					0						
t_h	Clear Hold Time					0						ns
t_{pw}	Clock Pulse Width HIGH					8.0						ns
	Clock Pulse Width LOW					8.0						
t_{pw}	Clear Pulse Width					20						ns
f_{max}	Max. Clock Frequency					50	70					MHZ

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LS323 8-Bit Universal Shift/Storage Registers

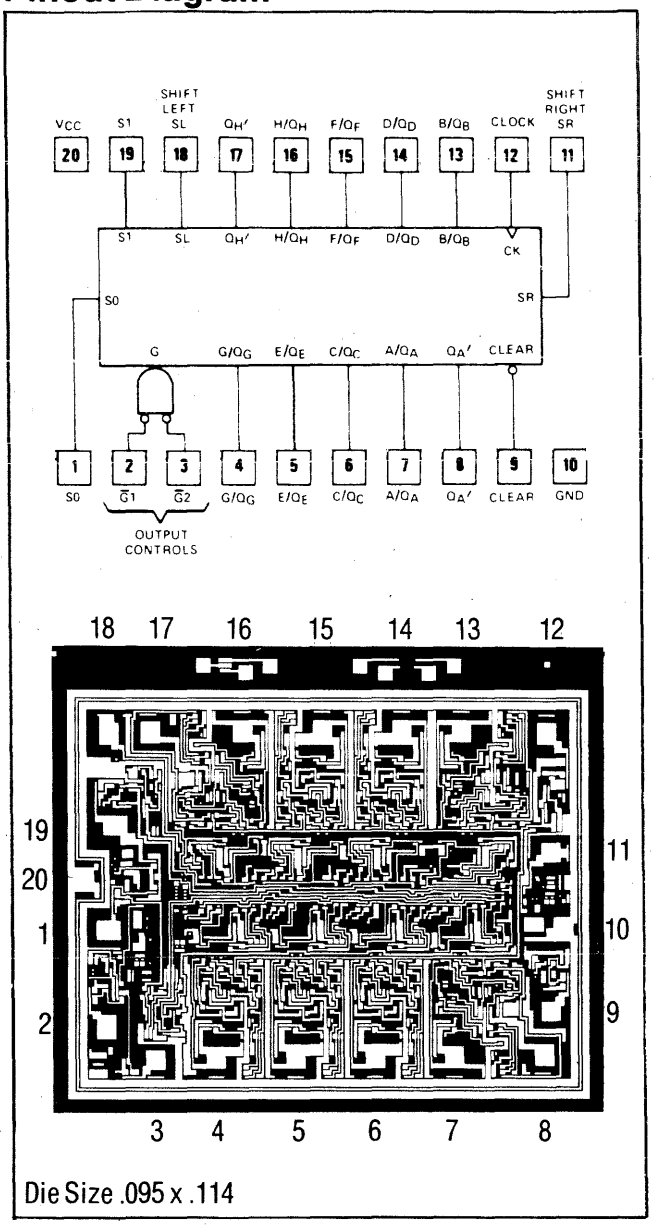
Features

- Multiplexed inputs/outputs provide improved bit density
- Four modes of operation:
  Hold (store) Shift Left
  Shift Right Load Data
- Operates with outputs enabled or at high Z
- 3-state outputs drive bus lines directly
- Can be cascaded for n-bit word lengths
- Typical power dissipation—175mW
- Guaranteed shift (clock) frequency—35MHz
- 9LS/54LS299 and 9LS/74LS299 are similar but have direct overriding clear

Description

These Low-Power Schottky eight-bit universal registers feature multiplexed inputs/outputs to achieve full eight-bit data handling in a single 20-pin package. Two function-select inputs and two output-control inputs can be used to choose the modes of operation listed in the function table. Synchronous parallel loading is accomplished by taking both function-select lines, S0 and S1, high. This places the three-state outputs in a high-impedance state, which permits data that is applied on the input/output lines to be clocked into the register. Reading out of the register can be accomplished while the outputs are enabled in any mode. The clear function is synchronous and a low level at the clear input clears the register on the next low-to-high transition of the clock.

Pinout Diagram



Die Size .095 x .114

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Function Table

Mode	Inputs								Inputs/Outputs								Outputs	
	Clear	Function Select		Output Control		Clock	Serial		A/Q_A	B/Q_B	C/Q_C	D/Q_D	E/Q_E	F/Q_F	G/Q_G	H/Q_H	$Q_{A'}$	$Q_{H'}$
		S1	S0	G1†	G2†		SL	SR										
Clear	L	X	L	L	L	↑	X	X	L	L	L	L	L	L	L	L	L	L
	L	L	X	L	L	↑	X	X	L	L	L	L	L	L	L	L	L	L
Hold	H	L	L	L	L	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	Q_{E0}	Q_{F0}	Q_{G0}	Q_{H0}	Q_{A0}	Q_{H0}
	H	X	X	L	L	L	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	Q_{E0}	Q_{F0}	Q_{G0}	Q_{H0}	Q_{A0}	Q_{H0}
Shift Right	H	L	H	L	L	↑	X	H	H	Q_{An}	Q_{Bn}	Q_{Cn}	Q_{Dn}	Q_{En}	Q_{Fn}	Q_{Gn}	H	Q_{Gn}
	H	L	H	L	L	↑	X	L	L	Q_{An}	Q_{Bn}	Q_{Cn}	Q_{Dn}	Q_{En}	Q_{Fn}	Q_{Gn}	L	Q_{Gn}
Shift Left	H	H	L	L	L	↑	H	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	Q_{En}	Q_{Fn}	Q_{Gn}	Q_{Hn}	H	Q_{Bn}	H
	H	H	L	L	L	↑	L	X	Q_{Bn}	Q_{Cn}	Q_{Dn}	Q_{En}	Q_{Fn}	Q_{Gn}	Q_{Hn}	L	Q_{Bn}	L
Load	H	H	H	X	X	↑	X	X	a	b	c	d	e	f	g	h	a	h

†When one or both output controls are high the eight input/output terminals are disabled to the high-impedance state; however, sequential operation or clearing of the register is not affected.

a . . . h = the level of the steady-state input at inputs A through H, respectively. These data are loaded into the flip-flops while the flip-flop outputs are isolated from the input/output terminals.

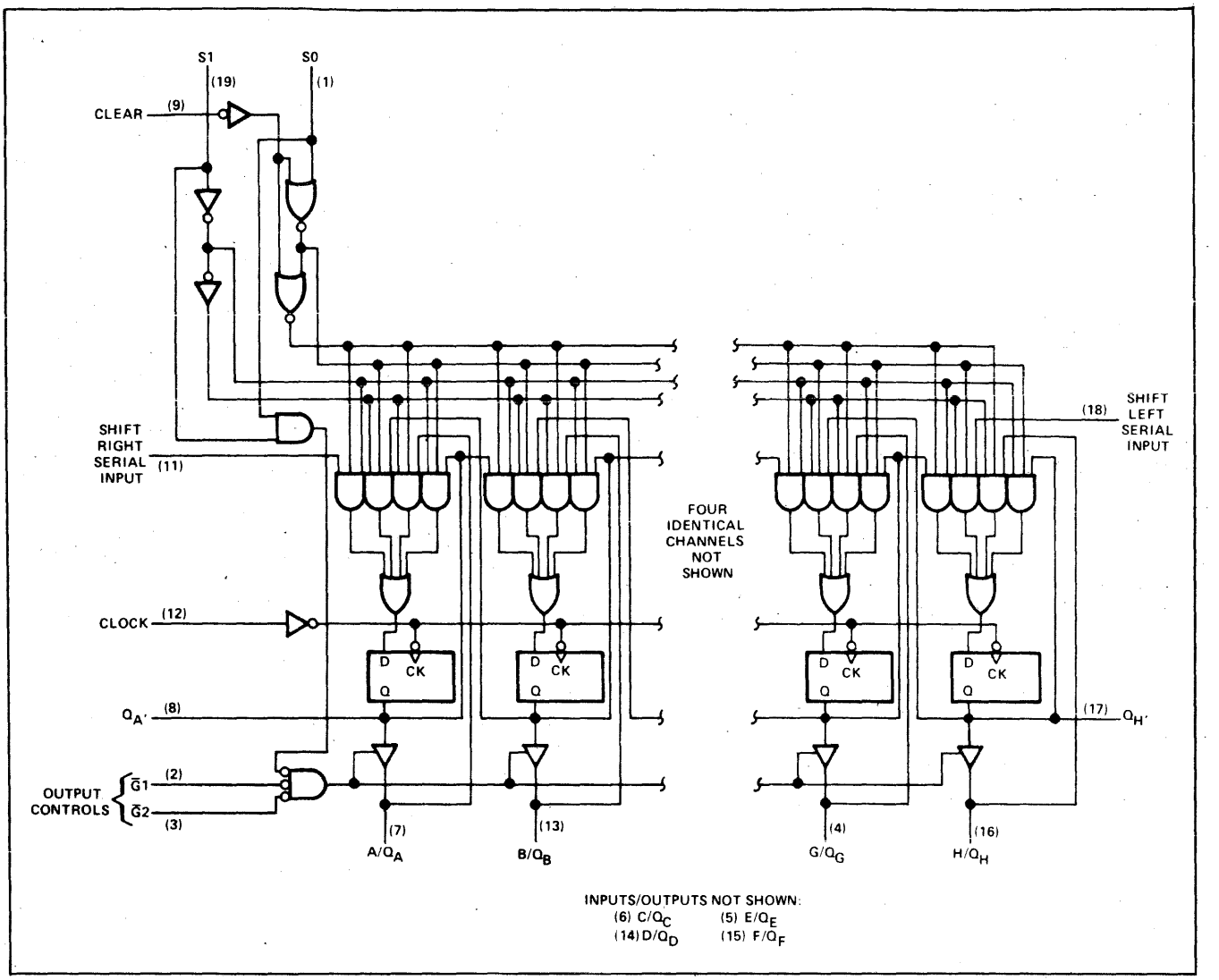
Switching Characteristics (V_{CC} = 5V)

Parameter	From (Input)	To (Output)	-55° C			+25° C			+125° C			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Test Conditions: C_L = 15pF, R_L = 2KOhms												
f_{max}						35	50					MHz
t_{PLH}	Clock	$Q_{A'}$ or $Q_{H'}$					15	25				ns
t_{PHL}							15	25				
Test Conditions: C_L = 45pF, R_L = 665 Ohms												
t_{PLH}	Clock	Q_A thru Q_H					15	25				ns
t_{PHL}						15	25					
t_{PZH}	G1, G2	Q_A thru Q_H					20	35				ns
t_{PZL}							20	35				
Test Conditions: C_L = 5pF, R_L = 665 Ohms												
t_{PHZ}	G1, G2	Q_A thru Q_H					15	25				ns
t_{PLZ}							15	25				

Notes: 1. For testing f_{max}, all outputs are loaded simultaneously, each with C_L and R_L as specified for the propagation times.

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Logic Diagram



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Octal D-Type Transparent Latches and Edge-Triggered Flip-Flops

LS373 LS374

Features

- Choice of 8 latches or 8 D-type flip-flops in a single package
- 3-state bus-driving outputs
- Full parallel-access for loading
- Clock/Enable input has hysteresis to improve noise rejection
- 54LS363 and 74LS364 are similar but have higher V_{OH} for MOS interface

Description

These 8-bit registers feature totem-pole three-state outputs designed specifically for driving highly-capacitive or relatively low-impedance loads. The high-impedance third state and increased high-logic-level drive provide these registers with the capability of being connected directly to and driving the bus lines in a bus-organized system without need for interface or pull-up components. They are particularly attractive for implementing buffer registers, I/O ports, bi-directional bus drivers, and working registers.

The eight latches of the LS373 are transparent D-type latches meaning that while the enable (G) is high the Q outputs will follow the data (D) inputs. When the enable is taken low the output will be latched at the level of the data that was setup.

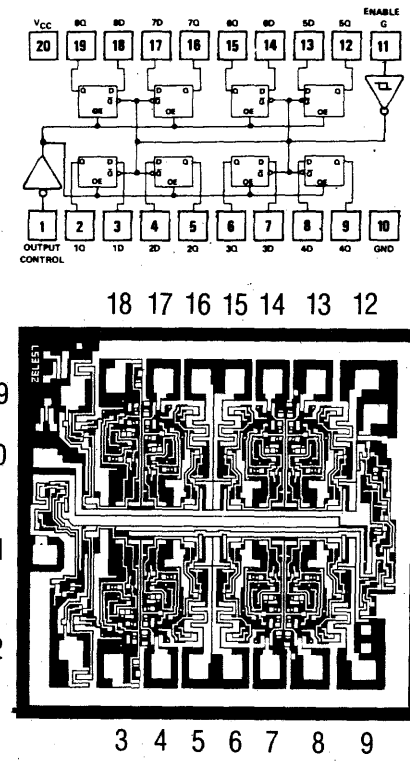
The eight flip-flops of the LS374 are edge-triggered D-type flip flops. On the positive transition of the clock, the Q outputs will be set to the logic states that were setup at the D inputs.

Schmitt-trigger buffered inputs at the enable/clock lines simplify system design as AC and DC noise rejection is improved by typically 400mV due to the input hysteresis. A buffered output control input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state the outputs neither load nor drive the bus lines significantly.

The output control does not affect the internal operation of the latches or flip-flops. That is, the old data can be retained or new data can be entered even while the outputs are off.

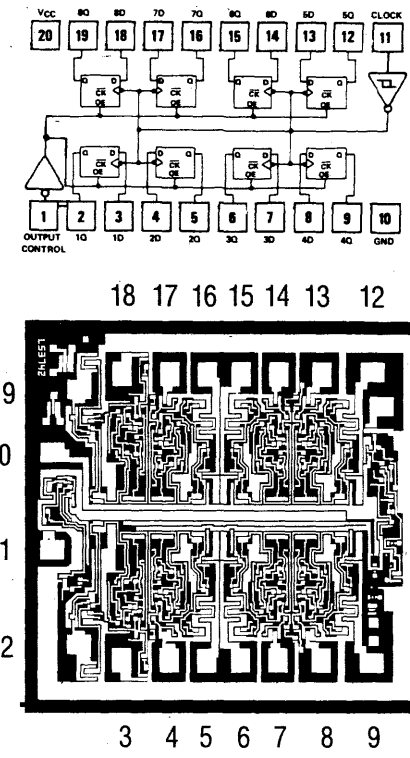
Pinout Diagrams

LS373



Die Size .084 x .080

LS374



Die Size .084 x .080

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LS373 LS374 Octal D-Type Transparent Latches and Edge-Triggered Flip-Flops

LS373 Function Table

Output Control	Enable G	D	Output
L	H	H	H
L	H	L	L
L	L	X	Q0
H	X	X	Z

LS374 Function Table

Output Control	Clock	D	Output
L	↑	H	H
L	↑	L	L
L	L	X	Q0
H	X	X	Z

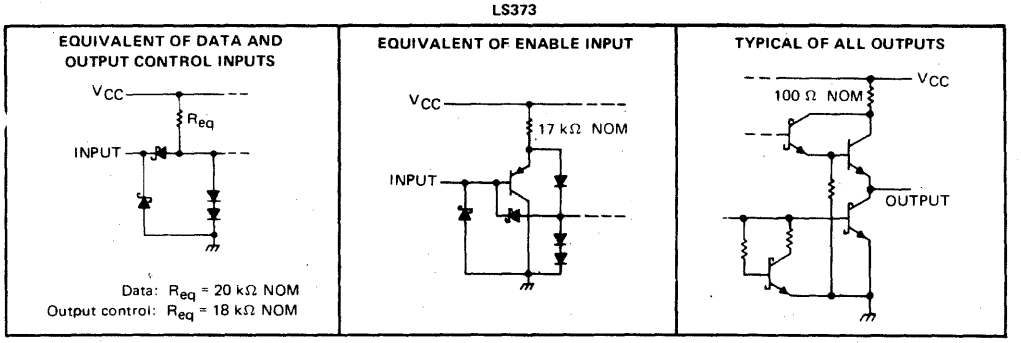
Recommended Operating Conditions

		9LS/54LS			9LS/74LS			Units
		Min.	Nom.	Max.	Min.	Nom.	Max.	
Supply Voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	Volts
High-Level Output Voltage, V_{OH}				5.5			5.5	V
High-Level Output Current, I_{OH}				-1			-2.6	mA
Width of Clock Pulse, $t_{w(clock)}$	High	15			15			ns
	Low	15			15			
Data Setup Time, t_{su}	LS373	0 ↓			0 ↓			ns
	LS374	20 ↑			20 ↑			
Data Hold Time, t_h	LS373	10 ↓			10 ↓			ns
	LS374	0 ↑			0 ↑			
Operating Free-Air Temperature, T_A		-55		125	0		70	°C

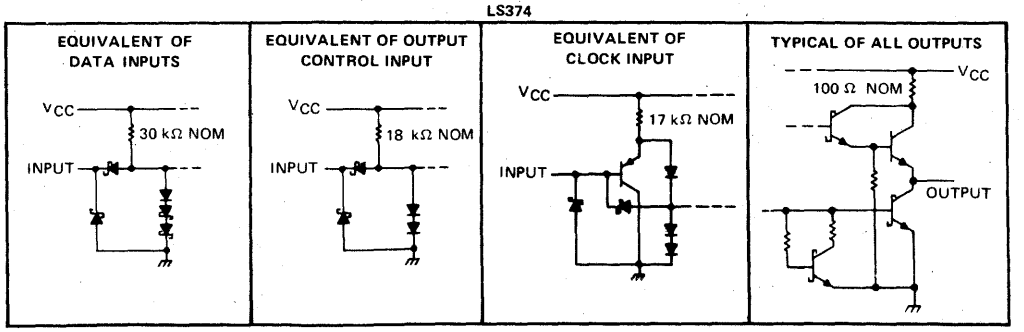
↑↓ The arrow indicates the transition of the clock/enable input used for reference: ↑ for the low-to-high transition, ↓ for the high-to-low transition.

Schematic of Inputs and Outputs

LS373



LS374



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Octal D-Type Transparent Latches and Edge-Triggered Flip-Flops

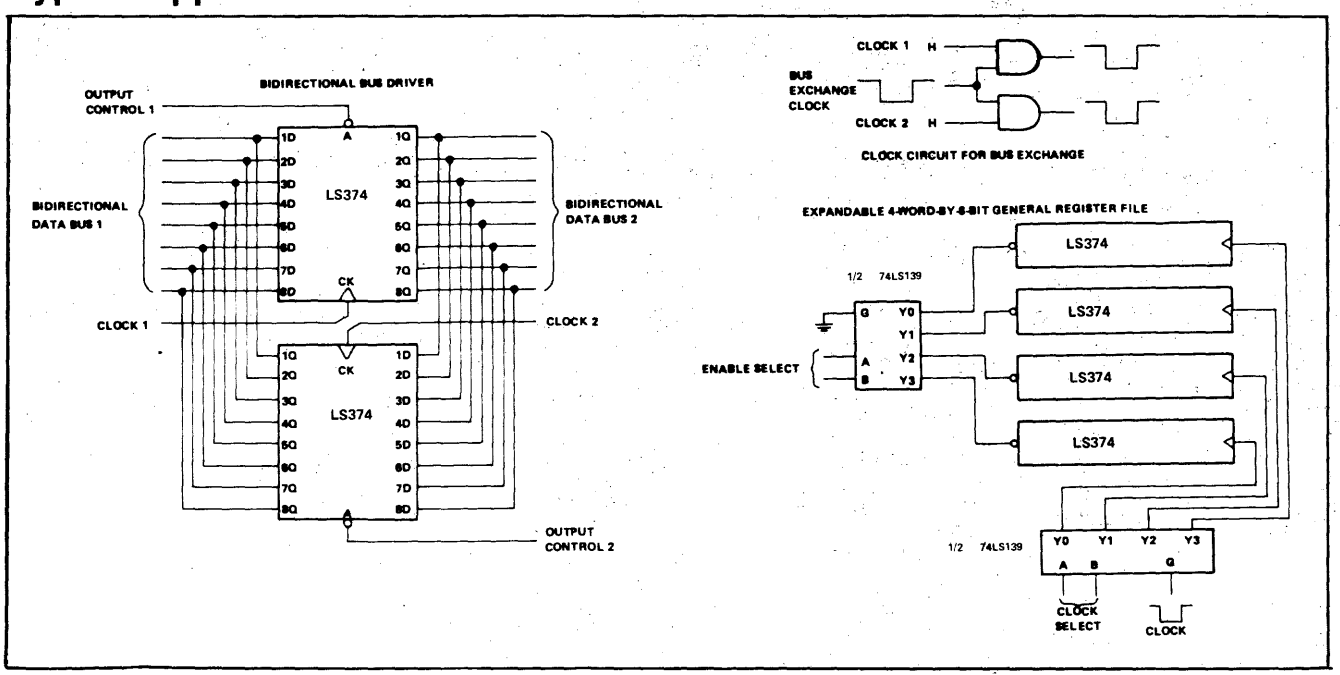
LS373 LS374

Electrical Characteristics

Parameter	Test Conditions[1]		9LS/54LS Min.	9LS/54LS Typ.[2]	9LS/54LS Max.	9LS/74LS Min.	9LS/74LS Typ.[2]	9LS/74LS Max.	Unit
V_{IH}			2			2			Volts
V_{IL}					0.7			0.8	Volts
V_{IK}	V_{CC} = Min., I_I = -18mA				-1.5			-1.5	Volts
V_{OH}	V_{CC} = Min., V_{IH} = 2.0V V_{IL} = V_{ILMax}., I_{OH} = Max.		2.4	3.4		2.4	3.1		Volts
V_{OL}	V_{CC} = Min., V_{IH} = 2.0V	I_{OL} = 12mA		0.25	0.4		0.25	0.4	Volts
	V_{IL} = V_{ILMax}.	I_{OL} = 24mA					0.35	0.5	
I_{OZH}	V_{CC} = Max., V_{IH} = 2.0V V_O = 2.7V				20			20	uA
I_{OZL}	V_{CC} = Max., V_{IH} = 2.0V V_O = 0.4V				-20			-20	uA
I_I	V_{CC} = Max., V_I = 7.0V				0.1			0.1	mA
I_{IH}	V_{CC} = Max., V_I = 2.7V				20			20	uA
I_{IL}	V_{CC} = Max., V_I = 0.4V				-0.4			-0.4	mA
I_{OS}[3]	V_{CC} = Max.		-30		-130	-30		-130	mA
I_{CC}[4]	V_{CC} = Max.	LS373		24	40		24	40	mA
	Output control at 4.5V	LS374		27	40		27	40	

Notes: 1. For conditions shown as Min. or Max., use the appropriate value specified under recommended operating conditions.
2. All typical values are at V_{CC} = 5.0V, T_A = 25°C.
3. Not more than one output should be shorted at a time and duration of short circuit should not exceed one second.
4. With all outputs open and 4.5V applied to all data and clear inputs, I_{CC} is measured after a momentary ground, then 4.5V is applied to clock.

Typical Application Data



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LS373 Switching Characteristics (VCC = 5V)

Parameter	From (Input)	To (Output)	-55° C			+25° C			+125° C			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Test Conditions: C_L = 45pF, R_L = 667 Ohms												
f_{max}												MHz
t_{PLH}	Data	Any Q					12	18				ns
t_{PHL}							12	18				
t_{PLH}	Clock or Enable	Any Q					20	30				ns
t_{PHL}							18	30				
t_{PZH}	Output Control	Any Q					15	28				ns
t_{PZL}							25	36				
Test Conditions: C_L = 5pF, R_L = 667 Ohms												
t_{PHZ}	Output Control	Any Q					12	20				ns
t_{PLZ}							15	25				

LS374 Switching Characteristics (VCC = 5V)

Parameter	From (Input)	To (Output)	-55° C			+25° C			+125° C			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Test Conditions: C_L = 45pF, R_L = 667 Ohms												
f_{max}						35	50					MHz
t_{PLH}	Data	Any Q										ns
t_{PHL}												
t_{PLH}	Clock or Enable	Any Q					15	28				ns
t_{PHL}							19	28				
t_{PZH}	Output Control	Any Q					20	28				ns
t_{PZL}							21	28				
Test Conditions: C_L = 5pF, R_L = 667 Ohms												
t_{PHZ}	Output Control	Any Q					12	20				ns
t_{PLZ}							14	25				

Notes: 1. Maximum clock frequency is tested with all outputs loaded.

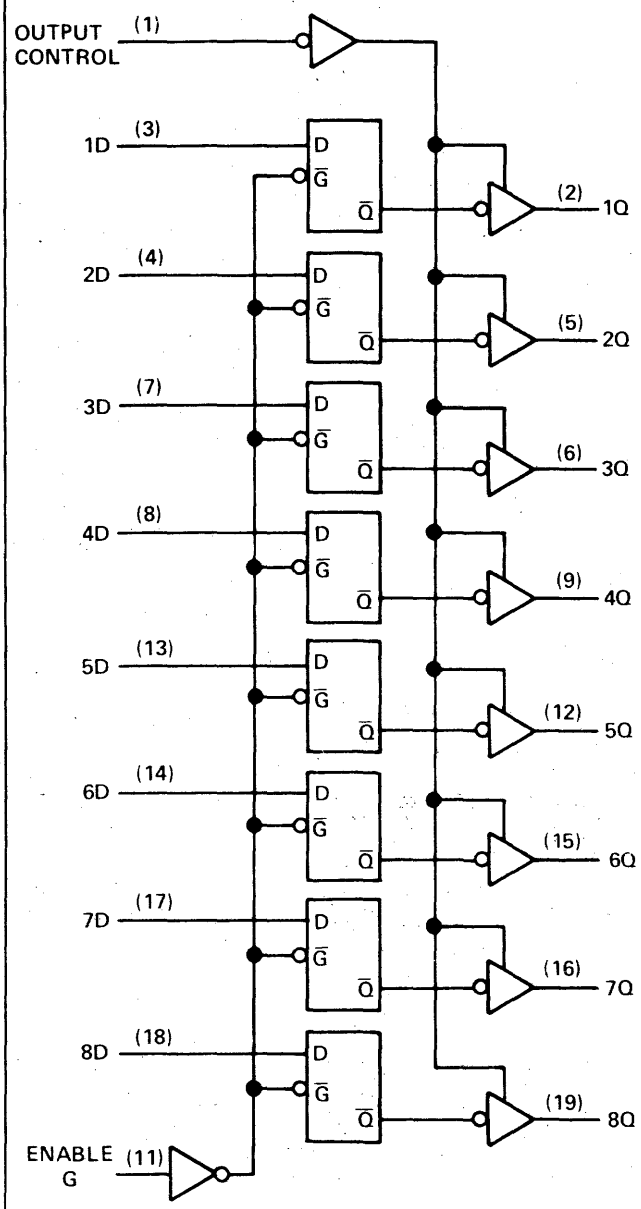
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Octal D-Type Transparent Latches and Edge-Triggered Flip-Flops

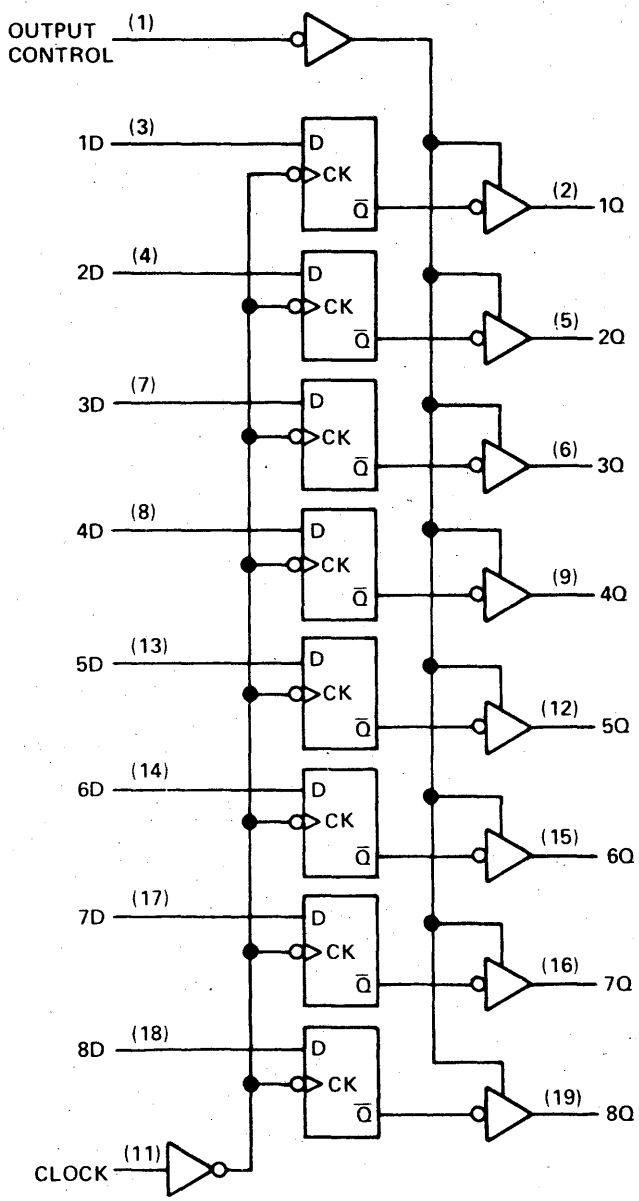
LS373 LS374

Logic Diagrams

LS373
TRANSPARENT LATCHES



LS374
POSITIVE-EDGE-TRIGGERED FLIP-FLOPS



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LS377 Octal D-Type Flip-Flops with Enable

Features

- LS377 contains eight flip-flops with single-rail outputs
- Individual data input to each flip-flop

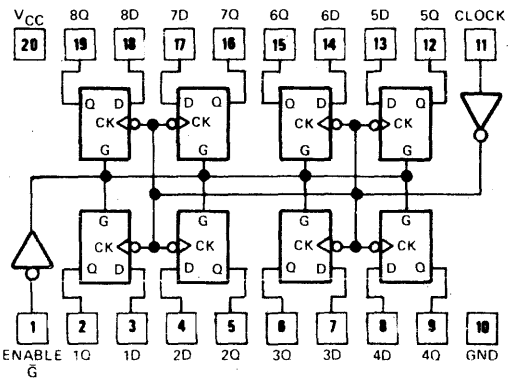
Description

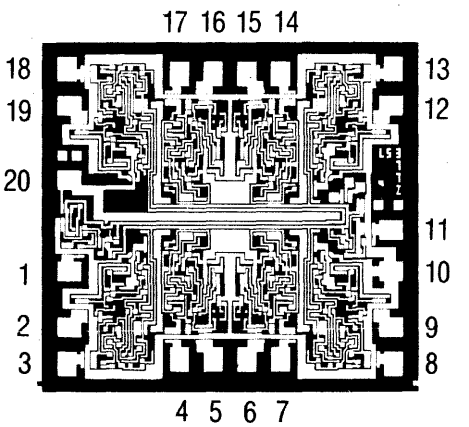
These monolithic, positive-edge-triggered flip-flops utilize TTL circuitry to implement D-type flip-flop logic with an enable input. The LS377 is similar to the LS273, but features a common enable instead of a common clear.

Information at the D inputs meeting the setup time requirements is transferred to the Q outputs on the positive-going edge of the clock pulse if the enable input G is low. Clock triggering occurs at a particular voltage level and is not directly related to the transition time of the positive-going pulse. When the clock input is at either the high or low level, the D input signal has no effect at the output. The circuits are designed to prevent false clocking by transitions at the G input.

These flip-flops are guaranteed to respond to clock frequencies ranging from 0 to 30MHz while maximum clock frequency is typically 40MHz. Typical power dissipation is 10mW per flip-flop.

Pinout Diagram





Die Size .078 x .071

Function Table

(Each flip-flop)

Inputs			Outputs	
$\bar{G}$	Clock	Data	Q	$\bar{Q}$
H	X	X	Q_0	$\bar{Q}_0$
L	↑	H	H	L
L	↑	L	L	H
X	L	X	Q_0	$\bar{Q}_0$

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Recommended Operating Conditions

		9LS/54LS			9LS/74LS			Unit
		Min.	Nom.	Max.	Min.	Nom.	Max.	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	Volts
High-Level Output Current, I_{OH}				-400			-400	uA
Low-Level Output Current, I_{OL}				4			8	mA
Clock Frequency, f_{clock}		0		30	0		30	MHz
Width of Clock or Clear Pulse, t_w		20			20			ns
Set-Up Time, t_{su}	Data input	20 ↑			20 ↑			ns
	Enable Active-State	25 ↑			25 ↑			
	Enable Inactive-State	10 ↑			10 ↑			
Hold Time, t_h		5 ↑			5 ↑			ns
Operating Free-Air Temperature, T_A		-55		125	0		70	°C

↑ The arrow indicates that the rising edge of the clock pulse is used for reference.

Electrical Characteristics Over Operating Range

Parameter	Test Conditions[1]		9LS/74LS			9LS/54LS			Unit
			Min.	Typ.[2]	Max.	Min.	Typ.[2]	Max.	
V_{IH}			2			2			Volts
V_{IL}					0.7			0.8	Volts
V_{IK}	V_{CC} = Min., I_I = -18mA				-1.5			-1.5	Volts
V_{OH}	V_{CC} = Min., V_{IH} = 2.0V V_{IL} = V_{IL}Max., I_{OH} = -400uA		2.5	3.5		2.7	3.5		Volts
V_{OL}	V_{CC} = Min., V_{IH} = 2.0V	I_{OL} = 4mA		0.25	0.4		0.25	0.4	Volts
	V_{IL} = V_{IL}Max.	I_{OL} = 8mA					0.35	0.5	
I_I	V_{CC} = Max., V_I = 7.0V				0.1			0.1	mA
I_{IH}	V_{CC} = Max., V_I = 2.7V				20			20	uA
I_{IL}	V_{CC} = Max., V_I = -0.4V				-0.4			-0.4	mA
I_{OS}[3]	V_{CC} = Max.		-20		-100	-20		-100	mA
I_{CC}[4]	V_{CC} = Max.			17	28		17	28	mA

Notes: 1. For conditions shown as Min. or Max., use the appropriate value specified under recommended operating conditions.
2. All typical values are at V_{CC} = 5.0V, T_A = 25° C.
3. Not more than one output should be shorted at a time and duration of short circuit should not exceed one second.
4. With all outputs open and 4.5V applied to all data and clear inputs, Icc is measured after a momentary ground, then 4.5V is applied to clock.

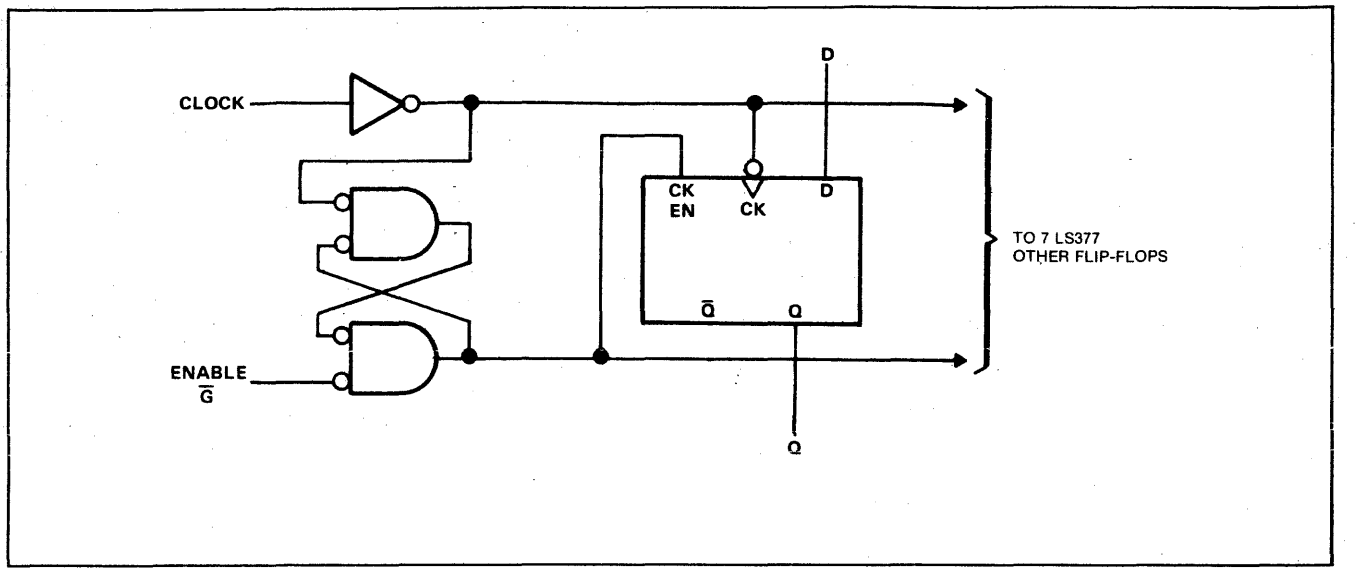
Switching Characteristics (V_{CC} = 5V)

Parameters	-55° C			+25° C			+125° C			Units
	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Test Conditions: C_L = 15pF, R_L = 2kOhms										
$f_{max.}$				30	40					MHz
t_{PLH}					17	27				ns
t_{PHL}					18	27				ns

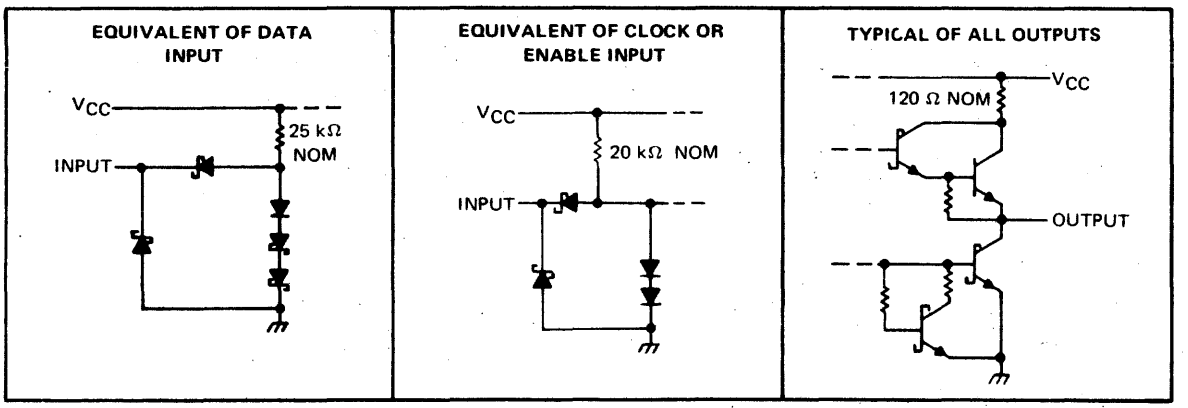
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LS377 Octal D-Type Flip-Flops with Enable

Logic Diagram



Schematics of Inputs and Outputs



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8-Bit Serial/Parallel Two's Complement Multiplier

LS384

Description

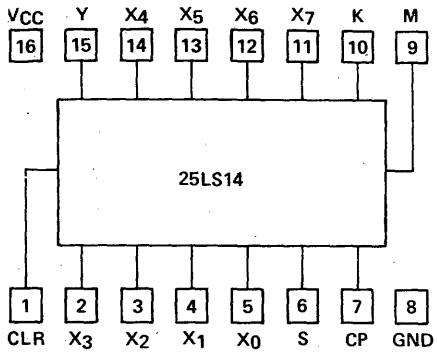
The LS384 is an 8-bit by 1-bit sequential logic element that performs digital multiplication of two numbers represented in two's complement form to produce a two's complement product without correction by using Booth's algorithm internally. The device accepts an 8-bit multiplicand (X input) and stores this data in eight internal latches. The X latches are controlled via the clear input. When the clear input is LOW, all internal flip-flops are cleared and the X latches are opened to accept new multiplicand data. When the clear input is HIGH, the latches are closed and are insensitive to X input changes.

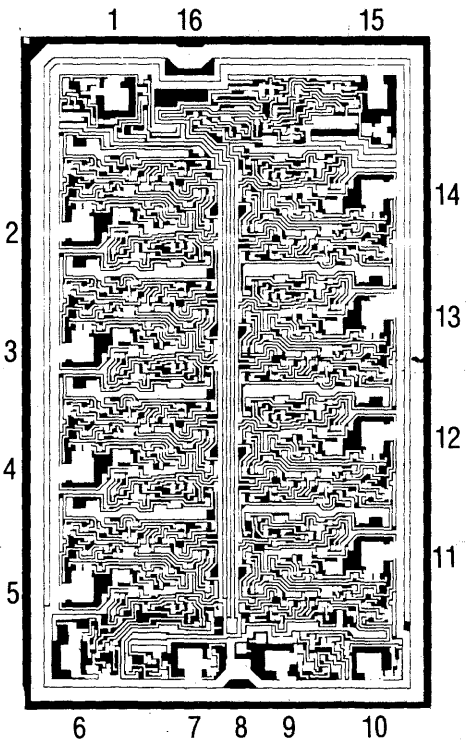
The multiplier word data is passed by the Y input in a serial bit stream—least significant bit first. The product is clocked out the S output least significant bit first.

The multiplication of an m-bit multiplicand by an n-bit multiplier results in an m + n bit product. The LS384 must be clocked for m + n clock cycles to produce this two's complement product. Likewise, the n-bit multiplier (Y-input) sign bit data must be extended for the remaining m-bits to complete the multiplication cycle.

The device also contains a K input so that devices can be cascaded for longer length X words. The sum (S) output of the device is connected to the K input of the succeeding device when cascading. Likewise, a mode input (M) is used to indicate which device contains the most significant bit. The mode input is wired HIGH or LOW depending on the position of the 8-bit slice in the total X word length.

Pinout Diagram





Die Size: .141 x .088

Recommended Operating Conditions

	9LS/54LS			9LS/74LS			
	Min.	Typ.	Max.	Min.	Typ.	Max.	Units
Supply Voltage V_{CC}	4.75	5	5.25	4.5	5	5.5	Volts
High-Level Output Current I_{OH}			-1			-1	mA
Low-Level Output Current I_{OL}		8	12		8	12	mA
Operating Free Air Temperature	-55		125	0		70	°C

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LS384 — 8-Bit Serial/Parallel Two's Complement Multiplier

Electrical Characteristics

Parameters	Test Conditions		9LS/74LS Min.	9LS/74LS Typ.	9LS/74LS Max.	9LS/54LS Min.	9LS/54LS Typ.	9LS/54LS Max.	Units
V_{OH}	V_{CC} = Min., I_{OH} = -1.0mA V_{IN} = V_{IH} or V_{IL}		2.5	3.4		2.7	3.4		Volts
V_{OL}	V_{CC} = Min.	I_{OL} = 8.0mA			.4			.4	Volts
	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 12mA			0.45			0.45	
V_{IH}	Guaranteed input logical HIGH voltage for all inputs		2.0			2.0			Volts
V_{IL}	Guaranteed input logical LOW voltage for all inputs				0.8			0.8	Volts
V_I	V_{CC} = Min., I_{IN} = -18mA				-1.2			-1.2	Volts
I_{IL}	V_{CC} = Max., V_{IN} = 0.4V	X, M			-0.48			-0.48	mA
		K, $\overline{CLR}$			-1.2			-1.2	
		CP			-1.6			-1.6	
		Y			-3.2			-3.2	
I_{IH}	V_{CC} = Max., V_{IN} = 2.7V	X, M			20			20	uA
		K, $\overline{CLR}$			30			30	
		CP			40			40	
		Y			80			80	
I_I	V_{CC} = Max., V_{IN} = 5.5V				1.0			1.0	mA
I_{SC}	V_{CC} = Max.		-40		-100	-40		-100	mA
I_{CC}	V_{CC} = Max.			91	155		91	155	mA

Switching Characteristics (V_{CC} = 5.0V)

Parameters	From (Input)	To (Output)	-55° C Min.	-55° C Typ.	-55° C Max.	+25° Min.	+25° Typ.	+25° Max.	+125° Min.	+125° Typ.	+125° Max.	Units
Test Conditions C_L = 15pF, R_L = 2.0kOhms												
t_{PLH}	Clock	Y					13	20				ns
t_{PHL}	Clock	Y					13	20				ns
t_{PHL}	Clear	X					17	25				ns
t_s	Set Up Time	Y to Clock				32						ns
t_h	Hold Time					0						ns
t_s	Set Up Time	K to Clock				18						ns
t_h	Hold Time					0						ns
t_s	Set Up Time	X_j to Clear				13						ns
t_h	Hold Time					0						ns
t_{pw}	Clock Pulse Width	Clock HIGH				15						ns
		Clock LOW				15						ns
t_{pw}	Clear Pulse Width					20						ns
t_s	Clear Recovery Time					18						ns
f_{max}[1]	Max. Clock Frequency					25	40					MHz

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8-Bit Serial/Parallel Two's Complement Multiplier

LS384

Function Table

Inputs						Internal	Output	Function
CLR	CP	K	M	X_i	Y	Y-1	S	
—	—	L	L	—	—	—	—	Most significant multiplier device
—	—	CS	H	—	—	—	—	Devices cascaded in multiplier string
L	—	—	—	OP	—	L	L	Load new multiplicand and clear internal sum and carry registers
H	—	—	—	—	—	—	—	Device Enabled
H	↑	—	—	—	L	L	AR	Shift sum register
H	↑	—	—	—	L	H	AR	Add multiplicand to sum register and shift
H	↑	—	—	—	H	L	AR	Subtract multiplicand from sum register and shift
H	↑	—	—	—	H	H	AR	Shift sum register

H = HIGH
L = LOW
↑ = LOW-to-HIGH transition
CS = Connected to S output of higher order device
OP = X_i latches open for new data (1 = 0, 7)
AR = Output as required per Booth's algorithm

Definition of Functional Terms

X_0, X_1, X_2, X_3, X_4, X_5, X_6, X_7 The eight data inputs for the multiplicand (X) data.

Y The serial input for the multiplier (Y) data—least significant bit first.

S The serial output for the product of X Y—least significant bit first.

CP Clock The buffered common clock input for the serial/parallel multiplier. All functions occur on the LOW-to-HIGH transition of the clock.

CLR Clear The buffered common clear for all flip-flops withing the device. When the clear is LOW all flip-flops are cleared. Also the buffered X-input latch enable. When the clear input is LOW, the X latches will accept new X-input data.

K The sum expansion input to the serial/parallel multiplier. Allows for cascading devices.

M The mode control input for the most significant bit of the multiplier. It is used in conjunction with cascading to determine the most significant bit.

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LS385 Quad Serial Adder/Subtractor

Features

- Four independent adder/subtractors
- Use with two's complement arithmetic
- Magnitude only addition/subtraction
- Advanced low-power Schottky

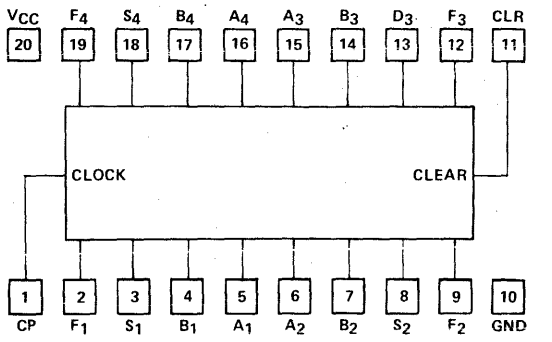
Description

The LS385 is a serial two's complement adder/subtractor designed for use in association with the LS384 serial/parallel two's complement multiplier. This device can also be used for magnitude only or one's complement addition or subtraction.

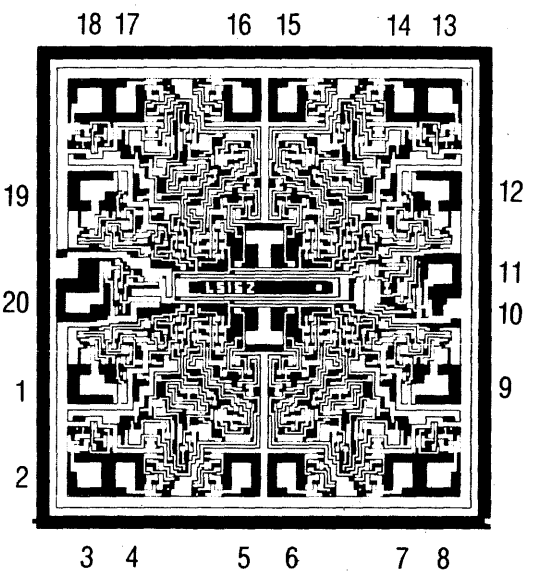
Four independent adder/subtractors are provided with common clock and clear inputs. The add function is A plus B and the subtract function is A minus B. The clear function sets the internal carry function to logic zero in the add mode and to logic one in subtract mode. This least significant carry is self propagating in the subtract mode as long as zeroes are applied to the A and B inputs at the LSB's. All internal flip-flops change state on the LOW-to-HIGH clock transition.

The LS385 is particularly useful for recursive or non-recursive digital filtering or butterfly networks in Fast Fourier Transforms.

Pinout Diagram



Note: Pin 1 is marked for orientation



Die Size: .098 x .094

Recommended Operating Conditions

	9LS/54LS			9LS/74LS			
	Min.	Typ.	Max.	Min.	Typ.	Max.	Units
Supply Voltage V_{CC}	4.5	5.0	5.5	4.75	5.0	5.25	Volts
High-Level Output Current I_{OH}			-0.44			-0.44	mA
Low-Level Output Current I_{OL}			8			8	mA
Operating Free Air Temperature	-55		125	0		70	°C

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Electrical Characteristics

Parameters	Test Conditions[1]		9LS/74LS Min.	9LS/74LS Typ.[2]	9LS/74LS Max.	9LS/54LS Min.	9LS/54LS Typ.[2]	9LS/54LS Max.	Units
V_{OH}	V_{CC} = Min., I_{OH} = -440uA V_{IN} = V_{IH} or V_{IL}		2.7			2.5			Volts
V_{OL}	V_{CC} = Min.	I_{OL} = 4.0mA			0.4			0.4	Volts
	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 8.0mA			0.45			0.45	
V_{IH}	Guaranteed input logical HIGH voltage for all inputs		2.0			2.0			Volts
V_{IL}	Guaranteed input logical LOW voltage for all inputs				0.8			0.7	Volts
V_I	V_{CC} = Min., I_{IN} = -18mA				1.5			1.5	Volts
I_{IL}[3]	V_{CC} = Max., V_{IN} = 0.4V				-0.36			-0.36	mA
I_{IH}[3]	V_{CC} = Max., V_{IN} = 2.7V				20			20	uA
I_I	V_{CC} = Max., V_{IN} = 7.0V				0.1			0.1	mA
I_{SC}[4]	V_{CC} = Max.		-30		-85	-30		-85	mA
I_{CC}[5]	V_{CC} = Max.			48	75		48	75	mA

Notes: 1. For conditions shown as Min. or Max., use the appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical limits are at V_{CC} = 5.0V, 25° C ambient and maximum loading.
3. Actual input curents = Input Load Current x Input Load Factor (See Loading Rules).
4. Not more than one output should be shorted at a time. Duration of the short circuit test should not exceed one second.
5. All inputs HIGH, measured after a LOW-to-HIGH clock transition.

Switching Characteristics (V_{CC} = 5.0V)

Parameters	From (Input)	To (Output)	-55° C Min.	-55° C Typ.	-55° C Max.	+25° C Min.	+25° C Typ.	+25° C Max.	+125° C Min.	+125° C Typ.	+125° C Max.	Units
Test Conditions C_L = 15pF, R_L = 2.0kOhms												
t_{PLH}	Clock	F					14	22				ns
t_{PHL}							14	22				
t_{PHL}	Clear	F					20	30				ns
t_s	Set Up Time	A, B, S				10						ns
t_h	Hold Time					0						
t_s	Clear Recovery Time					25						ns
t_h	Clear Hold Time					0						
t_{pw}	Clock Pulse Width	Clock HIGH				17						ns
		Clock LOW				17						
t_{pw}	Clear Pulse Width					20						ns
f_{max}[1]	Max. Clock Frequency					30	40					MHz

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LS385 Quad Serial Adder/Subtractor

Function Table

External Inputs					Internal Point		Output	
CP	CLR	S	A	B	C	C_1	F	Function
X	L	L	X	X	L	L	L	Clear
X	L	H	X	X	H	H	L	
L	H	X	X	X	NC	NC	NC	
H	H	X	X	X	NC	NC	NC	
↑	H	L	L	L	L	L	L	
↑	H	L	L	L	H	L	H	
↑	H	L	L	H	L	L	H	
↑	H	L	L	H	H	H	L	Add
↑	H	L	H	L	L	L	H	
↑	H	L	H	L	H	H	L	
↑	H	L	H	H	L	H	L	
↑	H	L	H	H	H	H	H	
↑	H	H	L	L	L	L	H	
↑	H	H	L	L	H	H	L	
↑	H	H	L	H	L	L	L	
↑	H	H	L	H	H	L	H	Subject
↑	H	H	H	L	L	H	L	
↑	H	H	H	L	H	H	H	
↑	H	H	H	H	L	L	H	
↑	H	H	H	H	H	H	L	

C = Data in the carry flip-flop before the clock transition

C_1 = Data in the carry flip-flop after the clock

X = Don't Care

NC= No Change

H = HIGH

L = LOW

↑ = LOW-to-HIGH Transision

Definition of Functional Terms

A_1, A_2, A_3, A_4 The "A" input into each adder/subtractor.

B_1, B_2, B_3, B_4 The "B" input into each adder/subtractor.

S_1, S_2, S_3, S_4 The add subtract control for each adder/subtractor. When S is LOW, the F function is A + B. When S is HIGH, the F function is A - B.

F_1, F_2, F_3, F_4 The four independent serial outputs of the adder/subtractor.

CP Clock The clock input for the device. All internal flip-flops change state on the LOW-to-HIGH transition.

CLR Clear When the clear input is LOW, the four independent adder/subtractors are asynchronously reset. The sum flip-flop is always set to logic "0". The carry flip-flop is set to logic "0" in the add mode and logic "1" in the subtract mode.

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4-Bit Cascadable Shift Registers with 3-State Outputs

LS395A

Features

- Three-state, 4-bit, cascadable, parallel-in, parallel-out registers
- LS395A offers three times the sink-current capability of LS395
- Low power dissipation—75mW typical (enabled)
- Applications:
  - N-bit serial-to-parallel converter
  - N-bit parallel-to-serial converter
  - N-bit storage register

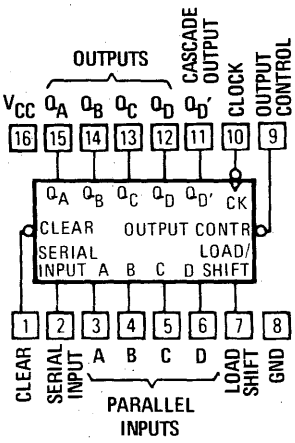
Description

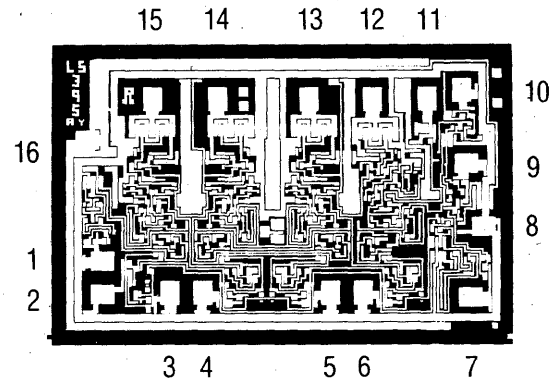
These 4-bit registers feature parallel inputs, parallel outputs, and clock, serial, load/shift, output control and direct overriding clear inputs.

Shifting is accomplished when the load/shift control is low. Parallel loading is accomplished by applying the four bits of data and taking the load/shift control input high. The data is loaded into the associated flip-flops and appears at the outputs after the high-to-low transition of the clock input. During parallel loading, the entry of serial data is inhibited.

When the output control is low, the normal logic levels of the four outputs are available for driving the loads or bus lines the outputs are disabled independently from the level of the clock by a high logic level at the output control input. The outputs then present a high impedance and neither load nor drive the bus line; however, sequential operation of the registers is not affected. During the high-impedance mode, the output at Q_D' is still available for cascading.

Pinout Diagram





Die Size .063 x .098

Function Table

Inputs								3-State Outputs				Cascade
	Load/Shift			Parallel								Output
Clear	Control	Clock	Serial	A	B	C	D	Q_A	Q_B	Q_C	Q_D	Q_D'
L	X	X	X	X	X	X	X	L	L	L	L	L
H	H	H	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	Q_{D0}
H	H	↓	X	a	b	c	d	a	b	c	d	d
H	L	H	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	Q_{D0}
H	L	↓	H	X	X	X	X	H	Q_{An}	Q_{Bn}	Q_{Cn}	Q_{Cn}
H	L	↓	L	X	X	X	X	L	Q_{An}	Q_{Bn}	Q_{Cn}	Q_{Cn}

When the output control is high, the 3-state outputs are disabled to the high-impedance state; however, sequential operation of the registers and the output at Q_D' are not affected.

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LS395A

4-Bit Cascadable Shift Registers with 3-State Outputs

Recommended Operating Conditions

		9LS/54LS395A			9LS/74LS395A			
		Min.	Typ.	Max.	Min.	Typ.	Max.	Units
Supply Voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	Volts
High-Level Output Current, I_{OH}	Q_A thru Q_D			-1			-2.6	mA
	Q_D			-400			-400	uA
Low-Level Output Current, I_{OL}	Q_A thru Q_D			12			24	mA
	Q_D			4			8	mA
Clock Frequency, f_{clock}		0		25	0		25	MHz
Width of Clock Pulse, $t_{w(clock)}$		25			25			ns
Setup Time, High-Level or Low-Level Data, t_{su}		20			20			ns
Hold Time, High-Level or Low-Level, t_h		10			10			ns
Operating Free-Air Temperature, T_A		-55		125	0		70	°C

Electrical Characteristics

Parameter		Test Conditions[1]		9LS/54LS395A			9LS/74LS395A			Units
				Min.	Typ.[2]	Max.	Min.	Typ.[2]	Max.	
V_{IH}				2			2			Volts
V_{IL}						0.7			0.8	Volts
V_{IK}		V_{CC} = Min., I_I = -18mA				-1.5			-1.5	Volts
V_{OH}	Q_A thru Q_D	V_{CC} = Min., V_{IH} = 2.0V		2.4	3.4		2.4	3.1		Volts
	Q_D	V_{IL} = V_{IL}Max., I_{OH} = Max.		2.5	3.4		2.7	3.4		
V_{OL}	Q_A, Q_B	V_{CC} = Min.,	I_{OL} = 12mA		0.25	0.4		0.25	0.4	Volts
	Q_C, Q_D	V_{IH} = 2.0V	I_{OL} = 24mA					0.35	0.5	
	Q_D	V_{IL} = V_{IL}Max.	I_{OL} = 4mA		0.25	0.4		0.25	0.4	
			I_{OL} = 8mA					0.35	0.5	
I_{OZH}	Q_A, Q_B Q_C, Q_D	V_{CC} = Max., V_{IH} = 2.0V V_O = 2.7V				20			20	uA
I_{OZL}	Q_A, Q_B Q_C, Q_D	V_{CC} = Max., V_{IH} = 2.0V V_O = 0.4V				-20			-20	uA
I_I		V_{CC} = Max., V_I = 7.0V				0.1			0.1	mA
I_{IH}		V_{CC} = Max., V_I = 2.7V				20			20	uA
I_{IL}		V_{CC} = Max., V_I = 0.4V				-0.4			-0.4	mA
I_{OS}[3]	Q_A thru Q_D	V_{CC} = Max.		-30		-130	-30		-130	mA
	Q_D			-20		-100	-20		-100	
I_{CC}	Condition A	V_{CC} = Max.[4]			22	34		22	34	mA
	Condition B				21	31		21	31	

Notes: 1. For conditions shown as Min. or Max., use the appropriate value specified under recommended operating conditions.
2. All typical values are at V_{CC} = 5.0V, T_A = 25° C.
3. Not more than one output should be shorted at a time and duration of the short-circuit should not exceed one second.
4. I_{CC} is measured with the outputs open, the serial input and mode control at 4.5V, and the data inputs grounded under the following conditions:
   A. Output control at 4.5V and a momentary 3V, then ground, applied to clock input.
   B. Output control and clock input grounded.

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4-Bit Cascadable Shift Registers with 3-State Outputs

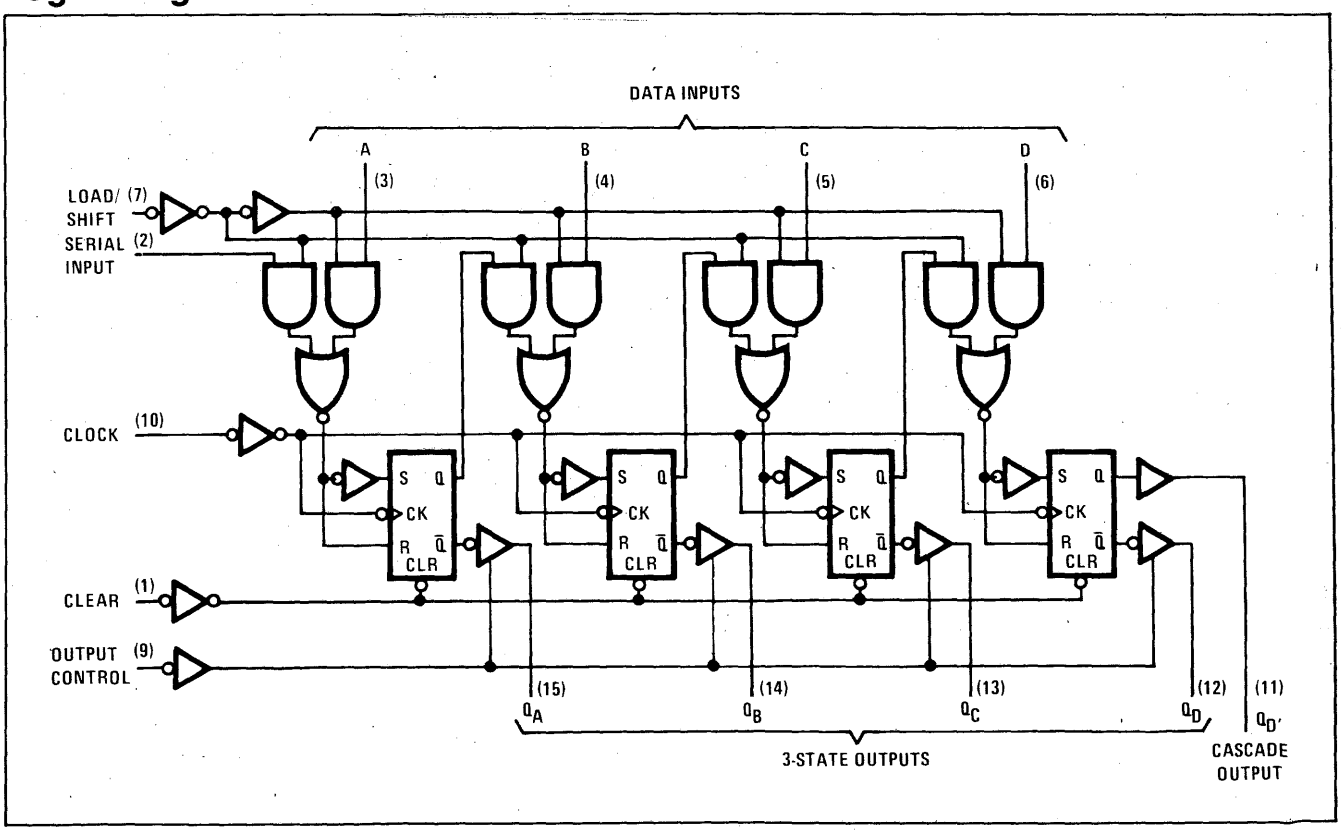
LS395A

Switching Characteristics (V_{CC} = 5.0V)

Parameters	-55° C			+25° C			+125° C			Units
	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Test Conditions: C_L = 45pF, R_L = 667 Ohms[1]; C_L = 15pF, R_L = 2kOhms[2]										
f_{max}				30	45					MHz
t_{PHL}					22	35				ns
t_{PLH}					15	30				ns
t_{PHL}					20	30				ns
t_{PZH}					15	25				ns
t_{PZL}					17	25				ns
Test Conditions: C_L = 5.0pF										
t_{PHZ}					11	17				ns
t_{PLZ}					12	20				ns

Notes: 1. Q_A, Q_B, Q_C, Q_D outputs.
2. Q_D' output.

Logic Diagram

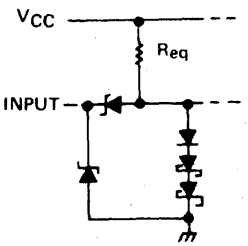


LS395A

4-Bit Cascadable Shift Registers with 3-State Outputs

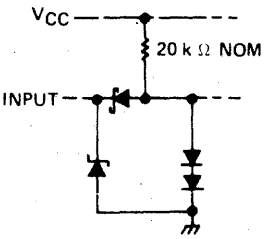
Schematics of Inputs and Outputs

EQUIVALENT OF SERIAL AND DATA INPUTS

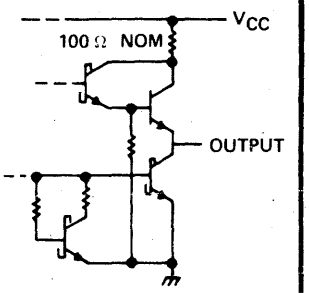


Serial: R_{eq} = 30 kΩ NOM
A, B, C, D: R_{eq} = 20 kΩ NOM

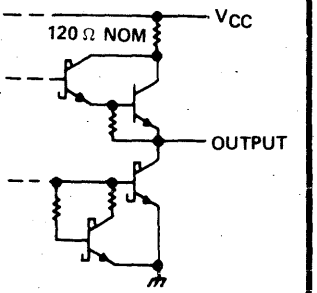
EQUIVALENT OF OTHER INPUTS



TYPICAL OF Q_A, Q_B, Q_C, Q_D OUTPUTS



TYPICAL OF Q_D' OUTPUTS



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54S/74S350
(AM25S10)

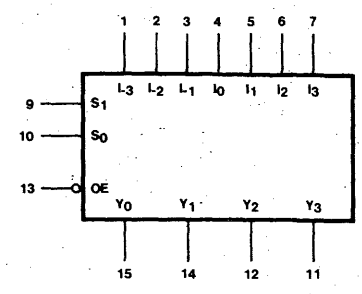
DESCRIPTION

The "350" is a combinatorial logic circuit that accepts a 4-bit data word and shifts the word 0, 1, 2, or 3 places. The number of places to be shifted is determined by two Select inputs S_0 and S_1. The 3-state outputs allow expansion of shifting over a larger number of places.

FEATURES

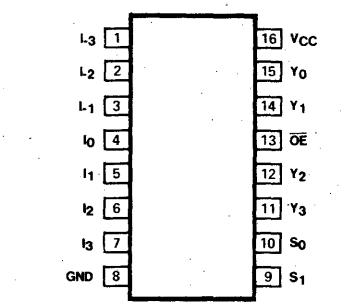
- **Shifts 4-bits of data to 0, 1, 2, 3 places under control of two select lines**
- **3-State outputs for bus organized systems**
- **Alternate source AM25S10**

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

PIN CONFIGURATION



ORDERING CODE (See Section 9 for further Package and Ordering Information)

PACKAGES	COMMERCIAL RANGES V_{CC}=5V±5%; T_A=0°C to +70°C	MILITARY RANGES V_{CC}=5V±10%; T_A=−55°C to +125°C
Plastic DIP	N74S350N	
Ceramic DIP	N74S350F	S54S350F
Flatpak		S54S350W

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE[a]

PINS	DESCRIPTION		54/74	54S/74S	54LS/74LS
S_0, S_1	Select inputs	I_{IH} (μA) I_{IL} (mA)		50 −2.0	
I_0, I_1, I_2, I_{-1}, I_{-2}	Data inputs	I_{IH} (μA) I_{IL} (mA)		75 −3.0	
I_3, I_{-3}	Data inputs	I_{IH} (μA) I_{IL} (mA)		50 −2.0	
$\overline{OE}$	Output Enable (active LOW) input	I_{IH} (μA) I_{IL} (mA)		50 −2.0	
Y_0 - Y_3	3-State outputs	I_{OH} (mA) I_{OL} (mA)		−2/−6.5 20	

NOTE

a. The slashed numbers indicate different parametric values for Military/Commercial temperature ranges respectively.

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FUNCTIONAL DESCRIPTION

The "350" is a combination logic circuit that shifts a 4-bit word from "0" to "3" places. No clocking is required as with shift registers.

The "350" can be used to shift any number of bits any number of places up or down by suitable interconnection. Shifting can be:

1. Logical - with logic zeros filled in at either end of the shifting field
2. Arithmetic - where the sign bit is extended during a shift down
3. End around - where the data word forms a continuous loop.

The 3-state outputs are useful for bus interface applications or expansion to a larger number of shift positions in end around shifting. The active LOW Output Enable ($\overline{OE}$) input controls the state of the outputs. The outputs are in the high impedance "off" state when $\overline{OE}$ is HIGH, and they are active when $\overline{OE}$ is LOW.

TRUTH TABLE

$\overline{OE}$	S_1	S_0	I_3	I_2	I_1	I_0	I_{-1}	I_{-2}	I_{-3}	Y_3	Y_2	Y_1	Y_0
H	X	X	X	X	X	X	X	X	X	Z	Z	Z	Z
L	L	L	D_3	D_2	D_1	D_0	X	X	X	D_3	D_2	D_1	D_0
L	L	H	X	D_2	D_1	D_0	D_{-1}	X	X	D_2	D_1	D_0	D_{-1}
L	H	L	X	X	D_1	D_0	D_{-1}	D_{-2}	X	D_1	D_0	D_{-1}	D_{-2}
L	H	H	X	X	X	D_0	D_{-1}	D_{-2}	D_{-3}	D_0	D_{-1}	D_{-2}	D_{-3}

H = HIGH voltage level
L = Low voltage level
X = Don't care
(Z) = High impedance (off) state
D_n = HIGH or LOW state of the referenced I_n input

LOGIC EQUATIONS

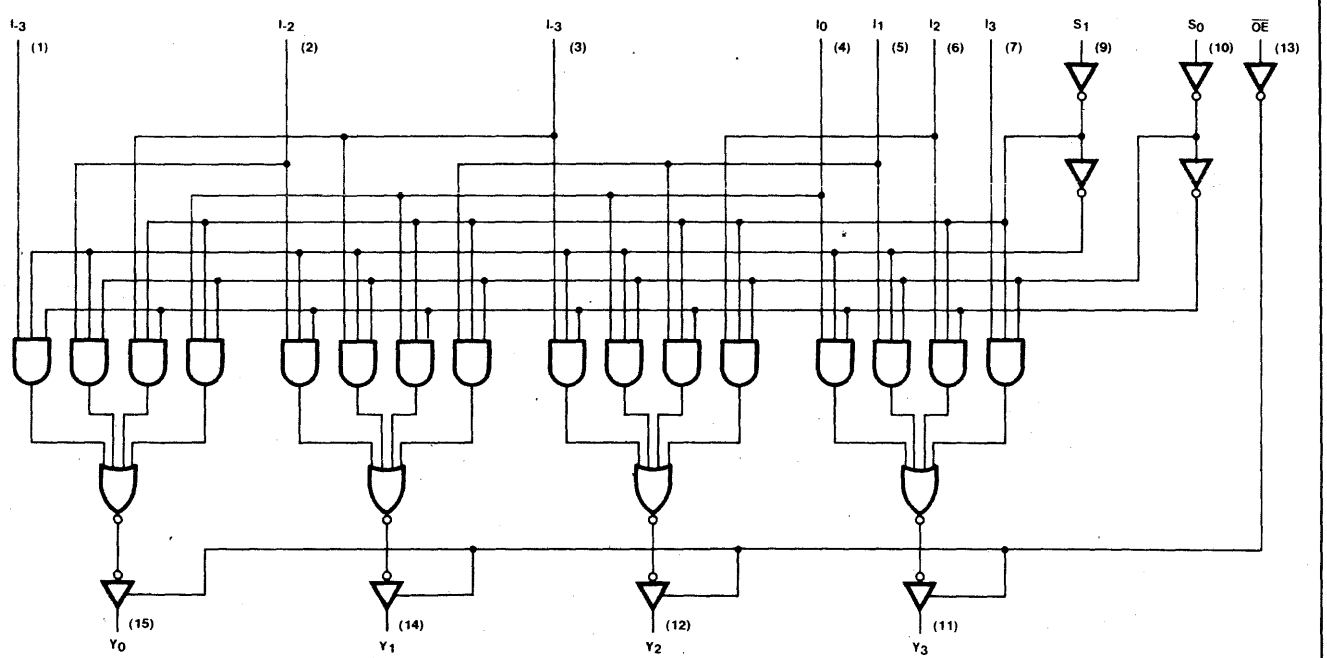
$$Y_0 = S_0 \bullet S_1 \bullet I_0 + S_0 \bullet S_1 \bullet I_{-1} + S_0 \bullet S_1 \bullet I_{-2} + S_0 \bullet S_1 \bullet I_{-3}$$

$$Y_1 = S_0 \bullet S_1 \bullet I_1 + S_0 \bullet S_1 \bullet I_0 + S_0 \bullet S_1 \bullet I_{-1} + S_0 \bullet S_1 \bullet I_{-2}$$

$$Y_2 = S_0 \bullet S_1 \bullet I_2 + S_0 \bullet S_1 \bullet I_1 + S_0 \bullet S_1 \bullet I_0 + S_0 \bullet S_1 \bullet I_{-1}$$

$$Y_3 = S_0 \bullet S_1 \bullet I_3 + S_0 \bullet S_1 \bullet I_2 + S_0 \bullet S_1 \bullet I_1 + S_0 \bullet S_1 \bullet I_0$$

LOGIC DIAGRAM

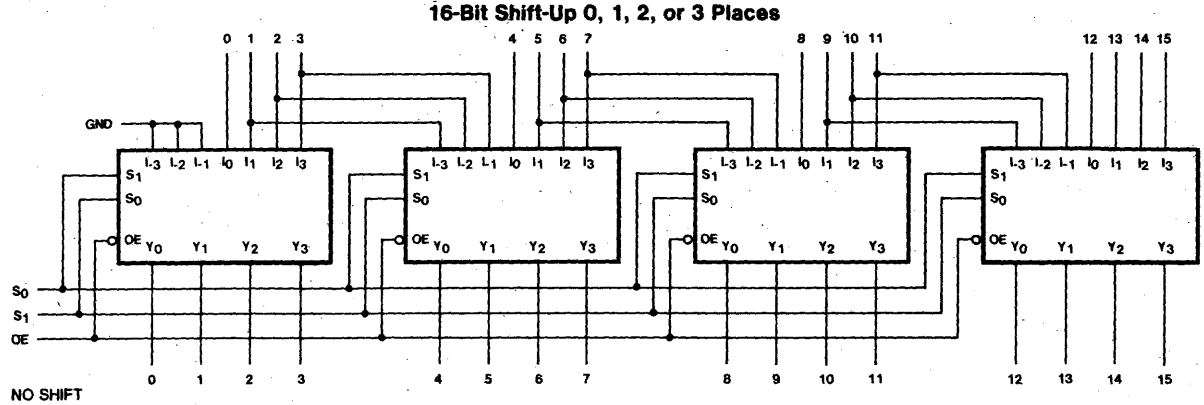


V_{CC} = Pin 16
GND = Pin 8
( ) = Pin Numbers

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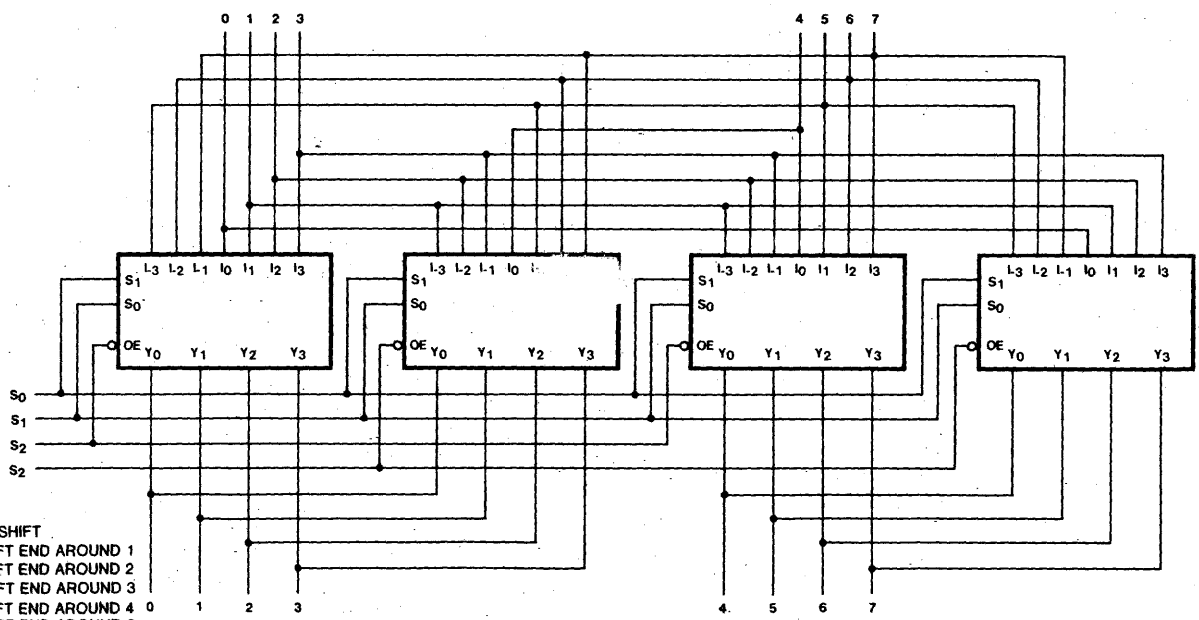
APPLICATIONS

16-Bit Shift-Up 0, 1, 2, or 3 Places



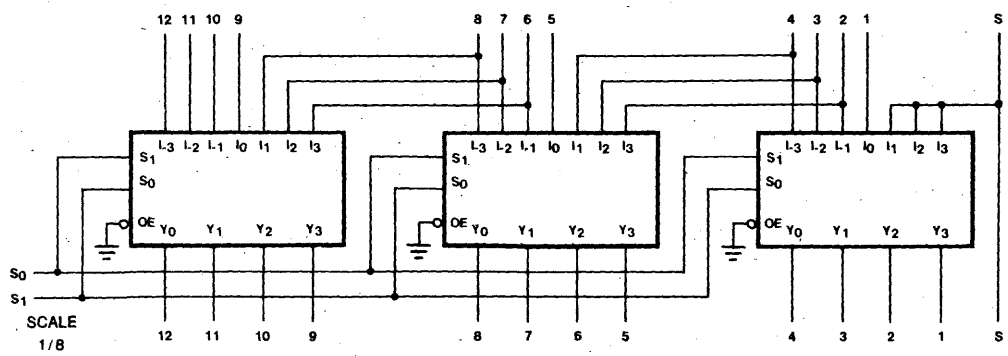
S_1	S_0	
L	L	NO SHIFT
L	H	SHIFT 1 PLACE
H	L	SHIFT 2 PLACES
H	H	SHIFT 3 PLACES

8-Bit End Around Shift 0, 1, 2, 3, 4, 5, 6, 7 Places



S_2	S_1	S_0	
L	L	L	NO SHIFT
L	L	H	SHIFT END AROUND 1
L	H	L	SHIFT END AROUND 2
L	H	H	SHIFT END AROUND 3
H	L	L	SHIFT END AROUND 4
H	L	H	SHIFT END AROUND 5
H	H	L	SHIFT END AROUND 6
H	H	H	SHIFT END AROUND 7

13-Bit 2's Complement Scaler



S_1	S_0		SCALE
L	L	÷8	1/8
L	H	÷4	1/4
H	L	÷2	1/2
H	H	NO CHANGE	1

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DUAL LINEAR-ANTILOG VOLTAGE CONTROLLED AMPLIFIER 2020

DESCRIPTION

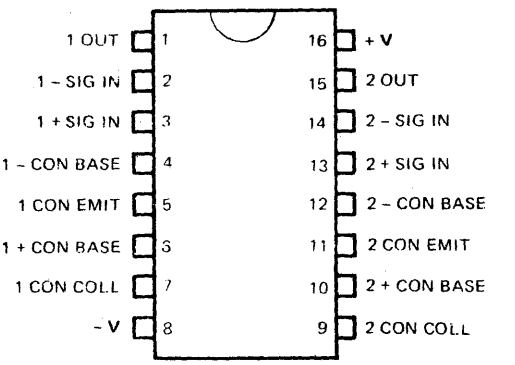
The SSM 2020 is a dual two quadrant multiplier designed to be used with op amps in a wide variety of precision audio-frequency applications including AGC circuits, Dividers and as a Biquad tuning element. Each channel has separate control and differential signal inputs and a current output. The device offers an exceptionally flexible control circuit for each channel which allows simultaneous linear and exponential voltage control of gain or either polarity of current control. Both channels are fully temperature compensated and have 84dB signal to noise ratios at less than 0.1% distortion.

FEATURES

- Max Supplies ±18V
- Dual Design (Independent Control Selection)
- 2% Channel Gain Matching
- 100dB Control Range
- Simultaneous Linear and Exponential Gain Control
- Differential Signal Inputs
- Current Output
- 84dB Signal to Noise
- 0.1% Distortion
- Fully Temperature Compensated

APPLICATIONS

- 2 and 4 Quadrant Multipliers
- Dividers
- AGC Circuits
- Voltage Controlled Filters
- Voltage Controlled Quadrature Oscillators
- Volume Controls
- Equalizers
- Compandors
- Antilog Amplifiers
- Voltage Controlled Current Sources



VOLTAGE CONTROLLED OSCILLATOR 2030

SSM2030 DESCRIPTION

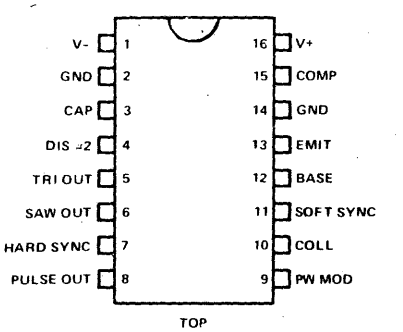
The SSM2030 is a precision voltage controlled oscillator designed specifically to meet the waveform and accuracy requirements of electronic music systems. It has both exponential and proportional linear sweep inputs which can control frequency over a 1,000,000 to 1 range with the same capacitor. Sweep accuracy is better than 0.25% over a 1,000 to 1 range and 0.1% over 100 to 1. The device has simultaneous sawtooth, triangle and pulse outputs. An internal comparator provides control of pulse output duty cycle from 0 to 100%. Hard and soft sync inputs make possible a rich variety of modulation and harmonic locking effects.

FEATURES

- Simultaneous Exponential and Proportional Linear Sweep Inputs
- High Sweep Accuracy (0.25% 1000 to 1)
- 1,000,000 to 1 Sweep Range
- 200 kHz Max Operating Frequency
- Simultaneous Sawtooth, Triangle and Pulse Outputs
- Pulse Duty Cycle Voltage Control Range (0 to 100%)
- All Outputs Short Circuit Protected
- Hard and Soft Sync Inputs
- Max Supplies ±18V

APPLICATIONS

- Music Synthesizers
- Electronic Organs
- Electronics Games
- Waveform Generation
- V to F and F to V Conversion
- Modulation Control Circuits
- Wide Range Phase-Locked Loops
- Frequency Multiplication and Division



Solid State Microtechnology For Music, 2076B Walsh Ave., Santa Clara, CA 95050, Phone (408)248-0917

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VOLTAGE CONTROLLED FILTER CIRCUIT 2040

DESCRIPTION

The SSM 2040 is a four section filter whose cutoff frequency can be exponentially voltage controlled over a 10,000 to 1 range. This flexible building-block can be used in virtually any active filter design including lowpass, highpass, bandpass and notch. Rolloff characteristics can be selected to be Butterworth, Bessel, Chevyshev, Cauer or any other filter type.

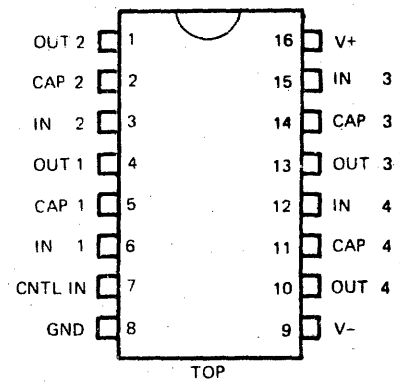
Applications include tracking filters, organs, music synthesizers, music phase shifters and sound effects generation.

FEATURES

- +/- 15V Supplies
- Exponential Frequency Control Response
- 4 Filter Sections in One Package
- Low Noise
- Low Distortion
- Guaranteed Control Rejection Characteristics 10,000:1 range

APPLICATIONS

- Voltage Controlled Filters:
  - Lowpass
  - Bandpass
  - Highpass
  - Allpass
  - Notch
  - Biquad
  - State Variable
  - Sallen & Key
  - Cauer
- Parametric Equalizers
- Music Synthesizers
- Music Phase Shifters
- Tracking Filters
- Low Distortion Sine VCO's



VOLTAGE CONTROLLED TRANSIENT GENERATOR 2050

DESCRIPTION:

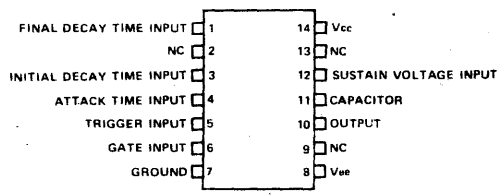
The SSM 2050 is a self-contained ADSR type electronic music transient generator. Attack, initial decay and final decay timers can be exponentially voltage controlled over a 10,000 to 1 range from 1 msec to more than 10 sec. The sustain level is linearly voltage controllable from 0 to 100%. The device has independant gate and trigger inputs for maximum flexibility and much effort has been taken to minimize the external parts count.

FEATURES:

- +/- 15V Supplies
- Exponential Time Control Response
- Minimum External Component Count
- Guaranteed Control Rejection Characteristics
- 10,000:1 Time Control Range
- Full ADSR Response
- Independent Gate & Trigger

APPLICATIONS

- Music Synthesizers
- Organs
- Rhythm Synthesizers
- Sound Effects Generators
- Electronic Games



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INTRODUCTION TO INTERFACE

INTERFACE.....

The Master Selection Guide provides sufficient information to make initial product selections. It enables you to find the products which are most appropriate to fulfill your major requirements and then provides data for many of the more important products.

All devices that appear in this section, both in the initial selection guide and in the data pages, are included in all other indexes. These index listings lead to the page and the line on that page where each device appears.

In the Interface Section the selection parameters differ drastically for each category; therefore, each has its own format. The analog to digital converter category has two formats: one for binary output devices and another for decimal units. Some of the products in this section, primarily analog to digital and digital to analog converters, are hybrids; the ones listed are those packaged to be compatible with IC's.

This section is not complicated by reference to package styles; the package style suffixes are usually deleted. For more information on each companies' suffixes, see the Part Number Guide. Throughout the Master Selection Guide, each full military temperature range (−55°C to 125°C) device is indicated by a dagger (†) before the manufacturer's name. Manufacturers' names are normally spelled out; however, a few are abbreviated and the abbreviations are explained on page 306.

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The manufacturers listed above are providing detailed information on their latest and most significant products.

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INTERFACE–Analog Switches

Switches with Drivers

Function	Switch Type	ON Resistance 25°C,Ω	Analog Signal Range, V	Supply Voltage	Device	Source	Line
SPST	CMOS	75	±11	±15,5	**HI5040-2**	**† Harris (696)**	
					HI5040-5	**Harris (696)**	
					IH5040M	† Intersil	
		80	±10	±15,5	IH5040C	Intersil	
	JFET	6	-5 to 4	±15,5	CAG10A	† Teledyne C	
			-5 to 10	±15	CAG6	† Teledyne C	
		10	-5 to 4	±15,5	CAG10C	† Teledyne C	
			-5 to 10	±15	CAG6-10	† Teledyne C	
		15	-10 to 5	±15,5	CAG10D	† Teledyne C	
		30	±5	±5,5	CAG10	† Teledyne C	10
			±8	-18,12	IH5001	Intersil	
		50	±8	-18,12	IH5002	Intersil	
			-10 to 4	±15,5	CAG10B	† Teledyne C	
			-10 to 5	-15,5	CAG14	† Teledyne C	
			±10	±15	2110BE	† Teledyne C	
		60	±10	±18,5	CAG30	† Teledyne C	
		100	±5	±15	2107BE	† Teledyne C	
	PMOS	80-300	±10	-20,10	TL610I	TI	
					TL610M	† TI	
		100-400	±10	-20,10	TL610C	TI	20
2xSPST	CMOS	35	±10	±15,5	IH5048M	† Intersil	
		45	±10	±15,5	IH5048C	Intersil	
		50	±15	±15,5	**HI5048-2**	**† Harris (696)**	
					HI5048-5	**Harris (696)**	
				±15	**DG300A**	**† Siliconix (819)**	
					DG300B	**Siliconix (819)**	
					DG300C	**Siliconix (819)**	
					DG304A	**† Siliconix (819)**	
					DG304B	**Siliconix (819)**	
					DG304C	**Siliconix (819)**	30
					DG381A	**† Siliconix (825)**	
					DG381B	**† Siliconix (825)**	
					DG381C	**† Siliconix (825)**	
		70	±15	±15	AD7513S	† AD	
					AD7513T	† AD	
					HI200-2	**† Harris (692)**	
					MP7513S	Micro Power	
					DG200A	† Siliconix	
		75	±11	±15,5	IH200M	† Intersil	
					IH5041M	† Intersil	40
			±15	±15,5	**HI5041-2**	**† Harris (696)**	
					HI5041-5	**Harris (696)**	
		80	±10	±15,5	IH5041C	Intersil	
					IH200C	Intersil	
			±15	±15	AD7513J	AD	
					AD7513K	AD	
					HI200-5	**Harris (692)**	
					MP7513J	Micro Power	
					MP7513K	Micro Power	
					DG200B	Siliconix	
					DG200C	Siliconix	50
	JFET	6	-6 to 10	-18,15	CAG27	† Teledyne C	
		10	-6 to 10	-18,15	CAG27-10	† Teledyne C	
			-7.5 to 15	±15,5	DG180A	† Intersil	
					DG180B	Intersil	
					DG180A	† Siliconix	
					DG180B	Siliconix	

(Continued)

Switches with Drivers (Cont'd.)

Function	Switch Type	ON Resistance 25°C,Ω	Analog Signal Range, V	Supply Voltage	Device	Source	Line
2xSPST	JFET	10				(Cont'd.)	
			±10	-18,12	DG141A	† Intersil	
					IH5005	† Intersil	60
					AH0141	**† National (1076)**	
					AH0141C	**National (1076)**	
					DG141A	† Siliconix	
				-20,10,5	DG180A	† Intersil	
					DG180B	Intersil	
					DG180A	† Siliconix	
					DG180B	Siliconix	
		15	±7.5	±15	DG151A	† Intersil	
					AH0151	**† National (1076)**	
					AH0151C	**National (1076)**	70
					DG151A	† Siliconix	
			±8	-18,12	DG141B	Intersil	
					DG441A	Intersil	
					DG141B	Siliconix	
		20	±5.5	±15	DG151B	Intersil	
					DG451A	Intersil	
					DG151B	Siliconix	
		30	-6 to 10	-18,15	CAG24	† Teledyne C	
			-7.5 to 15	±15,5	DG181A	† Intersil	
					IH181M	† Intersil	80
					AM181	**† National (1076)**	
					DG181A	† Siliconix	
			±10	-18,12	DG133A	† Intersil	
					IH5003	† Intersil	
					IH5006	† Intersil	
					AH0133	**† National (1076)**	
					AH0133C	**National (1076)**	
					DG133A	† Siliconix	
			-12.5 to 10	-20,10,5	DG181A	† Intersil	
					IH181M	† Intersil	90
					AM181	**† National (1076)**	
					DG181A	† Siliconix	
			for D/A				
			±10	-20	CDA2-3	† Teledyne C	
		35	±8	-18,12	DG433A	† Intersil	
		50	±7.5	±15	DG152A	† Intersil	
					AH0152	**† National (1076)**	
					AH0152C	**National (1076)**	
					DG152A	† Siliconix	
			-7.5 to 15	±15,5	DG181B	Intersil	100
					IH181C	Intersil	
					DG181B	Siliconix	
			±8	-18,12	DG133B	Intersil	
					DG133B	Siliconix	
			±10	-18,15	CAG13	† Teledyne C	
					CAG42	† Teledyne C	
					CAG45A	† Teledyne C	
				-18,12	IH5004	Intersil	
			-10 to 15	±15,5	AM281	National	
			-12.5 to 10	-20,10,5	DG181B	Intersil	110
					IH181C	Intersil	
					DG181B	Siliconix	
			-15 to 10	-20,10,5	AM281	National	
		75	-7.5 to 15	±15,5	**AM182**	**† National (1076)**	
			-15 to 10	-20,10,5	AM281	National	
			±10	±15	TL182M	† TI	

(Continued)

DT[1] means four terminals with a pair of normally open and normally closed contacts.

INTERFACE–Analog Switches (Cont'd)

Function	Switch Type	ON Resistance 25°C,Ω	Analog Signal Range, V	Supply Voltage	Device	Source	Line
Switches with Drivers						**(Cont'd.)**	
2xSPST	JFET	75				(Cont'd.)	
			-10 to 15	±15,5	DG182A	† Intersil	
					IH182M	† Intersil	
					DG182A	† Siliconix	
			-12.5 to 10	-20,10,5	**AM182**	**† National** **(1076)**	
			-15 to 10	-20,10,5	DG182A	† Intersil	
					IH182M	† Intersil	
					DG182A	† Siliconix	
		80	±8	-18,12	DG434A	Intersil	
			±10	-18,12	DG134A	† Intersil	10
					IH5007	Intersil	
					AH0134	**† National** **(1076)**	
					AH0134C	**National** **(1076)**	
					DG134A	† Siliconix	
		100	±5.5	±15	DG452	Intersil	
					DG152B	Siliconix	
			±8	-18,12	DG134B	Intersil	
					DG134B	Siliconix	
			±10	±15,5	TL182I	TI	
					TL182C	TI	20
			-10 to 15	±15,5	DG182B	Intersil	
					IH182C	Intersil	
					AM282	National	
					DG182B	Siliconix	
			-15 to 10	-20,10,5	DG182B	Intersil	
					IH182C	Intersil	
					AM282	National	
					DG182B	Siliconix	
	PMOS	75-200	-5 to 10	±15,5	DGM111A	† Siliconix	
			±10	-20,10,5	DGM111A	† Siliconix	30
		75-250	-5 to 10	±15	DGM111B	Siliconix	
			±10	-20,10,5	DGM111B	Siliconix	
		100-450	±10	-20,10,5	DG111	† Intersil	
					DG112	† Intersil	
4xSPST	CMOS	75	±11	±15,5	IH201M	† Intersil	
					IH202M	† Intersil	
					IH5052M	† Intersil	
					IH5053M	† Intersil	
		80	±10	±15,5	IH201C	Intersil	
					IH202C	Intersil	40
					IH5052C	Intersil	
					IH5053C	Intersil	
			±15	±15	**HI201-2**	**† Harris** **(694)**	
		100	±15	±15	AD7510DIJ	AD	
					AD7510DIK	AD	
					AD7510DIS	† AD	
					AD7511DIJ	AD	
					AD7511DIK	AD	
					AD7511DIS	† AD	
					AD7511DIT	† AD	50
					HI201-5	**Harris** **(694)**	
					MP7510DIJ	Micro Power	
					MP7510DIK	Micro Power	
					MP7510DIS	† Micro Power	
					MP7511DIJ	Micro Power	
					MP7511DIK	Micro Power	
					MP7511DIS	† Micro Power	
					MP7511DIT	† Micro Power	
		175	±15	±15	DG201A	† Siliconix	
						(Continued)	

Function	Switch Type	ON Resistance 25°C,Ω	Analog Signal Range, V	Supply Voltage	Device	Source	Line
Switches with Drivers						**(Cont'd.)**	
4xSPST	CMOS					(Cont'd.)	60
		200	±7.5	±7.5	SCL4066S	SSS	
			±15	±15	DG201B	Siliconix	
					DG201C	Siliconix	
		280	±7.5	±7.5	AD7516K	AD	
					AD7516T	† AD	
					F4066BC	Fairchild	
					F4066BM	† Fairchild	
					HD14066B	Hitachi	
					MP7516K	Micro Power	
					MP7516T	† Micro Power	70
					SIL4066B	† Mitel	
					SIL4066BE	Mitel	
					MC14066BA	† Motorola	
					MC14066BC	Motorola	
					CD4066BC	**National** **(1076)**	
					CD4066BM	**† National** **(1076)**	
					µPD4066	NEC America	
					MSM4066	OKI	
					CD4066B	† RCA	
					CD4066BE	RCA	80
					HBF4066AE	SGS	
					N4066A	Signetics	
					SCL4066B	† SSS	
					SCL4066BE	SSS	
					TC4066B	Toshiba	
		400	±7.5	±7.5	AD7516J	AD	
					AD7516S	† AD	
					HD14016B	Hitachi	
					MP7516J	Micro Power	
					MP7516S	† Micro Power	90
					SIL4016B	† Mitel	
					SIL4016BE	Mitel	
					MC14016BA	† Motorola	
					MC14016BC	Motorola	
					SCL4016B	† SSS	
					SCL4016BE	SSS	
					CM4016A	† Solitron	
					CM4016AE	Solitron	
					TP4016A/B	† TI	
					TP4316A	† TI	100
					TC4016	Toshiba	
		700	±7.5	±7.5	MSM4016	OKI	
		800	±7.5	±7.5	F4016C	Fairchild	
					F4016M	† Fairchild	
		850	±7.5	±7.5	**CD4016BC**	**National** **(1076)**	
					CD4016BM	**† National** **(1076)**	
					CD4016B	† RCA	
					CD4016BE	RCA	
					CM4016A	† Solitron	
					CM4016AE	Solitron	110
					CM4116A	† Solitron	
					CM4116AE	Solitron	
			Inverted control				
			±7.5	±7.5	SCL4416B	† SSS	
					SCL4416BE	SSS	
	JFET	10	±10	-18,2.8	CAM604A	† Teledyne C	
		30	±7.5	±15,5	**AM193**	**National** **(1076)**	
		50	-10 to 5	-15,5	CAG49	† Teledyne C	
		60	±10	-18,5	CAG49	† Teledyne C	
				±18,-7	CAG50	† Teledyne C	120
		75	±10	±15	SSS7510A	† PMI	
						(Continued)	

† Military Temperature Range (−55° to 125°C)

* Typical Values

Bold face indicates additional data is provided on the page noted.

INTERFACE–Analog Switches (Cont'd)

Switches with Drivers (Cont'd.)

Function	Switch Type	ON Resistance 25°C,Ω	Analog Signal Range, V	Supply Voltage	Device	Source	Line
4xSPST	JFET	75	±10	±15		(Cont'd.)	
					SSS7510B	† PMI	
					SSS7510E	PMI	
					SSS7510F	PMI	
					SSS7511A	† PMI	
					SSS7511B	† PMI	
					SSS7511E	PMI	
					SSS7511F	PMI	
				±15,5	**AM194**	**National (1076)**	
4xSPST Various Combinations of normally on/off							10
	JFET	100	±10	-18,15	CAG48A	† Teledyne C	
		200	±10	±15,0	**LF11201**	**† National (1035)**	
					LF11202	**† National (1035)**	
					LF11331	**† National (1035)**	
					LF11332	**† National (1035)**	
					LF11333	**† National (1035)**	
		250	±10	±15,0	**LF12201**	**National (1035)**	
					LF13201	**National (1035,1073)**	
					LF12202	**National (1035)**	20
					LF13202	**National (1035,1076)**	
					LF12331	**National (1035)**	
					LF13331	**National (1035)**	
					LF12332	**National (1035)**	
					LF13332	**National (1035)**	
					LF12333	**National (1035)**	
					LF13333	**National (1035,1073)**	
	PMOS	200-600	±10	-20,10,5	**AH0015**	**† National (1076)**	30
					AH0015C	**National (1076)**	
4xSPST Common Output							
	PMOS	100-450	±10	-20,10	DG116	† Intersil	
				-20,10,5	DG118	† Intersil	
		150-450	±10	-20,10,5	DG172A	† Siliconix	
		150-500	±10	-20,10,5	DG172B	Siliconix	
		200-600	±10	-20,10,5	DG172C	Siliconix	
5xSPST Common Output							
	PMOS	100-450	±10	-20,10	DG123	† Intersil	
					DG123A	† Siliconix	40
				-20,10,5	DG125	† Intersil	
					DG125A	† Siliconix	
		125-500	±10	-20,10	DG123B	Intersil	
					DG123B	Siliconix	
				-20,10,5	DG125B	Intersil	
					DG125B	Siliconix	
SPDT[1]	CMOS	35	±10	±15,5	IH5050M	† Intersil	
		45	±10	±15,5	IH5050C	Intersil	
		50	±15	±15,5	**HI5050-2**	**† Harris (696)**	
					HI5050-5	**Harris (696)**	50
				±15	**DG301A**	**† Siliconix (819)**	
					DG301B	**Siliconix (819)**	
					DG301C	**Siliconix (819)**	
					DG305A	**† Siliconix (819)**	
					DG305B	**Siliconix (819)**	
					DG305C	**Siliconix (819)**	
					DG387A	**† Siliconix (825)**	
					DG387B	**Siliconix (825)**	
					DG387C	**Siliconix (825)**	
		75	±11	±15,5	IH5042M	† Intersil	60

(Continued)

Switches with Drivers (Cont'd.)

Function	Switch Type	ON Resistance 25°C,Ω	Analog Signal Range, V	Supply Voltage	Device	Source	Line
SPDT[1]	CMOS	75				(Cont'd.)	
			±15	±15,5	**HI5042-2**	**† Harris (696)**	
					HI5042-5	**Harris (696)**	
		80	±10	±15,5	IH5042C	Intersil	
	JFET	6	-5 to 10	±15	CAG7	† Teledyne C	
		10	-5 to 10	±15	CAG7-10	† Teledyne C	
			-7.5 to 15	±15,5	DG186A	† Intersil	
					DG186B	Intersil	
					DG186A	† Siliconix	
					DG186B	Siliconix	70
			±10	-18,12	DG146A	† Intersil	
					AH0146	† National	
					AH0146C	National	
					DG146A	Siliconix	
			-12.5 to 10	-20,10,5	DG186A	† Intersil	
					DG186B	Intersil	
					DG186A	† Siliconix	
					DG186B	Siliconix	
		15	±7.5	±15	DG161A	† Intersil	
					AH0161	† National	80
					AH0161C	National	
					DG161A	Siliconix	
			±8	-18,12	DG146B	Intersil	
					DG446A	Intersil	
					DG146B	Siliconix	
		20	±5.5	±15	DG461A	Intersil	
					DG161B	Siliconix	
		30	-7.5 to 15	±15,5	DG187A	† Intersil	
					IH187M	† Intersil	
					AM187	† National	90
					DG187A	† Siliconix	
			±10	-18,12	DG144A	† Intersil	
					AH0144	† National	
					AH0144C	National	
					DG144A	† Siliconix	
			-12.5 to 10	-20,10,5	DG187A	† Intersil	
					IH187M	† Intersil	
					AM187	† National	
					DG187A	† Siliconix	
		35	±8	±8,12	DG444A	Intersil	100
		50	±7.5	±15	DG162A	† Intersil	
					AH0162	† National	
					AH0162C	National	
					DG162A	† Siliconix	
			-7.5 to 15	±15,5	DG187B	Intersil	
					IH187C	Intersil	
					DG187B	Siliconix	
			±8	-18,12	DG144B	Intersil	
					DG144B	Siliconix	
				±15	2126BG	† Teledyne C	110
			-10 to 15	±15,5	AM287	National	
			-12.5 to 10	-20,10,5	DG187B	Intersil	
					IH187C	Intersil	
					DG187B	Siliconix	
			-15 to 10	-20,10,5	AM287	National	
		75	-7.5 to 15	±15,5	AM188	† National	
			±10	±15,5	TL188M	† TI	
			-10 to 15	±15,5	DG188A	† Intersil	

(Continued)

DT[1] means four terminals with a pair of normally open and normally closed contacts.

INTERFACE–Analog Switches (Cont'd)

Switches with Drivers (Cont'd.)

Function	Switch Type	ON Resistance 25°C,Ω	Analog Signal Range, V	Supply Voltage	Device	Source	Line
						(Cont'd.)	
SPDT[1]	JFET	75	-10 to 15	±15,5	IH188M	† Intersil	
					DG188A	† Siliconix	
			-12.5 to 10	-20,10,5	AM188	† National	
			-15 to 10	-20,10,5	DG188A	† Intersil	
					IH188M	† Intersil	
					DG188A	† Siliconix	
		80	±8	-18,12	DG443A	Intersil	
			±10	-18,12	DG143	† Intersil	
					AH0143	† National	10
					AH0143C	National	
					DG143A	† Siliconix	
		100	±5.5	±15	DG162B	Siliconix	
			±8	±15	DG462A	Intersil	
			±10	±15,5	TL188I	TI	
					TL188C	TI	
				±15	AH2114	† National	
				-18,12	DG143B	Siliconix	
			-10 to 15	±15,5	DG188B	Intersil	
					IH188C	Intersil	20
					AM288	National	
					DG188B	Siliconix	
			-15 to 10	-20,10,5	DG188B	Intersil	
					IH188C	Intersil	
					AM288	National	
					DG188B	Siliconix	
		125	±10	±15	AH2114C	National	
	NPN-PNP						
		10	±10	-15,5	CDA23	† Teledyne C	
SPDT	JFET	50	-10 to 5	-15,5	CDA18	† Teledyne C	30
SPDT for D/A							
	NPN-PNP						
		10	10	10	CDA4A	† Teledyne C	
			0 to -10	-15	CDA1-3	† Teledyne C	
			±10	-15,5	CDA23	† Teledyne C	
				±15	CDA6	† Teledyne C	
SPDT[1]	PMOS	75-200	-5 to 15	±15	DG175A	† Siliconix	
			±10	-20,10,5	DG175A	† Siliconix	
		75-250	-5 to 15	±15	DG175B	Siliconix	
			±10	-20,10,5	DG175B	Siliconix	40
		100-400	±10	-20,10	TL604I	TI	
					TL604M	† TI	
		200-600	±10	-20,10	TL604C	TI	
SPDT	PMOS	100-400	±10	-20,10	SI3002A	† Siliconix	
					SI3002B	Siliconix	
					TL601I	TI	
					TL601M	† TI	
					TL607I	TI	
					TL607M	† TI	
		200-600	±10	-20,10	TL601C	TI	50
					TL607C	TI	
		200*	±10	-20,10	SH3002C	Fairchild	
					SH3002M	† Fairchild	
2xSPDT[1]	CMOS	35	±10	±15,5	IH5051M	† Intersil	
		45	±10	±15,5	IH5051C	Intersil	
						(Continued)	

Switches with Drivers (Cont'd.)

Function	Switch Type	ON Resistance 25°C,Ω	Analog Signal Range, V	Supply Voltage	Device	Source	Line
						(Cont'd.)	
2xSPDT[1]	CMOS	50	±15	±15,5	**HI5051-2**	**† Harris (696)**	
					HI5051-5	**Harris (696)**	
				±15	**DG303A**	**† Siliconix (819)**	
					DG303B	**Siliconix (819)**	60
					DG303C	**Siliconix (819)**	
					DG307A	**† Siliconix (819)**	
					DG307B	**Siliconix (819)**	
					DG307C	**Siliconix (819)**	
					DG390A	**† Siliconix (825)**	
					DG390B	**Siliconix (825)**	
					DG390C	**Siliconix (825)**	
		75	±11	±15,5	IH5043M	† Intersil	
			±15	±15,5	**HI5043-2**	**† Harris (696)**	
					HI5043-5	**Harris (696)**	70
		80	±10	±15,5	IH5043C	Intersil	
2xSPDT	CMOS	100	±15	±15	AD7512DIJ	AD	
					AD7512DIK	AD	
					AD7512DIS	† AD	
					AD7512DIT	† AD	
					MP7512DIJ	Micro Power	
					MP7512DIK	Micro Power	
					MP7512DIS	† Micro Power	
	PNP	10	±10	±15	CDA29A	† Teledyne C	
2xSPDT[1]	DMOS	50	±10	±15,5	SD5600	Signetics	80
	JFET	10	-7.5 to 15	±15,5	DG189A	† Intersil	
					DG189B	Intersil	
					DG189A	† Siliconix	
					DG189B	Siliconix	
			-12.5 to 15	-20,15,5	DG189A	† Intersil	
					DG189B	Intersil	
					DG189A	† Siliconix	
					DG189B	Siliconix	
		30	-7.5 to 15	±15,5	DG190A	† Intersil	
					IH190M	† Intersil	90
					AM190	† National	
					DG190A	† Siliconix	
			-12 to 15	-20,15,5	DG190A	† Intersil	
					IH190M	† Intersil	
					AM190	† National	
					DG190A	† Siliconix	
		50	-7.5 to 15	±15,5	DG190B	Siliconix	
			-10 to 15	±15,5	AM290	National	
			-12.5 to 15	-20,10,5	DG190B	Siliconix	
			-15 to 10	-20,10,5	AM290	National	100
		75	-7.5 to 15	±15,5	AM191	† National	
			-10 to 15	±15,5	DG191A	† Intersil	
					IH191M	† Intersil	
					DG191A	† Siliconix	
			-12.5 to 15	-20,10,5	AM191	† National	
			-15 to 10	-20,10,5	DG191A	† Intersil	
					IH191M	† Intersil	
					DG191A	† Siliconix	
		100	-10 to 15	±15,5	DG191B	Intersil	
					IH191C	Intersil	110
					AM291	National	
					DG191B	Siliconix	
			-15 to 10	-20,10,5	DG191B	Intersil	
					IH191C	Intersil	
						(Continued)	

† Military Temperature Range (−55° to 125°C)

* Typical Values

Bold face indicates additional data is provided on the page noted.

INTERFACE–Analog Switches (Cont'd)

Switches with Drivers (Cont'd.)

Function	Switch Type	ON Resistance 25°C,Ω	Analog Signal Range, V	Supply Voltage	Device	Source	Line
					(Cont'd.)		
2xSPDT[1]	JFET	100	-15 to 10	-20,10,5	AM291	National	
					DG191B	Siliconix	
		125	±10	±15,5	TL191M	† TI	
		150	±10	±15,5	TL191I	TI	
					TL191C	TI	
3xSPDT	CMOS	280	±7.5	±7.5	F4053BC	Fairchild	
					F4053BM	† Fairchild	
					HD14053B	Hitachi	
					SIL4053B	† Mitel	10
					SIL4053BE	Mitel	
					MC14053BA	† Motorola	
					MC14053BC	Motorola	
					CD4053BC	National	
					CD4053BM	† National	
					µPD4053	NEC America	
					MSM4053	OKI	
					CD4053B	† RCA	
					CD4053BE	RCA	
					SCL4053B	† SSS	20
					SCL4053BE	SSS	
					CM4053A	† Solitron	
					CM4053AE	Solitron	
					TP4053A/B	TI	
					TC4053	Toshiba	
	PMOS	200-800	±10	-20,10,5	DG170A	† Siliconix	
		250-850	±10	-20,10,5	DG170B	Siliconix	
					DG170C	Siliconix	
4xSPDT for D/A							
	CMOS	100	0.1	8	AD7519J	AD	30
					MP7519J	Micro Power	
4XSPDT	CMOS	—	—	8	MC14551BA	† Motorola	
					MC14551BC	Motorola	
4xSPDT	JFET	35	±10	-15,5	HCS310	HyComp	
	NMOS	—	—	8	DG515A	† Siliconix	
					DG515B	Siliconix	
					DG515C	Siliconix	
4xSPDT for D/A (current switch)							
	NPN	—	-10 to -3	±15	ULN-2140	Sprague	
					ULN-2141	Sprague	40
					ULN-2142	Sprague	
					ULS-2140	† Sprague	
					ULS-2141	† Sprague	
					ULS-2142	† Sprague	
			-2 to 10	15,-5	AD550J	AD	
					AD550K	AD	
					AD550L	AD	
					AD550S	† AD	
					AD550T	† AD	
					AD550U	† AD	50
					AD553J	AD	
					AD553K	AD	
					AD553L	AD	
					AD553S	† AD	
					AD553T	† AD	
					AD553U	† AD	
4xSPDT for D/A (voltage switch)							
	NPN	25	±3	15,-4	AD555L	AD	
					AD555U	† AD	
		40	±3	15,-4	AD555K	AD	60
					AD555J	AD	
		100	±3	15,-4	AD555J	AD	

(Continued)

Switches with Drivers (Cont'd.)

Function	Switch Type	ON Resistance 25°C,Ω	Analog Signal Range, V	Supply Voltage	Device	Source	Line
					(Cont'd.)		
4xSPDT for D/A (voltage switch)							
	NPN	100	±3	15,-4	AD555S	† AD	
4xSPDT	PNP	7	0 to -10	-15	CDA11-S12	Teledyne C	
		10	0 to -10	-15	CDA11	Teledyne C	
10xSPDT for D/A							
	NMOS	—	—	8	DG516A	† Siliconix	
					DG516B	Siliconix	70
					DG516C	Siliconix	
DPST	CMOS	75	±11	±15,5	IH5044M	† Intersil	
			±15	±15,5	**HI5044-2**	**† Harris**	**(696)**
					HI5044-5	**Harris**	**(696)**
		80	10	±15,5	IH5044	Intersil	
	PMOS	200	±10	±12	SH3003C	Fairchild	
					SH3003M	† Fairchild	
2xDPST	CMOS	35	±10	±15,5	IH5049M	† Intersil	
		45	±10	±15,5	IH5049C	Intersil	
		50	±15	±15,5	**HI5049-2**	**† Harris**	**(696)** 80
					HI5049-5	**Harris**	**(696)**
				±15	**DG302A**	**† Siliconix**	**(819)**
					DG302B	**Siliconix**	**(819)**
					DG302C	**Siliconix**	**(819)**
					DG306A	**† Siliconix**	**(819)**
					DG306B	**Siliconix**	**(819)**
					DG306C	**Siliconix**	**(819)**
					DG384A	**† Siliconix**	**(825)**
					DG384B	**Siliconix**	**(825)**
					DG384C	**Siliconix**	**(825)** 90
		75	±11	±15,5	IH5045M	† Intersil	
			±15	±15,5	**HI5045-2**	**† Harris**	**(696)**
					HI5045-5	**Harris**	**(696)**
		80	±10	±15,5	IH5045C	Intersil	
2xDPST Three Control Input							
	CMOS	200	±15	±15,5	HI1800A-5	Harris	
2xDPST	JFET	10	-7.5 to 15	±15,5	DG183A	† Intersil	
					DG183B	Intersil	
					DG183A	† Siliconix	
					DG183B	Siliconix	100
			±10	-18,12	DG140A	† Intersil	
					AH0140	† National	
					AH0140C	National	
					DG140A	† Siliconix	
			-12.5 to 10	-20,10,5	DG183A	† Intersil	
					DG183B	Intersil	
					DG183A	† Siliconix	
					DG183B	† Siliconix	
		15	±7.5	±15	DG153A	† Intersil	
					AH0153	† National	110
					AH0153C	National	
					DG153A	† Siliconix	
			±8	-18,12	DG440A	Intersil	
					DG140B	Siliconix	
		20	±5.5	±15	DG153B	Intersil	
					DG453A	Intersil	
					DG153B	Siliconix	
		30	-7.5 to 15	±15,5	DG184A	† Intersil	
					IH184M	† Intersil	
					AM184	† National	120

(Continued)

DT[1] means four terminals with a pair of normally open and normally closed contacts.

INTERFACE–Analog Switches (Cont'd)

Function	Switch Type	ON Resistance 25°C,Ω	Analog Signal Range, V	Supply Voltage	Device	Source	Line
Switches with Drivers						**(Cont'd.)**	
2xDPST	JFET	30	-7.5 to 15	±15,5		(Cont'd.)	
					DG184A	† Siliconix	
			±10	-18,12	DG129A	† Intersil	
					AH0129	† National	
					AH0129C	National	
					DG129A	† Siliconix	
			-12.5 to 10	-20,10,5	DG184A	† Intersil	
					IH184M	† Intersil	
					AM184	† National	
					DG184A	† Siliconix	10
		35	±8	-18,12	DG429A	Intersil	
		50	±7.5	±15	DG154A	† Intersil	
					AH0154	† National	
					AH0154C	National	
					DG154A	† Siliconix	
			-7.5 to 15	±15,5	DG184B	Intersil	
					IH184C	Intersil	
					DG184B	Siliconix	
			±8	-18,12	DG129B	Siliconix	
			-10 to 15	±15,5	AM284	National	20
			-12.5 to 15	-20,10,5	DG184B	Intersil	
					IH184C	Intersil	
					DG184B	Siliconix	
			-15 to 10	-20,10,5	AM284	National	
		60	±10	-18,15	CS4R101A	† Teledyne C	
		75	-7.5 to 15	±15,5	AM185	† National	
			-10 to 15	±15,5	DG185A	† Intersil	
					IH185M	† Intersil	
					DG185A	† Siliconix	
			-12.5 to 10	-20,10,5	AM185	† National	30
			-15 to 10	-20,10,5	DG185A	Intersil	
					IH185M	† Intersil	
					DG185A	† Siliconix	
		80	±8	-18,12	DG426A	Intersil	
			±10	-18,12	DG126A	† Intersil	
					AH0126	† National	
					AH0126C	National	
					DG126A	† Siliconix	
		100	±5.5	±15	DG154B	Intersil	
					DG454A	Intersil	40
					DG154B	Siliconix	
			±8	-18,12	DG126B	Siliconix	
			-10 to 15	±15,5	DG185B	Intersil	
					IH185C	Intersil	
					AM285	National	
					DG185B	Siliconix	
			-15 to 10	-20,10,5	DG185B	Intersil	
					IH185C	Intersil	
					AM285	National	
					DG185B	Siliconix	50
		125	±10	±15,5	TL185M	† TI	
		150	±10	±15,5	TL185I	TI	
					TL185C	TI	
2xDPST Common Output							
	PMOS	100-450	±10	-20,10,5	DGM122A	† Siliconix	
		125-500	±10	-20,10,5	DGM122B	Siliconix	
		200-600	±10	-20,10,5	AH0019	† National	
						(Continued)	

Function	Switch Type	ON Resistance 25°C,Ω	Analog Signal Range, V	Supply Voltage	Device	Source	Line
Switches with Drivers						**(Cont'd.)**	
2xDPST Common Output							
	PMOS	200-600	±10	-20,10,5		(Cont'd.)	
					AH0019C	National	60
3xDPST Common Output							
	PMOS	100-450	±10	-20,10	DG120	† Intersil	
				-20,10,5	DG121	† Intersil	
DPDT[1]	CMOS	50	±15	±15,5	**HI5046A-2**	**† Harris**	**(696)**
					HI5046A-5	**Harris**	**(696)**
		75	±11	±15,5	IH5046M	† Intersil	
			±15	±15,5	**HI5046-2**	**† Harris**	**(696)**
					HI5046-5	**Harris**	**(696)**
		80	±10	±15,5	IH5046C	Intersil	
	JFET	10	±10	-18,12	DG145A	† Intersil	70
					AH0145	† National	
					AH0145C	National	
					DG145A	† Siliconix	
		15	±7.5	±15	DG163A	† Intersil	
					AH0163	† National	
					AH0163C	National	
					DG163A	† Siliconix	
			±8	-18,12	DG445A	Intersil	
					DG145B	Siliconix	
		20	±5.5	±15	DG163B	Intersil	80
					DG463A	Intersil	
					DG163B	Siliconix	
		30	±10	-18,12	DG139A	† Intersil	
					AH0139	† National	
					AH0139C	National	
					DG139A	† Siliconix	
		35	±8	-18,12	DG439A	Intersil	
		50	±7.5	±15	DG164A	† Intersil	
					AH0164	† National	
					AH0164C	National	90
					DG164A	† Siliconix	
			±8	-18,12	DG139B	Siliconix	
		80	±8	-18,12	DG442A	Intersil	
			±10	-18,12	DG142A	† Intersil	
					AH0142	† National	
					AH0142C	National	
					DG142A	† Siliconix	
		100	±5.5	±15	DG164B	Intersil	
					DG464A	Intersil	
					DG164B	Siliconix	100
			±10	-18,12	DG142B	Siliconix	
2xDPDT	PMOS	150-1000	0 to -18	-(5-21)	TDA1195	Siemens	
2xDPDT with followers							
					TDA1028	Signetics	
DPDT	PMOS	150-450	±10	-20,10,5	DG173A	† Siliconix	
		150-500	±10	-20,10,5	DG173B	Siliconix	
		200-600	±10	-20,10,5	AH0014	† National	
					AH0014C	National	
DP4T with followers							
					TDA1029	Signetics	110
4PST	CMOS	50	±15	±15,5	**HI5047A-2**	**† Harris**	**(696)**
					HI5047A-5	**Harris**	**(696)**
		75	±11	±15,5	IH5047M	† Intersil	
						(Continued)	

† Military Temperature Range (−55° to 125°C)

* Typical Values

Bold face indicates additional data is provided on the page noted.

INTERFACE–Analog Switches (Cont'd)

Function	Switch Type	ON Resistance 25°C,Ω	Analog Signal Range, V	Supply Voltage	Device	Source	Line
Switches with Drivers							(Cont'd.)
4PST	CMOS	75					(Cont'd.)
			±15	±15,5	**HI5047-2**	**† Harris**	**(696)**
					HI5047-5	**Harris**	**(696)**
		80	±10	±15,5	IH5047C	Intersil	
8PST with shift register							
	DMOS	100	7	12	SD5350	Signetics	
4PDT for D/A							
	PNP	10	±10	±15,5	CDA28A	† Teledyne C	
Switches without Drivers							
SPST	JFET	30	±10		AM1000	† National	
		50	±15		AM1001	† National	10
		100	±0.2		IH5021C	Intersil	
					IH5021M	† Intersil	
					IH5023C	Intersil	
					IH5023M	† Intersil	
			0 to (Drive-4)		IH5037C	Intersil	
					IH5037M	† Intersil	
			±10		AM1002	† National	
		150	±0.2		IH5022C	Intersil	
					IH5022M	† Intersil	
					IH5024C	Intersil	20
					IH5024M	† Intersil	
			0 to (Drive-4)		IH5038C	Intersil	
					IH5038M	† Intersil	
2xSPST	JFET	100	±0.2		IH5017C	Intersil	
					IH5017M	† Intersil	
			0 to (Drive-4)		IH5033C	Intersil	
					IH5033M	† Intersil	
		150	±0.2		IH5020C	Intersil	
					IH5020M	† Intersil	
			0 to (Drive-4)		IH5036C	Intersil	30
					IH5036M	† Intersil	
2xSPST Common Output							
	JFET	100	±0.2		IH5019C	Intersil	
					IH5019M	† Intersil	
			0 to (Drive-4)		IH5035C	Intersil	
					IH5035M	† Intersil	
		150	±0.2		IH5018C	Intersil	
					IH5018M	† Intersil	
			0 to (Drive-4)		IH5034C	Intersil	
					IH5034M	† Intersil	40
3xSPST	JFET	100	±0.2		IH5015C	Intersil	
					IH5015M	† Intersil	
					AH5015C	**National**	**(1076)**
			0 to (Drive-4)		IH5031C	Intersil	
					IH5031M	† Intersil	
		150	±0.2		IH5016C	Intersil	
					IH5016M	† Intersil	
					AH5016C	**National**	**(1076)**
			0 to (Drive-4)		IH5032C	Intersil	
					IH5032M	† Intersil	50
3xSPST Common Output							
	JFET	100	±0.2		IH5013C	Intersil	
					IH5013M	† Intersil	
					AH5013C	National	
			0 to (Drive-4)		IH5029C	Intersil	
							(Continued)

Function	Switch Type	ON Resistance 25°C,Ω	Analog Signal Range, V	Supply Voltage	Device	Source	Line
Switches without Drivers							(Cont'd.)
3xSPST Common Output							
	JFET	100	0 to (Drive-4)				(Cont'd.)
					IH5029M	† Intersil	
		150	±0.2		IH5014C	Intersil	
					IH5014M	† Intersil	60
					AH5014C	National	
			0 to (Drive-4)		IH5030C	Intersil	
					IH5030M	† Intersil	
3xSPST	PMOS	200-600			MM455	† Intersil	
					MM555	Intersil	
					MM455	† National	
					MM555	National	
					Si455A	† Siliconix	
					Si555B	Siliconix	
4xSPST	DMOS	45	±5		SD5001	Signetics	70
			±10		SD5000	Signetics	
	JFET	100	±0.2		IH5011C	Intersil	
					IH5011M	† Intersil	
					AH5011C	**National**	**(1076)**
					AM97C11C	**National**	**(1076)**
					AM9711C	**National**	**(1076)**
			0 to (Drive-4)		IH5027C	Intersil	
					IH5027M	† Intersil	
		150	±0.2		IH5012C	Intersil	
					IH5012M	† Intersil	80
					AH5012C	**National**	**(1076)**
					AM97C12C	**National**	**(1076)**
					AM9712C	**National**	**(1076)**
			0 to (Drive-4)		IH5028C	Intersil	
					IH5028M	† Intersil	
		—			G125	† Intersil	
					G126	† Intersil	
					G127	† Intersil	
					G128	† Intersil	
					G129	Intersil	90
					G1330	Intersil	
					G1340	Intersil	
					G125A	† Siliconix	
					G125B	Siliconix	
					G126A	† Siliconix	
					G126B	Siliconix	
					G127A	† Siliconix	
					G127B	Siliconix	
					G128A	† Siliconix	
					G128B	Siliconix	100
4xSPST Common Output							
	DMOS	45	±5		SD5101	Signetics	
			±10		SD5100	Signetics	
	JFET	100	±0.2		IH5009C	Intersil	
					IH5009M	† Intersil	
					AH5009C	**National**	**(1073)**
					AM97C09	**National**	**(1073)**
					AM9709C	**National**	**(1073)**
			0 to (Drive-4)		IH5025C	Intersil	
					IH5025M	† Intersil	110
		150	±0.2		IH5010C	Intersil	
					IH5010M	† Intersil	
					AH5010C	National	
					AM97C10C	National	
					AM9710C	National	
							(Continued)

DT[1] means four terminals with a pair of normally open and normally closed contacts.

INTERFACE–Analog Switches (Cont'd)

Function	Switch Type	ON Resistance 25°C,Ω	Analog Signal Range, V	Supply Voltage	Device	Source	Line
Switches without Drivers							**(Cont'd.)**
4xSPST Common Output							
	JFET	150					(Cont'd.)
			0 to (Drive-4)		IH5026C	Intersil	
					IH5026M	† Intersil	
	—				G129	† Intersil	
					G130	† Intersil	
					G131	† Intersil	
					G132	† Intersil	
					G1350	Intersil	
					G1360	Intersil	10
					G129A	† Siliconix	
					G129B	Siliconix	
					G130A	† Siliconix	
					G130B	Siliconix	
					G131A	† Siliconix	
					G131B	Siliconix	
					G132A	† Siliconix	
					G132B	Siliconix	
4xSPST Two Outputs							
	JFET	—			G123	Intersil	20
	PMOS	—			G123A	† Siliconix	
					G123B	Siliconix	
4xSPST	NMOS	—			MEM780	GI	
					MEM781	GI	
	PMOS	200-600			MM452	† Intersil	
					MM552	Intersil	
					MM452	† National	
					MM552	National	
					Si452A	† Siliconix	
					Si552B	Siliconix	30
	—				MEM851	GI	
4xSPST Common Output							
	PMOS	—			G124	Intersil	
					MM451	† Intersil	
					MM551	Intersil	
					MM451	† National	
					MM551	National	
					G124A	† Siliconix	
					G124B	Siliconix	
4xSPST (current switch for D/A)							40
	—	—			LM11340	National	
					LM11341	National	
5xSPST Common Output							
	PMOS	—			G116A	† Intersil	
					G116B	Intersil	
					G116A	† Siliconix	
					G116B	Siliconix	
5xSPST Common Output plus output switch							
	PMOS	—			G117A	† Intersil	
					G117B	Intersil	50
					G117A	† Siliconix	
					G117B	Siliconix	
6xSPST Common Output							
	PMOS	—			MEM855	GI	
					MEM856	GI	
					G115	Intersil	
					G115A	† Intersil	
					G118A	† Intersil	
					G118B	Intersil	
					AM2009	† National	60
					AM2009C	National	
					MM5504	† National	
							(Continued)

Function	Switch Type	ON Resistance 25°C,Ω	Analog Signal Range, V	Supply Voltage	Device	Source	Line
Switches without Drivers							**(Cont'd.)**
6xSPST Common Output							
	PMOS	—					(Cont'd.)
					MM4504	National	
					G115A	† Siliconix	
					G115B	Siliconix	
					G118A	† Siliconix	
					G118B	Siliconix	
8xSPST Two Outputs							70
	PMOS	—			MEM857	GI	
10xSPST Three Outputs							
	NMOS	—			NMX5010	SMC	
	PMOS	—			MEM853	GI	
2xDPST Common Output							
	PMOS	—			G122A	† Siliconix	
					G122B	Siliconix	
					MM450	† Intersil	
					MM550	Intersil	
					MM450	† National	80
					MM550	National	
3xDPST Common Output							
	PMOS	—			G119C	Intersil	
					G119M	† Intersil	
					G119A	† Siliconix	
					G119B	Siliconix	
Multiplexers							
4 channel. See Switches 4xSPST							
4 channel differential							
	CMOS	270	±7.5	±7.5	MC14529BA	† Motorola	
		250	±15	±15	**MVD-409**	**Datel**	**(683)** 90
					MVD-409M	† Datel	
		270	±7.5	±7.5	MC14529BC	Motorola	
					CD4529BC	National	
					CD4529BM	† National	
		280	±7.5	±7.5	F4052BC	Fairchild	
					F4052BM	† Fairchild	
					HD14052B	Hitachi	
					SIL4052B	† Mitel	
					SIL4052BE	Mitel	
					MC14052BA	† Motorola	100
					MC14052BC	Motorola	
					CD4052BC	National	
					CD4052BM	† National	
					µPD4052	NEC America	
					MSM4052	OKI	
					CD4052B	† RCA	
					CD4052BE	RCA	
					SCL4052B	† SSS	
					SCL4052BE	SSS	
					CM4052B	† Solitron	110
					CM4052BE	Solitron	
					TP4052A/B	TI	
					TC4052B	Toshiba	
		300	±15	±15	AD7502J	AD	
					AD7502K	AD	
					AD7502S	† AD	
					MP7502J	Micro Power	
					MP7502K	Micro Power	
					MP7502S	† Micro Power	
		400	±15	±15	**HI1828A-2**	**† Harris**	**(699)** 120
					HI1828A-5	**Harris**	**(699)**
					DG509A	† Siliconix	
							(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Values

Bold face indicates additional data is provided on the page noted.

INTERFACE–Analog Switches (Cont'd)

Multiplexers (Cont'd.)

Function	Switch Type	ON Resistance 25°C,Ω	Analog Signal Range, V	Supply Voltage	Device	Source	Line
4 channel differential						(Cont'd.)	
	CMOS	450	±15	±15	DG509B	Siliconix	
					DG509C	Siliconix	
		1300	±15	±15	**MPC4D**	**Burr-Brown (659)**	
		1500	±15	±15	**HI509A-2**	**† Harris (709)**	
					MXD-409	**Datel (683)**	
					MXD-409M	**† Datel (683)**	
		1800	±15	±15	**HI509A-5**	**Harris (709)**	
	JFET	260	-15 to 11.5	±15	MUX-24A	† PMI	10
					MUX-24E	PMI	
		300	±10	±15,5	LF11306	† National	
					LF12306	National	
					LF13306	National	
		350*	-15 to 12	±15	**LF11509**	**† National (1035,1081)**	
					LF12509	**National (1035,1081)**	
					LF13509	**National (1035,1073,1081)**	20
		370	-15 to 12	±15	MUX-24B	† PMI	
					MUX-24F	PMI	
4 channel Sequential Commutator							
	PMOS	200-600	±10	-24,12	MM454	† National	
					MM554	National	
6 channel							
	JFET	60	±10	-18,2.8	CAM601A	† Teledyne C	
8 channel							
	CMOS	150	±8	±8	MS504	RTC	
		250	±15	±15	**MV-808**	**Datel (683)**	30
					MV-808M	† Datel	
		270	±7.5	±7.5	MC14529BA	† Motorola	
					MC14529BC	Motorola	
					CD4529BC	National	
					CD4529BM	† National	
		280	±7.5	±7.5	F4051BC	Fairchild	
					F4051BM	† Fairchild	
					HD14051B	Hitachi	
					SIL4051B	† Mitel	
					SIL4051BE	Mitel	40
					MC14051BA	† Motorola	
					MC14051BC	Motorola	
					CD4051BC	National	
					CD4051BM	† National	
					µPD4051	NEC America	
					MSM4051	OKI	
					CD4051B	† RCA	
					CD4051BE	RCA	
					SCL4051B	† SSS	
					SCL4051BE	SSS	50
					CM4051A	† Solitron	
					CM4051AE	Solitron	
					TP4051A/B	TI	
					TC4051B	Toshiba	
		300	±15	±15	AD7501J	AD	
					AD7501K	AD	
					AD7501S	† AD	
					AD7503J	AD	
					AD7503K	AD	
					AD7503S	† AD	60
					MP7501J	Micro Power	

(Continued)

Multiplexers (Cont'd.)

Function	Switch Type	ON Resistance 25°C,Ω	Analog Signal Range, V	Supply Voltage	Device	Source	Line
8 channel						(Cont'd.)	
	CMOS	300	±15	±15	MP7501K	Micro Power	
					MP7501S	† Micro Power	
					MP7503J	Micro Power	
					MP7503K	Micro Power	
					MP7503S	† Micro Power	
		400	±15	±15,5	**HI1818A-2**	**† Harris (699)**	
					HI1818A-5	**Harris (699)**	70
				±15	DG508A	† Siliconix	
		450	±15	±15	DG508B	Siliconix	
					DG508C	Siliconix	
		1300	±15	±15	**MPC8S**	**Burr-Brown (659)**	
		1500	±15	±15	MN4708	Analogic	
					MX-808	**Datel (683)**	
					MX-808M	**† Datel (683)**	
					HI508A-2	**† Harris (709)**	
		1800	±15	±15	**HI508A-5**	**Harris (709)**	
	JFET	260	-15 to 11.5	±15	MUX-08E	PMI	80
					MUX-88A	† PMI	
					MUX-88E	PMI	
		300	±10	±15,5	LF11305	† National	
					LF12305	National	
					LF13305	National	
		350*	-15 to 12	±15	**LF11508**	**† National (1035,1081)**	
					LF12508	**National (1035,1081)**	
					LF13508	**National (1035,1073,1081)**	90
		370	-15 to 12	±25	MUX-08F	PMI	
					MUX-88B	† PMI	
					MUX-88F	PMI	
	PMOS	150-250	±5	-20,5	DG501A	† Siliconix	
					DG501B	Siliconix	
					DG501C	Siliconix	
		150-400	±5	-20,5	SI3705	Siliconix	
		150-800	±10	-20,10	DG503A	† Siliconix	
					DG503B	Siliconix	100
		200-600	±5	-15,5	DG501A	† Siliconix	
		200-800	±5	-15,5	DG501B	Siliconix	
					DG501C	Siliconix	
		250-400	±5	-15,5	HMUX3705	† Hughes	
					AM3705	† National	
					AM3705	National	
		450	-15	-20	3708	Fairchild	
8 channel with shift register							
	DMOS	120	0-7	12	SD5350	Signetics	
8 channel, BCD input, latch							110
	PMOS	—	60	0-70	**LS7110**	**LSI Comp (494)**	
8 channel differential							
	CMOS	270	±15	±15	**MVD-807**	**Datel (683)**	
					MVD-807M	**† Datel (683)**	
		280	±7.5	±7.5	CD4097B	† RCA	
					CD4097BE	RCA	
		400	±15	±15	AD7507S	† AD	
					AD7507T	† AD	
					HI507-2	**† Harris (707)**	

(Continued)

DT[1] means four terminals with a pair of normally open and normally closed contacts.

INTERFACE–Analog Switches (Cont'd)

Function	Switch Type	ON Resistance 25°C,Ω	Analog Signal Range, V	Supply Voltage	Device	Source	Line
Multiplexers						**(Cont'd.)**	
8 channel differential						(Cont'd.)	
	CMOS	400	±15	±15	**HI507-5**	**Harris (707)**	
					MP7507S	† Micro Power	
					MP7507T	† Micro Power	
					DG507A	† Siliconix	
		450	±15	±15	AD7507J	AD	
					AD7507K	AD	
					MP7507J	Micro Power	
					MP7507K	Micro Power	10
					DG507B	Siliconix	
					DG507C	Siliconix	
		600	±10	±15	IH6216C	Intersil	
					IH6216M	† Intersil	
		1300	±15	±15	**MPC8D**	**Burr-Brown (659)**	
		1500	±15	±15	**MXD-807**	**Datel (683)**	
					MXD-807M	**† Datel (683)**	
					HI507A-2	**† Harris (707)**	
		1800	±15	±15	MN4708D	Analogic	
					HI507A-5	**Harris (707)**	20
					4551	Teledyne P	
	JFET	300	-15 to 11	±15	MUX-28A	† PMI	
					MUX-28E	PMI	
		350	-15 to 12	±15	LF11507	National	
		450	-15 to 11.5	±15	MUX-28B	† PMI	
					MUX-28F	PMI	
8 channel differential with storage, counter							
	PMOS	750	±5	-12,5	AY5-1016	GI	
					AY6-4016	† GI	
16 channel							30
	CMOS	270	±15	±15	**MV-1606**	**Datel (683)**	
					MV-1606M	† Datel	
		280	±7.5	±7.5	F4067BC	Fairchild	
					F4067BM	Fairchild	
					CD4067B	† RCA	
					CD4067BE	RCA	
		400	±15	±15	AD7506S	† AD	
					AD7506T	† AD	
					HI506-2	**† Harris (707)**	
					HI506-5	**Harris (707)**	40
					MP7506S	† Micro Power	
					MP7506T	† Micro Power	
					DG506A	† Siliconix	
		450	±15	±15	AD7506J	AD	
					AD7506K	AD	
					MP7506J	Micro Power	
					MP7506K	Micro Power	
					DG506B	Siliconix	
					DG506C	Siliconix	
		600	±10	±15	IH6116C	Intersil	
					IH6116M	† Intersil	50
		1000	-5 to 15	±15,5	**HI1840**	**† Harris (703)**	
		1300	±15	±15	**MPC16S**	**Burr-Brown (659)**	
		1500	±15	±15	**MX-1606**	**Datel (683)**	
					MX-1606M	**† Datel (683)**	
					HI506A-2	**† Harris (707)**	
		1800	±15	±15	MN4716	Analogic	
					HI506A-5	**Harris (707)**	
		—	±15	±15	TC5023	Toshiba	
						(Continued)	

Function	Switch Type	ON Resistance 25°C,Ω	Analog Signal Range, V	Supply Voltage	Device	Source	Line
Multiplexers						**(Cont'd.)**	
16 channel						(Cont'd.)	60
	PMOS	5K	-5 to 15	±15, 5	**HI1840-2**	**† Harris (703)**	
					4552	Teledyne P	
	JFET	300	-15 to 11	±15	MUX-16A	† PMI	
					MUX-16E	PMI	
		350	-15 to 12	±115	LF1106	National	
		450	-15 to 11.5	±15	MUX-16B	† PMI	
					MUX-16F	PMI	
16 channel with storage counter							
	PMOS	750	±5	-12,5	AY5-1016	GI	70
					AY6-4016	† GI	
18 channel with address latch							
	NMOS	600	0 to 6	12	MUX1600	GI	
32 channel with memory							
	CMOS	50	±9	±9	MT8804B	† Mitel	
					MT8804BE	Mitel	
Crosspoint Switches							
					MT8804B	† Mitel	
					MT8804BE	Mitel	
					MC3416	Motorola	80
					MC3466	Motorola	
					RC4444	Raytheon	
					RM4444	† Raytheon	
					CD22100	RCA	
					CD22101	RCA	
					CD22102	RCA	
					SD5300	Signetics	
Drivers							
High Current Switch Driver (to drive power transistor switches)							
					SG1629	† Silicon G	90
					SG3629	Silicon G	
2 channel							
					D112C	Intersil	
					D112M	† Intersil	
					D113C	Intersil	
					D113M	† Intersil	
					D120C	Intersil	
					D120M	† Intersil	
					D121C	Intersil	
					D121M	† Intersil	100
					D130A	† Siliconix	
					D130B	Siliconix	
					D139A	† Siliconix	
					D139B	Siliconix	
					D139C	Siliconix	
4 channel							
					MEM4900	GI	
					D129	Intersil	
					D129A	† Siliconix	
					D129B	Siliconix	110
4 channel for DMOS							
					SD5200	Signetics	
4 channel with Decoder							
					D132A	† Siliconix	
					D132B	Siliconix	
6 channel							
					D123C	Intersil	
					D123M	† Intersil	
						(Continued)	

† Military Temperature Range (−55° to 125°C)

* Typical Values

Bold face indicates additional data is provided on the page noted.

INTERFACE–Analog Switches (Cont'd)

Function	Switch Type	ON Resistance 25°C,Ω	Analog Signal Range, V	Supply Voltage	Device	Source	Line
Drivers					**(Cont'd.)**		
6 channel							
					(Cont'd.)		
					D125C	Intersil	
					D125M	† Intersil	
					D123A	† Siliconix	
					D123B	Siliconix	
					D125A	† Siliconix	
					D125B	Siliconix	
					CDR125A	† Teledyne C	

Function	Switch Type	ON Resistance 25°C,Ω	Analog Signal Range, V	Supply Voltage	Device	Source	Line

DT[4] means four terminals with a pair of normally open and normally closed contacts.

INTERFACE–Analog to Digital Converters

Bits Res.	Linearity Error ±LSB	Conversion Time ±½ LSB µS	Power Dis. mW (max.)	Bin. Output	Off. Bin. Output	Compl. Bin. Output	Compl. Off. Bin. Output	CTC or 2's Compl. Output	Sign. Magn. Output	Mux. In.	S&H	Integrating	Int. Ref.	Par. Out	Ser. Out	Device	Source
Binary Output																	
3, expandable 8-line																	
	1/125	0.016/0.02	2450	x	x									x		**ADC-HU3BGC**	**Datel (667)**
				x	x									x		**ADC-HU3BMM**	**† Datel (667)**
6	½	0.033*	1000	x		x		x			x			x		TDC1014J	TRW
		1000	20*	x											x	**TL507**	**TI (1152)**
8	½	0.033*	2500	x		x		x			x			x		TDC1007J	TRW
		0.4	400	x										x		TDC1001J	TRW
		0.9	1550	x		x	x						x	x	x	MN5101	Micro Net
				x		x	x						x	x	x	MN5101H	† Micro Net
		1	400	x										x		TDC1002J	TRW
			2700	x	x								x		x	ADH-8512-8	DDC
		1.5	1550	x		x	x						x	x	x	MN5100	Micro Net
				x		x	x						x	x	x	MN5100H	† Micro Net
		2.5	800	x	x			x					x	x		ADC541B-8	† Hybrid Sys.
				x	x			x					x	x		ADC541C-8	Hybrid Sys.
				x	x			x					x	x		ADC542B-8	† Hybrid Sys.
				x	x			x					x	x		ADC542C-8	Hybrid Sys.
			915			x							x	x	x	MN5140	Micro Net
						x							x	x	x	MN5140H	† Micro Net
					x								x	x	x	MN5141	Micro Net
					x								x	x	x	MN5141H	† Micro Net
					x								x	x	x	MN5142	Micro Net
					x								x	x	x	MN5142H	† Micro Net
				x									x	x	x	MN5143	Micro Net
				x									x	x	x	MN5143H	† Micro Net
			1000			x							x	x	x	MN5130	Micro Net
						x							x	x	x	MN5130H	† Micro Net
					x								x	x	x	MN5131	Micro Net
					x								x	x	x	MN5131H	† Micro Net
					x								x	x	x	MN5132	Micro Net
					x								x	x	x	MN5132H	† Micro Net
				x									x	x	x	MN5133	Micro Net
				x									x	x	x	MN5133H	† Micro Net
				x	x	x							x	x	x	MN5150	Micro Net
		2.8	900			x	x	x								**ADC82A**	**Burr-Brown (658)**
		6	1000			x							x	x	x	MN5120	Micro Net
						x							x	x	x	MN5120H	† Micro Net
					x								x	x	x	MN5121	Micro Net
					x								x	x	x	MN5121H	† Micro Net
					x								x	x	x	MN5122	Micro Net
					x								x	x	x	MN5122H	† Micro Net
				x									x	x	x	MN5123	Micro Net
				x									x	x	x	MN5123H	† Micro Net
		7	1165		x					x	x		x	x	x	MN7100	Micro Net
					x					x	x		x	x	x	MN7100H	† Micro Net
					x					x	x		x	x	x	MN7120	Micro Net
					x					x	x		x	x	x	MN7120H	† Micro Net

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Values

Bold face indicates additional data is provided on the page noted.

INTERFACE–Analog to Digital Converters (Cont'd)

Bits Res.	Linearity Error ±LSB	Conversion Time ±½ LSB µS	Power Dis. mW (max.)	Bin. Output	Off. Bin. Output	Compl. Bin. Output	Compl. Off. Bin. Output	CTC or 2's Compl. Output	Sign. Magn. Output	Mux. In.	S&H	Integrating	Int. Ref.	Par. Out	Ser. Out	Device	Source
Binary Output																	**(Cont'd.)**
8	½																(Cont'd.)
		12	720				x						x	x	x	MN509	Micro Net
							x						x	x	x	MN509H	† Micro Net
			900	x									x	x	x	MN502	Micro Net
				x									x	x	x	MN502H	† Micro Net
							x						x	x	x	MN503	Micro Net
							x						x	x	x	MN503H	† Micro Net
						x							x	x	x	MN504	Micro Net
						x							x	x	x	MN504H	† Micro Net
							x						x	x	x	MN507	Micro Net
							x						x	x	x	MN507H	† Micro Net
		20	350*	x	x								x	x	x	ZN432-8	† Ferranti
				x	x								x	x	x	ZN432B-8	Ferranti
				x	x								x	x	x	ZN432C-8	Ferranti
		20*	300	x									x	x		**NE5034**	**Signetics (809)**
		40	5*	x	x									x	x	AD7570J	AD
				x	x									x	x	MP7570J	Micro Power
				x	x									x	x	MP7570P	† Micro Power
		65	30	x						x				x		**ADC0808CC**	**National (1073,1074,1083)**
				x						x				x		**ADC0816CC**	**† National (1073)**
				x						x				x		ADC0816	† TI
				x						x				x		MM74C948	National
				x						x				x		INS8292	National
		100	70				x						x	x	x	MN5065	Micro Net
							x						x	x	x	MN5065H	† Micro Net
						x							x	x	x	MN5066	Micro Net
						x							x	x	x	MN5066H	† Micro Net
		100 µs*		x										x		**ADC0801**	**National (1066,1073,1074)**
		1800	20	x	x							x		x		**ADC-EK8B**	**Datel (662)**
			25	x								x		x		8700	Teledyne S
				x								x		x		8703	Teledyne S
			43	x										x		**ADC-ET8BM**	**† Datel (663)**
			50	x										x		**ADC-ET8BC**	**Datel (663)**
	1	1	2700	x	x											ADH-8512-7	DDC
		65	30	x						x				x		**ADC0809CC**	**National (1074,1083)**
				x						x				x		ADC0817CC	National
	2	50	255	x										x		ADC0800C	National
				x										x		**MM5357**	**National (220)**
		80	255	x										x		**ADC0800**	**National (1073,1074)**
				x										x		MM4357	National
8 (D/A, A/D, with counter)																	
	½	500	150	x	x								x	x		**ADC-MC8BC**	**Datel (664)**
			175	x									x	x		ZN425E	Ferranti
	1	500	175	x									x	x		ZN425J	† Ferranti

Bin.—Binary
Off.—Offset
Compl.—Complementary
Magn.—Magnitude
CTC—Compl. 2's Compl.
Int. Ref.—Internal Reference
Mux. In—Multiplexed Inputs
S&H—Sample and Hold
Par. Out—Parallel Output
Ser. Out—Serial Output

INTERFACE–Analog to Digital Converters (Cont'd)

Bits Res.	Linearity Error ±LSB	Conversion Time ±½ LSB µS	Power Dis. mW (max.)	Bin. Output	Off. Bin. Output	Compl. Bin. Output	Compl. Off. Bin. Output	CTC or 2's Compl. Output	Sign. Magn. Output	Mux. In.	S&H	Integrating	Int. Ref.	Par. Out	Ser. Out	Device	Source
Binary Output																	**(Cont'd.)**
8 (analog input for microprocessors)																	
	½	2.5	1350	x						x						**MP20**	**Burr-Brown (659)**
				x						x						**MP21**	**Burr-Brown (659)**
8 (analog to pulse width converter for microprocessor systems)																	
	½	—	15*							x						**MC14443**	**Motorola (782)**
										x						MC14447	Motorola
			75*							x						**µA9708C**	**Fairchild (944)**
										x						**µA9708M**	**† Fairchild (944)**
9	½	20	350	x	x								x	x	x	ZN432-9	† Ferranti
				x	x								x	x	x	ZN432B-9	Ferranti
				x	x								x	x	x	ZN432C-9	Ferranti
10	½	5	1400*			x	x	x					x	x	x	MN5240-10	Micro Net
		8	1400*			x	x	x					x	x	x	MNADC84-10	Micro Net
						x	x	x					x	x	x	MNADC85-10	† Micro Net
		10	1550			x	x	x					x	x	x	**ADC84-10**	**Burr-Brown (658)**
			1800		x	x	x	x					x	x	x	**ADC85-10**	**Burr-Brown (658)**
		20	350*	x	x								x	x	x	ZN432-10	† Ferranti
				x	x								x	x	x	ZN432B-10	Ferranti
				x	x								x	x	x	ZN432C-10	Ferranti
		21	950*			x	x	x					x	x	x	ADC80-10	Micro Net
		30	300	x	x								x	x		AD571K	AD
		120	5*	x	x									x	x	AD7570L	AD
				x	x									x	x	MP7570L	Micro Power
				x	x									x	x	MP7570S	† Micro Power
		6000	20	x	x							x		x		**ADC-EK10B**	**Datel (662)**
			25	x								x		x		8701	Teledyne S
				x								x		x		8704	Teledyne S
			43	x										x		**ADC-ET10BM**	**† Datel (663)**
			50	x										x		**ADC-ET10BC**	**Datel (663)**
	1	30	300	x	x								x	x		AD571J	AD
				x	x								x	x		AD571S	† AD
12	½	2	2700	x	x			x								ADH-8516-12	DDC
		5	1400*			x	x	x					x	x	x	MN5240-12	Micro Net
		8	1400*			x	x	x					x	x	x	MNADC84-12	Micro Net
						x	x	x					x	x	x	MNADC85-12	Micro Net
			2000			x	x	x					x	x	x	**ADC-HZ12BGC**	**Datel (669)**
						x	x	x					x	x	x	**ADC-HZ12BMM**	**† Datel (669)**
			2150			x	x				x		x	x		**ADC-HS12BGC**	**Datel (666)**
						x	x				x		x	x		**ADC-HS12BMM**	**† Datel (666)**
		9*	2845	x	x					x	x		x	x		**HDAS-8MC**	**Datel (660)**
				x	x					x	x		x	x		**HDAS-8MM**	**† Datel (660)**
				x	x					x	x		x	x		**HDAS-16MC**	**Datel (660)**
				x	x					x	x		x	x		**HDAS-16MM**	**† Datel (660)**
		10	1550			x	x	x					x	x	x	**ADC84-12**	**Burr-Brown (658)**
			1800			x	x	x					x	x	x	**ADC85-12**	**Burr-Brown (658)**
		13	745	x										x	x	MN5213	Micro Net
				x										x	x	MN5213H	† Micro Net
							x							x	x	MN5214	Micro Net

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Values

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INTERFACE–Analog to Digital Converters (Cont'd)

Bits Res.	Linearity Error ±LSB	Conversion Time ±½ LSB µS	Power Dis. mW (max.)	Bin. Output	Off. Bin. Output	Compl. Bin. Output	Compl. Off. Bin. Output	CTC or 2's Compl. Output	Sign. Magn. Output	Mux. In.	S&H	Integrating	Int. Ref.	Par. Out	Ser. Out	Device	Source
Binary Output																	**(Cont'd.)**
12	½	13	745				x							x	x	MN5214H	† Micro Net
							x							x	x	MN5215	Micro Net
							x							x	x	MN5215H	† Micro Net
			915	x									x	x	x	MN5210	Micro Net
				x									x	x	x	MN5210H	† Micro Net
							x						x	x	x	MN5211	Micro Net
							x						x	x	x	MN5211H	† Micro Net
							x						x	x	x	MN5212	Micro Net
							x						x	x	x	MN5212H	† Micro Net
						x							x	x	x	MN5216	Micro Net
						x							x	x	x	MN5216H	† Micro Net
		20	2000			x	x	x					x	x	x	**ADC-HX12BGC**	**Datel (668)**
						x	x	x					x	x	x	**ADC-HX12BMM**	**† Datel (668)**
		25	925	x	x			x					x	x	x	AD572A	AD
				x	x			x					x	x	x	AD572B	AD
				x	x			x					x	x	x	AD572S	† AD
			950*			x	x	x					x	x	x	**ADC80A-12**	**Burr-Brown (658)**
						x	x	x					x	x	x	**ADC80-12**	**Burr-Brown (658)**
						x	x	x					x	x	x	ADC80-12	Micro Net
			2100			x	x						x	x	x	MN5500	Micro Net
		30	725			x	x	x					x	x	x	ADC581B-12	† Hybrid Sys.
						x	x	x					x	x	x	ADC581C-12	Hybrid Sys.
			780	x	x								x		x	AD574K	AD
				x	x								x		x	AD574S	† AD
				x	x								x		x	AD574T	† AD
		40	1150			x	x						x	x	x	873-15	† Beckman
						x	x						x	x	x	873-88	Beckman
		50	435	x	x								x	x	x	7556C	Beckman
				x	x								x	x	x	7556M	† Beckman
			745	x										x	x	MN5203	Micro Net
				x										x	x	MN5203H	† Micro Net
							x							x	x	MN5204	Micro Net
							x							x	x	MN5204H	† Micro Net
							x							x	x	MN5205	Micro Net
							x							x	x	MN5205H	† Micro Net
			915	x									x	x	x	MN5200	Micro Net
				x									x	x	x	MN5200H	† Micro Net
							x						x	x	x	MN5201	Micro Net
							x						x	x	x	MN5201H	† Micro Net
							x						x	x	x	MN5202	Micro Net
							x						x	x	x	MN5202H	† Micro Net
						x							x	x	x	MN5206	Micro Net
						x							x	x	x	MN5206H	† Micro Net
			1370			x	x						x	x	x	MN515	Micro Net
						x	x						x	x	x	MN515H	† Micro Net
			1775	x	x								x	x	x	MN516	Micro Net

(Continued)

Bin.—Binary
Off.—Offset
Compl.—Complementary
Magn.—Magnitude
CTC—Compl. 2's Compl.
Int. Ref.—Internal Reference
Mux. In—Multiplexed Inputs
S&H—Sample and Hold
Par. Out—Parallel Output
Ser. Out—Serial Output

INTERFACE–Analog to Digital Converters (Cont'd)

Bits Res.	Linearity Error ±LSB	Conversion Time ±½ LSB µS	Power Dis. mW (max.)	Bin. Output	Off. Bin. Output	Compl. Bin. Output	Compl. Off. Bin. Output	CTC or 2's Compl. Output	Sign. Magn. Output	Mux. In.	S&H	Integrating	Int. Ref.	Par. Out	Ser. Out	Device	Source
Binary Output																	**(Cont'd.)**
12	½	50	1775														(Cont'd.)
				x	x								x	x	x	MN516H	† Micro Net
		175	80	x									x	x	x	MN5250	Micro Net
				x									x	x	x	MN5250H	† Micro Net
							x						x	x	x	MN5251	Micro Net
							x						x	x	x	MN5251H	† Micro Net
							x						x	x	x	MN5252	Micro Net
							x						x	x	x	MN5252H	† Micro Net
						x							x	x	x	MN5253	Micro Net
						x							x	x	x	MN5253H	† Micro Net
		200	40	x	x									x	x	7555C	Beckman
				x	x									x	x	7555M	† Beckman
			210	x										x	x	**ADC1210**	**National (1073,1074,220)**
				x										x	x	**ADC1210H**	**National (1073,1074,220)**
		350	26	x	x			x					x	x	x	**ADC-HC12BGC**	**Datel (665)**
				x	x			x					x	x	x	**ADC-HC12BMM**	**† Datel (665)**
		2400	43	x										x		**ADC-ET12BM**	**† Datel (663)**
		24000	20	x	x							x		x		**ADC-EK12B**	**Datel (662)**
			25	x								x		x		8702	Teledyne S
				x								x		x		8705	Teledyne S
		100K	20	x					x			x	x	x		ICL7109	Intersil
	1	2	2700	x	x			x								ADH-8516-11	DDC
		30	780	x	x								x		x	AD574J	AD
	1½	2400	50	x										x		**ADC-ET12BC**	**Datel (663)**
	2	200	210	x										x	x	**ADC1211**	**† National (1074)**
				x										x	x	**ADC1211C**	**National (1074)**
12 plus sign (2 device set)																	
	½	36000	—	x					x					x	x	LFB300	National
				x					x					x	x	MM5863	National
				x					x					x	x	**ADB1200C**	**National (1073,1074)**
				x					x					x	x	LFB300	National
12 (3-Digit BCD)																	
	¼	1200	20									x		x		**ADC-EK12DC**	**Datel (662)**
												x		x		**ADC-EK12DM**	**† Datel (662)**
	½	50	1775										x	x	x	MN517	Micro Net
													x	x	x	MN517H	† Micro Net
	1	6000*	50									x	x		x	AD2020	AD
12 (2 Device Set)																	
	½	250000	40	x					x			x	x	x		ICL7104-12	Intersil
			360	x					x			x	x	x		ICL8052A	Intersil
13	½	40000*	64					x						x		MP7550B	Micro Power
			72					x				x		x	x	AD7550B	AD
14	½	250	300				x						x	x	x	MN5260	Micro Net
14 (3½-Digit BCD)																	
	½	12000	25									x		x		8750	Teledyne S

† Military Temperature Range (−55° to 125°C)

* Typical Values

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INTERFACE–Analog to Digital Converters (Cont'd)

Bits Res.	Linearity Error ±LSB	Conversion Time ±½ LSB µS	Power Dis. mW (max.)	Bin. Output	Off. Bin. Output	Compl. Bin. Output	Compl. Off. Bin. Output	CTC or 2's Compl. Output	Sign. Magn. Output	Mux. In.	S&H	Integrating	Int. Ref.	Par. Out	Ser. Out	Device	Source
Binary Output																**(Cont'd.)**	
14 (2 Device Set)																	
	½	250000	40	x					x			x	x	x		ICL7104-14	Intersil
			360	x					x			x	x	x		ICL8052A	Intersil
16	4	100	1440			x	x	x					x	x	x	MN5280	Micro Net
16 (2 Device Set)																	
	½	250000	40	x					x			x	x	x		ICL7104-16	Intersil
			360	x					x			x	x	x		ICL8052A	Intersil

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INTERFACE–Analog to Digital Converters (Cont'd)

Digits	Device	Source	Line
Decimal Output			
Bargraph (Analog Output)	UAA170	Siemens	
	UAA180	Siemens	
2½ Digits, v to f Converter	ADD2500	National	
3 Digits, Integrating	**LD130**	**Siliconix (827)**	
3 Digits, Dual Slope, 2 Device Sets	CA3161	RCA	
	CA3162	RCA	10
3 Digits, Dual Slope, Building Block, for microprocessor systems, e.g. TMS1000	TL505	TI	
3-1/3 Digits, Dual Slope	**LD131**	**Siliconix (827)**	
3½ Digits, Integrating	MN2301	Analogic	
	ADC-EK12DC	**Datel (662)**	
	ADC-EK12DM	**† Datel (662)**	
	ZNA1116E	Ferranti	20
	ICL7106	Intersil	
	ICL7107	Intersil	
	MC904	IPI	
	MP7138	Micro Power	
	MC14433	Motorola	
	ADC3511	**National (1073,1074,252)**	
	ADD3500	National	
	ADD3501	**National (1074)**	
	MM74C935-1	National	30
	MM74C937-1	National	
	8750	Teledyne S	
3½ Digits, Integrating, 2 device sets	ICL7101	Intersil	
	ICL7103	Intersil	
	ICL8052	Intersil	
	ICL8053	Intersil	
	ICL8068	Intersil	
	LD110	Intersil	
	LD111	Intersil	40
	LD114	Intersil	
	LD110	**Siliconix (829)**	
	LD111	**Siliconix (829)**	
	LD111A	**Siliconix (829)**	
	LD114	Siliconix	
	TL502	TI	
	TL503	TI	
3½ Digits, 2 device sets	MP7104	Micro Power	
3¾ Digits, Integrating	ZNA216	Ferranti	50
	ADD3701	**National (1074,268)**	
	ADC3711	**National (1073,1074,252)**	
	MM74C936-1	National	
	MM74C938-1	National	
	S190	Siemens	
3½-4½ Digits, Ramp Type, 2 device sets	MC1405	Motorola	60
	MC1505	† Motorola	
	MC14435	Motorola	
	MC14435E	† Motorola	

Digits	Device	Source	Line
Decimal Output (Cont'd.)			
4½ Digits, Dual Slope, 2 device sets	ICL7103A	Intersil	
	ICL8052A	Intersil	
	ICL8053A	Intersil	
	ICL8068A	Intersil	
	LF12300	National	
	LF13300	**National (10 3 5,1074)**	70
	ADB4500	National	
	ADB4510	National	
	LD120	**Siliconix (831)**	
	LD121	**Siliconix (831)**	
	TL500	TI	
	TL501	TI	
	TL502	TI	
	TL503	TI	

† Military Temperature Range (−55° to 125°C)

* Typical Values

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INTERFACE–Digital to Analog Converters

D/A Converters

Bits Res.	Linearity Error ±LSB	Settling Time ±½ LSB µS	Power Dis. mW (max.)	Bin. Input	Off. Bin. Input	Compl. Bin. Input	Compl. Off. Bin. Input	CTC or 2's Compl. Input	Sign. Magn. Input	TTL Logic	CMOS Logic	ECL Logic	Int. Ref.	Mult.	Latches	Device	Source
4-Bit—16 Lines																	
	½	25*	125	x								x				**DAC-HU4BGC**	**Datel (680)**
				x								x				**DAC-HU4BMM**	**† Datel (680)**
6	¼	3	250			x	x									µPC603	NEC America
						x	x			x			x			DAC-01	† PMI
						x	x			x			x			DAC-01B	† PMI
						x	x			x			x			DAC-01C	PMI
						x	x			x			x			DAC-01F	† PMI
						x	x			x			x			DAC-01H	PMI
	1/3	3	250			x	x	x		x			x			MP5520A	† Micro Power
						x	x	x		x			x			MP5520B	† Micro Power
						x	x	x		x			x			MP5520C	Micro Power
						x	x	x		x			x			MP5520F	† Micro Power
			200			x	x	x		x			x			MP5520H	Micro Power
	½	0.3	240			x	x							x		MC1406	Motorola
						x	x							x		MC1506	† Motorola
		3	200			x	x	x		x			x			MP5520D	Micro Power
			250			x	x			x			x			DAC-01D	PMI
		23*	400		x	x				x			x			MN301	Micro Net
					x	x				x			x			MN301H	† Micro Net
6/12-Binary Serial																	
	½	—	5							x	x			x	x	µA9706C	Fairchild
										x	x			x	x	µA9706M	† Fairchild
										x	x			x	x	µA9706AC	Fairchild
										x	x			x	x	µA9706AM	† Fairchild
8	1/8	0.15	1.5*	x	x	x	x				x			x		AD7523L	AD
				x	x	x	x				x			x		MP7523L	Micro Power
	1/8*	0.04*	450	x						x				x		**HI5608-2**	**† Harris (730)**
				x						x				x		**HI5608-4**	**Harris (730)**
				x						x				x		**HI5608-5**	**Harris (730)**
				x						x				x		**HI5608-8**	**† Harris (730)**
	¼	0.135	174	x	x	x	x			x	x	x		x		DAC-08A	† AMD
				x	x	x	x			x	x	x		x		µA0801A	† Fairchild
				x	x	x	x			x	x	x		x		µA0801H	Fairchild
				x	x	x	x			x	x	x		x		DAC-08A	† Motorola
				x	x	x	x			x	x	x		x		DAC-08H	Motorola
				x						x				x		**DAC0802**	**† National (1074)**
				x						x				x		**DAC0802C**	**National (1074)**
				x	x	x	x			x	x	x		x		DAC-08A	† PMI
				x	x	x	x			x	x	x		x		DAC-08H	PMI
				x	x	x	x			x	x	x		x		DAC-08A	† Raytheon
				x	x	x	x			x	x	x		x		DAC-08H	Raytheon
				x	x	x	x			x	x	x		x		DAC-08A	† Signetics
				x	x	x	x			x	x	x		x		DAC-08H	Signetics
				x	x	x				x	x	x		x		NE5009	Signetics
				x	x	x				x	x	x		x		SE5009	† Signetics
		0.15	1.5*	x	x	x	x				x			x		AD7523K	AD
				x	x	x	x				x			x		MP7523K	Micro Power

(Continued)

Bin.—Binary
Off.—Offset
Compl.—Complementary
Magn.—Magnitude
Int. Ref.—Internal Reference
CTC—Compl. 2's Compl.
Mult.—Multiplying

INTERFACE–Digital to Analog Converters (Cont'd)

Bits Res.	Linearity Error ±LSB	Settling Time ±½ LSB µS	Power Dis. mW (max.)	Bin. Input	Off. Bin. Input	Compl. Bin. Input	Compl. Off. Bin. Input	CTC or 2's Compl. Input	Sign. Magn. Input	TTL Logic	CMOS Logic	ECL Logic	Int. Ref.	Mult.	Latches	Device	Source
D/A Converters																	**(Cont'd.)**
8	¼																(Cont'd.)
		0.16*	123(5V)	x	x	x	x	x		x	x			x	x	AM6080AC	AMD
				x	x	x	x	x		x	x			x	x	AM6080AM	† AMD
				x	x	x	x	x	x	x	x			x	x	AM6081AC	AMD
				x	x	x	x	x	x	x	x			x	x	AM6081AM	† AMD
		0.2*	255*	x						x	x	x	x	x	x	NE5119	Signetics
				x						x	x	x	x	x	x	SE5119	† Signetics
		0.25*	265	x	x					x	x			x		AD1408-9	AD
				x	x					x	x			x		AD1508-9	† AD
		2*	255	x						x	x	x	x	x	x	NE5019	Signetics
				x						x	x	x	x	x	x	SE5019	† Signetics
	½	0.01	450	x		x				x					x	TDC1016J	TRW
		0.01*	500*	x								x		x		MC10318	Motorola
		0.025	630	x	x					x			x			**DAC-HF8BGC**	**Datel (677)**
				x	x					x			x			**DAC-HF8BMM**	**† Datel (677)**
		0.135	174	x	x	x	x			x	x	x		x		DAC-08	† AMD
				x	x	x				x	x	x		x		µA0801	† Fairchild
				x	x	x	x			x	x	x		x		DAC-08	† Motorola
				x	x	x				x				x		**DAC0800**	**† National (1073,1074)**
				x	x	x	x			x	x	x		x		DAC-08	† PMI
				x	x	x	x			x	x	x		x		DAC-08	† Raytheon
				x	x	x	x			x	x	x		x		DAC-08	† Signetics
				x	x	x				x	x	x		x		SE5008	† Signetics
			570	x						x			x			MN3015	Micro Net
				x						x			x			MN3015H	† Micro Net
		0.15	1.5*	x	x	x	x				x			x		AD7523J	AD
				x	x	x	x				x			x		MP7523J	Micro Power
			136	x	x					x	x	x		x		DAC-08BC	Datel
				x	x					x	x	x		x		**DAC-08BM**	**† Datel (670)**
			174	x	x	x	x			x	x	x		x		DAC-08E	AMD
				x	x	x	x			x	x	x		x		µA0801E	Fairchild
				x	x	x	x			x	x	x		x		DAC-08E	Motorola
				x	x	x				x				x		**DAC0800C**	**National (1073,1074)**
				x	x	x	x			x	x	x		x		DAC-08E	PMI
				x	x	x	x			x	x	x		x		DAC-08E	Raytheon
				x	x	x	x			x	x	x		x		DAC-08E	Signetics
				x	x	x				x	x	x		x		NE5008	Signetics
		0.16*	123 (5V)	x	x	x	x	x		x	x			x	x	AM6080C	AMD
				x	x	x	x	x		x	x			x	x	AM6080M	† AMD
				x	x	x	x	x	x	x	x			x	x	AM6081C	AMD
			123(5V)	x	x	x	x	x	x	x	x			x	x	AM6081M	† AMD
		0.2	240			x	x			x			x			**DAC90B**	**Burr-Brown (658)**
						x	x			x			x			**DAC90S**	**† Burr-Brown (658)**
		0.20*	255	x						x	x	x	x	x	x	**NE5118**	**Signetics (810)**
				x						x	x	x	x	x	x	**SE5118**	**† Signetics (810)**

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Values

Bold face indicates additional data is provided on the page noted.

INTERFACE–Digital to Analog Converters (Cont'd)

D/A Converters (Cont'd.)

Bits Res.	Linearity Error ±LSB	Settling Time ±½ LSB µS	Power Dis. mW (max.)	Bin. Input	Off. Bin. Input	Compl. Bin. Input	Compl. Off. Bin. Input	CTC or 2's Compl. Input	Sign. Magn. Input	TTL Logic	CMOS Logic	ECL Logic	Int. Ref.	Mult.	Latches	Device	Source
																	(Cont'd.)
8	½	0.25*	265	x						x	x			x		SSS1408A-8	AMD
				x						x	x			x		SSS1508A-8	† AMD
				x	x					x	x			x		AD1408-8	AD
				x	x					x	x			x		AD1508-8	† AD
				x	x					x	x			x		SSS1408A-8	PMI
				x	x					x	x			x		SSS1508A-8	† PMI
		0.25/1.0	900			x	x	x		x			x	x		**DAC82K**	**Burr-Brown (658)**
						x	x	x		x			x	x		**DAC82S**	**† Burr-Brown (658)**
		0.3*	280	x	x					x	x			x		AD559K	AD
				x	x					x	x			x		AD559S	† AD
			305	x						x	x			x		1408-8	AMD
				x						x	x			x		1508-8	† AMD
				x	x					x	x			x		**DAC-IC8BC**	**Datel (671)**
				x	x					x	x			x		**DAC-IC8BM**	**† Datel (671)**
				x						x	x			x		µA0802	† Fairchild
				x						x	x			x		µA0802A	Fairchild
				x										x		MC1408-8	Motorola
				x										x		MC1508-8	† Motorola
				x						x				x		**DAC0808**	**† National (1073,1074)**
				x						x				x		**DAC0808C**	**National (1073,1074)**
				x						x				x		**LM1408-8**	**National (1073)**
				x						x				x		LM1508-8	† National
				x						x				x		MC1408-8	Signetics
				x						x				x		MC1508-8	† Signetics
		1	750	x						x			x			MN3008	Micro Net
				x						x			x			MN3008H	† Micro Net
					x					x			x			MN3009	Micro Net
					x					x			x			MN3009H	† Micro Net
		1.5	30	x	x					x	x			x		DAC331B-8	† Hybrid Sys.
				x	x	x				x	x			x		DAC331C-8	Hybrid Sys.
			200	x						x						**HI-1080**	**Harris (711)**
		2*	255*	x						x	x	x	x	x	x	**NE5018**	**Signetics (808)**
				x						x	x	x	x	x	x	**SE5018**	**† Signetics (808)**
		2.5	570	x	x	x				x			x			MN3014	Micro Net
				x	x	x				x			x			MN3014H	† Micro Net
		3	830	x	x	x				x			x		x	MN3020	Micro Net
				x	x	x				x			x		x	MN3020H	† Micro Net
		4	300	x	x	x				x	x		x			DAC336B-8	† Hybrid Sys.
				x	x	x				x	x		x			DAC336C-8	Hybrid Sys.
		20	300	x						x	x		x			DAC337B-0	† Hybrid Sys.
				x						x	x		x			DAC337C-0	Hybrid Sys.
					x					x	x		x			DAC337B-1	† Hybrid Sys.
					x					x	x		x			DAC337C-1	Hybrid Sys.
		23*	585			x				x	x		x			MN3000	Micro Net (Continued)

Bin.—Binary
Off.—Offset
Compl.—Complementary
Magn.—Magnitude
Int. Ref.—Internal Reference
CTC—Compl. 2's Compl.
Mult.—Multiplying

INTERFACE–Digital to Analog Converters (Cont'd)

Bits Res.	Linearity Error ±LSB	Settling Time ±½ LSB µS	Power Dis. mW (max.)	Bin. Input	Off. Bin. Input	Compl. Bin. Input	Compl. Off. Bin. Input	CTC or 2's Compl. Input	Sign. Magn. Input	TTL Logic	CMOS Logic	ECL Logic	Int. Ref.	Mult.	Latches	Device	Source	
D/A Converters																		**(Cont'd.)**
																		(Cont'd.)
8	½	23*	585			x				x	x		x			MN3000H	† Micro Net	
					x					x	x		x			MN3001	Micro Net	
					x					x	x		x			MN3001H	† Micro Net	
				x						x	x		x			MN3002	Micro Net	
				x						x	x		x			MN3002H	† Micro Net	
					x					x	x		x			MN3006	Micro Net	
					x					x	x		x			MN3006H	† Micro Net	
		30	570	x	x	x				x			x			MN3013	Micro Net	
				x	x	x				x			x			MN3013H	† Micro Net	10
	1	0.15	174	x	x	x	x			x	x	x		x		DAC-08C	AMD	
				x	x	x	x			x	x	x		x		µA801C	Fairchild	
				x	x	x	x			x	x	x		x		DAC-08C	Motorola	
				x	x	x				x				x		**DAC0801C**	**National**	**(1074)**
				x	x	x	x			x	x	x		x		DAC-08C	NEC America	
				x	x	x	x			x	x	x		x		DAC-08C	PMI	
				x	x	x	x			x	x	x		x		DAC-08C	Raytheon	
				x	x	x	x			x	x	x		x		DAC-08C	Signetics	
				x	x	x				x	x	x		x		NE5007	Signetics	
		0.25*	265	x	x					x	x			x		SSS1408A-7	AMD	20
				x	x					x	x			x		AD1408-7	AD	
				x	x					x	x			x		µA0802B	Fairchild	
				x	x					x	x			x		SSS1408A-7	PMI	
		0.3*	305	x						x	x			x		1408-7	AMD	
				x										x		MC1408-7	Motorola	
				x						x				x		**DAC0807C**	**National**	**(1074)**
				x						x				x		**LM1408-7**	**National**	**(1073)**
				x						x				x		MC1408-7	Motorola	
		3	200	x						x						**HI-1085**	**† Harris**	**(711)**
	1¼	0.3*	305	x							x			x		MC3408	Motorola	30
	2	0.25*	265	x	x					x	x			x		SSS1408A-6	AMD	
				x	x					x	x			x		µA0802C	Fairchild	
				x	x					x	x			x		SSS1408A-6	PMI	
		0.3*	305	x						x	x			x		1408-6	AMD	
				x										x		MC1408-6	Motorola	
				x						x				x		**DAC0806C**	**National**	**(1074)**
				x						x				x		**LM1408-6**	**National**	**(1073)**
				x						x				x		MC1408-6	Signetics	
8-2 Digit BCD																		
	¼	0.135	194							x	x	x		x		DAC-20A	† Motorola	40
										x	x	x		x		DAC-20E	Motorola	
										x	x	x		x		DAC-20A	† PMI	
										x	x	x		x		DAC-20E	PMI	
	½	0.135	194							x	x	x		x		DAC-20	† Motorola	
										x	x	x		x		DAC-20C	Motorola	
		0.15	194							x	x	x		x		DAC-20	† PMI	
										x	x	x		x		DAC-20C	PMI	

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Values

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INTERFACE–Digital to Analog Converters (Cont'd)

D/A Converters (Cont'd.)

Bits Res.	Linearity Error ±LSB	Settling Time ±½ LSB µS	Power Dis. mW (max.)	Bin. Input	Off. Bin. Input	Compl. Bin. Input	Compl. Off. Bin. Input	CTC or 2's Compl. Input	Sign. Magn. Input	TTL Logic	CMOS Logic	ECL Logic	Int. Ref.	Mult.	Latches	Device	Source
8-2 Digit BCD																	(Cont'd.)
	½	23*	630							x	x		x			MN3010	Micro Net
										x	x		x			MN3010H	† Micro Net
8(7-Bits plus Sign) Companding																	
	½ step	0.5	192							x						AM6070AC	AMD
										x						AM6070AM	† AMD
										x						AM6071AC	AMD
										x						AM6071AM	† AMD
		0.5*	192							x	x	x		x		DAC-76B	† PMI
										x	x			x		DAC-76E	PMI
										x	x	x		x		DAC-86E	PMI
										x	x	x		x		DAC-87E	PMI
	1 step	0.5	192							x						AM6070C	AMD
										x						AM6070M	† AMD
										x						AM6071C	AMD
										x						AM6071M	† AMD
		0.5*	192							x	x	x		x		DAC-76	† PMI
										x	x	x		x		DAC-76C	PMI
										x	x	x		x		DAC-86C	PMI
										x	x	x		x		DAC-87C	PMI
	1½ step	0.5*	192							x	x	x		x		DAC-76D	PMI
	—	0.5	192							x						AM6072C	AMD
										x						AM6072M	† AMD
										x						AM6073C	AMD
										x						AM6073M	† AMD
8 (A/D, D/A, with counter)																	
	½	2.0	175	x						x	x		x			ZN425E	Ferranti
	1	2.0	175	x						x	x		x			ZN425J	† Ferranti
8 plus sign																	
	½	20	750	x						x				x		MN380	Micro Net
				x						x				x		MN380H	† Micro Net
Dual 8-Bit, data latches, addressable																	
	1	—	1350	x						x			x		x	**MP10**	**Burr-Brown (659)**
				x						x			x		x	**MP11**	**Burr-Brown (659)**
9 plus sign																	
	½	15	600		x		x			x				x		MN411	Micro Net
					x		x			x				x		MN411H	† Micro Net
		60	600		x		x			x				x		MN410	Micro Net
					x		x			x				x		MN410H	† Micro Net
10	1/8	0.5*	50	x	x	x	x			x	x			x		MP7620J	Micro Power
	¼	0.25	75	x		x				x	x	x		x		DAC-10A	† PMI
		0.25*	275	x	x					x	x		x			AD561K	AD
				x	x					x	x		x			AD561T	† AD
		0.5*	50	x	x	x	x			x	x			x		MP7620K	Micro Power
	¼*	0.6*	780	x						x	x			x		**HI5610-2**	**† Harris (724)**
				x						x	x			x		**HI5610-4**	**Harris (724)**

(Continued)

Bin.—Binary
Compl.—Complementary
CTC—Compl. 2's Compl.
Off.—Offset
Magn.—Magnitude
Int. Ref.—Internal Reference
Mult.—Multiplying

INTERFACE–Digital to Analog Converters (Cont'd)

Bits Res.	Linearity Error ±LSB	Settling Time ±½ LSB µS	Power Dis. mW (max.)	Bin. Input	Off. Bin. Input	Compl. Bin. Input	Compl. Off. Bin. Input	CTC or 2's Compl. Input	Sign. Magn. Input	TTL Logic	CMOS Logic	ECL Logic	Int. Ref.	Mult.	Latches	Device	Source
D/A Converters																	**(Cont'd.)**
																	(Cont'd.)
10	¼*	0.6*	780	x						x	x			x		**HI5610-5**	**Harris (724)**
				x						x	x			x		**HI5610-8**	**† Harris (724)**
	½	0.01	450	x		x				x					x	TDC1017J	TRW
		0.025	705	x	x					x			x			**DAC-HF10BGC**	**Datel (677)**
				x	x					x			x			**DAC-HF10BMM**	**† Datel (677)**
		0.25	75	x	x	x	x			x	x	x		x		DAC-10B	† PMI
				x	x	x	x			x	x	x		x		DAC-10E	PMI
				x	x	x	x			x	x	x		x		DAC-101A	† PMI
				x	x	x	x			x	x	x		x		DAC-101E	PMI
			380	x							x			x		MC3410	Motorola
				x							x			x		MC3510	† Motorola
		0.25*	275	x	x					x	x		x			AD561J	AD
				x	x					x	x		x			AD561S	AD
		0.375	250		x	x	x			x			x			DAC-100A	PMI
					x	x	x			x			x			DAC-100A	† PMI
		0.5	30	x	x					x	x			x		**DAC-HA10BC-1**	**Datel (675)**
				x	x					x	x			x		**DAC-HA10BM-1**	**† Datel (675)**
		0.5*	0.025	x	x					x	x			x		**DAC-HA10BC**	**Datel (675)**
				x	x					x	x			x		**DAC-HA10BM**	**† Datel (675)**
			20*	x	x	x	x			x	x			x		AD7520L	AD
				x	x	x	x			x	x			x		AD7520U	† AD
				x	x	x	x			x	x			x		AD7530L	AD
				x	x	x	x							x		AD7520L	Intersil
				x	x	x	x							x		AD7520U	† Intersil
				x	x	x	x			x	x			x		AD7530L	Intersil
				x	x	x	x			x	x			x		MP7520L	Micro Power
				x	x	x	x			x	x			x		MP7520P	Micro Power
				x	x	x	x			x	x			x		MP7520U	† Micro Power
			40	x	x	x	x			x	x			x	x	AD7522L	AD
				x	x	x	x			x	x			x	x	AD7522U	† AD
			50	x	x					x	x			x	x	MP7522L	Micro Power
				x	x	x	x			x	x			x	x	MP7522U	† Micro Power
				x	x	x	x			x	x			x		MP7620L	Micro Power
		1	18	x	x					x				x		MDA100-10	† DDC
			54	x	x					x				x		MDA101-10	† DDC
		1.5	30	x	x					x	x			x		DAC331B-10	† Hybrid Sys.
				x	x					x	x			x		DAC331C-10	Hybrid Sys.
		4*	255	x						x	x	x	x	x	x	**NE5020**	**Signetics (809)**
		5	825				x			x			x			DAC346C-10B	Hybrid Sys.
						x				x			x			DAC346C-10U	Hybrid Sys.
		15	170	x				x		x	x			x		DAC348B-10	† Hybrid Sys.
				x				x		x	x			x		DAC348C-10	Hybrid Sys.
		20	150				x			x	x		x			DAC347LPB-10B	† Hybrid Sys.
							x			x	x			x		DAC347LPC-10B	Hybrid Sys.
						x				x	x			x		DAC347LPB-10U	† Hybrid Sys.
						x				x	x			x		DAC347LPC-10U	Hybrid Sys.

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Values

Bold face indicates additional data is provided on the page noted.

INTERFACE–Digital to Analog Converters (Cont'd)

Bits Res.	Linearity Error ±LSB	Settling Time ±½ LSB µS	Power Dis. mW (max.)	Bin. Input	Off. Bin. Input	Compl. Bin. Input	Compl. Off. Bin. Input	CTC or 2's Compl. Input	Sign. Magn. Input	TTL Logic	CMOS Logic	ECL Logic	Int. Ref.	Mult.	Latches	Device	Source
D/A Converters																	**(Cont'd.)**
10	½																(Cont'd.)
		23*	585			x				x			x			MN3003	Micro Net
						x				x			x			MN3003H	† Micro Net
					x					x			x			MN3004	† Micro Net
					x					x			x			MN3004H	† Micro Net
				x						x			x			MN3005	Micro Net
				x						x			x			MN3005H	† Micro Net
					x					x			x			MN3007	Micro Net
					x					x			x			MN3007H	† Micro Net
		30	—		x					x				x		M/DA2005-1	HyComp
		40	300	x						x	x		x			DAC337B-3	† Hybrid Sys.
				x						x	x		x			DAC337C-3	Hybrid Sys.
					x					x	x		x			DAC337B-4	† Hybrid Sys.
					x					x	x		x			DAC337C-4	Hybrid Sys.
		50	230		x		x				x			x		MN3100	Micro Net
					x		x				x			x		MN3100H	† Micro Net
		500*	24	x						x	x			x		**AD7520L**	**National (1073)**
				x						x	x			x		AD7520U	† National
				x						x	x			x		**DAC1020**	**† National (1073,1074,1080)**
				x						x	x			x		**DAC1020C**	**National (1073,1074,1080)**
	1	0.25	75	x	x	x	x			x	x	x		x		DAC-10F	PMI
				x	x	x	x			x	x	x		x		DAC-101B	† PMI
				x	x	x	x			x	x	x		x		DAC-101F	PMI
			380	x							x			x		MC3410C	Motorola
			390	x	x					x	x					**DAC-IC10BC**	**Datel (673)**
		0.3	250		x	x	x			x			x			DAC-100B	† PMI
					x	x	x			x			x			DAC-100B	PMI
		0.5*	20*	x	x	x	x			x	x			x		AD7520K	AD
				x	x	x	x			x	x			x		AD7520T	† AD
				x	x	x	x			x	x			x		AD7530K	AD
				x	x	x	x			x	x			x		AD7520K	Intersil
				x	x	x	x			x	x			x		AD7520T	† Intersil
				x	x	x	x			x	x			x		AD7530K	Intersil
				x	x	x	x			x	x			x		MP7520K	Micro Power
				x	x	x	x			x	x			x		MP7520N	Micro Power
				x	x	x	x			x	x			x		MP7520T	† Micro Power
			40	x	x	x	x			x	x			x	x	AD7522K	AD
				x	x	x	x			x	x			x	x	AD7522T	† AD
			50	x	x	x	x			x	x			x	x	MP7522K	Micro Power
				x	x	x	x			x	x			x	x	MP7522T	† Micro Power
				x	x	x	x			x	x			x		MP7620M	Micro Power
		1.5*	300		x			x		x	x		x			DAC-04AC	PMI
					x			x		x	x		x			DAC-04BC	PMI
					x			x		x	x		x			DAC-06E	PMI
			350	x						x	x		x			DAC-03AD	PMI

(Continued)

Bin.—Binary Compl.—Complementary CTC—Compl. 2's Compl.
Off.—Offset Magn.—Magnitude Int. Ref.—Internal Reference Mult.—Multiplying

INTERFACE–Digital to Analog Converters (Cont'd)

Bits Res.	Linearity Error ±LSB	Settling Time ±½ LSB µS	Power Dis. mW (max.)	Bin. Input	Off. Bin. Input	Compl. Bin. Input	Compl. Off. Bin. Input	CTC or 2's Compl. Input	Sign. Magn. Input	TTL Logic	CMOS Logic	ECL Logic	Int. Ref.	Mult.	Latches	Device	Source
D/A Converters																	**(Cont'd.)**
10	1	1.5*	350	x						x	x		x			DAC-03BD	PMI (Cont'd.)
		500*	24	x						x	x			x		**AD7520K**	**National (1073)**
				x						x	x			x		**AD7520T**	**National (1073)**
				x						x	x			x		**DAC1021**	**† National (1073,1074)**
				x						x	x			x		**DAC1021C**	**National (1073,1074)**
	2	0.225	250		x	x	x			x			x			DAC-100C	PMI
					x	x	x			x			x			DAC-100C	† PMI
		0.5*	20*	x	x	x	x			x	x			x		AD7520J	AD
				x	x	x	x			x	x			x		AD7520S	† AD
				x	x	x	x			x	x			x		AD7530J	AD
				x	x	x	x			x	x			x		AD7520J	Intersil
				x	x	x	x			x	x			x		AD7520S	† Intersil
				x	x	x	x			x	x			x		AD7530J	Intersil
				x	x	x	x			x	x			x		MP7520J	Micro Power
				x	x	x	x			x	x			x		MP7520M	† Micro Power
				x	x	x	x			x	x			x		MP7520S	Micro Power
			40	x	x	x	x			x	x			x	x	AD7522J	AD
				x	x	x	x			x	x			x	x	AD7522S	† AD
			50	x	x	x	x			x	x			x	x	MP7522J	Micro Power
				x	x	x	x			x	x			x	x	MP7522S	† Micro Power
		1.5*	300		x			x		x	x		x			DAC-04CC	PMI
					x			x		x	x		x			DAC-06F	PMI
			350	x						x	x		x			DAC-03CD	PMI
					x			x		x	x		x			DAC-06A	PMI
		500*	24	x						x	x			x		**AD7520J**	**National (1073)**
				x						x	x			x		**AD7520S**	**† National (1073)**
				x						x	x			x		**DAC1022**	**† National (1073,1074)**
				x						x	x			x		**DAC1022C**	**National (1073,1074)**
	3	0.225	250		x	x	x			x			x			DAC-100D	PMI
					x	x	x			x			x			DAC-100D	† PMI
		0.5*	50	x	x	x	x			x	x			x		MP7520H	Micro Power
		1.5*	350		x			x		x	x		x			DAC-06B	PMI
	4	1.5*	300		x			x		x	x		x			DAC-06G	PMI
			350	x						x	x		x			DAC-03DD	PMI
		2.5*	350					x		x	x		x			DAC-04DD	PMI
	5	1.5*	350					x		x	x		x			DAC-06C	† PMI
	8	0.5*	50	x	x	x	x			x	x			x		MP7520G	Micro Power
10 plus Sign	½	6	300	x												µPC610	NEC America
	1	1.5*	300	x					x	x	x		x			DAC-02AC	PMI
				x					x	x	x		x			DAC-02BC	PMI
				x					x	x	x		x			DAC-05E	PMI
	2	1.5*	300	x					x	x	x		x			DAC-02CC	PMI (Continued)

† Military Temperature Range (−55° to 125°C) * Typical Values

Bold face indicates additional data is provided on the page noted.

INTERFACE–Digital to Analog Converters (Cont'd)

Bits Res.	Linearity Error ±LSB	Settling Time ±½ LSB µS	Power Dis. mW (max.)	Bin. Input	Off. Bin. Input	Compl. Bin. Input	Compl. Off. Bin. Input	CTC or 2's Compl. Input	Sign. Magn. Input	TTL Logic	CMOS Logic	ECL Logic	Int. Ref.	Mult.	Latches	Device	Source
D/A Converters																	**(Cont'd.)**
10 plus Sign																	(Cont'd.)
	2	1.5*	300	x					x	x	x		x			DAC-05F	PMI
			350	x					x	x	x		x			DAC-05A	†PMI
	3	1.5*	350	x					x	x	x		x			DAC-05B	†PMI
				x					x	x	x		x			DAC-05C	PMI
	4	1.5*	300	x					x	x	x		x			DAC-05G	PMI
		2.5*	350	x					x	x	x		x			DAC-02DD	PMI
11 plus Sign dynamic range (7-Bit plus Sign Format)																	
	½ step	0.5	192							x						AM6071AC	AMD
										x						AM6071AM	†AMD
		0.5*	207							x	x	x		x		DAC-76B	†PMI
										x	x	x		x		DAC-76E	PMI
										x	x	x		x		DAC-86E	PMI
										x	x	x		x		DAC-87E	PMI
	1 step	0.5	192							x						AM6071C	AMD
										x						AM6071M	†AMD
		0.5*	207							x	x	x		x		DAC-76C	PMI
										x	x	x		x		DAC-86C	PMI
										x	x	x		x		DAC-87C	PMI
	—	0.5	192							x						AM6073C	AMD
										x						AM6073M	†AMD
12	¼	0.4	365	x	x					x	x					**DAC-681C**	**Datel (674)**
			400	x	x					x	x			x		AD566K	AD
				x	x					x	x			x		AD566S	†AD
				x	x					x	x			x		AD566T	†AD
			500	x	x					x	x			x		AD565K	AD
				x	x					x	x			x		AD565S	†AD
				x	x					x	x			x		AD565T	†AD
			780	x						x	x			x		**HI562-2**	**†Harris (713)**
				x						x	x			x		**HI562-8**	**Harris (713)**
		0.75*	150	x	x	x	x			x	x	x		x		DAC-12A	†PMI
		1.5*	465	x	x					x	x			x		AD562S/BIN	AD
			500	x	x	x	x			x	x			x		SSS562S/BIN	†PMI
			475	x	x					x	x		x			AD563K/BIN	AD
				x	x					x	x		x			AD563S/BIN	†AD
				x	x					x	x		x			AD563T/BIN	†AD
		1.8	500	x	x	x	x			x	x		x	x		MN562-SD-BIN	Analogic
			700	x	x	x	x			x	x		x	x		MN563-SD-BIN	Analogic
		5	575	x	x					x	x		x			AD564/BIN	AD
				x	x					x	x		x			AD564S/BIN	†AD
				x	x					x	x		x			AD564T/BIN	†AD
	½	0.050	780	x	x					x			x			**DAC-HF12BGC**	**Datel (677)**
				x	x					x			x			**DAC-HF12BMM**	**†Datel (677)**
			1200	x	x					x			x	x		DAC391B-12	†Hybrid Sys.
				x						x			x	x		DAC391C-12	Hybrid Sys.
		0.085*	780	x						x	x			x		**HI5612-2**	**†Harris (718)**

(Continued)

Bin.—Binary
Compl.—Complementary
CTC—Compl. 2's Compl.
Off.—Offset
Magn.—Magnitude
Int. Ref.—Internal Reference
Mult.—Multiplying

INTERFACE–Digital to Analog Converters (Cont'd)

D/A Converters (Cont'd.)

Bits Res.	Linearity Error ±LSB	Settling Time ±½ LSB µS	Power Dis. mW (max.)	Bin. Input	Off. Bin. Input	Compl. Bin. Input	Compl. Off. Bin. Input	CTC or 2's Compl. Input	Sign. Magn. Input	TTL Logic	CMOS Logic	ECL Logic	Int. Ref.	Mult.	Latches	Device	Source
																	(Cont'd.)
12	½	0.085*	780	x						x	x			x		**HI5612-4**	**Harris (718)**
				x						x	x			x		**HI5612-5**	**Harris (718)**
				x						x	x			x		**HI5612-8**	**† Harris (718)**
		0.3/3*	625*			x	x	x		x			x			**DAC1285**	**† National (1073,1074)**
						x	x	x		x			x			**DAC1285C**	**National (1073,1074)**
			800			x	x	x		x			x			**DAC80/CBI**	**Burr-Brown (658)**
						x	x	x		x			x			**DAC85/CBI**	**Burr-Brown (658)**
						x	x	x		x			x			**DAC85C/CBI**	**Burr-Brown (658)**
					x	x	x	x		x			x			DAC87-CBI	† Burr-Brown
			850*			x	x	x		x			x			DAC80/CBI	Micro Net
						x	x	x		x			x			DAC85/CBI	† Micro Net
						x	x	x		x			x			DAC85/CBI	Micro Net
			925			x	x	x		x			x			DAC80/CBI	AD
						x	x	x		x			x			DAC85/CBI	† AD
						x	x	x		x			x			DAC85C/CBI	AD
		0.4	365	x	x					x	x					**DAC-681M**	**† Datel (674)**
			400	x	x					x	x			x		AD566J	AD
				x	x					x	x			x		DAC862B	Burr-Brown
				x	x					x	x			x		DAC862S	† Burr-Brown
			500	x	x					x	x		x			AD565J	AD
			780	x						x	x			x		**HI562-4**	**Harris (713)**
				x						x	x			x		**HI562-5**	**Harris (713)**
		0.5	0.05	x	x					x	x			x		**DAC-HA12BC**	**Datel (675)**
				x	x					x	x			x		**DAC-HA12BM**	**† Datel (675)**
			30	x	x					x	x			x		**DAC-HA12BC-1**	**Datel (675)**
				x	x					x	x			x		**DAC-HA12BM-1**	**† Datel (675)**
		0.5/3*	850			x	x			x			x			DAC-SCB1	DDC
		0.6	1200	x	x					x			x	x		DAC392B-12	Hybrid Sys.
				x	x					x				x	x	DAC392C-12	Hybrid Sys.
		0.75	150	x		x				x	x	x		x		DAC-12B	† PMI
				x		x				x	x	x		x		DAC-12F	PMI
		1	20	x	x					x				x		MDA120-12	† DDC
			20*	x	x	x	x			x	x			x		AD7541B	AD
				x	x	x	x			x	x			x		AD7541K	AD
				x	x	x	x			x	x			x		AD7541T	† AD
				x	x	x	x			x	x			x		ICL7541K	Intersil
				x	x	x	x			x	x			x		ICL7541T	Intersil
		1.5	450			x	x			x	x		x			DAC335B-12	† Hybrid Sys.
						x	x			x	x		x			DAC335C-12	Hybrid Sys.
		1.5*	465	x	x					x	x			x		AD562K/BIN	AD
			475	x	x					x	x		x			AD563J/BIN	AD
			500	x						x	x			x		SSS562A/BIN	PMI
				x						x	x			x		SSS562K/BIN	PMI
		1.8	500	x	x	x	x			x	x		x	x		MN562-AD-BIN	Analogic

(Continued)

† Military Temperature Range (–55° to 125°C)

* Typical Values

Bold face indicates additional data is provided on the page noted.

INTERFACE–Digital to Analog Converters (Cont'd)

D/A Converters (Cont'd.)

Bits Res.	Linearity Error ±LSB	Settling Time ±½ LSB µS	Power Dis. mW (max.)	Bin. Input	Off. Bin. Input	Compl. Bin. Input	Compl. Off. Bin. Input	CTC or 2's Compl. Input	Sign. Magn. Input	TTL Logic	CMOS Logic	ECL Logic	Int. Ref.	Mult.	Latches	Device	Source
																	(Cont'd.)
12	½	1.8	500	x	x	x	x			x	x		x	x		MN562-ID-BIN	Analogic
				x	x	x	x			x	x		x	x		MN562-KD-BIN	Analogic
			700	x	x	x	x			x	x		x	x		MN563-JD-BIN	Analogic
				x	x	x	x			x	x		x	x		MN563-KD-BIN	Analogic
				x	x	x	x			x	x		x	x		MN563-TD-BIN	Analogic
		2	50	x	x	x	x			x	x			x		**MP7621B**	**Micro Power (765)**
				x	x	x	x			x	x			x		**MP7621K**	**Micro Power (765)**
				x	x	x	x			x	x			x		**MP7621T**	**† Micro Power (765)**
			150*	x	x					x			x			4058	Teledyne P
		2*	20*	x	x	x	x			x	x			x		7521M	† Beckman
				x	x					x	x			x	x	7545C	Beckman
				x	x					x	x			x	x	7545M	† Beckman
		3	30	x	x					x	x			x		DAC331B-12	† Hybrid Sys.
				x	x	x	x			x	x			x		DAC331C-12	Hybrid Sys.
			810		x					x	x					MN364	Micro Net
					x					x	x					MN364H	† Micro Net
						x				x	x					MN366	Micro Net
						x				x	x					MN366H	† Micro Net
			900	x	x					x			x		x	**DAC-HK12BGC**	**Datel (678)**
				x	x					x			x		x	**DAC-HK12BMM**	**† Datel (678)**
								x		x			x		x	DAC-HK12BC-2	Datel
								x		x			x		x	**DAC-HK12BMM-2**	**† Datel (678)**
			1050			x	x			x			x			**DAC-HZ12BGC**	**Datel (681)**
						x	x			x			x			**DAC-HZ12BMM**	**† Datel (681)**
		4	300	x		x	x			x	x		x		x	DAC336B-12	† Hybrid Sys.
		5	575	x	x					x	x		x			AD564J/BIN	AD
		4	300	x		x	x			x	x		x		x	DAC336C-12	Hybrid Sys.
		5	800			x	x			x	x		x			**DAC1200**	**† National (1073,1074)**
						x	x			x	x		x			**DAC1200C**	**National (1073,1074)**
			825			x	x			x			x			DAC346C-12	Hybrid Sys.
			1600			x	x			x			x		x	MN3500	Micro Net
		5*	525*			x	x			x	x		x			MN3850	Micro Net
						x	x			x	x		x			MN3850H	† Micro Net
			675*			x	x			x			x		x	MN3860	Micro Net
						x	x			x			x		x	MN3860H	† Micro Net
		6	400*	x	x			x			x		x		x	HI5712	Harris
		6/50*	330			x	x	x		x	x		x			7580I/V	Beckman
		7	750			x	x			x			x			MN415	Micro Net
						x	x			x			x			MN415H	† Micro Net
			870				x			x	x					MN360	Micro Net
							x			x	x					MN360H	† Micro Net
						x				x	x					MN362	Micro Net
						x				x	x					MN362H	† Micro Net
			1155	x	x					x			x			MN416	Micro Net (Continued)

Bin.—Binary
Compl.—Complementary
CTC—Compl. 2's Compl.
Off.—Offset
Magn.—Magnitude
Int. Ref.—Internal Reference
Mult.—Multiplying

INTERFACE–Digital to Analog Converters (Cont'd)

Bits Res.	Linearity Error ±LSB	Settling Time ±½ LSB µS	Power Dis. mW (max.)	Bin. Input	Off. Bin. Input	Compl. Bin. Input	Compl. Off. Bin. Input	CTC or 2's Compl. Input	Sign. Magn. Input	TTL Logic	CMOS Logic	ECL Logic	Int. Ref.	Mult.	Latches	Device	Source
D/A Converters																	**(Cont'd.)**
																	(Cont'd.)
12	½	7	1155	x	x					x			x			MN416H	† Micro Net
		15	170	x				x		x	x			x		DAC348B-12	† Hybrid Sys.
				x				x		x	x			x		DAC348C-12	Hybrid Sys.
			300	x	x					x	x		x			DAC349B-12	† Hybrid Sys.
				x	x					x	x		x			DAC349C-12	Hybrid Sys.
		20	150				x			x	x		x			DAC347LPB-12B	† Hybrid Sys.
							x			x	x		x			DAC347LPC-12B	Hybrid Sys.
						x				x	x		x			DAC347LPB-12U	† Hybrid Sys.
						x				x	x		x			DAC347LPC-12U	Hybrid Sys.
		30	—	x		x				x				x		M/DA2000	HyComp
		35	90			x				x			x			MN371	Micro Net
						x				x			x			MN371H	† Micro Net
			1065	x		x				x	x		x			MN3210	Micro Net
							x			x	x		x			MN3211	Micro Net
		50	75				x			x	x		x			DAC356LPB-12	† Hybrid Sys.
							x			x	x		x			DAC356LPC-12	Hybrid Sys.
			175				x			x	x		x			DAC356B-12	† Hybrid Sys.
							x			x	x		x			DAC356C-12	Hybrid Sys.
			1653			x	x					x	x			ADH-030-12	DDC
		70	90				x			x	x		x			MN370	Micro Net
							x			x	x		x			MN370H	† Micro Net
	½*	10	360	x	x					x	x		x	x	x	7546C	Beckman
				x	x					x	x		x	x	x	7546M	† Beckman
	1	0.3/3*	625*			x	x	x		x			x			**DAC1280C**	**National (1073,1074)**
		0.5/3*	850			x	x			x			x			DAC-SCCB1	DDC
		0.75	150	x	x	x	x			x	x	x		x		DAC-12G	PMI
		1	20	x	x					x				x		MDA120-11	† DDC
				x	x	x	x			x	x			x		**MP7621K**	**Micro Power (765)**
			20*	x	x	x	x			x	x			x		AD7541A	AD
				x	x	x	x			x	x			x		AD7541J	AD
				x	x	x	x			x	x			x		ICL7541J	Intersil
				x	x	x	x			x	x			x		ICL7541S	† Intersil
			50*	x	x	x	x			x	x			x		AD7541S	† AD
		2	50	x	x	x	x			x	x			x		**MP7621A**	**Micro Power (765)**
				x	x	x	x			x	x			x		**MP7621J**	**Micro Power (765)**
				x	x	x	x			x	x			x		**MP7621S**	**† Micro Power (765)**
		30	—	x		x				x				x		M/DA2005	HyComp
		50	1653			x	x					x	x			ADH-030-11	DDC
	2	0.04	—	x	x							x	x			DA4000	HyComp
		0.5*	20*	x	x	x	x			x	x			x		AD7521L	AD
				x	x	x	x			x	x			x		AD7521U	† AD
				x	x	x	x			x	x			x		AD7531L	AD
				x	x	x	x			x	x			x		AD7521L	Intersil
				x	x	x	x			x	x			x		AD7521U	† Intersil
				x	x	x	x			x	x			x		AD7531L	Intersil

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Values

Bold face indicates additional data is provided on the page noted.

INTERFACE–Digital to Analog Converters (Cont'd)

Bits Res.	Linearity Error ±LSB	Settling Time ±½ LSB µS	Power Dis. mW (max.)	Bin. Input	Off. Bin. Input	Compl. Bin. Input	Compl. Off. Bin. Input	CTC or 2's Compl. Input	Sign. Magn. Input	TTL Logic	CMOS Logic	ECL Logic	Int. Ref.	Mult.	Latches	Device	Source
D/A Converters																	**(Cont'd.)**
12	2	0.5*	20*														(Cont'd.)
				x	x	x	x			x	x			x		MP7521L	Micro Power
				x	x	x	x			x	x			x		MP7521P	Micro Power
				x	x	x	x			x	x			x		MP7521U	† Micro Power
		5	800			x	x			x	x		x			**DAC1201**	**† National (1074)**
						x	x			x	x		x			**DAC1201C**	**National (1074)**
		50	1653			x	x					x	x			ADH-030-10	DDC
		500*	24	x						x	x			x		**AD7521L**	**National (1073)**
				x						x	x			x		AD7521U	† National
				x						x	x			x		**DAC1220**	**† National (1073,1074,1080)**
				x						x	x			x		**DAC1220C**	**National (1073,1074,1080)**
	4	0.5*	20*	x	x	x	x			x	x			x		AD7521K	AD
				x	x	x	x			x	x			x		AD7521T	† AD
				x	x	x	x			x	x			x		AD7531K	AD
				x	x	x	x			x	x			x		AD7521K	Intersil
				x	x	x	x			x	x			x		AD7521T	† Intersil
				x	x	x	x			x	x			x		AD7531K	Intersil
				x	x	x	x			x	x			x		MP7521K	Micro Power
				x	x	x	x			x	x			x		MP7521N	Micro Power
				x	x	x	x			x	x			x		MP7521T	† Micro Power
		50	1653			x	x					x	x			ADH-030-8	DDC
		500*	24	x						x	x			x		**AD7521K**	**National (1073)**
				x						x	x			x		**AD7521T**	**† National (1073)**
				x						x	x			x		**DAC1221**	**† National (1073,1074)**
				x						x	x			x		**DAC1221C**	**National (1073,1074)**
	8	0.5*	20*	x	x	x	x			x	x			x		AD7521J	AD
				x	x	x	x			x	x			x		AD7521S	† AD
				x	x	x	x			x	x			x		AD7531J	AD
				x	x	x	x			x	x			x		AD7521J	Intersil
				x	x	x	x			x	x			x		AD7521S	† Intersil
				x	x	x	x			x	x			x		AD7531J	Intersil
				x	x	x	x			x	x			x		MP7521J	Micro Power
				x	x	x	x			x	x			x		MP7521M	Micro Power
				x	x	x	x			x	x			x		MP7521S	† Micro Power
		500*	24	x						x	x			x		**AD7521J**	**National (1073)**
				x						x	x			x		**AD7521S**	**† National (1073)**
				x						x	x			x		**DAC1222**	**† National (1073,1074)**
				x						x	x			x		**DAC1222C**	**National (1073,1074)**
	16	0.5*	50	x	x	x	x			x	x			x		MP7521H	Micro Power
	32	0.5*	50	x	x	x	x			x	x			x		MP7521G	Micro Power
12-3 Digit BCD																	
	1/10	1.5*	465							x	x			x		AD562K/BCD	AD
										x	x			x		AD562S/BCD	† AD

(Continued)

Bin.—Binary Compl.—Complementary CTC—Compl. 2's Compl.
Off.—Offset Magn.—Magnitude Int. Ref.—Internal Reference Mult.—Multiplying

INTERFACE–Digital to Analog Converters (Cont'd)

D/A Converters (Cont'd.)

Bits Res.	Linearity Error ±LSB	Settling Time ±½ LSB µS	Power Dis. mW (max.)	Bin. Input	Off. Bin. Input	Compl. Bin. Input	Compl. Off. Bin. Input	CTC or 2's Compl. Input	Sign. Magn. Input	TTL Logic	CMOS Logic	ECL Logic	Int. Ref.	Mult.	Latches	Device	Source
12-3 Digit BCD																	(Cont'd.)
1/10	1.5*		475							x	x		x			AD563J/BCD	AD
										x	x		x			AD563K/BCD	AD
										x	x		x			AD563S/BCD	† AD
										x	x		x			AD563T/BCD	† AD
			500							x	x	x		x		SSS562S/BCD	† PMI
		1.8	500							x	x		x	x		MN562-SD-BCD	Analogic
			700							x	x		x	x		MN563-SD-BCD	Analogic
		5	575							x	x		x			AD564J/BCD	AD
										x	x		x			AD564K/BCD	AD
										x	x		x			AD564S/BCD	† AD
										x	x		x			AD564T/BCD	† AD
			800										x			**DAC1202**	**† National (1074)**
													x			**DAC1202C**	**National (1074)**
¼	0.3/3*		925							x	x		x			DAC80/CCD	AD
										x	x		x			DAC85/CCD	† AD
										x	x		x			DAC85C/CCD	AD
		3	900										x		x	**DAC-HK12DGC**	**Datel (678)**
													x		x	**DAC-HK12DMM**	**† Datel (678)**
		3*	1050							x			x			**DAC-HZ12DGC**	**Datel (681)**
										x			x			**DAC-HZ12DMM**	**† Datel (681)**
½	0.3/3*		800							x			x			**DAC80/CCD**	**Burr-Brown (658)**
										x			x			**DAC85/CCD**	**† Burr-Brown (658)**
										x			x			**DAC85C/CCD**	**Burr-Brown (658)**
			850*							x			x			DAC80/CCD	Micro Net
										x			x			DAC85/CCD	† Micro Net
										x			x			DAC85C/CCD	Micro Net
		0.5	30							x	x		x			**DAC-HA12DC-1**	**Datel (675)**
										x	x		x			**DAC-HA12DM-1**	**† Datel (675)**
		0.5*	0.05							x	x		x			**DAC-HA12DC**	**Datel (675)**
										x	x		x			**DAC-HA12DM**	**† Datel (675)**
			20*							x	x			x		ICL7113K	Intersil
										x	x			x		ICL7113T	† Intersil
		0.5/3*	850							x			x			DAC-SCCD	DDC
										x			x			DAC-SCCCD	DDC
		1.5*	500							x	x	x		x		SSS562A/BCD	PMI
										x	x	x		x		SSS562K/BCD	PMI
		5	800										x			**DAC1203**	**† National (1074)**
		1.8	500							x	x		x	x		MN562-AD-BCD	Analogic
										x	x		x	x		MN562-ID-BCD	Analogic
										x	x		x	x		MN562-KD-BCD	Analogic
			700							x	x		x	x		MN563-JD-BCD	Analogic
										x	x		x	x		MN563-KD-BCD	Analogic
										x	x		x	x		MN563-TD-BCS	Analogic
		5	450							x	x		x			DAC335B-3D	† Hybrid Sys.

(Continued)

† Military Temperature Range (−55° to 125°C) * Typical Values

Bold face indicates additional data is provided on the page noted.

INTERFACE–Digital to Analog Converters (Cont'd)

D/A Converters (Cont'd.)

Bits Res.	Linearity Error ±LSB	Settling Time ±½ LSB µS	Power Dis. mW (max.)	Bin. Input	Off. Bin. Input	Compl. Bin. Input	Compl. Off. Bin. Input	CTC or 2's Compl. Input	Sign. Magn. Input	TTL Logic	CMOS Logic	ECL Logic	Int. Ref.	Mult.	Latches	Device	Source
12-3 Digit BCD																	(Cont'd.)
	½	5	450							x	x		x			DAC335C-3D	Hybrid Sys.
			800										x			**DAC1203C**	**National (1074)**
		15	300							x	x		x			DAC349B-3D	† Hybrid Sys.
										x	x		x			DAC349C-3D	Hybrid Sys.
		35	1065							x	x		x			MN3212	Micro Net
	2	0.3/3*	800							x			x			**DAC1286**	**† National (1074)**
										x			x			**DAC1286C**	**National (1074)**
		0.5*	20*							x	x			x		ICL7113J	Intersil
										x	x			x		ICL7113S	† Intersil
		0.75*	150							x	x	x		x		DAC-30B	† PMI
										x	x	x		x		DAC-30E	PMI
	4	0.3*/3*	800							x			x			**DAC1287C**	**National (1074)**
		0.75*	150							x	x	x		x		DAC-30F	PMI
12 plus Sign dynamic range (7-Bit plus Sign Format)																	
	½ step	0.5	192							x						AM6070AC	AMD
										x						AM6070AM	† AMD
			207							x	x	x		x		DAC-86E	PMI
	1 step	0.5	192							x						AM6070C	AMD
										x						AM6070M	† AMD
										x	x	x		x		DAC-76	† PMI
			207							x	x	x		x		DAC-86C	PMI
	—	0.5	192							x						AM6072C	AMD
										x						AM6072M	† AMD
12, Pulse Output																	
	¼	4ms	—	x						x	x					ICL7105	Intersil
13	1	0.1	980				x			x			x			2615-12	DDC
		1.6	1100				x			x			x			SDAC-12	DDC
	2	0.1	980				x			x			x			2615-11	DDC
		1.6	1100				x			x			x			SDAC-11	DDC
	4	0.1	980				x			x			x			2615-10	DDC
		1.6	1100				x			x			x			SDAC-10	DDC
13(3 Device Set)																	
	1	1.8	3475					x		x			x			DDAC-12	DDC
	2	1.8	3475					x		x			x			DDAC-11	DDC
	4	1.8	3475					x		x			x			DDAC-10	DDC
14	½	3	30	x	x					x	x			x		DAC331B-14	† Hybrid Sys.
				x	x					x	x			x		DAC331C-14	Hybrid Sys.
	1	0.5	0.05	x	x					x	x			x		**DAC-HA14BC**	**Datel (676)**
				x	x					x	x			x		**DAC-HA14BM**	**† Datel (676)**
			30	x	x					x	x			x		**DAC-HA14BC-1**	**Datel (676)**
				x	x					x	x			x		**DAC-HA14BM-1**	**† Datel (676)**
	2	20	900	x						x				x		DAC-U12-1	† DDC
				x						x				x		DAC-U12-3	DDC
	4	20	900	x	x					x				x		DAC-U11-1	† DDC
				x	x					x				x		DAC-U11-3	DDC

Bin.—Binary
Off.—Offset
Compl.—Complementary
Magn.—Magnitude
Int. Ref.—Internal Reference
CTC—Compl. 2's Compl.
Mult.—Multiplying

INTERFACE–Digital to Analog Converters (Cont'd)

Bits Res.	Linearity Error ±LSB	Settling Time ±½ LSB µS	Power Dis. mW (max.)	Bin. Input	Off. Bin. Input	Compl. Bin. Input	Compl. Off. Bin. Input	CTC or 2's Compl. Input	Sign. Magn. Input	TTL Logic	CMOS Logic	ECL Logic	Int. Ref.	Mult.	Latches	Device	Source	
D/A Converters																		**(Cont'd.)**
16	½	35	420	x						x	x		x			MN3310	Micro Net	
		50	900			x				x						DAC327C-16ER	Hybrid Sys.	
	2	35	1170			x	x			x			x			**DAC-HP16BMC**	**Datel**	**(679)**
						x	x			x			x			**DAC-HP16BMM**	**† Datel**	**(679)**
		50/100*	575*			x				x			x			**DAC70/CSB**	**† Burr-Brown**	**(658)**
						x				x			x			**DAC70C/CSB**	**Burr-Brown**	**(658)**
	3	50/100*	575*				x			x			x			**DAC70/COB**	**† Burr-Brown**	**(658)**
							x			x			x			**DAC70C/COB**	**Burr-Brown**	**(658)**
	4	50	900			x				x			x			DAC327C-16	Hybrid Sys.	
16-4 Digit BCD																		
	½	15	1170							x			x			**DAC-HP16DMC**	**Datel**	**(679)**
										x			x			**DAC-HP16DMM**	**† Datel**	**(679)**
		35	420							x	x		x			MN3300	Micro Net	
		50	900							x			x			DAC327C-4D	Hybrid Sys.	
										x						DAC327C-4DER	Hybrid Sys.	
		50/100*	575*							x			x			**DAC70/CCD**	**† Burr-Brown**	**(658)**
										x			x			**DAC70C/CCD**	**Burr-Brown**	**(658)**

† Military Temperature Range (−55° to 125°C)

* Typical Values

Bold face indicates additional data is provided on the page noted.

INTERFACE–Display Drivers

Function	Device	Source	Line
Display Drivers			
Display Driver, 4-Digit (Stores segment and address data, drives 7-8 segment digits)	MM74C911	National	
Display Driver, 6-Digit BCD (Stores segment and address data, drives 7-8 segment digits)	MM74C912	National	
Display Driver, 6 Digit Hex(Stores Segment and address data, drives 7 segments)	MM74C917	National	
BCD to 7-Segment LED Driver Adjustable Current	DS7858	National	10
	DS8858	National	
BCD to 7-Segment LED Decoder/Driver, Constant Current	NE586	Signetics	
	NE587	Signetics	
	DS8857	National	
BCD to 7-Segment Latch/Decoder/Driver	DI-260	Dionics	
BCD to 7-Segment LED Latch/Decoder/Driver, with ripple blanking	F4734BC	Fairchild	20
	F4734BM	† Fairchild	
BCD plus 1 to 7-Segment Display Driver; output 1-16	U143	Telefunken	
BCD (Hexadecimal) to 7-Segment LED Decoder/Driver, Constant Current, with Latch	9368C	Fairchild	
	MD4368B	† Mitel	
	MD4368BE	Mitel	30
BCD (Hexadecimal) to 7-Segment LED Decoder/Driver	M54405	Mitsubishi	
BCD (Hexadecimal) to 7-Segment LED Decoder/Driver, with Latch	MD4311B	† Mitel	
	MD4311BE	Mitel	
	DS8673	National	
BCD to 7-Segment LED Decoder/Driver with Latch, output 0-9,—, E, H, L, P	9374C	Fairchild	40
	DS8674	National	
BCD to 7-Segment Decoder/Driver, Active High, Resistive Pull-Up	54LS48	† Fairchild	
	74LS48	Fairchild	
	5448	† Fairchild	
	7448	Fairchild	
	54LS248	† Fairchild	
	74LS248	Fairchild	50
	9307C	Fairchild	
	9307M	† Fairchild	
	HD74LS48	Hitachi	
	HD74LS248	Hitachi	
	M53248	Mitsubishi	
	MC5448	† Motorola	
	MC7448	Motorola	
	SN54LS48	† Motorola	
	SN74LS48	Motorola	
	SN54LS248	† Motorola	60
	SN74LS248	Motorola	
	MC8307	Motorola	
	MC9307	† Motorola	
	DM5448	† National	
	DM7448	National	

(Continued)

Function	Device	Source	Line
Display Drivers (Cont'd.)			
BCD to 7-Segment Decoder/Driver, Active High, Resistive Pull-Up (Cont'd.)	DM54LS48	† National	
	DM74LS48	National	
	DM54LS248	† National	70
	DM74LS248	National	
	DS7856	† National	
	DS8856	National	
	5448	† Signetics	
	7448	Signetics	
	N8T05	Signetics	
	S8T05	† Signetics	
	SN5448	† TI	
	SN7448	TI	
	SN54248	† TI	80
	SN74248	TI	
	SN54LS48	† TI	
	SN74LS48	TI	
	SN54LS248	† TI	
	SN74LS248	TI	
BCD to 7-Segment Decoder/Driver, Active High, Open Collector	5449	† Fairchild	
	7449	Fairchild	
	54LS49	† Fairchild	90
	74LS49	Fairchild	
	54LS249	† Fairchild	
	74LS249	Fairchild	
	HD74LS49	Hitachi	
	HD74LS249	Hitachi	
	MC5449	† Motorola	
	MC7449	Motorola	
	SN54LS249	Motorola	
	SN74LS249	† Motorola	
	SN54LS49	† Motorola	100
	SN74LS49	Motorola	
	DM54LS49	† National	
	DM74LS49	National	
	DM54LS249	† National	
	DM74LS249	National	
	N8T06	Signetics	
	S8T06	† Signetics	
	SN5449	† TI	
	SN7449	TI	
	SN54249	† TI	110
	SN74249	TI	
	SN54LS49	† TI	
	SN74LS49	TI	
	SN54LS249	† TI	
	SN74LS249	TI	
BCD (Hexadecimal) to 7-Segment Decoder/Driver with Latch Active Low, Open Collector	9370C	Fairchild	
BCD to 7-Segment Decoder/Driver Active Low, Open Collector	MC4039	Motorola	
	N8T04	Signetics	120
	S8T04	† Signetics	
	SN54LS347	† TI	
	SN74LS347	TI	
	SN54LS447	† TI	
	SN74LS447	TI	
BCD to 7-Segment Decoder/Driver, Active Low, Open Collector, 15v Output	54LS47	† Fairchild	
	74LS47	Fairchild	130
	5447	† Fairchild	
	7447	Fairchild	
	54LS247	† Fairchild	

(Continued)

Function	Device	Source	Line
Display Drivers (Cont'd.)			
BCD to 7-Segment Decoder/Driver, Active Low, Open Collector, 15v Output (Cont'd.)	74LS247	Fairchild	
	9317BC	Fairchild	
	9317BM	† Fairchild	
	HD74LS47	Hitachi	140
	HD7447A	Hitachi	
	HD74LS247	Hitachi	
	M53247	Mitsubishi	
	M54406	Mitsubishi	
	SN54LS47	† Motorola	
	SN74LS47	Motorola	
	MC5447	† Motorola	
	MC7447	Motorola	
	SN54LS247	† Motorola	
	SN74LS247	Motorola	150
	DM5447A	† National	
	DM7447A	National	
	DM54LS47	† National	
	DM74LS47	National	
	DM54LS247	† National	
	DM74LS247	National	
	μPB7447	NEC America	
	5447	† Signetics	
	7447	Signetics	
	383A/C	Teledyne S	160
	383B/M	† Teledyne S	
	SN5447A	† TI	
	SN7447A	TI	
	SN54247	† TI	
	SN74247	TI	
	SN54LS47	† TI	
	SN74LS47	TI	
	SN54LS247	† TI	
	SN74LS247	TI	
	SN54LS347	† TI	170
	SN74LS347	TI	
	TD3447	Toshiba	
	TD34247	Toshiba	
BCD to 7-Segment Decoder/Driver, Active Low, Open Collector, 30v Output	5446	† Fairchild	
	7446	Fairchild	
	9317CC	Fairchild	
	9317CM	† Fairchild	
	HD7446A	Hitachi	180
	MC5446	† Motorola	
	MC7446	Motorola	
	DM5446A	† National	
	DM7446A	National	
	μPB7446	NEC America	
	5446	† Signetics	
	7446	Signetics	
	SN5446A	† TI	
	SN7446A	TI	
	SN54246	† TI	190
	SN74246	TI	
BCD to 7-Segment Decoder/Driver, for gas discharge displays	384A/C	Teledyne S	
	384B/M	† Teledyne S	
BCD to 7-Segment Latch/Decoder/Driver (CMOS with Bipolar Output)	F4511BC	Fairchild	
	F4511BM	† Fairchild	
	HD14511B	Hitachi	200
	SIL4511B	† Mitel	
	SIL4511BE	Mitel	
	MC14511BA	† Motorola	

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Values

INTERFACE–Display Drivers (Cont'd)

Display Drivers (Cont'd.)

BCD to 7-Segment Latch/Decoder/Driver (CMOS with Bipolar Output) (Cont'd.)

Device	Source
MC14513BA	† Motorola
MC14513BC	Motorola
MC14511BC	Motorola
CD4511BC	National
CD4511BM	† National
MSM561	OKI
MSM4511	OKI
CD4511B	† RCA
CD4511BE	RCA
SCL4511B	† SSS
SCL4511BE	SSS
CM4511B	† Solitron
CM4511BE	Solitron
TP4511B	TI
TC5002	Toshiba

BCD (Hexadecimal) to 7-Segment Latch/Decoder/Driver (CMOS with bipolar output)

Device	Source	
MC14495	**Motorola**	**(786)**

BCD to 7-Segment Latch/Decoder/Driver, output 1-16

Device	Source
SAB3211	Siemens

BCD to 7-Segment Decoder/Driver; for fluorescent displays

Device	Source
DI-250	Dionics

BCD to 7-Segment Decoder/Driver, for Liquid Crystal Displays

Device	Source
SIL4055B	† Mitel
SIL4055BE	Mitel
CD4055B	† RCA
CD4055BE	RCA
TC4055	Toshiba

BCD to 7-Segment Latch/Decoder/Driver, for Liquid Crystal Displays

Device	Source
MC14543BA	† Motorola
MC14543BC	Motorola

BCD to 7-Segment Latch/Decoder/Driver (Strobed Latch), for Liquid Crystal Displays

Device	Source	
LS7100	**LSI Comp**	**(494)**
SIL4056B	† Mitel	
SIL4056BE	Mitel	
MC14543BA	† Motorola	
MC14543BC	Motorola	
CD4056B	† RCA	
CD4056BE	RCA	
SCL4543A	SSS	
TC4056B	Toshiba	

7-Segment to BCD Converter/Driver

Device	Source
MM54C915	† National
MM74C915	National

4-Segment Liquid Crystal Display Driver

Device	Source
CD4054B	RCA
TC4054B	Toshiba

4-Digit Liquid Crystal Display Driver, Multiplexed BCD to LCD Decoder/Driver, AC Drive

Device	Source
ICM7211	Intersil
ICM7211A	Intersil
DF411	Siliconix
DF414	Siliconix

4-Digit LCD Driver; data and digit select code input latches for μP interface

Device	Source
ICM7211M	Intersil
ICM7211AM	Intersil

30-Bit LCD Driver/Register

Device	Source
MD4330B	† Mitel
MD4330BE	Mitel

(Continued)

Display Drivers (Cont'd.)

30-Bit LCD Driver/Register (Cont'd.)

Device	Source
MD4331B	† Mitel
MD4331BE	Mitel

Hex High Voltage Indicator Driver Open Collector (to 55v)

Device	Source
HD536	Harris

Hex TTL to LED Bulb Driver, with Latch

Device	Source
DS8859	National
DS8869	National

7-Digit/Segment MOS to Fluorescent Display Driver

Device	Source
XR2271	Exar

7-Digit MOS to Gas Discharge Display Driver

Device	Source
XR2272	Exar

4-Digit/Segment Fluorescent Display Driver

Device	Source
DI503	Dionics
DI504	Dionics

6-Digit/Segment Fluorescent Display Driver

Device	Source
DI508	Dionics
DI509	Dionics
UDN-6116	Sprague
UDN-6126	Sprague

8-Digit/Segment Fluorescent Display Driver

Device	Source	
DI513	Dionics	
DI514	Dionics	
DI514A	Dionics	
DI534A	Dionics	
XR6118	**Exar**	**(931)**
XR6128	Exar	
μPB249	NEC America	
UDN-6118	Sprague	
UDN-6128	Sprague	

12-Line Fluorescent Driver

Device	Source
SN75530	TI

4-Digit Gas Discharge Display Anode Driver

Device	Source
DI500	Dionics
DI502	Dionics
UDN-6144	Sprague

5-Digit Gas Discharge Display Anode Driver

Device	Source
UHD-490	† Sprague
UHP-490	Sprague

6-Digit Gas Discharge Display Anode Driver

Device	Source
DI505	Dionics
DI507	Dionics
DI603A	Dionics
DI604A	Dionics
DI605A	Dionics
DS7891	† National
DS8891	National
UDN-6164	Sprague
UHD-491	† Sprague
UHP-491	Sprague
UHP-495	Sprague
SN75481	TI

7-Digit Gas Discharge Display Anode Driver

Device	Source
MC3490	Motorola
MC3494	Motorola

8-Digit Gas Discharge Display Anode Driver

Device	Source
DI510	Dionics
DI512	Dionics
DI803A	Dionics
DI804A	Dionics
DI805A	Dionics
DS7887	† National
DS8887	National

(Continued)

Display Drivers (Cont'd.)

8-Digit Gas Discharge Display Anode Driver (Cont'd.)

Device	Source
DS7897	† National
DS8897	National
UDN-6184	Sprague

5-Segment Gas Discharge Display Cathode Driver

Device	Source
UHP-480	Sprague

7-Segment Gas Discharge Display Cathode Driver

Device	Source
DS7885	† National
DS8885	National
UHP-481	Sprague

7-Segment Gas Discharge Display Cathode Driver, with BCD Decoder

Device	Source
DD700	Beckman
DS7880	† National
DS8880	National
DS8884A	National
DS8980	National
DS8880	Signetics
SN75480	TI
SN75484	TI

7-Segment Gas Discharge Display Cathode Driver, with BCD Decoder, 8 outputs

Device	Source
DD704	Beckman

8-Segment Gas Discharge Display Cathode Driver

Device	Source
DI210	Dionics
DI220	Dionics
DI230	Dionics
DI240	Dionics
DI300	Dionics
DI302	Dionics
MC3491	Motorola
MC3492	Motorola
DS7889	† National
DS8889	National
UDN-7180	Sprague

4-Digit LED Driver, BCD or Binary to 7-Segment Decoder/Driver, data and digit select code latches for μP interface

Device	Source
ICM7212M	Intersil
ICM7212AM	Intersil
UDN-7183	Sprague
UDN-7184	Sprague
UDN-7186	Sprague
UHP-482	Sprague

4-Digit LED Driver, Mutliplexed BCD or Binary to 7-Segment Decoder/Driver

Device	Source
ICM7212	Intersil
ICM7212A	Intersil

LED Driver System, 8 Decade, 8x8 memory, Decoder (Versions either Hardwire or processor controlled; with 7 segment and digit drivers for either common anode or cathode LEDs; 2-6 V supply)

Device	Source
ICM7218A	Intersil
ICM7218B	Intersil
ICM7218C	Intersil
ICM7218D	Intersil
ICM7218E	Intersil

12-Digit Digitron Driver

Device	Source
EA7050	EA
EA7052	EA

4-Digit CMOS to LED Cathode Driver

Device	Source
DS8650	National
DS8658	National

7-Segment CMOS to LED Driver

Device	Source
DS8651	National

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Values

Bold face indicates additional data is provided on the page noted.

INTERFACE–Display Drivers (Cont'd)

Function	Device	Source	Line
Display Drivers (Cont'd.)			
7-Segment CMOS to LED Driver (Cont'd.)			
	DS8659	National	
6-Digit MOS to LED Cathode Driver			
	9664C	Fairchild	
	9664AC	Fairchild	
	9664BC	Fairchild	
	75492AC	Fairchild	
	75492BC	Fairchild	
	MC75492	Motorola	
	DS75492	National	10
	DS75494	National	
	DS8870	National	
	DS8877	National	
	DS8892	National	
	NE582	Signetics	
	D140	Siliconix	
	SN75492	TI	
	SN75492A	TI	
	SN75494	TI	
7-Digit MOS to LED Cathode Driver			20
	DS8844	National	
	SN75497	TI	
7-Digit MOS TO LED Cathode Driver, with low battery indicator			
	DS8866	National	
	DS8977	National	
8-Digit MOS to LED Cathode Driver			
	HD2903	Hitachi	
	DS8863	National	
	DS8865	National	30
	DS8871	National	
	DS8963	National	
9-Digit MOS to LED Cathode Driver			
	DS8855	National	
	DS8872	National	
	DS8973	National	
	DS8974	National	
	DS8975	National	
	DS8976	National	
	SN75498	TI	40
9-Digit MOS to LED Cathode Driver, with low battery indicator			
	DS8864	National	
	DS8873	National	
9-Digit MOS to LED Cathode Driver with shift register decoding			
	DS8874	National	
	DS8876	National	
	DS8879	National	
12-Digit MOS to LED Cathode Driver (for National Calculators)			50
	DS8868	National	
14-Digit Decoder/Driver			
	DS8665	National	
	DS8666	National	
14-Digit Decoder/Driver, with low battery indicator			
	DS7664	† National	
	DS8664	National	
4-Segment MOS to LED Anode Driver			
	75491AC	Fairchild	60
	75491BC	Fairchild	
	MC75491	Motorola	
	DS7895	† National	
	DS8895	† National	
	DS75491	National	

(Continued)

Function	Device	Source	Line
Display Drivers (Cont'd.)			
4-Segment MOS to LED Anode Driver (Cont'd.)			
	DS75493	National	
	SN75491	TI	
	SN75491A	TI	
	SN75493	TI	70
5-Segment MOS to LED Anode Driver			
	DS8861	National	
8-Segment MOS to LED Anode Driver			
	HD2902	Hitachi	
	MC676	Motorola	
	DS8867	National	
Bargraph LED Display Driver			
	LB1405	Sanyo	
	UAA170	Siemens	
	UAA180	Siemens	80
	U237	Telefunken	
	U247	Telefunken	
	TL489	TI	
	TL490	TI	
Bargraph (Gas Discharge) Display Driver			
	NE580	**Signetics (805)**	
Baragraph VF Display Driver			
	TL491	TI	
BCD-To-Decimal Decoder/Driver (Nixie Driver)			
	5441	† Fairchild	90
	7441	Fairchild	
	M53241	Mitsubishi	
	MC676	Motorola	
	DM5441A	† National	
	DM7441A	National	
	H158	SGS	
	382A/C	Teledyne S	
	382B/M	† Teledyne S	
BCD-To-Decimal Decoder/Driver with Blanking (for cold cathode indicator tubes)			100
	74141	Fairchild	
	HD74141	Hitachi	
	MC54141	† Motorola	
	MC74141	Motorola	
	DM54141	† National	
	DM74141	National	
	μPB74141	NEC America	
	SN74141	TI	
Plasma Display Controller and ASCII Keyboard Interface			110
	CY-300	Cybernetic	
5-line Plasma Display Axis Driver			
	DI5140	Dionics	
	DI5180	Dionics	
	DI5240	Dionics	
	DI5280	Dionics	
Quad AC Plasma Display Axis Driver			
	SN55426	† TI	
	SN75426	TI	
	SN55427	† TI	120
	SN75427	TI	
12-Line AC Plasma Display Axis Driver			
	SN75510	TI	
	SN75511	TI	
32-line AC Plasma Display Axis Driver			
	SN75500	TI	
	SN75501	TI	
	SN75502	TI	
	SN75503	TI	

Function	Device	Source	Line
Display Drivers (Cont'd.)			
BCD-To-Decimal Decoder/Driver (for lamps)			130
	380A/C	Teledyne S	
	380B/M	† Teledyne S	
	381A/C	Teledyne S	
	381B/M	† Teledyne S	
Lamp Driver; See below and various high current drivers under Interface-Memory and Peripheral Drivers			
Lamp Drivers (to 90 V, 2.0 A)			
	S75V01	**Siliconix (833)**	
	S75V03	**Siliconix (833)**	
Lamp Driver			140
	CSR301	Teledyne C	
4-Channel Incandescent Lamp Driver			
	CLD4	Teledyne C	
Display Controllers and Keyboard Interface: See Microprocessors-General Purpose			

† Military Temperature Range (−55° to 125°C)

* Typical Values

INTERFACE–Error Checking Circuits

Function	Max. Serial Data Rate MHz	Supply Voltage	Device	Source
Error Checking Circuits				
CRCC Generator	10	5	**9401C**	**Fairchild (1893,1894)**
			9401M	**† Fairchild (1893,1894)**
			9411C	**Fairchild (1893,1894)**
			9411M	**† Fairchild (1893,1894)**
	3	5	MC8500	Motorola
	10	60ma, 5v	8X01	Signetics
Deskew-Queue Register	3*	5	MC8520	Motorola
Error Detection/Correction Circuit (ECL)	—	-5.2	MC10163	Motorola
			MC10193	Motorola
Error Pattern Register	3	5	MC8501	Motorola
LRCC Data Register	3	5	MC8502	Motorola
Single Error Hamming Code Detector and Generator	—	5	MC4041	Motorola
Polynominal Generator	4*	5	MC8506	Motorola
Universal Polynomial Generator	3.5*	5	MC8503	Motorola
Universal Polynomial 4 Bit Generator	17*	5	MC8504	Motorola

† Military Temperature Range (−55° to 125°C)

* Typical Values

Bold face indicates additional data is provided on the page noted.

INTERFACE–Keyboard Encoder-Decoders

No. of Keys	No. of Output Bits	Code	Max. Clock Rate KHz	Supply Voltage	Comments	Device	Source
Keyboard Encoder-Decoders							
16	4	1 of 16	—	5	Strobe output, Key rollover output, 2 of 8 keyboard to binary encoder, one of four row inputs and column inputs (telephone key pads) give binary output, strobe.	**HD0165** MC14419	**Harris (731)** Motorola
		Binary	—	3-15	2 key rollover, 3 state output	MM54C922 MM74C922	† National National
20	5	Binary	—	3-15	2 key rollover, 3 state output	MM54C923 MM74C923	† National National
76	9	Mask Programmable	—	-(12-18), 5	To 4 independent 9-Bit codes per switch	MM5746	National
	10	Mask Programmable	—	-(12-18), 5	To 4 independent 10-Bit codes per switch	MM5745	National
88	8 plus Parity	Mask, Programmable	100	-12,5	Programmable parity, strobe width, strobe delay. Two key rollover. 8 x 11 matrix, 3 levels.	AY5-2376 M58609 KR2376	GI Mitsubishi SMC
90	9	Mask Programmable	200	-12,5	Programmable strobe width. 9 x 10 matrix. N or two key rollover. 4 levels. Repeat.	MM5740	National
	10	Mask Programmable	100	-12,5	9 x 10 matrix, 4 Mode, 2 or N key rollover	AY5-3600 KR3600	GI SMC
		External ROM Programmable	100	-12, 5	9 x 10 matrix, 4 mode, 2 or N key rollover	AY5-3600 - PRO KR3600-PRO	GI SMC
		Mask Programmable	100	-12,5	90 Key, 4 mode encoder, N key rollover	MP3802	Plessey
91	9 plus parity	Mask Programmable	100	-12,5	2 key rollover, 4 mode encoder	M58620	Mitsubishi
99	10	Mask Programmable	250	-12,5	9 x 9 matrix. N key rollover, 4 levels. No repeat.	EA2000 EA2007	EA EA
					99 Key, 4 Mode Encoder	EA2030	EA
112	10	Mask Programmable	66	5	112 bits for internal programming of function keys; 4 mode	AY3-4592	GI
128	9	Mask Programmable	100	5	16x8 matrix, three-state I/O, 2 or 3 key alarm	MSM3914A	OKI

† Military Temperature Range (−55° to 125°C)

* Typical Values

INTERFACE–Line Circuits

Line Drivers-Single Ended

No. Per Device	Output	Party Line	Power Supply	Comments	Device	Source
2	±4 to 6v	No	±9 to ±15	RS232, RS423, CCITT V.26, V.28	9636AC	Fairchild
					9636AM	† Fairchild
	±6v	No	±12	4 Input; RS232B, C; MIL188	N8T15	Signetics
	±8v	No	±12	RS232C; MIL188; CCITT V.24	75150	Fairchild
					M54650	Mitsubishi
					DS75150	National
					RM55150	† Raytheon
					SN75150	TI
	TTL	No	5,12	130 Ohm Twisted Pair	9621C	AMD
					9621M	† AMD
					9621	Fairchild
					9621M	† Fairchild
					RC9621	Raytheon
					RM9621	† Raytheon
	High Current	Yes	5	Emitter Follower for Coax/Twisted Pair	μA8T13C	Fairchild
					μA8T13M	† Fairchild
					75121	Fairchild
					MC8T13	Motorola
					DS55121	† National
					DS75121	National
					N8T13	Signetics
					S8T13	† Signetics
					N8T13	TI
					SN55121	† TI
					SN75121	TI
				Coax/Twisted Pair; IBM360, 370	μA8T23C	Fairchild
					μA8T23M	† Fairchild
					55123M	† Fairchild
					75123	Fairchild
					MC8T23	Motorola
					DS75123	National
					N8T23	Signetics
					N8T23	TI
					S8T23	† TI
					SN75123	TI
3	±6v	No	±12	RS232B/C, CCITT, MIL188	9616C	AMD
					9616M	† AMD
					9616	Fairchild
					9616E	Fairchild
					9616M	† Fairchild
	High Current	No	5	IBM360	HD2904	Hitachi
4	±4 to 6V	Yes	±5	RS423, Three-State	AM26LS29C	AMD
			±5.5	RS423, Three-state	AM26LS29M	† AMD
		No	±5	RS423, RS422 with mode control	AM26LS30C	AMD
					DS3691C	National
			±5.5	RS423, RS422 with mode control	AM26LS30M	† AMD
					DS3691M	National
	±6 to 9v	No	±9 to ±15	RS232C, CCITT V.24	1488	AMD
					XR1488	Exar
					μA1488	Fairchild
					HD75188	Hitachi
					MC1488	Motorola
					DS1488	National
					RC1488	Raytheon
					MC1488	Signetics
					SG1488	Silicon G
					MC1488	TI
					SN75188	TI
	±5 to ±7	No	±12	RS232C, CCITT V.24	AM2616C	AMD
					AM2616M	† AMD
	TTL	No	5	Active Pull-Up	AM2614C	AMD
					AM2614M	† AMD
		Yes	5	Three-State	RC8T09	Raytheon

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Values

Bold face indicates additional data is provided on the page noted.

INTERFACE–Line Circuits (Cont'd)

No. Per Device	Output	Party Line	Power Supply	Comments	Device	Source
Line Drivers-Single Ended						**(Cont'd.)**
4	TTL	Yes	5	Three-State		(Cont'd.)
					RM8T09	† Raytheon
					N8T09	Signetics
					S8T09	† Signetics
				2-Input NAND, 80 ma	96101C	Fairchild
					96101M	† Fairchild
				4-Input AND, NAND; Three-State	DM7831	† AMD
					DM8831	AMD
					DS7831	† National
					DS8831	National
					DS7831	† TI
					DS8831	TI
				DS7831 w/o Vcc Clamp	DS7832	† National
					DS8832	National
					DS7832	† TI
					DS8832	TI
6	NTDS	No	5, -15	NTDS	MOA-268B	† Interdesign
8	TTL	Yes	5	Three-State (Also see index for 74S244, 74LS244, 67S304, 67LS304)	AM25LS241C	AMD
					AM25LS241M	† AMD
					SN54LS241	† AMD
					SN74LS241	AMD
					SN54S241	† AMD
					SN74S241	AMD
					AM25LS244C	AMD
					AM25LS244M	† AMD
					SN54LS244	† AMD
					SN74LS244	AMD
					SN54S244	† AMD
					SN74S244	AMD
					54LS241	† Fairchild
					74LS241	Fairchild
					54LS44	† Fairchild
					74LS244	Fairchild
					54LS541	† Fairchild
					74LS541	Fairchild
					54LS241	**† MMI (768)**
					74LS241	**MMI (768)**
					54S241	**† MMI (768)**
					74S241	**MMI (768)**
					54LS244	**† MMI (768)**
					74LS244	**MMI (768)**
					54S244	**† MMI (768)**
					74S244	**MMI (768)**
					57LS301	**† MMI (768)**
					67LS301	**MMI (768)**
					57S301	**† MMI (768)**
					67S301	**MMI (768)**
					57LS304	**† MMI (768)**
					67LS304	**MMI (768)**
					57S304	**† MMI (768)**
					67S304	**MMI (768)**
					SN54LS241	† Motorola
					SN74LS241	Motorola
					SN54LS244	† Motorola
					SN74LS244	Motorola
					SN54LS541	† Motorola
					SN74LS541	Motorola
					9LS241C	**Raytheon (525)**
					9LS241M	**† Raytheon (525)**
					25LS241C	**† Raytheon (525)**
					25LS241M	**Raytheon (525)**
					54LS241	**† Raytheon (525)**
					74LS241	**Raytheon (525)**
					9LS244C	**Raytheon (525)**
					9LS244M	**† Raytheon (525)**
					25LS244C	**Raytheon (525)**

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Values

INTERFACE–Line Circuits (Cont'd)

No. Per Device	Output	Party Line	Power Supply	Comments	Device	Source	
Line Drivers-Single Ended							**(Cont'd.)**
8	TTL	Yes	5	Three-State (Also see index for 74S244, 74LS244, 67S304, 67LS304)			(Cont'd.)
					25LS244M	**† Raytheon**	**(525)**
					54LS244	**† Raytheon**	**(525)**
					74LS244	**Raytheon**	**(525)**
					74LS241	Signetics	
					74LS244	Signetics	
					SN54LS241	† TI	
					SN74LS241	TI	
					SN54S241	† TI	
					SN74S241	TI	
					SN54LS244	† TI	
					SN74LS244	TI	
				Three-State, Inverting	AM25LS240C	AMD	
					AM25LS240M	† AMD	
					SN54LS240	† AMD	
					SN74LS240	AMD	
					SN54S240	AMD	
					SN74S240	AMD	
					54LS240	† Fairchild	
					74LS240	Fairchild	
					54LS540	† Fairchild	
					74LS540	Fairchild	
					54LS240	**† MMI**	**(768)**
					74LS240	**MMI**	**(768)**
					54S240	**† MMI**	**(768)**
					74S240	**MMI**	**(768)**
					57LS300	**† MMI**	**(768)**
					67LS300	**MMI**	**(768)**
					57S300	**† MMI**	**(768)**
					67S300	**MMI**	**(768)**
					57LS306	**† MMI**	**(768)**
					67LS306	**MMI**	**(768)**
					57S306	**† MMI**	**(768)**
					67S306	**MMI**	**(768)**
					57LS307	**† MMI**	**(768)**
					67LS307	**MMI**	**(768)**
					57S307	**† MMI**	**(768)**
					67S307	**MMI**	**(768)**
					SN54LS240	† Motorola	
					SN74LS240	Motorola	
					SN54LS540	† Motorola	
					SN74LS540	Motorola	
					9LS240C	**Raytheon**	**(522)**
					9LS240M	**† Raytheon**	**(522)**
					25LS240C	**Raytheon**	**(522)**
					25LS240M	**† Raytheon**	**(522)**
					54LS240	**† Raytheon**	**(522)**
					74LS240	**Raytheon**	**(522)**
					74LS240	Signetics	
					SN54LS240	† TI	
					SN74LS240	TI	
					SN54S240	† TI	
					SN74S240	TI	
Line-Drivers - Differential							
2	High Current TTL						
		No	5	40 ma, Active Pull-up/Pull-down	9612C	Fairchild	
					9612M	† Fairchild	
				50 ma, Active Pull-up/Pull-down	9612EC	Fairchild	
				40 ma, Open Collector/Active Pull-up	9614C	AMD	
					9614M	† AMD	
					9614C	Fairchild	
					9614M	† Fairchild	
					DS55114	† National	
					DS75114	National	

(Continued)

† Military Temperature Range (−55° to 125°C) * Typical Values

Bold face indicates additional data is provided on the page noted.

INTERFACE–Line Circuits (Cont'd)

Line-Drivers - Differential (Cont'd.)

No. Per Device	Output	Party Line	Power Supply	Comments	Device	Source
2	High Current TTL					
		No	5	40 ma, Open Collector/Active Pull-up		(Cont'd.)
					9614C	TI
					SN55114	† TI
					SN75114	TI
		Yes	5	40 ma, Open Collector/Active Pull-up, Three-State	DS55113	† National
					DS75113	National
					SN55113	† TI
					SN75113	TI
		No	5	40 ma, 4-Input AND, NAND	DM7830	† AMD
					DM8830	AMD
					54S140	† Fairchild
					74S140	Fairchild
					HD74S140	Hitachi
					DM74S140	National
					DS7830	† National
					DS8830	National
					DS7830	† Signetics
					DS8830	Signetics
					54S140	† Signetics
					74S140	Signetics
					DS7830	† TI
					DS8830	TI
					SN54S140	† TI
					SN74S140	TI
					SN55183	† TI
					SN75183	TI
		Yes	5	40 ma, 4-Input AND, NAND; Three-State	DM7831	† AMD
					DM8831	AMD
					DS7831	† National
					DS8831	National
					DS7831	† TI
					DS8831	TI
				DS7831 w/o Vcc Clamp	DM7832	† AMD
					DM8832	AMD
					DS7832	† National
					DS7832	† TI
					DS8832	TI
		No	5	40 ma, RS422	9638C	Fairchild
					9638M	† Fairchild
					SN55128	† TI
					SN75158	TI
		Yes	5	40 ma, RS422, Three-State	9634C	Fairchild
					9634M	† Fairchild
					DS8832	National
					SN75159	TI
	±3v	Yes	±5	RS422 at low data rates, RS423	AM26LS30C	AMD
			±5.5	RS422 at low data rates, RS423	AM26LS30M	† AMD
	High Current CMOS					
		No	3-15	CMOS 50 ma, 4-Input AND, NAND	MM78C30	† National
					MM88C30	National
	3.5 ma	Yes	±5	Twisted Pair; Level Shifting	SN55109	† AMD
					SN75109	AMD
					55109	† Fairchild
					75109	Fairchild
					HD75109	Hitachi
					MC75109	Motorola
					DS55109	† National
					DS75109	National
					RM55109	† Raytheon
					SN55109A	† TI
					SN75109A	TI

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Values

INTERFACE–Line Circuits (Cont'd)

No. Per Device	Output	Party Line	Power Supply	Comments	Device	Source
Line-Drivers - Differential						**(Cont'd.)**
2						(Cont'd.)
	6.5ma	Yes	±5	Twisted Pair Level Shifting	SN55110	† AMD
					SN75110	AMD
					55110A	† Fairchild
					75110A	Fairchild
					HD75110	Hitachi
					MC75110	Motorola
					DS55110	† National
					DS75110	National
					RM55110	† Raytheon
					SN55110A	† TI
					SN75110A	TI
	18 ma	Yes	±5	Higher current 75110	75112	Fairchild
					SN75112	TI
3	2 ma	Yes	5	Constant Current	HD545	Harris
4	11 ma	Yes	±5	Quad 75110	MC3453A	Motorola
	High Current TTL					
		No	5	50 ohm lines	74128	Signetics
					SN74128	TI
				75 ohm lines	54128	† Signetics
					SN54128	† TI
		Yes	5	Three-State	DS1688	† National
					DS3688	National
					N8T100	Signetics
					N8T101	Signetics
				RS-422, RS-423, Three-State	MC3487	Motorola
					DS3487	National
	20 ma	Yes	5	RS-422, Three-State	AM26LS31C	AMD
					AM26LS31M	† AMD
					DM26LS31C	† National
					DM26LS31M	National
					AM26LS31C	TI
					AM26LS31M	† TI
	40 ma	Yes	5	RS-422, Fed. 1020, Three-State	SN75151	TI
					SN75153	TI
	High Current CMOS					
		No	3-15	CMOS, 25 ma	MM78C29	† National
					MM88C29	National

See also Drivers under digital logic families

† Military Temperature Range (−55° to 125°C) * Typical Values

Bold face indicates additional data is provided on the page noted.

INTERFACE–Line Circuits (Cont'd)

No. Per Device	Receiver Input Threshold	Common Mode Voltage	Supply Voltage	Comments	Device	Source
Line Receivers - Single Ended						
2	Ref ±0.1v		5	Ext. Reference Adjustable from 1.5 to 3.5v	MC75140	Motorola
					SN55140	†TI
					SN75140	TI
					SN55141	†TI
					SN75141	TI
				Ext. Ref. Adj. 1.5 to 3.5v with optional internal 2.5v Reference	SN55142	†TI
					SN75142	TI
					SN55143	†TI
					SN75143	TI
	0.4 to 2.4	±15	5	Differential Input, Single Ended Data	AM2615C	AMD
					AM2615M	†AMD
	±2.0		5	RS232B	DS7822	†National
					DS8822	National
3	0.7 to 1.7		5	Hysteresis, IBM 360/370	μA8T24C	Fairchild
					μA8T24M	†Fairchild
					55124	†Fairchild
					75124	Fairchild
					MC8T24	Motorola
					DS75124	National
					N8T24	Signetics
	0.75 to 2.25		5	Hysteresis, RS232C, CCITT V.24	9617C	AMD
					9617M	†AMD
					9617C	Fairchild
	0.8 to 2.0 v		5	Hysteresis, High-Speed	μA8T14C	Fairchild
					μA8T14M	†Fairchild
					55122	†Fairchild
					75122	Fairchild
					MC8T14	Motorola
					DS55122	†National
					DS75122	National
					N8T14	Signetics
					S8T14	†Signetics
					SN55122	†TI
					SN75122	TI
		0.86 to 2.40	5	High Speed	HD2915	Hitachi
		1.15 to 1.55	5	IBM 360	HD2905	Hitachi
4	±3/0.8 to 3		5 or 12	RS232C, Hysteresis, Fail Safe Option	55154	†Fairchild
					75154	Fairchild
					M54654	Mitsubishi
					DS75154	National
					RM55154	†Raytheon
					RC75154	Raytheon
					SG55154	†Silicon G
					SG75154	Silicon G
					SN75154	TI
	0.75 to 1.5v		5	RS232C, Programmable Threshold, Hysteresis	1489	AMD
					μA1489	Fairchild
					HD75154	Hitachi
					M54655	Mitsubishi
					MC1489	Motorola
					DS1489	National
					RC1489	Raytheon
					MC1489	Signetics
					SG1489	Silicon G
					SN75189	TI
	0.75 to 2.25		5	RS232C, Programmable Threshold, wider hysteresis than 1489	1489A	AMD
					XR1489A	Exar
					μA1489A	Fairchild
					HD75189	Hitachi
					M54656	Mitsubishi
					MC1489A	Motorola
					DS1489A	National
					RC1489A	Raytheon
					MC1489A	Signetics

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Values

INTERFACE–Line Circuits (Cont'd)

No. Per Device	Receiver Input Threshold	Common Mode Voltage	Supply Voltage	Comments	Device	Source
Line Receivers - Single Ended						**(Cont'd.)**
4	0.75 to 2.25		5	RS232C, Programmable Threshold, wider hysteresis than 1489		(Cont'd.)
					SG1489A	Silicon G
					SN75189A	TI
	0.97 to 2.65		5	Hysteresis, 120 Ohm System	DS7836	† National
	1.05 to 2.5		5	Hysteresis, 120 Ohm System	DS8836	National
	1.2 to 1.8		5	120 Ohm System, No Hysteresis, NOR Input	DS7640	† National
	1.25 to 2.25		5	RS-232C	AM2617	AMD
	1.3 to 1.7		5	120 Ohm System, No Hysteresis, NOR Input	DS8640	National
	1.5 to 2.0		5	120 Ohm System, Hysteresis, NOR Input	N8T380	Signetics
	1.7		5	No Hysteresis, NOR Input	96106	Fairchild
	5 to 7.5		15	Hysteresis, Interface to CMOS	367A	Teledyne S
					367M	† Teledyne S
				Hysteresis, Open Collector, Interface to CMOS	368A	Teledyne S
					368M	† Teledyne S
	5.5 to 8		12	Hysteresis, Interface to CMOS	367B	Teledyne S
					367C	† Teledyne S
				Hysteresis, Open Collector, Interface to CMOS	368B	† Teledyne S
					368C	Teledyne S
6	0.97 to 2.65		5	Hysteresis, 120 Ohm System	DS7837	† National
	1.05 to 2.50		5	Hysteresis, 120 Ohm System	MC3437	Motorola
					DS8837	National
					N8T37	Signetics
	6	-1 to -4.5/-1.5 to -13	5	NTDS	MOB-272	† Interdesign
7	0.7 to 1.7		5	IBM360/370	SN75125	TI
					SN75127	TI
8	0.7 to 1.7		5	IBM360/370	SN75128	TI
					SN75129	TI
Also see Line Receivers-Differential						
Line Receivers - Differential						
2	±0.35/0.3 to 3		5	Adj. RS232B,C, MIL-188	N8T16	Signetics
	±0.2/0.3	±10/15	5	Twisted Pair, ±15v CMV, Response Control	DS78LS120	† National
					DS88LS120	National
	±0.2/0.5	±7/15	5	RS232, RS422/3	9637C	Fairchild
					9637M	† Fairchild
					SN55157	† TI
					SN75157	TI
	±0.5/2	±0/15	5,12	±15v CMV	9620M	† AMD
					9620M	† Fairchild
		±0/12	5,12	±12 v CMV	9620C	AMD
					9620C	Fairchild
	±0.3/0.3	±0/15	5	±15v CMV, Response Control	DS78L20	† National
					DS88L20	National
	±0.5/1	±0/15	5	±15V CMV, Response Control	9615C	AMD
					9615M	† AMD
					9615C	Fairchild
					9615M	† Fairchild
					SN55115	† TI
					SN75115	TI
					DM7820	† AMD
		±10/15	5	Twisted Pair, ±15v CMV, Response Control	DM8820	AMD
					DS78C20	† National
					DS88C20	National
					DS7820	† National
					DS8820	National
					DS7820	† Signetics

(Continued)

† Military Temperature Range (−55° to 125°C) * Typical Values

Bold face indicates additional data is provided on the page noted.

INTERFACE–Line Circuits (Cont'd)

Line Receivers - Differential (Cont'd.)

No. Per Device	Receiver Input Threshold	Common Mode Voltage	Supply Voltage	Comments	Device	Source
						(Cont'd.)
2	±0.5/1	±10/15	5	Twisted Pair, ±15v CMV, Response Control	DS8820	Signetics
		±5/15	5	±15v CMV	9613C	Fairchild
					9613M	† Fairchild
		±3/15	5	Twisted Pair, ±3/15 v CMV, Response Control	DM7820A	† AMD
					DM8820A	AMD
					DS7820A	† National
					DS8820A	National
					DS7820A	† Signetics
					DS8820A	Signetics
					DS7820	† TI
					DS8820	TI
					SN55182	† TI
					SN75182	TI
	±0.5/3	±25	±12	Adjusts RS232C/MIL-188, ±25 v CMV, Hysteresis	9627C	Fairchild
					9627M	† Fairchild
					SN75152	TI
	±2	±7.5	-10,5	130 Ohm Termination	9622C	Fairchild
					RC9622	Raytheon
		±10	-10,5	130 Ohm Termination	9622M	† Fairchild
					RM9622	† Raytheon
	±0.010	±3	±5	10 mv, MOS Sense, Active Pull-up	SN75207	AMD
					55207	† Fairchild
					75207	Fairchild
					DS75207	National
					75S207	Signetics
					SN75207	TI
				75207 with Diode Protected Input Stage	SN75207B	TI
				10 mv, MOS Sense, Three-State	DS3604	AMD
					DS3604	National
				10 mv, MOS Sense, Open Collector	SN75208	AMD
					55208	† Fairchild
					75208	Fairchild
					DS75208	National
					75S208	Signetics
					SN75208	TI
				75208 with Diode Protected Input Stage	SN75208B	TI
	±0.025	±3	±5	25 mv, Active Pull-up	55107A	† Fairchild
					75107A	Fairchild
					HD75107A	Hitachi
					MC55107	† Motorola
					MC75107	Motorola
					DS55107	† National
					DS75107	National
					RC75107A	Raytheon
					RM55107A	† Raytheon
					75S107	Signetics
					SN55107A	† TI
					SN75107A	TI
				25 mv, Three-State 55107	DS1603	† AMD
					DS3603	AMD
					DS1603	† National
					DS3603	National
				25 mv, Open Collector	55108A	Fairchild
					75108A	Fairchild
					HD75108A	Hitachi
					MC55108	† Motorola
					MC75108	Motorola
					DS55108	† National
					DS75108	National
					RC75108A	Raytheon
					RM55108A	† Raytheon

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Values

INTERFACE–Line Circuits (Cont'd)

No. Per Device	Receiver Input Threshold	Common Mode Voltage	Supply Voltage	Comments	Device	Source
Line Receivers - Differential						**(Cont'd.)**
2	±0.025	±3	±5	25 mv, Open Collector		(Cont'd.)
					75S108	Signetics
					SN55108A	† TI
					SN75108A	TI
				55107A with Diode Protected Input Stage	SN55107B	† AMD
					SN75107B	AMD
					55107B	† Fairchild
					75107B	Fairchild
					DS55107	† National
					DS75107	National
					SN55107B	† TI
					SN75107B	TI
				55108A with Diode Protected Input Stage	SN55108B	† AMD
					SN75108B	AMD
					551088B	† Fairchiid
					75108B	Fairchild
					DS55108	† National
					DS75108	National
					SN55108B	† TI
					SN75108B	TI
3	±0.075		±5	100 Ohm Twisted Pair, Shielded	HD548	Harris
	±1.5 ma		±5	100 Ohm Twisted Pair, Shielded	HD546	Harris
					HD549	Harris
4	±0.025	±3	±5	Four 75107, Active Pull-Up	MC3450	Motorola
					DS3650	National
				Four 75108, Open Collector	MC3452	Motorola
					DS3652	National
	±0.2	±3	5	Three-state, RS422/423	MC3486	Motorola
					DS3486	National
		±7	5	Three-State, RS-422/423	AM26LS32C	AMD
					AM26LS32M	† AMD
					DM26LS32C	National
					DM26LS32M	† National
					AM26LS32C	TI
					AM26LS32M	† TI
		±15	5	50 mv Hysteresis	DS1689	† National
					DS3689	National
					DS1690	† National
					DS3690	National
					DS3651	National
	±0.5	±15	5	Three-State	AM26LS33C	AMD
					AM26LS33M	† AMD
					DM26LS33C	National
					DM26LS33M	† National
					AM26LS33C	TI
					AM26LS33M	† TI

See also Receivers-listed under Digital-ECL and Digital-HNIL/HTL Miscellaneous sections

† Military Temperature Range (−55° to 125°C) * Typical Values

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INTERFACE–Line Circuits (Cont'd)

No. Per Device	Receiver Input Threshold	Output	Supply Voltage	Comments	Device	Source
Line Transceivers - Single Ended						
2	MOS/TTL	MOS/TTL	5	Transceiver/Port Controller	N8T30	Signetics
4	0.6 to 2.0	TTL	5	General Purpose Interface Bus, Open Collector, for MOS input	MC3446A	Motorola
					MC3446	TI
	0.7 to 2.0	TTL	5	Three-State, Hysteresis	AM25LS242M	† AMD
					AM25LS243M	† AMD
					SN54S242	† AMD
					SN54S243	† AMD
					SN54LS242	† AMD
					SN54LS243	† AMD
					54LS242	† Fairchild
					54LS243	† Fairchild
					SN54LS242	† Motorola
					SN54LS243	† Motorola
					9LS242M	**† Raytheon (528)**
					25LS242M	**† Raytheon (528)**
					54LS242	**† Raytheon (528)**
					9LS243M	**† Raytheon (528)**
					25LS243M	**† Raytheon (528)**
					54LS243	**† Raytheon (528)**
					SN54LS242	† TI
					SN54LS243	† TI
				Three-State, Bus Transceiver	AM2915AM	† AMD
					2915AM	† MMI
					MC2915AM	† Motorola
					AM2915AM	† Raytheon
				Three-State, Bus Transceiver, Parity Generator/Checker	AM29176AM	† AMD
					AM2917AM	† AMD
					2916AM	† MMI
					2917AM	† MMI
					MC2916AM	† Motorola
					MC2917AM	† Motorola
					AM2916AM	† Raytheon
					AM2917AM	† Raytheon
	0.8 to 1.8	TTL/MOS	5	General Purpose Inteface Bus, Bidirectional Bus Tranceiver, three-state	MC3448A	Motorola
	0.8 to 2.0	TTL	5	Three-State, Bus Transceiver	AM2915AC	AMD
					F2915AC	Fairchild
					9425	Fairchild
					2915AC	MMI
					MC2915AC	Motorola
					µPB2915A	NEC Micro
					AM2915AC	Raytheon
				Three-State, Bus Transceiver, Parity Generator/Checker	AM2916AC	AMD
					AM2917AC	AMD
					F2916AC	Fairchild
					9426	Fairchild
					F2917AC	Fairchild
					9427	Fairchild
					2916AC	MMI
					2917AC	MMI
					MC2916AC	Motorola
					MC2917AC	Motorola
					µPB2916A	NEC Micro
					µPB2917A	NEC Micro
					AM2916AC	Raytheon
					AM2917AC	Raytheon
				General Purpose Interface Bus, Open Collector, 100 ma output	MC3440A	Motorola
					MC3441A	Motorola
					MC3442	Motorola
					MC3443A	Motorola
					DS8641	Motorola
					DS7641	† National
					DS8641	National
					MC3443	TI
				General Purpose Bus, Open Collector, 100 ma,for 50 ohm system	DS8642	National
				Three-State (Inverting)	N8T26	AMD

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Values

INTERFACE–Line Circuits (Cont'd)

No. Per Device	Receiver Input Threshold	Output	Supply Voltage	Comments	Device	Source	
Line Transceivers - Single Ended							**(Cont'd.)**
4	0.8 to 2.0	TTL	5	Three-State (Inverting)			(Cont'd.)
					S8T26	† AMD	
					8T26	Fairchild	
					HD268T26	Hitachi	
					MC6880	Motorola	
					MC8T26A	Motorola	
					DS8T26A	National	
					DS8T26AM	† National	
					N8T26A	Signetics	
					N8T126	**Signetics**	**(2297)**
					S8T126	**† Signetics**	**(2297)**
					N8T127	**Signetics**	**(2297)**
					S8T127	**† Signetics**	**(2297)**
					SN75136	TI	
				Three-State(Non-Inverting)	N8T28A	AMD	
					S8T28A	† AMD	
					8T28	Fairchild	
					MC6889	Motorola	
					MC8T28	Motorola	
					DS8T28	National	
					DS8T28M	† National	
					N8T28	Signetics	
					N8T128	**Signetics**	**(2297)**
					S8T128	**† Signetics**	**(2297)**
					N8T129	**Signetics**	**(2297)**
					S8T129	**† Signetics**	**(2297)**
				Three-State, Hysteresis	AM25LS242C	AMD	
					SN74LS242	† AMD	
					SN74S242	AMD	
					AM25LS243C	AMD	
					SN74S243	AMD	
					SN74LS243	AMD	
					74LS242	Fairchild	
					74LS243	Fairchild	
					SN74LS242	Motorola	
					SN74LS243	Motorola	
					9LS242C	**Raytheon**	**(528)**
					25LS242C	**Raytheon**	**(528)**
					74LS242	**Raytheon**	**(528)**
					9LS243C	**Raytheon**	**(528)**
					25LS243C	**Raytheon**	**(528)**
					74LS243	**Raytheon**	**(528)**
					74LS242	Signetics	
					74LS243	Signetics	
					SN74LS242	TI	
					SN74LS243	TI	
				Three-State, dual rank latches	SN54S266	† TI	
					SN74S226	TI	
	0.97 to 2.65	TTL	5	Open Collector, 1 v Hysteresis	DS7838	† AMD	
					DS7838	† National	
	1.05 to 2.50	TTL	5	Open Collector, 1 v Hysteresis	DS8838	AMD	
					MC3438	Motorola	
					DS8838	National	
					N8T38	Signetics	
	1.4 to 2.05	TTL	5	Open Collector, Hysteresis	AM26S12AM	† AMD	
					AM26S12AC	AMD	
	1.5 to 2.4	TTL	5	2-Input, Open Collector 100ma Drivers	AM2905M	† AMD	
					2905M	† MMI	
					MC2905M	† Motorola	
					AM2905M	† Raytheon	
				2-Input, Open Collector 100ma Drivers, Parity Generator/Checker	AM2906M	† AMD	
					2906M	† MMI	
					MC2906M	† Motorola	
					AM2906M	† Raytheon	

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† Military Temperature Range (−55° to 125°C) * Typical Values

Bold face indicates additional data is provided on the page noted.

INTERFACE–Line Circuits (Cont'd)

Line Transceivers - Single Ended (Cont'd.)

No. Per Device	Receiver Input Threshold	Output	Supply Voltage	Comments	Device	Source
						(Cont'd.)
4	1.5 to 2.4	TTL	5	Open Collector, 100ma output, Parity Generator/Checker	AM2907M	† AMD
					2907M	† MMI
					MC2907M	† Motorola
					AM2907M	† Raytheon
	1.5 to 3.2	TTL	5	Open Collector, 100 ma output	SG55138	† Silicon G
					SN55138	† TI
	1.6 to 1.8	TTL	5	Open Collector, Hysteresis	AM26S12M	† AMD
					AM26S12C	AMD
	1.6 to 2.3	TTL	5	2-Input, Open Collector 100 ma Drivers	AM2905C	AMD
					F2905C	Fairchild
					9415	Fairchild
					2905C	MMI
					MC2905C	Motorola
					µPB2905A	NEC Micro
					AM2905C	Raytheon
				2-Input, Open Collector, 100 ma Drivers, Parity Generator/Checker	AM2906C	AMD
					F2906C	Fairchild
					9416	Fairchild
					2906C	MMI
					MC2906C	Motorola
					µPB2906A	NEC Micro
					AM2906C	Raytheon
				Open Collector, 100 ma output, Parity Generator/Checker	AM2907C	AMD
					F2907C	Fairchild
					9417	Fairchild
					2907C	MMI
					MC2907C	Motorola
					µPB2907A	NEC Micro
					AM2907C	Raytheon
	1.6 to 2.4	TTL	5	Open Collector, 100 ma output	AM26S10M	† AMD
					AM26S11M	† AMD
					9640M	† Fairchild
					9641M	† Fairchild
					DM26S10M	† National
					DM26S11M	† National
					AM26S10M	† TI
					AM26S11M	† TI
				Open Collector, 100 ma, Hysteresis	9642M	† Fairchild
	1.75 to 2.25	TTL	5	Open Collector, 100 ma output	AM26S10C	AMD
					AM26S11C	AMD
					9640C	Fairchild
					9641C	Fairchild
					MC26S10	Motorola
					MC26S11	Motorola
					DM26S10C	National
					DM26S11C	National
					AM26S10C	TI
					AM26S11C	TI
				Open Collector, 100 ma, Hysteresis	9642C	Fairchild
	1.8 to 2.9	TTL	5	Open Collector, 100 ma output	SG75138	Silicon G
					SN75138	TI
	1.05 to 2.50	TTL	5	Three-State, T/R Disables, Hysteresis	DS7833	† National
					DS8833	National
				Inverting 7833/8833	DS7835	† National
					DS8835	National
				Three-State, NOR Gate, Transmit Disable, Hysteresis	DS7839	† National
					DS8839	National
				Inverting 7839/8839	DS7834	† National
					DS8834	National
					N8T34	Signetics
8	CMOS	TTL	5	Bidirectional Bus Driver, Three-State	MD4245A	† Mitel

(Continued)

† Military Temperature Range (−55° to 125°C) * Typical Values

INTERFACE–Line Circuits (Cont'd)

No. Per Device	Receiver Input Threshold	Output	Supply Voltage	Comments	Device	Source	
Line Transceivers - Single Ended							**(Cont'd.)**
8	CMOS	TTL	5	Bidirectional Bus Driver, Three-State			(Cont'd.)
					MD4245AE	Mitel	
	TTL	TTL	5	Bidirectional Bus Transceiver, Three-State	AM8304	AMD	
					DP8304	National	
	0.7 to 2.0	TTL	5	Bidirectional Bus Transceiver, Open Collector	SN54LS641	† Motorola	
					SN54LS642	† Motorola	
					SN54LS641	† TI	
					SN54LS642	† TI	
					SN54LS644	† TI	
				Bidirectional Bus Transceiver, Three State	SN54LS245	† AMD	10
					54LS245	† Fairchild	
					54LS245	**† MMI** (774)	
					57LS305	**† MMI** (774)	
					57LS310	**† MMI** (774)	
					SN54LS245	† Motorola	
					SN54LS640	† Motorola	
					SN54LS645	† Motorola	
					SN54LS245	† TI	
					SN54LS640	† TI	
					SN54LS643	† TI	20
					SN54LS645	† TI	
	0.8 to 2.0	TTL	5	Bidirectional Bus Transceiver, Open Collector	SN74LS641	Motorola	
					SN74LS642	Motorola	
					SN74LS641	TI	
					SN74LS641-1	TI	
					SN74LS642	TI	
					SN74LS642-1	TI	
					SN74LS644	TI	
					SN74LS644-1	TI	
				Bidirectional Bus Transceiver, Three State	SN74LS245	AMD	30
					74LS245	Fairchild	
					74LS245	**MMI** (774)	
					67LS305	**MMI** (774)	
					67LS310	**MMI** (674)	
					SN74LS245	Motorola	
					SN74LS640	Motorola	
					SN74LS645	Motorola	
					74LS245	Signetics	
					N8T125	Signetics	
					SN74LS245	TI	40
					SN74LS640	TI	
					SN74LS640-1	TI	
					SN74LS643	TI	
					SN74LS643-1	TI	
					SN74LS645	TI	
					SN74LS645-1	TI	
				General Purpose Interface Bus	SN75160	TI	
					SN75161	TI	
					SN75162	TI	
Line Transceivers - Differential							
1	±0.5/±1v	TTL	5	Independent Three-State 55113 Driver and 55115 Receiver	SN55116	† TI	50
					SN75116	TI	
				Three-State 8 Pin, 40 ma	SN55117	† TI	
					SN75117	TI	
				Same as 55116 with Three-State Receiver	SN55118	† TI	
					SN75118	TI	
				Same as 55117 with Three-State Receiver	SN55119	† TI	
					SN75119	TI	

† Military Temperature Range (−55° to 125°C) * Typical Values

Bold face indicates additional data is provided on the page noted.

INTERFACE–Memory and Peripheral Drivers

Memory & Peripheral Drivers

Function	Device	Source	Line
Dual CCD Memory Driver, with enable inputs	SN75430	TI	
Dual CCD Memory Driver, with enable inputs and protect	SN75431	TI	
MOS Dynamic Memory, Address Refresh Logic Circuitry	3222	Intel	
	MC8505	Motorola	
MOS Dynamic Memory, 4k Address Multiplexer and Refresh Counter	**96LS32**	**Fairchild (479)**	10
	96S32	**Fairchild (479)**	
	3232	Intel	
	MC3232A	Motorola	
MOS Dynamic Memory Interface, Microprocessor to 16K RAM	MC3480	Motorola	
MOS Dynamic Memory, 16k Address Multiplexer and Refresh Counter	3242	Intel	20
Clock Generator/Oscillator, to 10 MHz, 8 and 1 Divider, for Microprocessors	ICM7209	† Intersil	
MOS Clock Driver	MH0007	† National	
	MH0012	† National	
	MH0007C	National	
	MH0012C	National	
Dual MOS Clock Driver	0026	† AMD	30
	0026C	AMD	
	0056	† AMD	
	0056C	AMD	
	0026	Fairchild	
	SH013C	Fairchild	
	SH013M	† Fairchild	
	9646	Fairchild	
	MMH0026	† Motorola	
	MMH0026C	Motorola	40
	MH0009	† National	
	MH0009C	National	
	MH0013	† National	
	MH0013C	National	
	DS0025	† National	
	DS0025C	National	
	DS0026	† National	
	DS0026C	National	
	DS0056	† National	
	DS0056C	National	50
	SN75369	TI	
Two Phase Oscillator/Clock Driver (for MOS systems)	DS7803	† National	
	DS8803	National	
	DS7807	† National	
	DS8807	National	
	DS8813	National	
	DS8817	National	
Two Phase Oscillator Driver (for CCD Shift Register Memories)	CS233	Cherry	60
Quad NMOS Memory Driver	MC3459	Motorola	
	MC3460	Motorola	
	DS1644	† National	
	DS3644	National	

(Continued)

Memory & Peripheral Drivers (Cont'd.)

Function	Device	Source	Line
Quad NMOS Memory Driver (Cont'd.)	DS1674	† National	
	DS3674	National	
	DS36144	National	70
	DS36174	National	
Quad MOS Driver (for clock inputs 2416 and 2444 CCD Memories)	5244	Intel	
Quad Port Driver, for 5270 RAM	DS1640	† National	
	DS3640	National	
	DS1670	† National	
	DS3670	National	
Dual MOS Clock Driver, bootstrapped for single supply systems	DS1642	† National	80
	DS3642	National	
	DS1671	† National	
	DS3671	National	
	DS1672	† National	
	DS3672	National	
Quad MOS Clock Driver, decodes input address	DS3643	National	
	DS3673	National	90
Quad, MOS Memory Decoder/Clock Driver	DS36143	National	
	DS36173	National	
6-Bit MOS Refresh Counter/Driver	DS1646	† National	
	DS3646	National	
	DS1676	† National	
	DS3676	National	
Quad TTL to MOS Driver, Three-State	SN75357	TI	100
	SN75367	TI	
Quad TTL to NMOS Memory Driver (for 7001, etc.)	MC3466	Motorola	
Quad TTL to NMOS Memory Driver (for 2105, 2107, etc.)	9645	Fairchild	
	3245	Fairchild	
	3245	Intel	
	5235	Intel	
	MC3245	Motorola	110
Dual TTL to MOS Driver (MOS Memory Interface)	9644	Fairchild	
	DS75361	National	
	DS75362	National	
	DS75364	National	
	MH8805	National	
	75361A	Signetics	
	SN75350	TI	
	SN75361A	TI	
Dual AND TTL to MOS Driver (NMOS Memory Interface)	9643	Fairchild	120
	DS3622	National	
	DS75322	National	
	SN75322	TI	
	SN75363	TI	
Dual Channel TTL to MOS Memory Interface (for TMS4062, AMS6002, etc.)	SN75370	TI	

Memory & Peripheral Drivers (Cont'd.)

Function	Device	Source	Line
Quad NAND TTL to MOS Driver (MOS Memory Interface- clock driver)	HD2912	Hitachi	130
	HD2916	Hitachi	
	3207A	Intel	
	3207A-1	Intel	
	MC75365	Motorola	
	DS75365	National	
	3207A	Signetics	
	3207A-1	Signetics	
	SN75355	TI	140
	SN75365	TI	
	SN75366	TI	
	SN75375	TI	
Quad TTL to MOS Driver	MEM4900	GI	
TTL to MOS Shifter; See also Digital-TTL-Translators			
Dual ECL to MOS Driver	SN75320	TI	
	SN75321	TI	
Dual Channel ECL to MOS Driver (MOS Memory Interface; also ECL to TTL driver)	MC75358	Motorola	150
	MC75368	Motorola	
	SN75368	TI	
Dual MOS Logic to MOS Memory Driver	SN75364	TI	
Dual ECL to TTL/MOS Driver	SN75441	TI	
Hex MOS to Power Transistor-Level Shifter/Driver	M54520	Mitsubishi	160
Hex Latch/Driver, for MOS Memories	DS3645	Motorola	
	DS3675	Motorola	
	DS1645	† National	
	DS3645	National	
	DS1675	† National	
	DS3675	National	
Quad MOS Memory I/O Register	DS3647	Motorola	
	DS3677	Motorola	170
	DS36147	Motorola	
	DS36177	Motorola	
	DS1647	† National	
	DS3647	National	
	DS1677	† National	
	DS3677	National	
	DS16147	† National	
	DS36147	National	
	DS16177	† National	
	DS36177	National	180
Disc Memory Video Amplifer, for magnetic servo head	SSI101A	Silicon Sys.	
Disc Memory Fault Detector	SSI103	Silicon Sys.	
Disc Memory Head Selector	SSI102	Silicon Sys.	
Disc Memory Head Control Circuit, for moving heads	SSI104	Silicon Sys.	
Disc Memory Head Control Circuit, for fixed heads	SSI105	Silicon Sys.	190
Gated Decoder, for SSI104/5	SSI106	Silicon Sys.	

† Military Temperature Range (−55° to 125°C)

* Typical Values

INTERFACE–Memory and Peripheral Drivers (Cont'd)

Memory & Peripheral Drivers (Cont'd.)

Function	Device	Source	Line
Quad Predriver, Open Collector, 50 ma Sink (for magnetic memories)	MC4042	Motorola	
Dual Memory Driver, 400 ma Sink (for magnetic memories)	MC4043	Motorola	
Memory Driver Dual, 400 ma Sink/Source, Decode (for magnetic memories)	75324	Fairchild	
	DS3629	National	
	DS75324	National	
	75324	Signetics	10
	SN75324	TI	
Memory Driver, Quad, 600 ma Sink	55326M	† Fairchild	
	75326C	Fairchild	
	SN55326	† TI	
	SN75326	TI	
Memory Driver, Quad, 600 ma Source	55327M	† Fairchild	
	75327C	Fairchild	
	SN55327	† TI	20
	SN75327	TI	
Memory Switch, Quad, 600mA Sink/Source	SN75328	TI	
	SN75330	TI	
Memory Driver, Dual 600 ma Sink/Source	55325M	† Fairchild	
	75325	Fairchild	
	MC55325	† Motorola	
	MC75325	Motorola	
	DS55325	† National	30
	DS75325	National	
	55325	† Signetics	
	75325	Signetics	
	SG55325	† Silicon G	
	SG75325	Silicon G	
	SN55325	† TI	
	SN75325	TI	
Quad Multiplexer/Driver, for MOS systems	DS1648	† National	
	DS3648	National	40
	DS1678	† National	
	DS3678	National	
Hex Inverter/MOS Driver, Three-State	DS1649	† National	
	DS3649	National	
	DS1679	† National	
	DS3679	National	
Hex Inverter/MOS Driver, disable causes logic 1 state	DS16149	† National	
	DS36149	National	50
	DS16179	† National	
	DS36179	National	
Dual Buffer, to 40V, 2A	LPD4106	Lambda	
Dual AND Driver, HNIL, 250 ma, Open Collector	391	Teledyne S	
Dual Peripheral AND Driver	55450A/B	† Fairchild	
	55451A/B	† Fairchild	
	55460	† Fairchild	60
	55461	† Fairchild	
	55471	† Fairchild	
	75450	Fairchild	

(Continued)

Memory & Peripheral Drivers (Cont'd.)

Function	Device	Source	Line
Dual Peripheral AND Driver (Cont'd.)	75451	Fairchild	
	75460	Fairchild	
	75461	Fairchild	
	75471B	Fairchild	
	HD75450A	Hitachi	
	HD75451A	Hitachi	70
	M54504	Mitsubishi	
	M54600	Mitsubishi	
	M54601	Mitsubishi	
	MC75450	Motorola	
	MC75451	Motorola	
	SN75451B	Motorola	
	MC75461	Motorola	
	DS55450	† National	
	DS55451	† National	
	DS55460	† National	80
	DS55461	† National	
	DS75450	National	
	DS75451	National	
	DS75460	National	
	DS75461	National	
	RM55450	† Raytheon	
	RM55451	† Raytheon	
	PBD3513	RIFA	
	75450B	Signetics	
	75451B	Signetics	90
	SG55450	† Silicon G	
	SG55451	† Silicon G	
	SG55460	† Silicon G	
	SG55461	† Silicon G	
	SG75450	Silicon G	
	SG75451	Silicon G	
	SG75460	Silicon G	
	SG75461	Silicon G	
	SN55450B	† TI	
	SN55451B	† TI	100
	SN55460	† TI	
	SN55461	† TI	
	SN75466	TI	
	SN55470	† TI	
	SN55471	† TI	
	SN75401	TI	
	SN75411	TI	
	SN75430	TI	
	SN75431	TI	
	SN75450B	TI	110
	SN75451B	TI	
	SN75460	TI	
	SN75461	TI	
	SN75470	TI	
	SN75471	TI	
Dual Peripheral AND Driver, to 70v 300ma	MC1471	Motorola	
	SN75476	TI	
Dual Peripheral AND Driver, to 70v 500ma	SN75416	TI	120
Dual Peripheral AND Driver, to 80v, 300 ma	DS1611	† National	
	DS3611	National	
	DS3611	Signetics	
	UDN5711	Signetics	
	UDN-3611	Sprague	
	UDN-5711	Sprague	
Dual Peripheral AND Driver, for CMOS	DS1631	† National	
	DS3631	National	130

Memory & Peripheral Drivers (Cont'd.)

Function	Device	Source	Line
Dual 2-Input AND Power Driver (40V, to 2A)	LPD4101	Lambda	
Dual 4-Input AND Driver, HNIL 250 ma Open Collector	390	Teledyne S	
4-Input AND Current Driver (45v, to 1.5A peak)	DH0006	† National	
	DH0006C	National	
4-Input AND High Voltage-High Current Driver (4.5v, to 3A peak)	DH0008	† National	140
	DH0008C	National	
Quad 2-Input AND Driver (to 70v, sinks 300 ma)	MN304	Micro Net	
	MN304H	† Micro Net	
	UDS-5706H	† Sprague	
Quad 2-Input AND Power Driver, Open Collector (to 100v, sinks 500ma)	UHC/D-400	† Sprague	
	UHC/D-406	† Sprague	
	UHC/D-500	Sprague	150
	UHC/D-506	Sprague	
	UHP-400	Sprague	
	UHP-406	Sprague	
	UHP-500	Sprague	
	UHP-506	Sprague	
Quad 2-Input NAND Driver (to 70v, sinks 300 ma)	UDN-5707A	Sprague	
	UDS-5707H	† Sprague	
Dual NAND Driver, HNIL, 250 ma, Open Collector	392	Teledyne S	160
4-input NAND High Voltage, High Current Driver (40 to 100v, sinks 150 to 500 ma)	SH2001C	Fairchild	
	SH2001M	† Fairchild	
	SH2002C	Fairchild	
	SH2002M	† Fairchild	
	SH2200C	Fairchild	
	SH2200M	† Fairchild	
	SH2201C	Fairchild	
	SH2201M	† Fairchild	170
4-Input NAND High Voltage, High Current Drivers (40v, 0.15 to 0.25A)	DH0011	† National	
	DH0011C	National	
4-Input NAND High Voltage, High Current Drivers (50, 70 or 100v, 0.25 to 0.5A)	DH0016C	National	
	DH0017C	National	
	DH0018C	National	
Dual Peripheral NAND Driver	55452A	† Fairchild	180
	55462	† Fairchild	
	55472B	† Fairchild	
	75452	Fairchild	
	75462	Fairchild	
	75472B	Fairchild	
	HD75452	Hitachi	
	M54501	Mitsubishi	
	M54502	Mitsubishi	
	M54602	Mitsubishi	190
	M54605	Mitsubishi	
	MC75452	Motorola	
	MC75462	Motorola	
	SN75452B	Motorola	
	DS55452	† National	
	DS55462	† National	

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Values

Bold face indicates additional data is provided on the page noted.

INTERFACE–Memory and Peripheral Drivers (Cont'd)

Memory & Peripheral Drivers (Cont'd.)

Dual Peripheral NAND Driver (Cont'd.)

Device	Source
DS75452	National
DS75462	National
RM55452	† Raytheon
75452B	Signetics
SG55452	† Silicon G
SG55462	† Silicon G
SG75452	Silicon G
SG75462	Silicon G
SN75402	TI
SN75412	TI
SN75432	TI
SN75447	TI
SN55452B	† TI
SN75452B	TI
SN55462	† TI
SN75462	TI
SN55472	† TI
SN75472	TI
SN75475	TI

Dual 4-Input NAND Driver, HNIL, 250 ma Open Collector

Device	Source
395	Teledyne S

Dual Peripheral NAND Driver, to 70v, 300ma

Device	Source
MC1472	Motorola
SN75477	TI

Dual Peripheral NAND Driver, to 70v, 500ma

Device	Source
SN75417	TI

Dual Peripheral NAND Driver, to 80v, 300ma

Device	Source
DS1612	† National
DS3612	National
DS3612	Signetics
UDN5712	Signetics
UDN-3612	Sprague
UDN-5712	Sprague

Dual Peripheral NAND Driver, for CMOS

Device	Source
DS1632	† National
DS3632	National

Quad 2-Input NAND Driver, to 30v, sinks 250ma

Device	Source
MC693	Motorola

Quad 2-Input NAND Driver, to 30v, sinks 100ma

Device	Source
M54503	Mitsubishi

Quad 2-Input NAND Power Driver, Open Collector, to 100v, sinks 500 ma

Device	Source
UHC/D-407	† Sprague
UHC/D-408	† Sprague
UHC/D-507	† Sprague
UHC/D-508	† Sprague
UHP-407	Sprague
UHP-408	Sprague
UHP-507	Sprague
UHP-508	Sprague

Quad PIN Diode Driver (Also see: Linear-Other Devices)

Device	Source
UDS-5790	† Sprague
UDS-5791	† Sprague

Power Peripheral Driver, CMOS/TTL Input (to 150 V, versions: 0.01 to 16 A)

Device	Source	
VF-01	**Supertex**	**(835)**
VF-12	**Supertex**	**(835)**
VF-13	**Supertex**	**(835)**
VF-14	**Supertex**	**(835)**

Power Peripheral Driver/Logic Switch, to 90 V, 2.0 A (relay, solenoid, and hammer driver)

Device	Source	
S75V01	**Siliconix**	**(833)**

(Continued)

Memory & Peripheral Drivers (Cont'd.)

Power Peripheral Driver/Logic Switch, to 90 V, 2.0 A (relay, solenoid, and hammer driver) (Cont'd.)

Device	Source	
S75V03	**Siliconix**	**(833)**

Relay Driver, to 70v, 500ma

Device	Source
CSR301	Teledyne C

Relay Driver, to 65v, sinks 300 ma, OR Input for 48v telephone relays

Device	Source
DS1686	† National
DS1687	† National
DS3686	National
DS3687	National

Dual Relay Driver, to 60v, sinks 1a

Device	Source
831	Beckman

Dual OR Driver, HNIL, 250 ma, Open Collector

Device	Source
393	Teledyne S

Dual Peripheral OR Driver

Device	Source
55453A/B	† Fairchild
55463	† Fairchild
55473B	† Fairchild
75453	Fairchild
75463	Fairchild
75473B	Fairchild
75453	Hitachi
M54603	Mitsubishi
MC75453	Motorola
MC75463	Motorola
SN75453B	Motorola
DS55453	† National
DS55463	† National
DS75453	National
DS75463	National
RM55453	† Raytheon
75453B	Signetics
SG55453	Silicon G
SG55463	Silicon G
SG75453	Silicon G
SG75463	Silicon G
SN55453B	† TI
SN55463	† TI
SN55473	† TI
SN75403	TI
SN75413	TI
SN75433	TI
SN75448	TI
SN75453B	TI
SN75463	TI
SN75473	TI

Dual Peripheral OR Driver, to 30v, 300ma

Device	Source
MC1473	Motorola
SN75478	TI

Dual Peripheral OR Driver, to 30v, 500ma

Device	Source
SN75418	TI

Dual Peripheral OR Driver, to 80v, 300ma

Device	Source
DS1613	† National
DS3613	Signetics
DS3613	National
UDN5713	Signetics
UDN-3613	Sprague
UDN-5713	Sprague

Dual Peripheral OR Driver, ECL Input

Device	Source
SN75441	TI

Dual Peripheral OR Driver, for CMOS

Device	Source
DS1633	† National
DS3633	National

Dual 2-Input OR Power Driver (40V, to 2A)

Device	Source
LPD4104	Lambda

Memory & Peripheral Drivers (Cont'd.)

Quad 2-Input OR Driver, to 70v, sinks 300ma

Device	Source
UDN-5703A	Sprague
UDS-5703H	† Sprague

Quad 2-Input OR Power Driver, Open Collector, to 100v, sinks 500ma

Device	Source
UHC/D-402	† Sprague
UHC/D-403	† Sprague
UHC/D-502	Sprague
UHC/D-503	Sprague
UHP-402	Sprague
UHP-403	Sprague
UHP-502	Sprague
UHP-503	Sprague

Dual NOR Driver, HNIL, 250 ma, Open Collector

Device	Source
394	Teledyne S

Dual Peripheral NOR Driver

Device	Source
55454A/B	† Fairchild
55464	† Fairchild
55474	† Fairchild
75454	Fairchild
75464	Fairchild
75474B	Fairchild
HD75454	Hitachi
M54604	Mitsubishi
MC75454	Motorola
SN75454B	Motorola
MC75464	Motorola
DS55454	† National
DS55464	† National
DS75454	National
DS75464	National
RM55454	† Raytheon
75454B	Signetics
SG55454	† Silicon G
SG55464	† Silicon G
SG75454	Silicon G
SG75464	Silicon G
SN55454B	† TI
SN55464	† TI
SN55474	† TI
SN75404	TI
SN75414	TI
SN75434	TI
SN75449	TI
SN75454B	TI
SN75464	TI
SN75474	TI

Dual Peripheral NOR Driver, to 30v, 300ma

Device	Source
MC1479	Motorola
SN75479	TI

Dual Peripheral NOR Driver, to 30v, 500ma

Device	Source
SN75419	TI

Dual Peripheral NOR Driver, to 80v, 300ma

Device	Source
DS1614	† National
DS3614	National
DS3614	Signetics
UDN5714	Signetics
UDN-3614	Sprague
UDN-5714	Sprague

Dual Peripheral NOR Driver, for CMOS

Device	Source
DS1634	† National
DS3634	National

Quad 2-Input NOR Driver, to 70v, sinks 300ma

Device	Source
UDN-5733A	Sprague
UDS-5733H	† Sprague

† Military Temperature Range (−55° to 125°C)

* Typical Values

INTERFACE–Memory and Peripheral Drivers (Cont'd)

Memory & Peripheral Drivers (Cont'd.)

Quad 2-Input NOR Power Driver, Open Collector, to 100v, sinks 500ma

Device	Source
UHC/D-432	†Sprague
UHC/D-433	†Sprague
UHC/D-532	†Sprague
UHC/D-533	†Sprague
UHP-432	Sprague
UHP-433	Sprague
UHP-532	Sprague
UHP-533	Sprague

High Current Switch Driver (to drive high power, high speed NPN switching transistors)

Device	Source
SG1629	†Silicon G
SG3629	Silicon G

Driver, Open Collector/Emitter, for 150mA (load connected to negative supply)

Device	Source
PBD3520	RIFA

Driver, single, 125mA, for relays, motors, lamps

Device	Source
PBD3510	RIFA
PBD3511	RIFA

Driver, to 80v, 0.2a; for relays, lamps

Device	Source
DI445	Dionics

Driver, dual, to 80v, 0.2a; for relays, lamps

Device	Source
DI446	Dionics

Driver, dual, to 80v, sinks 5a, (relay, solenoid, hammer driver)

Device	Source
SH3011	**Fairchild (955)**

Dual Darlington Switch, to 80v, 1.5a

Device	Source
ULN-2061	Sprague
ULN-2062	Sprague

Quintuple High Voltage Interface (Outputs can accept high negative voltages in "off" state)

Device	Source
SP1404	Plessey
SP1406	Plessey

Driver, dual, 2-input, Sink or Source 500mA

Device	Source
SG1627	**†Silicon G (1129)**
SG3627	**Silicon G (1129)**

Quad Darlington Switch, to 80v, 1.5a

Device	Source
ULN-2064	Sprague
ULN-2065	Sprague
ULN-2066	Sprague
ULN-2067	Sprague
ULN-2068	Sprague
ULN-2069	Sprague
ULN-2070	Sprague
ULN-2071	Sprague
ULN-2074	Sprague
ULN-2075	Sprague
ULN-2076	Sprague
ULN-2077	Sprague
ULN2064	TI
ULN2065	TI

Quad Power Drive, with enable, sinks 500ma

Device	Source
UDN-2540	Sprague

Quad Latch/Driver

Device	Source
UCN-4401	Sprague

5-Channel Relay Driver for telephone relays

Device	Source
AY5-9050	GI

Hammer Driver (to 6A-pulsed output)

Device	Source
DH0028C	National

Driver, 5 channel Darlington, to 400ma

Device	Source
LB1287	Sanyo
LB1288	Sanyo
XR2200	Exar

(Continued)

Memory & Peripheral Drivers (Cont'd.)

Driver, 5 channel Darlington, to 400ma (Cont'd.)

Device	Source
XR2200M	†Exar

Driver, 5 channel, CMOS/TTL Input (lamp, relay driver, load to negative supply)

Device	Source
UDN-2957A	Sprague

Driver, 5 channel, CMOS/PMOS Input (lamp, relay driver, load to negative supply)

Device	Source
UDN-2956A	Sprague

Hex Universal Driver (400 ma)

Device	Source
NE582	Signetics

Driver, 7 Channel, CMOS/TTL Input (hammer, lamp, relay driver)

Device	Source
XR2203	**Exar (931)**
XR2203M	**†Exar (931)**
9667	Fairchild
MC1413	Motorola
PBD352303	RIFA
ULN2003	Signetics
L203	SGS
SG2003	Silicon G
SG3853	Silicon G
ULN-2003A	Sprague
ULN-2005A	Sprague
ULN-2013A	Sprague
ULN-2015A	Sprague
ULN-2023A	Sprague
ULN-2025A	Sprague
SN75468	TI
ULN2003A	TI

Driver, 7 Channel, CMOS/PMOS Input (hammer, lamp, relay driver)

Device	Source
XR2204	**Exar (931)**
XR2204M	**†Exar (931)**
9668	Fairchild
MC1416	Motorola
PBD352304	RIFA
ULN2004	Signetics
ULN-2004A	Sprague
ULN-2014A	Sprague
ULN-2024A	Sprague
SN75469	TI
ULN2004A	TI

Driver, 7 Channel, MOS/TTL Input (hammer, lamp, relay driver)

Device	Source
XR2201	**Exar (931)**
XR2201M	**†Exar (931)**
9665	Fairchild
MC1411	Motorola
PBD352301	RIFA
ULN2001	Signetics
L201	SGS
SG2001	Silicon G
SG3851	Silicon G
ULN-2001A	Sprague
ULN-2011A	Sprague
ULN-2021A	Sprague
SN75466	TI
ULN2001A	TI

Driver, 7 Channel, PMOS Input (hammer, lamp, relay driver)

Device	Source
XR2202	**Exar (931)**
XR2202M	**†Exar (931)**
9666	Fairchild
MC1412	Motorola
PBD352302	RIFA
ULN2002	Signetics

(Continued)

Memory & Peripheral Drivers (Cont'd.)

Driver, 7 Channel, PMOS Input (hammer, lamp, relay driver) (Cont'd.)

Device	Source
L202	SGS
SG2002	Silicon G
SG3852	Silicon G
ULN-2002A	Sprague
ULN-2012A	Sprague
ULN-2022A	Sprague
SN75467	TI
ULN2002A	TI

Addressable Peripheral Driver (Latched, 8-Output Driver)

Device	Source
NE590	**Signetics (807)**
NE591	**Signetics (807)**
NE592	Signetics

Driver, 8 Channel, CMOS/TTL Input (hammer, lamp, relay driver)

Device	Source
ULN-2803A	Sprague
ULN-2805A	Sprague
ULN-2813A	Sprague
ULN-2815A	Sprague
ULN-2823A	Sprague
ULN-2825A	Sprague

Driver, 8 Channel, CMOS/PMOS Input (hammer, lamp, relay driver)

Device	Source
ULN-2804A	Sprague
ULN-2814A	Sprague
ULN-2824A	Sprague

Driver, 8 Channel, MOS/TTL Input (hammer, lamp, relay driver)

Device	Source
ULN-2801A	Sprague
ULN-2811A	Sprague
ULN-2821A	Sprague

Driver, 8 Channel, PMOS Input (hammer, lamp, relay driver)

Device	Source
ULN-2802A	Sprague
ULN-2812A	Sprague
ULN-2822A	Sprague

Driver, 8 Channel, CMOS/TTL Input (lamps, relay driver)

Device	Source
UDN-2981A	Sprague
UDN-2983A	Sprague

Driver, 8 Channel, CMOS/PMOS Input (lamp, relay driver)

Device	Source
UDN-2982A	Sprague
UDN-2984A	Sprague

Eight Latch/Drivers

Device	Source
UCN-4801	Sprague

Printer Controller, for 5 x 7 dot matrix printers

Device	Source
CY-480	Cybernetic

Printer Driver, 5 Channel

Device	Source
HD2919	Hitachi
LB1287	Sanyo
LB1288	Sanyo

Printer Solenoid Driver

Device	Source
DS3654	National

Thermal Print Head Driver

Device	Source
SN75270	TI
SN75490	TI

Printing Calculator Circuits

Device	Source
DS8654	National
DS8655	National
DS8656	National
DS8692	National
DS8693	National

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Values

Bold face indicates additional data is provided on the page noted.

INTERFACE–Memory and Peripheral Drivers (Cont'd)

Function	Device	Source	Line
Memory & Peripheral Drivers (Cont'd.)			
Printing Calculator Circuits		(Cont'd.)	
	DS8694	National	

Function	Device	Source	Line

Function	Device	Source	Line

† Military Temperature Range (−55° to 125°C)

* Typical Values

INTERFACE–Sense Amplifiers

Sense Amplifiers

Dual Channel Gated Sense Amplifier (for core memories)

Device	Source
CA1541	† RCA

Dual Core Memory Sense Amplifier, Separate Outputs

Device	Source
5524	† Fairchild
5525	† Fairchild
55224	† Fairchild
55225	† Fairchild
7524	Fairchild
7525	Fairchild
75224	Fairchild
75225	Fairchild
HA1902	Hitachi
DS5524	† National
DS5525	† National
DS7524	National
DS7525	National
7524	Signetics
SG5524	† Silicon G
SG5525	† Silicon G
SG7524	Silicon G
SG7525	Silicon G
SN5524	† TI
SN7524	TI

Dual Core Memory Sense Amplifier, Complemetary Output, Latch Capability

Device	Source
5520	† Fairchild
7520	Fairchild
DS5520	† National
DS5521	† National
DS7520	National
DS7521	National
7520	Signetics
SG5520	† Silicon G
SG5521	† Silicon G
SG7520	Silicon G
SG7521	Silicon G
SN5520	† TI
SN7520	TI

Dual Core Memory Sense Amplifier, Single Open Collector Output

Device	Source
DS5522	† National
DS5523	† National
DS7522	National
7522	Signetics
SG5522	† Silicon G
SG5523	Silicon G
SG7522	Silicon G
SG7523	Silicon G
SN5522	† TI
SN7522	TI

Dual Core Memory Sense Amplifier, Output Register

Device	Source
SN7526	TI

Dual Core Memory Sense Amplifier, Separate Outputs, Test Points

Device	Source
5528	† Fairchild
5529	† Fairchild
7528	Fairchild
7529	Fairchild
DS5529	† National
DS7528	National
DS7529	National
7528	Signetics
SG5528	† Silicon G
SG7528	Silicon G
SG5529	† Silicon G
SG7529	Silicon G
SN5528	† TI

(Continued)

Sense Amplifiers (Cont'd.)

Dual Core Memory Sense Amplifier, Separate Outputs, Test Points (Cont'd.)

Device	Source
SN7528	TI

Dual Core Memory Sense Amplifier, Separate Inverted Outputs

Device	Source
55234	† Fairchild
55235	† Fairchild
75234	Fairchild
75235	Fairchild
75234	Signetics
SN55234	† TI
SN75234	TI

Dual Core Memory Sense Amplifier, Separate Inverted Outputs, Test Points

Device	Source
55238	† Fairchild
55239	† Fairchild
75238	Fairchild
75239	Fairchild
SN55238	† TI
SN75238	TI

Dual Core Memory Sense Amplifier, Separate Open Collector Outputs

Device	Source
5534	† Fairchild
5535	† Fairchild
55232	† Fairchild
55233	† Fairchild
7534	Fairchild
7535	Fairchild
75232	Fairchild
75233	Fairchild
DS5534	† National
DS5535	† National
DS7534	National
DS7535	National
75232	Signetics
SG5534	† Silicon G
SG5535	† Silicon G
SG7534	Silicon G
SG7535	Silicon G
SN55232	† TI
SN75232	TI

Dual Core Memory Sense Amplifier, Separate Open Collector Outputs, Test Points

Device	Source
5538	† Fairchild
5539	† Fairchild
5580	Fairchild
7539	Fairchild
DS5538	† National
DS5539	† National
DS7538	National
DS7539	National
SG5538	† Silicon G
SG5539	† Silicon G
SG7538	Silicon G
SG7539	Silicon G

MOS to TTL Level Converter, High Speed, Three-State

Device	Source
MC4000	Motorola
MC4300	† Motorola

Dual Sense Amplifier (for MOS Memory or line receiver)

Device	Source
DS163	† AMD
DS363	AMD
DS1603	† AMD
DS3603	AMD
DS3604	AMD
SN75207	AMD
SN75208	AMD

(Continued)

Sense Amplifiers (Cont'd.)

Dual Sense Amplifier (for MOS Memory or line receiver) (Cont'd.)

Device	Source
75207	Fairchild
75208	Fairchild
DS3604	National
DS1603	† National
DS3603	National
DS75207	National
DS75208	National
75S207	Signetics
75S208	Signetics
SN75207	TI
SN75208	TI

Dual Sense Amplifier (NMOS memories to ECL 10K)

Device	Source
HD103461	Hitachi
MC3461	Motorola

Dual MOS to TTL Level Converter, Latch, Three-State (Sense Amp)

Device	Source
MC4068	Motorola
MC4368	† Motorola
MC54468	† Motorola
MC74468	Motorola
DS3625	National
DS7802	† National
DS7806	† National
DS8802	National
DS8806	National
N8T25	Signetics

Translators: See also Digital-TTL (Translators)

Quad Sense Amplifier, Three-State

Device	Source
MC3430	Motorola
MC3431	Motorola
MC3432	Motorola
MC3433	Motorola
DS3651	National
DS3653	National

Hex MOS Sense Amplifier (MOS to TTL Converter) Three-State

Device	Source
DS1605	† National
DS1606	† National
DS1607	† National
DS1608	† National
DS3605	National
DS3606	National
DS3607	National
DS3608	National

Hex MOS Sense Amplifier, Open Collector (for 1103)

Device	Source
3208A	Intel

Hex MOS Sense Amplifiers with Latches, Three-State

Device	Source
3408A	Intel

4-Input Sense Amplifier (for plated wire or thick/thin film memories)

Device	Source
MC1444	Motorola
MC1544	† Motorola

† Military Temperature Range (−55° to 125°C)

* Typical Values

Bold face indicates additional data is provided on the page noted.

INTERFACE–Transmitters-Receivers

Serial Transmitters-Receivers

Function	Max Serial Data Rate in KHZ	Supply Voltage	Device	Source	Line
(ACIA) Asynchronous Communications Interface Adapter (Links 8-Bit bidirectional data bus to serial asynchronous data communications, including to 6860)	50	5	**S6850**	**AMI (1818)**	
			F6850	**Fairchild (1887,1891)**	
			HD46850	Hitachi	
			MC6850	**Motorola (1977)**	
Asynchronous Addressable Receiver/Transmitter	4.8	3-18	**MC14469**	**Motorola (788)**	10
Digital Modem (Modulation, demodulation and supervisory control, up to 600bps.)	4.8	3-18	F6860	Fairchild	
	0.6	5	MC6860	Motorola	
PSAR (Programmable Synchronous-Asynchronous Receiver) Synchronous/Asynchronous serial to parallel converter with programmable character length and programmable serial data rate.	100	-12,5	AY8-1472B	GI	
			PT1472B	Western	20
	640	-12,±5	NC2259	Nitron	
		-12,5	PT1472B-01	Western	
PSAT (Programmable Synchronous-Asynchronous Transmitter) Synchronous/Asynchronous parallel to serial converter that has programmable character length and programmable serial data rate.	100	-12,5	AY8-1482B	GI	
			PT1482B	Western	
	200	-12,±5	NC2257	Nitron	
			NC2260	Nitron	30
	640	-12,5	PT1482B-01	Western	
PSART (Programmable Synchronous-Asynchronous Receiver-Transmitter) Serial to parallel and parallel to serial converter that can operate in Full Duplex Mode.	50	5	8251	Intel	
			μPD8251	**NEC Micro (2204)**	
	80	5,12	**3843-3**	**Fairchild (1887,1892)**	
	100	5,12	**3843-2**	**Fairchild (1887,1892)**	40
	320	5,12	**3843-1**	**Fairchild (1887,1892)**	
BOART (Bus Orientated Programmable Asynchronous Receiver/Transmitter	9.6	5	TR1983	Western	
SDLC/HDLC/ADCCP Controller	1500	5	SD1933	Western	
	2000	5	SD1933-01	Western	
Synchronous Receiver/Transmitter (Bi-Sync/SDLC)	800	±5,12	μPD379	NEC Micro	50
SPCC (Sync-Protocol Communications Controller) Bit and Byte Orientated	1000	5	**F3846**	**Fairchild (1887,1892)**	
			F6856	**Fairchild (1887,1892)**	
UART (Universal Asynchronous Receiver-Transmitter) complete serial to parallel and parallel to serial interface)	1.2	-12,5	10371	Rockwell	
	10	-12,±5	S1757	AMI	60

(Continued)

Serial Transmitters-Receivers (Cont'd.)

Function	Max Serial Data Rate in KHZ	Supply Voltage	Device	Source	Line
UART (Universal Asynchronous Receiver-Transmitter) complete serial to parallel and parallel to serial interface)				(Cont'd.)	
	12.5	-12.5	**S1883**	**AMI (629)**	
	20	-12,5	AY6-1013	† GI	
			TR1402	Western	
			TR1602	Western	
	25	-12,5	COM2017	SMC	
			COM2502	SMC	
	30	5	AY3-1015D	GI	
			COM8017	SMC	70
			COM8052	SMC	
		5 to 14	AY3-1014A	GI	
		-12,5	MM5303	National	
			TR1602-03	Western	
	40	-12,5	AY5-1013A	GI	
			COM2017H	SMC	
			COM2502H	SMC	
			TR1602-04	Western	
	50	±5,12	μPD369	NEC Micro	
		-12,5	TR1602-05	Western	80
	56	5	**INS8250**	**National (2018)**	
	60	5	COM8017	SMC	
			TR1863	Western	
	100	5	HCMP1854C	† Hughes	
			CDP1854C	† RCA	
	125	5	**HD6402C-9**	**Harris (1930)**	
	200	5	**HD6402-2**	**† Harris (1930)**	
			HD6402-9	**Harris (1930)**	
			HD6403-2	† Harris	
			HD6403-9	Harris	90
			IM6402	Intersil	
			IM6402M	† Intersil	
			IM6403	Intersil	
			IM6403M	† Intersil	
			COM6402	SMC	
			TR1863-01	Western	
		4-6	SCP1854L	SSS	
		-12,5	TMS6011	TI	
	375	10	**HD6402A-2**	**† Harris (1930)**	
		5	**HD6402A-9**	**Harris (1930)**	100
	400	5	**HD6402A-9**	**Harris (1930)**	
			HD6403A-2	† Harris	
			HD6403A-9	Harris	
		3–12	HCMP1854	† Hughes	
			CDP1854	† RCA	
		4-12	SCP1854	† SSS	
	800	5	MB8868A	Fujitsu	
USRT (Universal Synchronous Receiver-Transmitter) Complete serial to parallel and parallel to serial interface.	250	-12,5	COM2601	SMC	110
	500	5	**S2350**	**AMI (634)**	
USART (Universal Synchronous/Asynchronous Receiver/Transmitter)	56	5	TR1953	Western	
	256	5,12	**3843**	**Fairchild (1887,1892)**	

† Military Temperature Range (−55° to 125°C)

* Typical Values

INTERFACE–Transmitters-Receivers (Cont'd)

Serial Transmitters-Receivers (Cont'd.)

Function	Max Serial Data Rate in KHZ	Supply Voltage	Device	Source	Line
USYNRT (Universal Synchronous Receiver/Transmitter) Multi-Protocol, Bit and Byte Oriented	1500	5,12	COM5025	SMC	
MPCC (Multi-Protocol Communications Controller) Bit and Byte Oriented	500	5	**2652**	**Signetics (2306)**	
Universal Communications Interface (receives or transmits data to serial data bus when addressed and commanded by bus. Links the bus to serial or parallel I/0 devices)	500	-10,5	UMC-16	Trans-Data	
ASTRO (Asynchronous/Synchronous Receiver/Transmitter) to interface serial communications channel with a parallel digital system (i.e. microprocessors)	1000	12,±5	INS1671	National	10
			COM1671	SMC	
			UC1671	Western	
			UC1671-01	Western	
			UC1971	Western	
Baud Rate Generator (Programmable Divider)	1000	12,5	COM5026	SMC	
			COM5026T	SMC	20
			COM5046	SMC	
			COM5046T	SMC	
			COM8046	SMC	
			COM8046T	SMC	
		12,±5	F4702BC	Fairchild	
			F4702BM	† Fairchild	
			HD4702-2	**† Harris (1926)**	
			HD4702-9	**Harris (1926)**	
			HD6405-2	**† Harris (1926)**	
			HD6405-9	**Harris (1926)**	30
			MC14411	Motorola	
			MM5307	National	
Baud Rate Generator (Programmable Divider), Dual	1000	12,5	COM5016	SMC	
			COM5016T	SMC	
			COM5036	SMC	
			COM5036T	SMC	
			COM8016	SMC	
			COM8016T	SMC	
		12,±5	BR1941	Western	40
			BR1941-05	Western	
			BR1941-06	Western	

† Military Temperature Range (−55° to 125°C)

* Typical Values

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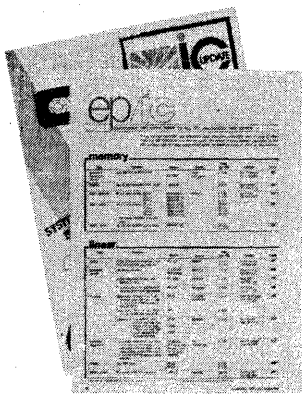
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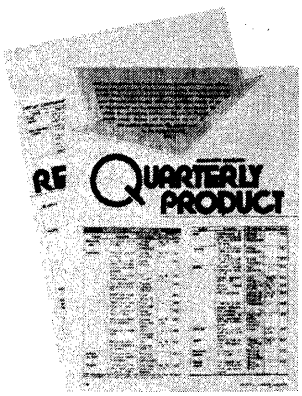
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Communications Circuits

Part No.	Description	Process	Power Supplies	Input/ Output	Package
S1883	Universal Asynchronous Receiver/Transmitter (UART)	P-I^2	-12V, ± 5V	TTL	40 Pin Plastic, 40 Pin SLAM
S2350	Universal Synchronous Receiver/Transmitter (USRT)	N-SiGate	+5V	TTL	40 Pin Plastic 40 Pin SLAM
S2559A/B	Digital Tone Generator	CMOS	+3.5V to +13V	TTL-CMOS	16 Pin Plastic
S2559C/D	Digital Tone Generator	CMOS	+2.75 to +10V	TTL-CMOS	16 Pin Plastic, 16 Pin Cer-Dip
S2560A/B	Key Pulser	CMOS	+12V		18 Pin Package
S2561	Tone Ringer	CMOS	+13.5V		18 Pin Package
S2562	Repertory Dialer	CMOS			40 Pin Package

TouchControl™ Interface Circuits

Part No.	Description	Process	Power Supplies	Input/ Output	Packages
S9260/61	Seven-Switch Interface	P-I^2	-13.5V to -18V	CMOS/TTL	22 Pin Plastic
S9263/64/65	Sixteen-Switch Interface	P-I^2	-13.5V to -18V	CMOS/MOS/ TTL	40 Pin Plastic
S9262	Fourteen-Switch Interface	P-I^2	-13.5V to -18V	MOS/TTL	22 Pin Plastic
S9266	Thirty-Two-Switch Interface	P-I^2	-13.5V to -18V	MOS/TTL	40 Pin Plastic

TCK-100 TouchControl™ Kit

The AMI TouchControl kit demonstrates the ease with which this unique system of capacitive switching may be implemented. Included in the kit are a printed circuit board and AMI's S9263 TouchControl circuit. The printed wiring board, which has sixteen touch switches etched into its top surface, contains on its reverse side all the interconnection necessary to interface the S9263 outputs with sixteen light emitting diodes. Additional components required for the kit are readily available, and assembly of the kit should take less than an hour's time.

The TouchControl™ Concept

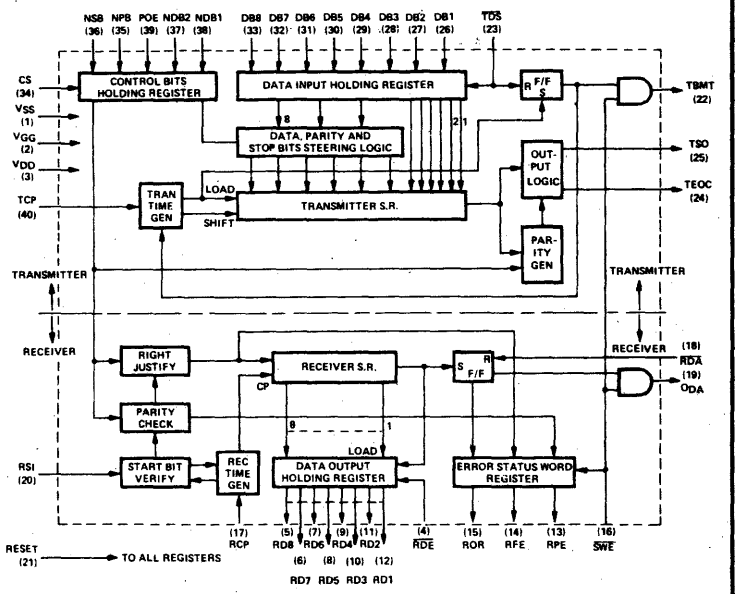
TouchControl™ panels replace mechanical switches with non-moving electronically sensitive glass (or other material) panels that respond to the touch of a finger. The most apparent advantage of TouchControl is the visual appeal of a flat keyboard, which may be designed in a wide variety of patterns and colors. In addition to the advanced styling features, TouchControl also offers several practical benefits, such as the reliability of non-moving electronic controls and electrical isolation of the entire switch area. TouchControl also provides safety advantages, complete moisture proofing and ease of cleaning. Contact your nearest AMI Sales Office for additional information about the TouchControl concept.

Typical Applications

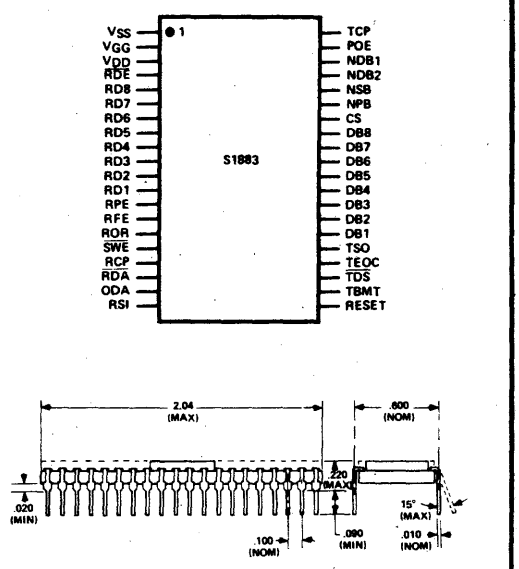
- Appliance Control Panels
- Home Entertainment Systems
- Power Tool Controls
- Television Sets
- Automotive Controls
- Telephones
- Games
- Industrial Controllers
- Computer Terminals
- Keyboards
- Instrumentation
- 16-to01 Multiplexers
- Microprocessor Interface

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Universal Asynchronous Receiver/Transmitter (UART)



S1883 BLOCK DIAGRAM



PIN/PACKAGE CONFIGURATION

FEATURES

- 12.5 K Baud Data Rates
- 5-8 Bit Word Length
- Parity Generation/Checking Odd, Even, None
- Framing and Overflow Error Detection
- 1, 1.5, or 2 Stop Bits
- Double Buffered Input/Output
- Independent Transmit/Receive Rates
- Start and Stop Bits Generated and Detected
- Interchangeable with TMS6011, COM2017, TR1602, AY-5-1013
- Tri-State Outputs

FUNCTIONAL DESCRIPTION

The S1883 Universal Asynchronous Receiver Transmitter (UART) is a single chip MOS/LSI device that totally replaces the asynchronous parallel to serial and serial to parallel conversion logic required to interface a word parallel controller or data terminal to a bit serial communication network.

For asynchronous data transmission with a non-contiguous data bit stream, the UART automatically inserts a START bit preceding each character and under program control 1, 1.5, or 2 stop bits at the end of each character. To detect incoming characters in a noisy environment the UART employs a START bit detection network and allows errorless recovery of data with up to 42% distortion.

The UART will transmit or receive data characters of 5, 6, 7, or 8 bit length. Options allow the generation and checking of odd, even parity or no parity. The odd or even parity bit is automatically added to the character length for transmission. The parity bit is removed, checked and an error flag set if incorrectly received.

The data or baud rate at the receiver input and transmitter output are determined independently by external clock inputs. The clock inputs must be 16 times the data rate required at the serial input and output. The independent clocks allow for either half or full duplex operation.

The UART provides a buffer register in both the transmitter and receiver to allow a full character time for responding to a received data ready or transmit data request signal. The UART generates a MARK signal if the transmit register is not loaded with a data character and also indicates an overflow error if two characters are received without a RDA input.

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TYPICAL APPLICATIONS

- Computer Peripherals
- Communication Concentrators
- Integrated Modems
- Industrial Data Transmission
- TTY Terminals
- Time Division Multiplexing

ABSOLUTE MAXIMUM RATINGS

Ambient Temperature Under Bias	0°C to +70°C
Storage Temperature	−65°C to +150°C
Positive Voltage on Any Pin with Respect to V_{SS}	+.3 Volt
Negative Voltage on Any Pin with Respect to V_{SS}	−20.0 Volt

NOTE: Stresses greater than those listed as Maximum Ratings may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operation section of this specification are not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC (STATIC) CHARACTERISTICS

$T_A = 0° - +70°C$, $V_{SS} = +5$ Volt ±5%, $V_{GG} = -12$ Volt ±5%

Symbol	Parameter	Min	Max	Unit	Condition
V_{IH}	Input High Voltage	V_{SS} -1.0	V_{SS} +0.3	Volt	Internal Pull-up
V_{IL}	Input Low Voltage	V_{GG}	0.8	Volt	Resistor Provided
I_{LI}	Input Load Current		-1.2	mamp	V_{IN} = 0 Volt
V_{OH}	Output High Voltage	2.4		Volt	I_{OH} = - 100 uamp
V_{OL}	Output Low Voltage		.4	Volt	I_{OL} = 1.6 mamp
C_{IN}	Input Capacitance		20	pf	$V_{IN} = V_{SS}$
C_{OUT}	Output Capacitance		10	pf	$V_{OUT} = V_{SS}$
I_{SS}	V_{SS} Supply Current		30	mamp	$\overline{SWE} = \overline{RDE} = V_{IL}$
I_{GG}	V_{GG} Supply Current		40	mamp	ITTL Load

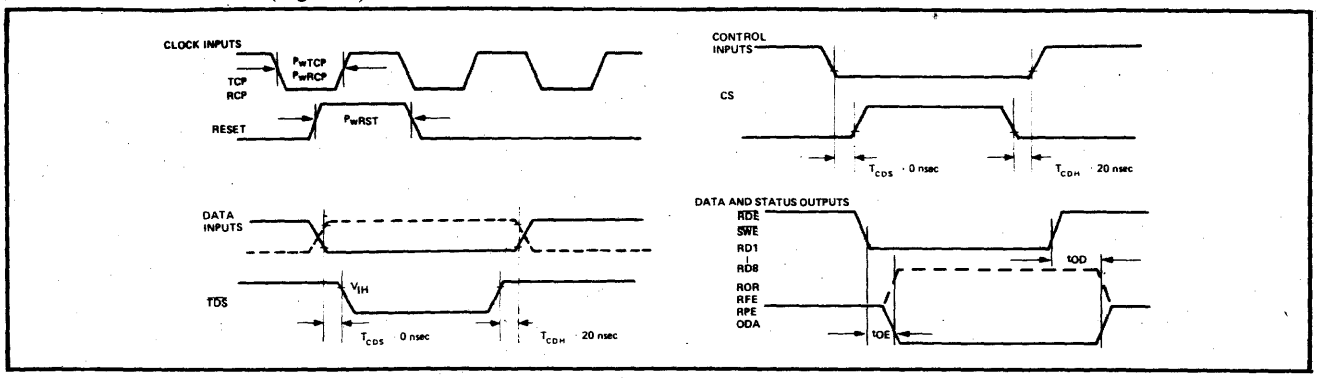
AC (DYNAMIC) CHARACTERISTICS

$T_A = 0°C - +70°C$; $V_{SS} = +5$ Volt ±5%; $V_{GG} = -12$ Volt ±5%

Symbol	Parameter	Min	Max	Unit	Condition
TCP, RCP	Clock Frequency	DC	200	KHz	
Input Pulse Widths					
PWTCP	Transmit Clock	2.5		usec	C_L = 20pf
PWRCP	Receive Clock	2.5		usec	1 TTL Load
PWCS	Control Strobe	250		nsec	
PWTDS	Transmit Data Strobe	250		nsec	
PWRST	RESET	1.0		μsec	
PWSWE	Status Word Enable	500		nsec	
PWRDA	Reset Data Available	500		nsec	
PWRDE	Receive Data Enable	250		nsec	
Switching Characteristics					
t_{CDS}	Control Set Up Time	0		nsec	Figure 1
t_{CDH}	Control Hold Time	20		nsec	Figure 1
t_{OE}	Output Enable Time		500	nsec	
t_{OD}	Output Disable Time		500	nsec	

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TIMING WAVEFORMS (Figure 1)



PIN DEFINITIONS

Pin	Label	Function
(1)	V_{SS}	+5 Volt ± 5%
(2)	V_{GG}	−12 Volt ± 5%
(3)	V_{DD}	Ground
(21)	RESET	The transmitter status outputs TBMT and TEOC are set to V_{OH} indicating the input transmitter buffer register is empty. The TSO output generates V_{OH} or MARK until a valid data character has been loaded into the transmitter and valid data transmission begins. The receiver status output ODA, is reset to the V_{OL} state.
(38)	NDB1	Number Data Bits/Character
(37)	NDB2	Number Data Bits/Character
(36)	NSB	Number Stop Bits The bit length of each data character and the number of stop bits added to each transmitted character are defined by these three inputs. The character word length does not include the parity bit and is common to both the transmitter and receiver if operating in the full duplex mode.

NSB	NDB2	NDB1	BITS/CHARACTER	STOP BITS
V_{IL}	V_{IL}	V_{IL}	5	1
V_{IL}	V_{IL}	V_{IH}	6	1
V_{IL}	V_{IH}	V_{IL}	7	1
V_{IL}	V_{IH}	V_{IH}	8	1
V_{IH}	V_{IL}	V_{IL}	5	1.5
V_{IH}	V_{IL}	V_{IH}	6	2
V_{IH}	V_{IH}	V_{IL}	7	2
V_{IH}	V_{IH}	V_{IH}	8	2

(35)	NPB	NO PARITY BIT. A V_{IH} eliminates the PARITY bit from being transmitted causing the STOP bit(s) to immediately follow the last data bit. The receiver assumes the bit(s) following the last data bit to be STOP bits. The RPE output is also forced to a V_{OL} condition.
(39)	POE	PARITY ODD/EVEN. If the NPB input is V_{IL}, the parity mode is ODD if POE is V_{IL} and EVEN if POE is V_{IH}. The parity mode is the same for both the transmitter and receiver.
(34)	CS	CONTROL STROBE. A V_{IH} loads POE, NDB1, NDB2, NPB, NSB into the CONTROL HOLDING REGISTER. To load the control inputs for static operation CS can be hard-wired to V_{IH}.
(26)	DB1	TRANSMITTER DATA BITS. Input data on DB1-DB8 are strobed into the DATA INPUT
(27)	DB2	HOLDING REGISTER by $\overline{TDS}$.
(28)	DB3	Input data is assumed right justified so DB1 is always the least significant bit and is the bit
(29)	DB4	
(30)	DB5	

Pin	Label	Function
(31)	DB6	transmitted following the START bit. For data words less than eight bits, the unused bits are
(32)	DB7	don't care inputs.
(33)	DB8	
(23)	$\overline{TDS}$	TRANSMITTER DATA STROBE. A V_{IL} enters data on the DB1-DB8 inputs into the INPUT HOLDING REGISTER. If the transmitter is in the idle state with both TBMT and TEOC at V_{OH}, the START bit will be generated on the first negative transition of the input clock TCP following the return of $\overline{TDS}$ to a V_{IH} state.
(25)	TSO	TRANSMITTER SERIAL OUTPUT. Data entered on DB1-DB8 are serially transmitted on TSO. A START (SPACE) bit precedes each character. A PARITY bit, if selected, and the correct number of STOP bits follow the last valid data bit. The TSO output is V_{OH} (MARK) when a valid character is not being transmitted.
(22)	TBMT	TRANSMITTER BUFFER EMPTY. A V_{OH} indicates the character in the INPUT HOLDING REGISTER has been transferred into the transmitter and a new character may be loaded into the INPUT HOLDING REGISTER. One complete character time (START BIT, DATA BITS, PARITY BIT, AND STOP BIT(S)) is available to load the next character. If a $\overline{TDS}$ is not generated within the time allotted, the TSO output will go into an idle state of V_{OH} or a MARK condition. TBMT will remain in the tri state mode unless $\overline{SWE}$ is a U_{ZL}.
(24)	TEOC	TRANSMITTER END OF CHARACTER. A V_{OL} to V_{OH} transition indicates the transmission of the character and stop bits have been completed. The V_{OH} is maintained until the leading edge of the next START bit (MARK to SPACE transition) is generated.
(40)	TCP	TRANSMITTER CLOCK PULSE. The transmitter input clock must be 16 times faster than the desired baud rate at TSO.
(17)	RCP	RECEIVER CLOCK PULSE. The receiver input clock must be 16 times the baud rate of data received on RSI.
(20)	RSI	RECEIVER SERIAL INPUT. Serial input data is received on RSI at a baud rate 1/16th the rate of RCP. The V_{IH} to V_{IL} (MARK to SPACE) transition beginning each START bit synchronizes the receiver to the incoming data. Data is assumed to be received least significant bit first.
(12)	RD1	RECEIVER DATA. Data outputs from the DATA OUTPUT HOLDING REGISTER are
(11)	RD2	active only when $\overline{RDE}$ is a V_{IL}. The eight data outputs are in a tri-state mode if $\overline{RDE}$ is a
(10)	RD3	V_{IH}. Data is presented at the outputs right justified with RDI the least significant bit. For
(9)	RD4	data word lengths less than 8 bits the unused bits will appear as V_{OL}.
(8)	RD5	
(7)	RD6	
(6)	RD7	
(5)	RD8	
(4)	$\overline{RDE}$	RECEIVER DATA ENABLE. A V_{IL} enables data in the DATA OUTPUT HOLDING REGISTER to the RECEIVER DATA output pins. For an output configuration not requiring a tri-state condition for RD1-RD8 the RDE input can be tied directly to ground enabling the data outputs at all times.
(19)	ODA	OUTPUT DATA AVAILABLE. A V_{OH} indicates a complete character has been received and transferred to the DATA OUTPUT HOLDING REGISTER. The ODA output will be in the tri-state mode unless $\overline{SWE}$ is a V_{IL}. For contiguous data inputs on RSI data will remain in the holding register one character time before being lost.
(18)	$\overline{RDA}$	RESET DATA AVAILABLE. A V_{IL} resets the ODA to a V_{OL}. If ODA is not reset by $\overline{RDA}$ the ROR will be set when the next complete character is received and transferred to the DATA OUTPUT HOLDING REGISTER.
(15)	ROR	RECEIVER OVERRUN. A V_{OH} indicates a second character has been received and transferred to the DATA OUTPUT HOLDING REGISTER without an intervening $\overline{RDA}$. If the previously received character has not been unloaded from the register the next character will be loaded and the first character lost. ROR will remain in the tri-state mode unless $\overline{SWE}$ is a V_{IL}.
(14)	RFE	RECEIVER FRAMING ERROR. A V_{OH} indicates a correct STOP bit was not received following the START bit and correct number of data bits. RFE will remain in the tri-state mode unless $\overline{SWE}$ is a V_{IL}.

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Pin	Label	Function
(13)	RPE	RECEIVER PARITY ERROR. A V_{OH} indicates the accumulated parity on the received character does not compare with the parity mode set by POE. RPE will remain in the tri-state mode unless $\overline{SWE}$ is a V_{IL}.
(16)	$\overline{SWE}$	STATUS WORD ENABLE. A V_{IL} enables the status outputs ODA, ROR, RFE, RPE and TBMT on the respective output lines. When $\overline{SWE}$ is V_{IH} all status outputs are in the tri-state mode. For output configurations not requiring a tri-state condition for the status outputs, $\overline{SWE}$ may be tied directly to ground.

APPLICATION DATA

Asynchronous data communications is typified by low data rates, non-contiguous data messages, and a MARK condition on the line between characters. As a result, each data character must be framed for recognition by START and STOP bits. The S1883 UART provides all the logic required to provide a complete full-duplex (transmit and receive simultaneously) asynchronous communication channel for baud rates up to 9600 bps. Included in the S1883 capabilities are; automatic START and STOP bit generation and detection; PARITY generation and detection on variable length characters; tri-state outputs for data and status for data bus configurations, double buffering for less critical timing, and a receiver allowing acceptance of data with up to 42% distortion.

RECEIVER OPERATION

Asynchronous communication line discipline dictates that each character, regardless of width, must be preceded by a START bit. The receiver input logic detects the V_{IH} to V_{IL} (MARK to SPACE) transition on the RSI line that is the leading edge of the START bit. For one half bit time after the leading edge, RSI is sampled for a V_{IL} to insure a proper START bit was present. The following data bits are then clocked into the receiver in the center of each bit period. If RSI returns to the V_{IH} condition before the mid-point of the START bit, the receiver returns to a search for a MARK to SPACE transition.

If at the time of transfer ODA has not been reset by a $\overline{RDA}$, indicating the previous character has not been read, the ROR error flag is set to V_{OH}. The previous data character and status will be lost as the new character is loaded. One full character time is available, assuming contiguous data input at RSI, after ODA is set to read the output character. The data is available at the outputs RD1-RD8 right justified with RD1 the least significant bit. For character widths less than 8 bits the unused outputs are forced to V_{OL}.

For data bus configurations the output data and status are tri-state lines enabled by $\overline{RDE}$ and $\overline{SWE}$ respectively. For polled systems $\overline{SWE}$ can be strobed for detection of ODA and error conditions prior to reading data. For interrupt driven systems $\overline{SWE}$ can be tied directly to ground and ODA used as a data ready interrupt input. A minimum of one character time is available to test the remaining error status bits and input the data character. Typically the same signal can be used for $\overline{RDE}$ and $\overline{RDA}$.

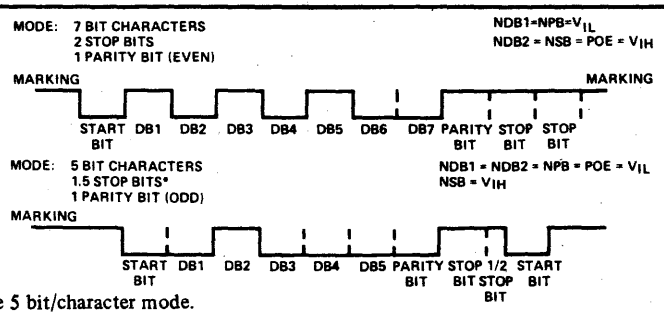
TRANSMITTER OPERATION

The transmit section of the S1883 is reset to a MARK condition with V_{OH} on TSO after receiving a pulse on RESET. Additionally, the transmitter is reset to a character request mode with TBMT and TEOC both at V_{OH}. If the character format is not static, the word length NDB1 and NDB2, parity mode NPB and POE, and number of stop bits NSB should be strobed into the UART with CS.

If both the DATA INPUT HOLDING REGISTER and the TRANSMITTER SHIFT REGISTER are empty the transmitter is in the idle state with TSO, TBMT and TEOC all at V_{OH}. The START bit for a data character loaded with a $\overline{TDS}$ pulse during the idle state is generated at the first negative transition of the TCP following the trailing edge of $\overline{TDS}$. TBMT goes to V_{OL} with the first $\overline{TDS}$. As soon as the character is transferred from the INPUT HOLDING REGISTER to the SHIFT REGISTER, TBMT returns to a V_{OH} and a second character can be loaded. Each character is transmitted with a START bit and 1, 1.5 or 2 stop bits controlled by the respective inputs.

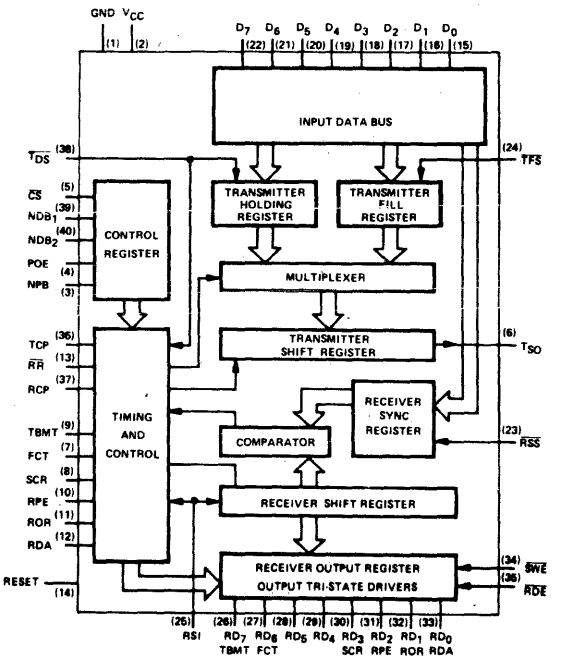
The TEOC is set to V_{OH} after the generation of the last STOP bit indicating the complete character has been transmitted.

TYPICAL DATA FORMAT

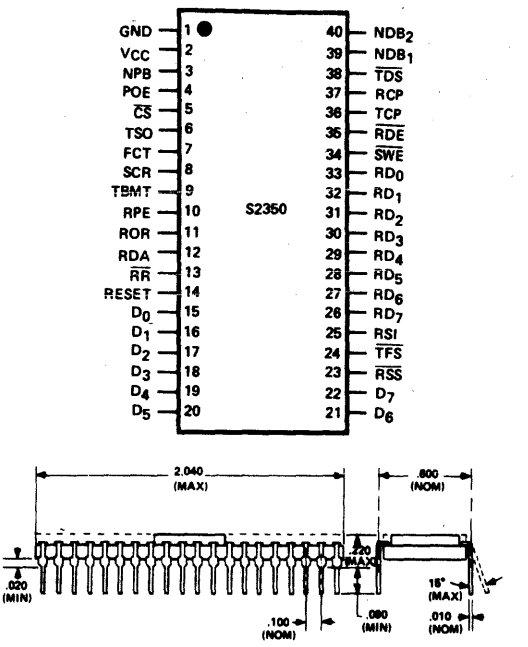


*1.5 stop bits generated only in the 5 bit/character mode.

Universal Synchronous Receiver/Transmitter (USRT)



BLOCK DIAGRAM



PIN/PACKAGE CONFIGURATION

FEATURES

- 500 KHz Data Rates
- Internal Sync Detection
- Fill Character Register
- Double Buffered Input/Output
- Bus Oriented Outputs
- 5–8 Bit Characters
- Odd/Even or No Parity
- Error Status Flags
- Single Power Supply (+5v)
- Input/Output TTL Compatible

FUNCTIONAL DESCRIPTION

The S2350 Universal Synchronous Receiver Transmitter (USRT) is a single chip MOS/LSI device that totally replaces the serial to parallel and parallel to serial conversion logic required to interface a word parallel controller or data terminal to a bit-serial, synchronous communication network.

The USRT consists of separate receiver and transmitter sections with independent clocks, data lines and status. Common with the transmitter and receiver are word length and parity mode. Data is transmitted and received in a NRZ format at a rate equal to the respective input clock frequency.

Data messages are transmitted as a contiguous character stream, bit synchronous with respect to a clock and character synchronous with respect to framing or "sync" characters initializing each message. The USRT receiver compares the contents of the internal Receiver Sync Register with the incoming data stream in a bit transparent mode. When a compare is made, the receiver becomes character synchronous formatting a 5, 6, 7, or 8 bit character for output each character time. The receiver has an output buffer register allowing a full character time to transfer the data out. The receiver status outputs indicate received data available (RDA), receiver overrun (ROR), receive parity error (RPE) and sync character received (SCR). Status bits are available on individual output lines and can also be multiplexed onto the output data lines for bus organized systems. The data lines have tri-state outputs.

The USRT transmitter outputs 5, 6, 7, or 8 bit characters with correct parity at the transmitter serial output (TSO). The transmitter is buffered to allow a full character time to respond to a transmitter buffer empty (TBMT) request for data. Data is transmitted in a NRZ format changing on the positive transition of the transmitter clock (TCP). The character in the transmitter fill register is inserted into the data message if a data character is not loaded into the transmitter after a TBMT request.

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TYPICAL APPLICATIONS

- Computer Peripherals
- Communication Concentrators
- Integrated Modems
- High Speed Terminals
- Time Division Multiplexing
- Industrial Data Transmission

ABSOLUTE MAXIMUM RATINGS

Ambient temperature under bias	0°C to + 70°C
Storage temperature	−65°C to +150°C
Positive voltage on any pin with respect to GROUND	+7 volt
Negative voltage on any pin with respect to GROUND	−0.5 volt
Power dissipation	0.75 watt

DC (STATIC) CHARACTERISTICS*

V_{CC} = +5V ±5V ±5%, T_A = 25°C unless otherwise noted.

Symbol	Parameter	Min.	Max.	Unit	Condition
V_{IH}	Input High Voltage	2.0	V_{CC}	Volt	
V_{IL}	Input Low Voltage	- 0.5	+0.8	Volt	
I_{IL}	Input Leakage Current		10	μa	V_{IN} = OTO V_{CC} Volts
V_{OH}	Output High Voltage	2.4		Volts	I_{OH} = −100μa
V_{OL}	Output Low Voltage		+0.4	Volts	I_{OL} = 1.6ma
C_{IN}	Input Capacitance		10	pf	V_{IN} = 0 Volt, f = 1.0 MHZ
C_{OUT}	Output Capacitance		12	pf	V_{IN} = 0 Volt, f = 1.0 MHZ
I_{CC}	V_{CC} Supply Current		100	ma	No Load

*Electrical characteristics included in this advanced product description are objective specifications and may be subject to change.

AC (DYNAMIC) CHARACTERISTICS

V_{CC} = +5V ±5%, T_A = 25°C unless otherwise noted.

Symbol	Parameter	Min.	Max.	Unit	Condition
TCP, RCP	Clock Frequency	DC	500	KHz	

Input Pulse Widths

P_{TCP}	Transmit Clock	900		nsec	C_L = 20pf
P_{RCP}	Receive Clock	900		nsec	1TTL Load
P_{RST}	Reset	500		nsec	
$P_{\overline{TDS}}$	Transmit Data Strobe	200		nsec	
$P_{\overline{TFS}}$	Transmit Fill Strobe	200		nsec	
$P_{\overline{RSS}}$	Receive Sync Strobe	200		nsec	
$P_{\overline{CS}}$	Control Strobe	200		nsec	
$P_{\overline{RDE}}$	Receive Data Enable	400		nsec	Note 1
$P_{\overline{SWE}}$	Status Word Enable	400		nsec	Note 1
$P_{\overline{RR}}$	Receiver Restart	500		nsec	

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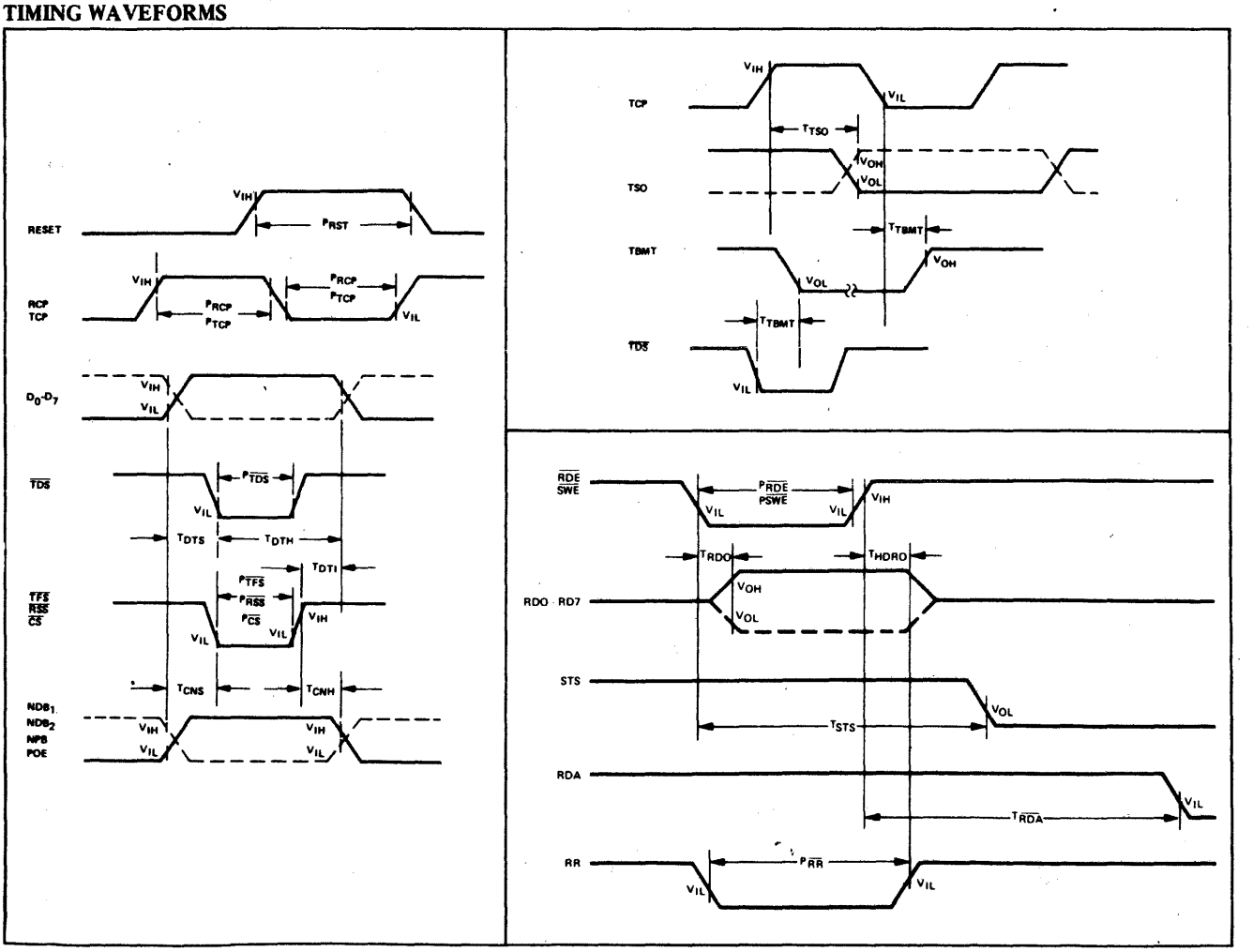
AC (DYNAMIC) CHARACTERISTICS (CONT'D)

SWITCHING CHARACTERISTICS

T_{TSO}	Delay, TCP Clock to Serial Data Out		700	nsec	
T_{TBMT}	Delay, TCP Clock to TBMT Output		1.4	μsec	
T_{TBMT}	Delay, $\overline{TDS}$ to TBMT		700	nsec	
T_{STS}	Delay, $\overline{SWE}$ to Status Reset		700	nsec	
T_{RDO}	Delay, $\overline{SWE}$, $\overline{RDE}$ to Data Outputs		400	nsec	1TTL Load
T_{HRDO}	Hold Time $\overline{SWE}$, $\overline{RDE}$ to Off State		400	nsec	C_L = 130 pf
T_{DTS}	Data Set Up Time $\overline{TDS}$, $\overline{TFS}$, $\overline{RSS}$, $\overline{CS}$	0		nsec	
T_{DTH}	Data Hold Time $\overline{TDS}$	700		nsec	
T_{DTI}	Data Hold Time $\overline{TFS}$, $\overline{RSS}$	200		nsec	
T_{CNS}	Control Set Up Time NDB1, NDB2, NPB, POE	0		nsec	
T_{CNH}	Control Hold Time NDB1, NDB2, NPB, POE	200		nsec	
T_{RDA}	Delay $\overline{RDE}$ to $\overline{RDA}$ Output	700		nsec	

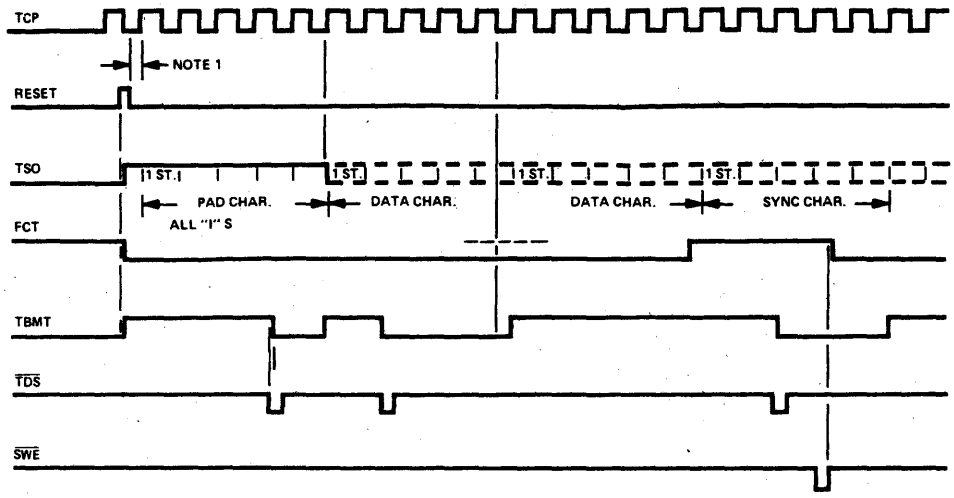
NOTE 1: Required to reset status and flags.

TIMING WAVEFORMS



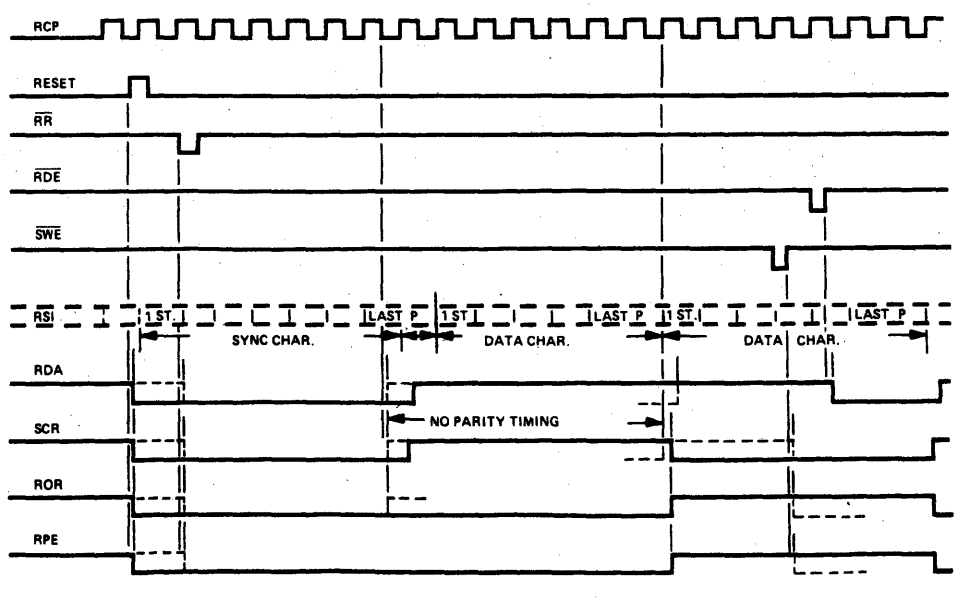
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TRANSMITTER TIMING DIAGRAM



NOTE 1 DATA TRANSMISSION WILL START ON THE FIRST LOW TO HIGH TRANSITION OF TCP AFTER RESET IS LOW. THE INITIAL RESET PULSE SHOULD NOT OCCUR UNTIL 100 MICROSECONDS AFTER POWER IS APPLIED.

RECEIVER TIMING DIAGRAM



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DIGITAL TONE GENERATOR

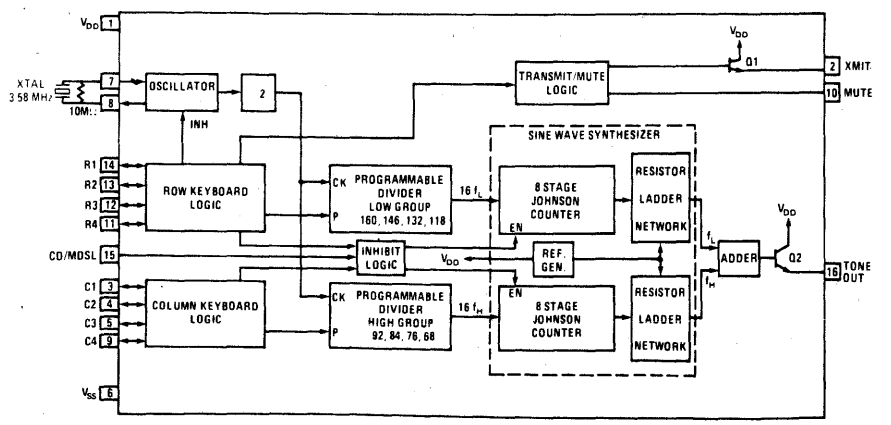
Features

- ☐ Wide Operating Supply Voltage Range: 3.5 to 13 Volts (A, B) 2.75 to 10 Volts (C, D)
- ☐ Low Power CMOS Circuitry Allows Device Power to be Derived Directly from the Telephone Lines or from Small Batteries, e.g., 9V.
- ☐ Uses TV Crystal Standard (3.58MHz to Derive all Frequencies thus Providing Very High Accuracy and Stability
- ☐ MUTE and Transmitter Drivers On Chip
- ☐ Interfaces Directly to a Standard Telephone Push-Button or Calculator Type X-Y Keyboard
- ☐ The Total Harmonic Distortion is Below Industry Specification
- ☐ On Chip Generation of a Reference Voltage to Assure Amplitude Stability of the Dual Tones Over the Operating Voltage and Temperature Range
- ☐ Dual Tone as well as Single Tone Capability
- ☐ Four Options Available:
  - A: 3.5 to 13V Mode Select
  - B: 3.5 to 13V Chip Disable
  - C: 2.75 to 10V Mode Select
  - D: 2.75 to 10V Chip Disable

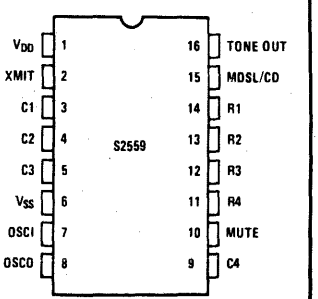
General Description

The S2559 Digital Tone Generator is specifically designed to implement a dual tone telephone dialing system. The device can interface directly to a standard pushbutton telephone keyboard or calculator type X-Y keyboard and operates directly from the telephone lines. All necessary dual-tone frequencies are derived from the widely used TV crystal standard providing very high accuracy and stability. The required sinusoidal waveform for the individual tones is digitally synthesized on the chip. The waveform so generated has very low total harmonic distortion. A voltage reference is generated on the chip which is stable over the operating voltage and temperature range and regulates the signal levels of the dual tones to meet the recommended telephone industry specifications. These features permit the S2559 to be incorporated with a slight modification of the standard 500 type telephone basic circuitry to form a pushbutton dual-tone telephone. Other applications of the device include radio and mobile telephones, remote control, Point-of-Sale, and Credit Card Verification Terminals and process control.

Block Diagram



Pin Configuration



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Absolute Maximum Ratings

DC Supply Voltage ($V_{DD} - V_{SS}$) S2559 A, B ..... +13.5V
DC Supply Voltage ($V_{DD} - V_{SS}$) S2559 C, D ..... +10.5V
Operating Temperature ..... −25°C to +70°C
Storage Temperature ..... −55°C to +125°C
Power Dissipation at 25°C 500mW
Input Voltage ..... $-0.6 \leqslant V_{in} \leqslant V_{DD} + 0.6$

S2559A & B Electrical Characteristics (Specifications apply over the operating temperature range of -25°C to +70°C unless otherwise noted. Absolute values of measured parameters are specified.)

Symbol	Parameter/Conditions		(V_{DD}-V_{SS}) Volts	Min.	Typ.	Max.	Units
	Supply Voltage						
V_{DD}	Tone Out Mode with One Valid Key Depressed			3.5		13.0	V
V_{DD}	Non Tone Out Mode (No Keys Depressed)			2.5		13.0	V
	Supply Current						
I_{DD}	Standby (No Keys Selected, Tone, MUTE and XMIT Outputs Unloaded)		13.0			130	μA
I_{OD}	Operating (One Key Selected, Tone, MUTE and XMIT Outputs Unloaded)		5.0			18	mA
	Tone Output[1]						
V_{OR}	Single Tone Mode, Output Voltage	Row Tone R_L = 600Ω	5.0	490		660	mVrms
		Row Tone R_L = 320Ω	12.0	440		600	mVrms
V_{OC}		Column Tone R_L = 600Ω	5.0	650		880	mVrms
		Column Tone R_L = 320Ω	12.0	590		790	mVrms
dB_{CR}	Ratio of Column to Row Tone		3.5-13.0	1.75	2.85	3.7	dB
% DIS	Distortion (Any Dual Tone)*		3.5-13.0			10	%
	XMIT, MUTE Outputs						
V_{OH}	XMIT, Output Voltage High (Pin 2) No Key Depressed	I_{OH} = 15mA	3.5	1.5			V
		I_{OH} = 50mA	10.0	8.0			V
V_{OL}	MUTE Output Voltage (Pin 10) Low No Key Depressed, No Load		3.5			0.4	V
			13.0			1.0	V
V_{OH}	One Key Depressed, No Load		3.5	2.6			V
			13.0	10.0			V
I_{OL}	MUTE Output Sink Current	V_{OL} = 0.5V	3.0	0.2			mA
			10.0	0.5			mA
I_{OH}	MUTE Output Source Current	V_{OH} = 2V	3.0	0.5			mA
		V_{OH} = 9V	10.0	0.5			mA
	Oscillator						
I_{OH}	Output Current	Sink V_{IL} = 0.5V	3.5	0.34			mA
		Source V_{IH} = 3.0V	3.5	0.23			mA
t_{SU}	Startup Time		3.5			6.0	mS
	Input Currents						
I_{IH}	Row, Column Inputs, Pull-up (Source) Current	V_{IH} = 3.0V	3.5			0.45	mA
		V_{IH} = 12.5V	13.0			1.48	mA
I_{IL}	Pull-down (Sink) Current	V_{IL} = 2.1V	3.5			0.1	mA
		V_{IL} = 9.1V	13.0			0.6	mA

*Distortion measured in accordance with the specification described in Ref. 1 as the "ratio of the total power of all extraneous frequencies in the voiceband above 500Hz accompanying the signal to the total power of the frequency pair."
[1]Amplitude specification limits apply at room temperature (+25°C) only.

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S2559C & D Electrical Characteristics (Specifications apply over the operating temperature range of -25°C to +70°C unless otherwise noted. Absolute values of the measured parameters are specified.)

Symbol	Parameter/Conditions		(V_{DD}-V_{SS}) Volts	Min.	Typ.	Max.	Units
	Supply Voltage						
V_{DD}	Tone Out Mode with Valid Key Depressed			2.75		10.0	V
	Non Tone Out Mode (No Key Depressed)			2.25		10.0	V
	Supply Current						
I_{DD}	Standby (No Key Selected, Tone, XMIT and MUTE Outputs Unloaded)		3.0		0.3	30	μA
			10.0		1.0	100	μA
	Operating (One Key Selected, Tone XMIT and MUTE Outputs Unloaded)		3.0		1.0	2.0	mA
			10.0		8.0	16.0	mA
	Tone Output[1]						
V_{OR}	Single Tone Mode Output Voltage	Row Tone, R_L = 390Ω	5.0	424	546	667	mVrms
		Row Tone, R_L = 240Ω	10.0	376	501	626	mVrms
V_{OC}		Column Tone, R_L = 390Ω	5.0	573	731	889	mVrms
		Column Tone, R_L = 240Ω	10.0	504	672	840	mVrms
dB_{CR}	Ratio of Column to Row Tone		3.0-10.0	1.75	2.54	3.75	dB
% DIS	Distortion (Any Dual Tone)*		3.0-10.0			10	%
	XMIT, MUTE Outputs						
V_{OH}	XMIT, Output Voltage, High (No Key Depressed) (Pin 2)	(I_{OH} = 15mA)	3.0	1.5	1.8		V
		(I_{OH} = 50mA)	10.0	8.5	8.8		V
I_{OF}	XMIT, Output Source Leakage Current, V_{OF} = 0V		10.0			100	μA
V_{OL}	MUTE (Pin 10) Output Voltage, Low, (No Key Depressed), No Load		2.75		0	0.5	V
			10.0		0	0.5	V
V_{OH}	MUTE, Output Voltage, High, (One Key Depressed), No Load		2.75	2.25	2.75		V
			10.0	9.5	10.0		V
I_{OL}	MUTE, Output Sink Current	V_{OL} = 0.5V	3.0	0.53	1.3		mA
			10.0	2.0	5.3		mA
I_{OH}	MUTE, Output Source Current	V_{OH} = 2.5V	3.0	0.17	0.41		mA
		V_{OH} = 9.5V	10.0	0.57	1.5		mA
	Oscillator Input/Output						
I_{OL}	Output Sink Current One Key Selected	V_{OL} = 0.5V	3.0	0.21	0.52		mA
		V_{OL} = 0.5V	10.0	0.80	2.1		mA
I_{OH}	Output Source Current One Key Selected	V_{OH} = 2.5V	3.0	0.13	0.31		mA
		V_{OH} = 9.5V	10.0	0.42	1.1		mA
I_{IL}	Input Current						
	Leakage Sink Current, One Key Selected	V_{IL} = 10.0V	10.0			1.0	μA
I_{IH}	Leakage Source Current One Key Selected	V_{IH} = 0.0V	10.0			1.0	μA
I_{IL}	Sink Current No Key Selected	V_{IL} = 0.5V	3.0	47	93		μA
		V_{IL} = 0.5V	10.0	65	130		μA
t_{START}	Oscillator Startup Time		2.75		0.4	1.2	mS
			10.0		0.25	0.75	mS
$C_{I/O}$	Input/Output Capacitance		3.0		12	16	pF
			10.0		10	14	pF

[1] Amplitude specification limits apply at room temperature (+25°C) only.

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S2559C & D Electrical Specifications (continued)

Symbol	Parameter/Conditions		(V_{DD}–V_{SS}) Volts	Min.	Typ.	Max.	Units
	Input Currents						
I_{IL}	Row & Column Inputs	Sink Current, V_{IL} = 3.0V (Pull-down)	3.0	6.5	16		μA
		Sink Current, V_{IL} = 10.0V (Pull-down)	10.0	9.2	24		μA
I_{IH}		Source Current, V_{IH} = 2.5V (Pull-up)	3.0	85	210		μA
		Source Current, V_{IH} = 9.5V (Pull-up)	10.0	280	740		μA
I_{IH}	Mode Select Input (S2559C)	Source Current, V_{IH} = 0.0V (Pull-up)	3.0	1.4	3.3		μA
		Source Current, V_{IH} = 0.0V (Pull-up)	10.0	18	46		μA
I_{IL}	Chip Disable Input (S2559D)	Sink Current, V_{IL} = 3.0V (Pull-down)	3.0	3.9	9.5		μA
		Sink Current, V_{IL} = 10.0V (Pull-down)	10.0	55	143		μA

*Distortion measured in accordance with the specification described in Ref. 1 as the "ratio of the total power of all extraneous frequencies in the voiceband above 500Hz accompanying the signal to the total power of the frequency pair."

Table 1. Comparisons of Specified vs Actual Tone Frequencies Generated by S2559

ACTIVE INPUT	OUTPUT FREQUENCY Hz		% ERROR SEE NOTE
	SPECIFIED	ACTUAL	
R1	697	699.1	+0.30
R2	770	766.2	-0.49
R3	852	847.4	-0.54
R4	941	948.0	+0.74
C1	1,209	1,215.9	+0.57
C2	1,336	1,331.7	-0.32
C3	1,477	1,471.9	-0.35
C4	1,633	1,645.0	+0.73

Table 2. XMIT and MUTE Output Functional Relationship

OUTPUT	'DIGIT' KEY RELEASED	'DIGIT' KEY DEPRESSED	COMMENT
XMIT	V_{DD}	High Impedance	Can source at least 50mA at 10V with 1.5V max. drop
MUTE	V_{SS}	V_{DD}	Can source or sink current

NOTE: % Error does not include oscillator drift.

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KEY PULSER

February 1978

Features

- ☐ Low Voltage CMOS Process for Direct Operation From Telephone Lines
- ☐ Inexpensive R-C Oscillator Design Provides Better than ±5% Accuracy Over Temperature and Unit to Unit Variations
- ☐ Dialing Rate Can Be Varied By Changing the Dial Rate Oscillator Frequency
- ☐ Dial Rate Select Input Allows Changing of the Dialing Rate by a 2:1 Factor Without the Need of Changing Oscillator Components
- ☐ Two Selections of Mark/Space Ratios (33-1/3 /66-2/3 or 40/60)
- ☐ Twenty Digit Memory for Input Buffering and for Redial With Access Pause Capability
- ☐ Mute and Dial Pulse Drivers on Chip
- ☐ Accepts Standard Telephone DPCT Keypad Arranged in a 2 of 7 Format; Also Capable of Logic Interface
- ☐ Ignores Multi Key Entries

General Description

The S2560 Key Pulser is a CMOS integrated circuit that converts pushbutton inputs to a series of pulses suitable for telephone dialing. It is intended as a replacement for the mechanical telephone dial and can operate directly from the telephone lines with minimum interface. Storage is provided for 20 digits, therefore, the last dialed number is available for redial until a new number is entered.

Unique Features of S2560A (18 Pin Package)

IDP scaled to the dialing rate such as to produce smaller IDP at higher dialing rates. Additionally, the IDP can be changed by a 2:1 factor at a given dialing rate by means of the IDP select input.

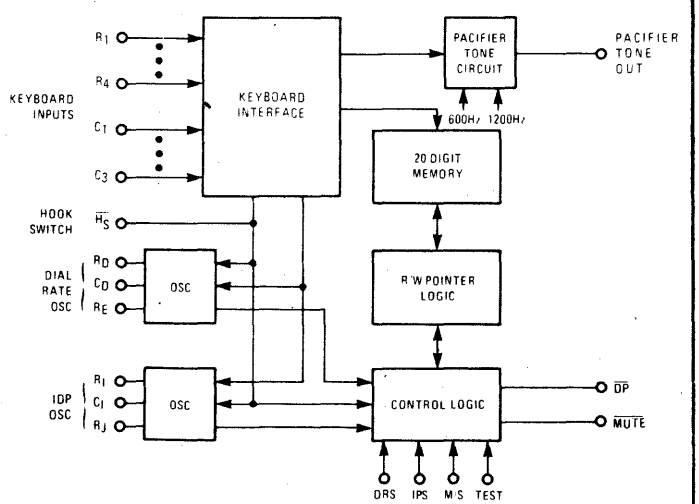
Unique Features of S2560B (24 Pin Package)

Separate IDP oscillator for selecting an IDP independent of the dialing rate. Provision for changing of the IDP by a 2:1 factor without the need of changing external components.

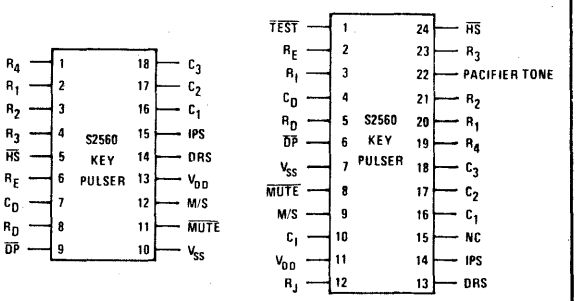
Alternating pacifier tone output simulates dual tone effects coincident with each keyboard number entry.

Data subject to change at any time without notice. These sheets transmitted for information only.

Block Diagram



Pin Configuration



ADVANCED PRODUCT DESCRIPTION

©IC MASTER 1979

Absolute Maximum Ratings

Supply Voltage	+5.5V
Operating Temperature Range	- 40°C to +85°C
Storage Temperature Range	- 40°C to +125°C
Voltage at Any Pin	V_{SS} - 0.3V to V_{DD} + 0.3V
Lead Temperature (Soldering, 10 Seconds)	300°C

Electrical Characteristics Specifications apply over the operating temperature range and 1.5V ≤ V_{DD} to V_{SS} ≤ 3.5V unless otherwise specified. Absolute values of the measured parameters are specified.

Symbol	Parameter	V_{DD} - V_{SS} (Volts)	Min.	Max.	Units	Conditions
	Output Current Levels					
I_{OLDP}	$\overline{DP}$ Output Low (Sink) Current	3.5	125		μA	V_{OUT} = 0.4V
I_{OHDP}	$\overline{DP}$ Output High (Source) Current	1.5 3.5	20 125		μA μA	V_{OUT} = 1V V_{OUT} = 2.5V
I_{OLM}	$\overline{MUTE}$ Output Low (Sink) Current	3.5	125		μA	V_{OUT} = 0.4V
I_{OHM}	$\overline{MUTE}$ Output High (Source) Current	1.5 3.5	20 125		μA μA	V_{OUT} = 1V V_{OUT} = 2.5V
I_{OLT}	Tone Output Low (Sink) Current	1.5	20		μA	V_{OUT} = 0.4V
I_{OHT}	Tone Output High (Source) Current	1.5	20		μA	V_{OUT} = 1V
I_{DD}	Quiescent Current	3.5		1	μA	"On Hook" $\overline{HS}$ = V_{DD}
I_{IL}, I_{IH}	Input Current Any Pin (Keyboard Inputs)	3.5	1	10	μA	V_{IN} = Open or V_{DD}
I_{IL}, I_{IH}	Input Current Any Other Pin	3.5		100	nA	V_{IN} = V_{SS} or V_{DD}
I_{DD}	Operating Current	3.5 3.5		20 60	μA μA	$\overline{DP}$, $\overline{MUTE}$ open, $\overline{HS}$=V_{SS} ("Off Hook") Keyboard processing and dial pulsing space fo = 2400Hz $\overline{DP}$, $\overline{MUTE}$ sourcing 20μA, other conditions as above
fo	Oscillator Frequency	1.5		10	kHz	
Δfo/fo	Frequency Deviation	1.5 to 2.5 2.5 to 3.5	-5 -5	+5 +5	% %	Fixed R-C oscillator components 50kΩ ≤ R_D ≤ 750kΩ; 100pF ≤ C_D* ≤ 3000pF; 1MΩ ≤ R_E ≤ 5MΩ *330pF most desirable value for C_D. Indicated and over the operating temperature range and unit to unit variations
	Input Voltage Levels					
V_{IH}	Logical "1"		V_{DD} - 0.25	V_{DD}	V	
V_{IL}	Logical "0"		V_{SS}	V_{SS} + 0.25	V	
C_{in}	Input Capacitance Any Pin			7.5	pF	

The device power supply should always be turned on before the input signal sources, and the input signals should be turned off before the power supply is turned off (V_{SS} ≤ V_I ≤ V_{DD} as a maximum limit). This rule will prevent over-dissipation and possible damage of the input-protection diode when the device power supply is grounded.

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August 1977

TONE RINGER

Features

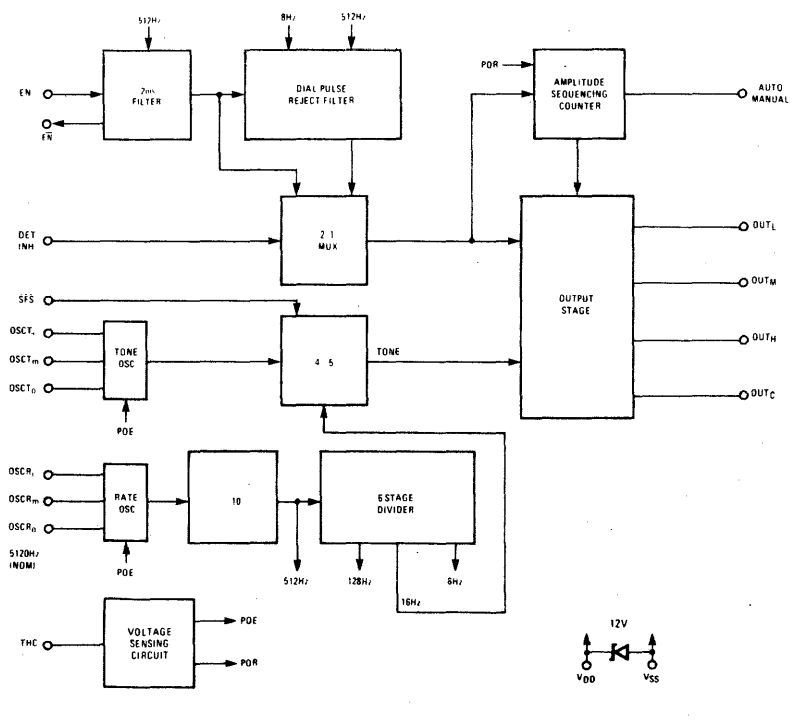
- ☐ CMOS Process for Low Power Operation
- ☐ Operates Directly from Telephone Lines with Simple Interface
- ☐ Also Capable of Logic Interface for Non-Telephone Applications
- ☐ Provides a Tone Signal that Shifts Between Two Predetermined Frequencies at Approximately 16Hz to Closely Simulate the Effects of the Telephone Bell
- ☐ Push-Pull Output Stage Allows Direct Drive, Eliminating Capacitive Coupling and Provides Increased Power Output
- ☐ 50mW Output Drive Capability at 10V Operating Voltage
- ☐ Auto Mode Allows Amplitude Sequencing such that the Tone Amplitude Increases in Each of the First Three Rings and Thereafter Continues at the Maximum Level
- ☐ Single Frequency Tone Capability

General Description

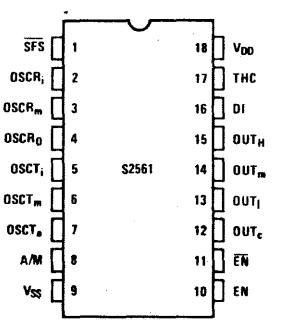
The S2561 Tone Ringer is a CMOS integrated circuit that is intended as a replacement for the mechanical telephone bell. It can be powered directly from the telephone lines with minimum interface and can drive a speaker to produce sound effects closely simulating the telephone bell.

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Block Diagram



Pin Configuration



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Absolute Maximum Ratings

Supply Voltage	+12V
Operating Temperature Range	-25°C to +70°C
Storage Temperature Range	-40°C to +125°C
Voltage at Any Pin	V_{SS} - 0.3V to V_{DD} + 0.3V
Lead Temperature (Soldering, 10sec)	300°C

Electrical Characteristics Specifications apply over the operating temperature range and 3.5V ⩽ V_{DD} to V_{SS} < 12V unless otherwise specified.

Symbol	Parameter	Min.	Max.	Units	Conditions
V_{DS}	Operating Voltage (V_{DD} to V_{SS})	8.0	13.5	V	Ringing, THC pin open
V_{DS}	Operating Voltage	4.0		V	"Auto" mode, non-ringing
I_{DS}	Operating Current		500	μA	Non-ringing, V_{DD} = 10V, THC pin open, DI pin open or V_{SS}
I_{DS}	Operating Current		25	μA	Non-ringing, V_{DD} = 6V, THC pin open
	Output Drive				
I_{OHC}	Output Source Current (OUT_H, OUT_C outputs)	5		mA	V_{DD} = 10V, V_{OUT} = 9V
I_{OLC}	Output Sink Current (OUT_H, OUT_C outputs)	5		mA	V_{DD} = 10V, V_{OUT} = 0.5V
I_{OHM}	Output Source Current (OUT_M output)	2		mA	V_{DD} = 10V, V_{OUT} = 9V
I_{OLM}	Output Sink Current (OUT_M output)	2		mA	V_{DD} = 10V, V_{OUT} = 0.5V
I_{OHL}	Output Source Current (OUT_L output)	1		mA	V_{DD} = 10V, V_{OUT} = 9V
I_{OLL}	Output Sink Current (OUT_L output)	1		mA	V_{DD} = 10V, V_{OUT} = 0.5V
	CMOS to CMOS				
V_{IH}	Input Logic "1" Level	0.7 V_{DD}	V_{DD} + 0.3	V	All inputs
V_{IL}	Input Logic "0" Level	V_{SS} - 0.3	0.3 V_{DD}	V	All inputs
V_{OHR}	Output Logic "1" Level (Rate output)	0.9V_{DD}		V	I_O = 10μA (Source)
V_{OLR}	Output Logic "0" Level (Rate output)		0.5	V	I_O = 10μA (Sink)
V_{OZ}	Output Leakage Current (OUT_H, OUT_M outputs in high impedance state)		1 -1	μA μA	V_{DD} = 10V, V_{OUT} = 0V V_{DD} = 10V, V_{OUT} = 10V
C_{in}	Input Capacitance		7.5	pF	Any pin
Δfo/fo	Oscillator Frequency Deviation	-5	+5	%	Fixed RC component values 1MΩ ⩽ R_{si}, R_{ti} ⩽ 5MΩ; 100kΩ ⩽ R_{sm}, R_{tm} ⩽ 750kΩ 150pF ⩽ C_{so}, C_{to} ⩽ 3000pF 330pF recommended value of C_{so} and C_{to}, supply voltage varied from 9V ± 2V (over temperature and unit-unit variations)
R_{LOAD}	Output Load Impedance Connected Across OUT_H and OUT_C	600		Ω	Tone Frequency Range = 300Hz to 3400Hz
I_{IH}, I_L	Leakage Current, V_{in} = V_{DD} or V_{SS}		100	nA	Any input, except DI pin V_{DD} = 10V
V_{TH}	POE Threshold Voltage	6.5	8	V	
V_Z	Internal Zener Voltage	11	13	V	I_Z = 5mA

The device power supply should always be turned on before the input signal sources, and the input signals should be turned off before the power supply is turned off (V_{SS} ⩽ V_I ⩽ V_{DD} as a maximum limit). This rule will prevent over-dissipation and possible damage of the input-protection diode when the device power supply is grounded.

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June 1978

REPERTORY DIALER

Features

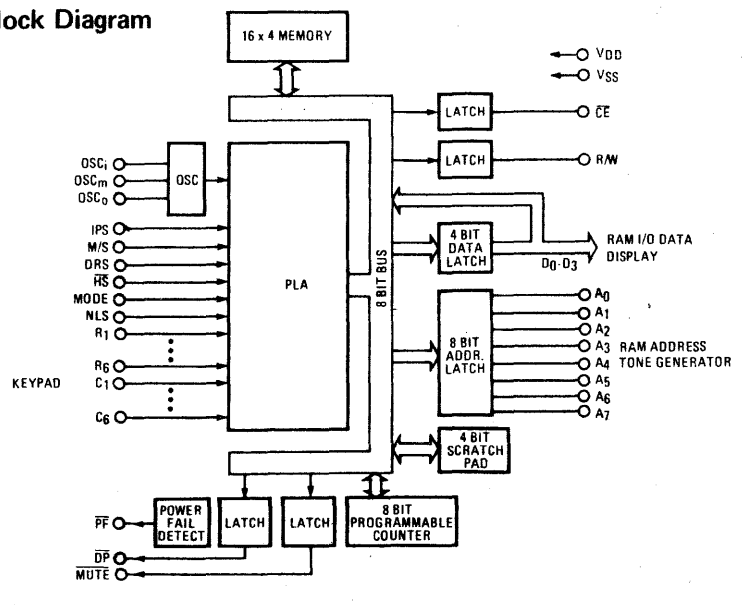
- ☐ CMOS Process Achieves Low Power Operation
- ☐ 8 or 16 Digit Number Capability (Pin Programmable)
- ☐ Dial Pulse and Mute Output
- ☐ Tone Outputs Obtained by Interfacing with Standard AMI S2559 Tone Generator
- ☐ Two Selections of Dial Pulse Rate
- ☐ Two Selections of Inter-Digit Pause
- ☐ Two Selections of Mark/Space Ratio (33-1/3 / 66-2/3 or 40/60)
- ☐ Memory Storage of 32 8-Digit Numbers or 16 16-Digit Numbers with Standard AMI S5101 RAM
- ☐ 16-Digit Memory for Input Buffering and for Redial with Access Pause Capability
- ☐ Accepts the Standard Telephone DPCT Keypad or SPST Switch X-Y Matrix Keyboards; Also Capable of Logic Interface
- ☐ Ignores Multi Key Entries
- ☐ Inexpensive, but Accurate R-C Oscillator Design Provides Better Than ±3% Accuracy Over Supply Voltage, Temperature and Unit-Unit Variations and Allows Different Dialing Rates, IDP and Tone Drive Timing by Changing the Time Base
- ☐ Power Fail Detection
- ☐ BCD Output with Update for Number Display Applications

General Description

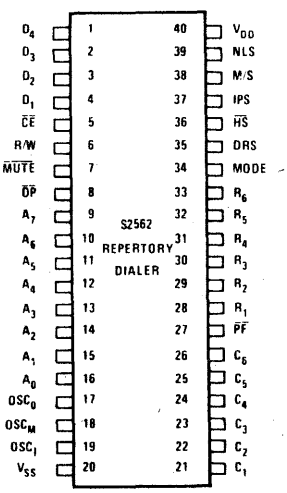
The S2562 Repertory Dialer is a CMOS integrated circuit that can perform storing or retrieving, normal dialing, redialing or auto dialing and displaying of one of several telephone numbers. It is intended to be used with the AMI standard S5101—256x4 RAM that functions as telephone number storage. With one S5101 up to 32 8-digit or 16 16-digit numbers can be stored. It can provide either dial pulses or DTMF tones with the addition of the AMI S2559 tone generator for either the dial or tone line applications.

Data subject to change at any time without notice. These sheets transferred for information only.

Block Diagram



Pin Configuration



ADVANCED PRODUCT DESCRIPTION

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Absolute Maximum Ratings

Supply Voltage	13.5V
Operating Temperature Range	-40°C to +85°C
Storage Temperature Range	-40°C to +125°C
Voltage at Any Pin	V_{SS} -0.3V to V_{DD} +0.3V
Lead Temperature (Soldering, 10 sec.)	200°C

Electrical Characteristics Specifications apply over the operating temperature range and $4.5V \leqslant V_{DD}$ to $V_{SS} \leqslant 5.5V$ unless otherwise specified. Absolute values of measured parameters are specified.

Symbol	Parameter	Min.	Max.	Units	Conditions
	Output Drive				
I_{OLDP}	$\overline{DP}$ Output Sink Current	400		μA	V_{OUT} = 0.4V, V_{DD} = 5V
I_{OHDP}	$\overline{DP}$ Output Source Current	400		μA	V_{OUT} = 3.6V, V_{DD} = 5V
I_{OLM}	$\overline{MUTE}$ Output Sink Current	400		μA	V_{OUT} = 0.4V, V_{DD} = 5V
I_{OHM}	$\overline{MUTE}$ Output Source Current	400		μA	V_{OUT} = 3.6V, V_{DD} = 5V
I_{OLPF}	$\overline{PF}$ Output Sink Current	100		μA	V_{OUT} = 0.4V, V_{DD} = 3V
I_{OHPF}	$\overline{PF}$ Output Source Current	100		μA	V_{OUT} = 3.6V, V_{DD} = 5V
	CMOS to CMOS				
V_{IL}	Logic "0" Input Voltage		1.5	V	All inputs, V_{DD} = 5V
V_{IH}	Logic "1" Input Voltage	3.5		V	All inputs, V_{DD} = 5V
V_{OL}	Logic "0" Output Voltage		0.5	V	All outputs except $\overline{DP}$, $\overline{MUTE}$, $\overline{PF}$, I_O = 10μA, V_{DD} = 5V
V_{OH}	Logic "1" Output Voltage	4.5		V	All outputs except $\overline{DP}$, $\overline{MUTE}$, $\overline{PF}$, I_O = -10μA, V_{DD} = 5V
	Current Levels				
I_{DD}	Quiescent Current		25	μA	Standby, V_{DD} = 5V
I_{DD}	Operating Current		500	μA	All valid input combinations, $\overline{DP}$, $\overline{MUTE}$, $\overline{PF}$ outputs open V_{DD} = 5V
I_{IL}, I_{IH}	Input Current Any Pin (keyboard inputs)	10	100	μA	V_{IN} = V_{SS} or V_{DD}, V_{DD} = 5V
I_{IL}, I_{IH}	Input Current All Other Pins		100	nA	V_{IN} = V_{SS} or V_{DD}, V_{DD} = 5V
I_{OZ}	Output Current in High Impedance State		1 -1	μA μA	V_{DD} = 5V, V_{OUT} = 0V data outputs (D1-D4) V_{DD} = 5V, V_{OUT} = 5V
fo	Oscillator Frequency	4	10	kHz	V_{DD} = 5V (min. duty cycle 30/70)
Δfo/fo	Frequency Deviation	-3	+3	%	V_{DD} - V_{SS} from 4.5V to 5.5V. Fixed R-C oscillator components $50k\Omega \leqslant R_M \leqslant 750k\Omega$; $1M\Omega \leqslant R_I \leqslant 5M\Omega$; $150pF \leqslant C_O \leqslant 3000pF$; 330pF most desirable value for C_O, fo < 10kHz over the operating temperature and unit-unit variations
C_{IN}	Input Capacitance, Any Pin		7.5	pF	

The device power supply should always be turned on before the input signal sources, and the input signals should be turned off before the power supply is turned off ($V_{SS} \leqslant V_I \leqslant V_{DD}$ as a maximum limit). This rule will prevent over-dissipation and possible damage of the input-protection diode when the device power supply is grounded.

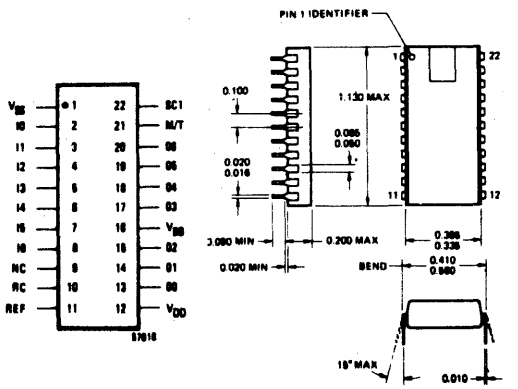
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TouchControl™ Interface

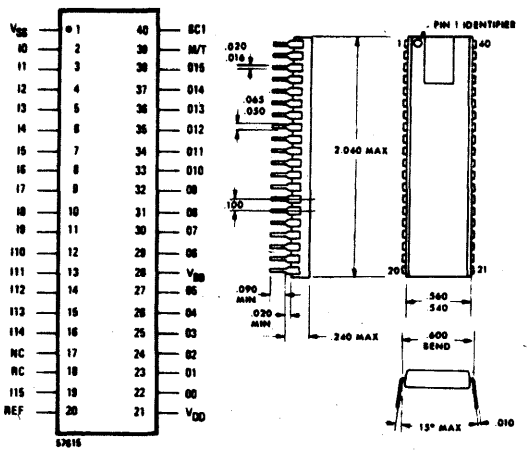
Features

- Interfaces with up to 16 Touch Switches
- Eliminates Contact Noise
- Comparator Sensing Permits Use with Wide Variety of Touch Switch Configurations
- Momentary or Toggle Operation Electrically Selectable
- Outputs are TTL/CMOS/MOS Compatible
- Simplifies Design of Touch-Sensitive Switches

ADVANCED PRODUCT DESCRIPTION



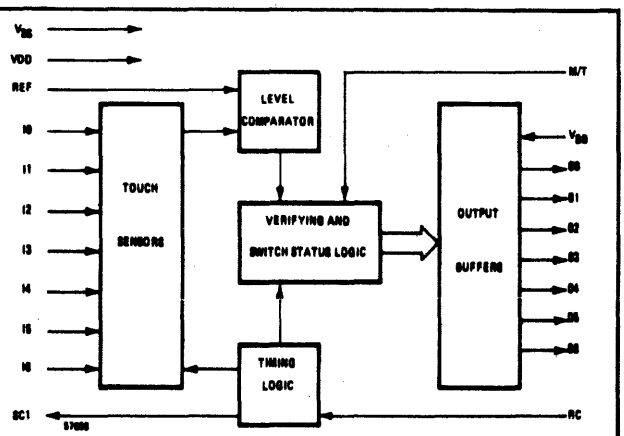
PIN/PACKAGE CONFIGURATION
S9260/S9261



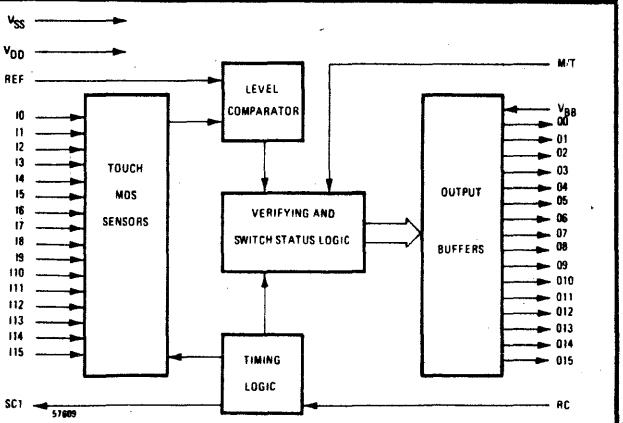
PIN/PACKAGE CONFIGURATION
S9263/S9264/S9265

General Description

These TouchControl interface circuits can be connected to either seven (S9260/S9261) or sixteen (S9263/S9264/S9265) touch switches. For each switch input, there is a corresponding separate output. The outputs are open drain with their sources connected in common to supply input V_{BB}. This permits the driving of TTL as well as MOS circuits, by varying the V_{BB} voltage. The M/T input controls operation of the outputs. In the momentary mode (M) output is active only while the touch switch is being activated (touched by the operator). In the toggle mode (T), alternate actuations of a touch switch will cause its associated output to latch either on or off. On the S9260 and S9263, the M/T input affects all outputs. On the S9261, S9264, and S9265, several switch inputs are permanently fixed in the momentary mode, thus allowing both momentary and toggle switch actuation to be implemented simultaneously.



BLOCK DIAGRAM – S9260/S9261 (7 SWITCHES)



BLOCK DIAGRAM – S9263/S9264/S9265 (16 SWITCHES)

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ABSOLUTE MAXIMUM RATINGS

Voltage on any pin relative to V_{SS}:	+0.3V to -20V	Storage temperature (Ambient)	- 65°C to + 150°C
Operating temperature range:	0°C to +70°C		

**FOR MULTIPLEXED TOUCHCONTROL CIRCUITS SEE AMI S9262 and S9266.*

ELECTRICAL CHARACTERISTICS

($0°C < T_A < 70°C$, $V_{SS} = 0V$; $V_{DD} = 13.5V$ to $-18.0V$ unless otherwise specified.)

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
V_{IL}	Input logic 0 level – all except "I" inputs.	+ 0.3	0	- 1.5	Volts	Note: M/T input is internally pulled up to V_{SS}
V_{IH}	Input logic 1 level – all except "I" inputs	- 10.0	- 12.0	- 18.0	Volts	
f_{RC}	Internal oscillator frequency measured at RC input.	50		100	kHz	
T_S	Switch delay time	50		200	msec	Frequency measured at RC Input = 50 kHz
T_{RST}	Time to reset all latches using M/T input.		100		msec	
V_{OL}	Output low voltage	V_{SS}		- 1.0	Volts	$V_{BB} = V_{SS}$; 10K resistive load to V_{DD}
V_{OH}	Output high voltage			V_{DD}		
V_{OL}	Output low voltage	V_{SS}		V_{SS} - 0.5	Volts	$V_{SS} = +5V$; $V_{BB} = 0V$ $V_{DD} = 12V$; 2800Ω resistive load to V_{SS}
V_{OH}	Output high voltage	V_{BB} + 0.4		V_{BB}		
SC1	Scan clock output:					Max. capacitive loading < 150 pF
	Output low voltage	V_{SS}		- 1.5		
	Output high voltage			V_{DD}		

OPERATION

Device operation can be understood by referring to Figure 1, depicting a typical application of the S9263. Each of the sixteen pairs of series capacitors labeled S1 – S16 is one touch switch located on a TouchControl panel. (For details on touch panel configuration and operation, see the TouchControl application note included in this APD.) In each capacitor pair, the two common plates represent the conductive area on the control panel surface that is to be touched. The other two plates are formed by two conductive surfaces parallel to the touched surface and located directly under it on the reverse side of the panel. Referring again to Figure 1, the S9263 generates a clock signal on output SC1 that is applied to one plate of each capacitor pair; this signal passes through the two series capacitors and is detected in the MOS circuit. When a panel switch surface is touched, the signal level into the chip dimishes, and the on-chip differential amplifier senses the change and performs the appropriate switching function. For example, if surface S1 is touched, the signal at input 13 decreases, and output 03, normally open, now becomes active and drives the S1 input to the TTL circuitry toward voltage level V_{BB}.

I INPUTS

Inputs from the touch switch pads to the TouchControl circuit are labeled I0 through I15 (S9263, S9264, and S9265) or I0 through I6 (S9260 and S9261). Each I input relates directly to an O output of identical numeral.

RC INPUT

A resistor connected to V_{DD} and a capacitor connected to V_{SS} are connected to the RC input pin to establish the on-chip clock frequency that controls the touch switch delay time. Nominal values for these components are suggested in Figure 1, but they may be varied to change clock frequency over a range of 50 kHz to 100 kHz.

REF INPUT

In order to allow flexibility in the choice of TouchControl panel materials, switch layout, and switch size, AMI Touch Control inputs have been designed to detect a differential change rather than an absolute change in level. To obtain a reference level, two resistors are connected to input REF, one to V_{SS} and the other to V_{DD}.

O OUTPUTS

Each output pin labeled "O" corresponds to an input pin labeled "1." Whenever an input is selected, the output becomes active and will drive an external load toward supply voltage V_{BB}. When outputs are not active, they are high impedance open drain.

V_{BB} SUPPLY

The sources of all output devices are common and connected to pin V_{BB}. This allows TTL compatibility as shown in Figure 1, as well as the ability to drive higher level signals. For instance, if V_{SS} = 0 volts, V_{DD} = - 16 volts, and V_{BB} = V_{SS}, then active outputs would drive a load connected to V_{DD} towards V_{SS}. The V_{BB} pin can be used also to switch analog signals; in this configuration the analog signals are applied to the "O" pins and V_{BB} is the output pin.

M/T INPUT

The M/T input pin selects the mode of switch operation, either momentary or toggle. With no connection to the M/T pin momentary operation is selected, and appropriate outputs are active only for the duration of touching a switch. In this mode, no output is active when no switch is touched. A V_{DD} level applied to M/T causes the circuit to operate in the toggle mode. In this condition, the brief touch of any switch will turn on the appropriate output, which will remain latched on until the switch is touched again. Subsequent activations of the switch will toggle the corresponding output on and off alternately. To reset all outputs when the toggle mode is selected, a pulse of V_{SS} level may be applied to the M/T input.

SCI OUTPUT

The SC1 output provides the clock signal for the Touch-Control panel. Its frequency is determined by the RC time constant, and it is connected in common with one of each of the two common conductive surfaces on the reverse side of the touch panel.

MOMENTARY AND TOGGLE COMBINATION

The S9261, S9264, and S9265 contain several outputs that are permanently in the momentary mode of operation. With the M/T input at V_{SS} these parts function identically to the S9260 and S9263. With M/T at a logic 1 level, however, the S9261 has four momentary and three toggle inputs. Table 1 shows the combinations available on all three parts.

TABLE 1. COMPARISON OF FEATURES

Part Number	Pin Count	Touch Switch Capacity			Number of Outputs
		Total Touch Switch Interface Capability	Touch Inputs Selectable For Either Momentary Or Toggle Operation Through Use of M/T Input	Touch Switch Inputs Fixed In Momentary Operation (Not affected by state of M/T input)	
S9260	22	7	7	0	7
S9261	22	7	3 (I4 thru I6)	4 (I0 thru I3)	7
S9263	40	16	16	0	16
S9264	40	16	8 (I8 thru I15)	8 (I0 thru I7)	16
S9265	40	16	12 (I4 thru I15)	4 (I0 thru I3)	16

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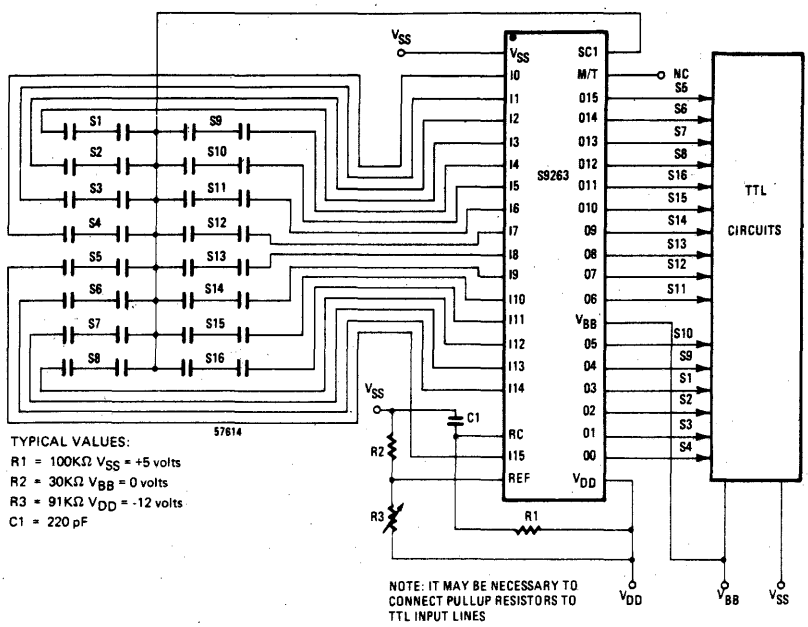


FIGURE 1. 16 SWITCH APPLICATION USING S9263

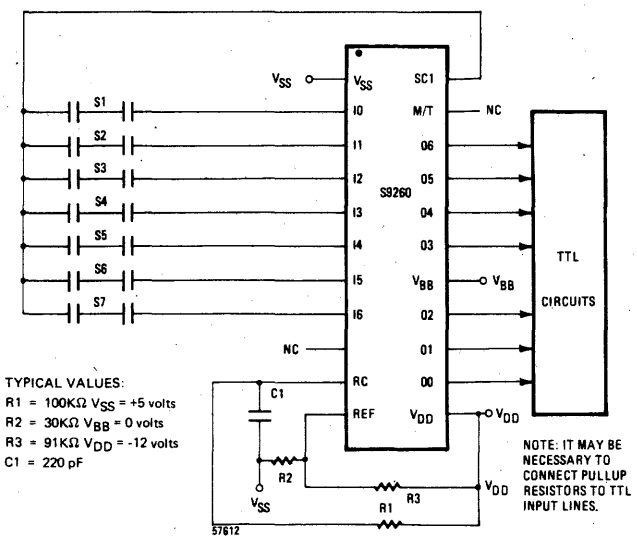
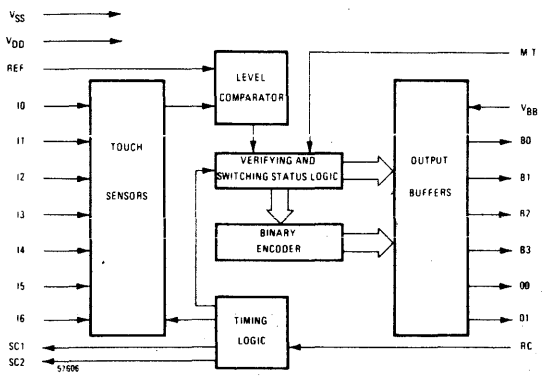


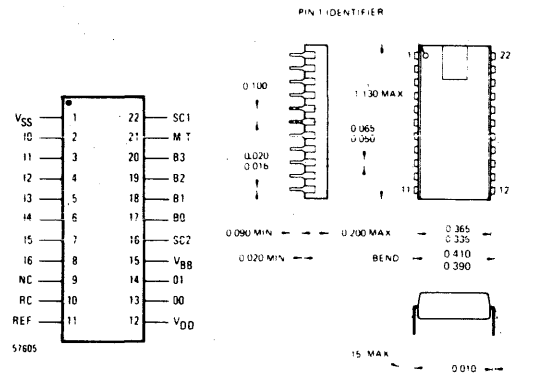
FIGURE 2. 7 SWITCH APPLICATION USING S9260

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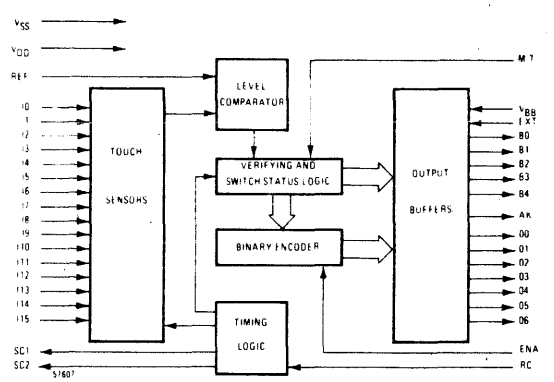
MULTIPLEXED
TOUCHCONTROL INTERFACE
SEPTEMBER 1976



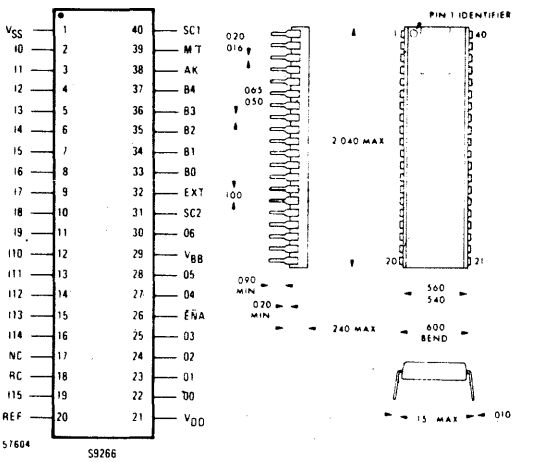
BLOCK DIAGRAM – S9262 (14 SWITCHES)



PIN/PACKAGE CONFIGURATION – S9262



BLOCK DIAGRAM – S9266 (32 SWITCHES)



PIN/PACKAGE CONFIGURATION – S9266

FEATURES

- Simplifies design of Touch-sensitive switches
- Interfaces with up to 32 touch switches
- Eliminates contact noise
- Comparator sensing permits use with wide variety of touch switch configurations
- Binary outputs provided
- Outputs are TTL compatible
- Permits design of totally isolated touch surfaces, facilitating UL approval

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S9262/S9266
MULTIPLEXED TOUCHCONTROL INTERFACE

GENERAL DESCRIPTION

The S9262 and S9266 TouchControl interface circuits permit almost any control panel containing mechanical switches to be easily replaced by a flat-surface capacitive control panel providing superior styling, reliability, ease of cleaning, and safety. Connecting directly to a screened or etched pattern on the panel's reverse side, these MOS circuits provide outputs to drive a variety of logic systems from household appliances to industrial controls. All system functions are then selected by merely touching the flat conductive TouchControl "switch" areas that have been deposited on the panel's front surface in practically any configuration desired.

These circuits can operate up to 32 TouchControl switches, and their outputs are encoded for easy interfacing with microprocessors. For applications requiring an individual output for each TouchControl switch, refer to AMI's S9260, S9261, S9263, S9264 and S9265.

FUNCTIONAL DESCRIPTION

Fabricated with P-channel ion implanted MOS/LSI technology, AMI TouchControl integrated circuits* are designed to interface with a variety of touch panel switches and provide a high degree of flexibility in the selection of touch panel materials, layout of touch pad configurations, and design of switching functions. These parts are designed to address an array of TouchControl switches in either a 2 x 7 matrix (S9262) or a 2 x 16 matrix (S9266) to interface with a total of either 14 or 32 switches. The outputs are binary encoded for easy interfacing with microprocessors or TTL, CMOS or MOS logic.

Both momentary and "push on - push off" (toggle) switching operations are available on AMI TouchControl circuits and are electrically selected by the logic level of the M/T input pin. To ensure reliable switch action, a built in delay is incorporated in all circuits requiring a minimum touch time for switch response.

TYPICAL APPLICATIONS

- Appliance Control Panels
- Home Entertainment Systems
- Power Tool Controls
- Televisions
- Automotive Controls
- Telephones
- Games
- Fast Food Waterproof Keyboards
- Moisture Proofing
- Industrial Controllers
- Computer Terminals
- Keyboards
- Instrumentation
- 16 to 1 Multiplexers
- Microprocessor Interface
- Vending Machines
- Cash Registers

ABSOLUTE MAXIMUM RATINGS

Voltage on any pin except EXT relative to V_{SS}:	+ 0.3V to - 20V	Operating temperature range:	0°C to + 70°C
Voltage on EXT pin relative to V_{SS}:	+ 0.3V to - 27V	Storage temperature (Ambient)	- 65°C to + 150°C

**For non-multiplexed TouchControl circuits see AMI S9260, S9261, S9263, S9264, S9265*

S9262/S9266
MULTIPLEXED TOUCHCONTROL INTERFACE

ELECTRICAL CHARACTERISTICS

($0°C \leq T_A \leq 70°C$; $V_{SS} = 0V$; $V_{DD} = -13.5V$ to $-18.0V$ unless otherwise specified.)

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITIONS
V_{IL}	Input logic 0 level – all except "I" inputs.	+ 0.3	0	- 1.5	Volts	Note: M/T and $\overline{ENA}$ inputs are internally pulled up to V_{SS}.
V_{IH}	Input logic 1 level – all except "I" inputs.	- 10.0	- 12.0	- 18.0	Volts	
f_{RC}	Internal oscillator frequency measured at RC input.	50		100	kHz	
T_S	Switch delay time	65		135	msec	Frequency measured at
T_{RST}	Time to reset all latches using M/T input.		100	135	msec	RC Input = 50 kHz.
V_{OL}	Output low voltage.	V_{SS}		- 1.0	Volts	$V_{BB} = V_{SS}$; 10K resistive load to V_{DD}.
V_{OH}	Output high voltage			V_{DD}		
V_{OL}	Output low voltage.	V_{SS}		V_{SS} - 0.5	Volts	$V_{SS} = +5V$; $V_{BB} = 0V$
V_{OH}	Output high voltage	V_{BB} + 0.4		V_{BB}		$V_{DD} = -12V$; 2800Ω resistive load to V_{SS}.
SC1, SC2	Scan clock output.					Max. capacitive loading ≤ 150 pF.
	Output low voltage	V_{SS}		- 1.5		
	Output high voltage.			V_{DD}		
I_{DD}	Supply Current		7.0	15.0	ma	Outputs unconnected

OPERATION

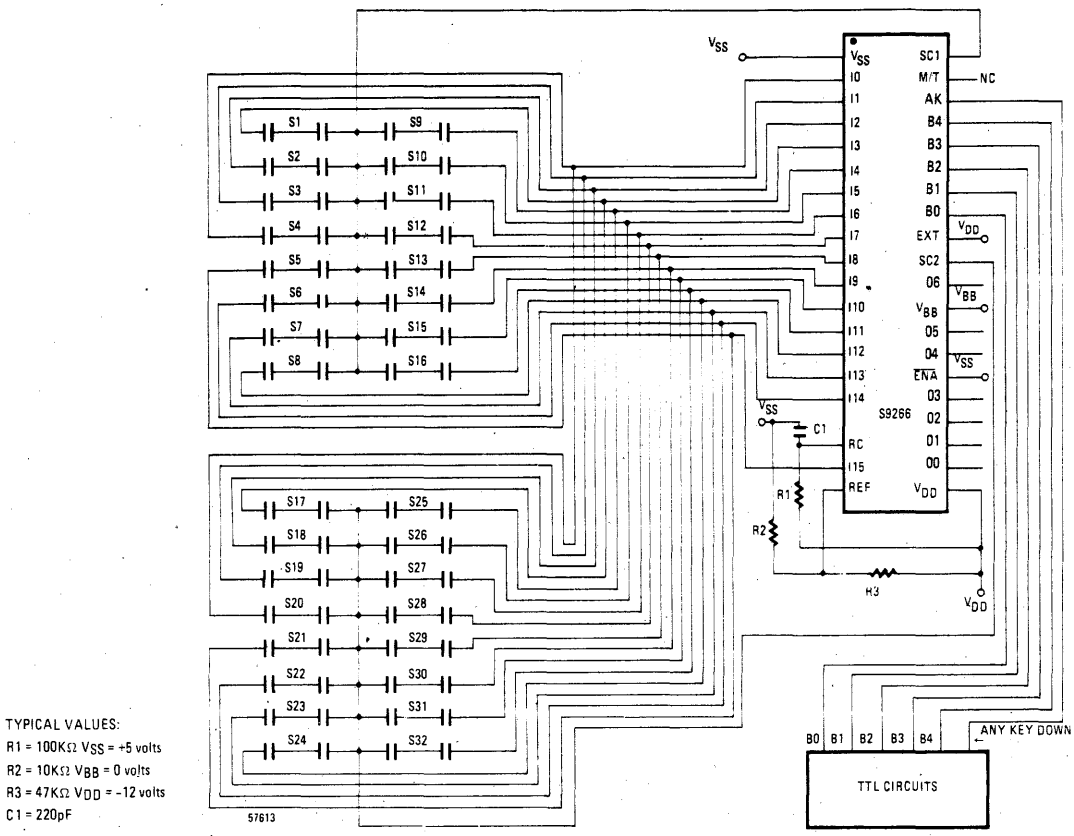
Device operation can be understood by referring to Figure 1, depicting a typical application of the S9266. Each of the 32 pairs of series capacitors labeled S1 – S32 is one touch switch located on a TouchControl panel constructed of glass, printed circuit board, epoxy, or other dielectric material. (For details on touch panel configuration and operation, see the TouchControl application note included in this APD.) In each capacitor pair, the two common plates represent the conductive area on the control panel surface that is to be touched. The other two plates are formed by two conductive surfaces parallel to the touched surface and located directly under it on the reverse side of the panel. Referring again to Figure 1, the S9266 generates a clock signal on output SC1 and a similar signal on output SC2. The SC1 clock output is connected to the common conductors of 16 of the 32 touch switches; the SC2 clock connects to the remaining 16 switches. For each touch switch the clock signal passes through the two series capacitors and is detected in the MOS circuit. When a panel switch surface is touched, the signal level into the chip diminishes, and the on-chip differential amplifier senses the change and performs the appropriate switching function.

I INPUTS

Inputs from the touch switch pads to the TouchControl circuit are labeled I0 through I15 (S9266), or I0 through I6 (S9262). The I inputs in conjunction with SC1 and SC2 outputs form a touch switch matrix of 2 x 16 or 2 x 7, respectively. In both these parts the outputs are binary coded and will be described later.

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S9262/S9266
MULTIPLEXED TOUCHCONTROL INTERFACE



TYPICAL VALUES:
R1 = 100KΩ V_{SS} = +5 volts
R2 = 10KΩ V_{BB} = 0 volts
R3 = 47KΩ V_{DD} = -12 volts
C1 = 220pF

FIGURE 1. 32 SWITCH APPLICATION USING S9266

RC INPUT

A resistor connected to V_{DD} and a capacitor connected to V_{SS} are connected to the RC input pin to establish the on-chip clock frequency that controls the rate of multiplexing and the touch switch delay time. Nominal values for these components are suggested in Figure 1, but they may be varied to change clock frequency over a range of 50kHz to 100 kHz.

REF INPUT

In order to allow flexibility in the choice of TouchControl panel materials, switch layout, and switch size, AMI TouchControl inputs have been designed to detect a differential change rather than an absolute change in level. To obtain a reference level, two resistors are connected to input REF, one connected to input REF, one connected to V_{SS} and the other to V_{DD}.

V_{BB} SUPPLY

The sources of all output devices (both "O" and "B" outputs) are common and connected to pin V_{BB}. This allows TTL compatibility as shown in Figure 1, as well as the ability to drive higher level signals. For instance, if V_{SS} = 0 volts, V_{DD} = - 16 volts, and V_{BB} = V_{SS}, then active outputs would drive a load connected to V_{DD} towards V_{SS}.

M/T INPUT

The M/T input pin selects the mode of switch operation, either momentary or toggle. Applying V_{SS} to the M/T pin selects momentary operation in which appropriate outputs are active only for the duration of touching a switch. In this mode, no output is active when no switch is touched. A V_{DD} level applied to M/T causes the circuit to operate in the toggle mode

S9262/S9266
MULTIPLEXED TOUCHCONTROL INTERFACE

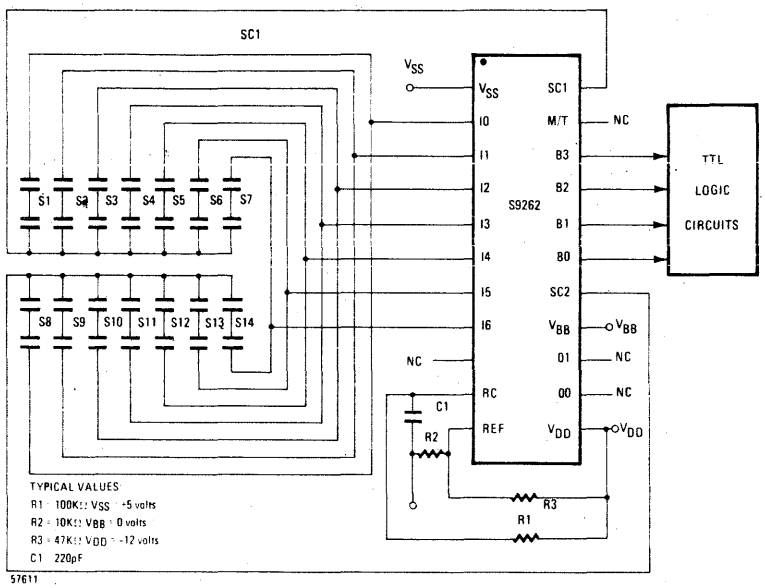


FIGURE 2. 14 SWITCH APPLICATION USING S9262

for "push-on, push-off" operation. Subsequent activation of the switch will toggle the corresponding output on and off alternately. It should be noted that each input should be cleared to the off state before selecting a new input to obtain meaningful data from the binary outputs. To reset all outputs when the toggle mode is selected, a pulse of V_{SS} level may be applied to the M/T input.

SC1 and SC2 OUTPUTS

The S9262 and S9266 have multiplexed inputs, using 2 x 7 and 2 x 16 matrices, respectively, to provide 14 and 32 input states. Clock signals SC1 and SC2 are used along with the "I" inputs to form these matrices as connected in the schematic of Figure 1.

O OUTPUTS

Each output pin labeled "O" corresponds to an input pin labeled "I". Whenever an input is selected, the output becomes active and will drive an external load toward supply voltage V_{BB}. This is true for momentary operation only; toggle operation is described in the section labeled "MT input." When "O" outputs are not active, they are high impedance open drain.

B AND AK OUTPUTS

The S9262 has four and the S9266 has five outputs labeled "B." These supply a binary code relating to the state of the inputs. Fourteen unique states are available on S9262 and thirty-two on S9266. The output configuration is identical to the "O" outputs. An extra output labeled AK is available on the S9266 and is active whenever any key is selected.

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S9262/S9266
MULTIPLEXED TOUCHCONTROL INTERFACE

ENA INPUT

Available on the S9266, the ENA input allows the outputs to be bussed and may be gated off by application of a logic 1 level. V_{SS} applied to the input enables all five outputs and AK.

EXT

The EXT pin is used in the output circuitry and should be connected to V_{DD}.

SCAN OUTPUT	TOUCHED INPUT	"B" OUTPUTS B0	B1	B2	B3	"O" OUTPUTS O0	O1
SC1	I0	0	0	0	0	1	0
SC1	I1	1	0	0	0	0	1
SC1	I2	0	1	0	0	0	0
SC1	I3	1	1	0	0	0	0
SC1	I4	0	0	1	0	0	0
SC1	I5	1	0	1	0	0	0
SC1	I6	0	1	1	0	0	0
SC2	I0	1	1	1	0	0	0
SC2	I1	0	0	0	1	0	0
SC2	I2	1	0	0	1	0	0
SC2	I3	0	1	0	1	0	0
SC2	I4	1	1	0	1	0	0
SC2	I5	0	0	1	1	0	0
SC2	I6	1	0	1	1	0	0
–	None	1	1	1	1	0	0

TABLE 1. OUTPUT ENCODING (V_{BB} = 0 VOLTS)

SCAN OUTPUT	TOUCHED INPUT	"B" OUTPUTS B0	B1	B2	B3	B4	"O" OUTPUTS O0	O1	O2	O3	O4	O5	O6	AK OUTPUT
SC1	I0	0	0	0	0	0	1	0	0	0	0	0	0	1
SC1	I1	1	0	0	0	0	0	1	0	0	0	0	0	1
SC1	I2	0	1	0	0	0	0	0	1	0	0	0	0	1
SC1	I3	1	1	0	0	0	0	0	0	1	0	0	0	1
SC1	I4	0	0	1	0	0	0	0	0	0	1	0	0	1
SC1	I5	1	0	1	0	0	0	0	0	0	0	1	0	1
SC1	I6	0	1	1	0	0	0	0	0	0	0	0	1	1
SC1	I7	1	1	1	0	0	0	0	0	0	0	0	0	1
SC1	I8	0	0	0	1	0	0	0	0	0	0	0	0	1
SC1	I9	1	0	0	1	0	0	0	0	0	0	0	0	1
SC1	I10	0	1	0	1	0	0	0	0	0	0	0	0	1
SC1	I11	1	1	0	1	0	0	0	0	0	0	0	0	1
SC1	I12	0	0	1	1	0	0	0	0	0	0	0	0	1
SC1	I13	1	0	1	1	0	0	0	0	0	0	0	0	1
SC1	I14	0	1	1	1	0	0	0	0	0	0	0	0	1
SC1	I15	1	1	1	1	0	0	0	0	0	0	0	0	1
SC2	I0	0	0	0	0	1	0	0	0	0	0	0	0	1
SC2	I1	1	0	0	0	1	0	0	0	0	0	0	0	1
SC2	I2	0	1	0	0	1	0	0	0	0	0	0	0	1
SC2	I3	1	1	0	0	1	0	0	0	0	0	0	0	1
SC2	I4	0	0	1	0	1	0	0	0	0	0	0	0	1
SC2	I5	1	0	1	0	1	0	0	0	0	0	0	0	1
SC2	I6	0	1	1	0	1	0	0	0	0	0	0	0	1
SC2	I7	1	1	1	0	1	0	0	0	0	0	0	0	1
SC2	I8	0	0	0	1	1	0	0	0	0	0	0	0	1
SC2	I9	1	0	0	1	1	0	0	0	0	0	0	0	1
SC2	I10	0	1	0	1	1	0	0	0	0	0	0	0	1
SC2	I11	1	1	0	1	1	0	0	0	0	0	0	0	1
SC2	I12	0	0	1	1	1	0	0	0	0	0	0	0	1
SC2	I13	1	0	1	1	1	0	0	0	0	0	0	0	1
SC2	I14	0	1	1	1	1	0	0	0	0	0	0	0	1
SC2	I15	1	1	1	1	1	0	0	0	0	0	0	0	1
	None	1	1	1	1	1	0	0	0	0	0	0	0	0

TOUCHCONTROL APPLICATION NOTES

PANEL CONSTRUCTION

A TouchControl switch panel consists of a single sheet of a rigid material with conductive surfaces applied on both sides as shown in Figure 3.

A number of materials may be used for touch panels, the selection of the material most suited for a particular application being dependent on such things as durability, appearance, ease of assembly, cost, and dielectric constant of the material.

Regardless of the selected panel material, a touch switch is formed by applying a single conductive surface to its front surface with two other conductive surfaces applied directly in line on the reverse side of the panel. Figure 3 shows three views of a typical touch panel containing two TouchControl switches. On switch one, conductive surface A is applied to the front of the panel and is the surface to be touched to effect a switch closure. Surfaces B and C are applied directly in line with A on the opposite side of the panel. A should cover completely and may overlap surfaces B and C.

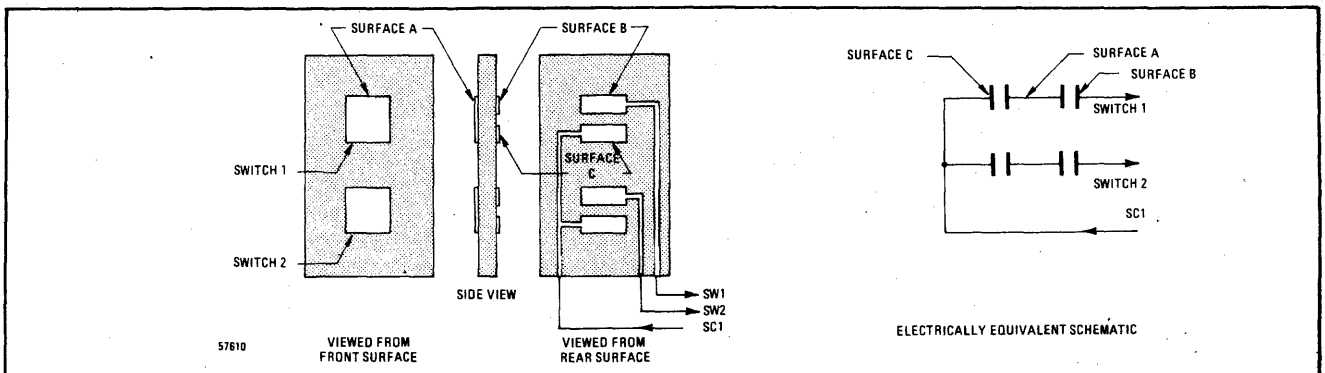
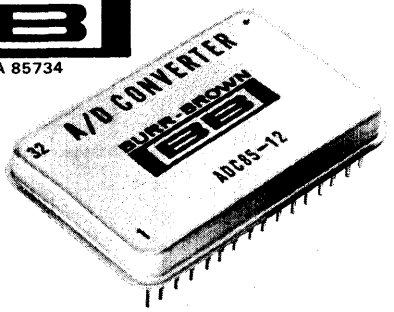
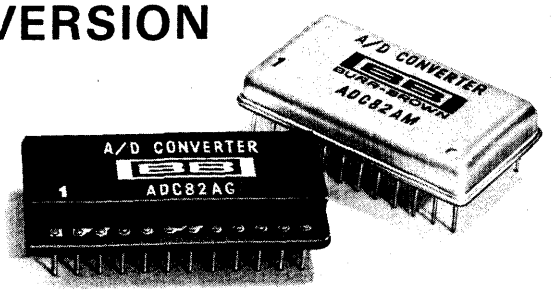


FIGURE 3. CONSTRUCTION OF A TWO SWITCH TOUCHCONTROL PANEL WITH EQUIVALENT ELECTRICAL CIRCUIT.

BURR-BROWN DATA CONVERSION

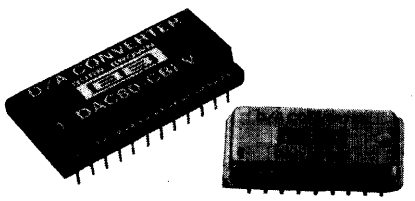
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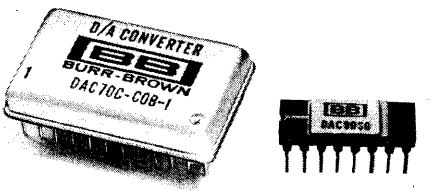




A/D CONVERTERS

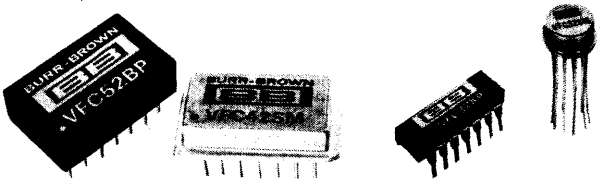
	Model	Resolution (Bits)	RANGE OF SPECIFICATIONS Linearity Error (% of FSR) max	Conversion Time (μsec)	Tempco Bipolar (ppm of FSR °C)max	Input Range (V)	Package
High Speed	ADC60	8 - 12	±0.0244 to ±0.195	.88 - 3.5	±15	±25 to +20	Module
Low Cost	ADC80	10 - 12	±0.012 to 0.048	21 - 25	±23	±2.5 to ±10	DIP
High Speed, Low Cost	ADC82	8	±0.2	2.8	±75	±2.5 to +20	DIP
	ADC84	10 - 12	±0.012 to ±0.048	6 - 10	±33	±2.5 to ±10	DIP
High Speed, Low Drift	ADC85	10 - 12	±0.012 to ±0.048	6 - 10	±18	±19 to ±53	DIP





D/A CONVERTERS

	Model	Resolution	Linearity Error Over Temp (% of FSR) max	Tempco (ppm of FSR °C) max	Output Range	Settling Time (FSR, ±1/2 LSB)	Package
Very High Speed	DAC60	10 - 12 Bits	±0.012 to ±0.048	±15	-5 to ±2.5mA	40 - 150nsec	Module
High Resolution	DAC70	16 Bits, 4 Digits	±0.003 to ±0.005	±9 to ±21	-2 to ±1mA	50μsec	DIP
Low Cost	DAC80	12 Bits, 3 Digits	±0.012	±25	±2.5 to ±10V, -2 to ±1mA	300nsec - 5μsec	DIP
Voltage Output	DAC82	8 Bits	±0.016	±50	±2.5 to ±10V, -1.6 to ±0.8mA	2.5μsec	DIP
Low Drift	DAC85	12 Bits, 3 Digits	±0.012	±5 to ±20	±2.5 to ±10V, -2 to ±1mA	300nsec to 5μsec	DIP
Monolithic	DAC90	8 Bits	±0.2	±75	-2, ±1mA	200nsec	DIP

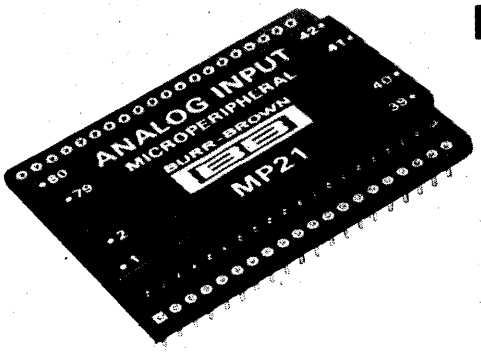


V/F CONVERTERS

	Model	V_{IN} Range (V)	F_{OUT} Range (kHz)	Linearity (% of FSR) max	Tempco (ppm of FSR/°C) max	Package
Low Cost, Monolithic	VFC32	User-selected	User-selected (500kHz, max)	±0.01, 10kHz ±0.05, 100kHz	±100 to ±150	DIP TO-100
Low Cost, Complete Hybrid	VFC42	0 to +10	0 to 10	±0.01	±100	DIP
	VFC52	0 to +10	0 to 100	±0.05	±100	DIP
Low Drift, Complete	VFC12	0 to +10	0 to 10	±0.01	50	Module
	VFC15	0 to +20	0 to 20	±0.01	50	Module
Very Low Drift, Complete	VFC12LD	0 to +10	0 to 10	±0.005	10	Module
	VFC15LD	0 to +20	0 to 20	±0.005	10	Module

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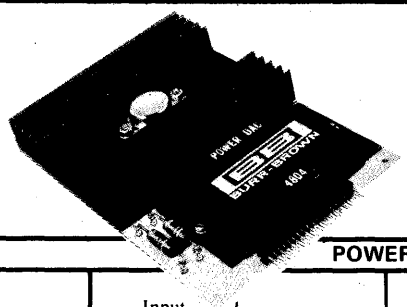


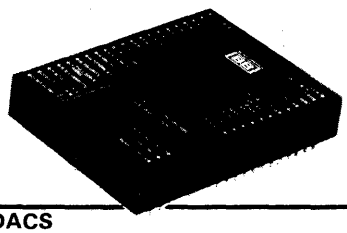
MICROPROCESSOR INTERFACED ANALOG INPUT SYSTEMS

	Model	RANGE OF SPECIFICATIONS Channels	Resolution (Bits)	Accuracy (% of FSR) max	Accuracy Drift (ppm/°C) max	Package
8080, SC/MP, Z-80, 8084, 8085	MP20	8 Differential	8	±0.4	±40	Module
	MP22	16 Single-ended	12	±0.1	±25	Module
6800, 650X, F8	MP21	8 Differential 16 Single-ended	8	±0.4 ±0.4, Low	±40	Module

MICROPROCESSOR INTERFACED ANALOG OUTPUT SYSTEMS

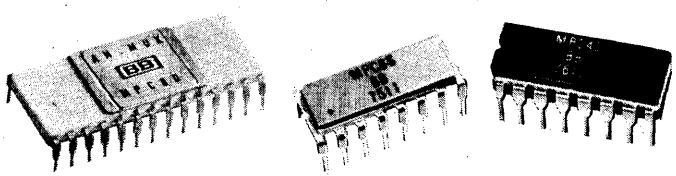
8080, SC/MP, Z-80, 8084, 8085	MP10	2	8	±0.4	±80	DIP
6800, 650X, F8	MP11	2	8	±0.4	±80	DIP





POWER DACS

	Model	Input Coding	Accuracy	Tempco (ppm of FSR/°C)	Output Voltage Range (V)	Output Current Range (mA)	Package
Digitally Controlled, Voltage and Current Limit	4800	12 Bit Binary Plus Sign	±0.012% of FSR	22	±10, ±60	±200	Module
	4801	3 Digit BCD Plus Sign	±0.012% of FSR	22	±10, ±60	±200	Module
Low Cost, High Current	4804	12 Bit Binary	±0.05% of Reading	50, max	User-selected to ±30	±1000	PC Card



SAMPLE/HOLD CIRCUITS

	Model	Gain/Offset Error (%), (mV)	Charge Offset (mV)	Droop Rate (mV/msec)	Tempco (ppm of 20V/°C)	Acquisition Time (μsec)	Package
Low Cost, Complete	SHC80	±0.01, ±2 max	±2 max	0.5 max	±2	10 max	DIP
High Speed, Complete	SHC85	±0.01, ±2 max	±2 max	0.5 max	±2	4.5 max	DIP
Low Cost, Monolithic	SHC298AM	±0.01max,±7max	±25 max	10 max	±4	10 max	TO-99
Very High Speed	SHM60	±0.01 max, ±1.5	±1.5	5	±2	1 max	Module

MULTIPLEXERS

	Model	Channels	Input Range (V)	On Resistance (kΩ) max	Crosstalk (% of Off Channel Signal	Settling Time (to 0.01%) (μsec)	Package
CMOS	MPC8S	8 Single-ended	±10	1.8	0.005	5	DIP
CMOS	MPC4D	4 Differential	±10	1.8	0.005	5	DIP
CMOS	MPC16S	16 Single-ended	±10	1.8	0.005	7	DIP
CMOS	MPC8D	8 Differential	±10	1.8	0.005	7	DIP

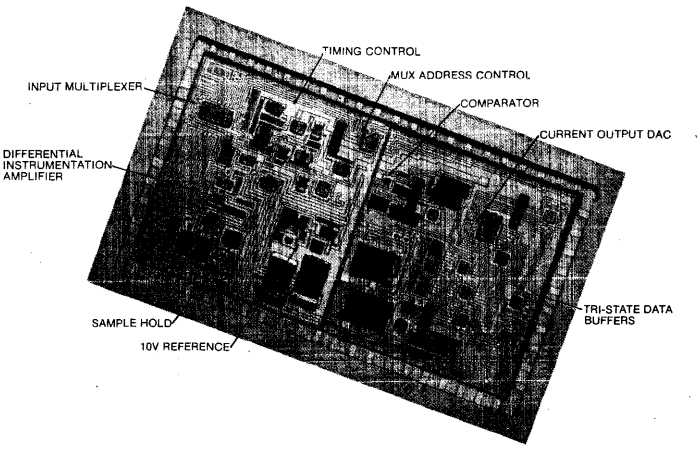
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HDAS-8, HDAS-16

12 BIT HYBRID DATA ACQUISITION SYSTEMS

DATEL SYSTEMS, INC.





FEATURES

- **12 Bit Resolution**
- **8 or 16 Channels**
- **Internal Instrumentation Amp**
- **50 kHz Throughput Rate**
- **Three State Outputs**

The HDAS-8, with 8 differential input channels, and the HDAS-16, with 16 single ended input channels, are industry's first complete 12 bit data acquisition systems in a single hybrid package. Acquisition and conversion times combined are 20μsec. maximum, giving a 50 kHz throughput rate. The 12 bit output data can be transferred out in three 4 bit bytes by means of three state data bus drivers. Output coding is straight binary for unipolar operation and offset binary for bipolar operation.

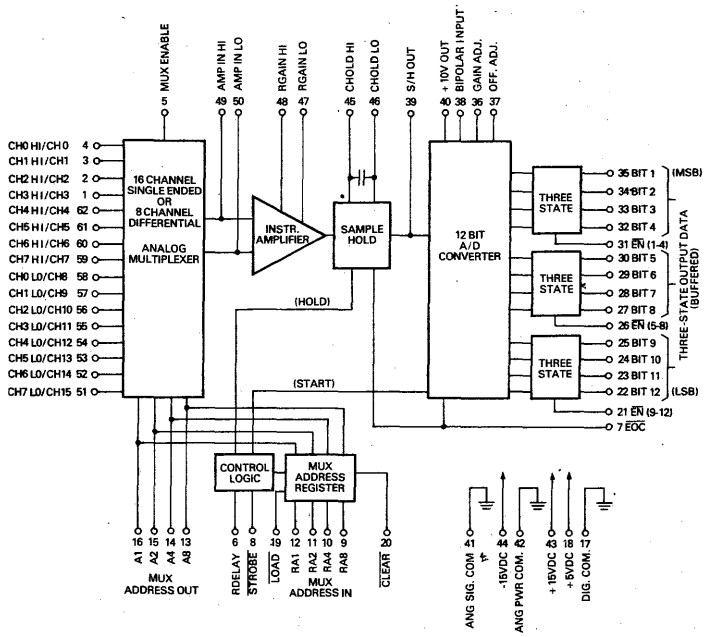
The HDAS circuitry includes an analog multiplexer, programmable gain instrumentation amplifier, sample-hold circuit with MOS hold capacitor, 10 volt buffered reference, 12 bit A/D converter, three state bus driver and digital control circuitry. The instrumentation amplifier can be programmed by a single external resistor for gains from 1 to 1000. This is an important feature for processing signals in the range of 10mV to 10 V full scale.

SPECIFICATIONS, Typical at 25°C

	HDAS-8	HDAS-16
No. Channels	8	16
Input Type	Differential	Single Ended
Input Range, unipolar FS	+10mV to +10 V	+10mV to +10 V
Input Range, bipolar FS	±10mV to ±10 V	±10mV to ±10 V
Common Mode Range	±11 V	—
Input Resistance	100 Meg.	100 Meg.
Input Bias Current, max.	200 pA	200 pA
Input Off. Voltage Drift	20μV/°C+(10μV/°C)G	
Input Gain Equation	G = 1+20K/R_G	
Channel Addressing	3-Bit Code	4-Bit Code
Address Input Logic	DTL, TTL	DTL, TTL
Resolution	12 Bits	12 Bits
Linearity Error, max.	½ LSB	½ LSB
Differential Nonlinearity, max.	½ LSB	½ LSB
Total Error, max.*	0.025%	0.025%
Gain Tempco, typ.	10 ppm/°C	10 ppm/°C
Gain Tempco, max.	30 ppm/°C	30 ppm/°C
No Missing Codes	Over Oper. Temp. Range	
Power Supply Sensitivity	0.01%/%	0.01%/%
Throughput Rate, max.	50 kHz	50 kHz
Acquisition Time	9 μsec.	9 μsec.
Conversion Time	9 μsec.	9 μsec.
Aperture Delay Time	100 nsec.	100 nsec.
Sample-Hold Droop	1 μV/μsec.	1 μV/μsec.
Feedthrough at 1 kHz, max.	0.01%	0.01%
Output Coding, unipolar	Straight Bin	Straight Bin
Output Coding, bipolar	Offset Bin.	Offset Bin.
Power Requirement	+15VDC at 67 mA max. −15 VDC at 71 mA max. +5VDC at 155 mA max.	
Package	Miniature 62 Pin	

*at maximum throughput rate

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The internal sample-hold device has excellent characteristics and has its own self contained MOS hold capacitor. Aperture delay time is 100nsec. and hold mode droop is 1μV/μsec. Nonlinearity error is less than ½ LSB and total error is 1 LSB maximum at 50 kHz throughput rate.

The HDAS units are especially useful for microcomputer based measurement and control systems. The package is a miniature 2.3 × 1.4 × 0.24 inches (58 × 36 × 6 mm) with 62 pins.

OUTPUT CODING

UNIPOLAR

Scale	0 to +5V	0 to +10 V	Straight Binary
+FS-1 LSB	+4.9988	+9.9976	1111 1111 1111
+¾FS	+3.7500	+7.5000	1100 0000 0000
+½FS	+2.5000	+5.0000	1000 0000 0000
+¼FS	+1.2500	+2.5000	0100 0000 0000
+1 LSB	+0.0012	+0.0024	0000 0000 0001
ZERO	0.0000	0.0000	0000 0000 0000

BIPOLAR

Scale	±5V	±10 V	Offset Binary
+FS-1 LSB	+4.9976	+9.9951	1111 1111 1111
+½FS	+2.5000	+5.0000	1100 0000 0000
ZERO	0.0000	0.0000	1000 0000 0000
−½FS	−2.5000	−5.0000	0100 0000 0000
−FS+1 LSB	−4.9976	−9.9951	0000 0000 0001
−FS	−5.0000	−10.000	0000 0000 0000

ORDERING INFORMATION

Model	Oper. Temp. Range	Seal	Price (1-9)
HDAS-8MC	0 to 70C	Hermetic	$325.00
HDAS-8MR	−25 to +85C	Hermetic	445.00
HDAS-8MM	−55 to +125C	Hermetic	750.00
HDAS-16MC	0 to 70C	Hermetic	325.00
HDAS-16MR	−25 to +85C	Hermetic	445.00
HDAS-16MM	−55 to +125C	Hermetic	750.00

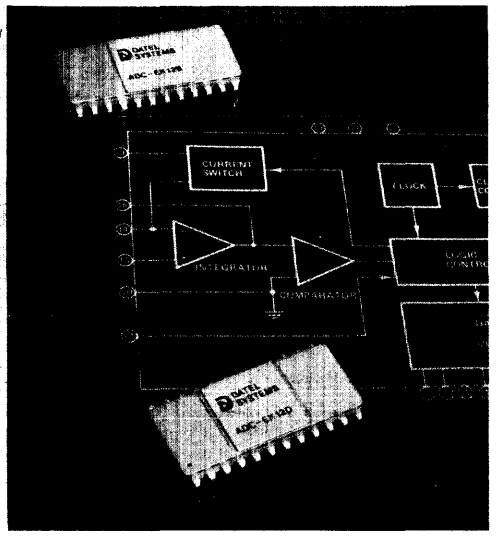
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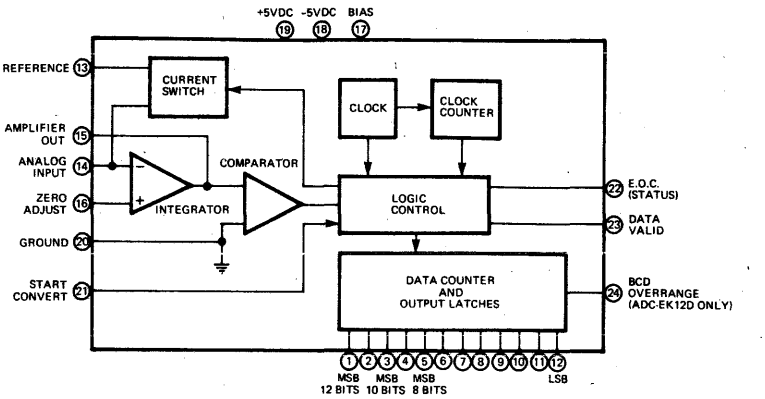
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ADC-EK SERIES

MONOLITHIC INTEGRATING A/D CONVERTERS

DATEL SYSTEMS, INC.





FEATURES

- **Charge Balancing Type**
- **Binary or BCD Models**
- **20 mW Power Consumption**
- **No Missing codes**
- **8, 10, 12 Bit Resolution**

The ADC-EK series are low power, integrating A/D converters fabricated on a single monolithic chip using CMOS technology. The circuit employs a charge balancing integrator, current switch, comparator, clock counter, data counter, and control logic circuitry to implement conversion. The charge balancing integration technique gives high linearity and noise immunity along with inherent monotonicity resulting in no missing codes. Output data appears in parallel form on latched outputs which are CMOS, low power TTL, or low power Schottky TTL compatible. The ADC-EK series consists of 5 different models with 8, 10, and 12 bit binary coding and 3½ digit BCD coding.

Conversion time is 1.8 to 24 milliseconds maximum depending on model. Nonlinearity is ±½ LSB max. while differential nonlinearity is ±¼ LSB typical.

SPECIFICATIONS, Typical at 25°C

	ADC-EK8B, 10B, 12B	ADC-EK12DC, DR
Resolution	8, 10, 12 Bits	3½ Digits
Conversion Time, 8 Bits	1.8 msec.	—
Conversion Time, 10 Bits	6.0 msec.	—
Conversion Time, 12 Bits	24 msec.	12 msec.
Gain Tempco, max.	40 ppm/°C	40 ppm/°C
Linearity Error, max.	½ LSB	¼ LSB
Differential Nonlinearity	¼ LSB	¼ LSB
Diff. Nonlinearity Tempco	1.7 ppm/°C	2.5 ppm/°C
No Missing Codes	Over Operating Temp. Range	
Power Supply Sensitivity	0.05%/%	0.05%/%
Analog Input Range	0 to +10μA	0 to +10 μA
Reference Input	−20 μA	−20 μA
Unipolar Coding	Straight Binary	BCD
Bipolar Coding	Offset Binary	—
Power Requirement	±5 VDC at 2 mA	±5 VDC at 2 mA
Package	24 Pin	24 Pin

ORDERING INFORMATION

Model	Oper. Temp. Range	Package	Price (1-24)
ADC-EK8B	0 to 70C	Plastic	$11.95
ADC-EK10B	0 to 70C	Ceramic	27.50
ADC-EK12B	0 to 70C	Ceramic	36.00
ADC-EK12DC	0 to 70C	Plastic	14.00
ADC-EK12DR	−25 to +85C	Ceramic	22.00

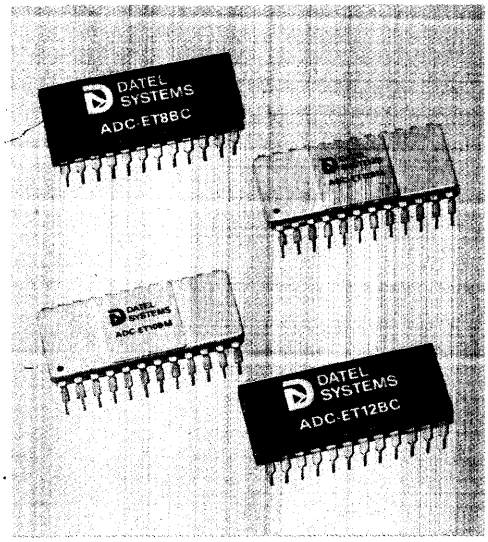
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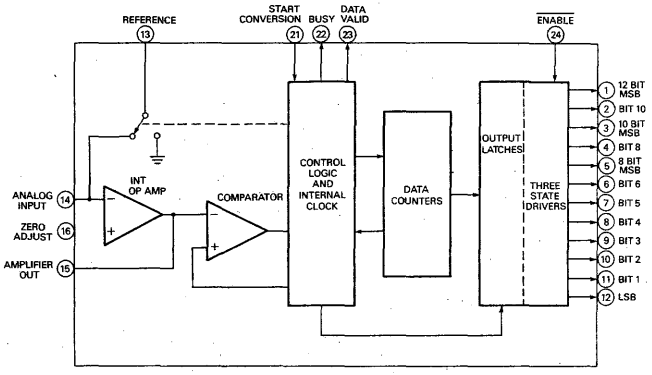
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ADC-ET SERIES

CMOS A/D'S WITH 3-STATE OUTPUTS

DATEL SYSTEMS, INC.





FEATURES

- **Monolithic CMOS**
- **3-State Outputs**
- **8, 10, 12 Bit Resolution**
- **¼ LSB Typical Linearity**
- **Integrating Type**

The ADC-ET series devices are low cost 8, 10, and 12 bit integrating A/D converters optimized for high accuracy, linearity and noise immunity. They operate at low power consumption, with sufficient speed to handle most industrial and instrumentation requirements. Discretely controllable three state outputs allow bus organized output connections making these units ideal for microprocessor interfacing.

Fabricated with monlithic CMOS techniques, each device is housed in a 24-pin dual in-line package. The converter consists of an integrating operational amplifier, comparator, current switch, internal clock, two counters, latching output buffers and control logic circuitry. Operation of the circuit requires only a few external passive components and connection to external reference and power supplies.

SPECIFICATIONS, Typical at 25°C

	ADC-ET8B	ADC-ET10B	ADC-ET12B
Resolution	8 Bits	10 Bits	12 Bits
Conversion Time, max.	1.8 msec.	6.0 msec.	24 msec.
Gain Tempco, typ.	25 ppm/°C	25 ppm/°C	25 ppm/°C
Gain Tempco, max.	75 ppm/°C	75 ppm/°C	75 ppm/°C
Nonlinearity, max.	½ LSB	½ LSB	±½ LSB*
Differential Nonlinearity	¼ LSB	¼ LSB	±¼ LSB
Diff. Nonlinearity Tempco	2.5 ppm/°C	2.5 ppm/°C	2.5 ppm/°C
No Missing Codes		Over Operating Temp. Range	
Power Supply Sensitivity, max.	0.05%/%	0.05%/%	0.05%/%
Analog Input Range	0 to +10 μA	0 to +10 μA	0 to +10 μA
Reference Input	−20 μA	−20 μA	−20 μA
Output Logic	LP TTL, CMOS	LP TTL, CMOS	LP TTL, CMOS
Unipolar Coding	Straight Bin.	Straight Bin.	Straight Bin.
Bipolar Coding	Offset Bin.	Offset Bin.	Offset Bin.
Power Requirement	±5V at 5 mA	±5V at 5 mA	±5V at 5 mA
Package	24 Pin	24 Pin	24 Pin

*±1½ LSB max. for ADC-ET12BC

ORDERING INFORMATION

Model	Oper. Temp. Range	Package	Price (1-24)
ADC-ET8BC	0 to 70C	Plastic	$13.50
ADC-ET8BM	−55 to +125C	Ceramic	40.00
ADC-ET10BC	0 to 70C	Plastic	17.50
ADC-ET10BM	−55 to +125C	Ceramic	50.00
ADC-ET12BC	0 to 70C	Plastic	18.50
ADC-ET12BR	−25 to +85C	Ceramic	39.50
ADC-ET12BM	−55 to +125C	Ceramic	68.00

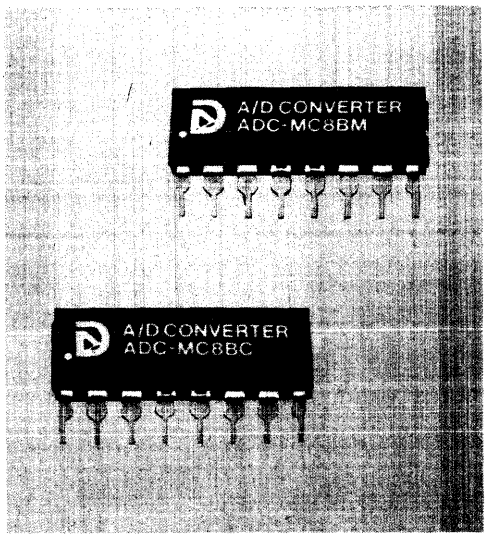
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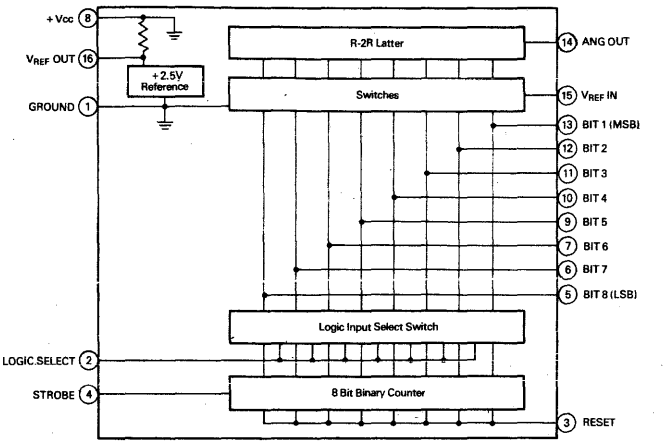
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ADC-MC8B

LOW COST, 8 BIT MONOLITHIC A/D CONVERTER

DATEL SYSTEMS, INC.





FEATURES

- **8 Bit Resolution**
- **Internal 2.5 V Reference**
- **+5 V Supply Operation**
- **Operates as A/D or D/A**
- **Low Cost**

The ADC-MC8B is an 8 bit monolithic, multifunction converter which operates from a single +5 V supply. This device can be operated as either an A/D or D/A converter by means of external pin connections. As a D/A converter it is complete, including an internal 2.5 V reference; the output voltage is 0 to +2.55 V when using the internal reference. When operating as an A/D converter, two external IC's are required: a 311 type comparator, and a 74132 type quad NAND gate. An internal counter develops the output code word with 500 μsec. required for a full scale conversion.

The ADC-MC8B design consists of eight current switches, a diffused resistor R-2R ladder network, a 2.5 V band gap reference, an 8 bit binary counter, and eight logic select switches. The logic select switches have a control input which determines whether the switches provide TTL outputs or accept TTL inputs. This converter can also be used with an external reference.

SPECIFICATIONS, Typical at 25°C

	ADC-MC8B
Resolution	8 Bits
Conversion Time	500 μsec.
Gain Tempco	40 ppm/°C
Nonlinearity Error, max.	½ LSB
Differential Nonlinearity, max.	½ LSB
No Missing Codes	Over Op. Temp. Range
Analog Input Ranges*	0 to +2.5 V 0 to +5 V 0 to +10 V
Input Impedance	Set by resistor used
Reference Output	+2.55 V
Output Logic	DTL/TTL
Output Logic	DTL/TTL
Unipolar Coding	Straight Binary
Bipolar Coding	Offset Binary
Power Requirement	+5 VDC at 30 mA
Package	16 Pin DIP

*determined by external resistors

ORDERING INFORMATION

Model	Oper. Temp. Range	Package	Price (1-24)
ADC-MC8BC	0 to 70C	Plastic	$ 9.50

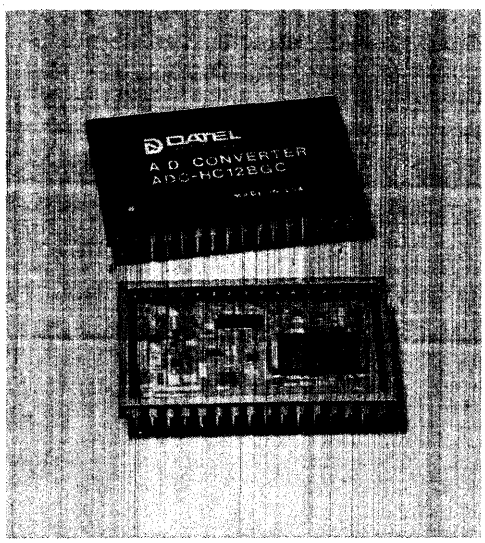
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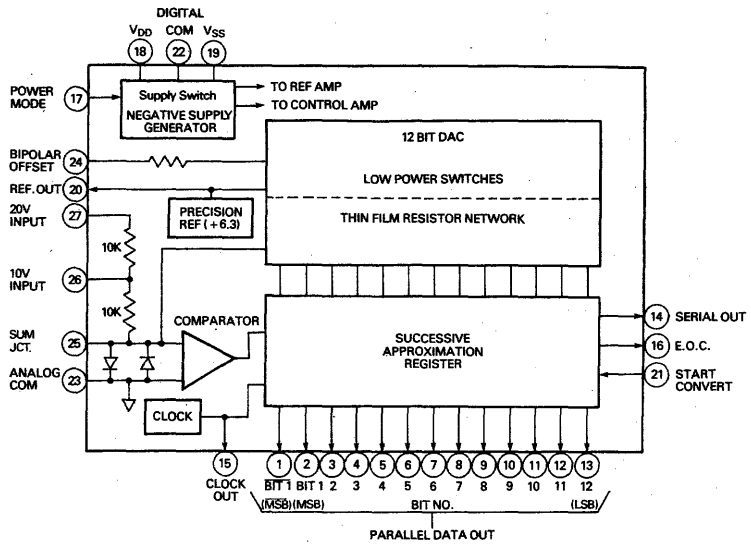
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ADC-HC12B

12 BIT, LOW POWER A/D CONVERTER

DATEL SYSTEMS, INC.





INTERFACE

Datel

FEATURES

- **Single Supply Operation**
- **CMOS Circuitry**
- **12 Bit Resolution**
- **6 Input Voltage Ranges**
- **26 mW Consumption at 1000 Conversions/Sec.**

The ADC-HC12B is a complete, low power 12 bit A/D converter utilizing CMOS circuitry. It is specifically designed for portable and remote instrumentation applications where low power consumption is essential; this unit operates from either a single +9 VDC to +15 VDC power source (interrupt mode) or from a dual ±9 VDC to ±15 VDC source (continuous mode). In the interrupt mode of operation the converter is initially in standby mode, drawing only 10 μA of current from the supply until a start convert pulse is applied to it. With the pulse applied the converter turns on, stabilizes, and then performs a 12 bit conversion and returns to the standby mode while the 12 bit data word is held at the output.

Power consumption is 112 milliwatts in the continuous mode and 26 milliwatts in the interrupt mode at 1,000 conversions per second. There are six different analog input voltage ranges.

SPECIFICATIONS, Typical at 25°C

	ADC-HC12B
Resolution	12 Bits
Conversion Time, continuous mode	305 μsec. max.
Conversion Time, interrupt mode	350 μsec. max.
Gain Tempco, max.	30 ppm/°C
Nonlinearity Error, max.	½ LSB
Differential Nonlinearity, max.	½ LSB
Differential Nonlinearity Tempco	2 ppm/°C of FSR
No Missing Codes	Over Op. Temp. Range
Power Supply Sensitivity	0.003%/%
Analog Input Ranges	0 to +5 V, +10 V, +20 V ±2.5 V, ±5 V, ±10 V
Input Impedance	5K, 10K, or 20K
Output Logic	CMOS
Unipolar Coding	Straight Binary
Bipolar Coding	Offset Binary Two's Complement
Power Requirement, continuous	±9 V to ±15 V
Power Requirement, interrupt	+9 V to +15 V
Package	32 Pin

ORDERING INFORMATION

Model	Oper. Temp. Range	Seal	Price (1-24)
ADC-HC12BGC	0 to 70C	Epoxy	$149.00
ADC-HC12BMC	0 to 70C	Hermetic	159.00
ADC-HC12BMR	−25 to +85C	Hermetic	199.00
ADC-HC12BMM	−55 to +125C	Hermetic	249.00

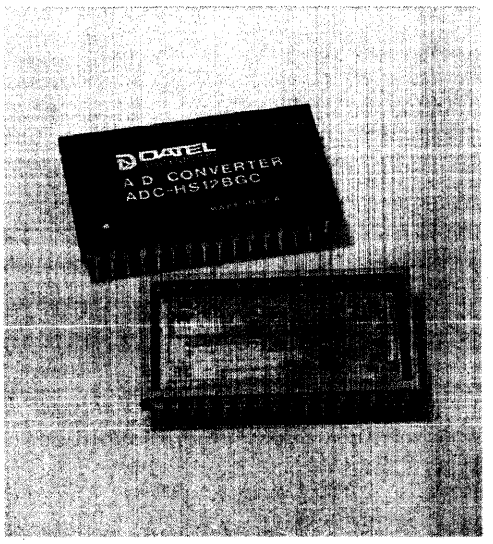
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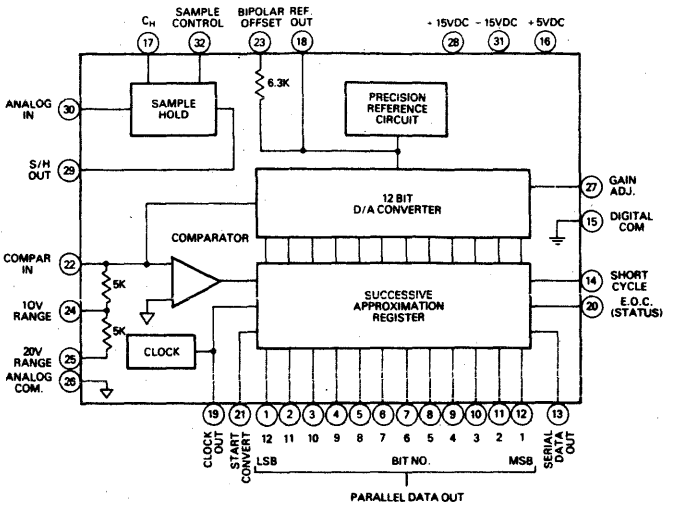
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ADC-HS12B

12 BIT A/D CONVERTER WITH SAMPLE HOLD

DATEL SYSTEMS, INC.





FEATURES

- **Internal Sample-Hold**
- **6 μsec. Acquisition Time**
- **8 μsec. Conversion Time**
- **12-Bit Resolution**
- **Programmable Input Ranges**

The ADC-HS12B is a high performance 12 bit A/D converter combined with a sample-hold in a miniature 32 pin package. It is specifically designed for systems applications where the sample-hold is an integral part of the conversion process. The sample hold has a 6 μsec. acquisition time and the A/D converter has an 8 μsec. conversion time. Five input voltage ranges are programmable by external pin connection. The input impedance to the sample-hold is 100 megohms, permitting direct connection to an analog multiplexer.

This converter incorporates proven thin film hybrid technology used in high volume production. The thin film resistor network is fabricated of nichrome on glass and then actively laser trimmed for best linearity. Other features include 20 ppm/°C gain tempco, 2 ppm/°C differential nonlinearity tempco and no missing codes over the operating temperature range.

SPECIFICATIONS, Typical at 25°C

	ADC-HS12B
Resolution	12 Bits
Acquisition Time	6 μsec.
Conversion Time, max.	8 μsec.
Gain Tempco, max.	20 ppm/°C
Nonlinearity Error, max.	½ LSB
Differential Nonlinearity, max.	½ LSB
No Missing Codes	Over Op. Temp. Range
Power Supply Sensitivity	0.002%/% max.
Analog Output Ranges	0 to +5 V, 0 to +10 V ±2.5 V, ±5 V, ±10 V
Input Impedance	100 Megohms
Input Bias Current	50 nA
Aperture Delay Time	50 nsec.
Aperture Uncertainty Time	5 nsec.
Hold Mode Droop	50 nV/μsec. max.
Hold Mode Feedthrough	0.01% max.
Output Logic	TTL
Unipolar Coding	Comp. Binary
Bipolar Coding	Comp. Offset Binary
Power Requirement	+15 VDC at 60 mA −15 VDC at 50 mA +5 VDC at 100 mA
Package	32 Pin

ORDERING INFORMATION

Model	Oper. Temp. Range	Seal	Price (1-24)
ADC-HS12BGC	0 to 70C	Epoxy	$155.00
ADC-HS12BMC	0 to 70C	Hermetic	169.00
ADC-HS12BMR	−25 to +85C	Hermetic	219.00
ADC-HS12BMM	−55 to +100C	Hermetic	259.00

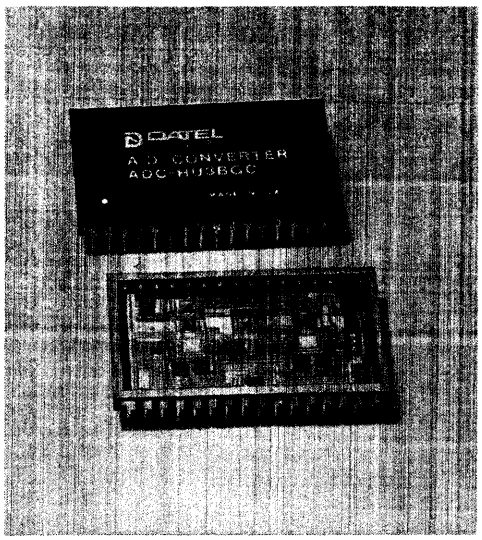
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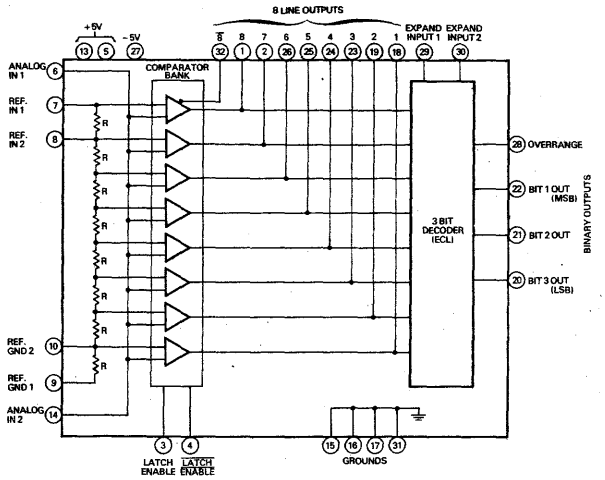
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ADC-HU3B

3 BIT EXPANDABLE FLASH A/D CONVERTER

DATEL SYSTEMS, INC.





NOTE: R = 23.5 ohms

FEATURES

- **3 Bits Plus Overrange**
- **50 MHz Conversion Rate**
- **0.1% Linearity**
- **Expandable Building Block**
- **Parallel (Flash) Technique**

The ADC-HU3B is an ultra-fast, 3 bit A/D converter using the flash (or parallel) conversion technique. Using thin-film hybrid construction this device performs a conversion every 20 nanoseconds maximum, giving a 50 MHz conversion rate. It is a miniature building block circuit which can be used alone as a 3 bit A/D, with two units corrected together for a 4 bit A/D, or with four units connected together for a 5 bit A/D. There are two sets of digital outputs: one directly from the comparator outputs gives a "thermometer scale" output; the other is a 3 bit decoded binary output with an overrange bit.

The ADC-HU3B is fabricated using a bank of 8 ultra-fast monolithic analog comparators. A 160 ohm tapped thin-film resistor network biases the comparators and is connected to an external voltage reference: the network is actively laser trimmed to give 0.1% linearity.

SPECIFICATIONS, Typical at 25°C

	ADC-HU3B
Resolution	3 Bits
Conversion Time, 8 line output	16 nsec. max.
Conversion Time, binary output	20 nsec. max.
Conversion Rate, binary output	50 MHz min.
Gain Tempco, max.	±25 ppm/°C
Nonlinearity, max.	±0.1%
Analog Input Ranges	0 to +2.1 V 0 to −2.1 V ±2.1 V
Input Bias Current	50 μA
Reference Input	±2 V
Reference Input Impedance	141 to 188 Ohms
Output Logic	ECL
Unipolar Coding	8 line (thermometer scale) Straight Binary
Bipolar Coding	8 line (thermometer scale) Offset Binary
Power Requirement	+5 VDC at 160 mA −5 VDC at 330 mA
Package	32 Pin

ORDERING INFORMATION

Model	Oper. Temp. Range	Seal	Price (1-24)
ADC-HU3BGC	0 to 70C	Epoxy	$189.00
ADC-HU3BMC	0 to 70C	Hermetic	199.00
ADC-HU3BMR	−25 to +85C	Hermetic	251.00
ADC-HU3BMM	−55 to +100C	Hermetic	304.00

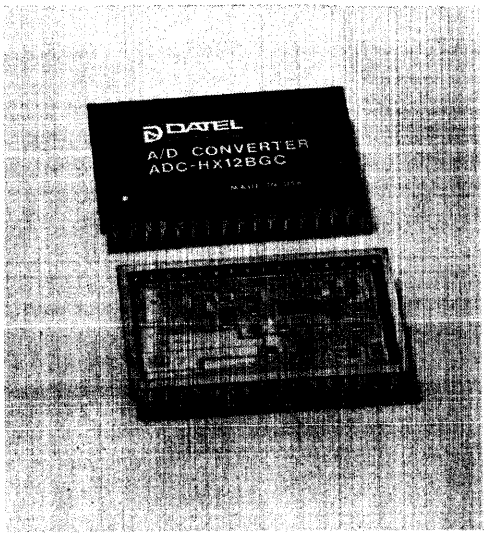
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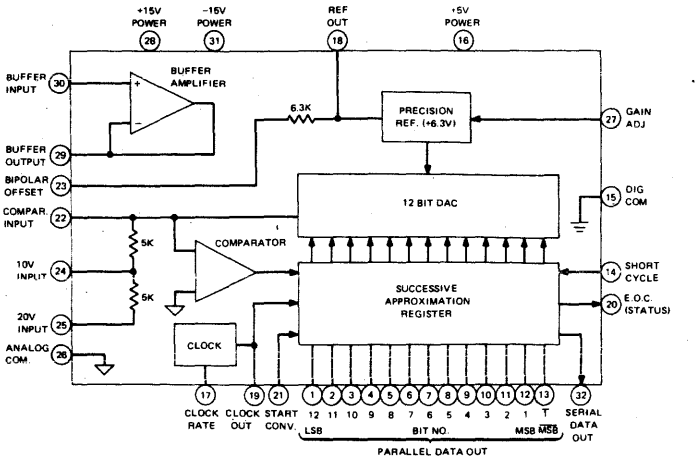
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ADC-HX12B

12 BIT, LOW COST A/D CONVERTER

DATEL SYSTEMS, INC.





FEATURES

- **12 Bit Resolution**
- **20 μsec. Conversion Time**
- **5 Programmable Ranges**
- **100 Megohm Buffer**
- **Lowest Cost**

The ADC-HX12B is a very low cost, 12 bit A/D converter which is functionally complete. It is fabricated with thin film hybrid technology to perform a conversion in 20 μsec. By means of external pin connections it can be programmed for 5 different input voltage ranges. An internal 100 megohm buffer is provided for high input impedance applications.

The circuit consists of a 12 bit DAC which employs quad current switches, a precision zener reference, a fast comparator, clock, successive approximation register, and buffer amplifier. A nichrome thin film resistor network is actively laser trimmed to achieve optimum linearity.

Output data is available in both parallel and serial forms. This converter can also be short cycled to achieve faster conversions at lower resolutions.

SPECIFICATIONS, Typical at 25°C

	ADC-HX12B
Resolution	12 Bits
Conversion Time, max.	20 μsec.
Gain Tempco, max.	20 ppm/°C
Nonlinearity Error, max.	½ LSB
Differential Nonlinearity, max.	½ LSB
Diff. Nonlinearity Tempco	2 ppm/°C of FSR
No Missing Codes	Over Op. Temp. Range
Power Supply Rejection, max.	0.002%/%
Analog Input Ranges	0 to +5 V, 0 to +10V ±2.5 V, ±5 V, ±10 V
Input Impedance	2.5 K, 5 K or 10 K
Buffer Input Impedance	100 Megohms
Buffer Bias Current	125 nA
Buffer Settling Time	3 μsec.
Unipolar Coding	Complementary Binary
Bipolar Coding	Comp. Offset Binary Comp. 2's Complement
Power Requirement	+15 VDC at 55 mA −15 VDC at 45 mA +5 VDC at 100 mA
Package	32 Pin

ORDERING INFORMATION

Model	Oper. Temp. Range	Seal	Price (1-24)
ADC-HX12BGC	0 to 70C	Epoxy	$ 87.00
ADC-HX12BMC	0 to 70C	Hermetic	105.00
ADC-HX12BMR	−25 to +85C	Hermetic	125.00
ADC-HX12BMM	−55 to +100C	Hermetic	169.00

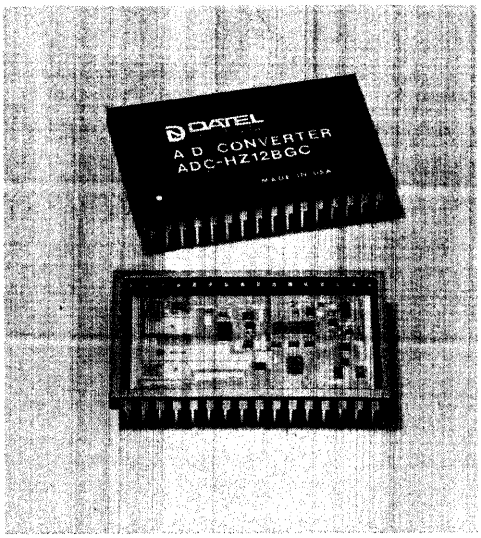
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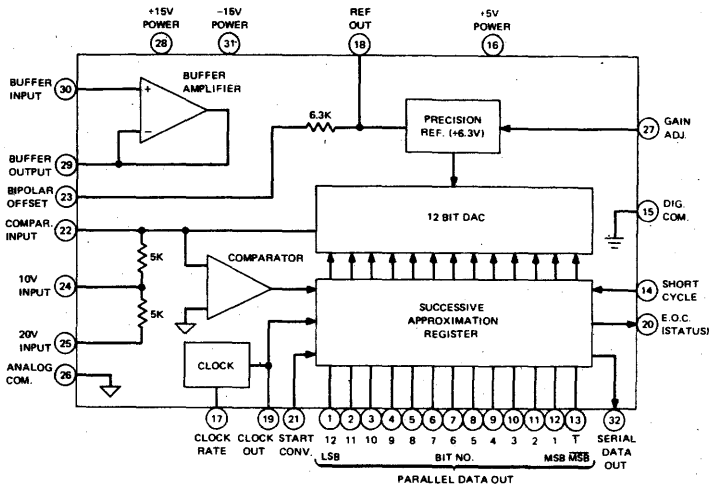
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ADC-HZ12B

12 BIT, HIGH PERFORMANCE A/D CONVERTER

DATEL SYSTEMS, INC.





FEATURES

- **8 μsec. Conversion Time**
- **20 ppm/°C Tempco**
- **5 Programmable Ranges**
- **Short Cycle Capability**
- **100 Megohm Buffer**

The ADC-HZ12B features high conversion speed in a hybrid 12 bit A/D converter. By employing a low capacitance nichrome-on-glass thin film resistor network, a conversion time of only 8 μsec. is achieved. This converter also has 5 different input voltage ranges determined by external pin connection and a 100 megohm buffer which may be connected if desired.

This ADC-HZ12B is functionally complete, incorporating a 12 bit DAC, precision reference, fast comparator, successive approximation register, a clock, and buffer amplifier. The thin film resistor network has excellent tracking characteristics resulting in no missing codes over the operating temperature range. The network is functionally laser trimmed.

Output coding is complementary binary, complementary offset binary, or complementary two's complement. Provision is made for precise, external adjustment of offset and gain.

SPECIFICATIONS, Typical at 25°C

	ADC-HZ12B
Resolution	12 Bits
Conversion Time, max.	8 μsec.
Gain Tempco, max.	20 ppm/°C
Nonlinearity Error, max.	½ LSB
Differential Nonlinearity, max.	½ LSB
Diff. Nonlinearity Tempco	2 ppm/°C of FSR
No Missing Codes	Over Op. Temp. Range
Power Supply Sensitivity, max.	0.002%/%
Analog Input Ranges	0 to +5 V, 0 to +10V ±2.5 V, ±5 V, ±10 V
Input Impedance	2.5K, 5K or 10K
Buffer Input Impedance	100 Megohms
Buffer Bias Current	125 nA
Buffer Settling Time	3 μsec.
Output Logic	TTL
Unipolar Coding	Complementary Binary
Bipolar Coding	Comp. Offset Binary Comp. 2's Complement
Power Requirement	+15 VDC at 55 mA −15 VDC at 45 mA +5 VDC at 100 mA
Package	32 Pin

ORDERING INFORMATION

Model	Oper. Temp. Range	Seal	Price (1-24)
ADC-HZ12BGC	0 to 70C	Epoxy	$125.00
ADC-HZ12BMC	0 to 70C	Hermetic	135.00
ADC-HZ12BMR	−25 to +85C	Hermetic	179.00
ADC-HZ12BMM	−55 to +100C	Hermetic	215.00

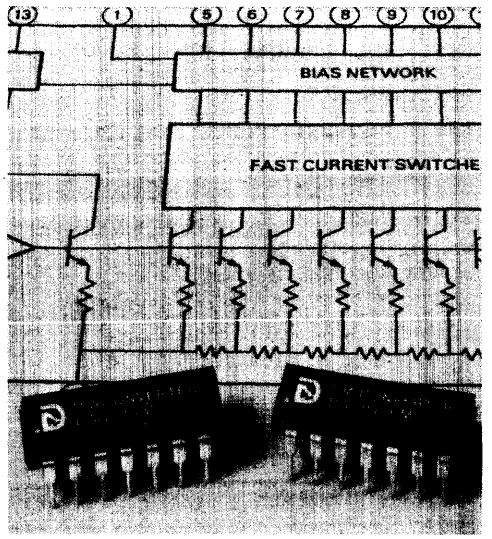
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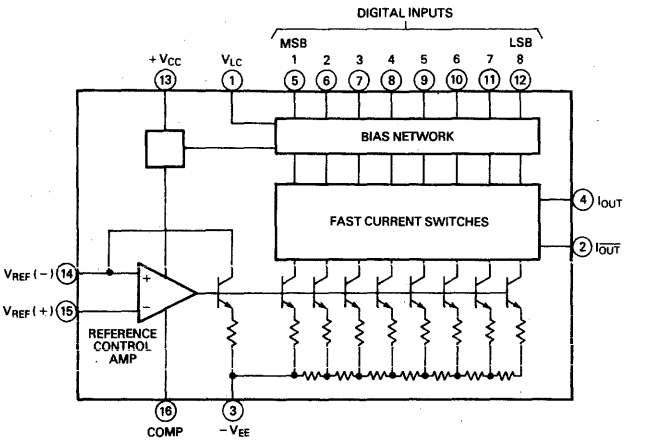
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DAC-08B

HIGH SPEED, MONOLITHIC 8 BIT D/A CONVERTER

DATEL SYSTEMS, INC.





INTERFACE

Datel

FEATURES

- **8 Bit Resolution**
- **85 nsec. Settling Time**
- **High Output Compliance**
- **1 or 2 Quadrant Multiplying**
- **Low Cost**

The DAC-08BC and DAC-08BM provide very high speed performance coupled with low cost and application flexibility. These units have guaranteed full 8-bit monotonicity with non-linearity of 0.19% over the full operating temperature range. High speed current steering switches achieve 85 nanosecond settling time with a very low glitch for full scale changes. A large output voltage compliance range (−10 to +18 Volts) allows direct current to voltage conversion with just an output resistor, omitting the need for an op amp in many cases.

The DAC-08 consists of 8 fast-switching current sources, a diffused R-2R resistor ladder, a bias circuit, and a reference control amplifier. The diffused resistor ladder gives excellent temperature tracking resulting in a gain temperature coefficient of 10 ppm/°C. The monolithic fabrication results in excellent linearity and tempco, fast output settling and low cost.

SPECIFICATIONS, Typical at 25°C

	DAC-08BC/BM
Resolution	8 Bits
Settling Time, to ½ LSB	85 nsec.
Gain Tempco	10 ppm/°C
Nonlinearity, max	½ LSB
Diff. Nonlinearity, max.	½ LSB
Monotonicity	Over Op. Temp. Range
Power Supply Sensitivity	0.002%/%
Analog Output Ranges	0 to 2.1 mA 0 to 4.2 mA
Output Voltage Compliance	−10 V to +18 V
Input Logic	DTL, TTL, HTL CMOS, ECL, HNIL
Coding, unipolar	Straight Binary
Coding, bipolar	Offset Binary
Power Requirement	+4.5 to +18 V at 3.8 mA −4.5 to −18 V at 7.8 mA
Package	16 Pin DIP

ORDERING INFORMATION

Model	Oper. Temp. Range	Package	Price (1-24)
DAC-08BC	0 to 70C	Plastic	$ 5.95
DAC-08BM	−55 to +125C	Ceramic	12.50

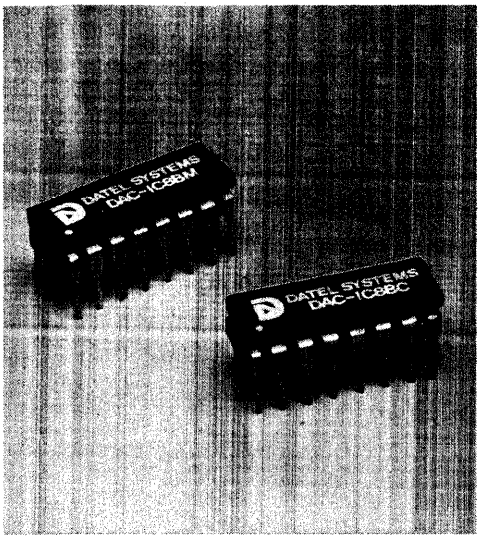
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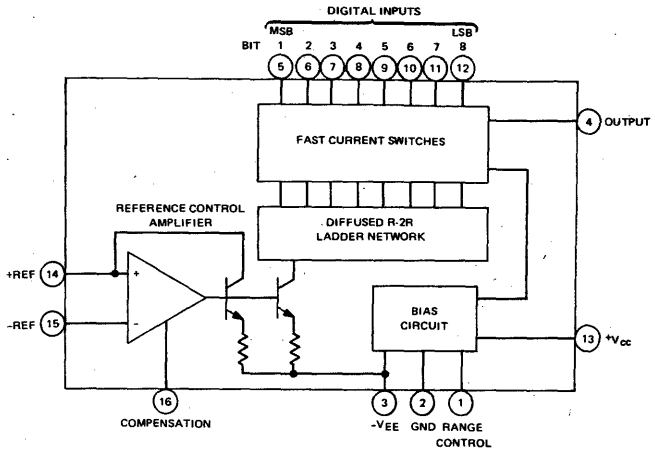
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DAC-IC8B

LOW COST, MONOLITHIC 8 BIT D/A CONVERTER

DATEL SYSTEMS, INC.





FEATURES

- **8 Bit Resolution**
- **300 nsec. Settling Time**
- **½ LSB Linearity**
- **DTL/TTL Inputs**
- **Low Cost**

The DAC- IC8B is an 8 bit monolithic D/A converter designed for low cost and flexible application. It is packaged in a 16 pin DIP and requires only an external output amplifier and reference for operation. A full scale output change settles in 300 nanoseconds for a current output; this can be converted into a fast voltage output with a monolithic operational amplifier such as Datel System's AM-452. Digital input coding is straight binary for unipolar operation and offset binary for bipolar operation and is compatible with standard DTL/TTL logic.

The DAC-IC8B circuit consists of 8 fast switching current sources, a diffused resistor R-2R ladder network, a bias circuit, and a reference control amplifier. The diffused ladder network results in excellent linearity and temperature tracking. An external reference current of 2 mA must be supplied from the reference voltage source and the reference can be varied for one or two quadrant multiplying operations. Two models are available for the commercial and military temperature ranges.

SPECIFICATIONS, Typical at 25°C

	DAC-IC8B
Resolution	8 Bits
Settling Time, to ½ LSB	300 nsec.
Gain Tempco	20 ppm/°C
Nonlinearity, max.	½ LSB
Diff. Nonlinearity	½ LSB
Power Supply Sensitivity	0.01%/%
Analog Output Ranges	0 to 2.1 mA 0 to 4.2 mA
Output Voltage Compliance	−0.6 V to +0.5 V
Input Logic	DTL/TTL
Coding, unipolar	Straight Binary
Coding, bipolar	Offset Binary
Power Requirement	+5 VDC at 22 mA −4.5 to −16.5 V at 13 mA
Package	16 Pin DIP

ORDERING INFORMATION

Model	Oper. Temp. Range	Package	Price (1-24)
DAC-IC8BC	0 to 70C	Ceramic	$ 4.95
DAC-IC8BM	−55 to +125C	Ceramic	13.50

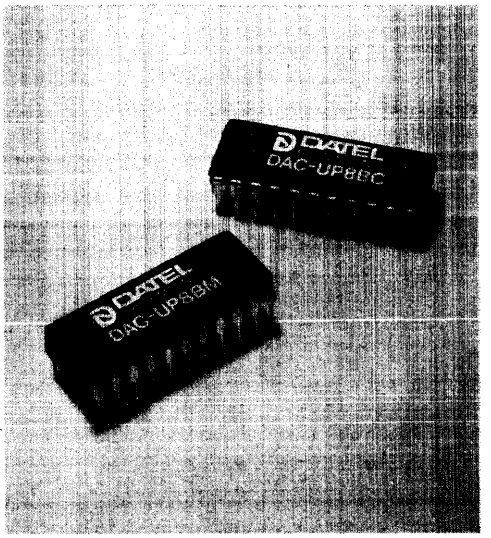
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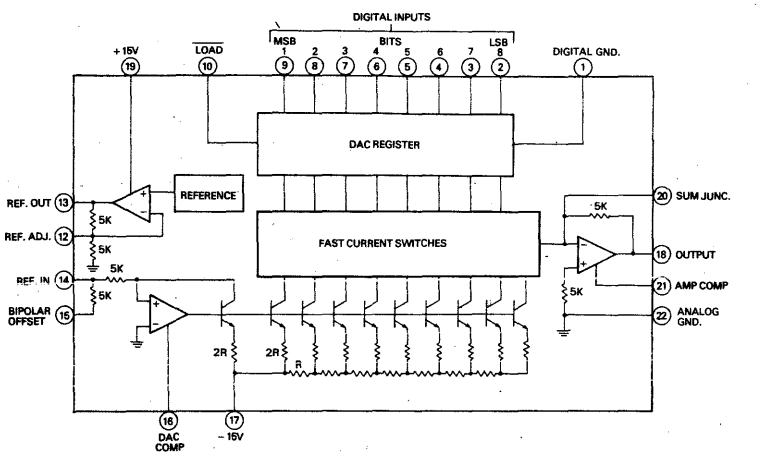
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DAC-UP8B

8 BIT MONOLITHIC DAC WITH INPUT REGISTER

DATEL SYSTEMS, INC.





FEATURES

- **Input Register**
- **Internal Reference**
- **Voltage Output**
- **Low Cost**
- **8 Bit Resolution**

The DAC-UP8BC and DAC-UP8BM are 8 bit monolithic DAC's with internal registers. Contained in the 22 pin DIP is a stable reference, a high-speed output amplifier and an 8 bit input latch. These microprocessor compatible converters are ideal for low cost applications. When the "load" input is low, the register is transparent and any change on the digital input pins will be reflected on the analog output. A low to high transition will latch this digital information and retain it until the "load" goes low. The output voltage range is 0 to +10 V for unipolar and ±5 V for bipolar. Typical settling time is 2 μsec for a full scale change.

The DAC design consists of 8 fast-switching current sources, a diffused R-2R resistor ladder network and a control amplifier. The diffused resistor network gives excellent temperature tracking resulting in a gain temperature coefficient of 20 ppm/°C. This bipolar monolithic device exhibits excellent linearity and temperature coefficients.

SPECIFICATIONS, Typical at 25°C

	DAC-UP8B
Resolution	8 Bits
Settling Time, to ½LSB	2μsec
Gain Tempco, max.	20 ppm/°C
Nonlinearity, max.	½ LSB
Differential Nonlinearity, max.	½ LSB
Monotonicity	Over Oper. Temp. Range
Power Supply Sensitivity	±1 mV/V
Analog Output Voltages	0 to +10V ±5 V
Output Current	±5 mA
Input Logic	DTL/TTL
Coding, unipolar	Straight Bin.
Coding, bipolar	Offset Bin.
Power Requirement	+15 VDC at 7 mA −15 VDC at 10 mA
Package	22 pin DIP

ORDERING INFORMATION

Model	Oper. Temp. Range	Package	Price (1-24)
DAC-UP8BC	0 to 70C	Plastic	$12.50
DAC-UP8BM	−55 to +125C	Ceramic	24.00

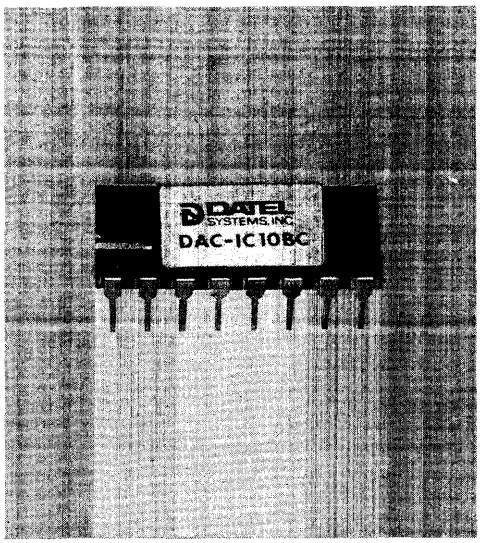
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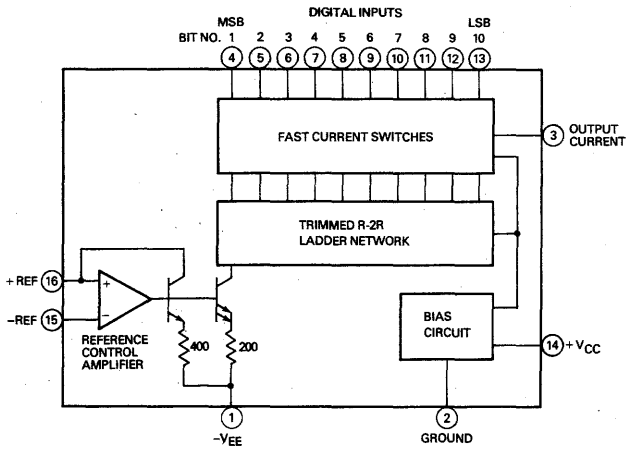
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DAC-IC10BC

LOW COST, MONOLITHIC 10 BIT D/A CONVERTER

DATEL SYSTEMS, INC.





FEATURES

- **10 Bit Resolution**
- **Straight Binary Coding**
- **Current Output**
- **250 nsec. Settling Time**
- **TTL/CMOS Compatible**

The DAC-IC10BC is a low cost, 10 bit monolithic DAC with fast output current settling time. It is packaged in a 16 pin ceramic DIP and requires only an external reference and operational amplifier for voltage output operation. A full scale change in output current settles in 250 nanoseconds, and with a fast I.C. op amp (such as Datel System's AM-452) a 10V output change can settle within 1 microsecond. Digital input coding is straight binary for unipolar operation, and offset binary for bipolar operation; the logic inputs are compatible with TTL or CMOS.

This converter is manufactured with monolithic bipolar technology. The circuit incorporates 10 fast switching current sources which drive a diffused resistor R-2R network. The ladder network is laser trimmed by cutting aluminum links. The circuit also contains a reference control amplifier and a bias circuit. An external reference current of 2 mA is required at the + Reference input terminal.

The DAC-IC10BC has ±1 bit linearity with guaranteed monotonicity at room temperature and has a tempco of 20 ppm/°C.

SPECIFICATIONS, Typical at 25°C

	DAC-IC10BC
Resolution	10 Bits
Settling Time, to ½ LSB	250 nsec.
Gain Tempco	20 ppm/°C
Nonlinearity, max.	1 LSB
Diff. Nonlinearity, max.	1 LSB
Monotonicity	at 25°C
Power Supply Sensitivity	0.02%/%
Analog Output Range	0 to 5 mA
Output Voltage Compliance	−2.5 V to +0.2 V
Input Logic	DTL, TTL, HTL HNIL, CMOS
Coding, unipolar	Straight Binary
Coding, bipolar	Offset Binary
Power Requirement	+5 VDC at 18 mA −15 VDC at 20 mA
Package	16 Pin DIP

ORDERING INFORMATION

Model	Oper. Temp. Range	Package	Price (1-24)
DAC-IC10BC	0 to 70C	Ceramic	$11.50

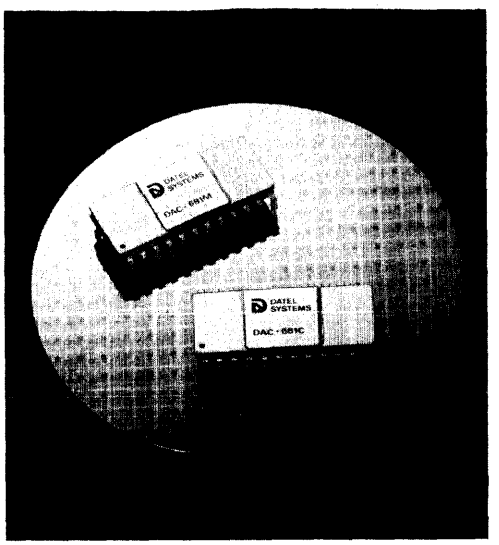
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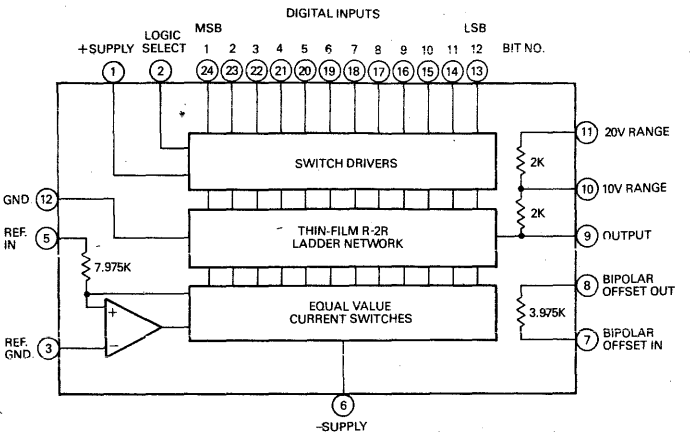
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DAC-681

MONOLITHIC 12 BIT D/A CONVERTER

DATEL SYSTEMS, INC.





FEATURES

- **12 Bit Resolution**
- **200 nsec. Settling Time**
- **5 ppm/°C Max. Gain Tempco**
- **5 Output Ranges**
- **562 Pin Compatible**

The DAC-681 is a new high performance monolithic 12 bit D/A converter fabricated with advanced bipolar technology. The circuit uses a precision, laser-trimmed thin film R-2R ladder network driven by equal-value switched current sources to achieve 1/4 LSB typical linearity, 200 nsec. settling time, and ±5 ppm/°C max. gain tempco.

The DAC-681 operates from TTL or CMOS input logic and provides a 0 to 5 mA or ±2.5 mA output current. The converter contains tracking feedback and bipolar offsetting resistors to provide five output voltage ranges when used with an external operational amplifier: 0 to +5V, 0 to +10V, ±2.5, ±5V, and ±10V. The DAC-681 features pin compatibility with 562 type DAC's while offering superior performance to these earlier devices.

SPECIFICATIONS, Typical at 25°C

	DAC-681
Resolution	12 Bits
Settling Time, to ½LSB	200 nsec.
Gain Tempco, max.	5 ppm/°C
Nonlinearity, max.	½ LSB
Diff. Nonlinearity	¼ LSB
Monotonicity	Over Op. Temp. Range
Power Supply Sensitivity	3.5 ppm/%
Output Current	0 to −5, ±2.5 mA
Output Voltage Ranges	0 to +5V 0 to +10V ±2.5V ±5V ±10V
Input Logic	DTL, TTL, CMOS
Coding, Unipolar	Straight Binary
Coding, Bipolar	Offset Binary
Power Requirement	+5 VDC at 9 mA −15 VDC at 28 mA
Package	24 Pin Ceramic

ORDERING INFORMATION

Model	Oper. Temp. Range	Package	Price (1-24)
DAC-681C	0 to 70C	Ceramic	$ 39.50
DAC-681M	−55 to +125C	Ceramic	145.00

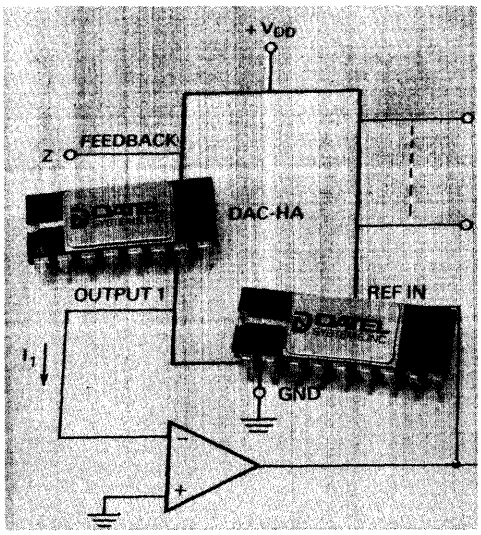
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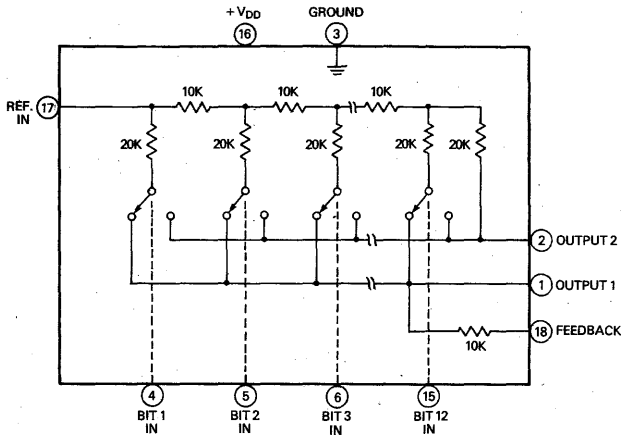
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DAC-HA10B, DAC-HA12B

DATEL SYSTEMS, INC.

LOW POWER CMOS 10 & 12 BIT MULTIPLYING D/A CONVERTERS





DAC-HA12B/D SHOWN

INTERFACE

Datel

FEATURES

- **10 & 12 Bit Resolution**
- **½ LSB Maximum Nonlinearity**
- **2 & 4 Quadrant Multiplying**
- **20 MHz Reference Bandwidth**
- **+5 V or +15 V Power Supply**

The DAC-HA series are high performance, multiplying digital to analog converters. They combine CMOS switches with laser trimmed nichrome thin film resistors to realize low power consumption with excellent linearity and drift characteristics. There are three models in this series: DAC-HA10B for 10 bit binary applications, DAC-HA12B for 12 bit binary applications and DAC-HA12D for 3 digit BCD applications. All units feature ±½ LSB maximum nonlinearity.

The thin film R-2R ladder network consists of 10K and 20K resistors with excellent tracking characteristics. The network provides a 10K input resistance to the required external reference, which can vary over ±12 V. The bandwidth for the reference input is 20 MHz. These devices are ideal for two and four quadrant multiplying applications and have output settling times of 1.3 & 5 μsec. Separate models are available for both +5 V and +15 V supply operation.

SPECIFICATIONS, Typical at 25°C

	DAC-HA10B	DAC-HA12B	DAC-HA12D
Resolution	10 Bits	12 Bits	3 Digits
Settling Time, to ½ LSB	1.3 μsec.	5 μsec.	5 μsec.
Gain Tempco, max.	20 ppm/°C	5 ppm/°C	5 ppm/°C
Nonlinearity, max.	½ LSB	½ LSB	½ LSB
Dif. Nonlinearity, max.	½ LSB	½ LSB	½ LSB
Monotonicity		Over Operating Temp. Range	
Feedthrough	0.01%	0.025%	0.025%
Power Supply Sensitivity	0.01%/%	5ppm/%	5ppm/%
Analog Output Current	±1 mA	±1 mA	±1 mA
Reference Input Range	±12 V	±12 V	±12 V
Reference Input Impedance	10K ±30%	10K ±30%	10K ±30%
Input Logic	TTL, CMOS	TTL, CMOS	TTL, CMOS
Coding, unipolar	Straight Bin.	Straight Bin.	BCD
Coding, bipolar	Offset Bin.	Offset Bin.	—
Power Requirement*	+5 VDC @ 1 μA +15 VDC @ 1.4mA	+5 VDC @ 1μA +15 VDC @ 1.4mA	+5 VDC @ 1μA +15 VDC @ 1.4mA
Package	16 Pin DIP	18 Pin DIP	18 Pin DIP

ORDERING INFORMATION

Model*	Oper. Temp. Range	Supply Voltage*	Price (1-24)
DAC-HA10BC	0 to 70C	+5 V	$ 31.00
DAC-HA10BR	−25 to +85C	+5 V	41.00
DAC-HA10BM	−55 to +125C	+5 V	73.00
DAC-HA12BC	0 to 70C	+5 V	52.00
DAC-HA12BR	−25 to +85C	+5 V	73.00
DAC-HA12BM	−55 to +125C	+5 V	104.00
DAC-HA12DC	0 to 70C	+5 V	52.00
DAC-HA12DR	−25 to +85C	+5 V	73.00
DAC-HA12DM	−55 to +125C	+5 V	104.00

*For +15 V powered version, add suffix −1 to the model numbers shown.

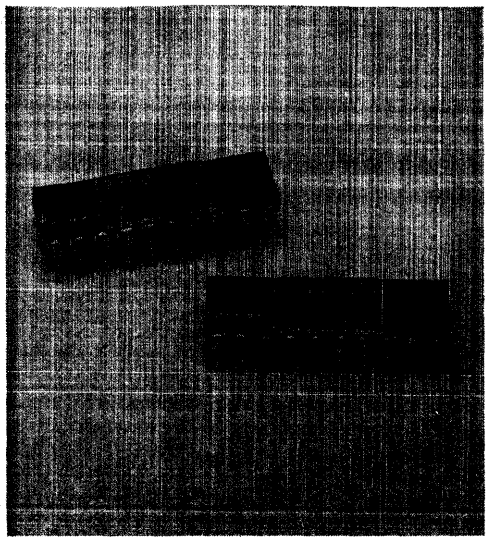
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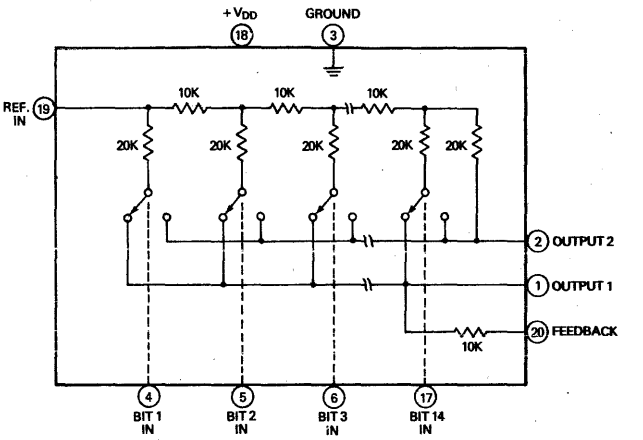
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DAC-HA14B

HIGH RESOLUTION, MULTIPLYING CMOS D/A CONVERTER

DATEL SYSTEMS, INC.





FEATURES

- **14 Bit Resolution**
- **2 & 4 Quadrant Multiplying**
- **7μsec. Settling Time**
- **5 ppm/°C Tempco, Max.**
- **20 MHz Reference Bandwidth**

The DAC-HA14B is a 14 bit, CMOS multiplying D/A converter. There are two versions, offering a choice of either +5 V or +15 V power supply operation. The +5 V model draws only 1 μA quiescent current while the +15 V model draws 1.4 mA. The device is packaged in a 20 pin ceramic DIP package.

The combination of low ON resistance CMOS switches and a laser-trimmed nichrome thin film resistor network result in a maximum nonlinearity of ±1 LSB with 14 bit monotonicity at 25°C. The gain temperature coefficient of the circuit is 5 ppm/°C maximum. The resistor network is an R-2R ladder with resistance values of 10K and 20K ohms.

The input resistance to the ladder is 10K ohms for the external reference source, which may be ±12 V. Bandwidth for the reference input is 20 MHz. The DAC-HA14B incorporates internal protection on the power supply and digital input terminals to prevent latch-up problems.

SPECIFICATIONS, Typical at 25°C

	DAC-HA14B
Resolution	14 Bits
Settling Time, to 1 LSB	7μsec.
Gain Tempco, max.	5 ppm/°C
Nonlinearity, max.	1 LSB
Differential Nonlinearity, max.	1 LSB
Monotonicity	At 25°C
Power Supply Sensitivity	5 ppm/%
Analog Output Current	±1 mA
Reference Input Range	±12 V
Reference Input Impedance	10K ±30%
Input Logic	TTL, CMOS
Coding, unipolar	Straight Binary
Coding, bipolar	Offset Binary
Power Requirement	+5 VDC @ 1μA +15 VDC @ 1.4 mA*
Package	20 pin DIP

*For models designated with – 1 suffix

ORDERING INFORMATION

Model	Oper. Temp. Range	Supply Voltage	Price (1-24)
DAC-HA14BC	0 to 70C	+5 V	$ 73.00
DAC-HA14BR	−25 to +85C	+5 V	104.00
DAC-HA14BM	−55 to +125C	+5 V	146.00
DAC-HA14BC-1	0 to 70C	+15 V	73.00
DAC-HA14BR-1	−25 to +85C	+15 V	104.00
DAC-HA14BM-1	−55 to +125C	+15 V	146.00

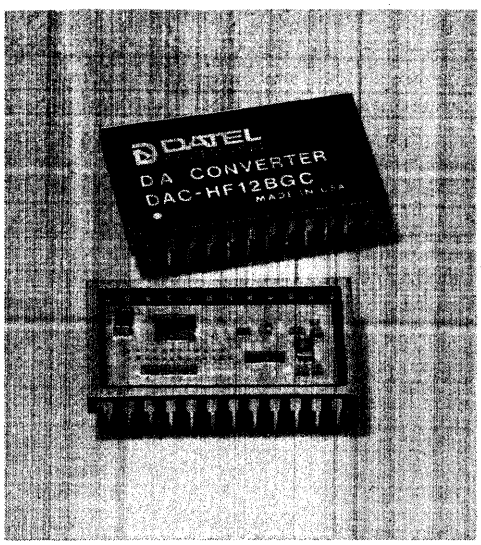
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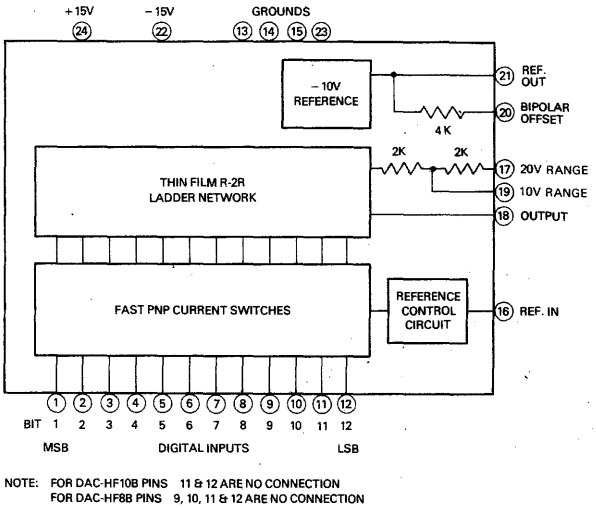
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DAC-HF SERIES

ULTRA-FAST, CURRENT OUTPUT D/A CONVERTERS

DATEL SYSTEMS, INC.





NOTE: FOR DAC-HF10B PINS 11 & 12 ARE NO CONNECTION
FOR DAC-HF8B PINS 9, 10, 11 & 12 ARE NO CONNECTION

FEATURES

- **8, 10, or 12 Bit Resolution**
- **25 nsec. Settling (8 or 10 Bits)**
- **50 nsec. Settling (12 Bits)**
- **Unipolar or Bipolar Operation**
- **5 mA Output Current**

The DAC-HF series features ultra-fast current outputs for 8, 10, and 12 bit resolutions. These state-of-the-art digital to analog converters give output settling times of 25 nanoseconds maximum for 8 and 10 bits and 50 nanoseconds maximum for 12 bits. They can be used to drive a load resistor directly for up to ±1.2 V outputs or with a fast inverting operational amplifier (Datel System's AM-500) for up to ±10 V outputs at sub-microsecond settling times. The required feedback resistors are incorporated inside the unit and give a selection of five different output ranges by external pin connection.

The circuit uses high speed PNP current switches combined with a low impedance R-2R ladder network. The network is fabricated with nichrome thin-film resistors which are then laser trimmed for optimum linearity. The output current is 0 to +5 mA or ±2.5 mA with a 400 ohm output impedance.

SPECIFICATIONS, Typical at 25°C

	DAC-HF8B	DAC-HF10B	DAC-HF12B
Resolution	8 Bits	10 Bits	12 Bits
Settling Time max.*	25 nsec.	25 nsec.	50 nsec.
Gain Tempco, max.	20 ppm/°C	20 ppm/°C	20 ppm/°C
Nonlinearity, max.	½ LSB	½ LSB	½ LSB
Diff. Nonlinearity, max.	½ LSB	½ LSB	½ LSB
Monotonicity	Over Operating Temp. Range		
Power Supply Sensitivity	0.01%/%	0.01%/%	0.01%/%
Analog Output Ranges	0 to +5 mA ±2.5 mA	0 to +5 mA ±2.5 mA	0 to +5 mA ±2.5 mA
Output Voltage Compliance	±1.2 V	±1.2 V	±1.2 V
Input Logic	DTL/TTL	DTL/TTL	DTL/TTL
Coding, unipolar	Straight Bin.	Straight Bin.	Straight Bin.
Coding, bipolar	Offset Bin.	Offset Bin.	Offset Bin.
Power Requirement	+15 VDC @ 30 mA −15 VDC @ 12 mA	+15 VDC @ 35 mA −15 VDC @ 12 mA	+15 VDC @ 40 mA −15 VDC @ 12 mA
Package	24 Pin	24 Pin	24 Pin

*To 1 LSB

ORDERING INFORMATION

Model	Oper. Temp. Range	Seal	Price (1-24)
DAC-HF8BGC	0 to 70C	Epoxy	$109.00
DAC-HF8BMC	0 to 70C	Hermetic	119.00
DAC-HF8BMR	−25 to +85C	Hermetic	159.00
DAC-HF8BMM	−55 to +125C	Hermetic	189.00
DAC-HF10BGC	0 to 70C	Epoxy	129.00
DAC-HF10BMC	0 to 70C	Hermetic	139.00
DAC-HF10BMR	−25 to +85C	Hermetic	179.00
DAC-HF10BMM	−55 to +125C	Hermetic	209.00
DAC-HF12BGC	0 to 70C	Epoxy	139.00
DAC-HF12BMC	0 to 70C	Hermetic	149.00
DAC-HF12BMR	−25 to +85C	Hermetic	189.00
DAC-HF12BMM	−55 to +125C	Hermetic	219.00

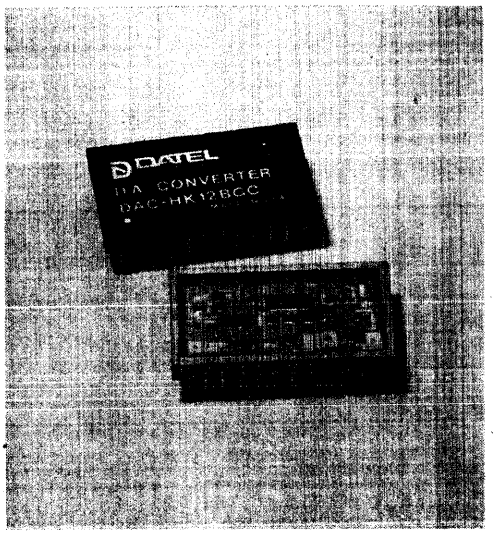
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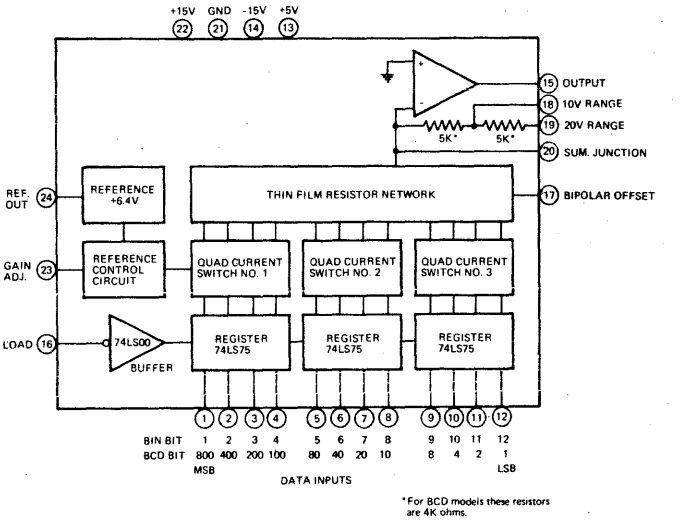
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DAC-HK SERIES

HIGH PERFORMANCE 12 BIT DAC'S WITH INPUT REGISTER

DATEL SYSTEMS, INC.





FEATURES

- **12 Bit Resolution**
- **Input Register**
- **20 ppm/°C Tempco**
- **Binary, BCD, or 2's Comp. Coding**
- **3 μsec. Settling Time**

The DAC-HK series D/A converters are high performance 12-bit devices with a fast settling voltage output. They incorporate a level controlled input storage register and are specifically designed for systems applications such as data-bus interfacing with computers. When the "load" input is high data in the storage register is held, and when the load input is low data is transferred through to the DAC. There are three basic models available by coding option: binary, BCD, and two's complement. The output voltage ranges are externally pin-programmable and include: 0 to +2.5 V, 0 to +5 V, 0 to +10 V, ±2.5 V, ±5 V, and ±10 V.

Quad current switches are combined with a low T.C. thin film resistor network and a low T.C. Zener reference to achieve better than 20 ppm/°C gain tempco. Optimum linearity is attained by functional laser trimming of the thin film nichrome resistors.

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SPECIFICATIONS, Typical at 25°C

	DAC-HK12B	DAC-HK12D
Resolution	12 Bits	3 Digits
Settling Time, to ½ LSB	3 μsec.	3 μsec.
Gain Tempco, max.	20 ppm/°C	20 ppm/°C
Nonlinearity, max.	½ LSB	¼ LSB
Differential Nonlinearity, max.	½ LSB	¼ LSB
Monotonicity	Over Oper. Temp. Range	
Power Supply Sensitivity	0.002%/%	0.002%/%
Analog Output Voltages	0 to +5 V	0 to +2.5 V
	0 to +10 V	0 to +5 V
	±2.5 V	0 to +10 V
	±5 V	—
	±10 V	—
Output Current	±5 mA	+5 mA
Input Logic	DTL/TTL	DTL/TTL
Coding, unipolar	Straight Bin.	BCD
Coding, bipolar	Offset Bin.	—
	Two's Comp.	—
Power Requirement	+15 VDC at 15 mA	
	−15 VDC at 30 mA	
	+5 VDC at 45 mA	
Package	24 Pin	

ORDERING INFORMATION

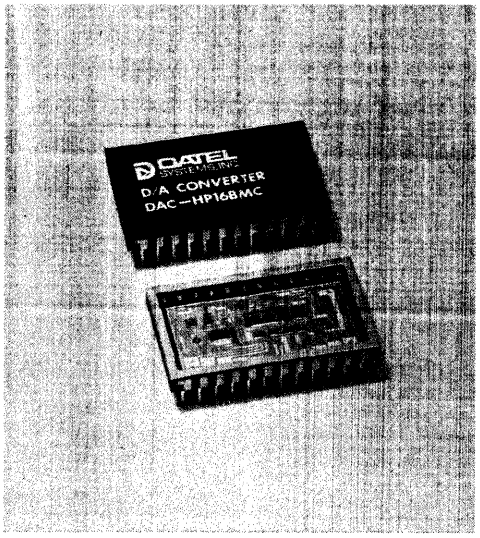
Model	Oper. Temp. Range	Coding	Seal	Price (1-24)
DAC-HK12BGC	0 to 70C	Binary	Epoxy	$ 62.00
DAC-HK12BMC	0 to 70C	Binary	Hermetic	73.00
DAC-HK12BMR	−25 to +85C	Binary	Hermetic	104.00
DAC-HK12BMM	−55 to +125C	Binary	Hermetic	146.00
DAC-HK12BGC-2	0 to 70C	2's Comp.	Epoxy	62.00
DAC-HK12BMC-2	0 to 70C	2's Comp.	Hermetic	73.00
DAC-HK12BMR-2	−25 to +85C	2's Comp.	Hermetic	104.00
DAC-HK12BMM-2	−55 to +125C	2's Comp.	Hermetic	146.00
DAC-HK12DGC	0 to 70C	BCD	Epoxy	62.00
DAC-HK12DMC	0 to 70C	BCD	Hermetic	73.00
DAC-HK12DMR	−25 to +85C	BCD	Hermetic	104.00
DAC-HK12DMM	−55 to +125C	BCD	Hermetic	146.00

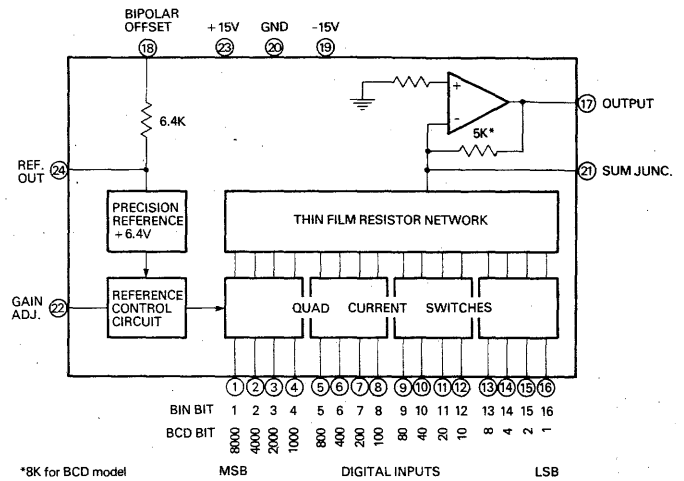
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DAC-HP16B, DAC-HP16D

HIGH RESOLUTION D/A CONVERTERS

DATEL SYSTEMS, INC.





INTERFACE

Datel

FEATURES

- **16 Bit Binary Model**
- **4 Digit BCD Model**
- **Linearity to 0.003%**
- **15 ppm/°C Tempco, Max.**
- **Voltage Output**

The DAC-HP series are high resolution D/A converters with voltage output. They are self-contained, including a low tempco zener reference circuit and output operational amplifier, all in a miniature 24 pin double spaced ceramic DIP package. There are two basic models in the series. The DAC-HP16B has 16 bit binary resolution with ±0.003% linearity while the DAC-HP16D has 4 digit BCD resolution with ±0.005% linearity. Input coding is complementary binary and complementary offset binary for the DAC-HP16B and complementary BCD for the DAC-HP16D. The binary version operates in both unipolar and bipolar modes with output voltages of 0 to +10 V and ±5 V; the BCD version operates in unipolar mode only with 0 to +10 V output.

The DAC-HP design incorporates thin film hybrid technology which has been in volume production. Selected low tempco nichrome on silicon thin film resistor networks are combined with tightly matched quad current switches to achieve 16 bit resolution.

SPECIFICATIONS, Typical at 25°C

	DAC-HP16B	DAC-HP16D
Resolution	16 Bits	4 Digits
Settling Time	35 μsec.	15 μsec.
Gain Tempco, max.	15 ppm/°C	15 ppm/°C
Nonlinearity, max.	0.003%	0.005%
Monotonicity, 10°C to 40°C	14 Bits	16 Bits
Power Supply, Sensitivity	0.002%/%	0.002%/%
Analog Output Ranges	0 to +10 V ±5 V	0 to +10 V —
Output Current	±5 mA	+5 mA
Input Logic	DTL/TTL	DTL/TTL
Coding, unipolar	Comp. Bin.	Comp. BCD
Coding, bipolar	Comp. Off. Bin.	—
Power Requirement	+15 VDC at 42 mA −15 VDC at 36 mA	
Package	24 Pin	

ORDERING INFORMATION

Model	Oper. Temp. Range	Seal	Price (1-24)
DAC-HP16BMC	0 to 70C	Hermetic	$125.00
DAC-HP16BMR	−25 to +85C	Hermetic	156.00
DAC-HP16BMM	−55 to +125C	Hermetic	219.00
DAC-HP16DMC	0 to 70C	Hermetic	125.00
DAC-HP16DMR	−25 to +85C	Hermetic	156.00
DAC-HP16DMM	−55 to +125C	Hermetic	219.00

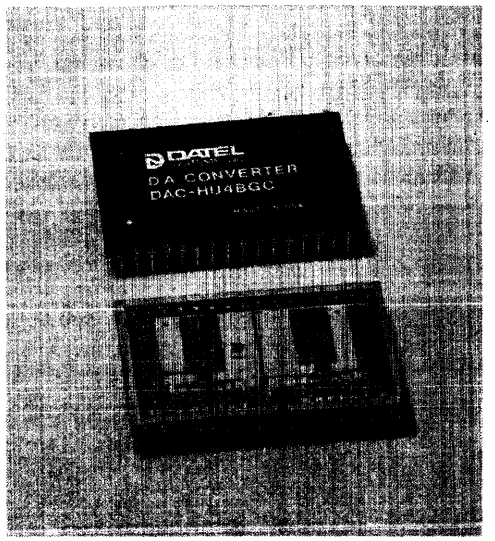
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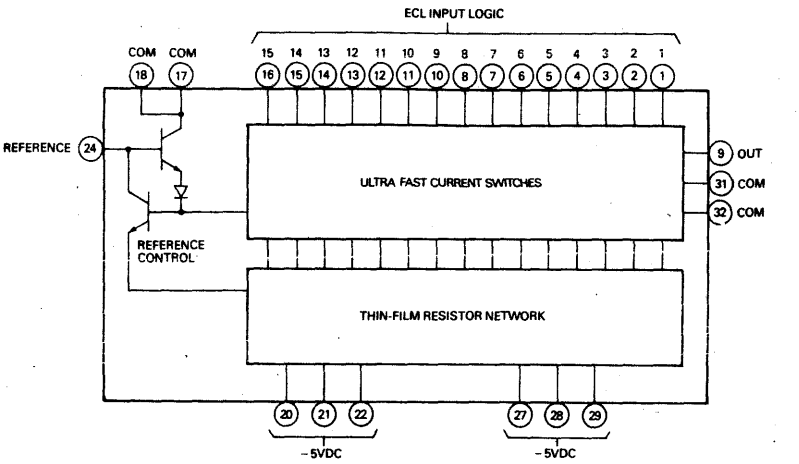
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DAC-HU4B

ULTRA-FAST, 4 BIT D/A CONVERTER

DATEL SYSTEMS, INC.





FEATURES

- **4 Bit Resolution**
- **25 nsec. Settling to 0.1%**
- **24 mA Output Current**
- **0.1% Linearity**
- **ECL 10,000 Input Logic**

The DAC-HU4B is an ultra-fast 4 bit hybrid DAC which is specifically designed as a building block component for use with Datel System's ADC-HU3B A/D converters in ultra high speed two stage A/D converters. The DAC-HU4B has a 15 line ECL 10,000 complementary input designed to be driven from two ADC-HU3B's. The output current is 24 mA with all of the current switches on and settling time to 0.1% is only 25 nsec. By connecting the input logic lines together in groups of 8, 4, 2, and 1, complementary binary coding can be realized.

In order to be used in higher resolution A/D converters, this device has a linearity of 0.1%.

The gain temperature coefficient of this circuit is 15 ppm/°C without the external reference. The power to this device is supplied from an operational amplifier which operates from an external reference. The nominal supply voltage is −5 V at 25 mA.

SPECIFICATIONS, Typical at 25°C

	DAC-HU4B
Resolution	4 Bits
Settling Time, to 0.1% FS	25 nsec.
Gain Tempco	15 ppm/°C
Nonlinearity, max.	0.1% FS
Diff. Nonlinearity, max.	0.1% FS
Monotonicity	Over Op. Temp. Range
Analog Output	0 to 24 mA FS
Output Voltage Compliance	±0.6 V
Output Impedance, min.	50K ohms
Output Leakage Current	100 nA
Input Logic	ECL 10,000
Coding	Complementary 15 line Complementary Binary
Power Requirement	−5 VDC at 25 mA
Package	32 Pin

ORDERING INFORMATION

Model	Oper. Temp. Range	Seal	Price (1-24)
DAC-HU4BGC	0 to 70C	Epoxy	$125.00
DAC-HU4BMC	0 to 70C	Hermetic	136.00
DAC-HU4BMR	−25 to +85C	Hermetic	178.00
DAC-HU4BMM	−55 to +125C	Hermetic	209.00

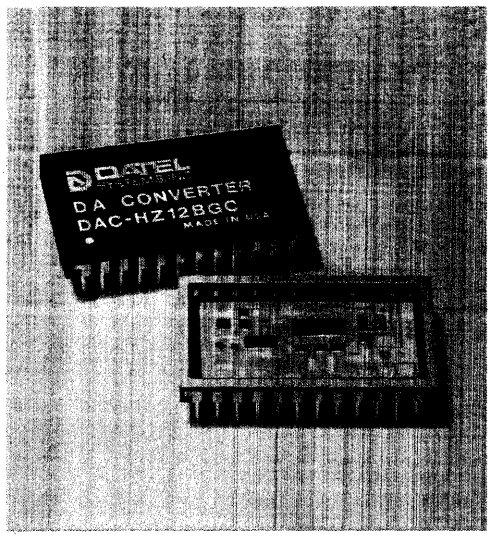
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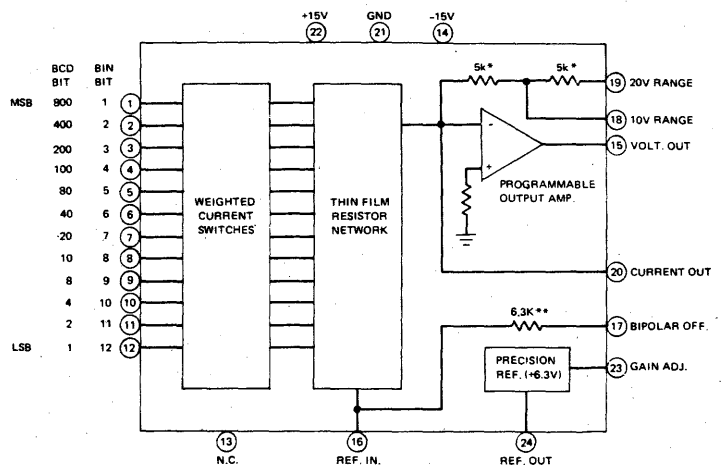
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DAC-HZ12B SERIES

DATEL SYSTEMS, INC.

LOW COST, HIGH PERFORMANCE 12 BIT D/A CONVERTERS





FEATURES

- **12 Bits Binary**
- **3 Digits BCD**
- **5 Output Ranges**
- **3 μsec. Settling Time**
- **20 ppm/°C Tempco**

The DAC-HZ series are high performance, hybrid 12 bit binary and 3 digit BCD digital-to-analog converters. They are complete and self-contained with a precision internal reference and fast output operational amplifier. Pin programmable output voltage ranges are provided for a high degree of application flexibility; the output voltage ranges are 0 to +5 V, 0 to +10 V, ±2.5 V, ±5 V, and ±10 V with only unipolar ranges available on the BCD models.

The internal design utilizes three quad current switches, two thin film resistor networks, a precision zener reference circuit, reference control circuit and output amplifier. The thin film resistor networks are functionally trimmed with a laser to precisely set the binary weights of the current switches. The excellent tracking of the thin film resistors in conjunction with the tightly matched current switches results in a differential nonlinearity tempco of only 2 ppm/°C.

SPECIFICATIONS, Typical at 25°C

	DAC-HZ12B	DAC-HZ12D
Resolution	12 Bits	3 Digits
Settling Time, to ½ LSB	3 μsec.	3 μsec.
Gain Tempco, max.	20 ppm/°C	20 ppm/°C
Nonlinearity, max.	½ LSB	¼ LSB
Diff. Nonlinearity, max.	½ LSB	¼ LSB
Monotonicity	Over Op. Temp. Range	
Power Supply Sensitivity	0.002%/%	0.002%/%
Analog Output Ranges	0 to +5 V	0 to +2.5 V
	0 to +10 V	0 to +5 V
	±2.5 V	0 to +10 V
	±5 V	—
	±10 V	—
Output Current	±5 mA	+5 mA
Input Logic	DTL/TTL	DTL/TTL
Coding, unipolar	Comp. Bin.	Comp. BCD
Coding, bipolar	Comp. Off. Bin.	—
Power Requirement	±15 VDC at 35 mA	
Package	24 Pin	

ORDERING INFORMATION

Model	Oper. Temp. Range	Seal	Price (1-24)
DAC-HZ12BGC	0 to 70C	Epoxy	$ 39.00
DAC-HZ12BGR	−25 to +85C	Epoxy	58.00
DAC-HZ12BMC	0 to 70C	Hermetic	52.00
DAC-HZ12BMR	−25 to +85C	Hermetic	73.00
DAC-HZ12BMM	−55 to +125C	Hermetic	125.00
DAC-HZ12DGC	0 to 70C	Epoxy	39.00
DAC-HZ12DGR	−25 to +85C	Epoxy	58.00
DAC-HZ12DMC	0 to 70C	Hermetic	52.00
DAC-HZ12DMR	−25 to +85C	Hermetic	73.00
DAC-HZ12DMM	−55 to +125C	Hermetic	125.00

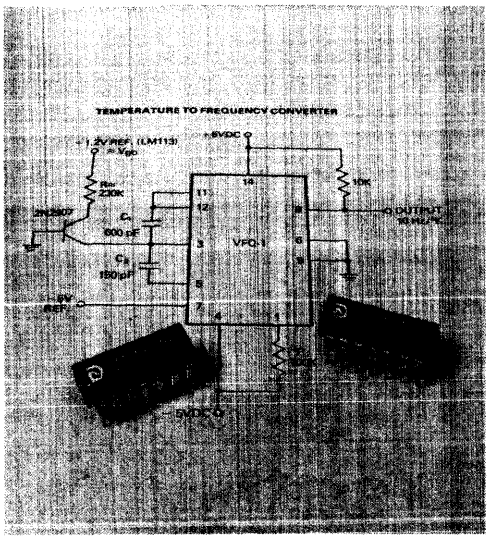
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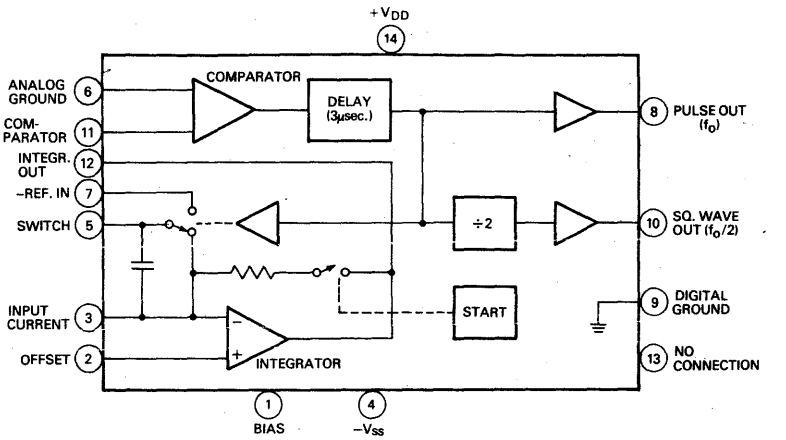
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VFQ-1

MONOLITHIC VOLTAGE TO FREQUENCY CONVERTER

DATEL SYSTEMS, INC.





FEATURES

- **10 kHz to 100 kHz FS**
- **0.01% Typ. Linearity at 10 kHz**
- **25 ppm/°C Tempco**
- **Open Collector Output**
- **Pulse or Square Wave Output**

Model VFQ-1 is a new monolithic voltage to frequency converter using combined bipolar and CMOS technologies. This device accepts a positive analog input current and produces an output pulse train with a frequency linearly proportional to an input current. In addition to the pulse output, there is also a square wave output at half the pulse frequency. The full scale output pulse rate can be set from 10 kHz to 100 kHz by means of two external capacitors. Linearities are typically 0.01% for 10 kHz full scale and 0.1% for 100 kHz full scale; linearity holds all the way down to zero.

The VFQ-1 internal circuitry includes an operational integrator, a comparator, digital delay circuit, single-pole double-throw electronic switch, a start circuit, a divide by two circuit, and two output driver circuits. It operates on the well-known charge balancing integrator principle. The two outputs are open collector NPN which can sink up to 10 mA and give a logic HI output up to +18 volts.

SPECIFICATIONS Typical at 25°C

	VFQ-1
Output Frequency	0 to 10 kHz 0 to 100 kHz
Linearity 10 kHz FS	0.01%
Linearity, 100 kHz FS	0.1%
Gain Tempco	25 ppm/°C
Output	Open Collector TTL
Output Waveforms	Pulses at f_O Sq. Wave at $f_O/2$
Output Settling Time	2 pulses
Input Current Range	0 to +10 μA
Input Overrange	+50 μA
Input Offset Voltage	50 mV
Reference Input	−3.5 to −6.5 V
Zero Drift	50 μV/°C max.
Power Supply Sensitivity	0.025%/V
Power Requirement	±5 V at 4 mA
Package	16 Pin DIP

ORDERING INFORMATION

Model	Oper. Temp. Range	Package	Price (1-24)
VFQ-1C	0 to 70C	Plastic	$ 7.95
VFQ-1R	−25 to +85C	Ceramic	13.50

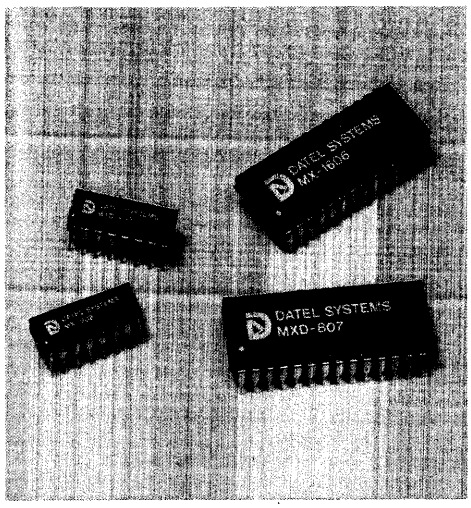
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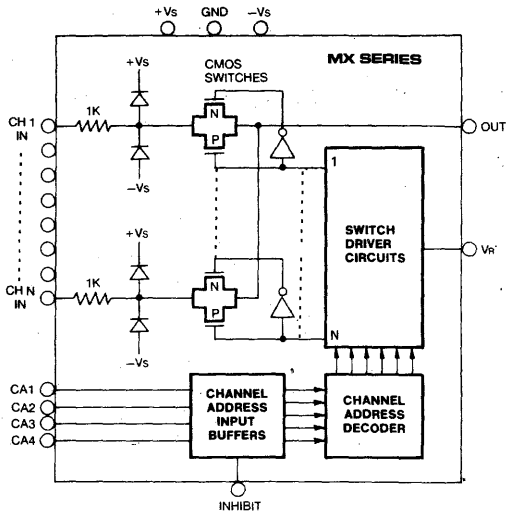
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MX AND MV SERIES

MONOLITHIC CMOS ANALOG MULTIPLEXERS

DATEL SYSTEMS, INC.





INTERFACE

Datel

FEATURES

- **Dielectrically Isolated CMOS**
- **Break-Before-Make Switching**
- **4, 8, and 16 Channels**
- **Single Ended and Differential**
- **Low Power Consumption**

This broad line of monolithic CMOS multiplexers offers 4 through 16 channel performance. The MX series has overvoltage protected switches with 1.5K ON resistance for 4, 8, and 16 channel applications while the MV series provides a lower 270 ohm ON resistance. Both single ended and differential input versions are available.

These devices are fabricated with a dielectrically isolated complementary MOS process. The digital inputs are DTL, DTL, and CMOS compatible and address the proper channel switch by means of a 2, 3, or 4 bit binary code. An inhibit input enables or disables the entire device and thus permits expansion of the number of channels by using several multiplexers together. Another important feature is the use of break-before-make switching to insure that no two channels are ever momentarily shorted together.

These multiplexers are ideal for multi-channel data acquisition systems where the multiplexer operates into a high impedance load such as a buffer amplifier or sample-hold.

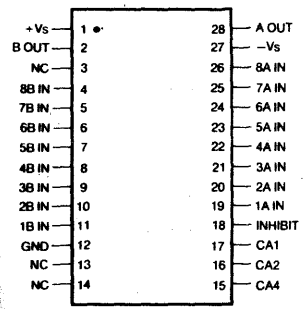
SPECIFICATIONS, Typical at 25°C

	MXD-409	MX-808
Number of Channels	4	8
Type Input	Differ.	Sing. End.
Input Voltage Range	±15V	±15V
Input Overvoltage, max.	±35V	±35V
Channel ON Resistance	1.5K	1.5K
Channel OFF Resistance	200 Meg.	200 Meg.
Channel OFF Leakage	30 pA	30 pA
Channel Addressing	2 bit code	3 bit code
Address Logic Compatibility	DTL/TTL/CMOS	DTL/TTL/CMOS
Transfer Accuracy	.01%	.01%
Crosstalk	−86 dB	−86 dB
Common Mode Rejection	120 dB	—
Turn ON Time	500 nsec.	500 nsec.
Turn OFF Time	300 nsec.	300 nsec.
Power Requirement	±15V	±15V
Package	16 Pin DIP	16 Pin DIP
Operating Temp. Range	0 to 70°C	0 to 70°C
Price (1-24)	$18.00	$18.00
MIP—Version (−55 to +125°C)	MXD-409M	MX-808M
MIL—Version Price	$54.00	$54.00

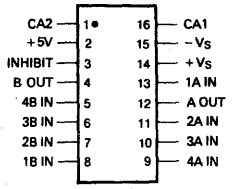
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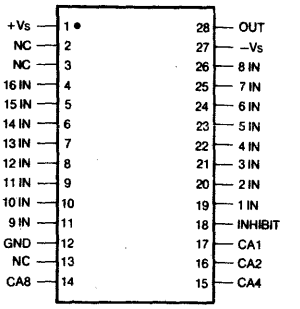
MVD-807



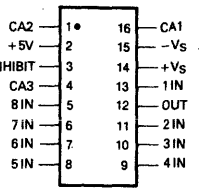
MVD-409



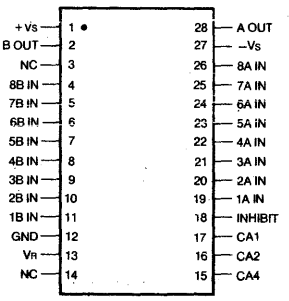
MV-1606



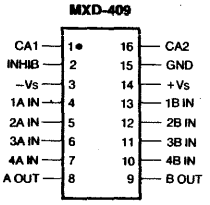
MV-808



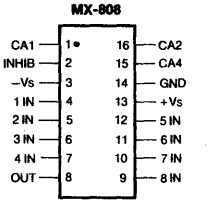
MXD-807



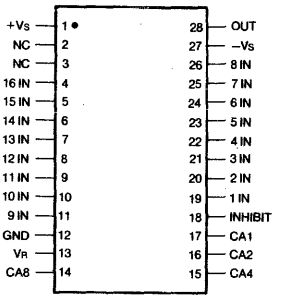
MXD-409



MX-808



MX-1606



MXD-807	MX-1606	MVD-409	MV-808	MVD-807	MV-1606
8	16	4	8	8	16
Differ.	Sing. End.	Differ.	Sing. End.	Differ.	Sing. End.
±15V	±15V	±15V	±15V	±15V	±15V
±35V	±35V	±17V	±17V	±17V	±17V
1.5K	1.5K	250Ω	250Ω	270Ω	270Ω
200 Meg.	200 Meg.	200 Meg.	200 Meg.	200 Meg.	200 Meg.
30 pA	30 pA	20 pA	20 pA	30 pA	30 pA
3 bit code DTL/TTL/CMOS	4 bit code DTL/TTL/CMOS	2 bit code DTL/TTL/CMOS	3 bit code DTL/TTL/CMOS	3 bit code DTL/TTL/CMOS	4 bit code DTL/TTL/CMOS
.01%	.01%	.01%	.01%	.01%	.01%
−86 dB	−86 dB	−86 dB	−86 dB	−86 dB	−86 dB
120 dB	—	120 dB	—	120 dB	—
500 nsec.	500 nsec.	350 nsec.	350 nsec.	300 nsec.	300 nsec.
300 nsec.	300 nsec.	250 nsec.	250 nsec.	300 nsec.	300 nsec.
±15V	±15V	±15V,+5V	±15V,+5V	±15V	±15V
28 Pin	28 Pin	16 Pin DIP	16 Pin DIP	28 Pin	28 Pin
0 to 70°C	0 to 70°C	0 to 70°C	0 to 70°C	0 to 70°C	0 to 70°C
$32.50	$32.50	$16.00	$16.00	$19.50	$19.50
MXD-807M	MX-1606M	MVD-409M	MV-808M	MVD-807M	MV-1606M
$75.00	$75.00	$41.00	$41.00	$57.00	$57.00

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NOTES:

CA = CHANNEL ADDRESS
Vs = SUPPLY VOLTAGE
VR = REFERENCE VOLTAGE
NC = NO CONNECTIONS

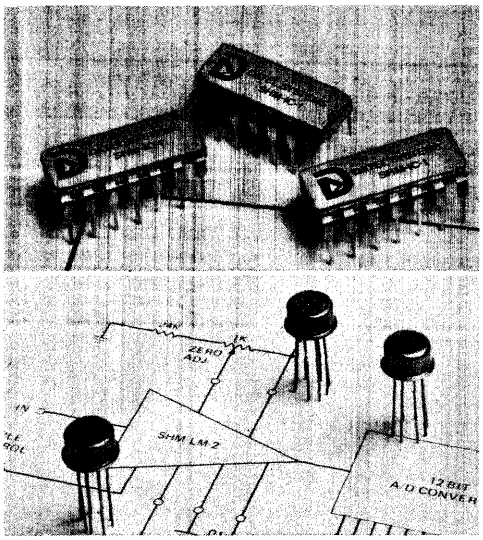
TOP VIEWS SHOWN

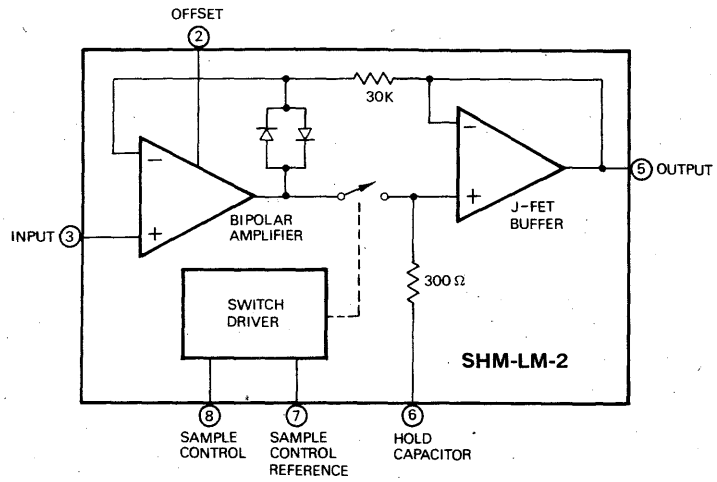
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SHM-IC-1, SHM-LM-2

MONOLITHIC SAMPLE-HOLDS

DATEL SYSTEMS, INC.





INTERFACE

Datel

FEATURES

- **Acquisition Time to 5 μsec.**
- **0.01% Accuracy**
- **Bandwidth to 2 MHz**
- **0.01% Feedthrough**
- **Low Cost**

These monolithic sample-hold devices feature excellent performance specifications at a low price. They are self-contained units requiring only an external hold capacitor for operation. The SHM-LM-2 operates in a fixed gain configuration of +1 while the SHM-IC-1 can be externally connected for gains of ±1 or for higher gains by means of two external resistors. Both models consist of a high impedance input amplifier, a fast electronic switch, and a high impedance output buffer amplifier. The circuit operates in a closed loop configuration for maximum accuracy.

Accuracy is 0.01% for both models making them useful in 12 bit A/D converter applications. For a 1000pF hold capacitor the acquisition time is 5 μsec. for the SHM-IC-1 and 6 μsec. for the SHM-LM-2. Better accuracy with lower feedthrough and hold mode droop can be achieved by using higher value hold capacitance such as .01 μF.

SPECIFICATIONS, Typical at 25°C, C_H = 1000pF

	SHM-IC-1	SHM-LM-2
Accuracy	0.01%	0.01%
Acquisition Time to 0.01%	5 μsec.	6 μsec.
Acquisition Time to 0.1%	4 μsec.	5 μsec.
Aperture Delay Time	50 nsec.	100 nsec.
Hold Mode Droop	50 μV/msec.	200 μV/msec.
Hold Mode Feedthrough, max.	0.01%	0.01%
Bandwidth	2 MHz	1 MHz
Sample-to-Hold Error, max.	20 mV	25 mV
Gain	±1	+1
Input Voltage Range, min.	±10 V	±11.5 V
Input Impedance	10^8 ohms	10^{10} ohms
Input Bias Current, max.	200 nA	50 nA
Input Offset Voltage Drift	20 μV/°C	10 mV*
Digital Control	DTL, TTL	DTL, TTL, CMOS
Output Voltage, min.	±10 V	±11.5 V
Output Current	±5 mA	±5 mA
Power Requirement	±15 V at 5 mA	±15 V at 6 mA
Package	14 Pin DIP	TO-99

*Over Oper. Temp. Range

ORDERING INFORMATION

Model	Oper. Temp. Range	Package	Price (1-24)
SHM-IC-1	0 to 70C	Ceramic	$12.00
SHM-IC-1M	−55 to +125C	Ceramic	53.00
SHM-LM-2	0 to 70C	Metal	6.50
SHM-LM-2M	−55 to +125C	Metal	50.00

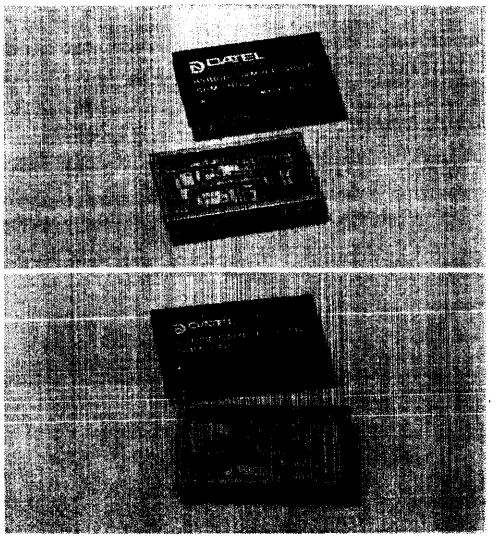
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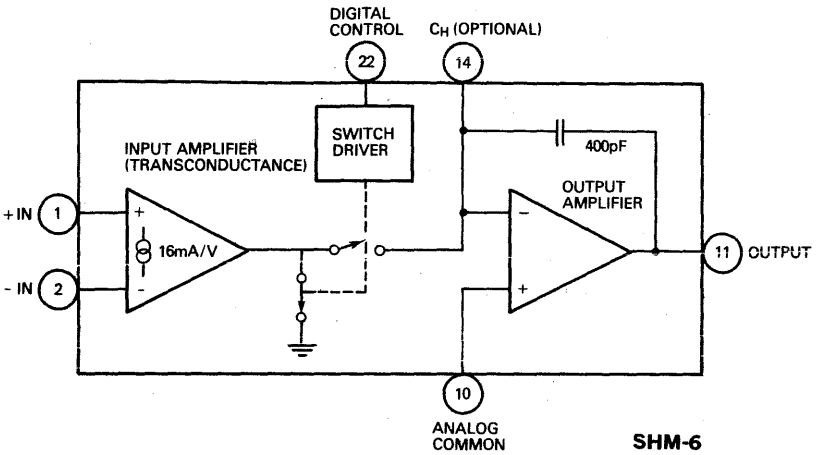
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SHM-6, SHM-HU

FAST, HYBRID SAMPLE-HOLDS

DATEL SYSTEMS, INC.





FEATURES

- **0.01% Accuracy (SHM-6)**
- **1.0 μsec. Acquisition Time (SHM-6)**
- **25 nsec. Acquisition Time (SHM-HU)**
- **50 MHz Bandwidth (SHM-HU)**
- **50 mA Output (SHM-6)**

These hybrid sample-hold circuits feature fast and ultra-fast acquisition times. The SHM-6 is designed for use with fast 12 bit A/D converters. Its accuracy is 0.01% and acquisition time is 1.0 μsec. maximum. Bandwidth is 5 MHz and aperture delay time is 20 nsec. In addition to its high accuracy and high speed this model also has a 50 mA output current. The input amplifier of the SHM-6 is an open loop transconductance amplifier which can be externally connected for closed loop gains of ±1 to ±10. The hold capacitor, of value 400pF, is included internally.

The SHM-HU is an ultra high speed sample-hold designed for video processing applications. It is specifically designed for use with Datel System's ADC-HU3B A/D converter and other ultra fast A/D's with resolutions up to 8 bits. It acquires a 5 V input change in just 25 nsec. and features a 10 psec. aperture uncertainty time. A 53 pF MOS hold capacitor is incorporated in the unit. The SHM-HU requires 4 external resistors and an external LH003 buffer amplifier.

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SPECIFICATIONS, Typical at 25°C

	SHM-6	SHM-HU
Accuracy	0.01%	0.1%
Acquisition time, to 0.01% max.	1.0 μsec.	—
Acquisition time, to 0.2%	—	25 nsec.
Aperture Delay Time	20 nsec.	6 nsec.
Aperture Uncertainty Time	2 nsec.	10 psec.
Hold Mode Droop	10 μV/μsec.	50 μV/μsec.
Hold Mode Feedthrough	0.01%	0.02%
Bandwidth	5 MHz	50 MHz
Sample-to-Hold Error	Adj. to zero	100 mV
Gain	±1 to 10	+0.975
Input Voltage Range, min.	±10 V	±2.5 V
Input Impedance	10^8 ohms	10^6 ohms
Input Bias Current, max.	10 nA	5 μA
Input Offset Voltage Drift	100 μV/°C	100 μV/°C
Digital Control	DTL, TTL	Diff. ECL
Output Voltage	±10 V	±2.5 V
Output Current	±50 mA	±10 mA
Power Requirement	+15 V at 55 mA −15 V at 60 mA +5 V at 30 mA	±15 V at 60 mA ±5 V at 70 mA
Package	32 Pin	24 Pin

ORDERING INFORMATION

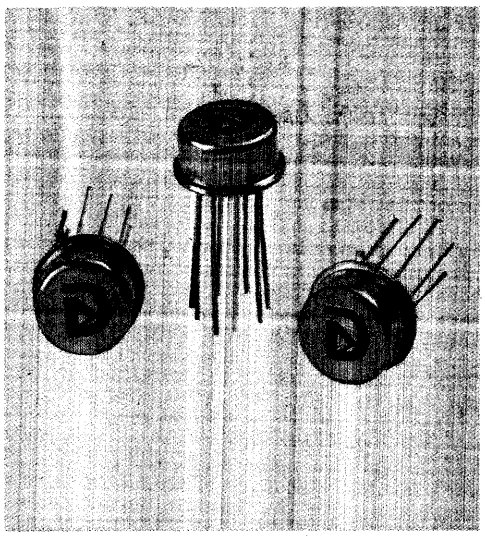
Model	Oper. Temp. Range	Seal	Price (1-24)
SHM-6GC	0 to 70C	Epoxy	$135.00
SHM-6MC	0 to 70C	Hermetic	146.00
SHM-6MR	−25 to +85C	Hermetic	188.00
SHM-6MM	−55 to +125C	Hermetic	219.00
SHM-HUGC	0 to 70C	Epoxy	135.00
SHM-HUMC	0 to 70C	Hermetic	146.00
SHM-HUMR	−25 to +85C	Hermetic	188.00
SHM-HUMM	−55 to +125C	Hermetic	219.00

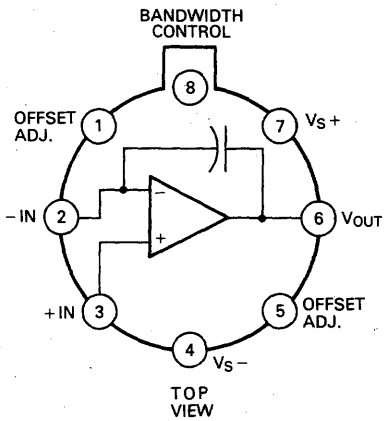
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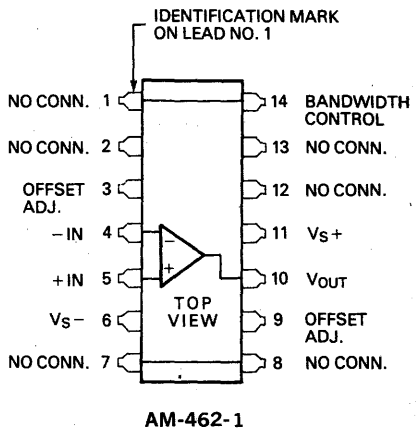
AM-400 SERIES

WIDE BANDWIDTH, FAST SETTLING OPERATIONAL AMPLIFIERS

DATEL SYSTEMS, INC.







AM-462-1

FEATURES

- **Gain Bandwidth to 100 MHz**
- **Slew Rate to 120 V/μsec.**
- **FET or Bipolar Inputs**
- **Settling Time to 200 nsec.**
- **CMRR to 100 dB**

This broad line of monolithic operational amplifiers is specifically designed for data acquisition and conversion applications where high speed is required. These amplifiers feature large gain bandwidth products, high slew rate, and fast settling times. In addition to these high speed characteristics they also have excellent DC parameters, making them good choices for high accuracy applications. The DC characteristics include low input bias currents, high input impedance, low input offset voltage drift, and high common mode rejection.

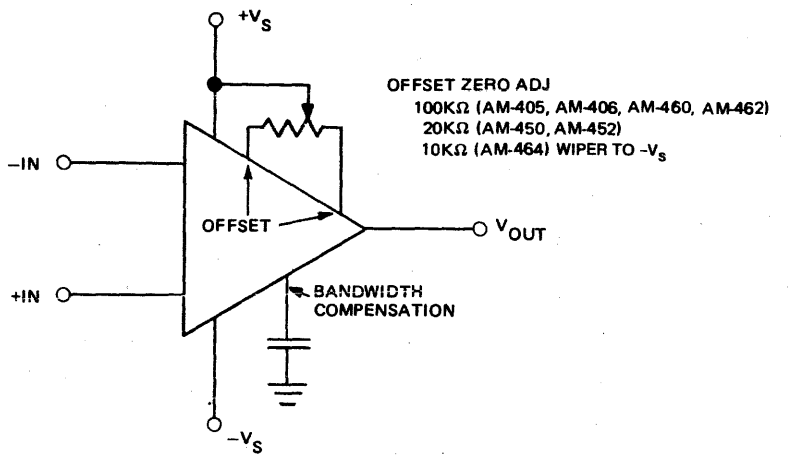
Four basic models of bipolar input amplifiers are offered together with two FET input models. The AM-464-2 is a fast settling amplifier with ±35V output swing for use in high output voltage DAC's and other high voltage applications.

These amplifiers are also useful in many other applications such as sample-hold circuits, high impedance buffer amplifiers, fast signal summing and fast absolute value circuits.

SPECIFICATIONS Typical at 25°C

	MOD. SLEW RATE AM-450-2	FAST SETTLING AM-452-2
DC Open Loop Gain	25K	15K
Gain Bandwidth Product	12 MHz	20 MHz
Slew Rate	30V/μsec.	120V/μsec.
Settling Time, 10V to 0.1%	330 nsec.	200 nsec.
Output, min.	±10V @ 10mA	±10V @ 10mA
Common Mode Range, min.	±10V	±10V
Common Mode Rejection	90 dB	90 dB
Input Impedance	50 Meg.	100 Meg.
Input Bias Current, max.	250nA	250nA
Input Offset Current, max.	50nA	50nA
Input Offset Voltage, max., adj. to 0	±8mV	±10mV
Input Offset Voltage Drift	20μV/°C	30μV/°C
Power Requirement	±15V @ 4mA	±15V @ 4mA
Temperature Range	0°C to 70°C	0°C to 70°C
Package	TO-99	TO-99
Price (1-24)	$7.95	$11.00
MIL-Version (−55°C to +125°C)	AM-450-2M	AM-452-2M
MIL-Version Price	$14.00	$25.00

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LOW COST AM-460-2	WIDEBAND AM-462-1/2	FAST SLEW FET AM-405-2	WIDEBAND FET AM-406-2	±35V SWING AM-464-2
150K	150K	15K	150K	100K
12 MHz	100 MHz	20 MHz	100 MHz	4 MHz
7V/μsec.	35V/μsec.	120V/μsec.	35V/μsec.	5V/μsec.
1.5 μsec.	1.0 μsec.	400 nsec.	—	—
±10V @ 10mA	±10V @ 10mA	±10V @ 10mA	±10V @ 10mA	±35V @ 10mA
±11V	±11V	±10V	±10V	±35V
100 dB	100 dB	90 dB	90 dB	74 dB
300 Meg.	300 Meg.	10^{12} ohms	10^{12} ohms	200 Meg.
25nA	25nA	20 pA	20 pA	30nA
25nA	25nA	20 pA	20 pA	30nA
±5mV	±5mV	±30mV	±15mV	±6mV
10μV/°C	15μV/°C	50μV/°C	50μV/°C	15μV/°C
±15V @ 3mA	±15V @ 3mA	±15V @ 6mA	±15V @ 4mA	±10V to ±40V @ 3.2mA
0°C to 70°C	0°C to 70°C	0°C to 70°C	0°C to 70°C	0°C to 70°C
TO-99	TO-116/TO-99	TO-99	TO-99	TO-99
$6.95	$9.50	$18.00	$15.00	$7.50
AM-460-2M	AM-462-1M/2M	AM-405-2M	AM-406-2M	AM-464-2M
$14.00	$17.00	$37.00	$29.00	$34.00

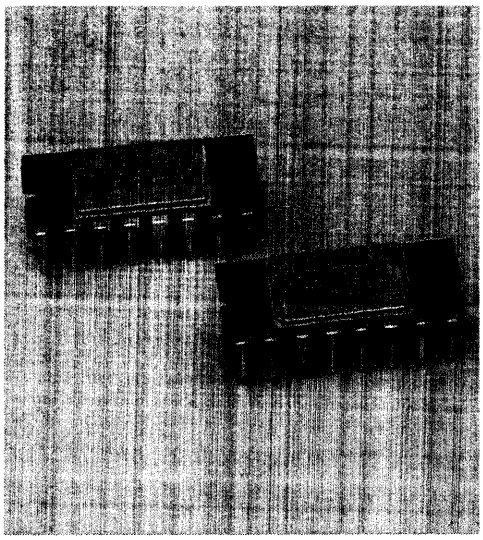
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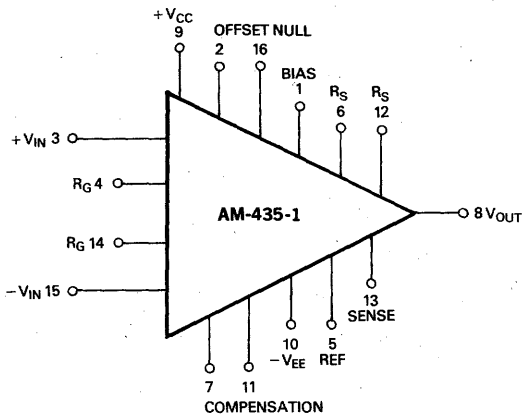
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AM-435

MONOLITHIC, FET INPUT INSTRUMENTATION AMPLIFIER

DATEL SYSTEMS, INC.





FEATURES

- **2 x 10^{12} Ohms Input Z**
- **0.02% Gain Linearity**
- **105 dB min. CMRR**
- **Low Noise JFET Inputs**
- **Single Resistor Gain Adjust**

DESCRIPTION

The AM-435 is a low cost, high performance, monolithic instrumentation amplifier. Tightly matched JFET input devices give very high input impedance with very low bias currents and low input offset voltage drift. The AM-435 is ideal for applications where high differential source impedances are encountered.

This amplifier is programmed by means of two external resistors, R_S and R_G. With R_S at a set value the gain may be varied from 1 to 1000 by changing R_G. Provision is also made for an external offset adjustment by means of a trimming potentiometer. Input impedance is 2 x 10^{12} ohms with bias currents of 40 pA maximum. Common mode rejection is greater than 105 dB at a gain of 1000. Input noise current is only 0.01 pA RMS and gain nonlinearity is typically 0.02%. The input offset voltage drift is typically 10μV/°C and output offset voltage drift is 600μV/°C.

SPECIFICATIONS, Typical at 25°C, G=1000

	AM-435-1C	AM-435-1M
Gain Range	1 to 1000	1 to 1000
Gain Nonlinearity	0.1%	0.05%
Gain Equation	R_S/R_G	R_S/R_G
Gain Tempco	3ppm/°C	3ppm/°C
Gain Equation Accuracy	0.05%	0.05%
Input Impedance	2 x 10^{12} ohms	2 x 10^{12} ohms
Input Bias Current, max.	40 pA	20 pA
Input Offset Current, max.	20 pA	10 pA
Input Offset Voltage, max.	30 mV	15 mV
Input Off. Voltage Drift	10μV/°C	10μV/°C
Output Off. Voltage Drift, G=1	600μV/°C	600μV/°C
Input Voltage Range, min.	±10V	±10V
Output	±10V at 5mA	±10V at 5mA
Common Mode Rej, G=1000	105 dB	115 dB
Bandwidth, G=1000	7KHz	7KHz
Slew Rate	1V/μsec.	1V/μsec.
Power Requirement	±15VDC at 1.5 mA	
Package	16 Pin DIP	

ORDERING INFORMATION

Model	Oper. Temp. Range	Package	Price (1-24)
AM-435-1C	0 to 70C	Ceramic	$11.50
AM-435-1M	−55 to +125C	Ceramic	27.00

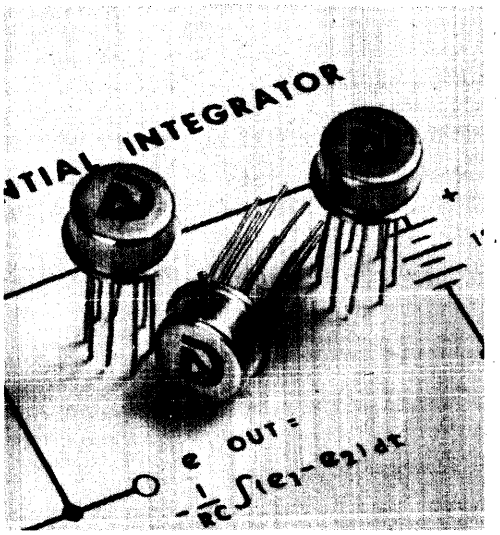
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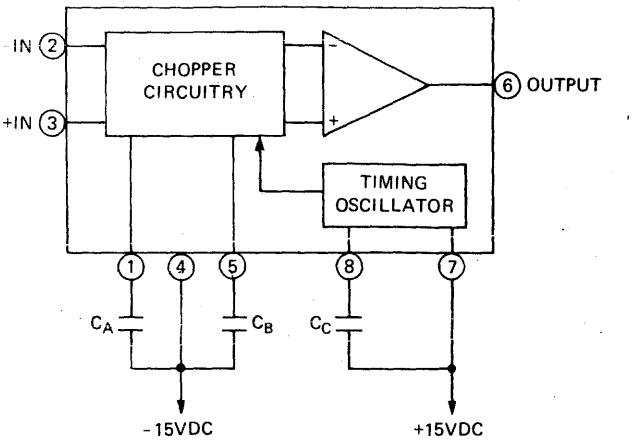
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AM-490-2

DATEL SYSTEMS, INC.

MONOLITHIC, DIFFERENTIAL INPUT CHOPPER STABILIZED OP AMP





FEATURES

- **Differential Inputs**
- **120 dB CMR**
- **Chopper Stabilized**
- **Drift as Low as 0.1 μV/°C**
- **5 x 10^8 Open Loop Gain**

Model AM-490-2 is a monolithic, chopper stabilized operational amplifier with differential inputs; it is specifically designed for applications requiring ultra-stable DC characteristics together with good bandwidth. This device is available in three different grades of maximum input offset voltage drift: 1.0, 0.3, and 0.1μV/°C. The extremely low input offset voltage drift and initial input offset voltage of only 20μV eliminate the requirement for zero adjustment in most applications. Other important input characteristics include an input impedance of 100 megohms, input bias current of 150pA, and input offset current drift of 1pA/°C. This permits the AM-490-2 to operate accurately with source impedances over 100 kilohms. A common mode rejection of 120 dB minimum and open loop gain of 5 x 10^8 result in extremely low output errors. Long term stability is typically 5μV per year.

SPECIFICATIONS, Typical at 25°C

	AM-490-2			
	A	**B**	**C**	**M**
DC Open Loop Gain		5 x 10^8		
Gain Bandwidth Product		3 MHz		
Slew Rate		2.5 V/μsec.		
Full Power Frequency		40 kHz		
Overload Recovery Time		200 msec.		
Output		±10 V at 7 mA		
Output Resistance		200 ohms		
Common Mode Range		±10 V min.		
Common Mode Rejection, ± 5V		120 dB min.		
Input Impedance		100 megohms		
Input Bias Current		150 pA		
Input Offset Current		50 pA		
Input Offset Voltage		20 μV		
Input Off. Volt. Drift, μV/°C max.	1.0	0.3	0.1	0.6
Long Term Stability		5 μV/year		
Power Supply Rejection		120 dB min.		
Power Requirement		±15 VDC at 5 mA max.		
Package		TO-99		

ORDERING INFORMATION

Model	Oper. Temp. Range	Input Offset Voltage Drift	Price (1-24)
AM-490-2A	0 to 70C	1.0 μV/°C max.	$29.00
AM-490-2B	0 to 70C	0.3 μV/°C max.	34.00
AM-490-2C	0 to 70C	0.1 μV/°C max.	39.00
AM-490-2M	−55 to +125C	0.6 μV/°C max.	95.00
AM-490-CK1	Capacitor Kit for AM-490 Series		4.50

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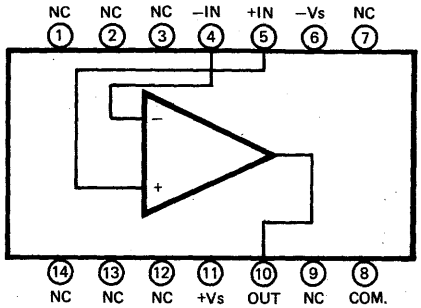
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AM-500

ULTRA-FAST HYBRID OP AMP

DATEL SYSTEMS, INC.





FEATURES

- **200 nsec. Settling to .01%**
- **1000V/μsec. Slew Rate**
- **100 MHz Gain Bandwidth**
- **10^6 Open Loop Gain**
- **50 mA Output Current**

The AM-500 series amplifiers are ultra-fast settling operational amplifiers for use in inverting applications. A unique feedforward amplifier design combines the characteristics of a low drift DC amplifier with those of a very fast AC amplifier. For optimum fast settling performance, this amplifier has an open loop gain roll-off of 6 dB per octave to beyond 100 MHz. Miniature thin-film hybrid construction permits an optimum combination of semiconductor devices and minimum lead lengths to realize the amplifier circuitry. Applications for the AM-500 series include fast integrators, sample-holds, fast waveform drivers, and fast D/A converter output amplifiers.

Output settling time is 200 nanoseconds max. to .01% for a 10 volt step change. Slew rate is 1000V/μsec. for positive output transitions and 1800V/μsec. for negative transitions. This high slew rate permits undistorted reproduction of a full load, 20V peak to peak sine-wave out to 16 MHz. Gain bandwidth product is 100 MHz minimum.

SPECIFICATIONS, Typical at 25°C

	AM-500
DC Open Loop Gain	10^6 V/V
Gain Bandwidth Product	100 MHz
Slew Rate, positive	1000 V/μsec.
Slew Rate, negative	1800 V/μsec.
Settling Time, 10 V to 1.0%	70 nsec.
Settling Time, 10 V to 0.1%	100 nsec.
Settling Time, 10 V to 0.01%	200 nsec. max.
Output	±10 V at 50 mA
Input Impedance	30 Meg.
Input Bias Current, max.	4 nA
Input Offset Current, max.	0.5 nA
Input Offset Voltage, max.	±3 mV
Input Offset Voltage Drift	5 μV/°C max.
Power Requirement	±15 VDC at 22 mA
Package	14 Pin DIP

ORDERING INFORMATION

Model	Oper. Temp. Range	Seal	Price (1-24)
AM-500GC	0 to 70C	Epoxy	$ 79.00
AM-500MC	0 to 70C	Hermetic	89.00
AM-500MR	–25 to +85C	Hermetic	99.00
AM-500MM	–55 to +125C	Hermetic	149.00

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HARRIS
SEMICONDUCTOR
PRODUCTS DIVISION
A DIVISION OF HARRIS CORPORATION

HI-200

Dual SPST CMOS Analog Switch

FEATURES

- ANALOG VOLTAGE RANGE ±15V
- ANALOG CURRENT RANGE 80mA
- TURN-ON TIME 240ns
- LOW R_{ON} 55Ω
- LOW POWER DISSIPATION 15mW
- TTL/CMOS COMPATIBLE
- NO DIGITAL INPUT CURRENT SPIKE

APPLICATIONS

- HIGH FREQUENCY ANALOG SWITCHING
- SAMPLE AND HOLD CIRCUITS
- DIGITAL FILTERS
- OP AMP GAIN SWITCHING NETWORKS

DESCRIPTION

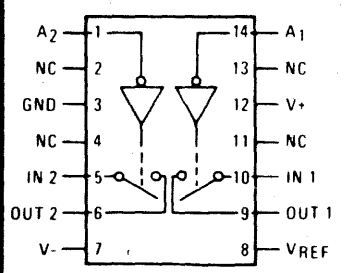
HI-200 is a monolithic device comprising two independently selectable SPST switches which feature fast switching speeds (290ns) combined with low power dissipation (15mW at 25°C). Each switch provides low "ON" resistance operation for input signal voltages up to the supply rails and for signal currents up to 80mA. Employing Dielectric Isolation and Complementary CMOS processing, HI-200 operates without any applications problems induced by latch-up or SCR mode phenomena.

All devices provide break-before-make switching and are TTL and CMOS compatible for maximum application versatility. HI-200 is an ideal component for use in high frequency analog switching. Typical applications include signal path switching, sample and hold circuit, digital filters and op amp gain switching networks.

HI-200 is available in D.I.P. (TO-116) and metal (TO-100) cans. HI-200-2 is specified from -55°C to +125°C while HI-200-5 operates from 0°C to +75°C. HI-200 is functionally and pin compatible with other available "200 series" switches.

PINOUT

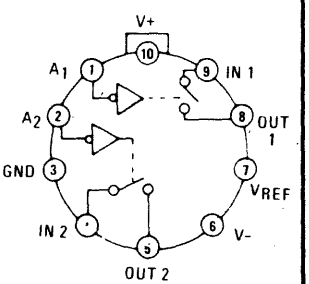
Package Code 4B



TO-116

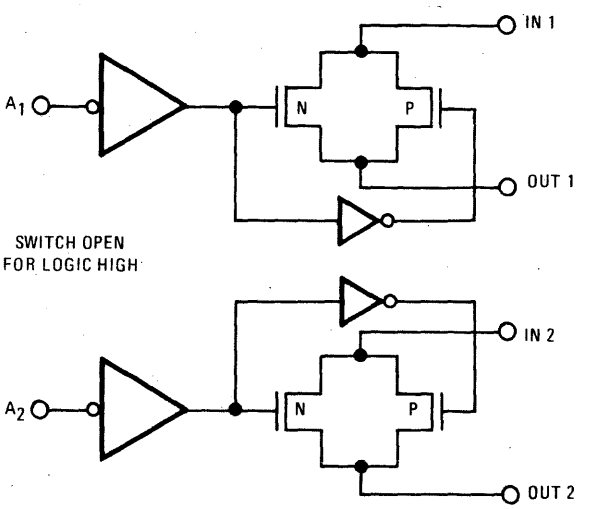
Package Code 2D

Top View



TO-100

FUNCTIONAL DIAGRAM



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow IC Handling Procedures.

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SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Supply Voltage Between Pins 6 and 10	+40V	Total Power Dissipation*	450mW
V_{REF} to Ground	+20V, -5V	Operating Temperature	
Digital Input Voltage:	$+V_{Supply}$ +4V	HI-200-2	-55°C to +125°C
	$-V_{Supply}$ -4V	HI-200-4	-20°C to +85°C
Analog Input Voltage (One Switch)	$+V_{Supply}$ +2.0V	HI-200-5	0°C to +75°C
	$-V_{Supply}$ -2.0V	Storage Temperature	-65°C to +150°C

*Derate 6mW/°C Above T_A = 75°C

ELECTRICAL CHARACTERISTICS

Unless Otherwise Specified
Supplies = +15V, -15V; V_{REF} = Open; V_{AH}(Logic Level High) = 3.0V V_{AL}(Logic Level Low) = +0.8V
For Test Conditions, consult Performance Characteristics

		HI-200-2** -55°C to +125°C			HI-200-5 0°C to +75°C			
PARAMETER	TEMP.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	UNITS
ANALOG SWITCH CHARACTERISTICS								
* V_S, Analog Signal Range	Full	-15		+15	-15		+15	V
* R_{ON}, On Resistance (Note 1)	+25°C		55	70		55	80	Ω
	Full		80	100		72	100	Ω
* $I_{S(OFF)}$, Off Input Leakage Current	+25°C		1			1		nA
	Full		100	500		10	500	nA
* $I_{D(OFF)}$, Off Output Leakage Current	+25°C		1			1		nA
	Full		100	500		10	500	nA
* $I_{D(ON)}$, On Leakage Current	+25°C		.02			.02		nA
	Full		6	500		6	500	nA
DIGITAL INPUT CHARACTERISTICS								
V_{AL}, Input Low Threshold	Full			0.8			0.8	V
V_{AH}, Input High Threshold	Full	3.0			3.0			V
* I_A, Input Leakage Current (High or Low) (Note 2)	Full			1.0			1.0	μA
SWITCHING CHARACTERISTICS								
t_{OPEN}, Break - Before Make Delay (Note 3)	+25°C		60			60		ns
t_{on}, Switch on Time	+25°C		240	500		240		ns
t_{off}, Switch off Time	+25°C		330	500		500		ns
"Off Isolation" (Note 4)	+25°C		70			70		dB
$C_{S(OFF)}$, Input Switch Capacitance	+25°C		5.5			5.5		pF
$C_{D(OFF)}$, Output Switch Capacitance	+25°C		5.5			5.5		pF
$C_{D(ON)}$, Output Switch Capacitance	+25°C		11			11		pF
C_A, Digital Input Capacitance	+25°C		5			5		pF
$C_{DS(OFF)}$, Drain-To-Source Capacitance	+25°C		0.5			0.5		pF
POWER REQUIREMENTS (Note 5)	+25°C		15			15		mW
P_D, Power Dissipation	Full			60			60	mW
* I^+, Current (Pin 10)	+25°C		0.5			0.5		mA
	Full			2.0			2.0	mA
* I^-, Current (Pin 6)	+25°C		0.5			0.5		mA
	Full			2.0			2.0	mA

NOTES:
1. V_{OUT} = ±10V I_{OUT} = 1mA
2. Digital Inputs Are MOS Gates - Typical Leakage is Less Than 1nA
3. V_{AH} = 4.0V
4. V_A = +3V, R_L = 1KΩ, C_L = 10pF, V_S = 3VRMS, f, 100 kHz
5. V_A = +3V or V_A = OV For Both Switches

*100% Tested For Dash 8 At +25°C And +125°C Only

**Note: HI-200-4 has same specifications as HI-200-2 over the reduced temperature range -20°C to +85°C

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HARRIS
SEMICONDUCTOR
PRODUCTS DIVISION
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HI-201

Quad SPST CMOS Analog Switch

FEATURES

- ANALOG VOLTAGE RANGE ±15V
- ANALOG CURRENT RANGE 80mA
- TURN-ON TIME 185ns
- LOW R_{ON} 65Ω
- LOW POWER DISSIPATION 15mW
- TTL/CMOS COMPATIBLE
- NO DIGITAL INPUT CURRENT SPIKE

APPLICATIONS

- HIGH FREQUENCY ANALOG SWITCHING
- SAMPLE AND HOLD CIRCUITS
- DIGITAL FILTERS
- OP AMP GAIN SWITCHING NETWORKS

DESCRIPTION

HI-201 is a monolithic device comprising four independently selectable SPST switches which feature fast switching speeds (185ns) combined with low power dissipation (15mW at 25°C). Each switch provides low "ON" resistance operation for input signal voltages up to the supply rails and for signal currents up to 80mA. Employing Dielectric Isolation and Complementary CMOS processing, HI-201 operates without any applications problems induced by latch-up or SCR-mode phenomena.

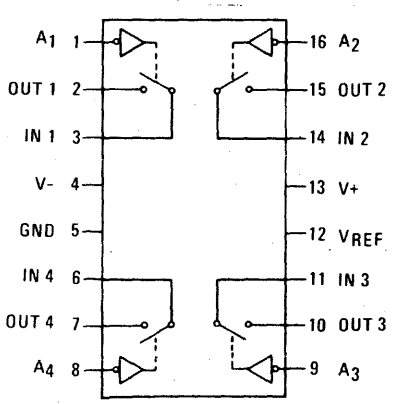
All devices provide break-before-make switching and are TTL and CMOS compatible for maximum application versatility. HI-201 is an ideal component for use in high frequency analog switching. Typical appliations include signal path switching, sample and hold circuit, digital filters and op amp gain switching networks.

HI-201 is available in a 16 lead dual-in-line package. HI-201-2 is specified from -55°C to +125°C while HI-201-5 operates from 0°C to +75°C. HI-201 is functionally and pin compatible with other available "200 series" switches.

PIN OUT

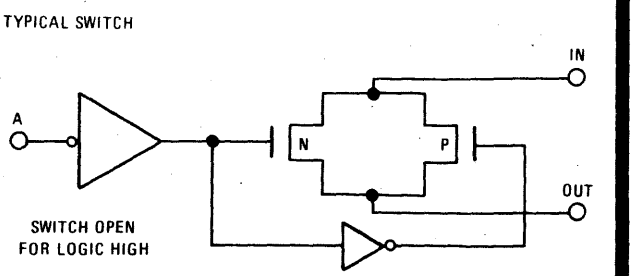
Package Code 4B

Top View



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow IC Handling Procedures.

FUNCTIONAL DIAGRAM



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SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Supply Voltage Between Pins 4 and 13	+40V	Total Power Dissipation*	750mW
V_{REF} to Ground	+20V, -5V	Operating Temperature	
Digital Input Voltage:	V_{Supply}(+) +4V	HI-201-2	-55°C to +125°C
	V_{Supply}(-) -4V	HI-201-4	-20°C to +85°C
Analog Input Voltage (One Switch)	$+V_{Supply}$ +2.0V	HI-201-5	0°C to +75°C
	$-V_{Supply}$ -2.0V	Storage Temperature	-65°C to +150°C

*Derate 8mW/°C Above T_A = +75°C

ELECTRICAL CHARACTERISTICS

Unless Otherwise Specified
Supplies = +15V, -15V; V_{REF} = Open; V_{AH} (Logic Level High) = 3.0V V_{AL} (Logic Level Low) = +0.8V
For Test Conditions, consult Performance Characteristics

		HI-201-2** -55°C to +125°C			HI-201-5 0°C to +75°C			
PARAMETER	TEMP.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	UNITS
ANALOG SWITCH CHARACTERISTICS								
*V_S, Analog Signal Range	Full	-15		+15	-15		+15	V
*R_{ON}, On Resistance (Note 1)	+25°C		65	80		65	100	Ω
	Full		85	125		75	125	Ω
*$I_{S(OFF)}$, Off Input Leakage Current	+25°C		2			2		nA
	Full			500			250	nA
*$I_{D(OFF)}$, Off Output Leakage Current	+25°C		2			2		nA
	Full			500			250	nA
*$I_{D(ON)}$, On Leakage Current	+25°C		2			2		nA
	Full			500			250	nA
DIGITAL INPUT CHARACTERISTICS								
V_{AL}, Input Low Threshold	Full			0.8			0.8	V
V_{AH}, Input High Threshold	Full	3.0			3.0			V
*I_A, Input Leakage Current (High or Low) (Note 2)	Full			1.0			1.0	μA
SWITCHING CHARACTERISTICS								
t_{OPEN}, Break - Before Make Delay (Note 3)	+25°C		30			30		ns
t_{on}, Switch ON Time	+25°C		185	500		185		ns
t_{off}, Switch OFF Time	+25°C		220	500		220		ns
"Off Isolation" (Note 4)	+25°C		80			80		dB
$C_{S(OFF)}$, Input Switch Capacitance	+25°C		5.5			5.5		pF
$C_{D(OFF)}$, Output Switch Capacitance	+25°C		5.5			5.5		pF
$C_{D(ON)}$, Output Switch Capacitance	+25°C		11			11		pF
C_A, Digital Input Capacitance	+25°C		5			5		pF
$C_{DS(OFF)}$, Drain-To-Source Capacitance	+25°C		0.5			0.5		pF
POWER REQUIREMENTS (Note 5)	+25°C		15			15		mW
P_D, Power Dissipation	Full			60			60	mW
*I+, Current (Pin 13)	+25°C		0.5			0.5		mA
	Full			2.0			2.0	mA
*I- Current (Pin 4)	+25°C		0.5			0.5		mA
	Full			2.0			2.0	mA

NOTES:
1. V_{OUT} = ±10V I_{OUT} = 1mA
2. Digital Inputs Are MOS Gates - Typical Leakage is Less Than 1nA
3. V_{AH} = 4.0V
4. V_A = 5V, R_L = 1KΩ, C_L = 10pF, V_S = 3VRMS, f = 100KHz
5. V_A = +3V or V_A = 0V For all Switches

* 100% Tested for Dash 8. ("Full" Tested at +25°C to +125°C)
** Note: HI-201-4 has same specifications as HI-201-2 over the reduced temperature range -20°C to +85°C

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HARRIS
SEMICONDUCTOR
PRODUCTS DIVISION
A DIVISION OF HARRIS CORPORATION

HI-5040 thru HI-5051
HI-5046A and HI-5047A

CMOS Analog Switches

FEATURES

- WIDE ANALOG SIGNAL RANGE ±15V
- LOW "ON" RESISTANCE (TYP) 25Ω
- HIGH CURRENT CAPABILITY (TYP) 80mA
- BREAK-BEFORE-MAKE SWITCHING
  - TURN-ON TIME (TYP) 370ns
  - TURN-OFF TIME (TYP) 280ns
- NO LATCH-UP
- INPUT MOS GATES ARE PROTECTED FROM ELECTROSTATIS DISCHARGE
- DTL, TTL, CMOS, PMOS COMPATIBLE

APPLICATIONS

- HIGH FREQUENCY SWITCHING
- SAMPLE AND HOLD
- DIGITAL FILTERS
- OP AMP GAIN SWITCHING

DESCRIPTION

This family of CMOS analog switches offers low-resistance switching performance for analog voltages up to the supply rails and for signal currents up to 80mA. "ON" resistance is low and stays reasonably constant over the full range of operating signal voltage and current. R_{ON} remains exceptionally constant for input voltages between +5V and -5V and currents up to 50mA. Switch impedance also changes very little over temperature, particularly between 0°C and +75°C. R_{ON} is nominally 25 ohms for HI-5048 through HI-5051 and HI-5046A/5047A and 50Ω for HI-5040 through HI-5047.

All devices provide break-before-make switching and are TTL and CMOS compatible for maximum application versatility. Performance is further enhanced by Dielectric Isolation processing which insures latch-free operation with very low input and output leakage currents (0.8nA at 25°C). This family of switches also features very low power operation (1.5mW at 25°C).

There are 14 devices in this switch series which are differentiated by type of switch action and value of R_{ON} (see Functional diagram). All devices are available in 16 pin D.I.P. packages. The HI-5040/5050 switches can directly replace IH-5040 series devices and are functionally compatible with the DG 180/190 family. Each switch type is available in the -55°C to +125°C and 0°C to +75°C performance grades.

FUNCTIONAL DESCRIPTION

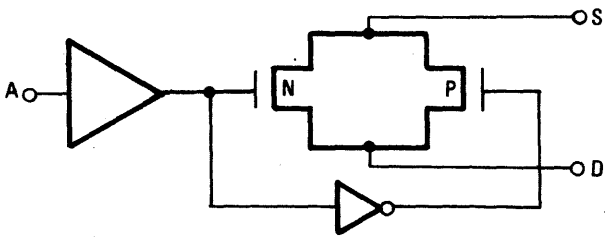
Package Code 4B

PART NUMBER	TYPE	RON
HI-5040	SPST	75Ω
HI-5041	DUAL SPST	75Ω
HI-5042	SPDT	75Ω
HI-5043	DUAL SPDT	75Ω
HI-5044	DPST	75Ω
HI-5045	DUAL DPST	75Ω
HI-5046	DPDT	75Ω
HI-5046A	DPDT	30Ω
HI-5047	4PST	75Ω
HI-5047A	4PST	30Ω
HI-5048	DUAL SPST	30Ω
HI-5049	DUAL DPST	30Ω
HI-5050	SPDT	30Ω
HI-5051	DUAL SPDT	30Ω

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow IC Handling Procedures.

FUNCTIONAL DIAGRAM

TYPICAL SWITCH



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SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Supply Voltage ($V^+ - V^-$)	36V	Analog Current (S to D)	80mA
V_R to Ground	V^+, V^-	Total Power Dissipation*	450mW
Digital and Analog	V^+ +4V	Operating Temperature	
Input Voltage	V^- -4V	HI-50XX-2	-55°C to +125°C
		HI-50XX-5	0°C to +75°C
		Storage Temperature	-65°C to +150°C

*Derate 6mW/°C above T_A = 75°C

ELECTRICAL CHARACTERISTICS

Unless Otherwise Specified
Supplies = +15V, -15V; V_R = 0V; V_{AH} (Logic Level High) = 3.0V; V_{AL} (Logic Level Low) = +0.8V, V_L = +5V
For Test Conditions, consult Performance Characteristics

PARAMETER	TEMP	-55°C to +125°C MIN	-55°C to +125°C TYP	-55°C to +125°C MAX	0°C to +75°C MIN	0°C to +75°C TYP	0°C to +75°C MAX	UNITS
ANALOG SWITCH CHARACTERISTICS								
* Analog Signal Range	Full	-15		+15	-15		+15	V
* Ron, "ON" Resistance (Note 1a)	+25°C		50			50		Ω
	Full			75			75	Ω
* Ron, "ON" Resistance (Note 1b)	+25°C		25			25		Ω
	Full			50			50	Ω
Ron, Channel-to-Channel Match (Note 1a)	+25°C		2	10		2	10	Ω
Ron, Channel-to-Channel Match (Note 1b)	+25°C		1	5		1	5	Ω
* $I_{S(OFF)} = I_{D(OFF)}$, Off Input or Output	+25°C		0.8			0.8		nA
Leakage Current	Full		100	500		100	500	nA
* $I_{D(ON)}$, On Leakage Current	+25°C		0.01			0.01		nA
	Full		2	500		2	500	nA
DIGITAL INPUT CHARACTERISTICS								
V_{AL}, Input Low Threshold	Full			0.8			0.8	V
V_{AH}, Input High Threshold	Full	3.0			3.0			V
* I_A, Input Leakage Current (High or Low)	Full		.01	1.0		.01	1.0	μA
SWITCHING CHARACTERISTICS								
t_{on}, Switch "ON" Time	+25°C		370	1000		370		ns
t_{off}, Switch "OFF" Time	+25°C		280	500		280		ns
Charge Injection (Note 2)	+25°C		5	20		5		mV
"OFF Isolation" (Note 3)	+25°C	75	80			80		dB
"Crosstalk" (Note 3)	+25°C	80	88			88		dB
$C_{S(OFF)}$, Input Switch Capacitance	+25°C		11			11		pF
$C_{D(OFF)}$, Output Switch Capacitance	+25°C		11			11		pF
$C_{D(ON)}$, Output Switch Capacitance	+25°C		22			22		pF
C_A, Digital Input Capacitance	+25°C		5			5		pF
$C_{DS(OFF)}$, Drain-To-Source Capacitance	+25°C		0.5			0.5		pF
POWER REQUIREMENTS								
P_D, Quiescent Power Dissipation	+25°C		1.5			1.5		mW
* I^+, +15V Quiescent Current	Full			0.3			0.5	mA
* I^-, -15V Quiescent Current	Full			0.3			0.5	mA
* I_L, +5V Quiescent Current	Full			0.3			0.5	mA
* I_R, Gnd Quiescent Current	Full			0.3			0.5	mA

NOTES: 1. $V_{OUT} = \pm 10V$, I_{OUT} = 1mA
a) For HI-5040 thru HI-5047
b) For HI-5048 thru HI-5051, HI-5046A/5047A
2. V_{IN} = 0V, C_L = 10,000pF
3. $R_L = 100\Omega$, f= 100 KHz, V_{IN} = 2 V_{PP}, C_L = 5pF

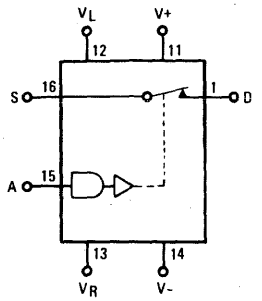
*100% Tested for Dash 8. ("Full" Tested at +25°C to +125°C)

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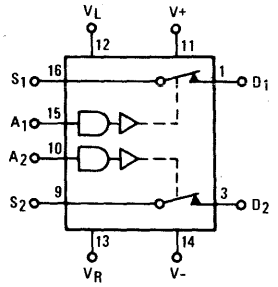
SWITCH FUNCTIONS

SWITCH STATES ARE FOR LOGIC "1" INPUT

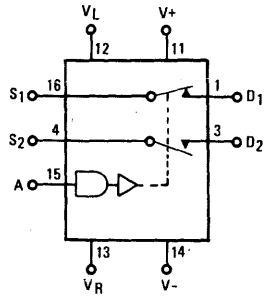
SPST
HI-5040 (75Ω)



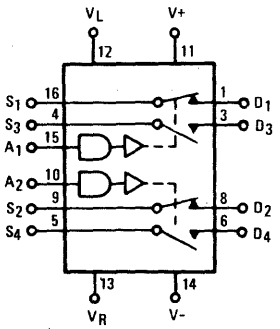
DUAL SPST
HI-5041 (75Ω)



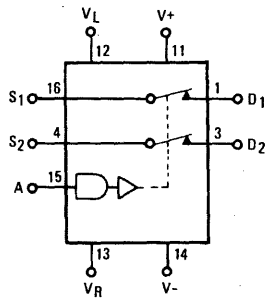
SPST
HI-5042 (75Ω)



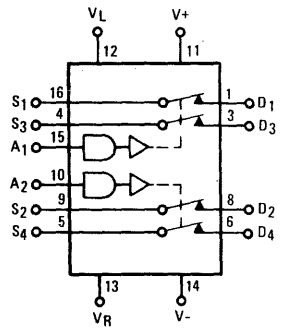
DUAL SPST
HI-5043 (75Ω)



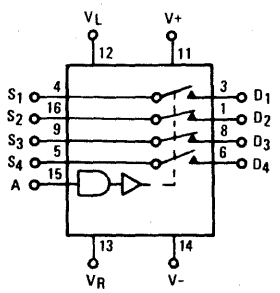
DPST
HI-5044 (75Ω)



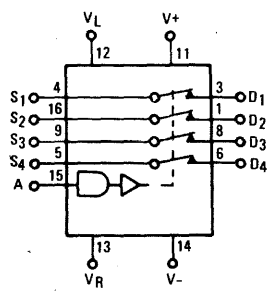
DUAL DPST
HI-5045 (75Ω)



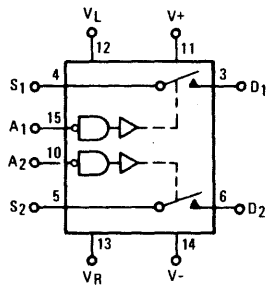
DPDT
HI-5046 (75Ω)
HI-5046A (30Ω)



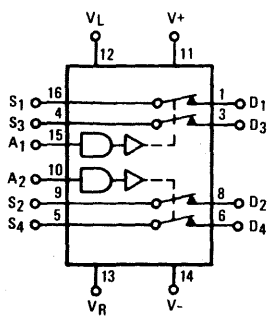
4PST
HI-5047 (75Ω)
HI-5047A (30Ω)



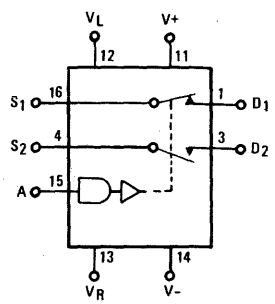
DUAL SPST
HI-5048 (30Ω)



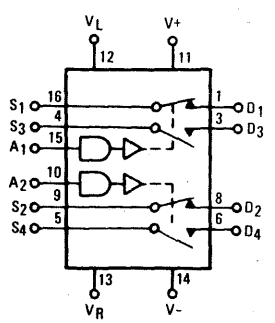
DUAL DPST
HI-5049 (30Ω)



SPST
HI-5050 (30Ω)



DUAL SPST
HI-5051 (30Ω)



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HI-1818A/1828A

Low Resistance 8 Channel CMOS Analog Multiplexers

FEATURES

- SIGNAL RANGE ±15V
- "ON" RESISTANCE (TYP.) 250Ω
- INPUT LEAKAGE AT +125°C (TYP.) 20nA
- ACCESS TIME (TYP.) 350ns
- POWER CONSUMPTION (TYP.) 5mW
- DTL/TTL COMPATIBLE ADDRESS
- -55°C to +125°C OPERATION

APPLICATIONS

- DATA ACQUISITION SYSTEMS
- PRECISION INSTRUMENTATION
- DEMULTIPLEXING
- SELECTOR SWITCH

DESCRIPTION

The HI-1818A/1828A are monolithic high performance CMOS analog multiplexers offering built-in channel selection decoding plus an inhibit (enable) input for disabling all channels. Dielectric Isolation (DI) processing is used for enhanced reliability and performance (see Application Note 521). Substrate leakage and parasitic capacitance are much lower, resulting in extremely low static errors and high throughput rates. Low output leakage (typically 0.1nA) and low channel ON resistance (250 Ω) assure optimum performance in low level or current mode applications.

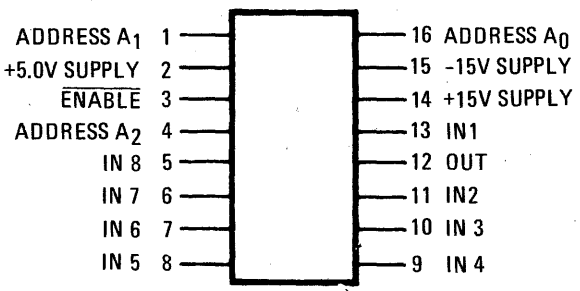
The 1818A is a single-ended 8 channel multiplexer, while the HI-1828A is a differential 8 channel version. Either device is ideally suited for medical instrumentation, telemetry systems, and microprocessor based data acquisition systems.

The HI-1818A-2 and HI-1828A are specified over -55°C to +125°C, while the -5 versions are specified over 0°C to +75°C.

PINOUT

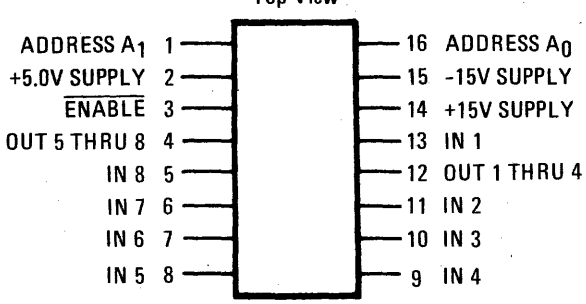
HI-1818A

Top View — Package Code 4B



HI-1828A

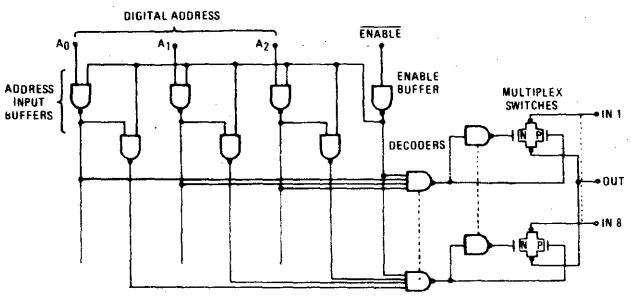
Top View — Package Code 4B



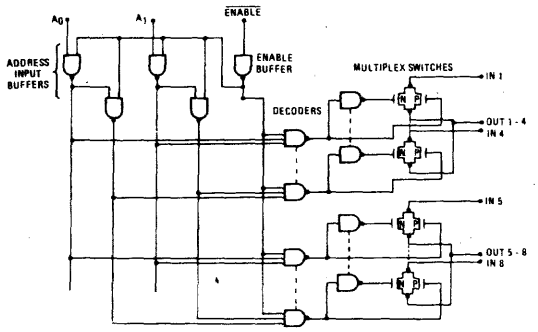
CAUTION: These devices are sensitive to electrostatic discharge. Users should follow IC Handling Procedures.

FUNCTIONAL DIAGRAM

HI-1818A



HI-1828A



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SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS (NOTE 1)

Supply Voltage Between Pins 14 and 15	40.0V	Digital Input Voltage	V-Supply to V+ Supply
Logic Supply Voltage, Pin 2	30.0V	Total Power Dissipation (Note 2)	780mW
Analog Input Voltage: V^+_{Supply}	+2V	Storage Temperature Range	-65°C to +150°C
V^-_{Supply}	-2V		

ELECTRICAL CHARACTERISTICS

Supplies = +15V, -15V, +5V

PARAMETER	TEMP.	HI-1818A-2/1828A-2 -55°C to +125°C MIN.	TYP.	MAX.	HI-1818A-5/1828A-5 0°C to +75°C MIN.	TYP.	MAX.	UNITS
ANALOG CHANNEL CHARACTERISTICS								
* V_{IN}, Analog Signal Range	Full	-15		+15	-15		+15	V
* R_{ON}, ON Resistance (Note 3)	+25°C		250	400		250	400	Ω
	Full		300	500		300	500	Ω
* I_S(OFF), Input Leakage Current	Full		20	50		20	50	nA
* I_D(ON), On Channel Leakage Current								
(HI-1818A)	Full		100	250		100	250	nA
(HI-1828A)	Full		50	125		50	125	nA
* I_D(OFF) Output Leakage Current								
(HI-1818A)	Full		100	250		100	250	nA
(HI-1828A)	Full		50	125		50	125	nA
DIGITAL INPUT CHARACTERISTICS								
V_{IL}, Input Low Threshold	Full			0.4			0.4	V
V_{IH}, Input High Threshold (Note 4)	Full	4.0			4.0			V
* I_{IN}, Input Leakage Current	Full		.01	1		.01	1	μA
SWITCHING CHARACTERISTICS								
T_S, Access Time (Note 5)	+25°C		350			350		ns
Break-Before-Make Delay	+25°C		100			100		ns
Settling Time (0.1%)	+25°C		1.08			1.08		μs
(0.025%)	+25°C		2.8			2.8		μs
C_{IN}, Channel Input Capacitance	+25°C		4			4		pF
C_{OUT}, Channel Output Capacitance								
(HI-1818A)	+25°C		20			20		pF
(HI-1828A)	+25°C		10			10		pF
C_{DS}(OFF), Drain-To-Source Capacitance	+25°C		0.6			0.6		pF
C_D, Digital Input Capacitance	+25°C		5			5		pF
POWER REQUIREMENTS								
P_D, Power Dissipation	Full		5			5		mW
P_{DS}, Standby Power (Note 6)	Full		5			5		mW
* I_+, Current Pin 14	Full		0.1	0.5		0.1	1	mA
* I_-, Current Pin 15	Full		0.3	1		0.3	2	mA
* I_L, Current Pin 2	Full		0.3	1		0.3	2	mA

NOTES:
1. Voltage ratings apply when voltages at all other pins are within their normal operating ranges.
2. Derate 9.25 mW/°C above 75°C.
3. $V_{OUT} = \pm 10V$ $I_{OUT} = -1mA$.
4. To drive from DTL/TTL circuits, 1K pull-up resistors to + 5.0V supply are recommended.
5. Time measured to 90% of final output level; $V_{OUT} = -5.0V$ to +5.0V, Digital Inputs = 0V to + 4.0V.
6. Voltage at Pin 3, $\overline{ENABLE}$ = + 4.0V.

*100% Tested for Dash 8. ("Full" Tested at +25°C to +125°C)

TRUTH TABLES

HI-1818A

ADDRESS A_2	A_1	A_0	$\overline{EN}$	"ON" CHANNEL
L	L	L	L	1
L	L	H	L	2
L	H	L	L	3
L	H	H	L	4
H	L	L	L	5
H	L	H	L	6
H	H	L	L	7
H	H	H	L	8
X	X	X	H	NONE

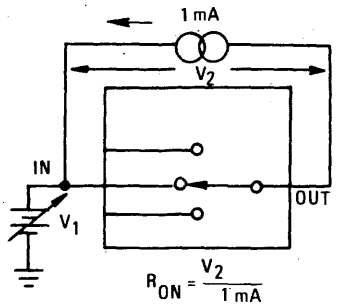
HI-1828A

ADDRESS A_1	A_0	$\overline{EN}$	"ON" CHANNELS
L	L	L	1 and 5
L	H	L	2 and 6
H	L	L	3 and 7
H	H	L	4 and 8
X	X	H	NONE

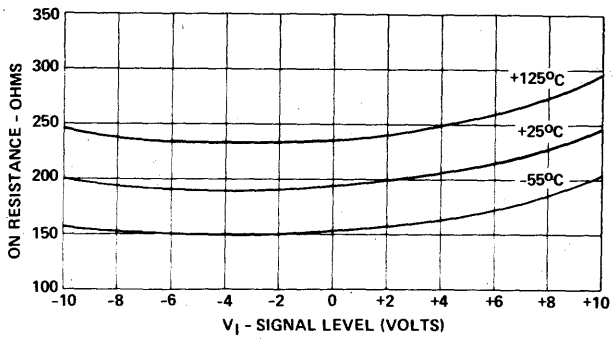
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PERFORMANCE CHARACTERISTICS

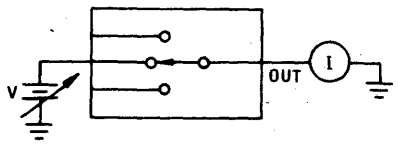
ON RESISTANCE vs ANALOG SIGNAL LEVEL



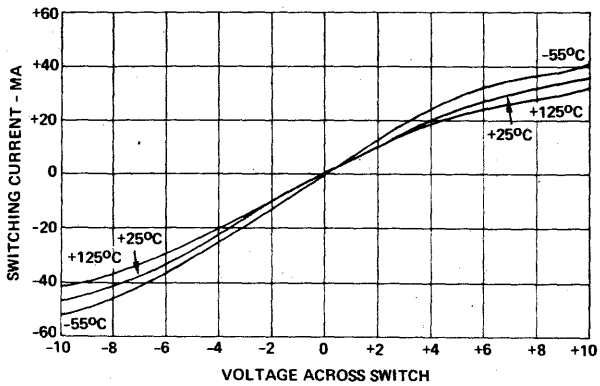
Test Circuit



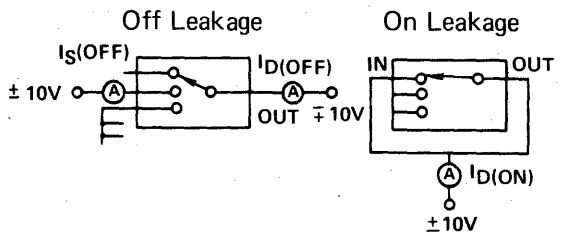
ON CHANNEL CURRENT vs VOLTAGE

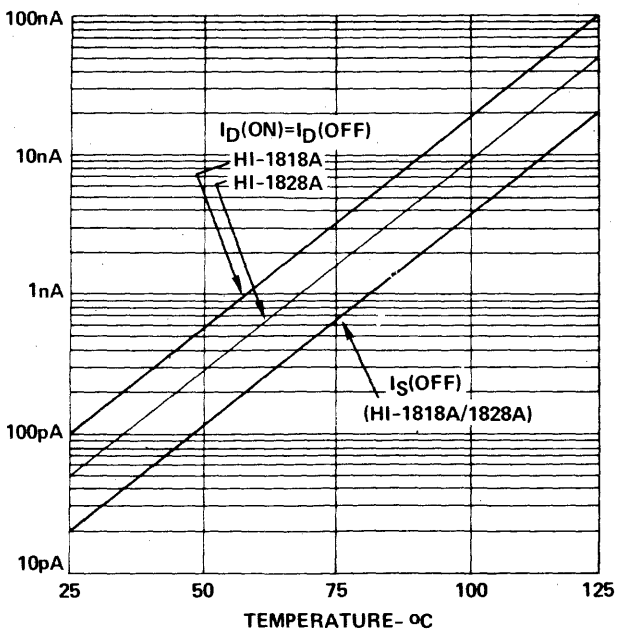


Test Circuit

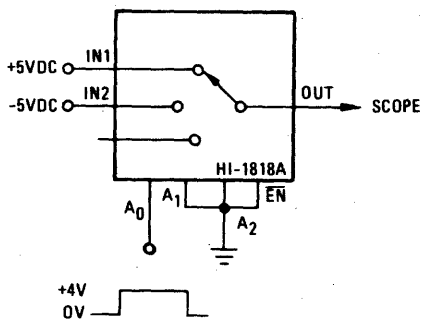


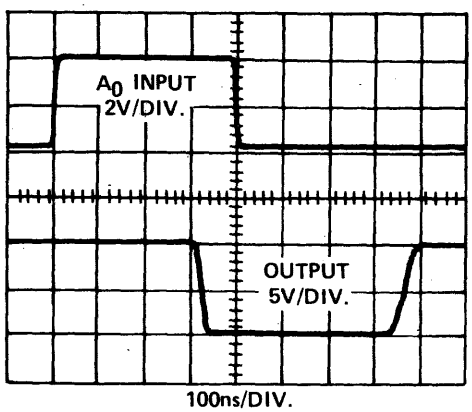
ON/OFF LEAKAGE CURRENTS vs TEMPERATURE





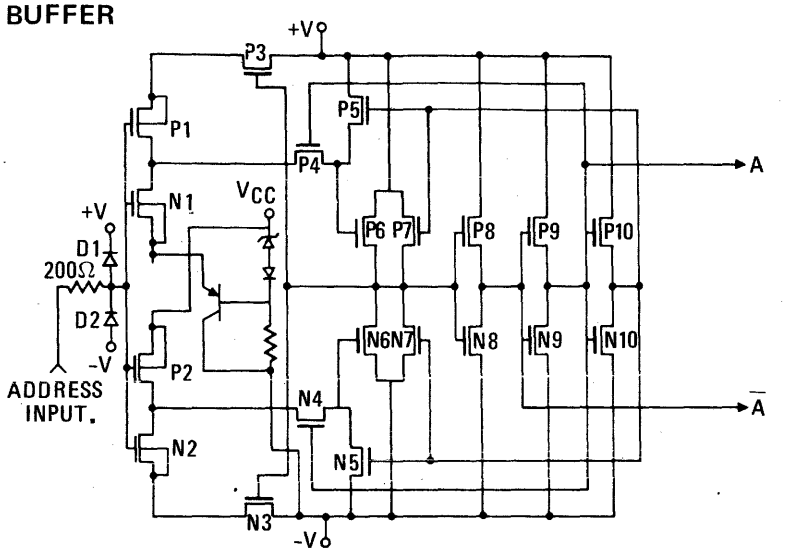
ACCESS TIME





SCHEMATIC DIAGRAM

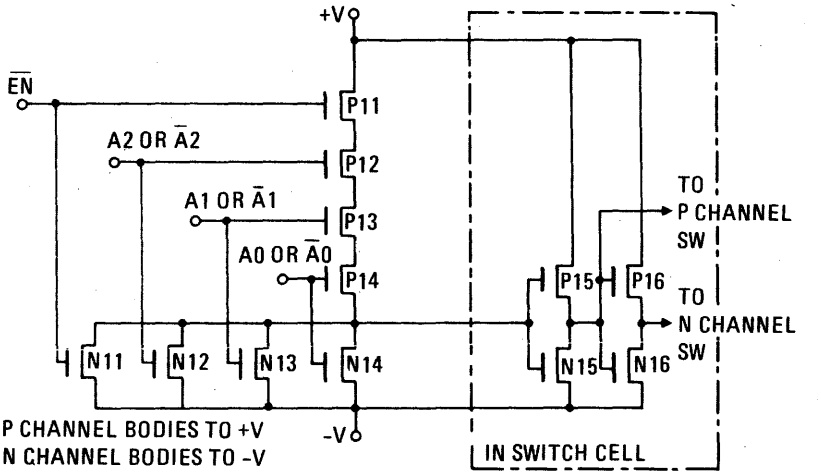
ADDRESS INPUT BUFFER



ALL N-CHANNEL BODIES TO V-

ALL P-CHANNEL BODIES TO V+ UNLESS OTHERWISE INDICATED.

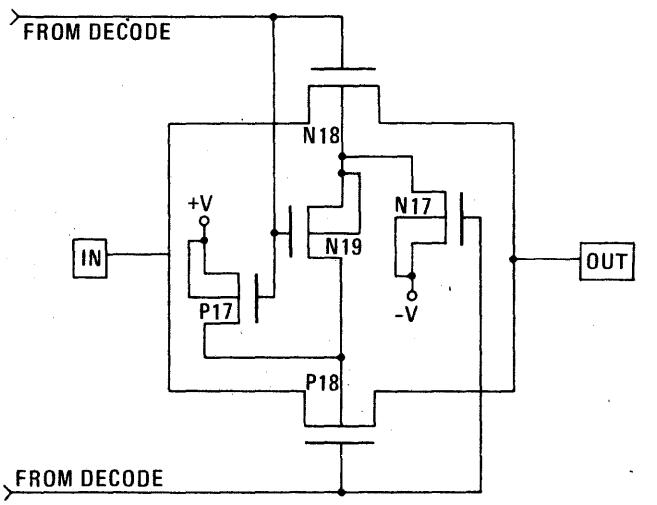
DECODER GATE



P CHANNEL BODIES TO +V
N CHANNEL BODIES TO -V

A2 OR Ā2 NOT USED FOR HI-1828A

MULTIPLEX SWITCH



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HI-1840

16 Channel CMOS Analog Multiplexer with High-Z Analog Input Protection

FEATURES

- HIGH ANALOG INPUT IMPEDANCE DURING POWER LOSS (OPEN) 500MΩ
- LOW POWER CONSUMPTION (STANDBY) 600μW
- ACCESS TIME 500ns
- EXCELLENT IN HI-REL REDUNDANT SYSTEMS
- BREAK-BEFORE-MAKE SWITCHING
- NO LATCH-UP

APPLICATIONS

- FAIL-SAFE DATA ACQUISITION SYSTEMS
- FAIL-SAFE TELEMETRY SYSTEMS
- AIRCRAFT INSTRUMENTATION AND CONTROL

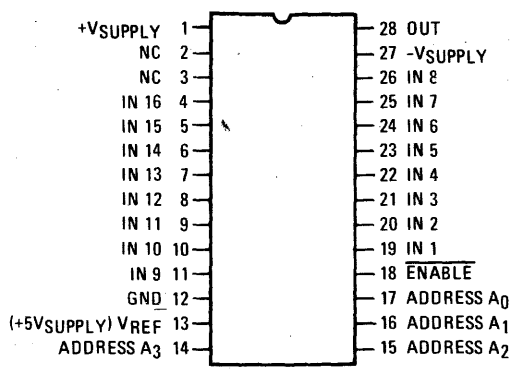
DESCRIPTION

The HI-1840 is a monolithic 16 channel multiplexer constructed with the Harris Linear Dielectric Isolation CMOS process. It is designed to provide a high input impedance to the analog source if device power fails (open) or the analog signal voltage inadvertently exceeds the supply rails during powered operation. Excellent for use in redundant applications, since the secondary device can be operated in a standby unpowered mode affording no additional power drain. But more significantly, a very high impedance exists between the active and inactive devices preventing any interaction. One of sixteen channel selection is controlled by a 4-bit binary address plus an Enable-Inhibit input which conveniently controls the ON/OFF operation of several multiplexers in a system. All digital inputs have electrostatic discharge protection. The HI-1840 is tested and guaranteed within the military temperature range and is available in a 28 pin dual-in-line package.

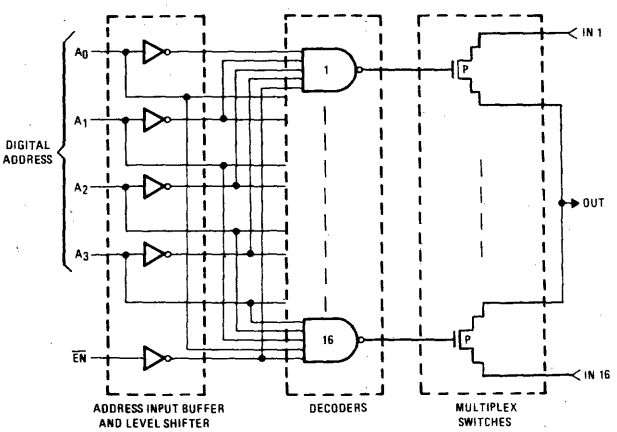
PINOUT

Package Code 1M

Top View



FUNCTIONAL DIAGRAM



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow IC Handling Procedures.

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SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Supply Voltage Between Pins 1 and 27 +40V
V_{REF} to Ground +20V.
V_{EN}, V_A, Digital Input Overvoltage:
V_A V_{Supply} (+) +4V
V_{Supply} (-) -4V
Analog Input Overvoltage:
V_S V_{Supply} (+) +10V
V_{Supply} (-) -10V

Total Power Dissipation* 1200mW
Operating Temperature:
HI-1840-2 -55°C to +125°C
Storage Temperature -65°C to +150°C

*Derate 8mW/°C above T_A = +25°C

ELECTRICAL CHARACTERISTICS

Unless Otherwise Specified:
Supplies = +15V, -15V: V_{REF}(Pin 13) = +5V; V_{AH}(Logic Level High) = 4.0V; V_{AL}(Logic Level Low) = +0.8V
For Test Conditions, consult Performance Characteristics section.

PARAMETER	TEMP.	-55°C to +125°C MIN.	TYP.	MAX.	UNITS
ANALOG CHANNEL CHARACTERISTICS					
*V_S, Analog Signal Range	Full	-5		+15	V
*R_{ON}, On Resistance (Note 1) V_{IN} = +15V	Full		0.5	1.0	KΩ
V_{IN} = -5V	Full		2.5	5.0	KΩ
*I_S(OFF), Off Input Leakage Current	+25°C		0.03		nA
	Full			±100	nA
*I_S(OFF), with Power Off (Note 8)	Full			±100	nA
*I_D(OFF), Off Output Leakage Current	+25°C		1.0		nA
	Full			±1000	nA
* I_D(OFF), or I_S(OFF) with Input Overvoltage Applied (Note 2)	+25°C		50		nA
	Full			±1000	nA
*I_D(ON), On Channel Leakage Current	+25°C		1.0		nA
	Full			±1000	nA
DIGITAL INPUT CHARACTERISTICS					
V_{AL}, Input Low Threshold | TTL Drive	Full			0.8	V
V_{AH}, Input High Threshold | (Note 7)	Full	4.0			V
V_{AL} | MOS Drive (Note 3)	+25°C			0.8	V
V_{AH} |	+25°C	6.0			V
*I_A, Input Leakage Current (High or Low)	Full			1.0	µA
SWITCHING CHARACTERISTICS					
t_A, Access Time	+25°C		500	1000	ns
t_{OPEN}, Break-Before-Make Delay	+25°C	20	80		ns
t_{ON}(EN), Enable Delay (ON)	+25°C		300	1000	ns
t_{OFF}(EN), Enable Delay (OFF)	+25°C		300	1000	ns
Settling Time (0.1%)	+25°C		1.2		µs
(0.025%)	+25°C		4.1		µs
"Off Isolation" (Note 4)	+25°C		65		dB
C_S(OFF), Channel Input Capacitance	+25°C		5		pF
C_D(OFF), Channel Output Capacitance :	+25°C		50		pF
C_A, Digital Input Capacitance	+25°C		5		pF
C_{DS}(OFF), Input ot Output Capacitance	+25°C		0.15		pF
POWER REQUIREMENTS					
P_D, Power Dissipation (Note 5)	+25°C		0.6	15.0	mW
(Note 6)	+25°C		0.6	15.0	mW
*I+, Current Pin 1 (Note 5)	Full		0.02	0.5	mA
*I-, Current Pin 27 (Note 5)	Full		0.02	0.5	mA
*I+, Standby (Note 6)	Full		0.02	0.5	mA
*I-, Standby (Note 6)	Full		0.02	0.5	mA

TRUTH TABLE

A_3	A_2	A_1	A_0	$\overline{EN}$	"ON" CHANNEL
X	X	X	X	H	NONE
L	L	L	L	L	1
L	L	L	H	L	2
L	L	H	L	L	3
L	L	H	H	L	4
L	H	L	L	L	5
L	H	L	H	L	6
L	H	H	L	L	7
L	H	H	H	L	8
H	L	L	L	L	9
H	L	L	H	L	10
H	L	H	L	L	11
H	L	H	H	L	12
H	H	L	L	L	13
H	H	L	H	L	14
H	H	H	L	L	15
H	H	H	H	L	16

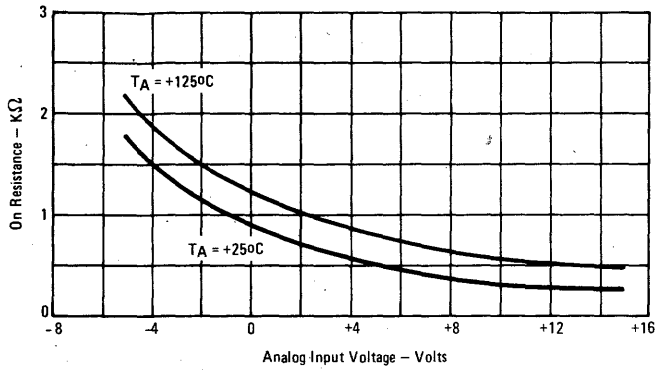
NOTES:
1. I_{OUT} = 1mA
2. Analog Overvoltage = ±20V
3. V_{REF} = +10V
4. V_{EN} = 4.0V, R_L = 1K, C_L = 7pF, V_S = 3VRMS, f = 500kHz
5. V_{EN} = 0.8V
6. V_{EN} = 4.0V
7. To drive from DTL/TTL circuits 1K pull-up to +5.0V supply are recommended.
8. All supplies (V+, V-, +5V) and digital inputs (A_0, A_1, A_2, A_3, EN) opened. Analog input ±10V.

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PERFORMANCE CHARACTERISTICS AND TEST CIRCUITS

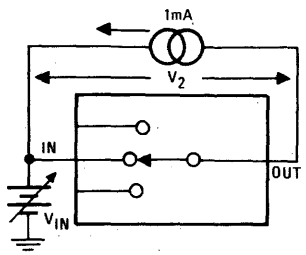
Unless Otherwise Specified: $T_A = 25^oC$, $V_{SUPPLY} = \pm 15V$, $V_{AH} = +4V$, $V_{AL} = 0.8V$ and $V_{REF} = 5V$.

ON RESISTANCE VS. ANALOG INPUT VOLTAGE

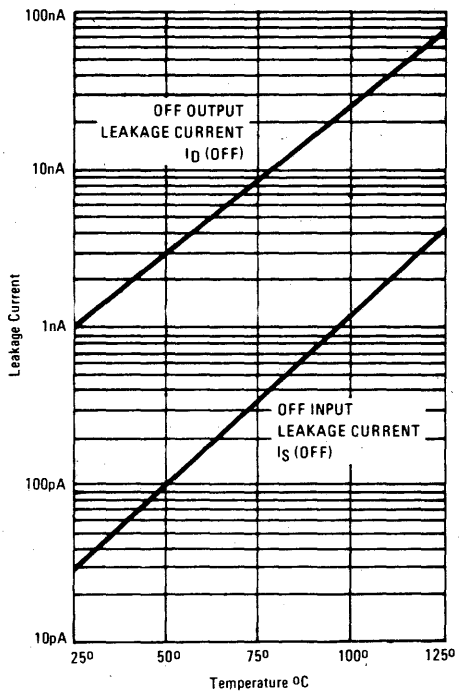


ON RESISTANCE vs. INPUT SIGNAL LEVEL

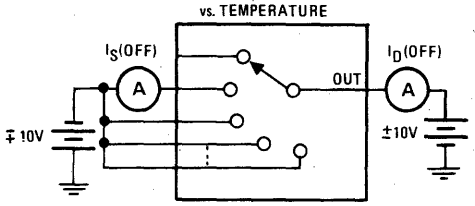
$R_{ON} = \frac{V_2}{1mA}$



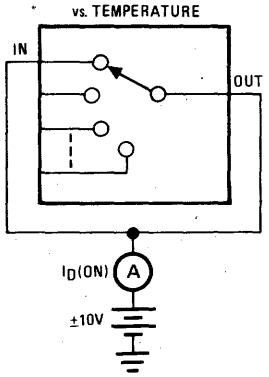
LEAKAGE CURRENT VS. TEMPERATURE



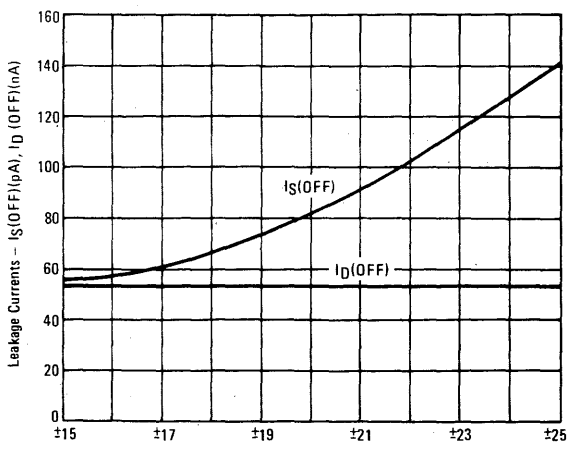
OFF LEAKAGE CURRENT vs. TEMPERATURE



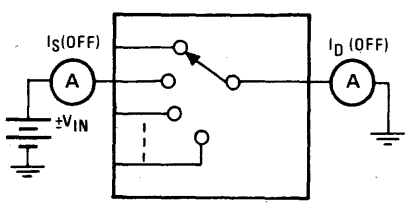
ON LEAKAGE CURRENT vs. TEMPERATURE



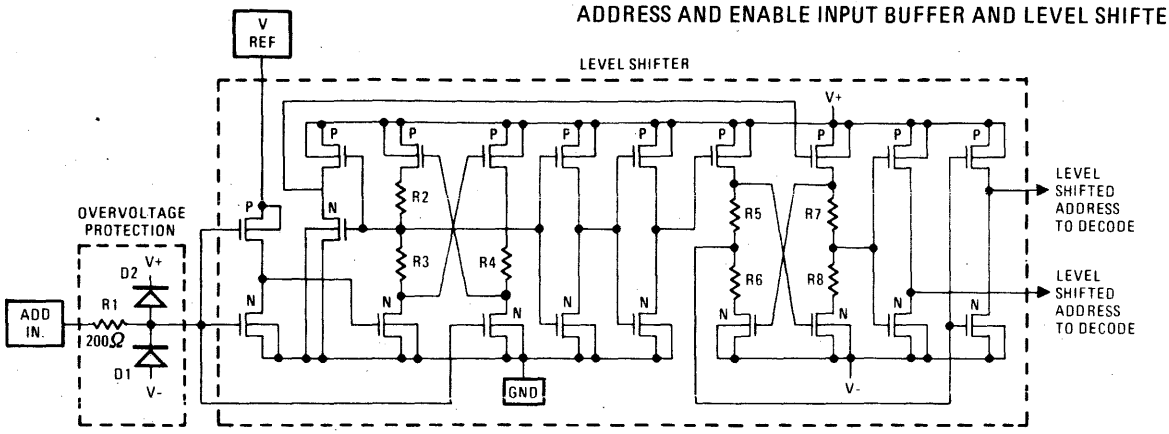
ANALOG INPUT OVERVOLTAGE CHARACTERISTICS



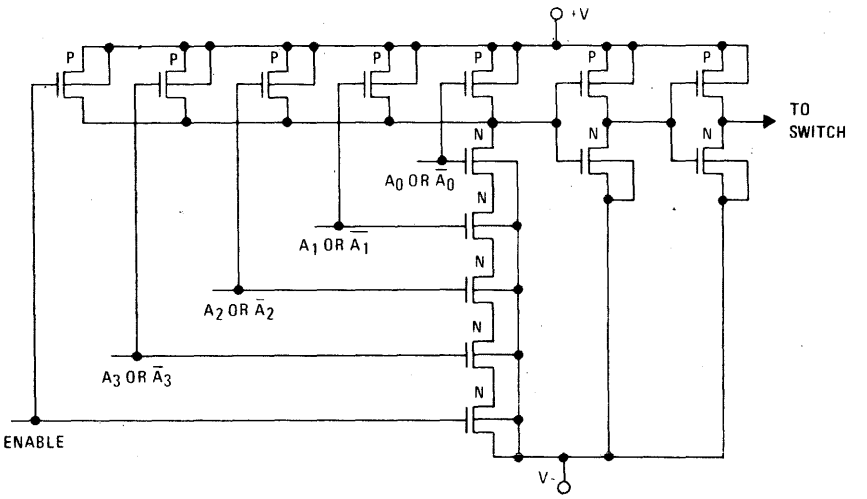
ANALOG INPUT OVERVOLTAGE CHARACTERISTICS



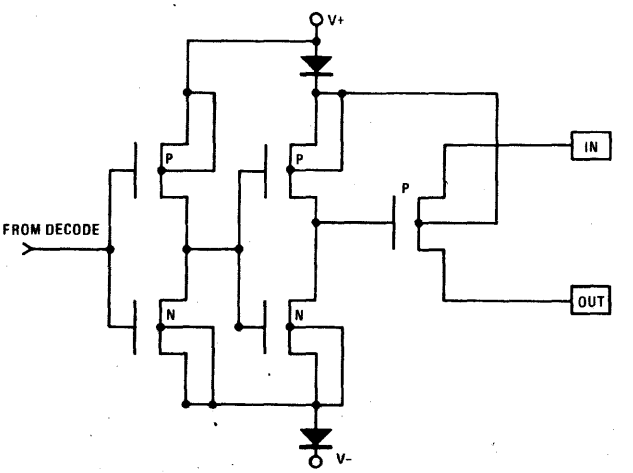
ADDRESS AND ENABLE INPUT BUFFER AND LEVEL SHIFTER



ADDRESS DECODER



MULTIPLEX SWITCH



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A DIVISION OF HARRIS CORPORATION

HI-506A/HI-507A

16 Channel CMOS Analog Multiplexer with Overvoltage Protection

FEATURES

- ANALOG/DIGITAL OVERVOLTAGE PROTECTION
- FAIL SAFE WITH POWER LOSS (NO LATCHUP)
- BREAK-BEFORE-MAKE SWITCHING
- DTL/TTL AND CMOS COMPATIBLE
- ANALOG SIGNAL RANGE ±15V
- ACCESS TIME (TYP.) 500ns
- SUPPLY CURRENT AT 1MHz ADDRESS TOGGLE (TYP.) 4mA
- STANDBY POWER (TYP.) 7.5mW

APPLICATIONS

- DATA ACQUISITION
- INDUSTRIAL CONTROLS
- TELEMETRY

DESCRIPTION

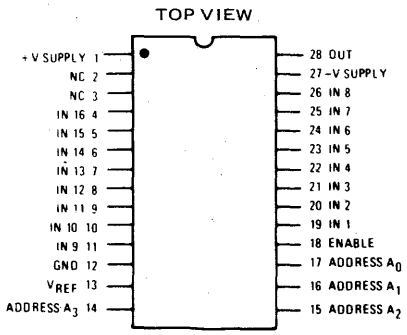
The HI-506A and HI-507A are dielectrically isolated CMOS analog multiplexers incorporating an important feature; they withstand analog input voltages much greater than the supplies. This is essential in any system where the analog inputs originate outside the equipment. They can withstand a continuous input up to 10 volts greater than either supply, which eliminates the possibility of damage when supplies are off, but input signals are present. Equally important they can withstand brief input transient spikes of several hundred volts; which otherwise would require complex external protection networks. Necessarily, ON resistance is somewhat higher than similar unprotected devices, but very low leakage currents combine to produce low errors. Application Notes 520 and 521 further explain these features.

The HI-506A-2 and HI-507A-2 are specified over -55°C to +125°C while the -5 versions are specified over 0°C to +75°C.

PINOUT

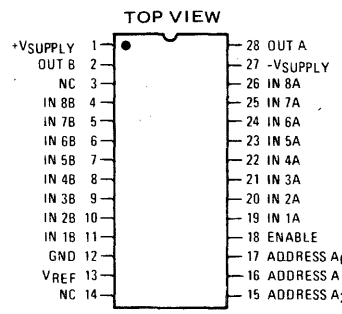
HI-506A **Package Code 1M**

TOP VIEW



HI-507A **Package Code 1M**

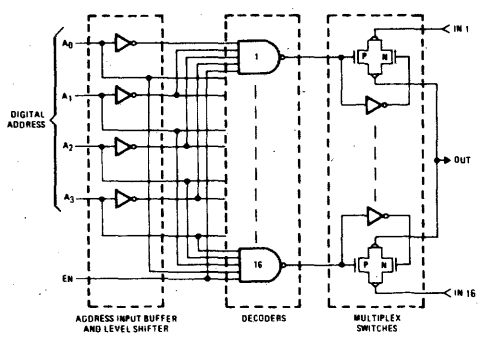
TOP VIEW



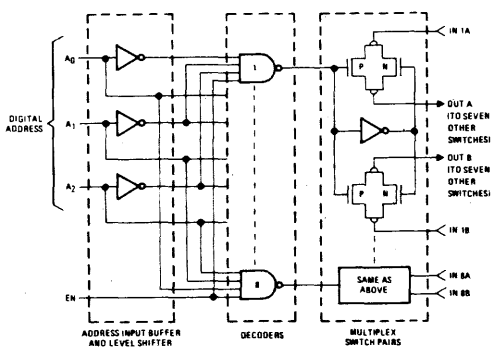
CAUTION: These devices are sensitive to electrostatic discharge. Users should follow IC Handling Procedures.

FUNCTIONAL DIAGRAM

HI-506A



HI-507A



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SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Supply Voltage Between Pins 1 and 27	40V	Total Power Dissipation*	1200mW
V_{REF} to Ground V+ to Ground	+20V	Operating Temperature	
V_{EN}, V_A, Digital Input Overvoltage:		HI-506A/507A-2	-55°C to +125°C
V_A (V_{Supply} (+))	+4V	HI-506A/507A-5	0°C to +75°C
V_A (V_{Supply} (−))	-4V	Storage Temperature	-65°C to +150°C
Analog Overvoltage:			
V_S (V_{Supply} (+))	+20V		
V_S (V_{Supply} (−))	-20V	*Derate 8mW/°C above T_A = +25°C	

ELECTRICAL CHARACTERISTICS (Unless Otherwise Specified)

Supplies = +15V, -15V; V_{REF} (Pin 13) = Open; V_{AH} (Logic Level High) = +4.0V; V_{AL} (Logic Level Low) = +0.8V
For Test Conditions, consult Performance Characterisitcs section.

PARAMETER		TEMP.	HI-506A/507A-2 -55°C to +125°C MIN.	TYP.	MAX.	HI-506A/507A-5 0°C to +75°C MIN.	TYP.	MAX.	UNITS
ANALOG CHANNEL CHARACTERISTICS									
*V_S, Analog Signal Range		Full	-15		+15	-15		+15	V
*R_{ON}, On Resistance (Note 1)		+25°C		1.2	1.5		1.5	1.8	KΩ
		Full		1.5	2.0		1.8	2.0	KΩ
*I_S (OFF), Off Input Leakage Current		+25°C		0.03			0.03		nA
		Full			±50			±50	nA
*I_D (OFF), Off Output Leakage Current		+25°C		1.0			1.0		nA
	HI-506A	Full			±500			±500	nA
	HI-507A	Full			±250			±250	nA
*I_D (OFF) with Input Overvoltage Applied (Note 2)		+25°C		4.0			4.0		nA
		Full			2.0				μA
*I_D (ON), On Channel Leakage Current		+25°C		0.1			0.1		nA
	HI-506A	Full			±500			±500	nA
	HI-507A	Full			±250			±250	nA
DIGITAL INPUT CHARACTERISTICS									
V_{AL}, Input Low Threshold | TTL Drive		Full			0.8			0.8	V
V_{AH}, Input High Threshold | (Note 7)		Full	4.0			4.0			V
V_{AL} | MOS Drive (Note 3)		+25°C			0.8			0.8	V
V_{AH} |		+25°C	6.0			6.0			V
*I_A, Input Leakage Current (High or Low)		Full			1.0			5.0	μA
SWITCHING CHARACTERISTICS									
t_A, Access Time		+25°C		0.5	1.0		0.5		μs
t_{OPEN}, Break-Before Make Delay		+25°C		80			80		ns
t_{ON} (EN), Enable Delay (ON)		+25°C		300			300		ns
t_{OFF} (EN), Enable Delay (OFF)		+25°C		300			300		ns
Settling Time (0.1%)		+25°C		1.3			1.3		μs
(0.025%)		+25°C		4.4			4.4		μs
"Off Isolation" (Note 4)		+25°C		65			65		dB
C_S (OFF), Channel Input Capacitance		+25°C		5			5		pF
C_D (OFF), Channel Output Capacitance	HI-506A	+25°C		50			50		pF
	HI-507A	+25°C		25			25		pF
C_A, Digital Input Capacitance		+25°C		5			5		pF
C_{DS} (OFF), Input to Output Capacitance		+25°C		0.1			0.1		pF
POWER REQUIREMENTS									
P_D, Power Dissipation		Full		7.5			7.5		mW
*I+, Current Pin 1 (Note 5)		Full		0.5	2.0		0.5	5.0	mA
*I-, Current Pin 27 (Note 5)		Full		0.02	1.0		0.02	2.0	mA
*I+, Standby (Note 6)		Full		0.5	2.0		0.5	5.0	mA
*I-, Standby (Note 6)		Full		0.02	1.0		0.02	2.0	mA

NOTES:
1. V_{OUT} = ±10V, I_{OUT} = -100 μA.
2. Analog Overvoltage = ±33V.
3. V_{REF} = +10V.
4. V_{EN} = 0.8V, R_L = 1K, C_L = 7pF, V_S = 3VRMS, f = 500KHz.
5. V_{EN} = +4.0V.
6. V_{EN} = 0.8V.
7. To drive from DTL/TTL circuits, 1KΩ pull-up resistors to +5.0V supply are recommended.

*100% Tested for Dash 8.
("Full" Tested at +25°C to +125°C)

TRUTH TABLES

HI-506A

A_3	A_2	A_1	A_0	EN	"ON" CHANNEL
X	X	X	X	L	NONE
L	L	L	L	H	1
L	L	L	H	H	2
L	L	H	L	H	3
L	L	H	H	H	4
L	H	L	L	H	5
L	H	L	H	H	6
L	H	H	L	H	7
L	H	H	H	H	8
H	L	L	L	H	9
H	L	L	H	H	10
H	L	H	L	H	11
H	L	H	H	H	12
H	H	L	L	H	13
H	H	L	H	H	14
H	H	H	L	H	15
H	H	H	H	H	16

HI-507A

A_2	A_1	A_0	EN	ON SWITCH PAIR
X	X	X	L	NONE
L	L	L	H	1
L	L	H	H	2
L	H	L	H	3
L	H	H	H	4
H	L	L	H	5
H	L	H	H	6
H	H	L	H	7
H	H	H	H	8

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HI-508A/509A

8 Channel CMOS Analog Multiplexers with Overvoltage Protection

FEATURES

- ANALOG/DIGITAL OVERVOLTAGE PROTECTION
- FAIL SAFE WITH POWER LOSS (NO LATCHUP)
- BREAK-BEFORE-MAKE SWITCHING
- DTL/TTL AND CMOS COMPATIBLE
- ANALOG SIGNAL RANGE ±15V
- ACCESS TIME (TYP.) 500ns
- SUPPLY CURRENT AT 1MHz ADDRESS TOGGLE (TYP.) 4mA
- STANDBY POWER (TYP.) 7.5mW

APPLICATIONS

- DATA ACQUISITION
- INDUSTRIAL CONTROLS
- TELEMETRY

DESCRIPTION

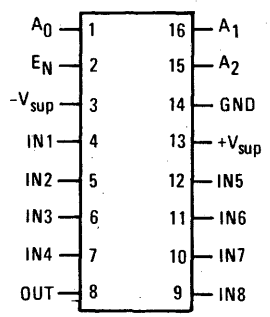
The HI-508A and HI-509A are dielectrically isolated CMOS analog multiplexers incorporating an important feature; they withstand analog input voltages much greater than the supplies. This is essential in any system where the analog inputs originate outside the equipment. They can withstand a continuous input up to 10 volts greater than either supply, which eliminates the possibility of damage when supplies are off, but input signals are present. Equally important, they can withstand brief input transient spikes of several hundred volts; which otherwise would require complex external protection networks. Necessarily, ON resistance is somewhat higher than similar unprotected devices, but very low leakage currents combine to produce low errors. Application Notes 520 and 521 further explain these features.

The HI-508A-2 and HI-509A-2 are specified over -55°C to +125°C while the -5 versions are specified over 0°C to +75°C.

PINOUT

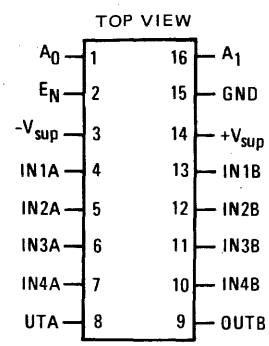
HI-508A — **Package Code 4B**

TOP VIEW



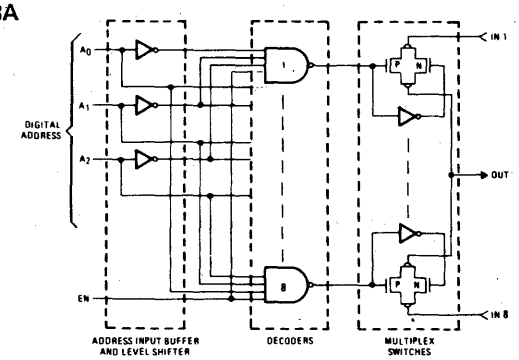
HI-509A — **Package Code 4B**

TOP VIEW

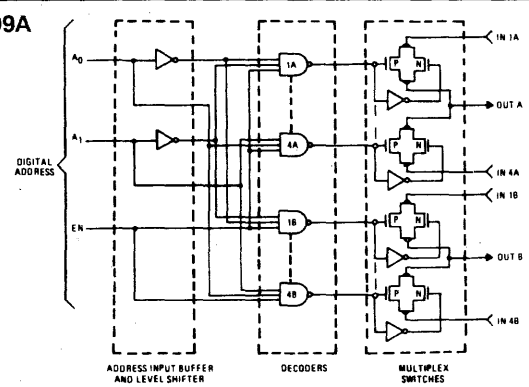


FUNCTIONAL DIAGRAM

HI-508A



HI-509A



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow IC Handling Procedures.

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SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Voltage between Supply Pins 40V

V+ to Ground 20V

V_{EN}, V_A, Digital Input Overvoltage:

V_A { V_{Supply} (+) +4V; V_{Supply} (-) -4V

Analog Input Overvoltage:

V_S { V_{Supply} (+) +20V; V_{Supply} (-) -20V

Total Power Dissipation* 725 mW

Operating Temperature:

HI-508A/HI-509A-2 -55°C to +125°C

HI-508A/HI-509A-5 0°C to +75°C

Storage Temperature -65°C to +150°C

*Derate 8mW/°C above t_A = 75°C

ELECTRICAL CHARACTERISTICS (Unless Otherwise Specified)

Supplies = +15V, -15V; V_{AH} (Logic Level High) = +4.0V; V_{AL} (Logic Level Low) = +0.8V
For Test Conditions, consult Performance Characterisitcs section.

PARAMETER	TEMP.	HI-508A/509A-2 -55°C to +125°C MIN.	TYP.	MAX.	HI-508A/509A-5 0°C to +75°C MIN.	TYP	MAX.	UNITS
ANALOG CHANNEL CHARACTERISTICS								
*V_S, Analog Signal Range	Full	-15		+15	-15		+15	V
* R_{ON}, On Resistance (Note 1)	+25°C		1.2	1.5		1.5	1.8	KΩ
	Full		1.5	1.8		1.8	2.0	KΩ
* $I_{S(OFF)}$, Off Input Leakage Current	+25°C		0.03			0.03		nA
	Full			±50			±50	nA
* $I_{D(OFF)}$, Off Output Leakage Current	+25°C		1.0			1.0		nA
HI-508A	Full			±250			±250	nA
* $I_{D(OFF)}$ with Input Overvoltage Applied (Note 2)	+25°C		4.0			4.0		nA
	Full			2.0				μA
* $I_{D(ON)}$, On Channel Leakage Current	+25°C		0.1			0.1		nA
HI-508A	Full			±250			±250	nA
DIGITAL INPUT CHARACTERISTICS								
V_{AL}, Input Low Threshold (Note 6)	Full			0.8			0.8	V
V_{AH}, Input High Threshold (Note 6)	Full	4.0			4.0			V
* I_A, Input Leakage Current (High or Low)	Full			1.0			1.0	μA
SWITCHING CHARACTERISTICS								
t_A, Access Time	+25°C		0.5	1.0		0.5		μs
t_{OPEN}, Break - Before Make Delay	+25°C		80			80		ns
$t_{ON(EN)}$, Enable Delay (ON)	+25°C		300			300		ns
$t_{OFF(EN)}$, Enable Delay (OFF)	+25°C		300			300		ns
Settling Time (0.1%)	+25°C		1.2			1.2		μs
(0.025%)	+25°C		3.5			3.5		μs
"OFF Isolation" (Note 3)	+25°C		65			65		dB
$C_{S(OFF)}$, Channel Input Capacitance	+25°C		5			5		pF
$C_{D(OFF)}$, Channel Output Capacitance								
HI-508A	+25°C		25			25		pF
HI-509A	+25°C		12			12		pF
C_A, Digital Input Capacitance	+25°C		5			5		pF
$C_{DS(OFF)}$, Input to Output Capacitance	+25°C		0.1			0.1		pF
POWER REQUIREMENTS								
P_D, Power Dissipation	Full		7.5			7.5		mW
*I+, Current (Note 4)	Full		0.5	2.0		0.5	5.0	mA
*I-, Current (Note 4)	Full		0.02	1.0		0.02	2.0	mA
*I+, Standby (Note 5)	Full		0.5	2.0		0.5	5.0	mA
*I-, Standby (Note 5)	Full		0.02	1.0		0.02	2.0	mA

NOTES:
1. V_{OUT} = ±10V, I_{OUT} = -100μA
2. Analog Overvoltage = ±33V
3. V_{EN} = 0.8V, R_L = 1K, C_L = 7pF, V_S = 3V RMS, f = 500KHz
4. V_{EN} = +4.0V
5. V_{EN} = 0.8V
6. To drive from DTL/TTL Circuits, 1KΩ pull-up resistors to +5.0V supply are recommended

*100% Tested for Dash 8. ("Full" Tested at +25°C to +125°C)

TRUTH TABLES

HI-508A

A_2	A_1	A_0	E_N	"ON" CHANNEL
X	X	X	L	NONE
L	L	L	H	1
L	L	H	H	2
L	H	L	H	3
L	H	H	H	4
H	L	L	H	5
H	L	H	H	6
H	H	L	H	7
H	H	H	H	8

HI-509A

A_1	A_0	EN	ON SWITCH PAIR
X	X	L	NONE
L	L	H	1
L	H	H	2
H	L	H	3
H	H	H	4

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HI-1080/1085

Precision Monolithic 8-Bit D to A Converter

FEATURES

- GUARANTEED ±1 L.S.B. ACCURACY OVER TEMPERATURE
  - HI-1080 -55°C to +125°C
  - HI-1085 0°C to +75°C
- FAST SETTLING 1.5 μs to ½ L.S.B.
- EXPANDABLE FOR HIGHER RESOLUTIONS
- MONOLITHIC CONSTRUCTION
- DTL/TTL COMPATIBLE INPUTS
- RELIABLE MONOLITHIC CONSTRUCTION MEETS REQUIREMENTS OF MIL-STD-883

APPLICATIONS

- WAVEFORM SYNTHESIZERS
- MICROPROCESSOR I/O INTERFACE
- HIGH REL APPLICATIONS
- A TO D CONVERTER (USING COMPARATOR AND DIGITAL LOGIC)
- DATA ACQUISITION SYSTEMS

DESCRIPTION

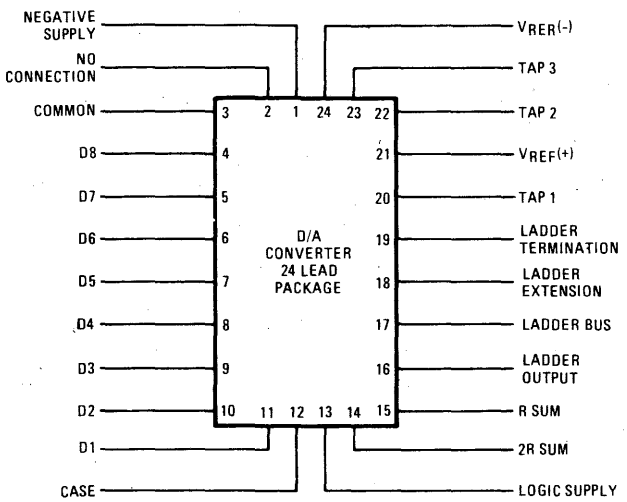
The HI-1080/1085 is a monolithic 8 bit digital-to-analog converter employing bipolar current switches feeding a thin film R-2R ladder network.

Because of the excellent stability of this device, it is practical to specify one all-inclusive accuracy parameter: ±1L.S.B. accuracy over the operating temperature range. This means that once the desired full scale output level is set at room temperature by adjustment of the input reference current, each of the 256 output levels will always measure within ±1 L.S.B. of the corresponding output of a "perfect" DAC. Thus the accuracy specification includes the worst case effects of all of the normally published errors such as non-linearity, zero drift, full scale drift, etc.

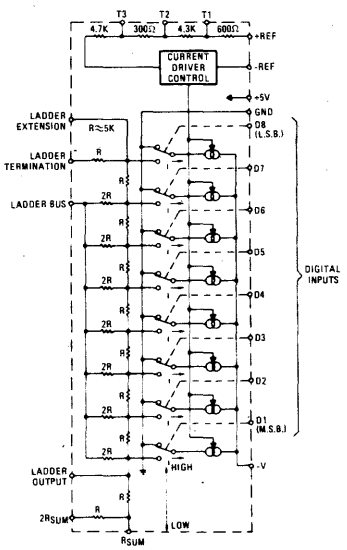
The device is exceptionally versatile, since it may be used in a voltage or current output mode, and may be offset to produce bipolar operation. Matched auxillary resistors are provided for amplifier feedback or current summing. Provisions are also made for scale factor adjustment and for cascading of additional D/A converters for extended resolution.

PINOUT

Top View — Package Code 4K



FUNCTIONAL DIAGRAM



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SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Maximum Ratings are limiting values above which permanent circuit damage may occur.

Voltage
- V+ +8.0V
- V- -18.0V

Digital Inputs: +5.5V

Ladder Common: +8.0V

I_{REF}: 1.6mA

Storage Temperature: $-65^{o}C \leq TA \leq +150^{o}C$

Power Dissipation: 450mW *

*Derate at 4mW/°C above 85°C ambient.

ELECTRICAL CHARACTERISTICS

Unless otherwise stated all measurements taken at V+ = +5V, V- = -15V
V_{REF} = +5V, V_{in}High = +2.4V, V_{in}Low = +0.4V
Unipolar, zero reference connection (Figure 3)

	TEMP	HI-1080 MIN	HI-1080 TYP	HI-1080 MAX	TEMP	HI-1085 MIN	HI-1085 TYP	HI-1085 MAX	UNITS
Resolution		8				8			Bits
Accuracy (Calibrated at 25°C) (Note 1)	+25°C		1/4	1/2					
	-55°C to +125°C		1/2	1	0°C to +75°C		1/2	1	L.S.B.
$V_{Full\ Scale}$ (Note 2) (Uncalibrated)	+25°C	-4.5	-4.98	-5.5	+25°C	-4.5	-4.98	-5.5	Volts
Power Supply Rejection (Note 3)	-55°C to +125°C	.05	.001		0°C to +75°C	.05	.001		L.S.B. per Volt
Settling Time (Note 4)	+25°C		1.5	3.0	+25°C		1.5		μs
Digital Inputs:									
High Threshold				2.0				2.0	Volts
Low Threshold (Note 5)		0.8				0.8			Volts
I_{in}High			.01	1	0°C to +75°C		.01	1	mA
I_{in} Low (Note 6)	-55°C to +125°C		-0.7	-1.0			-0.7	-1.0	mA
Supply Current:									
I+	-55°C to +125°C		8	10	0°C to +75°C		8	10	mA
I-			8	10			8	10	mA
I_{REF} (Note 7)			0.5	0.6			0.5	0.6	mA

NOTES: Test Conditions -

1. Any Input Combination
2. Inputs all low
3. $\Delta V_{OUT}/\Delta V_{SUPPLY}$
   V+ = +5 ± 0.5V
   V- = -15 ± 3V
4. To ±0.2% of full scale after full scale input step
   $R_L > 10M$
   $C_L < 5pF$
5. V+ = 4.5V
6. V_{in} = 2.4 Volts
   V+ = 5.5V
   V_{in} = 0.4 Volts
   V+ = 5.5V
7. V+ = +5.0V
   V- = -15.0V
   V_{REF} = +5.0V
   Inputs all low

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HARRIS
SEMICONDUCTOR
PRODUCTS DIVISION
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PRELIMINARY HI-562

12 Bit High Speed Monolithic Digital-to-Analog Converter

FEATURES

- MONOLITHIC CONSTRUCTION
- EXTREMELY FAST SETTLING — 200ns TO 0.01% (TYP.)
- LOW GAIN DRIFT — ±2ppm/°C (MAX.)
- EXCELLENT LINEARITY OVER TEMPERATURE — ±1/2 LSB (MAX.)
- DESIGNED FOR MINIMUM GLITCHES
- MONOTONIC OVER TEMPERATURE

APPLICATIONS

- CRT DISPLAY GENERATION
- HIGH SPEED A/D CONVERTERS
- VIDEO SIGNAL RECONSTRUCTION
- WAVEFORM SYNTHESIZERS
- HIGH SPEED DATA ACQUISITION
- HIGH-REL APPLICATIONS
- PRECISION INSTRUMENTS

DESCRIPTION

The Harris HI-562 is the first monolithic digital-to-analog converter to combine both ultra-high speed performance and true 12-bit accuracy on the same chip. The HI-562's fast output current settling of 200ns to 0.01% is achieved using dielectric isolation processing to reduce internal parasitics for fast rise and fall times during switching. Output glitches are minimized in the HI-562 by incorporating equally weighted current sources switched into an R-2R ladder network for symmetrical turn-ON and turn-OFF switching times. This creates within the chip a very uniform and constant thermal distribution for excellent linearity and also completely eliminates thermal transients during switching. High stability thin film resistor processing together with laser trimming provide the HI-562 with guaranteed true 12-bit linearity to within ±1/2 LSB maximum over the -55°C to +125°C temperature range. Beyond that, the HI-562's low offset and gain drift over this temperature range assure that its absolute accuracy when referred to a fixed 10V reference will not deviate more than ±3/2 LSB for unipolar mode operation (±2 LSB for bipolar operation). The input reference can be varied from +2V to +10V for two quadrant multiplying mode operation.

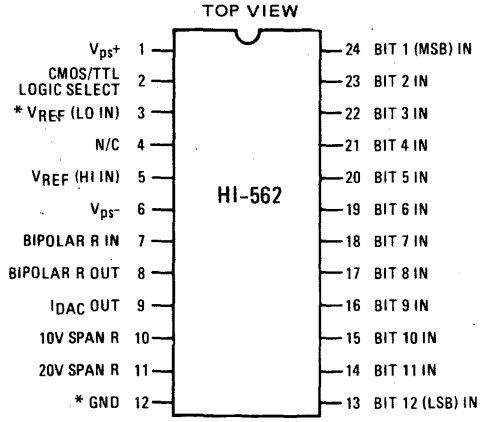
The HI-562 is recommended as a replacement for higher cost hybrid and modular units for increased reliability and accuracy in applications such as CRT displays, precision instruments and data acquisition systems requiring throughput rates as high as 5MHz for full range transitions. Its small size makes it an ideal choice as the heart of high speed A/D converter designs or as a building block in high speed or high resolution industrial process control systems. The HI-562 is also ideally suited for aircraft and space instrumentation where operation over a wide temperature range is required.

The HI-562-5 is specified for operation over 0°C to +70°C, the HI-562-4 over -25°C to +85°C and the HI-562-2 and HI-562-8 over -55°C to +125°C. Processing to MIL-STD-883A Class B screening is available by selecting the HI-562-8. All are available in a hermetically sealed 24-lead dual-in-line package.

PINOUT

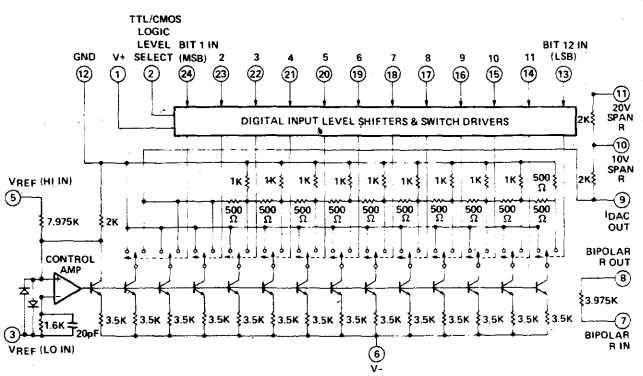
Package Code 1H

TOP VIEW



* Pins 3 and 12 connected to top and bottom case for high frequency shielding.

FUNCTIONAL DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Referred to Ground)[1]

Power Supply Inputs	$V_{PS}+$	+20V
	$V_{PS}-$	-20V
Reference Inputs	V_{REF} (Hi)	$\pm V_{PS}$
	V_{REF} (Lo)	0V
Digital Inputs	Bits 1-12	-1V, +12V
	CMOS/TTL Logic Select	-1V, +12V
Outputs	Pins 7, 8, 10, 11	$\pm V_{PS}$
	Pin 9	$+V_{PS}$, -5V

Power Dissipation Pd, Package	1000mW
Operating Temperature Range	
HI-562-2	-55°C to +125°C
HI-562-4	-25°C to +85°C
HI-562-5	0°C to +70°C
HI-562-8	-55°C to +125°C
Storage Temperature Range	-65°C to +150°C

ELECTRICAL CHARACTERISTICS (@ +25°C, $V_{PS}+$, = +5V, $V_{PS}-$ = -15V, V_{REF} = +10V, pin 2 open circuit unless otherwise noted)

PARAMETER	CONDITIONS	HI-562-2/HI-562-8 MIN	HI-562-2/HI-562-8 TYP	HI-562-2/HI-562-8 MAX	HI-562-4/HI-562-5 MIN	HI-562-4/HI-562-5 TYP	HI-562-4/HI-562-5 MAX	UNITS
INPUT CHARACTERISTICS								
Digital Inputs (3)	Bit ON "Logic 1" Bit OFF "Logic 0"							
TTL Input Voltage (2) Logic "1"	Over full temp. range	2.0			2.0			V
TTL Logic "0"				0.8			0.8	V
TTL Input Current (2) Logic "1"			20	100		20	100	nA
TTL Logic "0"			-50	-100		-50	-100	μA
CMOS Input Voltage Logic "1"	Pin 1 tied to pin 2, $+4.75V \leq V_{PS}+ \leq +12V$ over full temp. range	$0.7V_{PS}+$			$0.7V_{PS}+$			V
CMOS Logic "0"				$0.3V_{PS}+$			$0.3V_{PS}+$	V
CMOS Input Current Logic "1"			20	100		20	100	nA
CMOS Logic "0"			-50	-100		-50	-100	μA
Reference Input Input Resistance	I_{OUT} = 5mA (±20%)		8K			8K		Ω
Input Voltage			+10			+10		V
TRANSFER CHARACTERISTICS								
Resolution	Over full temp. range			12			12	Bits
Nonlinearity (3)	@ +25°C			±1/4		±1/4	±1/2	LSB
	Over full temp. range			±1/2			±1	
Differential Nonlinearity (3)	@ +25°C			±1/4		±1/4	±1/2	LSB
	Over full temp. range			MONOTONICITY GUARANTEED				
Relative Accuracy (6)	With 24.9Ω(1%) Trim Resistors							
Gain Error	All Bits ON			±0.024			±0.024	
Bipolar Offset Error	All Bits OFF			±0.024			±0.024	% FSR (4)
Unipolar Offset Error				±0.012			±0.012	
Adjustment Range	See Operating Instructions							
Gain	With 50Ω Trim		±0.3			±0.3		% FSR
Bipolar Offset	Potentiometers		±0.6			±0.6		
Temperature Stability	Drift specified with internal span resistors for voltage output							
Gain Drift (3)	Over full temp. range			±2			±3	ppm of FSR/°C
Offset Drift (3)								
Unipolar Offset	All Bits OFF			±0.4			±1	
Bipolar Offset				±1			±3	
Differential Nonlinearity	Over full temp. range		±1	±2		±2	±3	
Settling Time (3) to ±1/2 LSB	All Bits ON-to-OFF or OFF-to-ON		200	400		200	400	ns

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PARAMETER	CONDITIONS	HI-562-2/HI-562-8 MIN	HI-562-2/HI-562-8 TYP	HI-562-2/HI-562-8 MAX	HI-562-4/HI-562-5 MIN	HI-562-4/HI-562-5 TYP	HI-562-4/HI-562-5 MAX	UNITS
Major Carry Transient Peak Amplitude Settling Time to 90% Complete	From 011...1 to 100...0 or 100...0 to 011...1		0.7 35			0.7 35		mA ns
Power Supply Sensitivity (3) Unipolar Offset V_{ps}+ @ +5V or +15V V_{ps}- @ -15V	All Bits OFF		 ±0.5 ±0.5			 ±0.5 ±0.5		ppm of FSR/% V_{ps}
Bipolar Offset V_{ps}+ @ 5V or +15V V_{ps}- @ -15V	All Bits OFF, Bipolar mode		 ±1.5 ±1.5			 ±1.5 ±1.5		
Gain V_{ps}+ @ +5V or +15V V_{ps}- @ -15V	All Bits ON		 	 ±1 ±2		 	 ±1 ±2	
OUTPUT CHARACTERISTICS								
Output Current Unipolar Bipolar			 -5.0 ±2.5			 -5.0 ±2.5		mA
Resistance			1000			1000		ohms
Capacitance			20			20		pF
Output Voltage Ranges Unipolar Bipolar	Using external op amp and internal scaling resistors. See Figure 1 and Table 1 for connections		 0 to +5 0 to +10 ±2.5 ±5 ±10			 0 to +5 0 to +10 ±2.5 ±5 ±10		V
Compliance Limit (3)		-3		+10	-3		+10	V
Compliance Voltage (3)	Over full temp. range		±1.0			±1.0		V
Output Noise	0.1 to 10Hz (All Bits ON) 0.1 to 5MHz (All Bits ON)		30 100			30 100		µV (p-p)
MULTIPLYING MODE PERFORMANCE								
Quadrants	Bipolar Mode Reference Input; 2V to +10V		2			2		
Reference Voltage Feedthrough	Unipolar mode, all Bits OFF and +2V to +10V (p-p), 2kHz Sinewave		1			1		LSB (p-p)
Relative Accuracy	Reference Input @ $2V_{DC}$		±0.05			±0.05		% FSR
Output Slew Rate	All Bits ON and +2 to +10V Step change at reference input.		6			6		mA/µs
Settling Time to ±1/2 LSB			3			3		µs
Control Amplifier Bandwidth	Small signal		10			10		MHz
POWER REQUIREMENTS								
V_{ps}+ (7) V_{ps}-	Over full temp. range	4.5 13.5	5 15	15 16.5	4.75 13.5	5 15	15 16.5	V
I_{ps}+ (5) I_{ps}- (5)	All Bits ON or OFF in either TTL or CMOS mode		9 28			9 28		mA
I_{ps}+ (5) I_{ps}- (5)	Same as above except over full temp. range		11 33			11 33		mA

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NOTES

1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied.
2. $V_{ps}+$ tolerance is ±10% for HI-562-2, -8. and ±5% for HI-562-4, -5.
3. See Definitions.
4. FSR is "full scale range" and is 20V for ±10V range, 10V for ±5V range, etc.; or 5mA(±20%) for current output.
5. After 30 seconds warm-up.
6. Using an external op amp with internal span resistors and specified external trim resistors in place of potentiometers R_1 and R_2. Errors are adjustable to zero using R_1 and R_2 potentiometers. (See Operating Instructions Figure 2.)
7. Maximum $V_{ps}+$ is +12V for high level logic only, i.e. when pin 1 is tied to pin 2.

DEFINITIONS OF SPECIFICATIONS

DIGITAL INPUTS

The HI-562 accepts digital input codes in binary format and may be user connected for any one of three binary codes. Straight Binary, Two's Complement, or Offset Binary, (See Operating Instructions).

DIGITAL INPUT	ANALOG OUTPUT		
	Straight Binary	Offset Binary	Two's Complement*
MSB LSB			
000...000	Zero	-FS (Full Scale)	Zero
100...000	½FS	Zero	-FS
111...111	+FS – 1 LSB	+FS – 1 LSB	½FS – 1 LSB
011...111	½FS – 1 LSB	Zero – 1 LSB	+FS – 1 LSB
*Invert MSB with external inverter to obtain Two's Complement Coding			

ACCURACY

NONLINEARITY – Nonlinearity of a D/A converter is an important measure of its accuracy. It describes the deviation from an ideal straight line transfer curve drawn between zero (all bits OFF) and full scale (all bits ON).

DIFFERENTIAL NONLINEARITY – For a D/A converter, it is the difference between the actual output voltage change and the ideal (1 LSB) voltage change for a one bit change in code. A Differential Nonlinearity of ±1 LSB or less guarantees monotonictiy; i.e., the output always increases and never decreases for an increasing input.

SETTLING TIME

Settling time is the time required for the output to settle to within the specified error band for any input code transition. It is usually specified for a full scale or major carry transition.

DRIFT

GAIN DRIFT – The change in full scale analog output over the specified temperature range expressed in parts per million of full scale range per °C (ppm of FSR/°C). Gain error is measured with respect to +25°C at high (T_H) and low (T_L) temperatures. Gain drift is calculated for both high (T_H -25°C) and low ranges (+25°C -T_L) by dividing the gain error by the respective change in temperature. The specification is the larger of the two representing worst case drift.

OFFSET DRIFT – The change in analog output with all bits OFF over the specified temperature range expressed in parts per million of full scale range per °C (ppm of FSR/°C). Offset error is measured with respect to +25°C at high (T_H) and low (T_L) temperatures. Offset Drift is calculated for both high (T_H -25°C) and low (+25°C -T_L) ranges by dividing the offset error by the respective change in temperature. The specification given is the larger of the two, representing worst-case drift.

POWER SUPPLY SENSITIVITY

Power Supply Sensitivity is a measure of the change in gain and offset of the D/A converter resulting from a change in -15V, +5V or +15V supplies. It is specified under DC conditions and expressed as parts per million of full scale range per percent of change in power supply (ppm of FSR/%).

COMPLIANCE

Compliance voltage is the maximum output voltage range that can be tolerated and still maintain its specified accuracy. Compliance limit implies functional operation only and makes no claims to accuracy.

GLITCH

A glitch on the output of a D/A converter is a large transient spike resulting from unequal internal ON-OFF switching times. Worst case glitches usually occur at half-scale or the major carry code transition from 011...1 to 100...0 or vice versa. For example, if turn ON is greater than turn OFF for 011...1 to 100...0, an intermediate state of 000...0 exists, such that, the output momentarily glitches to zero output. Matched switching times and fast switching will reduce glitches considerably.

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DECOUPLING AND GROUNDING

For best accuracy and high frequency performance, the grounding and decoupling scheme shown in Figure 1 should be used. Decoupling capacitors should be connected close to the HI-562 (Preferrably to the device pins) and should be tantalum or electrolytic bypassed with ceramic types for best high frequency noise rejection.

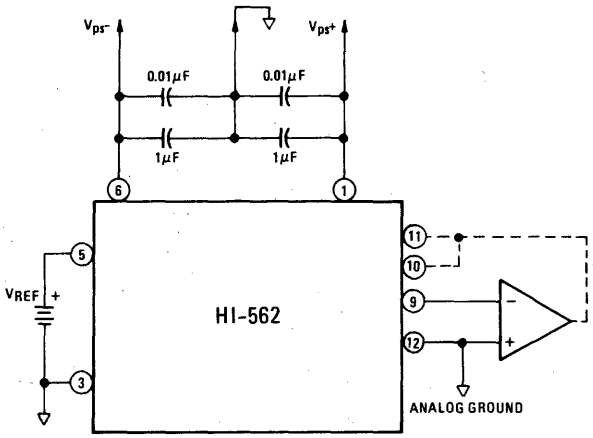
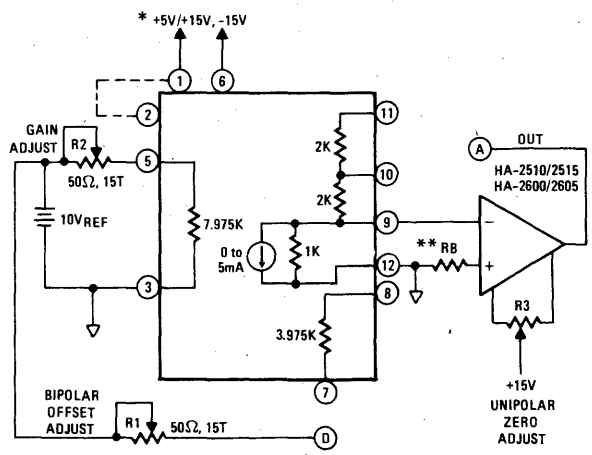


Figure 1

UNIPOLAR AND BIPOLAR VOLTAGE OUTPUT CONNECTIONS

CONNECTIONS – Using an external resistive load, the output compliance should not exceed ±1V to maintain specified accuracy. For higher output voltages, accuracy can be maintained by using an external op amp and the internal span resistors as shown in Figure 2 and defined in Table 1 for unipolar and bipolar modes.



* For TTL and DTL compatibility, connect +5V to pin 1 and leave pin 2 open. For CMOS compatibility, connect digital power supply ($+4.85V \leq V_{DD} \leq +12V$) to pin 1 and short pin 2 to pin 1.

** Bias resistor, RB, should be chosen to equalize op amp offset voltage due to bias current. Its value is calculated from the parallel combination of the current source output resistance (1K) and the op amp feedback resistor. See Table 1 for values of RB.

Figure 2

Table 1

	OUTPUT RANGE	CONNECTIONS Pin 7 to	Pin 8 to	Pin 10 to	Pin 11 to	BIAS (R_B) RESISTOR
Unipolar Mode	0 to +10V	N.C.	N.C.	A	N.C.	667Ω
	0 to +5V	N.C.	N.C.	A	9	500Ω
Bipolar Mode	±10V	D	9	N.C.	A	667Ω
	±5V	D	9	A	N.C.	580Ω
	±2.5V	D	9	A	9	444Ω

EXTERNAL GAIN AND ZERO CALIBRATION (See Figure 2)

The input reference resistor (7.975K) and bipolar offset resistors shown in Figure 2 are both intentionally set low by 25Ω to allow the user to externally trim-out initial errors to a very high degree of precision. The adjustments are made in the voltage output mode using an external op amp as current-to-voltage converter and the HI-562 internal scaling resistors as feedback elements for optimum accuracy and temperature coefficient. For best accuracy over temperature, select an op amp that has good front-end temperature coefficients such as the HA-2600/2605 with offset voltage and offset current tempco's of 5μV/°C and 1nA/°C, respectively. For high speed voltage mode applications where fast settling is required, the HA-2510/2515 is recommended for better than 1.5μs settling to 0.01%. Using either one, potentiometer R_3 conveniently nulls unipolar offset plus op amp offset in one operation (for HA-2510/2515 and HA-2600/2605 use R_3 = 20K and 100K, respectively). For bipolar mode operation, R_3 should be used to null op amp offset to optimize its tempco (i.e., short 9 to A and adjust R_3 for zero before calibrating in bipolar mode). The gain and bipolar offset adjustment range using 50Ω potentiometers is ±12 LSB and ±25 LSB respectively. If desired, the potentiometers can be replaced with fixed 24.9 Ω (1%) resistors resulting in an initial gain and bipolar offset accuracy of typically ±1/2 LSB.

UNIPOLAR CALIBRATION

Step 1: Unipolar Offset
- Turn all bits OFF
- Adjust R3 for zero volts output

Step 2: Gain
- Turn all bits ON
- Adjust R2 for an output of FS -1 LSB
  That is, adjust for:
  9.9976V for 0V to +10V range
  4.9988V for 0V to +5V range

BIPOLAR CALIBRATION

Step 1: Bipolar Offset
- Turn all bits OFF
- Adjust R1 for an output of:
  -10V for ±10V range
  -5V for ±5V range
  -2.5V for ±2.5V range

Step 2: Gain
- Turn bit 1 (MSB) ON; all other bits OFF
- Adjust R2 for zero volts output

HARRIS SEMICONDUCTOR PRODUCTS DIVISION
A DIVISION OF HARRIS CORPORATION

Preliminary

HI-5612

12 Bit High Speed Monolithic Digital-to-Analog Converter

FEATURES

- MONOLITHIC CONSTRUCTION
- EXTREMELY FAST SETTLING. . . . . .150ns TO ½LSB TYP.
- LOW GAIN DRIFT. . . . . .±5ppm/°C TYP.
- EXCELLENT LINEARITY OVER TEMPERATURE . . . . . .± ½LSB MAX.
- DESIGNED FOR MINIMUM GLITCHES
- MONOTONIC OVER TEMPERATURE

APPLICATIONS

- CRT DISPLAY GENERATION
- HIGH SPEED A/D CONVERTERS
- VIDEO SIGNAL RECONSTRUCTION
- WAVEFORM SYNTHESIZERS
- HIGH SPEED DATA ACQUISITION
- HIGH RELIABILITY APPLICATIONS
- PRECISION INSTRUMENTS

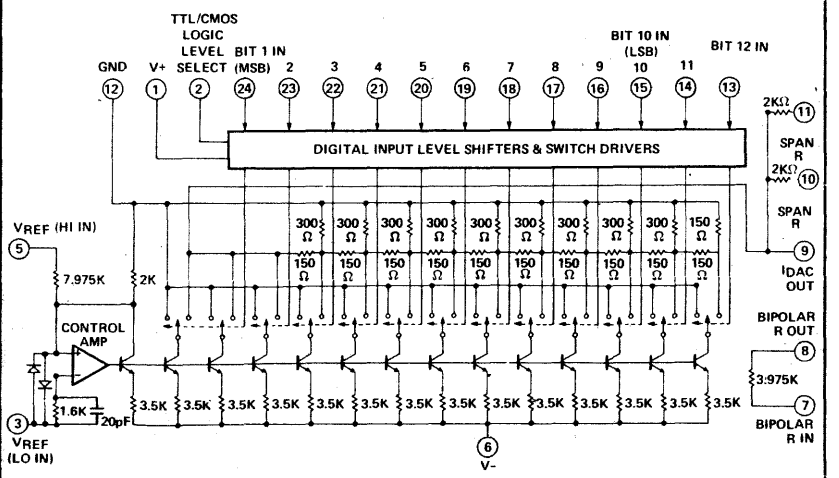
DESCRIPTION

The HI-5612 is an ultra-high speed 12 bit monolithic current output digital-to-analog converter. The fast output current settling of 150ns to ½LSB of its final value is achieved using dielectric isolation processing to reduce internal parasitics for fast rise and fall times during switching. Output glitches are minimized in the HI-5612 by incorporating equally weighted current sources switched into an R-2R ladder network for symmetrical turn-on and turn-off switching times. This creates within the chip a very uniform and constant thermal distribution for excellent linearity and also eliminates thermal transients during switching. High stability thin film resistor processing, together with laser trimming provide the HI-5612 with true 12 bit linearity to within ± ½LSB maximum over operating temperature range. The HI-5612's low offset and gain drift over the operating temperature range assures that its absolute accuracy when referred to a fixed 10V reference will not deviate more than ± 2LSB for both unipolar and bipolar operation.

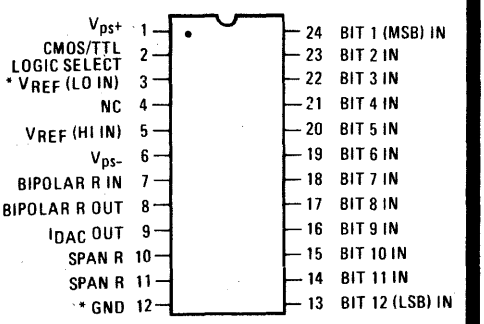
The HI-5612 is recommended as a replacement for high cost hybrid and modular units for increased reliability and accuracy in applications such as CRT Displays, precision instruments and data acquisition system requiring through-put rates as high as 7mHz for full range transitions. Its small size makes it an ideal choice as the essential part of high speed A/D converter designs or as a building block in high speed or high resolution industrial process control systems. The HI-5612 is also ideally suited for aircraft and space instrumentation where operation over a wide temperature range is required.

The HI-5612-5 is specified for operation over 0°C to +75°C, the HI-5612-2 and HI-5612-8 over -55°C to +125°C. Processing to MIL-STD-883A class B screening is available by selecting the HI-5612-8. All are available in a hermetically sealed 24 lead dual-in-line package.

FUNCTIONAL DIAGRAM



PINOUT



* Pin 3 connected to bottom case for high frequency shielding.

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ABSOLUTE MAXIMUM RATINGS (Referred to Ground)[1]

Power Supply Inputs	$V_{ps}+$	+20V
	$V_{ps}-$	-20V
Reference Inputs	VREF (Hi)	$\pm V_{ps}$
	VREF(Lo)	0V
Digital Inputs	Bits 1 - 12	-1V, +12V
	CMOS/TTL Logic Select	-1V, +12V
Outputs	Pins 7, 8, 10, 11	$\pm V_{ps}$
	Pin 9	$+V_{ps}$, -5V

Power Dissipation Pd, Package	1000mW
Operating Temperature Range	
HI-5612-2	-55°C to +125°C
HI-5612-5	0°C to +75°C
HI-5612-8	-55°C to +125°C
Storage Temperature Range	-65°C to +150°C

ELECTRICAL CHARACTERISTICS

(@ +25°C, $V_{ps}+$, = +5V, $V_{ps}-$ = -15V, V_{REF} = +10V, pin 2 ground unless otherwise noted)

		HI-5612-2 HI-5612-8			HI-5612-5			
PARAMETER	TEMP	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
INPUT CHARACTERISTICS								
Digital Inputs (2)								
TTL Logic Input Voltage (3)								
Logic "1"	Full	2.0			2.0			V
Logic "0"	Full			0.8			0.8	V
Input Current								
Logic "1"	Full		20	100		20	100	nA
Logic "0"	Full		-50	-100		-50	-100	μA
CMOS Logic Input Voltage (4)								
Logic "1"	Full	$0.7V_{ps}+$			$0.7V_{ps}+$			V
Logic "0"	Full			$0.3V_{ps}+$			$0.3V_{ps}+$	V
Input Current								
Logic "1"	Full		20	100		20	100	nA
Logic "0"	Full		-50	-100		-50	-100	μA
Reference Input								
Input Resistance			8K			8K		Ω
Input Voltage (I_{OUT} = 5mA + 20%)			+10			+10		V
TRANSFER CHARACTERISTICS								
Resolution	Full			12			12	Bits
Nonlinearity (5)	25°C			±½			±½	LSB
Differential Nonlinearity (5)	25°C			±½			±½	LSB
Relative Accuracy (6)								
Gain Error								(9)
(Input Code 11....1)			±0.024			±0.024		% FSR
Unipolar Offset Error								
(Input Code 00....0)			±0.05			±0.05		% FSR
Bipolar Offset Error								
(Input Code 00....0)			±0.024			±0.024		% FSR
(Adjustable to zero, see Figure 4, 5)								
Adjustment Range								
Gain			±0.25			±0.25		% FSR
Bipolar Offset			±0.25			±0.25		% FSR
Temperature Stability								
Gain Drift	Full		±5			±5		ppm/°C
Unipolar Offset Drift	Full		±3			±3		ppm/°C
Bipolar Offset Drift	Full		±3			±3		ppm/°C
Differential Nonlinearity	Full		±2			±2		ppm/°C
MONOTONICITY - GUARANTEED OVER FULL OPERATING TEMPERATURE RANGE								
Settling Time to ½LSB (5)								
From all 0's to all 1's			150			150		ns
From all 1's to all 0's			150			150		ns
Major Carry Switching to 90% Complete			50			50		ns

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PARAMETER	TEMP	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Power Supply Sensitivity (5)								
V_{ps}^+ = +5V, V_{ps}^- = -13.5V to -16.5V								
Gain								
(Input Code 11....1)				±2			±2	
Unipolar Offset								
(Input Code 00....0)			±0.5			±0.5		
Bipolar Offset								ppm of
(Input Code 00....0)			±1.5			±1.5		FSR/%V_{ps}
V_{ps}^- = -15V, V_{ps}^+ = 4.5V to 5.5V								
Gain								
(Input Code 11....1)				±1			±1	
Unipolar Offset								
(Input Code 00....0)			±0.5			±0.5		
Bipolar Offset								
(Input Code 00....0)			±1.5			±1.5		
OUTPUT CHARACTERISTICS								
Output Current								
Unipolar			-5.0			-5.0		mA
Bipolar			±2.5			±2.5		mA
Output Resistance			300			300		Ω
Output Capacitance			20			20		pF
Output Voltage Range (7)								
Unipolar			+10			+10		V
			+5			+5		V
Bipolar			±5			±5		V
			±2.5			±2.5		V
Output Compliance Limit (5)		-3		+10	-3		+10	V
Output Compliance Voltage (5)	Full		±1.5			±1.5		V
Output Noise Voltage (8)								
0.1Hz to 100Hz			10			10		μ V_{p-p}
0.1Hz to 1MHz			100			100		μ V_{p-p}
POWER REQUIREMENTS								
V_{ps}^+ (4)	Full	4.5	5	15	4.75	5	15	V
V_{ps}^-	Full	13.5	15	16.5	13.5	15	16.5	V
I_{ps}^+ (All 1's or all 0's in	25°C		9			9		mA
(10) either TTL or CMOS Mode)	Full		20			20		mA
I_{ps}^- (Same as above)	25°C		28			28		mA
(10)	Full		33			33		mA

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NOTES

1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied.
2. The HI-5612 accepts digital input codes in binary format and may be user connected for any one of three binary codes. Straight binary, offset binary, or two's complement binary. (See operating instructions)
3. For TTL and DTL compatibility connect +5V to pin 1 and ground pin 2. The $V_{ps}+$ tolerance is $\pm$10% for HI-5612-2, -8. And $\pm$ 5% for HI-5612-5.
4. For CMOS compatibility connect digital power supply ($+4.5V \leq V_{DD} \leq +10V$) to pin 1 and short pin 2 to pin 1.
5. See definitions.
6. Using an external op amp with internal span resistors and 24.9Ω $\pm$ 1% external trim resistors in place of potentiometers R1 and R2. These errors are adjustable to zero using R1 and R2. (See operating instructions)
7. Using an external op amp and internal span resistors. (See operating instructions for connections)
8. Specified for digital input in all '1's or all '0's.
9. FSR is "Full Scale Range" and is 10V for $\pm$ 5V range, 5V for $\pm$ 2.5V range, etc., or 5mA ($\pm$ 20%) for current output.
10. After 30 seconds warm-up.

DEFINITIONS OF SPECIFICATIONS

ACCURACY

NONLINEARITY - Nonlinearity of a D/A converter is an important measure of its accuracy. It describes the deviation from an ideal straight line transfer curve drawn between zero (all bits OFF) and full scale (all bits ON).

DIFFERENTIAL NONLINEARITY - For a D/A converter, it is the difference between the actual output voltage change and the ideal (1LSB) voltage change for a one bit change in code. A Differential Nonlinearity of $\pm$ 1LSB or less guarantees monotonicitiy; i.e., the output always increases and never decreases for and increasing input.

SETTLING TIME

Settling time is the time required for the output to settle to within the specified error band for any input code transition. It is usually specified for a full scale or major carry transition (01.....1 to 10.....0 or vice versa)

DRIFT

GAIN DRIFT - The change in full scale analog output over the specified temperature range expressed in parts per million of full scale range per ^{o}C (ppm of FSR/^{o}C). Gain error is measured with respect to +25^{o}C at high (T_H) and low (T_L) temperatures. Gain drift is calculated for both high (T_H -25^{o}C) and low ranges (+25^{o}C - T_L) by dividing the gain error by the respective change in temperature. The specification is the larger of the two representing worst case drift.

OFFSET DRIFT - The change in analog output with all bits OFF over the specified temperature range expressed in parts per million of full scale range per ^{o}C (ppm of FSR/^{o}C). Offset error is measured with respect to +25^{o}C at high (T_H) and low (T_L) temperatures. Offset Drift is calculated for both high (T_H -25^{o}C) and low (+25^{o}C -T_L) ranges by dividing the offset error by the respective change in temperature. The specification given is the larger of the two, representing worst case drift.

POWER SUPPLY SENSITIVITY

Power Supply Sensitivity is a measure of the change in gain and offset of the D/A converter resulting from a change in -15V, +5V or +15V supplies. It is specified under DC conditions and expressed as parts per million of full scale range per percent of change in power supply (ppm of FSR/%).

COMPLIANCE

Compliance voltage is the maximum output voltage range that can be tolerated and still maintain its specified accuracy. Compliance limit implies functional operation only and makes no claims to accuracy.

GLITCH

A glitch on the output of a D/A converter is a large transient spike resulting from unequal internal ON-OFF switching times. Worst case glitches usually occur at half-scale or the major carry code transition from 011.....1 to 100.....0 or vice versa. For example, if turn ON is greater than turn OFF for 011.....1 to 100.....0, an intermediate state of 000.....0 exists, such that, the output momentarily glitches to zero output. Matched switching times and fast switching will reduce glitches considerably.

OPERATING INSTRUCTIONS

DECOUPLING AND GROUNDING

For best accuracy and high speed performance, the grounding and decoupling scheme shown in Figure 1 should be used. Decoupling capacitors should be connected close to the HI-5612 (preferrably to the device pin) and should be tantalum or electrolytic bypassed with ceramic types for best high frequency noise rejection.

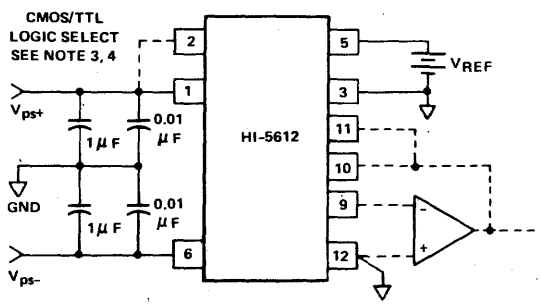


FIGURE 1

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HIGH PERCISION PERFORMANCE

The output accuracy of the HI-5612 depends mainly on the accuracy of the voltage applied to the VREF input of HI-5612 and it can be described roughly as VREF/8KΩ = ¼ full scale output current. This means the output of HI-5612 will change whenever VREF varies. For high precision performance a precision +10V voltage reference with reasonably low temperature coefficient such as HA-1600 is highly recommended. For voltage output operation use an external op amp as current-to-voltage converter and the HI-5612 internal scaling resistors as feedback elements for optimum accuracy and temperature coefficient. The selected op amp should have a good front-end temperature coefficient such as HA-2600/2605 with offset voltage and offset current tempco's of 5 μ V/°C and 1nA/°C, respectively. The input reference resistor (7.975KΩ) and bipolar offset resistor (3.975K Ω) are both intentionally set low by 25 Ω to allow the user to externally trim-out initial errors to a very high degree of precision. For high speed voltage output applications where fast settling is required, the HA-2510/2515 is recommended for better than 1.2 μ s settling to ½LSB.

UNIPOLAR VOLTAGE OUTPUT CONNECTIONS AND CALIBRATION

The connections for unipolar +10V and +5V voltage output using an external op amp and the internal span resistors are shown in Figure 2 and Figure 3, respectively.

CALIBRATION - UNIPOLAR

Step 1 Offset
- Turn all bits off (all 0's)
- Adjust R3 for zero volts output

Step 2 Gain
- Turn all bits on (all 1's)
- Adjust R1 for an output of FS-1LSB
- That is, adjust for:
- 9.99756V for 0V to +10V range
- 4.99878V for 0V to +5V range

UNIPOLAR - STRAIGHT BINARY
0V TO +10V OUTPUT RANGE

DIGITAL INPUT	ANALOG OUTPUT	
11 1	FS - 1LSB	= 9.99756V
10 0	½FS	= 5.00000V
01 1	½FS -1LSB	= 4.99756V
00 0	Zero	= 0.00000V

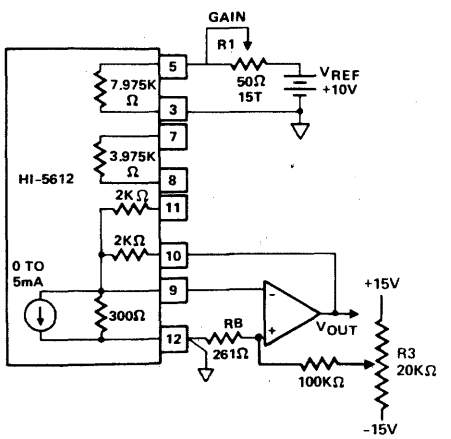


FIGURE 2

UNIPOLAR - STRAIGHT BINARY
0V TO +5V OUTPUT RANGE

DIGITAL INPUT	ANALOG OUTPUT	
11 1	FS - 1LSB	= 4.99878V
10 0	½FS	= 2.50000V
01 1	½FS -1LSB	= 2.49878V
00 0	Zero	= 0.00000V

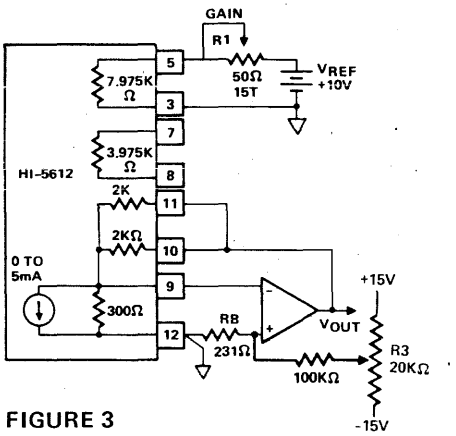


FIGURE 3

BIPOLAR VOLTAGE OUTPUT CONNECTIONS AND CALIBRATION

The connections for Bipolar ± 5V and ± 2.5V voltage output using an external op amp and the internal span resistors are shown in Figure 4 and Figure 5, respectively.

CALIBRATION - BIPOLAR

Step 1 Op Amp Null
- Short op amp output to op amp -input
- Adjust R3 for zero volts output

Step 2 Gain
- Turn all bits on (all 1's) record output voltage
- Turn all bits off (all 0's) record output voltage
- Adjust R1 till the difference between the readings is equal to:
  9.99756V for ± 5V range
  4.99878V for ±2.5V range

Step 3 Offset
- Turn bit 1 (MSB) on, all other bits off (10....0)
- Adjust R2 for zero volts output

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BIPOLAR - OFFSET BINARY
±5V OUTPUT VOLTAGE RANGE

DIGITAL INPUT	ANALOG OUTPUT	
11 1	+FS - 1LSB	= +4.99756V
10 0	Zero	= +0.00000V
01 1	Zero -1LSB	= -0.00244V
00 0	-FS	= -5.00000V

BIPOLAR - TWO'S COMPLEMENT **
±5V OUTPUT VOLTAGE RANGE

DIGITAL INPUT	ANALOG OUTPUT	
01 1	+FS - 1LSB	= +4.99756V
00 0	Zero	= +0.00000V
11 1	Zero -1LSB	= -0.00244V
10 0	-FS	= -5.00000V

** Invert MSB with external inverter to obtain two's complement coding.

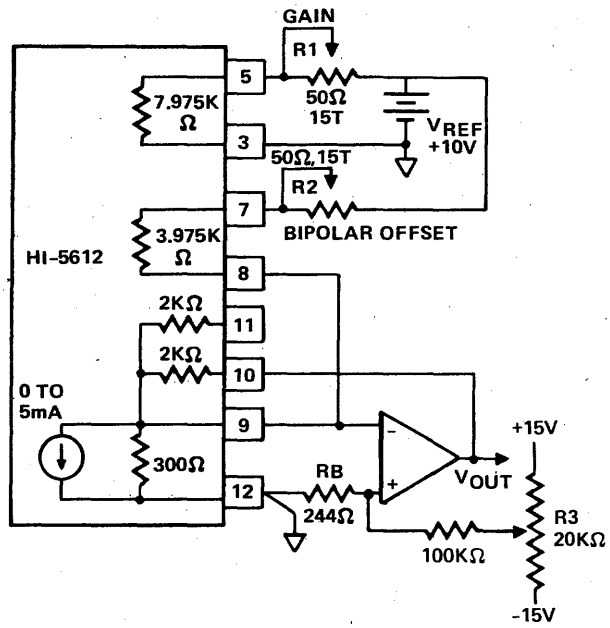


FIGURE 4

BIPOLAR - OFFSET BINARY
±2.5V OUTPUT VOLTAGE RANGE

DIGITAL INPUT	ANALOG OUTPUT	
11 1	+FS - 1LSB	= +2.49878V
10 0	Zero	= +0.00000V
01 1	Zero -1LSB	= -0.00122V
00 0	-FS	= -2.50000V

BIPOLAR - TWO'S COMPLEMENT **
±2.5V OUTPUT VOLTAGE RANGE

DIGITAL INPUT	ANALOG OUTPUT	
01 1	+FS - 1LSB	= +2.49878V
00 0	Zero	= +0.00000V
11 1	Zero -1LSB	= -0.00122V
10	-FS	= -2.50000V

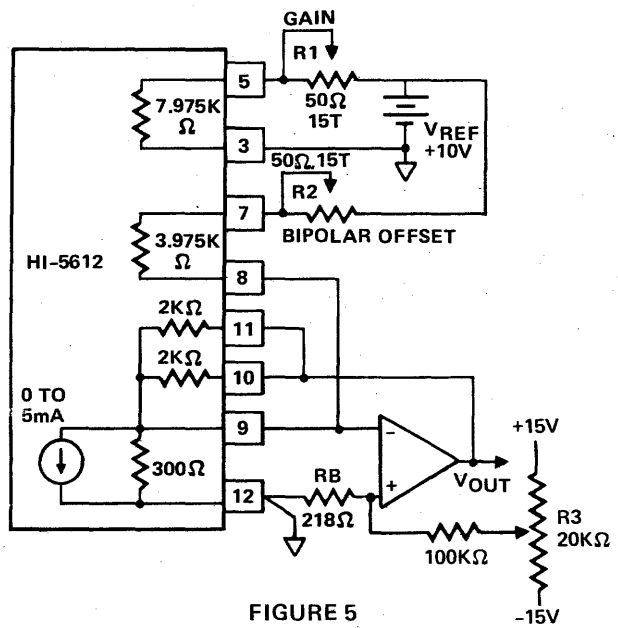


FIGURE 5

SALES OFFICES--

2016 QUAIL STREET
NEWPORT BEACH, CALIF. 92660
(714) 540-2176

SUITE 300
625 ELLIS STREET
MOUNTAIN VIEW, CALIF. 94043
(415) 964-6443

SUITE 115
2020 WEST MCNAB ROAD
FT. LAUDERDALE, FL. 33309
(305) 971-3200

SUITE 508
2355 S. ARLINGTON HTS. RD.
ARLINGTON HTS., ILL. 60005
(312) 437-4712

SUITE 301
177 WORCESTER STREET
WELLESLEY HILLS, MASS. 02181
(617) 237-5430

SUITE 519
2850 METRO DRIVE
BLOOMINGTON, MINN. 55420
(612) 854-3484

535 BROADHOLLOW ROAD
MELVILLE, L.I., N.Y. 11746
(516) 249-4500

SUITE 100
4972 NORTHCUTT PLACE
DAYTON, OHIO 45414
(513) 226-0636

SUITE 325
650 E. SWEDESFORD ROAD
WAYNE, PENN. 19087
(215) 687-6680

SUITE 7G
777 S. CENTRAL EXPRESSWAY
RICHARDSON, TEXAS 75080
(214) 231-9031

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MELBOURNE, FL. 32901
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Preliminary

HI-5610

10 Bit High Speed Monolithic Digital-to-Analog Converter

FEATURES

- MONOLITHIC CONSTRUCTION
- EXTREMELY FAST SETTLING. . . . . 85ns TO ½LSB TYP.
- LOW GAIN DRIFT. . . . . ±5ppm/°C TYP.
- EXCELLENT LINEARITY OVER TEMPERATURE . . . . . ±½LSB MAX.
- DESIGNED FOR MINIMUM GLITCHES
- MONOTONIC OVER TEMPERATURE

APPLICATIONS

- CRT DISPLAY GENERATION
- HIGH SPEED A/D CONVERTERS
- VIDEO SIGNAL RECONSTRUCTION
- WAVEFORM SYNTHESIZERS
- HIGH SPEED DATA ACQUISITION
- HIGH RELIABILITY APPLICATIONS
- PRECISION INSTRUMENTS

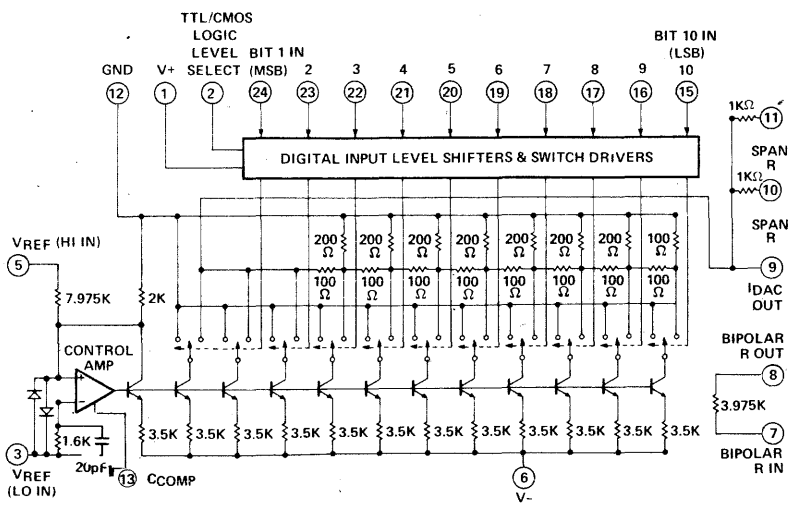
DESCRIPTION

The HI-5610 is an ultra-high speed 10 bit monolithic current output digital-to-analog converter. The fast output current settling of 85ns to ½LSB of its final value is achieved using dielectric isolation processing to reduce internal parasitics for fast rise and fall times during switching. Output glitches are minimized in the HI-5610 by incorporating equally weighted current sources switched into an R-2R ladder network for symmetrical turn-on and turn-off switching times. This creates within the chip a very uniform and constant thermal distribution for excellent linearity and also eliminates thermal transients during switching. High stability thin film resistor processing, together with laser trimming provide the HI-5610 with true 10 bit linearity to within ± ½LSB maximum over operating temperature range. The HI-5610's low offset and gain drift over the operating temperature range assures that its absolute accuracy when referred to a fixed 10V reference will not deviate more than ±1LSB for both unipolar and bipolar operation.

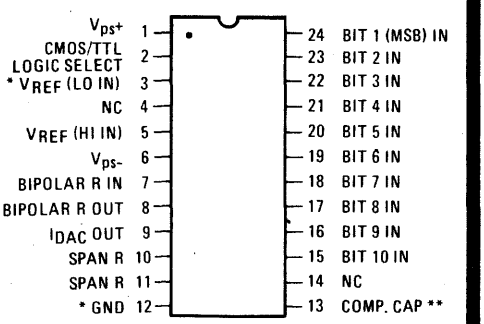
The HI-5610 is recommended as a replacement for high cost hybrid and modular units for increased reliability and accuracy in applications such as CRT Displays, precision instruments and data acquisition system requiring through-put rates as high as 12mHz for full range transitions. Its small size makes it an ideal choice as the essential part of high speed A/D converter designs or as a building block in high speed or high resolution industrial process control systems. The HI-5610 is also ideally suited for aircraft and space instrumentation where operation over a wide temperature range is required.

The HI-5610-5 is specified for operation over 0°C to +75°C, the HI-5610-2 and HI-5610-8 over -55°C to +125°C. Processing to MIL-STD-883A class B screening is available by selecting the HI-5610-8. All are available in a hermetically sealed 24 lead dual-in-line package.

FUNCTIONAL DIAGRAM



PINOUT



* Pin 3 connected to bottom case for high frequency shielding.

** For high speed operation, connect 0.01μF between Pin 13 and GND. Otherwise, leave Pin 13 open.

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SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS (Referred to Ground)[1]

Power Supply Inputs	$V_{ps}+$	+20V
	$V_{ps}-$	-20V
Reference Inputs	VREF (Hi)	$\pm V_{ps}$
	VREF(Lo)	0V
Digital Inputs	Bits 1 - 12	-1V, +12V
	CMOS/TTL Logic Select	-1V, +12V
Outputs	Pins 7, 8, 10, 11	$\pm V_{ps}$
	Pin 9	$+V_{ps}$, -5V

Power Dissipation Pd, Package	1000mW
Operating Temperature Range	
HI-5610-2	-55°C to +125°C
HI-5610-5	0°C to +75°C
HI-5610-8	-55°C to +125°C
Storage Temperature Range	-65°C to +150°C

ELECTRICAL CHARACTERISTICS (@ +25°C, $V_{ps}+$, = +5V, $V_{ps}-$ = -15V, V_{REF} = +10V, pin 2 ground unless otherwise noted)

		HI-5610-2 HI-5610-8			HI-5610-5			
PARAMETER	TEMP	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
INPUT CHARACTERISTICS								
Digital Inputs (2)								
TTL Logic Input Voltage (3)								
Logic "1"	Full	2.0			2.0			V
Logic "0"	Full			0.8			0.8	V
Input Current								
Logic "1"	Full		20	100		20	100	nA
Logic "0"	Full		-50	-100		-50	-100	μA
CMOS Logic Input Voltage (4)								
Logic "1"	Full	0.7 $V_{ps}+$			0.7 $V_{ps}+$			V
Logic "0"	Full			0.3 $V_{ps}+$			0.3 $V_{ps}+$	V
Input Current								
Logic "1"	Full		20	100		20	100	nA
Logic "0"	Full		-50	-100		-50	-100	μA
Reference Input								
Input Resistance			8K			8K		Ω
Input Voltage (I_{OUT} = 5mA + 20%)			+10			+10		V
TRANSFER CHARACTERISTICS								
Resolution	Full			10			10	Bits
Nonlinearity (5)	25°C			± ½			± ½	LSB
Differential Nonlinearity (5)	25°C			± ½			± ½	LSB
Relative Accuracy (6)								
Gain Error								(9)
(Input Code 11....1)			± 0.05			± 0.05		% FSR
Unipolar Offset Error								
(Input Code 00....0)			± 0.05			± 0.05		% FSR
Bipolar Offset Error								
(Input Code 00....0)			± 0.05			± 0.05		% FSR
(Adjustable to zero, see Figure 4, 5)								
Adjustment Range								
Gain			± 0.25			± 0.25		% FSR
Bipolar Offset			± 0.25			± 0.25		% FSR
Temperature Stability								
Gain Drift	Full		± 5			± 5		ppm/°C
Unipolar Offset Drift	Full		± 3			± 3		ppm/°C
Bipolar Offset Drift	Full		± 3			± 3		ppm/°C
Differential Nonlinearity	Full		± 2			± 2		ppm/°C
MONOTONICITY - GUARANTEED OVER FULL OPERATING TEMPERATURE RANGE								
Settling Time to ½LSB (5)								
From all 0's to all 1's			85			85		ns
From all 1's to all 0's			85			85		ns
Major Carry Switching to 90% Complete			40			40		ns

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PARAMETER	TEMP	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Power Supply Sensitivity (5) V_{ps}+ = +5V, V_{ps}- = -13.5V to -16.5V Gain (Input Code 11....1) Unipolar Offset (Input Code 00....0) Bipolar Offset (Input Code 00....0)			 ±0.5 ±1.5	 ±2		 ±0.5 ±1.5	 ±2	ppm of FSR/%V_{ps}
V_{ps}- = -15V, V_{ps}+ = 4.5V to 5.5V Gain (Input Code 11....1) Unipolar Offset (Input Code 00....0) Bipolar Offset (Input Code 00....0)			 ±0.5 ±1.5	 ±1		 ±0.5 ±1.5	 ±1	
OUTPUT CHARACTERISTICS								
Output Current Unipolar Bipolar			 -5.0 ±2.5			 -5.0 ±2.5		 mA mA
Output Resistance			200			200		Ω
Output Capacitance			20			20		pF
Output Voltage Range (7) Unipolar Bipolar			 +5 +2.5 ±2.5 ±1.25			 +5 +2.5 ±2.5 ±1.25		 V V V V
Output Compliance Limit (5)		-3		+10	-3		+10	V
Output Compliance Voltage (5)	Full		±1.5			±1.5		V
Output Noise Voltage (8) 0.1Hz to 100Hz 0.1Hz to 1MHz			 10 100			 10 100		 μVp-p μVp-p
POWER REQUIREMENTS								
V_{ps}+ (4)	Full	4.5	5	15	4.75	5	15	V
V_{ps}-	Full	13.5	15	16.5	13.5	15	16.5	V
I_{ps}+ (All 1's or all 0's in (10) either TTL or CMOS Mode)	25°C Full		9 20			9 20		mA mA
I_{ps}- (Same as above) (10)	25°C Full		25 30			25 30		mA mA

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NOTES

1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied.
2. The HI-5610 accepts digital input codes in binary format and may be user connected for any one of three binary codes. Straight binary, offset binary, or two's complement binary. (See operating instructions)
3. For TTL and DTL compatibility connect +5V to pin 1 and ground pin 2. The $V_{ps}+$ tolerance is ±10% for HI-5610-2, -8. And ± 5% for HI-5610-5.
4. For CMOS compatibility connect digital power supply ($+4.5V \leq V_{DD} \leq +10V$) to pin 1 and short pin 2 to pin 1.
5. See definitions.
6. Using an external op amp with internal span resistors and 24.9Ω ± 1% external trim resistors in place of potentiometers R1 and R2. These errors are adjustable to zero using R1 and R2. (See operating instructions)
7. Using an external op amp and internal span resistors. (See operating instructions for connections)
8. Specified for digital input in all '1's or all '0's.
9. FSR is "Full Scale Range" and is 5V for ± 2.5V range, 2.5V for ± 1.25V range, etc., or 5mA (± 20%) for current output.
10. After 30 seconds warm-up.

DEFINITIONS OF SPECIFICATIONS

ACCURACY

NONLINEARITY - Nonlinearity of a D/A converter is an important measure of its accuracy. It describes the deviation from an ideal straight line transfer curve drawn between zero (all bits OFF) and full scale (all bits ON).

DIFFERENTIAL NONLINEARITY - For a D/A converter, it is the difference between the actual output voltage change and the ideal (1LSB) voltage change for a one bit change in code. A Differential Nonlinearity of ± 1LSB or less guarantees monotonicitiy; i.e., the output always increases and never decreases for and increasing input.

SETTLING TIME

Settling time is the time required for the output to settle to within the specified error band for any input code transition. It is usually specified for a full scale or major carry transition (01.....1 to 10.....0 or vice versa)

DRIFT

GAIN DRIFT - The change in full scale analog output over the specified temperature range expressed in parts per million of full scale range per °C (ppm of FSR/°C). Gain error is measured with respect to +25°C at high (T_H) and low (T_L) temperatures. Gain drift is calculated for both high (T_H -25°C) and low ranges (+25°C - T_L) by dividing the gain error by the respective change in temperature. The specification is the larger of the two representing worst case drift.

OFFSET DRIFT - The change in analog output with all bits OFF over the specified temperature range expressed in parts per million of full scale range per °C (ppm of FSR/°C). Offset error is measured with respect to +25°C at high (T_H) and low (T_L) temperatures. Offset Drift is calculated for both high (T_H -25°C) and low (+25°C -T_L) ranges by dividing the offset error by the respective change in temperature. The specification given is the larger of the two, representing worst case drift.

POWER SUPPLY SENSITIVITY

Power Supply Sensitivity is a measure of the change in gain and offset of the D/A converter resulting from a change in -15V, +5V or +15V supplies. It is specified under DC conditions and expressed as parts per million of full scale range per percent of change in power supply (ppm of FSR/%).

COMPLIANCE

Compliance voltage is the maximum output voltage range that can be tolerated and still maintain its specified accuracy. Compliance limit implies functional operation only and makes no claims to accuracy.

GLITCH

A glitch on the output of a D/A converter is a large transient spike resulting from unequal internal ON-OFF switching times. Worst case glitches usually occur at half-scale or the major carry code transition from 011.....1 to 100.....0 or vice versa. For example, if turn ON is greater than turn OFF for 011.....1 to 100.....0, an intermediate state of 000.....0 exists, such that, the output momentarily glitches to zero output. Matched switching times and fast switching will reduce glitches considerably.

OPERATING INSTRUCTIONS

DECOUPLING AND GROUNDING

For best accuracy and high speed performance, the grounding and decoupling scheme shown in Figure 1 should be used. Decoupling capacitors should be connected close to the HI-5610 (preferrably to the device pin) and should be tantalum or electrolytic bypassed with ceramic types for best high frequency noise rejection.

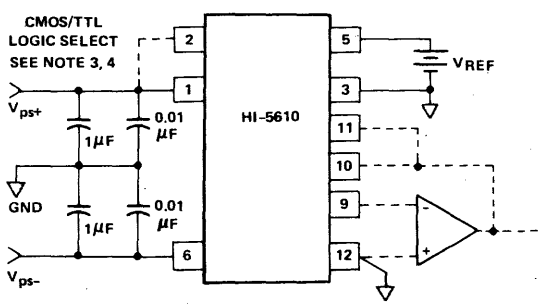


FIGURE 1

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HIGH PERCISION PERFORMANCE

The output accuracy of the HI-5610 depends mainly on the accuracy of the voltage applied to the VREF input of HI-5610 and it can be described roughly as VREF/8KΩ = ¼ full scale output current. This means the output of HI-5610 will change whenever VREF varies. For high precision performance a precision +10V voltage reference with reasonably low temperature coefficient such as HA-1600 is highly recommended. For voltage output operation use an external op amp as current-to-voltage converter and the HI-5610 internal scaling resistors as feedback elements for optimum accuracy and temperature coefficient. The selected op amp should have a good front-end temperature coefficient such as HA-2600/2605 with offset voltage and offset current tempco's of 5 μV/°C and 1nA/°C, respectively. The input reference resistor (7.975K Ω) and bipolar offset resistor (3.975K Ω) are both intentionally set low by 25 Ω to allow the user to externally trim-out initial errors to a very high degree of precision. For high speed voltage output applications where fast settling is required, the HA-2510/2515 is recommended for better than 1 μs settling to ½LSB.

UNIPOLAR VOLTAGE OUTPUT CONNECTIONS AND CALIBRATION

The connections for unipolar +5V and +2.5V voltage output using an external op amp and the internal span resistors are shown in Figure 2 and Figure 3, respectively.

CALIBRATION - UNIPOLAR

Step 1 Offset
- Turn all bits off (all 0's)
- Adjust R3 for zero volts output

Step 2 Gain
- Turn all bits on (all 1's)
- Adjust R1 for an output of FS-1LSB
  That is, adjust for:
  4.99512V for 0V to +5V range
  2.49756V for 0V to +2.5V range

UNIPOLAR - STRAIGHT BINARY
0V TO +5V OUTPUT RANGE

DIGITAL INPUT	ANALOG OUTPUT	
11 1	FS - 1LSB	= 4.99512V
10 0	½FS	= 2.50000V
01 1	½FS -1LSB	= 2.49512V
00 0	Zero	= 0.00000V

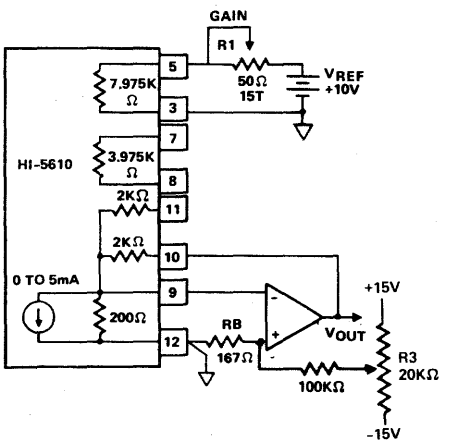


FIGURE 2

UNIPOLAR - STRAIGHT BINARY
0V TO +2.5V OUTPUT RANGE

DIGITAL INPUT	ANALOG OUTPUT	
11 1	FS - 1LSB	= 2.49756V
10 0	½FS	= 1.25000V
01 1	½FS -1LSB	= 1.24756V
00 0	Zero	= 0.00000V

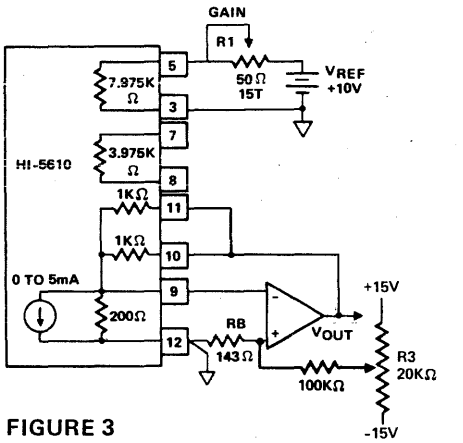


FIGURE 3

BIPOLAR VOLTAGE OUTPUT CONNECTIONS AND CALIBRATION

The connections for Bipolar ± 2.5V and ± 1.25V voltage output using an external op amp and the internal span resistors are shown in Figure 4 and Figure 5, respectively.

CALIBRATION - BIPOLAR

Step 1 Op Amp Null
- Short op amp output to op amp -input
- Adjust R3 for zero volts output

Step 2 Gain
- Turn all bits on (all 1's) record output voltage
- Turn all bits off (all 0's) record output voltage
- Adjust R1 till the difference between the readings is equal to:
  4.99512V for ± 2.5V range
  2.49756V for ±1.25V range.

Step 3 Offset
- Turn bit 1 (MSB) on, all other bits off (10....0)
- Adjust R2 for zero volts output

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BIPOLAR - OFFSET BINARY
± 2.5V OUTPUT VOLTAGE RANGE

DIGITAL INPUT	ANALOG OUTPUT	
11 1	+FS - 1 LSB	= +2.49512V
10 0	ZERO	= +0.00000V
01 1	Zero - 1 LSB	= -0.00488V
00 0	-FS	= -2.50000V

BIPOLAR TWO'S COMPLEMENT **
± 2.5V OUTPUT VOLTAGE RANGE

DIGITAL INPUT	ANALOG OUTPUT	
01 1	+FS - 1LSB	= +2.49512V
00 0	Zero	= +0.00000V
11 1	Zero - 1LSB	= -0.00488V
10 0	-FS	= -2.50000V

** Invert MSB with external inverter to obtain two's complement coding.

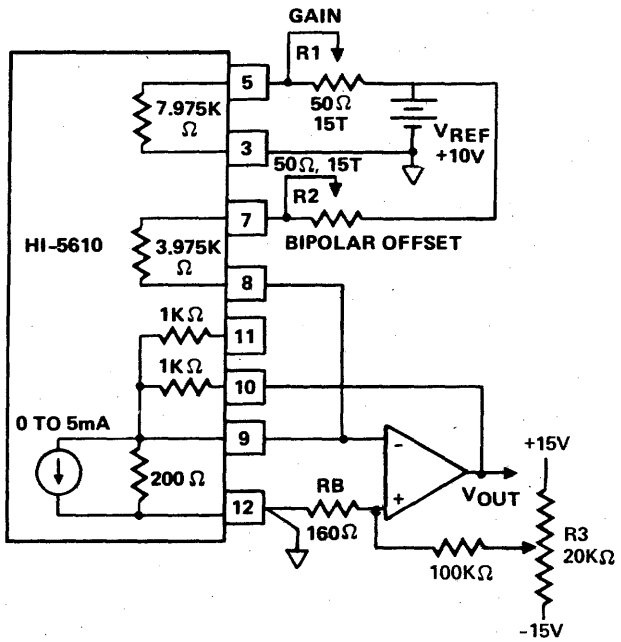


FIGURE 4

BIPOLAR - OFFSET BINARY
± 1.25V OUTPUT VOLTAGE RANGE

DIGITAL INPUT	ANALOG OUTPUT	
11 1	+FS - 1LSB	= +1.24756V
10 0	Zero	= +0.00000V
01 1	Zero - 1LSB	= -0.00244V
00 0	-FS	= -1.25000V

BIPOLAR - TWO'S COMPLEMENT **
± 1.25V OUTPUT VOLTAGE RANGE

DIGITAL INPUT	ANALOG OUTPUT	
01 1	+FS - 1LSB	= +1.24756V
00 0	Zero	= +0.00000V
11 1	Zero - 1LSB	= -0.00244V
10	-FS	= -1.25000V

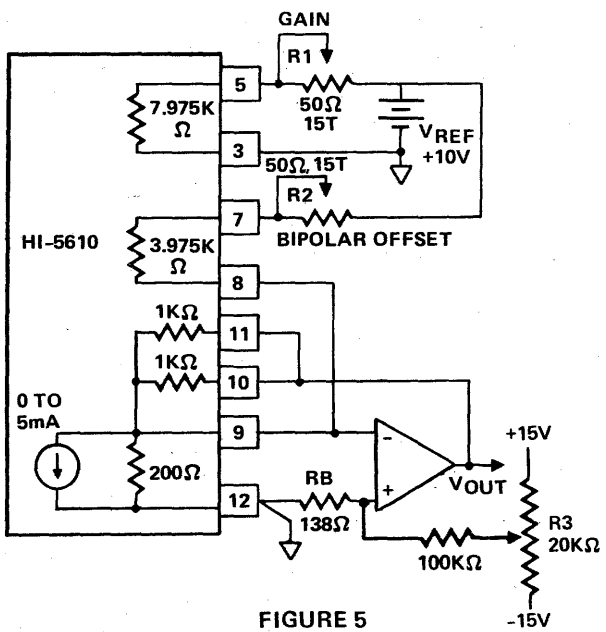


FIGURE 5

SALES OFFICES–

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(714) 540-2176

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625 ELLIS STREET
MOUNTAIN VIEW, CALIF. 94043
(415) 964-6443

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(305) 971-3200

SUITE 508
2355 S. ARLINGTON HTS. RD.
ARLINGTON HTS., ILL. 60005
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(617) 237-5430

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(612) 854-3484

535 BROADHOLLOW ROAD
MELVILLE, L.I., N.Y. 11746
(516) 249-4500

SUITE 100
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DAYTON, OHIO 45414
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650 E. SWEDESFORD ROAD
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HI-5608

8-Bit High Speed Monolithic Digital-to-Analog Converter

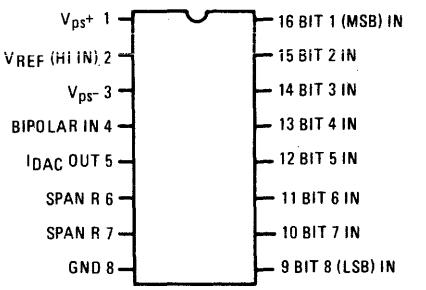
Advance Information

FEATURES

- MONOLITHIC CONSTRUCTION
- EXTREMELY FAST SETTLING . . . . . 45ns TO ½ LSB (TYP)
- LOW GAIN DRIFT . . . . . 10ppm/°C (TYP)
- LINEARITY GUARANTEED OVER TEMPERATURE . . . . . ¼ LSB (MAX)
- GAIN SETTLING AND FEEDBACK RESISTORS ON CHIP
- MONOTONICITY GUARANTEED OVER TEMPERATURE
- DESIGNED FOR MINIMUM GLITCHES
- 16-PIN HERMETIC PACKAGE

PINOUT

TOP VIEW



DESCRIPTION

The HI-5608 is an ultra-high speed 8-bit monolithic current output digital-to-analog converter. The fast output current settling of 45ns to ½ LSB of its final value is achieved using dielectric isolation processing to reduce internal parasitics for fast rise and fall times during switching. Output glitches are minimized in the HI-5608 by incorporating equally weighted current sources switched into an R-2R ladder network for symetrical turn-on and turn-off switching times. This creates within the chip a very uniform and constant thermal distribution for excellent linearity and also eliminates thermal transients during switching. High stability thin film resistor processing, together with laser trimming provide the HI-5608 with guaranteed true 8-bit linearity to within ± ¼ LSB maximum over operating temperature range. The HI-5608's low offset and gain drift over the operating temperature range assures that its absolute accuracy when referred to a fixed 10V reference will not deviate more than ± 3/8 LSB for both unipolar and bipolar operation.

The HI-5608 is recommended as a replacement for high cost hybrid and modular units for increased reliability and accuracy in applications such as CRT display, and data acquisition systems requiring through-put rates as high as 20MHz for full range transitions. Its small size makes it an ideal choice as the essential part of high speed A/D converter designs or as a building block in high speed industrial process control systems. The HI-5608 is also ideally suited for aircraft and space instrumentation where operation over a wide temperature range is required.

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HD-0165
Keyboard Encoder

FEATURES

- STROBE OUTPUT
- KEY ROLLOVER OUTPUT
- EXPANDABLE: 2 PACKAGES REQUIRED FOR FULL TELETYPEWRITER, EIGHT-BIT ENCODING
- SINGLE +5.0V SUPPLY REQUIRED
- DTL/TTL OUTPUTS
- MONOLITHIC RELIABILITY

APPLICATIONS

- MICROPROCESSOR DATA ENTRY (16 KEY TO HEX CODE)
- BCD DATA ENTRY
- TYPEWRITER TYPE KEYBOARDS
- CONTROL PANELS

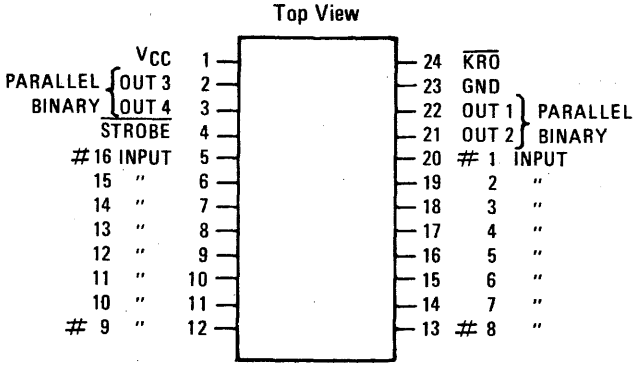
DESCRIPTION

The HD-0165 Keyboard Encoder is a 16 line to four-bit parallel encoder intended for use with manual data entry devices such as calculator or typewriter keyboards. In addition to the encoding function, there is a Strobe output and a Key Rollover output which energizes whenever two or more inputs are energized simultaneously. Any four-bit code can be implemented by proper wiring of the input lines. Inputs are normally wired through the key switches to the +5.0V power supply. Full typewriter keyboard encoding up to eight bits can be accomplished with two Encoder circuits by the use of double pole key switches or single pole switches with two isolation diodes per key. Outputs will interface with all popular DTL and TTL logic families. The circuit is packaged in a hermetic 24-pin dual-in-line package and operates over the temperature range of 0°C to +75°C.

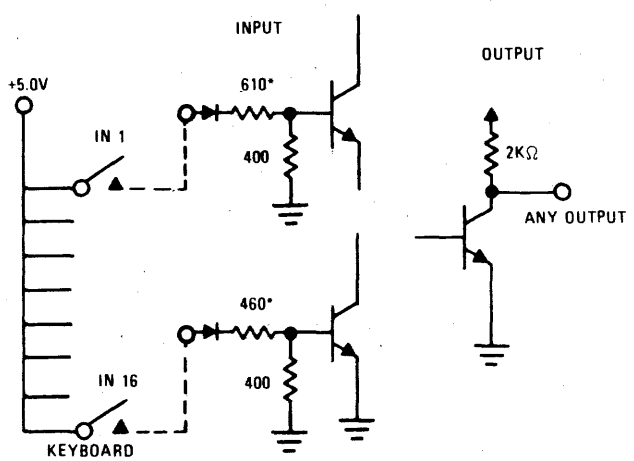
PINOUT

Package Code 4K

Top View



EQUIVALENT CIRCUITS



* EQUIVALENT RESISTORS FOR OTHER INPUTS ARE BETWEEN THESE TWO VALUES

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SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+7.0V	Output Current	30mA
Input Voltage	+5.5V	Storage Temperature	-65^{o} to $+150^{o}C$
Output Voltage	+5.5V	Operating Temperature (Case)	$0^{o}C$ to $+75^{o}C$

ELECTRICAL CHARACTERISTICS

Test Conditions: $V_{CC} = +5.0V \pm 5\%$
$T_{Case} = 0^{o}C$ to $+75^{o}C$
Unless otherwise specified

	PARAMETER	SYM.	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNITS	TEST CONDITIONS
D.C.	Input Current "1"	I_{IH}			17	mA	$V_{IN} = +5.0V$
D.C.	Output Voltage "0"	V_{OL}		+0.2	+0.4	V	$V_{IH} = +4.5V$ $I_{OL} = 10mA$
D.C.	Output Voltage "0"	V_{OL}			+0.4	V	$V_{IH} = +3.5V$ $I_{OL} = 3.2mA$
D.C.	Output Voltage "1"	V_{OH}	+2.4	+4.0		V	V_{IL} = Open Circuit, $I_{OH} = -240\mu A$
D.C.	Power Supply Current Operating	I_{CC}			52	mA	One Input at +5.25V
D.C.	Power Supply Current Maximum	I_{CCM}			88	mA	All Inputs at +5.25V
A.C.	Skew Time (Note 1)	T_{SK}		80	200	ns	$T_{Case} = 25^{o}C$, $V_{CC} = V_{IN} = +5.0V$, $C_L < 50pF$

NOTE: (1) Skew time is the maximum time differential between propagation delay times of any outputs including strobe and $\overline{K_{RO}}$.

TRUTH TABLE

INPUTS 1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	OUTPUTS 1	2	3	4	$\overline{St.}$	$\overline{K_{RO}}$
L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H	H	H	H	H	H
H	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H	H	H	H	L	H
L	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H	H	H	L	H
L	L	H	L	L	L	L	L	L	L	L	L	L	L	L	L	H	L	H	H	L	H
L	L	L	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H	H	L	H
L	L	L	L	H	L	L	L	L	L	L	L	L	L	L	L	H	H	L	H	L	H
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L	L	L	L	L	L	L	L	L	L	L	L	L	L	H	L	H	L	L	L	L	H
L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H	L	L	L	L	L	H
ANY TWO OR MORE HIGH																X	X	X	X	L	L

INPUTS: L = Open Circuit or < +1.0V H = > +4.5V Current Source
OUTPUTS: L = < +0.4V H = > +2.4V X = Erroneous Data

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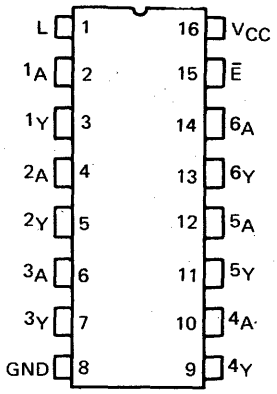
HD-6431
CMOS THREE-STATE LATCHING BUS DRIVER

Features

- SINGLE POWER SUPPLY
- HIGH NOISE IMMUNITY
- INDUSTRIAL AND MILITARY GRADES
- DRIVE CAPACITY. 300pF
- SOURCE CURRENT. 4mA
- SINK CURRENT 6mA
- PROPAGATION DELAY . . . . . 65nsec @ 5V

Pinout

TOP VIEW



Description

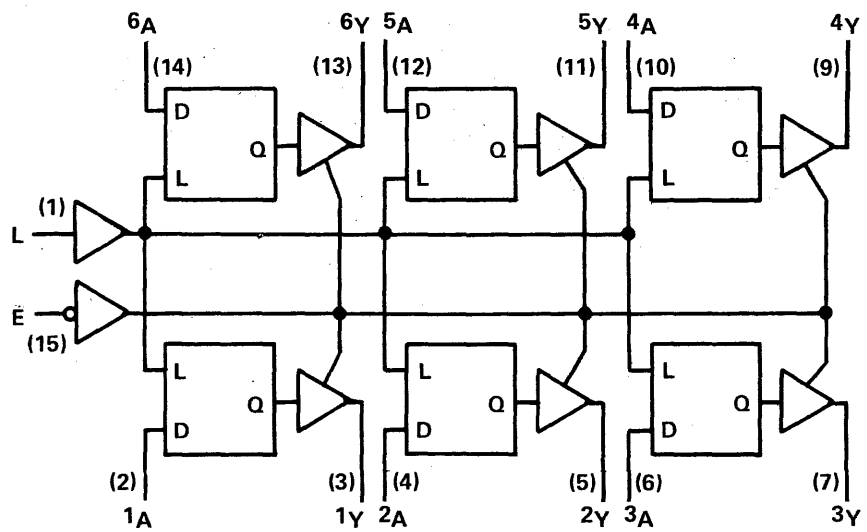
The HD-6431 is a self-aligned silicon gate CMOS Latching Three-State Bus Driver. This circuit consists of 6 non-inverting latching drivers with separate input and output. A high on the strobe line L allows data to go through the latches and a transition to low latches the data. A high on the Three-State control $\overline{E}$ forces the buffers to the high impedance mode without disturbing the latched data. New data may be latched in while the buffers are in the high impedance mode.

Truth Table

CONTROL INPUTS		DATA PORT STATUS	
$\overline{E}$	L	A	Y
H	L	X	HI-Z*
H	H	X	HI-Z
L	↓	X	*
L	H	L	L
L	H	H	H

* Data is latched to the value of the last input
X = Don't Care
HI-Z = High Impedance
↓ = Transition from High to Low level

Functional Diagram



ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+12.0V
Input or Output Voltage Applied	GND -0.3V to VCC +0.3V
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	
Industrial HD-6431A-9	-40°C to +85°C
Military HD-6431A-2	-55°C to +125°C
Operating Voltage Range	+4 to +11V

ELECTRICAL CHARACTERISTICS

V_{CC} = 10V ± 10%; T_A = Industrial or Military

D.C.

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
V_{IH}	Logical "1" Input Voltage	70% V_{CC}		V	
V_{IL}	Logical "0" Input Voltage		20% V_{CC}	V	
I_{IL}	Input Leakage	-10	10	μA	$0V \leq V_{IN} \leq V_{CC}$
V_{OH}	Logical "1" Output Voltage	V_{CC} -0.4		V	I_{OH} = -8.0mA, $\overline{E}$ = Low
V_{OL}	Logical "0" Output Voltage		0.4	V	I_{OL} = 12mA $\overline{E}$ = Low
I_O	Output Leakage	-10	10	μA	$0V \leq V_O \leq V_{CC}$, $\overline{E}$ = High
I_{CC}	Supply Current		100	μA	$V_{IN} = V_{CC}$ or GND, V_{CC} = 11V
C_{IN}	Input Capacitance*		5	pF	V_{IN} = 0V; T_A = 25°C; f = 1MHz
C_O	Output Capacitance*		15	pF	V_{IN} = 0V; T_A = 25°C; f = 1MHz

* Guaranteed and sampled, but not 100% tested.

C_L = 300pF

A.C.

		V_{CC} = 10.0V ① 25°C		V_{CC} = 10.0V ± 10% T_A = Indust. or Mil.		
SYMBOL	PARAMETER	MIN	MAX	MIN	MAX	UNITS
t_{PD}	Propagation Delay		35		45	ns
t_{EN}	Enable Time		35		45	ns
t_{DIS}	Disable Time		35		45	ns
t_{SET}	Input Set Up Time	10		10		ns
t_{HOLD}	Input Hold Time	10		10		ns
t_{PW}	Pulse Width	15		20		ns
t_R	Output Rise Time		30		40	ns
t_F	Output Fall Time		20		30	ns

NOTE ① All devices guaranteed at worst case limits. Room temperature, 10V data provided for information-not guaranteed.

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ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+8.0V
Input or Output Voltage Applied	GND -0.3V to V_{CC} +0.3V
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	
Industrial HD-6431-9	-40°C to +85°C
Military HD-6431-2	-55°C to +125°C
Operating Voltage Range	+4 to +7V

ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ± 10%; T_A = Industrial or Military

D.C.

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
V_{IH}	Logical "1" Input Voltage	70% V_{CC}		V	
V_{IL}	Logical "0" Input Voltage		20% V_{CC}	V	
I_{IL}	Input Leakage	-1.0	1.0	μA	$0V \leq V_{IN} \leq V_{CC}$
V_{OH}	Logical "1" Output Voltage	V_{CC} -0.4		V	I_{OH} = -4.0mA, $\overline{E}$ = Low
V_{OL}	Logical "0" Output Voltage		0.4	V	I_{OL} = 6.0mA $\overline{E}$ = Low
I_O	Output Leakage	-1.0	1.0	μA	$0V \leq V_O \leq V_{CC}$, $\overline{E}$ = High
I_{CC}	Supply Current		10	μA	$V_{IN} = V_{CC}$ or GND, V_{CC} = 5.5V
C_{IN}	Input Capacitance*		5	pF	V_{IN} = 0V; T_A = 25°C; f = 1MHz
C_O	Output Capacitance*		15	pF	V_{IN} = 0V; T_A = 25°C; f = 1MHz

* Guaranteed and sampled, but not 100% tested.

C_L = 300pF

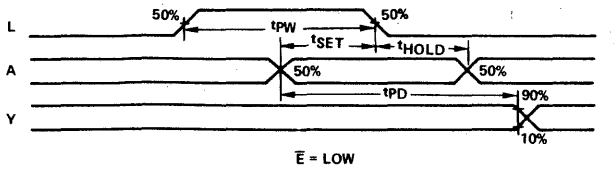
A.C.

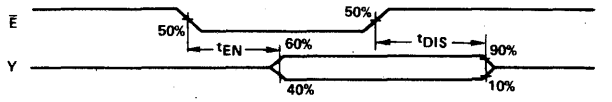
		V_{CC} = 5.0V ① 25°C		V_{CC} = 5.0V ± 10% T_A = Indus. or Mil.		
SYMBOL	PARAMETER	MIN	MAX	MIN	MAX	UNITS
t_{PD}	Propagation Delay		65		75	ns
t_{EN}	Enable Time		80		90	ns
t_{DIS}	Disable Time		80		90	ns
t_{SET}	Input Setup Time	15		15		ns
t_{HOLD}	Input Hold Time	15		15		ns
t_{PW}	Pulse Width	25		30		ns
t_R	Output Rise Time		80		90	ns
t_F	Output Fall Time		70		80	ns

NOTE ① All devices guaranteed at worst case limits. Room temperature, 5V data provided for information-not guaranteed.

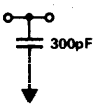
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Switching Waveforms

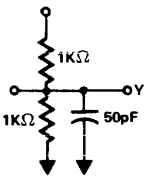




All inputs have t_R, $t_F \leq$ 20ns.



OUTPUT TEST CIRCUIT
FOR PROPAGATION DELAYS

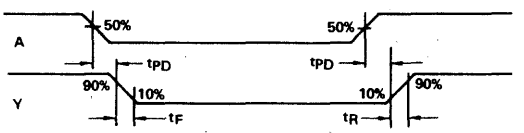


OUTPUT TEST CIRCUIT
FOR THREE-STATE DELAYS

DECOUPLING CAPACITORS

The transient current required to charge the load capacitance is given by $I_T = C\frac{dv}{dt}$. Assuming that all outputs may change state at the same time and that $\frac{dv}{dt}$ is constant; $I_T = \left(\Sigma C_L\right)\left(\frac{V_{CC} \times 80\%}{t_R \text{ or } t_F}\right)$ eg. [t_R = 80ns, V_{CC} = 5.0V, each C_L = 300pF, $I_T = (4)\left(300 \times 10^{-12}\right)\frac{5.0 \times 0.8}{80 \times 10^{-9}} = 90\text{mA.}$] This current spike may cause a large negative voltage spike on V_{CC}, which if it becomes a diode drop less than any input, may cause the device to latch up. It is recommended that a 0.1 μF ceramic disk decoupling capacitor be placed between V_{CC} and GND at each device to filter out this noise.

PROPAGATION DELAYS



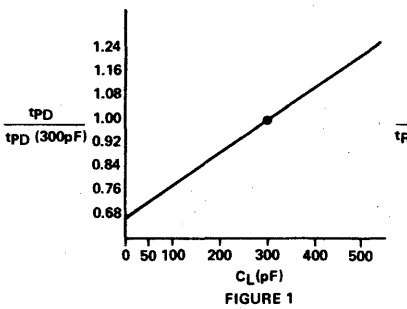


FIGURE 1

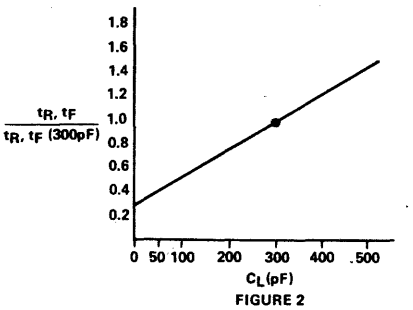


FIGURE 2

The above example will illustrate the calculation of a more useful propagation delay. The system in this example uses a 5 volt supply with a tolerance of ±10%, an ambient temperature of as high as 125°C, and a calculated load capacitance of 150pF. This application requires the HD-6431-2. The table of A.C. specs shows that t_{PD} at 4.5V and 125°C is 75nsec. Use the graph in Figure 1 to get the degradation multiple for 150pF. The number shown is 0.84. The adjusted propagation delay, to the 10% or 90% point, is therefore 75 x 0.84 or 63nsec. To obtain the rise and fall times check the A.C. specs for the rise and fall times at 4.5V and 125°C to obtain a worst case rise time of 90nsec. Use Figure 2 to find it's degradation multiple to be 0.65. The adjusted rise time is, therefore, 90 x 0.65 or 58nsec. To obtain the standard 50% to 50% propagation delay, add the adjusted propagation delay to half of the adjusted rise time to get a propagation delay of 92nsec. The rise time was used here because it is always the worst case.

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HD-6432

CMOS BI-DIRECTIONAL BUS DRIVER

Features

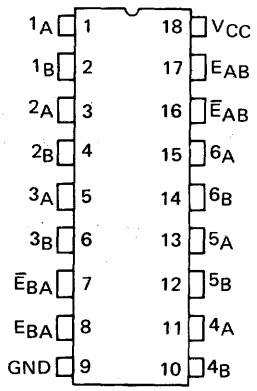
- SINGLE POWER SUPPLY
- HIGH NOISE IMMUNITY
- INDUSTRIAL AND MILITARY GRADES
- DRIVE CAPACITY. 300pF
- SOURCE CURRENT. 4mA
- SINK CURRENT 6mA
- PROPAGATION DELAY . . . . . 45nsec @ 5V

Description

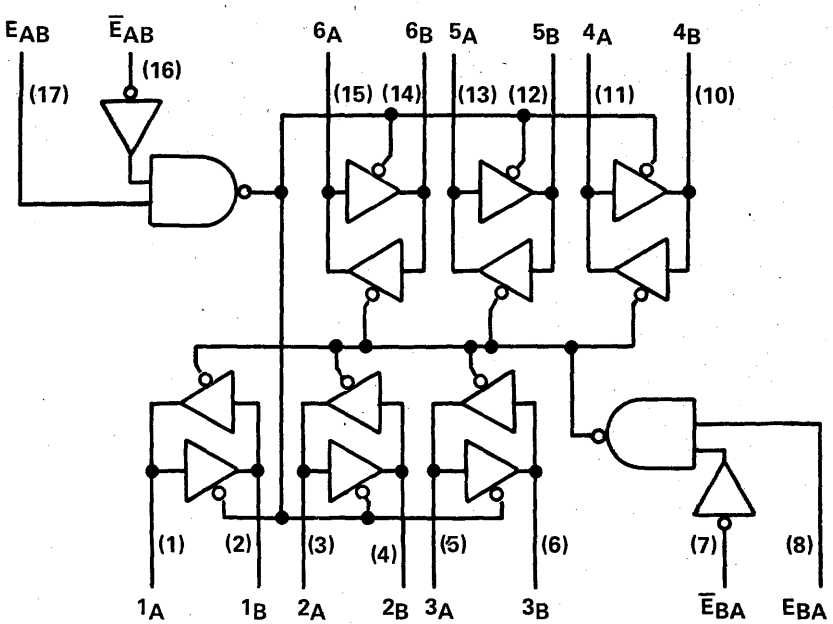
The HD-6432 is a self-aligned silicon gate CMOS bi-directional bus driver. This circuit consists of 12 drivers organized as 6 bi-directional pairs. Four enable lines select drive direction or Three-State mode.

Pinout

TOP VIEW



Functional Diagram



Truth Table

CONTROL INPUTS				DATA PORT STATUS	
E_{AB}	$\bar{E}_{AB}$	E_{BA}	$\bar{E}_{BA}$	A	B
L	X	H	L	O	I
X	H	H	L	O	I
H	L	X	H	I	O
H	L	L	X	I	O
L	X	L	X	ISOLATED	
X	H	X	H	ISOLATED	
L	X	X	H	ISOLATED	
X	H	L	X	ISOLATED	
H	L	H	L	NOT ALLOWED	

I = Input, O = Output, X = Don't Care

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ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+12.0V
Input or Output Voltage Applied	GND -0.3V to V_{CC} +0.3V
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	
Industrial HD-6432A-9	-40°C to +85°C
Military HD-6432A-2	-55°C to +125°C
Operating Voltage Range	+4 to +11V

ELECTRICAL CHARACTERISTICS

V_{CC} = 10V ± 10%; T_A = Industrial or Military

D.C.

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
V_{IH}	Logical "1" Input Voltage	70% V_{CC}		V	
V_{IL}	Logical "0" Input Voltage		20% V_{CC}	V	
I_{IL}	Input Leakage	-10	10	μA	$0V \leq V_{IN} \leq V_{CC}$
V_{OH}	Logical "1" Output Voltage	V_{CC} -0.4		V	I_{OH} = -8.0mA,
V_{OL}	Logical "0" Output Voltage		0.4	V	I_{OL} = 12mA
I_O	Output Leakage	-10	10	μA	$0V \leq V_O \leq V_{CC}$, $E_{AB} = E_{BA}$ = Low
I_{CC}	Supply Current		100	μA	$V_{IN} = V_{CC}$ or GND, V_{CC} = 11V
C_{IN}	Input Capacitance* (except I/O)		5	pF	V_{IN} = 0V; T_A = 25°C; f = 1MHz
$C_{I/O}$	I/O Capacitance*		20	pF	V_{IN} = 0V; T_A = 25°C; f = 1MHz

* Guaranteed and sampled, but not 100% tested.

C_L = 300pF

A.C.

		V_{CC} = 10.0V ① 25°C		V_{CC} = 10.0V ± 10% T_A = Indust. or Mil.		
SYMBOL	PARAMETER	MIN	MAX	MIN	MAX	UNITS
t_{PD}	Propagation Delay		35		45	ns
t_{EN}	Enable Time		40		50	ns
t_{DIS}	Disable Time		75		85	ns
t_R	Output Rise Time		40		50	ns
t_F	Output Fall Time		35		45	ns

NOTE ①: All devices guaranteed at worst case limits. Room temperature, 10V data provided for information–not guaranteed.

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ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+8.0V
Input or Output Voltage Applied	GND -0.3V to V_{CC} +0.3V
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	
Industrial HD-6432-9	-40°C to +85°C
Military HD-6432-2	-55°C to +125°C
Operating Voltage Range	+4 to +7V

ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ± 10%; T_A = Industrial or Military

D.C.

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
V_{IH}	Logical "1" Input Voltage	70% V_{CC}		V	
V_{IL}	Logical "0" Input Voltage		20% V_{CC}	V	
I_{IL}	Input Leakage	-1.0	1.0	μA	$0V \leq V_{IN} \leq V_{CC}$
V_{OH}	Logical "1" Output Voltage	V_{CC} -0.4		V	I_{OH} = -4.0mA
V_{OL}	Logical "0" Output Voltage		0.4	V	I_{OL} = 6.0mA
I_O	Output Leakage	-1.0	1.0	μA	$0V \leq V_O \leq V_{CC}$, $E_{AB} = E_{BA}$ = Low
I_{CC}	Supply Current		10	μA	$V_{IN} = V_{CC}$ or GND, V_{CC} = 5.5V
C_{IN}	Input Capacitance* (except I/O)		5	pF	V_{IN} = 0V; T_A = 25°C; f = 1MHz
$C_{I/O}$	I/O Capacitance*		20	pF	V_{IN} = 0V; T_A = 25°C; f = 1MHz

* Guaranteed and sampled, but not 100% tested.

C_L = 300pF

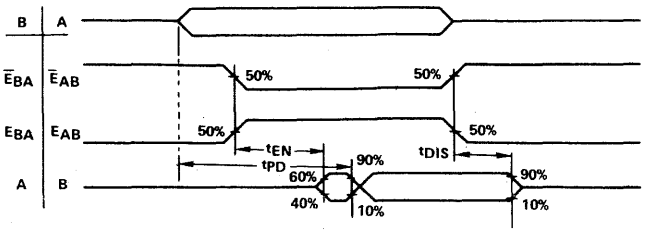
A.C.

		V_{CC} = 5.0V ① 25°C		V_{CC} = 5.0V ± 10% T_A = Indus. or Mil.		
SYMBOL	PARAMETER	MIN	MAX	MIN	MAX	UNITS
t_{PD}	Propagation Delay		45		55	ns
t_{EN}	Enable Time		65		75	ns
t_{DIS}	Disable Time		100		110	ns
t_R	Output Rise Time		100		110	ns
t_F	Output Fall Time		70		80	ns

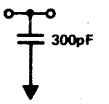
NOTE ①: All devices guaranteed at worst case limits. Room temperature, 5V data provided for information-not guaranteed.

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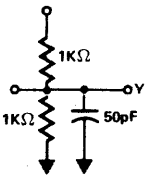
Switching Waveforms



All inputs have t_R, $t_F \leq 20$ns.



OUTPUT TEST CIRCUIT
FOR PROPAGATION DELAYS

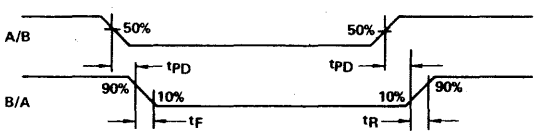


OUTPUT TEST CIRCUIT
FOR THREE-STATE DELAYS

DECOUPLING CAPACITORS

The Transient current required to charge the load capacitance is given by $I_T = C\frac{dv}{dt}$ Assuming that all outputs may change state at the same time and that $\frac{dv}{dt}$ is constant; $I_T = (\Sigma C_L)\left(\frac{V_{CC} \times 80\%}{t_R \text{ or } t_F}\right)$ eg. $\left[t_R = 100\text{ns} \quad V_{CC} = 5.0\text{V} \quad \text{each } C_L = 300\text{pF} \quad I_T = (6)(300 \times 10^{-12})\frac{5.0 \times 0.8}{100 \times 10^{-9}} = 72\text{mA.}\right]$ This current spike may cause a large negative voltage spike on V_{CC}, which if it becomes a diode drop less than any input, may cause the device to latch up. It is recommended that a 0.1 μF ceramic disk decoupling capacitor be placed between V_{CC} and GND at each device to filter out this noise.

PROPAGATION DELAYS



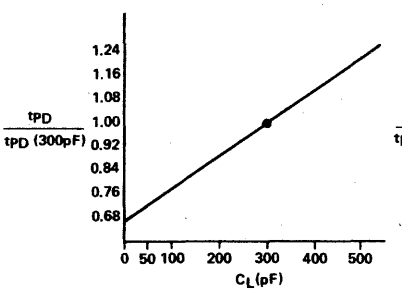


FIGURE 1

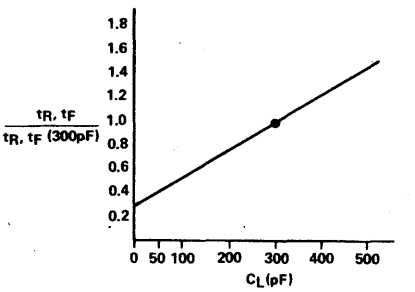


FIGURE 2

The above example will illustrate the calculation of a more useful propagation delay. The system in this example uses a 5 volt supply with a tolerance of ±10%, an ambient temperature of as high as 125°C, and a calculated load capacitance of 150pF. This application requires the HD-6432-2. The table of A.C. specs shows that t_{PD} at 4.5V and 125°C is 55nsec. Use the graph in Figure 1 to get the degradation multiple for 150pF. The number shown is 0.84. The adjusted propagation delay, to the 10% or 90% point, is therefore 55 x 0.84 or 46nsec. To obtain the rise and fall times check the A.C. specs for the rise and fall times at 4.5V and 125°C to obtain a worst case rise time of 110nsec. Use Figure 2 to find it's degradation multiple to be 0.65. The adjusted rise time is, therefore, 110 x 0.65 or 72nsec. To obtain the standard 50% to 50% propagation delay, add the adjusted propagation delay to half of the adjusted rise time to get a propagation delay of 82nsec. The rise time was used here because it is always the worst case.

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HD-6433
CMOS BUS SEPARATOR/DRIVER

Features

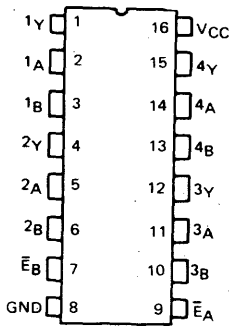
- SINGLE POWER SUPPLY
- HIGH NOISE IMMUNITY
- INDUSTRIAL AND MILITARY GRADES
- DRIVE CAPACITY. 300pF
- SOURCE CURRENT. 4mA
- SINK CURRENT 6mA
- PROPAGATION DELAY . . . . . 40nsec @ 5V

Description

The HD-6433 is a self-aligned silicon gate CMOS bus separator/driver. This circuit consists of 8 drivers organized as 4 pairs of bus separators which allow a unidirectional input bus and a unidirectional output bus to be interfaced with a bi-directional bus.

Pinout

TOP VIEW

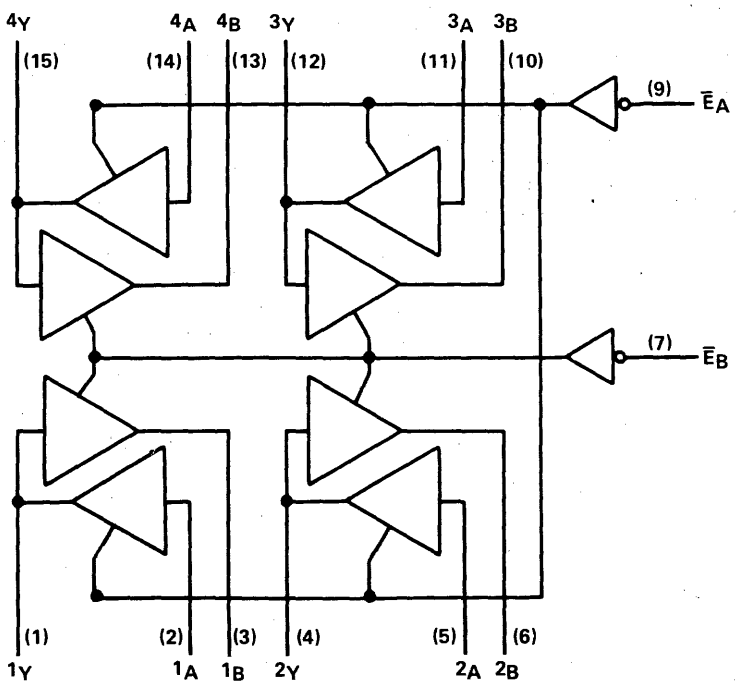


Truth Table

CONTROL INPUTS		FUNCTION		
$\bar{E}_A$	$\bar{E}_B$	A	B	Y
L	L	I	O	O
L	H	I	D	O
H	L	D	O	I
H	H	ISOLATED		

I = Input, O = Output,
D = Disconnected

Functional Diagram



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ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+12.0V
Input or Output Voltage Applied	GND -0.3V to V_{CC} +0.3V
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	
Industrial HD-6433A-9	-40°C to +85°C
Military HD-6433A-2	-55°C to +125°C
Operating Voltage Range	+4 to +11V

ELECTRICAL CHARACTERISTICS

V_{CC} = 10V ± 10%; T_A = Industrial or Military

D.C.

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
V_{IH}	Logical "1" Input Voltage	70% V_{CC}		V	
V_{IL}	Logical "0" Input Voltage		20% V_{CC}	V	
I_{IL}	Input Leakage	-10	10	μA	$0V \leq V_{IN} \leq V_{CC}$
V_{OH}	Logical "1" Output Voltage	V_{CC} -0.4		V	I_{OH} = -8.0mA
V_{OL}	Logical "0" Output Voltage		0.4	V	I_{OL} = 12mA
I_O	Output Leakage	-10	10	μA	$0V \leq V_O \leq V_{CC}$, $\overline{E}_A = \overline{E}_B$ = High
I_{CC}	Supply Current		100	μA	$V_{IN} = V_{CC}$ or GND, V_{CC} = 11V
C_{IN}	Input Capacitance* (except I/O)		5	pF	V_{IN} = 0V; T_A = 25°C; f = 1MHz
$C_{I/O}$	I/O Capacitance *		20	pF	V_{IN} = 0V; T_A = 25°C; f = 1MHz
C_O	Output Capacitance*		15	pF	V_{IN} = 0V; T_A = 25°C; f = 1MHz

* Guaranteed and sampled, but not 100% tested.

C_L = 300pF

A.C.

		V_{CC} = 10.0V ① 25°C		V_{CC} = 10.0V ± 10% T_A = Indust. or Mil.		
SYMBOL	PARAMETER	MIN	MAX	MIN	MAX	UNITS
t_{PD}	Propagation Delay		20		30	ns
t_{EN}	Enable Time		45		55	ns
t_{DIS}	Disable Time		45		55	ns
t_R	Output Rise Time		65		75	ns
t_F	Output Fall Time		55		65	ns

NOTE ① All devices guaranteed at worst case limits. Room temperature, 10V data provided for information-not guaranteed.

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ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+8.0V
Input or Output Voltage Applied	GND -0.3V to V_{CC} +0.3V
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	
Industrial HD-6433-9	-40°C to +85°C
Military HD-6433-2	-55°C to +125°C
Operating Voltage Range	+4 to +7V

ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ± 10%; T_A = Industrial or Military

D.C.

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
V_{IH}	Logical "1" Input Voltage	70% V_{CC}		V	
V_{IL}	Logical "0" Input Voltage		20% V_{CC}	V	
I_{IL}	Input Leakage	-1.0	1.0	μA	$0V \leq V_{IN} \leq V_{CC}$
V_{OH}	Logical "1" Output Voltage	V_{CC} -0.4		V	I_{OH} = -4.0mA
V_{OL}	Logical "0" Output Voltage		0.4	V	I_{OL} = 6.0mA
I_O	Output Leakage	-1.0	1.0	μA	$0V \leq V_O \leq V_{CC}$ $\overline{E}_A = \overline{E}_B$ = High
I_{CC}	Supply Current		10	μA	$V_{IN} = V_{CC}$ or GND, V_{CC} = 5.5V
C_{IN}	Input Capacitance* (except I/O)		5	pF	V_{IN} = 0V; T_A = 25°C; f = 1MHz
$C_{I/O}$	I/O Capacitance*		20	pF	V_{IN} = 0V; T_A = 25°C; f = 1MHz
C_O	Output Capacitance*		15	pF	V_{IN} = 0V; T_A = 25°C; f = 1MHz

* Guaranteed and sampled, but not 100% tested.

C_L = 300pF

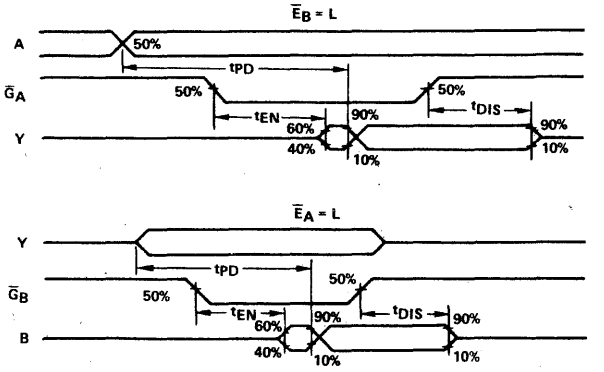
A.C.

		V_{CC} = 5.0V ① 25°C		V_{CC} = 5.0V ± 10% T_A = Indust. or Mil.		
SYMBOL	PARAMETER	MIN	MAX	MIN	MAX	UNITS
t_{PD}	Propagation Delay		40		50	ns
t_{EN}	Enable Time		60		70	ns
t_{DIS}	Disable Time		90		100	ns
t_R	Output Rise Time		85		95	ns
t_F	Output Fall Time		70		80	ns

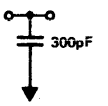
NOTE ① All devices guaranteed at worst case limits. Room temperature, 5V data provided for information-not guaranteed.

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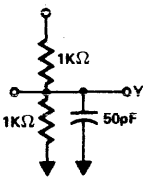
Switching Waveforms



All inputs have t_R, $t_F \leq 20$ns.



OUTPUT TEST CIRCUIT
FOR PROPAGATION DELAYS

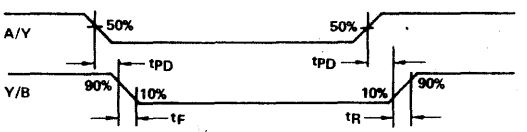


OUTPUT TEST CIRCUIT
FOR THREE-STATE DELAYS

DECOUPLING CAPACITORS

The transient current required to charge the load capacitance is given by $I_T = C\frac{dv}{dt}$. Assuming that all outputs may change state at the same time and that $\frac{dv}{dt}$ is constant; $I_T = \left(\Sigma C_L\right)\left(\frac{V_{CC} \times 80\%}{t_R \text{ or } t_F}\right)$ eg. [t_R = 85ns, V_{CC} = 5.0V, each C_L = 300pF, $I_T = (4)\left(300 \times 10^{-12}\right)\frac{5.0 \times 0.8}{85 \times 10^{-9}} = 56.5\text{mA}.$] This current spike may cause a large negative voltage spike on V_{CC}, which if it becomes a diode drop less than any input, may cause the device to latch up. It is recommended that a 0.1 μF ceramic disk decoupling capacitor be placed between V_{CC} and GND at each device to filter out this noise.

PROPAGATION DELAYS



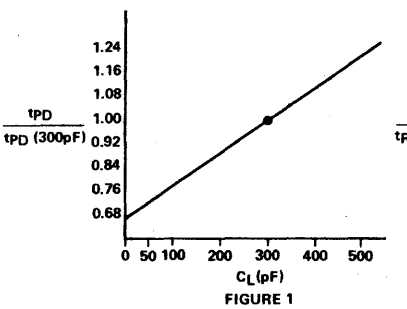


FIGURE 1

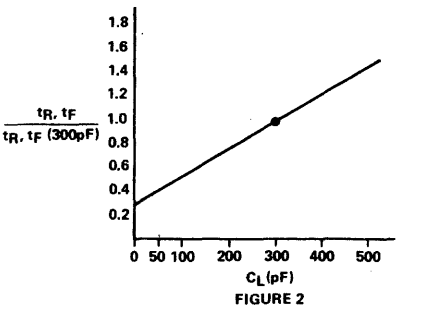


FIGURE 2

The above example will illustrate the calculation of a more useful propagation delay. The system in this example uses a 5 volt supply with a tolerance of ±10%, an ambient temperature of as high as 125°C, and a calculated load capacitance of 150pF. This application requires the HD-6433-2. The table of A.C. specs shows that t_{PD} at 4.5V and 125°C is 50nsec. Use the graph in Figure 1 to get the degradation multiple for 150pF. The number shown is 0.84. The adjusted propagation delay, to the 10% or 90% point, is therefore 50 x 0.84 or 42nsec. To obtain the rise and fall times check the A.C. specs for the rise and fall times at 4.5V and 125°C to obtain a worst case rise time of 95nsec. Use Figure 2 to find it's degradation multiple to be 0.65. The adjusted rise time is, therefore, 95 x 0.65 or 62nsec. To obtain the standard 50% to 50% propagation delay, add the adjusted propagation delay to half of the adjusted rise time to get a propagation delay of 73nsec. The rise time was used here because it is always the worst case.

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HARRIS
SEMICONDUCTOR
PRODUCTS DIVISION
A DIVISION OF HARRIS CORPORATION

HD-6440
CMOS LATCHED DECODER-DRIVER

Features

- HIGH SPEED DECODING FOR MEMORY ARRAYS
- INCORPORATES 3 ENABLE INPUTS TO SIMPLIFY EXPANSION
- LOW POWER . . . . . TYPICALLY<50 μ W @ 5V STANBDY
- HIGH NOISE IMMUNITY
- AVAILABLE IN BOTH MILITARY AND INDUSTRIAL TEMPERATURE RANGE
- HIGH CAPACITANCE DRIVE 200pF
- HIGH OUTPUT DRIVE . . . . . I_{OH} = -2mA, I_{OL} = 2.4mA
- SINGLE POWER SUPPLY

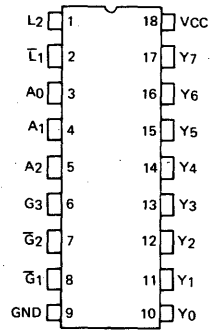
Description

The HD-6440 is a self aligned silicon gate latched decoder. One of 8 output lines is decoded, and brought to a low state, from the 3 input lines. There are two latch enables ($\overline{L_1}$, L_2), one complemented and one not, to eliminate the need for external gates. The output is enabled by three different output enables ($\overline{G_1}$, $\overline{G_2}$, G_3), two of them complemented and one not. Each output remains in a high state until it is selected, at which time it will go low.

When using high speed CMOS memories, the delay time of the HD-6440 and the enable time of the memory is usually less than the access time of the memory. This assures that memory access time will not be lengthened by the use of the HD-6440 latched decoder driver. The latch is useful for memory mapping or for systems which use a multiplexed bus.

Pinout

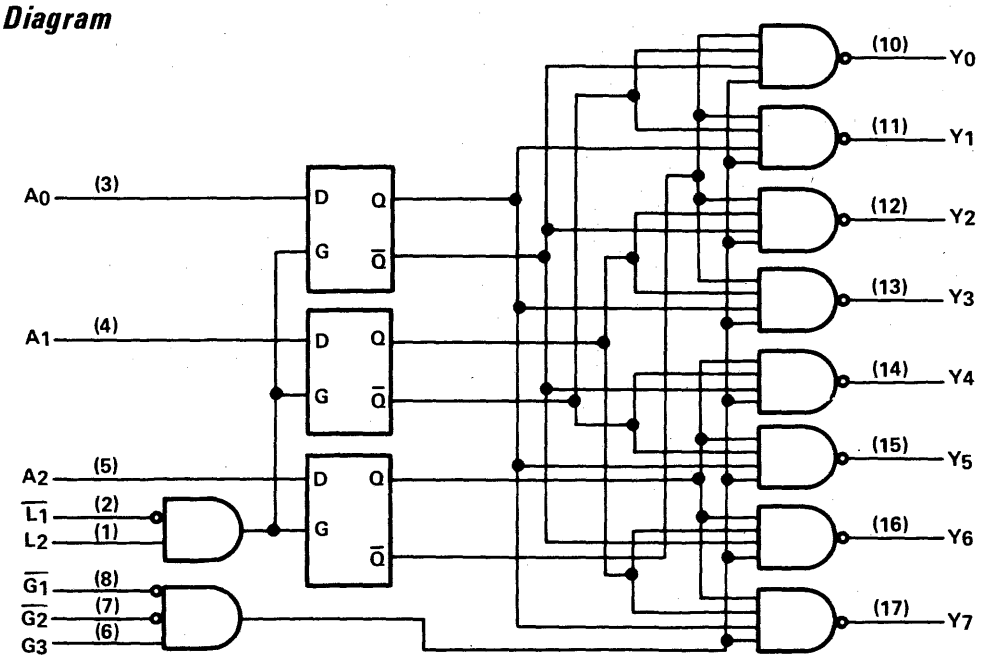
TOP VIEW



Truth Table

INPUTS							OUTPUTS								
Enable			Address												
$\overline{G_1}$	$\overline{G_2}$	G_3	$\overline{L_1}$	L_2	A_2	A_1	A_0	Y_0	Y_1	Y_2	Y_3	Y_4	Y_5	Y_6	Y_7	FUNCTION
X	X	L	X	X	X	X	X	H	H	H	H	H	H	H	H	DISABLE
X	H	X	X	X	X	X	X	H	H	H	H	H	H	H	H	
H	X	X	X	X	X	X	X	H	H	H	H	H	H	H	H	
L	L	H	L	H	L	L	L	L	H	H	H	H	H	H	H	DECODE
L	L	H	L	H	L	L	H	H	L	H	H	H	H	H	H	
L	L	H	L	H	L	H	L	H	H	L	H	H	H	H	H	
L	L	H	L	H	L	H	H	H	H	H	L	H	H	H	H	
L	L	H	L	H	H	L	L	H	H	H	H	L	H	H	H	
L	L	H	L	H	H	L	H	H	H	H	H	H	L	H	H	
L	L	H	L	H	H	H	L	H	H	H	H	H	H	L	H	
L	L	H	L	H	H	H	H	H	H	H	H	H	H	H	L	
L	L	H	X	L	X	X	X	Y_0	Y_1	Y_2	Y_3	Y_4	Y_5	Y_6	Y_7	LATCHED
L	L	H	H	X	X	X	X	Y_0	Y_1	Y_2	Y_3	Y_4	Y_5	Y_6	Y_7	

Functional Diagram



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ABSOLUTE MAXIMUM RATINGS

Supply Voltage	12.0V
Input or Output Voltage Applied	GND -0.3V to V_{CC} +0.3
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	
Industrial HD-6440A-9	-40°C to +85°C
Military HD-6440A-2	-55°C to +125°C
Operating Voltage Range	+4 to +11V

ELECTRICAL CHARACTERISTICS

V_{CC} = 10V ± 10%; T_A = Industrial or Military

D.C.

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
V_{IH}	Logical "1" Input Voltage	70% V_{CC}		V	
V_{IL}	Logical "0" Input Voltage		20% V_{CC}	V	
I_{IL}	Input Leakage	-10	10	μA	$0V \leq V_{IN} \leq V_{CC}$
V_{OH}	Logical "1" Output Voltage	V_{CC} - 0.4		V	I_{OH} = -5.0mA
V_{OL}	Logical "0" Output Voltage		0.4	V	I_{OL} = 5.0mA
I_{CC}	Supply Current		100	μA	V_{CC} = 11V
C_{IN}	Input Capacitance*		5	pF	V_{IN} = 0V; T_A = 25°C; f = 1MHz
C_O	Output Capacitance*		15	pF	V_{IN} = 0V; T_A = 25°C; f = 1MHz

* Guaranteed and sampled, but not 100% tested..

A.C.

C_L = 200pF

		V_{CC} = 10.0V ① 25°C		V_{CC} = 10.0V ± 10% T_A = Indus. or Mil.		
SYMBOL	PARAMETER	MIN	MAX	MIN	MAX	UNITS
t_{SET}	Input Setup Time	15		15		ns
t_{HOLD}	Input Hold Time	15		15		ns
t_{PD}	Propagation Delay		40		60	ns
t_{EN}	Enable Time		35		50	ns
t_{DIS}	Disable Time		35		50	ns
t_{PW}	Pulse Width	15		25		ns
t_R	Output Rise Time		45		60	ns
t_F	Output Fall Time		45		60	ns

NOTE ① All devices guaranteed at worst case limits. Room temperature, 10V data provided for information-not guaranteed.

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ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+8.0V
Input or Output Voltage Applied	GND -0.3V to V_{CC} +0.3
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	
Industrial HD-6440A-9	-40°C to +85°C
Military HD-6440A-2	-55°C to +125°C
Operating Voltage Range	+4 to +7V

ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ± 10%; T_A = Industrial or Military

D.C.

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
V_{IH}	Logical "1" Input Voltage	70% V_{CC}		V	
V_{IL}	Logical "0" Input Voltage		20% V_{CC}	V	
I_{IL}	Input Leakage	-1.0	1.0	μA	$0V \leq V_{IN} \leq V_{CC}$
V_{OH}	Logical "1" Output Voltage	V_{CC} - 0.4		V	I_{OH} = -2.4mA
V_{OL}	Logical "0" Output Voltage		0.4	V	I_{OL} = 2.4mA
I_{CC}	Supply Current		10	μA	V_{CC} = 5.5V
C_{IN}	Input Capacitance*		5	pF	V_{IN} = 0V; T_A = 25°C; f = 1MHz
C_O	Output Capacitance*		15	pF	V_{IN} = 0V; T_A = 25°C; f = 1MHz

*Guaranteed and sampled, but not 100% tested.

A.C.

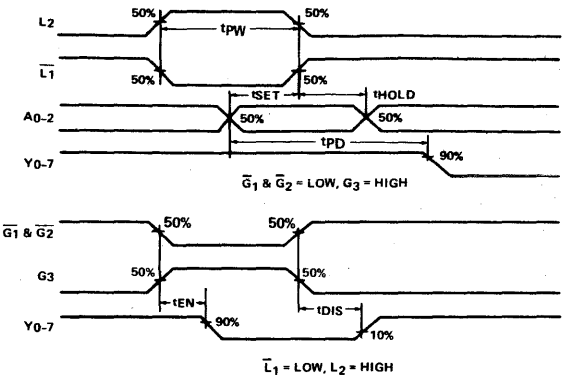
CL = 200pF

		V_{CC} = 5.0V ① 25°C		V_{CC} = 5.0V ± 10% T_A = Indust. or Mil.		
SYMBOL	PARAMETER	MIN	MAX	MIN	MAX	UNITS
t_{SET}	Input Setup Time	20		20		ns
t_{HOLD}	Input Hold Time	20		20		ns
t_{PD}	Propagation Delay		65		100	ns
t_{EN}	Enable Time		50		80	ns
t_{DIS}	Disable Time		50		90	ns
t_{PW}	Pulse Width	30		30		ns
t_R	Output Rise Time		60		90	ns
t_F	Output Fall Time		50		80	ns

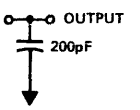
NOTE ① All devices guaranteed at worst case limits. Room temperature, 5V data provided for information–not guaranteed.

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Switching Waveforms



All Inputs have t_R, $t_F \leq 20$ns

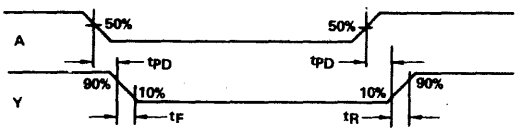


OUTPUT TEST CIRCUIT FOR PROPAGATION DELAYS

DECOUPLING CAPACITORS

The Transient current required to charge the load capacitance is given by $I_T = C\frac{dv}{dt}$. Assuming that all outputs may change state at the same time and that $\frac{dv}{dt}$ is constant; $I_T = \left(\Sigma C_L\right)\left(\frac{V_{CC} \times 80\%}{t_R \text{ or } t_F}\right)$ eg. [t_R = 60ns, V_{CC} = 5.0V, each C_L = 200pF, $I_T = (2)\ (200 \times 10^{-12})\ \frac{5.0 \times 0.8}{60 \times 10^{-9}} = 26.7$mA.] This current spike may cause a large negative voltage spike on V_{CC}, which if it becomes a diode drop less than any input, may cause the device to latch up. It is recommended that a 0.1μF ceramic disk decoupling capacitor be placed between V_{CC} and GND at each device to filter out this noise.

PROPAGATION DELAY



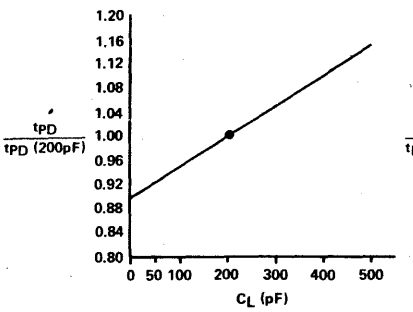


FIGURE 1

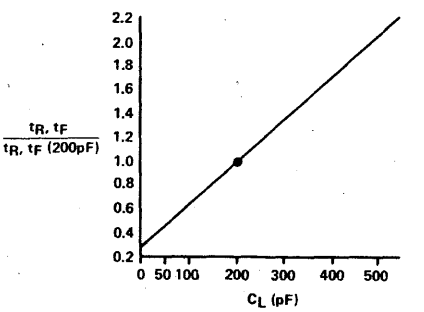


FIGURE 2

The above example will illustrate the calculation of a more useful propagation delay. The system in this example uses a 5 volt supply with a tolerance of ±10%, an ambient temperature of as high as 125°C, and a calculated load capacitance of 150pF. This application requires the HD-6440-2. The table of A.C. specs shows that t_{PD} at 4.5V and 125°C is 100nsec. Use the graph in Figure 1 to get the degradation multiple for 150pF. The number shown is 0.97. The adjusted propagation delay, to the 10% or 90% point, is therefore, 100 x 0.97 or 97nsec. To obtain the rise and fall times check the A.C. specs for the rise and fall times at 4.5V and 125°C to obtain a worst case rise time of 90nsec. Use Figure 2 to find it's degradation multiple to be 0.85. The adjusted rise time is therefore, 90 x 0.85 or 76.5nsec. To obtain the standard 50% to 50% propagation delay, add the adjusted propagation delay to half of the adjusted rise time to get a propagation delay of 135nsec. The rise time was used here because it is always the worst case.

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HD-6495

CMOS THREE-STATE BUFFER DRIVER

Features

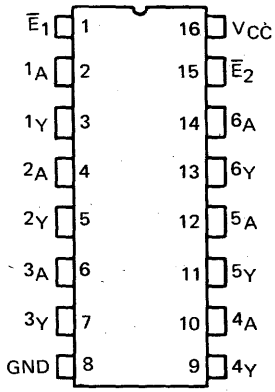
- SINGLE POWER SUPPLY
- HIGH NOISE IMMUNITY
- INDUSTRIAL AND MILITARY GRADES
- DRIVE CAPACITY 300pF
- SOURCE CURRENT 4mA
- SINK CURRENT 6mA
- PROPAGATION DELAY . . . . . 35nsec @ 5V

Description

The HD-6495 is a self aligned silicon gate CMOS Three-State buffer driver. The circuit consists of 6 non-inverting buffers with separate inputs and outputs which permit this driver to be used for bi-directional or uni-directional busing. A high on either Three-State control line $\overline{E}_1$ or $\overline{E}_2$ will force the drivers to the high impedance mode.

Pinout

TOP VIEW

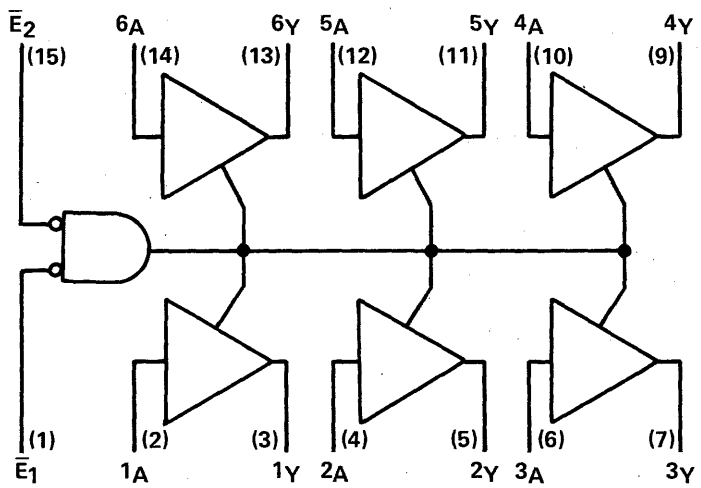


Truth Table

CONTROL INPUTS		INPUT	OUTPUT
$\overline{E}_1$	$\overline{E}_2$	A	Y
L	L	L	L
L	L	H	H
L	H	X	HI-Z
H	L	X	HI-Z
H	H	X	HI-Z

X = DON'T CARE
HI-Z = HIGH IMPEDANCE

Functional Diagram



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ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+12.0V
Input or Output Voltage Applied	GND -0.3V to V_{CC} +0.3V
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	
Industrial HD-6495A-9	-40°C to +85°C
Military HD-6495A-2	-55°C to +125°C
Operating Voltage Range	+4 to +11V

ELECTRICAL CHARACTERISTICS

V_{CC} = 10V ± 10%; T_A = Industrial or Military

D.C.

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
V_{IH}	Logical "1" Input Voltage	70% V_{CC}		V	
V_{IL}	Logical "0" Input Voltage		20% V_{CC}	V	
I_{IL}	Input Leakage	-10	10	μA	$0V \leq V_{IN} \leq V_{CC}$
V_{OH}	Logical "1" Output Voltage	V_{CC} -0.4		V	I_{OH} = -8.0mA, $\overline{E}_1 = \overline{E}_2$ = Low
V_{OL}	Logical "0" Output Voltage		0.4	V	I_{OL} = 12mA $\overline{E}_1 = \overline{E}_2$ = Low
I_O	Output Leakage	-10	10	μA	$0V \leq V_O \leq V_{CC}$, $\overline{E}_1 = \overline{E}_2$ = High
I_{CC}	Supply Current		100	μA	$V_{IN} = V_{CC}$ or GND, V_{CC} = 11V
C_{IN}	Input Capacitance*		5	pF	V_{IN} = 0V; T_A = 25°C; f = 1MHz
C_O	Output Capacitance*		15	pF	V_{IN} = 0V; T_A = 25°C; f = 1MHz

* Guaranteed and sampled, but not 100% tested.

C_L = 300pF

A.C.

		V_{CC} = 10.0V ① 25°C		V_{CC} = 10.0V ± 10% T_A = Indust. or Mil.		
SYMBOL	PARAMETER	MIN	MAX	MIN	MAX	UNITS
t_{PD}	Propagation Delay		30		40	ns
t_{EN}	Enable Time		60		70	ns
t_{DIS}	Disable Time		60		70	ns
t_R	Output Rise Time		65		75	ns
t_F	Output Fall Time		65		75	ns

NOTE ①: All devices guaranteed at worst case limits. Room temperature, 10V data provided for information–not guaranteed.

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ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+8.0V
Input or Output Voltage Applied	GND -0.3V to V_{CC} +0.3V
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	
Industrial HD-6495-9	-40°C to +85°C
Military HD-6495-2	-55°C to +125°C
Operating Voltage Range	+4 to +7V

ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ±10%; T_A = Industrial or Military

D.C.

SYMBOL	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
V_{IH}	Logical "1" Input Voltage	70% V_{CC}		V	
V_{IL}	Logical "0" Input Voltage		20% V_{CC}	V	
I_{IL}	Input Leakage	-1.0	1.0	μA	$0V \leq V_{IN} \leq V_{CC}$
V_{OH}	Logical "1" Output Voltage	V_{CC} -0.4		V	I_{OH} = -4.0mA, $\overline{E}_1 = \overline{E}_2$ = Low
V_{OL}	Logical "0" Output Voltage		0.4	V	I_{OL} = 6.0mA $\overline{E}_1 = \overline{E}_2$ = Low
I_O	Output Leakage	-1.0	1.0	μA	$0V \leq V_O \leq V_{CC}$, $\overline{E}_1 = \overline{E}_2$ = High
I_{CC}	Supply Current		10	μA	$V_{IN} = V_{CC}$ or GND, V_{CC} = 5.5V
C_{IN}	Input Capacitance*		5	pF	V_{IN} = 0V; T_A = 25°C; f = 1MHz
C_O	Output Capacitance*		15	pF	V_{IN} = 0V; T_A = 25°C; f = 1MHz

* Guaranteed and sampled, but not 100% tested.

C_L = 300pF

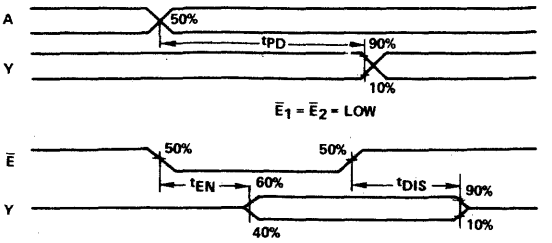
A.C.

		V_{CC} = 5.0V ① 25°C		V_{CC} = 5.0V ±10% T_A = Indus. or Mil.		
SYMBOL	PARAMETER	MIN	MAX	MIN	MAX	UNITS
t_{PD}	Propagation Delay		35		45	ns
t_{EN}	Enable Time		90		100	ns
t_{DIS}	Disable Time		90		100	ns
t_R	Output Rise Time		85		95	ns
t_F	Output Fall Time		65		75	ns

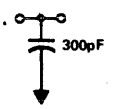
NOTE ① All devices guaranteed at worst case limits. Room temperature, 5V data provided for information–not guaranteed.

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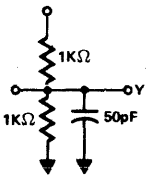
Switching Waveforms



All inputs have t_R, $t_F \leq$ 20ns.



OUTPUT TEST CIRCUIT
FOR PROPAGATION DELAYS

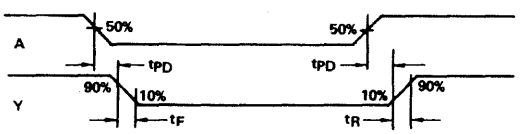


OUTPUT TEST CIRCUIT
FOR THREE-STATE DELAYS

DECOUPLING CAPACITORS

The transient current required to charge the load capacitance is given by $I_T = C\frac{dv}{dt}$. Assuming that all outputs may change state at the same time and that $\frac{dv}{dt}$ is constant; $I_T = \left(\Sigma C_L\right)\left(\frac{V_{CC} \times 80\%}{t_R \text{ or } t_F}\right)$ eg. $\left[t_R = 85ns, V_{CC} = 5.0V, \text{each } C_L = 300pF, I_T = (6)\left(300 \times 10^{-12}\right)\frac{5.0 \times 0.8}{85 \times 10^{-9}} = 84.7mA.\right]$ This current spike may cause a large negative voltage spike on V_{CC}, which if it becomes a diode drop less than any input, may cause the device to latch up. It is recommended that a 0.1 μF ceramic disk decoupling capacitor be placed between V_{CC} and GND at each device to filter out this noise.

PROPAGATION DELAYS



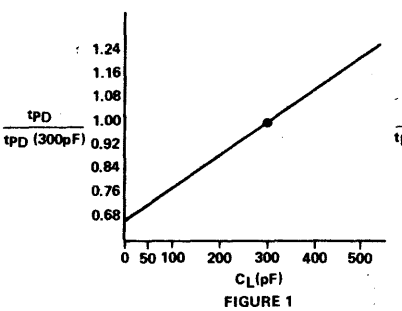


FIGURE 1

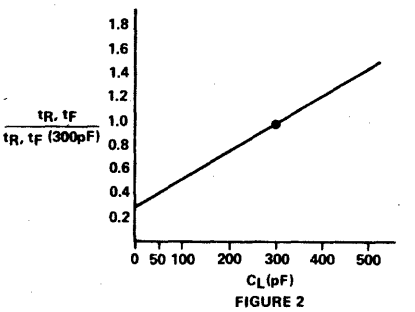


FIGURE 2

The above example will illustrate the calculation of a more useful propagation delay. The system in this example uses a 5 volt supply with a tolerance of ±10%, an ambient temperature of as high as 125°C, and a calculated load capacitance of 150pF. This application requires the HD-6495-2. The table of A.C. specs shows that t_{PD} at 4.5V and 125°C is 45nsec. Use the graph in Figure 1 to get the degradation multiple for 150pF. The number shown is 0.84. The adjusted propagation delay, to the 10% or 90% point, is therefore 45 x 0.84 or 38nsec. To obtain the rise and fall times check the A.C. specs for the rise and fall times at 4.5V and 125°C to obtain a worst case rise time of 95nsec. Use Figure 2 to find it's degradation multiple to be 0.65. The adjusted rise time is, therefore, 95 x 0.65 or 62nsec. To obtain the standard 50% to 50% propagation delay, add the adjusted propagation delay to half of the adjusted rise time to get a propagation delay of 69nsec. The rise time was used here because it is always the worst case.

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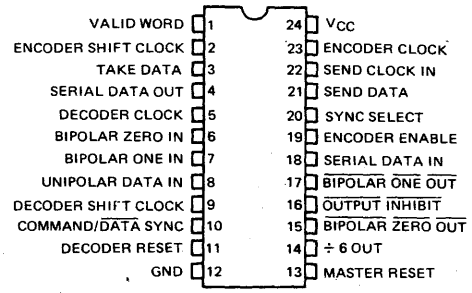
HD-15530

CMOS Manchester Encoder-Decoder

Features

- SUPPORT OF MIL-STD-1553
- 1.25 MEGABIT/SEC DATA RATE
- SYNC IDENTIFICATION AND LOCK-IN
- CLOCK RECOVERY
- MANCHESTER II ENCODE, DECODE
- SEPARATE ENCODE AND DECODE
- LOW OPERATING POWER: 50mW AT 5 VOLTS
- FULL MILITARY TEMPERATURE RANGE

Pinout



Description

The Harris HD-15530 is a high performance CMOS device intended to service the requirements of MIL-STD-1553 and similar Manchester II encoded, time division multiplexed serial data protocals. This LSI chip is divided into two sections, an Encoder and a Decoder. These sections operate completely independent of each other, except for the Master Reset function.

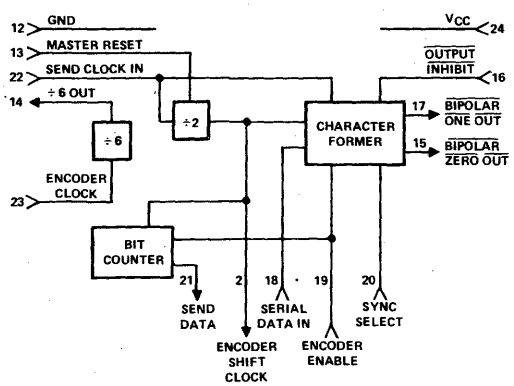
This circuit provides many of the requirements of MIL-STD-1553. The Encoder produces the sync pulse and the parity bit as well as the encoding of the data bits. The Decoder recognizes the sync pulse and identifies it as well as decoding the data bits and checking parity.

This integrated circuit is fully guaranteed to support the 1MHz data rate of MIL-STD-1553 over both temperature and voltage. It interfaces with CMOS, TTL or N channel support circuitry, and uses a standard 5 volt supply.

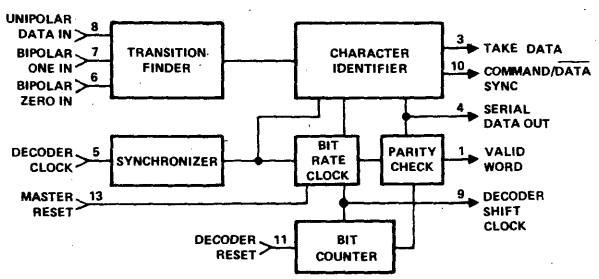
The HD-15530 could also be used in many party line digital data communications applications, such as an environmental control system driven from a single twisted pair cable or fiber optic cable throughout the building.

Block Diagrams

ENCODER



DECODER



Specifications HD-15530

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+7.0V
Input or Output Voltage Applied	GND -0.3V to V_{CC} +3.0V
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	
Industrial HD-15530-9	-40°C to +85°C
Military HD-15530-2	-55°C to +125°C

ELECTRICAL CHARACTERISTICS V_{CC} = 5.0V ±5% T_A = Industrial or Military

	SYMBOL	PARAMETER	MINIMUM	TYPICAL	MAXIMUM	UNITS	TEST CONDITIONS
D.C.	V_{IH}	Logical "1" Input Voltage	70% V_{CC}			V	
	V_{IL}	Logical "0" Input Voltage			20% V_{CC}	V	
	V_{IHC}	Logical "1" Input Voltage (Clock)	V_{CC} -0.5			V	
	V_{ILC}	Logical "0" Input Voltage (Clock)			GND +0.5	V	
	I_{IL}	Input Leakage	-1.0		+1.0	µA	$0V \leqslant V_{IN} \leqslant V_{CC}$
	V_{OH}	Logical "1" Output Voltage	2.4			V	I_{OH} = -3mA
	V_{OL}	Logical "0" Output Voltage			0.4	V	I_{OL} = 1.8mA
	I_{CCSB}	Supply Current Standby		0.5	2	mA	$V_{IN} = V_{CC}$ = 5.25V Outputs Open
	I_{CCOP}	Supply Current Operating*		8.0	10.0	mA	V_{CC} = 5.25V, f = 1MHz
	C_{IN}	Input Capacitance*		5.0	7.0	pF	
	C_O	Output Capacitance*		8.0	10.0	pF	
		*Guaranteed and sampled but not 100% tested.					
ENCODER TIMING V_{CC} = 5.0V ±5% T_A = Industrial or Military							
A.C.	F_{EC}	Encoder Clock Frequency			15	MHz	C_L = 50pF
	F_{ESC}	Send Clock Frequency			2.5	MHz	
	T_{ECR}	Encoder Clock Rise Time			8	ns	
	T_{ECF}	Encoder Clock Fall Time			8	ns	
	F_{ED}	Data Rate			1.25	MHz	
	T_{MR}	Master Reset Pulse Width	150			ns	
	T_{E1}	Shift Clock Delay			125	ns	
	T_{E2}	Serial Data Setup	75			ns	
	T_{E3}	Serial Data Hold	75			ns	
	T_{E4}	Enable Setup	90			ns	
	T_{E5}	Enable Pulse Width	80			ns	
	T_{E6}	Sync Setup	55			ns	
	T_{E7}	Sync Pulse Width	150			ns	
	T_{E8}	Send Data Delay			50	ns	
	T_{E9}	Bipolar Output Delay			130	ns	
DECODER TIMING V_{CC} = 5.0V ±5% T_A = Industrial or Military							
A.C.	F_{DC}	Decoder Clock Frequency			15	MHz	C_L = 50pF
	T_{DCR}	Decoder Clock Rise Time			8	ns	
	T_{DCF}	Decoder Clock Fall Time			8	ns	
	F_{DD}	Data Rate			1.25	MHz	
	T_{DR}	Decoder Reset Pulse Width	150			ns	
	T_{DRS}	Decoder Reset Setup Time	75			ns	
	T_{MR}	Master Reset Pulse Width	150			ns	
	T_{D1}	Bipolar Data Pulse Width	T_{DC} +10			ns	①
	T_{D2}	Sync Transition Span		18T_{DC}		ns	①
	T_{D3}	One Zero Overlap			T_{DC} -10	ns	①
	T_{D4}	Short Data Transition Span		6T_{DC}		ns	①
	T_{D5}	Long Data Transition Span		12T_{DC}		ns	①
	T_{D6}	Sync Delay (ON)		40	110	ns	
	T_{D7}	Take Data Delay (ON)		50	110	ns	
	T_{D8}	Serial Data Out Delay		80	80	ns	
	T_{D9}	Sync Delay (OFF)		90	110	ns	
	T_{D10}	Take Data Delay (OFF)		110	110	ns	
	T_{D11}	Valid Word Delay		90	110	ns	

NOTE ①: $15T_{DC} + 10 = [15 \text{ (Decoder Clock Period)}] + 10ns$ T_{DC} = Decoder Clock Period = $\frac{1}{F_{DC}}$

These parameters are guaranteed but not 100% tested.

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Pin Assignments

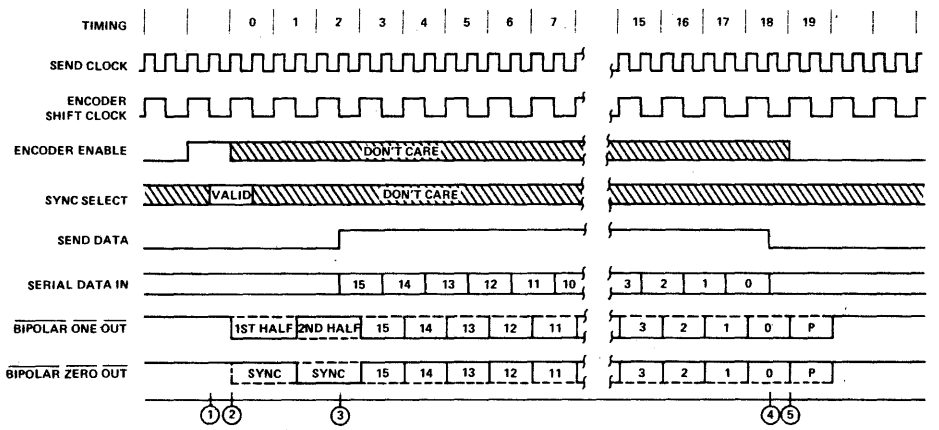
PIN	SECTION	NAME	DESCRIPTION
1	Decoder	VALID WORD	Output high indicates receipt of a valid word.
2	Encoder	ENCODER SHIFT CLOCK	Output for shifting data into the Encoder. This clock shifts data on a low-to-high transition.
3	Decoder	TAKE DATA	Output is high during receipt of data after identification fo a sync pulse.
4	Decoder	SERIAL DATA OUT	Delivers received data in correct NRZ format.
5	Decoder	DECODER CLOCK	Input drives the transition finder, and the synchronizer which in turn supplies the clock to the balance of the Decoder.
6	Decoder	BIPOLAR ZERO IN	A high input should be applied when the bus is in its negative state. This pin must be held high when the Unipolar input is used.
7	Decoder	BIPOLAR ONE IN	A high input should be applied when the bus is in its positive state, this pin must be held low when the Unipolar input is used.
8	Decoder	UNIPOLAR DATA IN	With pin 6 high and pin 7 low, this pin enters unipolar data into the transition finder circuit. If not used this input must be held low.
9	Decoder	DECODER SHIFT CLOCK	Output which delivers a frequency (Decoder Clock ÷ 12), synchronized by the recovered serial data stream.
10	Decoder	COMMAND SYNC	Output of a high from this pin occurs during output of decoded data which was preceded by a Command (or Status) synchronizing character. A low output indicates a Data synchronizing character.
11	Decoder	DECODER RESET	A high input to this pin during a rising edge of DECODER SHIFT CLOCK resets the decoder bit counting logic to a condition ready for a new word.
12	Both	GROUND	Ground supply pin.
13	Both	MASTER RESET	A high on this pin clears 2:1 counters in both the Encoder and Decoder.
14	Encoder	÷ 6 OUT	Output from 6:1 divider which is driven by the ENCODER CLOCK.
15	Encoder	$\overline{\text{BIPOLAR ZERO OUT}}$	An active low output designed to drive the zero or negative sense of a bipolar line driver.
16	Encoder	$\overline{\text{OUTPUT INHIBIT}}$	A low on this input forces pin 15 and pin 17 high, the inactive states.
17	Encoder	$\overline{\text{BIPOLAR ONE OUT}}$	An active low output designed to drive the one or positive sense of a bipolar line driver.
18	Encoder	SERIAL DATA IN	Accepts a serial data stream at a data rate equal to ENCODER SHIFT CLOCK.
19	Encoder	ENCODER ENABLE	A high on this input initiates the encode cycle. (Subject to the preceding cycle being complete.)
20	Encoder	SYNC SELECT	Actuates command sync for an input high and data sync for an input low.
21	Encoder	SEND DATA	Is an active high output which enables the external source of serial data.
22	Encoder	SEND CLOCK IN	Clock input at a frequency equal to the data rate X2.
23	Encoder	ENCODER	Input to the 6:1 divider.
24	Both	V_{CC}	Positive supply pin.

Encoder Operation

The Encoder requires a single clock with a frequency of twice the desired data rate applied at the SEND CLOCK input. An auxillary divide by six counter is provided on chip which can be utilized to produce the SEND CLOCK by dividing the DECODER CLOCK.

The Encoder's cycle begins when ENCODER ENABLE is high during a falling edge of ENCODER SHIFT CLOCK ①. This cycle lasts for one word length or twenty ENCODER SHIFT CLOCK periods. At the next low-to-high transition of the ENCODER SHIFT CLOCK, a high at SYNC SELECT input actuates a command sync or a low will produce a data sync for that word ② . When the Encoder is ready to accept data, the SEND DATA output will go high and remain high for sixteen ENCODER SHIFT CLOCK periods ③ . During these sixteen periods the data should be clocked into the SERIAL DATA input with every low-to-high transition of the ENCODER SHIFT CLOCK ③ – ④ . After the sync and the Manchester II coded data are transmitted through the $\overline{\text{BIPOLAR ONE}}$ and $\overline{\text{BIPOLAR ZERO}}$ outputs, the Encoder adds on an additional bit which is the parity for that word ⑤ . At any time a low on $\overline{\text{OUTPUT INHIBIT}}$ input will force both bipolar outputs to a high state but will not affect the Encoder in any other way.

To abort the Encoder transmission a positive pulse must be applied at MASTER RESET. Anytime after or during this pulse, a low to high transition on SEND CLOCK clears the internal counters and initializes the Encoder for a new word.



Decoder Operation

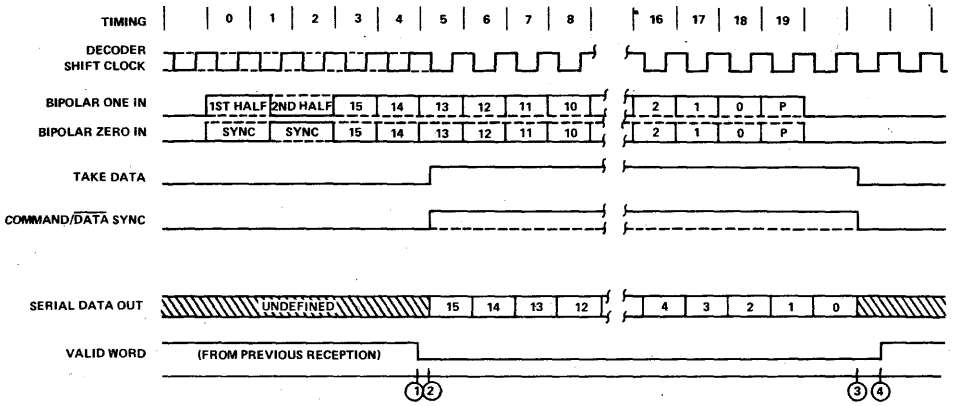
The Decoder requires a single clock with a frequency of 12 times the desired data rate applied at the DECODER CLOCK input. The Manchester II coded data can be presented to the Decoder in one of two ways. The BIPOLAR ONE and BIPOLAR ZERO inputs will accept data from a comparator sensed transformer coupled bus as specified in Military Spec 1553. The UNIPOLAR DATA input can only accept non-inverted Manchester II coded data. (e.g. from $\overline{\text{BIPOLAR ZERO OUT}}$ of an Encoder.)

The Decoder is free running and continuously monitors its data input lines for a valid sync character and two valid Manchester data bits to start an output cycle. When a valid sync is recognized ① , the type of sync is indicated on COMMAND/$\overline{\text{DATA}}$ SYNC output. If the sync character was a command sync, this output will go high ② and remain high for sixteen DECODER SHIFT CLOCK periods ③ , otherwise it will remain low. The TAKE DATA output will go high and remain high ② – ③ while the Decoder is transmitting the decoded data through SERIAL DATA OUT. The decoded data available at SERIAL DATA OUT is in a NRZ format. The DECODER SHIFT CLOCK is provided so that the decoded bits can get shifted into an external register on every low-to-high transition of this clock ② – ③ .

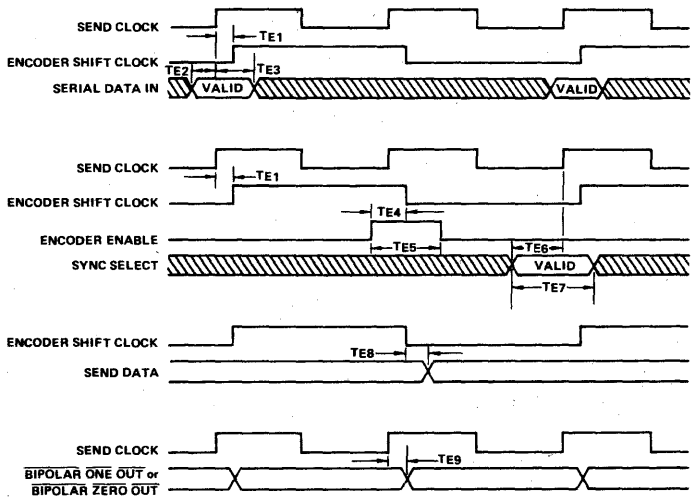
After all sixteen decoded bits have been transmitted ③ the data is checked for odd parity. A high on VALID WORD output ④ indicates a successful reception of a word without any Manchester or parity errors. At this time the Decoder is looking for a new sync character to start another output sequence.

At any time in the above sequence a high input on DECODER RESET during a low-to-high transition of DECODER SHIFT CLOCK will abort transmission and initialize the Decoder to start looking for a new sync character.

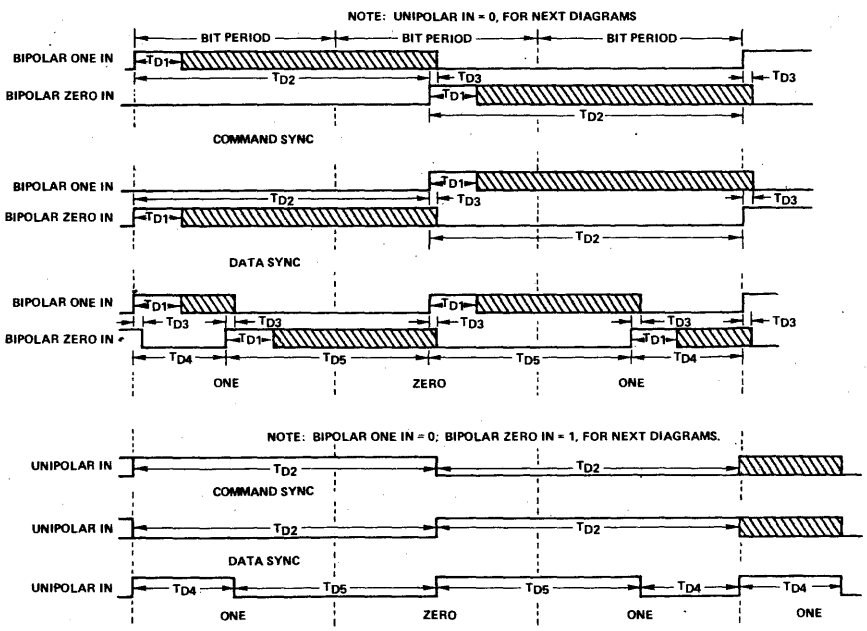
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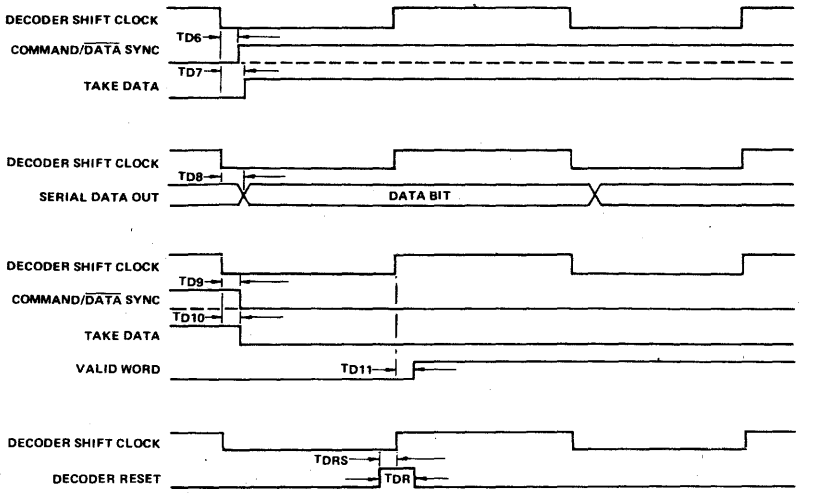
Encoder Timing



Decoder Timing

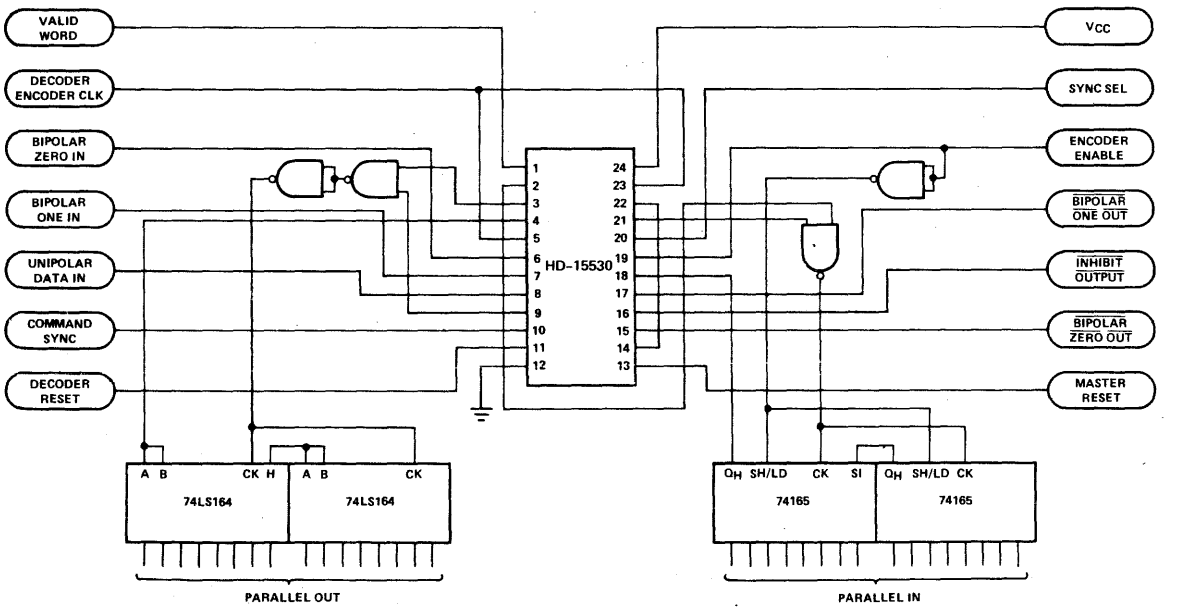


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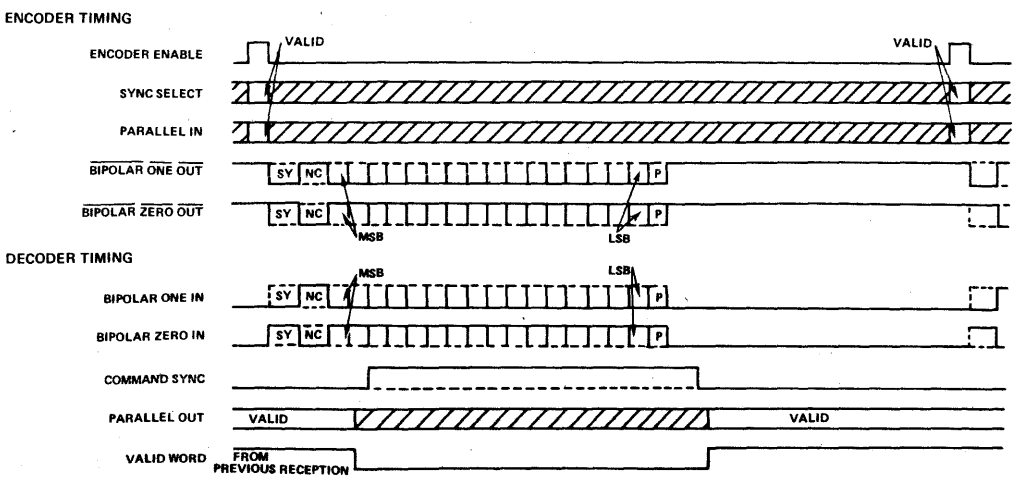


Applications

How to Make Our MTU Look Like a Manchester Encoded UART



Typical Timing Diagrams for a Manchester Encoded UART



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The 1553A standard defines a time division multiplexed data bus for application within aircraft. The bus is defined to be bipolar, and encoded in a Manchester II format, so no DC component appears on the bus. This allows transformer coupling and excellent isolation among systems and their environment.

The HD-15531 supports the full bipolar configuration, assuming a bus driver configuration similar to that in Figure 1. Bipolar inputs from the bus, like Figure 2, are also accommodated.

The signaling format in MIL-STD-1553A is specified on the assumption that the network of 32 or fewer terminals are controlled by a central control unit by means of Command Words, and Data. Terminals respond with Status Words, and Data. Each word is preceded by a synchronizing pulse, and followed by parity bit, occupying a total of 20 μ sec. The word formats are shown in Figure 4. The special abbreviations are as follows:

P	Parity, which is defined to be odd, taken across all 17 bits.
R/T	Receive on logical zero, transmit on ONE.
ME	Message Error if logical 1.
TF	Terminal Flag, if set, calls for controller to request self-test data.

The paragraphs above are intended only to suggest the content of MIL-STD-1553A, and do not completely describe its bus requirements, timing or protocols.

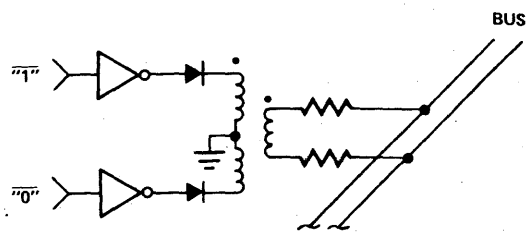


FIGURE 1 – Simplified MIL-STD-1533 Driver

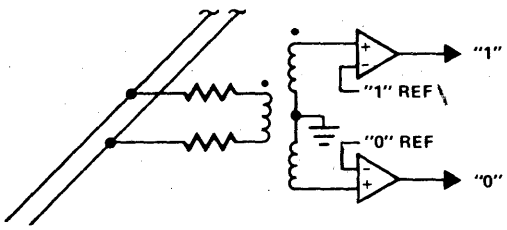


FIGURE 2 – Simplified MIL-STD-1553 Receiver

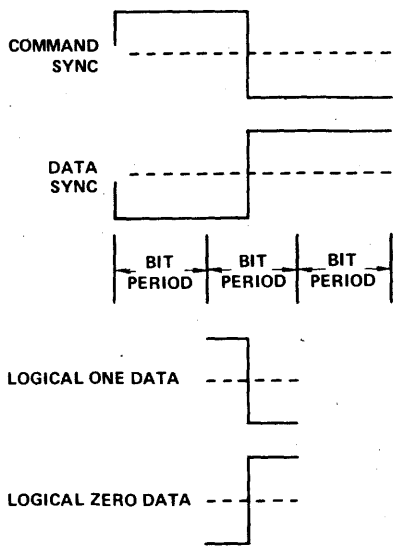


FIGURE 3 – MIL-STD-1553 Character Formats

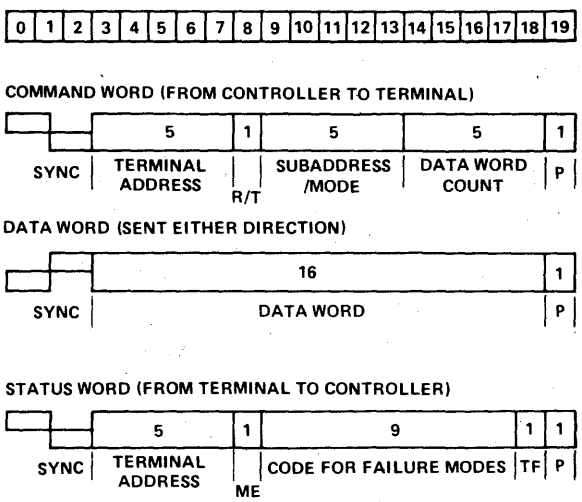


FIGURE 4 – MIL-STD-1553 Word Formats

NOTE: This page is a summary of MIL-STD-1553A and is not intended to describe the operation of the HD-15530.

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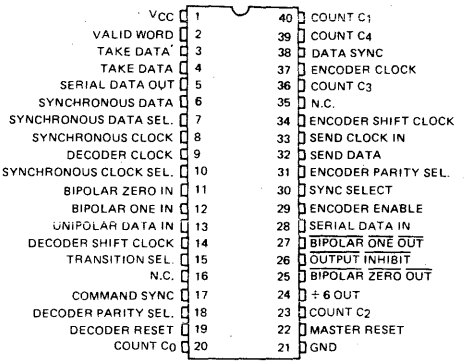
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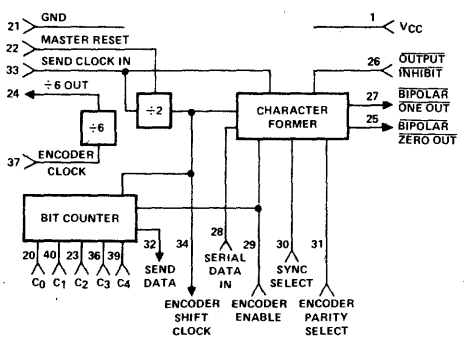
The HD-15531 also surpasses the requirements of MIL-STD-1553 by allowing the frame length to be programmable. The frame length may be programmed from 2 to 28 data bits plus sync and parity. This chip also allows selection of either even or odd parity for the Encoder and Decoder separately.

This integrated circuit is fully guaranteed to support the 1MHz data rate of MIL-STD-1553 over both temperature and voltage. It interfaces with CMOS, TTL or N channel support circuitry, and uses a standard 5 volt supply.

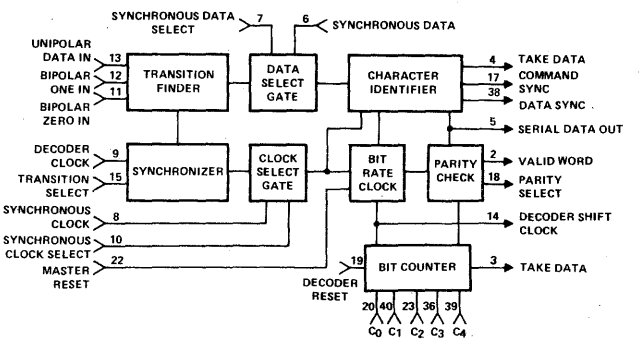
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Block Diagrams

ENCODER



DECODER



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P	Parity, which is defined to be odd, taken across all 17 bits.
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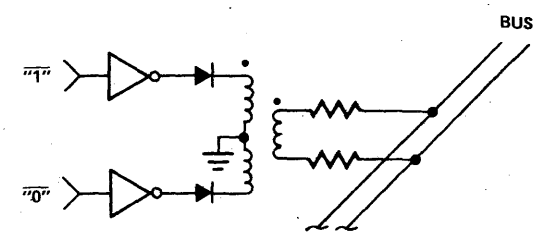


FIGURE 1 – Simplified MIL-STD-1533 Driver

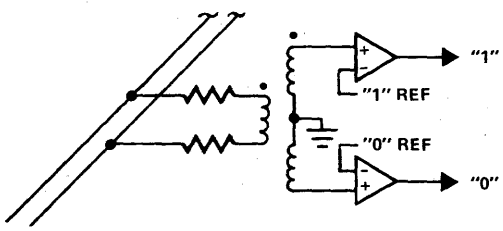


FIGURE 2 – Simplified MIL-STD-1553 Receiver

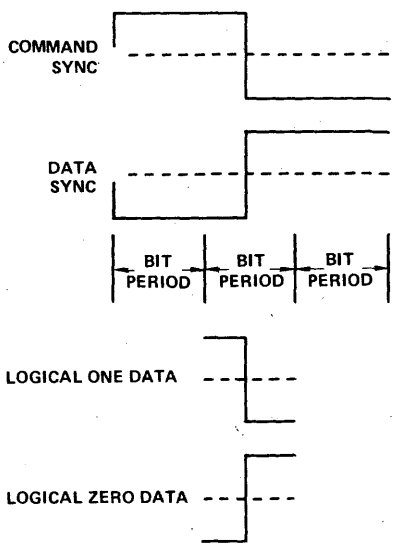


FIGURE 3 – MIL-STD-1553 Character Formats

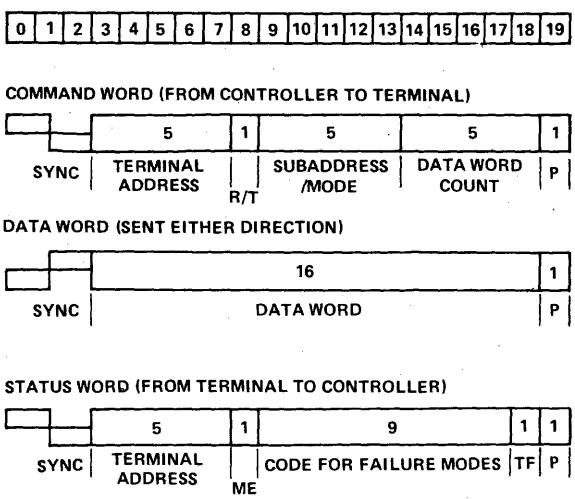


FIGURE 4 – MIL-STD-1553 Word Formats

NOTE: This page is a summary of MIL-STD-1553A and is not intended to describe the operation of the HD-15531.

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Specifications HD-15531

ABSOLUTE MAXUMUM RATINGS

Supply Voltage	+7.0V
Input or Output Voltage Applied	GND -0.3V to VCC +0.3V
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	
Industrial HD-15531-9	-40°C to +85°C
Military HD-15531-2	-55°C to +125°C

ELECTRICAL CHARACTERISTICS V_{CC} = 5.0V ±5% T_A = Industrial or Military

	SYMBOL	PARAMETER	MINIMUM	TYPICAL	MAXIMUM	UNITS	TEST CONDITIONS
D.C.	VIH	Logical "1" Input Voltage	70% VCC			V	
	VIL	Logical "0" Input Voltage			20% VCC	V	
	VIHC	Logical "1" Input Voltage (Clock)	VCC -0.5			V	
	VILC	Logical "0" Input Voltage (Clock)			GND +0.5	V	
	IIL	Input Leakage	-1.0		+1.0	µA	0V ≤ VIN ≤ VCC
	VOH	Logical "1" Output Voltage	2.4			V	IOH = -3mA
	VOL	Logical "0" Output Voltage			0.4	V	IOL = 1.8mA
	ICCSB	Supply Current Standby		0.5	2.0	mA	VIN = VCC = 5.25V Outputs Open
	ICCOP	Supply Current Operating*		8.0	10.0	mA	VCC = 5.25V, f = 15MHz
	CIN	Input Capacitance*		5.0	7.0	pF	
	CO	Output Capacitance*		8.0	10.0	pF	

*Guaranteed and sampled but not 100% tested.

	ENCODER TIMING						
A.C.	FEC	Encoder Clock Frequency			15	MHz	CL = 50pF
	FESC	Send Clock Frequency			2.5	MHz	
	TECR	Encoder Clock Rise Time			8	ns	
	TECF	Encoder Clock Fall Time			8	ns	
	FED	Data Rate			1.25	MHz	
	TMR	Master Reset Pulse Width	150			ns	
	TE1	Shift Clock Delay			125	ns	
	TE2	Serial Data Setup	75			ns	
	TE3	Serial Data Hold	75			ns	
	TE4	Enable Setup	90			ns	
	TE5	Enable Pulse Width	80			ns	
	TE6	Sync Setup	55			ns	
	TE7	Sync Pulse Width	150			ns	
	TE8	Send Data Delay			50	ns	
	TE9	Bipolar Output Delay			130	ns	

	DECODER TIMING						
A.C.	FDC	Decoder Clock Frequency			15	MHz	CL = 50pF
	FDS	Decoder Synchronous Clock			2.5	MHz	
	TDCR	Decoder Clock Rise Time			8	ns	
	TDCF	Decoder Clock Fall Time			8	ns	
	FDD	Data Rate			1.25	MHz	
	TDR	Decoder Reset Pulse Width	150			ns	
	TDRS	Decoder Reset Setup Time	75			ns	
	TMR	Master Reset Pulse Width	150			ns	
	TD1	Bipolar Data Pulse Width	TDC +10			ns	①
	TD2	Sync Transition Span		18TDC		ns	①
	TD3	One Zero Overlap			TDC -10	ns	①
	TD4	Short Data Transition Span		6TDC		ns	①
	TD5	Long Data Transition Span		12TDC		ns	①
	TD6	Sync Delay (ON)			110	ns	
	TD7	Take Data Delay (ON)			110	ns	
	TD8	Serial Data Out Delay			80	ns	
	TD9	Sync Delay (OFF)			110	ns	
	TD10	Take Data Delay (OFF)			110	ns	
	TD11	Valid Word Delay			110	ns	
	TD12	Synchronous Clock To Shift Clock Delay			75	ns	
	TD13	Synchronous Data Setup	30			ns	

NOTE ①: $15T_{DC} + 10 = [15 \text{ (Decoder Clock Period)}] + 10ns$ T_{DC} = Decoder Clock Period = $\frac{1}{F_{DC}}$

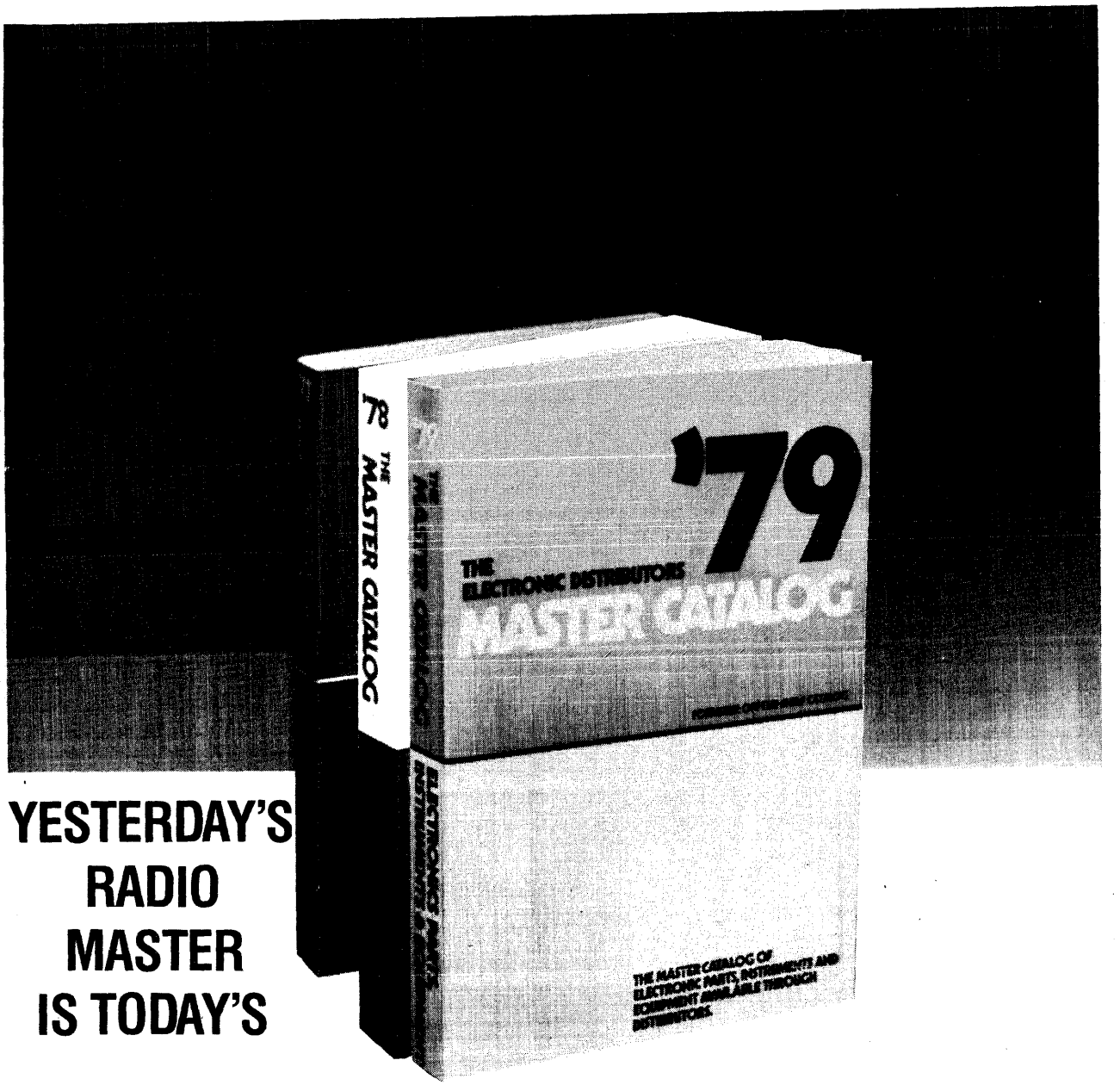
These parameters are guaranteed but not 100% tested.

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Pin Assignments

PIN	SECTION	NAME	DESCRIPTION
1	Both	VCC	Positive supply pin.
2	Decoder	VALID WORD	Output high indicates receipt of a valid word.
3	Decoder	TAKE DATA'	A continuous, free running signal provided for host timing or data handling. When data is present on the bus, this signal will be synchronized to the incoming data and will be identical to take data.
4	Decoder	TAKE DATA	Output is high during receipt of data after identification of a sync pulse
5	Decoder	SERIAL DATA OUT	Delivers received data in correct NRZ format.
6	Decoder	SYNCHRONOUS DATA	Input presents Manchester data directly to character identification logic. SYNCHRONOUS DATA SELECT must be held high to use this input. If not used this pin should be held high.
7	Decoder	SYNCHRONOUS DATA SELECT	In high state allows the synchronous data to enter the character identification logic.
8	Decoder	SYNCHRONOUS CLOCK	Input provides externally synchronized clock to the decoder.
9	Decoder	DECODER CLOCK	Input drives the transition finder, and the synchronizer which in turn supplies the clock to the balance of the decoder.
10	Decoder	SYNCHRONOUS CLOCK SELECT	In high state directs the SYNCHRONOUS CLOCK to control the decoder character identification logic. A low state selects the DECODER CLOCK
11	Decoder	BIPOLAR ZERO IN	A high input should be applied when the bus is in its negative state. This pin must be held high when the unipolar input is used.
12	Decoder	BIPOLAR ONE IN	A high input should be applied when the bus is in its positive state. This pin must be held low when the unipolar input is used.
13	Decoder	UNIPOLAR DATA IN	With pin 11 high and pin 12 low, this pin enters unipolar data into the transition finder circuit. If not used this input must be held low.
14	Decoder	DECODER SHIFT CLOCK	Output which delivers a frequency (DECODER CLOCK ÷ 12), synchronized by the recovered serial data stream.
15	Decoder	TRANSITION SELECT	A high input to this pin causes the transition finder to synchronize on every transition of input data. A low input causes the transition finder to synchronize only on mid-bit transitions.
16	Blank	N.C.	Not connected.
17	Decoder	COMMAND SYNC	Output of a high from this pin occurs during output of decoded data which was preceded by a Command (or Status) synchronizing character
18	Decoder	DECODER PARITY SELECT	An input for parity sense, calling for even parity with input high and odd parity with input low.
19	Decoder	DECODER RESET	A high input to this pin during a rising edge of DECODER SHIFT CLOCK resets the decoder bit counting logic to a condition ready for a new word.
20	Both	COUNT C_0	One of five binary inputs which establish the total bit count to be encoded or decoded.
21	Both	GROUND	Supply pin.
22	Both	MASTER RESET	A high on this pin clears 2:1 counters in both the encoder and decoder.
23	Both	COUNT C_2	See pin 20.
24	Encoder	÷ 6 OUT	Output from 6:1 divider which is driven by the ENCODER CLOCK.
25	Encoder	$\overline{\text{BIPOLAR ZERO OUT}}$	An active low output designed to drive the zero or negative sense of a bipolar line driver.
26	Encoder	$\overline{\text{OUTPUT INHIBIT}}$	A low on this pin forces pin 25 and 27 high, the inactive states.
27	Encoder	$\overline{\text{BIPOLAR ONE OUT}}$	An active low output designed to drive the one or positive sense of a bipolar line driver.
28	Encoder	SERIAL DATA IN	Accepts a serial data stream at a data rate equal to ENCODER SHIFT CLOCK.
29	Encoder	ENCODER ENABLE	A high on this pin initiates the encode cycle. (Subject to the preceeding cycle being complete.)
30	Encoder	SYNC SELECT	Actuates a Command sync for an input high and Data sync for an input low.
31	Encoder	ENCODER PARITY SELECT	Sets transmit parity odd for a high input, even for a low input.
32	Encoder	SEND DATA	Is an active high output which enables the external source of serial data
33	Encoder	SEND CLOCK IN	Clock input at a frequency equal to the data rate X2.
34	Encoder	ENCODER SHIFT CLOCK	Output for shifting data into the Encoder. This shift clock shifts data on a low-to-high transition.
35	Blank	N.C.	Not connected.
36	Both	COUNT C_3	See pin 20.
37	Encoder	ENCODER CLOCK	Input to the 6:1 divider.
38	Decoder	DATA SYNC	Output of a high from this pin occurs during output of decoded data which was preceded by a Data synchronizing character.
39	Both	COUNT C_4	See pin 20.
40	Both	COUNT C_1	See pin 20.

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MICRO POWER SYSTEMS

CMOS 12-Bit Monolithic Multiplying DAC

MP7621/7541

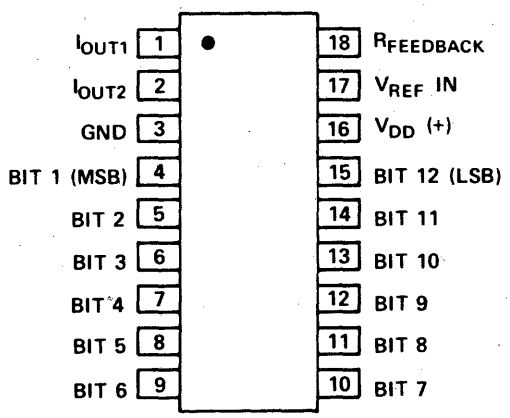
FEATURES

- 12-Bit Linearity (0.01%), achieved *without trimming* of ladder Rs
- Full Four-Quadrant Multiplication
- 2 ppm/°C Gain Error Tempco
- Plug-In Replacement For AD7541
- TTL/CMOS Compatible
- Low Power Consumption
- Low Feedthrough Error
- Low Cost

APPLICATIONS

Digital/Synchro Conversion
Programmable Amplifiers
Ratiometric A/D Conversion
Function Generation

PIN CONFIGURATION



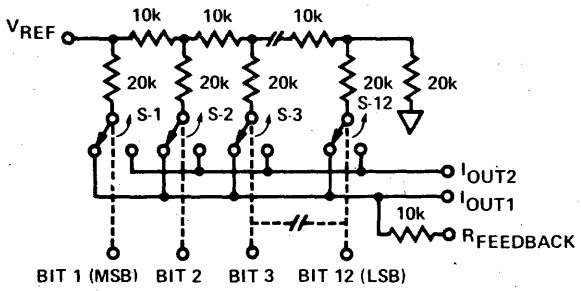
TOP VIEW

GENERAL DESCRIPTION

The MP7621 is a 12-bit monolithic digital-to-analog converter, featuring high-density CMOS. Precision thin-film deposition allows 12-bit linearity without laser trimming, thus eliminating any long-term instabilities the laser might introduce. Thermal compensation reduces Gain Error Tempco to 2 ppm/°C maximum.

Also, the MP7621 is a pin-compatible replacement for Analog Devices' AD7541. It meets or exceeds the performance of that device.

FUNCTIONAL DIAGRAM



DIGITAL INPUTS (DTL/TTL/CMOS COMPATIBLE)

Logic: A switch is closed to I_{OUT1} for its digital input in a "high" state.

ORDERING INFORMATION

Nonlinearity	Temperature Range and Package		
	Plastic 0° to +70°C	Ceramic −25°C to +85°C	Ceramic −55°C to +125°C
0.024%	MP7621JN	MP7621AD	MP7621SD
0.012%	MP7621KN	MP7621BD	MP7621TD

PRICES (100+)

MP7621JN	$16.00	MP7621AD	$23.60	MP7621SD	$62.80
MP7621KN	21.50	MP7621BD	25.40	MP7621TD	79.50

CIRCUIT DESCRIPTION

GENERAL CIRCUIT INFORMATION

The MP7621, a 12-bit multiplying D/A converter, consists of a highly stable thin film R-2R ladder and twelve CMOS current switches on a monolithic chip. Most applications require the addition of only an output operational amplifier and a voltage or current reference.

The simplified D/A circuit is shown above. An inverted R-2R ladder structure is used– that is, the binarily weighted currents are switched between the I_{OUT1} and I_{OUT2} bus lines thus maintaining a constant current in each ladder leg independent of the switch state.

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(408)247-5350

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PARAMETER	T_A = +25°C	T_A = min-max	TEST CONDITION
STATIC ACCURACY			
Resolution	12 bits min	12 bits min	
Nonlinearity			
MP7621JN, MP7621AD, MP7621SD	±0.024% FSR[1] max	±0.024% FSR max	$V_{OUT1} = V_{OUT2} = 0V$
MP7621KN, MP7621BD, MP7621TD	±0.012% FSR max	±0.012% FSR max	
Nonlinearity Tempco	2 ppm of FSR/°C max		
Gain Error[1, 2]	±0.3% FSR typ		
Gain Error Tempco[2]	2 ppm of FSR/°C max		
Power Supply Rejection	±.01% per % max	±0.02% per % max	V_{DD} = 14.5V – 15.5V
Output Leakage Current	±50nA max	±200nA max	V_{REF} = ±10V
DYNAMIC PERFORMANCE			
Output Current Settling Time[3]	2 μs max	2 μs max	To 0.012% of FSR
Feedthrough Error[3]	1mV p-p max	1mV p-p max	V_{REF} = 20V p-p @ 10 kHz
REFERENCE INPUT			
Input Resistance	5kΩ min, 20kΩ max	5kΩ min, 20kΩ max	
DIGITAL INPUTS			
V_{INH}	2.4V max	2.4V max	
V_{INL}	0.8V min	0.8V min	
Input Leakage Current	±1 μA max	±1 μA min	V_{IN} = 0 or 15V
Input Capacitance[3]	8pF max	8pF max	
Input Coding	Binary or Offset Binary (see page 6)		
ANALOG OUTPUTS			
Output Capacitance[3]			
C_{OUT1}	200pF max	200pF max	Digital Inputs = V_{INH}
C_{OUT2}	60pF max	60pF max	
C_{OUT1}	60pF max	60pF max	Digital Inputs = V_{INL}
C_{OUT2}	200pF max	200pF max	
POWER REQUIREMENTS			
V_{DD} Range	+5V min, +16V max	+5V min, +16V max	Accuracy is not guaranteed over this range.
I_{DD}	2mA max	2mA max	Digital Inputs = V_{INH} or V_{INL}

NOTES:
[1] FSR is Full Scale Range.
[2] Using internal feedback resistor.
[3] Guaranteed by design, not subject to test.
Specifications subject to change without notice.

ABSOLUTE MAXIMUM RATINGS

(T_A = +25°C unless otherwise noted)

V_{DD} (to GND) . . . . . +17V
V_{REF} (to GND) . . . . . ±25V
Digital Input Voltage Range . . . . . V_{DD} to GND
Output Voltage (Pin 1, Pin 2) . . . . . −100mV to V_{DD}
Power Dissipation (Package)
Up to +75°C. 450mW
Derate above +75°C by. . . . . 6mW/°C
Operating Temperature
JN, KN Versions . . . . . 0 to +70°C
AD, BD Versions. . . . . −25°C to +85°C
SD, TD Versions . . . . . −55°C to +125°C
Storage Temperature . . . . . −65°C to +150°C

CAUTION

1. Do not apply voltages higher than V_{DD} or less than GND potential on any terminal except V_{REF}.
2. The digital control inputs are zener protected; however permanent damage may occur on unconnected units under high energy electrostatic fields. Keep unused inputs in conductive foam at all times.

SPECIFICATION DEFINITIONS

NONLINEARITY: Error contributed by deviation of the DAC transfer function from a best straight line function. Normally expressed as a percentage of full scale range. For a multiplying DAC, this should hold true over the entire V_{REF} range.

RESOLUTION: Value of the LSB. For example, a unipolar converter with n bits has a resolution of (2^{-n}) (V_{REF}). A bipolar converter of n bits has a resolution of $[2^{-(n-1)}]$ $[V_{REF}]$. Resolution in no way implies linearity.

SETTLING TIME: Time required for the output function of the DAC to settle to within 1/2 LSB for a given digital input stimulus, i.e., 0 to Full Scale.

GAIN: Ratio of the DAC's operational amplifier output voltage to the input voltage.

FEEDTHROUGH ERROR: Error caused by capacitive coupling from V_{REF} to output with all switches OFF.

OUTPUT CAPACITANCE: Capacity from I_{OUT1} and I_{OUT2} terminals to ground.

OUTPUT LEAKAGE CURRENT: Current which appears on I_{OUT1} terminal with all digital inputs LOW or on I_{OUT2} terminal when all inputs are HIGH.

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TYPICAL PERFORMANCE CHARACTERISTICS

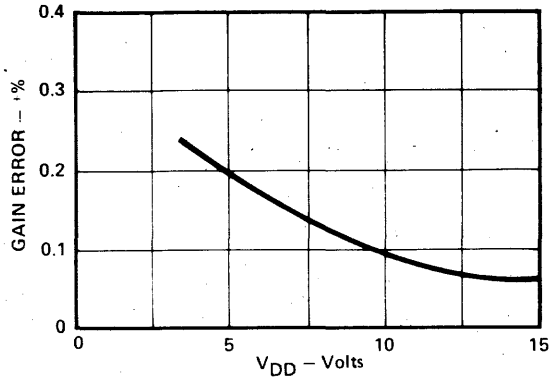


Figure 1. Gain Error vs. Supply Voltage

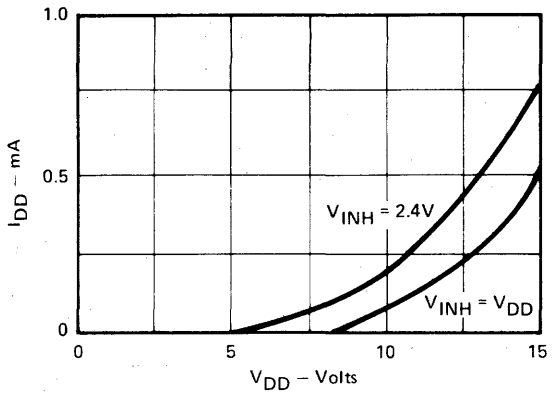


Figure 2. Supply Current vs. Supply Voltage

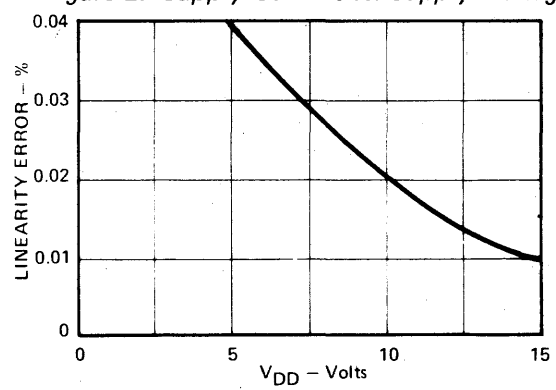


Figure 3. Linearity Error vs. Supply Voltage

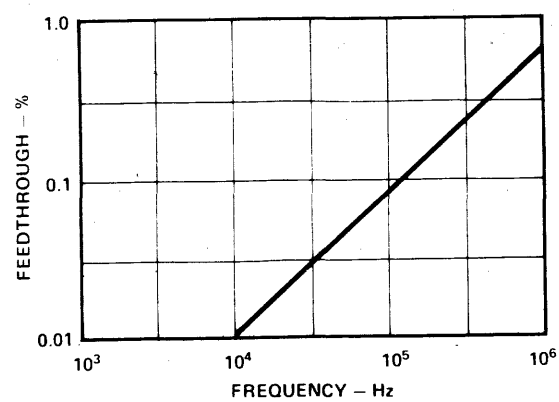


Figure 4. Feedthrough Error vs. Frequency

APPLICATION HINTS

Linearity depends upon the potential of I_{OUT1} and I_{OUT2} (pin 1 and pin 2) being exactly equal to GND (pin 3) and the output amplifier's non-inverting (+) input. Careful PC board layout and adjustment and selection of the amplifier's offset voltage and bias current are necessary.

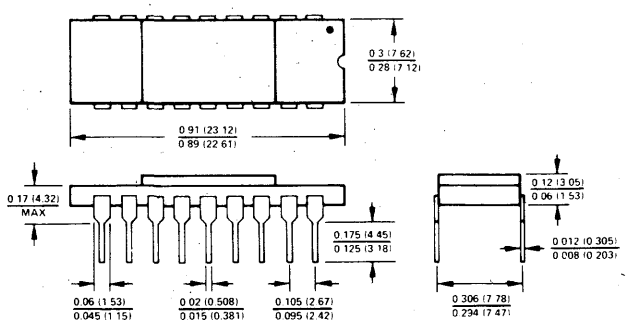
The input structures of some high speed operational amplifiers can attempt to draw substantial current during switch-on. Schottky diodes should be used in these circumstances to prevent the absolute maximum rating for V_{OUT1} and V_{OUT2} being exceeded.

The power supply should be carefully checked for noise, which would affect performance, and overshoot which could damage the device.

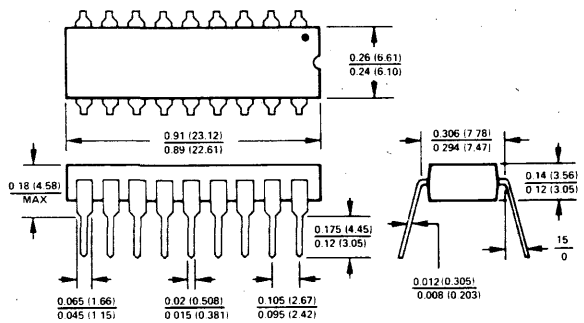
Unused digital inputs must always be grounded or taken to V_{DD} to ensure correct operation. Particular care should be taken when digital inputs are routed to another PC card. It is recommended that inputs open-circuited when PC cards are disconnected be taken to V_{DD} or GND via high value (1MΩ) resistors to prevent the accumulation of static charges.

OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).



18-PIN CERAMIC DIP



18-PIN PLASTIC DIP

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Octal Buffers

Features/Benefits

- 3-state outputs drive bus lines
- Schmitt trigger guarantees high noise margin
- Low current PNP inputs reduce loading
- 20-pin Skinny DIP™ saves space
- 8-bits matches byte boundaries
- Ideal for microprocessor interface

PART NUMBER	PKG	TEMP.	ENABLE	POLARITY	THRESH-OLD	POWER
SN74LS240 SN54LS240	N,J J	com mil	LOW	Invert	Hysteresis	LS
67LS306 57LS306	N,J J	com mil	LOW-HIGH			
SN74LS244 SN54LS244	N,J J	com mil	LOW	Non-invert		
SN74LS241 SN54LS241	N,J J	com mil	LOW-HIGH			
67LS300 57LS300	N,J N	com mil	LOW	Invert	Schmitt trigger	
67LS307 57LS307	N,J N	com mil	LOW-HIGH			
67LS304 57LS304	N,J N	com mil	LOW	Non-invert		
67LS301 57LS301	N,J N	com mil	LOW-HIGH			
SN74S240 SN54S240	N,J N	com mil	LOW	Invert	Hysteresis	S
67S306 57S306	N,J N	com mil	LOW-HIGH			
SN74S244 SN54S244	N,J N	com mil	LOW	Non-invert		
SN74S241 SN54S241	N,J N	com mil	LOW-HIGH			
67S300 57S300	N,J N	com mil	LOW	Invert	Schmitt trigger	
67S307 57S307	N,J N	com mil	LOW-HIGH			
67S304 57S304	N,J N	com mil	LOW	Non-Invert		
67S301 57S301	N,J N	com mil	LOW-HIGH			

1165 East Arques Avenue, Sunnyvale, CA 94086 Tel: (408) 739-3535 TWX: 910-339-9229 Monolithic Memories

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Description

The Octal Buffers provide high speed and high current interface capability for bus organized Digital Systems. The three-state drivers will source a termination to ground (up to 133Ω) or sink a pull-up to V_{CC} as in the popular 220Ω/330Ω computer peripheral termination. The PNP inputs provide improved fan-in with 0.2 mA I_{IL} on the Low Power Schottky buffers and 0.4 mA I_{OC} on the Schottky buffers.

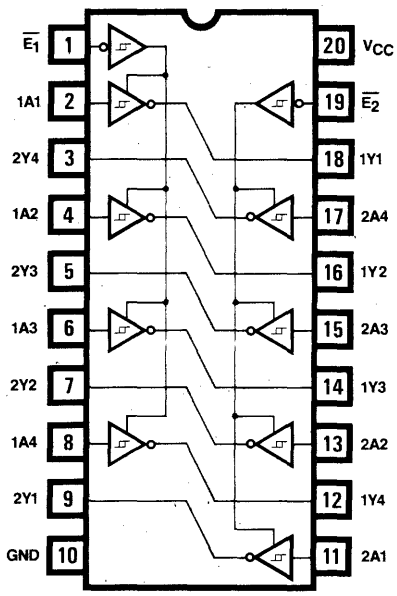
The 240 and 244 provide inverting and non-inverting outputs with active low enables. The 241 and 306 provide inverting and non-inverting outputs with both active low and active high enables allowing transceiver operation.

In addition to the standard Schottky and Low Power Schottky Octal Buffers, Monolithic Memories provides a full hysteresis with "a true" Schmitt trigger circuit. The improved performance characteristics are designed to be consistent with the SN54/74LS14 Hex Schmitt trigger and guarantee a full 400 mV noise immunity.

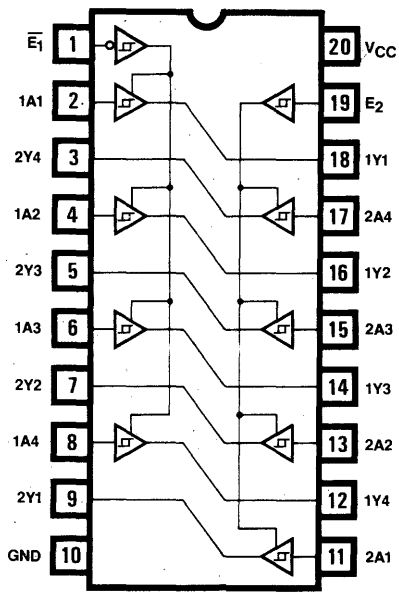
The Schmitt Trigger operation makes the LS buffers ideal for bus receivers in a noisy environment. The Schmitt Trigger operation on the S buffers acts as a safeguard against feedback oscillation and prevents slow transitions through the threshold region, insuring fast transitions and reducing I_{CC} spikes.

Logic Symbols

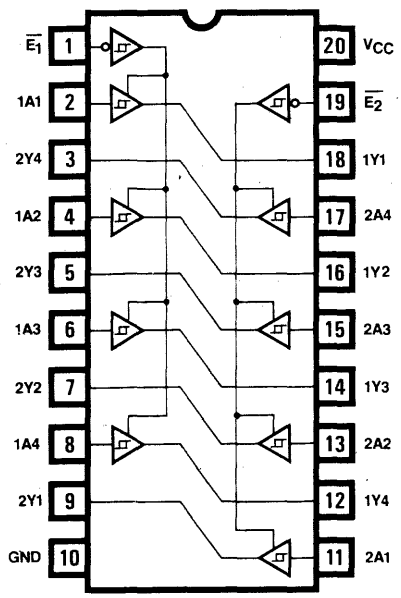
240, 300



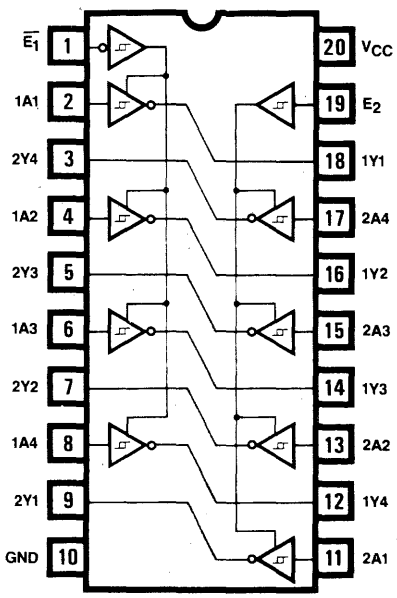
241, 301



244, 304



306, 307



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Absolute Maximum Ratings

Supply Voltage, V_{CC} 7V
Input Voltage 7V
Off-State Output Voltage 7V
Storage Temperature Range ..... −65°C to +150°C

Recommended Operating Conditions

SYMBOL	PARAMETER	MILITARY MIN	MILITARY NOM	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL NOM	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
I_{OH}	High-level output current			−12			−15	mA
I_{OL}	Low-level output current			12			24	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

Electrical Characteristics Over Recommended Operating Free Air Temperature Range

SYMBOL	PARAMETER		TEST CONDITIONS		MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.7			0.8	V
V_{IC}	Input clamp voltage		V_{CC} = MIN, I_I = −18 mA				−1.5			−1.5	V
	Hysteresis ($V_{T+} - V_{T-}$)		V_{CC} = MIN		0.2	0.4		0.2	0.4		V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = MAX, I_{OH} = −3mA		2.4	3.4		2.4	3.4		V
			V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.5 V, I_{OH} = MAX		2			2			
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} MAX	I_{OL} = 12 mA			0.4			0.4	V
				I_{OL} = 24 mA						0.5	
I_{OZH}	Off-state output current		V_{CC}, V_{IL} = MAX, V_{IH} = 2 V	V_O = 2.7 V			20			20	μA
I_{OZL}				V_O = 0.4 V			−20			−20	
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 7 V				0.1			0.1	mA
I_{IH}	High-level input current, any input		V_{CC} = MAX, V_I = 2.7 V				20			20	μA
I_{IL}	Low-level input current		V_{CC} = MAX, V_{IL} = 0.4 V				−0.2			−0.2	mA
I_{OS}	Short-circuit output current		V_{CC} = MAX		−40		−225	−40		−225	mA
I_{CC}	Supply current	Outputs high	V_{CC} = MAX, Outputs open	All		13	23		13	23	mA
		Outputs low		'LS240, LS306		26	44		26	44	
				'LS241, 'LS244		27	46		27	46	
		All outputs disabled		'LS240, LS306		29	59		29	50	
				'LS241, 'LS244		32	54		32	54	

Switching Characteristics V_{CC} = 5 V, T_A = 25°C

SYMBOL	PARAMETER	TEST CONDITIONS	LS240, LS306 MIN	LS240, LS306 TYP	LS240, LS306 MAX	LS241, LS244 MIN	LS241, LS244 TYP	LS241, LS244 MAX	UNIT
t_{PLH}	Propagation delay, low-to-high	C_L = 45 pF, R_L = 667 Ω, See Page 10-4		9	14		12	18	ns
t_{PHL}	Propagation delay, high-to-low			12	18		12	18	ns
t_{PZL}	Ouptut enable time to low level			20	30		20	30	ns
t_{PZH}	Output enable time to high level			15	23		15	23	ns
t_{PLZ}	Output disable time from low level	C_L = 5 pF, R_L = 667 Ω, See Page 10-4		15	25		15	25	ns
t_{PHZ}	Output disable time from high level			10	18		10	18	ns

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Absolute Maximum Ratings

Supply Voltage, V_{CC} 7V
Input Voltage 7V
Off-state ouptut voltage 7V
Storage temperature range ..... −65°C to +150°C

Recommended Operating Conditions

SYMBOL	PARAMETER	MILITARY MIN	MILITARY NOM	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL NOM	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
I_{OH}	High-level output current			−12			−15	mA
I_{OL}	Low-level output current			12			24	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

Electrical Characteristics Over Recommended Operating Free Air Temperature Range

SYMBOL	PARAMETER	TEST CONDITIONS		MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{T+}	Positive-going threshold voltage	V_{CC} = 5V		1.5	1.7	2.0	1.5	1.7	2.0	V
V_{T-}	Negative-going threshold voltage	V_{CC} = 5V		0.6	0.9	1.1	0.6	0.9	1.1	V
V_{IC}	Input clamp voltage	V_{CC} = MIN, I_I = −18 mA				−1.5			−1.5	V
	Hysteresis ($V_{T+} - V_{T-}$)	V_{CC} = 5V		0.4	0.8		0.4	0.8		V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = MAX, I_{OH} = −3mA		2.4	3.4		2.4	3.4		V
		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.5 V, I_{OH} = MAX		2			2			
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} MAX	I_{OL} = 12 mA			0.4			0.4	V
			I_{OL} = 24 mA						0.5	
I_{OZH}	Off-state output current	V_{CC}, V_{IL} = MAX, V_{IH} = 2 V	V_O = 2.7 V			20			20	μA
I_{OZL}			V_O = 0.4 V			−20			−20	
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 7 V				0.1			0.1	mA
I_{IH}	High-level input current, any input	V_{CC} = MAX, V_I = 2.7 V				20			20	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_{IL} = 0.4 V				−0.2			−0.2	mA
I_{OS}	Short-circuit output current	V_{CC} = MAX		−40		−225	−40		−225	mA
I_{CC}	Supply current	Outputs high	V_{CC} = MAX, Outputs open	LS300, LS307		13	23		13	23	mA
				LS301, LS304		18	31		18	31	
		Outputs low		LS300, LS307		26	44		26	44	
				LS301, LS304		32	46		32	46	
		All outputs disabled		LS300, LS307		29	59		29	50	
				LS301, LS304		34	54		34	54	

Switching Characteristics V_{CC} = 5 V, T_A = 25°C

SYMBOL	PARAMETER	TEST CONDITIONS	LS300, LS307 MIN	LS300, LS307 TYP	LS300, LS307 MAX	LS301, LS304 MIN	LS301, LS304 TYP	LS301, LS304 MAX	UNIT
t_{PLH}	Propagation delay, low-to-high	C_L = 45 pF, R_L = 667 Ω, See Page 10-4		19			19		ns
t_{PHL}	Propagation delay, high-to-low			19			19		ns
t_{PZL}	Ouptut enable time to low level			37			26		ns
t_{PZH}	Output enable time to high level			26			26		ns
t_{PLZ}	Output disable time from low level	C_L = 5 pF, R_L = 667 Ω, See Page 10-4		19			22		ns
t_{PHZ}	Output disable time from high level			19			22		ns

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Absolute Maximum Ratings

Supply Voltage, V_{CC} 7V
Input Voltage 5.5V
Off-State Output Voltage 5.5V
Storage Temperature Range ..... −65°C to +150°C

Recommended Operating Conditions

SYMBOL	PARAMETER		MILITARY MIN	MILITARY NOM	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL NOM	COMMERCIAL MAX	UNIT
V_{CC}	Supply Voltage		4.5	5	5.5	4.75	5	5.25	V
V_{OH}	High Level Output Voltage				5.5			5.5	V
I_{OH}	High Level Output Current				−1			−2.6	mA
t_W	Width of Clock/Gate	High	15			15			ns
		Low	15			15			
t_{SU}	Set Up Time	'LS373	0↓			0↓			ns
		'LS374	20↑			20↑			
t_H	Hold Time	'LS373	10↓			10↓			ns
		'LS374	0↑			0↑			
T_A	Operating Free Air Temperature		−55		125	0		70	°C

Electrical Characteristics Over Recommended Operating Free-Air Temperature Range

SYMBOL	PARAMETER	TEST CONDITIONS		MILITARY MIN	MILITARY TYP	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL TYP	COMMERCIAL MAX	UNIT
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.8			0.8	V
V_{IC}	Input clamp voltage	V_{CC} = MIN, I_I = −18mA				−1.5			−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL}MAX, I_{OH} = MAX		2.4	3.4		2.4	3.1		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL}MAX	I_{OL} = 12 mA		0.25	0.4		0.25	0.4	V
			I_{OL} = 24 mA					0.35	0.5	
I_{OZH}	High off-state current	V_{CC} = MAX, V_{IH} = 2V, V_O = 2.7 V				20			20	μA
I_{OZL}	Low off-state current	V_{CC} = MAX, V_{IH} = 2 V, V_O = 0.4 V				−20			−20	μA
I_I	Input current at max V_I	V_{CC} = MAX, V_I = 7 V				0.1			0.1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7 V				20			20	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4 V				−0.4			−0.4	mA
I_{OS}	Short-circuit current	V_{CC} = MAX		−30		−130	−30		−130	mA
I_{CC}	Supply current	V_{CC} MAX	Latch		24	40		24	40	mA
			Register		27	40		27	40	

Switching Characteristics V_{CC} = 5 V, T_A = 25°C

SYMBOL	PARAMETER	CONDITIONS	LATCH MIN	LATCH TYP	LATCH MAX	REGISTER MIN	REGISTER TYP	REGISTER MAX	UNIT
f_{MAX}	Maximum Clock Frequency	C_L = 45pF, R_L = 667Ω, See Page 10-4				35	50		MHz
t_{PLH}	Data to Output Delay			12	18				ns
t_{PHL}				12	18				
t_{PLH}	Clock/Gate to Output Delay			20	30		15	28	ns
t_{PHL}				18	30		19	28	
t_{PZH}	Output Enable Delay			15	28		20	28	ns
t_{PZL}				25	36		21	28	
t_{PHZ}	Output Disable Delay	C_L = 5pF, R_L = 667Ω, See Page 10-4		12	20		12	20	ns
t_{PLZ}				15	25		14	25	

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Absolute Maximum Ratings

Supply voltage, V_{CC} 7V
Input voltage 5.5V
Off-state output voltage 5.5V
Storage temperature range ..... −65°C to +150°C

Recommended Operating Conditions

SYMBOL	PARAMETER	MILITARY MIN	MILITARY NOM	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL NOM	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
I_{OH}	High-level output current			−12			−15	mA
I_{OL}	Low-level output current			48			64	mA
T_A	Operating free-air temperature	−55		125*	0		70	°C

*The SN54S241/244J operating at free air temperature above 116°C requires a heat sink such that $R_{\theta CA}$ is not more than 40°C/W

Electrical Characteristics Over Recommended Operating Free Air Temperature Range

SYMBOL	PARAMETER			CONDITIONS		S300, S307, MIN	S300, S307, TYP	S300, S307, MAX	S301, S304 MIN	S301, S304 TYP	S301, S304 MAX	UNIT
V_{T+}	Positive going threshold voltage			V_{CC} = 5V		1.5	1.7	1.9	1.5	1.7	1.9	V
V_{T-}	Negative-going threshold voltage			V_{CC} = 5V		0.7	0.9	1.1	0.7	0.9	1.1	V
V_{IC}	Input clamp voltage			V_{CC} = MIN, I_I = −18mA				−1.2			−1.2	V
	Hysteresis ($V_{T+} - V_{T-}$)			V_{CC} = MIN 5V		0.4	0.8		0.4	0.8		V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2V	74S	V_{IL} = 0.8V, I_{OH} = −1mA		2.7			2.7			V
			54S 74S	V_{IL} = 0.8V, I_{OH} = −3mA		2.4	3.4		2.4	3.4		
			54S 74S	V_{IL} = 0.5V, I_{OH} = MAX		2			2			
V_{OL}	Low level output voltage			V_{CC} = MIN, V_{IH} = 2V, V_{IL} = 0.8V, I_{OL} = MAX				0.55			0.55	V
I_{OZH}	Off state output current			V_{CC} = MAX, V_{IH} = 2V, V_{IL} = 0.8V	V_O = 2.4V			50			50	μA
I_{OZL}					V_O = 0.5V			−50			−50	μA
I_I	Maximum input current			V_{CC} = MAX, V_I = 5.5V				1			1	mA
I_{IH}	High level input current			V_{CC} = MAX, V_I = 2.7V				50			50	μA
I_{IL}	Low level input current	Any A		V_{CC} = MAX, V_I = 0.5V				−400			−400	μA
		Any E						−400			−400	μA
I_{OS}	Short circuit output current[1]			V_{CC} = MAX		−50		−225	−50		−225	mA
I_{CC}	Supply current	Outputs high		V_{CC} = MAX, Outputs Open	Military			123			147	mA
					Commercial			135			160	
		Outputs low			Military		100	145		120	170	
					Commercial		100	150		120	180	
		Outputs disabled			Military		100	145		120	170	
					Commercial		100	150		120	180	

Switching Characteristics V_{CC} = 5 V, T_A = 25 C

SYMBOL	PARAMETER	TEST CONDITIONS	S300, S307 MIN	S300, S307 TYP	S300, S307 MAX	S301, S304 MIN	S301, S304 TYP	S301, S304 MAX	UNIT
t_{PLH}	Data to output delay	C_L = 50 pF, R_L = 90Ω, See Page 10-4							ns
t_{PHL}									ns
t_{PZL}	Output enable delay								ns
t_{PZH}									ns
t_{PLZ}	Output disable delay	C_L = 5 pF, R_L = 90Ω, See Page 10-4							ns
t_{PHZ}									ns

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Octal Transceiver

SN74LS245, SN54LS245
67LS305, 67LS310, 57LS305, 57LS310

Features/Benefits

- **3-state outputs drive bus lines**
- **Schmitt trigger guarantees high noise margin**
- **Low current PNP inputs reduce loading**
- **20 pin Skinny DIP™ saves space**
- **8 bits matches byte boundaries**
- **Ideal for microprocessor interface**

Description

These Octal Bus transceivers are designed for asynchronous two-way communication between data buses. The control function implementation minimizes external timing requirements.

The device allows data transmission from the A bus to the B bus or from the B bus to the A bus depending upon the logic level at the direction control (DIR) input. The enable input ($\overline{E}$) can be used to disable the device so that the buses are effectively isolated.

In addition to the standard Octal transceivers, Monolithic Memories provides a full hysteresis with "a true" Schmitt Trigger circuit. The improved performance characteristics are designed to be consistent with the SN54/74LS14 Hex Schmitt Trigger and guarantee a full 400 mV noise immunity.

The Schmitt Trigger operation makes these LS transceivers ideal for noisy bus environments.

PART NUMBER	PKG	TEMP	POLARITY	THRESHOLD
SN74LS245	N,J	com	Non-invert	Hysteresis
SN54LS245	J	mil		
67LS305*	N,J	com	Non-invert	Schmitt trigger
57LS305*	J	mil		
67LS310*	N,J	com	Invert	
57LS310*	J	mil		

Function Table LS245, LS305

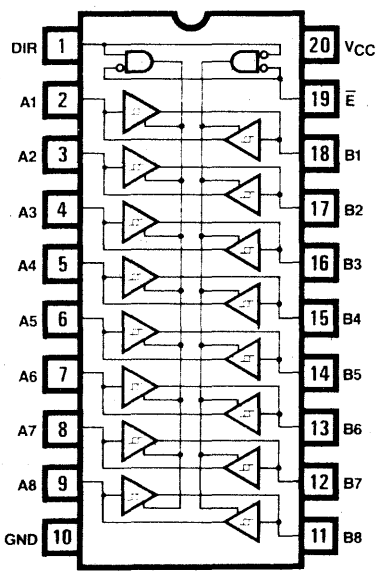
ENABLE $\overline{E}$	DIRECTION CONTROL DIR	OPERATION
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

Function Table LS310

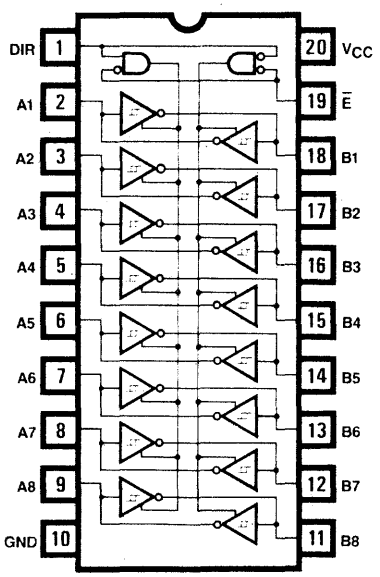
ENABLE $\overline{E}$	DIRECTION CONTROL DIR	OPERATION
L	L	$\overline{B}$ data to A bus
L	H	$\overline{A}$ data to B bus
H	X	Isolation

Logic Symbols

LS245, LS305



LS310



*Preliminary Data

1165 East Arques Avenue, Sunnyvale, CA 94086 Tel: (408) 739-3535 TWX: 910-339-9229 Monolithic Memories

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Absolute Maximum Ratings

Supply Voltage, V_{CC} 7V
Input Voltage 7V
Off-State Output Voltage 7V
Storage Temperature Range ..... −65°C to +150°C

Recommended Operating Conditions

SYMBOL	PARAMETER	MILITARY			COMMERCIAL			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
I_{OH}	High-level output current			−12			−15	mA
I_{OL}	Low-level output current			12			24	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

Electrical Characteristics

Over Recommended Operating Free Air Temperature Range

SYMBOL	PARAMETER		TEST CONDITIONS		MILITARY			COMMERCIAL			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.7			0.8	V
V_{IC}	Input clamp voltage		V_{CC} = MIN,	I_I = −18 mA			−1.5			−1.5	V
	Hysteresis ($V_{T+} - V_{T-}$) A or B input		V_{CC} = MIN		0.2	0.4		0.2	0.4		V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IH} = 2V, V_{IL} = V_{IL} max	I_{OH} = −3 mA	2.4	3.4		2.4	3.4		V
				I_{OH} = MAX	2			2			
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2V, V_{IL} = V_{IL} max	I_{OL} = 12 mA			0.4			0.4	V
				I_{OL} = 24 mA						0.5	
I_{OZH}	Off-state output current		V_{CC} = MAX,	V_O = 2.7 V			10			10	μA
I_{OZL}			$\overline{E}$ at 2 V	V_O = 0.4 V			200			200	
I_I	Input current at maximum Input voltage	A or B	V_{CC} = MAX,	V_I = 5V			0.1			0.1	mA
		DIR, $\overline{E}$		V_I = 7 V							
I_{IH}	High-level input current		V_{CC} = MAX,	V_{IH} = 2.7 V			20			20	μA
I_{IL}	Low-level input current		V_{CC} = MAX,	V_{IL} = 0.4 V			−0.2			−0.2	mA
I_{OS}	Short-circuit output current		V_{CC} = MAX		−40		−225	−40		−225	mA
I_{CC}	Supply current	Total, outputs high	V_{CC} = MAX,	Outputs open		48	70		48	70	mA
		Total, outputs low				68	90		88	90	
		Outputs at Hi-Z				64	95		64	95	

Switching Characteristics V_{CC} = 5 V, T_A = 25°C

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay, low-to-high	C_L = 45 pF, R_L = 667 Ω, See Page 10-4				ns
t_{PHL}	Propagation delay, high-to-low					ns
t_{PZL}	Output enable time to low-level					ns
t_{PZH}	Output enable time to high-level					ns
t_{PLZ}	Output disable time from low-level	C_L = 5 pF, R_L = 667 Ω, See Page 10-4				ns
t_{PHZ}	Output disable time from high-level					ns

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PRELIMINARY ADVANCE INFORMATION FINAL SPECIFICATIONS MAY CHANGE

Absolute Maximum Ratings

Supply Voltage, V_{CC} 7V
Input Voltage 7V
Off-State Output Voltage 7V
Storage Temperature Range ..... −65°C to +150°C

Recommended Operating Conditions

SYMBOL	PARAMETER	MILITARY			COMMERCIAL			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
I_{OH}	High-level output current			−12			−15	mA
I_{OL}	Low-level output current			12			24	mA
T_A	Operating free-air temperature	−55		125	0		70	°C

Electrical Characteristics

Over Recommended Operating Free Air Temperature Range

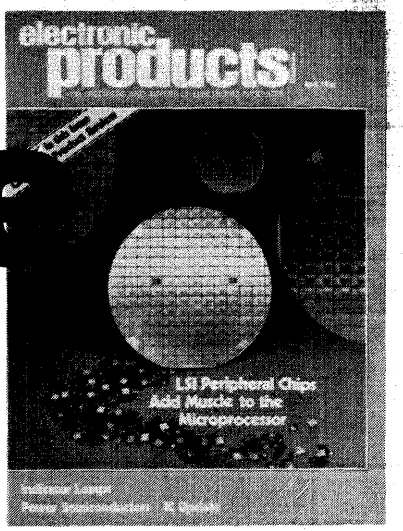
SYMBOL	PARAMETER		TEST CONDITIONS		MILITARY			COMMERCIAL			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{T+}	Positive-going threshold voltage		V_{CC} = 5V		1.5	1.7	1.9	1.5	1.7	1.9	V
V_{t-}	Negative-going threshold voltage		V_{CC} = 5V		0.7	0.9	1.1	0.7	0.9	1.1	V
V_{T-}	Input clamp voltage		V_{CC} = MIN,	I_I = −18 mA			−1.5			−1.5	V
	Hysteresis ($V_{T+} - V_{T-}$) A or B input		V_{CC} = MIN		0.4	0.8		0.4	0.8		V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IH} = 2V, V_{IL} = V_{IL} max	I_{OH} = −3 mA	2.4	3.4		2.4	3.4		V
				I_{OH} = MAX	2			2			
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2V, V_{IL} = V_{IL} max	I_{OL} = 12 mA			0.4			0.4	V
				I_{OL} = 24 mA						0.5	
I_{OZH}	Off-state output current		V_{CC} = MAX, $\overline{E}$ at 2 V	V_O = 2.7 V			10			10	μA
I_{OZL}				V_O = 0.4 V			−200			−200	
I_I	Input current at maximum Input voltage	A or B	V_{CC} = MAX,	V_I = 5.5V			0.1			0.1	mA
		DIR, $\overline{E}$		V_I = 7 V							
I_{IH}	High-level input current		V_{CC} = MAX,	V_{IH} = 2.7 V			20			20	μA
I_{IL}	Low-level input current		V_{CC} = MAX,	V_{IL} = 0.4 V			−0.2			−0.2	mA
I_{OS}	Short-circuit output current		V_{CC} = MAX		−40		−225	−40		−225	mA
I_{CC}	Supply current	Total, outputs high	V_{CC} = MAX,	Outputs open							mA
		Total, outputs low				62	90		62	90	
		Outputs at Hi-Z				64	95		64	95	

Switching Characteristics V_{CC} = 5 V, T_A = 25°C

SYMBOL	PARAMETER	TEST CONDITIONS	CS305, LS310			LS310			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	Propagation delay, low-to-high	C_L = 45 pF, R_L = 667 Ω See Page 10-4							ns
t_{PHL}	Propagation delay, high-to-low								ns
t_{PZL}	Output enable time to low-level								ns
t_{PZH}	Output enable time to high-level								ns
t_{PLZ}	Output disable time from low-level	C_L = 5 pF, R_L = 667 Ω See Page 10-4							ns
t_{PHZ}	Output disable time from high-level								ns

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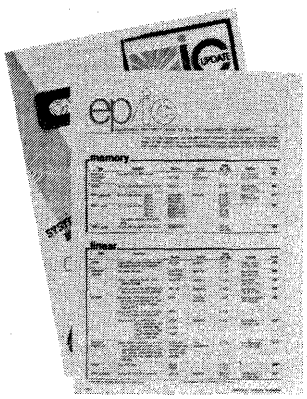
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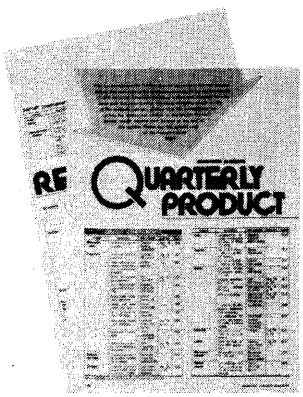
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MC14569B

McMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

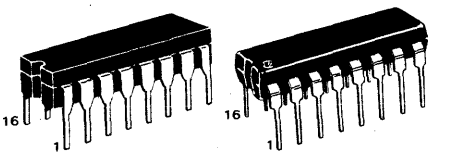
HIGH SPEED PROGRAMMABLE DIVIDE-BY-N DUAL 4-BIT BCD/BINARY COUNTER

HIGH SPEED PROGRAMMABLE DIVIDE-BY-N DUAL 4-BIT BCD/BINARY COUNTER

The MC14569B is a high speed programmable divide-by-N dual 4-bit BCD or binary down counter constructed with MOS P-channel and N-channel enhancement mode devices (complementary MOS) in a single monolithic structure.

It has been designed for use with the MC14568B phase comparator/counter in frequency synthesizers, phase-locked loops, and other frequency division applications requiring low power dissipation and/or high noise immunity.

- 9.5 MHz Typical Counting Rate at 10 V for Any Division Ratio Greater Than 1
- Speed-up Circuitry for Zero Detection and Preset Enable
- Each 4-Bit Counter Can Divide Independently in BCD or Binary Mode
- Quiescent Current = 5 nA typ/pkg @ 5 Vdc
- Can be Cascaded With MC14568B, MC14522B and MC14526B for Frequency Synthesizer Applications



L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

ORDERING INFORMATION

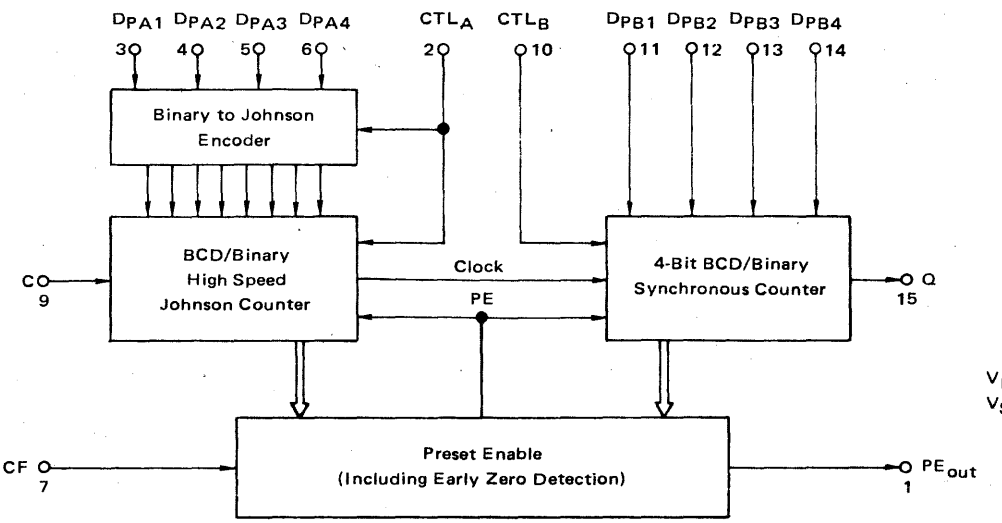
MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range — AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

BLOCK DIAGRAM

CTL = "0" for Binary Count
CTL = "1" for BCD Count



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DS 9454

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ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage "0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
$V_{in} = V_{DD}$ or 0		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
$V_{in} = 0$ or V_{DD}		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage# "0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (AL Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-3.0	–	-2.4	-4.2	–	-1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	-0.64	–	-0.51	-0.88	–	-0.36	–	
(V_{OH} = 9.5 Vdc)		10	-1.6	–	-1.3	-2.25	–	-0.9	–	
(V_{OH} = 13.5 Vdc)		15	-4.2	–	-3.4	-0.88	–	-2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current (CL/CP Device)	I_{OH}									mAdc
(V_{OH} = 2.5 Vdc) Source		5.0	-2.5	–	-2.1	-4.2	–	-1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	-0.52	–	-0.44	-0.88	–	-0.36	–	
(V_{OH} = 9.5 Vdc)		10	-1.3	–	-1.1	-2.25	–	-0.9	–	
(V_{OH} = 13.5 Vdc)		15	-3.6	–	-3.0	-8.8	–	-2.4	–	
(V_{OL} = 0.4 Vdc) Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	μAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	μAdc
Input Capacitance (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device) (Per Package)	I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	μAdc
		10	–	10	–	0.010	10	–	300	
		15	–	20	–	0.015	20	–	600	
Quiescent Current (CL/CP Device) (Per Package)	I_{DD}	5.0	–	50	–	0.005	50	–	150	μAdc
		10	–	100	–	0.010	100	–	300	
		15	–	200	–	0.015	200	–	600	
Total Supply Current**† (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs, all buffers switching)	I_T	5.0	(0.58 μA/kHz) f + I_{DD}							μAdc
		10	(1.20 μA/kHz) f + I_{DD}							
		15	(1.95 μA/kHz) f + I_{DD}							

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.
#Noise immunity specified for worst-case input combination.
Noise Margin for both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc
†To calculate total supply current at loads other than 50 pF:
$I_T(C_L) = I_T(50\ pF) + 1 \times 10^{-3} (C_L - 50) V_{DD} f$
where: I_T is in μA (per package), C_L in pF, V_{DD} in Vdc, and f in kHz is input frequency.
**The formulas given are for the typical characteristics only at 25°C.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

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SWITCHING CHARACTERISTICS (C_L = 50 pF, T_A = 25°C)

Characteristic	Symbol	V_{DD} Vdc	All Types			Unit
			Min	Typ	Max	
Output Rise Time	t_r	5.0	–	100	200	ns
		10	–	50	100	
		15	–	40	80	
Output Fall Time	t_f	5.0	–	100	200	ns
		10	–	50	100	
		15	–	40	80	
Turn-On Delay Time	t_{PLH}					ns
PE_{out}		5.0	–	420	700	
		10	–	175	300	
		15	–	125	250	
Q Output		5.0	–	675	1200	ns
		10	–	285	500	
		15	–	200	400	
Turn-Off Delay Time	t_{PHL}					ns
PE_{out}		5.0	–	380	600	
		10	–	150	300	
		15	–	100	200	
Q Output		5.0	–	530	1000	ns
		10	–	225	400	
		15	–	155	300	
Minimum Clock Pulse Width	PW_C	5.0	–	100	300	ns
		10	–	45	150	
		15	–	30	115	
Maximum Clock Pulse Frequency #	PRF	5.0	2.1	3.5	–	MHz
		10	5.7	9.5	–	
		15	7.8	13.0	–	
Maximum Clock Pulse Rise and Fall Time	t_r, t_f	5.0	NO LIMIT			μs
		10				
		15				

#This inplies that zero detection and preset enable is done while the clock is running at the specified frequency.

SWITCHING WAVEFORMS

FIGURE 1

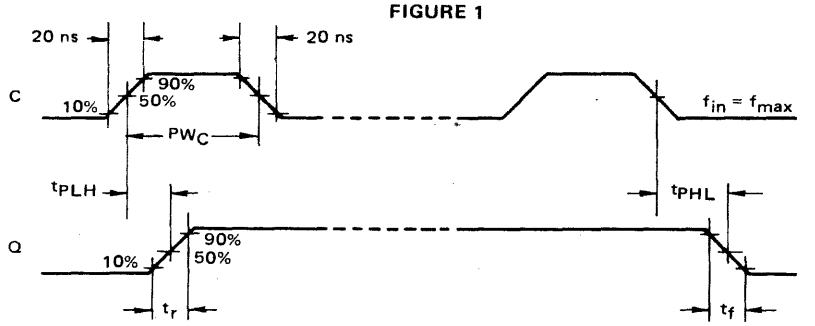
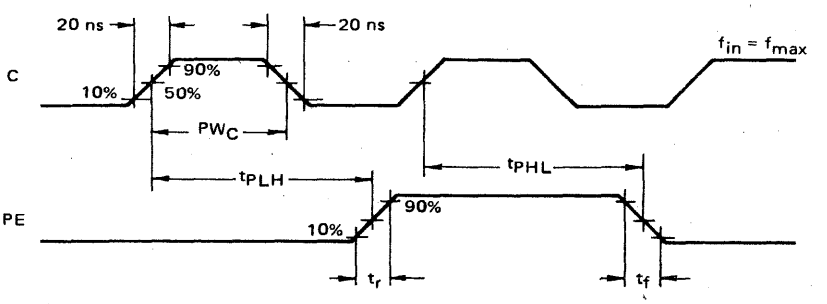


FIGURE 2



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OPERATING CHARACTERISTICS

The MC14569B includes a high speed Johnson counter followed by a BCD/binary 4-bit synchronous counter (see block diagram). The use of an encoder allows the Johnson counter to be programmed (i.e. preset) in BCD or binary code through inputs D_{PA1}, D_{PA2}, D_{PA3}, and D_{PA4}.

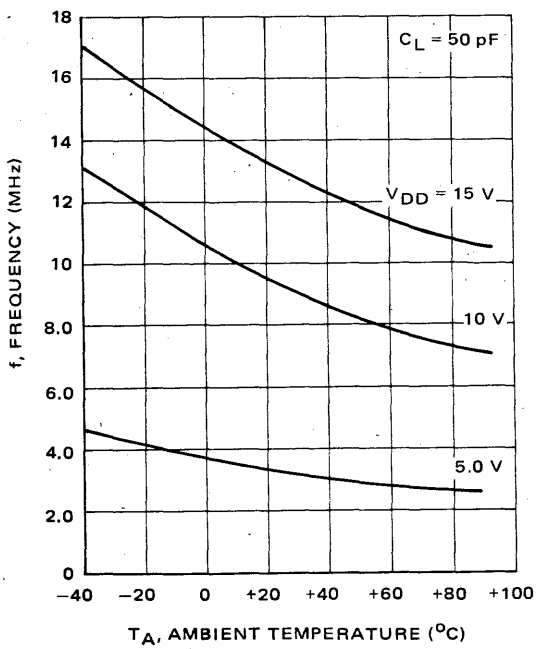
The BCD/binary counter can be programmed through inputs D_{PB1}, D_{PB2}, D_{PB3}, and D_{PB4}. For each counter a divide ratio of 10 (BCD count) or 16 (binary count) can be chosen independently by inputs CTL_A and CTL_B respectively. When one of those inputs is set high, the divide ratio of the corresponding counter is 10 (BCD); when it is set low, the division ratio is 16 (binary).

A Cascade Feedback input (pin 7), a Q output (pin 15) and a Preset Enable output (pin 1) made it possible to cascade the MC14568B, MC14522B and MC14526B with this device. CF, Q and PE_{out} of MC14569B must be respectively connected to "0", C and PE of the following counter.

When MC14569B is used alone, CF must be connected to V_{DD}. One pulse will appear on output PE_{out} every N clock periods (N being the value programmed on the D_P inputs). Both counters included in MC14569B, and eventually all the counters which are cascaded, should normally be preset at the programmed values during the clock period where they all reach the count zero. For best speed performance, preset is started as soon as count 1 is detected. As a consequence, it is not possible to program a frequency division ratio of one. However, it is possible to program a division ratio of 11 (i.e. $D_{PA1}, \ldots D_{PA4}$ = 1,0,0,0 and $D_{PB1}, \ldots D_{PB4}$ = 1,0,0,0), or a division ratio of 101 if another counter is cascaded with the MC14569B.

This high speed configuration makes it possible to guarantee a maximum clock pulse frequency of 5.7 MHz for a 10 V V_{DD} supply for any division ratio greater than one. Due to the presence of the early zero detection, the circuit must be used in the two least significant digit positions.

Because all the circuitry is static, there is no minimum frequency specification for the Clock input, C (pin 9).



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MC14443
MC14447

Advance Information

CMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

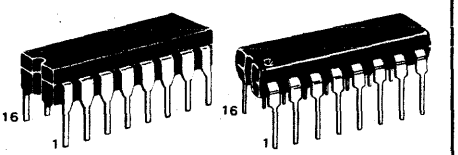
MICROPROCESSOR BASED
ANALOG TO DIGITAL CONVERTER

ANALOG TO DIGITAL CONVERTER LINEAR SUBSYSTEM

The MC14443 and the MC14447 devices are 6 channel, single slope, 8–10 bit analog to digital converter linear subsystems for microprocessor based data and control, systems. Contained in both devices are a one of 8 decoder, an 8 channel analog multiplexer, a buffer amplifier, a precision voltage to current converter, a ramp start circuit, and a comparator. The output driver of the MC14443 comparator is an open-drain N-channel capable of sinking up to 5 mA of current. The output of the MC14447 comparator has a standard B-Series P-channel, N-channel pair.

A processor system (such as the MC6800, MC141000 or MC3870) provides the addressing, timing, counting, and arithmetic operations required for implementing a full analog to digital converter system. A system made up of a processor and the linear subsystem has features such as automatic zeroing and variable scaling (weighting) of six separate analog channels.

- Quiescent Current 0.8 mA Typical at V_{DD} = 5 V
- Single Supply Operation +4.5 to +18 Volts
- MPU Compatible
- Typical Resolution — 10 Bits
- Typical Conversion Cycle as Fast as 300 μs
- Ratio Metric Conversion Minimizes Error



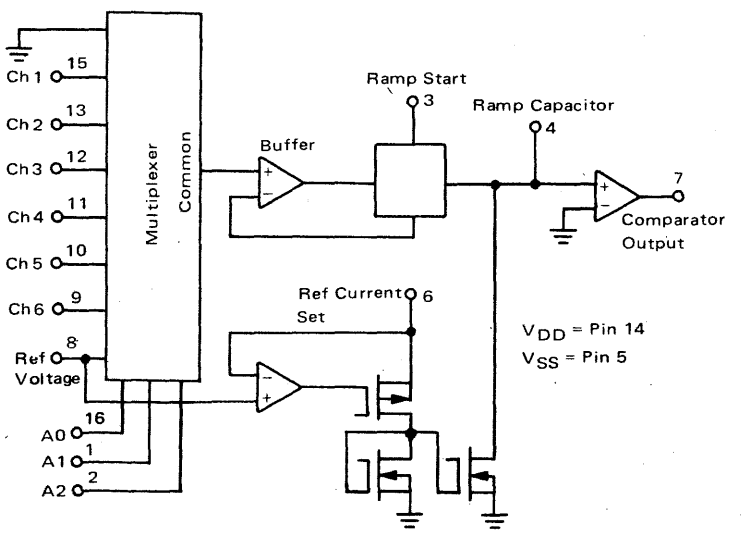
L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

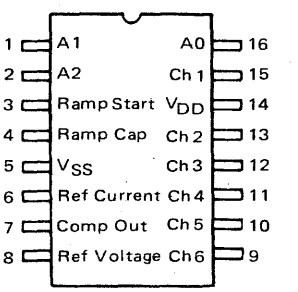
ORDERING INFORMATION

MC14XXX — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

BLOCK DIAGRAM



PIN ASSIGNMENT



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ADI-476

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MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range – AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$.

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage—Comparator "0" Level	V_{OL}	5.0	–	0.05	–	0.01	0.05	–	0.05	Vdc
V_{in} @ Pin 4 = 0 V		10	–	0.05	–	0.01	0.05	–	0.05	
		15	–	0.05	–	0.01	0.05	–	0.05	
V_{in} @ Pin 4 = 0.5 V "1" Level	V_{OH}	5.0	4.95	–	4.95	4.99	–	4.95	–	Vdc
(R_L = 10 k, MC14447 only)		10	9.95	–	9.95	9.99	–	9.95	–	
		15	14.95	–	14.95	14.99	–	14.95	–	
Input Voltage-Address, Ramp Start "0 Level"	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)		5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)		10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)		15	–	4.0	–	6.75	4.0	–	4.0	
"1" Level	V_{IH}									Vdc
(V_O = 0.5 or 4.5 Vdc)		5.0	3.5	–	3.5	2.75	–	3.5	–	
(V_O = 1.0 or 9.0 Vdc)		10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)		15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current—Comparator	I_{OH}									mAdc
V_{in} @ Pin 4 = 0.5 V (MC14447 only)										
(V_{OH} = 2.5 Vdc)		5.0	-2.5	–	-2.1	-4.2	–	-1.7	–	
(V_{OH} = 4.6 Vdc)		5.0	-0.52	–	-0.44	-0.88	–	-0.36	–	
(V_{OH} = 9.5 Vdc)		10	-1.3	–	-1.1	-2.25	–	-0.9	–	
(V_{OH} = 13.5 Vdc)		15	-3.6	–	-3.0	-8.8	–	-2.4	–	
V_{in} @ Pin 4 = 0 V	I_{OL}									mAdc
(V_{OL} = 0.4 Vdc)		5.0	0.52	–	0.44	0.88	–	0.36	–	
(V_{OL} = 0.5 Vdc)		10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)		15	3.6	–	3.0	8.8	–	2.4	–	
Input Current—Address, Ramp Start	I_{in}	15	–	±0.3	–	–	±0.3	–	±1.0	μAdc
Input Current—Analog Inputs	I_{in}	15	–	–	–	±0.1	±10	–	–	nAdc
Input Capacitance—Address, Ramp Start V_{in} = 0 V	C_{in}	15	–	–	–	5.0	7.5	–	–	pF
Quiescent Current	I_{DD}	5	–	–	–	0.8	–	–	–	mAdc
		10	–	–	–	1.5	–	–	–	
		15	–	–	–	1.7	–	–	–	
Crosstalk Between Any Two Input Channels	V_{Cr}	–	–	–	–	0	4.0	–	–	mVdc
Reference Current Range	I_R	–	–	–	10	–	50	–	–	μAdc
Common Mode Input Voltage	V_{CM}	5	–	–	0	–	2.5	–	–	Vdx
		10	–	–	0	–	7.0	–	–	
		15	–	–	0	–	12	–	–	
Buffer Amplifier Output Offset	V_{BO}	5	–	–	–	0.285	–	–	–	Vdc
		10	–	–	–	0.400	–	–	–	
		15	–	–	–	0.420	–	–	–	
Comparator Threshold	V_{TC}	5	–	–	–	0.195	V_{BO}	–	–	Vdc
		10	–	–	–	0.275	V_{BO}	–	–	
		15	–	–	–	0.290	V_{BO}	–	–	
Reference Voltage Range	V_R	5	–	–	2.0	–	2.5	–	–	Vdc
		10	–	–	2.0	–	7	–	–	
		15	–	–	2.0	–	12	–	–	
Conversion Linearity V_{in} = V_{DD} – 3 V for C > 100 pF	L_C	–	–	–	–	0.05	0.2	–	–	% Full Scale

*T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.

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SWITCHING CHARACTERISTICS (C_L = 50 pF, T_A = 25°C)

Characteristic		Symbol	V_{DD} Vdc	Typ	Max	Unit
Output Rise Time—Comparator	(MC14447 only)	t_r	5.0 10 15	100 50 40	200 100 80	ns
Output Fall Time—Comparator		t_f	5.0 10 15	40 20 15	80 40 30	ns
Propagation Delay Time—Comparator	MC14443 (R_L = 10 k to V_{DD})	t_{PLH}	5.0 10 15	2.0 1.0 0.75	– – –	μs
	MC14447	t_{PLH}	5.0 10 15	2.0 1.0 0.75	– – –	μs
	All Devices	t_{PHL}	5.0 10 15	2.0 1.0 0.75	– – –	μs
Multiplexer Propagation Delay		t_M	5.0 10 15	850 300 250	– – –	ns
Ramp Start Delay Time		t_{RS}	5.0 10 15	850 300 250	– – –	ns
Acquisition Time*		t_A	5.0 10 15	10 9.0 8.0	– – –	μs

*Acquisition Time includes multiplexer propagation delay, ramp start propagation delay and the time required to charge ramp capacitor to the selected input voltage.

DEVICE OPERATION

ADDRESS INPUTS SELECT (A0, A1, A2, Pins 1, 2, 16) The input voltage source to be presented to the measurement system according to the Truth Table shown in Figure 3.

RAMP START (Ramp Start, Pin 3) When the Ramp Start is low, the ramp capacitor is charged to a voltage associated with the selected input channel. When the Ramp Start is brought high,the connection to the input channel is broken and the capacitor begins to ramp toward V_{SS}.

RAMP CAPACITOR (Ramp Cap, Pin 4) The ramp capacitor is used to generate a time period when discharged from a selected voltage via a precise reference current.

NEGATIVE POWER SUPPLY (V_{SS}, Pin 5) This pin is system ground.

REFERENCE CURRENT (Ref Current, Pin 6) To discharge the ramp capacitor, the reference current is fixed via a resistor (R_{Ref}) to a positive supply from pin 6. Typical current is equal to $(V_{DD} - V_{Ref})/R_{Ref}$.

COMPARATOR OUTPUT (Comp Out, Pin 7) This output is low when the capacitor has reached the discharged voltage and is high otherwise.

REFERENCE VOLTAGE (Ref Voltage, Pin 8) This voltage can be set to a voltage between V_{SS} + 2 V and V_{DD} – 2 V. This is the known voltage to which the unknown is compared.

INPUT CHANNELS (Pins 9, 10, 11, 12, 13, 15) Input channels 1 through 6 are used to monitor up to six separate unknown voltages. Selection is via the address inputs.

POSITIVE POWER SUPPLY (V_{DD}, Pin 14) This pin is the package positive power supply pin.

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FIGURE 1 – VOLTAGE TO PULSE WIDTH CONVERSION

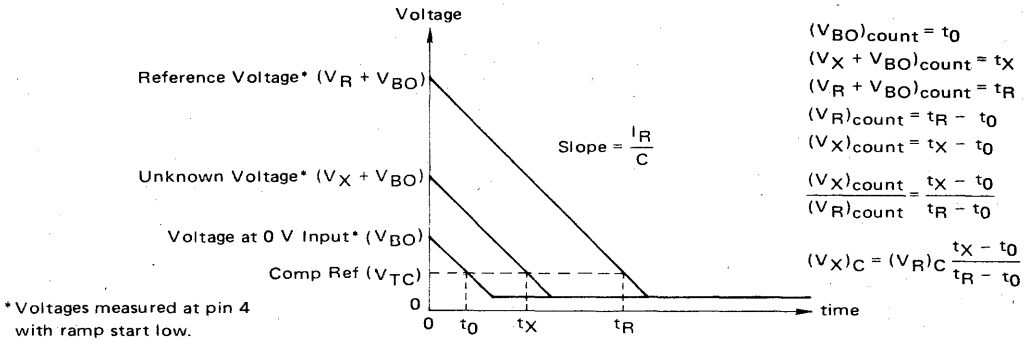
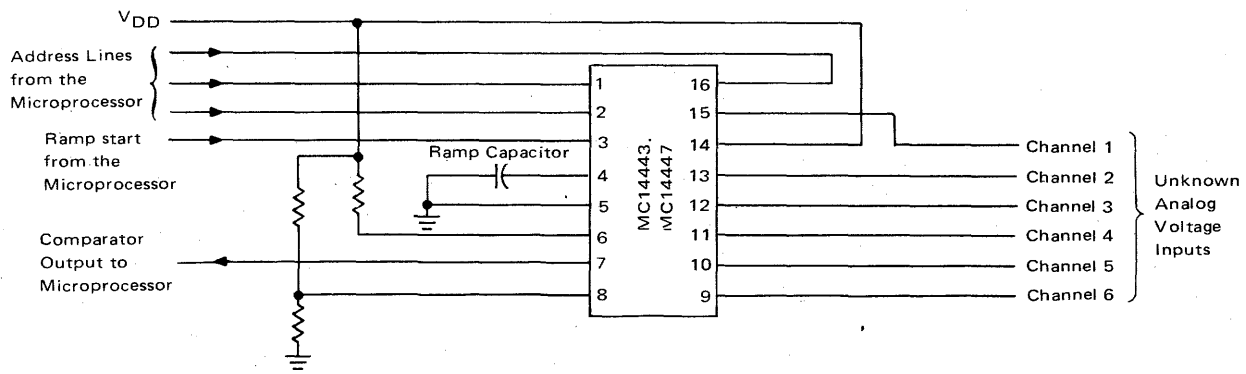


FIGURE 2 – TRUTH TABLE

A2	A1	A0	Input Selected	
0	0	0	V_{SS}	Channel 0 (ground)
0	0	1	Ch1	Channel 1
0	1	0	Ch2	Channel 2
0	1	1	Ch3	Channel 3
1	0	0	Ch4	Channel 4
1	0	1	Ch5	Channel 5
1	1	0	Ch6	Channel 6
1	1	1	V_{Ref}	Channel 7 (External Reference)

FIGURE 3 – TYPICAL APPLICATIONS CIRCUIT



CONVERSION SEQUENCE

Step No.	A2	A1	A3	Ramp Start	Comment
1.	1	1	1	0	Channel 7 Selected (Reference Voltage)
2.	1	1	1	1	Record time until Pin 7 goes low
3.	0	0	0	0	Channel 0 Selected (Ground)
4.	0	0	0	1	Record time until Pin 7 goes low
5.	0	0	1	0	Channel 1 Selected
6.	0	0	1	1	Record time until Pin 7 goes low
Calculate $t_{Ch7} - t_{Ch0} = t_{Ch7'}$ Step 2–Step 4					
Calculate $t_{Ch1} - t_{Ch0} = t_{Ch1'}$ Step 6–Step 4					
Calculate $V_{unknown} = V_{Ch7}(t_{Ch1'}/t_{Ch7'})$					
7.	0			0	Channel 2 Selected
8.	0			1	Record time until Pin 7 goes low
Calculate $t_{Ch2} - t_{Ch0} = t_{Ch2'}$					
Calculate $V_{unknown} = V_{Ch7}(t_{Ch2'}/t_{Ch7'})$					
etc.					

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MC14495

Advance Information

CMOS MSI

(LOW-POWER COMPLEMENTARY MOS)

BCD-TO-SEVEN SEGMENT HEXADECIMAL LATCH/DECODER/DRIVER

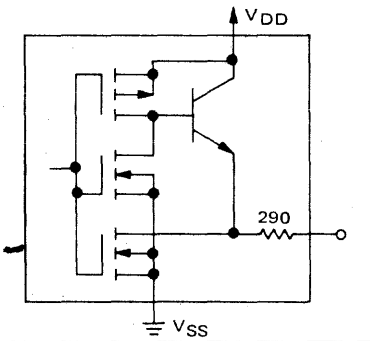
BCD-TO-SEVEN SEGMENT HEXADECIMAL LATCH/ DECODER/DRIVER

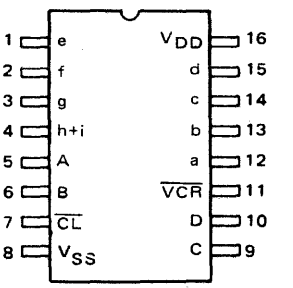
The MC14495 BCD-to-seven segment hexidecimal latch/decoder/ driver is constructed with complementary MOS (CMOS) enhancement mode devices and NPN bipolar output drivers in a single monolithic structure. The circuit provides the functions of a 4-bit storage latch. It can be used with LED seven segment displays without resistor interface at 5 volt supply. The resistors of typically 290 ohms are internal to the part.

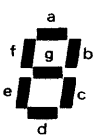
Applications include MPU systems display driver, instrument display driver, computer/calculator display driver, cockpit display driver, and various clock, watch, and timer uses.

- Low Logic Circuit Power Dissipation
- High-Current Sourcing Outputs With Internal Limiting Resistance
- Latch Storage of Code
- Supply Voltage Range = 4.5 Vdc to 16 Vdc
- Internal Input Level Shift:
  Input +5 CMOS to V_{DD} of +5 to +16 Vdc
  Input +5 V TTL with Pull-up, to V_{DD} of +5 to +16 Vdc

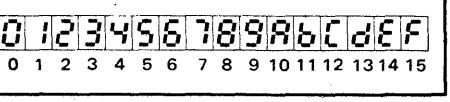
OUTPUT CIRCUIT
(Except Pin 11)



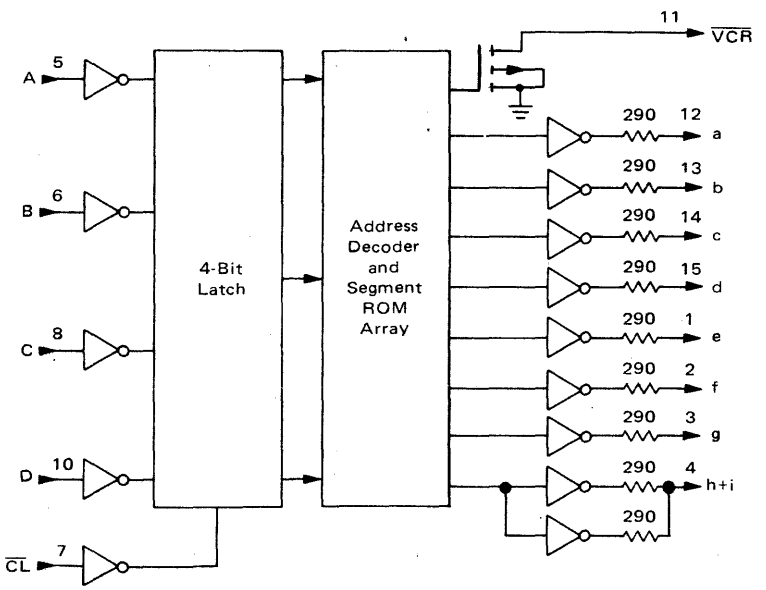




ALPHANUMERIC DISPLAY



BLOCK DIAGRAM



TRUTH TABLE

INPUTS				OUTPUTS									
D	C	B	A	a	b	c	d	e	f	g	h+i	VCR	DISPLAY
0	0	0	0	1	1	1	1	1	1	0	0	Open	0
0	0	0	1	0	1	1	0	0	0	0	0	Open	1
0	0	1	0	1	1	0	1	1	0	1	0	Open	2
0	0	1	1	1	1	1	1	0	0	1	0	Open	3
0	1	0	0	0	1	1	0	0	1	1	0	Open	4
0	1	0	1	1	0	1	1	0	1	1	0	Open	5
0	1	1	0	1	0	1	1	1	1	1	0	Open	6
0	1	1	1	1	1	1	0	0	0	0	0	Open	7
1	0	0	0	1	1	1	1	1	1	1	0	Open	8
1	0	0	1	1	1	1	1	0	1	1	0	Open	9
1	0	1	0	1	1	1	0	1	1	1	1	Open	A
1	0	1	1	0	0	1	1	1	1	1	1	Open	b
1	1	0	0	1	0	0	1	1	1	0	1	Open	C
1	1	0	1	0	1	1	1	1	0	1	1	Open	d
1	1	1	0	1	0	0	1	1	1	1	1	Open	E
1	1	1	1	1	0	0	0	1	1	1	1	0	F

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ADI-484

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MAXIMUM RATINGS (Voltages referenced to V_{SS}).

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Input Pin	I	10	mAdc
Operating Temperature Range	T_A	-40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C
Maximum Continuous Output Power (Source) per Output @ 25 °C Pins 1, 2, 3, 12, 13, 14, 15 Pin 14	P_{OHmax}	 50 100	mW

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

‡$P_{OHmax} = I_{OH}(V_{DD} - V_{OH})$

ELECTRICAL CHARACTERISTICS (All voltages referenced to V_{SS} = 0, T_A -25°C)

Characteristics	Symbol	Condition	Min	Typ	Max	Unit
DC Supply Voltage	V_{DD}		4.5		16	Vdc
Input Voltage	V_{IL}		—		0.8	Vdc
	V_{IH}	V_{DD} = 15V V_{DD} = 5.0V	4.0 3.5		— —	Vdc
Input Current	I_{in}		—		±10	μAdc
Output $\overline{VCR}$, Pin 11	I_{OH}	$V_{OH} = V_{DD}$	—		±10	μAdc
Open Drain Output	I_{OL}	V_{OL} = 0.5V, V_{DD} = 5.0V V_{OL} = 0.5V, V_{DD} = 15V	0.2 1.0		— —	mA
Outputs a, b, c, d, e, f, g	I_{OH}	V_{OH} = 2.0V, V_{DD} = 5.0V V_{OH} = 1.5V, V_{DD} = 5.0V V_{OH} = 12V, V_{DD} = 15V V_{OH} = 11.5V, V_{DD} = 15V	-7.5 — -7.5 —		 -11.5 -11.5	mA
	I_{OL}	V_{OL} = 1.0V, V_{DD} = 5.0V V_{OL} = 1.0V, V_{DD} = 15V	0.1 0.5		— —	mA
Output h + i	I_{OH}	V_{OH} = 2.0V, V_{DD} = 5.0V V_{OH} = 1.5V, V_{DD} = 5.0V V_{OH} = 12V, V_{DD} = 15V V_{OH} = 11.5V, V_{DD} = 15V	-15 — -15 —		— -23 — -23	mA
	I_{OL}	V_{OL} = 1V, V_{DD} = 5.0 V V_{OL} = 1.0 V, V_{DD} = 15V	0.2 1.0		— —	mA

INPUT/OUTPUT FUNCTIONS

Segment Driver (a, b, c, d, e, f, g, h, i; Pins 1, 2, 3, 4, 12, 13, 14, 15)

The segment drivers are emitter-follower NPN-transistors. To limit the output current, a resistor typically 290 ohms is integrated internally at each output. Therefore, external resistors are not necessary when driving an LED at the supply voltage of V_{DD} = 5.0 volts.

OUTPUT ($\overline{VCR}$; Pin 11)

This output is activated (goes to low) whenever the address corresponding to program 16 is selected. Otherwise the output is open. See the truth table.

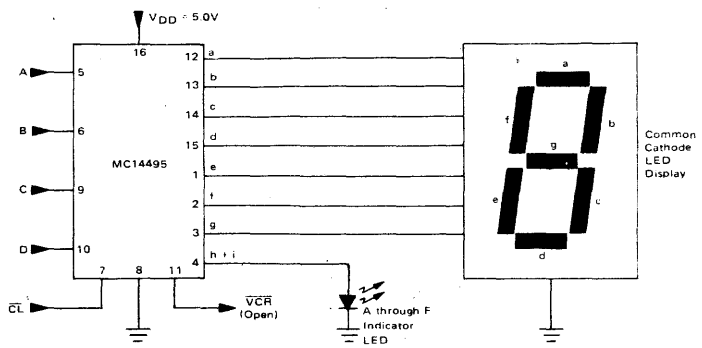
INPUT LATCH (A,B, C, D; Pins 5, 6, 8, 10)

The block diagram is shown on page 1. The inputs A, B, C, and D are fed to a 4-bit latch which is controlled by clock ($\overline{CL}$). Two modes of operation are available.

CLOCK ($\overline{CL}$; Pin 7)

The data on the inputs A, B, C and D will pass through the latch and will be displayed immediately when the clock is low. In this mode of operation the circuit is performing the function of a conventional decoder/driver. The data may be loaded into the latch when $\overline{CL}$ = low and will be latched with the rising edge of $\overline{CL}$. The data will remain stored as long as $\overline{CL}$ is high.

TYPICAL CIRCUIT @ V_{DD} = 5.0V



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MC14469

ADDRESSABLE ASYNCHRONOUS RECEIVER/TRANSMITTER

The MC14469 Addressable Asynchronous Receiver Transmitter is constructed with MOS P-channel and N-channel enhancement devices in a single monolithic structure (CMOS). The MC14469 receives one or two eleven-bit words in a serial data stream. One of the incoming words contains the address and when the address matches, the MC14469 will then transmit its information in two eleven-bit-word data streams. Each of the transmitted words contains eight data bits, even parity bit, start and stop bit.

The received word contains seven address bits and the address of the MC14469 is set on seven pins. Thus 2^7 or 128 units can be interconnected in simplex or full duplex data transmission. In addition to the address received, seven command bits may be received for data or control use.

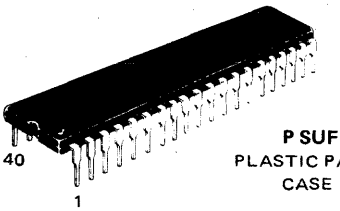
The MC14469 finds application in transmitting data from remote A-to-D converters, remote MPUs or remote digital transducers to the master computer or MPU.

- Supply Voltage Range – 4.5 Vdc to 18 Vdc
- Low Quiescent Current – 75 μAdc maximum @ 5 Vdc
- Data Rates to 4800 Baud
- Receive – Serial to Parallel
  Transmit – Parallel to Serial
- Transmit and Receive Simultaneously in Full Duplex
- Crystal or Resonator Operation for On-Chip Oscillator

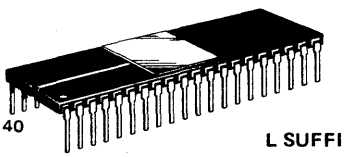
CMOS LSI

(LOW-POWER COMPLEMENTARY MOS)

ADDRESSABLE ASYNCHRONOUS RECEIVER/TRANSMITTER



P SUFFIX
PLASTIC PACKAGE
CASE 711



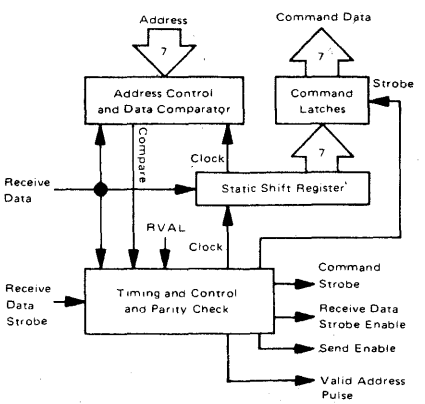
L SUFFIX
CERAMIC PACKAGE
CASE 715

ORDERING INFORMATION

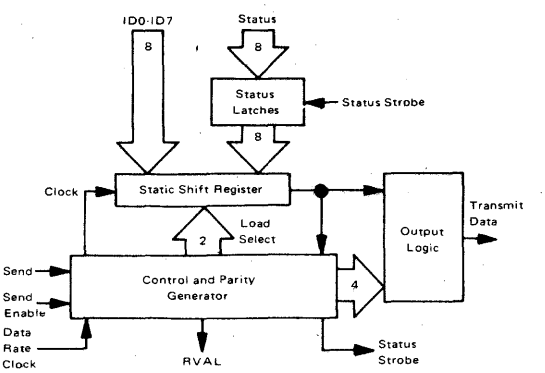
MC14xxx	Suffix	Denotes
	L	Ceramic Package
	P	Plastic Package

BLOCK DIAGRAMS

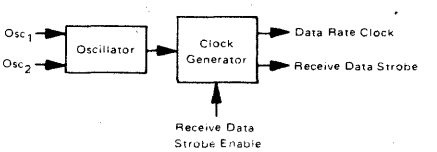
Receive



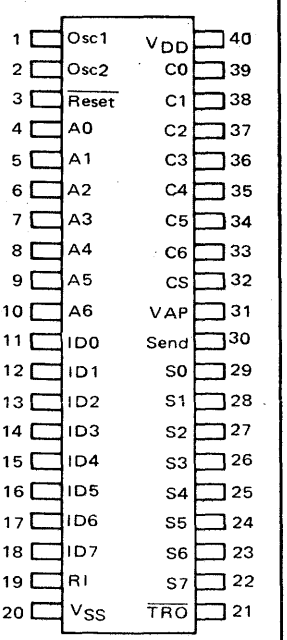
Transmit



Clocks



PIN ASSIGNMENTS



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MAXIMUM RATINGS (Voltages referenced to V_{SS}, Pin 20.

	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range	T_A	-40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}).

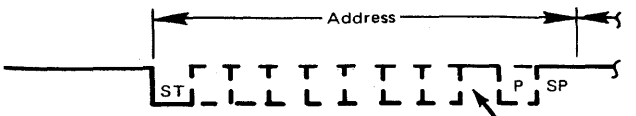
ELECTRICAL CHARACTERISTICS

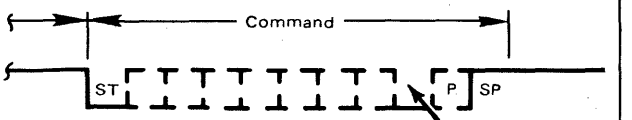
Characteristic		Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage	"0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0			10	–	0.05	–	0	0.05	–	0.05	
			15	–	0.05	–	0	0.05	–	0.05	
	"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}			10	9.95	–	9.95	10	–	9.95	–	
			15	14.95		14.95	15	–	14.95	–	
Input Voltage #	"0" Level	V_{IL}									Vdc
(V_O = 4.5 or 0.5 Vdc)			5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)			10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)			15	–	4.0	–	6.75	4.0	–	4.0	
	"1" Level	V_{IH}									Vdc
(V_O = 0.5 or 4.5 Vdc)			5.0	3.5	–	3.5	2.75	–	3.5	–	
(V_O = 1.0 or 9.0 Vdc)			10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)			15	11.0	–	11.0	8.25	–	11.0	–	
Output Drive Current (Except Pin 2)		I_{OH}									mAdc
(V_{OH} = 2.5 Vdc)	Source		5.0	-1.0	–	-0.8	-1.7	–	-0.6	–	
(V_{OH} = 4.6 Vdc)			5.0	-0.2	–	-0.16	-0.35	–	-0.12	–	
(V_{OH} = 9.5 Vdc)			10	-0.5	–	-0.4	-0.9	–	-0.3	–	
(V_{OH} = 13.5 Vdc)			15	-1.4	–	-1.2	-3.5	–	-1.0	–	
(V_{OL} = 0.4 Vdc)	Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)			10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)			15	3.6	–	3.0	8.8	–	2.4	–	
Output Drive Current (Pin 2 Only)		I_{OH}									mAdc
(V_{OH} = 2.5 Vdc)	Source		5.0	-0.19	–	-0.16	-0.32	–	-0.13	–	
(V_{OH} = 4.6 Vdc)			5.0	-0.04	–	-0.035	-0.07	–	-0.03	–	
(V_{OH} = 9.5 Vdc)			10	-0.09	–	-0.08	-0.16	–	-0.06	–	
(V_{OH} = 13.5 Vdc)			15	-0.29	–	-0.27	-0.48	–	-0.2	–	
(V_{OL} = 0.4 Vdc)	Sink	I_{OL}	5.0	0.1	–	0.085	0.17	–	0.07	–	mAdc
(V_{OL} = 0.5 Vdc)			10	0.17	–	0.14	0.28	–	0.1	–	
(V_{OL} = 1.5 Vdc)			15	0.50	–	0.42	0.84	–	0.3	–	
Maximum Frequency		f_{max}	4.5	400	–	365	550	–	310	–	kHz
Input Current		I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	μAdc
Pull-Up Current (Pins 4-18)		I_{up}	15	12	120	10	50	100	8.0	85	μAdc
Input Capacitance		C_{in}	–	–	–	–	5.0	7.5	–	–	pF
(V_{in} = 0)											
Quiescent Current		I_{DD}	5.0	–	75	–	0.010	75	–	565	μAdc
(Per Package)			10	–	150	–	0.020	150	–	1125	
			15	–	300	–	0.030	300	–	2250	
Supply Voltage		V_{DD}	–	+4.5	+18.0	+4.5	–	+18.0	+4.5	+18.0	Vdc

*T_{low} = -40°C
T_{high} = +85°C
=Noise immunity specified for worst-case input combination.
Noise Margin both "1" and "0" level = 1.0 Vdc min @ V_{DD} = 5.0 Vdc
2.0 Vdc min @ V_{DD} = 10 Vdc
2.5 Vdc min @ V_{DD} = 15 Vdc

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RECEIVE DATA (RI; Pin 19)

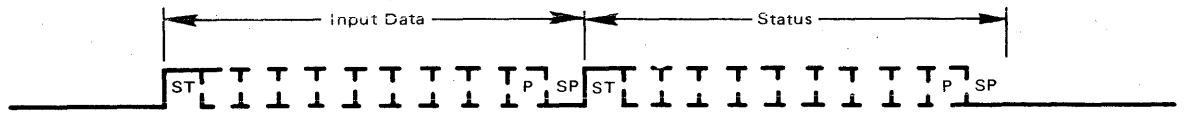




MC14469 Pin Number	4	5	6	7	8	9	10
Pin Designation	A0	A1	A2	A3	A4	A5	A6
MC6850 ACIA Pin Number	22	21	20	19	18	17	16
Pin Designation	D0	D1	D2	D3	D4	D5	D6

	39	38	37	36	35	34	33
	C0	C1	C2	C3	C4	C5	C6
	22	21	20	19	18	17	16
	D0	D1	D2	D3	D4	D5	D6

TRANSMIT DATA ($\overline{TRO}$; Pin 21)



MC14469 Pin Numbers	11	12	13	14	15	16	17	18	29	28	27	26	25	24	23	22
Pin Designation	ID0	ID1	ID2	ID3	ID4	ID5	ID6	ID7	S0	S1	S2	S3	S4	S5	S6	S7
MC6850 ACIA Pin Number	22	21	20	19	18	17	16	15	22	21	20	19	18	17	16	15
Pin Designation	D0	D1	D2	D3	D4	D5	D6	D7	D0	D1	D2	D3	D4	D5	D6	D7

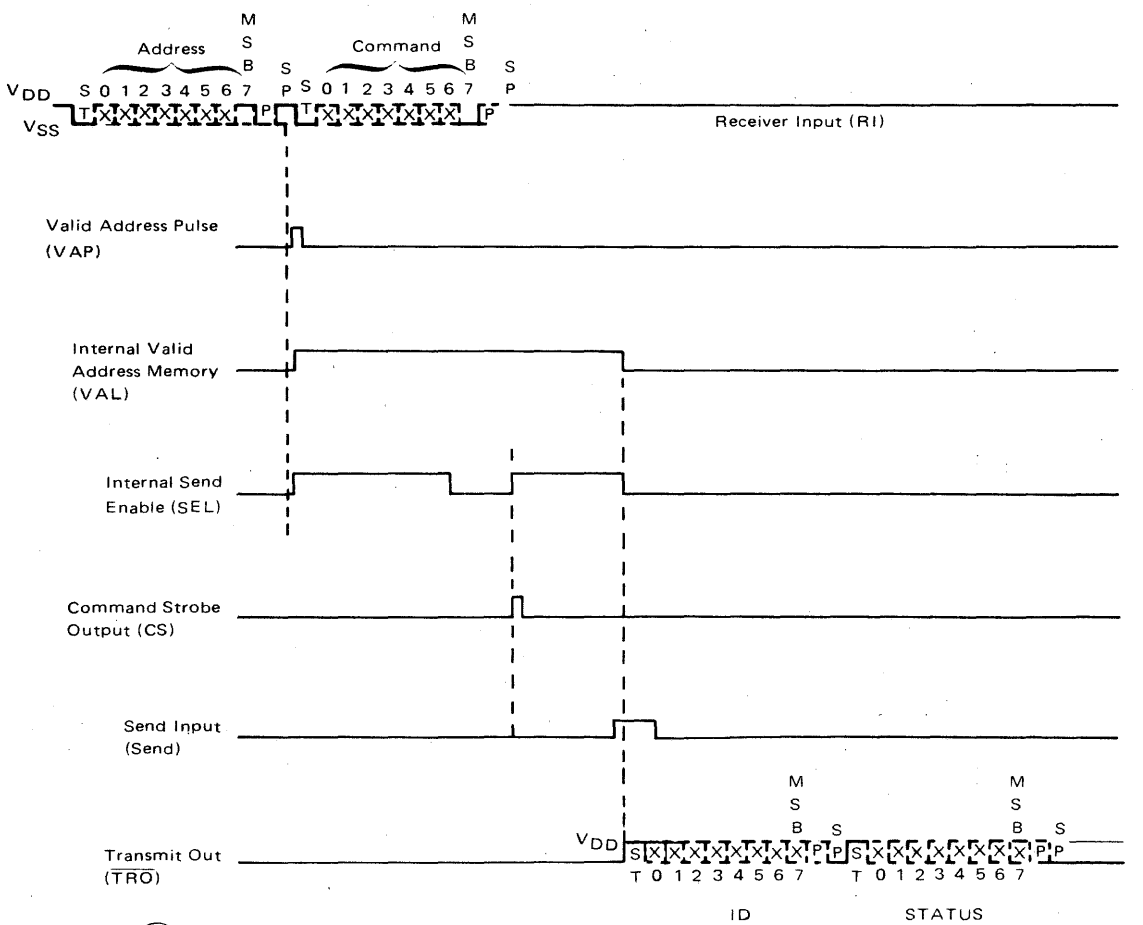
ST = Start Bit
P = Parity Bit
SP = Stop Bit

A0 → A6 = Address Bits
C0 → C6 = Command Bits
D0 → D7 = ACIA Bus Bits

ID0 → ID7 = MC14469 Identification Code
S0 → S7 = MC14469 Status Code

CORRESPONDING DATA POSITION AND PINS FOR MC14469 AND MC6850

TYPICAL RECEIVE/SEND CYCLE



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DEVICE OPERATION

OSCILLATOR (Osc1, Osc2; Pins 1, 2) — These pins are the oscillator input and output. (See Figure 1.)

RESET ($\overline{\text{Reset}}$; Pin 3) — When this pin is pulled low, the circuit is reset and ready for operation.

ADDRESS (A0-A6; Pin 4, 5, 6, 7, 8, 9, 10) — These are the address setting pins which contain the address match for the received signal.

INPUT DATA (ID0-ID7; Pins 11, 12, 13, 14, 15, 16, 17, 18) — These pins contain the input data for the first eight bits of data to be transmitted.

RECEIVE INPUT (RI; Pin 19) — This is the receive input pin.

NEGATIVE POWER SUPPLY (V_{SS}; Pin 20) — This pin is the negative power supply connection. Normally this pin is system ground.

TRANSMIT REGISTER OUTPUT SIGNAL ($\overline{\text{TRO}}$; Pin 21) — This pin transmits the outgoing signal. Note that it is inverted from the incoming signal. It must go through one stage of inversion if it is to drive another MC14469.

SECOND or STATUS INPUT DATA (S0-S7; Pins 22, 23, 24, 25, 26, 27, 28, 29) — These pins contain the input data for the second eight bits of data to be transmitted.

SEND (Send; Pin 30) — This pin accepts the send command after receipt of an address.

VALID ADDRESS PULSE (VAP; Pin 31) — This is the output for the valid address pulse upon receipt of a matched incoming address.

COMMAND STROBE (CS; Pin 32) — This is the output for the command strobe signifying a valid set of command data on pins 33-39.

COMMAND WORD (C0-C6; Pins 33, 34, 35, 36, 37, 38, 39) — These pins are the readout of the command word which is the second word of the received signal.

POSITIVE POWER SUPPLY (V_{DD}; Pin 40) — This pin is the package positive power supply pin.

OPERATING CHARACTERISTICS

The receipt of a start bit on the Receive Input (RI) line causes the receive clock to start at a frequency equal to that of the oscillator divided by 64. All received data is strobed in at the center of a receive clock period. The start bit is followed by eight data bits. Seven of the bits are compared against states of the address of the particular circuit (A0-A6), while the eighth bit signifies an address word "1", or a command word "0". Next, a parity bit is received and checked by the internal logic for even parity. Finally a stop bit is received. At the completion of the cycle if the address compared, a Valid Address Pulse (VAP) occurs. Immediately following the address word, a command word is received. It also contains a start bit, eight data bits, even parity bit, and a stop bit. The eight data bits are composed of a seven-bit command, and a "0" which indicates a command word. At the end of the command word a Command Strobe Pulse (CS) occurs.

A positive transition on the Send input initiates the transmit sequence. Again the transmitted data is made up of two eleven-bit words, i.e., address and command words. The data portion of the first word is made up from Input Data inputs (ID0-ID7), and the data for the second word from Second Input Data (S0-S7) inputs. The data on inputs S0-S7 is latched before the start of transmit of the first of the second two words. The transmitted signal is the inversion of the received signal, which allows the use of an inverting amplifier to drive the lines.

The oscillator can be crystal controlled or ceramic resonator controlled for required accuracy. Pin 1 may be driven from an external oscillator. See Figure 1.

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ABBREVIATIONS OF COMPANY NAMES

AD	Analog Devices
AMD	Advanced Micro Devices
AMI	American Microsystems, Inc.
Amperex	Amperex Electronics Corp.
Analogic	Analogic Corp.
Beckman	Beckman Instruments, Helipot Division
BEI	BEI Electronics
Burr-Brown	Burr-Brown Research
Cermetek	Cermetek
Cherry	Cherry Semiconductor
CMA	Consumer Microcircuits of America
Cybernetic	Cybernetic Micro Systems
Data General	Data General
Datel	Datel Systems
DDC	Data Devices Corp.
Delco	Delco Electronics
Dionics	Dionics Inc.
EA	Electronic Arrays
EMM/Semi	EMM Semi, Div. of Electronic Memories & Magnetics
Essex	Essex International
Exar	Exar Integrated Systems
Fairchild	Fairchild
Ferranti	Ferranti Electric
Fujitsu	Fujitsu
GI	General Instrument
Harris	Harris Semiconductor
Hitachi	Hitachi America Ltd.
Holt	Holt Inc.
Hughes	Hughes Aircraft Solid State Products
Hybrid Sys	Hybrid Systems
HyComp	HyComp
IMI	International Microcircuits, Inc.
Intech/FMI	Intech/Function Modules Inc.
Intel	Intel
Interdesign	Interdesign
Intersil	Intersil
IPI	Integrated Photomatrix, Inc.
Lambda	Lambda Electronics
LSI	LSI Computer Systems
Maruman	Maruman Integrated Circuits
Master Logic	Master Logic
Matrox	Matrox Electronics Systems
Micro Net	Micro Networks
Micropac	Micropac Industries
Micro Power	Micro Power Systems
Micro Tech	Microcircuits Technology
Mitel	Mitel Semiconductor
Mitsubishi	Mitsubishi Electric Co.
MMI	Monolithic Memories, Inc.
Monosil	Monosil
MOS	MOS Technology
Mostek	Mostek
Motorola	Motorola Semiconductor
National	National Semiconductor
NCR	NCR Corp., Microelectronics Division
NEC America	NEC America
NEC Micro	NEC Microcomputers
Nitron	Nitron
Nortec	Nortec Electronics
Novonics	Novonics
NPC	Nucleonic Products Co.
OEI	Optical Electronics, Inc.
OKI	OKI Semiconductor
Panasonic	Panasonic, Matsushita Electric Corp.
Photo Therm	Photo Therm
Plessey	Plessey Semiconductors
PMI	Precision Monolithics, Inc.
Raytheon	Raytheon Semiconductor
RCA	RCA Solid State Division
Reticon	Reticon
RIFA	RIFA
Rockwell	Rockwell Microelectronic Devices
RTC	Real Time Corp.
Sanken	Sanken Electric
Sanyo	Sanyo Electric
SGS	SGS-Ates Semiconductor
Siemens	Siemens
Signetics	Signetics (Philips)
Silicon G	Silicon General
Siliconix	Siliconix
Silicon Sys.	Silicon Systems, Inc.
Silitronics	Silitronics
SMC	Standard Microsystems
Solitron	Solitron Devices
Sprague	Sprague Electric Company
Supertex	Supertex, Inc.
SSM	Solid State Microtechnology for Music
SSS	Solid State Scientific
Synertek	Synertek
Telaris	Telaris
Teledyne C	Teledyne Crystalonics
Teledyne P	Teledyne Philbrick
Teledyne S	Teledyne Semiconductor
Telefunken	AEG-Telefunken
TI	Texas Instruments
TMX	TMX
Toshiba	Toshiba
Trans-Data	Trans-Data
TRW	TRW
Unitrode	Unitrode
Western	Western Digital
Zilog	Zilog

National Semiconductor

Preliminary
FEBRUARY 1978

DP8350 Series Programmable CRT Controllers

General Description

The DP8350 Series of CRT Controllers are single-chip bipolar (I^2L technology) circuits in a 40-pin package. They are designed to be dedicated CRT display refresh circuits.

The CRT Controller (CRTC) provides an internal dot rate crystal controlled oscillator for ease of system design. For systems where a dot rate clock is already provided, an external clock input may be used by the CRTC. In either case system synchronization is made possible with the use of the buffered Dot Rate Clock Output.

The DP8350 Series has 11 character generation related timing outputs. These outputs are compatible for systems with or without line buffers, using character ROMS, or DM8678-type latch/ROM/shift register circuits.

12 bits (4k) of bidirectional TRI-STATE® character memory addresses are provided by the CRTC for direct interface to character memory.

Three on-chip registers provide for external loading of the row starting address, cursor address, and top-of-page address.

A complete set of video outputs is available including cursor enable, programmable vertical blanking, programmable horizontal sync, and programmable vertical sync.

The DP8350 Series CRTC provides for a wide range of programmability using internal mask programmable ROMs:

- Character Field (both number of dots/character and number of scan lines/character)
- Characters per Row
- Character Rows per Video Frame

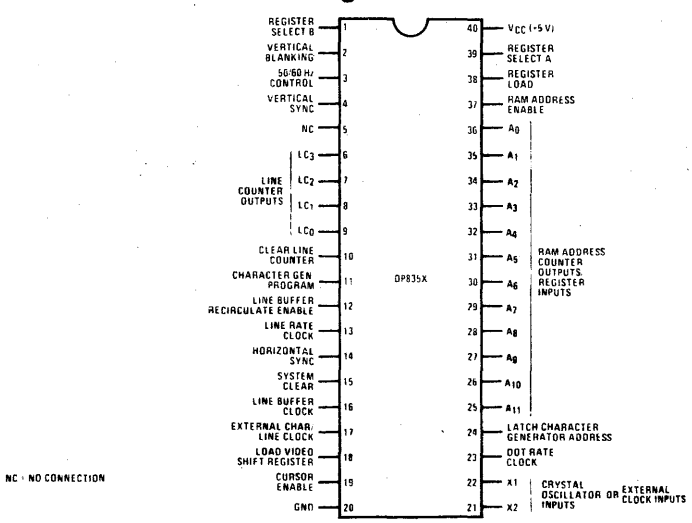
The CRTC also provides system sync and program inputs including 50/60 Hz control, system clear, external character/line rate clock, and character generator program.

The DP8350 Series operates on a single +5 V power supply. Outputs and inputs are TTL compatible.

Features

- Internal crystal controlled dot rate oscillator
- External dot rate clock input
- Buffered dot rate clock output
- Timing pulses for character generation
- Character memory address outputs (12 bits)
- Internal cursor address register
- Internal row starting address register
- Top-of-page address register (for scrolling)
- Programmable horizontal and vertical sync outputs
- Programmable cursor enable output
- Programmable vertical blanking output
- 50/60 Hz refresh rate
- Programmable characters/row (5 to 110)
- Programmable character field size (up to 16 dots x 16 scan line field size)
- Programmable character rows/frame (1 to 64)
- Single +5 V power supply
- Inputs and outputs TTL compatible
- Ease of system design/application

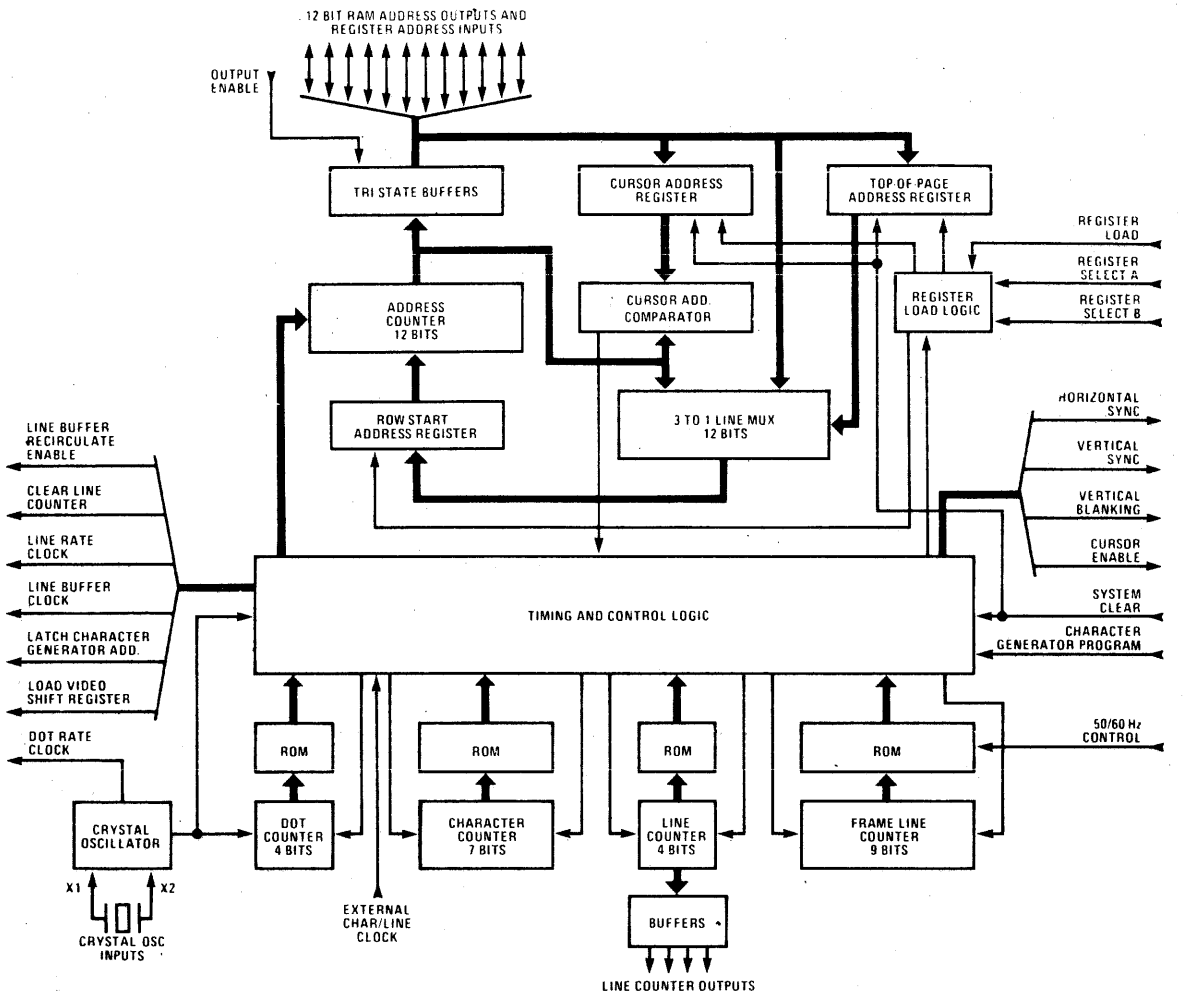
DP8350 Series Connnnection Diagram



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DP8350 Block Diagram



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DP8350 Functional Pin Description

CHARACTER GENERATION/TIMING OUTPUTS

The CRTC provides 11 interface timing outputs for line buffers, character generator ROM, DM8678-type latch/ROM/shift register combination character generators, and system status timing. All outputs are TTL compatible and directly interface to popular system circuits, including:

- DM8678 Series Character Generators
- MM52157, MM52179 Character ROMs
- DM74166 Dot Shift Register
- MK1007P, 33571/2, 2532 80-Bit Shift Registers (Line Buffers)

Dot Rate Clock: This output is buffered for use in system synchronization and interface to dot shift register. Positive edge clock at crystal oscillator frequency.

Load Video Shift Register: Buffered output at character rate frequency. Used for direct interface to dot shift register. This output is active only during video time and therefore performs both the horizontal and vertical blanking functions. Low level active.

Latch Character Generator Address: Buffered output at character rate frequency. Active at all times. Positive edge clock.

Line Buffer Clock: This output directly interfaces to line buffers. Output operates at character rate. Negative edge clock. Not active during horizontal blanking. The number of clocks per scan line is equivalent to the number of video characters per row.

Line Rate Clock: Line rate frequency output for use with DM8678-type character generator.

Line Counter Outputs (LC_0 to LC_3): Buffered outputs at line rate frequency for use with character ROMs without internal line counter. These outputs are also useful for system decode of present line position in character row. Outputs clock in sync with Line Rate Clock at start of horizontal blanking. Outputs are always active.

Clear Line Counter: Row rate clock – occurs in sync with Line Rate Clock during horizontal blanking between last line of any row and first line of a new row. This output is always active and is a negative edge clock – direct interface to the DM8678.

Line Buffer Recirculate Enable: This output interfaces to a line buffer and becomes inactive (logic "0" state) during the last line or the first line of a character row, depending on the state of the character generator program input. A low level on this output indicates (in line buffer applications) the time during which the line buffer is loaded with the next row of character codes.

Table 1. Character Generator Program Truth Table

Character Generator Program Input	Recirculate Enable Output Low Level and New Row Address at Address Outputs
"0"	Last line of character row
"1"	First line of character row

The pulse appears at the start of horizontal blanking prior to when the memory address bus must be transferred to the CRTC, then returns to the high state at the next horizontal blanking interval.

MEMORY ADDRESS OUTPUTS/INPUTS AND REGISTERS

CRT Character Address Outputs (TRI-STATE) – A_0 to A_{11}: 12 bits of bidirectional CRT character address counter outputs are provided by the CRTC. These outputs directly interface to the system RAM memory address bus.

Within a scan line the counter is pre-set to the address contained within the Row Start Register (RSR) three character times before the start of video time. The counter is then advanced sequentially at character rate to the max video character address plus 1 for the present scan line. This address is then held during the horizontal blanking interval up to three character times before video start for the next scan line. At this point the counter is again pre-set to the contents of the RSR and the above sequence is repeated. This sequence provides scan line address repetition for every scan line of a character location within a row. Row-to-row start address modifications are accomplished by updating the contents of the RSR.

During vertical blanking the address counter operation is modified by stopping the pre-set load of the contents of the RSR into the address counter, thereby allowing the address outputs to free run during vertical blanking. This allows minimum access time to the CRTC when the CRTC address counter outputs are being used for dynamic RAM refresh.

RAM Address Enable Input: At all times the status of the address counter outputs is controlled externally by the Enable Input. Logic "0" = TRI-STATE, Logic "1" = Active.

Internal Top-of-Page, Row Start, and Cursor Registers: Control pins are provided for loading the top-of-page, row start, and cursor address into three 12-bit CRTC registers from the bidirectional memory address pins.

The Top-of-Page Register (TOPR) holds the address of the first character of the first video row. This register allows display scroll with the CRTC without the use of external memory address adders. If the TOPR is not loaded after a system clear its contents will be zero and the address outputs will be sequential from zero at the top-of-page.

The Cursor Register (CR) holds the present address of the cursor and is cleared to zero after a system clear. Once the TOPR and CR registers have been loaded they need not be accessed again until modification of their contents is required. These registers may be loaded at any time, but to cause minimum display distortion it is recommended that they be loaded only during blanking intervals.

The Row Start Register (RSR) is the working register for the CRTC address counter. It determines the first video character address on a scan line to scan line basis.

Modification of this register after the start of video in a scan line will modify the address counter outputs at the start of video on the next scan line. (See address output description.) If the RSR is never externally loaded, the CRTC address outputs will be sequential on a row-to-row basis from the TOPR contents at the start of the video page. With external loading, row-to-row non-sequential operation of the CRTC address outputs is possible, thus row-to-row edit capability. When used in this mode the RSR should be loaded after the start of video time of the last scan line of the previous row. A load to the RSR during vertical blanking will also load the TOPR.

Table 2. Register Load Truth Table

Register Select A	Register Select B	Register Load Input	Register Access
0	0	0	No Select
0	1	0	Top-of-Page
1	0	0	Row Start*
1	1	0	Cursor
X	X	1	No Select

*During vertical blanking a load to this register will also load the top-of-page register.

VIDEO RELATED OUTPUTS

Horizontal Sync: This output provides the necessary line (scan) rate sync to either three-terminal or composite sync monitors. The pulse is programmable in position and width at character time increments. This output may also be programmed to have RS-170 compatible serration pulses during the vertical sync interval. The active logic state of this output is also programmable.

Vertical Sync: This output provides the necessary frame rate sync consistent with either three-terminal or composite type monitors. The pulse is programmable in position and width at line (scan) time increments. The active logic state of this output is also programmable.

Cursor Enable: When a match with the CRTC cursor address register and address counter occurs a pulse will appear at this output at that video character time (character field width) for every line in that row. This output may also be programmed to appear on only one line of a character row. With the character generator program pin in a logic "0" position the cursor enable output will not be valid on the last line of a character row for that row. Like the Load Video Shift Register Output, this output is not active during horizontal or vertical blanking. High level active output.

CRT SYSTEM CONTROL FUNCTIONS

50/60 Hz Control Input: This input controls the CRT system refresh rate. The CRTC may also be programmed for refresh rates other than 50 and 60 Hz.

50/60 Hz Control	Refresh Rate
1	60 Hz (f_1)
0	50 Hz (f_0)

Vertical Blanking Output: This output becomes active (logic "1") at the start of vertical blanking and may be programmed to stop at the end of any line of the character row before the start of the first video row. This output is useful for flag applications to other elements in the CRT system. Its active level is also programmable.

System Clear Input: This input when low sets and holds the CRTC at the start of vertical blanking for system sync and test. It also clears to zero the cursor and top-of-page registers. The input has hysteresis and may be connected to a resistor to V_{CC} and a capacitor to ground to provide power-up system clear.

Character Generator Program Input: This input modifies both the position of the recirculate enable output low level and the time at which the address outputs change to a new row address. It is intended to provide optimum use of the CRTC with character generator/ROMs programmed with or without active video on the first or last line of a character row. (See Recirculate Enable for truth table.)

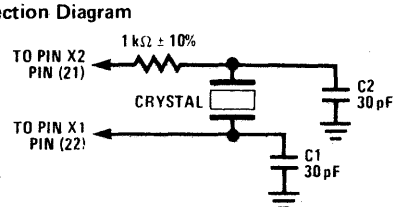
External Character/Line Rate Clock: This input is intended to aid testing of the CRTC and is not meant to be used as an active input in a CRT system. When this input is left open it is guaranteed not to interfere with normal operation.

Crystal Inputs X1 and X2: The oscillator is controlled by an external, parallel resonant crystal connected between the X1 and X2 pins. Normally, a fundamental mode crystal is used to determine the operating frequency of the oscillator; however, overtone mode crystals may be used.

Crystal Specifications (parallel resonant):

Type . . . . . AT-Cut Crystal
Tolerance . . . . . 0.005% at 25°C
Stability . . . . . 0.01% from 0°C to +70°C
Resonance . . . . . Fundamental (parallel)
Maximum Series Resistance . . . . . Dependent on frequency (for 10.92 MHz, 50 Ω)
Load Capacitance . . . . . 20 pF

Connection Diagram



If the DP8350 series is clocked at dot rate by a system clock, pin 22 (X1 input) should be clocked directly using a Schottky series circuit. Pin 21 (X2 input) may be left open.

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Timing Waveforms

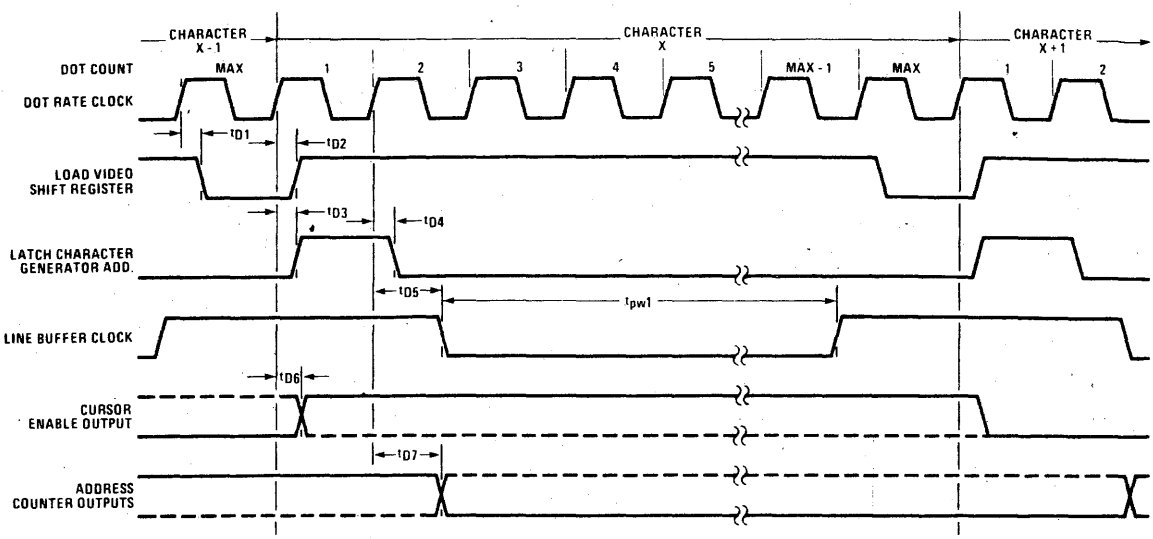
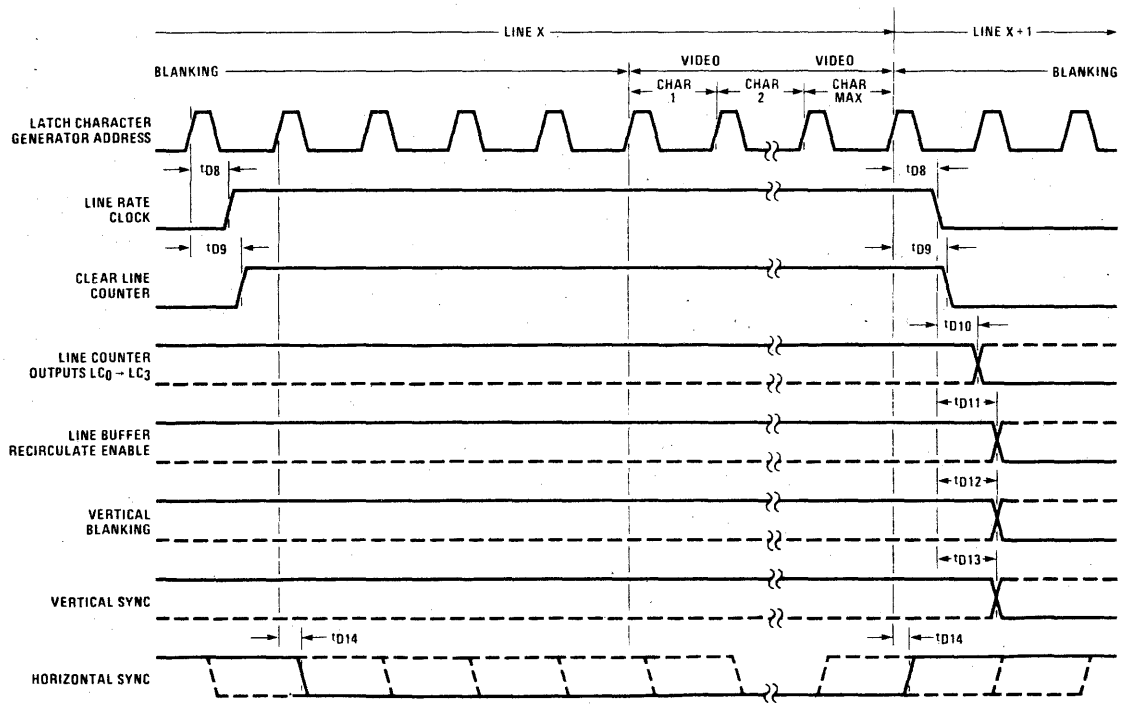


Figure 1. Dot/Character Rate Timing

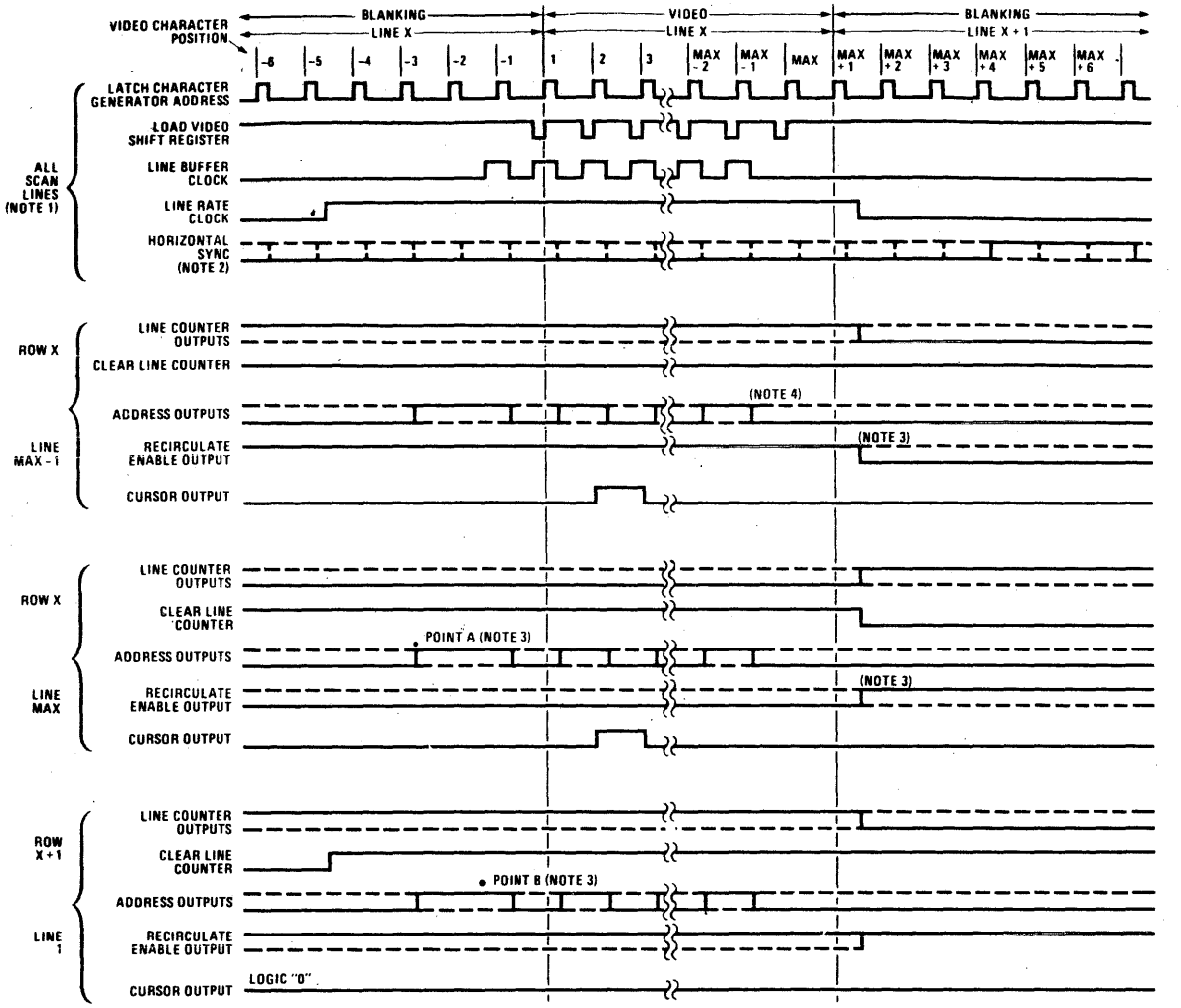


*THE POSITION OF THE START AND STOP POINTS OF THE HORIZONTAL SYNC PULSE ARE PROGRAMMABLE BY CHARACTER TIME – WITHIN ONE CHARACTER TIME THE POINTS WILL HAVE THE t_{D14} TIME RELATIONSHIP.

Figure 2. Character/Line Rate Timing

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Timing Waveforms (cont'd.)



Note 1: The load video shift register output is not active during vertical or horizontal blanking (remains in the logic "1" state during these intervals.

Note 2: The horizontal sync output start and stop point positions are user-programmable at character width intervals.

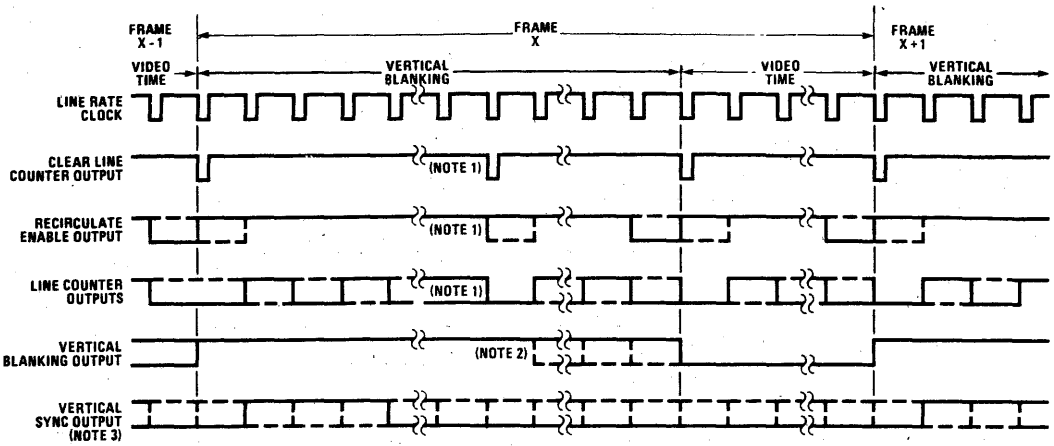
Note 3: The position of the recirculate enable output logic "0" level is dependent on the state of the character generator program input (CGPI). With CGPI = "0," recirculate enable occurs on the max line of a character row (solid line) and the address counter outputs roll over to the new row address at point A. With CGPI = "1," recirculate enable occurs on the first line of a character row (dashed line) and the address counter outputs roll over to the new row address at point B.

Note 4: The address counter outputs clock to the address of the last character of a video row plus 1. This address is then held during the horizontal blanking interval until video minus three character times. At this point the outputs are modified to the contents of the Row Start Register (RSR). With no external loading of the RSR the contents will be either the character address of the first character in the present row or the character address of the first character of the next video row (depending on the state of the Character Generator Program input) which will be sequential from the last character address of the last row. If the RSR was loaded, then the address outputs will be modified to the contents of the register.

Figure 3. Character/Line Rate Functional Diagram

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Timing Waveforms (cont'd.)

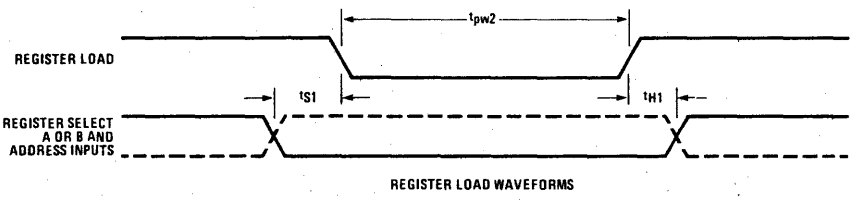


Note 1: One full row before start of video the line counter is set to zero state — this provides line counter synchronization in cases where the number of lines in vertical blanking are not even multiples of the number of lines per row.

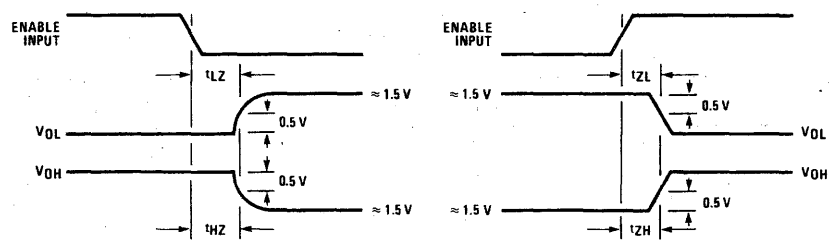
Note 2: The stop point of vertical blanking is programmable at line intervals within the last character row before start of video.

Note 3: The Vertical Sync Output start and stop points are programmable at line rate increments.

Figure 4. Line/Frame Rate Functional Diagram

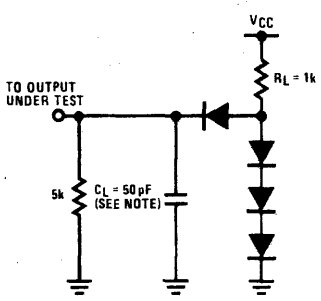


REGISTER LOAD WAVEFORMS

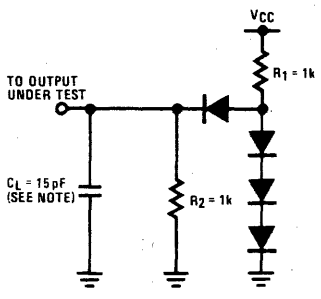


ADDRESS OUTPUTS ENABLE/DISABLE WAVEFORMS

Test Load Circuits



LOAD CIRCUIT 1



LOAD CIRCUIT 2

NOTE: C_L INCLUDES PROBE AND JIG CAPACITANCE
ALL DIODES ARE 1N914 OR EQUIVALENT.

Absolute Maximum Ratings (Note 1)

Supply Voltage, V_{CC}	7.0 V
Input Voltage	−1 V to +5.5 V
Output Voltage	5.5 V
Storage Temperature Range	−65°C to +150°C
Lead Temperature (soldering, 10 seconds)	300°C

Operating Conditions

	Min	Max	Units
V_{CC}, Supply Voltage	4.75	5.25	V
T_A, Ambient Temperature	0	+70	°C

Electrical Characteristics V_{CC} = 5 V ± 5%, T_A = 0°C to +70°C (Notes 2 and 3)

Parameter		Conditions	Min	Typ	Max	Units
V_{IH}	Logic "1" Input Voltage (System Clear)		2.6			V
	(All Other Inputs Except X1, X2)		2.0			V
V_{IL}	Logic "0" Input Voltage (System Clear)				0.8	V
	(All Other Inputs Except X1, X2)				0.8	V
$V_{IH}-V_{IL}$	System Clear Input Hysteresis			0.4		V
V_{clamp}	Input Clamp Voltage (All Inputs Except X1, X2, & Char/Line Rate Clock)	I_{IN} = −12 mA		−0.8		V
I_{IH}	Logic "1" Input Current (Address Outputs)	Enable Input = 0 V, V_{CC} = 5.25 V, V_R = 5.25 V		10		μA
	(All Other Inputs Except X1, X2)	V_{CC} = 5.25 V, V_R = 5.25 V		2		μA
I_{IL}	Input Current (Address Outputs)	Enable Input = 0 V, V_{CC} = 5.25 V, V_{IN} = 0.5 V		−20		μA
	(All Other Inputs Except X1, X2)	V_{CC} = 5.25 V, V_{IN} = 0.5 V		−20		μA
V_{OH}	Logic "1" Output Voltage	I_{OH} = −100 μA	3.2	4.1		V
		I_{OH} = −1 mA	2.5	3.3		V
V_{OL}	Logic "0" Output Voltage	I_{OL} = 5 mA		0.35	0.5	V
I_{OS}	Output Short Circuit Current	V_{CC} = 5 V, V_{OUT} = 0 V, (Note 4)		−40		mA
I_{CC}	Power Supply Current	V_{CC} = 5.25 V		170		mA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: Unless otherwise specified, min/max limits apply across the 0°C to +70°C temperature range and the 4.75 V to 5.25 V power supply range. All typical values are for T_A = 25°C and V_{CC} = 5.0 V.

Note 3: All currents into device pins are shown as positive; all currents out of device pins are shown as negative; all voltages are referenced to ground, unless otherwise specified. All values shown as max or min are so classified on absolute value basis.

Note 4: Only one output at a time should be shorted.

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Switching Characteristics V_{CC} = 5.0V, T_A = 25°C (Notes 1 and 2)

	Parameter	Conditions	Min	Typ	Max	Unit
t_{D1}	Dot Clock to Load Video Shift Register Negative Edge	C_L = 50pF, R_L = 1kΩ, Load Circuit 1		5		ns
t_{D2}	Dot Clock to Load Video Shift Register Positive Edge	C_L = 50pF, R_L = 1kΩ, Load Circuit 1		11		ns
t_{D3}	Dot Clock to Latch Character Generator Positive Edge	C_L = 50pF, R_L = 1kΩ, Load Circuit 1		11		ns
t_{D4}	Dot Clock to Latch Character Generator Negative Edge	C_L = 50pF, R_L = 1kΩ, Load Circuit 1		4		ns
t_{D5}	Dot Clock to Line Buffer Clock Negative Edge	C_L = 50pF, R_L = 1kΩ, Load Circuit 1		20		ns
t_{PW1}	Line Buffer Clock Pulse Width	C_L = 50pF, R_L = 1kΩ, Load Circuit 1		N(DT)*		ns
t_{D6}	Dot Clock to Cursor Enable Output Transition	C_L = 50pF, R_L = 1kΩ, Load Circuit 1		25		ns
t_{D7}	Dot Clock to Valid Address Output	C_L = 50pF, R_L = 1kΩ, Load Circuit 1		20		ns
t_{D8}	Latch Character Generator to Line Rate Clock Transition	C_L = 50pF, R_L = 1kΩ, Load Circuit 1		300+2DT		ns
t_{D9}	Latch Character Generator to Clear Line Counter Transition	C_L = 50pF, R_L = 1kΩ, Load Circuit 1		400+2DT		ns
t_{D10}	Line Rate Clock to Line Counter Output Transition	C_L = 50pF, R_L = 1kΩ, Load Circuit 1		180		ns
t_{D11}	Line Rate Clock to Line Buffer Recirculate Enable Transition	C_L = 50pF, R_L = 1kΩ, Load Circuit 1		200		ns
t_{D12}	Line Rate Clock to Vertical Blanking Transition	C_L = 50pF, R_L = 1kΩ, Load Circuit 1		200		ns
t_{D13}	Line Rate Clock to Vertical Sync Transition	C_L = 50pF, R_L = 1kΩ, Load Circuit 1		200		ns
t_{D14}	Latch Character Generator to Horizontal Sync Transition	C_L = 50pF, R_L = 1kΩ, Load Circuit 1		100		ns
t_{SI}	Register Select/Memory Address Setup Time Prior to Register Load Negative Edge			100		ns
t_{HI}	Register Select Memory Hold Time After Register Load Positive Edge			0		ns
t_{PW2}	Register Load Pulse Width			150		ns
f_{MAXdot}	Maximum Dot Rate Frequency			25		MHz
$f_{MAXchar}$	Maximum Character Rate Frequency			2.5		MHz
t_{LZ}, t_{HZ}	Delay from Enable Input to High Impedance State from Logic "0" and Logic "1"	C_L = 15pF, Load Circuit 2		25		ns
t_{ZL}, t_{ZH}	Delay from Enable Input to Logic "0" and Logic "1" from High Impedance State	C_L = 15pF, Load Circuit 2		25		ns

Note 1: Unless otherwise specified, all AC measurements are referenced to the 1.5V level of the input to 1.5V of the output.

Note 2: When external clock inputs are used, the input characteristics are Z_{OUT} = 50Ω and $t_R \leq 10$ns, $t_F \leq 10$ns.

*"DT" is defined as the duration (in ns) of one full cycle of the Dot Rate Clock (Item 20 of the ROM Program Table). "N" denotes the number of DTs per definition in Item 24 of the ROM Program Table.

DP8350 Series Option Program Table (Notes 1, 2, and 3)

Item No.	Parameter		Value	
1	Character (Font Size)	Dots per Character		
2		Scan Lines per Character		
3	Character Field (Block Size)	Dots per Character		
4		Scan Lines per Character		
5	Number of Video Characters per Row			
6	Number of Video Character Rows per Frame			
7	Number of Video Scan Lines (Item 4 x Item 6)			
8	Frame Refresh Rate (Hz) (two frequencies allowed)		f1 =	f0 =
9	Delay after/before Vertical Blank start to start of Vertical Sync (+/– Number of Scan Lines)			
10	Vertical Sync Width (Number of Scan Lines)			
11	Delay after Vertical Blank start to start of Video (Number of Scan Lines)			
12	Total Scan Lines per Frame (Item 7 + Item 11 = Item 13 ÷ Item 8)			
13	Horizontal Scan Frequency (Line Rate) (kHz) Item 8 x Item 12)			
14	Number of Character Times per Scan Line			
15	Character Clock Rate (MHz) Item 13 x Item 14)			
16	Character Time (ns) (1 ÷ Item 15)			
17	Delay after/before Horizontal Blank start to Horizontal Sync Start (+/– Character Times)			
18	Horizontal Sync Width (Character Times)			
19	Dot Frequency (MHz) (Item 3 x Item 15)			
20	Dot Time (ns) (1 ÷ Item 19)			
21	Vertical Blanking Stop before start of Video (Number of Scan Lines) (Range = Item 4 – 1 line to 0 lines)			
22	Cursor Enable on all Scan Lines of a Row? (Yes or No) If not, which Line?			
23	Does the Horizontal Sync Pulse have Serrations during Vertical Sync? (Yes or No)			
24	Width of Line Buffer Clock logic "0" state within a Character Time (Number of Dot Time increments)			
25	Serration Pulse Width, if used (Character Times)			
26	Horizontal Sync Pulse Active state logic level (1 or 0)			
27	Vertical Sync Pulse Active state logic level (1 or 0)			
28	Vertical Blanking Pulse Active state logic level (1 or 0)			

Note 1: If the Cursor Enable, Item 22, is active on only one line of a character row, then Item 21 must be either "1" or "0" unless it is the same as the line selected for Cursor Enable.

Note 2: Item 24 x Item 20 should be > 250 ns.

Note 3: Item 11 must be greater than Item 4 + 1.

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DP8350 Series Option Program Table

DP8350 Option: 80 Characters x 24 Rows, 5 x 7 Character Font, 7 x 10 Character Field

Item No.	Parameter		Value	
1	Character (Font Size)	Dots per Character	5	
2		Scan Lines per Character	7	
3	Character Field (Block Size)	Dots per Character	7	
4		Scan Lines per Character	10	
5	Number of Video Characters per Row		80	
6	Number of Video Character Rows per Frame		24	
7	Number of Video Scan Lines (Item 4 x Item 6)		240	
8	Frame Refresh Rate (Hz) (two frequencies allowed)		f1 = 60 Hz	f0 = 50 Hz
9	Delay after/before Vertical Blank start to start of Vertical Sync (+/– Number of Scan Lines)		4	30
10	Vertical Sync Width (Number of Scan Lines)		10	10
11	Delay after Vertical Blank start to start of Video (Number of Scan Lines)		20	72
12	Total Scan Lines per Frame (Item 7 + Item 11 = Item 13 ÷ Item 8)		260	312
13	Horizontal Scan Frequency (Line Rate) (kHz) Item 8 x Item 12)		15.6 kHz	
14	Number of Character Times per Scan Line		100	
15	Character Clock Rate (MHz) Item 13 x Item 14)		1.56 MHz	
16	Character Time (ns) (1 ÷ Item 15)		641 ns	
17	Delay after/before Horizontal Blank start to Horizontal Sync Start (+/– Character Times)		0	
18	Horizontal Sync Width (Character Times)		43	
19	Dot Frequency (MHz) (Item 3 x Item 15)		10.920 MHz	
20	Dot Time (ns) (1 ÷ Item 19)		91.6 ns	
21	Vertical Blanking Stop before start of Video (Number of Scan Lines) (Range = Item 4 – 1 line to 0 lines)		1	
22	Cursor Enable on all Scan Lines of a Row? (Yes or No) If not, which Line?		Yes	
23	Does the Horizontal Sync Pulse have Serrations during Vertical Sync? (Yes or No)		No	
24	Width of Line Buffer Clock logic "0" state within a Character Time (Number of Dot Time increments)		4	
25	Serration Pulse Width, if used (Character Times)		–	
26	Horizontal Sync Pulse Active state logic level (1 or 0)		1	
27	Vertical Sync Pulse Active state logic level (1 or 0)		0	
28	Vertical Blanking Pulse Active state logic level (1 or 0)		1	

FULL/HALF ROW CONTROL (PIN 5)

Device pin 5 converts the DP8350 programmed display from 80 characters by 24 rows to 80 characters by 12 rows.

Full/Half Row (Pin 5) Logic State	Display Size
1	80 by 24
0	80 by 12

With pin 5 in logic "0" state, the 12 character rows are equally spaced vertically on the CRT. Each row is spaced by one full row of blanked video.

Also in this mode the address counter outputs address the same memory space for two rows – the video row and the blanked row. Thus one half of the CRT memory space is addressed with pin 5 in logic "0" state as compared to pin 5 in logic "1" state.

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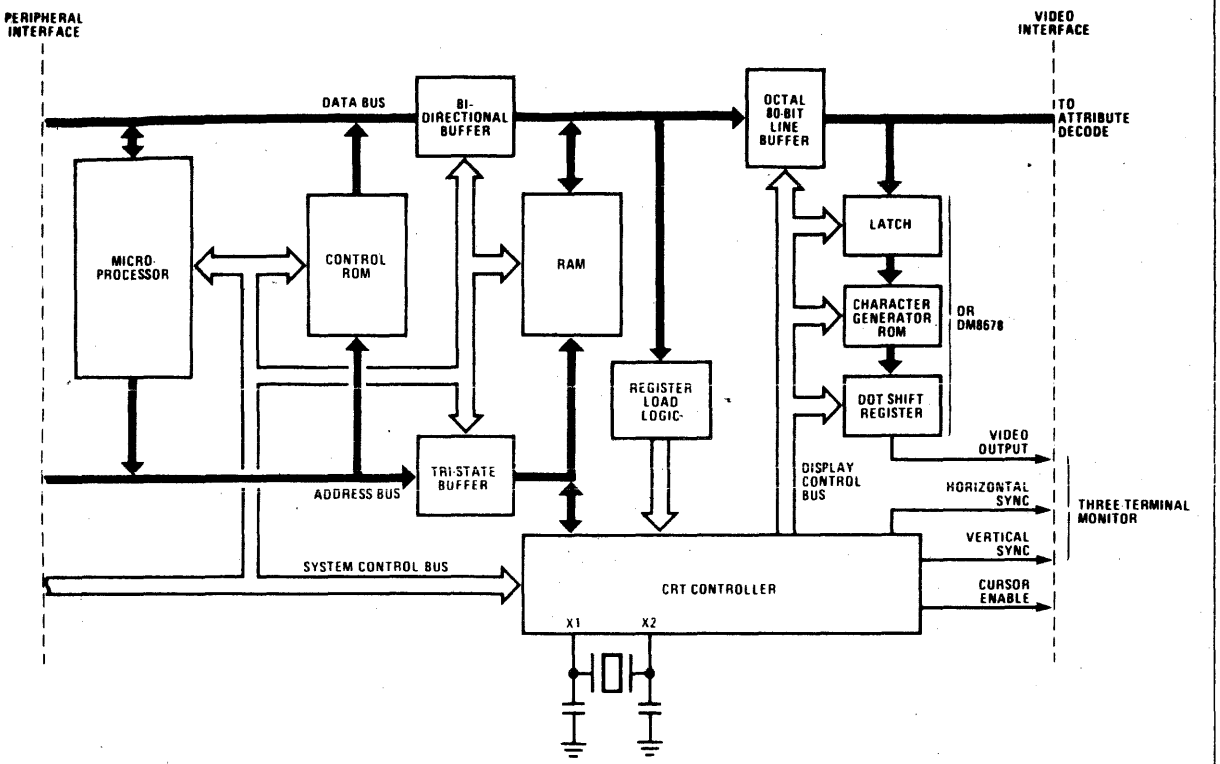


Figure 6. System Diagram Using a Line Buffer

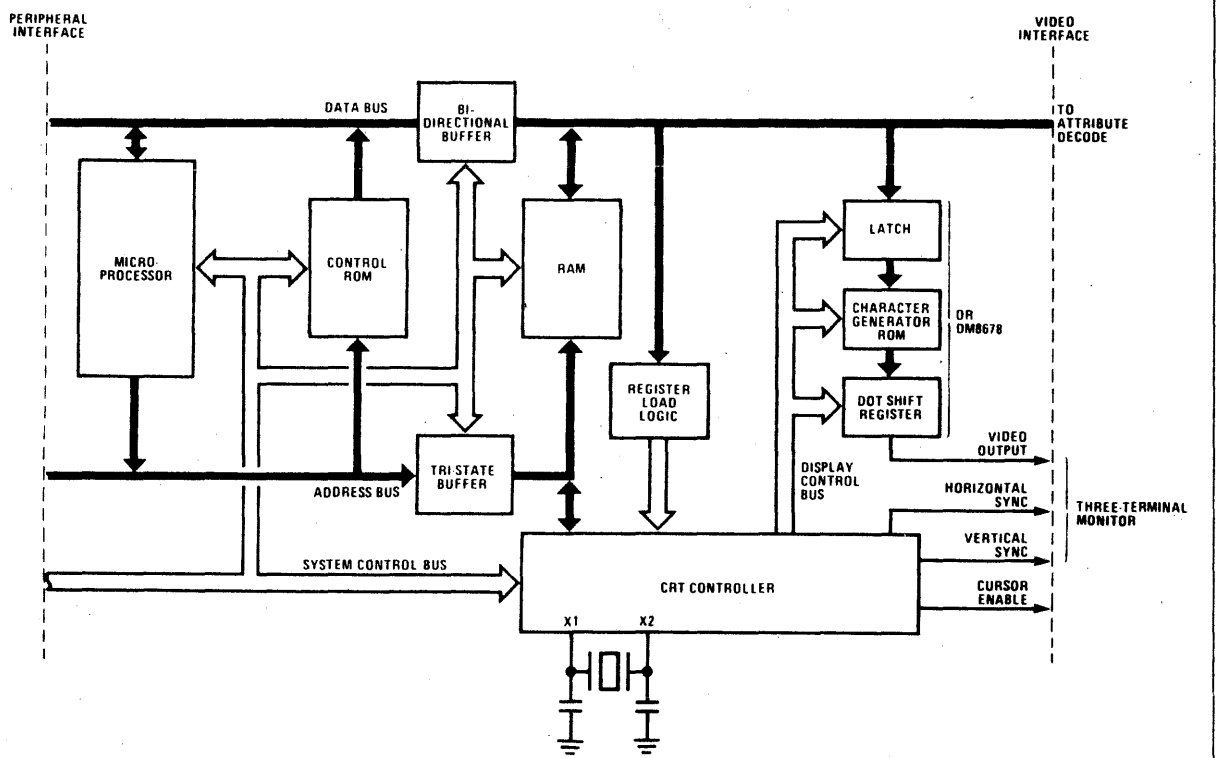


Figure 7. System Diagram with no Line Buffer

"TURN TO PAGES 238, 297 FOR FULL APPLICATION NOTE"

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NE580-F,N

DESCRIPTION

The NE580 is a dual bar-graph logic circuit designed to provide all the functions necessary to drive a gas discharge self-scan ™ bar-graph panel. The NE580 is configured to drive a 201 element bar-graph in either 5 or 6 phase operation. Phase number selection is obtained by applying a logic 0 or 1 level to the phase select pin. 3 phase operation for a 101 element device can be attained by a wire-or connection of adjacent cathode phase outputs.

The device inputs accept an analog voltage in the range 0 to 2.5V and performs an A/D conversion with reference to a fixed input voltage at the reference terminal. On-chip functions include a clock generator, linear ramp generator, control logic and ROM decoding. Output functions comprise 2 anode control lines, 2 overrange indication outputs, 6 cathode phase outputs and 1 cathode reset output. Refer to the system block diagram for clarification.

A minimum of external components are required for the whole conversion and display system shown in the typical application. The NE580 can be expanded to handle more analog channels using external comparators. Either LM393A or LM339A type comparators will function well. A few external low-cost logic packages can in addition provide binary or BCD encoded data to interface with a logic control system.

The device is supplied in a 22-pin plastic molded or ceramic dual-in-line package.

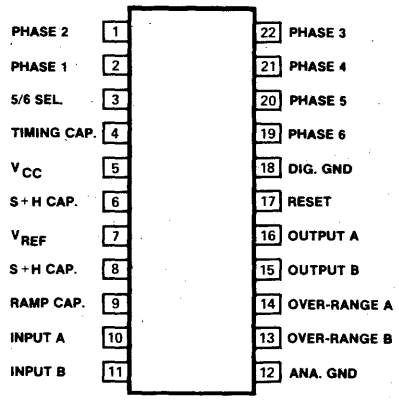
™-self-scan is a trademark of Burroughs Corporation.

FEATURES

- **Dual channel device**
- **Easily expandable to handle more channels.**
- **Single 5 volt supply**
- **3, 5 or 6 phase operation**
- **Can be custom masked for different cathode segment counts, (maximum 240)**
- **Equivalent 8-bit resolution of displayed information.**
- **Overrange indication outputs.**

PIN CONFIGURATION

F,N PACKAGE



ORDERING INFORMATION

Plastic DIL package—NE580N
Cerdip package—NE580F

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Supply voltage, V_{CC}	+7	V
Output voltage (all outputs)	$+V_{CC}$	V
Analog input voltage range	-0.3 to +7	V
Reference voltage input	$+V_{CC}$	V
Phase select input	+5.5	V
Analog/digital ground voltage differential	±0.3	V
Power dissipation		
plastic	500	mW
cerdip*	800	mW
Operating temperature range	0 to +70	°C
Storage temperature range	-65 to +150	°C
Soldering temperature (10sec)	300	°C

*NOTE

The plastic 22 pin package has a thermal impedance θ_{JA} of 120°C/W and the cerdip package, θ_{JA} of 75°C/W. Provided the maximum junction temperature is kept below 150°C then more power may be dissipated to a maximum of 1 watt.

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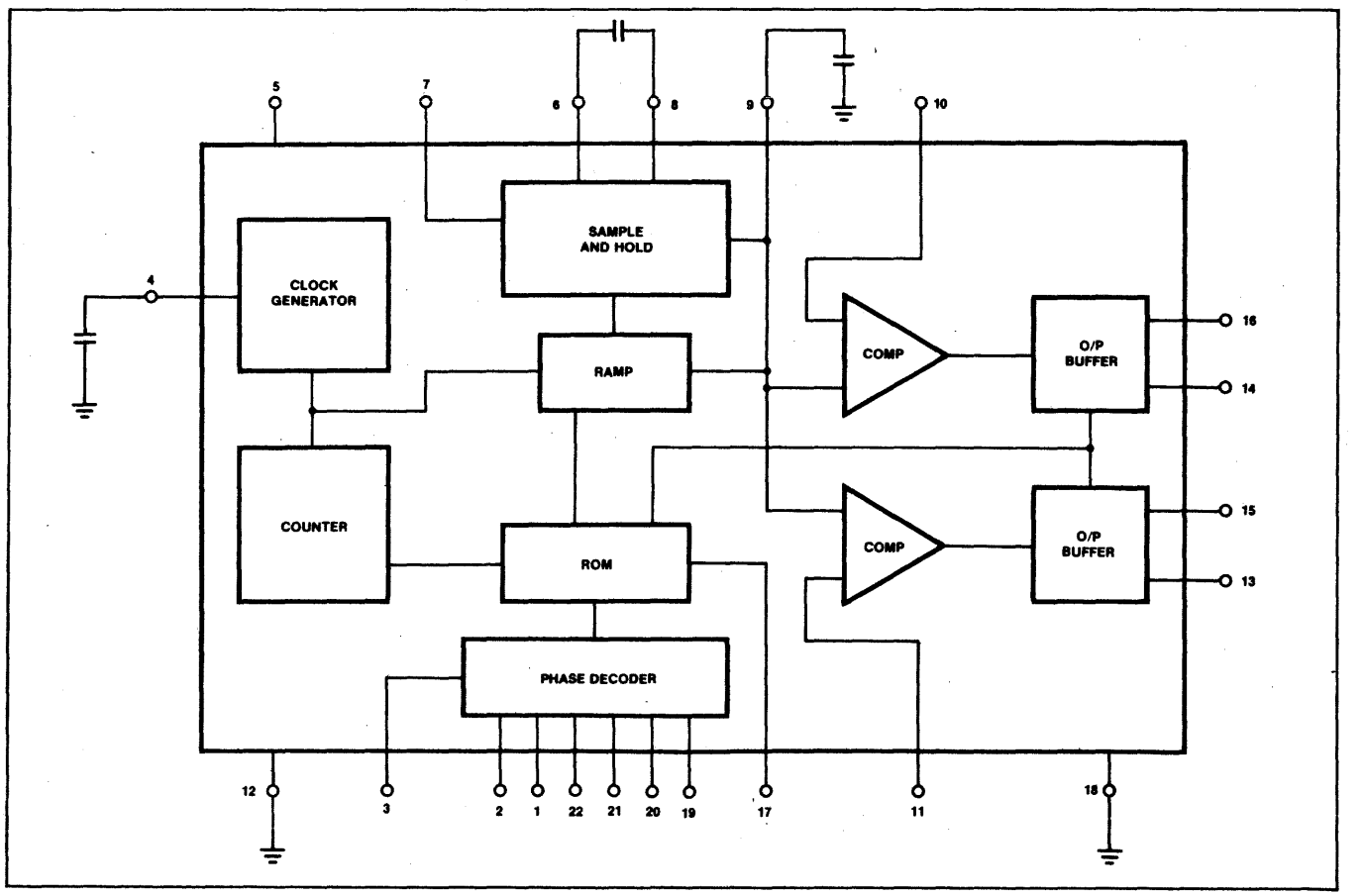
DC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_{CC} = 5V$ unless otherwise specified.

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
	Operating supply voltage range		4.75	5.0	5.25	V
V_{IN}	Input voltage range		0		2.5	V
V_{REF}	Applied reference voltage[1]		0		2.5	V
I_{BREF}	Bias current at reference voltage input	$V_{REF} = 2.5V$		500		nA
i_{IB}	Bias current at analog input	$V_{REF} = 2.5V$, $V_{IN} = 0V$		500		nA
$V_{OUT\ (1)}$	All outputs[2]	$I_{OUT} = -500\mu A$		3.5		V
$I_{OUT\ (1)}$	All outputs[2]	$V_{OUT} = 1.5V$		-1.0		mA
$I_{OUT\ (sc)}$	All outputs[2]	$V_{OUT} = 0V$		-1.5		mA
$V_{OUT\ (0)}$	All outputs	$I_{SINK} = 1.6mA$			0.4	V
F_C	Clock generator frequency	Timing capacitor $= .022\mu F$		25		KHz
Accuracy		$2V \leq V_{REF} \leq 2.5V$, $V_{IN} = V_{REF}$		±1		bar
I_{CC}	Supply current			50		mA

NOTES

1. Displayed accuracy is a function of reference voltage. Values of V_{REF} below 2 volts will impair conversion accuracy.
2. All logic outputs comprise an NPN transistor with 3kΩ pull-up resistor to 5 volts.

BLOCK DIAGRAM



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NE590-F,N • NE591-F,N

DESCRIPTION

The NE590/591 addressable peripheral drivers are high current latched drivers, similar in function to the 9334 address decoder. The device has 8 Darlington power outputs, each capable of 250mA load current. The outputs are turned on or off by respectively loading a logic high or logic low into the device data input. The required output is defined by a 3-bit address. The device must be enabled by a $\overline{CE}$ input line which also serves the function of further address decoding. A common clear input, $\overline{CLR}$, turns all outputs off when a logic low is applied.

The NE590 has 8 open collector Darlington outputs which sink current to ground. The device is packaged in a 16-pin molded or cerdip package.

The NE591 has 8 open emitter Darlington outputs which source current to an external load from a common collector line, V_S. This V_S line need not necessarily be the same as the 5 volt V_{CC} supply. The device is packaged in an 18-pin molded or cerdip package.

FEATURES

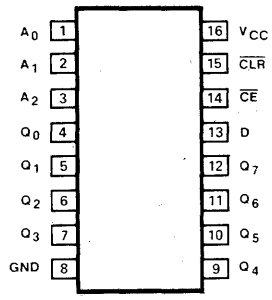
- **8 high current outputs**
- **Low-loading bus compatible inputs**
- **Power-on clear ensures safe operation**
- **NE590 will operate in addressable or demultiplex mode**
- **Allows random (addressed) data entry**
- **Easily expandable**
- **NE590 is pin compatible with 9334**

APPLICATIONS

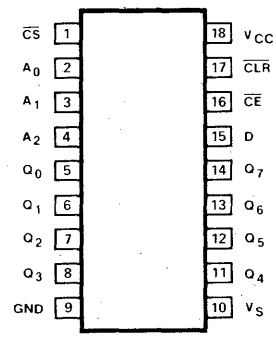
- **Relay driver**
- **Indicator lamp driver**
- **Triac trigger**
- **LED display digit driver**
- **Stepper motor driver**

PIN CONFIGURATIONS

NE590
F,N PACKAGE



NE591
F,N PACKAGE



PIN DESIGNATION

590 PIN NO.	591 PIN NO.	SYMBOL	NAME & FUNCTION
1-3	2-4	A_0-A_2	A 3-bit binary address on these pins defines which of the 8 output latches is to receive the data.
4-7, 9-12	5-8, 11-14	Q_0-Q_7	The 8 device outputs. The NE590 has open collector Darlington outputs. The NE591 has open emitter follower outputs.
13	15	D	The data input. When the chip is enabled, this data bit is transferred to the defined output such that: "1" turns output switch "ON" "0" turns output switch "OFF" Thus in logic terms, the NE590 inverts data to the relevant output. The NE591 retains true data at the output.
14	16	$\overline{CE}$	The chip enable. When this input is low, the output latches will accept data. When $\overline{CE}$ goes high, all outputs will retain their existing state, regardless of address or data input conditions.
15	17	$\overline{CLR}$	The clear input. When $\overline{CLR}$ goes low all output switches are turned "OFF". On the NE590, a high data input will override the clear function on the addressed latch. On the NE591, $\overline{CLR}$ low will override any other condition.
—	1	$\overline{CS}$	The chip select input provides for an additional level of address decoding.
—	10	V_S	The V_S line provides the power to all 8 output devices. It is connected to the collectors of all 8 output transistors. This pin may be connected to the V_{CC} or another supply.

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DESCRIPTION

The NE5018 is a complete 8-bit digital to analog converter subsystem on one monolithic chip. The data inputs have input latches, controlled by a latch enable pin. The data and latch enable inputs are ultra-low loading for easy interfacing with all logic systems. The latches appear transparent when the $\overline{LE}$ input is in the low state. When $\overline{LE}$ goes high, the input data present at the moment of transition is latched and retained until $\overline{LE}$ again goes low. This feature allows easy compatibility with most micro-processors.

The chip also comprises a stable voltage reference (5V nominal) and a high slew rate buffer amplifier. The voltage reference may be externally trimmed with a potentiometer for easy adjustment of full scale, while maintaining a low temperature co-efficient.

The output of the buffer amplifier may be offset so as to provide bipolar as well as unipolar operation.

FEATURES

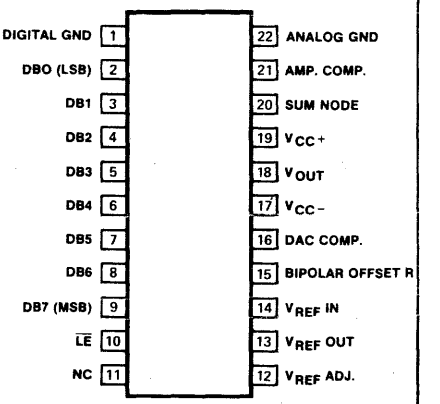
- **8-bit resolution**
- **Input latches**
- **Low-loading data inputs**
- **On-chip voltage reference**
- **Output buffer amplifier**
- **Accurate to ± 1/4 LSB (.1%)**
- **Monotonic to 8 bits**
- **Amplifier and reference both short-circuit protected**
- **Compatible with 2650,8080 and many other μP's**

APPLICATIONS

- **Precision 8-bit D/A converters**
- **A/D converters**
- **Programmable power supplies**
- **Test equipment**
- **Measuring instruments**
- **Analog-digital multiplication**

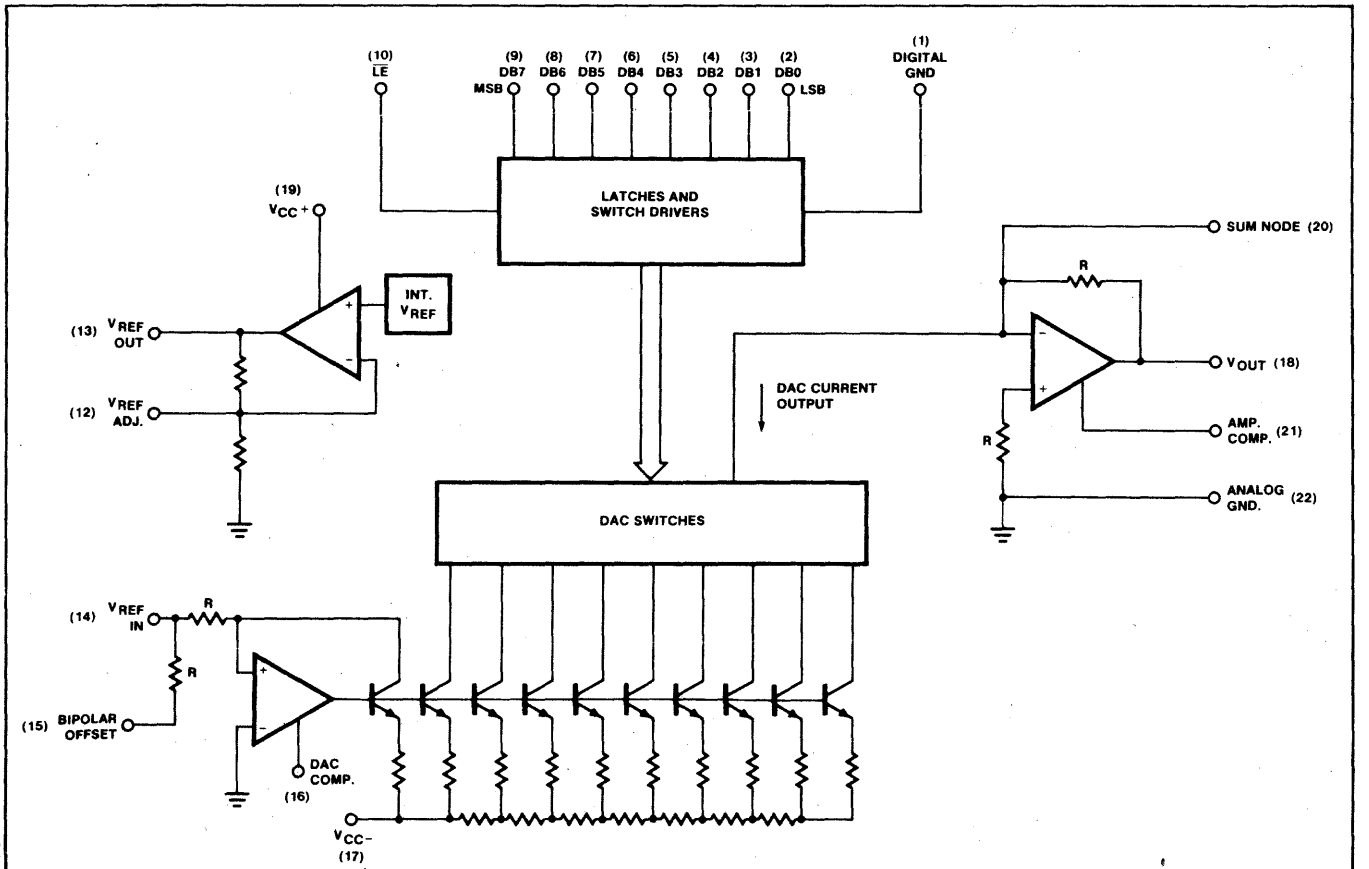
PIN CONFIGURATION

F,N PACKAGE



SE/NE5018 available in F package only.

BLOCK DIAGRAM



All R values equal 5KΩ and are thermally matched.

Figure 1

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10-BIT μP-COMPATIBLE D/A CONVERTER — NE 5020

DESCRIPTION

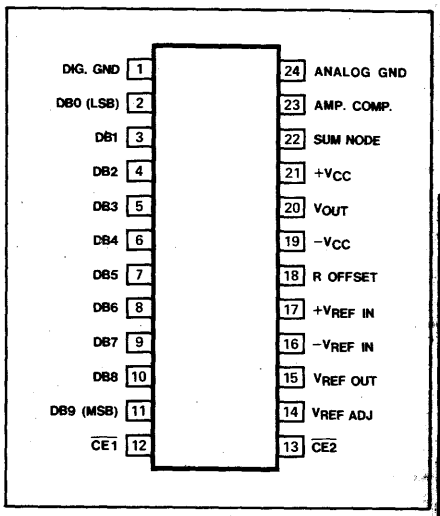
The NE5020 is a 10-bit voltage output D/A converter similar in design to the NE5018 8-bit DAC. The chip incorporates an R-2R ladder, input data latches, a voltage reference and an output operational amplifier. The divice can be configured for either unipolar or bipolar operation.

The 10 bits of digital data may be loaded into the latches simultaneously or as 2 bits of 2 and 8 bits respectively. $\overline{CE1}$ latches the 2 most significant bits. $\overline{CE2}$ latches the 8 least significant bits. $\overline{CE1}$ and $\overline{CE2}$ are tied together to load 10 bits in parallel. When loading from an 8 bit data bus $\overline{CE1}$ and $\overline{CE2}$ are controlled separately, and the 2 MSBs may be paralleled with any 2 of the least 8 significant bits.

FEATURES

- **10-bit resolution**
- **±0.05% accuracy**
- **Monotonic to 10-bits**
- **Unipolar (0 to 10V) and bipolar (−5 to +5V) operation**
- **10-bit data can be loaded from 8-bit data bus.**
- **Settling time - 5μs**
- **Latch enable pulse width 200ns minimum.**

PIN CONFIGURATION



INTERFACE

Signetics

ANALOG TO DIGITAL CONVERTER — NE5034

PRELIMINARY SPECIFICATIONS

NE5034-N,F

DESCRIPTION

The 5034 is an 8-bit resolution analog-to-digital converter. The circuitry is arranged to provide maximum design flexability.

The 5034 contains all of the elements comprising a true 8-bit accuracy analog-to-digital converter on one monlithic chip. These elements include the internal logic, voltage reference, comparator, clock, and output buffers. The output buffers are microprocessor addressable for bus compatibility.

The 5034 achieves fast conversion time (17μsec, Typ) using a single external capacitor to set the internal clock frequency. Faster conversion times are possible using an external clock.

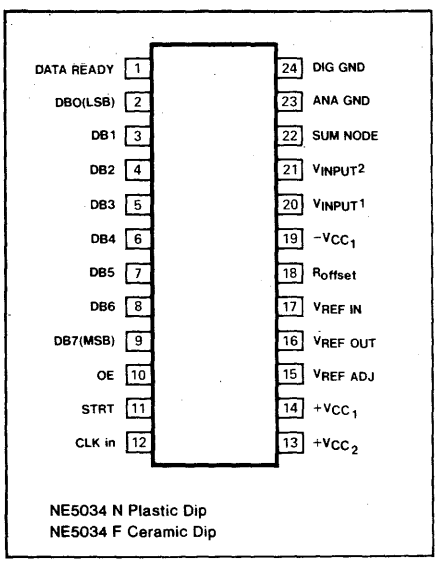
FEATURES

- **8-bit resolution and accuracy**
- **Micro-processor compatible logic**
- **Internal clock with external override for higher speed**
- **Pin programmable unipolar and bipolar inputs**
- **No missing codes over full operating temperature range**
- **System flexibility**

APPLICATIONS

- **A/D converters in micro-processor based systems**
- **High speed A/D systems**
- **Ratiometric A/D conversion**
- **Automated process controls**
- **Low cost A/D systems**

PIN CONFIGURATION



NE5034 N Plastic Dip
NE5034 F Ceramic Dip

SE5118-F • NE5118-N

DESCRIPTION

The NE5118 is a high-speed 8-bit digital to analog converter subsystem on one monolithic chip. The data inputs have input latches, controlled by a latch enable pin. The data and latch enable inputs are ultra-low loading for easy interfacing with all logic systems. The latches appear transparent when the $\overline{LE}$ input is in the low state. When $\overline{LE}$ goes high, the input data present at the moment of transition is latched and retained until $\overline{LE}$ again goes low. This feature allows easy compatibility with most microprocessors.

The chip also comprises a stable voltage reference (5V nominal). The voltage reference may be externally trimmed with a potentiometer for easy adjustment of full scale, while maintaining a low temperature co-efficient.

The output has high voltage compliance increasing versatility.

FEATURES

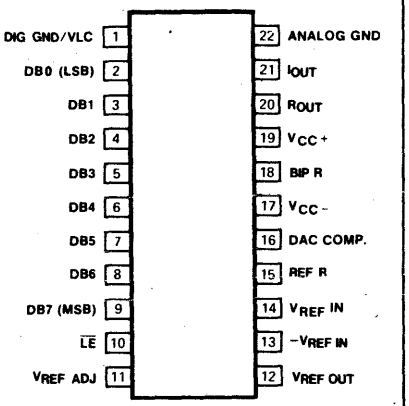
- 8-bit resolution
- Input latches
- Low-loading data inputs
- On-chip voltage reference
- Fast settling output current—200ns
- Accurate to ± 1/4 LSB
- Monotonic to 8 bits
- Reference short-circuit protected
- Compatible with 2650, 8080 and many other μP's

APPLICATIONS

- Precision 8-bit D/A converters
- A/D converters
- Programmable power supplies
- Test equipment
- Measuring instruments
- Analog-digital multiplication
- CRT display drivers
- High-speed modems

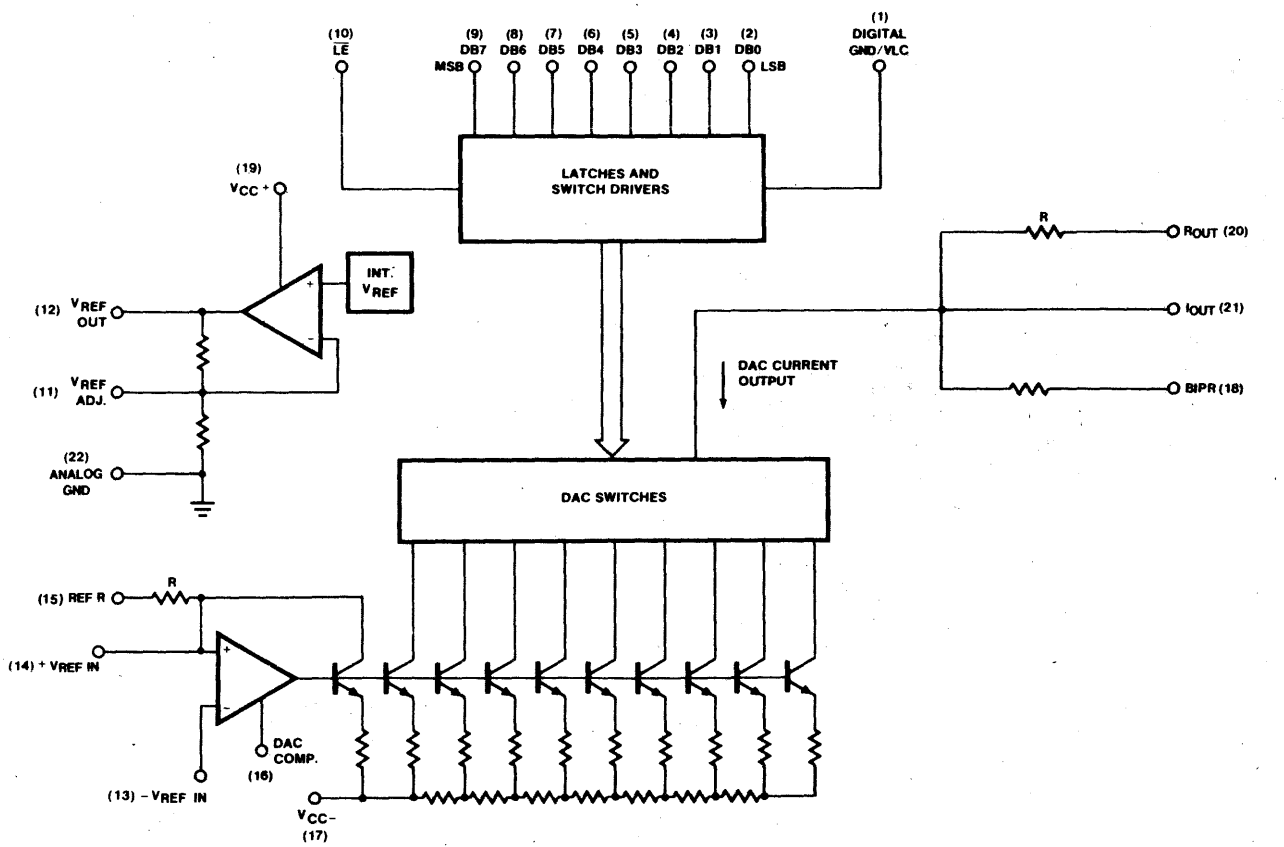
PIN CONFIGURATION

F,N PACKAGE



SE5118 available in F package only.

BLOCK DIAGRAM



All R values equal 5kΩ and are thermally matched.

Figure 1

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"I need to know if this device exists, and if there are any alternate sources. Where do I start?"

- Memory IC
- RAM
- Static
- 1024x1
- CMOS
- 250 Nanoseconds
- 5 Volts

If you're spending hours to solve a problem similar to the one above, you're behind the times...



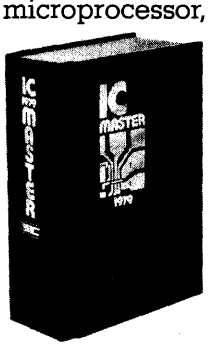
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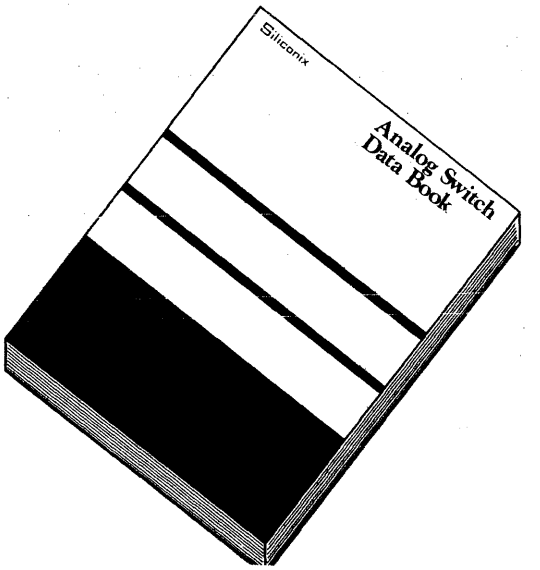
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Product Selector Guide by Applications



Send for Complete information in the New Analog Switch Data Book

Application	Feature of Application	Suggested Switches
Battery Operated or Battery Back-Up Supply	1) Low Power	**CMOS DG304-DG307** DG300-DG303, DG381-DG390 JFET DG126-DG164
	2) Minimum Number of Power Supplies	**CMOS DG300-DG307** (Can Also Be Used With Single Supply) CMOS DG200, DG201 (For MUX: DG506-DG509) (JFET DG126-DG164)
	3) Low Standby Power	**CMOS DG300-DG390** JFET DG126-DG164
Audio	1) Low Signal Distortion	**JFET DG180-DG191** CMOS DG300-DG390
	2) Low Noise	CMOS DG300-DG390 JFET DG180-DG191
	3) Wide Signal Range	**CMOS DG300-DG390** CMOS DG200, DG201 (MUX: DG506-DG509)
		JFET DG182, DG185, DG188, DG191
Video (High Frequency)	1) High OFF Impedance, Small Feedthrough of Signal	**JFET DG181, DG182, DG184, DG185, DG187, DG188, DG190, DG191** CMOS DG200, DG201 CMOS DG300-DG307, DG381-DG390
	2) Good Impedance Matching, Minimum Signal Drop Across Switch	**JFET DG180, DG183, DG186, DG189** DG181, DG184, DG187, DG190 CMOS DG300-DG390

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(Continued)

Application	Feature of Application	Suggested Switches
Differential Signal Switching	1) Good Matching of Switch Parameters	**CMOS DG300, DG302, DG303, DG304, DG306, DG307, DG381, DG384, DG390** CMOS DG200, DG201, DG507, DG509
	2) Low Thermocouple Offset Voltage	**JFET DG183, DG184, DG185 (10 Ω)**
		CMOS DG304, DG306, DG307 DG300, DG302, DG303 DG381, DG384, DG390
Small Signal (<1 V)	1) Low Noise	**JFET DG180, DG183, DG186, DG189** (Remainder of DG181-DG191 Family) CMOS DG300-DG390
	2) High Impedance Inputs or Load	**CMOS DG300-DG390** JFET DG181, DG182, DG184, DG185, DG187, DG188, DG190, DG191
	3) Low Thermocouple Offset Voltage	**CMOS DG304-DG307** DG300-DG303, DG381-DG390
		JFET DG180-DG191
Multiplexing	1) Break-Before-Make Switching	**CMOS DG506, DG507, DG508, DG509** PMOS DG501, DG503
	2) Binary Controlled Logic Inputs	
	3) Differential Multiplexing	CMOS DG507, DG509
	4) D/A Conversion	NMOS DG515, DG516
Sample and Hold	1) Low Droop Rate	**CMOS DG300-DG390** JFET DG180-DG191 CMOS DG200, DG201
	2) Low Sample to Hold Offset	**CMOS DG200, DG201** CMOS DG300-DG391 JFET DG181, DG182, DG184, DG185, DG187, DG188, DG190, DG191
	3) Fast Acquisition Speed	**JFET (10 Ω) DG180, DG183, DG186, DG189 (10 Ω)** Remainder of DG181-DG191 Family CMOS DG300, DG390 CMOS DG200, DG201
Switching to High Impedance Inputs	1) Low Error Voltage	**CMOS DG300, DG390** JFET DG180-DG191
	2) Low Switching Transient Error Voltage	**CMOS DG200, DG201** DG300-DG390
Low Cost	1) Best Performance for Lowest Cost	**CMOS DG200, DG201** DG300-DG390

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(Continued)

PMOS Medium Speed Analog Switches

DGM111	2XSPST	DG170	3XSPDT
DG116	4XSPST	DG171	SPST
DGM122	2XDPST	DG172	4XSPST
DG123	5XSPST	DG173	DPDT
DG125	5XSPST	DG175	SPDT

This series of analog switches contains 1-5 SPST functions as well as DPST, DPST, and DPDT functions. These switches interface with TTL/DTL logic.

- Analog Range ±10 V
- ON Resistance 50-450 Ω
- OFF Leakage 100 pA

TTL/DTL Compatible N-Channel Junction FET Analog Switches

DG126 through DG164

This series of analog switches includes SPST, DPST, and DPDT functions with low to medium ON resistance, constant over the analog voltage range, and medium speed.

- ON Resistance 10-80 Ω
- OFF Leakage 100 pA
- Standby Power 1 mW
- Analog Voltage Range ±10 V
- t_{ON} 600 nsec
- t_{OFF} 1.2 μsec

High Speed, High Frequency, DTL/TTL Compatible N-Channel Junction FET Analog Switches

DG180 through DG191

These switches feature very high switching speeds, high frequency signal handling capabilities, and constant ON resistance over analog voltage range.

- Analog Voltage Range ±10 V
- Break-Before-Make ±7.5 V
- t_{ON} 150 nsec
- t_{OFF} 100 nsec
- Signal Frequency Range 100 MHz

Medium Speed CMOS Switches and Analog Multiplexers

DG200	2XSPST
DG201	4XSPST
DG506	16 Channel MUX
DG507	8 Channel Diff. MUX
DG508	8 Channel MUX
DG509	4 Channel Diff. MUX

This series of CMOS switches features medium speed, low priced CMOS switches with voltage handling capabilities of ±15 V.

- V_{ANALOG} ±15 V
- Leakage 200 pA

High Speed, Low Power, Low R_{ON} CMOS Analog Switches

DG300-304-381	2XSPST
DG301-305-387	1XSPDT
DG302-306-384	2XDPST
DG303-307-390	2XSPDT

The DG300 series is a new group of CMOS devices featuring high speed, low R_{ON}, low power and ±15 V signal handling capabilities. DG300-309 have TTL/DTL/CMOS compatible inputs. DG304-307 have MOS compatible inputs and feature higher speed and lower power.

- R_{ON} 50 Ω
- t_{ON} 150 (TTL) 110 (CMOS)
- t_{OFF} 130 (TTL) 70 (CMOS)
- Power 5 μW (TTL) 1 μW (CMOS)
- Signal Frequency Range 100 MHz

8 Channel PMOS Multiplexer

DG501

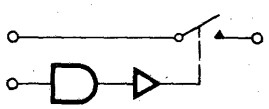
DG503

Low cost 8 channel multiplexer.

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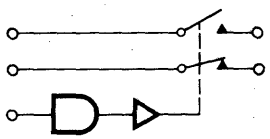
Siliconix drivers and associated FET switches are available as single-package integrated circuits. They are intended for applications where the switched analog signal must be isolated from the driving source and associated power supplies. Designs include monolithic devices with bipolar and Schottky transistors and MOSFETs on a single chip; monolithic CMOS switches and multiplexers; and multichip hybrids which combine discrete junction FET chips and a common driver in one package. The accompanying switch diagrams display a wide variety of switch functions. The devices shown in **boldface** are recommended parts for new designs.

SPST



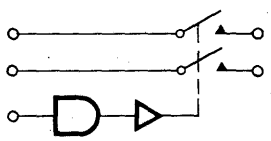
X2			X4	X5
DGM111	DG152	**DG300†**	**DG172***	DG123*
DG133	DG180	**DG304†**	**DG201†**	DG125*
DG134	DG181	**DG381†**		
DG141	DG182			
DG151	DG200†			

SPDT



X1		X2		X3
DG143	**DG187**			DG170*
DG144	**DG188**	DG189	**DG303†**	X4
DG146	**DG301†**	DG190	**DG307†**	DG515*
DG161	**DG305†**	DG191	**DG390†**	
DG162	**DG387†**			X10
DG186	Si3002*			DG516*

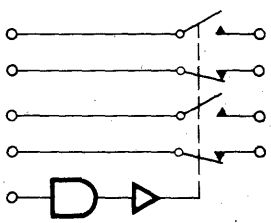
DPST



X2

DGM122*	DG183
DG126	**DG184**
DG129	**DG185**
DG140	**DG302†**
DG153	**DG306†**
DG154	**DG384†**

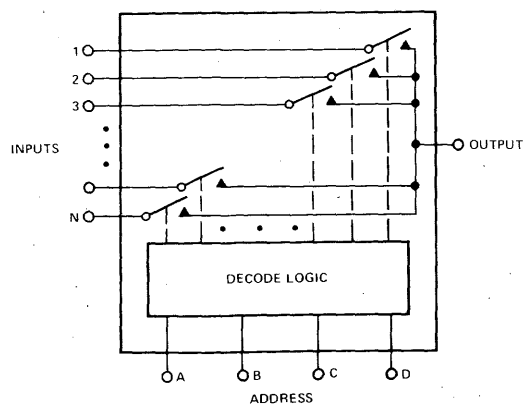
DPDT



X1

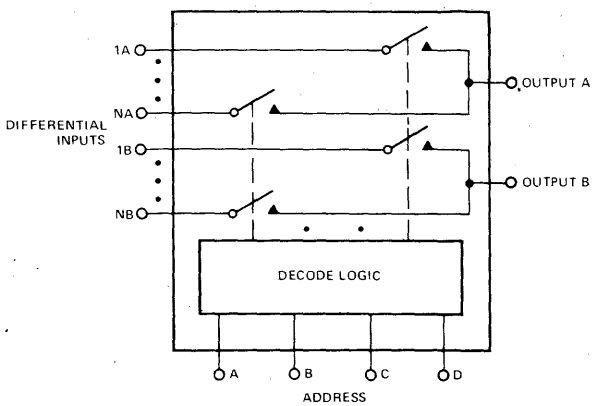
DG139	DG163
DG142	DG164
DG145	DG173*

MULTIPLEXER



8-Channel		16-Channel
DG501*	**DG508* †**	**DG506* †**
DG503*	Si3705*	

DIFFERENTIAL MULTIPLEXER



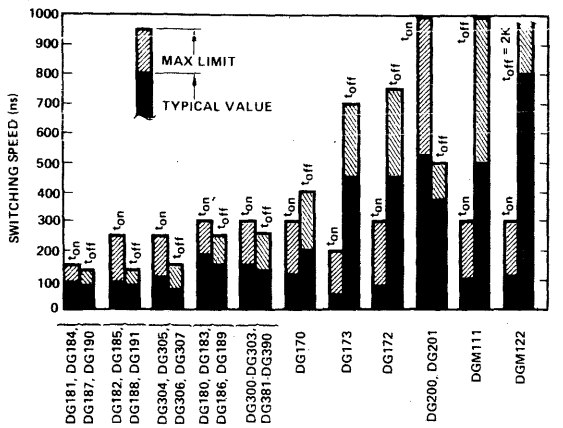
4-Channel	8-Channel
DG509* †	**DG507* †**

* Indicates one or more common drain connections † CMOS

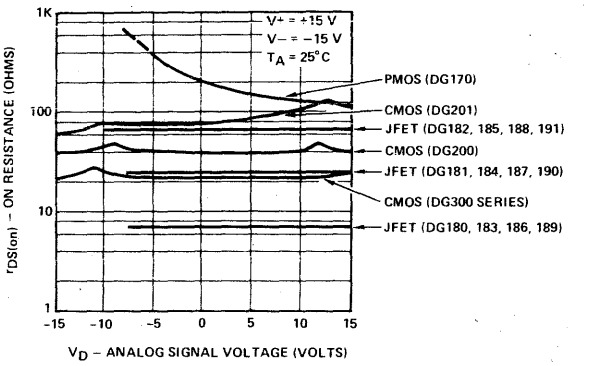
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TYPICAL PERFORMANCE CHARACTERISTICS

Typical Switching Speed



Typical $r_{DS(on)}$ vs V_D



NOTE: The CMOS switches are the only ones capable of switching signals down to the negative supply.

SELECTION GUIDE, LISTED BY PERFORMANCE:

$r_{DS(on)}$	
(Ω)	Device No.
10–15Ω	DG140, 141, 145, 146 DG151, 153, 161, 163 DG180, 183, 186, 189
30Ω	DG129, 133, 139, 144 DG181, 184, 187, 190
50Ω	DG152, 154, 162, 164 DG300, 301, 302, 303 DG304, 305, 306, 307 DG381, 384, 387, 390
100Ω & Up	DGM111, 122 DG170, 172, 173 DG201 DG506, 507, 508, 509 DG501, 503

t_{ON}/t_{OFF}	
(ns)	Device No.
150/130	DG181, 184, 187, 190
200/700	DG173
250/130	DG182, 185, 188, 191
250/150	DG304, 305, 306, 307
300/250	DG300, 301, 302, 303 DG381, 384, 387, 390 DG180, 183, 186, 189
300/400	DG170
300/750	DG172
800/1600	DG126, 129, 133, 134 DG152, 154
800/1600	DG139, 142, 143, 144 DG162, 164
1000/2500	DG140, 141, 145, 146 DG151, 153, 161, 163
1000/500	DG200, 201
1000/1500	DG506, 508, 509

Analog Signal Range (with ±15 V supply)	
(Volts)	Device No.
+15 to –15V	DG200, 201 DG300 through 390 DG506 through 509
+15 to –10V	DG182, 185, 188, 191
+15 to –7.5V	DG180, 181, 183, 184 DG186, 187, 189, 190
+15 to –5V	DGM111, 122 DG170, 172, 173

***Multiplexers**

Better performance than shown can be obtained from Siliconix analog switches by special sorting at customer request, or by using discrete FET devices chosen for optimal switching characteristics.

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ANALOG SWITCHES

Basic Part No.	Switch Type	$r_{DS(on)}$ Max (Ω) (Note 4)	Analog Voltage Range (V) (Note 4)	Switching Time (μsec) t_{ON}	Switching Time (μsec) t_{OFF}	Logic Levels (V) V_{INL}	Logic Levels (V) V_{INH}	Opt. Supply Voltage (V) (+) Sup. V_1	Opt. Supply Voltage (V) (−) Sup. V_2	Opt. Supply Voltage (V) Logic Sup. V_L	Opt. Supply Voltage (V) Ref. Sup. V_R	Comments
TWO CHANNEL SPST (See Analog Switch Configuration)												
DGM111	PMOS	75-200	+10 to −10	0.3	1.0	0.5	4.6	10	−20	5		
DG180	N-JFET	10	+10 to −12.5	0.3	0.25	0.8	2.0	10	−20	5	0	Break-Before-Make
		10	+15 to − 7.5	0.3	0.25	0.8	2.0	15	−15	5	0	15 V Supplies
DG181	N-JFET	30	+10 to −12.5	0.15	0.13	0.8	2.0	10	−20	5	0	Break-Before-Make
		30	+15 to − 7.5	0.15	0.13	0.8	2.0	15	−15	5	0	15 V Supplies
DG182	N-JFET	75	+10 to −15	0.25	0.13	0.8	2.0	10	−20	5	0	Break-Before-Make
		75	+15 to −10	0.25	0.13	0.8	2.0	15	−15	5	0	15 V Supplies
DG200	CMOS	70	+15 to −15	1.0	0.5	0.8	2.4	15	−15		(Note 3)	
DG300	CMOS	50	+15 to −15	0.3	0.25	0.8	4.0	15	−15	–	–	Low Power, TTL In
DG304	CMOS	50	+15 to −15	0.25	0.15	3.5	11.0	15	−15	–		Low Power, CMOS In
DG381	CMOS	50	+15 to −15	0.3	0.25	0.8	4.0	15	−15	–	–	Low Power, DG181 Pin Out
FOUR CHANNEL SPST (See Analog Switch Configuration)												
DG172	PMOS	150-450	+10 to −10	0.3	0.75	0.8	2.0	10	−20	5	0	
DG201	CMOS	175	+15 to −15	1.0	0.5	0.8	2.4	15	−15	–	(Note 3)	
ONE CHANNEL SPDT (See Analog Switch Configuration)												
DG186	N-JFET	10	+10 to −12.5	0.3	0.25	0.8	2.0	10	−20	5	0	Break-Before-Make
	N-JFET	10	+15 to − 7.5	0.3	0.25	0.8	2.0	15	−15	5	0	15 V Supplies
DG187	N-JFET	30	+10 to −12.5	0.15	0.13	0.8	2.0	10	−20	5	0	Break-Before-Make
	N-JFET	30	+15 to − 7.5	0.15	0.13	0.8	2.0	15	−15	5	0	15 V Supplies
DG188	N-JFET	75	+10 to −15	0.25	0.13	0.8	2.0	10	−20	5	0	Break-Before-Make
	N-JFET	75	+15 to −10	0.25	0.13	0.8	2.0	15	−15	5	0	15 V Supplies
DG301	CMOS	50	+15 to −15	0.3	0.25	0.8	4.0	15	−15			Low Power, TTL In
DG305	CMOS	50	+15 to −15	0.25	0.15	3.5	11.0	15	−15		–	Low Power, CMOS In
DG387	CMOS	50	+15 to −15	0.3	0.25	0.8	4.0	15	−15	–	–	Low Power, DG187 Pin Out
TWO CHANNEL SPDT (See Analog Switch Configuration)												
DG189	N-JFET	10	+10 to −12.5	0.3	0.25	0.8	2.0	10	−20	5	0	Break-Before-Make
	N-JFET	10	+15 to − 7.5	0.3	0.25	0.8	2.0	15	−15	5	0	15 V Supplies
DG190	N-JFET	30	+10 to −12.5	0.15	0.13	0.8	2.0	10	−20	5	0	Break-Before-Make
	N-JFET	30	+15 to − 7.5	0.15	0.13	0.8	2.0	15	−15	5	0	15 V Supplies
DG191	N-JFET	75	+10 to −15	0.25	0.13	0.8	2.0	10	−20	5	0	Break-Before-Make
	N-JFET	75	+15 to −10	0.25	0.13	0.8	2.0	15	−15	5	0	15 V Supplies
DG303	CMOS	50	+15 to −15	0.3	0.25	0.8	4.0	15	−15			Low Power TTL In
DG307	CMOS	50	+15 to −15	0.25	0.15	3.5	11.0	15	−15	–	–	Low Power, CMOS In
DG390	CMOS	50	+15 to −15	0.3	0.25	0.8	4.0	15	−15	–	–	Low Power, DG190 Pin Out
THREE CHANNEL SPDT (See Analog Switch Configuration)												
DG170	PMOS	200-800	+10 to −10	0.3	0.4	0.8	2.0	10	−20	5	0	
TWO CHANNEL DPST (See Analog Switch Configuration)												
DGM122	PMOS	100-450	+10 to −10	0.3	2.0	0.4	1 mA (1)	10	−20	5	0	
DG183	N-JFET	10	+10 to −12.5	0.3	0.25	0.8	2.0	10	−20	5	0	Break-Before-Make
	N-JFET	10	+15 to − 7.5	0.3	0.25	0.8	2.0	15	−15	5	0	15 V Supplies
DG184	N-JFET	30	+10 to −12.5	0.15	0.13	0.8	2.0	10	−20	5	0	Break-Before-Make
	N-JFET	30	+15 to − 7.5	0.15	0.13	0.8	2.0	15	−15	5	0	15 V Supplies
DG185	N-JFET	75	+10 to −15	0.25	0.13	0.8	2.0	10	−20	5	0	Break-Before-Make
	N-JFET	75	+15 to −10	0.25	0.13	0.8	2.0	15	−15	5	0	15 V Supplies
DG302	CMOS	50	+15 to −15	0.3	0.25	0.8	4.0	15	−15	–		Low Power, TTL In
DG306	CMOS	50	+15 to −15	0.25	0.15	3.5	11.0	15	−15			Low Power, CMOS In
DG384	CMOS	50	+15 to −15	0.3	0.25	0.8	4.0	15	−15	–	–	Low Power, DG184 Pin Out
ONE CHANNEL DPDT (See Analog Switch Configuration)												
DG173	PMOS	150-450	+10 to −10	0.2	0.7	0.8	2.0	10	−20	5	0	2 Input "OR" Control
FOUR CHANNEL SPDT D/A CONVERTER SUMMING NODE SWITCHES (See Analog Switch Configuration)												
DG515	NMOS		(see comments)	0.12	0.17	0.5	7.5	8.0	0			R_1 6.25 Ω, R_2 12.5 Ω, R_3 25 Ω, R_4 50 Ω
TEN CHANNEL SPDT D/A CONVERTER SUMMING NODE SWITCHES (See Analog Switch Configuration)												
DG516	NMOS		(see comments)	0.12	0.17	0.5	7.5	8.0	0			R_1 100 Ω, R_2 200 Ω, R_3 400 Ω, R_4 800 Ω, R_5 1600 Ω, R_6 −10 3200 Ω

ABBREVIATIONS

Prop. – propagation
Chn. – channel
Sw. – switch
Drvr. – driver
Comp. – complementary
Ind. – independent
Com. – common
MUX – multiplexer
NA – not applicable
Trmnls. – terminals
Diffrntl. – differential

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(Continued)

ANALOG MULTIPLEXERS

Basic Part No.	Process Type	$r_{DS(on)}$ Max (Ω) (Note 4)	Analog Voltage Range (V) (Note 4)	Transition Time (μsec) (Note 2)	Logic Levels (V) V_{INL}	Logic Levels (V) V_{INH}	Opt. Supply Voltage (V) (+) Sup. V_1	Opt. Supply Voltage (V) (−) Sup. V_2	Opt. Supply Voltage (V) Ref. Sup. V_R	Comments
EIGHT CHANNEL MUX + ENABLE (See Analog Switch Configuration)										
DG501	PMOS	150-250	+ 5 to − 5	1.5	0.6	3.5	5	−20	0	Logic Pullup Resistors
DG503	PMOS	150-800	+10 to −10	1.5	0.6	8.5	10	−20	0	
DG508	CMOS	400	+15 to −15	1.0	0.8	2.4	15	−15	—	Break-Before-Make
SIXTEEN CHANNEL MUX + ENABLE (See Analog Switch Configuration)										
DG506	CMOS	400	+15 to −15	1.0	0.8	2.4	15	−15	(Note 3)	Break-Before-Make
FOUR CHANNEL DIFFERENTIAL MUX + ENABLE (See Analog Switch Configuration)										
DG509	CMOS	400	+15 to −15	1.0	0.8	2.4	15	−15	—	Break-Before-Make
EIGHT CHANNEL DIFFERENTIAL MUX + ENABLE (See Analog Switch Configuration)										
DG507	CMOS	400	+15 to −15	1.0	0.8	2.4	15	−15	(Note 3)	Break-Before-Make

DRIVERS FOR FET SWITCHES

Basic Part No.	Inputs	Outputs	Function and Uses	ON Level $V_{(out)}$ ON − V_2 At Rated Current(s)	OFF Level $V_{(out)}$ OFF At Rated Current Or $I_{(out)}$ OFF At Rated Voltage	Input Logic for V_{OUT} (low)	Input Limits V_{INL} (V)	Input Limits V_{INH} (V) (I_{INH}) (mA)	Optimum Supply Voltages (V) V_1	V_2	V_L	V_R	Switching Time (μs) t_{ON}	t_{OFF}
D125	6	6	Six Separate MOSFET-Drivers	0.4 V @ 5 mA	0.1 μA @ 10 V	0	0.5	4.6	(Note 5)	−20	5	—	0.6	1.2
D129	7	4	Four Channel (BV=50) MOSFET-Driver with Decode	0.7 V @ 10 mA	0.1 μA @ 10 V	1	0.7	2.2	(Note 5)	−20	—	—	0.25	0.8
D139	2	4	Dual High-Speed Drivers/with Compli-mentary Outputs	1.1 V @ 10 μA 1.5 V @ 2 mA	V_1 − 2 V @ 2 mA	Output and Compliment Available	0.8 0.8	2.0 2.0	10 10	−20 −20	5 5	0 0	0.17 0.17	0.2 0.2

MULTIPLE FET SWITCHES

Basic Part No.	Sources	Drains	Gates	Switch Function	Switch Type	r_{DS} MAX (Ω) @ V_S = +10 V	r_{DS} MAX (Ω) @ V_S = −10 V	BV_{DSS}	$I_{S(off)}$ (nA)	$V_{GS(th)}$ Min	$V_{GS(th)}$ Max	
G115	6	1	6	SP6T	PMOS	100	450	−30	0.5	−1.5	−4.0	6 Switches, Common Out
G123	4	2	4	2XSPDT	PMOS	100	450	−30	0.5	−1.5	−4.0	4 Switches

NOTES:

1. Current Driven Device – I_{INH} = 1 mA
2. The appropriate switching characteristic for multiplexers is $t_{TRANSITION}$, not t_{ON}, t_{OFF}.
3. V_{REF} = 1.5 V is used when supply voltages < ±15 V are used. Not needed when supply voltages of ±15 V are used.
4. Analog voltage range is a function of supply voltages. Where a FET switch is PMOS or CMOS, r_{DS} is also a function of Supply Voltage and Analog Voltage. See individual data sheets for more detail. Values shown are for temperature suffix A.
5. Device normally operates with resistor to +10 V.

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Monolithic CMOS Analog Switches

designed for . . .

- **Portable, Battery Operated Circuits**
- **Low Leakage Switching i.e. Sample and Hold Circuits**
- **Communication Systems**
- **Low Level Switching Circuits**
- **Fast Switching Circuits such as Multiplexers**
- **Standard Linear Dual Supply Voltages or Single Supply Systems**

BENEFITS

- **Low Standby Power**
  - 0.06 μW Typical
- **Minimizes Signal Error**
  - 0.1 nA Typical Leakage
- **Low Operating Power**
  - 0.06 μW Typical for DG304-407
- **Reduced Voltage Drop Across Switch in ON Condition**
  - $r_{ds(on)} < 50\ \Omega$
- **Minimizes Switching Time**
  - Typ t_{on} & $t_{off} < 200$ ns
- **Minimizes System Power Requirements**
  - Single Supply Operation Capabilities
- **Easily Interfaced**
  - TTL, DTL and CMOS Input Compatible
- **Reduces External Component Requirements**
  - Logic Input Overvoltage Protection

DESCRIPTION

The DG300 through DG307 switch family features four switching functions using CMOS technology for low and nearly constant ON resistance (less than 50 Ω) over the full analog signal range. In the ON condition the switches will conduct current in either direction with no offset voltage. With low power dissipation, (a few milliwatts for the DG300-303, a few hundred microwatts for the DG304-307), this series of switches becomes an ideal candidate for battery-powered or remote switching applications. The switching speed is among the fastest available with the low quiescent power dissipation. In the OFF condition, the switches will block voltages up to 30 V peak-to-peak. A logic input driver controls the ON/OFF state of the switches. (See the "Pin Configuration" for switch status with a logic "1" input.) The DG300-303 switches are TTL and CMOS input compatible and have a logic "0" state with an input less than 0.8 V and a logic "1" state with an input greater than 4.0 V. A pull-up resistor should be added for totem pole TTL outputs. The DG304-307 switches are CMOS input compatible and have a logic "0" state with an input less than 3.5 V and a logic "1" state with an input greater than 11 V (for 15 V positive supply). The logic inputs are protected against overvoltage up to 18 V above and 36 V below the positive supply. The combination of low cost, low power, low resistance and fast speed optimizes system design.

PIN CONFIGURATIONS

DUAL SPST DG300 or DG304

Metal Can Package: V+ (SUBSTRATE AND CASE); D_1, D_2, S_1, S_2, IN_1, IN_2, NC, V−, GND — TOP VIEW

Dual-In-Line and Flat Package: NC, D_1, NC, S_1, NC, IN_1, GND, V+, D_2, NC, S_2, NC, IN_2, V− — TOP VIEW

ORDER NUMBERS:
DG300AA OR DG300BA
DG304AA OR DG304BA

ORDER NUMBERS:
DG300AP OR DG300BP
DG304AP OR DG304BP
DG300CJ
DG304CJ
DG300AL OR DG304AL

LOGIC	SWITCH
0	OFF
1	ON

SPDT DG301 or DG305

Dual-In-Line and Flat Package: NC, D_1, NC, S_1, NC, IN, GND, V+, D_2, NC, S_2, NC, NC, V− — TOP VIEW

Metal Can Package: V+ (SUBSTRATE AND CASE); D_1, D_2, S_1, S_2, IN, NC, NC, V−, GND — TOP VIEW

ORDER NUMBERS:
DG301AP OR DG301BP
DG305AP OR DG305BP
DG301CJ
DG305CJ
DG301AL OR DG305AL

ORDER NUMBERS:
DG301AA OR DG301BA
DG305AA OR DG305BA

LOGIC	SW 1	SW 2
0	OFF	ON
1	ON	OFF

DUAL DPST DG302 or DG306

Dual-In-Line and Flat Package: NC, S_3, D_3, D_1, S_1, IN_1, GND, V+, S_4, D_4, D_2, S_2, IN_2, V− — TOP VIEW

ORDER NUMBERS:
DG302AP OR DG302BP
DG306AP OR DG306BP
DG302CJ
DG306CJ
DG302AL OR DG306AL

LOGIC	SWITCH
0	OFF
1	ON

DUAL SPDT DG303 or DG307

LOGIC	SW 1 SW 2	SW 3 SW 4
0	OFF	ON
1	ON	OFF

ORDER NUMBERS:
DG303AP OR DG303BP
DG307AP OR DG307BP
DG303CJ
DG307CJ
DG303AL OR DG307AL

Dual-In-Line and Flat Package: NC, S_3, D_3, D_1, S_1, IN_1, GND, V+, S_4, D_4, D_2, S_2, IN_2, V− — TOP VIEW

SWITCH STATES ARE FOR LOGIC "1" INPUTS (POSITIVE LOGIC)

"SEE PRODUCT APPLICATION GUIDE ON PAGE 812"

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ABSOLUTE MAXIMUM RATINGS

V_{IN} to Ground . . . . . V^+ +18 V, V^+ −36 V
V_S or V_D . . . . . V^+ to V^-
V^+ to Ground . . . . . +36 V
V^+ to V^- . . . . . +36 V
Current, Any Terminal (Except S or D) . . . . 30 mA
Current, S or D, Continuous . . . . . 30 mA
Pulsed 1 ms 10% Duty Cycle . . . . . 100 mA
Operating Temperature (A Suffix) . . . −55 to +125°C
(B Suffix) . . . −20 to +85°C
(C Suffix) . . . . 0 to +70°C
Storage Temperature (A & B Suffix) . . −65 to +150°C
(C Suffix) . . . . −65 to +125°C

Power Dissipation*
14 Pin Sidebraze DIP (P)** . . . . . 825 mW
14 Pin Plastic DIP (J)*** . . . . . 470 mW
Metal Can (A)**** . . . . . 450 mW
Flat Package (L)***** . . . . . 750 mW

*Device mounted with all leads welded or soldered to PC board.
**Derate 11 mW/°C above 75°C
***Derate 6.5 mW/°C above 25°C
****Derate 6 mW/°C above 75°C
*****Derate 10 mW/°C above 75°C

ELECTRICAL CHARACTERISTICS

All DC parameters are 100% tested at 25°C. Lots are sample tested for AC parameters and high and low temperature limits to assure conformance with specifications.

		Characteristics			Typ[1] 25°C	Max Limits A/B Suffix −55°C/−20°C	A/B Suffix 25°C	A/B Suffix 125°C/85°C	C Suffix 0°C	C Suffix 25°C	C Suffix 70°C	Unit	Test Conditions V+ = +15 V, V− = −15 V, Gnd = 0 V	
1	SWITCH	$r_{DS(on)}$	Drain Source ON Resistance		30	50	50	75	50	50	75	Ω	V_D = +10 V, I_S = −10 mA	Note 2
2					30	50	50	75	50	50	75		V_D = −10 V, I_S = +10 mA	
3		$I_{S(off)}$	Source OFF Leakage Current		0.1		1	100		5	100	nA	V_S = +15 V, V_D = −15 V	Note 2
4					−0.1		−1	−100		−5	−100		V_S = −15 V, V_D = +15 V	
5		$I_{D(off)}$	Drain OFF Leakage Current		0.1		1	100		5	100		V_D = +15 V, V_S = −15 V	
6					−0.1		−1	−100		−5	−100		V_D = −15 V, V_S = +15 V	
7		$I_{D(on)}$	Channel ON Leakage Current		0.1		1	100		5	100		V_D = V_S = +15 V	Note 2
8					−0.1		−2	−200		−5	−200		V_D = V_S = −15 V	
9	INPUTS	I_{INH}	Input Current Input Voltage High	DG300-303 Only	−0.001	−1	−1	−1		−1		μA	V_{IN} = +5 V	
10				DG300-307	0.001	1	1	1		1			V_{IN} = +15 V	
11		I_{INL}	Input Current Input Voltage Low		−0.001	−1	−1	−1		−1			V_{IN} = 0	
12	DYNAMIC	t_{on}	Turn ON Time	DG300-303 Only	150		300					nS	See Switching Time Test Circuit	
13		t_{off}	Turn OFF Time		130		250							
14		t_{on}	Turn ON Time	DG304-307 Only	110		250							
15		t_{off}	Turn OFF Time		70		150							
16		$t_{on} - t_{off}$	Break-Before-Make Interval	DG301/303 DG305/307 Only	50								See Break-Before-Make Time Test Circuit	
17		$C_{S(off)}$	Source OFF Capacitance		14							pF	V_S = 0, Note 2	f = 1 MHz
18		$C_{D(off)}$	Drain OFF Capacitance		14								V_D = 0, Note 2	
19		$C_{D(on)} + C_{S(on)}$	Channel ON Capacitance		40								V_D = V_S = 0, Note 2	
20		C_{IN}	Input Capacitance		6								V_{IN} = 0	
21					3.5								V_{IN} = +15 V	
22			OFF Isolation[3]		62							dB	V_{IN} = 0, R_L = 1K Ω, C_L = +15 pF V_S = 1 V_{RMS}, f = 500 kHz	
23	SUPPLY	I+	Positive Supply Current	DG300-303 Only	0.23	1	0.5	0.5		1		mA	V_{IN} = 4 V (One Input) (All Other Inputs = 0)	
24		I−	Negative Supply Current		−0.001	−10	−10	−100		−100		μA		
25		I+	Positive Supply Current		0.001	10	10	100		100			V_{IN} = 0.8 V (All Inputs)	
26		I−	Negative Supply Current		−0.001	−10	−10	−100		−100				
27		I+	Positive Supply Current	DG304-307 Only	0.001	10	10	100		100			V_{IN} = +15 V (All Inputs)	
28		I−	Negative Supply Current		−0.001	−10	−10	−100		−100				
29		I+	Positive Supply Current		0.001	10	10	100		100			V_{IN} = 0 (All Inputs)	
30		I−	Negative Supply Current		−0.001	−10	−10	−100		−100				

NOTES:
1. Typical values are for DESIGN AID ONLY, not guaranteed and not subject to production testing.
2. V_{IN} = Input voltage to perform proper function, DG300-303: V_{IN} – For logic "1" = 4 V, for logic "0" = 0.8 V
DG304-307: V_{IN} – For logic "1" = 11 V, for logic "0" = 3.5 V
3. "OFF" Isolation $\triangleq$ 20 log V_S/V_D, V_S = Input to OFF switch, V_D = Output

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Monolithic CMOS Analog Switches

designed for . . .

- **Portable, Battery Operated Circuits**
- **Low Leakage Switching i.e. Sample and Hold Circuits**
- **Communication Systems**
- **Low Level Switching Circuits**
- **Fast Switching Circuits such as Multiplexers**
- **Standard Linear Dual Supply Voltages or Single Supply Systems**

BENEFITS

- **Low Standby Power**
  - 0.06 μW Typical
- **Minimizes Signal Error**
  - 0.1 nA Typical Leakage
- **Low Operating Power**
  - 7.5 mW Typical
- **Reduced Voltage Drop Across Switch in ON Condition**
  - $r_{ds(on)} < 50\ \Omega$
- **Minimizes Switching Time**
  - Typ t_{on} & $t_{off} < 200$ ns
- **Minimizes System Power Requirements**
  - Single Supply Operation Capabilities
- **Easily Interfaced**
  - TTL, DTL / CMOS Input Compatible
  - Pin to Pin Replacement for DG180 Series Switches
- **Reduces External Component Requirements**
  - Logic Input Overvoltage Protection

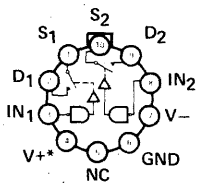
DESCRIPTION

The DG381 through DG390 switch family features four switching functions using CMOS technology for low and nearly constant ON resistance (less than 50 Ω) over the full analog signal range. In the ON condition the switches will conduct current in either direction with no offset voltage. With low power dissipation, a few milliwatts, this series of switches becomes an ideal candidate for battery-powered or remote switching applications. The switching speed is among the fastest available with the low quiescent power dissipation. In the OFF condition, the switches will block voltages up to 30 V peak-to-peak. A logic input driver controls the ON/OFF state of the switches. (See the "Pin Configuration" for switch status with a logic "1" input.) The switches are TTL and CMOS input compatible and have a logic "0" state with an input less than 0.8 V and a logic "1" state with an input greater than 4.0 V. A pull-up resistor should be added for totem pole TTL outputs. The logic inputs are protected against overvoltage up to 18 V above and 36 V below the positive supply. The combination of low cost, low power, low resistance and fast speed optimizes system design.

PIN CONFIGURATIONS

DUAL SPST DG381

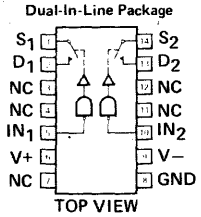
Metal Can Package



TOP VIEW

ORDER NUMBERS:
DG381AA OR DG381BA

Dual-In-Line Package



TOP VIEW

ORDER NUMBERS:
DG381AP OR DG381BP

DG381CJ

LOGIC	SW 1 SW 2
0	ON
1	OFF

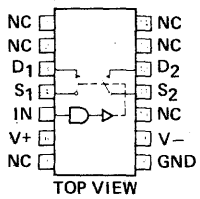
*(SUBSTRATE AND CASE)

SPDT DG387

LOGIC	SW 1	SW 2
0	OFF	ON
1	ON	OFF

*(SUBSTRATE AND CASE)

Dual-In-Line Package

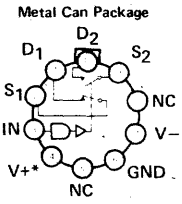


TOP VIEW

ORDER NUMBERS:
DG387AP OR DG387BP

DG387CJ

Metal Can Package



TOP VIEW

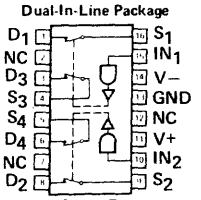
ORDER NUMBERS:
DG387AA OR DG387BA

DUAL DPST DG384

ORDER NUMBERS:
DG384AP OR DG384BP

DG384CJ

Dual-In-Line Package



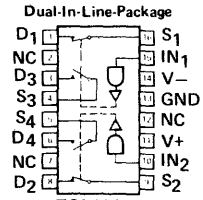
TOP VIEW

LOGIC	SW 1–4
0	OFF
1	ON

DUAL SPDT DG390

LOGIC	SW 1 SW 2	SW 3 SW 4
0	OFF	ON
1	ON	OFF

Dual-In-Line-Package



TOP VIEW

ORDER NUMBERS:
DG390AP OR DG390BP

DG390CJ

SWITCH STATES ARE FOR LOGIC "1" INPUTS (POSITIVE LOGIC)

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ABSOLUTE MAXIMUM RATINGS

V_{IN} to Ground . . . . . V+ +18 V, V+ −36 V
V_S to V_D . . . . . V+, V−
V+ to Ground . . . . . +36 V
V+ to V− . . . . . +36 V
Current, Any Terminal (Except S or D) . . . . 30 mA
Current, S or D, Continuous . . . . . 30 mA
Pulsed 1 ms 10% Duty Cycle . . . . . 100 mA
Operating Temperature (A Suffix) . . −55 to +125°C
(B Suffix) . . −20 to +85°C
(C Suffix) . . . 0 to +70°C
Storage Temperature (A & B Suffix) . . −65 to +150°C
(C Suffix) . . . . −65 to +125°C

Power Dissipation*
14 Pin Sidebraze DIP (P)** . . . . . 825 mW
14 Pin Plastic DIP (J)*** . . . . . 470 mW
Metal Can (A)**** . . . . . 450 mW

*Device mounted with all leads welded or soldered to PC board.
**Derate 11 mW/°C above 75°C
***Derate 6.5 mW/°C above 25°C
****Derate 6 mW/°C above 75°C

ELECTRICAL CHARACTERISTICS

All DC parameters are 100% tested at 25°C. Lots are sample tested for AC parameters and high and low temperature limits to assure conformance with specifications.

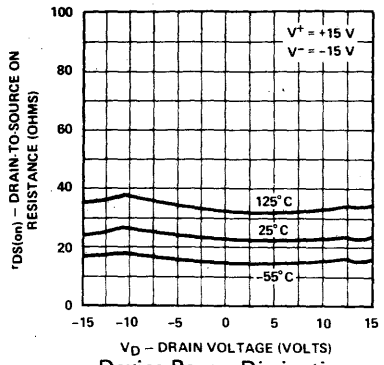
		Characteristics		Typ[1] 25°C	Max Limits A/B Suffix −55°C/ −20°C	A/B Suffix 25°C	A/B Suffix 125°C/ 85°C	C Suffix 0°C	C Suffix 25°C	C Suffix 70°C	Unit	Test Conditions V+ = +15 V, V− = −15 V, Gnd = 0 V	
1	SWITCH	$r_{DS(on)}$	Drain Source ON Resistance	30	50	50	75	50	50	75	Ω	V_D = +10 V, I_S = −10 mA	Note 2
2				30	50	50	75	50	50	75		V_D = −10 V, I_S = +10 mA	
3		$I_{S(off)}$	Source OFF Leakage Current	0.1		1	100		5	100	nA	V_S = +15 V, V_D = −15 V	Note 2
4				−0.1		−1	−100		−5	−100		V_S = −15 V, V_D = +15 V	
5		$I_{D(off)}$	Drain OFF Leakage Current	0.1		1	100		5	100		V_D = +15 V, V_S = −15 V	
6				−0.1		−1	−100		−5	−100		V_D = −15 V, V_S = +15 V	
7		$I_{D(on)}$	Channel ON Leakage Current	0.1		1	100		5	100		V_D = V_S = +15 V	Note 2
8				−0.1		−2	−200		−5	−200		V_D = V_S = −15 V	
9	IN	I_{INH}	Input Current Input Voltage High	−0.001	−1	−1	−1		−1		μA	V_{IN} = +5 V	
10				0.001	1	1	1		1			V_{IN} = +15 V	
11		I_{INL}	Input Current Input Voltage Low	−0.001	−1	−1	−1		−1			V_{IN} = 0	
12	DYNAMIC	t_{on}	Turn ON Time	150		300					nS	See Switching Time Test Circuit	
13		t_{off}	Turn OFF Time	130		250							
14		$t_{on} - t_{off}$	Break-Before-Make Interval DG387/390 only	50								See Break-Before-Make Time Test Circuit	
15		$C_{S(off)}$	Source OFF Capacitance	14							pF	V_S = 0, Note 2	f = 1 MHz
16		$C_{D(off)}$	Drain OFF Capacitance	14								V_D = 0, Note 2	
17		$C_{D(on)} + C_{S(on)}$	Channel ON Capacitance	40								V_D = V_S = 0, Note 2	
18		C_{IN}	Input Capacitance	6								V_{IN} = 0	
19				3.5								V_{IN} = +15 V	
20			OFF Isolation[3]	62							dB	V_{IN} = 0, R_L = 1K Ω, C_L = +15 pF V_S = 1 V_{RMS}, f = 500 kHz	
21	SUPPLY	I+	Positive Supply Current	0.23	1	0.5	0.5		1		mA	V_{IN} = 4 V (One Input) (All Other Inputs = 0)	
22		I−	Negative Supply Current	−0.001	−10	−10	−100		−100		μA		
23		I+	Positive Supply Current	0.001	10	10	100		100			V_{IN} = 0.8 V (All Inputs)	
24		I−	Negative Supply Current	−0.001	−10	−10	−100		−100				

NOTES:
1. Typical values are for DESIGN AID ONLY, not guaranteed and not subject to production testing
2. V_{IN} = Input voltage to perform proper function, V_{IN} for logic "1" = 4 V, for logic "0" 0.8 V
3. "OFF" Isolation $\triangleq$ 20 log V_S/V_D = Input to OFF switch, V_D = Output

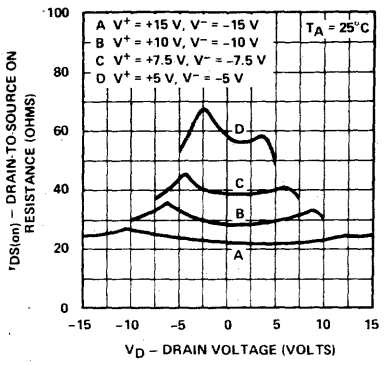
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TYPICAL CHARACTERISTICS

$r_{DS(on)}$ vs V_D and Temperature

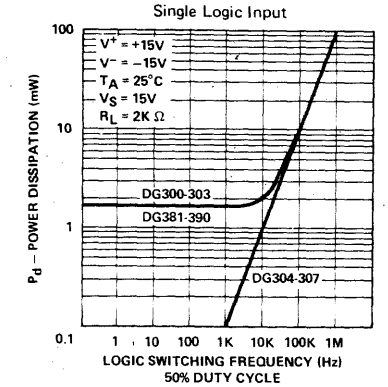


$r_{DS(on)}$ vs V_D and Power Supply Voltage

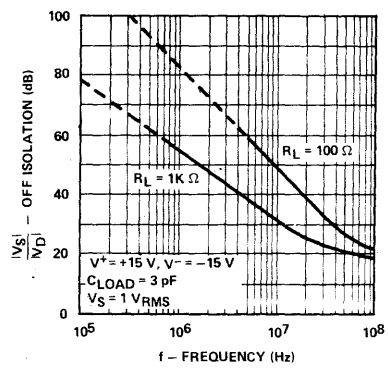


Device Power Dissipation vs Switching Frequency

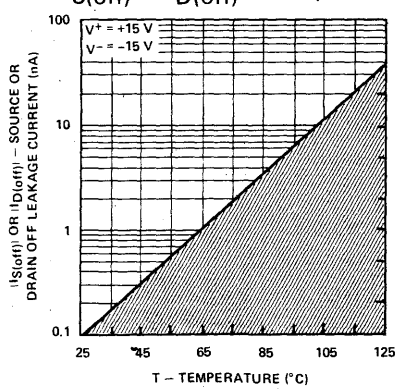
Single Logic Input



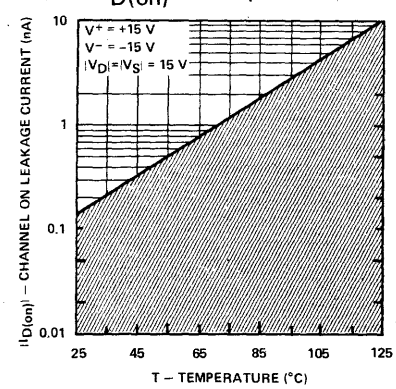
OFF Isolation vs Frequency



$I_{S(off)}$ or $I_{D(off)}$ vs Temperature*

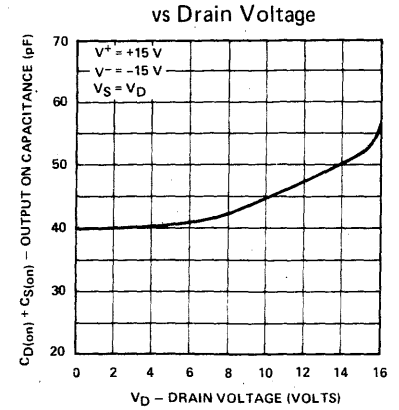


$I_{D(on)}$ vs Temperature*

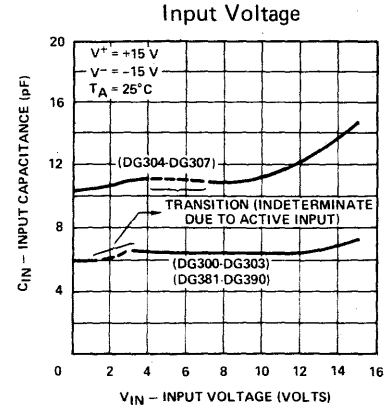


*The net leakage into the source or drain is the n-channel leakage minus the p-channel leakage. This difference can be positive, negative, or zero depending on the analog voltage and temperature, and will vary greatly from unit to unit.

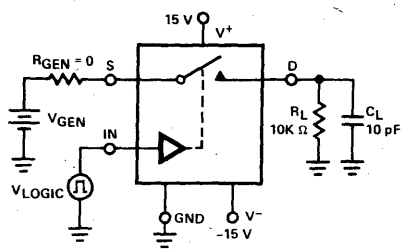
Output ON Capacitance vs Drain Voltage



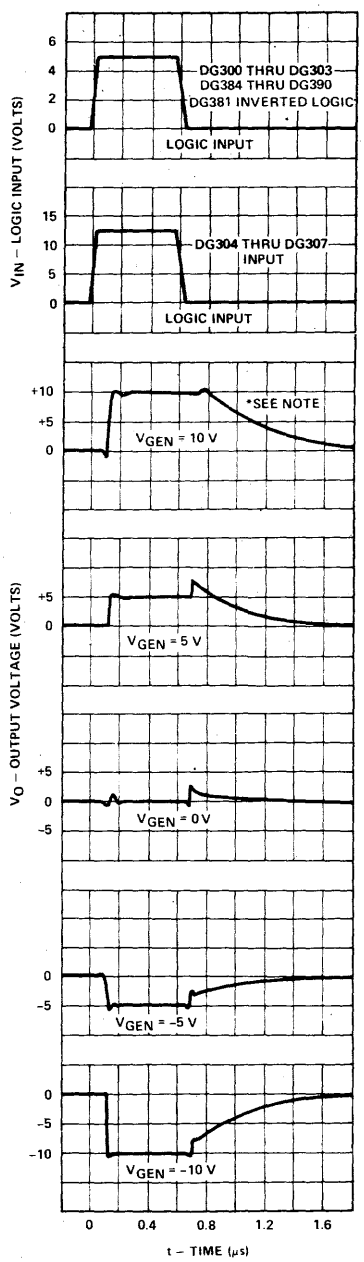
Input Capacitance vs Input Voltage



Typical delay, rise, fall, settling times, and switching transients in this circuit.



If R_{GEN}, R_L or C_L is increased, there will be proportional increases in rise and/or fall RC times. Applying V_{GEN} to D rather than S results in much greater spikes.

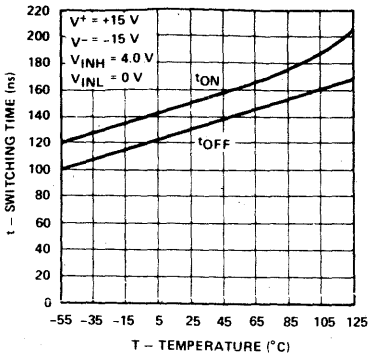


*Note: The turn-off time is primarily limited here by the RC time constant (100 ns) of the load.

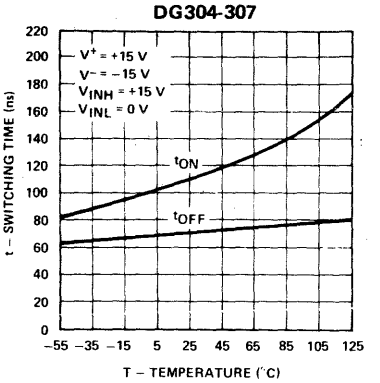
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TYPICAL CHARACTERISTICS (Cont'd)

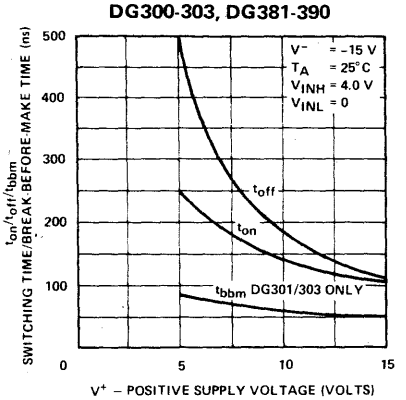
Switching Time vs Temperature
DG300-303, DG381-390



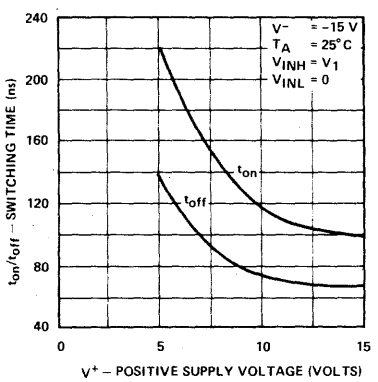
Switching Time vs Temperature
DG304-307



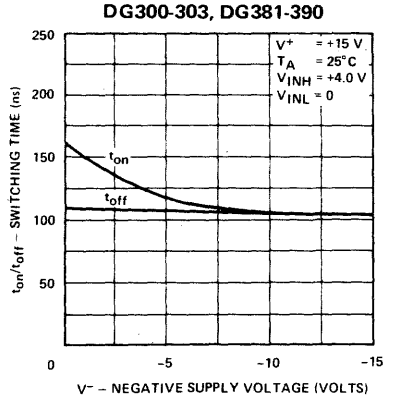
Switching Time and Break-Before-Make Time vs Positive Supply Voltage
DG300-303, DG381-390



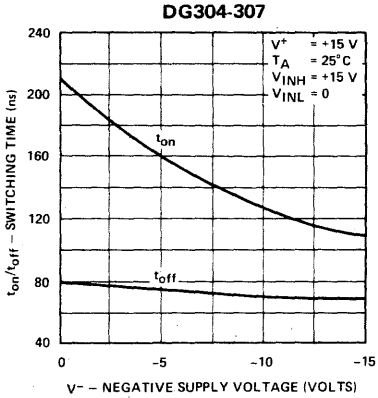
Switching Time vs Positive Supply Voltage
DG304-307



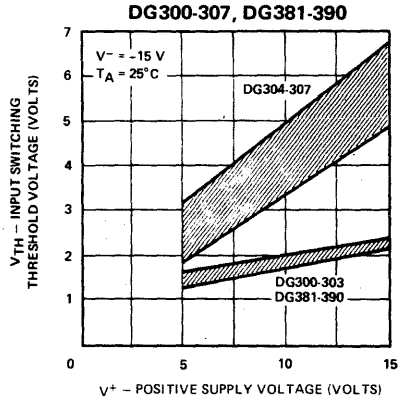
Switching Time vs Negative Supply Voltage
DG300-303, DG381-390



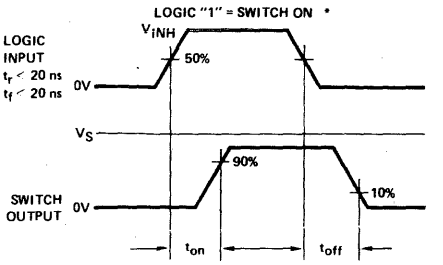
Switching Time vs Negative Supply Voltage
DG304-307



Input Switching Threshold vs Positive Supply Voltage
DG300-307, DG381-390

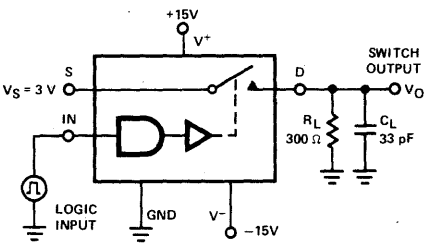


SWITCHING TIME TEST CIRCUIT (DG300-307 DG381-390)

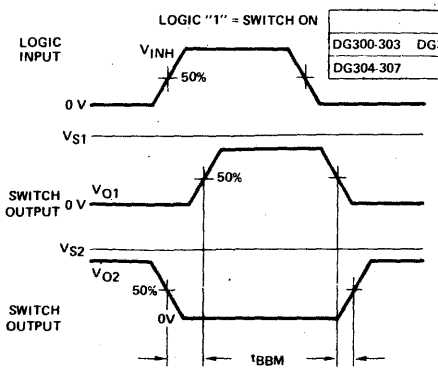


		VINH
DG300-303	DG381-DG390	4 V
DG304-307		15 V

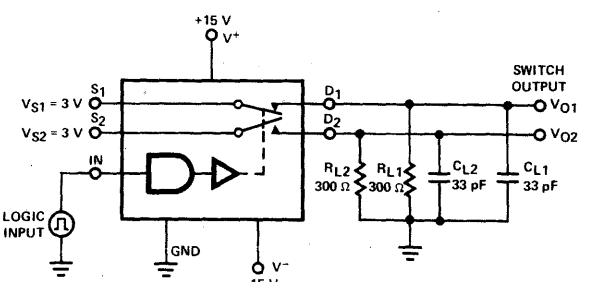
*INVERTED LOGIC FOR DG381



BREAK-BEFORE-MAKE TIME TEST CIRCUIT SPDT (DG301, DG303, DG305, DG307, DG384, DG390)



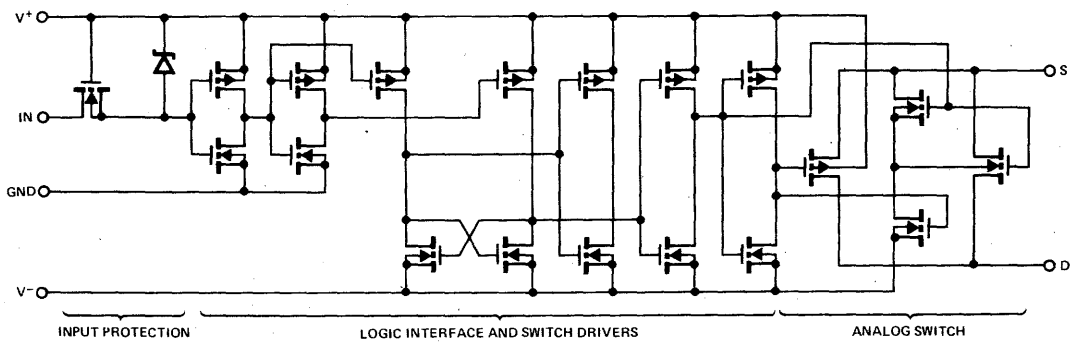
		VINH
DG300-303	DG381-DG390	4 V
DG304-307		15 V



"SEE PRODUCT APPLICATION GUIDE ON PAGE 812"

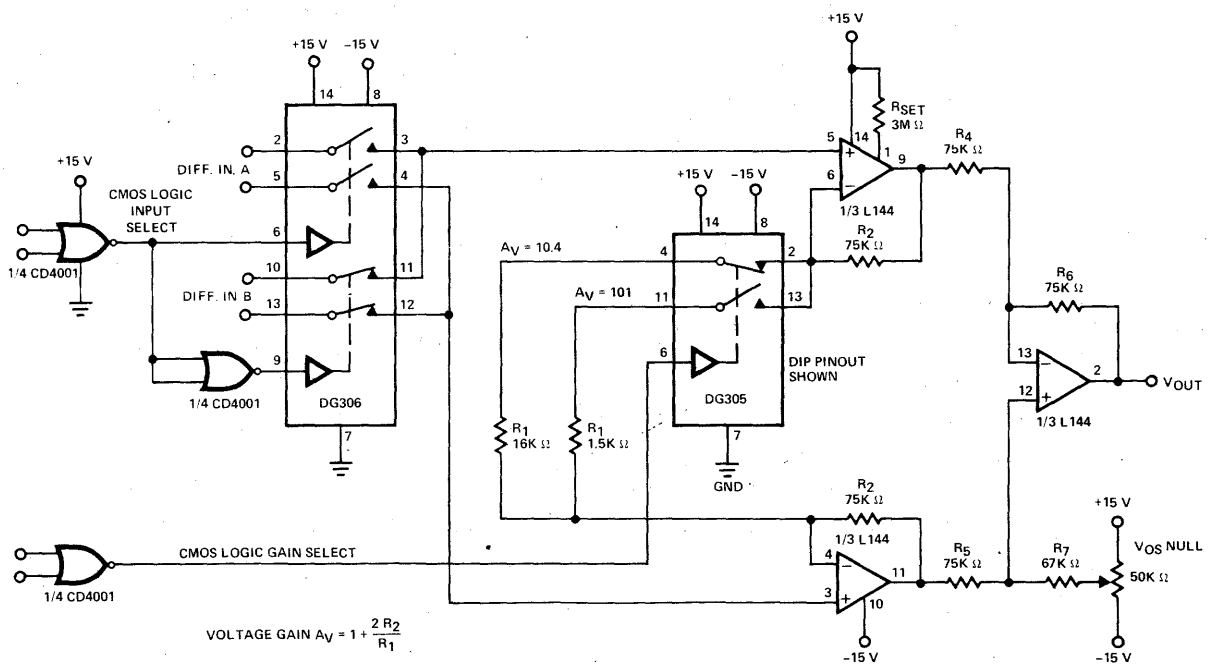
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PARTIAL SCHEMATIC OF TYPICAL SWITCH (DG300-307, DG381-390)

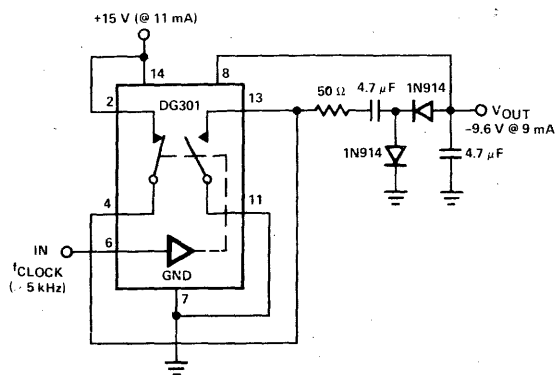


APPLICATIONS

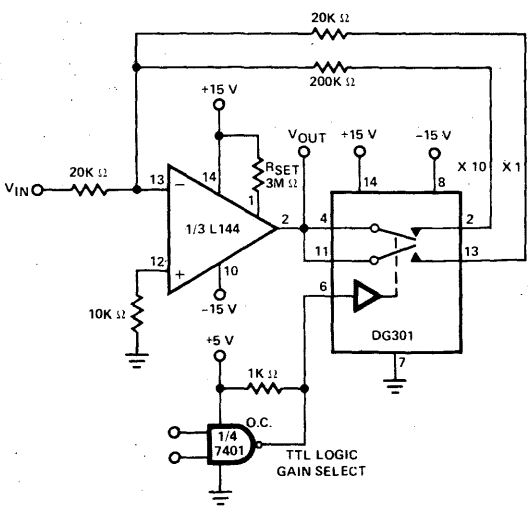
Low Power Instrumentation Amplifier With
Digitally Selectable Inputs and Gain



Negative Voltage Converter For Use In
Single Supply Systems



Low Power Inverting Amplifier With
Digitally Selectable Gain



"SEE PRODUCT APPLICATION GUIDE ON PAGE 812"

©IC MASTER 1979

four digit LCD decoder driver

designed for . . .

■ Driving Liquid Crystal Displays Directly

BENEFITS

- Reduces Complexity of Driving LCD Displays
- Only 1 Package Required to Drive Up to a 4 Digit Display
- Minimal Power Consumption
  - Typically 1.5 mW
- Easily Interfaces with Most Logic Families
- No External Oscillator Required
- No Display Buffering Required
- Easy Multiple Driver Interfacing
- Eliminates DC Biases which Degrade Display Lifetime
- Blank Digital Code on Chip

DESCRIPTION

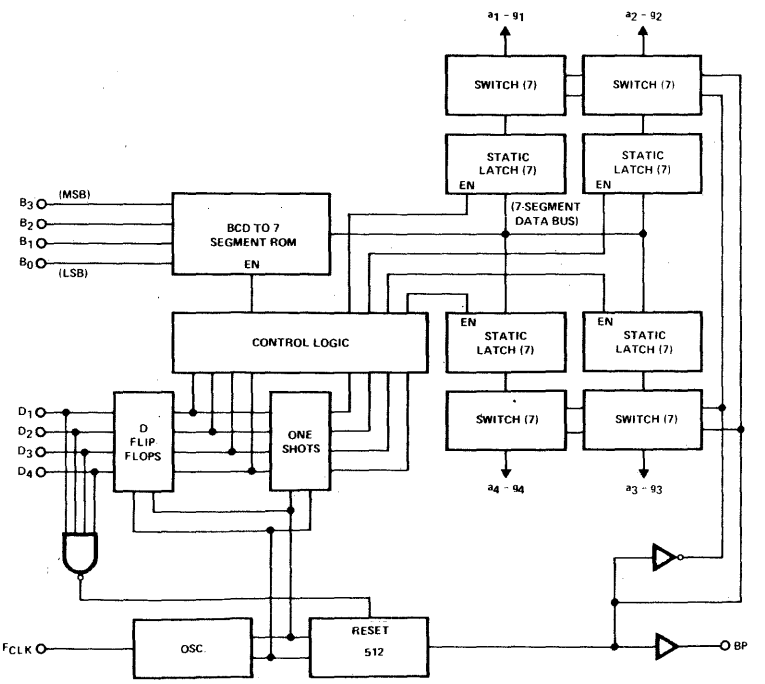
The DF412 Four Digit LCD Decoder Driver is a CMOS Monolithic multiplexed BCD to LCD Decoder Driver. One DF412 contains all of the circuitry needed to decode up to 4 digits of multiplexed BCD information and derive the AC signals needed to drive a 4 digit LCD display.

An on board oscillator, its frequency being controlled by an external capacitor, develops a backplane (BP) signal which is a square wave swinging between ground (V_{SS}) and the positive supply (V_{DD}). Segment drivers supply square waves of the same frequency as the backplane but either in phase for an OFF segment or out of phase for an ON segment. In this manner of LCD digit driving the net DC voltage applied between segment and backplane is zero, a necessary requirement for long display life. Digital input levels are defined as input voltages > 5 V being a logic "1" and input voltages < 0.8 V being a logic "0" with V_{DD} = 6 V.

BCD input data is decoded into 7 segment form using an on board ROM. The 7 segment data is then latched into the appropriate static latches via the digit strobe inputs and control logic.

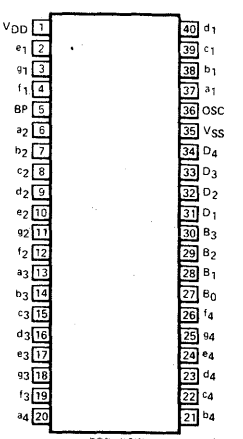
The pinout of the DF412 allows easy PC board interfaces to Dual In-Line LCDs as well as edge connecting types of displays.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION

Dual-In-Line Package



TOP VIEW
V_{DD} COMMON TO SUBSTRATE

ORDER NUMBER DF412CJ

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± 3 digit A/D converter
± 3⅓ digit A/D converter

designed for . . .

- **Digital Voltmeters, Panel Meters**
- **Digital Thermometers**
- **General Instrumentation (Noise, Light, pH, etc.)**
- **Microprocessor Interfaces to Analog Signals**

BENEFITS

- Accuracy of 0.1% ±1 Count For Full Use of 3 Digits
- Low Power Consumption of 25 mW
- Minimum External Parts Count
- Auto-Zero and Auto-Polarity
- Buffered Signal and Reference Inputs ($Z_{IN} > 10^9\ \Omega$)
- Internal Oscillator Uses Only One External Capacitor
- Wide Sampling Range of 1 to 60/Second
- Multiplexed BCD Output For Simple Display and μ-P Interface

DESCRIPTION

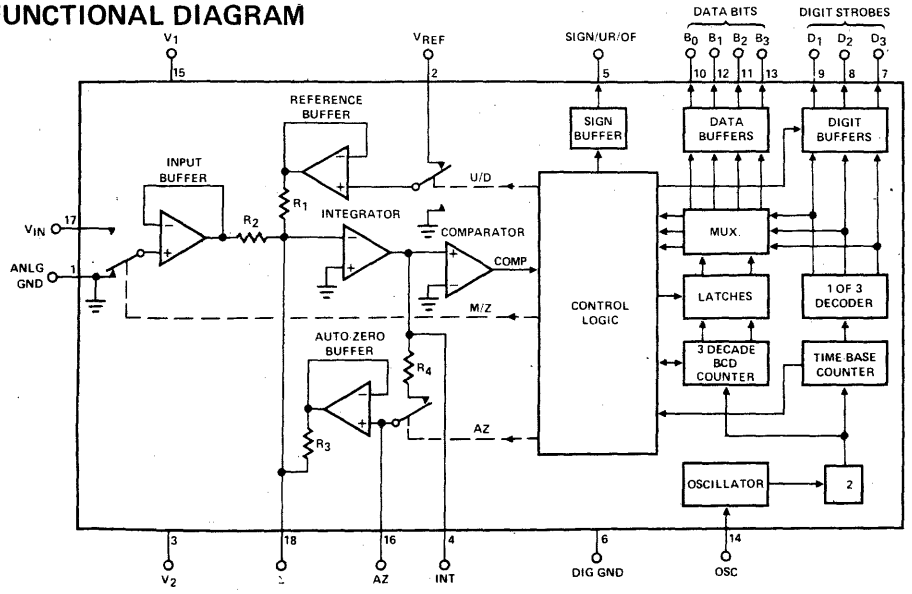
The LD130 combines both the analog and digital subsystems of a 3 digit A/D system in a single monolithic CMOS I.C. The "Quantized Feedback" conversion scheme, introduced by Siliconix, provides the LD130 with an Auto-Zero, Auto-Polarity A/D system requiring only a single reference voltage. External parts are minimized by the on-chip resistors and buffer amplifiers. These high impedance input and reference buffer amplifiers eliminate source loading errors providing the outstanding temperature coefficient and ratio operation inherent in this system. Break-before-make switch action insures that neither the analog input nor the reference voltage will be shorted to ground at any time.

The LD130 3 digit A/D is made functionally complete by the following additions:

1. C_{AZ} (0.10 μF) between AZ and Σ pins
2. C_{INT} (0.033 μF) between INT and Σ pins
3. C_{OSC} (0.001 μF) between OSC and Digital Ground
4. $V_{REF} \cong 2.000$ V
5. ±5 V supplies (@ 3 mA)

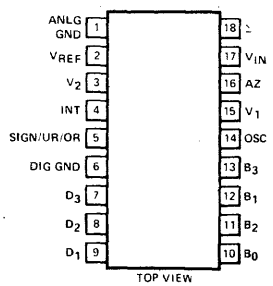
The LD131 is functionally equivalent to the 3 digit LD130 A/D converter with the exception of not having overrange blinking when the count exceeds 999.

FUNCTIONAL DIAGRAM



PIN CONFIGURATION

Dual-In-Line Package



ORDER NUMBER LD130CJ

ORDER NUMBER LD130BP

ORDER NUMBER LD131CJ

"SEE PRODUCT APPLICATION GUIDE ON PAGE 812"

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ABSOLUTE MAXIMUM RATINGS

V_{IN} . . . . . $V_1 + 0.3$ V, $V_2 - 0.3$ V
$V_1 - V_2$ . . . . . 16 V
V_1 . . . . . 8 V
Current at V_{IN} . . . . . 1 mA
Voltage on any pin . . . . . $V_1 + 0.3$ V, $V_2 - 0.3$ V
V_{REF} . . . . . V_1
Operating Temperature (BP) . . . . . −20 to 85°C
Operating Temperature (CJ) . . . . . 0 to 70°C
Storage Temperature (B Suffix) . . . . . −65 to 150°C
Storage Temperature (C Suffix) . . . . . −65 to 125°C
Power Dissipation* (J Package) . . . . . 450 mW
Power Dissipation (P Package). . . . . 1000 mW

*Device mounted with all leads welded or soldered to PC Board, Derate 6.3 mW/°C above 25°C.

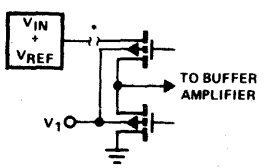
ELECTRICAL CHARACTERISTICS

All DC parameters are 100% tested at 25°C. Lots are sample tested for AC parameters and High Temperature Limits to assure conformance with specifications.

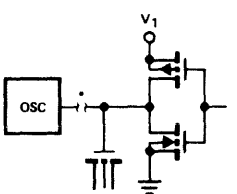
		CHARACTERISTIC		MIN	TYP	MAX	UNIT	TEST CONDITIONS $V_1 = +5$ V, $V_2 = -5$ V, $V_{REF} = 2.000$ V, $T_A = 25°C$, $C_{INT} = 0.033\ \mu F$, $C_{strg} = 0.1\ \mu F$
1	GENERAL		Linearity			0.1	% rdg	
2	GENERAL		Noise		0.3		LSB	Peak-to-Peak noise apparent when going from one steady reading to another.
3	GENERAL		Zero T.C.		10		μV/°C	$0 \leq T_A \leq 70°C$
4	GENERAL		Gain T.C.		15		ppM/°C	$0 \leq T_A \leq 70°C$
5	GENERAL		NMR Normal Mode Rejection	36			dB	$f_{series} = 60$ Hz, $f_{osc} = 24$ kHz
6	INPUT	I_{IN}	V_{IN} Input Bias Current		7		pA	$T_A = 25°C$
7	INPUT	I_{IN}	V_{IN} Input Bias Current		90		pA	$T_A = 70°C$
8	INPUT	I_{IN}	V_{IN} Input Bias Current			1	nA	$T_A = 85°C$, (BP Only)
9	INPUT	I_{REF}	V_{REF} Input Bias Current		7		pA	$T_A = 25°C$
10	INPUT	I_{REF}	V_{REF} Input Bias Current		90		pA	$T_A = 70°C$
11	INPUT	I_{REF}	V_{REF} Input Bias Current			1	nA	$T_A = 85°C$, (BP Only)
12	INPUT	I_{AZ}	AZ Input Bias Current			1	nA	$T_A = 85°C$, (BP Only), $V_{AZ} = -1$ V
13	INPUT	f_{CLK}	Clock Frequency	6*	30	370*	kHz	
14	INPUT	D.C.$_{CLK}$	Clock Duty Cycle	30/70		70/30	%	
15	INPUT	I_{INL}	Clock Input Current Low			1	mA	$V_{INL} = 0.25$ V
16	INPUT	I_{INH}	Clock Input Current High			1	mA	$V_{INH} = 4.75$V
17	OUT	V_{OL}	All Outputs			0.4	V	$I_{OL} = 1.6$ mA Over Operating Temperature Range
18	OUT	V_{OH}	Digit Strobes	2.4			V	$I_{OH} = -400\ \mu A$ Over Operating Temperature Range
19	OUT	V_{OH}	Data Bits, Sign/UR/OR	2.4			V	$I_{OH} = -100\ \mu A$ Over Operating Temperature Range
20	SUPPLY	I_1	Supply Current			6	mA	
21	SUPPLY	I_2	Supply Current			−4	mA	
22	SUPPLY	$PSRR_1$	V_1 Supply Rejection		0.6		mV/V	
23	SUPPLY	$PSRR_2$	V_2 Supply Rejection		1.4		mV/V	

Typical values are for Design Aid Only, not guaranteed and not subject to production testing. *LD131 Specs only

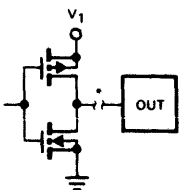
INPUT/OUTPUT SCHEMATICS



V_{IN} or V_{REF} Input



Oscillator Input



Output Buffers (Digits, Bits, SIGN/UR/OR)

*Protection circuitry not shown.

©IC MASTER 1979

3½ digit A/D converter set

designed for . . .

- **High Performance Digital Voltmeters**
- **Digital Panel Meters**
- **Digital Instrumentation Readouts**
- **Microprocessor A/D Interface Subsystem**
- **Auto-Zeroed Microvolt or Strain-Gauge Systems**

BENEFITS

- Three Usable Ranges with a Single Resistor Change. 1.999 V, 199.9 nV, 19.99 mV
- Excellent System Performance From Basic 0.02% ±1 Count Accuracy
- Wide Sampling Rate: 1/3 to 40/Second
- High Gain Stability (5 ppm/°C) with Buffered Reference Input
- Reduced Signal Loading with MOSFET Input ($Z_{IN} > 10^9\ \Omega$)
- Auto-Zero System Minimizes Internal and External Offset and Drift Over Temperature
- Auto-Polarity with a Single Reference
- Easy Interface to Displays with Strobed BCD Output Format
- Overrange and Underrange Signals Available

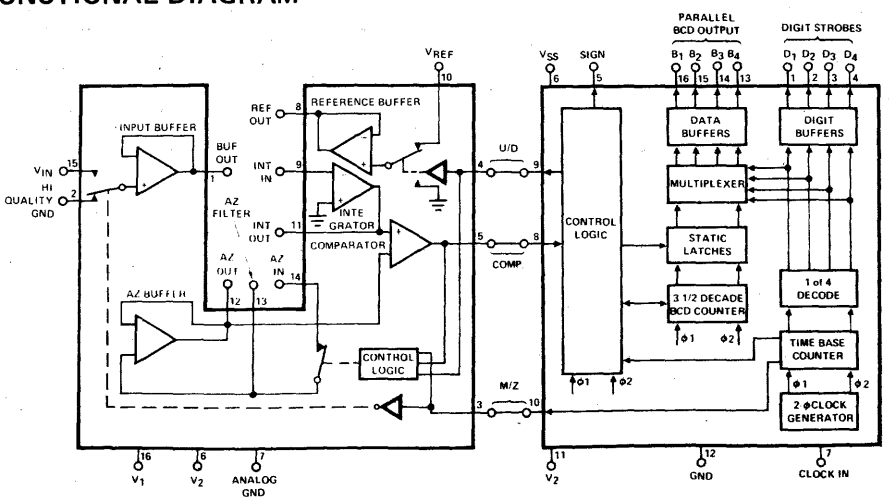
DESCRIPTION

The "Quantized Feedback" conversion scheme used in the LD110/LD111A set provides an Auto-Zeroing, Auto-Polarity A/D system requiring only a single reference voltage.

The monolithic LD111A high performance analog processor contains a bipolar comparator, a bipolar integrating amplifier, a bipolar reference amplifier, two MOSFET input unity gain amplifiers, several P-channel enhancement mode analog switches and the necessary level shifting drivers to allow the analog and digital processors to be directly interfaced. The high impedance input and reference buffer amplifiers eliminate source loading errors and provide the outstanding temperature coefficient inherent in this system. Break-before-make switch action insures that neither the analog input nor the reference voltage will be shorted to ground at any time.

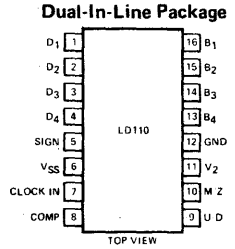
The PMOS LD110 synchronous digital processor combines the counting, storage and data multiplexing functions with the random logic necessary to control the quantized charge-balancing function of the analog processor. Seventeen static latches store the 3 1/2 digits of BCD data as well as overrange, underrange and polarity information. Nine push-pull output buffers (capable of driving one standard TTL load each) provide the sign, digit strobe and multiplexed BCD data outputs, all of which are active high. The digit scan is an interlaced format of digits 1, 3, 2 and 4.

FUNCTIONAL DIAGRAM



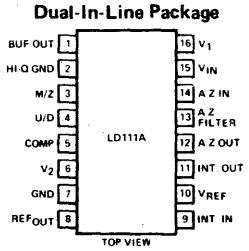
PIN CONFIGURATIONS

Dual-In-Line Package



ORDER NUMBER LD110CJ

Dual-In-Line Package



ORDER NUMBER LD111ACJ

ABSOLUTE MAXIMUM RATINGS

I_{IN} (Pin 15, 2) . . . . . ±1 mA
$V_1 - V_2$ (LD111A) . . . . . 30 V
V_{SS} . . . . . 6 V
$V_{SS} - V_2$ (LD110) . . . . . 20 V
Voltage On Any Pin Relative to V_{SS} (LD110) . . . . . 0.3 V to −20 V
V_{REF} . . . . . V_1

Operating Temperature . . . . . 0 to 70°C
Storage Temperature . . . . . −65 to +125°C
Power Dissipation (Package)* . . . . . 750 mW

*Device mounted with all leads welded or soldered to PC board. Derate 6.3 mW/°C above 25°C.

ELECTRICAL CHARACTERISTICS

All DC parameters are 100% tested at 25°C. Lots are sample tested for AC parameters to assure conformance with specifications.

			Characteristics	Min	Typ	Max	Unit	Test Conditions, Unless Noted: V_1 = +12 V, V_2 = −12 V, V_{SS} = 5 V, V_{REF} = 8.2 V, T_A = 25°C, R_1 = 100K Ω
1	GENERAL		Linearity		0.02		% rdg	
2			Noise		0.1		LSB	Peak-to-Peak Noise Apparent When Going From One Steady Reading to Another
3			Gain T.C.		5		ppm/°C	
4		NMR	Normal Mode Rejection		40		dB	f_{noise} = 60 Hz
5		f_{IN}	Clock Frequency	2	30.7	250	kHz	50% Duty Cycle
6		$r_{DS(on)}$	ON Resistance, Auto Zero Switch		6	20	K Ω	$V_{AZ(in)}$ = −4.0 V, I_S = −30 μA
7	INPUT	I_{CL}	Clock Input Current, Low			−500	μA	V_{CLOCK} in = 0.4 V
8		I_{IN}	Input Bias Current		4		pA	T_A = 25°C
9					40			T_A = 70°C
10	AMPLIFIERS	I_{source}	Reference Buffer	−400	−800		μA	V_{INL} (U/D) = 0.8 V, V_{OUT} = 0
11		I_{sink}	AZ Buffer		800			V_{AZ} = −4 V, V_{OUT} = 0 V
12		I_{sink}	Input Buffer	400	800			V_{IN} = −2 V, V_{OUT} = 0 V
13		I_{source}	Input Buffer	−50	−100			V_{IN} = 2 V, V_{OUT} = 0 V
14		V_{offset}	AZ Buffer	−100		100	mV	V_{OUT} = 0V
15	OUTPUT	V_{OL1}	Measure/Zero Voltage, Low			0.4	V	I_{OL} = 150 μA
16		V_{OH1}	Measure/Zero Voltage, High	2.4				I_{OH} = −200 μA
17		V_{OL2}	Up/Down Logic Voltage, Low			0.4		I_{OL} = 250 μA
18		V_{OH2}	Up/Down Logic Voltage, High	2.4				I_{OH} = −200 μA
19		V_{OH3}	Analog Comparator Voltage	2.4				I_{OH} = −100 μA
20		V_{OL3}	Digits, Bits, Voltage, Low			0.4		I_{OL} = 1.6 mA
21		V_{OL4}	Sign Voltage, Low			0.6		I_{OL} = 1.6 mA
22		V_{OH4}	Data Bits Voltage, High	2.4				I_{OH} = −200 μA
23		V_{OH5}	Digits, Sign Voltage, High	2.4				I_{OH} = −800 μA
24	SUPPLY	I_1	Supply Current		2.2	4.0	mA	
25		I_{2A}	Supply Current, LD111A		−1.8	−3.5		
26		I_{2D}	Supply Current, LD110		−17	−23		
27		I_{SS}	Supply Current		17.4	24		
28		$PSRR_1$	Power Supply Rejection Ratio, V_1	80	85		dB	
29		$PSRR_2$	Power Supply Rejection Ratio, V_2	60	65			
30			Reference Voltage Rejection		1		%Δrdg/ΔV_{REF}	$R_{REF} = R_2$ = 100K Ω, V_{IN} = 2 V

Typical values are for DESIGN AID ONLY, not guaranteed and not subject to production testing

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4½ digit A/D converter set

designed for . . .

- **High Accuracy Digital Voltmeters, Panel Meters**
- **Digital Scales, Thermometers**
- **Microprocessor Data Acquisition Systems**
- **Scientific Instrumentation**

BENEFITS

- **0.005% ±1 Count Accuracy Ensures High System Performance**
- **Two Ranges, ±2.0000 V or ±200.0 mV, With Single Resistor Change**
- **28,500 Count Maximum For 185% Overrange**
- **Sample Rate From One to Five/Second**
- **Auto-Zero Cycle Nulls Out Internal and External Amplifier Offsets**
- **Auto-Polarity Operation with One Reference**
- **Multiplexed BCD Output For Easy Interface To Displays**
- **Two Overrange Outputs, Underrange Output, Blink Inhibit, and Convert-On-Command Capabilities Allow Easy Interface to External Circuitry and Microprocessors**

DESCRIPTION

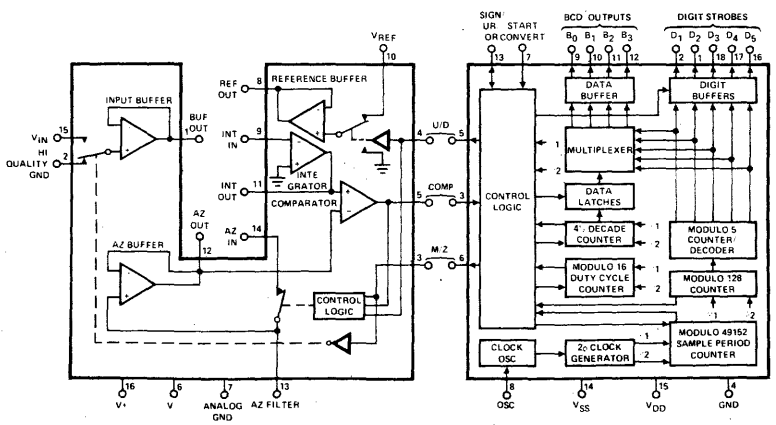
The LD120/LD121 4 1/2 digit A/D system uses Siliconix's proprietary "Quantized Feedback" (patent pending) conversion technique. Intrinsic features of this system are Auto-Polarity, Auto-Zero and ratiometric operation. No critical components are required except for a stable voltage reference. The technique offers superior linearity, normal mode rejection, and stability due to the simultaneous integration of the unknown input and the reference voltages. Unlike other conversion techniques, the integrator output voltage never represents more than 100 counts, thus critical, high resolution performance is not required of either the integrator or comparator.

The LD120 analog processor is fabricated with a unique combined PMOS/Bipolar process. It contains all the necessary amplifiers, MOSFET switches, and switch driver circuits for the system. The reference voltage input is fully buffered on the LD120 to eliminate the reference switch resistance as a source of error. All the amplifiers are internally compensated. The LD120 directly interfaces the LD121 digital processor with no additional active components required.

The LD121 synchronous processor contains all the digital circuitry for the quantized feedback system. Device outputs supply two overrange signals, underrange, sign and 4 1/2 digits of multiplexed BCD data. (All outputs are TTL compatible). Overrange is also indicated by blinking digit strobes above 20,000 counts. An input is provided to inhibit this feature at user option. Microprocessor controlled operation is simplified by a start conversion input that allows conversion-on-command.

Both devices are supplied in space saving 300 mil dual-in-line plastic packages. The LD120 has 16 pins and the LD121 has 18 pins.

FUNCTIONAL BLOCK DIAGRAM

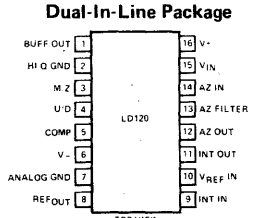


LD120 LD121

SWITCH STATES ARE FOR A LOGIC "0" AT U/D AND M/Z INPUTS.

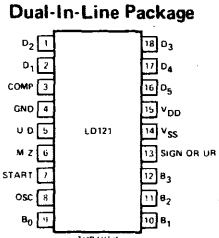
PIN CONFIGURATIONS

Dual-In-Line Package



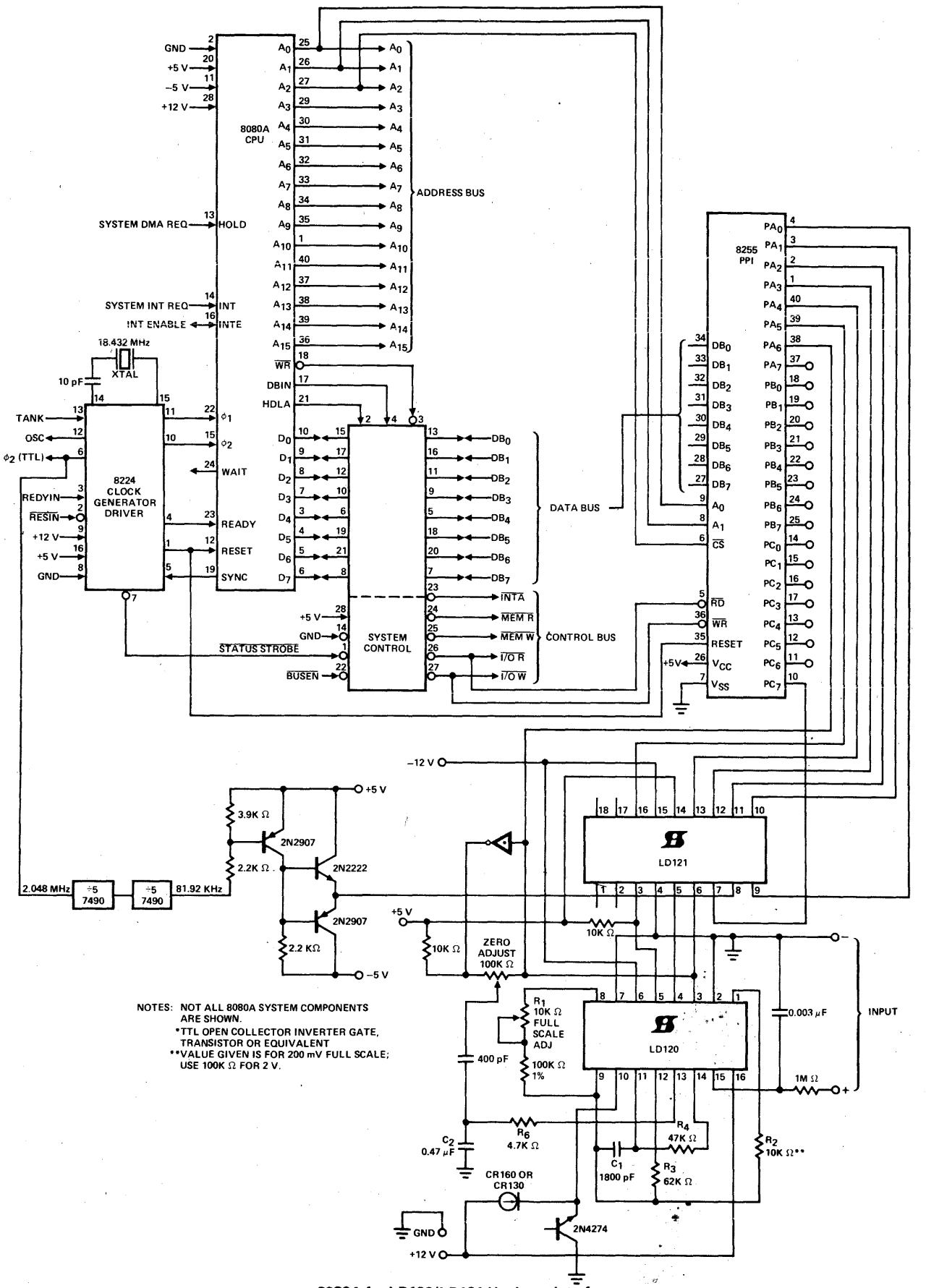
ORDER NUMBER LD120CJ

Dual-In-Line Package



ORDER NUMBER LD121CJ

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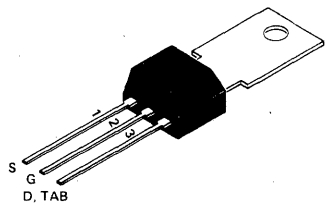
NOTES: NOT ALL 8080A SYSTEM COMPONENTS ARE SHOWN.
*TTL OPEN COLLECTOR INVERTER GATE, TRANSISTOR OR EQUIVALENT
**VALUE GIVEN IS FOR 200 mV FULL SCALE; USE 100K Ω FOR 2 V.

8080A for LD120/LD121 Hardware Interface
Figure 1

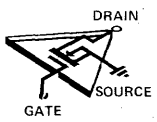
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high speed power peripheral driver (2.0A, 80V) *designed for . . .*

- **Peripheral Drivers for EDP and Process Control Systems**
- **Laser Diode Pulsing**
- **High Speed Line Drivers**
- **CMOS to High Current Interfacing**
- **TTL to High Current Interfacing**
- **Switching Reactive Loads**



TO-202



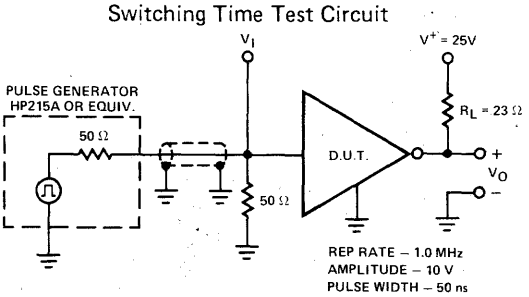
BENEFITS

- Directly Interfaces to CMOS, TTL, DTL and MOS Logic Families
  - Low Drive Current ($I_{GSS} < 100$ nA)
  - Threshold Voltage 0.8 to 2.0 V
- Fan Out From CMOS > 100
- No Power Supply Required
- Permits Improved Data Transmission Rates
  - Propagation Delay Typically 4 nsec
- Reduces Component Count and Design Time/Effort
  - Drives Inductive Loads Directly
  - High Speed
- Improves Reliability
  - Free From Secondary Breakdown Failures and Voltage Derating
  - Input Protected From Static Discharge

ABSOLUTE MAXIMUM RATINGS

Output Voltage	80 V
Continuous Output Current	2.0 A
Peak Output Current	3.0 A
Voltage at Input	±30 V
Power Dissipation at 25°C Case Temperature	15 W
Linear Derating Factor	67 mW/°C
Storage Temperature	−40°C to +150°C
Operating Temperature	−40°C to +150°C
Lead Temperature (1/16" from case for 10 seconds)	300°C

Switching Time Test Circuit



NOTES: 1. Pulse Test – 80 μs, 1% duty cycle
2. Sample Test

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		Characteristic		Min	Typ	Max	Unit	Test Conditions
1	STATIC	V_{IH}	High Level Input Voltage		3.4		V	V_O = 25 V, I_O = 0.1 A
2					4.8		V	V_O = 25 V, I_O = 0.3 A
3					8.0		V	V_O = 25 V, I_O = 1.0 A
4		V_{IL}	Low Level Input Voltage		1.2	0.8	V	V_O = 25 V, I_O = 1.0 mA
5		I_{IH}	High Level Input Current		1	100	nA	V_i = 10 V, V_O = 0 V
6		I_{IL}	Low Level Input Current		1	500	nA	V_i = 0.0 V, V_O = 25 V
7		V_{OL}	Low Level Output Voltage (Note 1)		0.4		V	I_O = 0.1 A, V_i = 5.0 V
8					1.2	1.5	V	I_O = 0.3 A, V_i = 5.0 V
9					2.5	3.0	V	I_O = 1.0 A, V_i = 10 V
10	DYNAM	t_{on}	Turn-ON Time (Note 2)			20	ns	See Switching Time Test Circuit
11		t_{off}	Turn-OFF Time (Note 2)			20	ns	

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Supertex inc.

ED-15 / ED-11 / ED-9 ENCODER - DECODER

FEATURES

- Encoder/Decoder in one circuit
- Schmidt Trigger Input for excellent noise rejection
- Built-in oscillator
- Zener diode to regulate the power supply
- Low power, high noise immunity CMOS technology
- Ability to decode original signals

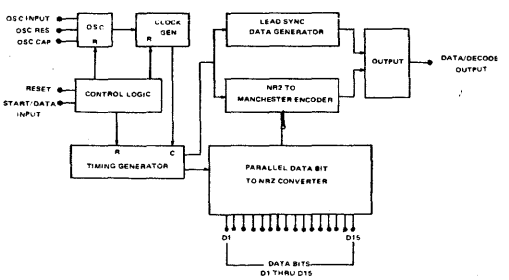
TYPICAL APPLICATIONS

- ☐ Smoke and Fire Alarm Control Systems
- ☐ Theft Alarm Systems
- ☐ Digital Locks
- ☐ Garage Door Openers
- ☐ Security Systems
- ☐ Digital Paging Systems
- ☐ Pocket Pagers
- ☐ Systems that require Special Identification Code
- ☐ Recognition or Transmission

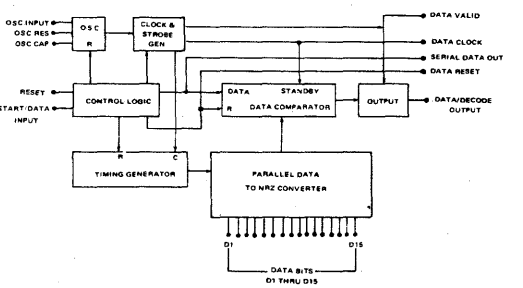
GENERAL DESCRIPTION

ED-15 is a single monolithic chip using metal-gate CMOS technology for low cost, low power, high yield and high reliability. It is a dual purpose circuit, capable of working either as an encoder or as a decoder on special purpose coded identification applications where exclusive recognition of a special code is required. It will decode 1 of 32,768 codes. In the transmit mode each circuit is capable of generating all the possible codes by connecting the Data inputs to V_{DD} or GRD or "1" or "0". A 16 bit shift register (i.e. 4015's) can be attached to a ED-15 for monitoring a large number of encoders and interrogate each input. The encoder code will be loaded into the shift register.

BLOCK DIAGRAM AS A TRANSMITTER



BLOCK DIAGRAM AS A RECEIVER



ED-11 OPTION

The ED-11 is also a multi-purpose circuit identical to ED-15, but it decodes 1 of 2048 codes and transmits 4 bits of control data.

In the transmit mode each circuit is capable of generating all of the 2048 codes by connecting the Data inputs 1 thru 11 to V_{DD} for a "1". A "0" is automatically programmed by leaving the data line open because all the data lines have a pull-down resistor to GRD. Data bits 12 thru 15 can be used to transmit control information up to 16 codes by connecting them to V_{DD} or GRD. In adding external 4 bit shift registers (i.e. ½4015 or two 4013's) it can receive control information that will only be processed after the decoder recognizes the first 11 bits of data. Data bits 1 thru 11 are the only bits that are decoded, but Data Valid will not operate until the 15th bit.

ED-9 OPTION

ED-9 is also a multi-purpose circuit packaged in a 18 pin and has the capability of encoding and decoding 512 codes. Pins handling Serial Data Output, Data Reset, Data Clock Output and Data Valid are not on this device. So the monitoring capability is not available. Apart from these differences mentioned, the ED-9 operates exactly like the ED-15 and ED-11.

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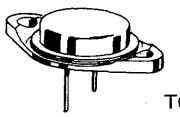
VF-01/VF-12/VF-13/VF-14 N-CHANNEL AND P-CHANNEL ENHANCEMENT-MODE MOSFET DRIVERS

October 1978

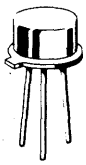
APPLICATIONS

- ☐ High Speed Switching Drivers
- ☐ CMOS Logic to High Current/High Voltage Interface Driver
- ☐ Microprocessor to High Current/ High Voltage Interface Driver
- ☐ TTL to High Current Interface Driver
- ☐ High performance Linear Amplifiers
- ☐ Inductive Load Drivers
- ☐ DC to DC Converters
- ☐ Switching Power Supplies
- ☐ Low Power Complementary High Current/High Voltage Driver
- ☐ Display Driver

Packages



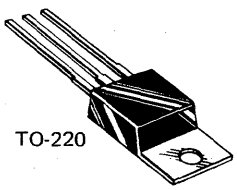
TO-3



TO-39



TO-92



TO-220

BENEFITS

- Directly Interfaces to CMOS, TTL, DTL, and MOS Logic Families.
- Low Drive Current Requirement ($I_{GSS} < 100$ nA).
- Permits more Efficient and Compact Switching Designs, Typical T_{ON} and T_{OFF} less than 5 nsec for 2 Amp device. Very short propagation delay and virtually no storage time delay.
- Reduces Component Count and Design Time/Effort, Drives Inductive Loads Directly, High Gain, Fan-Out from a CMOS Logic Gate exceeds 100 if speed is not critical. Easily Paralleled without Base Current Sharing Resistors to obtain very high Current Output.
- Improves Reliability, Free from Secondary Breakdown and Voltage Derating Output Current decreases as Temperature Increases.

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VF-01/VF-12/VF-13/VF-14 N-CHANNEL AND P-CHANNEL ENHANCEMENT-MODE MOSFET DRIVERS

GENERAL DESCRIPTION

These four device families are normally-off MOSFET Drivers especially suited for Switching and Amplifier Applications where High Input Impedance, High Gain, High Frequency, and Fast Switching speed is desired. They combine the power handling capability of bipolar transistors with the high input impedence and negative temperature coefficient of field effect transistors. The key device parameters are, on-resistance, RDS (on), threshold voltage (V_T), and breakdown voltage (BVDSS). RDS (on) is related to die size, drain current, and V_T. BV_{DSS} depends on V_T and the silicon material used in the device manufacture.

Devices are available with and without Zener input protection.

ELECTRICAL CHARACTERISTICS

	Device Type	Current (Amps)	Voltage ** (Volts)	RDS(on)* (Ohms)	gm* (mhos)	Package Options				
						TO 3	TO39	TO92	TO220	Dice
N-Channel	VF-01	1-2	30-150	2-10	.25	X	X	X	X	X
	VF-12	8-16	30-200	.2-1	3.0	X	X		X	X
	VF-13	.5-1	30-150	4-20	.12		X	X		X
	VF-14	.02	30-150	16-80	.03		X	X		X
P-Channel	VF-01	.5-1	30-150	4-20	.12	X	X	X	X	X
	VF-12	4-8	30-150	.4-2	1.5	X	X		X	X
	VF-13	.25-.5	30-150	8-40	.06		X	X		X
	VF-14	.01	30-150	30-150	.015		X	X		X

*Dependent on current and voltage rating

**Higher voltages will be available in 1979

X Available

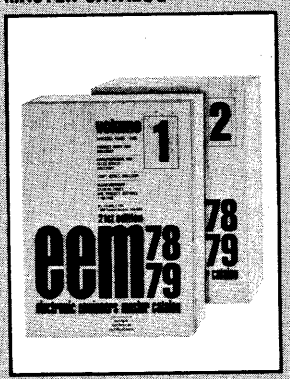
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WE KNOW OUR STUFF

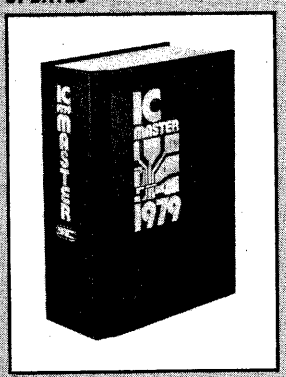
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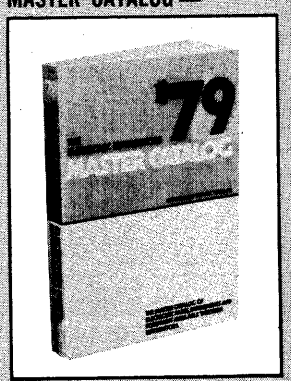
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INTRODUCTION TO LINEAR

The Master Selection Guide provides sufficient information to make initial product selections. It enables you to find the products which are most appropriate to fulfill your major requirements and then provides data for many of the more important products.

All devices that appear in this section, both in the initial selection guide and in the data pages, are included in all other indexes. These index listings lead to the page and the line on that page where each device appears.

In the Linear section over 1000 operational amplifiers are covered. Since there are so many devices, the operational amplifier entries have been given special consideration. Separate lists are provided for those which have High Speed, High Voltage capability, Wide Bandwidth, etc. Under General Purpose, four amplifier types are listed; these are the ones that the high volume manufacturers indicate are the most widely used; however, quad amplifiers should also be considered when appropriate. If you have located an op amp in a specialized category, you can review its characteristics by finding it in the Part Number or Product Indexes and looking it up in the Operational Amplifier Characteristics and in the Data Sections.

Following the special lists, the "Operational Amplifier-Characteristics" listings, categorize amplifiers by input parameters. They are arranged in order of increasing offset voltage, bias current, offset current and then voltage drift. The other parameters listed do not affect the sequence in which the devices are presented. The column labeled "Comp" indicates the number of external components normally used for compensation; for example, "0" means no compensation is required.

Consumer circuits such as audio amplifiers, AM, FM, and TV circuits as well as some digital devices (watches, calculators, etc.) are covered by model number in the Consumer Circuit Section. Linear devices and unusual circuits which do not fit elsewhere are listed under the heading "Other Linear Devices."

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The manufacturers listed above are providing detailed information on their latest and most significant products.

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LINEAR–Amplifiers, Special Purpose

Special Purpose

Function	Device	Source	Line
AC Amplifier, Dual with automatic gain control, for tape recorders	M5130	Mitsubishi	
	M51301	Mitsubishi	
AC Amplifier, Quad, Single Supply	CA3048	†RCA	
	CA3052	RCA	
AGC/Squelch Amplifier (Gain Controlled Amplifier)	LM170	† National	
	LM270	National	10
	LM370	National	
AGC Generator, for SSB receivers	SL621C	Plessey	
	SL1621C	Plessey	
AGC Generator (voice operated gain adjusting device)	SL620C	Plessey	
	SL622C	Plessey	
	SL1620C	Plessey	
	SL1626C	Plessey	
Amplifier, CATV. See Linear—Consumer Circuits, TV			20
Amplifier, Audio with three NPN transistors	LM389	National	
Amplifier, triple for active filters (See also Linear—Other Devices, Active Filters)	TAA960	Signetics	
Current Amplifier (unity gain, 100 ma output)	SH0002C	Fairchild	
	LH0002	† National	
	LH0002C	National	
	9910	†OEI	30
Current Amplifier (unity gain, 200 ma output)	**3553**	**† Burr-Brown (920)**	
	9963	†OEI	
Current Amplifier (unity gain, 300 ma output)	MC1438	Motorola	
	MC1538	† Motorola	
Current Amplifier (unity gain, 500 ma output)	823	Beckman	
	9911	†OEI	
Current Amplifier (unity gain, 600 ma output)	**HA-2630**	**† Harris (982)**	40
	HA-2635	**Harris (982)**	
Current Amplifiers, See also Linear-Followers			
Differential Input/Differential Output Amplifier (bandwidth less than 2 MHz)	µA730C	Fairchild	
	µA730M	† Fairchild	
	MC1590G	† Motorola	
	CA3000	†RCA	
	CA3007	†RCA	50
	NE515	Signetics	
	SE515	† Signetics	
Differential Input/Single Output DC Amplifier with switched inputs for a gain of ±1	MN2120	Micro Net	
	MN2120H	† Micro Net	
Differential/Cascode Amplifier (dc to r.f.)	MC3330	Motorola	
	LM3028	† National	
	LM3053	† National	60
	CA3028	†RCA	
	CA3028A	†RCA	
	CA3028B	†RCA	
	CA3053	†RCA	

Special Purpose (Cont'd.)

Function	Device	Source	Line
Followers. See Linear-Followers			
Floppy Disc Read Amplifier System	MC3470	Motorola	
Front End Amplifier, for ultrasonic or infrared remote control systems	TDA4180	Telefunken	
Gated Linear Amplifier (operational amplifier)	ZN424	Ferranti	70
Hearing Aid Amplifiers. See Linear-Consumer Circuits			
Instrumentation, (Differential Input, Independent Gain Adjustment)	AD520J	AD	
	AD520K	AD	
	AD520S	†AD	
	AD521J	AD	
	AD521K	AD	
	AD521S	†AD	80
	AD522A	AD	
	AD522B	AD	
	AD522S	†AD	
	3626A	**Burr-Brown (920)**	
	3626B	**Burr-Brown (920)**	
	3626C	**Burr-Brown (920)**	
	3629	**† Burr-Brown (920)**	
	3630A	Burr-Brown	
	3630B	Burr-Brown	
	3630C	Burr-Brown	90
	3630S	Burr-Brown	
	3660J	**Burr-Brown (920)**	
	3660K	**Burr-Brown (920)**	
	3660S	**† Burr-Brown (920)**	
	3662	**Burr-Brown (920)**	
	HC3020	HyComp	
	MN2200	Micro Net	
	MN2200H	† Micro Net	
	LH0036	**† National (1073)**	
	LH0036C	**National (1073)**	100
	LH0037	**† National (1073)**	
	LH0037C	**National (1073)**	
Instrumentation, (Differential FET Input, Independent Gain Adjustment)	3670J	Burr-Brown	
	3670K	Burr-Brown	
	3670S	† Burr-Brown	
	AM-435-1C	**Datel (689)**	
	AM-435-1M	**† Datel (689)**	
	LF152	† National	110
	LF252	National	
	LF352	**National (1073)**	
	LF152	†TI	
	LF252	TI	
	LF352	TI	
Instrumentation, (unity gain)	**3627**	**Burr-Brown (920)**	
Instrumentation, with low pass filter	MN2200	Micro Net	
	MN2200H	† Micro Net	120
Isolation Amplifier, Optically Coupled	**3650**	**Burr-Brown (921)**	
	3652HG	**Burr-Brown (921)**	
Amplifier for IR remote control (1300 db gain, 8 kHz bandwidth)	U250	Telefunken	

Special Purpose (Cont'd.)

Function	Device	Source	Line
Linear-Antilog Amplifier, Dual (Differential input, separate control input)	SSM2000	SSM	
	SSM2020	**SSM (564)**	130
Log/Antilog Amplifier, (Antilog)	ICL8049C	Intersil	
	2910	†OEI	
Log/Antilog Amplifier, (Log)	**4127**	**Burr-Brown (921)**	
	ICL8048C	Intersil	
	2910	†OEI	
	TL441C	TI	
	TL441M	†TI	
Microphone/Headphone Amplifier	M51304	Mitsubishi	140
	SL630C	Plessey	
	SL1630	Plessey	
Microphone Amplifier (for microphones in telephones)	TAA970	Signetics	
	TCA980	Signetics	
Mixer (to 200 MHz)	S042	Siemens	
MOS Amplifier, MOS and NPN transistors, 3 terminal	TAA320	Signetics	150
	TAA320A	Signetics	
Operational Amplifier, Dual with Dual Voltage Comparator	MC3405	Motorola	
	MC3505	† Motorola	
Operational Amplifier/Voltage Comparator, Dual	**LM192**	**† National (1054)**	
	LM292	**National (1054)**	
	LM392	**National (1054)**	
	LM2924	**National (1054)**	160
Operational Transconductance Amplifier	CA3060	RCA	
	CA3060	†RCA	
	CA3060A	†RCA	
	CA3060B	†RCA	
	CA3080	RCA	
	CA3080A	†RCA	
Operational Transconductance Amplifier, Dual	**LM11600**	**† National (1050)**	
	LM13600	**National (1050)**	170
	LM13600A	**National (1050)**	
Power Amplifier, Motor and Actuator Driver, to 24V, 3a	ICH8510C	Intersil	
	ICH8510M	† Intersil	
	ICH8520C	Intersil	
	ICH8520M	† Intersil	
	ICH8530C	Intersil	
	ICH8530M	† Intersil	
Power Amplifier/Switch (equivalent to an operational amplifier with uncommitted Darlington power output transistor), Programmable Gain	CA3094	†RCA	180
	CA3094A	†RCA	
	CA3094B	†RCA	
Power Transistor Driver/Amplifier; boosts ±12V op amp outputs to ±30V	ICL8063	Intersil	
	ICL8063M	† Intersil	
Preamplifier JFET (to precede operational amplifiers and comparators)	HA-2000	†Harris	190

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Values

LINEAR–Amplifiers, Special Purpose (Cont'd)

Function	Device	Source	Line
Special Purpose (Cont'd.)			
Preamplifier JFET (to precede operational amplifiers and comparators) (Cont'd.)			
	HA-2005	Harris	
Preamplifier, Infrared (74 db gain, 100 kHz bandwidth)			
	TDA4050	Siemens	
Preamplifier, Low Noise (35 to 67 db gain, 3.6 MHz bandwidth)			
	SL1202	† Plessey	
	SL1203	† Plessey	
Preamplifier, Low Noise (49-59 db gain, 6.5 MHZ bandwidth)			10
	SL1205	Plessey	
Preamplifier, Low Noise. (60db gain, 15MHz bandwidth)			
	ZN459	† Ferranti	
	ZN459C	Ferranti	
	ZN459CP	Ferranti	
Preamplifier, Low Noise (40db gain, 20 MHz bandwidth)			
	9913	OEI	20
Preamplifier, Precision (to precede operational amplifiers)			
	LM121	† National	
	LM221	National	
	LM321	National	
	LM121A	† National	
	LM221A	National	
	LM321A	National	
Preamplifier, Temperature Controlled			
	μA727C	Fairchild	30
	μA727M	† Fairchild	
Preamplifier, with ALC transistors for tape recorders			
	LA3201	Sanyo	
	TDA2054	SGS	
	TDA1002	Signetics	
	TA7137	Toshiba	
	TA7137-ST	Toshiba	
	TA7307	Toshiba	
Programmable Channel Op Amp (one of 4 input stages can be connected to single output)			40
	HA-2400	**† Harris**	**(964)**
	HA-2404	**Harris**	**(964)**
	HA-2405	**Harris**	**(964)**
Programmable gain amplifier, digitally controlled gain			
	3606	**Burr-Brown**	**(920)**
	MN2020	Micro Net	
Read Amplifier/Preamplifier (for magnetic tape memory systems)			
	MC3467	Motorola	
	MC3468	Motorola	50
RF Amplifiers, Hybrids; Capable of operation above 100 MHZ (See also: Consumer Circuits— T.V., CATV Amplifiers)			
	MHW401	Motorola	
	MHW590	Motorola	
	MHW591	Motorola	
	MHW592	Motorola	
	MHW593	Motorola	
	MHW601	Motorola	
	MHW602	Motorola	60
	MHW603	Motorola	
	MHW709	Motorola	
	MHW710	Motorola	
	CA2800	TRW	
	CA2810	TRW	
		(Continued)	

Function	Device	Source	Line
Special Purpose (Cont'd.)			
RF Amplifiers, Hybrids; Capable of operation above 100 MHZ (See also: Consumer Circuits— T.V., CATV Amplifiers) (Cont'd.)			
	CA2820	TRW	
	CA2830	TRW	70
	CA2840	TRW	
	CA2842	TRW	
	CA2850	TRW	
	CA2851	TRW	
	CA2870	TRW	
	CA2871	TRW	
	CA2875	TRW	
	CA2876	TRW	
	CA2880	TRW	
R.F. Amplifier, Gated			80
	MC1445	Motorola	
	MC1545	† Motorola	
Signal Sources Switch, (Buffer Amplifiers with input switches)			
	TDA1028	Signetics	
	TDA1029	Signetics	
Single-ended Input/Output Amplifier, Triple			
	CA3035	RCA	
Two Wire Transmitter (Sends current signal over same two lines from which it is powered)			90
	LH0045	† National	
	LH0045C	National	
Video, IF and RF Amplifiers			
	592C	AMD	
	592M	† AMD	
	733	† AMD	
	733C	AMD	
	μA703C	Fairchild	
	μA703M	† Fairchild	
	μA733C	Fairchild	100
	μA733M	† Fairchild	
	μA753	Fairchild	
	TBA970	Fairchild	
	HA1110	Hitachi	
	HA17733	Hitachi	
	733C	Intersil	
	733M	† Intersil	
	753	Intersil	
	MC1350	Motorola	
	MC1410	Motorola	110
	MC1510	† Motorola	
	MC1550	† Motorola	
	MC1552	† Motorola	
	MC1553	† Motorola	
	MC1590G	† Motorola	
	MC1733	† Motorola	
	MC1733C	Motorola	
	NE592	Motorola	
	SE592	† Motorola	
	LM171	† National	120
	LM271	National	
	LM371	National	
	LM703	† National	
	LM703C	National	
	LM733	† National	
	LM733L	National	
	LM3011	National	
	AN606	Panasonic	
	AN607	Panasonic	
	AN608	Panasonic	130
	SL541	Plessey	
	SL550	Plessey	
	SL560	Plessey	
	SL610C	Plessey	
		(Continued)	

Function	Device	Source	Line
Special Purpose (Cont'd.)			
Video, IF and RF Amplifiers (Cont'd.)			
	SL611C	Plessey	
	SL612C	Plessey	
	SL1550	Plessey	
	SL1610C	Plessey	
	SL1611C	Plessey	140
	SL1612C	Plessey	
	SL1030	† Plessey	
	RC733	Raytheon	
	RM733	† Raytheon	
	CA3001	† RCA	
	CA3002	† RCA	
	CA3004	† RCA	
	CA3005	† RCA	
	CA3006	† RCA	
	CA3011	† RCA	150
	CA3012	† RCA	
	CA3020	† RCA	
	CA3020A	RCA	
	CA3021	† RCA	
	CA3022	† RCA	
	CA3023	† RCA	
	CA3040	† RCA	
	TBA400	Siemens	
	NE592	Signetics	
	SE592	† Signetics	160
	TAA263	Signetics	
	TBA1440	Signetics	
	TDA2541	Signetics	
	μA733	† Signetics	
	μA733C	Signetics	
	SG733	† Silicon G	
	SG733C	Silicon G	
	SG1401	† Silicon G	
	SG2401	Silicon G	
	SG3001	† Silicon G	170
	SG3401	Silicon G	
	TDA440	Telefunken	
	μA733C	TI	
	μA733M	† TI	
	TA7061A	Toshiba	
	TA7084	Toshiba	
	TA7084A	Toshiba	
Gain Controlled IF Amplifier			
	μA757	Fairchild	
	SL550	Plessey	180
Limiting Amplifier/Detector (IF or RF)			
	SL613C	Plessey	
	SL1613C	Plessey	
Voltage Controlled Amplifier: See also Compander under: Linear—Telecommunication Circuits			
Voltage Controlled Amplifier			
	SSM2000	SSM	
	SSM2020	**SSM**	**(564)**
Wideband Amplifier with low level video detection (7 to 200 MHz for log IF amplifiers)			190
	SL521	Plessey	
	SL571	Plessey	
	SL525	† Plessey	
	SL613C	Plessey	
	SL1521	† Plessey	
	SL1522	Plessey	
	SL1523	Plessey	
Wideband Amplifier, Logarithmic limiting (4 to 85 MHz)			
	SL530C	Plessey	

† Military Temperature Range (−55° to 125°C)

* Typical Values

Bold face indicates additional data is provided on the page noted.

LINEAR–Amplifiers, Special Purpose (Cont'd)

Function	Device	Source	Line
Special Purpose (Cont'd.)			
Wideband Amplifier, Triple	CA3035	†RCA	

† Military Temperature Range (−55° to 125°C)

* Typical Values

LINEAR–Arrays

Transistor Arrays

Function	Device	Source	Line
Dual Transistors, Monolithic NPN Tightly Matched			
	AD810	† AD	
	AD811	† AD	
	AD812	† AD	
	AD813	† AD	
	AD814	† AD	
	AD815	† AD	
	AD816	† AD	
	IT120	Intersil	
	IT120A	Intersil	10
	IT121	Intersil	
	IT122	Intersil	
	LM114	† Intersil	
	LM114A	† Intersil	
	LM115	† Intersil	
	LM115A	† Intersil	
	MP301	Micro Power	
	MP302	Micro Power	
	MP303	Micro Power	
	MP310	Micro Power	20
	MP311	Micro Power	
	MP312	Micro Power	
	LM114	† National	
	LM114A	† National	
	LM115	† National	
	LM115A	† National	
	LM194	† National	
	LM394	National	
	LM3018A	† National	
	LM3018	† National	30
	SL301	Plessey	
	SL360	Plessey	
	SL362	Plessey	
	MAT-01	† PMI	
	MAT-01A	† PMI	
	MAT-01F	† PMI	
	MAT-01G	† PMI	
Dual Transistors, Monolithic PNP, Tightly Matched			
	AD820	† AD	
	AD821	† AD	40
	AD822	† AD	
	IT130	Intersil	
	IT130A	Intersil	
	IT131	Intersil	
	IT132	Intersil	
	MP350	Micro Power	
	MP351	Micro Power	
	MP352	Micro Power	
Dual Transistors, Monolithic NPN, Logarithmic Conformance			50
	AD818	† AD	
	MP318	Micro Power	
	MAT-01	† PMI	
	MAT-01A	† PMI	
	MAT-01F	† PMI	
	MAT-01G	† PMI	
Dual Transistors, Monolithic PNP, Logarithmic Conformance			
	MP358	Micro Power	
Dual Transistors, NPN, Matched plus a third transistor			60
	SL303	Plessey	
Dual Matched Transistor Pairs, NPN			
	SL354	Plessey	
Darlington Pair and two Matched NPN Transistors			
	μA3018M	† Fairchild	
	μA3018AM	† Fairchild	
	LM3018	† National	
	LM3018A	† National	

(Continued)

Transistor Arrays (Cont'd.)

Function	Device	Source	Line
Darlington Pair and two Matched NPN Transistors (Cont'd.)			
	LM3118	† National	70
	LM3118A	† National	
	SFC2018	† NPC	
	SL3018	† Plessey	
	SL3018A	† Plessey	
	SL3118	† Plessey	
	SL3118A	† Plessey	
	CA3018	† RCA	
	CA3018A	† RCA	
	CA3118	† RCA	
	CA3118A	† RCA	80
	SG3018	† Silicon G	
	SG3018A	† Silicon G	
	SG3818	Silicon G	
	SG3818A	Silicon G	
Dual Darlington (NPN)			
	μA3036M	† Fairchild	
	SFC2036	† NPC	
	SL305	Plessey	
	CA3036	† RCA	
Dual Darlington (NPN-PNP Quasi Complementary)			90
	TDA1410	SGS	
	TDA1420	SGS	
Dual Darlington Switch			
	ULN-2061	Sprague	
	ULN-2062	Sprague	
Quad Darlington Switch			
	ULN-2064	Sprague	
	ULN-2065	Sprague	
	ULN-2066	Sprague	
	ULN-2067	Sprague	100
	ULN-2068	Sprague	
	ULN-2069	Sprague	
	ULN-2070	Sprague	
	ULN-2071	Sprague	
	ULN-2074	Sprague	
	ULN-2075	Sprague	
	ULN-2076	Sprague	
	ULN-2077	Sprague	
	UDN-2841	Sprague	
	UDN-2842	Sprague	110
	UDN-2843	Sprague	
	UDN-2844	Sprague	
	UDN-2845	Sprague	
	UDN-2846	Sprague	
	UDN2841	TI	
	UDN2842	TI	
	UDN2843	TI	
	UDN2844	TI	
	UDN2845	TI	
	UDN2846	TI	120
	ULN2064	TI	
	ULN2065	TI	
Four High Current NPN Transistors (Core Driver)			
	FQ3724	Fairchild	
	FQ3725	Fairchild	
	MHQ4001A	Motorola	
	MHQ4002A	Motorola	
	MHQ4013	Motorola	
	MHQ4014	Motorola	
	MPQ3303	Motorola	130
	MPQ3725	Motorola	
	MPQ3725A	Motorola	
	MPQ4003	Motorola	
	MPQ4004	Motorola	
	DH3725C	National	

(Continued)

Transistor Arrays (Cont'd.)

Function	Device	Source	Line
Four High Current NPN Transistors (Core Driver) (Cont'd.)			
	DH6376C	National	
	AN807	Panasonic	
	CA3138	† RCA	
	CA3138A	† RCA	140
	CA3724	† RCA	
	CA3725	† RCA	
	TPQ3724	Sprague	
	TPQ3725	Sprague	
	TPQ3725A	Sprague	
Four High Current PNP Transistors (Core Driver)			
	FQ3467	Fairchild	
	FQ3468	Fairchild	
	MHQ3467	Motorola	
	DH3467C	National	150
Differential Pair and Three NPN Transistors			
	μA3045M	† Fairchild	
	μA3046C	Fairchild	
	μA3086C	Fairchild	
	HA1127	Hitachi	
	MC3346	† Motorola	
	MC3386	† Motorola	
	LM3045	† National	
	LM3046	National	
	LM3086	National	160
	LM3145	† National	
	LM3145A	† National	
	LM3146	National	
	LM3146A	National	
	SFC2046	† NPC	
	AN903	Panasonic	
	AN905	Panasonic	
	SL3045	† Plessey	
	SL3046	Plessey	
	SL3086	Plessey	170
	SL3145	† Plessey	
	SL3146	Plessey	
	CA3045	† RCA	
	CA3046	† RCA	
	CA3086	† RCA	
	CA3146	RCA	
	CA3146A	RCA	
	L159	SGS	
	TBA331	SGS	
	TCA671	Siemens	180
	TCA871	Siemens	
	TCA971	Siemens	
	TCA991	Siemens	
	SG3045	Silicon G	
	SG3046	Silicon G	
	SG3086	† Silicon G	
	SG3146	Silicon G	
	SG3821	Silicon G	
	SG3886	Silicon G	
	ULS-2045	† Sprague	190
	ULN-2046	Sprague	
	ULN-2086	Sprague	
Three NPN and two PNP Transistors			
	CA3096	† RCA	
	CA3096A	† RCA	
	CA3096C	† RCA	
Five High Current NPN Transistors			
	SL3083	† Plessey	
	SL3183	† Plessey	
	CA3083	† RCA	200
	CA3183	† RCA	
	CA3183A	† RCA	
	CA3083	† Signetics	

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Values

Bold face indicates additional data is provided on the page noted.

LINEAR–Arrays (Cont'd)

Transistor Arrays (Cont'd.)

Function	Device	Source	Line
Five High Current NPN Transistors (Cont'd.)			
	CA3183	† Signetics	
	CA3183A	† Signetics	
	TDA3083	Signetics	
	SG3083	† Silicon G	
	SG3183	† Silicon G	
	SG3183A	† Silicon G	
	ULN-2083	Sprague	
	ULS-2083	† Sprague	
Five High Frequency NPN Transistors, (f_t > GHz)			10
	SL3127	Plessey	
	CA3127	RCA	
Dual Darlington (NPN) and two NPN Transistors			
	SG3823	Silicon G	
Dual Differential Amplifiers (NPN) with diode			
	M5109	Mitsubishi	
Dual Differential Amplifiers (NPN), to 120 MHz			
	µA3026	† Fairchild	
	µA3054	Fairchild	
	CA3054	Motorola	20
	LM3026	† National	
	LM3054	National	
	AN904	Panasonic	
	CA3026	† RCA	
	CA3054	RCA	
	SG3822	Silicon G	
	ULN-2054A	Sprague	
Dual Differential Amplifiers (NPN), biasing, to above 100 MHz			
	NE510	Signetics	30
	NE511	Signetics	
	SE510	† Signetics	
	SE511	† Signetics	
Dual Differential Amplifiers (NPN), to 500 MHz			
	CA3049	† RCA	
	CA3102	† RCA	
Dual Differential Darlington Amplifiers (NPN) with Diode Bias String			
	CA3050	† RCA	
	CA3051	RCA	40
Three Differential Amplifiers (NPN)			
	ULN-2047A	Sprague	
One Darlington PNP Pair, and one Current Mirror Pair with shared Diode, and two PNP Transistors			
	MC1416	Motorola	
	CA3084	RCA	
Five High Voltage, High Current NPN Darlington Amplifiers			
	M54516	Mitsubishi	
	M54521	Mitsubishi	50
	LB1287	Sanyo	
	LB1288	Sanyo	
Five High Voltage, High Current NPN Darlington Amplifiers, Source, for load connected to negative supply			
	UDN-2956A	Sprague	
	UDN-2957A	Sprague	
Seven NPN Transistors, Common Emitter			
	SL3081	Plessey	
	CA3081	† RCA	60
	CA3081	Signetics	
	TDA3081	Signetics	
	SG3081	Silicon G	
	ULN-2081A	Sprague	

Transistor Arrays (Cont'd.)

Function	Device	Source	Line
Seven High Current NPN Transistors, Common Collector			
	SL3082	Plessey	
	CA3082	† RCA	
	CA3082	Signetics	
	TDA3082	Signetics	70
	SG3082	Silicon G	
	ULN-2082A	Sprague	
Seven NPN Darlingtons			
	M54514	Mitsubishi	
	LB1270	Sanyo	
Seven High Current Darlingtons			
	M54517	Mitsubishi	
	M54519	Mitsubishi	
	ULN-2031A	Sprague	
	ULN-2032A	Sprague	80
	ULN-2033A	Sprague	
Seven High Current, High Voltage NPN Darlington Amplifiers, Open Collector, to 50v, 500ma			
	XR2201	**Exar** (931)	
	XR2201M	**† Exar** (931)	
	XR2202	**Exar** (931)	
	XR2202M	**† Exar** (931)	
	XR2203	**Exar** (931)	
	XR2203M	**† Exar** (931)	
	XR2204	**Exar** (931)	90
	XR2204M	**† Exar** (931)	
	9665	Fairchild	
	9666	Fairchild	
	9667	Fairchild	
	9668	Fairchild	
	M54523	Mitsubishi	
	M54524	Mitsubishi	
	M54525	Mitsubishi	
	MC1411	Motorola	
	MC1412	Motorola	100
	MC1413	Motorola	
	MC1416	Motorola	
	ULN2001	Signetics	
	ULN2002	Signetics	
	ULN2003	Signetics	
	ULN2004	Signetics	
	PBD352301	RIFA	
	PBD352302	RIFA	
	PBD352303	RIFA	
	L201	SGS	110
	L202	SGS	
	L203	SGS	
	L204	SGS	
	SG2001	Silicon G	
	SG2002	Silicon G	
	SG2003	Silicon G	
	SG3851	Silicon G	
	SG3852	Silicon G	
	SG3853	Silicon G	
	ULN-2001A	Sprague	120
	ULN-2002A	Sprague	
	ULN-2003A	Sprague	
	ULN-2004A	Sprague	
	ULN-2005A	Sprague	
	ULS-2001H	† Sprague	
	ULS-2002H	† Sprague	
	ULS-2003H	† Sprague	
	ULS-2004H	† Sprague	
	SN75466	TI	
	SN75467	TI	130
	SN75468	TI	
	SN75469	TI	
	ULN2001A	TI	

(Continued)

Transistor Arrays (Cont'd.)

Function	Device	Source	Line
Seven High Current, High Voltage NPN Darlington Amplifiers, Open Collector, to 50v, 500ma (Cont'd.)			
	ULN2002A	TI	
	ULN2003A	TI	
	ULN2004A	TI	
Seven High Current, High Voltage NPN Darlington Amplifiers, Open Collector, to 50v, 600ma			140
	ULN-2011A	Sprague	
	ULN-2012A	Sprague	
	ULN-2013A	Sprague	
	ULN-2014A	Sprague	
	ULN-2015A	Sprague	
Seven High Current, High Voltage NPN Darlington Amplifiers, Open Collector, to 95v, 500ma			
	NE5501	Signetics	
	NE5502	Signetics	
	NE5503	Signetics	150
	NE5504	Signetics	
	ULN-2021A	Sprague	
	ULN-2022A	Sprague	
	ULN-2023A	Sprague	
	ULN-2024A	Sprague	
	ULN-2025A	Sprague	
Eight High Current, High Voltage NPN Darlington Amplifiers, Open Collector, to 50v, 500ma			
	ULN-2801A	Sprague	
	ULN-2802A	Sprague	160
	ULN-2803A	Sprague	
	ULN-2804A	Sprague	
	ULN-2805A	Sprague	
Eight High Current, High Voltage NPN Darlington Amplifiers, Open Collector, to 50v, 600ma			
	ULN-2811A	Sprague	
	ULN-2812A	Sprague	
	ULN-2813A	Sprague	
	ULN-2814A	Sprague	
	ULN-2815A	Sprague	170
Eight High Current, High Voltage NPN Darlington Amplifiers, Open Collector, to 95v, 500ma			
	ULN-2821A	Sprague	
	ULN-2822A	Sprague	
	ULN-2823A	Sprague	
	ULN-2824A	Sprague	
	ULN-2825A	Sprague	
Eight High Current, High Voltage NPN Darlington Amplifiers, Current Source			
	UDN-2981A	Sprague	180
	UDN-2982A	Sprague	
	UDN-2983A	Sprague	
	UDN-2984A	Sprague	
Super Beta Differential Cascode Amplifier and three NPN Transistors			
	CA3095	† RCA	

Special Arrays

Function	Device	Source	Line
Audio Amplifier and three NPN transistors			
	LM389	National	
CMOS (Three p-channel and three n-channel enhancement MOS Transistors tested for linear operation)			190
	CA3600	† RCA	
Thyristor/Transistor Array (SCR, Programmable Unijunction Transistor, PNP/NPN Transistor Pair, NPN Transistor and Zener Diode)			
	CA3097	† RCA	

† Military Temperature Range (−55° to 125°C)

* Typical Values

LINEAR–Arrays (Cont'd)

Function	Device	Source	Line
Special Arrays (Cont'd.)			
Transistor/Diode Array (Three NPN Transistors two Zener Diodes and one Diode)	CA3093	RCA	
Eight SCRs	TCP2410	TI	
	TCP2411	TI	

Function	Device	Source	Line

Function	Device	Source	Line

† Military Temperature Range (−55° to 125°C)

* Typical Values

Bold face indicates additional data is provided on the page noted.

LINEAR–Comparators

Comparators-Single

Offset Voltage mv (25°C)	Bias Current (25°C)	Offset Current (25°C)	Response Time ns	Max. Differential Voltage	Gain	Fan Out	Supply Voltage	Device	Source
0.8	50nA	3nA	270	11	200K		5 to ±18	CMP-02	†PMI
								CMP-02B	PMI
								CMP-02E	PMI
	600nA	25nA	180	11	200K		5 to ±18	CMP-01	†PMI
								CMP-01B	PMI
								CMP-01E	PMI
1.0	6.0μA	1.5μA	55	15	—	—	±15,5	HA-4950	†Harris
	15μA	1μA	60	5	1400		-6,12	RM710A	Raytheon
2.0	10μA	1μA	6.5	6			-5.2,6	685L	AMD
								685M	†AMD
			12	6		5	-6,5	686M	†AMD
	15μA	3μA	80	5	12.5K		-6,12	TL810M	†TI
	20μA	3μA	40	5	40K*	10	-3 to -12,12	LM106	†AMD
								LM206	AMD
								LM106	†National
								LM206	National
								LM106	†TI
								LM206	TI
			40*	5	1250	1	-6,12	μA710M	†Fairchild
								MC1710	†Motorola
								LM710	†National
								μA710	†Signetics
								SG710	†Silicon G
								SFC2710	†NPC
								μA710M	†TI
			60	5	1250	1	-6,12	RM710	†Raytheon
2.8	100nA	15nA	270	11	100K		5 to ±18	CMP-02C	PMI
	900nA	80nA	180	11	200K		5 to ±18	CMP-01C	PMI
3.0	50nA	10nA	200	10	35K		±5 to ±18	μA734M	†Fairchild
	100nA	10nA	165*	30	200K*	5	5, 0 to ±15	LM111	†TI
			200*	30	200K*	5	5, 0 to ±15	AD111	†AD
								AD211	AD
								μA111M	†Fairchild
								111	†Intersil
								211	Intersil
								LM111	†Motorola
								LM211	Motorola
								LM111	†National
								LM211	National
								SFC2111	†NPC
								SFC2211	NPC
								CA111	†RCA
								CA211	RCA
								LM111	†Raytheon
								LM211	Raytheon
								LM111	†Signetics
								LM211	Signetics
								SG111	†Silicon G
								SG211	Silicon G
			250	30	200K*	5	5, 0 to ±15	LM111	†AMD
								LM211	AMD
		20nA	250*	15	15K		5-15, ±5-±15	ICL8001M	†Intersil
	5μA	2μA*	20	5	3K*	2	5,(-6, 5-±15)	LM161	†National
								LM261	National
	10μA	1μA	12	6			-6, 5	686C	AMD
	25μA	7μA	80	5	10K		-6, 12	TL510M	†TI
3.5	20μA	5μA	80	5	10K		-6,12	TL510C	TI
								TL810C	TI
4.0	50pA	25pA	200*	30	200K*	5	5, 0 to ±15	LF111	†AMD
								LF211	AMD

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Values

LINEAR–Comparators (Cont'd)

Offset Voltage mv (25°C)	Bias Current (25°C)	Offset Current (25°C)	Response Time ns	Max. Differential Voltage	Gain	Fan Out	Supply Voltage	Device	Source
Comparators-Single									**(Cont'd.)**
4.0	50pA	25pA	200*	30	200K*	5	5, 0 to ±15		(Cont'd.)
								μAF111	† Fairchild
								LF111	**† National (1035)**
								LF211	National
	2μA	0.5μA	26	5	5K*		5,(-6, 5-±10)	**SE527**	**† Signetics (1107)**
	12μA	3μA	22	5	5K*		5,(-6, 5-±10)	**SE529**	**† Signetics (1107)**
5.0	6.0μA	1.5μA	55	15	—	—	±15,5	HA-4955	Harris
	150nA	25nA	200*	10	25K	2	±5 to ±15	μA734C	Fairchild
			1300*	36	200K*		2 to 36	TL331M	† TI
		50nA	1300*	36	200K*		2 to 36	TL331C	TI
	250nA	50nA	250*	15	15K		5-15, ±5-±15	ICL8001C	Intersil
	10μA	2μA	20	5	3K*	2	(-6, 5 to ±15)	LM361	National
	20μA	3μA	14*	5	3K*	4	±5	LM160	† National
								LM260	National
								LM360	National
	25μA	5μA	40	5	40K*	10	-3 to -12,12	LM306	National
								LM306	TI
			40*	5	40K*	10	-3 to -12,12	LM306	AMD
					1000	1	-6,12	MC1710C	Motorola
								LM710C	National
								μPC71	NEC America
								RC710	Raytheon
								SG710C	Silicon G
								μA710C	Signetics
								μA710C	TI
	35μA	5μA	48	5		10	±5	NE526	Signetics
								SE526	† Signetics
	75μA	10μA	40*	5	750		-6,12	TL710M	† TI
6.0	2μA	0.75μA	26	5	5K*		5,(-6, 5-±10)	**NE527**	**Signetics (1107)**
	20μA	5μA	22	5	5K*		5,(-6, 5-±10)	**NE529**	**Signetics (1107)**
	60μA	7.5μA	25*	5	5K*	2	±4.5 to ±6.5	μA760C	Fairchild
								μA760M	† Fairchild
	250nA	100nA	250	10	15K		±6 to ±18	AD351J	AD
								AD351K	AD
								AD351S	† AD
7.5	250nA	50nA	165*	30	200K*	5	5, 0 to ±15	LM311	TI
			200*	30	200K*	5	5, 0 to ±15	AD311	AD
								μA311C	Fairchild
								311	Intersil
								LM311	Motorola
								LM311	National
								μPC271	NEC America
								μPC311	NEC America
								SFC2311	NPC
								CA311	RCA
								LM311	Raytheon
								LM311	Signetics
								SG311	Silicon G
								μAF311	Fairchild
			250	30	200K*	5	5, 0 to ±15	LM311	AMD
	100μA	15μA	40*	5	700		-6,12	TL710C	TI
10.0	150pA	75pA	200*	30	200K*	5	5, 0 to ±15	LF311	AMD
								μAF311	Fairchild
								LF311	National
30.0	50μA	20μA	55	5	100	6	5	9915	OEI
—	100nA	—	50*	Vcc	—	—	1.7 to 6	M51201	Mitsubishi

† Military Temperature Range (−55° to 125°C)

* Typical Values

Bold face indicates additional data is provided on the page noted.

LINEAR–Comparators (Cont'd)

Offset Voltage mv (25°C)	Bias Current (25°C)	Offset Current (25°C)	Response Time ns	Max. Differential Voltage	Gain	Fan Out	Supply Voltage	Device	Source
Comparators-Dual									
1.5	15μA	1μA	40	5	1400	1	-6,12	RM711A	† Raytheon
2.0	100nA	25nA	1300*	36	50K		2 to 36	LM193A	† National
								LM193A	† Signetics
	250nA	50nA	1300*	36	50K		2 to 36	LM293A	National
								LM393A	National
								LM293A	Signetics
								LM393A	Signetics
	10μA	1μA	8	6			-5.2, 5	687AM	† AMD
			10	6			-5.2, 5	687M	† AMD
	15μA	3μA	80	5	12.5K		-6,12	TL514M	† TI
								TL820M	† TI
	20μA	3μA	30*	5	1250	1	-6,12	LM1514	† National
			40	5	40K*	10	-3 to -12,12	SN52506	† TI
			40*	5	1250		-6,12	MC1514	† Motorola
								RM1514	† Raytheon
3.0	100nA	10nA	200*	30	200K*	5	5, 0 to ±15	LH2111	† AMD
								LH2211	AMD
								LH2111	† Intersil
								LH2111	† National
								LH2211	National
								LH2111	Raytheon
								LH2211	Raytheon
								LH2111	† Signetics
								LH2211	Signetics
			250	30	200K*		5, 0 to ±15	1500M	† AMD
								1500L	AMD
	10μA	1μA	8	6			-5.2, 5	687AL	AMD
			10	6			-5.2, 5	687L	AMD
	45μA	7μA	40	5	40K*	10	-3 to -12, 12	TL506M	† TI
3.5	20μA	3μA	80	5	12.5K		-6,12	TL811M	† TI
		5μA	80	5	10K		-6,12	TL514C	TI
								TL820C	TI
	75μA	10μA	40*	5	700	1	-6,12	MC1711	† Motorola
					750	1	-6,12	μA711M	† Fairchild
								LM711	† National
								RM711	† Raytheon
								μA711	† Signetics
			60	5	750	1	-6,12	SG711	Silicon G
			80	5	750	1	-6,12	μA711M	† TI
4.0	500nA	75nA	80*	5	10K	2	5, 0 to ±15	LM119	† AMD
								LM219	AMD
								LM119	† National
								LM219	National
								LM119	† Signetics
								LM219	Signetics
5.0	100nA	25nA	1300*	36	50K		2 to 36	LM193	† National
								LM193	† Signetics
								LM193	† TI
	250nA	50nA	1300*	36	50K		2 to 36	LM293	National
								LM393	National
								LM293	Signetics
								LM393	Signetics
								LM293	TI
								LM393	TI
	600nA	150nA	5000	30			4.5 to 20	μPC379	NEC America
	25μA	5μA	30*	5	1000	1	-6,12	LM1414	National
			40*	5	1000		-6,12	MC1414	Motorola
								RC1414	Raytheon

(Continued)

† Military Temperature Range (−55° to 125°C) * Typical Values

LINEAR–Comparators (Cont'd)

Offset Voltage mv (25°C)	Bias Current (25°C)	Offset Current (25°C)	Response Time ns	Max. Differential Voltage	Gain	Fan Out	Supply Voltage	Device	Source
Comparators-Dual									**(Cont'd.)**
5.0									(Cont'd.)
	30μA	5μA	33*	5	10K		-6,12	TL811C	TI
	100μA	15μA	40*	5	700	1	-6,12	μA711C	Fairchild
								MC1711C	Motorola
								SFC2711	NPC
								LM711C	National
								RC711	Raytheon
								μA711C	Signetics
								SG711C	Silicon G
								μA711C	TI
6.0	30pA	20pA	200*	36	50K	1	4 to 44	CA3290B	RCA
6.5	40μA	7.5μA	28*	5	40K*	10	−3 to −12, 12	TL506C	TI
7.0	250nA	50nA	1500*	36	25K		2 to 36	LM2903	National
								LM2903	Signetics
								LM2903	TI
7.5	250nA	50nA	200*	30	200K*	5	5, 0 to ±15	LH2311	AMD
								LH2311	Intersil
								MC3411	Motorola
								LH2311	National
								LH2311	Raytheon
								LH2311	Signetics
			250	30	200K		5, 0 to ±15	1500C	AMD
	20μA	5μA	18	6	5K*	10	±5	NE521	Signetics
			25	6	5K*	10	±5	NE522	Signetics
	100μA	15μA	40*	5	700		-6,12	TL720C	TI
8.0	1μA	0.2μA	80*	5	8K	2	5, 0 to ±15	LM319	AMD
								μPC319	NEC America
								LM319	National
								LM319	Signetics
								TDA0319	Signetics
10	40pA	25pA	200*	36	50K	2	4 to 36	CA3290A	RCA
20	50pA	30pA	200*	36	25K	2	4 to 36	CA3290	RCA
Comparators-Quad									
0.8	100nA	25nA	1300	36	50K	2	2-36/±1-±18	CMP-04B	† PMI
								CMP-04F	PMI
2.0*	20μA	1μA*	55	5	1.2K*	10	±5	MC3430	Motorola
								MC3431	Motorola
			65	5	1.2K*	10	±5	MC3432	Motorola
								MC3433	Motorola
2.0	100nA	25nA	1300*	36	50K	2	2-36/±1-±18	LM139A	† AMD
								LM139A	† Intersil
								LM139A	† Motorola
								LM139A	† National
								PM139A	† PMI
								CA139A	† RCA
								SG139A	† Silicon G
					200K*	2	2-36/±1-±18	LM139A	Signetics
	250nA	50nA	1300*	36	50K	2	2-36/±1-±18	LM239A	AMD
								LM339A	AMD
								LM239A	Intersil
								LM339A	Intersil
								LM239A	Motorola
								LM339A	Motorola
								LM239A	National
								LM339A	National
								PM239A	PMI
								PM339A	PMI
								CA239A	RCA
								CA339A	RCA

(Continued)

† Military Temperature Range (−55° to 125°C) * Typical Values

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LINEAR–Comparators (Cont'd)

Offset Voltage mv (25°C)	Bias Current (25°C)	Offset Current (25°C)	Response Time ns	Max. Differential Voltage	Gain	Fan Out	Supply Voltage	Device	Source
Comparators-Quad									**(Cont'd.)**
2.0	250nA	50nA	1300*	36	50K	2	2-36/±1-±18		(Cont'd.)
								SG239A	Silicon G
								SG339A	Silicon G
					200K*	2	2-36/±1-±18	LM239A	Signetics
								LM339A	Signetics
2.5	5nA	0.5nA	10ms	36	25K		2 to 36	L161	Siliconix
3.0	6μA	1.5μA	35*	6	25k*	—	±15,5	**HA-4920**	**† Harris (1014)**
	75nA	25nA	130*	15	400K*		5 to ±15	**HA-4900**	**Harris (1012)**
5.0	100nA	25nA	1300*	36	200K*	2	2-36/±1-±18	LM139	† AMD
								μA139	† Fairchild
								LM139	† Intersil
								LM139	† Motorola
								LM139	† National
								PM139	† PMI
								LM139	† Raytheon
								CA139	† RCA
								LM139	† Signetics
								SG139	† Silicon G
								LM139	† TI
	250nA	50nA	1300*	36	200K*	2	2-36/±1-±18	LM239	AMD
								LM339	AMD
								μA239	Fairchild
								μA339	Fairchild
								LM239	Intersil
								LM339	Intersil
								LM239	Motorola
								LM339	Motorola
								LM239	National
								LM339	National
								μPC177	NEC America
								μPC339	NEC America
								PM239	PMI
								PM339	PMI
								LM239	Raytheon
								LM339	Raytheon
								CA239	RCA
								CA339	RCA
								LM239	Signetics
								LM339	Signetics
								SG239	Silicon G
								SG339	Silicon G
								LM239	TI
								LM339	TI
				15	200K*	1	3-15	MM54C909	† National
								MM74C909	National
	2 Operational Amplifiers, 2 Comparators								
	500nA	75nA	1300*	36	200K*		3-36	MC3505	† Motorola
6.0	8μA	2μA	35*	6	25k*	—	±15,5	**HA-4925**	**Harris (1014)**
7.0	250nA	50nA	1300*	36	50K	2	2-36/±1-±18	LM2901	Fairchild
								HA172901	Hitachi
								LM2901	Motorola
								LM2901	National
								μPC2901	NEC America
								LM2901	Raytheon
								LM2901	Signetics
								LM2901	TI
7.5	150nA	50nA	130*	15	400K*		5 to ±15	**HA-4905**	**† Harris (1012)**
	2 Operational Amplifiers, 2 Comparators								
9.0	10	500nA	1300*	36			3-36	MC3405	Motorola
20	500nA	3nA*	2000*	Vcc	2K	1	2 to 28	MC3302	Motorola
								μA3302C	Fairchild
								RV3302	Raytheon

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Values

LINEAR–Comparators (Cont'd)

Offset Voltage mv (25°C)	Bias Current (25°C)	Offset Current (25°C)	Response Time ns	Max. Differential Voltage	Gain	Fan Out	Supply Voltage	Device	Source
Comparators-Quad									**(Cont'd.)**
20	500nA	3nA*	2000*	Vcc	2K	1	2 to 28	MC3302 SG3302	(Cont'd.) Signetics Silicon G
		100nA	1300*	Vcc	2K	2	5 to ±15	LM3302	National
Comparators-Hex									
5	100nA	25nA	1300	±36	200K	4	2-36/±1-±18	TL336C	TI
	250nA	25nA	1300	±36	200K	4	3-36/±1-±18	TL336M	†TI

Special purpose comparators (Alarm Circuits; Analog-Digital Control Circuits; Comparators, Programmable; Level Detectors; Voltage Sensors, etc.) are listed under Linear-Other Devices.

† Military Temperature Range (−55° to 125°C)

* Typical Values

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LINEAR–Consumer Circuits

Function	Device	Source	Line
Consumer Circuits			
Alarm Circuits: See Linear-Other Devices, Alarms			
Amplifier, AGC/Squelch			
	LM170	†National	
	LM270	National	
	LM370	National	
Amplifier, with AGC, for recorders			
	HA1319	Hitachi	
	HA1361	Hitachi	
	TDA1002	Signetics	
Amplifier, Dual with AGC, for stereo recorders			10
	HA11122	Hitachi	
	M5130	Mitsubishi	
	M51301	Mitsubishi	
Amplifier, Dual, Tone, for stereo recorders			
	M5138	Mitsubishi	
Amplifier, Hearing Aid			
	CS263	Cherry	
	MP5003	Micro Power	
	MP5014	Micro Power	
	MP5014A	Micro Power	20
	μPC12	NEC America	
	OM200	Panasonic	
	CA3078	†RCA	
	OM200	Signetics	
	TAA370	Signetics	
Amplifier System (for tape recorders)			
	TA7223	Toshiba	
	TA7628	Toshiba	
AM IF Amplifier			
	LM172	†National	30
	LM272	National	
	LM372	National	
AM Receiver System			
	μA720	Fairchild	
	μA7330	Fairchild	
	HA1151	Hitachi	
	HA1197	Hitachi	
	HA1199	Hitachi	
	LM1820	National	
	LM1860	National	40
	AN259	Panasonic	
	CA3088	†RCA	
	CA3123	†RCA	
	TCA440	Siemens	
	TDA1046	Siemens	
	NE546	Signetics	
	TCA440	Signetics	
	TBA651	SGS	
	ULN-2249	Sprague	
	SN76635	TI	50
	TA7306	Toshiba	
	TA7615	Toshiba	
AM RF, IF, Detector, AGC			
	ZN414	Ferranti	
AM RF, Mixer, IF			
	μPC30	NEC America	
	μPC1021	NEC America	
AM Tuner (RF, IF, detector, AGC, meter driver)			
	LA1240	Sanyo	
AM/FM IF Amplifier			60
	μA757	†Fairchild	
	μPC27	NEC America	
	μPC577	NEC Ameriea	
	AN203	Panasonic	
	AN210	Panasonic	
	AN353	Panasonic	
		(Continued)	

Function	Device	Source	Line
Consumer Circuits (Cont'd.)			
AM/FM IF Amplifier (Cont'd.)			
	LA1201	Sanyo	
	TAA991	Siemens	
AM/FM IF and AF Amplifier			70
	TBA460	Siemens	
AM/FM Radio Frequency Display Driver and Clock			
	T1400	Toshiba	
AM/FM Receiver System			
	MCC401	Cherry	
	MCC402	Cherry	
	μA721	Fairchild	
	HA11120	Hitachi	
	HA11123	Hitachi	
	HA11211	Hitachi	80
	HA11251	Hitachi	
	HA11402	Hitachi	
	LM273	National	
	LM274	National	
	LM373	National	
	LM374	National	
	AN217	Panasonic	
	AN253	Panasonic	
	AN260	Panasonic	
	AN277	Panasonic	90
	AN366	Panasonic	
	SL437	Plessey	
	SL624C	Plessey	
	TDA1220	SGS	
	TDA1230	SGS	
	TBA570	Signetics	
	TBA700	Signetics	
	TDA1083	Sprague	
	TDA1090	Sprague	
	ULN-2204A	Sprague	100
	ULN-2242	Sprague	
	TBA570	Telefunken	
	TDA1083	Telefunken	
	TA7613	Toshiba	
	TA7614	Toshiba	
AM/FM Tuner, Radio Frequency Display and Clock			
	LC7250	Sanyo	
AM/FM/SSB Detector			
	SL624C	Plessey	
AM/FM/SW/Tuner, Radio Frequency Display and Clock			110
	MSL2316	OKI	
	MSM5523	OKI	
	MSM5524	OKI	
AM/SSB Detector			
	SL623C	Plessey	
	SL1623	Plessey	
	SL1625	Plessey	
AM/FM Tuner Control and Clock			
	AY3-8110	GI	120
	AY3-8112	GI	
	AY3-8114	GI	
	AY3-8115	GI	
	AY3-8116	GI	
	AY3-8117	GI	
	Stereomega	GI	
Appliance Timer			
	FCM7040	Fairchild	
	AY5-1230	GI	
	AY5-1231	GI	130
	AY5-1232	GI	
	AY5-1233	GI	
		(Continued)	

Function	Device	Source	Line
Consumer Circuits (Cont'd.)			
Appliance Timer (Cont'd.)			
	AY3-1250	GI	
	AY3-1251	GI	
	AY5-1260	GI	
	CD22017	RCA	
	UCN-4105	Sprague	
Audio Amplifier, with voice operated gain adjusting device			140
	SL1626	Plessey	
Audio Amplifier and Preamplifier, low power			
	TCA210	Signetics	
Audio Amplifier, low power			
	TBA915	Signetics	
Audio Controls (loudness, treble, bass)			
	TDA4290	Siemens	
Audio Controls, Stereo, dc operated			
	TCA730	Signetics	
	TCA740	Signetics	150
Audio Driver			
	MC3320	Motorola	
	MC3321	Motorola	
	LM391	National	
	NE540	Signetics	
	NE541	Signetics	
Audio Noise Reduction, Compander. See Linear-Telecommunications Circuits			
Audio, Noise Reduction, Dolby			
	μA7300	Fairchild	160
	HA11226	Hitachi	
	LM1101	National	
	LM1101A	National	
	NE545B	Signetics	
	NE645B	Signetics	
	NE646B	Signetics	
Audio, Power Amplifier, <5 Watts			
	μA7307	**Fairchild**	**(936)**
	TBA641	**Fairchild**	**(937)**
	TBA820	**Fairchild**	**(936)** 170
	HA1306	Hitachi	
	HA1325	Hitachi	
	HA1329	Hitachi	
	HA1367	Hitachi	
	M5115	Mitsubishi	
	M5115R	Mitsubishi	
	M5118	Mitsubishi	
	M5155	Mitsubishi	
	M51501	Mitsubishi	
	M51182	Mitsubishi	180
	M51512	Mitsubishi	
	M51513	Mitsubishi	
	MC1306	Motorola	
	MC1384	Motorola	
	MC1454	Motorola	
	MC1554	†Motorola	
	MC3360	Motorola	
	LM380	National	
	LM386	National	
	LM388	National	190
	LM389	National	
	LM390	National	
	μPC41	NEC America	
	μPC1025	NEC America	
	AN214	Panasonic	
	AN215	Panasonic	
	AN252	Panasonic	
	AN374	Panasonic	
		(Continued)	

† Military Temperature Range (−55° to 125°C)

* Typical Values

LINEAR–Consumer Circuits (Cont'd)

Consumer Circuits (Cont'd.)

Function	Device	Source	Line
Audio, Power Amplifier, <5 Watts (Cont'd.)			
	SL414	Plessey	
	SL424	Plessey	
	CA3020	†RCA	
	CA3094	†RCA	
	LA4030	Sanyo	
	LA4031	Sanyo	
	LA4032	Sanyo	
	LA4050	Sanyo	
	LA4051	Sanyo	10
	LA4100	Sanyo	
	LA4101	Sanyo	
	LA4102	Sanyo	
	LA4110	Sanyo	
	LA4112	Sanyo	
	LA4200	Sanyo	
	LA4201	Sanyo	
	LA4220	Sanyo	
	LA4430	Sanyo	
	TAA611	SGS	20
	TBA641	SGS	
	TBA820	SGS	
	TCA830	SGS	
	NE540	Signetics	
	SE540	Signetics	
	TCA160	Signetics	
	TCA760	Signetics	
	ULN-2280	Sprague	
	ULN-2281	Sprague	
	ULN-2283	Sprague	30
	TBA0800	Telefunken	
	TCA830	Telefunken	
	SN76000	TI	
	SN76011	TI	
	SN76021	TI	
	SN76024	TI	
	TA7066	Toshiba	
	TA7140	Toshiba	
	TA7200	Toshiba	
	TA7207	Toshiba	40
	TA7208	Toshiba	
	TA7209	Toshiba	
	TA7211	Toshiba	
	TA7212	Toshiba	
	TA7220	Toshiba	
	TA7204	Toshiba	
Audio, Power Amplifier, 5-10 Watts			
	μA783	**Fairchild (936)**	
	μA706	**Fairchild (937)**	
	TBA800	**Fairchild (937)**	50
	TBA810	**Fairchild (936)**	
	TDA2002	**Fairchild (936)**	
	TDA2002A	**Fairchild (936)**	
	HA1308	Hitachi	
	HA1317	Hitachi	
	HA1322	Hitachi	
	HA1338	Hitachi	
	HA1339A	Hitachi	
	HA1342A	Hitachi	
	HA1366	Hitachi	60
	HA1368	Hitachi	
	HA1371	Hitachi	
	HA1372	Hitachi	
	HA1379	Hitachi	
	HA1380	Hitachi	
	HA1382	Hitachi	
	HA1383	Hitachi	
	HA1390	Hitachi	
	TBA800	Hitachi	

(Continued)

Consumer Circuits (Cont'd.)

Function	Device	Source	Line
Audio, Power Amplifier, 5-10 Watts (Cont'd.)			70
	TBA810	Hitachi	
	M5112	Mitsubishi	
	TDA2002	Motorola	
	TDA2002A	Motorola	
	LM383	National	
	LM383A	National	
	LM384	National	
	TDA2002	National	
	TDA2002A	National	
	μPC571	NEC America	80
	μPC578	NEC America	
	μPC1020	NEC America	
	μPC1155	NEC America	
	μPC1156	NEC America	
	AN272	Panasonic	
	AN315	Panasonic	
	AN7150	Panasonic	
	AN7151	Panasonic	
	SL415	Plessey	
	SL425	Plessey	90
	TBA800	Plessey	
	CA810	RCA	
	CA810M	RCA	
	CA810A	RCA	
	CA810AM	RCA	
	CA2002	RCA	
	CA3131	RCA	
	CA3132	RCA	
	SI1010	Sanken	
	LA4230	Sanyo	100
	LA4250	Sanyo	
	LA4420	Sanyo	
	STK011	Sanyo	
	TDA1037	Siemens	
	TBA800	SGS	
	TBA810	SGS	
	TCA940E	SGS	
	TDA2002	SGS	
	TDA2002A	SGS	
	TDA2870	Siemens	110
	TDA1004A	Signetics	
	TDA1010	Signetics	
	TDA2611	Signetics	
	TDA2002	Sprague	
	ULN-3701	Sprague	
	TBA810	Telefunken	
	TCA940	Telefunken	
	TDA2002	Telefunken	
	TDA2002A	Telefunken	
	SN76005	TI	120
	TA7201	Toshiba	
	TA7202	Toshiba	
	TA7205A	Toshiba	
	TA7213	Toshiba	
	TA7216	Toshiba	
	TA7217	Toshiba	
	TA7218	Toshiba	
	TA7222	Toshiba	
	TA7222A	Toshiba	
	TA7228	Toshiba	130
Audio Power Amplifier, >10 Watts			
	HA1350	Hitachi	
	HA1370	Hitachi	
	HA1388	Hitachi	
	LM391	National	
	ESM532	NPC	
	TCA940	SGS	
	SI1020	Sanken	

(Continued)

Consumer Circuits (Cont'd.)

Function	Device	Source	Line
Audio Power Amplifier, >10 Watts (Cont'd.)			140
	SI1030	Sanken	
	SI1050	Sanken	
	STK015	Sanyo	
	STK016	Sanyo	
	STK020	Sanyo	
	STK022	Sanyo	
	STK024	Sanyo	
	STK025G	Sanyo	
	STK031	Sanyo	
	STK032	Sanyo	
	STK035	Sanyo	150
	STK036	Sanyo	
	STK050	Sanyo	
	STK055	Sanyo	
	STK057	Sanyo	
	STK058	Sanyo	
	STK060	Sanyo	
	STK062	Sanyo	
	STK070	Sanyo	
	STK075	Sanyo	
	STK077	Sanyo	160
	STK078	Sanyo	
	STK080	Sanyo	
	STK082	Sanyo	
	STK084	Sanyo	
	STK086	Sanyo	
	STK0030	Sanyo	
	STK0035	Sanyo	
	STK0040	Sanyo	
	STK0045	Sanyo	
	STK0065	Sanyo	170
	TDA2010	SGS	
	TDA2020	SGS	
	TDA2030	SGS	
	TA7210	Toshiba	
Audio Power Amplifier, Dual, <5 Watts			
	HA1374	Hitachi	
	LM377	National	
	LM378	National	
	LM1877	National	
	AN274	Panasonic	180
	AN313	Panasonic	
	ULN-2274	Sprague	
	ULN-2278	Sprague	
	TA7203	Toshiba	
	TA7214	Toshiba	
	TA7215	Toshiba	
Audio Power Amplifier, Dual, 5-10 Watts			
	DA-101	Delco	
	HA1377	Hitachi	
	M51515	Mitsubishi	190
	LM379	National	
	STK433	Sanyo	
	STK435	Sanyo	
	TDA1009	Signetics	
	TA7227	Toshiba	
Audio Power Amplifier, Dual, >10 Watts			
	STK040A	Sanyo	
	STK041	Sanyo	
	STK043	Sanyo	
	STK437	Sanyo	200
	STK439	Sanyo	
	STK441	Sanyo	
Audio Preamplifier			
	ZN459C	Ferranti	
	ZN459CP	Ferranti	
	ZN459T	†Ferranti	

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Values

Bold face indicates additional data is provided on the page noted.

LINEAR–Consumer Circuits (Cont'd)

Function	Device	Source	Line
Consumer Circuits (Cont'd.)			
Audio Preamplifier (Cont'd.)			
	HA1406	Hitachi	
	HA1457	Hitachi	
	HA12008	Hitachi	
	ML120	Mitsubishi	
	M5212	Mitsubishi	
	M5213	Mitsubishi	
	LM3080	National	
	LM3080A	National	
	μPC566	NEC America	10
	μPC573	NEC America	
	μPC592	NEC America	
	μPC1023	NEC America	
	μPC1024	NEC America	
	μPC1032	NEC America	
	AN127	Panasonic	
	AN136	Panasonic	
	AN262	Panasonic	
	AN270	Panasonic	
	SL561	Plessey	20
	CA3080	RCA	
	CA3080A	†RCA	
	LA3110	Sanyo	
	LA3120	Sanyo	
	LA3130	Sanyo	
	LA3150	Sanyo	
	TAA263	Signetics	
	TAA310A	Signetics	
	TAA1002	Signetics	
	TA7063	Toshiba	30
	TA7120	Toshiba	
	TA7122A	Toshiba	
	TA7129	Toshiba	
	TA7136A	Toshiba	
Audio, Preamplifier with ALC			
	LA3201	Sanyo	
	LA3210	Sanyo	
	TA7307	Toshiba	
Audio, Preamplifier, Dual			
	XR4739	Exar	40
	XR4739M	†Exar	
	μA739	Fairchild	
	μA381	Fairchild	
	μA749	†Fairchild	
	HA1451	Hitachi	
	HA1452	Hitachi	
	HA1452W	Hitachi	
	HA12012	Hitachi	
	M5152	Mitsubishi	
	M51521	Mitsubishi	50
	LM1303	National	
	LM381	National	
	LM382	National	
	LM387	National	
	AN215	Panasonic	
	AN264	Panasonic	
	AN360	Panasonic	
	AN370	Panasonic	
	CA3048	RCA	
	CA3052	RCA	60
	LA3115	Sanyo	
	LA3122	Sanyo	
	LA3133	Sanyo	
	LA3155	Sanyo	
	LA3160	Sanyo	
	NE542	Signetics	
	LM381	Signetics	
	LM382	Signetics	
	LM387	Signetics	

(Continued)

Function	Device	Source	Line
Consumer Circuits (Cont'd.)			
Audio, Preamplifier, Dual (Cont'd.)			70
	PA239	Signetics	
	TCA490	Signetics	
	ULN-2231	Sprague	
	SN76130	TI	
	SN76131	TI	
	SN76149	TI	
	TA7108	Toshiba	
	TA7312	Toshiba	
Audio Preamplifier, Quad			
	XR4212	Exar	80
	XR4212M	†Exar	
Automotive Adaptive Sense Amplifier (one-shot with peak detector adjusted shut-off threshold)			
	LM1815	National	
Automotive, Ignition Circuit			
	MC3333	Motorola	
Automotive, Lamp Monitor			
	ULN-2401	Sprague	
Automotive, Low Coolant Detector			
	ULN-2429	Sprague	90
Automotive, Speed Control Processor			
	MC14460	Motorola	
Automotive, Tachometer Circuit. See Tachometer Circuit below.			
Automotive, Timer			
	ULN-2430	Sprague	
Automotive, Traffic Information Broadcast Decoders			
	S280	Siemens	
	S281	Siemens	
	S551	Siemens	100
	S552	Siemens	
Automotive, Voltage Regulator			
	MC3325	Motorola	
	MC3326	Motorola	
Calculator			
	C/CF583	GI	
	C/CF585	GI	
	C/CF589	GI	
	C/CF593	GI	
	C/CF594	GI	110
	C/CF595	GI	
	C/CF596	GI	
	C/CF598	GI	
	C/CF599	GI	
	C683D	GI	
	C/CF683	GI	
	C685D	GI	
	C/CF685	GI	
	CF687	GI	
	C687D	GI	120
	CF689	GI	
	CF689/HV	GI	
	C689D	GI	
	C1683D	GI	
	C1685D	GI	
	C1687D	GI	
	C1689D	GI	
	HD37320	Hitachi	
	HD37330	Hitachi	
	HD37350	Hitachi	130
	HD38401	Hitachi	
	HD38411	Hitachi	
	HD43300	Hitachi	
	HD43311	Hitachi	

(Continued)

Function	Device	Source	Line
Consumer Circuits (Cont'd.)			
Calculator (Cont'd.)			
	HD43330	Hitachi	
	HD43335	Hitachi	
	HD43337	Hitachi	
	MPS7529-001	MOS	
	MPS7529-007	MOS	140
	MPS7529-009	MOS	
	MPS7529-012	MOS	
	MPS7529-013	MOS	
	MPS7529-014	MOS	
	MPS7529-017	MOS	
	MPS7529-022	MOS	
	MPS7529-103	MOS	
	MPS7529-104	MOS	
	MPS7529-201	MOS	
	MPS7529-216	MOS	150
	MPS7529-305	MOS	
	MPS7530-001	MOS	
	MPS7530-010	MOS	
	MPS7530-201	MOS	
	MPS7530-217	MOS	
	MM5725	National	
	MM5734	National	
	MM5736	National	
	MM5737	National	
	MM5738	National	160
	MM5739	National	
	MM5758	National	
	MM5760	National	
	MM5762	National	
	MM5763	National	
	MM5764	National	
	MM5765	National	
	MM57123	National	
	MM5766	National	
	MM5767	National	170
	MM5777	National	
	MM5780	National	
	MM5791	National	
	MM5794	National	
	MM5795	National	
	MM57103	National	
	MM57104	National	
	MM57109	National	
	μPD276	NEC America	
	μPD277	NEC America	180
	μPD278	NEC America	
	μPD284	NEC America	
	μPD286	NEC America	
	μPD299	NEC America	
	μPD940	NEC America	
	μPD941	NEC America	
	μPD943	NEC America	
	μPD946	NEC America	
	μPD947	NEC America	
	μPD950	NEC America	190
	μPD951	NEC America	
	μPD952	NEC America	
	μPD1201	NEC America	
	μPD1801	NEC America	
	MN5530	Panasonic	
	MN5540	Panasonic	
	MN5550	Panasonic	
	MN5556	Panasonic	
	MN5701	Panasonic	
	MN5710	Panasonic	200
	MN5750	Panasonic	
	MN5752	Panasonic	
	TMS1018	TI	

† Military Temperature Range (−55° to 125°C)

* Typical Values

LINEAR–Consumer Circuits (Cont'd)

Consumer Circuits (Cont'd.)

Function	Device	Source	Line
Calculator, Display Interface, (use with printer)			
	C719	GI	
Calculator, Printing			
	EA7251	EA	
	EA7261	EA	
	C717X	GI	
	C718	GI	
	C1720	GI	
	HD38510	Hitachi	
	HD38513	Hitachi	
	HD38516	Hitachi	10
	HD38530	Hitachi	
	HD38533	Hitachi	
	HD38546	Hitachi	
	HD38548	Hitachi	
	HD38550	Hitachi	
	HD38560	Hitachi	
	HD38570	Hitachi	
	HD38580	Hitachi	
	HD38585	Hitachi	
	μPD299	NEC America	20
	1022	SMC	
Camera, Exposure Control			
	CS100	Cherry	
	CS102	Cherry	
	CS122	Cherry	
	CS127	Cherry	
	CS129	Cherry	
	CS130	Cherry	
	CS131	Cherry	
	CS132	Cherry	30
	CS137	Cherry	
	CS460	Cherry	
	CS461	Cherry	
	CS462	Cherry	
	CS463	Cherry	
	CS464	Cherry	
	CS480	Cherry	
	CS481	Cherry	
	CS482	Cherry	
	CS483	Cherry	40
	CS484	Cherry	
	CS485	Cherry	
	CS486	Cherry	
	CS487	Cherry	
	CS488	Cherry	
	CS489	Cherry	
	CS580	Cherry	
	μPC558	NEC America	
	μPC589	NEC America	
Camera, Strobe Light Controller			50
	CS139	Cherry	
Citizens Band Programmer, for PLL			
	HD42851	Hitachi	
	HD42853	Hitachi	
	MM57190	National	
	LC7120	Sanyo	
	LC7123	Sanyo	
	TC9116	Toshiba	
	TC9117	Toshiba	
Citizens Band Remote Controller and Display Driver			60
	FCB8010	Fairchild	
	HD42854	Hitachi	
	HD42855	Hitachi	
	MN6080	Panasonic	
	LC7181	Sanyo	
	LC7190	Sanyo	
	LC7191	Sanyo	

Consumer Circuits (Cont'd.)

Function	Device	Source	Line
CB Transceiver Receiver			
	TA7618	Toshiba	
	TMS1022	TI	70
Citizen Band, See Linear-Phase Locked Loops/Synthesizers			
Clock (See also Digital-CMOS Oscillators/Dividers)			
See also Clock, Alarm Clock; Clock, Alarm Clock Radio			
	S2709	AMI	
	S1856	AMI	
	AY5-1200A	GI	
	AY5-1202A	GI	
	AY5-1203A	GI	80
	AY5-1204A	GI	
	AY5-1224A	GI	
	HD44010	Hitachi	
	CK3500	GI	
	CK3500F	GI	
	ICM7028	Intersil	
	ICM7038A	Intersil	
	ICM7038B	Intersil	
	ICM7051	Intersil	
	M54860	Mitsubishi	90
	C1200	**LSI Comp** **(494)**	
	MC14440	Motorola	
	MM5218	National	
	MM5309	National	
	MM5311	National	
	MM5312	National	
	MM5313	National	
	MM5314	National	
	MM5315	National	
	MM5375	National	100
	MM5376	National	
	MM5377	National	
	MM5378	National	
	MM5379	National	
	MM53110	National	
	μPD811	NEC America	
	μPD815	NEC America	
	μPD816	NEC America	
	MSM5509	OKI	
	MSM5528	OKI	110
	MSM5529	OKI	
	MSM5929	OKI	
	MN6070	Panasonic	
	CD22011	RCA	
	CD22012	RCA	
	CD22014	RCA	
	CD22015	RCA	
	SAJ341	Siemens	
	SAA1028	Signetics	
	SAJ250	Signetics	120
	UCN-4103	Sprague	
	UCN-4104	Sprague	
	UCN-4112	Sprague	
	UCN-4116	Sprague	
Clock, Alarm Clock			
	S2622	AMI	
	EA2318	EA	
	EA5316	EA	
	EA7316	EA	
	EA7317	EA	130
	3817	Fairchild	
	HD38980	Hitachi	
	HD38988	Hitachi	
	HD38991A	Hitachi	
	HD38992A	Hitachi	
	HD42022	Hitachi	

(Continued)

Consumer Circuits (Cont'd.)

Function	Device	Source	Line
Clock, Alarm Clock		(Cont'd.)	
	HD43115	Hitachi	
	HD43870	Hitachi	
	HD43890	Hitachi	140
	451	Hughes	
	ICM1115	Intersil	
	ICM1115A	Intersil	
	ICM1115B	Intersil	
	ICM7038	Intersil	
	ICM7049	Intersil	
	ICM7050	Intersil	
	M58412	Mitsubishi	
	M58413	Mitsubishi	
	MK50250	Mostek	150
	MK50253	Mostek	
	MK50254	Mostek	
	MM5316	National	
	MM5370	National	
	MM5371	National	
	MM5375	National	
	MM5376	National	
	MM5385	National	
	MM5386	National	
	MM5387	National	160
	MM5396	National	
	MM5397	National	
	MM53108	National	
	MM5402	National	
	MM5405	National	
	MM58143	National	
	MM58144	National	
	μPD832	NEC America	
	μPD833	NEC America	
	μPD5388	NEC America	170
	MN6052	Panasonic	
	MN6053	Panasonic	
	MN6091	Panasonic	
	MN6092	Panasonic	
	SAA1114	Signetics	
	UCN-4111	Sprague	
Clock, Alarm Clock Radio			
	S1998A	AMI	
	S1998C	AMI	
	S1988E	AMI	180
	S1988F	AMI	
	3817	Fairchild	
	CK3300	GI	
	MM5282	National	
	MM5283	National	
	MM5284	National	
	MSM5523	OKI	
	MSM5524	OKI	
Coinbox Circuit			
	AY1-8622	GI	190
	LM8091	Sanyo	
	LM8092	Sanyo	
FM Detector. See Linear-Phase Locked Loop Circuits and IF Amplifier/Detector below.			
FM IF Amplifier			
	μA753	Fairchild	
	μA3076	Fairchild	
	HA1201	Hitachi	
	HA1211	Hitachi	
	MC1350	Motorola	200
	MC1355	Motorola	
	MC3310	Motorola	
	AN278	Panasonic	
	AN377	Panasonic	

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Values

Bold face indicates additional data is provided on the page noted.

LINEAR–Consumer Circuits (Cont'd)

Consumer Circuits (Cont'd.)

Function	Device	Source	Line
FM IF Amplifier (Cont'd.)			
	CA3002	†RCA	
	CA3005	†RCA	
	CA3006	†RCA	
	CA3012	†RCA	
	CA3028	†RCA	
	CA3076	†RCA	
	LA1111	Sanyo	
	LA1222	Sanyo	
	ULN2209	Signetics	10
	ULN-2209	Sprague	
	SN76676	TI	
	SN76678	TI	
	TA7302	Toshiba	
	TA7303	Toshiba	
FM IF Amplifier/Detector			
	μA2136	Fairchild	
	μA3065	Fairchild	
	μA3075	Fairchild	
	μA3089	Fairchild	20
	μA3089M	†Fairchild	
	HA1137	Hitachi	
	HA11225	Hitachi	
	HA12401	Hitachi	
	HA12411	Hitachi	
	M5143	Mitsubishi	
	M5144	Mitsubishi	
	M51172	Mitsubishi	
	M51177	Mitsubishi	
	MC1351	Motorola	30
	MC1356	Motorola	
	LM1351	National	
	LM1841	National	
	LM2111	National	
	LM2113	National	
	LM273	National	
	LM274	National	
	LM373	National	
	LM374	National	
	LM3065	National	40
	LM3075	National	
	LM3089	National	
	TBA120	National	
	μPC1004	NEC America	
	μPC1028	NEC America	
	TAA661	Plessey	
	TBA120	Plessey	
	TBA750	Plessey	
	CA2111A	†RCA	
	CA3013	RCA	50
	CA3014	†RCA	
	CA3041	RCA	
	CA3042	RCA	
	CA3043	†RCA	
	CA3065	RCA	
	CA3075	†RCA	
	CA3089	†RCA	
	CA3189	RCA	
	LA1150	Sanyo	
	LA1230	Sanyo	60
	TCA3089	SGS	
	TDA1200	SGS	
	TDA1230	SGS	
	S041	Siemens	
	TBA120	Siemens	
	TDA1047	Siemens	
	CA3089	Signetics	
	CA3089D2	Signetics	
	TBA120S	Signetics	

(Continued)

Consumer Circuits (Cont'd.)

Function	Device	Source	Line
FM IF Amplifier/Detector (Cont'd.)			70
	TBA120U	Signetics	
	TBA750	Signetics	
	TCA420	Signetics	
	TCA770	Signetics	
	ULN2111	Signetics	
	ULN2211	Signetics	
	TCA3089	Sprague	
	TDA1200	Sprague	
	ULN-2111	Sprague	
	ULN-2136	Sprague	80
	ULN-2287	Sprague	
	ULN-2289	Sprague	
	TBA120	Telefunken	
	SN76642	TI	
	SN76643	TI	
	SN76669	TI	
	SN76675	TI	
	SN76689	TI	
	TA7321	Toshiba	
FM, IF Amplifier, PLL, Squelch, narrow band			90
	SL660	Plessey	
	SL662	Plessey	
	SL664	Plessey	
	SL665	Plessey	
FM Muting/Tuning Point System			
	HA1149	Hitachi	
FM Noise Canceller			
	HA11219	Hitachi	
	HA12410	Hitachi	
	M51011	Mitsubishi	100
	AN101	Panasonic	
	LA2100	Sanyo	
FM Receiver System with squelch and scan control			
	MC3357	Motorola	
FM, RF/IF Amplifier			
	AN219	Panasonic	
	CA3127	†RCA	
	TCA770	Signetics	
FM Stereo Decoder			
	XR1310	Exar	110
	μA732	Fairchild	
	μA758	Fairchild	
	μA767	Fairchild	
	μA1310	Fairchild	
	HA1115	Hitachi	
	HA1120	Hitachi	
	HA1142	Hitachi	
	HA1156	Hitachi	
	HA1173	Hitachi	
	HA1196	Hitachi	120
	HA11223	Hitachi	
	HA11227	Hitachi	
	M5132	Mitsubishi	
	M5133	Mitsubishi	
	M5153	Mitsubishi	
	MC1309	Motorola	
	MC1310	Motorola	
	LM1304	National	
	LM1305	National	
	LM1307	National	130
	LM1310	National	
	LM1800	National	
	LM1810	National	
	μPC554	NEC America	
	μPC585	NEC America	
	μPC587	NEC America	

(Continued)

Consumer Circuits (Cont'd.)

Function	Device	Source	Line
FM Stereo Decoder (Cont'd.)			
	μPC1026	NEC America	
	AN211	Panasonic	
	AN271	Panasonic	140
	AN362	Panasonic	
	AN363	Panasonic	
	SL758	Plessey	
	SL1310	Plessey	
	CA758	RCA	
	CA1310	RCA	
	CA3090A	†RCA	
	LA3300	Sanyo	
	LA3301	Sanyo	
	LA3350	Sanyo	150
	TBA450	Siemens	
	μA758	Signetics	
	TCA290	Signetics	
	TDA1005	Signetics	
	ULN-2110	Sprague	
	ULN-2244	Sprague	
	ULN-2245	Sprague	
	SN76104	TI	
	SN76105	TI	
	SN76110	TI	160
	SN76111	TI	
	SN76113	TI	
	SN76115	TI	
	SN76116	TI	
	TA7155	Toshiba	
	TA7156	Toshiba	
	TA7157	Toshiba	
	TA7323	Toshiba	
	TA7604	Toshiba	
	TA7624	Toshiba	170
FM Tuner			
	TDA1062	Telefunken	
Four Channel Sound			
	μA1312	Fairchild	
	HA1327	Hitachi	
	HA1328	Hitachi	
	HA1333	Hitachi	
	HA1334	Hitachi	
	MC1312	Motorola	
	MC1314	Motorola	180
	MC1315	Motorola	
	LM1852	National	
	LM1853	National	
	QSI5022	Panasonic	
	CG392	Signetics	
	CG477	Signetics	
Games, T.V.			
	AY3-8500	GI	
	AY3-8500-1	GI	
	AY3-8515	GI	190
	AY3-8550	GI	
	AY3-8550-1	GI	
	AY3-8603	GI	
	AY3-8603-1	GI	
	AY3-8604	GI	
	AY3-8605	GI	
	AY3-8605-1	GI	
	AY3-8606	GI	
	AY3-8606-1	GI	
	AY3-8607-1	GI	200
	AY3-8610	GI	
	AY3-8610-1	GI	
	AY3-8615	GI	
	AY3-8700-1	GI	

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Values

LINEAR–Consumer Circuits (Cont'd)

Function	Device	Source	Line
Consumer Circuits (Cont'd.)			
Games, T.V. (Cont'd.)			
	AY3-8710	GI	
	AY3-8760	GI	
	AY3-8765	GI	
	AY3-8900	GI	
	AY3-8900-1	GI	
	AY3-8950	GI	
	AY3-8950-1	GI	
	RA3-9600	GI	
	RO3-9500	GI	10
	RO3-9501	GI	
	RO3-9503	GI	
	MPS7600-001	MOS	
	MPS7600-002	MOS	
	MPS7600-004	MOS	
	MPS7600-005	MOS	
	MPS7601-001	MOS	
	MPS7601-002	MOS	
	MPS7601-004	MOS	
	MPS7601-005	MOS	20
	LM1889	National	
	MM4789	National	
	MM5789	National	
	MM53104	National	
	MM57100	National	
	MM57105	National	
	MM57106	National	
	MM57186	National	
	VES	Nortec	
	SN76400	TI	30
	SN76401	TI	
	SN76402	TI	
	SN76423	TI	
	SN76424	TI	
	SN76425	TI	
	SN76426	TI	
	SN76427	TI	
	SN76428	TI	
	SN76429	TI	
	SN76430	TI	40
	SN76431	TI	
	SN76442	TI	
	SN76443	TI	
	SN76445	TI	
	SN76450	TI	
	SN76460	TI	
	SN76462	TI	
Games, T.V.; Audio Synthesizer, 5-Bit D/A with driver for small speaker			
	ICM7219	Intersil	50
Games, T.V. Color Converter (converts game chip B/W outputs to Color)			
	AY3-8515	GI	
	AY3-8615	GI	
Games, T.,V., Color Processor (generates single composite color signal from game chip input)			
	AY3-8915	GI	
Games, T.V.; Sound Generator			
	AY3-8910	GI	
	AY3-8912	GI	60
	SN76477	TI	
Games, T.V., Programmable Video Interface			
	2636	**Signetics (2301)**	
Games, T.V.; T.V. Game to Cassette Deck Interface			
	AY3-8920	GI	

Function	Device	Source	Line
Consumer Circuits (Cont'd.)			
Games, T.V., Video Display Generator			
	S68047	**AMI (1830)**	
	MC6847	**Motorola (1979)**	
Ground Fault Interrupter			
	µA7390	Fairchild	70
	MC3426	Motorola	
	LM1850	National	
Light Dimmer, for touch sensor to control SCR			
	S556	Siemens	
Microwave Oven Controller			
	AY5-1260	GI	
	TMS1117	TI	
Motor Speed Regulator			
	CS140	Cherry	
	CS175	Cherry	80
	µA7391	Fairchild	
	µA7392	Fairchild	
	HA1373	Hitachi	
	M51970	Mitsubishi	
	LM1815	National	
	SL440	Plessey	
	TCA900	SGS	
	TCA910	SGS	
	TCA955	Siemens	
	TDA1151	SGS	90
Motor Speed Regulator, PLL			
	TM4503	Toshiba	
Motor Speed Regulator, PLL, for record players, VTR			
	MSM5810	OKI	
	MSM5811	OKI	
	MSM5814	OKI	
	MSM5815	OKI	
	MSM5816	OKI	
Motor Speed Regulator, with erase oscillator, for tape recorders			100
	TDA1003A	Signetics	
Motor Speed Regulator, with tape end indicator, for tape recorders			
	TDA1006	Signetics	
Motor, Stepping Motor Drive.			
	SAA1027	Signetics	
Music, Electronic Piano Keyboard Interface			
	AY1-1320	GI	
Music, Voltage Controlled Oscillator			
	SSM2030	**SSM (564)**	110
Music, Voltage Controlled Transient Generator			
	SSM2050	**SSM (565)**	
Music, See Organ Circuits			
Organ, Arpeggio, Chord and Bass Accompaniment Generator			
	M251	SGS	
Organ, Chord Generator			
	AY5-1317A	GI	
	S163	Siemens	
Organ, Delay Circuit, See also Analog Shift Registers under Linear-Other Devices.			120
	S10110	AMI	
	S10111	AMI	
	SAD512	Reticon	
	SAD1024A	Reticon	
Organ, Electronic Attenuator			
	XR13600	**Exar (933)**	
	MC3340	Motorola	
		(Continued)	

Function	Device	Source	Line
Consumer Circuits (Cont'd.)			
Organ, Electronic Attenuator (Cont'd.)			
	CA3080	RCA	130
	CA3080A	†RCA	
Organ, Frequency Divider, 4 Stage			
	AY1-5051	GI	
Organ, Frequency Divider, 5 Stage			
	AY1-6721/5	GI	
Organ, Frequency Divider, 6 Stage			
	S10129	AMI	
	S10130	AMI	
	S10131	AMI	
	EA5823	EA	140
	EA5824	EA	
	AY1-6721/6	GI	
	HD3111	Hitachi	
	MM5554	National	
	MM5823	National	
	MM5824	National	
	LM3216	Sanyo	
Organ, Frenquency Divider, 6 Stage, with gating, five outputs			
	TDA1008	Signetics	150
Organ, Frequency Divider, 7 Stage			
	S2193	AMI	
	F4727	Fairchild	
	EA5821	EA	
	AY1-1007B	GI	
	AY1-5050	GI	
	MC1302	Motorola	
	HBF4727	SGS	
	HBF4737	SGS	
	SAJ410	Siemens	160
	SAJ110	Signetics	
Organ, Frequency Divider, 8-stage, with staircase generator			
	SAJ205	Siemens	
Organ, Frequency Generator. See also Organ, Top Octave Generator			
	M087	SGS	
Organ, Gate for Key Contact			
	H629	SGS	
Organ, Key Divider			170
	S10430	AMI	
Organ, Latch Pedal Sustain			
	M147	SGS	
Organ, Noise Generator			
	S2688	AMI	
	MM5837	National	
Organ, Priority Latching Network			
	AY1-1313	GI	
Organ, Rhythm Circuit			
	S2566	AMI	180
	S2567	AMI	
	S8890	AMI	
	S9660	AMI	
	AY5-1315	GI	
	MCM6550	Motorola	
	MM5871	National	
	LM8271	Sanyo	
	LM8272	Sanyo	
	LM8371	Sanyo	
	LM8372	Sanyo	190
	LM8471	Sanyo	
	LM8972	Sanyo	
		(Continued)	

† Military Temperature Range (−55° to 125°C)

* Typical Values

Bold face indicates additional data is provided on the page noted.

LINEAR–Consumer Circuits (Cont'd)

Function	Device	Source	Line
Consumer Circuits (Cont'd.)			
Organ, Rhythm Circuit (Cont'd.)			
	M252	SGS	
	M253	SGS	
	M254	SGS	
	M255	SGS	
Organ, Serial to Parallel Converter, 33-Bits			
	MM5559	National	
Organ, Top Octave Generator			
	S50240	AMI	
	S50241	AMI	10
	S50242	AMI	
	S50243	AMI	
	S50244	AMI	
	S50245	AMI	
	EA5240	EA	
	EA5241	EA	
	EA5242	EA	
	AY1-0212	GI	
	AY1-0212A	GI	
	AY3-0214	GI	20
	AY3-0215	GI	
	AY3-0216	GI	
	MK50240	Mostek	
	MK50241	Mostek	
	MK50242	Mostek	
	MM5555	National	
	MM5556	National	
	MM5832	National	
	MM5833	National	
	MM5891	National	30
	NC1183	Nitron	
	NC1184	Nitron	
	LM8071	Sanyo	
Organ, Voltage Controlled Filter, Four Stage			
	SSM2040	**SSM** **(565)**	
Peak Power Meter Driver, Dual (for hi-fi stereo)			
	TA7318	Toshiba	
Plunger Driver			
	TA7226	Toshiba	
Protector Circuit (overcurrent detection for OCL and speaker)			40
	TA7317	Toshiba	
Radio Receiver, Noise Inverter for car radios			
	TDA1068	Telefunken	
Radio, Receiver, Counter/Display and Clock			
	AY5-8100	GI	
	AY5-8102	GI	
Remote Control Transmitters, Receivers. See Citizen Band and T.V. Remote Control			
RF Amplifier/Mixer			50
	CA3005	†RCA	
	CA3006	†RCA	
	CA3049	†RCA	
	CA3127	†RCA	
	SD6000	Signetics	
RF Detector/Video Amplifier			
	SL510	Plessey	
	SL511	Plessey	
	CA3068	RCA	
Servo Driver			60
	NE543	Signetics	
	NE544	Signetics	
	NE644	Signetics	

Function	Device	Source	Line
Consumer Circuits (Cont'd.)			
Security Systems Detector			
	L911	**Siliconix** **(1135)**	
Smoke Detector			
	MEM4962	GI	
	MEM4963	GI	
	MD4301	Mitel	
	MD4302	Mitel	70
	MD4303	Mitel	
	MD4304	Mitel	
	MC14461	Motorola	
	MC14462	Motorola	
	MC14463	Motorola	
	MC14464	Motorola	
	MC14465	Motorola	
	LM1801	National	
	NF5301	National	
	SFF25309	NPC	80
	SM110	Siliconix	
	SM120	Siliconix	
	SD1	Supertex	
	SD2	Supertex	
	SD3	Supertex	
	SCL5331	SSS	
	SCL5331A	SSS	
Sonar Transceiver			
	LM1812	National	
Sound Generator			90
	CS158	Cherry	
	CS258	Cherry	
	AY3-8910	GI	
	AY3-8912	GI	
	ICM7219	Intersil	
	SN76477	TI	
SSB Detector			
	SL623C	Plessey	
	SL624C	Plessey	
Synthesizers. See Linear - Phase Locked Loop/Synthesizer Circuits			100
Switches, Capacitance or Touch Sensing			
	S9260	**AMI** **(648)**	
	S9261	**AMI** **(648)**	
	S9262	**AMI** **(652)**	
	S9263	**AMI** **(648)**	
	S9264	**AMI** **(648)**	
	S9265	**AMI** **(648)**	
	S9266	**AMI** **(652)**	
	HA1190	Hitachi	110
	HA1194	Hitachi	
	SAS560	Hitachi	
	SAS570	Hitachi	
	SAS560	Siemens	
	SAS570	Siemens	
	SAS580	Siemens	
	SAS590	Siemens	
	SAS6800	Siemens	
	SAS6810	Siemens	
	TCA205	Siemens	120
	SAS660	Telefunken	
	SAS670	Telefunken	
	SAS6600	Telefunken	
	SAS6610	Telefunken	
	SAS6700	Telefunken	
	SAS6710	Telefunken	
	U112	Telefunken	
	U113	Telefunken	
	U221	Telefunken	

Function	Device	Source	Line
Consumer Circuits (Cont'd.)			
Switches, Capacitive Touch Input (keyboard encoder and prioritizer)			130
	TMS1976	TI	
Tachometer Circuit			
	LM2907	National	
	LM2917	National	
	AN603	Panasonic	
	SN76810	TI	
Tape Recorder Audio System; electronic switching between record and playback			
	LM1818	National	140
Tape Recorder System (motor speed control, automatic stop, dc manual stop, biasing and erasing oscillator)			
	TDA7770	SGS	
Tape Recorder Controller (mode change, abscence recording)			
	TC9121	Toshiba	
Tape Recorder System (power amps, preamp with ALC, meter driver, mute control)			
	TA7224	Toshiba	150
Tape Recorder System (power amp, preamp with ALC, meter driver)			
	TA7225	Toshiba	
Tape Recorder System (head, MIC, headphone, buffer, and record amps; meter driver)			
	TA7617	Toshiba	
Tape Deck Key Controller			
	M54410	Mitsubishi	
Telephone. See Linear - Telecommunication Circuits			
Thermo Controller (for air conditioners, refrigerators, etc.)			160
	TA7165	Toshiba	
Thermometer Circuit, Digital (-40 to 0°C)			
	AY3-1270	GI	
Timers. See Appliance Timers, Clock, Watch circuits in this section and Linear-Timers			
Tuning Voltage Stabilizer, for use with variable capacitance diodes			
	TAA550	Signetics	
	TCA530	Signetics	170
	TCA750	Signetics	
	TAA550	SGS	
T.V. AFT System			
	μA3064	†Fairchild	
	HA1108	Hitachi	
	HA1126	Hitachi	
	M5134	Mitsubishi	
	M5135	Mitsubishi	
	CA3139	Motorola	
	MC1364	Motorola	180
	LM3064	National	
	μPC423	NEC America	
	AN220	Panasonic	
	AN221	Panasonic	
	AN222	Panasonic	
	AN320	Panasonic	
	AN321	Panasonic	
	AN325	Panasonic	
	AN326	Panasonic	
	CA3044	†RCA	190
	CA3064	†RCA	
	CA3139	RCA	
	LA1364	Sanyo	
	ULN-2264	Sprague	

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Values

LINEAR–Consumer Circuits (Cont'd)

Function	Device	Source	Line
Consumer Circuits (Cont'd.)			
T.V. AFT System (Cont'd.)			
	SN76565	TI	
	TA7070	Toshiba	
T.V. Camera Sync. Generator			
	3262A	Fairchild	
	3262B	Fairchild	
	ZNA134	Ferranti	
	MM5320	National	
	MM5321	National	
	MN6060	Panasonic	10
	S178	Siemens	
TV, CATV Amplifers (hybrid)			
	AFT414	Amperex	
	AFT415	Amperex	
	AFT417	Amperex	
	AFT419	Amperex	
	MHW559	Motorola	
	MHW560	Motorola	
	MHW561	Motorola	
	MHW562	Motorola	20
	MHW570	Motorola	
	MHW572	Motorola	
	MHW580	Motorola	
	MHW594	Motorola	
	MHW595	Motorola	
	MHW1121	Motorola	
	MHW1127	Motorola	
	MHW1171	Motorola	
	MHW1172	Motorola	
	MHW1182	Motorola	30
	MHW1221	Motorola	
	MHW1222	Motorola	
	MHW1341	Motorola	
	MHW1342	Motorola	
	MHW1343	Motorola	
	MHW1391	Motorola	
	MHW1392	Motorola	
	CA2100	TRW	
	CA2300	TRW	
	CA2301	TRW	40
	CA2418	TRW	
	CA2600	TRW	
	CA2601	TRW	
T.V. Channel Display (see also T.V. Tuning below)			
	AY5-8300	GI	
	AY5-8301	GI	
	U143	Telefunken	
T.V. Channel Display with Time			
	AY5-8310	GI	
	AY5-8311	GI	50
	AY5-8320	GI	
	AY5-8321	GI	
	AY5-8322	GI	
	AY5-8324	GI	
	MM5318	National	
	MM5810	National	
	MM5841	National	
	MM58106	National	
T.V. Channel Selection			
	M51231	Mitsubishi	60
	M51232	Mitsubishi	
	M51233	Mitsubishi	
	μPC1009	NEC America	
	LB1500	Sanyo	
	LB1501	Sanyo	
	LB1515	Sanyo	
	SAS560	Siemens	
		(Continued)	

Function	Device	Source	Line
Consumer Circuits (Cont'd.)			
T.V. Channel Selection (Cont'd.)			
	SAS570	Siemens	
	SAS580	Siemens	70
	SAS590	Siemens	
	TDA2620	Signetics	
	TDA2630	Signetics	
	TDA2631	Signetics	
	ML231	TI	
	ML232	TI	
	SN76701	TI	
	SN76702	TI	
	SN76710	TI	
	SN76721	TI	80
	SN76727	TI	
	TA7171	Toshiba	
	TA7172	Toshiba	
	TA7177	Toshiba	
	TA7178	Toshiba	
	TA7315	Toshiba	
T.V. Character Generator (indicates tuning voltage scale and band info on screen)			
	U191	Telefunken	
T.V. Chroma Circuits			90
	μA746	Fairchild	
	μA780	Fairchild	
	μA781	Fairchild	
	μA787	Fairchild	
	μA788	Fairchild	
	TAA630	Fairchild	
	TBA510	Fairchild	
	TBA520	Fairchild	
	TBA540	Fairchild	
	TBA560	Fairchild	100
	TBA990	Fairchild	
	TDA2510	Fairchild	
	TDA2521	Fairchild	
	TDA2522	Fairchild	
	TDA2530	Fairchild	
	TDA2560	Fairchild	
	HA11247	Hitachi	
	HA11412	Hitachi	
	HA11580	Hitachi	
	M5190	Mitsubishi	110
	M5192	Mitsubishi	
	M5193	Mitsubishi	
	M5194	Mitsubishi	
	MC1323	Motorola	
	MC1324	Motorola	
	MC1327	Motorola	
	MC1398	Motorola	
	MC1399	Motorola	
	LM746	National	
	LM1828	National	120
	LM1848	National	
	LM3067	National	
	LM3070	National	
	LM3071	National	
	LM3126	National	
	TBA510	National	
	TBA530	National	
	TBA540	National	
	TBA560	National	
	TBA990	National	130
	μPC562	NEC America	
	μPC580	NEC America	
	μPC1380	NEC America	
	AN225	Panasonic	
	AN227	Panasonic	
	AN234	Panasonic	
		(Continued)	

Function	Device	Source	Line
Consumer Circuits (Cont'd.)			
T.V. Chroma Circuits (Cont'd.)			
	AN235	Panasonic	
	AN236	Panasonic	
	AN237	Panasonic	140
	AN242	Panasonic	
	AN281	Panasonic	
	AN282	Panasonic	
	AN288	Panasonic	
	AN289	Panasonic	
	AN342	Panasonic	
	AN343	Panasonic	
	AN380	Panasonic	
	SL901	Plessey	
	SL917	Plessey	150
	SL918	Plessey	
	SL1327	Plessey	
	TBA520	Plessey	
	TBA530	Plessey	
	TBA540	Plessey	
	TBA560	Plessey	
	TBA990	Plessey	
	TCA800	Plessey	
	CA1398	RCA	
	CA3066	RCA	160
	CA3067	RCA	
	CA3070	RCA	
	CA3071	RCA	
	CA3072	RCA	
	CA3121	RCA	
	CA3125	RCA	
	CA3126	RCA	
	CA3128	RCA	
	CA3135	RCA	
	CA3137	RCA	170
	CA3143	RCA	
	CA3144	RCA	
	CA3151	RCA	
	CA3170	RCA	
	CA3172	RCA	
	CA3221	RCA	
	LA1366N	Sanyo	
	LA1367	Sanyo	
	LA1368	Sanyo	
	LA1369	Sanyo	180
	LA1373	Sanyo	
	LA1374	Sanyo	
	LA1375	Sanyo	
	LA1376	Sanyo	
	LA1390	Sanyo	
	LA1397	Sanyo	
	TDA2140	SGS	
	TDA2150	SGS	
	TDA2160	SGS	
	TAA6301	Siemens	190
	TDA2522	Siemens	
	TDA2530	Siemens	
	TDA2560	Siemens	
	MC1327	Signetics	
	MC1399	Signetics	
	TAA630	Signetics	
	TBA327	Signetics	
	TBA395	Signetics	
	TBA396	Signetics	
	TBA500	Signetics	200
	TBA510	Signetics	
	TBA520	Signetics	
	TBA530	Signetics	
	TBA540	Signetics	
	TBA550	Signetics	
		(Continued)	

† Military Temperature Range (−55° to 125°C)

* Typical Values

Bold face indicates additional data is provided on the page noted.

LINEAR–Consumer Circuits (Cont'd)

Consumer Circuits (Cont'd.)

Function	Device	Source	Line
T.V. Chroma Circuits (Cont'd.)			
	TBA560	Signetics	
	TBA990	Signetics	
	TCA640	Signetics	
	TCA650	Signetics	
	TCA660	Signetics	
	TCA800	Signetics	
	TDA2500	Signetics	
	TDA2510	Signetics	
	TDA2520	Signetics	10
	TDA2522	Signetics	
	TDA2523	Signetics	
	TDA2530	Signetics	
	TDA2560	Signetics	
	TDA2670	Signetics	
	TBA395	Sprague	
	TBA396	Sprague	
	TDA1327	Sprague	
	ULN-2124	Sprague	
	ULN-2127	Sprague	20
	ULN-2216	Sprague	
	ULN-2217	Sprague	
	ULN-2218	Sprague	
	ULN-2219	Sprague	
	ULN-2224	Sprague	
	ULN-2228	Sprague	
	ULN-2229	Sprague	
	ULN-2261	Sprague	
	ULN-2268	Sprague	
	ULN-2293	Sprague	30
	ULN-2269	Sprague	
	ULN-2298	Sprague	
	TBA520	Telefunken	
	TBA530	Telefunken	
	TBA540	Telefunken	
	TBA560	Telefunken	
	TBA990	Telefunken	
	TDA2140	Telefunken	
	TDA2150	Telefunken	
	TDA2151	Telefunken	40
	TDA2160	Telefunken	
	TDA2161	Telefunken	
	SN76242	TI	
	SN76243	TI	
	SN76246	TI	
	SN76267	TI	
	SN76298	TI	
	TA7141A	Toshiba	
	TA7148	Toshiba	
	TA7149	Toshiba	50
	TA7150	Toshiba	
	TA7161	Toshiba	
	TA7167	Toshiba	
	TA7168	Toshiba	
	TA7169	Toshiba	
	TA7173	Toshiba	
	TA7174	Toshiba	
	TA7192	Toshiba	
	TA7193	Toshiba	
T.V. Color Bar Generator			60
	MM5332	National	
	NE549	Signetics	
TV Color Control for VIR broadcasts			
	HA11409	Hitachi	
	MN5330	Panasonic	
T.V. Contrast Control			
	TA7134	Toshiba	

Consumer Circuits (Cont'd.)

Function	Device	Source	Line
T.V. Convergence Circuit			
	HA1146	Hitachi	
	HA1147	Hitachi	70
	HA1148	Hitachi	
T.V. Frequency Synthesis Control (converts tuning data into frequency information for SDA100 system)			
	SM564	Siemens	
T.V. Games, see Games, T.V.			
T.V. Horizontal Processor			
	μA1391	Fairchild	
	μA1394	Fairchild	
	TBA920	Fairchild	
	TBA120S	Fairchild	80
	TDA2590	Fairchild	
	TDA2591	Fairchild	
	HA1160	Hitachi	
	MC1391	Motorola	
	MC1394	Motorola	
	LM1391	National	
	LM1394	National	
	TBA920	National	
	μPC570	NEC America	
	SL451	Plessey	90
	TBA920	Plessey	
	TBA940	Plessey	
	TBA950	Plessey	
	CA1391	RCA	
	CA1394	RCA	
	CA3147	RCA	
	CA920A	RCA	
	LA1384	Sanyo	
	TDA1180	SGS	
	TDA1280	SGS	100
	TDA2590	Siemens	
	TBA720A	Signetics	
	TBA920	Signetics	
	TDA2571	Signetics	
	TDA2573	Signetics	
	TDA2581	Signetics	
	TDA2590	Signetics	
	ULN-2291	Sprague	
	ULN-2294	Sprague	
	SN76525	TI	110
	TA7151	Toshiba	
T.V. Horizontal & Vertical Processor			
	HA11218	Hitachi	
	HA11235	Hitachi	
	LM1880	National	
	AN202	Panasonic	
	AN232	Panasonic	
	AN332	Panasonic	
	AN334	Panasonic	
	LA1381	Sanyo	120
	LA1382	Sanyo	
	TCA511	SGS	
	NE2622	Signetics	
	LM1880	Signetics	
T.V. Input Encoder (for sets without remote control)			
	U190	Telefunken	
T.V. Picture Sharpness			
	M51380	Mitsubishi	
	M51381	Mitsubishi	
	TA7126	Toshiba	130
	TA7135	Toshiba	
T.V. Remote Control (also for other remote control applications)			
	S2600	**AMI (467)**	

(Continued)

Consumer Circuits (Cont'd.)

Function	Device	Source	Line
T.V. Remote Control (also for other remote control applications) (Cont'd.)			
	S2601	**AMI (467)**	
	S2742	**AMI (471)**	
	S2743	**AMI (471)**	
	μA9706	Fairchild	140
	μA9706A	Fairchild	
	AY5-8410	GI	
	AY5-8411	GI	
	AY5-8420	GI	
	AY5-8450	GI	
	AY5-8460	GI	
	AY5-8461	GI	
	AY3-8470	GI	
	AY3-8475	GI	
	SAA1024	GI	150
	SAA1025	GI	
	M51240	Mitsubishi	
	M51480	Mitsubishi	
	M51481	Mitsubishi	
	MC14422	Motorola	
	MC6525	Motorola	
	MC6526	Motorola	
	MC6527	Motorola	
	LM1812	National	
	MM53102	National	160
	MM53103	National	
	MM53112	National	
	MM53116	National	
	ML920	Plessey	
	SL490	Plessey	
	CA3013	RCA	
	CA3014	RCA	
	CA3035	†RCA	
	M054	SGS	
	M055	SGS	170
	M1024	SGS	
	M1025	SGS	
	S175	Siemens	
	SAB3209	Siemens	
	SAB3210	Siemens	
	SAB3270	Siemens	
	SAB4209	Siemens	
	SAF1031	Signetics	
	SAF1032	Signetics	
	U318M	Telefunken	180
	U321M	Telefunken	
	U327	Telefunken	
	U334	Telefunken	
	SN76730	TI	
T.V. Signal Processor (Jungle Circuit)			
	MC1344	Motorola	
	LM1845	National	
	AN228	Panasonic	
	AN229	Panasonic	
	AN230	Panasonic	190
	AN231	Panasonic	
	AN249	Panasonic	
	AN328	Panasonic	
	AN331	Panasonic	
	AN349	Panasonic	
	AN350	Panasonic	
	TBA550	Plessey	
	CA3120	RCA	
	CA3142	RCA	
	LA1388	Sanyo	200
	LA3181	Sanyo	
	LA3182	Sanyo	
	LA3187	Sanyo	
	TBA311	SGS	

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Values

LINEAR–Consumer Circuits (Cont'd)

Function	Device	Source	Line
Consumer Circuits (Cont'd.)			
T.V. Signal Processor (Jungle Circuit) (Cont'd.)			
	TBA550	Signetics	
	TBA890	Signetics	
	TBA900	Signetics	
	TDA2680	Signetics	
	TDA2690	Signetics	
	ULN-2125	Sprague	
	SN76524	TI	
	SN76544	TI	
	SN76545	TI	10
T.V. Sound Circuit			
	μA3065	Fairchild	
	TDA1190	Fairchild	
	TDA1190Z	Fairchild	
	HA1124	Hitachi	
	HA1125	Hitachi	
	HA1364	Hitachi	
	M5143	Mitsubishi	
	M5144	Mitsubishi	
	M5147	Mitsubishi	20
	MC1331	Motorola	
	MC1351	Motorola	
	MC1357	Motorola	
	MC1358	Motorola	
	TDA1190	Motorola	
	LM1351	National	
	LM1808	National	
	LM2111	National	
	LM2113	National	
	LM3065	National	30
	TBA120	National	
	μPC558	NEC America	
	μPC575	NEC America	
	μPC576	NEC America	
	AN239	Panasonic	
	AN206	Panasonic	
	AN240	Panasonic	
	AN241	Panasonic	
	AN255	Panasonic	
	AN341	Panasonic	40
	AN340	Panasonic	
	SL432	Plessey	
	SL437	Plessey	
	TAA570	Plessey	
	TAA661	Plessey	
	TBA120	Plessey	
	TBA750	Plessey	
	CA1190	RCA	
	CA2111	†RCA	
	CA3041	RCA	50
	CA3042	RCA	
	CA3043	†RCA	
	CA3065	RCA	
	CA3075	†RCA	
	CA3134	RCA	
	LA1363	Sanyo	
	LA1365	Sanyo	
	TDA1190	SGS	
	TDA2190	SGS	
	TBA120	Siemens	60
	TDA2840	Siemens	
	TBA120S	Signetics	
	TBA120U	Signetics	
	TBA750	Signetics	
	TDA2610	Signetics	
	ULN2111	Signetics	
	ULN2211	Signetics	
	TDA1190	Sprague	
	ULN-2111	Sprague	
		(Continued)	

Function	Device	Source	Line
Consumer Circuits (Cont'd.)			
T.V. Sound Circuit (Cont'd.)			70
	ULN-2211	Sprague	
	ULN-2212	Sprague	
	ULN-2290	Sprague	
	TBA120	Telefunken	
	SN76643	TI	
	SN76651	TI	
	SN76660	TI	
	SN76665	TI	
	SN76666	TI	
	SN76688	TI	80
	TA7051	Toshiba	
	TA7072	Toshiba	
	TA7073A	Toshiba	
	TA7130	Toshiba	
	TA7146	Toshiba	
	TA7176	Toshiba	
	TA7314	Toshiba	
T.V. Timer, Programmable			
	MM53100	National	
	MM53105	National	90
T.V. Tone Control			
	TA7125	Toshiba	
T.V. Touch Tuner. See also Switches, Capacitance above.			
	ML231	Plessey	
	ML232	Plessey	
	TDA2620	Signetics	
	TDA2630	Signetics	
	TDA2631	Signetics	
	SAS660	Telefunken	100
	SAS670	Telefunken	
T.V. Touch Tuner Control Interface			
	ML236	Plessey	
	ML237	Plessey	
	ML238	Plessey	
	ML239	Plessey	
T.V. Tuner Controller			
	SH1549	Fairchild	
	AY3-8203	GI	
	MEM4956	GI	110
	T1002	GI	
	T1102	GI	
	T1201	GI	
	U193	Telefunken	
T.V. Tuning Indicator			
	AY3-8330A	GI	
	AY3-8331	GI	
	AY3-8335	GI	
T.V. Tuning System			
	Economega	GI	120
	Omega	GI	
	SDA100	Siemens	
T.V. Vertical Deflection			
	TDA1170	Fairchild	
	TDA1270	Fairchild	
	MC1393	Motorola	
	μPC1031	NEC America	
	AN232	Panasonic	
	AN332	Panasonic	
	AN334	Panasonic	130
	LA1383	Sanyo	
	TDA1170	SGS	
	TDA1270	SGS	
	TDA1370	SGS	
	TDA2600	Signetics	
		(Continued)	

Function	Device	Source	Line
Consumer Circuits (Cont'd.)			
T.V. Vertical Deflection (Cont'd.)			
	TA7152	Toshiba	
T.V. Video Circuits			
	TBA970	Fairchild	
	HA1152	Hitachi	140
	HA11220	Hitachi	
	HA11221	Hitachi	
	HA11422	Hitachi	
	M5169	Mitsubishi	
	M5181	Mitsubishi	
	M5183	Mitsubishi	
	M5184	Mitsubishi	
	M5185	Mitsubishi	
	M5186	Mitsubishi	
	M5187	Mitsubishi	150
	M5195	Mitsubishi	
	M51247	Mitsubishi	
	M51248	Mitsubishi	
	MC1330	Motorola	
	MC1330A1	Motorola	
	MC13330A2	Motorola	
	MC1331	Motorola	
	MC1349	Motorola	
	MC1350	Motorola	
	MC1352	Motorola	160
	MC1372	Motorola	
	XC1373	Motorola	
	LM1807	National	
	LM1889	National	
	TBA440	National	
	μPC595	NEC America	
	μPC596	NEC America	
	AN239	Panasonic	
	AN245	Panasonic	
	AN246	Panasonic	170
	AN247	Panasonic	
	AN248	Panasonic	
	AN279	Panasonic	
	AN349	Panasonic	
	AN350	Panasonic	
	SL437	Plessey	
	SL456	Plessey	
	SL457	Plessey	
	TBA440	Plessey	
	TCA270	Plessey	180
	TDA440	Plessey	
	CA270	RCA	
	CA1352	RCA	
	CA3068	RCA	
	CA3136	RCA	
	LA1352	Sanyo	
	LA1353	Sanyo	
	TBA1440	Siemens	
	TBA1441	Siemens	
	TDA5500	Siemens	190
	TBA440	Signetics	
	TBA1440	Signetics	
	TBA1440G	Signetics	
	TBA1441	Signetics	
	TCA270	Signetics	
	TCA540	Signetics	
	TDA2540	Signetics	
	TDA2541	Signetics	
	TDA440	SGS	
	TDA440	Telefunken	200
	TDA4400	Telefunken	
	TDA4410	Telefunken	
	TDA4420	Telefunken	
	TDA4421	Telefunken	
		(Continued)	

† Military Temperature Range (−55° to 125°C)

* Typical Values

Bold face indicates additional data is provided on the page noted.

LINEAR–Consumer Circuits (Cont'd)

Function	Device	Source	Line
Consumer Circuits (Cont'd.)			
T.V. Video Circuits (Cont'd.)			
	TDA4430	Telefunken	
	SN76600	TI	
	SN76644	TI	
	SN76650	TI	
	TC5003	Toshiba	
	TA7069	Toshiba	
	TA7074	Toshiba	
	TA7075	Toshiba	
	TA7076	Toshiba	10
	TA7124	Toshiba	
	TA7145	Toshiba	
	TA7147	Toshiba	
	TA7162	Toshiba	
T.V. Video Pulse Generator			
	S178	Siemens	
Video Tape Recorder			
	HA11701	Hitachi	
	HA11702	Hitachi	
	HA11703	Hitachi	20
	HA11704	Hitachi	
	HA11705	Hitachi	
	HA11706	Hitachi	
	HA11707	Hitachi	
	AN301	Panasonic	
	AN302	Panasonic	
	AN303	Panasonic	
	AN304	Panasonic	
	AN305	Panasonic	
	AN306	Panasonic	30
	AN307	Panasonic	
	AN316	Panasonic	
	AN318	Panasonic	
	AN605	Panasonic	
	TDA2700	Signetics	
	TDA2710	Signetics	
	TDA2720	Signetics	
	TDA2730	Signetics	
Video Tape Recorder Timer			
	VTR3300	GI	40
Watch-Alarm			
	ICM7220A	Intersil	
	ICM7221	Intersil	
	ICM7222	Intersil	
	MSM5516	OKI	
	CD22007-2	RCA	
	SY5009	Synertek	
Watch, Analog (See also Digital-CMOS Oscillators/Dividers)			
	HC43850	Hitachi	50
	ICM7047	Intersil	
	MC14450	Motorola	
	MC14451	Motorola	
	μPD809	NEC America	
	SY5008	Synertek	
Watch, Digital (See also Digital-CMOS Oscillators/Dividers)			
	S1424A	AMI	
	S1424C	AMI	
	S1427A	AMI	60
	S2732	AMI	
	S10305	AMI	
	HDO4821	Harris	
	HDO4822	Harris	
	HDO4823	Harris	
	HDO4830	Harris	
	HDO4831	Harris	
		(Continued)	

Function	Device	Source	Line
Consumer Circuits (Cont'd.)			
Watch, Digital (See also Digital-CMOS Oscillators/Dividers) (Cont'd.)			
	HC42022	Hitachi	70
	HC42030	Hitachi	
	HC43032	Hitachi	
	HC43802	Hitachi	
	HC43803	Hitachi	
	300	Hughes	
	359	Hughes	
	371	Hughes	
	398	Hughes	
	5810	Intel	
	ICM1424	Intersil	80
	ICM1424M	Intersil	
	ICM7200	Intersil	
	ICM7202	Intersil	
	ICM7203	Intersil	
	ICM7204	Intersil	
	ICM7210	Intersil	
	ICM7210C	Intersil	
	ICM7210M	Intersil	
	ICM7210MC	Intersil	
	ICM7214	Intersil	90
	ICM7214M	Intersil	
	ICM7220	Intersil	
	ICM7220B	Intersil	
	ICM7220M	Intersil	
	ICM7220MA	Intersil	
	ICM7220MC	Intersil	
	ICM7221	Intersil	
	ICM7222	Intersil	
	MP7145	Micro Power	
	MP7155	Micro Power	100
	MP7175	Micro Power	
	MC14440	Motorola	
	MC14470	Motorola	
	MC14478	Motorola	
	MC14479	Motorola	
	MC14480	Motorola	
	MCC14471	Motorola	
	MCC14472	Motorola	
	MCC14479	Motorola	
	MC14480	Motorola	110
	MCC14481	Motorola	
	MM58104	National	
	MM58115	National	
	MM58117	National	
	MM58118	National	
	MM58119	National	
	MM58120	National	
	MM5829	National	
	MM5860	National	
	MM58601	National	120
	MM5880	National	
	MM58801	National	
	MM5882	National	
	MM5885	National	
	MM5886	National	
	MM58127	National	
	MM58128	National	
	MM58129	National	
	MM58130	National	
	MM58190	National	130
	MM58192	National	
	MM58193	National	
	μPD810	NEC America	
	μPD819	NEC America	
	μPD824	NEC America	
	μPD826	NEC America	
	μPD828	NEC America	
		(Continued)	

Function	Device	Source	Line
Consumer Circuits (Cont'd.)			
Watch, Digital (See also Digital-CMOS Oscillators/Dividers) (Cont'd.)			
	μPD829	NEC America	140
	μPD844	NEC America	
	5024	Nortec	
	5055	Nortec	
	MSM5513	OKI	
	MSM5514	OKI	
	MSM5515	OKI	
	MSM5970	OKI	
	MN6050	Panasonic	
	MN6051	Panasonic	
	MN6052	Panasonic	150
	MN6053	Panasonic	
	MN6070	Panasonic	
	MM6090	Panasonic	
	MN6091	Panasonic	
	MN6092	Panasonic	
	MS680	RTC	
	MS681	RTC	
	MS682	RTC	
	MS683	RTC	
	CD22001	RCA	160
	CD22003	RCA	
	CD22006	RCA	
	SCL5450	SSS	
	SCL5451	SSS	
	SCL54301	SSS	
	SCL54302	SSS	
	SCL54303	SSS	
	SY5001	Synertek	
	SY5002	Synertek	
	SY5007	Synertek	170
Watch, Digital-Calculator			
	MM58101	National	
	MM58102	National	
Watch-Message			
	325	Hughes	
	328	Hughes	
Stopwatch			
	400	Hughes	
	ICM7045	Intersil	
	ICM7205	Intersil	180
	ICM7215	Intersil	
	C1200	**LSI Comp (494)**	
	CD22008-1	RCA	
	DF213	Siliconix	
	DF214	Siliconix	
Watch/stopwatch			
	ICM7220C	Intersil	
	MM5890	National	
	SY5009	Synertek	

† Military Temperature Range (−55° to 125°C)

* Typical Values

LINEAR–Followers

Bias Current na 25°C	Offset Voltage mv 25°C	Voltage Drift µv/°C	Unity Gain Bandwidth MHz min	Slew Rate v/µs	Output v @ ma	Supply Range	Comments	Device	Source
Followers									
0.1	10	25*	100*	1000	9 @ 90	±5 to ±20	Fast Follower	LH0033	† National
	50	400	200	3000	10 @ 200	±11 to ±18	Very Fast, FET	9963	† OEI
0.15	20	25*	100*	1000	9 @ 90	±5 to ±20	Fast Follower	LH0033C	National
0.2	25	300*	200*	2000	10 @ 200	±5 to ±20	Very Fast Follower	LH0063	† National
	50	300*	200*	2000	10 @ 200	±5 to ±20	Very Fast Follower	LH0063C	National
0.2*	50	300*	300*	2000	10 @ 200	±5 to ±20	Gain 0.094 (50 ohm)	**3553**	**† Burr-Brown (920)**
0.3	1.0	10	8.0*	12	10@10	±5 to ±18	High Speed Follower	BUF-02A	† PMI
								BUF-02E	PMI
0.5	3.0	20	8.0*	9	10@10	±5 to ±18	High Speed Follower	BUF-02B	† PMI
								BUF-02F	PMI
1.0	10.0	—	—	4*	12 @ 2	±5 to ±18	Follower	TCA410A	Signetics
3	4.0	6*	12*	30*	10 @ 1	±5 to ±18	Follower, replaces 102	SG210	Silicon G
			20*	30*	10 @ 1	±5 to ±18	Follower, replaces 102	LM210	AMD
								LM210	National
							Dual 210 Follower	LH2210	National
		10*	20*	30*	10 @ 1	±5 to ±18	Follower, replaces 102	110	† Intersil
								210	Intersil
		12*	12*	30*	10 @ 1	±5 to ±18	Follower, replaces 102	SG110	† Silicon G
			20*	30*	10 @ 1	±5 to ±18	Follower, replaces 102	LM110	† AMD
								µA110M	† Fairchild
								LM110	† National
							Dual 110 Follower	LH2110	Intersil
								LH2110	† National
	10.0	—	—	4*	12 @ 2	±5 to ±18	Follower	TCA410B	Signetics
								TCA410D	Signetics
5	20.0	100	200	1000	10 @ 500	±11 to ±18	Fast, High Current	9911	† OEI
7.0	0.1	3	0.6*	0.17*	10@15	±3 to ±18	Precision Follower	BUF-01A	† PMI
								BUF-01E	PMI
	0.2	5	0.6*	0.17*	10 @ 15	±3 to ±18	Precision Follower	BUF-01B	† PMI
								BUF-01F	PMI
7	7.5	10*	12*	30*	10 @ 1	±5 to ±18	Follower, replaces 102	SG310	Silicon G
			20*	30*	10 @ 1	±5 to ±18	Follower, replaces 102	LM310	AMD
								µA310C	Fairchild
								310	Intersil
								LM310	Motorola
								LM310	National
							Dual 310 Follower	LH2310	Intersil
								LH2310	† National
10	5.0	6*	8*	10*	10 @ 1	±15	Follower	SG102	† Silicon G
			10*	10*	10 @ 1.25	±12 to ±18	Follower	LM102	† National
			20*	20*	10 @ 1.25	±5 to ±18	Follower	LM202	AMD
			—	—	10 @ 1.25	±15	Follower	µA102M	† Fairchild
								102	† Intersil
		12*	20*	20*	10 @ 1.25	±5 to ±18	Follower	LM102	† AMD
15	10.0	15*	8*	10*	10 @ 1	±15	Follower	SG202	Silicon G
			10*	10*	10 @ 1.25	±12 to ±18	Follower	LM202	National
			—	—	10 @ 1.25	±15	Follower	202	Intersil
20	20.0	100	60	2000	10 @ 100	±6 to ±18	Very Fast Follower	9910	† OEI
30	15.0	20*	8*	10*	10 @ 1	±15	Follower	SG302	Silicon G
			10*	10*	10 @ 1.25	±12 to ±18	Follower	LM302	National
			20*	20*	10 @ 1.25	±5 to ±18	Follower	LM302	AMD
			—	—	10 @ 1.25	±15	Follower	µA302C	Fairchild
								302	Intersil

See also Linear-Amplifiers, Special Purpose - Current Amplifiers

† Military Temperature Range (−55° to 125°C)

* Typical Values

Bold face indicates additional data is provided on the page noted.

LINEAR–Operational Amplifiers

General Purpose

The 101A series consists of the 101A (-55°C to 125°C), the 201A (-25°C to 85°C) and the 301 (0°C to 70°C). These units require an external compensation capacitor which permits the bandwidth to be optimized for particular applications.

Device	Source	Line
LM101A	AMD	
AD101A	AD	
µA101A	Fairchild	
101A	Intersil	
LM101A	Motorola	10
LM101A	**National (1035)**	
CA101A	RCA	
LM101A	Raytheon	
LM101A	Signetics	
SG101A	Silicon G	
LM101A	TI	
TA7506	Toshiba	

The performance of the 741 series is similar to the 101. These units include internal compensation to make the device stable and to eliminate the need for an external capacitor.

Device	Source	Line
741	AMD	
AD741	AD	
µA741	Fairchild	
HA17741	Hitachi	
ICL741	Intersil	
MC1741	Motorola	
LM741	**National (1035)**	
µPC741	NEC America	
SFC2741	NPC	30
OP-02	PMI	
PM741	PMI	
SSS741	PMI	
CA741	RCA	
RC741	Raytheon	
SG741	Silicon G	
µA741	Signetics	
TDA0741	Signetics	
µA741	TI	
TA7504	Toshiba	40

Dual Amplifiers. The 1458 (0°C to 70°C) and the 1558 (-55°C to 125°C) offer approximately the same performance as the 741. Compensation is built in.

Device	Source	Line
1458	AMD	
XR1458	Exar	
µA1458	Fairchild	
HA171458	Hitachi	
MC1458	Motorola	
LM1458	National	
µPC1458	NEC America	50
OP-14	PMI	
PM1458	PMI	
SSS1458	PMI	
CA1458	RCA	
RC1458	Raytheon	
MC1458	Signetics	
SG1458	Silicon G	
MC1458	TI	

FET Input. Bipolar/JFET available in standard (155), wideband (156) and uncompensated (157) versions, premium performance (A and B suffixes), and various temperature ranges (155, 255, 355, etc are available.) Some versions approach the low cost of the units below.

Device	Source	Line
LF155	AMD	60
µAF155	Fairchild	
LF155	Intersil	
LF155	Motorola	
LF155	**National (1035)**	

* (Continued)

General Purpose (Cont'd.)

FET Input. Bipolar/JFET available in standard (155), wideband (156) and uncompensated (157) versions, premium performance (A and B suffixes), and various temperature ranges (155, 255, 355, etc are available.) Some versions approach the low cost of the units below. (Cont'd.)

Device	Source	Line
PM155	PMI	70
LF155	Raytheon	
LF155	Signetics	
LF155	TI	

FET Input. The "741" of the FET input devices has yet to be established. Such a device requires very low cost, several sources, and many users. Commercial devices in the 155 series above meet some of these criteria, however, devices from the series below are generally lower in cost.

Device	Source	Line
µAF771	Fairchild	80
CA3140	Intersil	
LF351	**National (1035,1073)**	
LF13741	National	90
CA3140	RCA	
CA3160	RCA	
TL081	TI	

High Output Current

ma @ v	Device	Source	Line
2700 @ 24	ICH8530C	Intersil	
	ICH8530M	† Intersil	
2000 @ 30	**3572A**	**Burr-Brown (920)**	
2000 @ 24	ICH8520C	Intersil	100
	ICH8520M	† Intersil	
1100 @ 11	833-21	Beckman	
	LH0021	† National	
1000 @ 30	**3571A**	**Burr-Brown (920)**	
1000 @ 24	ICH8510C	Intersil	
	ICH8510M	† Intersil	
1000 @ 10	LH0021C	National	110
500 @ 10	LH0061	† National	
	LH0061C	National	
200 @ 10	µA759	† Fairchild	
	µA759C	Fairchild	
130 @ 13	LH0041	† National	
	LH0041C	National	120
100 @ 10	**3554A**	**Burr-Brown (920)**	
	3554B	**Burr-Brown (920)**	
	3554S	Burr-Brown	
	LH0003	National	
100 @ —	CA3094	RCA	
75 @ 145	**3583**	**Burr-Brown (920)**	
60 @ 30	**3580J**	**Burr-Brown (920)**	130
50 @ 10	9914	OEI	
	1430	Teledyne P	
50 @ 5	LH0005	National	
	LH0005A	† National	
47 @ 14	LH0020	† National	
	LH0020C	National	140
40 @ 4	LH0005C	National	
38 @ 11	CA3033A	† RCA	
	CA3047A	RCA	
32 @ 8	TAA851	Telefunken	
	TAA865	Telefunken	
30 @ 70	3581J	Burr-Brown	150
20 @ 12	TAA761	Siemens	
	TAA762	† Siemens	
	TAA765	Siemens	
	TAA2761	Siemens	

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Values

LINEAR–Operational Amplifiers (Cont'd)

ma @ v	Device	Source	Line
High Output Current (Cont'd.)			
20 @ 12		(Cont'd.)	
	TAA2762	Siemens	
	TAA2765	Siemens	
	TAA4761	Siemens	
	TAA4765	Siemens	
	TCA311	Siemens	
	TCA312	Siemens	
	TCA315	Siemens	
	TCA325	Siemens	
	TCA331	Siemens	10
	TCA332	† Siemens	
	TCA335	Siemens	
20 @ 10			
	9912	† OEI	
20 @ 8			
	TAA861	Siemens	
	TAA862	† Siemens	
	TAA865	Siemens	
18 @ 9			
	CA3033	† RCA	20
15 @ 145			
	3582J	Burr-Brown	
	3584	**Burr-Brown (920)**	
15 @ 30			
	LH0004C	National	
15 @ 10			
	HA-2620	**† Harris (980)**	
	HA2620	Intersil	

Unity Gain Slew Rate (v/µsec min)	Device	Source	Line
High Speed			
2500 (g=5)			
	9909	OEI	30
1000			
	AM-500GC	**Datel (691)**	
	AM-500MC	**† Datel (691)**	
	9914	OEI	
800(g=2)			
	NE539	Signetics	
600			
	9912	† OEI	
	9932	OEI	
500			40
	1430	Teledyne P	
400			
	LH0024	† National	
350			
	LH0032	† National	
	LH0032C	National	
300			
	9916	† OEI	
280			
	HA-2530	**† Harris (974)**	50
250			
	HA-2535	**Harris (974)**	
	LH0024C	National	
	1435	† Teledyne P	
250(g=5)			
	9906	† OEI	
200			
	9908	† OEI	
	9917	OEI	
100(g=3)			60
	HA-2520	**Harris (972)**	
100			
	AD509K	AD	
	AD509S	† AD	
	3550K	**Burr-Brown (920)**	
80			
	AD509J	AD	
	3507J	**Burr-Brown (920)**	
	1322	† Teledyne P	
	1322-01	Teledyne P	70
65			
	3550J	**Burr-Brown (920)**	
	3550S	**† Burr-Brown (920)**	
50			
	LM118	† AMD	
	LM318	AMD	
	AD518	AD	
	AD518S	† AD	
	AD528	AD	
	AD528S	† AD	80
	AD581J	AD	
	AD581K	AD	
	µA118	† Fairchild	
	µA318	Fairchild	
	HA-2510	**† Harris (968)**	
	LH0062	† National	
	LH0062C	National	
	LM118	**† National (1035)**	
	LM318	National	
	SFC2118	† NPC	90
	SFC2318	NPC	
	LM118	† Raytheon	

(Continued)

Unity Gain Slew Rate (v/µsec min)	Device	Source	Line
High Speed (Cont'd.)			
50		(Cont'd.)	
	LM318	Raytheon	
	LM118	† TI	
	LM318	TI	

† Military Temperature Range (−55° to 125°C)

* Typical Values

Bold face indicates additional data is provided on the page noted.

LINEAR–Operational Amplifiers (Cont'd)

High Voltage

Maximum Supply Voltage	Device	Source	Line
±150			
	3582J	† Burr-Brown	
	3583	**Burr-Brown (920)**	
	3584	**Burr-Brown (920)**	
±75			
	3581J	† Burr-Brown	
±40			
	3571A	**† Burr-Brown (920)**	
	3572A	**† Burr-Brown (920)**	
	AM-464-2	**Datel (687)**	10
	AM-464-2M	**† Datel (687)**	
	HA-2640	**† Harris (984)**	
	HA-2645	**Harris (984)**	
	MC1536	† Motorola	
	LH0004	† National	
	LH0004C	National	
	LM143	† National	
	LM243	National	
	LM144	† National	
	SG1536	Silicon G	20
	1332	Teledyne P	
±35			
	3580J	**Burr-Brown (920)**	
±34			
	MC1436	Motorola	
	LM344	National	
	SG1436	Silicon G	
±30			
	ICH8510C	Intersil	
	ICH8510M	† Intersil	30
	ICH8520C	Intersil	
	ICH8520M	† Intersil	
	ICH8530C	Intersil	
	ICH8530M	† Intersil	
	MC1436C	Motorola	
	LM343	National	
	SG1436C	Silicon G	

Low Bias Current

Rated values do not usually include thermal rise due to circuit operation.

Current pa 25°C	Device	Source	Line
0.01			40
	ICH8500A	Intersil	
0.075			
	AD515L	AD	
	3528C	**Burr-Brown (920)**	
0.1			
	3523L	**Burr-Brown (920)**	
	ICH8500	Intersil	
0.15			
	AD515K	AD	
0.25			50
	AD523L	AD	
	3523K	**Burr-Brown (920)**	
0.3			
	AD515J	AD	
0.5			
	AD523K	AD	
	3523J	**Burr-Brown (920)**	
1.0			
	AD523J	AD	
	3522L	**Burr-Brown (920)**	60
	ICL8007AC	Intersil	
	ICL8007AM	† Intersil	
	LH0052	**† National (1073)**	
	1439	Teledyne P	
2.0			
	3527B	**Burr-Brown (920)**	
5.0			
	ADM501	AD	
	ADM506	AD	
	AD506L	AD	70
	3522K	**Burr-Brown (920)**	
	3522S	**Burr-Brown (920)**	
	3527A	**Burr-Brown (920)**	
	3527C	**Burr-Brown (920)**	
	LH0052C	**National (1073)**	
	CA3080	RCA	
	CA3080A	† RCA	
	1425-01	Teledyne P	
	1425-02	Teledyne P	

Low Drift

Voltage Drift (μv/°C Max)	Device	Source	Line
0.1			80
	AM-490-2C	**Datel (690)**	
0.3			
	AM-490-2B	**Datel (690)**	
	HA-2904	**Harris (996)**	
0.5			
	AD504M	AD	
	AD510L	AD	
	AD517L	AD	
	3510C	**Burr-Brown (920)**	
	LH0044A	**† National (1073)**	90
	LH0044AC	**National (1073)**	
	LH0044B	**National (1073)**	
	OP-05A	PMI	
0.6			
	SSS725A	† AMD	
	AM-490-2M	**† Datel (690)**	
	μA714	† Fairchild	
	HA-2900	**† Harris (996)**	
	OP-05E	PMI	
	OP-07A	† PMI	100
	SSS725A	† PMI	
	SSS725E	PMI	
1.0			
	AD504L	AD	
	AD504S	† AD	
	AD510K	AD	
	AD510S	† AD	
	AD517K	AD	
	AD517S	† AD	
	3500E	**Burr-Brown (920)**	110
	3510B	**Burr-Brown (920)**	
	3510S	**† Burr-Brown (920)**	
	3521L	**Burr-Brown (920)**	
	AM-490-2A	**Datel (690)**	
	μA725A	† Fairchild	
	μA725E	Fairchild	
	LH0044	**† National (1073)**	
	LH0044C	**National (1073)**	
	LM725A	National	
	SSS725	† PMI	120
	SSS725B	PMI	
	OP-05	† PMI	
1.0 (Dual Unit)			
	OP-10	† PMI	
	OP-10A	† PMI	
	OP-10E	PMI	
1.3			
	μA174	† Fairchild	
	μA714E	Fairchild	
	OP-07	† PMI	130
	OP-07E	PMI	
1.5			
	3510A	**Burr-Brown (920)**	
	OP-05C	PMI	
	OP-20B	PMI	
	OP-20F	PMI	
	SSS725C	PMI	
1.5 (Dual Unit)			
	OP-10C	PMI	
1.6			140
	μA714C	Fairchild	
	OP-07C	PMI	
2.0			
	3527C	**Burr-Brown (920)**	

† Military Temperature Range (−55° to 125°C)

* Typical Values

LINEAR–Operational Amplifiers (Cont'd)

Low Power

Programmable

The current drain limits of these units are approximately 10-300 µa.

Supply Current µa @ ±15v	Device	Source	Line
	µA776	† Fairchild	
	µA776C	Fairchild	
	HA-2720	**Harris** (990)	
	HA-2725	**Harris** (990)	
	4250	† Intersil	
	4250C	Intersil	
	ICL8021C	Intersil	10
	ICL8021M	† Intersil	
	MC1776	† Motorola	
	MC1776C	Motorola	
	MC3476	Motorola	
	LM4250	† National	
	LM4250C	National	
	CA3078	† RCA	
	CA3078A	† RCA	
	CA3094	† RCA	
	CA3094A	† RCA	20
	CA3094B	† RCA	
	CA6078A	† RCA	
	SG1250	† Silicon G	
	SG2250	Silicon G	
	SG3250	Silicon G	
	SG4250	† Silicon G	
	SG4250C	Silicon G	
	UC4250	† Solitron	
	UC4250C	Solitron	
Non-Adjustable			
45			
	OP-20B	† PMI	
	OP-20C	† PMI	
	OP-20F	PMI	
	OP-20G	PMI	
	OP-20H	PMI	
125			
	LH0001	National	
150			
	HA-2700	**Harris** (988)	40
	HA-2704	**Harris** (988)	
	HA-2705	**Harris** (988)	
200			
	TL061	TI	
See TL061 series			
600			
	AD108	† AD	
	LM108	† AMD	
	LM112	† AMD	
	LM212	AMD	50
	µA108	† Fairchild	
	108	† Intersil	
	LM108	† Motorola	
	LM108	**† National** (1035)	
	LM112	† National	
	LM212	National	
	LM216A	National	
	LM316A	National	
	SFC2108	NPC	
	OP-08	† PMI	60
	OP-12	† PMI	
	PM108	† PMI	
	LM108	Raytheon	
	LM108	† Signetics	
	SG108	Silicon G	

See corresponding 108A, 208A, and 308A series as well

Programmable

Adjustable Current/Performance

Single (1 unit per package)

Function	Device	Source	Line
	µA776C	Fairchild	70
	µA776M	† Fairchild	
	HA-2720	**† Harris** (990)	
	HA-2725	**Harris** (990)	
	4250	Intersil	
	4250C	Intersil	
	ICL8021C	Intersil	
	ICL8021M	† Intersil	
	MC1776	† Motorola	
	MC1776C	Motorola	
	MC3476	Motorola	80
	LM4250	† National	
	LM4250C	National	
	CA3078	RCA	
	CA3078A	† RCA	
	CA3080	RCA	
	CA3080A	† RCA	
	CA3094	† RCA	
	CA3094A	† RCA	
	CA3094B	† RCA	
	SG1250	† Silicon G	90
	SG2250	Silicon G	
	SG3250	Silicon G	
	SG4250	† Silicon G	
	SG4250C	Silicon G	
	TL066	TI	
Dual (2 units per package)			
	HA-2730	**† Harris** (993)	
	HA-2735	**Harris** (993)	
	ICL8022C	Intersil	
	ICL8022M	† Intersil	100
	LH24250	† National	
	LH24250C	National	
Triple (3 units per package)			
	ICL8023C	Intersil	
	ICL8023M	† Intersil	
	CA3060	RCA	
	CA3060	† RCA	
	CA3060A	RCA	
	CA3060B	RCA	
	L144A	† Siliconix	110
	L144B	Siliconix	
	L144C	Siliconix	
	SL144	Siltronics	
Quad (4 units per package)			
	XR146	**† Exar** (929)	
	XR246	**Exar** (929)	
	XR346	**Exar** (929)	
	XR4202	**Exar** (930)	
	XR4202M	**† Exar** (930)	
	MC3474	Motorola	120
	MC3475	Motorola	
	MC3575	† Motorola	
	LM146	**† National** (1035)	
	LM246	National	
	LM346	National	

Single Supply

Single (1 unit per package)

Supply Voltage	Device	Source	Line
5 to 16			
	OP-20B	† PMI	
	OP-20C	† PMI	
	OP-20F	PMI	130
	OP-20G	PMI	
	OP-20H	PMI	
	CA3130	† RCA	
	CA3130A	† RCA	
	CA3130B	† RCA	
to 24			
	CA3094	† RCA	
to 36			
	µA759	† Fairchild	
	µA759C	Fairchild	140
	CA3140	Intersil	
	CA3140	RCA	
	CA3094A	† RCA	
to 44			
	CA3140B	† Intersil	
	CA3140B	† RCA	
	CA3094B	† RCA	
Dual (2 units per package)			
10 to 16			
	DA-101	Delco	150
3 to 26			
	LM2904	Motorola	
	LM2904	National	
	CA2904	RCA	
	LM2904	TI	
3 to 30			
	LM158	† Motorola	
	LM258	Motorola	
	LM358	Motorola	
	LM158	† National	160
	LM258	National	
	LM358	National	
	LM158A	† National	
	LM258A	National	
	LM358A	National	
	CA158	† RCA	
	CA258	RCA	
	CA358	RCA	
	LM158	† Signetics	
	LM258	Signetics	170
	LM358	Signetics	
	NE532	**† Signetics** (1109)	
	SA532	Signetics	
	SE532	**Signetics** (1109)	
	LM158	† TI	
	LM258	TI	
	LM358	TI	
3 to 36			
	µA798	Fairchild	
	MC3458	Motorola	180
4 to 36			
	CA3240	RCA	
8 to 36			
	TBA231	SGS	
Quad (4 units per package)			
4 to 18			
	µA3401C	Fairchild	
	LM3401	National	
	MC3401	Motorola	
	CA3401	† RCA	190

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Values

Bold face indicates additional data is provided on the page noted.

LINEAR–Operational Amplifiers (Cont'd)

Single Supply (Cont'd.)

Supply Voltage	Device	Source	Line
4 to 18		(Cont'd.)	
	RC3401	Raytheon	
3 to 26			
	HA17902	Hitachi	
	LM2902	Motorola	
	LM2902	National	
4 to 28			
	µA3301C	Fairchild	
	MC3301	Motorola	
	LM3301	National	10
	RC3301	Raytheon	
3 to 30			
	LM124	† AMD	
	LM224	AMD	
	LM324	AMD	
	µA124	† Fairchild	
	µA224	Fairchild	
	µA324	Fairchild	
	LM124	† Intersil	
	LM224	Intersil	20
	LM324	Intersil	
	LM124	† Motorola	
	LM224	Motorola	
	LM324	Motorola	
	LM124	**† National (1035)**	
	LM224	National	
	LM324	National	
	µPC224	NEC America	
	µPC324	NEC America	
	CA124	† RCA	30
	CA224	RCA	
	CA324	RCA	
	LM124	† Raytheon	
	LM224	Raytheon	
	LM324	Raytheon	
	LM124	† Signetics	
	LM224	Signetics	
	LM324	Signetics	
	SA534	Signetics	
	SG124	† Silicon G	40
	SG224	Silicon G	
	SG324	Silicon G	
	LM124	† TI	
	LM224	TI	
	LM324	TI	
	TL321C	TI	
	TL321M	† TI	
3 to 32			
	LM2902	Motorola	
	LM2902	Raytheon	50
	RC4137	Raytheon	
	RM4137	† Raytheon	
	RV4137	Raytheon	
	LM2902	Signetics	
	LM2902	TI	
4 to 32			
	LM2900	National	
	LM3900	**National (1035)**	
	LM2900	Raytheon	
	LM3900	Raytheon	60
	LM2900	TI	
	LM3900	TI	
3 to 36			
	XR3303	Exar	
	XR3403	Exar	
	XR3503M	† Exar	
	µA3303C	Fairchild	

(Continued)

Single Supply (Cont'd.)

Supply Voltage	Device	Source	Line
3 to 36		(Cont'd.)	
	µA3403C	Fairchild	
	µA3503M	† Fairchild	70
	MC3303	Motorola	
	MC3403	Motorola	
	MC3503	† Motorola	
	RC3403	Raytheon	
	RM3503	† Raytheon	
	RV3403	Raytheon	
	MC3403C	TI	
	MC3503	† TI	
4 to 36			
	LM1900	National	80
	LM1900	Raytheon	
	LM1900	TI	

Wide Band

Unity Gain Bandwidth MHz	Device	Source	Line
500*			
	1435	† Teledyne P	
300			
	9914	OEI	
200			
	9916	† OEI	
100			
	AM-500GC	**Datel (691)**	90
	AM-500MC	**† Datel (691)**	
	9906	OEI	
	9908	† OEI	
	9909	OEI	
	9912	OEI	
	NE5539	Signetics	
70*			
	3554A	**Burr-Brown (920)**	
	3554B	**Burr-Brown (920)**	
	3554S	† Burr-Brown	100
	LH0024	† National	
	LH0024C	National	
	LH0032	† National	
	LH0032C	National	
65*			
	µA715C	Fairchild	
	µA715M	† Fairchild	
	HA17715	Hitachi	
60*			
	9912	† OEI	110
	1430	Teledyne P	
50*			
	3551J	**Burr-Brown (920)**	
	3551S	**† Burr-Brown (920)**	
	CA3015	† RCA	
	CA3015A	† RCA	
	CA3016	† RCA	
	CA3016A	† RCA	
	CA3030	RCA	
	CA3030A	RCA	120
	CA3038	† RCA	
	CA3038A	† RCA	
40			
	9932	OEI	
38*			
	CA3100	† RCA	
35*			
	AD507J	AD	
	AD507K	AD	
	AD507S	† AD	130
	9917	OEI	
30*			
	µA702C	Fairchild	
	µA702M	† Fairchild	
	MC1712	Motorola	
	LH0003	† National	
	LH0003C	National	
	LH0005	† National	
	LH0005A	National	
	LH0005C	† National	140
	µPC51A	NEC America	
	µPC702	NEC America	
	SL702C	Plessey	
	RC702	Raytheon	
	RM702	† Raytheon	
	TL702M	† TI	
	TL702C	TI	
	µA702M	† TI	

† Military Temperature Range (−55° to 125°C)

* Typical Values

LINEAR–Operational Amplifiers-Characteristics

Single Units

In this list the "Comp." column indicates the number of compensation components required at unity gain. Thus 0 indicates a fully compensated amplifier. The bandwidth and slew rate are listed with the amplifier compensated for unity gain.

Offset Voltage mv (25°C)	Bias Current na. (25°C)	Offset Current na. (25°C)	Voltage Drift µv/°C	Band-width MHz	Slew Rate v/µs	Voltage Gain v/v	CMRR db	Comp.	Comments	Device	Source
0.020*	0.15*	0.05*	0.1	3*	2.5*	1M	120	3	Chopper Stabilized	**AM-490-2C**	**Datel (690)**
			0.3	3*	2.5*	1M	120	3	Chopper Stabilized	**AM-490-2B**	**Datel (690)**
			0.6	3*	2.5*	1M	120	3	Chopper Stabilized	**AM-490-2M**	**† Datel (690)**
			1.0	3*	2.5*	1M	120	3	Chopper Stabilized	**AM-490-2A**	**Datel (690)**
0.025	1	0.25	0.5	0.25*	0.1*	1M	110	0	Ultra Low Offset Voltage, Low Drift	AD517L	AD
	2	2	0.6	1.2*	0.25*	300K	110	0	Ultra Low Offset Voltage. Low Drift	µA714A OP-07A	† Fairchild † PMI
	10	2.5	2	0.3*	0.1*	1M	110	0	Trimmed Offset	AD510L	AD
	15	2.5	0.5	0.4*	0.06*	1M	120	1	Precision, Low Noise	**LH0044A** **LH0044AC**	**† National (1073)** **National (1073)**
	20	20	0.75	—	—	5-1000	100	0	Instrumentation (2 amps available as pair)	**3629B**	**† Burr-Brown (920)**
	25	30	0.5	—	—	5-1000	100	0	Instrumentation(2 amps available as pair)	3629S **3629C**	† Burr-Brown **Burr-Brown (920)**
	35	50	3	—	—	5-1000	100	0	Instrumentation (2 amps available as pair)	**3629A**	**Burr-Brown (920)**
0.05	0.050	0.0005*	75*	1*	6*	20K	70	0	FET	3540J	† Burr-Brown
	1	0.5	0.4	3*	2.5*	10M	130	3	Chopper Stabilized	**HA-2904**	**Harris (996)**
	2	0.75	1	0.25*	0.1*	1M	100	0	Ultra Low Offset Voltage, Low Drift	AD517K AD517S	AD † AD
	13	4.0	1	0.3	0.1*	1M	110	0	Trimmed Offset	AD510K AD510S	AD † AD
	30	5	0.5	0.4*	0.06*	500K	114	1	Precision, Low Noise	**LH0044B**	**National (1073)**
			1	0.4*	0.06*	500K	114	1	Precision, Low Noise	**LH0044**	**† National (1073)**
0.06	1	0.5	0.6	3*	2.5*	1M	120	3	Chopper Stabilized	**HA-2900**	**† Harris (996)**
	15	10	0.5	0.4*	0.5	1M	110	1	Low Drift	**3510C**	**Burr-Brown (920)**
0.075	3	2.8	1.3	1.2*	0.25*	200K	110	0	Ultra Low Offset Voltage, Low Drift	µA714 OP-07	† Fairchild † PMI
	4	3.8	1.3	1.2*	0.25*	200K	106	0	Ultra Low Offset Voltage, Low Drift	µA714E OP-07E	Fairchild PMI
0.08	1	0.5	0.2*	3*	2.5*	1M	120	3	Chopper Stablilized	**AM-490** **HA-2905** 1340	**Datel (690)** **Harris (996)** Teledyne P
	15	0.5	1.5	0.1*	—	1M	105	0	Precision, Low Power	OP-20B OP-20F	† PMI PMI
0.10	25	5	3	3*	0.1*	250K	94	0	Trimmed Offset	AD510J	AD
	35	5	1	0.4*	0.06*	500K	114	1	Precision, Low Noise	**LH0044C**	**National (1073)**
	70	1	0.6	—	—	1M	120	4	Instrumentation	SSS725A	† PMI
			0.8	—	—	1M	120	4	High Performance 725	SSS725A	† AMD
0.12	25	15	1	0.4*	0.5	1M	110	1	Low Drift	**3510B** **3510S**	**Burr-Brown (920)** **† Burr-Brown (920)**
0.15	2	0.2	2.5	0.8*	0.12*	80K	104	0	Improved 108A, low bias, compensated	OP-12A OP-12E	† PMI PMI
								1	Improved 108A, low bias	OP-08A OP-08E	† PMI PMI
		2	0.9	1.2*	0.25*	300K	114	0	Instrumentation	OP-05A	† PMI
	5	1	3	0.25*	0.1*	1M	94	0	Ultra Low Offset Voltage, Low Drift	AD517J	AD
	7	6	1.8	1.2*	0.25*	120K	100	0	Ultra Low Offset Voltage, Low Drift	µA714C	Fairchild

(Continued)

† Military Temperature Range (−55° to 125°C) * Typical Values

Bold face indicates additional data is provided on the page noted.

LINEAR–Operational Amplifiers-Characteristics (Cont'd)

Offset Voltage mv (25°C)	Bias Current na. (25°C)	Offset Current na. (25°C)	Voltage Drift µv/°C	Band-width MHz	Slew Rate v/µs	Voltage Gain v/v	CMRR db	Comp.	Comments	Device	Source
Single Units											**(Cont'd.)**
0.15	7	6	1.8	1.2*	0.25*	120K	100	0	Ultra Low Offset Voltage, Low Drift		(Cont'd.)
										OP-07C	PMI
	12	6	2.5	1.2*	0.25*	120K	94	0	Ultra Low Offset, Low Drift	OP-07D	PMI
	35	20	2	0.4*	0.5	1M	110	1	Low Drift	**3510A**	**Burr-Brown (920)**
0.20	15	10	2	0.3*	0.1*	1-1000	80	0	Instrumentation	AD522B	AD
	18	08	3.0	0.1*	—	800K	100	0	Precision, Low Power	OP-20C	†PMI
										OP-20G	PMI
	25	20	6	0.3*	0.1*	1-1000	75	0	Instrumentation	AD522S	†AD
0.25	0.00015	0.00004	5	0.5*	0.3	—	80	—	Ultra Low Bias FET	**3528B**	**Burr-Brown (920)**
	0.001	0.0005	3	0.7*	0.3	40K	76	0	Precision, Low Drift FET	AD545M	AD
	0.002	0.0003*	5	1*	0.6	100K	76*	0	Low Drift FET	**3527B**	**Burr-Brown (920)**
	0.005	0.0003*	2	1*	0.6	100K	76*	0	Ultra Low Drift FET	**3527C**	**Burr-Brown (920)**
	0.010	0.002*	1	1.5*	0.6	100K	90*	0	Ultra Low Drift FET	**3521L**	**Burr-Brown (920)**
	0.015	0.002*	2	1.5*	0.6	100K	90*	0	Ultra Low Drift FET	**3521K**	**Burr-Brown (920)**
	0.020	0.020*	5	1.5*	0.6	50K	90*	0	Ultra Low Drift FET	**3521J**	**Burr-Brown (920)**
										3521R	**†Burr-Brown (920)**
0.30	2	0.2	3.5	0.8*	0.12*	80K	104	0	Improved 108A, low power, compensated		
										OP-12B	†PMI
										OP-12F	PMI
								1	Improved 108A, low power	OP-08B	†PMI
										OP-08F	PMI
	25	2	5	0.1*	—	500K	90	0	Precision, Low Power	OP-20H	PMI
0.40	25	20	6	0.3*	0.1*	1-1000	75	0	Instrumentation	AD522A	AD
0.5	0.000075	0.00002	10	0.5*	0.3	—	70	—	Ultra Low Bias FET	**3528C**	**Burr-Brown (920)**
	0.0001	0.00005	25	1*	0.6	100K	80*	0	Ultra Low Bias FET	**3523L**	**Burr-Brown (920)**
	0.00025	0.0001	25	1*	0.6	100K	80*	0	Ultra Low Bias FET	**3523K**	**Burr-Brown (920)**
	0.0003	0.00008	10	0.5*	0.3	—	66	—	Ultra Low Bias FET	**3528A**	**Burr-Brown (920)**
	0.001	0.0001	5	1*	1.5	100K	80	0	Precision FET	**LH0052**	**†National (1073)**
		0.0005	5	0.7*	0.3	40K	76	0	Precision, Low Drift FET	AD545L	AD
	0.005	0.001*	25	1*	0.6	50K	90*	0	Low Offset FET	**3522K**	**Burr-Brown (920)**
										3522S	**Burr-Brown (920)**
		0.0003*	10	1*	0.6	100K	76*	0	Low Drift FET	**3527A**	**Burr-Brown (920)**
	0.020	0.002*	10	1.5*	0.6	50K	90*	0	Ultra Low Drift FET	**3521H**	**Burr-Brown (920)**
	0.025	0.010	5	1.0*	3	200K	80	0	Precision Bipolar JFET	AD542L	AD
	0.050	0.01	5	2.5*	3	50K	95	0	Precision Bipolar JFET	LFT155	†National
										LFT355	National
				4	10	50K	95	0	Precision Wideband JFET	LFT156	†National
										LFT356	National
				14*	10	100K	86	0	Bipolar-JFET, bias comp.	OP-15A	†PMI
										OP-15E	PMI
				19*	18	100K	86	0	Wideband-JFET, bias comp.	OP-16A	†PMI
										OP-16E	PMI
				—	45	100K	86	—	Wideband, Decompensated, Settles to 0.01% in 1.5 µs		
										OP-17A	†PMI
										OP-17E	PMI
			5*	0.8*	40	60K	86	1	Wideband-JFET, Comp. for G>10	**HA-5110-2**	**†Harris (1008)**
				18*	12*	75K	86	0	Wideband-JFET	**HA-5100-2**	**†Harris (1006)**
										HA-5100-5	**Harris (1006)**
			10*	0.8*	40	60K	86	1	Wideband-JFET, Comp. for G>10	**HA-5110-5**	**Harris (1008)**
	0.2	0.1	10*	3*	13*	50K	70	0	Low Offset JFET	TL087M	†TI
	0.4	0.05	10*	3*	13*	25K	70	0	Low Offset JFET	TL087C	TI

(Continued)

† Military Temperature Range (−55° to 125°C) * Typical Values

LINEAR–Operational Amplifiers-Characteristics (Cont'd)

Offset Voltage mv (25°C)	Bias Current na. (25°C)	Offset Current na. (25°C)	Voltage Drift µv/°C	Band-width MHz	Slew Rate v/µs	Voltage Gain v/v	CMRR db	Comp.	Comments	Device	Source
Single Units											**(Cont'd.)**
0.5											(Cont'd.)
	2	0.2	5	1*	0.3*	80K	96	1	Precision Bipolar, Low Bias	LM108A	† AMD
										LM208A	AMD
										AD108A	† AD
										AD208A	AD
										µA108AM	† Fairchild
										µA208AM	Fairchild
										108A	† Intersil
										208A	Intersil
										LM108A	† Motorola
										LM208A	Motorola
										LM108A	**† National (1035)**
										LM208A	National
										SFC2108A	† NPC
										SFC2208A	NPC
										PM108A	† PMI
										PM208A	PMI
										LM108A	† Raytheon
										LM208A	† Raytheon
										LM108A	† Signetics
										LM208A	Signetics
										SG108A	† Silicon G
										SG208A	Silicon G
				0.3*	0.1	80K	96	0	Compensated 108A	SG1118A	† Silicon G
										SG2118A	Silicon G
	3	2.8	2	1.2*	0.25*	200K	114	0	Instrumentation	OP-05	† PMI
	4	3.8	2	1.2*	0.25*	200K	110	0	Instrumentation	OP-05E	PMI
	7	1	5	1*	0.3*	80K	96	1	Precision Bipolar	LM308A	AMD
										AD308A	AD
										µA308AC	Fairchild
										308A	Intersil
										LM308A	Motorola
										LM308A	National
										PM308A	PMI
										LM308A	Raytheon
										LM308A	Signetics
										SG308A	Silicon G
				0.3*	0.1	80K	96	0	Compensated 308A	SG3118A	Silicon G
	30	5	5	1*	0.25*	80K	90	1	High Accuracy 301	AD301AL	AD
	35	2	8	0.8	0.25	100K	90	0	General Purpose	OP-02A	† PMI
										OP-02E	PMI
	50	5	5	1*	0.5*	50K	90	0	Higher Accuracy 741	AD741L	AD
		30	1	1.5*	0.8	100K*	100*	0	Low Drift	**3500E**	**Burr-Brown (920)**
	75	5	2	1	0.005*	1000K	110	4	High Accuracy Instrumentation	µA725AM	† Fairchild
	80	5	0.6	—	—	1000K	120	4	Instrumentation	SSS725E	PMI
			1	—	—	1000K	120	4	Instrumentation	SSS725	PMI
		10	0.5	0.3*	0.12*	1000K	110	1	Precision Low Noise	AD504M	AD
			1.0	0.3*	0.12*	1000K	110	1	Precision Low Noise	AD504L	AD
										AD504S	† AD
	500	200	15	0.3	—	—	72	0	Instrumentation	HC3020	HyComp
0.7	30	2	5	2.5*	18*	50K	90	0	High Speed	MP5501A	Micro Power
										MP5501H	† Micro Power
										OP-01	† PMI
										OP-01H	PMI
0.75	80	5	1	—	—	1000K	110	4	Instrumentation	SSS725B	PMI
			2.8*	—	—	1000K	110	4	High Performance 725	SSS725B	AMD
			—	1*	0.3*	50K	80	0	High Performance	µA741AM	† Fairchild
				0.44	0.3	50K	80	0	High Performance	µA741EC	Fairchild
1.0	0.000075	—	25	0.35	0.3	50K	70	0	FET Electrometer	AD515L	AD

(Continued)

† Military Temperature Range (−55° to 125°C) * Typical Values

Bold face indicates additional data is provided on the page noted.

LINEAR–Operational Amplifiers-Characteristics (Cont'd)

Offset Voltage mv (25°C)	Bias Current na. (25°C)	Offset Current na. (25°C)	Voltage Drift µv/°C	Band-width MHz	Slew Rate v/µs	Voltage Gain v/v	CMRR db	Comp.	Comments	Device	Source
Single Units											**(Cont'd.)**
1.0											(Cont'd.)
	0.00015	—	15	0.35	0.3	100K	80	0	FET Electrometer	AD515K	AD
	0.0005	0.0002	50	1*	0.6	100K	80*	0	Ultra Low Bias FET	**3523J**	**Burr-Brown (920)**
	0.005	0.0002	10	1*	1	75K	76	0	Precision FET	**LH0052C**	**National (1073)**
	0.001	0.0005	15	0.7*	0.3	40K	70	0	Precision Low Drift FET	AD545K	AD
	0.002	0.001	25	0.7*	0.3	20K	66	0	Precision Low Drift FET	AD545J	AD
	0.005	0.002	25	4*	3	25K	80*	0	General Purpose FET	ADM501C	AD
				1	3	50K	70		Low Bias Current, FET	1425-01	Teledyne P
		0.002*	10	1	3	50K	70	0	Low Bias Current, FET	1425-02	Teledyne P
		—	10	1*	3	75K	80	0	High Accuracy, FET	AD506L	AD
	0.010	0.002*	50	1*	0.6	50K	90*	0	Low Offset FET	**3522J**	**Burr-Brown (920)**
		0.005*	25	1	3	50K	70		Low Drift, FET	1426-01	Teledyne P
				10*	65	25K	70*	0	Fast Settling, 1 µs to 0.01%	**3550J**	**Burr-Brown (920)**
										3550S	**† Burr-Brown (920)**
				20*	100	25K	70*	0	Fast Settling, 0.6 µs to 0.01%	**3550K**	**Burr-Brown (920)**
		—	25	4*	3	25K	80*	0	General Purpose FET	ADM501B	AD
	0.015	—	25	10*	50	50K	80	0	Fast Wide band, High Accuracy, FET Input	AD528K	AD
										AD528S	† AD
	0.025	0.01	10	1.0*	3	50K	76	0	Precision Bipolar JFET	AD542S	† AD
						200K	80	0	Precision Bipolar JFET	AD542K	AD
		0.01*	5	1	3	50K	70	0	Low Drift, FET	1426-03	Teledyne P
			10	1	3	50K	70	0	Low Drift, FET	1426-02	Teledyne P
	0.050	0.01	15	70	1000	100K	44	1	150ns Settling to 0.05%	**3554B**	**Burr-Brown (920)**
			25	70	1000	100K	44	1	150ns settling to 0.05%	3554S	† Burr-Brown
	0.10	0.01	50	50*	250*	100K	70*	1	Wideband, Fast Settling	**3551J**	**Burr-Brown (920)**
										3551S	**† Burr-Brown (920)**
		0.02	10	13*	7.5	75K	86	0	Bipolar-JFET, bias comp.	OP-15B	† PMI
										OP-15F	PMI
				18*	12	75K	86	0	Wideband-JFET, bias comp.	OP-16B	† PMI
										OP-16F	PMI
				—	35	75K	86	—	Wideband, Decompensated, Settles to 0.01% in 1.5 µs	OP-17B	† PMI
										OP-17F	PMI
		0.05	5*	18*	12*	60K	80	0	Wideband-JFET	**HA-5105-5**	**Harris (1006)**
		0.05*	15*	0.6*	35*	50K	80	1	Wideband-JFET, Comp. for G>10	**HA-5115-5**	**Harris (1008)**
	5	0.5	10	0.8*	0.12*	40K	84	0	Precision, low input current	OP-12C	† PMI
										OP-12G	PMI
								1	Precision, low input current	OP-08C	† PMI
										OP-08G	PMI
	15	7*	3	1.5*	1	45K	100*	0	Low Bias, Low Noise	**3500C**	**Burr-Brown (920)**
			5	1.5*	1	45K	100*	0	Low Bias, Low Noise	**3500T**	**† Burr-Brown (920)**
		7	—	—	1.5*	50K	—	0	Low Input Bias, High Slew Rate	ULS-2171	† Sprague
	100	20	4*	1*	0.25*	25K	70	2	General Purpose, Low Quiescent Power	LH0001	† National
						30K	70	2	High Voltage	LH0004	† National
			5	1*	0.005*	1000K	110	4	High Accuracy Instrumentation	µA725M	† Fairchild
										LM725	† National
				0.5*	0.01*	1000K	110	4	Instrumentation	RM725	† Raytheon
				—	—	1000K	110	4	Instrumentation	725	† AMD

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Values

LINEAR–Operational Amplifiers-Characteristics (Cont'd)

Offset Voltage mv (25°C)	Bias Current na. (25°C)	Offset Current na. (25°C)	Voltage Drift µv/°C	Band-width MHz	Slew Rate v/µs	Voltage Gain v/v	CMRR db	Comp.	Comments	Device	Source
Single Units											**(Cont'd.)**
1.0	100	20	5	—	—	1000K	110	4	Instrumentation		(Cont'd.)
										µPC154	NEC America
										PM725	† PMI
	200	50	6	1*	0.4*	25K	80	3	General Purpose	RM709A	† Raytheon
	250	70	20	—	—	20K	70	1	General Purpose	TA7502B	Toshiba
1.3	7	6	4.5	1.2*	0.25*	120K	100	0	Instrumentation	OP-05C	PMI
							120	0	Instrumentation	µPC254	NEC America
	110	13	4.5	—	—	500K	100	4	Instrumentation	SSS725C	PMI
1.5	0.010	—	25	1*	3	50K	80	0	High Accuracy, FET	AD506K	AD
			50	1*	3	50K	80	0	High Accuracy, FET	AD506S	† AD
	80	5	2	—	—	1000K	120	4	High Performance 725	SSS725	† AMD
				0.5*	0.005*	1000K	120	4	Instrumentation	LM725A	† National
			2*	—	—	1000K	120	4	High Performance 725	SSS725E	AMD
	100	15	3	0.3*	0.12*	500K	100	1	Low Drift, Low Noise	AD504K	AD
	120	45	4*	1*	0.25*	30K	70	2	High Voltage	LH0004C	National
2.0	0.010	0.0005*	15	1*	3	50K	70	0	Low Offset Voltage, FET	ICL8007M-2	† Intersil
		0.005*	50	1	3	50K	70	—	Low Bias Current, FET	1425	Teledyne P
		—	75	4*	3	25K	80*	0	General Purpose FET	ADM501	AD
										ADM506	AD
	0.020	0.010	15	4*	10*	50K	86	1	MOS FET, Single Supply, Strobe	CA3130B	† RCA
						100K	86	0	MOS FET Single Supply, Strobe	CA3160B	† RCA
	0.025	0.01*	50	1	3	100K	72		Low Drift, FET	1426	Teledyne P
	0.025*	0.010*	20	1.0*	3	50K	76	0	Precision Bipolar JFET	AD542J	AD
	0.030	0.01	5*	4.5*	9*	50K	86	0	MOS FET, Single Supply	CA3140B	† Intersil
										CA3140B	† RCA
	0.050	0.01	5	2.5*	3	50K	85	0	Bipolar - JFET	LF155A	† AMD
										LF355A	AMD
										µAF155A	† Fairchild
										µAF355A	Fairchild
										LF155A	† Intersil
										LF355A	Intersil
										LF155A	† Motorola
										LF355A	Motorola
										PM155A	† PMI
										PM355A	PMI
										LF155A	**† National (1035)**
										LF355A	National
										LF155A	† Raytheon
										LF355A	Raytheon
										LF155A	† Signetics
										LF355A	Signetics
										LF155A	† TI
										LF355A	TI
				4	10	50K	85	0	Wideband - JFET	LF156A	† AMD
										LF356A	AMD
										µAF156A	† Fairchild
										µAF356A	Fairchild
										LF156A	Intersil
										LF356A	Intersil
										LF156A	† Motorola
										LF356A	Motorola
										LF156A	**† National (1035)**
										LF356A	**National (1035)**
										PM156A	† PMI
										PM356A	PMI
										LF156A	† Raytheon
										LF356A	Raytheon
										LF156A	† Signetics
										LF356A	Signetics

(Continued)

† Military Temperature Range (−55° to 125°C) * Typical Values

Bold face indicates additional data is provided on the page noted.

LINEAR–Operational Amplifiers-Characteristics (Cont'd)

Offset Voltage mv (25°C)	Bias Current na. (25°C)	Offset Current na. (25°C)	Voltage Drift µv/°C	Band-width MHz	Slew Rate v/µs	Voltage Gain v/v	CMRR db	Comp.	Comments	Device	Source
Single Units											**(Cont'd.)**
2.0	0.050	0.01	5	4	10	50K	85	0	Wideband - JFET		(Cont'd.)
										LF156A	† TI
										LF356A	TI
				—	40	50K	85	—	Wideband Decompensated	LF157A	† AMD
										LF357A	AMD
										µAF157A	† Fairchild
										µAF357A	Fairchild
										LF157A	† Intersil
										LF357A	Intersil
										LF157A	† Motorola
										LF357A	Motorola
										LF157A	**† National (1035)**
										LF357A	National
										PM157A	† PMI
										PM357A	PMI
										LF157A	† Raytheon
										LF357A	Raytheon
										LF157A	† Signetics
										LF357A	Signetics
										LF157A	† TI
										LF357A	TI
			50	70	1000	100K	44	1	150ns Settling to 0.05%	**3554A**	**Burr-Brown (920)**
	0.10	0.050	10*	3*	13*	50K	80	0	Bipolar FET	**µA771A**	**† Fairchild (938)**
		0.05	10*	4*	13*	50K	80	0	Wideband Bipolar JFET	**LF351A**	**National (1035)**
		0.05*	40	0.5*	3	50K	80	1	High Current, High Power	**3571A**	**Burr-Brown (920)**
										3572A	**Burr-Brown (920)**
	0.50	—	75	60*	500	200K	—	0	Inverting, Settles to 0.01% in 200 ns		
										1430	Teledyne P
	2	0.2	15	1*	0.2*	50K	85	0	Micropower, Supply Current 600 µa	LM112	† AMD
										LM212	AMD
										LM112	† National
										LM212	National
					0.1*	50K	85	0	Compensated 108/208	SG1118	† Silicon G
										SG2118	Silicon G
					0.3*	50K	85	1	Precision Bipolar	LM108	† AMD
										LM208	AMD
										AD108	† AD
										AD208	AD
										µA108M	† Fairchild
										µA208M	Fairchild
										108	† Intersil
										208	Intersil
										LM108	† Motorola
										LM208	Motorola
										LM108	**† National (1035)**
										LM208	National
										SFC2108	† NPC
										SFC2208	NPC
										PM108	† PMI
										PM208	PMI
										LM108	† Raytheon
										LM208	Raytheon
										LM108	† Signetics
										LM208	Signetics
										SG108	† Silicon G
										SG208	Silicon G
				0.3*	0.3*	50K	85	1	Low Noise 108	108LN	† Intersil
	3	2	10	0.5*	0.1	45K	100*	0	Low Bias Current	**3501C**	**Burr-Brown (920)**
	5	0.5	10	—	1.7*	2.5K	80	3	Wideband	µA702M	† TI
	7	3	10	0.5*	0.1	45K	100*	0	Low Bias Current	**3501B**	**Burr-Brown (920)**
										3501S	**† Burr-Brown (920)**

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Values

LINEAR–Operational Amplifiers-Characteristics (Cont'd)

Offset Voltage mv (25°C)	Bias Current na. (25°C)	Offset Current na. (25°C)	Voltage Drift µv/°C	Band-width MHz	Slew Rate v/µs	Voltage Gain v/v	CMRR db	Comp.	Comments	Device	Source
Single Units											**(Cont'd.)**
2.0											(Cont'd.)
	15	5	3	3	1.5	40K	80	0	High Performance, High Gain	MC1556	† Motorola
										RM1556A	† Raytheon
	20	10*	5	1.5*	1	45K	100*	0	Low Bias, Low Noise	**3500B**	**Burr-Brown (920)**
			10	1.5*	1	45K	100*	0	Low Bias, Low Noise	**3500S**	**† Burr-Brown (920)**
	25	3	15	0.5	0.5*	50K	80	1	Low Offset Current	µA777M	† Fairchild
										µA777M	† TI
	50	5	8	2.5*	18*	50K	80	0	High Speed	MP5501E	Micro Power
										MP5501F	† Micro Power
										OP-01E	PMI
										OP-01F	† PMI
			10	0.8	0.25	50K	90	0	General Purpose	OP-02	† PMI
										OP-02C	PMI
			15	1*	0.4	50K	80	0	High Performance, Low Drift	1319-01	† Teledyne P
			—	—	—	100K	80	0	High Performance 741	SSS741	† AMD
										SSS741	† PMI
					0.6*	50K	—	0	General Purpose	ULS-2151	† Sprague
		10	15	4*	1.5	25K	80	0	High Performance, High Gain	RM4131	† Raytheon
		50	25	1*	0.4	50K	80	0	High Performance, Low Drift	1319	Teledyne P
	60	10	15	3*	25	50K	70	0	High Slew Rate	SE530	† Signetics
				—	10	50K	70	0	High Slew Rate	SE535	† Signetics
					40	50K	70	1	60V/µs Comp. for g=5	SE538	† Signetics
	75	10	15	1*	0.5*	50K	80	0	General Purpose, Compensated	LM107	† AMD
										LM207	AMD
										µA107M	† Fairchild
										µA207M	Fairchild
										107	† Intersil
										207	Intersil
										LM107	† Motorola
										LM207	Motorola
										LM107	† National
										LM207	National
										SFC2107	† NPC
										SFC2207	NPC
										LM107	† Raytheon
										LM207	Raytheon
										CA107	† RCA
										CA207	RCA
										LM107	† Signetics
										LM207	Signetics
										SG107	† Silicon G
										SG207	Silicon G
										LM107	† TI
										LM207	TI
									Higher Accuracy 741	AD741S	† AD
							90	0	Higher Accuracy 741C	AD741K	AD
							80	1	General Purpose, Improved 101, Uncompensated		
										AD101A	† AD
										AD201A	AD
										LM101A	† AMD
										LM201A	AMD
										µA101AM	† Fairchild
										µA201AM	Fairchild
										101A	† Intersil
										201A	Intersil
										LM101A	† Motorola
										LM201A	Motorola
										LM101A	**† National (1035)**
										LM201A	National
										LM101A	† Raytheon

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Values

Bold face indicates additional data is provided on the page noted.

LINEAR–Operational Amplifiers-Characteristics (Cont'd)

Offset Voltage mv (25°C)	Bias Current na. (25°C)	Offset Current na. (25°C)	Voltage Drift µv/°C	Band-width MHz	Slew Rate v/µs	Voltage Gain v/v	CMRR db	Comp.	Comments	Device	Source
Single Units											**(Cont'd.)**
2.0	75	10	15	1*	0.5*	50K	80	1	General Purpose, Improved 101, Uncompensated		
											(Cont'd.)
										LM201A	Raytheon
										CA101A	†RCA
										CA201A	RCA
										LM101A	† Signetics
										LM201A	Signetics
										SG101A	† Silicon G
										SG201A	Silicon G
										LM101A	†TI
										LM201A	TI
				0.8*	0.5*	50K	80	1	Low Noise 101A	101ALN	† Intersil
		—	15*	4*	120	100K	—	0	High Speed Inverting	AD505J	AD
	200	50	10	5*	0.3*	25K	80	3	General Purpose	µA709AM	† Fairchild
										MC1709A	† Motorola
										LM709A	**† National (1035)**
										SFC2709A	†NPC
										µA709A	† Signetics
										µA709AM	†TI
	800	200	—	10*	6*	50K	80	1	Wideband, low noise	SE5334	† Signetics
										SE5334A	† Signetics
	4000	1500	1.2*	15*	3*	0.7K	70	1	6 Volt, Wideband	CA3008A	RCA
										CA3010A	†RCA
										CA3029A	RCA
										CA3037A	†RCA
	5000	500	2.5*	7*	1.5*	2.5K	80	2	Wideband	MC1712	† Motorola
			10	30*	3.5*	2.5K	80	3	Wideband	µA702M	† Fairchild
										RM702	† Raytheon
										µA702M	†TI
	6000	1600	1.2*	50*	7*	2K	80	1	12 Volt, Wideband	CA3015A	†RCA
										CA3016A	†RCA
										CA3030A	RCA
										CA3038A	†RCA
2.5	100	20	3*	1*	0.25*	25K	70	2	Micropower, High Performance	LH0001A	† National
	125	35	2*	1*	0.005*	250K	94	4	High Accuracy Instrumentation	725C	AMD
										µA725C	Fairchild
										LM725C	National
										µPC725	NEC America
										PM725C	PMI
										RC725	Raytheon
			3	—	—	250K	96	4	725 type	µPC154A	NEC America
	200	40	5	0.3*	0.12*	250K	94	1	Low Drift, Low Noise	AD504J	AD
	250	50	10*	1*	0.25*	100K	90	2	High Gain Instrumentation, 50 ma	LH0020	† National
3.0	0.0003	—	50	0.35	0.3	40K	66	0	FET Electrometer	AD515J	AD
	0.020	0.020*	25	5	20*	50K	110*	0	High Voltage FET	3581J	Burr-Brown
				3*	20*	100K	110*	0	High Voltage FET	3582J	Burr-Brown
				5*	20*	400K	110*	0	High Voltage FET	**3583**	**Burr-Brown (920)**
				7*	—	1000K	110*	2	High Voltage FET	**3584**	**Burr-Brown (920)**
	0.030	—	50	10*	50	25K	70	0	Fast Wideband, High Accuracy FET	AD528J	AD
	0.050	0.015	—	1*	0.3*	40K	80	0	High Performance, Low Input Current		
										LM216A	AMD
										LM316A	AMD
										LM216A	National
										LM316A	National
	0.2	0.05	10*	3*	13*	50K	80	0	Low noise, Bipolar-FET	TL071BC	TI

(Continued)

† Military Temperature Range (−55° to 125°C) * Typical Values

LINEAR–Operational Amplifiers-Characteristics (Cont'd)

Offset Voltage mv (25°C)	Bias Current na. (25°C)	Offset Current na. (25°C)	Voltage Drift µv/°C	Band-width MHz	Slew Rate v/µs	Voltage Gain v/v	CMRR db	Comp.	Comments	Device	Source
Single Units											**(Cont'd.)**
3.0	0.2	0.05									(Cont'd.)
			15	12*	5	50K	82	0	Bipolar-JFET, bias comp.	OP-15C OP-15G	† PMI PMI
				17*	9	50K	82	0	Wideband-JFET, bias comp.	OP-16C OP-16G	† PMI PMI
				—	25	50K	82	—	Wideband, Decompensated, Settles to 0.01% in 1.6 µs	OP-17C OP-17G	† PMI PMI
		0.1	10*	1*	3.5*	4K	80	0	Low power, Bipolar-JFET	TL061BC	TI
									Programmable Bipolar FET	TL066BC	TI
				3*	13*	50K	80	0	Bipolar-JFET	TL081BC TL088C TL088M	TI TI † TI
	4	0.5	5	100	1000	1000K	0		Settles to 0.01% in 200ns	**AM-500GC** **AM-500MC**	**Datel (691)** **Datel (691)**
			7	100	1000	1000K	0	—	Fast Settling	**AM-500MR**	**Datel (691)**
			10	100	1000	1000K	0	—	Fast Settling	**AM-500MM**	**† Datel (691)**
	5	3	10*	—	0.1*	40K	80	0	Programmable Amplifier	**HA-2720**	**† Harris (990)**
	7.5	3	—	0.25*	0.16*	100K	70	0	Programmable	4250 LM4250 SG4250 UC4250	† Intersil † National † Silicon G † Solitron
	10	2	15	0.3*	0.13*	50K	80	0	Micropower	RM4132	† Raytheon
				12*	4	100K	80	0	High Impedance	**HA-2600** HA2600	**† Harris (976)** † Intersil
	12	5	4*	—	0.2*	100K	70	0	Programmable	SG1250 SG2250	† Silicon G Silicon G
	15	15	15	35*	25	100K	80	1	Wideband, General Purpose	AD507K	AD
	20	7.5	5*	0.27*	0.16*	50K	70	0	Low Power Adjustable Current	ICL8021M	† Intersil
		10	5	—	20	300K	106	0	High Speed	AM-470-2M	† Datel
			5*	1*	10	400K	86	0	Wide Response, Low Power	**HA-2700** **HA-2704**	**† Harris (988)** **Harris (988)**
	25	5	10*	—	—	4K	60	3	Matched Transistors	LH0005A	† National
	50	5	—	—	—	50K	80	0	Higher Performance	SSS741B	PMI
	80	30	15	0.4	0.3	50K	80	0	Higher Performance	**LM741A** **LM741E**	**† National (1035)** **National (1035)**
								1	High Slew Rate Inverting	**HA-2530**	**† Harris (974)**
			—	1*	0.6	50K	80	0	to 500 ma, single supply	µA759	† Fairchild
	100	25	—	—	—	25K	70	0	High Performance 741	SSS741 SSS741G	† PMI † PMI
	110	30	15	0.43	0.3	50K	80	0	JAN 741	38510/10101	† Intersil
	200	50	20	1*	0.5*	50K	80	0	Higher Accuracy 741C	AD741J	AD
									High Current	AD512K	AD
			25	1*	0.5*	50K	80	0	High Current	AD512S	† AD
	300	100	—	2*	1	25K	70	1	±1 amp	833-21	† Beckman
			3*	1*	1.5*	100K	70	1	0.2 amp Power	LH0041	† National
			10	1*	0.4*	25K	70	3	High Gain	RM709	† Raytheon
			25	1*	1.5	100K	70	1	1.0 amp Power	LH0021	† National
	500	60	5*	1*	34*	50K	80	3	Fast General Purpose	1339-02	† Teledyne P
			—	—	4.2*	15K		2	High Slew Rate	ULS-2139	† Sprague
		75	3*	2*	4.2*	50K	80	2	General Purpose	MC1539	† Motorola
	2000	200	4*	10*	—	20K	70	0	General Purpose Wide Bandwidth	LH0003	† National

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† Military Temperature Range (−55° to 125°C) * Typical Values

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LINEAR–Operational Amplifiers-Characteristics (Cont'd)

Offset Voltage mv (25°C)	Bias Current na. (25°C)	Offset Current na. (25°C)	Voltage Drift µv/°C	Band-width MHz	Slew Rate v/µs	Voltage Gain v/v	CMRR db	Comp.	Comments	Device	Source
Single Units											**(Cont'd.)**
3.0	2000	200	4*	10*	—	20K	70	0	General Purpose Wide Bandwidth		(Cont'd.)
										LH0003C	National
3.5	0.015	—	75	1*	3	20K	70	0	High Accuracy, FET	AD506J	AD
	12	2.5	6*	—	0.04*	40K	80	1	Micropower	CA3078A	†RCA
									Low Noise, Micropower	CA6078A	†RCA
4.0	0.010	0.002	10	1*	1.5	100K	80	0	High Performance FET	LH0022	† National
	15	2	15	4*	2*	40K	80	0	High Performance, High Gain	RM1556	† Raytheon
			—	1*	2.5*	100K	80	0	High Performance	MC1556	† Motorola
										MC1556	Signetics
										SG1556	† Silicon G
		15	10*	35*	25	100K	80	1	Wide Band, High Impedance	**HA-2620**	**† Harris (980)**
										HA2620	† Intersil
			20	35*	20	100K	80	1	Wideband, General Purpose	AD507S	† AD
	25	12	15*	4*	5*	100K	80	0	High Voltage	**HA-2640**	**† Harris (984)**
	200	50	15	12*	10	50K	80	0	High Speed, Fast Settling	AD518K	AD
			20	12*	10	50K	80	0	High Speed, Fast Settling	AD518S	† AD
	250	50	—	15*	50	50K	80	0	Precision High Speed	LM118	† AMD
										LM218	AMD
										µA118	† Fairchild
										µA218	Fairchild
										LM118	**† National (1035)**
										LM218	National
										SFC2118	† NPC
										SFC2218	NPC
										LM118	† Raytheon
										LM218	**Raytheon**
										LM118	† TI
										LM218	TI
	300	100	5*	1*	25	50K	70	1	0.5a, Wideband	LH0061	† National
	700	100	25	—	—	18K	70	1	20ma Output	TAA762	† Siemens
										TAA862	† Siemens
	1500	300	—	10*	6*	25K	70	1	Low noise, Comp. for G=3	XR5534AC	Exar
										XR5534AM	Exar
										NE5534	**Signetics (1117)**
										SE5534	**Signetics (1117)**
										NE5534A	**Signetics (1117)**
										SE5534A	**Signetics (1117)**
										NE5534	TI
										SE5534	TI
										NE5534A	TI
										SE5534A	TI
					13*	100K*	80	1	Low Noise, Comp. for G=3	AM-435-2C	Datel
										AM-435-2M	† Datel
	30000	5000	20*	70*	400	4K	60*	3	High Slew Rate	LH0024	† National
4.5	170	32	6*	—	0.04*	25K	80	1	Micropower	CA3078	RCA
5.0	0.001	0.0005*	25	1*	0.6	50K	90*	0	Low Offset FET	**3522L**	**Burr-Brown (920)**
	0.005	0.0006		2*	50*	—	80	0	Micropower, Transconductance Amplifier		
										CA3080	RCA
										CA3080A	†RCA
	0.025	0.002	25	15*	50	50K	80	0	Precision, High Speed, FET	LH0062	† National
	0.030	0.02	6*	4*	10*	50K	80	0	MOS-Bipolar	CA3160A	†RCA
			10*	4*	10*	50K	80	1	MOS, Single Supply, Strobe	CA3130A	†RCA
	0.040	0.02	6*	4.5*	9*	20K	70	0	MOS FET, Single Supply	CA3140A	Intersil
										CA3140A	RCA
	0.10	0.01	100	8	50	50K	60	0	FET, settles to 0.01% in 1µs	1414-83	† Teledyne P
		0.02	5*	2.5*	5*	50K	85	0	Bipolar - JFET	LF155	† AMD

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† Military Temperature Range (−55° to 125°C) * Typical Values

LINEAR–Operational Amplifiers-Characteristics (Cont'd)

Offset Voltage mv (25°C)	Bias Current na. (25°C)	Offset Current na. (25°C)	Voltage Drift µv/°C	Band-width MHz	Slew Rate v/µs	Voltage Gain v/v	CMRR db	Comp.	Comments	Device	Source	
Single Units												**(Cont'd.)**
5.0	0.10	0.02	5*	2.5*	5*	50K	85	0	Bipolar - JFET			(Cont'd.)
										LF255	AMD	
										µAF155	† Fairchild	
										µAF255	Fairchild	
										LF155	† Intersil	
										LF255	Intersil	
										LF155	† Motorola	
										LF255	Motorola	
										LF355B	Motorola	
										LF155	**† National**	**(1035)**
										LF255	National	
										LF355B	National	
										PM155	† PMI	
										PM255	PMI	
										LF155	† Raytheon	
										LF255	Raytheon	
										LF155	† Signetics	
										LF255	Signetics	
										LF355B	Signetics	
										LF155	† TI	
										LF255	TI	
				5*	7.5*	50K	85	0	Wideband - JFET	LF156	† AMD	
										LF256	AMD	
										µAF156	† Fairchild	
										µAF256	Fairchild	
										LF156	† Intersil	
										LF256	Intersil	
										LF156	† Motorola	
										LF256	Motorola	
										LF356B	Motorola	
										LF156	**† National**	**(1035)**
										LF256	National	
										LF356B	National	
										PM156	† PMI	
										PM256	PMI	
										LF156	† Raytheon	
										LF256	Raytheon	
										LF156	† Signetics	
										LF256	Signetics	
										LF356B	Signetics	
										LF156	† TI	
										LF256	TI	
				—	—	50K	85	—	Wideband Decompensated	LF157	† AMD	
										LF257	AMD	
										µAF157	† Fairchild	
										µAF257	Fairchild	
										LF157	† Intersil	
										LF257	Intersil	
										LF157	† Motorola	
										LF257	Motorola	
										LF357B	Motorola	
										LF157	**† National**	**(1035)**
										LF257	National	
										LF357B	National	
										PM157	† PMI	
										PM257	PMI	
										LF157	† Raytheon	
										LF257	Raytheon	
										LF157	† Signetics	
										LF257	Signetics	
										LF357B	Signetics	
										LF157	† TI	
										LF257	TI	
		0.025	25*	70*	350	1K	50	2	Ultra Fast FET	LH0032	† National	
		0.10	10*	3*	13*	50K	80	0	Bipolar FET	**µA771**	**† Fairchild**	**(938)**
	0.20	0.1	10*	4*	13*	50K	80	0	Wideband Bipolar-JFET	LF351B	National	

(Continued)

† Military Temperature Range (−55° to 125°C) * Typical Values

Bold face indicates additional data is provided on the page noted.

LINEAR–Operational Amplifiers-Characteristics (Cont'd)

Offset Voltage mv (25°C)	Bias Current na. (25°C)	Offset Current na. (25°C)	Voltage Drift µv/°C	Band-width MHz	Slew Rate v/µs	Voltage Gain v/v	CMRR db	Comp.	Comments	Device	Source
Single Units											**(Cont'd.)**
5.0											(Cont'd.)
	4	1	10	1*	0.5*	20K	80	0	Low Input Current 741	AD502L	AD
				0.5*	—	15K	65	1	Low Input Current 709	AD801B	AD
		2	20	0.5*	—	15K	65	1	Low Input Current 709	AD801A	AD
			40	0.5*	—	15K	65	1	Low Input Current 709	AD801S	† AD
	7	4	20	1*	0.5*	20K	80	0	Low Input Current 741	AD502K	AD
	10	5	7*	1*	0.5*	20K	70	0	Low Input Current	ICL8008M	† Intersil
			10*	—	0.1*	25K	74	0	Programmable Amplifier	**HA-2725**	**Harris (990)**
			20*	1*	0.5*	20K	80	0	Darlington 741	AD502S	† AD
		6	—	0.25*	0.16*	50K	70	0	Programmable	4250C	Intersil
										LM4250C	National
										SG4250C	Silicon G
										UC4250C	Solitron
	15	5	20	0.5*	0.1	45K	100*	0	Low Bias Current	**3501A**	**Burr-Brown (920)**
										3501R	**† Burr-Brown (920)**
	20	3	—	1*	2*	100K	80	0	High Voltage	MC1536	† Motorola
										SG1536	† Silicon G
				—	2.5*	100K	80	1	High Voltage	LM144	† National
	25	5	20	0.3*	0.13*	50K	70	0	Micropower	RC4132	Raytheon
		25	10*	12*	4	80K	74	0	High Impedance	**AM-460-2**	**Datel (687)**
										AM-460-2M	**† Datel (687)**
										HA-2602	**† Harris (976)**
										HA-2605	**Harris (976)**
										HA2602	† Intersil
										HA2605	Intersil
			15*	35*	20	80K	74	1	Wide Band, High Impedance	**AM-462-1**	**Datel (687)**
										AM-462-1M	† Datel
										AM-462-2	**Datel (687)**
										AM-462-2M	**† Datel (687)**
										HA-2622	**† Harris (980)**
										HA-2625	**Harris (980)**
										HA2622	† Intersil
										HA2625	Intersil
			20*	12*	—	80K	74	0	Wideband	3506J	Burr-Brown
			30*	1	—	80K	74	1	Wideband	**3508J**	**Burr-Brown (920)**
			—	10*	20	80K	100*	1	Wideband, High Gain	1321	Teledyne P
										1321-01	† Teledyne P
	30	15*	20	1.5*	0.6	45K	100*	0	Low Bias, Low Noise	**3500A**	**Burr-Brown (920)**
										3500R	**† Burr-Brown (920)**
	35	10	20	1.5	3	40K	70	0	High Performance, High Gain	RC1556A	Raytheon
	40	2.5	30*	1*	10	200K	80	0	Micropower FET High Current Out	1323	Teledyne P
		15	5	—	20	300K	106	0	High Speed	AM-470-2C	Datel
										AM-470-2M	† Datel
			10	1*	10	200K	80	0	Wide Response, Low Power	**HA-2705**	**Harris (988)**
		20	0.5	0.2	2.5	1-1000	70	1	Full Instrumentation	AD520K	AD
										AD520S	† AD
	50	15	—	0.2	0.35	50K	70	0	Programmable Low Power	MC1776	† Motorola
		20	—	—	1.5*	25K	—	0	Low Input Bias, High Slew Rate	ULN-2171	Sprague
	100	20	10	2.5*	18*	25K	80	0	High Speed	MP5501C	Micro Power
										MP5501G	† Micro Power
										OP-01C	PMI
										OP-01G	† PMI
			30	0.5	0.5*	25K	70	1	Precision	SG777C	Silicon G
										µA777C	TI
				1*	0.5*	25K	70	1	Precision	µA777C	Fairchild
			—	—	—	50K	70	0	High Performance 741C	SSS741C	AMD

(Continued)

† Military Temperature Range (–55° to 125°C) * Typical Values

LINEAR–Operational Amplifiers-Characteristics (Cont'd)

Offset Voltage mv (25°C)	Bias Current na. (25°C)	Offset Current na. (25°C)	Voltage Drift µv/°C	Band-width MHz	Slew Rate v/µs	Voltage Gain v/v	CMRR db	Comp.	Comments	Device	Source
Single Units											**(Cont'd.)**
5.0	100										(Cont'd.)
		25	—	—	—	50K	70	0	High Performance 741	SSS741G	† PMI
		50	3*	—	—	20-40K	80	1	Micropower	µPC153A	NEC America
										µPC253A	NEC America
		100	—	1*	0.4*	50K	70	0	Programmable	**XR146**	**Exar (929)**
	120	40	6*	3*	20	50K	70	0	High Slew Rate	NE530	Signetics
	150	20	20	4*	2*	25K	70	0	High Performance, High Gain	RC4131	Raytheon
		30	—	—	—	50K	70	0	Single Supply	TL321I	TI
										TL321M	† TI
		40	6*	—	10	50K	70	0	High Slew Rate	NE535	Signetics
					60*	50K	70	1	60V/µs, Comp. for G=5	NE538	Signetics
	180	25	6.6*	—	3*	22K	93	2	High Output Current	CA3033A	† RCA
			—	—	3*	22K	93	2	High Output Current	CA3047A	RCA
	200	20	5*		250	100K	80	1	High Slew Rate, Inverting	**HA-2535**	**Harris (974)**
		25	20*	12*	25	20K	80	0	High Slew Rate	**HA-2500**	**† Harris (966)**
										HA2500	† Intersil
		50	20*	8*	15*	50K	80	1	Four Addressable Inputs, Single Amplifier		
										HA-2400	**† Harris (964)**
										HA-2404	**Harris (964)**
		60	3*	1*	0.25*	25K	70	2	Micropower, High Performance	LH0001AC	National
		—	10*	10*	130	25K	—	2	High Speed Inverting	ICL8017M	† Intersil
	250	20	20	1*	0.5*	25K	96	1	General Purpose	LM301A	Raytheon
								0	General Purpose	LM307	Raytheon
			25	1*	0.4	50K	80	0	High Performance, Low Drift	1319	Teledyne P
		50	—	—	0.6*	25K	—	0	General Purpose	ULN-2151	Sprague
	300	150	10*	7*	3.5	25K	80	0	Low Noise	**HA-909**	**† Harris (958)**
	350	35	6.6*	—	2.7*	16K	84	2	High Output Current	CA3033	† RCA
			—	—	2.7*	16K	84	2	High Output Current	CA3047	RCA
	500	150	20	—	—	20K	70	1	General Purpose	TA7502	Toshiba
										TA7502A	Toshiba
		200	3*	0.5*	0.3*	25K	70	3	General Purpose	µA709M	† Fairchild
										MC1709	† Motorola
										LM709	**† National (1035)**
										µA709	† Signetics
										µA709M	† TI
				0.8*	5*	50K	70	0	Wideband 741	SG1217	† Silicon G
				1*	0.5*	50K	70	0	General Purpose Compensated	AD741	† AD
										741M	† AMD
										µA741M	† Fairchild
										ICL741	† Intersil
										M5141	Mitsubishi
										MC1741	Motorola
										MC1741	† Motorola
										LM741	**† National (1035)**
										PM741	PMI
										RM741	† Raytheon
										CA741	† RCA
										µA741	† Signetics
										SG741	† Silicon G
										µA741M	† TI
									Low Noise 741	741LN	† Intersil
										CA6741	† RCA
									Compensated 101	LH101	† National
										LH101	† Raytheon
								1	General Purpose, Uncompensated	LM101	† AMD

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† Military Temperature Range (−55° to 125°C) * Typical Values

Bold face indicates additional data is provided on the page noted.

LINEAR–Operational Amplifiers-Characteristics (Cont'd)

Offset Voltage mv (25°C)	Bias Current na. (25°C)	Offset Current na. (25°C)	Voltage Drift µv/°C	Band-width MHz	Slew Rate v/µs	Voltage Gain v/v	CMRR db	Comp.	Comments	Device	Source
Single Units											**(Cont'd.)**
5.0	500	200	3*	1*	0.5*	50K	70	1	General Purpose, Uncompensated		(Cont'd.)
										LM201	AMD
										µA101	† Fairchild
										LM101	**† National (1035)**
										LM101	† Raytheon
										CA101	† RCA
										LM101	† Signetics
										SG101	† Silicon G
									Uncompensated 741	748M	† AMD
										µA748M	† Fairchild
										MC1748	† Motorola
										LM748	† National
										LM748C	National
										SL748A	Plessey
										RM748	† Raytheon
										CA748	† RCA
										µA748	† Signetics
										SG748	† Silicon G
										µA748M	† TI
					10	50K	70	0	High Slew Rate 741	MC1741S	† Motorola
										MC1741S	Signetics
										SG741S	† Silicon G
									Low Noise 741	MC1741NS	Motorola
			4*	30*	0.7*	20K	70	2	Programmable	CA3094	† RCA
										CA3094A	† RCA
										CA3094B	† RCA
			—	0.5*	35	50K	70	1	High Slew Rate	RM4531	† Raytheon
				1*	0.7	50K	70	0	High Speed 741	ICL741MHS	† Intersil
					30*	50K	70	1	High Slew Rate	SE531	† Signetics
				—	—	100K*	70	0	General Purpose	M51802	Mitsubishi
	700	100	25	—	50*	10K	65	0	20ma output	TCA322	† Siemens
	750	250	6*	65*	15	15K	74	3	High Speed High Gain	µA715M	† Fairchild
										715	† AMD
	800	200	20	—		2K	70	3	709 Type	µPC55A	NEC America
	1000	150	8*	—	2*	40K	90	3	General Purpose	MC1533	Motorola
	2000	400	—	38*	25*	0.6K	76	1	Large Signal Wideband	CA3100	† RCA
	7000	2000	5*	—	—	2K	70	1	702 Type	µPC51A	NEC America
	7500	2000	5*	7*	1.5*	2K	70	2	Wideband	MC1712C	Motorola
			20	30*	3.5*	2K	70	3	Wideband	µA702C	Fairchild
										µPC702	NEC America
										SL702C	Plessey
										RC702	Raytheon
	10000	2000	10*		1.7*	1.4K	70	3	General Purpose	TL702M	† TI
						4.5K	70	3	General Purpose	MC1530	† Motorola
	12000	5000	1.2*	15*	3*	0.7K	70	1	6 Volt, Wideband	CA3008	† RCA
										CA3010	† RCA
										CA3029	RCA
										CA3037	† RCA
	15000	4000	10*	6.5*	200*	28K*	—	1	Wideband, Comp. for G>5	**HA-5190**	**† Harris (1010)**
										HA-5195	**Harris (1010)**
	20000	—	10	—	800	250	70	1	Fast, slews 800 V/µs	NE5539	Signetics
										SE5539	† Signetics
			25	500*	250	10K	80	1	Settles to 0.01% in 70 ns	1435	† Teledyne P
	24000	5000	3.5*	50*	7*	2K	80	1	12 Volt, Wideband	CA3015	† RCA
										CA3016	† RCA
										CA3030	RCA
										CA3038	† RCA
6.0	0.025	0.002	15	1*	1	75K	70	0	High Performance FET	LH0022C	National

(Continued)

† Military Temperature Range (−55° to 125°C) * Typical Values

LINEAR–Operational Amplifiers-Characteristics (Cont'd)

Offset Voltage mv (25°C)	Bias Current na. (25°C)	Offset Current na. (25°C)	Voltage Drift µv/°C	Band-width MHz	Slew Rate v/µs	Voltage Gain v/v	CMRR db	Comp.	Comments	Device	Source
Single Units											**(Cont'd.)**
6.0											(Cont'd.)
	0.2	0.05	10*	3*	13*	50K	80	0	Low Noise Bipolar-JFET	TL071AC TL071M TL070AC TL070M	TI †TI TI †TI
		0.1	10*	1*	3.5*	40K	80	0	Low Power Bipolar JFET	TL061AC TL061M	TI †TI
								1	Low Power Bipolar-JFET	TL060AC TL060M	TI †TI
								0	Programmable Bipolar JFET	TL066AC TL066M	TI †TI
				3*	13*	50K	80	0	Bipolar-JFET	µPCF081 TL070C TL080AC TL081M	NEC America TI TI †TI
								1	Bipolar-JFET	TL080AC TL080M	TI †TI
	25	10	6*	—	0.2*	75K	70	0	Programmable	SG3250	Silicon G
		12	40	1*	0.5*	20K	80	0	Low Input Current 741	AD502J	AD
		20	15*	—	0.5*	20K	70	0	Low Input Current	ICL8008C	Intersil
		25	15*	35*	20	80K	74	1	Wideband, General Purpose	AD507J	AD
	30	30	15*	0.6	17	70K	74	0	Wideband	**HA-2627**	**Harris** **(978)**
				4*	5*	100K	74	0	High Voltage	**AM-464-2** **AM-464-2M** **HA-2645** 1332	**Datel** **(687)** **†Datel** **(687)** **Harris** **(984)** Teledyne P
			—	0.05	4	70K	74	0	Wideband	**HA-2607**	**Harris** **(978)**
	35	10	5*	0.27*	0.16*	50K	70	0	Low Power Adjustable Current	ICL8021C	Intersil
	50	25	—	0.2	0.35*	50K	70	0	Programmable Low Power	MC1776C	Motorola
					0.8*	50K	70	0	Programmable Low Power	MC3476	Motorola
	100	25	—	—	—	25K	70	0	High Performance 741C	SSS741C	PMI
		30	5*	—	0.3*	25K	70	1	Supply to ±10v	TCA520	Signetics
	250	50	—	1*	0.5	25K	80	0	to 500 ma, single supply	µA759C	Fairchild
	500	100	—	1*	0.5*	20K	64	0	741 type	L141	SGS
		200	3*	1*	10	20K	70	0	High Slew Rate 741	MC1741SC SG741SC	Motorola Silicon G
									Low Noise 741	MC1741NC	Motorola
			5*	0.8*	5*	20K	70	0	Wideband 741C	SG3217	Silicon G
				1*	1	100K	70	1	0.2 amp Power	LH0041C	National
			10*	1*	0.25	100K	90	2	High Gain, Instrumentation, 50 ma Output	LH0020C	National
					0.5*	25K	70	0	Low Noise 741	ICL741CLN	Intersil
			15*	0.2*	0.2*	20K	70	0	High Power	µA791C TBA0791	Fairchild NPC
			30	1*	1*	100K	70	0	1.0 amp Power	LH0021C	National
			—	1*	0.5*	20-50K	70	1	General Purpose	748C µA748C MC1748C SFC748C SL748 RC748 CA748C µA748C TDA0748 SG748C	AMD Fairchild Motorola NPC Plessey Raytheon RCA Signetics Signetics Silicon G

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Values

Bold face indicates additional data is provided on the page noted.

LINEAR–Operational Amplifiers-Characteristics (Cont'd)

Offset Voltage mv (25°C)	Bias Current na. (25°C)	Offset Current na. (25°C)	Voltage Drift µv/°C	Band-width MHz	Slew Rate v/µs	Voltage Gain v/v	CMRR db	Comp.	Comments	Device	Source
Single Units											**(Cont'd.)**
6.0	500	200	—	1*	0.5*	20-50K	70	1	General Purpose		(Cont'd.)
										µA748C	TI
									High Reliability	L148	SGS
					0.5	20-50K	70	0	General Purpose Compensated	AD741C	AD
										µA741C	Fairchild
										HA17741	Hitachi
										ICL741C	Intersil
										MC1741C	Motorola
										LM741C	**National (1035)**
										µPC151	NEC America
										µPC741	NEC America
										SFC741C	NPC
										PM741C	PMI
										RC741	Raytheon
										CA741C	RCA
										µA741C	Signetics
										MC1741SC	Signetics
										SA741C	Signetics
										TDA0741	Signetics
										SG741C	Silicon G
										µA741C	TI
					0.7	25K	70	0	High Speed 741	ICL741CHS	Intersil
				—	10	20K	70	1	1a output	TDB0791	NPC
		300	10*	7*	5*	20K	74	0	Low Noise	**HA-911**	**Harris (958)**
				12*	50	25K	70	0	High Speed, Fast Settling	AD518J	AD
	1000	300	6*	—	18*	12K	65	1	20ma Output	TAA761	Siemens
										TAA765	Siemens
	1200	500	5*	4*	100*	10K	70	2	Gated	ZN424	Ferranti
	1500	200	—	0.5*	35*	20K	70	1	High Slew Rate	RC4531	Raytheon
				1*	20	20K	70	1	High Slew Rate, High Performance	NE531	Signetics
7.0	200	10*	10*	10*	130*	25K	—	2	High Speed Inverting	ICL8017C	Intersil
		50	—	—	—	25K	65	0	Single Supply	TL321C	TI
	400	75	5*	—	—	3K	63	0	250 mA output, electronic shutdown	**LM13080**	**National (1057)**
7.5	7	1	6*	—	—	25K	80	1	308 Type	µPC156A	NEC America
			30	1*	0.3*	25K	80	0	Micropower, Supply Current 800µa	LM312	AMD
										LM312	National
				0.3*	0.1	25K	80	0	Compensated 308	SG3118	Silicon G
				1*	0.3*	25K	80	1	Precision Bipolar	AD308	AD
										LM308	AMD
										µA308C	Fairchild
										308	Intersil
										LM308	Motorola
										LM308	National
										SFC2308	NPC
										PM308	PMI
										LM308	Raytheon
										LM308	Signetics
										SG308	Silicon G
			—	0.3*	0.3*	25K	80	1	Low Noise 308	308LN	Intersil
	15	2	30		0.1	25K	80	1	Precision	1660	AMD
				0.3*	0.1	25K	80	1	Improved 201, 301A	SG1660	Silicon G
								0	Improved 307, 741	SG1760	Silicon G
	250	50	30	1*	0.5*	25K	70	0	General Purpose, Compensated	LM307	AMD
										µA307C	Fairchild
										307	Intersil
										LM307	Motorola
										LM307	National
										SFC2307	NPC
										CA307	RCA

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† Military Temperature Range (−55° to 125°C)

* Typical Values

LINEAR–Operational Amplifiers-Characteristics (Cont'd)

Offset Voltage mv (25°C)	Bias Current na. (25°C)	Offset Current na. (25°C)	Voltage Drift µv/°C	Band-width MHz	Slew Rate v/µs	Voltage Gain v/v	CMRR db	Comp.	Comments	Device	Source
Single Units											**(Cont'd.)**
7.5	250	50	30	1*	0.5*	25K	70	0	General Purpose, Compensated		(Cont'd.)
										LM307	Signetics
										SG307	Silicon G
										LM307	TI
								1	General Purpose Uncompensated	AD301A	AD
										LM301A	AMD
										µA301A	Fairchild
										HA17301	Hitachi
										301A	Intersil
										LM301A	Motorola
										LM301A	National
										µPC157	NEC America
										µPC301	NEC America
										SFC2301A	NPC
										CA301A	RCA
										LM301A	Signetics
										TDA0301	Signetics
										SG301A	Silicon G
										LM301A	TI
			—	0.8*	0.5*	25K	70	1	Low Noise 301A	301ALN	Intersil
	350	35	—	—	—	16K	84	2	General Purpose	M5133	Mitsubishi
	600	60	5*	1*	34*	40K	80	3	Fast General Purpose	1339-01	Teledyne P
	1000	100	12*	1*	34*	15K	80	3	Fast General Purpose	1339	Teledyne P
		150	3*	2*	4.2*	15K	80	2	General Purpose	MC1439	Motorola
		300	6*	—	18*	5K	60	0	20ma Output	TCA321	Siemens
										TCA325	Siemens
	1500	250	6	65*	10	10K	74	3	High Speed	715C	AMD
										HA17715	Hitachi
										µA715C	Fairchild
		500	6*	1*	0.5*	20K	65	0	Compensated 201	LH201	National
										LH201	Raytheon
								1	General Purpose	LM301	AMD
										µA201M	Fairchild
										LM201	National
										LM201	Raytheon
										CA201	RCA
										LM201	Signetics
										SG201	Silicon G
			6-10*	1*	0.3*	15K	65	3	General Purpose	µA709C	Fairchild
										M51709	Mitsubishi
										LM709C	**National** (1035)
										RC709	Raytheon
										µA709C	Signetics
										SA709C	Signetics
										µA709C	TI
	2000	100	—	—	4.2*	50K	—	2	High Slew Rate	ULN-2139	Sprague
		500	10*	—	2*	30K	80	3	General Purpose	MC1433	Motorola
8.0	40	10	—	1*	2.5*	70K	70	1	High Voltage	LM344	National
	200	25	20*	10*	50	10K	80	0	High Slew Rate	**HA-2510**	**† Harris** (968)
										HA2510	Intersil
				20*	100	10K	80	1	100v/µs, Gain=3	**HA-2520**	**† Harris** (972)
										HA2520	† Intersil
			30	20*	100	10K	80	1	High Speed, Fast Settling	AD509K	AD
										AD509S	† AD
	250	50	20*	12*	20	15K	74	0	High Slew Rate	**AM-450-2**	**Datel** (687)
										AM-450-2M	**† Datel** (687)
										HA-2502	**† Harris** (966)
										HA-2505	**Harris** (966)
										HA2502	† Intersil
										HA2505	Intersil

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Values

Bold face indicates additional data is provided on the page noted.

LINEAR–Operational Amplifiers-Characteristics (Cont'd)

Offset Voltage mv (25°C)	Bias Current na. (25°C)	Offset Current na. (25°C)	Voltage Drift µv/°C	Band-width MHz	Slew Rate v/µs	Voltage Gain v/v	CMRR db	Comp.	Comments	Device	Source
Single Units											**(Cont'd.)**
8.0	250	50	20*								(Cont'd.)
				6*	20	16K	74	0	Fast Slewing	3505J	Burr-Brown
	40000	15000	25*	70*	250	3K	60*	3	High Slew Rate	LH0024C	National
9.0	250	50	30*	8*	15*	50K	74	1	Four Addressable Inputs Single Amplifier	**HA-2405**	**Harris (964)**
10.0	0.010	0.0005*	10	1*	3	50K	70	0	FET Input	ICL8007C-4	Intersil
			15	1*	3	50K	70	0	FET Input	ICL8007C-5	Intersil
										ICL8007M-5	† Intersil
	0.050	0.020*	30	3*	15*	20K	86*	0	High Voltage FET	**3580J**	**† Burr-Brown (920)**
	0.15	0.05	—	1*	0.3*	20K	80	0	High Performance, Low Input Current	LM216	AMD
										LM316	AMD
										LM216	National
										LM316	National
										LM216	Raytheon
										LM316	Raytheon
	0.20	0.05	5*	2.5	5*	25K	80	0	Bipolar - JFET	LF355	AMD
										µAF355	Fairchild
										LF355	Intersil
										LF355	Motorola
										LF355	National
										PM355	PMI
										LF355	Raytheon
										LF355	Signetics
										LF355	TI
				5	12*	25K	80	0	Wideband - JFET	LF356	AMD
										µAF356	Fairchild
										LF356	Intersil
										LF356	Motorola
										LF356	**National (1035,1073)**
										PM356	PMI
										LF356	Raytheon
										LF356	Signetics
										LF356	TI
				—	—	25K	80	—	Wideband Decompensated	LF357	AMD
										µAF357	Fairchild
										LF357	Intersil
										LF357	Motorola
										LF357	National
										PM357	PMI
										LF357	Raytheon
										LF357	Signetics
										LF357	TI
			10*	3*	13*	25K	70	0	Low Noise Bipolar-JFET	TL071C	TI
								1	Low Noise Bipolar-JFET	TL070C	TI
		0.1	10*	3*	13*	50K	70	0	Bipolar FET	**µA771C**	**Fairchild (938)**
				4*	13	25K	70	0	Bipolar-JFET	**LF351**	**National (1035,1073)**
	10	3	150	—	250	0.7K	50	1	100MHZ Unity Gain Frequency	9906	OEI
	30	10	20	4*	2*	40K	70	0	High Performance, High Gain	RC1556	Raytheon
			—	1*	2.5*	70K	70	0	High Performance	MC1456	Motorola
										SG1456	Silicon G
	40	10	65	1*	1.5	—	70	0	2a continuous	**3573**	**Burr-Brown (920)**
			—	1*	2*	70K	70	0	High Voltage	MC1436	Motorola
										MC1456	Signetics
										SG1436	Silicon G
	50	20	20*	—	—	2K	55	3	Matched Input Transistors	LH0005	† National

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Values

LINEAR–Operational Amplifiers-Characteristics (Cont'd)

Offset Voltage mv (25°C)	Bias Current na. (25°C)	Offset Current na. (25°C)	Voltage Drift µv/°C	Band-width MHz	Slew Rate v/µs	Voltage Gain v/v	CMRR db	Comp.	Comments	Device	Source
Single Units											**(Cont'd.)**
10.0											(Cont'd.)
	80	40	1000	0.2	2.5	1-1000	65	1	Full Instrumentation	AD520J	AD
	100	25	25*	—	—	2K	50	3	Matched Input Transistors	LH0005C	† National
	150	25	—	—	0.4*	2.5K	65	3	Darlington Input	MC1531	† Motorola
	250	50	20*	20*	80	7.5K	74	1	High Speed, Fast Settling	AD509J	AD
			25*	12*	15	15K	74	0	High Slew Rate	**HA-2507**	**Harris** (970)
					40	7.5K	74	0	High Slew Rate	**HA-2512**	**† Harris** (968)
										HA2512	Intersil
				20*	80	7.5K	74	1	80V/µs Gain = 3	**HA-2522**	**† Harris** (972)
										HA2522	† Intersil
			30*	12*	40	7.5K	74	0	High Slew Rate	**HA-2515**	**Harris** (968)
					30	7.5K	74	0	High Slew Rate	**HA-2517**	**Harris** (970)
					40	7.5K	74	0	High Slew Rate	HA2515	Intersil
					80	7.5K	74	1	80V/µs Gain = 3	**AM-452-2**	**Datel** (687)
										AM-452-2M	**† Datel** (687)
										HA-2525	**Harris** (972)
										HA2525	Intersil
				20*	60	7.5K	74	0	High Slew Rate	**HA-2527**	**Harris** (970)
					80	7.5K	89*	1	High Slew Rate	1322	Teledyne P
										1322-01	† Teledyne P
				—	80	7K	74	1	Fast Slewing	**3507J**	**Burr-Brown** (920)
	500	200	5*	1*	25	25K	60	1	0.5A, wideband	LH0061C	National
			—	15*	50	25K	70	0	Precision, high speed	LM318	AMD
										µA318	Fairchild
										LM318	National
										µPC159A	NEC America
										SFC2318	NPC
										LM318	TI
	600	200	—	15*	50	25K	70	2	Precision, High Speed	LM318	Raytheon
	750	—	—	—	—	14K	—	1	Telephone Channel Amplifier	L045	SGS
	1000	300	6*	—	18*	0.56K	60	1	to 90 ma Output	TAA861	Siemens
										TAA865	Siemens
										TAA861	Telefunken
										TAA865	Telefunken
	2000	100	2*	10*	5*	1K	75	2	Differential Output	MC1520	† Motorola
	15000	4000	—	—	1.7	3K	65	3	General Purpose	MC1430	Motorola
		5000	5*	—	1.7*	1K	65	3	General Purpose	TL702C	TI
12.0	0.020	0.02	20*	5*	10*	80K	74	1	Wideband, FET Input	**HA-2060A**	**† Harris** (962)
			40*	5*	10*	80K	70	1	Wideband, FET Input	**HA-2065A**	**Harris** (962)
	90	25	—	1*	2*	50K	50	0	High Voltage	MC1436C	Motorola
										SG1436C	Silicon G
		30	—	1*	2.5	25K	110*	0	High Performance	MC1456C	Motorola
										SG1456C	Silicon G
14.0	0.020	0.02	20*	8*	40*	7.5K	74	1	120V/µs Gain = 3	**HA-2050A**	**† Harris** (960)
			40*	8*	40*	7.5K	70	1	120V/µs Gain = 3	**HA-2055A**	**Harris** (960)
	20	—	75*	20*	60	40K*	90	0	High Slew Rate	1434	Teledyne P
	200	15	50*	—	—	10K	65	1	Darlington Input	TCA312	† Siemens
										TCA332	† Siemens
15.0	0.010	0.005	25	1	3	100K	80	0	General Purpose, Low Drift	1421-02	Teledyne P
	0.015	0.01	50	1	3	100K	72	0	General Purpose, Low Drift	1421-01	Teledyne P
	0.020	0.01	10*	0.14*	1*	1-1000	75	2	Full Instrumentation FET	**AM-435-1M**	**† Datel** (689)
										LF152	† National
	0.050	0.025	50	1	3	50K	72	0	General Purpose	1421	Teledyne P
		0.030	10*	4*	10*	50K	70	1	MOS FET Single Supply, Strobe	CA3130	† RCA

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† Military Temperature Range (−55° to 125°C) * Typical Values

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LINEAR–Operational Amplifiers-Characteristics (Cont'd)

Single Units (Cont'd.)

Offset Voltage mv (25°C)	Bias Current na. (25°C)	Offset Current na. (25°C)	Voltage Drift µv/°C	Band-width MHz	Slew Rate v/µs	Voltage Gain v/v	CMRR db	Comp.	Comments	Device	Source
											(Cont'd.)
15.0	0.050	0.030	8*	4*	10*	50K	70	0	MOS FET, Single Supply	CA3160	†RCA
				4.5*	9*	20K	70	0	MOS FET, Single Supply	CA3140	Intersil
										CA3140	†RCA
	0.065	0.005	35	15*	50	25K	70	0	Precision, High Speed, FET	LH0062C	National
	0.20	0.05	10*	1*	0.5*	25K	70	0	JFET-741	LF13741	National
			25*	50*	350	1K	50	2	Ultra Fast FET	LH0032C	National
		0.10	5*	1*	6*	50K	80	0	FET Input	LH740A	† National
			10*	3*	13*	50K	70	0	Bipolar FET	**µA771L**	**Fairchild (938)**
	0.4	0.2	10*	1*	3.5*	3K	70	0	Low Power Bipolar-JFET	TL061C	TI
								1	Low Power Bipolar-JFET	TL060C	TI
								0	Programmable Bipolar-JFET	TL066C	TI
				3*	13*	25K	70	0	Bipolar-JFET	µPCF081	NEC America
										TL081C	TI
								1	Bipolar-JFET	TL080C	TI
	300	100	—	—	1.4*	1.5K	60	3	Darlington Input	MC1431	Motorola
	4000	200	2*	10*	5*	0.75K	60	2	Differential Output	MC1420	Motorola
20.0	0.00025	—	60	0.5*	3	40K	80	0	Electrometer, FET	AD523L	AD
	0.0005	—	30	0.5*	3	40K	80	0	Electrometer, FET	AD523K	AD
	0.010	0.002*	25	1*	2.5	31K	86*	0	High Performance, Low Bias FET	3503B	Burr-Brown
										3503S	† Burr-Brown
		—	25	0.75*	0.5*	50K	70	0	Low Noise FET	AD514L	AD
	0.020	0.0005*	75	1*	6*	50K	70	0	High Performance FET	ICL8007M	† Intersil
		—	25	0.75*	0.5	50K*	70	0	Low Noise FET	AD514K	AD
			50	0.75*	0.5*	50K*	70	0	Low Noise FET	AD514S	† AD
	0.025	0.002*	50	1*	0.5*	25K	80*	0	Low Noise	**3542J**	**Burr-Brown (920)**
										3542S	**† Burr-Brown (920)**
		0.010	20	1*	1.5	50K	70	0	Low Cost FET Input	LH0042	† National
		—	25	1*	6*	50K	70	0	Low Cost FET Input	AD540K	AD
			50	1*	6*	50K	70	0	Low Cost FET Input	AD540S	† AD
					0.5*	25K	80	0	FET	AD3542J	AD
	0.030	0.005*	20*	1*	6*	50K	70	0	FET	SU536	Signetics
	0.050	0.005	25	1*	1	25K	70	0	Low Cost FET	LH0042C	National
	0.50	0.15	5*	1*	6*	50K	80	0	FET Input	LH740AC	National
	0.050	—	25	1*	6*	25K	70	0	Low Cost FET	AD0042C	AD
	0.10	—	25	1*	3	50K	80	0	Low Cost FET Input	AD503K	AD
										AD503S	† AD
	0.20	0.15	20*	3*	6*	50K	64	0	High Slew Rate FET	µA740M	† Fairchild
	50	20	12*	—	9*	0.5K	60	1	Darlington Input	TBB1331	Siemens
	200	25	12*	—	—	6K	60	0	Darlington Input	TCA311	Siemens
										TCA315	Siemens
								1	Darlington Input	TCA331	Siemens
25.0	0.020	0.02	50*	5*	10*	80K	74	1	120V/µs Gain=3	**HA-2060**	**† Harris (962)**
				8*	40*	7.5K	74	1	High Slew Rate, FET	**HA-2050**	**† Harris (960)**
	40000	10000	1000	100	600	1K	50	2	Wide Gain-Bandwidth	9912	† OEI
30.0	0.001	0.0002*	50	1*	2.5	20K	86	0	Low Bias FET	ICL8007AM	† Intersil
										ICL8007AC	Intersil
		—	50*	1*	6*	20K	86	0	FET	1439	Teledyne P
	0.040	0.020	10*	0.14*	1*	1-1000	65	2	Full Instrumentation, FET	**AM-435-1C**	**Datel (689)**
										LF252	National
										LF352	**National (1073)**

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† Military Temperature Range (−55° to 125°C)

* Typical Values

LINEAR–Operational Amplifiers-Characteristics (Cont'd)

Offset Voltage mv (25°C)	Bias Current na. (25°C)	Offset Current na. (25°C)	Voltage Drift µv/°C	Band-width MHz	Slew Rate v/µs	Voltage Gain v/v	CMRR db	Comp.	Comments	Device	Source
Single Units											**(Cont'd.)**
30.0											(Cont'd.)
	30*	2	0.06*	1*	6*	1000K	80*	0	High Slew Rate FET	µA740C	Signetics
	30000	10000	150	200	300	1K	50	0	Wide band	9916	†OEI
	50000	20000	100	300	1K	4K	90	1	Wide band	9914	OEI
50.0	0.00001	—	—	—	0.5*	20K	60	0	Ultra Low Bias FET	ICH8500A	Intersil
	0.0001	—	—	—	0.5*	20K	60	0	Ultra Low Bias FET	ICH8500	Intersil
	0.001	0.0005*	90	0.5*	3	20K	70	0	Electrometer, FET	AD523J	AD
		—	50	0.3*	—	10K	70		MOS FET	µPC250A	NEC America
	0.015	—	75	1*	3	20K	70	0	Low Cost FET Input	AD503J	AD
	0.025	0.005*	75	1*	2.5	20K	86*	0	High Performance, Low Bias FET	3503A 3503R	Burr-Brown †Burr-Brown
	0.050	0.0005*	75	1*	6*	20K	70	0	High Performance, FET	3540J ICL8007C	Burr-Brown Intersil
									Low Cost FET	1424	Teledyne P
		—	75	0.75*	0.5*	20K	70	0	Low Noise FET	AD514J	AD
				1*	6*	20K	70	0	Low Cost FET	AD540J	AD
60.0	0.020	0.02	60*	5*	10*	80K	70	1	Wideband, FET Input	**AM-406-2** **AM-406-2M** **HA-2065** 1433	**Datel (687)** **†Datel (687)** **Harris (962)** Teledyne P
				8*	40*	7.5K	70	1	120V/µs Gain = 3	**AM-405-2** **AM-405-2M** **HA-2055**	**Datel (687)** **†Datel (687)** **Harris (960)**
90.0	0.10	0.005*	30*	1*	6*	50K	64	0	FET, High Input Impedance	NE536	Signetics
	50000	20000	1000	100	2500	2K	60	2	High Gain-Bandwidth, Fast Slewing	9909	OEI
110.0	2	0.3	20*	1*	6*	20K	55	0	High Slew Rate FET	µA740C	Fairchild
200.0	0.01	—	50*	1*	0.4*	10K	70*		MOS FET	µPC152A	NEC America
—	0.05	0.01	100	35	200	500	60	0	Wide band FET	9917	OEI
	0.3	0.1	500	40	600	300	50	2	Wideband, Fast Slewing	9932	OEI
			3000	100	200	0.3K	50	0	Wideband, Fast Slewing	9908	OEI
Dual Units											
0.5	0.06	0.025	5*	—	13*	50K	80	0	Precision BIFET	MC35003A	†Motorola
	0.075	0.03	5*	—	13*	50K	80	0	Precision BIFET	MC34003A	Motorola
	2	0.2	15	1*	0.3*	80K	96	1	Dual 108A	LH2108A LH2108A LH2208A PM2108A PM2208A LH2108A LH2208A	†Intersil †National National †PMI PMI †Signetics Signetics
	3	2.8	2	1.2*	0.25*	200K	114	0	Dual Matched Instrumentation	OP-10 OP-10A	†PMI †PMI
	4	3.8	2	1.2*	0.25*	200K	110	0	Dual Matched Instrumentation	OP-10E	PMI
	7	1	30	1*	0.3*	80K	96	1	Dual 308A	LH2308A LH2308A PM2308A LH2308A	Intersil National PMI Signetics
	20	0.1	10	3	13	50K	80	0	Bipolar-JFET	TL287C TL287M	TI †TI
0.75	50	2	8	0.8	0.5	100K	90	0	Dual Matched	OP-04A OP-04E OP-14A OP-14E	†PMI PMI †PMI PMI
1.0	0.075	0.05	5*	—	13*	50K	80	0	Precision BIFET	MC35003B	†Motorola

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† Military Temperature Range (−55° to 125°C) * Typical Values

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LINEAR–Operational Amplifiers-Characteristics (Cont'd)

Offset Voltage mv (25°C)	Bias Current na. (25°C)	Offset Current na. (25°C)	Voltage Drift µv/°C	Band-width MHz	Slew Rate v/µs	Voltage Gain v/v	CMRR db	Comp.	Comments	Device	Source
Dual Units											**(Cont'd.)**
1.0											(Cont'd.)
	0.1	0.025	10	4.5	10	100K	86	0	Precision Bipolar-JFET	OP-25B OP-20F	† PMI PMI
	0.15	0.07	5*	—	13*	50K	80	0	Precision BIFET	MC34003B	Motorola
1.3	7	6	4.5	1.2*	0.25*	120K	100	0	Dual Matched Instrumentation	OP-10C	PMI
2.0	0.05	0.07	5*	—	13*	25K	70	0	Precision BIFET	MC34003	Motorola
	0.10	0.05	10*	3*	13*	50K	80	0	Bipolar FET	**µA772A**	**† Fairchild (938)**
				4*	13*	50K	80	0	Dual 351A	**LF353A**	**National (1035)**
	2	0.2	15	1*	0.3*	50K	85	1	Dual 108	LH2108 LH2208 PM2108 PM2208 LH2108 LH2208	† National National PMI PMI † Signetics Signetics
	50	5	—	—	—	100K	80	0	Dual High Performance 741	SSS747 SSS747	† AMD † PMI
		10	15	1*	—	50K	70	0	Low Power, Single Supply	LM158A CA158A	National † RCA
									Single Supply	SE532A	† Signetics
		25	5	1.5*	0.8	100K*	100*		Matched Amplifier Pairs	**3500MP**	**Burr-Brown (920)**
	60	10	15	1*	10	50K	70	0	High slew rate	SE5535	† Signetics
				3*	35*	50K	70	0	High Slew Rate	**SE5530**	**† Signetics (1114)**
				—	—	50K	70	1	40 V/µs, G=5	**SE5538**	**† Signetics (1120)**
	75	5	10	0.8	0.5	50K	90	0	Dual Matched	OP-04 OP-04C OP-14 OP-14C	PMI PMI † PMI PMI
		10	15	1*	0.5*	50K	80	1	Dual LM101A High Performance	1501L 1501M LH2101A LH2201A LH2101A LH2101A LH2201A LH2101A LH2201A LH2101A LH2201A	† AMD † AMD † AMD AMD Intersil † National National Raytheon Raytheon † Signetics Signetics
	800	200	—	10*	6*	50K	80	1	Dual 5534	**XR5532M** **XR5533M** **SE5532** **SE5532A** **SE5533** **SE5533A**	**† Exar (929)** **† Exar (929)** **† Signetics (1116)** **† Signetics (1116)** **† Signetics (1117)** **† Signetics (1117)**
3.0	0.2	0.05	10*	3*	13*	50K	80	0	Low Noise Bipolar-JFET	TL072BC	TI
			15	4.0	8	75K	80	0	Precision Bipolar-JFET	OP-25C OP-25G	† PMI PMI
		0.1	10*	1*	3.5*	4K	80	0	Low Power, Bipolar JFET	TL062BC	TI
				3*	15*	50K	80	0	Bipolar JFET	TL082BC TL288C TL288M	TI TI † TI
	5	3	10*	25*	0.1*	40K	80	0	Programmable	**HA-2730**	**† Harris (993)**
	15	5	—	.25*	0.16*	100K	70	0	Programmable Dual LM4250	LH24250	† National
	20	7.5	5*	0.27*	0.16*	50K	70	0	Low Power Adjustable Current	ICL8022M	† Intersil
	50	5	—	—	—	50K	80	0	Higher Performance	SSS747B	PMI
	80	15	15	1*	—	50K	70	0	Low Power, Single Supply	LM258A CA258A	National RCA

(Continued)

† Military Temperature Range (−55° to 125°C) * Typical Values

LINEAR–Operational Amplifiers-Characteristics (Cont'd)

Offset Voltage mv (25°C)	Bias Current na. (25°C)	Offset Current na. (25°C)	Voltage Drift µv/°C	Band-width MHz	Slew Rate v/µs	Voltage Gain v/v	CMRR db	Comp.	Comments	Device	Source
Dual Units											**(Cont'd.)**
3.0	80										(Cont'd.)
		30	15	0.44	0.3	50K	80	0	Dual 741	µA747AM	† Fairchild
										µA747EC	Fairchild
										LM747A	† National
										LM747E	National
	100	30	8*	8*	2	25K	80	0	High Slew Rate	**HA-2650**	**† Harris (986)**
			20	1*	—	25K	65	0	Low Power, Single Supply	LM358A	National
										CA358A	RCA
	750	400	3*	—	2*	20K	70	3	Audio Preamp	µA749C	Fairchild
										µA749M	† Fairchild
	3000	300	10*	1*	0.01*	4K	70*	3	General Purpose	MC1535	† Motorola
4.0	700	100	25	—	—	18K	70	0	20ma output	TAA2762	† Siemens
	1500	300	—	10*	6*	25K	70	1	Dual 5534	**XR5532C**	**Exar (929)**
										XR5533C	**Exar (929)**
	150	25	—	—	—	50K	70	0	2 op amp/comparators	**LM192**	**† National (1054)**
	1500	300	—	10*	6*	25K	70	1	Dual 5534	XR5533AC	Exar
										NE5532	**Signetics (1116)**
										NE5532A	**Signetics (1116)**
										NE5533	**† Signetics (1117)**
										NE5533A	**Signetics (1117)**
5.0	0.04	0.02	15*	45*	9*	20K	70	0	Dual 3140A, MOS FET	CA3240A	RCA
	0.10	0.10	10*	3*	13*	50K	80	0	Bipolar FET	**µA772**	**† Fairchild (938)**
	0.20	0.10	10*	4*	13*	50K	80	0	Dual 351B	LF353B	National
	7.5	3	3*	1*	15*	200K	70	0	Multi-Purpose Programmable	µA776M	† Fairchild
	10	5	10*	—	0.1*	25K	74	0	Programmable	**HA-2735**	**Harris (993)**
		25	10*	1*	0.6*	50K	70	0	Single Supply, I/O operates to ground	µA798M	† Fairchild
	100	25	—	—	—	50K	70	0	Dual High Performance 741C	SSS747C	AMD
										SSS747C	PMI
										SSS747G	† PMI
										SSS1458	PMI
										SSS1558	† PMI
		40	—	0.8*	0.5*	4K	60	0	Low Power	TL022M	† TI
	120	40	6*	3*	35*	50K	70	0	High Slew Rate	**NE5530**	**Signetics (1114)**
	150	30	7*	1*	—	50K	70	0	Half LM124	LM158	† Motorola
										LM158	† National
										CA158	† RCA
										CA258	RCA
										LM258	National
										LM158	† Signetics
										LM258	Signetics
										SE532	**† Signetics (1109)**
										LM158	† TI
		40	6*	1*	10	50K	70	0	High Slew Rate, Dual 535	NE5535	Signetics
				—	60*	—	70	1	60 V/µs, G=5, Dual 538	**NE5538**	**Signetics (1120)**
	200	60	8*	8*	2	20K	74	0	High Slew Rate	**HA-2655**	**Harris (986)**
		80	—	0.8*	0.5*	1K	60	0	Low Power	TL022C	TI
	250	50	—	—	—	25K	65	0	2 op amp/comparators	**LM292**	**National (1054)**
										LM392	**National (1054)**
	500	50	10*	1*	0.6*	50K	70	0	Single Supply	MC3558	† Motorola
		200	1.5*	1	0.3*	25K	70	3	Matched Dual 709	RM1537	† Raytheon
			2-15*	1*	0.5*	50K	70	0	Dual 741	747M	† AMD
										1558	† AMD
										µA747M	† Fairchild
										µA1558M	† Fairchild
										MC1747	† Motorola

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Values

Bold face indicates additional data is provided on the page noted.

LINEAR–Operational Amplifiers-Characteristics (Cont'd)

Offset Voltage mv (25°C)	Bias Current na. (25°C)	Offset Current na. (25°C)	Voltage Drift µv/°C	Band-width MHz	Slew Rate v/µs	Voltage Gain v/v	CMRR db	Comp.	Comments	Device	Source	
Dual Units												**(Cont'd.)**
5.0	500	200	2-15*	1*	0.5*	50K	70	0	Dual 741			(Cont'd.)
										MC1558	† Motorola	
										LM747	† National	
										LM1558	† National	
										PM747	† PMI	
										PM1558	† PMI	
										CA747	† RCA	
										CA1558	† RCA	
										RM747	† Raytheon	
										RM1558	† Raytheon	
										MC1558	† Signetics	
										TDA1458	Signetics	
										µA747	† Signetics	
										SG747	† Silicon G	
										SG1558	† Silicon G	
										µA747M	† TI	
										MC1558	† TI	
										TA75458	Toshiba	
										TA75747	Toshiba	
									Low Noise	MC1558N	† Motorola	
					0.25	25K	70	3	Dual MC1709	MC1537	† Motorola	
			—	2	1.5*	50K	70	0	Dual Wideband 741	RM4558	† Raytheon	
										RM4558	† TI	
				2.5	1.5	50K	70	0	Dual Wideband 741	MC4558	† Motorola	
										MC4558A	Motorola	
									Low Noise	MC4558N	† Motorola	
				3	1.5	50K	70	0	3MHz min. Bandwidth	RM4559	† Raytheon	
				—	10	50K	70	0	High Slew Rate 1558	MC1558S	† Motorola	
	5000	500	10*	1*	0.01*	3.5K	70	3	General Purpose	MC1435	Motorola	
	7000	6000	—	2*	50	—	80	0	Transconductance Amplifier	**LM11600**	**† National**	**(1050)**
		8000	6000	—	2*	50	80	0	Transconductance Amplifier	**LM13600**	**National**	**(1050)**
										LM13600A	**National**	**(1050)**
6.0	0.2	0.05	10*	3*	13*	50K	80	0	Low Noise Bipolar-JFET	**XR072**	**Exar**	**(926)**
										XR072M	**† Exar**	**(926)**
										TL072AC	TI	
										TL072M	† TI	
		0.1	10*	1*	3.5*	4K	80	0	Low Power Bipolar-JFET	TL062AC	TI	
										TL062M	† TI	
				3*	13*	50K	80	0	Bipolar JFET	**XR082**	**Exar**	**(927)**
										XR082M	**† Exar**	**(927)**
										XR083	**Exar**	**(927)**
										XR083M	**† Exar**	**(927)**
										TL082AC	TI	
										TL082M	† TI	
										TL083AC	TI	
										TL083M	† TI	
	10	6	3*	1*	15*	50K	70	0	Multi-Purpose Programmable	µA776C	Fairchild	
	30	10	5*	0.27*	0.16*	50K	70	0	Low Power Adjustable Current	ICL8022C	Intersil	
			—	0.25*	0.16*	75K	70	0	Programmable Dual LM4250	LH24250C	National	
	250	50	7*	1*	0.6*	25K	65	0	Half LM244/324	LM258	Motorola	
										LM358	Motorola	
										NE532	**Signetics**	**(1109)**
										SA532	Signetics	
		75	10*	1*	0.6*	20K	70	0	Single Supply, I/O operates to ground	µA798C	Fairchild	
	500	200	—	1*	0.5*	20-50K	70	0	Dual 741C	1458	AMD	
										747C	AMD	
										XR1458	Exar	
										µA747C	Fairchild	

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Values

LINEAR–Operational Amplifiers-Characteristics (Cont'd)

Offset Voltage mv (25°C)	Bias Current na. (25°C)	Offset Current na. (25°C)	Voltage Drift µv/°C	Band-width MHz	Slew Rate v/µs	Voltage Gain v/v	CMRR db	Comp.	Comments	Device	Source
Dual Units											**(Cont'd.)**
6.0	500	200	—	1*	0.5*	20-50K	70	0	Dual 741C		(Cont'd.)
										µA1458C	Fairchild
										HA171458	Hitachi
										HA17747	Hitachi
										MC1458	Motorola
										MC1747C	Motorola
										LM747C	National
										LM1458	National
										µPC251	NEC America
										µPC1458	NEC America
										PM747C	PMI
										PM1458	PMI
										CA747C	RCA
										CA1458	RCA
										RC747	Raytheon
										RC1458	Raytheon
										µA747C	Signetics
										SA747C	Signetics
										MC1458	Signetics
										SA1458	Signetics
										SG747C	Silicon G
										SG1458	Silicon G
										µA747C	TI
										MC1458	TI
				2	0.5*	20K	70	0	Dual Wideband 741C	MC4558C	Motorola
									Low Noise	MC4558NC	Motorola
				3	1.5	20K	70	0	3MHz min. Bandwidth	**RC4559**	**Raytheon (1104)**
										RV4559	Raytheon
				3*	1	20K	70	0	Wideband 741	XR4558	Exar
										µA4558	Fairchild
										µPC4558	NEC America
										RC4558	Raytheon
										RC4558	TI
									Low Noise	XR4739	Exar
										RC4739	Raytheon
			10*	1*	0.8*	20K	70	0	Low Noise	MC1458N	Motorola
					10	20K	70	0	High Slew Rate 1458	MC1458S	Motorola
	1000	300	6*	—	—	10K	65	0	20ma output	TAA2761	Siemens
										TAA2765	Siemens
		500	—	—	—	12K*	70	2	Low Noise	TCA490	Signetics
	2000	1000	—	—	1*	6.5K	70	2	Low Noise	µA739	Fairchild
										TBA231	SGS
7.0	250	50	7*	1*	—	25K	65	0	Half LM224	LM358	Motorola
										LM358	National
										CA358	RCA
										LM358	Signetics
										NE532	**Signetics (1109)**
										LM258	TI
										LM358	TI
						100K	50	0	Low Power, Single Supply	LM2904	Motorola
										LM2904	National
										CA2904	RCA
										LM2904	TI
			—	—	—	100*	50K	0	2 op amp/comparators	**LM2924**	**National (1054)**
	500	50	—	1*	—	100K*	55*	0	258 type	TDA0358	Signetics
7.5	7	1	30	1*	0.3*	25K	80	1	Dual 308	LH2308	National
										PM2308	PMI
	250	50	30	1*	0.5*	25K	70	1	Dual High Performance	1501C	AMD
										LH2301A	AMD
										LH2301A	Intersil
										LH2301A	National

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† Military Temperature Range (−55° to 125°C)

* Typical Values

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LINEAR–Operational Amplifiers-Characteristics (Cont'd)

Offset Voltage mv (25°C)	Bias Current na. (25°C)	Offset Current na. (25°C)	Voltage Drift µv/°C	Band-width MHz	Slew Rate v/µs	Voltage Gain v/v	CMRR db	Comp.	Comments	Device	Source
Dual Units											**(Cont'd.)**
7.5	250	50	30	1*	0.5*	25K	70	1	Dual High Performance		(Cont'd.)
										LH2301A	Raytheon
										LH2301A	Signetics
	1500	500	1.5*	1*	0.3*	15K	65	3	Matched Dual 709	RC1437	Raytheon
					0.25*	15K	65	3	Matched Dual MC1709C	MC1437	Motorola
10.0	0.20	0.05	10*	3*	13*	25K	70	0	Low Noise Bipolar-FET	XR072C	Exar
										TL072C	TI
		0.10	10*	3*	13*	50K	70	0	Bipolar FET	**µA772C**	**Fairchild (938)**
				4*	13*	25K	70	0	Dual 351, wide band	**LF353**	**National (1035,1073)**
										SE571	**† Signetics (1112)**
	500	50	7*	1	0.6	20K	70	0	Single Supply	MC3458	Motorola
	30	15	12*	—	18*	3K	80	0	Darlington Input	TBC2332	† Siemens
	700	300	15*	1.1*	0.5*	20K	60	0	General Purpose	µA1458CC	Fairchild
										MC1458C	Motorola
	1500	600	—	—	—	10K	70	0	Audio Preamp	µA749D	Fairchild
15.0	0.20	0.10	10*	3*	13*	50K	70	0	Bipolar FET	**µA772L**	**Fairchild (938)**
	0.4	0.2	10*	1*	3.5*	3K	70	0	Low Power Bipolar-JFET	TL062C	TI
				3*	13*	25K	70	0	Bipolar-JFET	**XR082C**	**Exar (927)**
										XR083C	**Exar (927)**
										TL082C	TI
										TL083C	TI
		800*	—	—	—	32K*	—	0	Audio 5 watts/channel	DA-101	Delco
	50	25	12*	—	18*	3K	65	0	Darlington Input	TBB2331	Siemens
										TBE2335	Siemens
20.0	0.02	0.0005*	75	1*	6*	50K	70	0	FET Input Dual	ICL8043M	† Intersil
50.0	0.05	0.0005*	75	1*	6*	20K	70	0	FET Input Dual	ICL8043C	Intersil
Triple Units											
3.0	30	7.5	5*	0.27*	0.16*	50K	70	0	Low Power Programmable	ICL8023M	† Intersil
5.0	70	14	—	0.02*	0.1*	—	70	0	Micropower, Transconductance Amplifier	CA3060	† RCA
	200	50	3.3*	0.6*	0.4*	3K	80	0	Programmable	L144A	† Siliconix
										L144B	Siliconix
	550	100	—	0.045*	1*	—	70	0	Micropower, Transconductance Amplifier	CA3060	† RCA
	5000	1000	—	0.11*	8*	—	70	0	Micropower, Transconductance Amplifier	CA3060	† RCA
6.0	30	10	5*	0.27*	0.16*	50K	70	0	Low Power Programmable	ICL8023C	Intersil
7.0	150	50	—	2*	0.7*	20K	70	0	Low Power, Programmable	SL144C	Siltronics
10.0	250	70	3.3*	0.6*	0.4*	1K	70	0	Programmable	L144C	Siliconix
	2000	200*	—	5	0.46	4K*	90*	2	Supply ±6 v	TCA220	Signetics
Quad Units											
0.5	300	20	10	1.5	0.7	100K	100	0	Symmetrical, Matched	OP-09A	† PMI
										OP-09E	PMI
										OP-11A	† PMI
										OP-11E	PMI
2.0	0.10	0.05	10*	3*	13*	50K	80	0	Bipolar FET	**µA774A**	**† Fairchild (938)**
				4*	13*	50K	80	0	Wideband, Quad 351A	**LF347A**	**National (1035)**
	50	10	20	1*	—	50K	70	0	Low Power	LM124A	† AMD

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Values

LINEAR–Operational Amplifiers-Characteristics (Cont'd)

Offset Voltage mv (25°C)	Bias Current na. (25°C)	Offset Current na. (25°C)	Voltage Drift µV/°C	Band-width MHz	Slew Rate v/µs	Voltage Gain v/v	CMRR db	Comp.	Comments	Device	Source
Quad Units											**(Cont'd.)**
2.0	50	10	20	1*	—	50K	70	0	Low Power		(Cont'd.)
										LM124A	**† National (1035)**
										LM124A	Signetics
2.5	200	75	2*	8*	4*	100K	86	0	Wideband	**HA-4602-2**	**† Harris (998,1000)**
	500	50	15	1.5	0.7	100K	100	0	Symmetrical, Matched	OP-09B	† PMI
										OP-09F	PMI
										OP-11B	† PMI
										OP-11F	PMI
3.0	0.2	0.05	10*	3*	13*	50K	80	0	Low Noise, Bipolar-JFET	TL074BC	TI
										TL064AC	TI
		0.1	10*	1*	3.5*	4K	80	0	Low Power Bipolar-JFET	TL064BC	TI
				3*	3	50K	80	0	JFET	TL084BC	TI
	80	15	20	1*	—	50K	70	0	Low Power	LM224A	AMD
										LM224A	National
										LM224A	Signetics
	100	30	30	1*	—	25K	65	0	Low Power	LM324A	AMD
										LM324A	National
										LM324A	Signetics
	200	30	5*	3	1.2	25K	80	0	Noise 2µV max	RM4156	† Raytheon
					3.5*	1.6*	50K	80	0	XR741M	† Exar
				3.5*	1.6*	50K	80	0	Quad 741	**HA-4741-2**	**† Harris (1002)**
										HA4741-2	† Raytheon
3.5	300	100	2*	8*	4*	75K	80	0	Wideband	**HA-4605-5**	**Harris (1000)**
4.0	400	50	5*	1*	1.2*	50K	70	0	LM124 with improved output	RM3503A	† Raytheon
5.0	0.10	0.10	10*	3*	13*	50K	80	0	Bipolar FET	**µA774**	**† Fairchild (938)**
	0.20	0.10	10*	4*	13*	50K	80	0	Wideband, Quad 351B	LF347B	National
	100	10	—	1*	0.4*	50K	70	0	Programmable, Low power	**XR146**	**Exar (929)**
										LM146	**† National (1035)**
		25	—	1*	0.5*	50K	70	0	Quad 741 with standard npn input stage		
										LM148	† AMD
										µA148	† Fairchild
										LM148	† Intersil
										LM148	† Motorola
										LM148	**† National (1035)**
										LM148	† Raytheon
										LM148	† TI
				4*	2.0*	50K	70	0	Wideband quad 741 for gains >5	LM149	† AMD
										LM149	† Intersil
										LM149	† National
										LM149	† Raytheon
		40	—	0.8*	0.5*	4K	60	0	Low Power	TL044M	† TI
	150	30	7*	1*	—	50K	70	0	Single Supply; I/O Operates to ground		
										LM124	† AMD
										LM224	AMD
										µA124	† Fairchild
										LM124	† Intersil
										LM124	† Motorola
										LM224	Motorola
										LM124	**† National (1035)**
										LM224	National
										LM124	† Raytheon
										CA124	† RCA
										LM124	† Signetics
										LM224	Signetics
										SG124	† Silicon G
										LM124	† TI
										LM224	TI

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† Military Temperature Range (−55° to 125°C) * Typical Values

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LINEAR–Operational Amplifiers-Characteristics (Cont'd)

Offset Voltage mv (25°C)	Bias Current na. (25°C)	Offset Current na. (25°C)	Voltage Drift µv/°C	Band-width MHz	Slew Rate v/µs	Voltage Gain v/v	CMRR db	Comp.	Comments	Device	Source
Quad Units											**(Cont'd.)**
5.0											(Cont'd.)
	200	50	—	1.5*	0.6*	25K	80	0	Low Power	ULN-4236A	Sprague
										ULN-4436A	Sprague
	250	80	—	0.8	0.5*	1K	60	0	Low Power	TL044C	TI
	300	50	5*	3	1.2	25K	80	0	Noise 2µV max	**RC4156**	**Raytheon (1110)**
										RV4156	Raytheon
				3.5*	1.6*	25K	80	0	Quad 741	XR4741C	Exar
										HA-4741-5	**Harris (1002)**
										HA4741-5	Raytheon
			—	3*	1*	25K	80	0	Quad 741	ULN-4136A	Sprague
										ULN-4336A	Sprague
	500	50	10*	1*	0.6*	50K	70	0	Single Supply; I/O Operates to ground		
										XR3503	† Exar
										µA3503M	† Fairchild
										MC3503	† Motorola
										RM3503	† Raytheon
										MC3503	† TI
									2 op amps, 2 comparators	MC3505	Motorola
			—	2	1.5*	5K	70	0	Programmable Quad 741	**XR4202**	**Exar (930)**
										MC4202	Motorola
					1.6*	20K	70	0	Low Noise, Low Power	XR4212M	† Exar
		200	15*	1	0.5*	50K	70	0	Quad 741	MC4741	† Motorola
			—	3*	1.5*	50K	70	0	Quad 741, High Gain	XR4136M	† Exar
										µA4136M	† Fairchild
										PM4136	† PMI
										RM4136	† Raytheon
										RM4136	† TI
6.0	0.2	0.05	—	8	20	50K	80	0	FET, wideband	MC3571	† Motorola
			10*	3*	13*	50K	80	0	Low Noise Bipolar-JFET	**XR074**	**Exar (926)**
										XR074M	**† Exar (926)**
										TL074AC	TI
										TL074M	† TI
		0.1	10*	1*	3.5*	4K	80	0	Low Power Bipolar-JFET	TL064C	TI
										TL064AC	TI
										TL064M	† TI
				3*	13*	50K	80	0	Bipolar JFET	**XR084**	**Exar (927)**
										XR084M	**† Exar (927)**
										TL084AC	TI
										TL084M	† TI
										TL085AC	TI
									Programmable, Bipolar - JFET	**XR094**	**Exar (928)**
										XR094M	**† Exar (928)**
										XR095	Exar
										XR095M	**† Exar (928)**
	200	50	—	1*	0.5*	25K	70	0	Quad 741 with standard npn input stage		
										LM248	AMD
										LM348	AMD
										µA248	Fairchild
										µA348	Fairchild
										LM248	Intersil
										LM348	Intersil
										LM248	Motorola
										LM348	Motorola
										LM248	National
										LM348	National
										LM248	Raytheon
										LM348	Raytheon
										LM248	TI
										LM348	TI

(Continued)

† Military Temperature Range (−55° to 125°C) * Typical Values

LINEAR–Operational Amplifiers-Characteristics (Cont'd)

Offset Voltage mv (25°C)	Bias Current na. (25°C)	Offset Current na. (25°C)	Voltage Drift µv/°C	Band-width MHz	Slew Rate v/µs	Voltage Gain v/v	CMRR db	Comp.	Comments	Device	Source
Quad Units											**(Cont'd.)**
											(Cont'd.)
6.0	200	50	—	4*	2*	25K	70	0	Wideband quad for gains>5	LM249	AMD
										LM349	AMD
										µA349	Fairchild
										LM249	Intersil
										LM349	Intersil
										LM249	National
										LM349	National
										LM249	Raytheon
										LM349	Raytheon
	500	50	—	1*	1.2*	25K	70	0	LM324 with improved output	RC3403A	† Raytheon
										RV3403A	Raytheon
				2	1.6	5K	70	0	Quad 741	XR4212C	Exar
		100	—	1*	0.4*	25K	70	0	Programmable, Low power	**XR246**	**Exar (929)**
										XR346	**Exar (929)**
										LM246	National
										LM346	National
		200	—	3*	1*	20K	60-70	0	Quad 741	XR4136C	Exar
										µA4136C	Fairchild
										µPC4136	NEC America
										PM4136C	PMI
										RC4136	Raytheon
										RV4136	Raytheon
										RC4136	† TI
				1*	0.5*	20K	70	0	Quad 741	MC4741C	Motorola
	1000	300	6*	—	—	10K	65	0	20ma output	TAA4761	Siemens
										TAA4765	Siemens
7.0	150	30	—	—	—	20K	60	0	Single Supply	TA75902	Toshiba
	250	50	7*	1*	—	25K	65	0	Single Supply; I/O Operates to ground		
										LM324	AMD
										µA224	Fairchild
										µA324	Fairchild
										LM224	Intersil
										LM324	Intersil
										LM324	Motorola
										LM324	National
										CA224	RCA
										CA324	RCA
										LM224	Raytheon
										LM324	Raytheon
										LM224	Signetics
										LM324	Signetics
										SA534	Signetics
										SG224	Silicon G
										SG324	Silicon G
										LM224	TI
										LM324	TI
						100K*	50	0	Single Supply	HA17902	Hitachi
										LM2902	National
	500	50	—	—	—	100K*	85*	0	324 type	µPC324	NEC America
										µPC451	NEC America
						100K	50	0	Single Supply	µPC2902	NEC America
7.5	500	50	—	1*	—	100K*	85*	0	Single supply, 324 type	TDA0324	Signetics
8.0	500	75	10*	1*	0.6*	20K	70	0	Single Supply: I/O Operates to ground		
										XR3303	Exar
										µA330C	Fairchild
										MC3303	Motorola
10.0	0.20	0.05	10*	3*	13*	25K	70	0	Low Noise Bipolar-JFET	**XR074C**	**Exar (926)**
										TL074C	**TI**
										TL075C	TI

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Values

Bold face indicates additional data is provided on the page noted.

LINEAR–Operational Amplifiers-Characteristics (Cont'd)

Offset Voltage mv (25°C)	Bias Current na. (25°C)	Offset Current na. (25°C)	Voltage Drift µv/°C	Band-width MHz	Slew Rate v/µs	Voltage Gain v/v	CMRR db	Comp.	Comments	Device	Source
Quad Units											**(Cont'd.)**
10.0	0.20	0.05									(Cont'd.)
			0.10	5	15*	25K	70	0	Bipolar-JFET, Quad 351	**LF347**	**National (1035,1073)**
		0.10	10*	3*	13*	50K	70	0	Bipolar FET	**µA774C**	**Fairchild (938)**
	500	50	10*	1*	0.6*	20K	70	0	Single Supply; I/O Operates to ground		
										XR3403	Exar
										µA3403	Fairchild
										MC3403	Motorola
										RC3403	Raytheon
										MC3403	TI
									2 op amps, 2 comparators	MC3405	Motorola
			—	1*	2*	15K	70	0	LM224 with improved output	RV3403A	Raytheon
				—	—	100K	85*	0	Extended Temp LM224	LM2902	Motorola
										LM2902	Raytheon
										LM2902	Signetics
										LM2902	TI
	600	300	—	3*	1*	15K	60	0	Quad 741	RC4136C	Raytheon
										RC4136C	TI
15.0	0.20	0.05	—	7*	20	25K	70	0	FET, wideband	MC3471	Motorola
		0.10	10*	3*	13*	50K	70	0	Bipolar FET	**µA774L**	**Fairchild (938)**
	0.40	0.2	10*	1*	3.5*	3K	70	0	Low Power Bipolar-JFET	TL064C	TI
				3*	13*	25K	70	0	Bipolar FET	XR084C	Exar
										TL084C	TI
										TL085C	TI
									Programmable Bipolar - JFET	**XR094C**	**Exar (928)**
										XR095C	**Exar (928)**
	50	25	12*	—	—	3K	65	0	Darlington Input	TBB4331	Siemens
										TBE4335	Siemens
—	100	—	—	2.5*	0.5/20*	2K	—	0	Current Mirror, Single Supply	LM1900	† National
										LM1900	†TI
	200	—	—	2.5*	0.5/20*	1.2K	—	0	Current Mirror, Single Supply	LM2900	National
										LM3900	**National (1035)**
										LM2900	Raytheon
										LM3900	Raytheon
										LM2900	TI
										LM3900	TI
	300	—	—	4*	0.6*	1K	—	0	Current Mirror, Single Supply	µA3301C	Fairchild
										MC3301	Motorola
										RC3301	Raytheon
				2.5*	0.5/20*	1.2K	—	0	Current Mirror, Single Supply	LM3301	National
										LM3401	National
				5*	0.6*	1K	—	0	Current Mirror, Single Supply	µA3401C	Fairchild
										MC3401	Motorola
										CA3401	†RCA
										RC3401	Raytheon
Hex Units											
5	100	25	—	1.0	0.5	25K	70	0	Hex 741 W/NPN input	TL326M	†TI
6	200	50	—	1.0	0.5	15K	70	0	Hex 741 W/NPN input	TL326C	TI

† Military Temperature Range (−55° to 125°C)

* Typical Values

LINEAR–Phase Locked Loops/Synthesizers

Phase Locked Loop Circuits

Note: Stereo Decoders are listed under Consumer Circuits

Function	Device	Source	
Counter Logic Control	SP8790	Plessey	
Counter Control Logic (Use with MC12012 for high frequency programming)	MC12014	Motorola	
Crystal Oscillator (0.1 to 2.0 MHz)	MC12060	Motorola	
	MC12560	† Motorola	
Crystal Oscillator (2 to 20 MHz)	MC12061	Motorola	
	MC12561	† Motorola	
Digital Mixer	MC12000	Motorola	
Double Balanced Mixer	MC12002	Motorola	
	MC12502	† Motorola	
FSK Modulator/Demodulator	XR210	Exar	
	XR210M	† Exar	
	XR2211	**† Exar**	**(922)**
	XR2211M	**† Exar**	**(922)**
	XR2211C	**Exar**	**(922)**
	XR2212C	**Exar**	**(923)**
	XR2212M	**† Exar**	**(923)**
	XR2211C	Raytheon	
	XR2211M	† Raytheon	
Offset Control System (for synthesizer tuned transceivers)	MC12020	Motorola	
	MC12021	Motorola	
	MC12520	† Motorola	
	MC12521	Motorola	
Phase Comparator and Programmable Counter	MC14568BA	† Motorola	
	MC14568BC	Motorola	
Phase-Frequency Detector	11C44C	Fairchild	
	MC4044	Motorola	
	MC4344	† Motorola	
	MC12040	Motorola	
	MC12540	† Motorola	
Phase Locked Loop	**XR215**	**Exar**	**(922)**
	XR215M	**† Exar**	**(922)**
	M5136	Mitsubishi	
	M51361	Mitsubishi	
	SL652	Plessey	
	NE564	**Signetics**	**(1111)**
	SE564	**† Signetics**	**(1111)**
	SN54LS297	† TI	
	SN74LS297	TI	
Phase Locked Loop (CMOS)	F4046BC	Fairchild	
	F4046BM	† Fairchild	
	SIL4046B	† Mitel	
	SIL4046BE	Mitel	
	MC14046BA	† Motorola	
	MC14046BC	Motorola	
	CD4046BC	National	
	CD4046BM	† National	
	CD4046B	† RCA	
	CD4046BE	RCA	
	SCL4046B	† SSS	
	SCL4046BE	SSS	

(Continued)

Phase Locked Loop Circuits (Cont'd.)

Function	Device	Source	
Phase Locked Loop (CMOS) (Cont'd.)	SCL4446B	† SSS	
	SCL446BE	SSS	
Phase Locked Loop for Motor Control; See Linear-Consumer Circuits, Motor Speed Regulator			
Phase Locked Loop Control (Oscillator, programmable divider, phase comparator)	MP7156	Micro Power	
	SP8760	Plessey	
PLL Peripheral (VCO, mixer, amp for CB)	LM1861	National	
	LM1862	National	
	AN103	Panasonic	
	TA7310	Toshiba	
Prescaler, for AM/FM	TD6101	Toshiba	
	TD6102	Toshiba	
Prescaler, for FM radio	DS8629	National	
	SP8627	Plessey	
	SP8628	Plessey	
	SP8629	Plessey	
Programmers and Controllers for Citizens Band See Linear-Consumer Circuits			
Programmer, for CB Synthesizer	MM57190	National	
Synthesizer	TC9100	Toshiba	
Synthesizer, 200 channel, for AM/FM	**8X08**	**Signetics**	**(1124)**
Synthesizer (Programmable Divider, to 1021 channels, adder, phase comparator)	HCTR0320	Hughes	
Synthesizer, AM/FM Tuner (2 device set)	TC9123	Toshiba	
	TC9124	Toshiba	
Synthesizer, Citizens Band	11C84	Fairchild	
	11C85	Fairchild	
	HCTR0347	Hughes	
	MP7139	Micro Power	
	MP7189	Micro Power	
	MC145104	Motorola	
	MC145106	Motorola	
	MC145107	Motorola	
	MC145109	Motorola	
	MC145112	Motorola	
	DS8900	National	
	LM1861	National	
	LM1862	National	
	MM55104	National	
	MM55106	National	
	MM55107	National	
	MM55108	National	
	MM55109	National	
	MM55110	National	
	MM55114	National	
	MM55116	National	
	MM55122	National	
	μPD861	NEC America	
	NC6400A	Nitron	
	NC6402B	Nitron	
	NC6403	Nitron	
	NC6405A	Nitron	

(Continued)

Phase Locked Loop Circuits (Cont'd.)

Function	Device	Source	
Synthesizer, Citizens Band (Cont'd.)	MSM5807	OKI	
	MN6040	Panasonic	
	MN6040A	Panasonic	
	MN6040B	Panasonic	
	SP8920	Plessey	
	SP8921	Plessey	
	SP8922	Plessey	
	SP8923	Plessey	
	LC7110	Sanyo	
	NE575	Signetics	
	TC9102	Toshiba	
	TC9106	Toshiba	
	TC9107	Toshiba	
Synthesizer/Programmer, CB	DS8900	National	
	TC9112	Toshiba	
Synthesizer, AM/FM/CB/SW	MM55117	National	
	MM55118	National	
	MM55119	National	
	MM55120	National	
Synthesizer, CB/Marine Radio, to 82 channels	NC6400	Nitron	
	NC6405A	Nitron	
Synthesizer, T.V., dual 82 channels	NC6410A	Nitron	
Synthesizer, Externally Programmable	NC6422	Nitron	
	NC6423	Nitron	
Synthesizer (Programmable Dividers, Phase Comparator)	S187	Siemens	
Tone Decoder	XR567C	Exar	
	XR567M	† Exar	
	XR2211C	**Exar**	**(922)**
	XR2211M	**† Exar**	**(922)**
	LM567	† National	
	LM567C	National	
	XR2211C	Raytheon	
	XR2211M	† Raytheon	
	NE567	Signetics	
	SE567	† Signetics	
Dual Tone Decoder	XR2567C	Exar	
	XR2567M	† Exar	
	XR2567C	Raytheon	
	XR2567M	† Raytheon	
Dual Tone Decoder/Receiver	MT8820A	† Mitel	
	MT8820AE	Mitel	
Tone Generator	FX205	CMA	
Two Modulus Prescaler (÷3/4)	SP8720	Plessey	
	SP8725	Plessey	
Two Modulus Prescaler ÷4/8)	TD6102	Toshiba	
	11C91C	Fairchild	
	11C91M	† Fairchild	
	95H91C	Fairchild	
	95H91M	† Fairchild	
	MC12009	Motorola	

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Values

Bold face indicates additional data is provided on the page noted.

LINEAR–Phase Locked Loops/Synthesizers (Cont'd)

Phase Locked Loop Circuits (Cont'd.)

Function	Device	Source	Line
Two Modulus Prescaler ÷4/8) (Cont'd.)			
	MC12509	† Motorola	
	SP8740	Plessey	
	SP8745	Plessey	
Two Modulus Prescaler (÷6/7)			
	SP8741	Plessey	
	SP8746	Plessey	
Two Modulus Prescaler (÷8/9)			
	MC12011	Motorola	
	MC12511	† Motorola	10
	SP8743	Plessey	
	SP8748	Plessey	
Two Modulus Prescaler (÷10/11)			
	11C90C	Fairchild	
	11C90M	† Fairchild	
	95H90C	Fairchild	
	95H90M	† Fairchild	
	MC12013	Motorola	
	MC12513	† Motorola	
	MSL2318	OKI	20
	SP8640	Plessey	
	SP8641	Plessey	
	SP8642	Plessey	
	SP8643	Plessey	
	SP8646	Plessey	
	SP8647	Plessey	
	SP8685	Plessey	
	SP8690	Plessey	
	SP8695	Plessey	
	TD6101	Toshiba	30
Two Modulus Prescaler (÷5/6, 10/11, 10/12)			
	MC12012	Motorola	
Two Modulus Prescaler(÷20/22)			
	SP8785	Plessey	
	SP8786	Plessey	
Two Modulus Prescaler (÷248/256)			
	11C83	Fairchild	
Count Extender, ÷8 (extends division ratio of a Two Modulus Prescaler while retaining the difference, ie÷10/11 becomes ÷80/81)			40
	SP8794A	† Plessey	
	SP8794B	Plessey	
	SP8794M	Plessey	
Count Extender, ÷4, ÷10/11 becomes ÷40/41			
	SP8790A	† Plessey	
	SP8790B	Plessey	
	SP8790M	Plessey	
For other Prescalers see Digital-Special, Dividers, Digital-ECL			
VCO			50
	11C58C	Fairchild	
	MC1648	† Motorola	
	MC1658	Motorola	
	SP1648	Plessey	
	SP1658	Plessey	
	SN54LS324	† TI	
	SN74LS324	TI	
VCO and Phase Comparator			
	LM565	Motorola	
	LM565	National	60
	LM565C	† National	
	NE560	Signetics	
	SE560	† Signetics	
	NE561	Signetics	
	SE561	† Signetics	

(Continued)

Phase Locked Loop Circuits (Cont'd.)

Function	Device	Source	Line
VCO and Phase Comparator (Cont'd.)			
	NE562	Signetics	
	SE562	† Signetics	
	NE565	Signetics	
	SE565	† Signetics	70
	TA7133	Toshiba	
VCO-Function Generator, (Includes square and triangular waveforms - but not sine.)			
	XR2207	**Exar (925)**	
	XR2207C	**Exar (925)**	
	XR2209C	**Exar (925)**	
	XR2209M	**† Exar (925)**	
	LM566	National	
	LM566C	† National	
	XR2207C	Raytheon	80
	XR2207M	† Raytheon	
	XR2209C	Raytheon	
	XR2209M	† Raytheon	
	NE566	Signetics	
	SE566	† Signetics	
VCO-Waveform Generator (pulse, sawtooth and triangle)			
	SSM2030	**SSM (564)**	
VCO-Waveform Generator (Includes sinewave output among its functions)			90
	XR205	Exar	
	XR2206	**† Exar (924)**	
	XR2206C	**Exar (924)**	
	XR2206M	**† Exar (924)**	
	XR8038	Exar	
	XR8038M	† Exar	
	ICL8038C	Intersil	
	ICL8038M	† Intersil	
VCO, Amplifier, Analog Multiplier			
	XR-S200	Exar	100
	XR205	Exar	
VCO, Phase Comparator, Multiplier			
	SL651	Plessey	
VCO, Phase Comparator Multiplier, with Auxiliary Amplifier			
	SL650	† Plessey	
Dual VCO			
	11C24C	Fairchild	
	MC4024	Motorola	
	MC4324	† Motorola	110
	SN54LS124	† TI	
	SN54S124	† TI	
	SN74LS124	TI	
	SN74S124	TI	
	SN54LS325	TI	
	SN74LS325	TI	
	SN54LS326	† TI	
	SN74LS326	TI	
	SN54LS327	† TI	
	SN74LS327	TI	120
	SN54LS328	† TI	
	SN74LS328	TI	

† Military Temperature Range (−55° to 125°C)

* Typical Values

LINEAR–Telecommunication Circuits

Telecommunication Circuits

Function	Device	Source	Line
Address Selector (Gives output if sequential input is entered in a fixed order within a maximum time interval)	7511-01	Telaris	
Baseband Modulator/Demodulator (50db carrier suppression)	SL1001	Plessey	
Baseband Channel Amplifier (24-27db amplifier)	SL1020	Plessey	
Codec, μ255 Law	S2900	AMI	10
	S2901	AMI	
	2910	Intel	
	MK5150	Mostek	
	LF3700	National	
	MM58100	National	
	TP3001	**National (1074)**	
	NC331	Nitron	
	NC332	Nitron	
	ST100	**Signetics (1106)**	20
	DF331	**Siliconix (1133)**	
	DF332	**Siliconix (1133)**	
Codec, A Law	2911	Intel	
	MK5155	Mostek	
	MC14406	**Motorola (1030)**	
	MC14407	**Motorola (1030)**	
	LF3700	National	
	MM58150	National	
	TP3002	**National (1074)**	30
	NC341	Nitron	
	NC342	Nitron	
	SM61A	Siemens	
	S291	Siemens	
	DF341	Siliconix	
	DF342	Siliconix	
Codec, μ255/A Law	AY3-9900	GI	
	SM61B	Siemens	
	S291	Siemens	40
Compander (Signal Compressor/Expander)	XR2216	Exar	
	LM2704	National	
	LM2705	National	
	LM2706	National	
	LM2707	National	
	LM3704	National	
	LM3705	National	
	LM3706	National	
	LM3707	National	50
	L150	SGS	
	NE570	**Signetics (1112)**	
	SE570	**† Signetics (1112)**	
	NE571	**Signetics (1112)**	
Companding Analog to Digital Converter	MN5110	Micro Net	
	MN5111	Micro Net	
	NC331	Nitron	
	NC341	Nitron	
	DF331	**Siliconix (1133)**	60
	DF341	Siliconix	
Companding Digital to Analog Converter	NC332	Nitron	
	NC342	Nitron	
	DF332	**Siliconix (1133)**	
	DF342	Siliconix	

Telecommunication Circuits (Cont'd.)

Function	Device	Source	Line
Companding A/D and D/A Converter	LF2700	National	
	MM8100	National	
Delta Modulation System, Continuously Variable Slope	FX209	CMA	70
	FX309	CMA	
	HC55516-2	† Harris	
	HC55516-8	† Harris	
	HC55516-9	Harris	
	HC55532-2	† Harris	
	HC55532-8	† Harris	
	HC55532-9	Harris	
	MC3417	Motorola	
	MC3418	Motorola	80
Dialer, Microcomputer (clock, stopwatch, redial, 16/32 number)	TZ2001	GI	
Dialer, Push Button Telephone Dialer Circuit (Converts push button inputs to pulses)	**S2560**	**AMI (642)**	
	AY5-9100	GI	
	AY5-9106	GI	
	AY5-9110	GI	
	AY5-9118	GI	90
	AY5-9120	GI	
	AY5-9151	GI	
	AY5-9152	GI	
	AY5-9153	GI	
	AY5-9154	GI	
	AY9-9600	GI	
	MT4320	Mitel	
	MT4321	Mitel	
	MT4322	Mitel	
	MT4325	Mitel	100
	MK5098	Mostek	
	MK5099	Mostek	
	MC14408	Motorola	
	MC14409	Motorola	
	MM5393	National	
	NC320	Nitron	
	NC321	Nitron	
	NC322	Nitron	
	CRC8000	Rockwell	
	CRC8001	Rockwell	110
	S120	Siemens	
	DF320	Siliconix	
	DF321	Siliconix	
	DF322	Siliconix	
Dialer Memory (16 x 4 for Push Button Dialing)	S121	Siemens	
Dialer, Repertory	**S2562**	**AMI (646)**	
	AY5-9200	GI	
	MK5170	Mostek	120
	SFF19200	NPC	
(Dialer) Clock Generator (for AY5-9100/9200)	AY5-9500	GI	
Tone Decoder (Three tone, 8 combinations sequential code receiver)	FX307	CMA	
Tone Decoder (Operates from 0.01 Hz to 500 kHz)	XR567	† Exar	
	XR567C	Exar	
	XR2211C	**Exar (922)**	130
	XR2211M	**† Exar (922)**	
	LM567	† National	
	LM567C	National	

(Continued)

Telecommunication Circuits (Cont'd.)

Function	Device	Source	Line
Tone Decoder (Operates from 0.01 Hz to 500 kHz) (Cont'd.)	XR2211C	Raytheon	
	XR2211M	† Raytheon	
	NE567	Signetics	
	SE567	† Signetics	
Dual Tone Decoder (Operates from 0.01 Hz to 500 kHz)	XR2567	Exar	140
	XR2567M	† Exar	
	XR2567C	Raytheon	
	XR2567M	† Raytheon	
Dual Tone Decoder	AY5-9801	GI	
	AY5-9802	GI	
	AY5-9803	GI	
	AY5-9804	GI	
	AY5-9805	GI	150
	AY5-9806	GI	
	AY5-9807	GI	
	AY5-9808	GI	
	AY5-9821	GI	
	AY5-9822	GI	
	AY5-9823	GI	
	AY5-9824	GI	
	AY5-9825	GI	
	AY5-9826	GI	
	AY5-9827	GI	160
	AY5-9828	GI	
	MT8820	Mitel	
	CRC8030	Rockwell	
	7516-01	Telaris	
Dual Tone Receiver Circuit (with filters)	MH88200	Mitel	
	MH88205	Mitel	
Dual Tone Receiver Circuit (combine with filters for touch tone receiver)	MT8820	Mitel	170
	MK5102-5	Mostek	
	AF104	National	
	AF106	National	
	AF107	National	
	AF108	National	
	AF110	National	
	SM301	Siemens	
	7640-01	Telaris	
Quad Tone Decoder	883-5	Beckman	180
Tone Ringer (operates from ring signal, drives speaker)	**S2561**	**AMI (644)**	
	ML8204	Mitel	
	ML8205	Mitel	
Dual Squaring Translator with Squelch (for touchtone systems)	FM900	BEI	
Relay Driver (For 48v telephone relays)	AY5-9050	GI	190
	DS1686	† National	
	DS1687	† National	
	DS3686	National	
	DS3687	National	
	UDN-2580	Sprague	
	UDN-2956	Sprague	
	UD7-2957	Sprague	

† Military Temperature Range (−55° to 125°C)

* Typical Values

Bold face indicates additional data is provided on the page noted.

LINEAR–Telecommunication Circuits (Cont'd)

Telecommunication Circuits (Cont'd.)

Function	Device	Source	Line
Encoder 2 of 8 keyboard to Binary Encoder (4 x 4 Key Input to 4 line output)	MC14419	Motorola	
Bandpass (touchtone) Filters	883-X	†Beckman	
	FM951	BEI	
	FM952	BEI	
	FM953	BEI	
	FM954	BEI	
	CH1295	Cermetek	
	CH1296	Cermetek	
	ACF7323C	GI	10
	ACF7363C	GI	
	ACF7383C	GI	
	ACF7711C	GI	
	AF101	National	
	AF102	National	
	AF103	National	
	AF111	National	
	AF112	National	
	AF113	National	
	AF114	National	20
Bandpass Filters	ACF7310C	GI	
	ACF7311C	GI	
	ACF7320C	GI	
	AF99	National	
Bandpass Filter and Detector	ACF7300C	GI	
Filter, Dial Tone Suppression	ACF7401C	GI	
Filter, 2600Hz Suppression	ACF7410C	GI	30
Filter, PCM	ACF7270C	GI	
	ACF7271C	GI	
	ACF7272C	GI	
	ACF7273C	GI	
	AF132	National	
	AF133	National	
	AF134	National	40
Dual Tone Generator (Touchtone Frequencies)	**S2559**	**AMI**	**(638)**
	S2559A	**AMI**	**(638)**
	S2559B	**AMI**	**(638)**
	S2559C	**AMI**	**(638)**
	S2559D	**AMI**	**(638)**
	ICM7206	Intersil	
	ICM7206A	Intersil	
	ICM7206B	Intersil	
	MK5086-1	Mostek	50
	MK5086-2	Mostek	
	MK5087	Mostek	
	MK5089	Mostek	
	MK5090	Mostek	
	MK5091	Mostek	
	MC14401	Motorola	
	MC14403	Motorola	
	MC14405	Motorola	
	MC14410	Motorola	
	MM5395	National	60
	S359	Siemens	
	7603-01	Telaris	
	7603-02	Telaris	
Dual Tone Generator (Generates 12-16 tone pairs)	AY3-9400	GI	
	AY3-9401	GI	

(Continued)

Telecommunication Circuits (Cont'd.)

Function	Device	Source	Line
Dual Tone Generator (Generates 12-16 tone pairs) (Cont'd.)	AY3-9410	GI	
	AY9-9086	GI	
Gyrator	TCA580	Signetics	70
	AF120	National	
Limiter (limits voltage on two-wire speech)	U225	Telefunken	
Tri-port Memory(T1 carrier)	R8040	Rockwell	
Serial Reciever(changes T1-D2 or T1-D3 input to parallel output)	R8060	Rockwell	
Serial Transmitter (Generates 193-Bit data stream in T1-D2 or T1-D3 format)	R8050	Rockwell	80
Dual Limiter (Touchtone Amplitude Limiter)	883-4	Beckman	
Modem, Frequency Division Multiplex Transmitter and Receiver	LM1823	National	
	LM1826	National	
Modem (Frequency-Shift Keying Modulator/Demodulator)	XR210	Exar	
	XR210M	†Exar	
	MC14412	Motorola	
	ESM501	NPC	90
Modem, FSK Modulator	**XR2206**	**Exar**	**(924)**
	XR2206M	**†Exar**	**(924)**
	XR2207	**Exar**	**(925)**
	XR2207M	**†Exar**	**(925)**
Modem, FSK Demodulator	**XR2211**	**Exar**	**(922)**
	XR2211M	**†Exar**	**(922)**
Modem (For Serial Communications at up to 600 bps)	MC6860	Motorola	100
Modem Circuits, for 103/113 and other FSK systems	CH1213	Cermetek	
	CH1214	Cermetek	
	CH1223	Cermetek	
	CH1224	Cermetek	
	CH1252	Cermetek	
	CH1257	Cermetek	110
	CH1262	Cermetek	
	CH1267	Cermetek	
	CH1271	Cermetek	
	CH1272	Cermetek	
	CH1273	Cermetek	
	CH1280	Cermetek	
Modem Circuits, for CCITT FSK System	CH1215	Cermetek	
	CH1216	Cermetek	120
	CH1225	Cermetek	
	CH1226	Cermetek	
	CH1253	Cermetek	
	CH1258	Cermetek	
	CH1259	Cermetek	
	CH1263	Cermetek	
	CH1268	Cermetek	
	CH1276	Cermetek	
PCM Repeater	XR-C240	Exar	130

(Continued)

Telecommunication Circuits (Cont'd.)

Function	Device	Source	Line
PCM Repeater (Cont'd.)	XR-C277	Exar	
Signal Processing Peripheral	S2811	AMI	
Telephone Restricter	CRN330	NPC	
Digital Filter Switch (Tone Decoder)	FX105	CMA	
Frequency Sensitive Switch (Provides two set points adjustable with external components.)	FX101	CMA	140
Frequency Sensitive Switch (Provides set points with widely adjustable hysteresis)	FX301	CMA	
Frequency Sensitive Switch (Provides two set points and three state outputs)	FX401	CMA	
Tone Operated Switch (Bistable tone operated switch)	FX501	CMA	
Tone Operated Monostable Timer (Tone operated for remote switching)	FX601	CMA	150
Tone Transmitter (Three tone sequential code transmitter)	FX207	CMA	
Tone Transceiver (Decodes and encodes 5 sequential tones)	FX407	CMA	
	FX507	CMA	
	FX607	CMA	160
Tone Transceiver Code Selector (Programs 3 codes for FX407/507)	FX707	CMA	
Tone Transceiver (Single tone transmitter-receiver simplex.)	FX107	CMA	
Two-wire-to-Four wire converter (replaces hybrid transformer)	ST120	Signetics	
Crosspoint Array (Double 4 x 4 switch matrix)	MC3466	Motorola	170
	RC4444	Raytheon	
	RM4444	Raytheon	
Crosspoint Array (4 x 4 switch matrix)	CD22100	RCA	
Crosspoint Array (8 x 2 switch matrix)	SD5301	Signetics	
Crosspoint Array (8x4 switch matrix)	MT8804B	†Mitel	
	MT8804BE	Mitel	180

† Military Temperature Range (−55° to 125°C)

* Typical Values

LINEAR–Timers

Function	Device	Source	Line
Timers			
Timer			
	NE555	† AMD	
	SE555	AMD	
	CS555	Cherry	
	XR555C	Exar	
	XR555M	† Exar	
	XRL555	**Exar (923)**	
	µA555C	Fairchild	
	HA17555	Hitachi	
	NE555	Intersil	10
	SE555	† Intersil	
	M51843	Mitsubishi	
	MC1455	Motorola	
	MC1555	† Motorola	
	LM555C	National	
	LM555M	† National	
	µPC1555	NEC America	
	RC555	Raytheon	
	RM555	† Raytheon	
	CA555	† RCA	20
	CA555C	RCA	
	NE555	Signetics	
	SE555	† Signetics	
	TDA0555	Signetics	
	SA555	Signetics	
	SG555	† Silicon G	
	SG555C	Silicon G	
	ULN-3303	Sprague	
	ULN-3304	Sprague	
	355A/C	Teledyne S	30
	355B/M	† Teledyne S	
	SE555	† TI	
	NE555	TI	
Timer, Adjustable Threshold			
	MC1422	Motorola	
Timer, delayed switch ON/OFF (for driving relays, lamps, etc.)			
	PBA3008	RIFA	
	PBA3009	RIFA	
Timer, Detector/Timer, LED Driver, audio oscillator			40
	MD4301	Mitel	
	MD4302	Mitel	
	MD4303	Mitel	
	MD4304	Mitel	
Timer, Precision Decade, Direct 7 Segment and Digit Drivers			
	ICM7045	Intersil	
	ICM7045A	Intersil	
Timer, Industrial, with ÷5, ÷6, ÷10, ÷4096 counters, 1 Hz output			50
	CD22017	RCA	
Timer, Internal Current Source			
	XR320	Exar	
	XR320M	† Exar	
Timer, Low Power (Supply 3v)			
	SN76812	TI	
Timer (CMOS 555), Low Power			
	ICM7555	Intersil	
Timer/Microwave Oven Controller			
	AY5-1260	GI	60
	TMS1117	TI	
Timer, Precision			
	LM122	† National	
	LM222	National	
	LM322	National	
	LM2905	National	
		(Continued)	

Function	Device	Source	Line
Timers (Cont'd.)			
Timer, Precision (Cont'd.)			
	LM3905	National	
Timer with Counter, (time constant 128 RC)			
	XR2242C	**Exar (924)**	70
	XR2242M	**† Exar (924)**	
Timer with ÷12 Counter (time constant 7200 RC)			
	ZN1034E	Ferranti	
Timer, Programmable (includes a counter for long time delays) Binary Control			
	XR2240C	Exar	
	XR2240M	† Exar	
	µA2240	Fairchild	
	ICL8240	Intersil	
	MC14541BA	† Motorola	80
	MC14541BC	Motorola	
	µA2240C	TI	
	µA2240M	† TI	
Timer, Programmable (includes counter) Decimal Control			
	ICL8250	Intersil	
Timer, Programmable (includes counter) Hours/Minutes/Seconds Control			
	ICL8260	Intersil	
Timer, for Video Tape Controller			90
	VTR3300	GI	
Dual Timer (dual 555)			
	NE556	AMD	
	SE556	† AMD	
	XR556C	Exar	
	XR556M	† Exar	
	µA556	Fairchild	
	NE556	Intersil	
	SE556	† Intersil	
	MC3456	Motorola	100
	MC3556	† Motorola	
	LM556	† National	
	LM556C	National	
	RC556	Raytheon	
	RM556	† Raytheon	
	TDB0556	Siemens	
	NE556	Signetics	
	SE556	† Signetics	
	SA556	Signetics	
	SG556	† Silicon G	110
	SG556C	Silicon G	
	NE556	TI	
	SE556	† TI	
Dual Timer (dual 555), pinout variations			
	XR2556C	Exar	
	XR2556M	† Exar	
Dual Timer(CMOS 556) Low Power			
	ICM7556	Intersil	
Dual Set Point Timer (includes timer, selectable time range)			120
	DF215	Siliconix	
4 Digit Up/Down Presettable Counter/Timer, settable register with comparison to counter, multiplexed 7-segment and BCD output (Maximum count 5959)			
	ICM7217B	Intersil	
	ICM7217C	Intersil	
	ICM7227B	Intersil	
	ICM7227C	Intersil	
Counter/Timer(50 ms-4800 hr)			
	M58479	Mitsubishi	130
		(Continued)	

Function	Device	Source	Line
Timers (Cont'd.)			
Counter/Timer(50 ms-4800 hr) (Cont'd.)			
	M58482	Mitsubishi	
Universal Timer (includes two 4-digit counters, comparator, clock oscillator and divider)			
	MM5865	National	
Dual Monostable Timer			
	FX109	CMA	
Quad Timer, Current Sink Output			
	NE558	Signetics	
	SA558	Signetics	140
	SE558	† Signetics	
Quad Timer, Current Source Output			
	NE559	Signetics	
	SA559	Signetics	
	SE559	† Signetics	
Tone Triggered Timer			
	FX601	CMA	
Other Timer Circuits: See Linear-Consumer Circuits, Appliance Timers; Clocks; Watches; Stopwatches; T.V. Timers and Digital-CMOS Oscillators/Dividers			150

† Military Temperature Range (−55° to 125°C)

* Typical Values

Bold face indicates additional data is provided on the page noted.

LINEAR–Voltage Regulators

Fixed, Positive

For low amounts of current, voltage references can be used as voltage regulators. See Linear—Other Devices, Reference Diodes

Output Voltage	Output Current	Device	Source		Line
2.6	100 ma	µA78L26C	Fairchild		
		MC78L02C	Motorola		
		µA78L02C	Signetics		
		µA78L02C	TI		
		µA78L02AC	TI		
		TA7316	Toshiba		
5	100 ma	**µA78L05C**	**Fairchild**	**(935)**	10
		MC78L05C	Motorola		
		LM140LA-5	**National**	**(1060)**	
		LM240LA-5	**National**	**(1060)**	
		LM340LA-5	**National**	**(1060)**	
		LM78L05A	**National**	**(1060)**	
		LM78L05C	**National**	**(1060)**	
		µPC78L05	NEC America		
		µA78L05C	Signetics		
		µA78L05C	TI		
		µA78L05AC	TI		20
		TA78L005	Toshiba		
		TA78L005A	Toshiba		
	200 ma	LM109H	Motorola		
		LM209H	Motorola		
		LM309H	Motorola		
		LH0075	National		
		LM109H	**† National**	**(1060)**	
		LM209H	**National**	**(1060)**	
		LM309H	**National**	**(1060)**	
		SFC2109	† NPC		30
		SFC2209	NPC		
		SFC2309	NPC		
		TBA625A	Plessey		
		LM109H	† Raytheon		
		LM209H	Raytheon		
		LM309H	Raytheon		
		LM209DB	Signetics		
		LM309DB	Signetics		
		SG109T	† Silicon G		
		SG209T	Silicon G		40
		SG309T	Silicon G		
		LM109	† TI		
		LM209	TI		
		LM309	TI		
	250 ma	**LM342-5**	**National**	**(1060)**	
		L192-5	SGS		
	500 ma	805-V5	† Beckman		
		µA78M05C	**Fairchild**	**(935)**	
		µA78M05M	**† Fairchild**	**(935)**	
		MC7705C	Motorola		50
		MC78M05C	Motorola		
		LM341-5	**National**	**(1060)**	
		LM78M05	**National**	**(1060)**	
		µPC78M05	NEC America		
		L194-5	SGS		
		LM109DA	† Signetics		
		LM209DA	Signetics		
		LM309DA	Signetics		
		µA78M05	† Signetics		
		µA78M05C	Signetics		60
		µA78MHV05	† Signetics		
		µA78MHV05C	Signetics		
		SG7805AT	† Silicon G		
		SG7805ACT	Silicon G		
		µA78M05C	TI		
		µA78M05M	† TI		
	600 ma	L005T1	SGS		

(Continued)

Fixed, Positive (Cont'd.)

Output Voltage	Output Current	Device	Source		Line
5					(Cont'd.)
	750 ma	809-V5	† Beckman		
	850 ma	L129	SGS		70
	1 a	**µA109M**	**† Fairchild**	**(934)**	
		µA209M	**Fairchild**	**(934)**	
		µA309C	**Fairchild**	**(934)**	
		LM109K	† Motorola		
		LM209K	Motorola		
		LM309K	Motorola		
		MC7805C	Motorola		
		LM109K	**† National**	**(1060)**	
		LM209K	**National**	**(1060)**	
		LM309K	**National**	**(1060)**	80
		SFC2109M	NPC		
		LM109K	† Raytheon		
		LM209K	Raytheon		
		LM309K	Raytheon		
		L7805	† SGS		
		L7805C	SGS		
		LM209DA	Signetics		
		LM309DA	Signetics		
		SG109K	† Silicon G		
		SG209K	Silicon G		90
		SG309K	Silicon G		
		SG7805AR	† Silicon G		
		SG7805ACR	Silicon G		
		SG7805CR	† Silicon G		
		SG7805R	Silicon G		
		TA78005	Toshiba		
	1.2 a	SI3551M	Sanken		
	1.5 a	**µA7805C**	**Fairchild**	**(935)**	
		µA7805M	**† Fairchild**	**(935)**	
		LAS1505	Lambda		100
		LAS15A05	Lambda		
		LM140-5	**† National**	**(1060)**	
		LM140A-5	**† National**	**(1060)**	
		LM340-5	**National**	**(1060)**	
		LM340A-5	National		
		LM7805	**National**	**(1060)**	
		µPC7805	NEC America		
		LM109DB	† Signetics		
		LM209DB	Signetics		
		LM309DB	Signetics		110
		µA7805	† Signetics		
		µA7805C	Signetics		
		µA78HV05	Signetics		
		LM340-5	Signetics		
		SG7805AK	† Silicon G		
		SG7805ACK	Silicon G		
		SG7805ACP	Silicon G		
		SG7805CK	Silicon G		
		SG7805CP	Silicon G		
		SG7805K	† Silicon G		120
		LM340-5	TI		
		TL7805AC	TI		
		TL7805C	TI		
	2 a	LAS1605	Lambda		
		SI3050G	Sanken		
		SI3552M	Sanken		
		L2005	SGS		
	3 a	µA233	Fairchild		
		SH123	† Fairchild		
		SH223	Fairchild		130
		SH323	Fairchild		
		LM123	Motorola		

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Values

LINEAR–Voltage Regulators (Cont'd)

Fixed, Positive (Cont'd.)

Output Voltage	Output Current	Device	Source		Line
5	3 a			(Cont'd.)	
		LM323	Motorola		
		LAS1405	Lambda		
		LM123	**† National**	**(1060)**	
		LM223	**National**	**(1060)**	
		LM323	**National**	**(1060)**	
		SI3554M	Sanken		
		SG123	† Silicon G		
		SG223	Silicon G		
		SG323	Silicon G		10
	5 a	**μA78H05**	**Fairchild**	**(934,952)**	
		SH1705	**Fairchild**	**(954)**	
		LAS1905	Lambda		
		42050-055	Micropac		
	10 a	**μA78P05**	**Fairchild**	**(934)**	
		42050-510	Micropac		
	20a	42055-520	Micropac		
6	100 ma	**LM140LA-6**	**National**	**(1060)**	
		LM240LA-6	**National**	**(1060)**	20
		LM340LA-6	**National**	**(1060)**	
		LM78L06A	**National**	**(1060)**	
		LM78L06C	**National**	**(1060)**	
		TA78L006	Toshiba		
		TA78L006A	Toshiba		
	200 ma	LH0075	National		
	250 ma	**LM342-6**	**National**	**(1060)**	
	500 ma	**μA78M06C**	**Fairchild**	**(935)**	
		μA78M06M	**† Fairchild**	**(935)**	
		MC78M06C	Motorola		30
		LM341-6	**National**	**(1060)**	
		LM78M06	**National**	**(1060)**	
		SG7806AT	† Silicon G		
		SG7806ACT	Silicon G		
		SG7806T	† Silicon G		
		SG7806CT	Silicon G		
		μA78M06C	Signetics		
		μA78M06M	† Signetics		
		μA78MHV06	† Signetics		
		μA78MHV06C	Signetics		40
		μA78M06C	TI		
		μA78M06M	† TI		
	1 a	SG7806ACR	Silicon G		
		SG7806AR	† Silicon G		
		SG7806CR	Silicon G		
		SG7806R	† Silicon G		
	1.5 a	**μA7806C**	**Fairchild**	**(935)**	
		μA7806M	**† Fairchild**	**(935)**	•
		LAS1506	Lambda		
		MC7806C	Motorola		50
		LM140-6	**† National**	**(1060)**	
		LM140A-6	**† National**	**(1060)**	
		LM340-6	**National**	**(1060)**	
		LM340A-6	**National**	**(1060)**	
		LM7806	**National**	**(1060)**	
		TDB7806	Siemens		
		SG7806AK	† Silicon G		
		SG7806ACK	Silicon G		
		SG7806CK	Silicon G		
		SG7806K	† Silicon G		60
		SG7806ACP	Silicon G		
		SG7806CP	Silicon G		
		μA78HV06	Signetics		
		μA7806	† Signetics		

(Continued)

Fixed, Positive (Cont'd.)

Output Voltage	Output Current	Device	Source		Line
6	1.5 a			(Cont'd.)	
		μA7806C	Signetics		
		LM340-6	Signetics		
		LM340-6	TI		
		μA7806C	TI		
		μA7806M	† TI		7(
	2 a	LAS1606	Lambda		
		CJSE017	Solitron		
		CJSE019	Solitron		
		CJSE021	Solitron		
	3 a	LAS1406	Lambda		
	5 a	LAS1906	Lambda		
	10 a	42050-610	Micropac		
	20a	42055-620	Micropac		
6.2	100 ma	μA78L62C	Fairchild		
		μA78L06C	Signetics		8(
		μA78L06C	TI		
		μA78L06AC	TI		
7	100 ma	TA78L007	Toshiba		
		TA78L007A	Toshiba		
	10 a	42050-710	Micropac		
	20a	42055-720	Micropac		
7.5	100 ma	TA78L075	Toshiba		
		TA78L075A	Toshiba		
	1a	L7875	† SGS		
		L7875C	SGS		90
	2 a	L2075	SGS		
8	100 ma	DVR-8	Delco		
		μA78L08C	**Fairchild**	**(935)**	
		MC78L08C	Motorola		
		LM140LA-8	**† National**	**(1060)**	
		LM240LA-8	**National**	**(1060)**	
		LM340LA-8	**National**	**(1060)**	
		LM78L08A	**National**	**(1060)**	
		LM78L08C	**National**	**(1060)**	
		μPC78L08	NEC America		100
		μA78L08	TI		
		μA78L08AC	TI		
		TA78L008	Toshiba		
		TA78L008A	Toshiba		
	200 ma	LH0075	National		
	250 ma	**LM342-8**	**National**	**(1060)**	
	500 ma	**μA78C08C**	**Fairchild**	**(935)**	
		μA78M08C	**Fairchild**	**(935)**	
		μA78M08M	**† Fairchild**	**(935)**	
		MC78M08C	Motorola		110
		LM341-8	**National**	**(1060)**	
		LM78M08	**National**	**(1060)**	
		μPC78M08	NEC America		
		μA78M08C	Signetics		
		μA78M08M	† Signetics		
		μA78MHV08	Signetics		
		μA78MHV08C	† Signetics		
		SG7808AT	† Silicon G		
		SG7808ACT	Silicon G		
		SG7808T	† Silicon G		120
		SG7808CT	Silicon G		
		μA78M08C	TI		
		μA78M08M	† TI		
	1 a	SG7808AR	† Silicon G		
		SG7808ACR	Silicon G		

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Values

Bold face indicates additional data is provided on the page noted.

LINEAR–Voltage Regulators (Cont'd)

Output Voltage	Output Current	Device	Source		Line
Fixed, Positive				**(Cont'd.)**	
8	1 a			(Cont'd.)	
		SG7808R	† Silicon G		
		SG7808CR	Silicon G		
	1.5 a	**μA7808C**	**Fairchild**	**(935)**	
		μA7808M	**† Fairchild**	**(935)**	
		LAS1508	Lambda		
		MC7808C	Motorola		
		LM140-8	**† National**	**(1060)**	
		LM140A-8	**† National**	**(1060)**	
		LM340-8	**National**	**(1060)**	10
		LM340A-8	**National**	**(1060)**	
		LM7808	**National**	**(1060)**	
		μPC7808	NEC America		
		μA7808	† Signetics		
		μA7808C	Signetics		
		μA78HV08	Signetics		
		LM340-8	Signetics		
		SG7808AK	† Silicon G		
		SG7808ACK	Silicon G		
		SG7808CK	Silicon G		20
		SG7808K	† Silicon G		
		SG7808ACP	Silicon G		
		SG7808CP	Silicon G		
		LM340-8	TI		
		μA7808C	TI		
	2 a	LAS1608	Lambda		
	3 a	LAS1408	Lambda		
	10 a	42050-810	Micropac		
	5 a	LAS1908	Lambda		
	20a	42055-820	Micropac		30
8.2	100 ma	μA78C82C	Fairchild		
		μA78L82C	Fairchild		
8.5	200 ma	TBA435	Plessey		
	1 a	μA7885	Fairchild		
		L7885	† SGS		
		L7885C	SGS		
		μA7885C	TI		
	2 a	L2085	SGS		
9	100 ma	**μA78L09C**	**Fairchild**	**(935)**	
		μA78L09C	TI		40
		μA78L09AC	TI		
		TA78L009	Toshiba		
		TA78L009A	Toshiba		
	750 ma	809-V9	† Beckman		
	20a	42055-920	Micropac		
10	100 ma	**LM140LA-10**	**† National**	**(1060)**	
		LM240LA-10	**National**	**(1060)**	
		LM340LA-10	**National**	**(1060)**	
		LM78L10A	National		
		LM78L10C	**National**	**(1060)**	50
		μA78L10C	TI		
		μA78L10AC	TI		
		TA78L010	Toshiba		
		TA78L010A	Toshiba		
	200 ma	LH0075	National		
	250 ma	**LM342-10**	**National**	**(1060)**	
	500 ma	**μA78C10C**	**Fairchild**	**(935)**	
		LM78M10	**National**	**(1060)**	
		μA78M10C	TI		
	1.5 a	LAS1510	Lambda		60
				(Continued)	

Output Voltage	Output Current	Device	Source		Line
Fixed, Positive				**(Cont'd.)**	
10	1.5 a			(Cont'd.)	
		LM140-10	**† National**	**(1060)**	
		LM140A-10	**† National**	**(1060)**	
		LM340-10	**National**	**(1060)**	
		LM340A-10	**National**	**(1060)**	
		LM7810	**National**	**(1060)**	
		LM340-10	TI		
		μA7810C	TI		
	2 a	LAS1610	Lambda		
	3 a	LAS1410	Lambda		70
	5 a	LAS1910	Lambda		
	9 a	42050-109	Micropac		
	20a	42055-1020	Micropac		
12	100 ma	**μA78L12C**	**Fairchild**	**(935)**	
		MC78L12C	Motorola		
		LM140LA-12	**† National**	**(1060)**	
		LM240LA-12	**National**	**(1060)**	
		LM340LA-12	**National**	**(1060)**	
		LM78L12A	**National**	**(1060)**	
		LM78L12C	**National**	**(1060)**	80
		μPC78L12	NEC America		
		μA78L12C	Signetics		
		μA78L12C	TI		
		μA78L12AC	TI		
		TA78L012	Toshiba		
		TA78L012A	Toshiba		
	200 ma	LH0075	National		
		TBA625B	Plessey		
	250 ma	**LM342-12**	**National**	**(1060)**	
		L192-12	SGS		90
	500 ma	**μA78C12C**	**Fairchild**	**(935)**	
		μA78M12C	**Fairchild**	**(935)**	
		μA78M12M	**† Fairchild**	**(935)**	
		MC78M12C	Motorola		
		LM341-12	**National**	**(1060)**	
		LM78M12	**National**	**(1060)**	
		μPC78M12	NEC America		
		L036T1	SGS		
		L194-12	SGS		
		SG7812AT	† Silicon G		100
		SG7812CT	Silicon G		
		SG7812ACT	Silicon G		
		SG7812T	† Silicon G		
		μA78M12C	Signetics		
		μA78M12M	† Signetics		
		μA78MHV12	† Signetics		
		μA78MHV12C	Signetics		
		μA78M12M	† TI		
		μA78M12C	TI		
	720 ma	L130	SGS		110
	750 ma	809-V12	† Beckman		
	1 a	SI3120E	Sanken		
		SI3120T	Sanken		
		STK521	Sanyo		
		STK541	Sanyo		
		L7812	† SGS		
		L7812C	SGS		
		SG7812AR	† Silicon G		
		SG7812ACR	Silicon G		
		SG7812CR	Silicon G		120
		SG7812R	† Silicon G		
		TA78012	Toshiba		
				(Continued)	

† Military Temperature Range (−55° to 125°C)

* Typical Values

LINEAR–Voltage Regulators (Cont'd)

Output Voltage	Output Current	Device	Source		Line
Fixed, Positive				**(Cont'd.)**	
12				(Cont'd.)	
	1.5 a	**μA7812C**	**Fairchild**	**(935)**	
		μA7812M	**† Fairchild**	**(935)**	
		LAS1512	Lambda		
		LAS15A12	Lambda		
		MC7812C	Motorola		
		LM140-12	**† National**	**(1060)**	
		LM140A-12	**† National**	**(1060)**	
		LM340-12	**National**	**(1060)**	
		LM340A-12	**National**	**(1060)**	10
		LM7812	**National**	**(1060)**	
		μPC7812	NEC America		
		SI3120G	Sanken		
		SI3120M	Sanken		
		μA7812	† Signetics		
		μA7812C	Signetics		
		μA78HV12	Signetics		
		LM340-12	Signetics		
		SG7812K	† Silicon G		
		SG7812AK	† Silicon G		20
		SG7812ACK	Silicon G		
		SG7812CK	Silicon G		
		SG7812ACP	Silicon G		
		SG7812CP	Silicon G		
		μA7812C	TI		
		LM340-12	TI		
	2 a	LAS1612	Lambda		
		STK531	Sanyo		
		L2012	SGS		
	3 a	LAS1412	Lambda		30
	5 a	**μA78H12**	**Fairchild**	**(934,952)**	
		LAS1912	Lambda		
	8 a	42050-128	Micropac		
	16 a	42055-1216	Micropac		
13	300 ma	TA7221	Toshiba		
13.2	100 ma	TA78L132	Toshiba		
		TA78L132A	Toshiba		
13.8	1.5a	μA7814	† Signetics		
		μA7814C	Signetics		40
	2a	**μA78CB**	**Fairchild**	**(934)**	
		LAS15CB	Lambda		
	3 a	LAS14CB	Lambda		
	5 a	LAS19CB	Lambda		
14	2 a	LAS16CB	Lambda		
	8 a	42050-148	Micropac		
	16 a	42055-1416	Micropac		
15	400 μa	L037T1	SGS		
	100 ma	**μA78L15C**	**Fairchild**	**(935)**	
		MC78L15C	Motorola		50
		LM140LA-15	**† National**	**(1060)**	
		LM240LA-15	**National**	**(1060)**	
		LM340LA-15	**National**	**(1060)**	
		LM78L15A	**National**	**(1060)**	
		LM78L15C	**National**	**(1060)**	
		μPC78L15	NEC America		
		μA78L15C	Signetics		
		μA78L15C	TI		
		μA78L15AC	TI		
		TA78L015	Toshiba		60
		TA78L015A	Toshiba		

(Continued)

Output Voltage	Output Current	Device	Source		Line
Fixed, Positive				**(Cont'd.)**	
15				(Cont'd.)	
	200 ma	LH0075	National		
		TBA625C	Plessey		
	250 ma	L192-15	SGS		
		LM342-15	**National**	**(1060)**	
	500 ma	801-V15	† Beckman		
		μA78C15C	**Fairchild**	**(935)**	
		μA78M15C	**Fairchild**	**(935)**	
		μA78M15M	**† Fairchild**	**(935)**	70
		MC78M15C	Motorola		
		LM341-15	**National**	**(1060)**	
		LM78M15	**National**	**(1060)**	
		μPC78M15	NEC America		
		L194-15	SGS		
		μA78M15	† Signetics		
		μA78M15C	Signetics		
		μA78MHV15	† Signetics		
		μA78MHV15C	Signetics		
		SG7815AT	† Silicon G		80
		SG7815ACT	Silicon G		
		SG7815CT	Silicon G		
		SG7815T	† Silicon G		
		μA78M15C	TI		
		μA78M15M	† TI		
	600 ma	L131	SGS		
	750 ma	809-V15	† Beckman		
	1 a	SI3150E	Sanken		
		SI3150T	Sanken		
		L7815	† SGS		90
		L7815C	SGS		
		SG7815AR	† Silicon G		
		SG7815ACR	Silicon G		
		SG7815R	† Silicon G		
		SG7815CR	Silicon G		
		TA78015	Toshiba		
	1.5 a	**μA7815C**	**Fairchild**	**(935)**	
		μA7815M	**† Fairchild**	**(935)**	
		LAS1515	Lambda		
		LAS15A15	Lambda		100
		MC7815C	Motorola		
		LM140-15	**† National**	**(1060)**	
		LM140A-15	**† National**	**(1060)**	
		LM340-15	**National**	**(1060)**	
		LM340A-15	**National**	**(1060)**	
		LM7815	**National**	**(1060)**	
		SI3150G	Sanken		
		SI3150M	Sanken		
		μA7815	† Signetics		
		μA7815C	Signetics		110
		μA78HV15	Signetics		
		LM340-15	Signetics		
		SG7815AK	† Silicon G		
		SG7815ACK	Silicon G		
		SG7815CK	Silicon G		
		SG7815K	† Silicon G		
		SG7815ACP	Silicon G		
		SG7815CP	Silicon G		
		μA7815C	TI		
		LM340-15	TI		120
	2 a	LAS1615	Lambda		
		L2015	SGS		
		CJSE001	Solitron		
		CJSE003	Solitron		
		CJSE005	Solitron		

(Continued)

† Military Temperature Range (−55° to 125°C) * Typical Values

Bold face indicates additional data is provided on the page noted.

LINEAR–Voltage Regulators (Cont'd)

Output Voltage	Output Current	Device	Source		Line
Fixed, Positive				**(Cont'd.)**	
15				(Cont'd.)	
	3 a	LAS1415	Lambda		
	5 a	**μA78H15**	**Fairchild**	**(934,952)**	
		LAS1915	Lambda		
	8 a	42050-158	Micropac		
	16 a	42055-1516	Micropac		
16	8 a	42050-168	Micropac		
	12 a	42055-1612	Micropac		
17	500 ma	**μA78C17C**	**Fairchild**	**(935)**	10
	2 a	L2017	SGS		
18	100 ma	**μA78L18**	**Fairchild**	**(935)**	
		MC78L18C	Motorola		
		LM140LA-18	**† National**	**(1060)**	
		LM240LA-18	**National**	**(1060)**	
		LM340LA-18	**National**	**(1060)**	
		LM78L18A	**National**	**(1060)**	
		LM78L18C	**National**	**(1060)**	
		TA78L018	Toshiba		
		TA78L018A	Toshiba		20
	200 ma	LH0075	National		
	250 ma	**LM342-18**	**National**	**(1060)**	
	500 ma	**μA78C18C**	**Fairchild**	**(935)**	
		MC78M18C	Motorola		
		LM341-18	**National**	**(1060)**	
		LM78M18	**National**	**(1060)**	
		SG7818AT	† Silicon G		
		SG7818ACT	Silicon G		
		SG7818CT	Silicon G		
		SG7818T	† Silicon G		30
	1 a	STK522	Sanyo		
		STK542	Sanyo		
		L7818	† SGS		
		L7818C	SGS		
		SG7818AR	† Silicon G		
		SG7818ACR	Silicon G		
		SG7818R	† Silicon G		
		SG7818CR	Silicon G		
	1.5 a	**μA7818C**	**Fairchild**	**(935)**	
		μA7818M	**† Fairchild**	**(935)**	40
		MC7818C	Motorola		
		LAS1518	Lambda		
		LM140-18	**† National**	**(1060)**	
		LM140A-18	**† National**	**(1060)**	
		LM340-18	**National**	**(1060)**	
		LM340A-18	**National**	**(1060)**	
		LM7818	**National**	**(1060)**	
		μPC7818	NEC America		
		LM340-18	Signetics		
		μA7818	† Signetics		50
		μA7818C	Signetics		
		μA78HV18	Signetics		
		SG7818AK	† Silicon G		
		SG7818ACK	Silicon G		
		SG7818CK	Silicon G		
		SG7818K	† Silicon G		
		SG7818ACP	Silicon G		
		SG7818CP	Silicon G		
		μA7818C	TI		
		LM340-18	TI		60
	2 a	STK532	Sanyo		
	8 a	42050-188	Micropac		

(Continued)

Output Voltage	Output Current	Device	Source		Line
Fixed, Positive				**(Cont'd.)**	
18				(Cont'd.)	
	12 a	42055-1812	Toshiba		
20	100 ma	TA78L020	Toshiba		
		TA78L020A	Toshiba		
	500 ma	**μA78C20C**	**Fairchild**	**(935)**	
		μA78M20C	**Fairchild**	**(935)**	
		μA78M20M	**† Fairchild**	**(935)**	
		MC78M20C	Motorola		70
		μA78M20C	Signetics		
		μA78M20M	† Signetics		
		μA78MHV20	† Signetics		
		μA78MHV20C	Signetics		
		μA78M20C	TI		
		μA78M20M	† TI		
	1.5 a	LAS1520	Lambda		
	2 a	CJSE009	Solitron		
		CJSE011	Solitron		
		CJSE013	Solitron		80
	8 a	42050-208	Micropac		
	10 a	42055-2010	Micropac		
22	500 ma	**μA78C22**	**Fairchild**	**(935)**	
		μA78M22C	TI		
	1.5	μA7822C	TI		
	4 a	42050-224	Micropac		
	10 a	42055-2210	Micropac		
24	100 ma	**μA78L24**	**Fairchild**	**(935)**	
		MC78L24C	Motorola		
		LM140LA-24	**† National**	**(1060)**	90
		LM240LA-24	**National**	**(1060)**	
		LM340LA-24	**National**	**(1060)**	
		LM78L24A	**National**	**(1060)**	
		LM78L24C	**National**	**(1060)**	
		TA78L024	Toshiba		
		TA78L024A	Toshiba		
	250 ma	**LM342-24**	**National**	**(1060)**	
	300 ma	STK507	Sanyo		
	500 ma	**μA78C24C**	**Fairchild**	**(935)**	
		μA78M24C	**Fairchild**	**(935)**	100
		μA78M24M	**† Fairchild**	**(935)**	
		MC78M24C	Motorola		
		SG7824AT	† Silicon G		
		SG7824ACT	Silicon G		
		SG7824T	† Silicon G		
		SG7824CT	Silicon G		
		LM341-24	**National**	**(1060)**	
		LM78M24	**National**	**(1060)**	
		μA78M24	† Signetics		
		μA78M24C	Signetics		110
		μA78MHV24	† Signetics		
		μA78MHV24C	Signetics		
		μA78M24C	TI		
		μA78M24M	† TI		
	1 a	SI3240E	Sanken		
		SI3240T	Sanken		
		STK523	Sanyo		
		STK543	Sanyo		
		L7824	† SGS		
		L7824C	SGS		120
		SG7824AR	† Silicon G		
		SG7824ACR	Silicon G		
		SG7824R	† Silicon G		
		SG782CR	Silicon G		

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Values

LINEAR–Voltage Regulators (Cont'd)

Fixed, Positive (Cont'd.)

Output Voltage	Output Current	Device	Source		Line
24				(Cont'd.)	
	1.5 a	**μA7824C**	**Fairchild**	**(935)**	
		μA7824M	**† Fairchild**	**(935)**	
		LAS1524	Lambda		
		MC7824C	Motorola		
		LM140-24	**† National**	**(1060)**	
		LM140A-24	**† National**	**(1060)**	
		LM340-24	**National**	**(1060)**	
		LM340A-24	**National**	**(1060)**	
		LM7824	**National**	**(1060)**	10
		μPC7824	NEC America		
		SI3240G	Sanken		
		SI3240T	Sanken		
		μA7824	† Signetics		
		μA7824C	Signetics		
		μA78HV24	Signetics		
		LM340-24	Signetics		
		SG7824AK	† Silicon G		
		SG7824ACK	Silicon G		
		SG7824K	† Silicon G		20
		SG7824CK	Silicon G		
		SG7824ACP	Silicon G		
		SG7824CP	Silicon G		
		μA7824C	TI		
		LM340-24	TI		
	2 a	STK533	Sanyo		
		L2024	SGS		
	4 a	42050-244	Micropac		
	10 a	42055-2410	Micropac		
26	4 a	42050-264	Micropac		30
	8 a	42055-2608	Micropac		
28	1.5 a	LAS1528	Lambda		
	4 a	42050-284	Micropac		
	8 a	42055-2808	Micropac		
30	4 a	42050-304	Micropac		
31	Shunt	TAA550	National		
		TBA271A	SGS		
		TAA550	Signetics		
32	Shunt	AN155	Panasonic		
	4 a	42050-324	Micropac		40
33	Shunt	TAA550	National		
		TBA271B	SGS		
		TAA550	Signetics		
34	4 a	42050-344	Micropac		
35	Shunt	TAA550	National		
		TBA271C	SGS		
		TAA550	Signetics		
36	4 a	42050-364	Micropac		
190	20 ma	DI-900	Dionics		
	50 ma	DI-905	Dionics		50

Fixed, Negative

Output Voltage	Output Current	Device	Source		Line
2	1 a	MC7902C	Motorola		
	1.5 a	LAS1802	Lambda		
	2 a	μA79E02	† Fairchild		
		μA79E02C	Fairchild		
3	100 ma	MC79L03C	Motorola		
	200 ma	LH0076	National		

Fixed, Negative (Cont'd.)

Output Voltage	Output Current	Device	Source		Line
5	100 ma	MC79L05C	Motorola		
		LM79L05A	**National**	**(1060)**	
		LM79L05	**National**	**(1061)**	
		LM320L05	**National**	**(1061)**	60
	200 ma	LH0076	National		
	250 ma	**LM320ML05**	**National**	**(1061)**	
	500 ma	**μA79M05C**	**Fairchild**	**(934)**	
		LM120H5.0	**† National**	**(1061)**	
		LM220H5.0	**National**	**(1061)**	
		LM320H5.0	National		
		LM320MP5.0	**National**	**(1061)**	
		LM79M05	**National**	**(1061)**	
		μA79M05	† Signetics		
		μA79M05C	Signetics		70
		SG120-05T	† Silicon G		
		SG220-05T	Silicon G		
		SG320-05T	Silicon G		
		μA79M05	TI		
	750 ma	859-V5	† Beckman		
	1 a	SG120-05R	† Silicon G		
		SG220-05R	Silicon G		
		SG320-05R	Silicon G		
	1.5 a	**μA7905C**	**Fairchild**	**(934)**	
		LAS18A05	Lambda		80
		LM7905	**National**	**(1061)**	
		MC7905C	Motorola		
		LM120K5.0	**† National**	**(1061)**	
		LM220K5.0	**National**	**(1061)**	
		LM320K5.0	**National**	**(1061)**	
		LM320T5.0	**National**	**(1061)**	
		LAS1805	Lambda		
		μA7905	† Signetics		
		μA7905C	Signetics		
		SG120-05K	† Silicon G		90
		SG220-05K	Silicon G		
		SG220-05P	Silicon G		
		SG320-05K	Silicon G		
		SG320-05P	Silicon G		
		SG7905	† Silicon G		
		SG7905C	Silicon G		
		μA7905C	TI		
	2 a	μA79E05	† Fairchild		
		μA79E05C	Fairchild		
	3 a	**LM145K5.0**	**† National**	**(1061)**	100
		LM245K5.0	**National**	**(1061)**	
		LM345K5.0	**National**	**(1061)**	
	5 a	42051-055	Micropac		
5.2	100 ma	**LM320L5.2**	**National**	**(1061)**	
	250 ma	**LM320ML5.2**	**National**	**(1061)**	
	500 ma	**LM120H5.2**	**† National**	**(1061)**	
		LM220H5.2	**National**	**(1061)**	
		LM320H5.2	National		
		LM320MP5.2	**National**	**(1061)**	
		LM79M05.2	**National**	**(1061)**	110
		μA79M05.2	† Signetics		
		μA79M05.2C	Signetics		
		SG120-5.2T	† Silicon G		
		SG220-5.2T	Silicon G		
		SG320-5.2T	Silicon G		
	1 a	SG120-5.2R	† Silicon G		
		SG220-5.2R	Silicon G		
		SG320-5.2R	Silicon G		
	1.5 a	LAS18052	Lambda		

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Values

Bold face indicates additional data is provided on the page noted.

LINEAR–Voltage Regulators (Cont'd)

Output Voltage	Output Current	Device	Source		Line
Fixed, Negative				**(Cont'd.)**	
5.2	1.5 a			(Cont'd.)	
		MC7905.2C	Motorola		
		LM120K5.2	**† National**	**(1061)**	
		LM220K5.2	**National**	**(1061)**	
		LM320K5.2	**National**	**(1061)**	
		LM320T5.2	**National**	**(1061)**	
		LM7905.2	**National**	**(1061)**	
		μA7905.2	† Signetics		
		μA7905.2C	Signetics		
		SG120-5.2K	Silicon G		10
		SG220-5.2K	Silicon G		
		SG220-5.2P	Silicon G		
		SG320-5.2K	Silicon G		
		SG320-5.2P	Silicon G		
		SG7905.2	† Silicon G		
		SG7905.2C	Silicon G		
		μA7952C	TI		
	3 a	**LM145K5.2**	**† National**	**(1061)**	
		LM245K5.2	**National**	**(1061)**	
		LM345K5.2	**National**	**(1061)**	20
6	100 ma	**LM320L06**	**National**	**(1061)**	
		LM79L06A	**National**	**(1060)**	
	200 ma	LM0076	National		
	250 ma	**LM320ML06**	**National**	**(1061)**	
	500 ma	**μA79M06C**	**Fairchild**	**(934)**	
		LM120H6.0	**† National**	**(1061)**	
		LM220H6.0	**National**	**(1061)**	
		LM320H6.0	National		
		LM320MP6.0	**National**	**(1061)**	
		LM79M06	**National**	**(1061)**	30
		μA79M06	† Signetics		
		μA79M06C	Signetics		
		μA79M06	TI		
	1.5 a	**μA7906C**	**Fairchild**	**(934)**	
		LAS1806	Lambda		
		MC7906C	Motorola		
		LM7906	**National**	**(1061)**	
		LM120K6.0	**† National**	**(1061)**	
		LM220K6.0	**National**	**(1061)**	
		LM320K6.0	**National**	**(1061)**	40
		LM320T6.0	**National**	**(1061)**	
		μA7906	† Signetics		
		μA7906C	Signetics		
		μA7906C	TI		
	2 a	CJSE018	Solitron		
		CJSE020	Solitron		
	5 a	42051-065	Micropac		
7	5 a	42051-075	Micropac		
8	100 ma	LM320L08	National		
		LM79L08A	**National**	**(1060)**	50
	200 ma	LM0076	National		
	250 ma	**LM320ML08**	**National**	**(1061)**	
	500 ma	**μA79M08C**	**Fairchild**	**(934)**	
		LM120H8.0	**† National**	**(1061)**	
		LM220H8.0	**National**	**(1061)**	
		LM320H8.0	National		
		LM320MP8.0	**National**	**(1061)**	
		LM79M08	**National**	**(1061)**	
		μA79M08	† Signetics		
		μA79M08C	Signetics		60
		μA79M08	TI		
	1.5 a	**μA7908C**	**Fairchild**	**(934)**	
				(Continued)	

Output Voltage	Output Current	Device	Source		Line
Fixed, Negative				**(Cont'd.)**	
8	1.5 a			(Cont'd.)	
		LAS1808	Lambda		
		MC7908C	Motorola		
		LM7908	**National**	**(1061)**	
		LM120K8.0	**† National**	**(1061)**	
		LM220K8.0	**National**	**(1061)**	
		LM320K8.0	**National**	**(1061)**	
		LM320T8.0	**National**	**(1061)**	70
		μA7908	† Signetics		
		μA7908C	Signetics		
		SG7908	† Silicon G		
		SG7908C	Silicon G		
		μA7908C	TI		
	5 a	42051-085	Micropac		
9	100 ma	**LM320L09**	**National**	**(1061)**	
	200 ma	**LM120H9.0**	**† National**	**(1061)**	
		LM220H9.0	**National**	**(1061)**	
		LM320H9.0	National		80
		LH0076	National		
	500 ma	**LM320MP9.0**	**National**	**(1061)**	
	1 a	**LM120K9.0**	**† National**	**(1061)**	
		LM220K9.0	**National**	**(1061)**	
		LM320K9.0	**National**	**(1061)**	
		LM320T9.0	**National**	**(1061)**	
	1.5 a	42051-095	Micropac		
10	100 ma	LM79L10A	National		
	250 ma	**LM320ML10**	**National**	**(1061)**	
	1.5 a	LAS1810	Lambda		90
	5 a	42051-105	Micropac		
12	100 ma	MC79L12C	Motorola		
		LM320L12	**National**	**(1061)**	
		LM79L12A	**National**	**(1060)**	
		LM79L12	**National**	**(1061)**	
	200 ma	LH0076	National		
		LM120H12	**† National**	**(1061)**	
		LM220H12	**National**	**(1061)**	
		LM320H12	National		
		SG120-12T	† Silicon G		100
		SG220-12T	Silicon G		
		SG320-12T	Silicon G		
	250 ma	**LM320L12**	**National**	**(1061)**	
	500 ma	**μA79M12C**	**Fairchild**	**(934)**	
		LM320MP12	**National**	**(1061)**	
		LM79M12	**National**	**(1061)**	
		μA79M12	† Signetics		
		μA79M12C	Signetics		
		μA79M12	TI		
	750 ma	859-V12	† Beckman		110
	1 a	**LM120K12**	**† National**	**(1061)**	
		LM220K12	**National**	**(1061)**	
		LM320K12	**National**	**(1061)**	
		LM320T12	**National**	**(1061)**	
		SG120-12R	† Silicon G		
		SG220-12R	Silicon G		
		SG320-12R	Silicon G		
	1.5 a	**μA7912C**	**Fairchild**	**(934)**	
		LAS1812	Lambda		
		LAS18A12	Lambda		120
		MC7912C	Motorola		
		LM7912	**National**	**(1061)**	
		μA7912	† Signetics		
				(Continued)	

† Military Temperature Range (−55° to 125°C)

* Typical Values

LINEAR–Voltage Regulators (Cont'd)

Output Voltage	Output Current	Device	Source		Line
Fixed, Negative				**(Cont'd.)**	
12	1.5 a			(Cont'd.)	
		µA7912C	Signetics		
		SG120-12K	† Silicon G		
		SG220-12K	Silicon G		
		SG220-12P	Silicon G		
		SG320-12K	Silicon G		
		SG320-12P	Silicon G		
		SG7912	† Silicon G		
		SG7912C	Silicon G		
		µA7912C	TI		10
	4 a	42051-124	Micropac		
14	4 a	42051-144	Micropac		
15	100 ma	MC79L15C	Motorola		
		LM320L15	**National**	**(1061)**	
		LM79L15A	**National**	**(1060)**	
		LM79L15	**National**	**(1061)**	
	200 ma	LH0076	National		
		LM120H15	**† National**	**(1061)**	
		LM220H15	**National**	**(1061)**	
		LM320H15	National		20
		SG120-15T	† Silicon G		
		SG220-15T	Silicon G		
		SG320-15T	Silicon G		
	250 ma	**LM320ML15**	**National**	**(1061)**	
	500 ma	851-V15	† Beckman		
		µA79M15C	**Fairchild**	**(934)**	
		LM320MP15	**National**	**(1061)**	
		LM79M15	**National**	**(1061)**	
		µA79M15	Signetics		
		µA79M15C	† Signetics		30
		µA79M15	TI		
	750 ma	859-V15	† Beckman		
	1 a	**LM120K15**	**† National**	**(1061)**	
		LM220K15	**National**	**(1061)**	
		LM320K15	**National**	**(1061)**	
		LM320T15	**National**	**(1061)**	
		SG120-15R	† Silicon G		
		SG220-15R	Silicon G		
		SG320-15R	Silicon G		
	1.5 a	**µA7915C**	**Fairchild**	**(934)**	40
		LAS1815	Lambda		
		LAS18A15	Lambda		
		MC7915C	Motorola		
		LM7915	**National**	**(1061)**	
		µA7915	† Signetics		
		µA7915C	Signetics		
		SG120-15K	† Silicon G		
		SG220-15K	Silicon G		
		SG220-15P	Silicon G		
		SG320-15K	Silicon G		50
		SG320-15P	Silicon G		
		SG7915	† Silicon G		
		SG7915C	Silicon G		
		µA7915C	TI		
		µA7915	† TI		
	2 a	CJSE002	Solitron		
		CJSE004	Solitron		
		CJSE006	Solitron		
	4 a	42051-154	Micropac		
16	4 a	42051-164	Micropac		60
18	100 ma	MC79L18C	Motorola		
		LM320L18	**National**	**(1061)**	

(Continued)

Output Voltage	Output Current	Device	Source		Line
Fixed, Negative				**(Cont'd.)**	
18	100 ma			(Cont'd.)	
		LM79L18A	**National**	**(1060)**	
		LM79L18	**National**	**(1061)**	
	200 ma	LH0076	National		
		LM120H18	**† National**	**(1061)**	
		LM220H18	**National**	**(1061)**	
		LM320H18	National		
	250 ma	**LM320ML18**	**National**	**(1061)**	70
	500 ma	**LM320MP18**	**National**	**(1061)**	
		LM79M18	**National**	**(1061)**	
		µA79M18	† Signetics		
		µA79M18C	Signetics		
	1 a	**LM120K18**	**† National**	**(1061)**	
		LM220K18	**National**	**(1061)**	
		LM320K18	**National**	**(1061)**	
		LM320T18	**National**	**(1061)**	
	1.5 a	**µA7918C**	**Fairchild**	**(934)**	
		LAS1818	Lambda		80
		MC7918C	Motorola		
		LM7918	**National**	**(1061)**	
		µA7918	† Signetics		
		µA7918C	Signetics		
		µA7918C	TI		
	4 a	42051-184	Micropac		
20	500 ma	µA79M20C	Fairchild		
		µA79M20	TI		
	1.5 a	LAS1820	Lambda		
	2 a	CJSE010	Solitron		90
		CJSE012	Solitron		
		CJSE014	Solitron		
	3 a	42051-204	Micropac		
22	3 a	42051-223	Micropac		
24	100 ma	MC79L24C	Motorola		
		LM320L24	**National**	**(1061)**	
		LM79L24A	**National**	**(1060)**	
		LM79L24	**National**	**(1061)**	
	200 ma	**LM120H24**	**† National**	**(1061)**	
		LM220H24	**National**	**(1061)**	100
		LM320H24	National		
	250 ma	**LM320ML24**	**National**	**(1061)**	
	500 ma	**µA79M24C**	**Fairchild**	**(934)**	
		LM320MP24	**National**	**(1061)**	
		LM79M24	**National**	**(1061)**	
		µA79M24	† Signetics		
		DF334	**Siliconix**	**(1133)**	
		µA79M24C	Signetics		
		µA79M24	TI		
	1 a	**LM120K24**	**† National**	**(1061)**	110
		LM220K24	**National**	**(1061)**	
		LM320K24	**National**	**(1061)**	
		LM320T24	**National**	**(1061)**	
	1.5 a	**µA7924C**	**Fairchild**	**(934)**	
		LAS1824	Lambda		
		MC7924C	Motorola		
		LM7924	**National**	**(1061)**	
		µA7924	† Signetics		
		µA7924C	Signetics		
		µA7924C	TI		120
	3 a	42051-243	Micropac		
26	3 a	42051-263	Micropac		

† Military Temperature Range (−55° to 125°C)

* Typical Values

Bold face indicates additional data is provided on the page noted.

LINEAR–Voltage Regulators (Cont'd)

Output Voltage	Output Current	Device	Source	Line
Fixed, Negative			**(Cont'd.)**	
28	1.5 a	LAS1828	Lambda	
	3 a	42051-283	Micropac	
30	3 a	42051-303	Micropac	
31	Shunt	TAA550	National	
		TBA271A	SGS	
		TAA550	Signetics	
32	Shunt	AN155	Panasonic	
	3 a	42051-323	Micropac	
33	Shunt	TAA550	National	
		TBA271B	SGS	10
		TAA550	Signetics	
34	3 a	42051-343	Micropac	
35	Shunt	TAA550	National	
		TBA271C	SGS	
		TAA550	Signetics	
36	3 a	42051-363	Micropac	
Fixed, Dual				
±5	200 ma	**NE5551**	**Signetics (1122)**	
		SE5551	**† Signetics (1122)**	
±6	200 ma	**NE5552**	**Signetics (1122)**	
		SE5552	**† Signetics (1122)**	20
	5 a	42051	Micropac	
±12	100 ma	LM126	† National	
		LM226	National	
		LM326	National	
	200 ma	**NE5553**	**Signetics (1122)**	
		SE5553	**† Signetics (1122)**	
-12,5	100 ma	LM127	† National	
		LM227	National	
		LM327	National	
	200 ma	**NE5555**	**Signetics (1122)**	30
		SE5555	**† Signetics (1122)**	
±15	100 ma	XR1468	Exar	
		XR1568	† Exar	
		XR4195	Exar	
		MC1468	Motorola	
		MC1568	† Motorola	
		LM125	† National	
		LM225	National	
		LM325	National	
		RC4195	Raytheon	40
		RM4195	† Raytheon	
		SG1468	Silicon G	
		SG1568	† Silicon G	
		SG4501	Silicon G	
		TA7179	Toshiba	
	200 ma	**NE5554**	**Signetics (1122)**	
		SE5554	**† Signetics (1122)**	
		SG1501A	† Silicon G	
		SG2501A	Silicon G	
		SG3501A	Silicon G	50

Output Voltage	Output Current	Device	Source	Line

† Military Temperature Range (−55° to 125°C)

* Typical Values

LINEAR–Voltage Regulators (Cont'd)

Adjustable, Positive

Arranged in sequence by Output Voltage-High, Output Current, and then Output Voltage-Low.

Output Voltage Hi	Low	Output Current	Device	Source	Line
9	3	500 ma	806	† Beckman	
15	2.6	300 ma	LAS14U	Lambda	
	5	1.5 a	SI3580M	Sanken	
20	2	20 ma	300	Intersil	
			LM300	National	
			SFC2300	NPC	
			SG300	Silicon G	
	5	5a	**μA78HG**	**Fairchild (934,953)**	10
21	9	500 ma	802	† Beckman	
26	1.8	12 ma	CA3085	† RCA	
27	0	200ma	LH0075	† National	
			LH0075C	National	
30	3	Shunt	TL430	Signetics	
			TL430	TI	
	4.5	12 ma	LM305	AMD	
			μA305C	**Fairchild (934)**	
			305	Intersil	20
			LM305	Motorola	
			LM305	National	
			μPC141	NEC America	
			μPC325	NEC America	
			LM305	Raytheon	
			SG305	Silicon G	
			LM305	TI	
		50 ma	TA7186	Toshiba	
	2	20 ma	100	† Intersil	
			200	Intersil	30
			LM100	† National	
			LM200	National	
			SFC2100	† NPC	
			SFC2200	NPC	
			SG100	† Silicon G	
			SG200	Silicon G	
	5	500 ma	**μA78MG**	**Fairchild (934)**	
			μA78MG	† Signetics	
			μA78MGC	Signetics	
		1 a	**μA78G**	**Fairchild (934)**	40
			μA78G	† Signetics	
			μA78GC	Signetics	
	4	1.5 a	LAS15U	Lambda	
		2 a	LAS16U	Lambda	
		5 a	LAS19U	Lambda	
	3	1.8a	L200	SGS	
	2.6	3 a	LAS14U	Lambda	
	5	5 a	**μA78HG**	**Fairchild (934,953)**	
32	—	200 ma	M5199	Mitsubishi	50
	2.5	200 ma	MC1469G	Motorola	
		500 ma	MC1469R	Motorola	
	20	500 ma	804	† Beckman	
	—	1a	M5199A	Mitsubishi	
200 ma	3.3	200ma	TA7089	Toshiba	
32	1.2	3a	**LM150**	**† National (1060,1065)**	

(Continued)

Adjustable, Positive (Cont'd.)

Output Voltage Hi	Low	Output Current	Device	Source	Li
32	1.2	3a			(Cont'd.)
			LM250	**National (1060,1065)**	6
			LM350	**National (1060,1065)**	
		5 a	**LM138**	**† National (1060)**	
			LM238	**National (1060)**	
			LM338	**National (1060)**	
36	1.7	100 ma	CA3085A	† RCA	
	2.5	100 ma	**TL431**	**TI (1140)**	
37	5	25 ma	**μA376C**	**Fairchild (934)**	
			LM376	National	
			LM376	TI	7
		50 ma	SE550	† Signetics	
	2	150 ma	723	† AMD	
			723C	AMD	
			μA723C	**Fairchild (934)**	
			μA723M	† Fairchild	
			HA17723	Hitachi	
			723	† Intersil	
			723C	Intersil	
			MC1723	† Motorola	
			MC1723C	Motorola	8
			LM723	† National	
			LM723C	National	
			SFC2723C	† NPC	
			SFC2723EC	NPC	
			CA723	† RCA	
			CA723C	RCA	
			RC723	Raytheon	
			RM723	† Raytheon	
			μA723	† Signetics	
			μA723C	Signetics	9
			SA723C	Signetics	
			TDA0723	Signetics	
			SG723	† Silicon G	
			SG723C	Silicon G	
			μA723C	TI	
			μA723M	† TI	
	2.5	200 ma	MC1561G	† Motorola	
			MC1569G	† Motorola	
	1.2	500ma	SG117T	† Silicon G	
			SG217T	Silicon G	10
			SG317T	Silicon G	
			TL117L	† TI	
	2.5	500 ma	MC1561R	† Motorola	
			MC1569R	† Motorola	
	1.2	1.5 a	LM117	† Motorola	
			LM217	Motorola	
			LM317	Motorola	
			LM117H	**† National (1060)**	
			LM217H	**National (1060)**	
			LM317H	**National (1060)**	11
			SG117K	† Silicon G	
			SG217K	Silicon G	
			SG317K	Silicon G	
			LM117	† TI	
			LM217	TI	
			LM317	TI	
38	2	100 ma	SG3532	Silicon G	
		150 ma	LAS723	Lambda	
			LAS1000	Lambda	

† Military Temperature Range (−55° to 125°C)

* Typical Values

Bold face indicates additional data is provided on the page noted.

LINEAR–Voltage Regulators (Cont'd)

Output Voltage Hi	Low	Output Current	Device	Source	Line
Adjustable, Positive (Cont'd.)					
40	4.5	12 ma	LM105	AMD	
			LM205	AMD	
			μA105M	**† Fairchild (934)**	
			105	† Intersil	
			205	Intersil	
			LM105	† Motorola	
			LM205	Motorola	
			LM105	† National	
			LM205	National	
			SFC2105	† NPC	10
			SFC2205	NPC	
			LM105	† Raytheon	
			LM205	Raytheon	
			SG105	† Silicon G	
			SG205	Silicon G	
			LM105	† TI	
			LM205	TI	
		45 ma	LM305A	AMD	
			μA305AC	**Fairchild (934)**	
			305A	Intersil	20
			LM305A	National	
			SFC2305	NPC	
			SG305A	Silicon G	
			LM305A	Raytheon	
			LM305A	TI	
	2	50 ma	NE550	Signetics	
		150 ma	SE550L	† Signetics	
46	1.7	100 ma	CA3085B	† RCA	
48	2	100 ma	SG1532	† Silicon G	
			SG2532	Silicon G	30
		150 ma	LAS723B	Lambda	
			LAS1100	Lambda	
56	8	1 a	CJCA001	Solitron	
			CJCA007	Solitron	
57	1.2	1.5 a	**LM117HV**	**National (1060)**	
			LM217HV	**National (1060)**	
			LM317HV	**National (1060)**	
1000	0	100 ma	MC1466	Motorola	
			MC1566	† Motorola	
Adjustable, Negative					
21	9	500 ma	852	† Beckman	40
22	3.8	500 ma	TA7085	Toshiba	
24	2.2	5a	**μA79HGC**	**Fairchild (934,953)**	
27	0	200 ma	LH0076	† National	
			LH0076C	National	
30	0.035	20 ma	**μA304C**	**Fairchild (934)**	
			LM304H	Motorola	
			LM304	National	
			μPC142	NEC America	
			LM304	Raytheon	50
			SG304	Silicon G	
			LM304	TI	
	2.2	500 ma	**μA79MG**	**Fairchild (934)**	
			μA79MG	† Signetics	
			μA79MGC	Signetics	
		1 a	**μA79G**	**Fairchild (934)**	
			μA79G	† Signetics	
			μA79GC	Signetics	
	2.6	1.5 a	LAS18U	Lambda	

Output Voltage Hi	Low	Output Current	Device	Source	Line
Adjustable, Negative (Cont'd.)					
32	3.8	200 ma	MC1463G	Motorola	60
			MC1463R	Motorola	
		500 ma	MC1463R	Motorola	
			TA7085	Toshiba	
37	2	50 ma	SG1511	† Silicon G	
			SG3511	Silicon G	
	3.6	200 ma	MC1563G	† Motorola	
		500 ma	MC1563R	† Motorola	
	1.2	500 ma	**LM137H**	**† National (1061,1064)**	
			LM137P	**† National (1061,1064)**	70
			LM237H	**National (1061,1064)**	
			LM237P	**National (1061,1064)**	
			LM337H	**National (1061,1064)**	
			LM337P	**National (1061,1064)**	
			LM137L	† TI	80
		1.5 a	**LM137K**	**† National (1061,1064)**	
			LM137T	**† National (1061,1064)**	
			LM237K	**National (1061,1064)**	
			LM237T	**National (1061,1064)**	
			LM337K	**National (1061,1064)**	90
			LM337T	**National (1061,1064)**	
			LM237	TI	
			LM337	TI	
40	0.015	20 ma	**μA104M**	**† Fairchild (934)**	
			LM104H	† Motorola	
			LM204H	Motorola	
			LM104	† National	
			LM204	National	
			SFC2104	† NPC	100
			SFC2204	NPC	
			SG104	† Silicon G	
			SG204	Silicon G	
			SG304	Silicon G	
			LM104	† TI	
			LM204	TI	
56	8	1 a	CJCA002	Solitron	
			CJCA008	Solitron	
57	1.2	1.5 a	**LM137HV**	**† National (1061,1064)**	110
			LM237HV	**National (1061)**	
			LM337HV	**National (1061,1064)**	
Adjustable, Dual					
±20	±8	100 ma	MC1468L	Motorola	
			MC1568L	† Motorola	
			SG1468J	Silicon G	
			SG1568J	† Silicon G	
	±14.5	100 ma	MC1568R	† Motorola	
			MC1468R	Motorola	
			SG1468T	Silicon G	120
			SG1568T	† Silicon G	

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Values

LINEAR–Voltage Regulators (Cont'd)

Adjustable, Dual (Cont'd.)

Output Voltage Hi	Output Voltage Low	Output Current	Device	Source	Line
				(Cont'd.)	
±20	±5	200 ma	**NE5554**	**Signetics (1122)**	
±28	±10	100 ma	SG1501	† Silicon G	
			SG2501	Silicon G	
			SG3501	Silicon G	
			SG4501	Silicon G	
			SG3502	Silicon G	
			SG1502	† Silicon G	
			SG2502	Silicon G	
±32	±0.05	100 ma	RC4194D	Raytheon	10
			SG4194CJ	Silicon G	
		200 ma	RC4194TK	Raytheon	
			SG4194CR	Silicon G	
±42	±0.05	100 ma	XR4194M	† Exar	
			RM4194D	† Raytheon	
			SG4194MJ	† Silicon G	
		200 ma	XR4194MK	† Exar	
			RM4194TK	† Raytheon	
			SG4194MR	† Silicon G	

Switching Regulators

Output Voltage Hi	Output Voltage Low	Output Current	Device	Source		Line
Switching Regulator Circuits						20
			XR1524	**† Exar**	**(930)**	
			XR2524	**Exar**	**(930)**	
			XR3524	**Exar**	**(930)**	
			ZN1066	Ferranti		
			μA78S40	**Fairchild**	**(935)**	
			μA78S60	Fairchild		
			SH1605	**Fairchild**	**(954)**	
			MC3380	Motorola		
			MC3420	Motorola		
			MC3520	† Motorola		30
			TL494C	Motorola		
			TL494M	† Motorola		
			TL495C	Motorola		
			TL495M	† Motorola		
			LM1524	**† National**	**(1063)**	
			LM2524	**National**	**(1063)**	
			LM3524	**National**	**(1063)**	
			SL442	Plessey		
			CA3085	RCA		
			NE5560	**Signetics**	**(1123)**	40
			SE5560	Signetics		
			SG1524	† Signetics		
			SG2524	Signetics		
			SG3524	Signetics		
			TDA1060	Signetics		
			TDA2640	Signetics		
			SG1524	**† Silicon G**	**(1128)**	
			SG2524	**Silicon G**	**(1128)**	
			SG3524	**Silicon G**	**(1128)**	
			SG1524	† TI		50
			SG3524	TI		
			TL494C	**TI**	**(1144)**	
			TL494M	† TI		
			TL495C	**TI**	**(1144)**	
			TL497I	TI		
			TL497M	† TI		
			PIC600	Unitrode		
			PIC601	Unitrode		
			PIC610	Unitrode		
			PIC611	Unitrode		60
			PIC625	Unitrode		
			PIC626	Unitrode		
			PIC635	Unitrode		
			PIC636	Unitrode		

† Military Temperature Range (−55° to 125°C)

* Typical Values

Bold face indicates additional data is provided on the page noted.

LINEAR–Other Devices

Other Linear Devices

Function	Device	Source	Line
AC Amplifier, Quad, Single Supply	CA3048	RCA	
AC Detector (Detects presence or absence of ac signals, includes adjustable threshold and time delay.)	3050	Intech/FMI	
Active Filters (See also Linear-Telecommunications Circuits)	881	Beckman	
	UAF11	**Burr-Brown (921)**	
	UAF11H	† Burr-Brown	10
	UAF15	Burr-Brown	
	UAF15H	† Burr-Brown	
	AFT76	**Burr-Brown (921)**	
	UAF21	**Burr-Brown (921)**	
	UAF21H	**† Burr-Brown (921)**	
	UAF25	Burr-Brown	
	UAF25H	† Burr-Brown	
	UAF31	**Burr-Brown (921)**	
	UAF41	**Burr-Brown (921)**	
	CH1290	Cermetek	20
	CH1295	Cermetek	
	CH1296	Cermetek	
	FLT-U2	Datel	
	ACF7032C	GI	
	ACF7092C	GI	
	AF100	**† National (1073)**	
	AF150	**National (1073)**	
	AF151	**National (1073)**	
Active Filters, Bandpass, Adjusts 60-270 Hz	AF99	National	30
Active Filter, Voltage Controlled, 4 stage	**SSM2040**	**SSM (565)**	
Alarm Circuit	**S2561**	**AMI (644)**	
	MD4301A	Mitel	
	MD4301B	Mitel	
	MD4302A	Mitel	
	MD4303A	Mitel	
	MD4304A	Mitel	
	M5170	Mitsubishi	40
	L911	**Siliconix (1135)**	
	ULN-2232	Sprague	
	ULN-2425	Sprague	
	ULN-2601	Sprague	
Alarm Circuits, Triple Alert/Alarm (Each circuit has two inputs, when the first one is low an open collector LED driver is turned on. When the second one is low -independent of the first -the output is flashed at an adjustable rate).	3020	Intech/FMI	50
Alarm Circuits, Temperature	3030	Intech/FMI	
Alarm Circuits, Tone Alarm (Comparator with ac output)	3010	Intech/FMI	
Alarms, Voltage. See Voltage Alarms below.			
Amplifiers: See Linear-Amplifiers, Special Purpose and Operational Amplifiers			
Amplifier-Detector (for firing SCR's or operating relays)	ULN-2301	Sprague	60
Amplifier-SCR firing Circuit	ULN-2300	Sprague	

Other Linear Devices (Cont'd.)

Function	Device	Source	Line
Analog Memory, Triple (Three analog outputs which can be stepped up or down)	S175	Siemens	
Analog Multiplexer, 16-bit, Parallel-In, Serial Out	CCD16MUX	Micro Tech	
Analog Multiplexer, 16-bit, Serial-In, Parallel-Out	CCD16DMUX	Micro Tech	70
Analog to Digital Converter and vice versa (See Linear-Telecommunication Circuits: Delta Modulation and Companding A/D Converters			
Analog Shift Register, 130x2, with storage (See also Serial Analog Delay below)	CCD311	Fairchild	
Analog Shift Register (455x2)	CCD321	Fairchild	
Analog Shift Register, 185 stage, 190x2 stage	S10110	AMI	80
	S10111	AMI	
Analog Shift Register, 455 stage, video delay	R5102	Reticon	
Analog Shift Register, 910 stage, video delay	R5103	Reticon	
Analog Shift Register, 2000 stage, audio delay	R5101	Reticon	
Analog Shift Register, Quad 64 stage	CCD64	Micro Tech	
Analog Shift Register, 256 stage	CCD256SERP	Micro Tech	90
	CCD256SPS	Micro Tech	
Analog Shift Register, (Bucket Brigade Device) (Dual 64 stage, acts as a variable delay line in the audio range)	MN3003	Panasonic	
Analog Shift Register, (Bucket Brigade Device) (512 stage)	MN3002	Panasonic	
	MN3004	Panasonic	100
	NE502	Signetics	
	NE503	Signetics	
Analog Shift Register, (Bucket Brigade Device) Dual 512 stage, acts as a variable delay line in the audio frequency range)	MN3001	Panasonic	
Analog Shift Register, (Bucket Brigade Device) (1024 stage)	BBD3007	Panasonic	
Analog Shift Register, (Bucket Brigade Device) (4096 stage)	MN3005	Panasonic	110
Analog Signal Averager (32 sample)	R5701	Reticon	
Balanced Modulator	SL1025	Plessey	
Balanced Modulator/Demodulator	µA796C	Fairchild	
	MC1496	Motorola	
	MC1596	† Motorola	120
	MC12002	Motorola	
	MC12502	† Motorola	
	LM1496	National	
	LM1596	† National	
	AN610	Panasonic	
	SL640C	Plessey	

(Continued)

Other Linear Devices (Cont'd.)

Function	Device	Source	Line
Balanced Modulator/Demodulator (Cont'd.)	SL641C	Plessey	
	SL1001A	Plessey	
	SL1001B	Plessey	130
	SL1496	Plessey	
	SL1596	† Plessey	
	SL1640	Plessey	
	SL1641	Plessey	
	L025	SGS	
	S042	Siemens	
	MC1496	Signetics	
	MC1596	† Signetics	
	N5596	Signetics	
	TCA820	Signetics	140
	TCA240	Signetics	
	SG1496	Silicon G	
	SG1596	Silicon G	
	TA7320	Toshiba	
Double-Balanced Modulator/Demodulator	SL1696	Plessey	
	SL1796	Plessey	
Ring Modulator, four transistor	SL355	Plessey	
	TBA673	Plessey	150
	TBA673	Signetics	
	U350	Siliconix	
Blowout Resistant Transistor (simulates 40 v transistor with special protection)	LM195	† National	
	LM295	National	
	LM395	National	
Bucket Brigade Devices, See Analog Shift Registers this section			
Crystal Oscillators	SL680	Plessey	160
	SL1680	Plessey	
Comparators, Programmable with Memory (High/Low Comparator)	CA3098	† RCA	
	CA3099	† RCA	
Constant Current Source, 1 µa to 10 ma	LM134	† National	
	LM234	National	
	LM334	**National (1073)**	170
Constant Current Supply, to 0.6a	TDA1251	SGS	
Correlator, Analog to Analog	R5403	Reticon	
Correlator, Binary to Analog	R5401	Reticon	
	TDC1004	TRW	
Customized Arrays (Linear and Digital circuits, customized in final metalization)	XR-CHIP	Exar	180
	XR-I²L-CHIP	Exar	
	ULA	Ferranti	
	MONOCHIP	Interdesign	
	MOA	Interdesign	
	MOB	Interdesign	
	MOC	Interdesign	
	MOD	Interdesign	
	MOE	Interdesign	
	MOF	Interdesign	
	MOG	Interdesign	190
	MUA	Interdesign	

† Military Temperature Range (−55° to 125°C)

* Typical Values

LINEAR–Other Devices (Cont'd)

Function	Device	Source	Line
Other Linear Devices (Cont'd.)			
Data Acquisition System, 6 channel, sample/hold, pulse width output			
	μA9708	**Fairchild (944)**	
Data Acquisition System, 8 channel (expandable), sample/hold, 8-bit conversion			
	MN7100	Micro Net	
	MN7100H	† Micro Net	
	MN7110	Micro Net	
	MN7110H	† Micro Net	
	MN7120	Micro Net	
	MN7120H	† Micro Net	
Data Acquistion System, 16 channel 8-bit conversion			10
	ADC0816	**National (1073,1074,1084)**	
	ADC0817	**National (1074,1084)**	
	MM74C948	National	
Data Acquistion System, 8 channel differential, sample/hold, 12-bit conversion			
	HDAS-8MC	**Datel (660)**	
	HDAS-8MM	**† Datel (660)**	
Data Acquisition System, 8 channel differential, 16 channel single ended, sample/hold, 12 bit conversion (2 device set)			20
	AD363K	AD	
	AD563S	† AD	
Data Acquistion System, 16 channel, sample/hold, 12-bit conversion			
	HDAS-16MC	**Datel (660)**	
	HDAS-16MM	**† Datel (660)**	
DC to DC Converter			
	CS138	Cherry	30
	CS139	Cherry	
DC to DC Converter: See Regulators, Switching, under Linear - Voltage Regulators.			
Deglitcher (suppresses transients at outputs of D/A)			
	4902	Teledyne P	
Demodulator, Phase Sensitive, for synchro or resolver systems			
	MN2120	Micro Net	
	MN2120H	† Micro Net	
Divider (See also Multipliers/Dividers below)			40
	AD535J	AD	
	AD535K	AD	
	4291	**Burr-Brown (921)**	
Dual Transistors, Monolithic, Matched, See Linear-Arrays			
DVM Circuits-See Interface-Analog to Digital Converters, also Digital-Special			
Earth Leakage Detector			
	M54121	Mitsubishi	
Flasher (LED)			50
	MD4302AE	Mitel	
	MD4304AE	Mitel	
	LM3909	National	
	LM3909	Siliconix	
Fluid Detector (oscillator, balance detector)			
	CS166	Cherry	
	LM1830	National	
	ULN-2429	Sprague	
Frequency Switch, Programmable			
	MC3344	Motorola	60

Function	Device	Source	Line
Other Linear Devices (Cont'd.)			
Frequency/Tone Operated Devices-See Linear-Telecommunication Circuits			
Frequency to Voltage Converter (tachometer-speed switch)			
	LM2907	National	
	LM2917	National	
Frequency to Voltage (Pulse) Converter			
	SAK140	Signetics	
Frequency to Voltage/Voltage to Frequency Converter			
	VFC32	**Burr-Brown (658)**	
	VFC32M	**† Burr-Brown (658)**	
	VFC42	**Burr-Brown (658)**	70
	VFC42M	**† Burr-Brown (658)**	
	VFC52	**Burr-Brown (659)**	
	VFC52M	**† Burr-Brown (658)**	
	VFQ-1C	**Datel (682)**	
	XR4151C	Exar	
	XR4151M	† Exar	
	μA4151	Fairchild	
	μA7151	† Fairchild	
	A8400	**Intech/FMI (1027)**	
	A8402	**Intech/FMI (1028)**	80
	A8404	Intech/FMI	
	LM131	**† National (1074)**	
	LM131A	**† National (1077)**	
	LM231	National	
	LM231A	**National (1077)**	
	LM331	National	
	LM331A	**National (1077)**	
	RC4151	**Raytheon (1094)**	
	RM4151	† Raytheon	
	RV4151	Raytheon	90
	RC4152	**Raytheon (1096)**	
	RM4152	† Raytheon	
	RV4152	Raytheon	
	RC4153	**Raytheon (1098)**	
	RM4153	† Raytheon	
	9400	Teledyne S	
Function Generator (Counter, ROM, D/A), See also Linear-Phase Locked Loop Circuits			
	MN350	Micro Net	
	MN351	Micro Net	100
	MN352	Micro Net	
Hall Effect Devices (Sense magnetic field) See also Digital-Other Digital Devices			
	DN835	Panasonic	
	TCA450	Signetics	
	UGN-3501	Sprague	
	UGN-3600	Sprague	
	UGN-3601	Sprague	
Image Sensor, Circular, Self Scanning			
	RO64	Reticon	110
	RO720A	Reticon	
Image Sensor, 256x1, CCD			
	CCD110F	Fairchild	
Image Sensor, CC Photodiode, 256x1			
	CCPD256	Reticon	
Image Sensor, 1024x1, CCD			
	CCD131	Fairchild	
Image Sensor, CC Photodiode, 1024x1			
	CCPD1024	Reticon	
Image Sensor, 1728x1, CCD			
	CCD121H	Fairchild	120
Image sensor, CC Photodiode, 1728x1			
	CCPD1728	Reticon	

Function	Device	Source	Line
Other Linear Devices (Cont'd.)			
Image Sensor, Linear Self Scanning			
	IPL3010	IPI	
	IPL3016	IPI	
	IPL3032	IPI	
	IPL4050	IPI	
	IPL4064	IPI	
	IPL4100	IPI	130
	IPL4128	IPI	
	IPL4256	IPI	
	IPL7050	IPI	
	IPL7064	IPI	
	IPL7100	IPI	
	IPL7128	IPI	
	IPL7256	IPI	
	M128	IPI	
	M256	IPI	
	M512	IPI	140
	M768	IPI	
	M1024	IPI	
	MEL512	Panasonic	
	RL16	Reticon	
	RL64	Reticon	
	RL128	Reticon	
	RL256	Reticon	
	RL512	Reticon	
	RL512SF	Reticon	
	RL936	Reticon	150
	RL1024	Reticon	
	RL1024SF	Reticon	
	RL1728	Reticon	
	RL1872	Reticon	
	RL2048	Reticon	
Image Area Sensor, Self Scanning			
	2D1	IPI	
	RA32X32	Reticon	
	RA50X50	Reticon	
	RA100X100	Reticon	160
Image Area Sensor, 100x100, CCD			
	CCD202	Fairchild	
Image Area Sensor, 190x224, CCD			
	CCD211	Fairchild	
Impedance Converter (Gyrator)			
	AF120	National	
	TCA580	Signetics	
LED, Constant Current			
	NSL4944	National	
Level Detector, Precision, (with internal reference, Schmitt trigger action)			170
	CS127	Cherry	
	CS401	Cherry	
	CS402	Cherry	
	CS450	Cherry	
	M54101	Mitsubishi	
	M54120	Mitsubishi	
	TL560C	TI	
Level Detector, Precision Dual			
	CS122	Cherry	180
	CS129	Cherry	
	CS130	Cherry	
Level Meter, analog input drives a bar of LED's			
	M51903	Mitsubishi	
	M51904	Mitsubishi	
	LM2914	National	
	LB1405	Sanyo	
	UAA170	Siemens	
	UAA180	Siemens	
	TL489	TI	190

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Values

Bold face indicates additional data is provided on the page noted.

LINEAR–Other Devices (Cont'd)

Function	Device	Source	Line
Other Linear Devices (Cont'd.)			
Level Meter, analog input drives a bar of LED's (Cont'd.)			
	TL490	TI	
Level meter, analog input drives V.F. display			
	TL491	TI	
Light to Current Converter			
	LM1890	National	
	LM1891	National	
	LM1892	National	
Light to Frequency Converter			
	IPL13	IPI	10
Light Detector (with buffer amplifier)			
	MCC401	Cherry	
	IPL16	IPI	
	μPC558	NEC America	
	CA3062	RCA	
	U103	Telefunken	
	U123	Telefunken	
Light Activated Switch			
	MCC401	Cherry	
	MCC402	Cherry	20
	MCC450	Cherry	
	ZNP100	Ferranti	
	IPL15	IPI	
	IPL17	IPI	
	PS12	IPI	
	PS24	IPI	
	U102	Telefunken	
	U221	Telefunken	
	PF30	Unitrode	
	PR30	Unitrode	30
	PF60	Unitrode	
	PR60	Unitrode	
	PF100	Unitrode	
	PR100	Unitrode	
	PF200	Unitrode	
	PR200	Unitrode	
	PF300	Unitrode	
	PR300	Unitrode	
	PF400	Unitrode	
	PR400	Unitrode	40
Low Battery Indicator, triggers on 3v (for use with 3 NiCd cells)			
	ICM7201	Intersil	
Motor Load Control			
	PT-107	Photo Therm	
Motor, Stepping Motor Driver			
	SAA1027	Signetics	
Motor Speed Regulator (for small dc motors). See also Linear—Consumer Circuits.			
	MCC140	Cherry	50
	CS175	Cherry	
	μA7391	Fairchild	
	μA7392	Fairchild	
	LM1815	National	
	SL440	Plessey	
	TCA955	Siemens	
	TCA900	SGS	
	TCA910	SGS	
	TDA1003A	Signetics	
	TDA1006	Signetics	60
Multifunction Converter (generates output = (V1 ÷ V2)			
	LH0094	National	
Multipliers			
	XR2208	Exar	
		(Continued)	

Function	Device	Source	Line
Other Linear Devices (Cont'd.)			
Multipliers (Cont'd.)			
	XR2208M	† Exar	
	XR2228	**Exar (933)**	
	XR2228M	**† Exar (933)**	
	A8495	Intech/FMI	70
	A8595	† Intech/FMI	
	ICL8013C	Intersil	
	ICL8013M	† Intersil	
	MC1494	Motorola	
	MC1594	† Motorola	
	MC1495	Motorola	
	MC1595	† Motorola	
	SL1495	Plessey	
	SL1595	† Plessey	
	CA3091	† RCA	80
	SG1402	† Silicon G	
	SG2402	Silicon G	
	SG3402	Silicon G	
	SG1495	Silicon G	
	SG1595	† Silicon G	
	TA7158	Toshiba	
Multiplier, Dual (Linear-Antilog Voltage Controlled Amplifier)			
	SSM2000	SSM	
	SSM2020	**SSM (564)**	90
Multipliers/Dividers			
	AD530J	AD	
	AD530K	AD	
	AD530L	AD	
	AD530S	† AD	
	AD532J	AD	
	AD532K	AD	
	AD532S	† AD	
	AD533J	AD	
	AD533K	AD	100
	AD533L	AD	
	AD533S	† AD	
	AD534J	AD	
	AD534K	AD	
	AD534L	AD	
	AD534S	† AD	
	AD534T	† AD	
	4201	Burr-Brown	
	4203	**Burr-Brown (921)**	
	4203S	† Burr-Brown	110
	4204	**Burr-Brown (921)**	
	4204S	**† Burr-Brown (921)**	
	4205	**Burr-Brown (921)**	
	4205S	**† Burr-Brown (921)**	
	4206	**Burr-Brown (921)**	
	4213	**Burr-Brown (921)**	
	4213S	**† Burr-Brown (921)**	
	4214	**Burr-Brown (921)**	
	4214M	**† Burr-Brown (921)**	
	RC4200	**Raytheon (1102)**	120
	RC4200A	Raytheon	
Multifunction Convertors (XY/Z)expM			
	AD531J	AD	
	AD531K	AD	
	AD531L	AD	
	AD531S	† AD	
	4301	**Burr-Brown (921)**	
	4302	**Burr-Brown (921)**	
Noise Generator (psuedo-random sequence generator for audio)			130
	S2688	AMI	
	MM5837	National	

Function	Device	Source	Line
Other Linear Devices (Cont'd.)			
Oscillator/Buffer			
	LM175	† National	
	LM275	National	
	LM375	National	
Oscillator, Quadrature			
	4423	**Burr-Brown (921)**	
Overvoltage Protector			
	L2OV5	Lambda	140
	L2OV6	Lambda	
	L2OV9	Lambda	
	L2OV12	Lambda	
	L2OV15	Lambda	
	L2OV20	Lambda	
	L2OV24	Lambda	
	L2OV28	Lambda	
	L6OV5	Lambda	
	L6OV6	Lambda	
	L6OV9	Lambda	150
	L6OV10	Lambda	
	L6OV12	Lambda	
	L6OV15	Lambda	
	L6OV18	Lambda	
	L6OV20	Lambda	
	L6OV24	Lambda	
	L6OV28	Lambda	
	MC3423	Motorola	
	MC3523	† Motorola	
	MC3423	TI	160
	MC3523	† TI	
Parallel In, Serial Out (32 sample analog memory)			
	R5501	Reticon	
Peak Detector (senses and holds peak)			
	4085	**Burr-Brown (921)**	
	4085M	**† Burr-Brown (921)**	
	5902	† OEI	
AC Phase Control			
	U111	Telefunken	
Phase Control (for incandescent lamps controlled by touch plates)			170
	U229	Telefunken	
Phase Sensitive Demodulator			
	MN2120	Micro Net	
	MN2120H	† Micro Net	
PIN Diode Driver			
	DH0035	† National	
	DH0035C	National	
	UDS-5790	† Sprague	
	UDS-5791	† Sprague	180
Power Supply Control (Oscillator with variable mark/space for switching supplies) See Linear-Voltage Regulators, Switching			
	SL442	Plessey	
Power Supply Controller (voltage reference, pulse generator and timing circuitry, error amp)			
	TL496C	**TI (1148)**	
Power Supply Control (voltage reference, over and under voltage sensing)			
	XR1543	† Exar	190
	XR2543	Exar	
	XR3543	Exar	
	SG1543	**† Silicon G (1129)**	
	SG2543	**Silicon G (1129)**	
	SG3543	**Silicon G (1129)**	
Pressure Transducers, Absolute			
	LX1400A	National	
		(Continued)	

† Military Temperature Range (−55° to 125°C)

* Typical Values

LINEAR–Other Devices (Cont'd)

Function	Device	Source	Line
Other Linear Devices (Cont'd.)			
Pressure Transducers, Absolute		(Cont'd.)	
	LX1600A	National	
	LX1600AF	National	
	LX1700A	National	
	LX1700AF	National	
	LX1700AN	National	
	LX1700AFN	National	
Pressure Transducers, Gage			
	LX1600G	National	
	LX1700G	National	10
	LX1700GN	National	
Pressure Transducers, Differential			
	LX0603D	National	
Pressure Transducers, Backward Gage			
	LX0603GB	National	
	LX1600GB	National	
	LX1700GB	National	
	LX1600D	National	
	LX1700DD	National	
	LX1700DDF	National	20
Pulse Width (and PRF) to Voltage Converter			
	3910	OEI	
Read Amplifier/Preamplifier (for magnetic tape memories)			
	MC3467	Motorola	
	MC3468	Motorola	
Reference Diode Voltage (two terminal active circuit) 1.220v ±5%			
	MP5010	Micro Power	
	MP5010A	Micro Power	30
	LM113	**† National (1062)**	
	LM113-1	**† National (1062)**	
	LM113-2	**National (1062)**	
	LM313	**National (1062)**	
Reference Voltage, 1.23v			
	ICL8069	Intersil	
	ICL8069M	† Intersil	
Reference Voltage, 1.26v (two terminal active circuit)			
	ZN423	Ferranti	
Reference Voltage, 2.45 V (two terminal active circuit)			40
	ZN404	Ferranti	
	ZN458	Ferranti	
Reference Voltage, 2.5v			
	AD580J	AD	
	AD580K	AD	
	AD580L	AD	
	AD580S	† AD	
	AD580T	† AD	
	AD580U	† AD	
	MP5530	Micro Power	50
	MP5540	Micro Power	
	MC1403	Motorola	
	MC1503	† Motorola	
	LM136	**† National (1062)**	
	LM136A	**† National (1062)**	
	LM236	**National (1062)**	
	LM236A	**National (1062)**	
	LM336	**National (1062,1073)**	
	LM336A	National	60
	SG1503	**Silicon G (1128)**	
	SG2503	**Silicon G (1128)**	
	SG3503	**Silicon G (1128)**	
Reference voltage; 2.5, 5, 7.5, and 10v			
	AD584J	AD	
		(Continued)	

Function	Device	Source	Line
Other Linear Devices (Cont'd.)			
Reference voltage; 2.5, 5, 7.5, and 10v		(Cont'd.)	
	AD584K	AD	
	AD584L	AD	
	AD584S	† AD	
	AD584T	† AD	70
	AD584U	† AD	
Reference Voltage, 5v			
	MP5531	Micro Power	
	MP5541	Micro Power	
	LM136-5	**† National (1062)**	
	LM136A-5	**† National (1062)**	
	LM236-5	**National (1062)**	
	LM236A-5	**National (1062)**	
	LM336-5	**National (1062,1073)**	80
	LM336B-5	**National (1062)**	
	REF-02	† PMI	
	REF-02A	† PMI	
	REF-02C	PMI	
	REF-02D	PMI	
	REF-02E	PMI	
	REF-02H	PMI	
Reference Voltage, 6.9v temperature stabilized			
	LM129	**† National (1062)**	
	LM329	**National (1062,1073)**	90
	LM199	**† National (1062)**	
	LM299	**National (1062)**	
	LM399	**National (1060,1062,1073)**	
	LM199A	**† National (1062)**	
	LM299A	**National (1062)**	
	LM399A	**National (1060,1062)**	
	LM3999	**National (1062,1073)**	100
	LM129	† Raytheon	
	LM329	Raytheon	
	LM199	† Raytheon	
	LM299	Raytheon	
	LM399	Raytheon	
	LM199A	† Raytheon	
	LM299A	Raytheon	
	LM399A	Raytheon	
	LM3999	Raytheon	110
Reference Voltage, 10V(or - 10V)			
	AD2700J	AD	
	AD2700L	AD	
	AD2700S	† AD	
	AD2700U	† AD	
	AD2701J	AD	
	AD2701L	AD	
	AD2701S	† AD	
	AD2701U	† AD	
	AD581J	AD	120
	AD581K	AD	
	AD581L	AD	
	AD581S	† AD	
	AD581T	† AD	
	AD581U	† AD	
	HA-1600-5	**Harris (1016)**	
	HA-1610-2	**† Harris (1018)**	
	HA-1610-5	**Harris (1018)**	
	R675B-1	† Hybrid Sys.	
	R675C-1	Hybrid Sys.	130
	R675B-2	† Hybrid Sys.	
	R675C-2	Hybrid Sys.	
	R675B-4	† Hybrid Sys.	
		(Continued)	

Function	Device	Source	Line
Other Linear Devices (Cont'd.)			
Reference Voltage, 10V(or - 10V)		(Cont'd.)	
	R675C-4	Hybrid Sys.	
	R675B-5	† Hybrid Sys.	
	R675C-5	Hybrid Sys.	
	R675B-7	† Hybrid Sys.	
	R675C-7	Hybrid Sys.	
	R675B-8	† Hybrid Sys.	140
	R655C-8	Hybrid Sys.	
	MN2000	Micro Net	
	MN2000H	† Micro Net	
	MN2001	Micro Net	
	MN2001H	† Micro Net	
	MN2002	Micro Net	
	MN2002H	† Micro Net	
	MN2003	Micro Net	
	MN2003H	† Micro Net	
	MP5532	Micro Power	150
	MP5542	Micro Power	
	LH0070	**† National (1062,1073)**	
	REF-01	† PMI	
	REF-01A	† PMI	
	REF-01C	PMI	
	REF-01D	PMI	
	REF-01E	PMI	
	REF-01H	PMI	
Reference Voltage, 10.24v			160
	LH0071	**National (1062,1073)**	
Reference Voltage, ±10v			
	AD2702L	AD	
	AD2702U	† AD	
	R675B-3	† Hybrid Sys.	
	R675C-3	Hybrid Sys.	
	R675B-6	† Hybrid Sys.	
	R675C-6	Hybrid Sys.	
	MN2004	Micro Net	170
	MN2004H	† Micro Net	
	MN2005	Micro Net	
	MN2005H	† Micro Net	
Reference Voltage, Adjustable			
	TL430	TI	
Reference Diode (two terminal active circuit) 1.8 to 5.6v			
	LM103	† National	
Regulator Diode with Amplifier (6.8 to 11v)			180
	MCA-series	Motorola	
Residual Current Detector			
	M54122	Mitsubishi	
Resolver Systems: See Phase Sensitive Demodulator above			
	HRCDX-14	DDC	
	HRDC-10	DDC	
	HRDC-14	DDC	
	HRCT-14	DDC	
	HSCDX-14	DDC	190
	HSCT-14	DDC	
	HSDC-10	DDC	
	HSDC-14	DDC	
	HSDC-360	DDC	
	HXCDX-14	DDC	
	HXCT-14	DDC	
	HXDC-10	DDC	
	HXDC-14	DDC	
	MSDC-8700	DDC	

† Military Temperature Range (−55° to 125°C)

* Typical Values

Bold face indicates additional data is provided on the page noted.

LINEAR–Other Devices (Cont'd)

Other Linear Devices (Cont'd.)

Function	Device	Source	Line
Resolver System: Digital to Synchro Converter or Resolver			
	HDSC-14	DDC	
	9517	DDC	
	9518	DDC	
RMS to DC Converter			
	AD536J	AD	
	AD536K	AD	
	AD536AJ	AD	
	AD536AK	AD	
	AD536AS	† AD	
	4340	**Burr-Brown (921)**	10
	4341	**Burr-Brown (921)**	
	LH0091	† National	
	LH0091C	National	
Sample and Hold Circuits			
	LF198	AMD	
	LF298	AMD	
	LF398	† AMD	
	AD582	AD	
	AD582S	† AD	
	AD583K	AD	20
	AD583S	† AD	
	SHC23	Burr-Brown	
	SHC23ET	† Burr-Brown	
	SHC80	**Burr-Brown (659)**	
	SHC85	**Burr-Brown (659)**	
	SHC85ET	Burr-Brown	
	SHC298AM	**Burr-Brown (659)**	
	SHM-HUGC	**Datel (686)**	
	SHM-HUMM	**† Datel (686)**	
	SHM-IC-1	**Datel (685)**	30
	SHM-IC-1M	**† Datel (685)**	
	SHM-LM-2	**Datel (685)**	
	SHM-LM-2M	**† Datel (685)**	
	SHM-6GC	**Datel (686)**	
	SHM-6MM	**† Datel (686)**	
	SH-8518	DDC	
	μAF198	† Fairchild	
	μAF398	Fairchild	
	HA-2420	**Harris (1020)**	
	HA-2425	**† Harris (1020)**	40
	SH703	Hybrid Sys.	
	IH5110	† Intersil	
	IH5111	† Intersil	
	IH5112	Intersil	
	IH5113	Intersil	
	IH5114	Intersil	
	IH5115	Intersil	
	MN343	Micro Net	
	MN343H	† Micro Net	
	MN344	Micro Net	50
	MN344H	† Micro Net	
	MN346	Micro Net	
	MN346H	† Micro Net	
	MN347	Micro Net	
	MN347H	† Micro Net	
	MN7130	Micro Net	
	MN7130H	† Micro Net	
	LH0023	**† National (1073)**	
	LH0023C	**National (1073)**	
	LH0043	**† National (1073)**	60
	LH0043C	**National (1073)**	
	LH0053	**† National (1073)**	
	LH0053C	**National (1073)**	
	SHM6401	National	
	LF198	† National	
	LF298	National	
	LF398	**National (1073)**	
	SMP11E	PMI	

(Continued)

Other Linear Devices (Cont'd.)

Function	Device	Source	Line
Sample and Hold Circuits (Cont'd.)			
	SMP11F	PMI	70
	SMP81E	PMI	
	SMP81F	PMI	
	LF198	† Signetics	
	NE5537	**Signetics (1119)**	
	SE5537	**† Signetics (1119)**	
	CSH101A	† Teledyne C	
	4856	Teledyne P	
Sample and Hold Circuit, with multiplexer			
	MN7130	Micro Net	
	MN7130H	† Micro Net	80
SCR/TRIAC Control (Burst Control)			
	L121	SGS	
SCR/TRIAC Control (Phase Control)			
	SL440	Plessey	
	L120	SGS	
	UAA145	Telefunken	
	UAA146	Telefunken	
Serial Analog Delay (Analog storage units with read in/read out shift register) (See also Analog Shift Registers above)			90
	SAD100	Reticon	
	SAD512	Reticon	
	SAD512D	Reticon	
	SAD1024A	Reticon	
(Serial) Analog Delay, Tapped (Bucket Brigade with 32 taps)			
	TAD32A	Reticon	
Serial Analog Memory (Analog storage with independent read-in and read-out shift registers)			
	SAM64	Reticon	100
	SAM128LR	Reticon	
	SAM128V	Reticon	
Servo Amplifier, for motor control			
	SH3015	**Fairchild (956)**	
	NE543	Signetics	
	NE544	Signetics	
	NE644	Signetics	
Servo Controller, for VTR or dc servos			
	M51401	Mitsubishi	
Servo Controller, Proportional Control			110
	XR2264	Exar	
	XR2265	Exar	
Sinewave Generator: See also Linear-Phase Locked Loop Circuits			
	FX205	CMA	
Smoke Detectors: See Linear-Consumer Circuit			
Sonar Transceiver			
	LM1812	National	
Square Law Device (two quadrant)			
	SL645C	Plessey	120
Switch Driver, for power transistors			
	SG1629	† Silicon G	
	SG3629	Silicon G	
Switching Regulators. See Linear-Voltage Regulators, Switching			
Tachometer: See Frequency to Voltage and Frequency Switch above			
Temperature Controlled Differential Pair			
	μA726C	Fairchild	
	μA726M	† Fairchild	130

Other Linear Devices (Cont'd.)

Function	Device	Source	Line
Temperature Transducers			
	AD590J	AD	
	AD590K	AD	
	AD590L	AD	
	LM134	† National	
	LM234	National	
	LM334	**National (1073)**	
	LM135	† National	
	LM235	National	
	LM335	**National (1073)**	140
	LM3911	**National (1073)**	
	LM1913	† National	
	LM2913	National	
	LM3913	National	
	LX5600	† National	
	LX5700	† National	
	μPC3911	NEC America	
	REF-02	† PMI	
	REF-02A	† PMI	
	REF-02C	PMI	150
	REF-02D	PMI	
	REF-02E	PMI	
	REF-02H	PMI	
Thermal Converter (matched transistors, diffused resistors)			
	4131	Burr-Brown	
Threshold Switch (2/3 supply voltage)			
	CS102	Cherry	
	CS560	Cherry	
	TCA345	Siemens	160
Threshold Switch (Oscillator, switch with hysteresis)			
	TCA105	Siemens	
Tone Ringer (Generates ringing sound to operate a speaker)			
	S2561	**AMI (644)**	
	ML8204	Mitel	
	ML8205	Mitel	
Traffic Decoder (traffic signal control and detector)			
	LA2200	Sanyo	
Transversal Filter (Mask Programmed Weighting)			170
	R5602	Reticon	
Transversal Filter, Quad Chirped (for discrete Fourier Transform and power spectral density applications)			
	R5601-1	Reticon	
	R5601-2	Reticon	
Timers: See Linear-Timers			
Track and Hold			
	ADH-050	DDC	
	ADH-051	DDC	
Dual Voltage Level Alarm (activated if either input differs by more than ±5 to ±25% of selected value)			180
	3041	Intech/FMI	
Dual Voltage Level Indicator: See Window Discriminator below			
Quad Voltage Level Monitor/Alarm (activated if any of 4 inputs differs by more than ±5, ±10 or ±20% of selected value)			
	3040	Intech/FMI	
	ULN-2401	Sprague	
Voltage Detector, Indicator, Regulator, (Programmable Zener)			190
	ICL8211C	Intersil	
	ICL8211M	† Intersil	
	ICL8212C	Intersil	
	ICL8212M	† Intersil	

† Military Temperature Range (−55° to 125°C)

* Typical Values

LINEAR–Other Devices (Cont'd)

Function	Device	Source	Line
Other Linear Devices (Cont'd.)			
Voltage Overvoltage Protector. (Crowbar) See Overvoltage Protector above			
Voltage to Frequency Converter	AD537J	AD	
	AD537K	AD	
	AD537S	† AD	
	3930	OEI	
Voltage to Frequency/Frequency to Voltage Converter	**VFC32**	**Burr-Brown (658)**	
	VFC32M	**† Burr-Brown (658)**	
	VFC42	**Burr-Brown (658)**	
	VFC42M	**† Burr-Brown (658)**	
	VFC52	**Burr-Brown (659)**	10
	VFC52M	**† Burr-Brown (658)**	
	VFQ-1C	**Datel (682)**	
	XR4151	Exar	
	XR4151M	† Exar	
	µA4151	Fairchild	
	µA7151	Fairchild	
	A8400	**Intech/FMI (1027)**	
	A8402	**Intech/FMI (1028)**	
	A8404	Intech/FMI	
	LM131	**† National (1074)**	20
	LM131A	**† National (1077)**	
	LM231	National	
	LM231A	**National (1077)**	
	LM331	National	
	LM331A	**National (1077)**	
	3930	† OEI	
	RC4151	**Raytheon (1094)**	
	RM4151	† Raytheon	
	RV4151	Raytheon	
	RC4152	**Raytheon (1096)**	30
	RM4152	† Raytheon	
	RV4152	Raytheon	
	RC4153	**Raytheon (1098)**	
	RM4153	† Raytheon	
	9400	Teledyne S	
Window Discriminator (indicates when input is above or below two limits)	CS180	Cherry	
Window Discriminator (indicates voltage above, below, inside, or outside two adjustable limits)	TCA965	Siemens	40
Power Control Zero Voltage Switch	**SL445A**	**Plessey (1087)**	
Zero Voltage and Zero Crossing Triggers (Triac and SCR control)	µA742C	Fairchild	
	M5172	Mitsubishi	
	CA3059	Motorola	
	CA3079	Motorola	
	MC3370	Motorola	50
	SL443	Plessey	
	SL446	Plessey	
	SL447	Plessey	
	SL448	Plessey	
	SL449	† Plessey	
	CA3058	† RCA	
	CA3059	† RCA	
	CA3079	† RCA	
	TCA280	Signetics	
	TDA1023	Signetics	60
	TDA1024	Signetics	
	SG3058	† Silicon G	
	SG3059	Silicon G	
	SG3079	Silicon G	

(Continued)

Function	Device	Source	Line
Other Linear Devices (Cont'd.)			
Zero Voltage and Zero Crossing Triggers (Triac and SCR control) (Cont'd.)	U106	Telefunken	
	U112	Telefunken	
	7601-01	Telaris	
	7603-02	Telaris	70
	TL440C	TI	
	TA7606	Toshiba	

† Military Temperature Range (−55° to 125°C)

* Typical Values

Bold face indicates additional data is provided on the page noted.



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- RAM
- Static
- 1024x1
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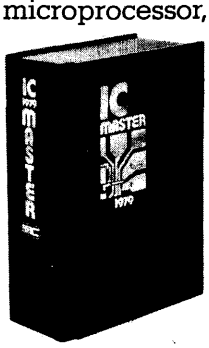
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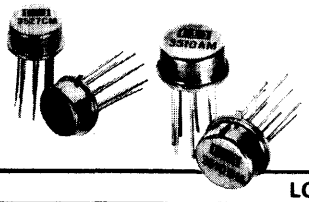
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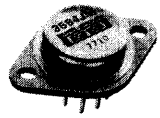
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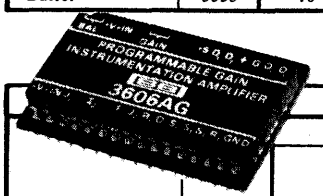




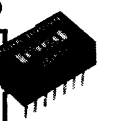


		RANGE OF SPECIFICATIONS							
		Rated Output		Offset Voltage at 25°C	Offset Voltage Temp. Drift	Bias Current at 25°C	Frequency Response Unity Gain	Frequency Response Slew Rate	
	Model	±V	±mA	mV	μV/°C	pA	MHz	V/μsec	Package
LOW DRIFT									
Chopper-Stabilized	3291	10	5	.02 - .10	.10 - 1	±50 to ±100	3	6	Module
	3354	10	5	.03 - .10	.10 - 1	±20 to ±50	6	6	Module
	3271	50 - 110	20	.05	1	±80	1	20	Module
Bipolar	3510	10	10	.06 - .15	0.5 - 2	±15 to ±35nA	0.4	0.5	TO-99
	3500	10	10	1 - 5	3 - 20	±15 to ±30nA	1.5	0.6 - 1	TO-99
	3501	10	5	2 - 5	5 - 20	±3 to ±15nA	0.5	0.1	TO-99
FET	3521	10	10	.25 - .50	1 - 10	-10 to -20	1	0.6	TO-99
	3527	10	10	.25 - .50	2 - 10	-2 to -5	1	0.6	TO-99
LOW BIAS CURRENT									
Varactor	3430	10	5	Adj to 0	10 - 30	±0.01	2kHz	.4V/msec	Module
	3431	10	5	Adj to 0	10 - 30	±0.01	2kHz	.4V/msec	Module
FET	3523	10	10	0.5 - 1	25 - 50	-0.1 - 0.5	1	0.6	TO-99
	3522	10	10	0.5 - 1	10 - 50	-1 to -10	1	0.6	TO-99
	3527	10	10	.25 - .50	2 - 10	-2 to -5	1	0.6	TO-99
	3521	10	10	.25 - .50	1 - 10	-10 to -20	1	0.6	TO-99
	3542	10	10	20	50	-25	1	0.5	TO-99
	3528	10	5	.1 - .2	5 - 10	±0.075 to -.30	0.7	0.3	TO-99
HIGH VOLTAGE									
FET	3584	65 - 145	15	3	25	-20	20	150	TO-3
	3583	40 - 140	75	3	25	-20	5	30	TO-3
	3580	10 - 145	15 - 60	3 - 10	25 - 30	-20 to -50	5	15 - 20	TO-3
HIGH CURRENT									
FET	3571	30	1A	2	40	-100	0.5	3	TO-3
	3572	30	2A	2	40	-100	0.5	3	TO-3
	3573	23	2A	5	10	15nA	1	2.6	TO-3
Buffer	3553	10	200	50	300	-200	32	2000	TO-3
	3329	10	100	50	-	bipolar	1	-	DIL

		Rated Output		Offset Voltage at 25°C	Offset Voltage Temp. Drift	Frequency Response A = BW	Frequency Response Slew Rate	t_s ±0.1%	Compensation	
	Model	±V	±mA	mV	μV/°C	MHz	V/μsec	nsec		Package
WIDEBAND										
Differential	3554	10	100	1 - 2	15 - 50	1000,A=1000	1000	120	ext	TO-3
	3551	10	10	1	50	50, A = 10	250	400	ext	TO-99
	3550	10	10	1	50	10 - 20, A = 1	65 - 100	400	int	TO-99
	3508	10	10	5	30	100, A = 100	20	-	ext	TO-99
	3507	10	10	10	30	20, A = 10	80	200	ext	TO-99
Buffer	3553	10	200	50	300	32	2000	-	-	TO-3



INSTRUMENTATION AMPLIFIERS

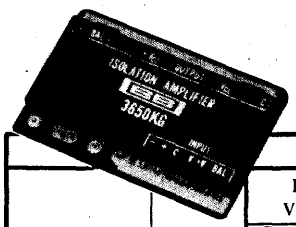


		Gain			Input Parameters		Dynamic Response	
	Model	Range (V/V)	Non-Linearity G = 100, max	Rated Output V/mA	CMR, DC to 60Hz, G = 10 1kΩ, Unbal	Offset Voltage vs Temp max (μV/°C)	G = 100 ±3dB, BW	Package
LOW DRIFT								
Lowest Drift	3620	0.1 - 10,000	±0.01%	±10/±10	74dB	±(10 + .25/G)	10kHz	Module
Low Drift, Low Cost	3626	5 - 1000	±0.01%	±10/±5	80dB, min	±(1 + 5/G)	14kHz	DIP
	3629	5 - 1000	±0.004%	±10/±10	90dB, min	±(0.75 + 5/G)	30kHz	DIP
General Purpose, Low Cost	3660	1 - 1000	±0.1%	±10/±10	76dB, min	±(10 + 1000/G)	72kHz	TO-100
	3662	1 - 1000	±0.05%	±10/±10	84dB	±(2 + 400/G)	72kHz	DIP
Buffer, Unity Gain, Differential	3627	1 (fixed)	±0.001% G = 1	±10/±5	100dB	20	800kHz G = 1	TO-99
Very-high Accuracy	3630	1 - 1000	±0.003%	±10/±5	96dB, min	±(.25 + 10/G)	25kHz	DIP
PROGRAMMABLE GAIN								
Digitally Controlled	3606	1 - 1024	0.003%	±10/±5	94dB	10μV/°C, typ ±(1 + 50/G)	50kHz	DIP

*Contact factory for current price.

FOR ADDITIONAL DETAILS REFER TO THE BURR-BROWN GENERAL CATALOG OR CONTACT YOUR NEAREST BURR-BROWN REPRESENTATIVE

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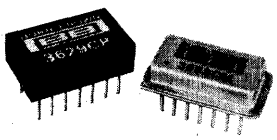
ISOLATION AMPLIFIERS

BURR-BROWN

TUCSON, ARIZONA 85734

	Model	Input Voltage Common Mode (V)	Input Voltage Differential (V)	Input Impedance Common Mode (Ω)	Input Impedance Differential (Ω)	Isolation Voltage Continuous (V)Peak	Isolation Voltage Pulse/Test (V)Peak	Isolation Mode Rejection, min DC (dB)	Isolation Mode Rejection, min 60Hz (dB)	Leakage Current at Test Voltage (μA)	Gain Nonlinearity max (%)	Gain Nonlinearity typ (%)	±3dB Freq. (kHz)	External Isolation Power Required	Package
TRANSFORMER COUPLED															
Low Drift, Bipolar	3450	±10	±15	5×10^9	10^7	±500	±2000	160	120	1	±0.01	±0.003	1.5	No	Module
Low Bias, FET	3451	±10	±15	10^{11}	10^{11}	±500	±2000	160	120	1	±0.05	±0.01	2.5	No	Module
	3452	±10	±15	10^{11}	10^{11}	±2000	±5000	160	120	1	±0.05	±0.01	2.5	No[1]	Module
	3455	±10	±15	10^{11}	10^{11}	[2]	[2]	160	120	[2]	±0.05	±0.01	2.5	No[1]	Module
True 3-wire Inst. Amp.	3456A	±10	±15	5×10^9	10^7	±2000	±5000	160	130	25	±0.01	±0.02	2.5	No	Module
	3456B	±10	±15	5×10^9	10^7	±2000	±5000	160	130	25	±0.01	±0.02	2.5	No	Module
OPTICALLY COUPLED															
Balanced Current Input	3650HG	±10	±15	10^9	25[3]	±2000	±5000	140	120	.25[4]	±0.02	±0.05	15	Yes[5]	DIP
	3650JG	±10	±15	10^9	25[3]	±2000	±5000	140	120	.25[4]	±0.02	±0.05	15	Yes[5]	DIP
	3650KG	±10	±15	10^9	25[3]	±2000	±5000	140	120	.25[4]	±0.02	±0.05	15	Yes[5]	DIP
Balanced FET Input	3652HG	±10	[6]	10^{11}	10^{11}	±2000	±5000	140	120	.25[4]	±0.05	±0.1	15	Yes[5]	DIP
	3652JG	±10	[6]	10^{11}	10^{11}	±2000	±5000	140	120	.25[4]	±0.05	±0.1	15	Yes[5]	DIP

(1) ±15V at ±10mA isolated power available to power external circuitry. (2) Isolation voltage tested at both ±5000Vp pulse test and 2500V, rms, 60Hz; leakage current tested for 2μA max, at 240V, rms, 60Hz. (3) 3650 is a current input device; to reduce input errors, very low input impedance is desirable. (4) At 240V/60Hz. (5) Models 700 or 710 isolated DC/DC converters may be used to provide isolated power. (6) Protected up to ±6000V.





ANALOG CIRCUIT FUNCTIONS

Model	RANGE OF SPECIFICATIONS: Accuracy at 25°C, max No Trimming Required	RANGE OF SPECIFICATIONS: Specification Temp. Range (°C)	Package
MULTIPLIER/DIVIDERS			
4203	1 - 2%	-55 to +150	TO-100
4204	0.25 - 0.50%	-55 to +125	DIP
4205	1 - 2%	-55 to +125	TO-100
4206	0.25% - 0.50%	0 to +70	DIP
4213	0.50 - 1%	-55 to +125	TO-100
4214	0.50 - 1%	-55 to +125	DIP

	Model	Comments	Package
SPECIAL FUNCTIONS			
Logarithmic Amplifier	4127	0.50 - 1% accuracy; 2 current input signals or 2 voltage input signals	DIP
Divider	4291	±0.25 to 1% untrimmed accuracy	DIP
Multifunction Converter (Multiply, divide, square root, etc.)	4301	Hermetically sealed metal package; compatible with 4302	DIP
	4302	$E_o = V_Y (V_Z/V_X)^m$; plastic package.	DIP
Peak Detector	4085	Read-out of DC voltage equal to peak value of complex wave form	DIP
RMS-to-DC Converter	4340	Laser-trimmed, no external trimming; metal package	DIP
	4341	Externally trimmed; low cost in plastic package	DIP
Oscillators	4023/25	Fixed-frequency (10Hz to 20kHz)	Module
	4423	Very-low cost, RC programmable, 0 to 20kHz	DIP
Comparators	4115/04	Provides window or dual limit for comparison	Module
	4082/03	Drives lamps, relays or logic loads	Module
Fixed-Frequency Active Filters	ATF76 Series	Pre-tuned, multiple pole bandpass, low-pass, and notch filters	DIP
Universal Active Filters	UAF41 UAF31 UAF21 UAF11	Variable type, 4-resistor, programmable, 2-pole filters; Q and f_c can be programmed; 3 outputs provide low-pass, high-pass and bandpass transfer functions; complex filter response by cascading.	DIP

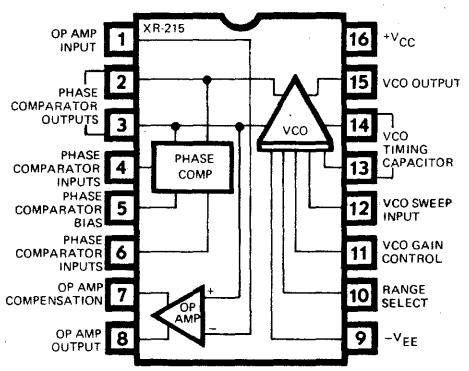
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XR-215 HIGH-FREQUENCY PHASE-LOCKED LOOP

The XR-215 is a highly versatile monolithic phase-locked loop (PPL) system designed for a wide variety of applications in both analog and digital communication systems. It is especially well suited for FM demodulation, frequency synthesis and tracking filter applications. The XR-215 operates over a power supply voltage ranging from 5V to 26V and has a wide frequency band of 0.5 Hz to 35 MHz. It can interface with conventional DTL, TTL, and ECL logic families.

FUNCTIONAL BLOCK DIAGRAM



FEATURES

Wide Frequency Range: 0.5 Hz to 35 MHz
Wide Supply Voltage Range: 5V to 26V
Digital Programming Capability
DTL, TTL, and ECL Logic Compatibility
Wide Dynamic Range: 300μV to 3V
ON-OFF Keying and Sweep Capability
Wide Tracking Range: Adjustable from ±1% to ±50%
High-Quality FM Detection: Distortion 0.15%
Signal/Noise 65 dB

APPLICATIONS

FM Demodulation
Frequency Synthesis
FSK Coding/Decoding (MODEM)
Tracking Filters
Signal Conditioning
FM, FSK, and Sweep Generation
Crystal Controlled Detection
Wideband Frequency Discrimination
Voltage-to-Frequency Conversion

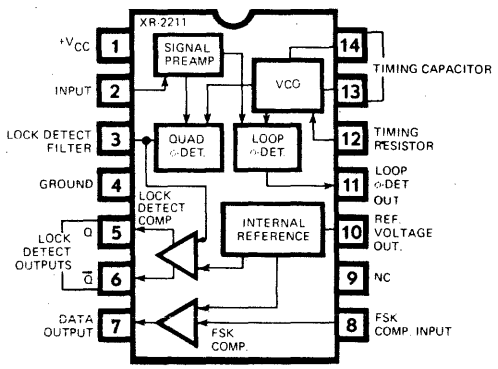
ORDER INFORMATION

Part Number	Package	Operating Temperature
XR-215	Ceramic	0°C to +75°C

XR-2211 FSK DEMODULATOR/ TONE DECODER

The XR-2211 is a monolithic phase-locked loop system especially designed for data communications and is particularly well-suited for FSK modem applications. It has a supply voltage range of 4.5V to 20V and a wide frequency range of 0.01 Hz to 300 kHz. The circuit accommodates analog signals between 2 mV and 3V and interfaces with conventional DTL, TTL, and ECL logic families. The XR-2211 consists of a basic PLL for tracking an input signal within the passband, a quadrature phase detector for carrier detection, and an FSK voltage comparator for FSK demodulation. Independent external components set center frequency, bandwidth, and output delay.

FUNCTIONAL BLOCK DIAGRAM



FEATURES

Wide Frequency Range	0.01 Hz to 300 kHz
Wide Supply Voltage Range	4.5V to 20V
DDT/TTL/ECL Logic Compatibility	
FSK Demodulation, with Carrier-Detection	
Wide Dynamic Range	2 mV to 3 Vrms
Adjustable Tracking Range (±1% to ±80%)	
Excellent Temperature Stability	20 ppm/°C, Typical

APPLICATIONS

FSK Demodulation
Data Synchronization
Tone Decoding
FM Detection
Carrier Detection

ORDER INFORMATION

Part Number	Package	Operating Temperature
XR-2211M	Ceramic	−55°C to +125°C
XR-2211N	Ceramic	−40°C to +85°C
XR-2211P	Plastic	−40°C to +85°C
XR-2211CN	Ceramic	0°C to +75°C
XR-2211CP	Plastic	0°C to +75°C

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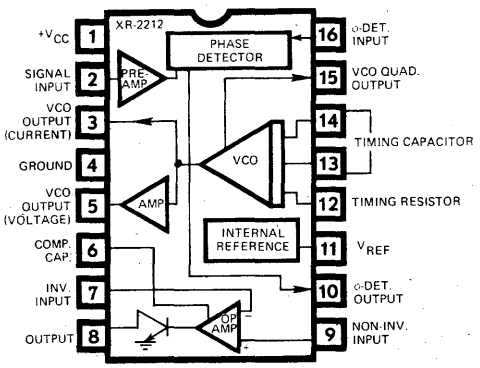
Phase-Locked Loops

XR-2212 PRECISION PHASE-LOCKED LOOP

The XR-2212 is an ultra-stable monolithic phase-locked loop (PLL) system especially designed for data communication and control system applications. It offers 20 ppm/°C temperature stability and is ideally suited for frequency synthesis, FM detection, and tracking filter applications.

The XR-2212 precision PLL is directly compatible with MOS, DTL, and TTL logic families and microprocessor peripheral systems. The circuit consists of a PLL system made up of an input preamplifier, a phase detector, a stable voltage-controlled oscillator (VCO), and a high-gain differential amplifier. The center frequency, bandwidth, and the tracking range of the PLL are controlled independently by the choice of external components.

FUNCTIONAL BLOCK DIAGRAM



FEATURES

Quadrature VCO Outputs	
Wide Frequency Range	0.01 Hz to 300 kHz
Wide Supply Voltage Range	4.5V to 20V
MOS/TTL/ECL Logic Compatibility	
Wide Dynamic Range	
Adjustable Tracking Range (±1% to ±80%)	
Excellent Temperature Stability	20 ppm/°C, Typical

APPLICATIONS

Frequency Synthesis	FSK Demodulation
Data Synchronization	Signal Conditioning
FM Detection	Clock Extraction
Tracking Filters	

ORDER INFORMATION

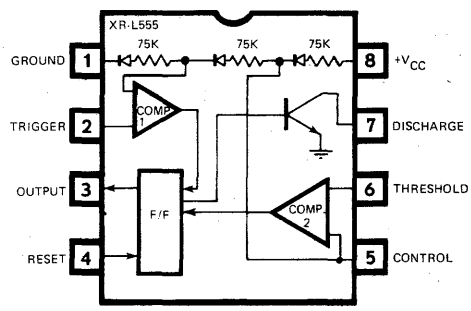
Part Number	Package	Operating Temperature
XR-2212M	Ceramic	−55°C to +125°C
XR-2212N	Ceramic	−40°C to +85°C
XR-2212P	Plastic	−40°C to +85°C
XR-2212CN	Ceramic	0°C to +75°C
XR-2212CP	Plastic	0°C to +75°C

Timing Circuits

XR-L555 MICROPOWER TIMING CIRCUIT

The XR-L555 is a stable micropower controller capable of producing accurate timing pulses with low power dissipation. Typical power dissipation is 900 microwatts at 5V. The circuit offers both the monostable or the astable modes of operation and can operate with power supplies as low as 2.7 volts. It may be triggered or reset on falling waveforms. The output can source up to 50 mA or drive TTL circuits. The XR-L555 features temperature stability and low-voltage operation, ideal as a micropower clock oscillator or VCO for low-power CMOS systems. It can operate up to 1500 hours with only two 300 mA-Hr NiCd batteries.

FUNCTIONAL BLOCK DIAGRAM



FEATURES

Pin Compatible with Standard 555 Timer
Less than 1 mW Power Dissipation (V+ = 5V)
Timing from Microseconds to Minutes
Over 1000-Hour Operation with 2 NiCd Batteries
Low Voltage Operation (V+ = 2.7V)
Operates in Both Monostable and Astable Modes
CMOS, TTL, and DTL Compatible Outputs
Adjustable Duty Cycle
Temperature Stability of .005%/°C

APPLICATIONS

Battery Operated Timing	Micropower Oscillator
Micropower Clock Generator	Sequential Timing
Pulse Shaping and Detection	Pulse-Width Modulation
Micropower PLL Design	Pulse Position Modulation
Missing Pulse Detection	Appliance Timing
Power-On Reset Controller	Remote-Control Sequencer

ORDER INFORMATION

Part Number	Package	Operating Temperature
XR-L555M	Ceramic	−55°C to +125°C
XR-L555CN	Ceramic	0°C to +75°C
XR-L555CP	Plastic	0°C to +75°C

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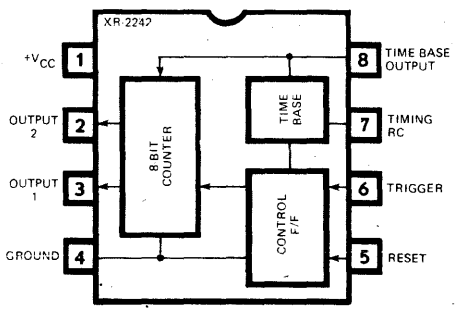
Timing Circuits

XR-2242 LONG-RANGE TIMER

The XR-2242 is a monolithic Timer/Controller capable of producing ultra-long time delays from microseconds to days. Two timing circuits can be cascaded to generate time delays or timing intervals of up to one year. The circuit is comprised of an internal time-base oscillator, an 8-bit binary counter and a control flip-flop. For a given external RC network connected to the timing terminal, the circuit produces an output timing pulse of 128 RC. If two circuits are cascaded, a total time delay of $(128)^2$ or 16,384 RC is obtained.

In monostable timer applications, the output terminal (pin 3) is connected back to the reset terminal, the circuit continues to operate in an astable mode, subsequent to a trigger input.

FUNCTIONAL BLOCK DIAGRAM



FEATURES

Timing from Microseconds to Days
Wide Supply Range: 4.5V to 15V
TTL and DTL Compatible Outputs
High Accuracy: 0.5%
Excellent Supply Rejection: 0.2%/V
Monostable and Astable Operation

APPLICATIONS

Long Delay Generation
Sequential Timing
Precision Timing
Ultra-Low Frequency Oscillator
Interval Timing

ORDER INFORMATION

Part Number	Package	Operating Temperature
XR-2242M	Ceramic	−55°C to +125°C
XR-2242CN	Ceramic	0°C to +75°C
XR-2242CP	Plastic	0°C to +75°C

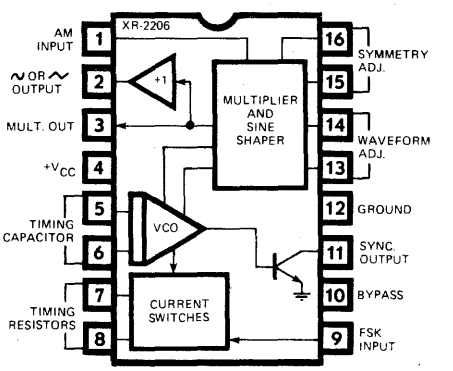
Function Generators

XR-2206 MONOLITHIC FUNCTION GENERATOR

The XR-2206 is a monolithic function generator integrated circuit capable of producing high quality sine, square, triangle, ramp, and pulse waveforms of high stability and accuracy. The output waveforms can be both amplitude and frequency modulated by an external voltage. Frequency of operation can be selected externally over a range of 0.01 Hz to more than 1 MHz.

This circuit is ideally suited for communications, instrumentation, and function generator applications requiring sinusoidal tone, AM, FM, or FSK generation. It has a typical drift specification of 20 ppm/°C.

FUNCTIONAL BLOCK DIAGRAM



FEATURES

Low Sinewave Distortion (THD .5%)
Insensitive to Signal Sweep
Excellent Stability (20 ppm/°C, Typical)
Wide Sweep Range (2000:1, Typical)
Low Supply Sensitivity (0.01%/V, Typical)
Linear Amplitude Modulation
Adjustable Duty-Cycle (1% to 99%)
TTL Compatible FSK Controls
Wide Supply Range (10V to 26V)

APPLICATIONS

Waveform Generation
Sine, Square, Triangle, Ramp
Sweep Generation
AM/FM Generation
FSK and PSK Generation
Voltage-to-Frequency Conversion
Tone Generation
Phase-Locked Loops

ORDER INFORMATION

Part Number	Package	Operating Temperature
XR-2206M	Ceramic	−55°C to +125°C
XR-2206N	Ceramic	0°C to +75°C
XR-2206P	Plastic	0°C to +75°C
XR-2206CN	Ceramic	0°C to +75°C
XR-2206CP	Plastic	0°C to +75°C

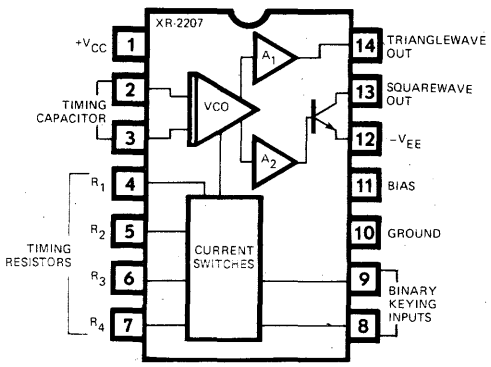
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XR-2207 VOLTAGE-CONTROLLED OSCILLATOR

The XR-2207 is a monolithic voltage-controlled oscillator (VCO) integrated circuit featuring excellent frequency stability and a wide tuning range. The circuit provides simultaneous triangle and squarewave outputs over a frequency range of 0.01 Hz to 1 MHz. It is ideally suited for FM, FSK, sweep or tone generation, and phase-locked loop applications.

The XR-2207 has a typical drift specification of 20 ppm/°C. The oscillator frequency can be linearly swept over a 1000:1 range with an external control voltage.

FUNCTIONAL BLOCK DIAGRAM



FEATURES

Excellent Temperature Stability (20 ppm/°C)
Linear Frequency Sweep
Adjustable Duty Cycle (0.1% to 99.9%)
Two or Four Level FSK Capability
Wide Sweep Range (1000:1 Minimum)
Logic Compatible Input and Output Levels
Wide Supply Voltage Range (±4V to ±13V)
Low Power Sensitivity (0.15%/V)
Wide Frequency Range (0.01 Hz to 1 MHz)
Simultaneous Triangle and Squarewave Outputs

APPLICATIONS

FSK Generation
Voltage and Current-to-Frequency Conversion
Stable Phase-Locked Loop
Waveform Generation
  Triangle, Sawtooth, Pulse, Squarewave
FM and Sweep Generation

ORDER INFORMATION

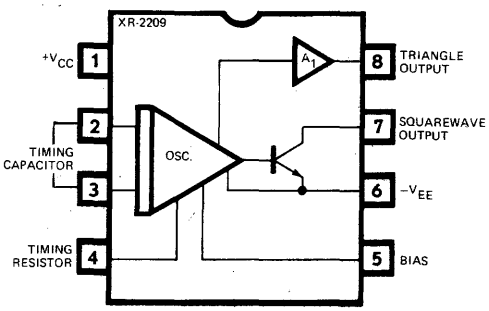
Part Number	Package	Operating Temperature
XR-2207M	Ceramic	−55°C to +125°C
XR-2207N	Ceramic	0°C to +75°C
XR-2207P	Plastic	0°C to +75°C
XR-2207CN	Ceramic	0°C to +75°C
XR-2207CP	Plastic	0°C to +75°C

XR-2209 PRECISION OSCILLATOR

The XR-2209 is a monolithic variable frequency oscillator circuit featuring excellent temperature stability and a wide linear sweep range. The circuit provides simultaneous triangle and squarewave outputs over a frequency range of 0.01 Hz to 1 MHz. The frequency is set by an external RC product. It is ideally suited for frequency modulation, voltage-to-frequency or current-to-frequency conversion, sweep or tone generation, as well as for phase-locked loop applications when used in conjunction with a phase comparator such as the XR-2208.

The circuit is comprised of three functional blocks: a variable frequency oscillator, and two buffer amplifiers. The XR-2209 has a typical drift specification of 20 ppm/°C. Its frequency can be linearly swept over a 1000:1 range with an external control signal.

FUNCTIONAL BLOCK DIAGRAM



FEATURES

Excellent Temperature Stability (20 ppm/°C)
Linear Frequency Sweep
Wide Sweep Range (1000:1 Minimum)
Wide Supply Voltage Range (± 4V to ± 13V)
Low Supply Sensitivity (0.15%/V)
Wide Frequency Range (0.01 Hz to 1 MHz)
Simultaneous Triangle and Squarewave Outputs

APPLICATIONS

Voltage and Current-to-Frequency Conversion
Stable Phase-Locked Loop Oscillator
Waveform Generation
FM and Sweep Generation

ORDER INFORMATION

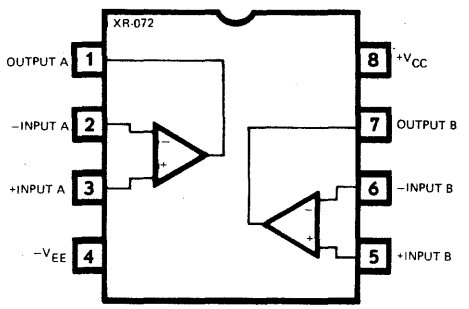
Part Number	Package	Operating Temperature
XR-2209M	Ceramic	−55°C to +125°C
XR-2209CN	Ceramic	0°C to +75°C
XR-2209CP	Plastic	0°C to +75°C

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XR-072 DUAL LOW-NOISE BIFET OPERATIONAL AMPLIFIER

The XR-072 family of junction-FET input dual op-amps are the low-noise version of Exar's XR-082 dual BIFET op-amp circuits. The combination of low noise, high slew-rate and the low output distortion characteristics of these op-amps make them ideal for high gain audio preamplification or analog signal processing systems.

FUNCTIONAL BLOCK DIAGRAM



FEATURES

Direct Replacement for Texas Instruments TL072
Low Noise (V_n = 18 nV/$\sqrt{Hz}$ Typ.)
Low Harmonic Distortion (0.01% Typ.)
Same Pin Configuration as XR-1458/XR-4558
Low Power Consumption
Low Input Bias and Offset Currents
Output Short-Circuit Protection
High Input Impedance . . . FET-Input Stage
Internal Frequency Compensation
Latch-Up-Free Operation
High Slew-Rate . . . 13 V/μs, Typ.

APPLICATIONS

High-Quality Audio Preamplification
Low-Level Signal Detection
Active Filter Design
Signal Conditioning
Analog Amplification
Audio Signal Processing

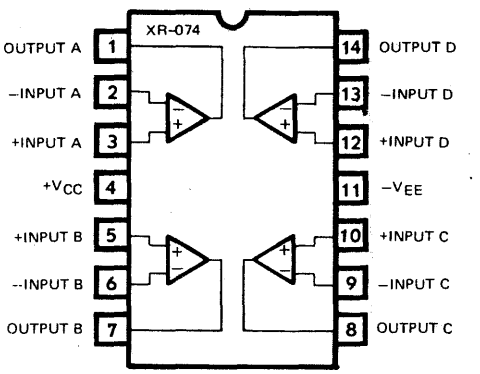
ORDER INFORMATION

Part Number	Package	Operating Temperature
XR-072M	Ceramic	−55°C to +125°C
XR-072N	Ceramic	−25°C to +85°C
XR-072P	Plastic	−25°C to +85°C
XR-072CN	Ceramic	0°C to +75°C
XR-072CP	Plastic	0°C to +75°C

XR-074 QUAD LOW-NOISE BIFET OPERATIONAL AMPLIFIER

The XR-074 junction FET-input quad operational amplifier is the low-noise version of Exar's XR-084 quad BIFET op-amp circuit. The low noise and low harmonic distortion characteristics make the XR-074 family of quad op-amps ideally suited for high-fidelity and audio preamplifier applications. Each of the four low-noise op-amps on the chip is fabricated using ion-implantation technology which combines well-matched junction FETs and high-performance bipolar transistors on the same monolithic integrated circuit.

FUNCTIONAL BLOCK DIAGRAM



FEATURES

Direct Replacement for Texas Instruments TL074
Low Noise (V_n = 18 nV/$\sqrt{Hz}$ Typ.)
Same Pin Configuration as XR-3403
High-Impedance Junction FET-Input Stage
Internal Frequency Compensation
Low Power Consumption
Low Harmonic Distortion (0.01% Typ.)
Output Short-Circuit Protection
High Slew-Rate . . . 13 V/μs, Typ.

APPLICATIONS

High-Quality Audio Preamplification
Low-Level Signal Detection
Active Filter Design
Signal Conditioning
Analog Amplification
Audio Signal Processing

ORDER INFORMATION

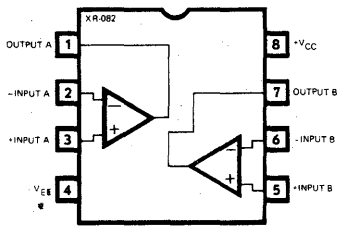
Part Number	Package	Operating Temperature
XR-074M	Ceramic	−55°C to +125°C
XR-074N	Ceramic	−25°C to +85°C
XR-074P	Plastic	−25°C to +85°C
XR-074CN	Ceramic	0°C to +75°C
XR-074CP	Plastic	0°C to +75°C

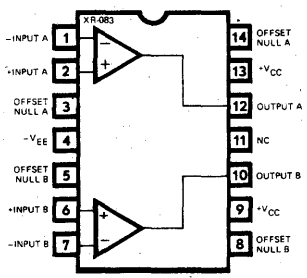
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XR-082/XR-083 DUAL BIFET OPERATIONAL AMPLIFIERS

The XR-082/XR-083 family of junction-FET input (BIFET) dual operational amplifiers are designed to offer high performance and a wider selection than conventional bipolar op-amps. Each amplifier features high slew rate, low input bias and offset currents, and low offset voltage drift with temperature.

FUNCTIONAL BLOCK DIAGRAMS





Note: Pins 9 and 13 are internally connected.

FEATURES

Direct Replacement for Texas Instrument TL082 and TL083
Low Power Consumption
Wide Common-Mode and Differential Voltage Ranges
Low Input Bias and Offset Currents
Output Short-Circuit Protection
High Input Impedance: FET Input Stage
Internal Frequency Compensation
Latch-Up Free Operation
High Slew Rate: 13V/μs, Typical

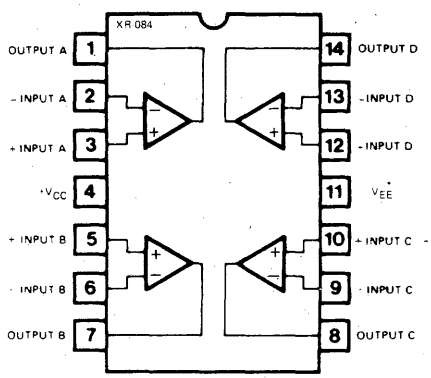
ORDER INFORMATION

Part Number	Package	Operating Temperature
XR-082M	Ceramic	−55°C to +125°C
XR-082N	Ceramic	−25°C to +85°C
XR-082P	Plastic	−25°C to +85°C
XR-082CN	Ceramic	0°C to +75°C
XR-082CP	Plastic	0°C to +75°C
XR-083M	Ceramic	−55°C to +125°C
XR-083N	Ceramic	−25°C to +85°C
XR-083P	Plastic	−25°C to +85°C
XR-083CN	Ceramic	0°C to +75°C
XR-083CP	Plastic	0°C to +75°C

XR-084 QUAD BIFET OPERATIONAL AMPLIFIER

The XR-084 junction-FET input (BIFET) quad operational amplifier is designed to offer higher performance than conventional bipolar quad op-amps. Each of the four op-amps on the chip is closely matched in performance characteristics, and each amplifier features high slew rate, low input bias and offset currents, and low offset voltage drift with temperature. The XR-084 FET input quad op-amp is fabricated using ion-implantation technology which combines well-matched junction FETs and high-performance bipolar transistors on the same monolithic integrated circuit.

FUNCTIONAL BLOCK DIAGRAM



FEATURES

Direct Replacement for Texas Instrument TL084
Same Pin Configuration as XR-3403, LM324
High-Impedance Junction-FET Input Stage
Internal Frequency Compensation
Low Power Consumption
Wide Common-Mode and Differential Voltage Ranges
Low Input Bias and Offset Currents
Output Short-Circuit Protection
Latch-Up Free Operation
High Slew Rate: 13V/μs, Typical

APPLICATIONS

Active Filter Design
Sample/Hold and Servo Systems
Audio Signal Processing
Analog Control Systems

ORDER INFORMATION

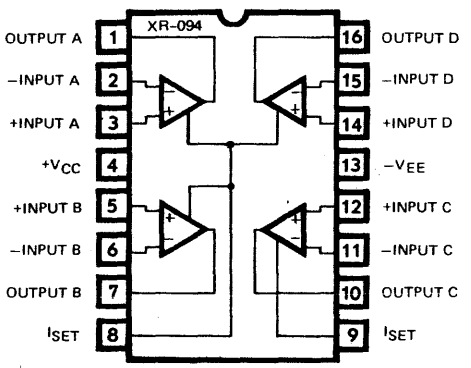
Part Number	Package	Operating Temperature
XR-084M	Ceramic	−55°C to +125°C
XR-084N	Ceramic	−25°C to +85°C
XR-084P	Plastic	−25°C to +85°C
XR-084CN	Ceramic	0°C to +75°C
XR-084CP	Plastic	0°C to +75°C

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XR-094 QUAD PROGRAMMABLE BIFET OPERATIONAL AMPLIFIER

The XR-094 is a programmable version of the XR-084 family of quad FET-input operational amplifiers. The circuit offers partitioned programming where the three of the four op-amps on the chip are programmed by one external bias-setting resistor, and the fourth op-amp is programmed by a second bias-setting resistor. These two external setting resistors permit the user to program the gain-bandwidth product, slew-rate and the supply current, especially for low power applications. The XR-094 programmable BIFET quad op-amp is fabricated using ion-implantation technology which combines well-matched junction FETs and high-performance bipolar transistors on the same monolithic integrated circuit.

FUNCTIONAL BLOCK DIAGRAM



FEATURES

Programmable Version of Texas Instruments TL084
Same Pin Configuration as LM146/246/346
Programmable for Micropower Operation
Partitioned Programming (Single/Triple Combination)
High-Impedance Junction-FET Input Stage
Internal Frequency Compensation
Low Input Bias and Offset Currents

APPLICATIONS

Active Filter Design
Sample/Hold and
Servo Systems
Audio Signal Processing
Analog Control Systems
Telephone Channel Filters

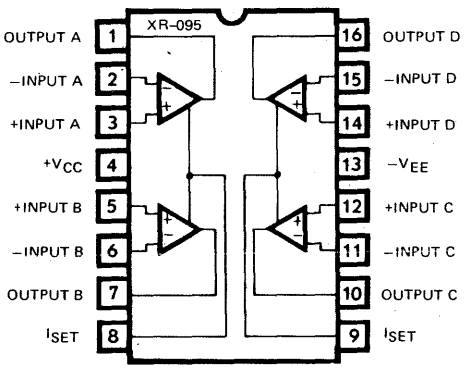
ORDER INFORMATION

Part Number	Package	Operating Temperature
XR-094M	Ceramic	−55°C to +125°C
XR-094N	Ceramic	−25°C to +85°C
XR-094P	Plastic	−25°C to +85°C
XR-094CN	Ceramic	0°C to +75°C
XR-094CP	Plastic	0°C to +75°C

XR-095 QUAD PROGRAMMABLE BIFET OPERATIONAL AMPLIFIER

The XR-095 is a programmable version of the XR-084 family of quad FET-input operational amplifiers. The circuit offers partitioned programming of the individual op-amp sections on the chip: two of the op-amps are programmed by one bias-setting resistor, and the remaining two op-amps are programmed by a separate bias-setting resistor. These two external setting resistors permit the user to program the gain-bandwidth product, slew-rate and the supply current, especially for low power applications. The XR-095 programmable BIFET quad op-amp is fabricated using ion-implantation technology which combines well-matched junction FETs and high-performance bipolar transistors on the same monolithic integrated circuit.

FUNCTIONAL BLOCK DIAGRAM



FEATURES

Programmable Version of Texas Instruments TL084
Same Pin Configuration as LM346-2
Partitioned Programming (Two Dual Combination)
Programmable for Micropower Operation
High-Impedance Junction-FET Input Stage
Internal Frequency Compensation
Low Input Bias and Offset Currents

APPLICATIONS

Active Filter Design
Sample/Hold and
Servo Systems
Audio Signal Processing
Analog Control Systems
Telecommunication Systems

ORDER INFORMATION

Part Number	Package	Operating Temperature
XR-095M	Ceramic	−55°C to +125°C
XR-095N	Ceramic	−25°C to +85°C
XR-095P	Plastic	−25°C to +85°C
XR-095CN	Ceramic	0°C to +75°C
XR-095CP	Plastic	0°C to +75°C

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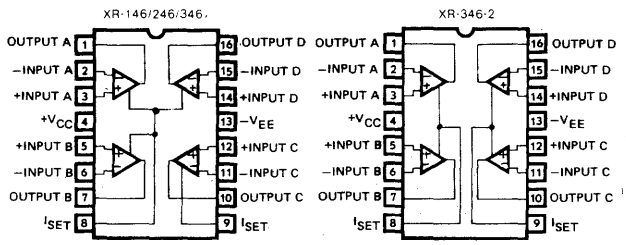
Operational Amplifiers

XR-146/246/346 PROGRAMMABLE QUAD OPERATIONAL AMPLIFIER

The XR-146 family of quad operational amplifiers contain four independent high-gain, low-power, programmable op-amps on a monolithic chip. The use of external bias setting resistors permit the user to program gain-bandwidth product, supply current, input bias current, input offset current, input noise and the slew rate.

The basic XR-146 family of circuits offer partitioned programming of the internal op-amps where one setting resistor is used to set the bias levels in the three op-amps, and a second bias setting is used for the remaining op-amp. Its modified version, the XR-346-2 provides a separate bias setting resistor for each of the two op-amp pairs.

FUNCTIONAL BLOCK DIAGRAMS



FEATURES

Direct Replacement for LM146/246/346 (XR-146 Family)
Direct Replacement for LM346-2 (XR-346-2)
Programmable Electrical Characteristics
Low Supply Current (350 μA per Amplifier)
Large DC Voltage Gain (120 dB)
Low Noise Voltage (25 nV/$\sqrt{\text{Hz}}$)
Wide Power Supply Range (±1.5V to ±22V)
Class AB Output Stage—No Crossover Distortion

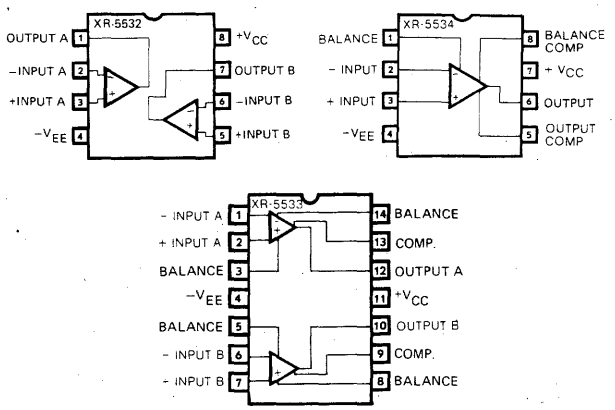
ORDER INFORMATION

Part Number	Package	Operating Temperature
XR-146M	Ceramic	−55°C to +125°C
XR-246N	Ceramic	−25°C to +85°C
XR-246P	Plastic	−25°C to +75°C
XR-346CN	Ceramic	0°C to +75°C
XR-346CP	Plastic	0°C to +75°C
XR-346-2CN	Ceramic	0°C to +75°C
XR-346-2CP	Plastic	0°C to +75°C

XR-5532/5533/5534 LOW-NOISE OPERATIONAL AMPLIFIER

The XR-5532/5533/5534 ultra-low noise operational amplifiers are especially designed for high quality audio and instrumentation applications. The XR-5532 and the XR-5534 both come in 8-pin packages. The XR-5532 is a dual op amp, and the XR-5533 is a 14-pin version of the XR-5532. Compared to the standard 741- or 301-type op amps, these operational amplifiers show an order of magnitude better noise performance and small-signal bandwidth, and higher output drive capability. They are all internally compensated, and the dual versions offer independent offset adjustments for each of the two op amps.

FUNCTIONAL BLOCK DIAGRAMS



FEATURES

Direct Replacement for NE5532
Ultra-Low Input Noise (4 nV/$\sqrt{\text{Hz}}$ Typ.)
Wide Small-Signal Bandwidth (10 MHz Typ.)
High Output Drive Capability (10 V rms into 600Ω)
Wide Supply Range (± 3V to ± 20V)
Wide Power Bandwidth (200 kHz)
High Slew-Rate: 6V/μsec Dual Version 13 V/μsec
Independent Offset Adjustments (Dual Versions)

APPLICATIONS

Professional Audio Equipment
Instrumentation and Servo Control
Telephone Channel Amplifier
Low-Level Signal Processing
Audio Preamplification

ORDER INFORMATION

Part Number	Package	Operating Temperature
XR-5532M/33M/34M	Ceramic	−55°C to +125°C
XR-5532CN/33CN/34CN	Ceramic	0°C to +75°C
XR-5532CP/33CP/34CP	Plastic	0°C to +75°C

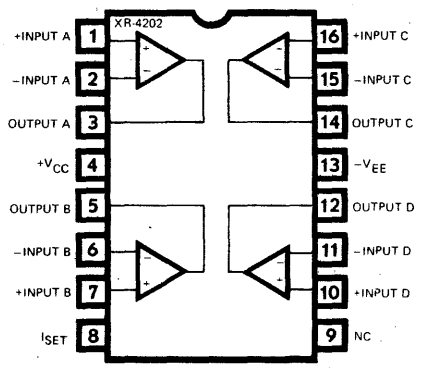
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Operational Amplifiers

XR-4202 PROGRAMMABLE QUAD OPERATIONAL AMPLIFIER

The XR-4202 is an array of four independent operational amplifiers on a single silicon chip. The operating current of the array is externally controlled by a single setting resistor or current source, allowing the user to trade-off power dissipation for bandwidth for all of the four amplifiers in the package.

FUNCTIONAL BLOCK DIAGRAM



FEATURES

Programmable
Micropower Operation
Wide Input Voltage and Common Mode Range
Internal Frequency Compensation
No Latch-Up
Matched Parameters
Short Circuit Protection

APPLICATIONS

Active Filter Design
Signal Conditioning
Analog Amplification
Audio Signal Processing

ORDER INFORMATION

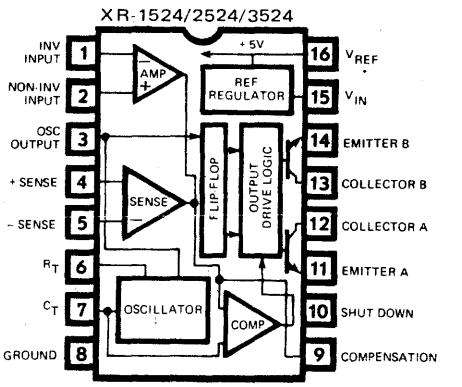
Part Number	Package	Operating Temperature
XR-4202N	Ceramic	−40°C to +85°C
XR-4202P	Plastic	−40°C to +85°C

Voltage Regulators

XR-1524/2524/3524 PULSE WIDTH MODULATING REGULATOR

This monolithic integrated circuit contains all the control circuitry for a regulating power supply inverter or switching regulator. Included in a 16-pin dual-in-line package is the voltage reference, error-amplifiers, oscillator, pulse-width modulator, pulse-steering flip-flop, dual alternating output switches and current-limiting and shut-down circuitry. This device can be used for switching regulators of either polarity, transformer coupled DC to DC converters, transformerless voltage doublers and polarity converters, as well as other power control applications. The XR-1524 is specified for operation over the full military temperature range of -55°C to +125°C, while the XR-2524 and XR-3524 are designed for commercial applications of 0°C to +70°C.

FUNCTIONAL BLOCK DIAGRAM



FEATURES

Direct Replacement for SG1524/2524/3524
Complete PWM Power Control Circuitry
Single-Ended or Push-Pull Outputs
Lines and Load Regulation of 0.2%
1% Maximum Temperature Variation
Total Supply Current Less than 10 mA
Operation Beyond 100 kHz

ORDER INFORMATION

Part Number	Package	Operating Temperature
XR-1524M	Ceramic	−55°C to +125°C
XR-2524N	Ceramic	0°C to +75°C
XR-2524P	Plastic	0°C to +75°C
XR-3524CN	Ceramic	0°C to +75°C
XR-3524CP	Plastic	0°C to +75°C

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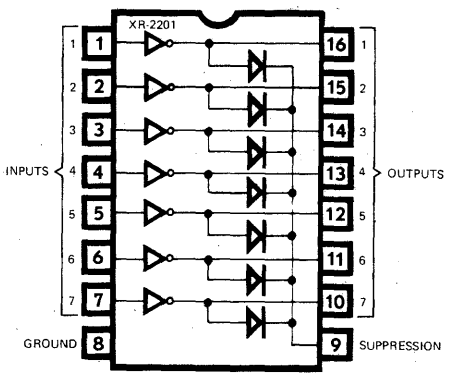
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High Current Drivers

XR-2201/2202/2203/2204 HIGH-VOLTAGE, HIGH-CURRENT DARLINGTON TRANSISTOR ARRAYS

The XR-2201/2202/2203/2204 Darlington transistor arrays are comprised of seven silicon NPN Darlington pairs on a single monolithic substrate. All feature open-collector outputs and internal protecton diodes for driving inductive loads. Peak inrush currents of up to 600 mA are allowable, making them also ideal for driving tungsten filament lamps. Although the maximum continuous collector current rating is 500 mA for each driver, the outputs may be paralleled to achieve higher load current capability.

FUNCTIONAL BLOCK DIAGRAM



FEATURES

High Peak Current Capability: 600 mA
Internal Protection Diodes for Driving Inductive Loads
Directly Compatible with TTL, CMOS, PMOS, and DTL Logic Families
Exact Replacement for Sprague Types ULN2001A, ULN2002A, ULN2003A, and ULN2004A

APPLICATIONS

Solenoid and Relay Driver
High Current LED Driver
Printing Calculator Hammer Driver
High Current Switch
Tungsten Lamp Driver

ORDER INFORMATION

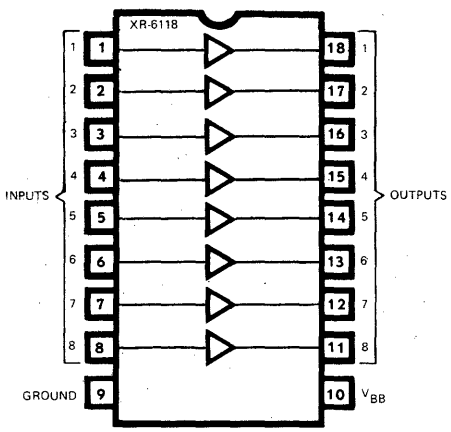
Part Number	Package	Operating Temperature
XR-2201CP	Plastic	0°C to +85°C
XR-2202CP	Plastic	0°C to +85°C
XR-2203CP	Plastic	0°C to +85°C
XR-2204CP	Plastic	0°C to +85°C

Display Drivers

XR-6118 FLUORESCENT DISPLAY DRIVER

The XR-6118 is a high-voltage monolithic IC consisting of eight NPN Darlington Output stages, along with their common-emitter type input stages. The circuit is designed to interface between low-level digital logic and high-voltage vacuum fluorescent displays. The XR-6118 is capable of driving the digits and/or segments of these displays and are designed to permit all eight outputs to be activated simultaneously. Pulldown resistors are incorporated into each output and no external components are required for most fluorescent display applications. It is directly compatible with standard or Schottky TTL, DTL, and 5-volt CMOS logic families.

FUNCTIONAL BLOCK DIAGRAM



FEATURES

Direct Replacement for Sprague UDN-6118A
Digit or Segment Drivers
Low Input Current
Integral Output Pulldown Resistors
Low Power
Reliable Monolithic Construction
High Output Breakdown Voltage

APPLICATIONS

Fluorescent Driver
Gas-Discharge Display Driver
High-Voltage Switching

ORDER INFORMATION

Part Number	Package	Operating Temperature
XR-6118N	Ceramic	0°C to +85°C
XR-6118P	Plastic	0°C to +85°C

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Semi-custom Bipolar Program

The Exar bipolar semi-custom design program offers a variety of "semi-custom" chips to fulfill various application performance requirements and complexities.

These semi-custom chips offer a unique method of manufacturing an almost unlimited variety of custom linear and digital integrated circuits with greatly reduced cost and development time. Exar makes this possible by stocking wafers that are completely fabricated except for the final process step of device interconnection which metalizes the selected components together in the required circuit configurations.

BIPOLAR SEMI-CUSTOM CHIPS

Chip Type	Chip Size in Mils	Breakdown Voltage	NPN	PNP
A100	73 X 83	22V	60	18
B100	85 X 85	22V	69	12
C100	87 X 78	28V	48	10
D100	80 X 80	36V	50	16*
+F100	91 X 110	22V	97	32*

+Presently under development

*Dual collector PNP transistors

Exar offers a design kit which contains simple instructions and guidelines for designing the metal mask as well as actual breadboard components (consisting of NPN and PNP arrays and integrated resistors), which are representative of the devices available on the semi-custom chips. This provides the design engineer with the ability to closely evaluate his design performance prior to integrating it on a monolithic chip.

Semi-custom I^2L Program

With the introduction of the I^2L Gate-Array chips, Exar has extended its semi-custom design program to the Integrated Injection Logic (I^2L) technology. This unique method of custom LSI development technique now makes it possible to manufacture an almost unlimited variety of digital or analog/digital circuits using I^2L technology, at a greatly reduced development cost and time.

I^2L SEMI-CUSTOM CHIPS

Characteristics	Chip Type		
	XR-300	XR-400	XR-500
Chip Size (mils)	104 X 140	111 X 111	122 X 185
I^2L Gates	288	272	520
Max. Operating Voltage			
A-Option	6V	6V	6V
B-Option	15V	15V	15V
Bipolar I/O Interfaces	28	38	40
Bonding Pads	34	38	42

The XR-300 and the XR-500 gate-arrays are intended primarily for digital LSI designs. The XR-400 gate-array features the advantages of combining analog and digital functions on the same IC chip. These I^2L gate-array chips are customized using two or more custom mask patterns which are simultaneously generated from a pencil layout, using Exar's unique computerized mask generation technique. In this manner, the chip layout is greatly simplified and gate-utilization efficiency is increased.

Exar also offers an I^2L design kit which is intended to familiarize the designer with the basic features of I^2L technology and provide helpful design guidelines in reducing his design from concept to breadboard and finally to the IC layout stage.

Full Custom Development

Exar offers a complete design and production capability for full-custom IC development using Exar's bipolar and I^2L technologies. This provides an excellent complement to Exar's unique semi-custom capability.

Exar's full-custom IC development and production capabilities offer complete flexibility to meet changing customer needs or design problems. We can develop a complete custom IC starting from your "black-box" specifications or reduce your working breadboard prototype to a monolithic chip. Alternately, if you have the facilities and resources to do the IC design and the layout, Exar will provide you with the device characteristics and IC layout rules for the particular process suitable to your design and review your IC layout for you. Then, Exar can generate the IC tooling and fabricate your IC prototypes for you.

Exar's bipolar process technology is compatible with the manufacturing processes available from many of the other IC manufacturers. Thus, if you have developed a set of IC tooling with another manufacturer and would like an alternate or substitute supplier for your custom IC product, in most cases your existing IC tooling may be directly compatible with Exar's technology.

Exar's Engineering Department has two custom IC design groups dedicated to the development of linear and digital custom LSI. We pride ourselves in our flexibility and quick response to your needs.

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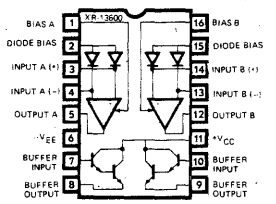
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Special Functions

XR-13600 DUAL OPERATIONAL TRANSCONDUCTANCE AMPLIFIER

The XR-13600 consists of 2 programmable transconductance amplifiers with high input impedance and push-pull outputs. The 2 amplifiers share common supplies but otherwise operate independently. Each amplifier's transconductance is directly proportional to its applied bias current. To improve signal-to-noise performance, predistortion diodes are included on the inputs. Independent Darlington emitter followers are included to buffer the outputs. Other XR-13600 features: direct replacement for LM-13600, transconductance adjustable over 4 decades, excellent transconductance-control linearity. Other applications: current-controlled amplifiers, impedances, filters, and oscillators; multipliers/attenuators; sample-and-hold circuits; and electronic music synthesis. Available in commercial grade plastic package.

FUNCTIONAL BLOCK DIAGRAM



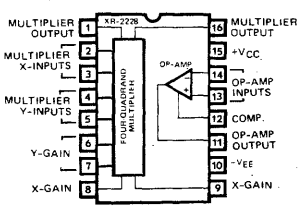
ORDER INFORMATION

Part Number	Package	Operating Temperature
XR-13600CP	Plastic	0°C to +75°C

XR-2228 MULTIPLIER/ DETECTOR

The XR-2228 multiplier/detector circuit is designed as a basic building block for analog signal processing and communication systems. Because of its wide common-mode range and differential inputs, the XR-2228 can interface with any of the existing PLL circuits in designing synchronous AM detection or frequency translation systems. It can be used as a phase-detector for frequencies up to 100 MHz. Other applications: AM generation, triangle-to-sinewave conversion, and frequency translation. Available in military and commercial grade ceramic packages or commercial plastic.

FUNCTIONAL BLOCK DIAGRAM



ORDER INFORMATION

Part Number	Package	Operating Temperature
XR-2228M	Ceramic	−55°C to +125°C
XR-2228CN	Ceramic	−40°C to +85°C
XR-2228CP	Plastic	0°C to +75°C

Application Notes & Technical Literature

Exar's technical staff and applications engineers have prepared a number of application notes and comprehensive Data Books which cover most of the key features and applications of Exar's IC products.

APPLICATION NOTES

AN-01: Stable FSK Modems Featuring the XR-2206, XR-2207 and XR-2211
AN-02: XR-C240 Monolithic PCM Repeater
AN-03: Active Filter Design With IC Op Amps
AN-04: XR-C277 Low-Voltage PCM Repeater IC
AN-05: Tri-State FSK Modem Design Using XR-2206/ XR-2211
AN-06: Precision PLL System Using XR-2207/ XR-2208
AN-07: Single-Chip Frequency Synthesizer Employing the XR-2240
AN-08: Dual-Tone Decoding with XR-567 and XR-2567
AN-09: Sinusoidal Output From XR-215 Monolithic PLL Circuit
AN-10: XR-C262 High-Performance PCM Repeater
AN-11: A Universal Sinewave Converter Using the the XR-2208 and XR-2211
AN-12: A Wide Tracking Range Precision PLL System Using the XR-2212 and XR-4151
AN-13: Frequency Selective AM Detection Using Monolithic Phase-Locked Loops
AN-14: A Complete Function Generator System Using the XR-2206
AN-15: An Electronic Music Synthesizer Using the XR-2207 and the XR-2240
AN-16: Semi-Custom LSI Design with I^2L Gate Arrays
AN-17: XR-C409 Monolithic I^2L Test Circuit

TECHNICAL LITERATURE

Timer Data Book. Provides a collection of technical articles and application information on monolithic timer IC products.

Phase-Locked Loop Data Book. Covers the fundamentals of design and applications of monolithic phase-locked loop (PLL) circuits.

Function Generator Data Book. Contains a number of technical articles and application notes on monolithic voltage-controlled oscillator (VCO) and function generator IC products.

Operational Amplifier Data Book. Contains a collection of technical articles on the fundamentals of monolithic IC op amps.

Applications Data Book. Contains a complete and up-to-date set of application notes prepared by Exar's technical staff on FSK modems, active filters, telecommunication circuits, electronic music synthesis and many more.

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LINEAR VOLTAGE REGULATOR

DEVICE TYPE	PACKAGE TYPE	STANDARD V_{OUT} RANGE	STANDARD I_{OUT}	THERMAL RESISTANCE 0°/W		FUNCTION POLARITY
				PACKAGE	ΘJC	
μA78CB	TO-220 TO-3	13.8 V	2 A	TO-220 TO-3	5.0 5.5	fixed positive
μA79M00	TO-220 TO-39	-5 V -6 V -8 V -12 V -15 V -20 V -24 V	500 mA	TO-220 TO-39	5.0 25	fixed negative
μA7900	TO-220 TO-3	-5 V -6 V -8 V -12 V -15 V -18 V -24 V	1 A	TO-220 TO-3	5.0 5.5	fixed negative
μA78MG	8Z (U1C) TO-39 (4 LD)	5 - 30 V	500 mA	8Z (U1) TO-39	11 25	adjustable positive
μA78G	8Z (U1C) TO-3 (4 LD)	5 - 30 V	1 A	8Z (U1) TO-3	11 5.5	adjustable positive
μA79G	8Z (U1C) TO-3 (4 LD)	-2.2, -30 V	1 A	8Z (U1) TO-3	11 5.5	adjustable negative
μA79MG	8Z (U1C) TO-39 (4 LD)	-2.2, -30 V	500 mA	8Z (U1) TO-39	11 25	adjustable negative
μA105 **μA305** **μA376** **μA305A**	TO-5 9T	4.5 - 40 V 4.5 - 40 V 4.5 - 40 V 4.5 - 40 V	12 mA 12 mA 25 mA 45 mA	TO-5 9T	* *	adjustable positive
μA104 **μA304**	5N 5N	-.015 - 40 V -.035 - 30 V	25 mA 25 mA	5N 5N	* *	adjustable negative
μA78HG	TO-3	5 - 24 V	5 A	TO-3	2.5	adjustable positive hybrid
μA79HG	TO-3	-2.25 - 24 V	5 A	TO-3	3.0	adjustable negative hybrid
μA78H00	TO-3	5 V, 12 V, 15 V	5 A	TO-3	2.5	fixed positive hybrid
μA109 **μA209** **μA309**	TO-3	5 V 5 V 5 V	1 A	TO-3	5.5	fixed positive
SH323SC	TO-3	5 V	3 A	TO-3	5.5	fixed positive hybrid
μA78P05	TO-3	5 V	10 A	TO-3	5.5	fixed positive hybrid
μA78S40	9B	1.3 to 40 V	1.5 A	9B	*	switching regulator
μA723	5N 6A 9A	2 - 37 V	150 mA	5N 6A 9A	* * *	general purpose regulator

*REFER TO VR HANDBOOK FOR FURTHER INFORMATION.

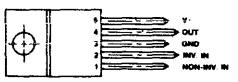
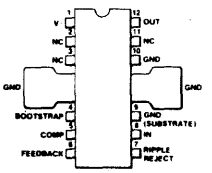
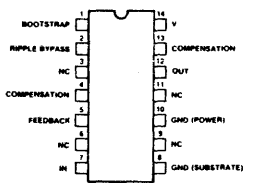
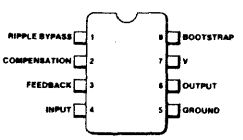
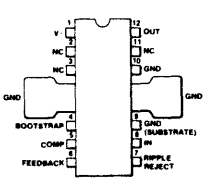
FAIRCHILD
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LINEAR VOLTAGE REGULATOR

DEVICE TYPE	PACKAGE TYPE	STANDARD V_{OUT} RANGE	STANDARD I_{OUT}	THERMAL RESISTANCE 0°/W		FUNCTION POLARITY
				PACKAGE	ΘJC	
μA78L00	TO-92 TO-39	2.6 V 5.0 V 6.2 V 8.0 V 8.2 V 9.0 V 12.0 V 15.0 V 18.0 V 24.0 V	100 mA	TO-92 TO-39	* 25	fixed positive
μA78C00	8Y (U1C) (TO-202)	8 V 10 V 12 V 15 V 17 V 18 V 20 V 22 V 24 V	500 mA	8Y (U1)	8.0	fixed positive
μA78M00	TO-220 8Y (U1C) TO-39	5 V 6 V 8 V 12 V 15 V 20 V 24 V	500 mA	TO-220 8Y (U1) TO-39	5.0 8.0 25	fixed positive
μA7800	TO-220 TO-3	5 V 6 V 8 V 8.5 V 12 V 15 V 18 V 24 V	1 A	TO-220 TO-3	5.0 5.5	fixed positive

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LINEAR POWER AUDIO

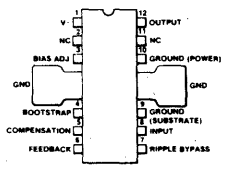
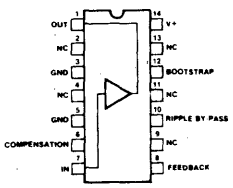
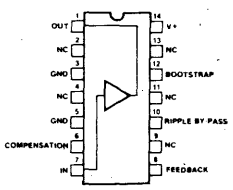
DEVICE TYPE	PIN CONFIGURATION	TYPICAL PERFORMANCE			FEATURES			PACKAGE INFORMATION		TYPICAL APPLICATIONS
		SUPPLY VOLTAGE V	SPEAKER IMPEDANCE Ω	POWER OUTPUT W	OVER-VOLTAGE PROTECTION	THERMAL SHUTDOWN	AC SHORT-CIRCUIT PROTECTION	PACKAGE OUTLINE	THERMAL RESISTANCE MAX °C/W	
TDA2002V **TDA2002H**		16 16 14.4 14.4	2 4 2 4	10 6.5 8 5.2	X	X	X	GO-V GO-H	4 4	• Automotive, Mobile and CB radios • General purpose audio
TDA2002AV **TDA2002AH**		16 16 14.4 14.4	2 4 2 4	10 6.5 8 5.2		X	X	GO-V GO-H	4 4	• General purpose audio
μA783P3C **μA783P4C**		24 24 14.4 6	8 16 4 4	9 5 6 1		X		P3C P4C	12 10	• High voltage (to 30 V) line operated radios, TV and HI-FI • Aircraft audio applications
TBA820 **TBA820L**		12 9 9 6 3.5	8 4 8 4 4	2 1.6 1.2 0.75 0.22				9C 9A	80 80	• Low power radio & TV • Battery operated general purpose audio • Low voltage applications
μA7307TC		9 9 6 3.5 3	4 8 4 4 4	1.6 1.2 0.75 0.22 0.09				9T	95	• Low cost, low voltage • Low power applications • Battery operated equipment
TBA810DS **TBA810DAS**		16 14.4 9 6	4 4 4 4	7 6 2.5 1	X	X		P3C P4C	12 10	• Automotive, Mobile and CB radios • General purpose audio
TBA810S **TBA810AS**		16 14.4 9 6	4 4 4 4	7 6 2.5 1		X		P3C P4C	12 10	• General purpose audio

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LINEAR POWER AUDIO

DEVICE TYPE	PIN CONFIGURATION	TYPICAL PERFORMANCE			FEATURES			PACKAGE INFORMATION		TYPICAL APPLICATIONS
		SUPPLY VOLTAGE V	SPEAKER IMPEDANCE Ω	POWER OUTPUT W	OVER-VOLTAGE PROTECTION	THERMAL SHUTDOWN	AC SHORT-CIRCUIT PROTECTION	PACKAGE OUTLINE	THERMAL RESISTANCE MAX °C/W	
TBA800 **TBA800A**		24 16	16 8	5 3				P3C P4C	12 10	• TV sound output • Line operated radios and TV • Small screen TV vertical deflection
706APC*		16 14 9 6	4 4 4 4	7 5.5 2.2 1				9H	11	• Normally used in low power applications without additional heatsink • General purpose audio • Battery operated radios
706BPC*		16 14 9 6	4 4 4 4	7 5.5 2.2 1				9J	12	• Normally used in higher power applications than the μA706APC • General purpose audio • Line and battery operated radios & HI-FI
TBA641A12*		9 9 6	8 4 4	1.2 2.2 1				9H quil	11	• Low power radio and TV • Battery operated general purpose equipment
TBA641B11*		14 9	4 4	4.5 2.2				9J quil	12	• General purpose audio

*NOT RECOMMENDED FOR NEW DESIGNS

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μAF771 SINGLE • μAF772 DUAL • μAF774 QUAD BIFET

FET INPUT OPERATIONAL AMPLIFIER FAMILY

FAIRCHILD LINEAR INTEGRATED CIRCUITS

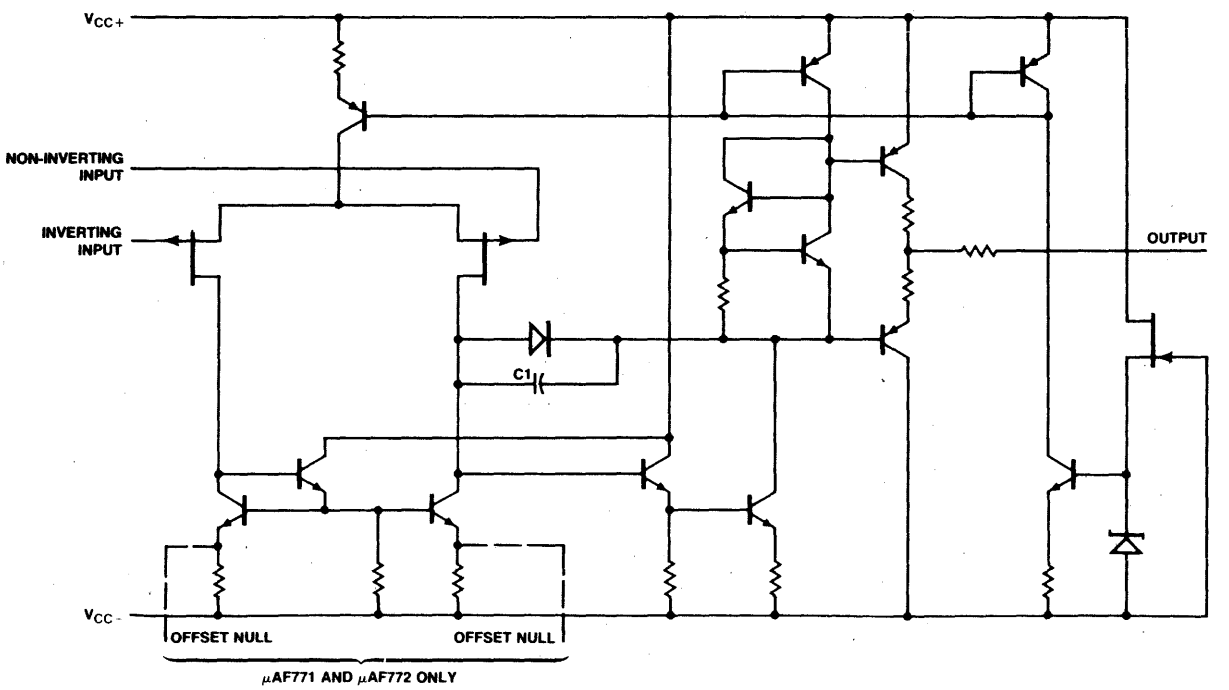
GENERAL DESCRIPTION – These monolithic BIFET input operational amplifiers incorporate well matched ion implanted BIFETS on the same chip with standard bipolar transistors. The key features of these op amps are low input bias currents in the sub nanoamp range plus high slew rate (13 V/μs typically) and wide bandwidth (3.0 MHz typically).

- **LOW INPUT BIAS CURRENT – 200 pA FOR μAF774C**
- **LOW INPUT OFFSET CURRENT – 100 pA FOR μAF774C**
- **HIGH SLEW RATE – 13 V/μs TYPICALLY**
- **WIDE BANDWIDTH – 3.0 MHz TYPICALLY**

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±18 V
Internal Power Dissipation (Note 1)	
DIP Package (9A) (6A)	670 mW
Molded Mini DIP Package (9T)	310 mW
Hermetic Package (5S)	500 mW
Differential Input Voltage	±30
Input Voltage Range (Note 2)	±16
Output Short Circuit Duration	continuous
Storage Temperature Range	
(5S) (6A)	−65°C to +150°C
(9A) (9T)	−55°C to +125°C
Operating Temperature Range	
μAF77 • A, μAF77 •	−55°C to +125°C
μAF77 • A, μAF77 •, μAF77 • C, μAF77 • L,	0°C to +70°C
Pin Temperature	
Molded Package (9T, 9A) Soldering 10 s	260°C
Hermetic Package (5S, 6A) Soldering 60 s	300°C

SCHEMATIC DIAGRAM (Each Amplifier)



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DC ELECTRICAL CHARACTERISTICS

SYMBOL	CHARACTERISTICS	CONDITIONS	μAF771A/2A/4A			μAF771/2/4			μAF771C/2C/4C			μAF771L/2L/4L			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
The Following Specifications Apply for $V_S = \pm 15$ V, $T_A = 25°C$															
V_{OS}	Input Offset Voltage	$R_S = 10$ kΩ			2.0			5.0			10			15	mV
A_{VOL}	Large Signal Voltage Gain	$V_O = \pm 10$ V, $R_L = 2$ kΩ	50	100		50	100		50	100		50	100		V/mV
The Following Specifications Apply for $V_S = \pm 15$ V, $0°C \leq T_A \leq 70°C$															
V_{OS}	Input Offset Voltage	$R_S = 10$ kΩ			4.0			7.0			13			−20	mV
$\Delta V_{OS}/\Delta T$	Average TC of Input Offset Voltage	$R_S = 10$ kΩ		10			10			10			10		μV/°C
I_{OS}	Input Offset Current	$T_j = 25°C$, (Notes 3, 4)			50			100			100			100	pA
		$T_j < 70°C$			2.0			4.0			4.0			4.0	nA
I_B	Input Bias Current	$T_j = 25°C$, (Notes 3, 4)		50	100		50	100		50	200		50	200	pA
		$T_j \leq 70°C$			4.0			4.0			8.0			8.0	nA
R_{IN}	Input Resistance	$T_j = 25°C$		10^{12}			10^{12}			10^{12}			10^{12}		Ω
A_{VOL}	Large Signal Voltage Gain	$V_O = \pm 10$ V, $R_L = 2$ kΩ	25			25			25			25			V/mV
V_O	Output Voltage Swing	$R_L = 10$ kΩ	±12	±13.5		±12	±13.5		±12	±13.5		±12	±13.5		V
V_{CM}	Input Common Mode Voltage Range		±11	15 −12		±11	15 −12		±11	15 −12		±11	15 −12		V
CMMR	Common Mode Rejection Ratio	$R_S \leq 10$ kΩ	80			80			70			70			dB
PSRR	Supply Voltage Rejection Ratio	(Note 5)	80			80			70			70			dB
I_S	Supply Current	μAF771		1.8	2.8		1.8	2.8		1.8	2.8		1.8	2.8	mA
		μAF772		3.2	5.0		3.2	5.0		3.2	5.0		3.2	5.0	
		μAF774		6.1	9.5		6.1	9.5		6.1	9.5		6.1	9.5	
The Following Specifications Apply for $-55°C \leq T_A \leq +125°C$															
V_{OS}	Input Offset Voltage	$R_S = 10$ kΩ			5.0			8.0							mV
$\Delta V_{OS}/\Delta T$	Average TC of Input Offset Voltage			25			25								μV/°C
A_{VOL}	Large Signal Voltage Gain	$V_S = \pm 15$ V, $T_A = 25°C$ $V_O = \pm 10$ V, $R_L = 2$ kΩ	25			25									V/mV
I_B	Input Bias Current	$T_j = 125°C$ (Note 4)			50			50							nA

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AC ELECTRICAL CHARACTERISTICS (Note 3)

SYMBOL	CHARACTERISTICS	CONDITIONS	μAF771A/2A/4A			μAF771/2/4			μAF771C/2C/4C			μAF771L/2L/4L			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew Rate	V_S = ±15 V, T_A = 25°C		13			13			13			13		V/μs
GBW	Gain Bandwidth Product	V_S = ±15 V, T_A = 25°C		3.0			3.0			3.0			3.0		MHz
e_n	Equivalent Input Noise Voltage	T_A = 25°C R_S = 100 Ω, f = 1000 Hz		16			16			16			16		nV/√Hz
i_n	Equivalent Input Noise Current	T_j = 25°C, f = 1000 Hz		0.01			0.01			0.01			0.01		pA/√Hz

NOTES:

1. Rating applies to ambient temperatures up to 70°C above T_A = 70°C. Derate linearly 6.3 mW/°C for the metal can, 5.6 mW/°C for the mini DIP and 8.3 mW/°C for the DIP.
2. Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage.
3. These specifications apply for V_S = ±15 V and 0°C ≤ T_A ≤ +70°C. V_{OS}, I_B and I_{OS} are measured at V_{CM} = 0.
4. The input bias currents are junction leakage currents which approximately double for every 10°C inrease in the junction temperature, T_j. Due to limited production test time, the input bias currents measured are correlated to junction temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, P_D. $T_j = T_A = \Theta_{jA} P_D$ where Θ_{jA} is the thermal resistance from junction to ambient. Use of a heat sink is recommended if input bias current is to be kept to a minimum.
5. Supply voltage rejection ratio is measured for both supply magnitudes increasing or decreasing simultaneously in accordance with common practice.

CHARACTERISTICS MEASUREMENT INFORMATION

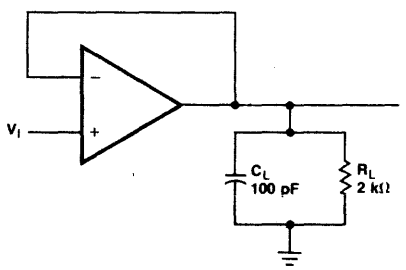


Fig. 1. UNITY GAIN AMPLIFIER.

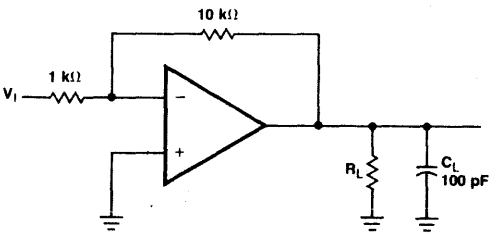


Fig. 2. GAIN-OF-10 INVERTING AMPLIFIER.

INPUT OFFSET VOLTAGE NULL CIRCUITS

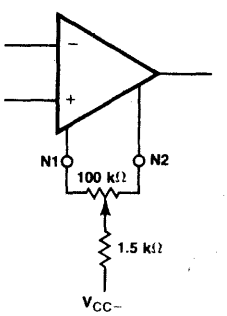


Fig. 3.
(μAF771 Only)

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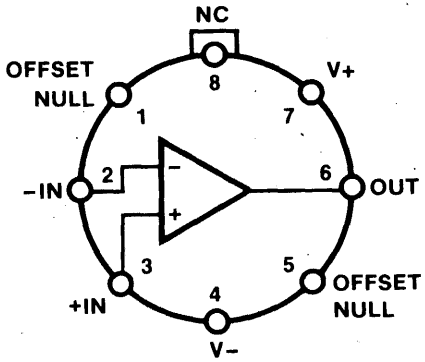
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CONNECTION DIAGRAMS AND ORDERING INFORMATION

μAF771

8-PIN METAL CAN
(TOP VIEW)

PACKAGE OUTLINE 5B



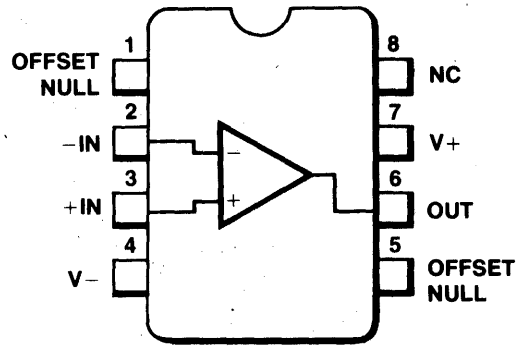
Note: Pin 4 connected to case.

ORDER INFORMATION

TYPE	PART NO.
μAF771A	μAF771AHM
μAF771	μAF771BHM
μAF771A	μAF771AHC
μAF771	μAF771BHC
μAF771C	μAF771HC
μAF771L	μAF771LHC

8-PIN MINI DIP
(TOP VIEW)

PACKAGE OUTLINES 9T
PACKAGE CODES T



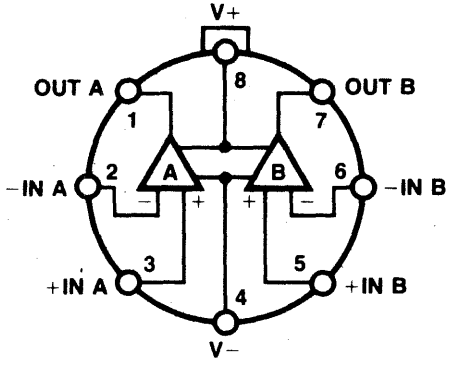
ORDER INFORMATION

TYPE	PART NO.	TYPE	PART NO.
μAF771A	μAF771ATC	μAF771L	μAF771LTC
μAF771	μAF771BTC	μAF771	μAF771BRC
μAF771C	μAF771TC	μAF771C	μAF771RC
		μAF771L	μAF771LRC

μAF772

8-PIN METAL CAN
(TOP VIEW)

PACKAGE OUTLINE 5S
PACKAGE CODE H

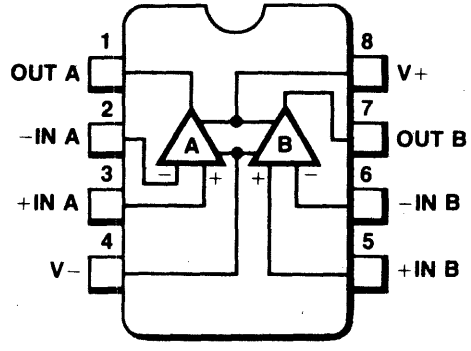


ORDER INFORMATION

TYPE	PART NO.
μAF772A	μAF772AHM
μAF772	μAF772BHM
μAF772A	μAF772AHC
μAF772	μAF772BHC
μAF772C	μAF772HC
μAF772L	μAF772LHC

8-PIN MINI DIP
(TOP VIEW)

PACKAGE OUTLINE 9T
PACKAGE CODE T

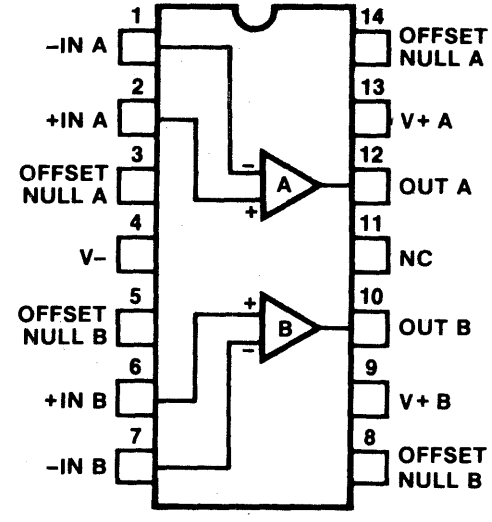


ORDER INFORMATION

TYPE	PART NO.
μAF772A	μAF772ATC
μAF772	μAF772BTC
μAF772C	μAF772TC
μAF772L	μAF772LTC

14-PIN DIP
(TOP VIEW)

PACKAGE OUTLINE 6A 9A
PACKAGE CODE D P



ORDER INFORMATION

TYPE	PART NO.
μAF772A	μAF772ADM
μAF772	μAF772BDM
μAF772A	μAF772ADC
μAF772A	μAF772APC
μAF772	μAF772BDC
μAF772	μAF772BPC
μAF772C	μAF772DC
μAF772C	μAF772PC
μAF772L	μAF772LDC
μAF772L	μAF772LPC

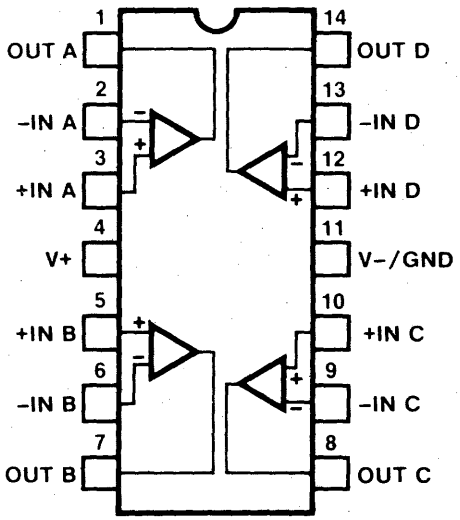
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CONNECTION DIAGRAMS AND ORDERING INFORMATION (Cont'd.)

μAF774

14-PIN DIP
(TOP VIEW)

PACKAGE OUTLINE	6A	9A
PACKAGE CODE	D	P



ORDER INFORMATION

TYPE	PART NO.
μAF774A	μAF774ADM
μAF774	μAF774BDM
μAF774A	μAF774ADC
μAF774A	μAF774APC
μAF774	μAF774BDC
μAF774	μAF774BPC
μAF774C	μAF774DC
μAF774C	μAF774PC
μAF774L	μAF774LDC
μAF774L	μAF774LPC

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μA9708

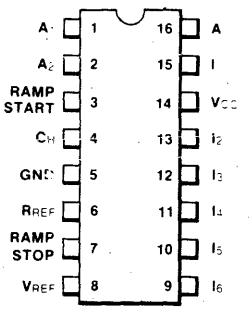
6-CHANNEL, 8-BIT, MICROPROCESSOR COMPATIBLE
ANALOG-TO-DIGITAL CONVERTER SUBSYSTEM*

GENERAL DESCRIPTION — The μA9708 is a single slope 8-bit, 6-channel ADC subsystem that provides all of the necessary analog functions for a microprocessor-based data control system. The device uses a microprocessor system like the F3870 or F6800 to provide the necessary addressing, timing and counting functions and includes a 1 of 8 decoder, 8-channel analog multiplexer, sample and hold, ramp integrator, precision ramp reference, and a comparator on a single monolithic chip.

- **MPU COMPATIBLE**
- **EXCELLENT LINEARITY OVER FULL TEMP RANGE - ±0.2% MAX**
- **TYPICAL 300 μs CONVERSION TIME PER CHANNEL**
- **WIDE DYNAMIC RANGE INCLUDES GROUND**
- **AUTO-ZERO AND FULL-SCALE CORRECTION CAPABILITY**
- **RATIOMETRIC CONVERSION — NO PRECISION REFERENCE REQUIRED**
- **SINGLE-SUPPLY OPERATION**
- **TTL COMPATIBLE**
- **DOES NOT REQUIRE ACCESS TO DATA BUS OR ADDRESS BUS**

CONNECTION DIAGRAM
16-PIN DUAL IN-LINE

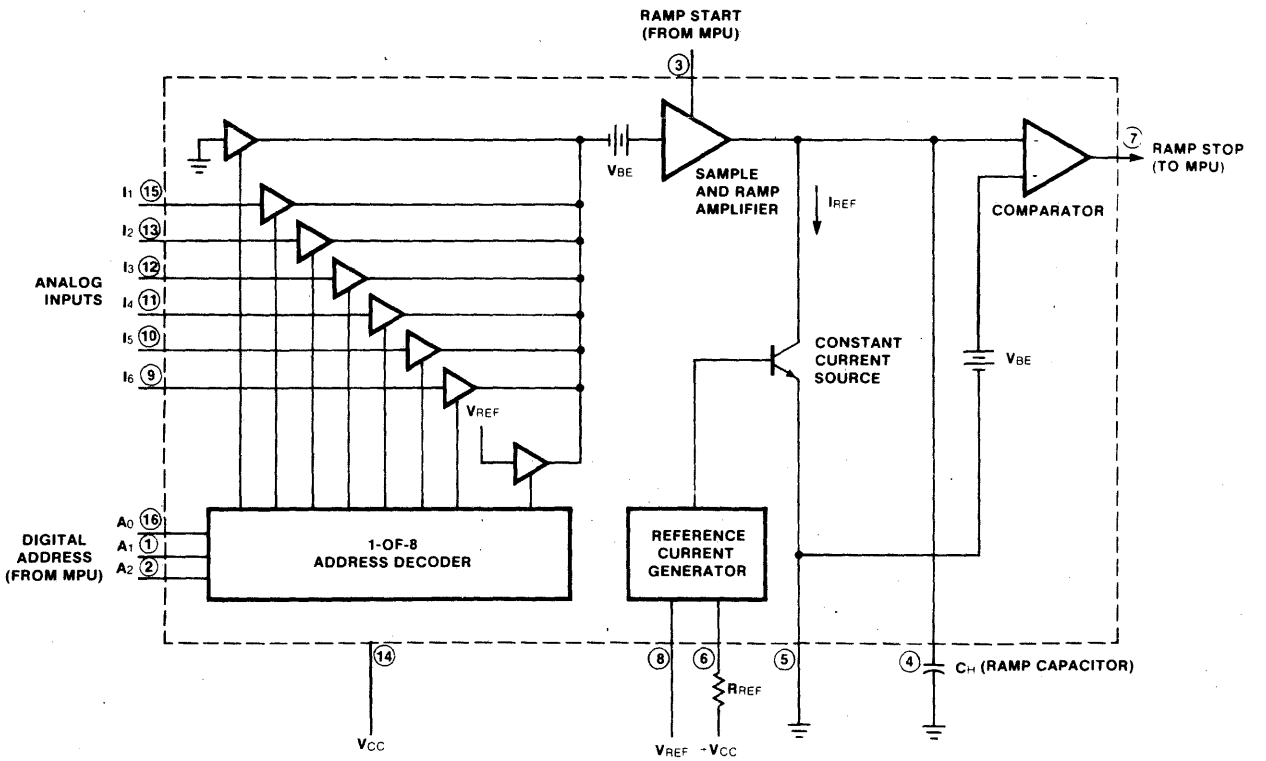
(TOP VIEW)
PACKAGE OUTLINES 7B 9B
PACKAGE CODES D P



ORDER INFORMATION

TYPE	PART NO.
μA9708	μA9708DM
μA9708	μA9708DC
μA9708	μA9708PC

BLOCK DIAGRAM



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ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V_{CC})	18 V
Comparator Output (Ramp Stop)	-0.3 V to +18 V
Analog Input Range	-0.3 V to 30 V
Digital Input Range	-0.3 V to 30 V
Output Sink Current	10 mA
Operating Temperature Range	
μA9708PC, μA9708DC	0°C to 70°C
μA9708DM	-55°C to 125°C
Storage Temperature Range	-65°C to +150°C
Continuous Total Dissipation	
Ceramic DIP Package	900 mW
Plastic DIP Package	1000 mW
Pin Temperature, Ceramic DIP (Soldering, 60 s)	300°C
Plastic DIP (Soldering, 10 s)	260°C

RECOMMENDED OPERATING CONDITIONS

CHARACTERISTICS	MIN	TYP	MAX	UNITS
Supply Voltage (V_{CC})	4.75	5.0	15	V
Reference Voltage (V_{REF})*	2.8		5.25	V
Ramp Capacitor (C_H)	300			pF
Reference Current (I_R)	12		50	μA
Analog Input Range	0		V_{REF}	V
Ramp Stop Output Current			1.6	mA

*2 V ≤ V_{REF} ≤ (V_{CC} -2 V)

CHANNEL SELECTION

INPUT ADDRESS LINE			SELECTED ANALOG INPUT
A_2	A_1	A_0	
0	0	0	Ground
0	0	1	I_1
0	1	0	I_2
0	1	1	I_3
1	0	0	I_4
1	0	1	I_5
1	1	0	I_6
1	1	1	V_{REF}

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ELECTRICAL CHARACTERISTICS: Over recommended operating conditions, -55°C ≤ T_A ≤ +125°C, for μA9708DM and 0°C ≤ T_A ≤ +70°C for μA9708DC or μA9708PC; unless otherwise specified.

CHARACTERISTICS	SYMBOL	CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
Conversion Accuracy	E_A	Over entire temperature range (Note 1)		±0.2	±0.3	%
Linearity	E_R	Applies to any one channel (Note 2)		±0.08	±0.2	%
Multiplexer Input Offset Voltage	V_{OSM}	Channel ON		2.0	4.0	mV
Conversion Time Per Channel	t_C	Analog Input = 0v to V_{REF} C_H = 300 pF, I_{REF} = 50 μA		296	350	μs
Acquisition Time	t_A	C_H = 1000 pF		20	40	μs
Acquistion Current	I_A		150			μA
Ramp Start Delay Time	t_O			100		ns
Multiplexer Address Time	t_M			1.0		μs
Digital Input HIGH Voltage	V_{IH}	A_0, A_1, A_2, ramp start	2.0			V
Digital Input LOW Voltage	V_{IL}	A_0, A_1, A_2, ramp start			0.8	V
Analog Input Current	I_B	Channel ON or OFF	-3.0	-1.0		μA
Input LOW Current	I_{IL}	A_0, A_1, A_2, ramp start = 0.4 V	-15	-5		μA
Input HIGH Current	I_{IH}	A_0, A_1, A_2, ramp start = 5.5 V			1.0	μA
Input Offset Current	I_{OS}			1.0	3.0	μA
Comparator Logic "1" Output Leakage Current	I_{OH}	V_{OH} = 15 V			10	μA
Comparator Logic "0" Output Voltage	V_{OL}	I_{OL} = 1.6 mA			0.4	V
Power Supply Rejection Ratio	PSRR	(Note 3)	40			dB
Crosstalk Between Any Two Channels		(Note 4)	60			dB
Power Supply Current	I_{CC}	V_{CC} = 5 V to 15 V, I_0 = 0		7.5	15	mA
Input Capacitance	C_{IN}			3.0		pF
Comparator Output Capacitance	C_{OUT}			5.0		pF

NOTES:
1. Conversion accuracy is defined as the deviations from a straight line drawn between the points defined by channel address 000 (0 scale) and channel address 111 (full scale) for all channels.
2. Linearity is defined as the deviation from a straight line drawn between the 0 and full scale points for each channel.
3. Power supply rejection ratio is defined as the conversion error contributed by power supply voltage variations while resolving mid scale on any channel.
4. Crosstalk between channels = 20 log $\frac{\Delta V_{CH}}{\Delta V_i}$

FUNCTIONAL DESCRIPTION

This Analog to Digital Converter is a single-slope 8-bit, 6-channel A/D converter that provides all of the necessary analog functions for a microprocessor-based data/control system. The device uses the processor system to provide the necessary addressing, timing and counting functions and includes a 1 of 8 decoder, 8-channel analog multiplexer, sample and hold, precision current reference, ramp integrator and comparator on a single monolithic chip.

For applications that require auto-zero or auto-calibration, *(See Figures 2-5)* line select address 0, 0, 0 and 1, 1, 1 may be used in conjunction with the arithmetic capability of the microprocessor to provide ground and scaling factors. Address 0, 0, 0 internally connects the input of the ramp generator to ground and may be used for zero offset correction in subsequent conversions. Address 1, 1, 1 internally connects the input of the ramp generator, to the voltage reference, V_{REF}, and may be used for scale factor correction in subsequent conversions. For the following, refer to the Functional Block Diagram.

Six separate external analog voltage inputs may come into terminals I_1-I_6 and the specific analog input to be converted is selected via address terminals A_0-A_2. The analog input voltage level is transferred to the external ramp capacitor connected to pin 4 when the input to the ramp start terminal (pin 3) is at a logic 0 *(See Figure 1)*. The time to charge the capacitor is the acquisition time

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which is a function of the output impedance of an amplifier internal to the A/D and the value of the capacitor. After charging the external capacitor the ramp start terminal is switched to a logic 1 which introduces a high impedance between the analog input voltage and the external capacitor.

The capacitor begins to discharge at a controlled rate. The controlled rate of discharge (ramp) is established by the external reference voltage, the external reference resistor, the value of the external capacitor and the internal leakage of the A/D. Connected to the capacitor terminal is a comparator internal to the A/D with its output going to the ramp stop terminal (pin 7). The comparator output is a logical one when the capacitor is charged and switches to a logic 0 when the capacitor is in a discharged state. The ramp time is the time from when ramp start goes high (logic "1") to when ramp stop goes low (logic "0"). The microprocessor must be programmed to determine this conversion time. The ideal (no undesirable internal source impedances, leakage paths, errors on levels where comparator switches or delay time) conversion time is calculated as follows.

$$\text{Ramp Time} = V_1 \frac{C_H}{I_R}$$

Where V_1 = Analog Input Voltage being measured

C_H = External Ramp Capacitor

$$I_R = \frac{V_{CC} - V_{REF}}{R_{REF}}$$

Where V_{CC} = Power Supply Voltage

V_{REF} = Reference Voltage

R_{REF} = Reference Resistor

In actual use the errors due to a nonideal A/D can be minimized by using a microprocessor to make the calculations. *(See Figures 2 through 5)*

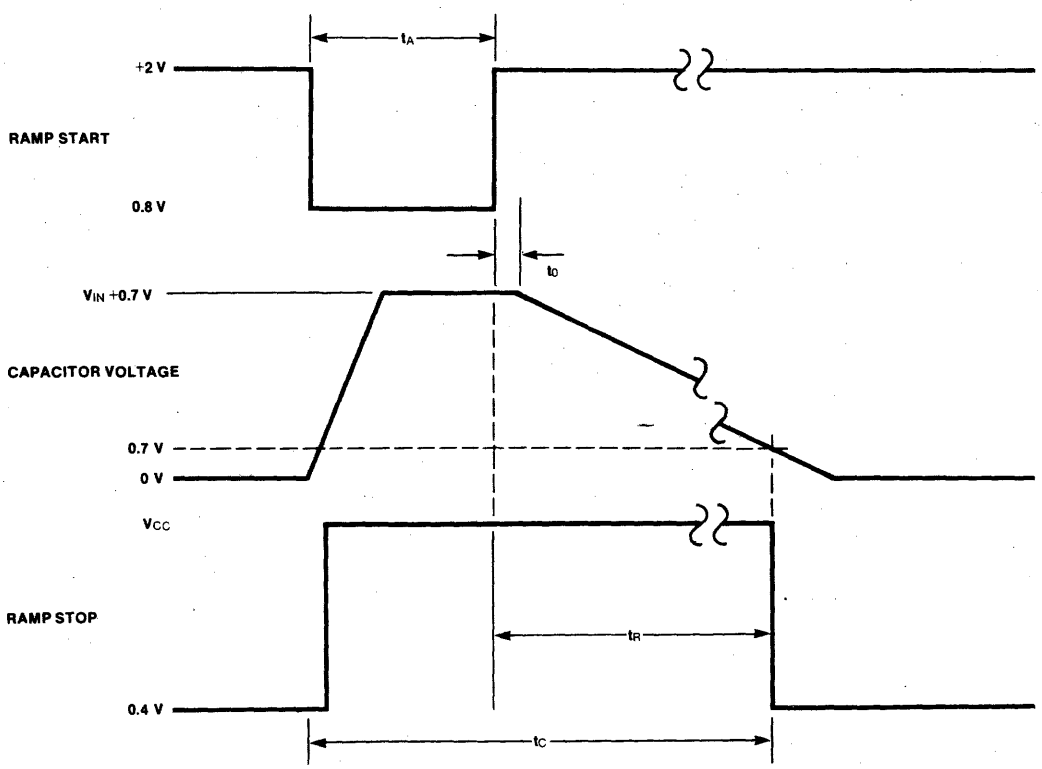


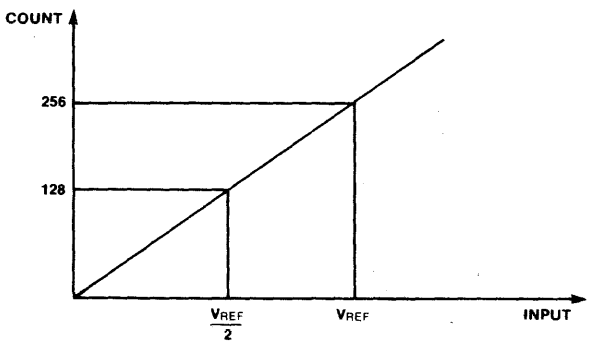
Fig. 1 Equivalent Timing Waveform for Test Circuits and Applications

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APPLICATION HINTS AND FORMULAS

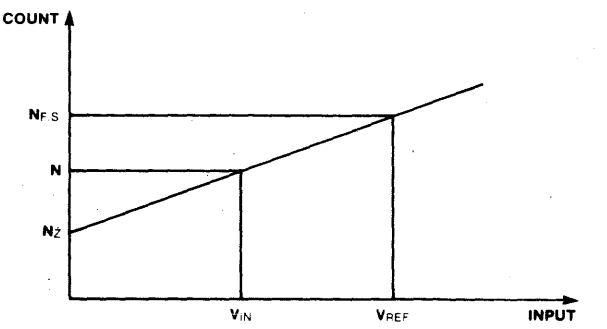
1. The capacitor node impedance is approximately 30 μΩ and should have no parallel resistance for proper operation.
2. t_R when V_{IN} = 0 V will be finite (i.e., the comparator will always toggle for $V_{IN} \geq 0$ V.)
3. The ramp stop output is open collector, and an external pull up resistor is required.
4. All digital inputs and outputs are TTL compatible.
5. For proper operation timing commences on the 0 to 1 transition of ramp start and terminates on the 1 to 0 transition of ramp stop.
6. $t_A \geq \frac{C_H}{150\ \mu A - I_R} \times V_{REF}$
7. t_R (ramp time) $= \frac{C_H}{I_R} \times V_{IN}$, $t_R\big|_{max} = \frac{C_H}{I_R} \times V_{REF}$
8. $I_R = \frac{V_{CC} - V_{REF}}{R_{REF}}$
9. $2\ V \leq V_{REF} \leq (V_{CC} - 2\ V)$
10. Address lines A_0, A_1, A_2 must be stable throughout the sampling interval, t_A.
11. Pin 6 (R_{REF}) should be bypassed to ground via a 0.02 μF capacitor.

AUTO-ZERO AND FULL-SCALE FEATURES



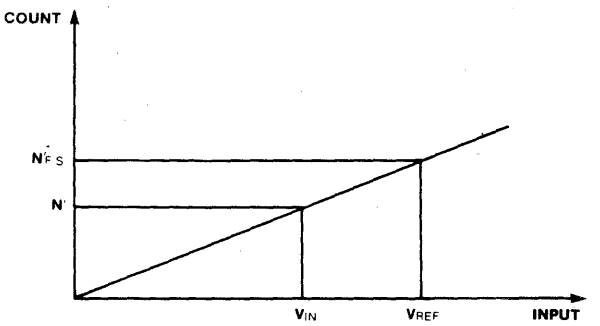
- NO ZERO OFFSET
- NO FULL-SCALE ERROR
- COUNT (N) = $\frac{V_{IN}}{V_{REF}}$ = 256

Fig. 2 Ideal Transfer Function



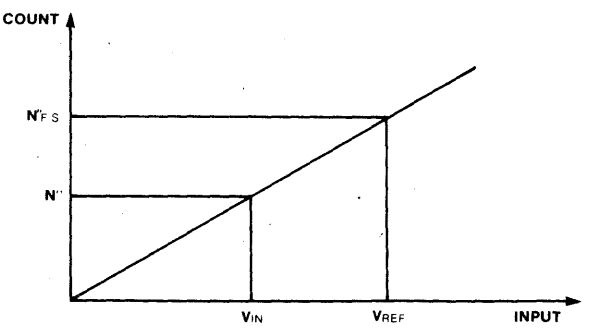
- $N_{FS} \neq 256$
- $N_Z \neq 0$
- (N) HAS BOTH FULL-SCALE AND ZERO ERRORS.

Fig. 3 Transfer Function with Zero and Full-Scale Error



- $N' = N - N_Z$
- N' HAS FULL-SCALE ERROR

Fig. 4 Zero-Correction Added

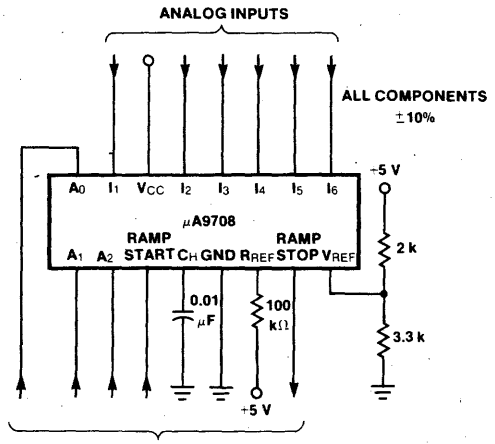


- $N'' = (N - N_Z) \times \frac{256}{(N_{FS} - N_Z)}$

Fig. 5 Both Zero and Full-Scale Correction Added

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TEST CIRCUITS



INPUT TIMING:

$t_A > 400\ \mu s$

$$V_{REF} = \left(\frac{3.3\ k\Omega}{2\ k\Omega + 3.3\ k\Omega}\right) 5\ V = 3.1\ V$$

$$I_R = \frac{5 - 3.1}{100\ k\Omega} = 19\ \mu A$$

$$t_R\Big|_{max} = \text{full scale ramp time} = \frac{0.01 \times 10^{-6}}{19 \times 10^{-6}} \times 3.1 = 1.6\ ms$$

NOTE:
For evaluation purposes, the ramp start timing generation can be implemented with a μA555 timer (astable operation) or MPU evaluation kit, and a time internal meter for ramp time measurement. The TIM meter will measure the time between the 0 to 1 transition of the ramp start and the 1 to 0 transition of the ramp stop. The ramp stop is open collector, and must have an external pull up resistor to V_{CC}.

Fig. 6 Slow Speed Evaluation Circuit for Ratiometric Operation

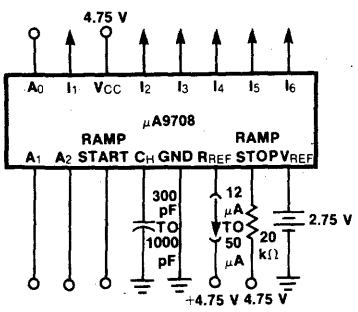


Fig. 7 Linearity/Acquisition Time/Conversion Time Test Circuit

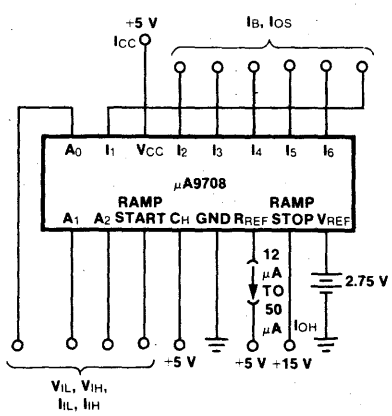
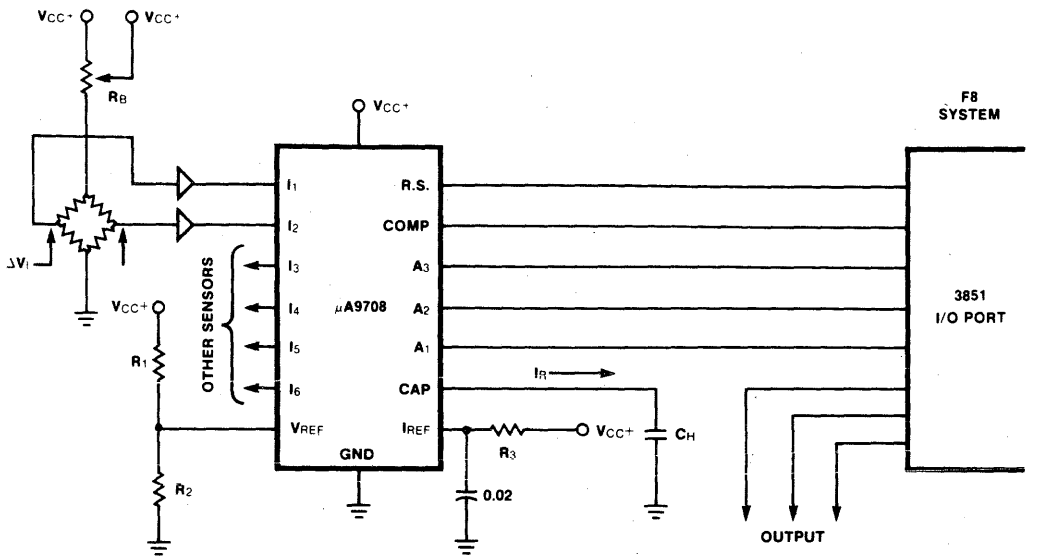


Fig. 8 Static Measurements

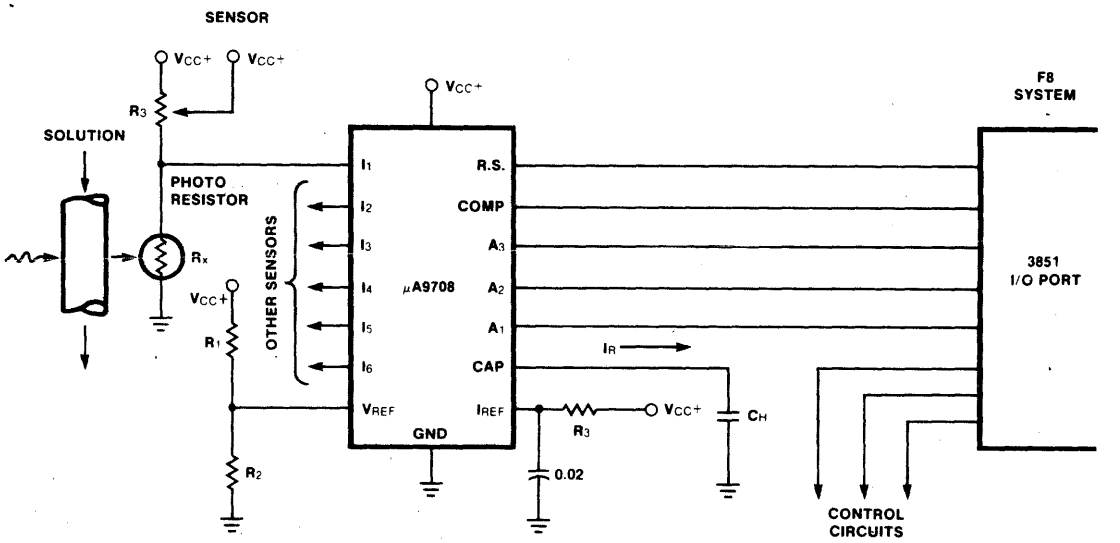
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TYPICAL APPLICATIONS



ΔV_I = (Applied Force) and can be Linearized (if necessary) in F8 Software.

Ratiometric Strain Gage Sensor/Controller



APPLICATIONS:

- **BEVERAGE BREWERS/DISPENSERS**
- **CHEMICAL SOLUTION CONTROL**
- **AUTOMATIC LIQUID MIXING CONTROL**

$$\text{RAMP CURRENT} = I_R = V_{CC}\left(\frac{R_1}{R_1 + R_2}\right)\left(\frac{1}{R_3}\right)$$

$$V_I = \left(\frac{R_X}{R_X + R_B}\right) V_{CC+}$$

$$\text{RAMP TIME} = V_I \frac{C_H}{I_R} = \left(\frac{R_X}{R_X + R_B}\right)\left(1 + \frac{R_2}{R_1}\right)\left(C_H R_3\right)$$

Opaque Solution Controller

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SYSTEM HINTS:

Several alternatives exist from a hardware/software standpoint in microprocessor based systems using the μA9708.

1. The ramp time measurement may be implemented in software using a register increment, followed by a branch back depending on the status of the ramp stop.

2. Alternately, the ramp stop may be tied into the interrupt structure in systems containing a programmable binary timer. This scheme has the following advantages:

   A. The CPU is not committed during the ramp time interval.
   B. It requires only 4 bits of an I/O port for control signals.

3. The auto-zero/auto-full-scale (see *Figures 2-5*) should use double precision, rounded (as opposed to truncated) arithmatics. Several points are worth noting:

   A. The subtractions are single op code instructions.
   B. The full scale correction uses a multiply by 256 and can be accomplished by a shift left 8 bits (usually one instruction) or placing (N-Nz) in the MSB register and setting the LSB register to zero, for the double precision divide.
   C. The divisor ($N_{F.S.}$ - Nz) MSB's register will always be zero.

These schemes have the following advantages:

A. No access to the data buss or address buss is required, by the A/D system.
B. 4 I/O bits completely support the A/D system.
C. Since auto full scale/auto zero are implemented in software and long term drift (aging) effects are eliminated.
D. Software overhead is minimal (typically 30 bytes).
E. Where ratiometric operation is permissible, the 4 external components may be ±5% tolerance, including the power supply.

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μA78H00/μA78HG SERIES

5 AMP VOLTAGE REGULATOR

FAIRCHILD LINEAR INTEGRATED CIRCUITS

GENERAL DESCRIPTION

Fixed Output – The μA78H00 series hybrids are regulators with fixed output voltages and 5 A output current capability with all the inherent characteristics of the monolithic 3-terminal regulators, i.e., full thermal overload, short-circuit and safe-area protection. The μA78H00 is packaged in a hermetically sealed TO-3 providing 50 W power dissipation. The regulator consists of a monolithic chip driving a discrete series-pass element and two short-circuit detection transistors. A beryllium-oxide substrate is used in conjunction with an isothermal layout to optimize the thermal characteristics of the device and still maintain electrical isolation between the various chips. This unique circuit design limits the maximum junction temperature of the power output transistor to provide full automatic thermal overload protection. If the safe operating area is ever exceeded, the device simply shuts down, rather than failing or damaging other system components. This feature eliminates the need to design costly output circuitry and overly conservative heat sinking arrangements typical of high-current regulators built from discrete components.

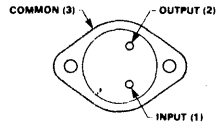
Adjustable Regulators – The μA78HG is an adjustable 4-terminal positive voltage regulator capable of supplying in excess of 5 A over a 5.0 V to 24 V output range. The same features and construction details of the μA78H00 series have been incorporated into the μA78HG. Only two (2) external resistors are required to set the output voltage. Input and output capacitors should be used to improve input filtering and transient response.

- **5 A OUTPUT CURRENT**
- **INTERNAL CURRENT AND THERMAL LIMITING**
- **INTERNAL SHORT-CIRCUIT CURRENT LIMIT**
- **LOW DROP-OUT VOLTAGE**
- **50 W POWER DISSIPATION**

ABSOLUTE MAXIMUM RATINGS

Input Voltage	
μA78H05, 12, 15	25 V
μA78HG	40 V
Internal Power Dissipation	50 W @ 25°C Case
Maximum Input-to-Output Voltage Differential	25 V
Operating Junction Temperature Range	
μA78H00C (fixed voltage series)	0°C to 150°C
μA78HGC (adjustable voltage series)	0°C to 150°C
Military Temperature Range (consult factory)	−55°C to 150°C
Storage Temperature Range	−55°C to 150°C
Lead Temperature (Soldering, 60 s)	300°C

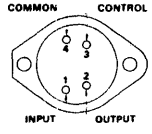
CONNECTION DIAGRAMS
TO-3 PACKAGE
(TOP VIEW)
PACKAGE OUTLINE GJ
PACKAGE CODE K



ORDER INFORMATION

OUTPUT VOLTAGE	TYPE	PART NO.
5.0 V	78H05C	μA78H05KC
12 V	78H12C	μA78H12KC
15 V	78H15C	μA78H15KC

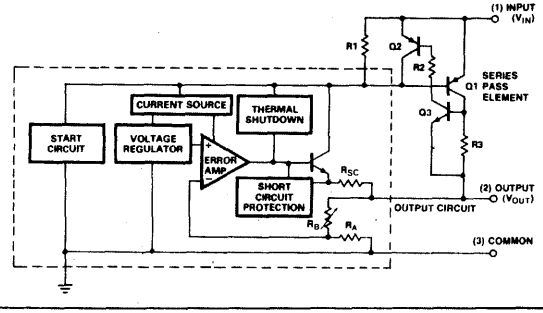
TO-3 PACKAGE
(TOP VIEW)
PACKAGE OUTLINE GK
PACKAGE CODE K



ORDER INFORMATION

OUTPUT VOLTAGE	TYPE	PART NO.
5–24 V Adjustable	78HGC	μA78HGKC

BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS: T_J = 25°C, I_{OUT} = 2.0 A unless otherwise specified.

SYMBOL	CHARACTERISTICS	CONDITIONS	μA78H12 MIN	μA78H12 TYP	μA78H12 MAX	UNITS
V_{OUT}	Output Voltage	I_{OUT} = 2.0 A, V_{IN} = 19 V	11.5	12	12.5	V
ΔV_{OUT}	Line Regulation (Note 1)	V_{IN} = 16 to 25 V		20	120	mV
ΔV_{OUT}	Load Regulation (Note 1)	10 mA ≤ I_{OUT} ≤ 5.0 A, V_{IN} = 19 V		20	120	mV
I_Q	Quiescent Current	I_{OUT} = 0, V_{IN} = 17 V			10	mA
RR	Ripple Rejection	I_{OUT} = 1.0 A, f = 210 Hz, 5.0 V_{p-p}	60			dB
V_n	Output Noise	10 Hz ≤ f ≤ 100 kHz, V_{IN} = 17 V		75		μV_{RMS}
	Dropout Voltage	I_O = 5.0 A		3.0		V
		I_O = 3.0 A		2.6		V
I_{OS}	Short Circuit Current Limit	V_{IN} = 19 V		7.0		A_{pk}

ELECTRICAL CHARACTERISTICS: T_J = 25°C, I_{OUT} = 2.0 A unless otherwise specified.

SYMBOL	CHARACTERISTICS	CONDITIONS	μA78H15 MIN	μA78H15 TYP	μA78H15 MAX	UNITS
V_{OUT}	Output Voltage	I_{OUT} = 2.0 A, V_{IN} = 20 V	14.4	15	15.6	V
ΔV_{OUT}	Line Regulation (Note 1)	V_{IN} = 19 to 25 V		30	150	mV
ΔV_{OUT}	Load Regulation (Note 1)	10 mA ≤ I_{OUT} ≤ 5.0 A, V_{IN} = 20 V		30	150	mV
I_Q	Quiescent Current	I_{OUT} = 0, V_{IN} = 20 V			10	mA
RR	Ripple Rejection	I_{OUT} = 1.0 A, f = 210 Hz, 5.0 V_{p-p}	60			dB
V_n	Output Noise	10 Hz ≤ f ≤ 100 kHz, V_{IN} = 20 V		75		μV_{RMS}
	Dropout Voltage	I_O = 5.0 A		3.0		V
		I_O = 3.0 A		2.6		V
I_{OS}	Short Circuit Current Limit	V_{IN} = 20 V		7.0		A_{pk}

ELECTRICAL CHARACTERISTICS: T_J = 25°C, I_{OUT} = 2.0 A unless otherwise specified.

SYMBOL	CHARACTERISTICS	CONDITIONS	μA78HG (Adjustable) MIN	μA78HG (Adjustable) TYP	μA78HG (Adjustable) MAX	UNITS (Note 2)
V_{OUT}	Output Voltage	I_{OUT} = 2.0 A, V_{IN} = V_{OUT} + 3.5 V	5.0	Note 3	24	V
ΔV_{OUT}	Line Regulation (Note 1)	V_{IN} = 8.5 to 25 V			1%	V_{OUT}
ΔV_{OUT}	Load Regulation (Note 1)	10 mA ≤ I_{OUT} ≤ 5.0 A, V_{IN} = 10 V			1%	V_{OUT}
I_Q	Quiescent Current	I_{OUT} = 0, V_{IN} = V_{OUT} + 5.0 V			10	mA
RR	Ripple Rejection	I_{OUT} = 1.0 A, f = 210 Hz, 5.0 V P-P	60			dB
V_n	Output Noise	10 Hz ≤ f ≤ 100 kHz, V_{IN} = V_{OUT} + 5.0V		50		μV_{RMS}
	Dropout Voltage	I_O = 5.0 A		3.0		V
		I_O = 3.0 A		2.6		V
I_{OS}	Short Circuit Current Limit	V_{IN} = 10 V		7.0		A_{pk}
V_C	Control Pin Voltage	V_{IN} = 10 V	4.8	5.0	5.2	V

ELECTRICAL CHARACTERISTICS: T_J = 25°C, I_{OUT} = 2.0 A unless otherwise specified.

SYMBOL	CHARACTERISTICS	CONDITIONS	μA78H05 MIN	μA78H05 TYP	μA78H05 MAX	UNITS
V_{OUT}	Output Voltage	I_{OUT} = 2.0 A, V_{IN} = 10 V	4.8	5.0	5.2	V
ΔV_{OUT}	Line Regulation	V_{IN} = 8.5 to 25 V		10	50	mV
ΔV_{OUT}	Load Regulation	10 mA ≤ I_{OUT} ≤ 5.0 A, V_{IN} = 10 V		10	50	mV
I_Q	Quiescent Current	I_{OUT} = 0, V_{IN} = 10 V			10	mA
RR	Ripple Rejection	I_{OUT} = 1.0 A, f = 210 Hz, 5.0 V_{P-P}	60			dB
V_n	Output Noise	10 Hz ≤ f ≤ 100 kHz, V_{IN} = 10 V		40		μV_{RMS}
	Dropout Voltage	I_O = 5.0 A		3.0		V
		I_O = 3.0 A		2.6		V
I_{OS}	Short Circuit Current Limit	V_{IN} = 10 V		7.0		A_{pk}

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μA79HG

5 AMP NEGATIVE ADJUSTABLE VOLTAGE REGULATOR

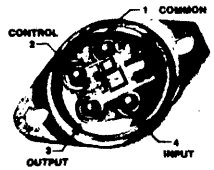
FAIRCHILD HYBRID PRODUCTS

GENERAL DESCRIPTION — The μA79HG is an adjustable 4-terminal negative voltage regulator capable of supplying in excess of -5 A over a -24 V to -2.2 V output range. The μA79HG hybrid voltage regulator has been designed with all the inherent characteristics of the monolithic 4-terminal regulator; i.e., full thermal overload and short-circuit protection. The μA79HG is packaged in a hermetically-sealed 4-pin TO-3 package providing 50 W power dissipation. The regulator consists of a monolithic chip driving a discrete-series pass element and short-circuit detection transistors.

- **-5 A OUTPUT CURRENT**
- **INTERNAL CURRENT AND THERMAL LIMITING**
- **INTERNAL SHORT-CIRCUIT CURRENT LIMIT**
- **LOW DROP-OUT VOLTAGE**
- **50 W POWER DISSIPATION**
- **ELECTRICALLY NEUTRAL CASE**

CONNECTION DIAGRAM

TO-3 PACKAGE
(TOP VIEW)
PACKAGE CODE K



ORDER INFORMATION

OUTPUT VOLTAGE	TEMP. RANGE	PART NO.
-24 to -2.11 V	0 to +150°C	μA79HGKC

ABSOLUTE MAXIMUM RATINGS

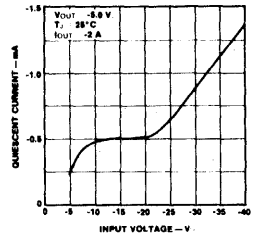
Input Voltage	-40 V
Internal Power Dissipation	50 W @ 25°C Case
Maximum Input-to-Output Voltage Differential	-20 V
Operating Junction Temperature Range	0°C to 150°C
Storage Temperature Range	-55°C to 150°C
Lead Temperature (Soldering, 60 s)	300°C

ELECTRICAL CHARACTERISTICS: T_J = 25°C, I_{OUT} = -2.0 A unless otherwise specified.

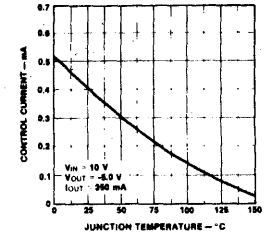
CHARACTERISTIC	CONDITION	MIN	TYP	MAX	UNITS
Input Voltage Range		-40		-7.0	V
Nominal Output Voltage Range	$V_{IN} = V_{OUT}$ - 5V	-24		-2.11	V
Output Voltage Tolerance	-40 V ≤ V_{IN} ≤ -7 V			4%	%(V_{OUT})
Line Regulation	-40 ≤ V_{IN} ≤ -7 V		0.4	1.0	%(V_{OUT})
Load Regulation	$V_{IN} = V_{OUT}$ -10 V, -10 mA ≤ I_{OUT} ≤ -5.0 A		0.7	1.0	%(V_{OUT})
Control Pin Current				3.0	μA
Quiescent Current	V_{IN} = -10 V			-5.0	mA
Ripple Rejection	-18 V ≤ V_{IN} ≤ -8.5 V V_{OUT} = -5 V, f = 120 Hz		50		dB
Output Noise Voltage	10 Hz ≤ f ≤ 100 kHz, V_{OUT} = -5.0 V		200		μV
Dropout Voltage	I_{OUT} = -5 A		-2.0		V
Peak Output Current	V_{IN} = -10 V		-8		A
Control Pin Voltage (Reference)	V_{IN} = -10 V	-2.35		-2.11	V

TYPICAL PERFORMANCE CURVES

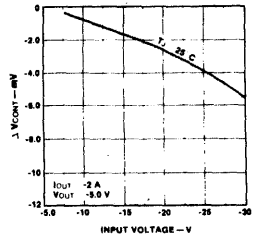
QUIESCENT CURRENT AS A FUNCTION OF INPUT VOLTAGE



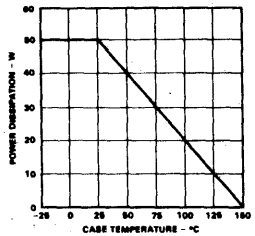
CONTROL CURRENT AS A FUNCTION OF TEMPERATURE



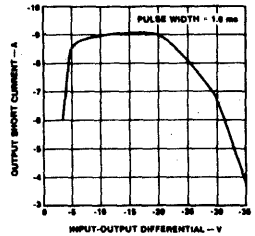
DIFFERENTIAL CONTROL VOLTAGE AS A FUNCTION OF INPUT VOLTAGE



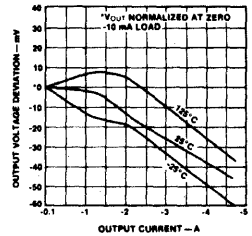
MAXIMUM POWER DISSIPATION



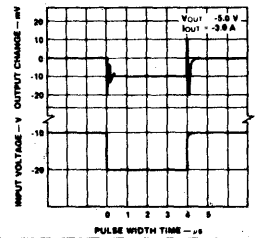
OUTPUT SHORT CURRENT AS A FUNCTION OF INPUT-OUTPUT DIFFERENTIAL VOLTAGE



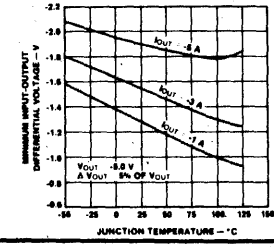
LOAD REGULATION AS A FUNCTION OF OUTPUT CURRENT



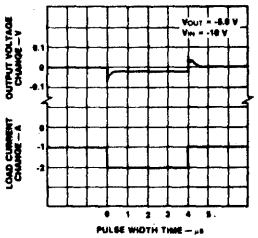
LINE TRANSIENT RESPONSE



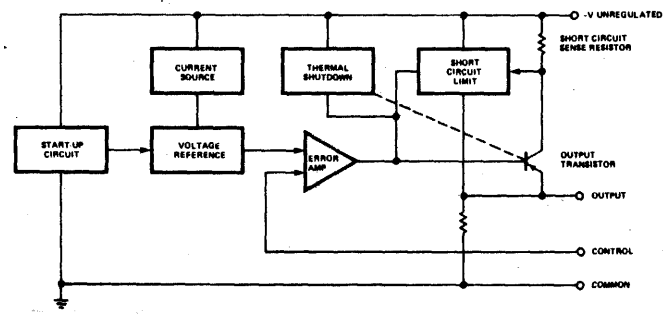
DROPOUT VOLTAGE AS A FUNCTION OF JUNCTION TEMPERATURE



LOAD TRANSIENT RESPONSE



FUNCTIONAL BLOCK DIAGRAM



SH1605

5 AMP, HIGH EFFICIENCY SWITCHING REGULATOR

FAIRCHILD HYBRID PRODUCTS

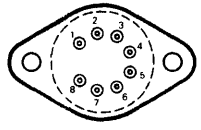
GENERAL DESCRIPTION — The SH1605 is a hybrid switching regulator with high output current capabilities. It incorporates a temperature-compensated voltage reference, a duty-cycle controllable oscillator, error amplifier, high current-high voltage output switch, and a power diode. The SH1605 can supply 5 A of regulated output current over a wide range of output voltage.

- **STEP DOWN SWITCHING REGULATOR**
- **OUTPUT ADJUSTABLE FROM 3.0 TO 30 V**
- **5 A OUTPUT CURRENT**
- **HIGH EFFICIENCY**
- **UP TO 150 W OUTPUT POWER**
- **STANDARD 8-PIN TO-3 PACKAGE**

ABSOLUTE MAXIMUM RATINGS

V_{IN} - $V_{OUT(Min)}$	5 V
Input Voltage	35 V Max
Output Current	6 A
Operating Temperature T_J	150°C
Internal Power Dissipation	20 W
Storage Temperature Range	-65°C to +150°C
Duty Cycle	20 ≤ D ≤ 80%
V_{7-8}	60 V
I_{7-8}	6 A

CONNECTION DIAGRAM
8-PIN TO-3 TYPE

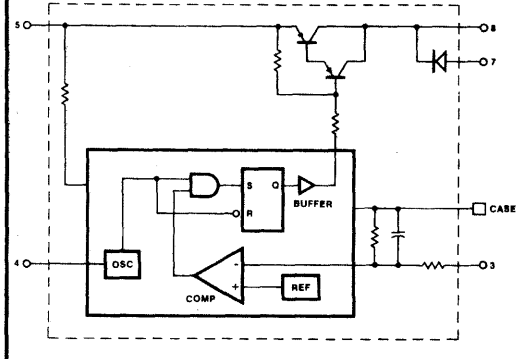


PIN	FUNCTION
1	NC
2	NC
3	Error Amplifier Input
4	Timing Capacitor
5	Input
6	NC
7	Steering Diode (Anode)
8	V_{OUT}
Case	Ground

ORDER INFORMATION

OUTPUT VOLTAGE	TEMPERATURE RANGE	PART NUMBER
3 V TO 30 V	0°C to +70°C Ambient	SH1605

BLOCK DIAGRAM



DESIGN EQUATIONS

Efficiency (η) = $\frac{P_{OUT} \times 100}{P_{IN}}$

Transistor DC Losses (P_T) = $I_{OUT} \times V_S \frac{t_{ON}}{t_{ON} + t_{OFF}}$

Diode DC Losses (P_D) = $I_{OUT} \times V_F \frac{t_{OFF}}{t_{ON} + t_{OFF}}$

Drive Circuit Losses (D_L) = $\frac{V_{IN}2}{300} \times \frac{t_{ON}}{t_{ON} + t_{OFF}}$

Switching Losses Transistor (P_S) = $V_{IN} \times I_{OUT} \frac{t_r + t_f}{2\,(t_{ON} + t_{OFF})}$

Transistor Duty Cycle = $\frac{t_{ON}}{t_{ON} + t_{OFF}} = \frac{V_{OUT}}{V_{IN}}$

Diode Duty Cycle = $\frac{t_{OFF}}{t_{ON} + t_{OFF}} = 1 - \frac{V_{OUT}}{V_{IN}}$

Power Inductor (P_L) = $I_{OUT}2 \times R_L$ (Winding Resistance)

Efficiency (η) = $\frac{V_{OUT}\ I_{OUT}}{V_{OUT}\ I_{OUT} + P_T + P_D + D_L + P_S + P_L} \times 100$

FAIRCHILD • SH1605

ELECTRICAL CHARACTERISTICS: T_C = 25°C, V_{IN} = 15 V unless otherwise specified.

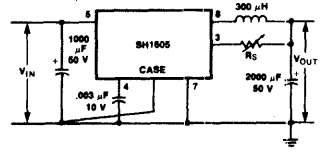
SYMBOL	CHARACTERISTICS	CONDITIONS	SH1605 MIN	SH1605 TYP	SH1605 MAX	UNITS
V_{OUT}	Output Voltage	$V_{IN} \geq V_O$ + 5 V, I_O = 2 A	3.0		30.0	V
V_S	Switch Saturation	I_{OUT} = 5.0 A, I_{OUT} = 2.0 A		1.5 1.0	2.0 1.2	V V
V_F	Diode On Voltage	I_{OUT} = 5.0 A, I_{OUT} = 2.0 A		2.2 1.6	2.8 2.0	V V
V_{CC}	Supply Voltage		10		35	V
I_{RD}	Diode Reverse Current	V_{RD} = 25 V		2.0		μA
I_Q	Quiescent Current	I_{OUT} = 0.2 A		30		mA
	Reference and Oscillator Section					
V_3	Voltage on Pin 3			2.5		V
$\Delta V_3/T$	V_3 Temperature Coefficient			150		ppm/°C
I_4	Charging Current-Pin 4			25		μA
V_4	Voltage Swing-Pin 4			0.5		V
$I_{\downarrow 4}$	Discharging Current - Pin 4			225		μA

SWITCHING CHARACTERISTICS

SYMBOL	CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNITS
t_r	Voltage Rise Time	I_{OUT} = 2.0 A I_{OUT} = 5.0 A		700 1.8		ns μs
t_f	Voltage Fall Time	I_{OUT} = 2.0 A I_{OUT} = 5.0 A		700 900		ns ns
t_s	Storage Time	I_{OUT} = 5.0 A		2.6		μs
t_d	Delay Time	I_{OUT} = 5.0 A		2.5		μs
	Thermal Characteristics					
P_D	Power Dissipation	I_{OUT} = 5.0 A V_{OUT} = 10 V		16		W
η	Efficiency	V_{OUT} = 10 V I_{OUT} = 5 A		75		%
θ_{J-C}	Thermal Resistance			4.5		°C/W

NOTES:
1. θ_{C-A} Typical is 30°C/W for natural convection cooling.
2. For heatsinking requirements see power derating curve.

TYPICAL APPLICATION



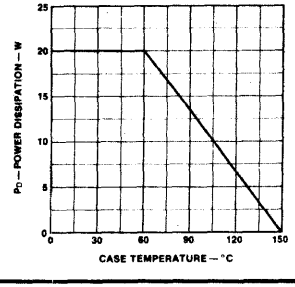
R_S = SET V_{OUT}

$R_S = \frac{2 \times 10^3\ (V_{OUT} - 2.5)}{2.5}$

V_{IN} = 12-18 V
V_{OUT} = 5 V
I_{OUT} = 5 A (Max)
I_{OUT} = 1 A (Min)
η = 70%

Load Reg. = 50 mV
Line Reg. = 50 mV
Ripple = 100 mV

POWER DERATING CURVE



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SH1705

5 VOLT, 5 AMP REGULATOR WITH BRIDGE

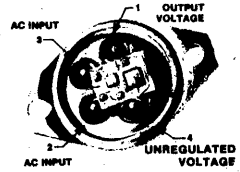
FAIRCHILD HYBRID PRODUCTS

GENERAL DESCRIPTION — The SH1705 is a 5 V, 5 A regulator with a 5 A diode bridge rectifier contained in the same TO-3 package. With the addition of a power transformer, a filter capacitor and a small bypass capacitor, the SH1705 forms a complete power supply. The regulator section is identical with the μA78H05A and may be used separately from the rectifier.

- **BUILT IN RECTIFIER BRIDGE**
- **5 A OUTPUT CURRENT**
- **INTERNAL CURRENT AND THERMAL LIMITING**
- **LOW DROPOUT VOLTAGE**
- **50 W POWER DISSIPATION**
- **HERMETICALLY SEALED**

CONNECTION DIAGRAM

TO-3 PACKAGE
(TOP VIEW)
PACKAGE CODE K



PIN	FUNCTION
1	Output Voltage
2	AC Input
3	AC Input
4	$V_{unregulated}$
Case	Ground

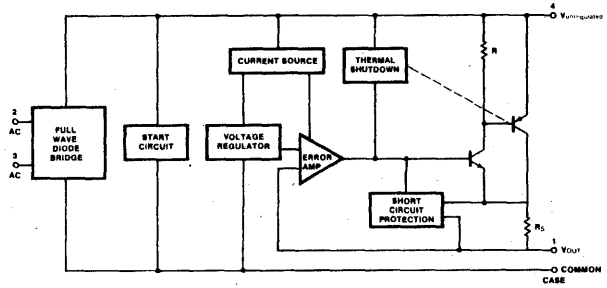
ORDER INFORMATION

Output Voltage	Temp. Range	Order Code
5 V	0°C to +150°C	SH1705

ABSOLUTE MAXIMUM RATINGS

Input Voltage	23 V_{RMS}
Internal Power Dissipation (25° C Case)	50 W
Regulator Section Input To Output Differential Voltage	25 V_{DC}
Input Current Peak-Cycle	20 A
Input Current Repetitive	14 A
Operating Junction Temp. Range	0 to 150° C
Storage Temperature Range	-65 to +150° C
Lead Solder Temperature (10 s)	300° C

BLOCK DIAGRAM

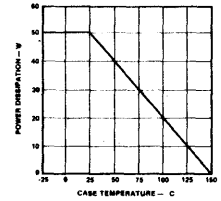


ELECTRICAL CHARACTERISTICS: Filt. Cap. = 6000 μF, V_{IN} = 12 V_{RMS}, C_{OUT} = 0.2 μF, 25°C, I_{OUT} = 2 A unless otherwise specified.

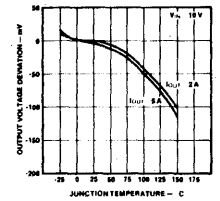
SYMBOL	CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNITS
V_{OUT}	Output Voltage	I_{OUT} = 2 A	4.8	5.0	5.2	V
ΔV_{OUT}	Line Regulation	V_{IN} 8.6 V_{RMS} to 23 V_{RMS}		10	30	mV
ΔV_{OUT}	Load Regulation	10 mA ≤ I_{OUT} ≤ 5 A		10	50	mV
	Input Voltage	I_{OUT} = 0 to 3 A	8.6		23	V_{RMS}
		I_{OUT} = 3 to 5 A	11.4		15	V_{RMS}
I_Q	Quiescent Current	I_{OUT} = 0		3	10	mA
R_R	Ripple Rejection	60 Hz Line	60			db
I_{OS}	Short Circuit Current			7		A
	Dropout Voltage	I_{OUT} = 5.0 A - Note 1		2.0		V
		I_{OUT} = 3 A - Note 1		1.8		V

TYPICAL PERFORMANCE CHARACTERISTICS

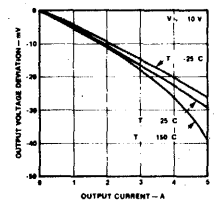
MAXIMUM POWER DISSIPATION



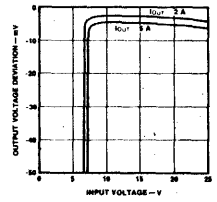
OUTPUT VOLTAGE DEVIATION AS A FUNCTION OF JUNCTION TEMPERATURE



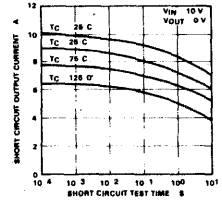
LOAD REGULATION



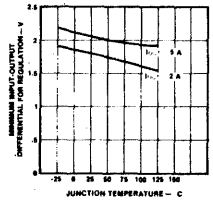
REGULATOR SECTION LINE REGULATION



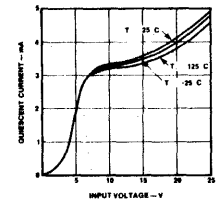
SHORT CIRCUIT CURRENT



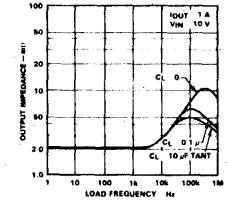
REGULATOR SECTION DROP OUT VOLTAGE



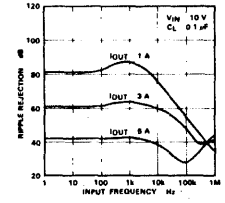
QUIESCENT CURRENT



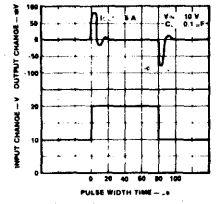
OUTPUT IMPEDANCE



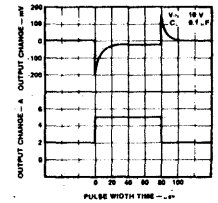
REGULATOR SECTION RIPPLE REJECTION



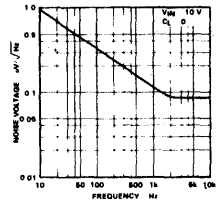
LINE TRANSIENT RESPONSE



LOAD TRANSIENT RESPONSE



OUTPUT NOISE VOLTAGE



SH3015

SERVO AMPLIFIER AND MOTOR DRIVER

FAIRCHILD HYBRID PRODUCTS

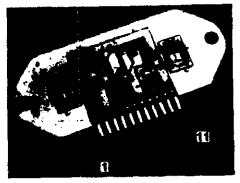
GENERAL DESCRIPTION — The SH3015 is a high-power amplifier designed for applications requiring high currents and high voltage capability. This product is designed to supply up to 6 A continuously to load between ±35 V. The SH3015 incorporates a μA741 Operational Amplifier input with current and voltage gain stages to reach this capability. The design allows the user to set the output current limit to the level required. The SH3015 is stable when driving resistive and inductive loads and the output is protected from voltage transients at the output due to inductive kickback. Output current is selectively limited by placing resistors between the supply pins and the respective current limit pins.

- **INTERNALLY COMPENSATED**
- **PROGRAMMABLE CURRENT LIMITING**
- **STABLE WITH INDUCTIVE LOADS**
- **CASE IS ELECTRICALLY ISOLATED**

ABSOLUTE MAXIMUM RATINGS

Internal Power Dissipation DC (25°C case)	70 W
Internal Power Dissipation (1 s max x 25°C case)	100 W
Power Supply Voltages	±40 V
Input Voltage-Either Input	±15 V
Input Voltage-Differential	30 V
Output Current DC	10 A
1 s max	15 A
Operating Case Temperature Range	0 to 70°C
Storage Temperature Range	-20°C to +85°C
Lead Solder Temperature (10 s)	300°C

PIN CONNECTIONS
(TOP VIEW)

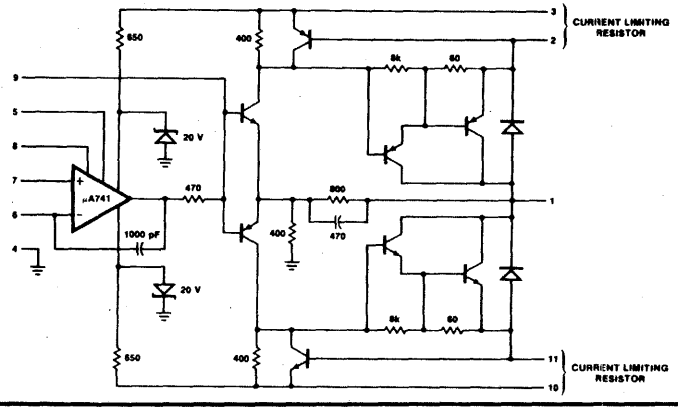


PIN	FUNCTION
1	Output
2	I_{SC} +
3	V+
4	Ground
5	Offset Adj.
6	Inverting Input
7	Non-inverting Input
8	Offset Adj.
9	Disable Input
10	V-
11	I_{SC}-

ORDER INFORMATION

TEMP RANGE	PART NO.
0° to 70°C	SH3015

EQUIVALENT CIRCUIT



ELECTRICAL CHARACTERISTICS: V± = 24 V, Case = 25°C

CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNIT
Input Offset Voltage	R_S = < 10 kΩ			±6	mV
Input Offset Current				200	nA
Input Bias Current				500	nA
Input Voltage Range		±15			V
Output Voltage Swing	I_{OUT} < 10 A	±20			V
Supply Current	I_{OUT} = 0, V ± = 40 V		14	20	mA
Voltage Gain		40,000			

SH3011

DUAL 5 AMP DRIVER

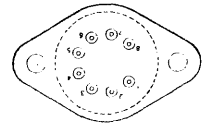
GENERAL DESCRIPTION — The SH3011 is a dual high-current driver designed for a wide range of applications. The device is capable of driving two 5 amp loads (10 amps combined) at a 50% duty cycle. The inputs are TTL compatible and outputs are completely separate.

- **OUTPUT CURRENT OF 5 AMP EACH**
- **100% DUTY CYCLE OPERATION**
- **TTL COMPATIBLE INPUTS**
- **FAST SWITCHING TIMES**
- **UNCOMMITTED COLLECTOR AND EMITTER**
- **TWO INDEPENDENT DRIVERS IN ONE PACKAGE**

ABSOLUTE MAXIMUM RATINGS

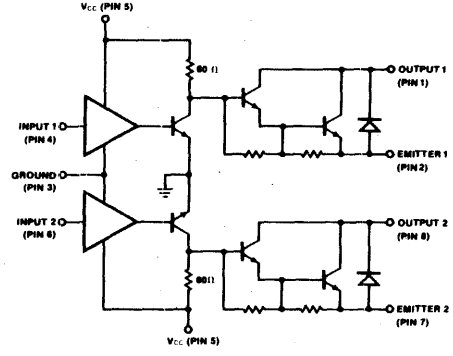
Supply Voltage (V_{CC})	7 V
Collector to Emitter Voltage (V_{CE})	80 V
Continuous Collector Current	5 A
Peak Collector Current	8 A
Operating Case Temperature Range	0 to 75°C
Storage Temperature Range	-65 to +150°C
Lead Solder Temperature (10 s)	300°C

CONNECTING DIAGRAM
8-PIN TO-3 TYPE



Pin	Function
1	Output-driver 1
2	Emitter-driver 1
3	Ground
4	Input-driver 1
5	V_{CC}
6	Input-driver 2
7	Emitter-driver 2
8	Output-driver 2

EQUIVALENT CIRCUIT



ELECTRICAL CHARACTERISTICS

SYMBOL	CHARACTERISTICS	CONDITIONS	MIN	TYP NOTE 1	MAX	UNIT
V_{IH}	Input HIGH Voltage		2.0			V
V_{IL}	Input LOW Voltage				0.8	V
I_{OH}	Output HIGH Current	V_{CC} = 5.0 V, V_{OH} = 40.0 V, V_{IH} = 2.0 V		15		μA
V_{OL}	Output LOW Voltage	V_{CC} = 5.0 V, V_{IL} = 0.8 V, I_{OL} = 3.0 A		1.4		V
		V_{CC} = 5.0 V, V_{IL} = 0.8 V, I_{OL} = 5.0 A		1.8		V
I_I	Input Current at Maximum Input Voltage	V_{CC} = 5.5 V, V_I = 5.5 V			1.0	mA
I_{IH}	Input HIGH Current	V_{CC} = 5.5 V, V_I = 2.4 V			40.0	μA
I_{IL}	Input LOW Current	V_{CC} = 5.5 V, V_I = 0.4 V		-1.0	-1.6	mA
I_{CCH}	Supply Current, Output HIGH	V_{CC} = 5.0 V, V_I = 5.0 V		170		mA
I_{CCL}	Supply Current, Output LOW	V_{CC} = 5.0 V, V_I = 0 V		98		mA

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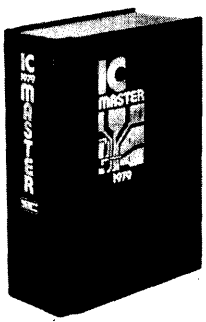
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HA-909/911

Wideband, Low Noise, Operational Amplifiers

FEATURES

- LOW BROADBAND NOISE — 1μV R.M.S.
- LOW NOISE VOLTAGE — 7nV/$\sqrt{Hz}$
- LOW OFFSET VOLTAGE — 2mV
- WIDE BANDWIDTH — 7MHz
- POWER BANDWIDTH — 20kHz
- SUPPLY RANGE — ±5V TO ±20V
- INTERNALLY COMPENSATED

APPLICATIONS

- HIGH Q, WIDEBAND FILTERS
- AUDIO AMPLIFIERS
- SIGNAL GENERATORS

DESCRIPTION

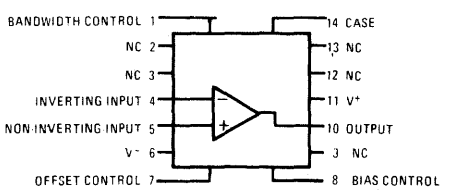
HA-909 and HA-911 are monolithic ampliifers delivering very low noise and excellent bandwidth specifications without the need for external compensation. Additional features of these dielectrically isolated devices include low offset voltage, offset trim capabitlity (14-pin flat package only), and high output current drive capabitlity.

With 7MHz bandwidth and internal compensation these amplifiers are extremely useful in many active filter designs. In audio circuitry requiring quiet operation these devices offer 1 μ V typical broadband noise (10Hz to 1kHz) and 20kHz power bandwidth. 2mV typical offset voltage, offset trim capability, and 20mA output current drive capability (±10.0V swing) make these amplifiers useful in signal conditioning circuits.

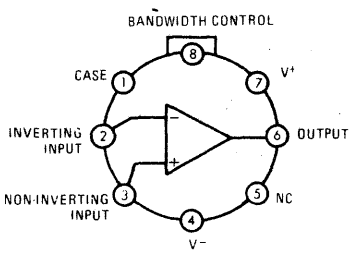
HA-909 and HA-911 are available in metal can (TO-99) and 14-pin flat packages. HA-909 is specified over the -55°C to +125°C range. HA-911 is specified from 0°C to +75°C.

PINOUT

TO-86 — TOP VIEW — **Package Code 9V**

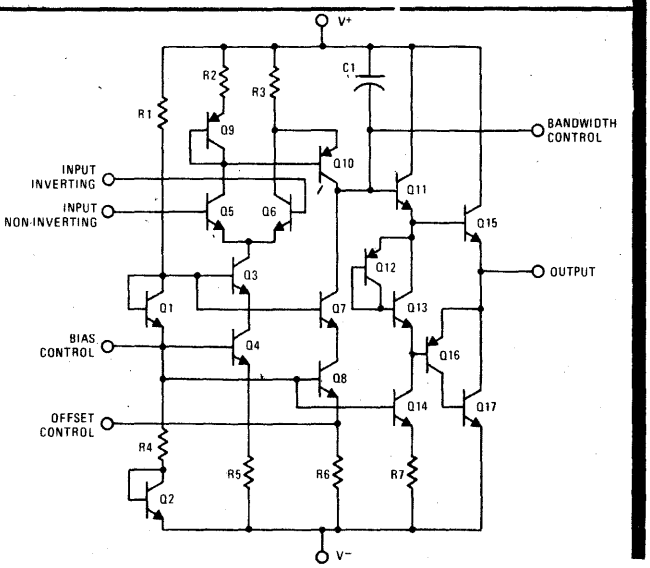


TO-99 — TOP VIEW — **Package Code 2A**



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow IC Handling Procedures.

SCHEMATIC



SEE PAGES 1022-1025 FOR PACKAGE SELECTION GUIDE

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ABSOLUTE MAXIMUM RATINGS

Voltage Between V^+ and V^- Terminals		50.0V
Differential Input Voltage		±7.0V
Peak Output Current		±50mA
Internal Power Dissipation (Note 10)		300mW
Operating Temperature Range –	HA-909	$-55^oC \leq T_A \leq +125^oC$
	HA-911	$0^oC \leq T_A \leq +75^oC$
Storage Temperature Range		$-65^oC \leq T_A \leq +150^oC$

ELECTRICAL CHARACTERISTICS

TEST CONDITIONS: V_{Supply} = ±15.0V unless otherwise specified.

PARAMETER	TEMP.	HA-909 -55°C to +125°C MIN.	HA-909 TYP.	HA-909 MAX.	HA-911 0°C to +75°C MIN.	HA-911 TYP.	HA-911 MAX.	UNITS
INPUT CHARACTERISTICS								
* Offset Voltage	+25°C		2.0	5.0		2.0	6.0	mV
	Full			6.0			7.5	mV
Equivalent Input Noise (Note 9)	+25°C		1.0	5.0		1.0		μV
Input Noise Voltage	+25°C		7			7		nV/√Hz
* Bias Current	+25°C		87	300		200	500	nA
	Full			750		300	750	nA
* Offset Current	+25°C		25	150		100	300	nA
	Full		50	300		150	450	nA
Offset Current Average Drift	Full		1.0			1.0		nA/°C
Input Resistance	+25°C	200	600		100	250		KΩ
	Full	100	300					KΩ
Common Mode Range	Full	+12.0			+12.0			V
TRANSFER CHARACTERISTICS								
* Large Signal Voltage Gain (Notes 1, 4)	+25°C	25K	45K		20K	45K		V/V
	Full	25K	45K		15K	45K		V/V
Full Power BW	+25°C		20			20		KHz
* Common Mode Rejection Ratio (Note 2)	Full	80	96		74	90		dB
Unity Gain Bandwidth (Note 3)	+25°C		7			7		MHz
OUTPUT CHARACTERISTICS								
Output Voltage Swing (Note 1)	Full	+12.0			+11.0			V
* Output Current (Note 4)	+25°C	+20			+15			mA
Output Resistance	+25°C		150			500		Ohms
TRANSIENT RESPONSE								
Rise Time (Notes 1, 5, 6 & 8)	+25°C		40	75		40	75	ns
Overshoot (Notes 1, 5, 6 & 8)	+25°C		15	40		15	40	%
* Slew Rate (Notes 1, 5 & 8)	+25°C	+3.5	+5.0			+5.0		V/μs
		-1.2	-2.0			-2.0		
POWER SUPPLY CHARACTERISTICS								
* Supply Current	+25°C		1.8	2.5		1.8	2.5	mA
* Power Supply Rejection Ratio (Note 7)	Full	80	92		74	90		dB

NOTES:
1. R_L = 2KΩ
2. V_{CM} = ±5.0V
3. V_O < 90mV
4. V_O = ±10.0V
5. C_L = 100pF
6. V_O = ±200mV
7. V_{Sup} = ±9.0V to ±15.0V
8. See Transient Response test circuits and waveforms - page 3.
9. 10 - 1000Hz, R_S = 10K
10. Derate by 6.6mW/°C above 105°C

*100% Tested For DASH 8

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A DIVISION OF HARRIS CORPORATION

HA-2050/2055/2050A 2055A

High Slew Rate F.E.T. Input Operational Amplifiers

FEATURES

- HIGH SLEW RATE — 120V/μs
- FAST SETTLING — 400ns
- WIDE POWER BANDWIDTH — 2MHz
- HIGH GAIN BANDWIDTH — 20MHz
- HIGH INPUT IMPEDANCE — 10^{12} OHMS
- LOW BIAS CURRENT — 1pA
- TRUE OP AMP – CAN BE OPERATED INVERTING OR NON-INVERTING

APPLICATIONS

- DATA ACQUISITION
- SIGNAL CONDITIONING
- R.F. AND VIDEO AMPLIFICATION

DESCRIPTION

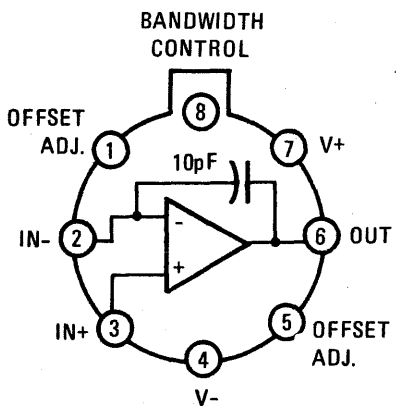
The HA-2050/2055 is an operational amplifier combining the advantages of very high slew rate and wide bandwidth with ultra-low input current and high input resistance. These devices are ideal for use in sample-and-hold circuits, A/D, D/A and sampled data systems; and for use in wide band R.F. or video systems where wide bandwidth at high output levels is required. The device may be operated inverting or noninverting; and external compensation is required only when operated at closed loop gains less than three. An internal feedback capacitor is provided to cancel phase shift in the feedback loop due to input capacitance.

The HA-2050 is guaranteed for operation from -55°C to +125°C and the HA-2055 is guaranteed from 0°C to +75°C.

PINOUT

TO-99 — Package Code 2A

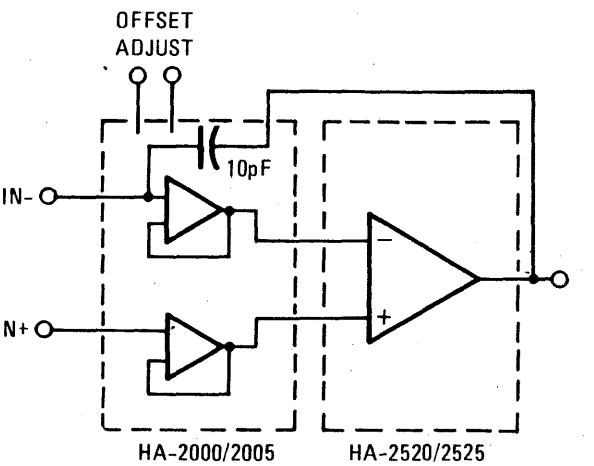
Top View



Case Connected to V+

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow IC Handling Procedures.

FUNCTIONAL DIAGRAM



SEE PAGES 1022-1025 FOR PACKAGE SELECTION GUIDE

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SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Voltage Between V+ and V− Terminals	35.0V	Internal Power Dissipation (Note 10)	300mW	
Differential Input Voltage	±15.0V	Operating Temp. Range	$-55^{o}C \leq T_A \leq +125^{o}C$	(HA-2050)
Output Current	50mA		$0^{o}C \leq T_A \leq +75^{o}C$	(HA-2055)
		Storage Temp. Range	$-65^{o}C \leq T_A \leq +150^{o}C$	

ELECTRICAL CHARACTERISTICS

Test Conditions: V_{Supply} = ±15.0V unless otherwise specified.

PARAMETER	TEMP.	HA-2050/HA-2050A −55°C to +125°C LIMITS MIN.	TYP.	MAX.	HA-2055/HA-2055A 0°C to +75°C LIMITS MIN.	TYP.	MAX.	UNITS
INPUT CHARACTERISTICS								
* Offset Voltage (Note 1)								
HA-2050 / HA-2055	+25°C		15	25		30	60	mV
	Full			30			65	mV
HA-2050A / HA-2055A	+25°C		7	14		7	14	mV
	Full			17			17	mV
Bias Current	+25°C		1	20		1	20	ρA
* (125°C)	Full		0.5	10		0.02	1	nA
Offset Current	+25°C		0.5	20		0.5	20	ρA
* (125°C)	Full		0.1	5		.005	0.5	nA
Input Resistance	+25°C		10^{12}			10^{12}		Ω
Input Capacitance	+25°C		5			5		ρF
Common Mode Range	Full	±10.0			±10.0			V
TRANSFER CHARACTERISTICS								
* Large Signal Voltage Gain (Note 2,5)	+25°C	7.5K	15K		7.5K	15K		V/V
	Full	5K			5K			V/V
* Common Mode Rejection Ratio (Note 3)	Full	74	90		70	90		dB
Gain Bandwidth Product (Note 4)	+25°C		20			20		MHz
OUTPUT CHARACTERISTICS								
* Output Voltage Swing (Note 2)	Full	±10	±12		±10	±12		V
* Output Current	+25°C	±10	±20		±10	±20		mA
Full Power Bandwidth (Note 5)	+25°C		2,000			2,000		kHz
TRANSIENT RESPONSE (NOTES 2, 8, 9)								
Rise Time (Note 6)	+25°C		50			50		ns
Overshoot (Note 6)	+25°C		25			25		%
Slew Rate (Note 5)	+25°C		120			120		V/μs
Settling Time	+25°C		0.4			0.4		μs
POWER SUPPLY CHARACTERISTICS								
* Supply Current	+25°C		6.0	8.0		6.0	8.0	mA
* Power Supply Rejection Ratio (Note 7)	Full	74	90		70	90		dB

NOTES:
1. Adjustable to zero with 100KΩ pot between pins 1 and 5; wiper to V+.
2. R_L = 2K
3. V_{CM} = ±5.0V
4. $A_V > 10$
5. V_O = ±10V
6. V_O = ±200mV
7. ΔV = ±5.0V
8. C_L = 50pF
9. A_V = +3, See transient response test circuit and wave forms, page 4.
10. Derate by 6.6mW/°C above 105°C

*100% Tested for DASH 8

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HA-2060/2065/ 2060A/2065A

Wide Band F.E.T. Input Operational Amplifier

FEATURES

- GAIN BANDWIDTH PRODUCT 100MHz
- HIGH INPUT IMPEDANCE 10^{12} OHMS
- LOW BIAS CURRENT 1pA
- HIGH SLEW RATE 35V/μs
- WIDE POWER BANDWIDTH 600kHz
- TRUE OP AMP – CAN BE OPERATED INVERTING OR NON-INVERTING

APPLICATIONS

- SIGNAL CONDITIONING
- ACTIVE FILTERS
- SIGNAL GENERATORS

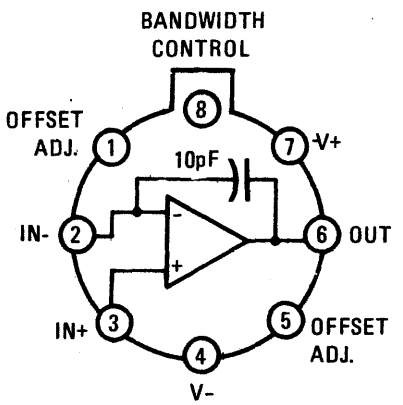
DESCRIPTION

The HA-2060/2065 is an operational amplifier combining the advantages of very wide bandwidth and high slew rate with ultra-low input current and high input resistance. These devices are ideal for use in sample-and-hold circuits, active filters, wide band amplifiers, high gain amplifiers with superior bandwidth, and wherever very low closed loop gain and phase shift errors are required. The device may be operated inverting or noninverting; and external compensation is required only when operating at closed loop gains less than five. An internal feedback capacitor is provided to cancel phase shift in the feedback loop due to input capacitance.

The HA-2060 is guaranteed for operation from -55°C to +125°C and the HA-2065 is guaranteed from 0°C to +75°C.

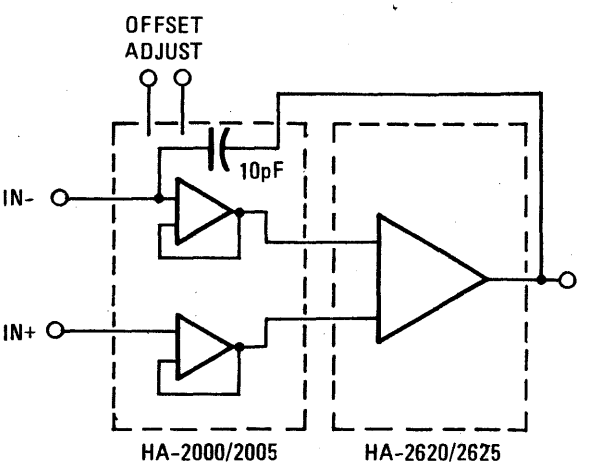
PINOUT

TO-99 Top View **Package Code 2A**



Case Connected to V+

FUNCTIONAL DIAGRAM



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow IC Handling Procedures.

SEE PAGES 1022-1025 FOR PACKAGE SELECTION GUIDE

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ABSOLUTE MAXIMUM RATINGS

Voltage Between V+ and V- Terminals	35.0V	Internal Power Dissipation (Note 10)	300mW
Differential Input Voltage	±12V	Operating Temp. Range	$-55^{o}C \leq T_A \leq +125^{o}C$ (HA-2060)
Output Current / Full Short Circuit Protection			$0^{o}C \leq T_A \leq +75^{o}C$ (HA-2065)
		Storage Temp. Range	$-65^{o}C \leq T_A \leq +150^{o}C$

ELECTRICAL CHARACTERISTICS

Test Conditions: $V_{Supply} = \pm 15.0V$ unless otherwise specified.

PARAMETER	TEMP.	HA-2060/HA-2060A -55°C to +125°C LIMITS MIN.	TYP.	MAX.	HA-2065/HA-2065A 0°C to +75°C LIMITS MIN.	TYP.	MAX.	UNITS
INPUT CHARACTERISTICS								
* Offset Voltage (Note 1)								
HA-2060 / HA-2065	+25°C		15	25		15	60	mV
	Full			30			65	mV
HA-2060A / HA-2065A	+25°C		7	12		7	12	mV
	Full			15			15	mV
Bias Current	+25°C		1	20		1	20	ρA
* (125°C)	Full		0.5	10		0.02	1	nA
Offset Current	+25°C		0.5	20		0.5	20	ρA
* (125°C)	Full		0.1	5		.005	.5	nA
Input Resistance	+25°C		10^{12}			10^{12}		Ω
Input Capacitance	+25°C		5			5		ρF
Common Mode Range	Full	±10.0			±10.0			V
TRANSFER CHARACTERISTICS								
* Large Signal Voltage Gain (Note 2 5)	+25°C	80K	150K		80K	150K		V/V
	Full	60K			70K			V/V
* Common Mode Rejection Ratio (Note 3)	Full	74	90		70	90		dB
Gain Bandwidth Product (Note 4)	+25°C		100			100		MHz
OUTPUT CHARACTERISTICS								
* Output Voltage Swing (Note 2)	Full	±10	±12		±10	±12		V
* Output Current	+25°C	±10	±18		±10	±18		mA
Full Power Bandwidth (Note 5)	+25°C		600			600		kHz
TRANSIENT RESPONSE (NOTES 2, 8, 9)								
Rise Time (Note 6)	+25°C		50			50		ns
Overshoot (Note 6)	+25°C		25			25		%
Slew Rate (Note 5)	+25°C		35			35		V/μs
POWER SUPPLY CHARACTERISTICS								
* Supply Current	+25°C		4.0	6.0		4.0	6.0	mA
* Power Supply Rejection Ratio (Note 7)	Full	74	90		70	90		dB

NOTES:
1. Adjustable to zero with 100K Ω pot between pins 1 and 5; wiper to V+.
2. $R_L = 2K$
3. $V_{CM} = \pm 5.0V$
4. $A_V > 10$
5. $V_O = \pm 10V$
6. $V_O = \pm 200mV$
7. $\Delta V = \pm 5.0V$
8. $C_L = 50 \rho F$
9. $A_V = +5$, See transient response test circuits and waveforms, page 4.
10. Derate by 6.6mW/°C above 105°C

*100% Tested for DASH 8

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HA-2400/2404/2405

PRAM™ Four Channel Programmable Amplifier

FEATURES

- PROGRAMMABILITY
- HIGH SLEW RATE 30V/μs
- WIDE GAIN BANDWIDTH 40MHz
- HIGH GAIN 150,000
- LOW OFFSET CURRENT 5nA
- HIGH INPUT IMPEDANCE 30MΩ
- SINGLE CAPACITOR COMPENSATION
- DTL/TTL COMPATIBLE INPUTS

APPLICATIONS

- THOUSANDS OF NEW APPLICATIONS; PROGRAM
  - SIGNAL SELECTION/MULTIPLEXING
  - OP AMP GAIN
  - OSCILLATOR FREQUENCY
  - FILTER CHARACTERISTICS
  - ADD-SUBTRACT FUNCTIONS
  - INTEGRATOR CHARACTERISTICS
  - COMPARATOR LEVELS

DESCRIPTION

HA-2400/2404/2405 comprise a series of four-channel programmable amplifiers providing a level of versatility unsurpassed by any other monolithic operational amplifier. Versatility is achieved by employing four input amplifier channels, any one (or none) of which may be electronically selected and connected to a single output stage through DTL/TTL compatible address inputs. The device formed by the output and the selected pair of inputs is an op amp which delivers excellent slew rate, gain bandwidth and power bandwidth performance. Other advantageous features for these dielectrically isolated amplifiers include high voltage gain and input impedance coupled with low input offset voltage and offset current. External compensation is not required on this device at closed loop gains greater than 10.

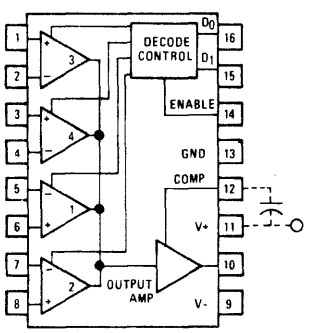
Each channel of the HA-2400/2404/2405 can be controlled and operated with suitable feedback networks in any of the standard op amp configurations. This specialization makes these amplifiers excellent components for multiplexing, signal selection, and mathematical function designs. With 30V/μs slew rate, 40MHz gain bandwidth, and 30M ohms input impedance these devices are ideal building blocks for signal generators, active filters, and data acquisition designs. Programmability coupled with 2mV typical offset voltage and 5nA offset current makes these amplifiers outstanding components for signal conditioning circuits.

HA-2400/2404/2405 are available in a 16 pin dual-in-line package. HA-2400 is specified from -55°C to +125°C. HA-2404 is specified over the -25°C to +85°C range, while HA-2405 operates from 0°C to +75°C.

PINOUT

(TOP VIEW)

Package Code 4B



TRUTH TABLE

D_1	D_0	EN	SELECTED CHANNEL
L	L	H	1
L	H	H	2
H	L	H	3
H	H	H	4
X	X	L	NONE

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow IC Handling Procedures.

SCHEMATIC

Condensed circuit diagram for a programmable amplifier (PRAM HA-2400)

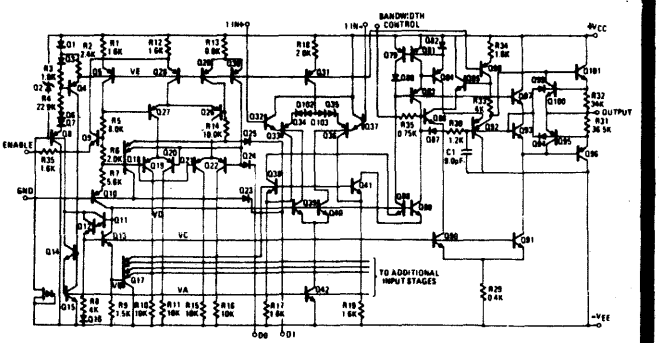


Diagram includes: ONE INPUT STAGE, DECODE CONTROL, BIAS NETWORK AND OUTPUT STAGE

SEE PAGES 1022-1025 FOR PACKAGE SELECTION GUIDE

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ABSOLUTE MAXIMUM RATINGS

Voltage Between V+ and V− Terminals	45.0V	Internal Power Dissipation (Note 13)	300mW
Differential Input Voltage	$\pm V_{Supply}$	Operating Temperature Range	$-55^oC \leq T_A \leq +125^oC$ (HA-2400)
Digital Input Voltage	−0.76V to +10.0V		$-25^oC \leq T_A \leq +85^oC$ (HA-2404)
Output Current	Short Circuit Protected		$0^oC \leq T_A \leq +75^oC$ (HA-2405)
		Storage Temperature Range	$-65^oC \leq T_A \leq +150^oC$

ELECTRICAL CHARACTERISTICS

Test Conditions: $V_{Supply} = \pm 15.0V$ unless otherwise specified.

Digital inputs: $V_{IL} = +0.5V$, $V_{IH} = +2.4V$
Limits apply to each of the four channels, when addressed.

PARAMETER	TEMP.	HA-2400/HA-2404 LIMITS MIN.	TYP.	MAX.	HA-2405 LIMITS MIN.	TYP.	MAX.	UNITS
INPUT CHARACTERISTICS								
* Offset Voltage	+25°C		2	5		4	9	mV
	Full			7			11	mV
* Bias Current (Note 12)	+25°C		50	200		50	250	nA
	Full			400			500	nA
* Offset Current (Note 12)	+25°C		5	50		5	50	nA
	Full			100			100	nA
Input Resistance (Note 12)	+25°C		30			30		MΩ
Common Mode Range	Full	±10.0			±10.0			V
TRANSFER CHARACTERISTICS								
* Large Signal Voltage Gain (Note 1,5)	+25°C	50K	150K		50K	150K		V/V
	Full	25K			25K			V/V
* Common Mode Rejection Ratio (Note 2)	Full	80	100		74	100		dB
Gain Bandwidth (Note 3)	+25°C		40			40		MHz
(Note 4)	+25°C		8			8		MHz
OUTPUT CHARACTERISTICS								
Output Voltage Swing (Note 1)	Full	±10.0	±12.0		±10.0	±12.0		V
Output Current	+25°C		20			20		mA
Full Power Bandwidth (Notes 3, 5)	+25°C		500			500		kHz
(Notes 4,5)	+25°C		200			200		kHz
TRANSIENT RESPONSE								
Rise Time (Notes 4,6)	+25°C		20			20		ns
Overshoot (Notes 4,6)	+25°C		25			25		%
Slew Rate (Notes 3,7)	+25°C		30			30		V/μs
(Notes 4,7)	+25°C		8			8		V/μs
Settling Time (Notes 4, 7, 8)	+25°C		1.5			1.5		μs
CHANNEL SELECT CHARACTERISTICS								
Digital Input Current ($V_{IN} = 0V$)	Full		1			1		mA
Digital Input Current ($V_{IN} = +5.0V$)	Full		5			5		nA
Output Delay (Note 9)	+25°C		100			100		ns
Crosstalk (Note 10)	+25°C	-80	-110		-74	-110		dB
POWER SUPPLY CHARACTERISTICS								
* Supply Current	+25°C		4.8	6.0		4.8	6.0	mA
* Power Supply Rejection Ratio (Note 11)	Full	74	90		74	90		dB

NOTES:
1. $R_L = 2K\Omega$
2. $V_{CM} = \pm 5$ V.D.C.
3. $A_V = +10$, $C_{COMP} = 0$, $R_L = 2K\Omega$, $C_L = 50pF$
4. $A_V = +1$, $C_{COMP} = 15pF$, $R_L = 2K\Omega$, $C_L = 50pF$
5. $V_{OUT} = 20V$ peak-to-peak
6. $V_{OUT} = 400$ mV peak-to-peak
7. $V_{OUT} = 10.0V$ peak-to-peak
8. To 0.1% of final value
9. To 10% of final value; output then slews at normal rate to final value.
10. Unselected input to output; $V_{IN} = \pm 10$ V.D.C.
11. $V_{SUPP} = \pm 10V$ D.C. to $\pm 20V$ D.C.
12. Unselected channels have approximately the same input parameters.
13. Derate by 4.3mW/°C above 105°C

*100% Tested For DASH 8

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HA-2500/02/05

Precision High Slew Rate Operational Amplifiers

FEATURES

- HIGH SLEW RATE 30V/μS
- FAST SETTLING 330ns
- WIDE POWER BANDWIDTH 500kHz
- HIGH GAIN BANDWIDTH 12MHz
- HIGH INPUT IMPEDANCE 100MΩ
- LOW OFFSET CURRENT 10nA
- INTERNALLY COMPENSATED

APPLICATIONS

- DATA ACQUISTION SYSTEMS
- R.F. AMPLIFIERS
- VIDEO AMPLIFIERS
- SIGNAL GENERATORS
- PULSE AMPLIFICATION

DESCRIPTION

HA-2500/2502/2505 comprise a series of monolithic operational amplifiers whose designs are optimized to deliver excellent slew rate, bandwidth, and settling time specifications. The outstanding dynamic features of this internally compensated device are complemented with low offset voltage and offset current.

These dielectrically isolated amplifiers are ideally suited for applications such as data acquisition, R.F., video, and pulse conditioning circuits. Slew rate of ±25V/μs and 330ns (0.1%) settling time make these devices excellent components in fast, accurate data acquisition and pulse amplification designs. 12 MHz bandwidth and 500kHz power bandwidth make these devices well suited to R.F. and video applications. With 2mV typical offset voltage plus offset trim capability and 10nA offset current, HA-2500/2502/2505 are particularly useful components in signal conditioning designs.

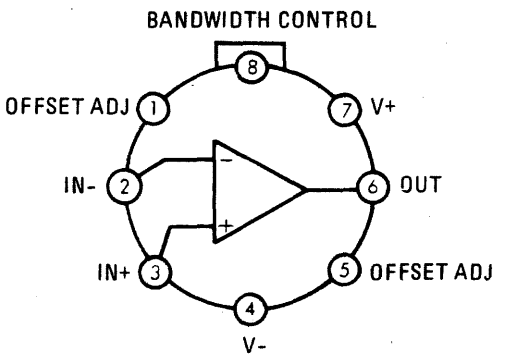
The gain and offset voltage figures of the HA-2500 series are optimized by internal component value changes while the similar design of the HA-2510 series is maximized for slew rate.

HA-2500/2502/2505 are available in metal can (TO-99) packages. HA-2500 and HA-2502 are specified over the -55°C to +125°C range. HA-2505 is specified from 0°C to +75°C.

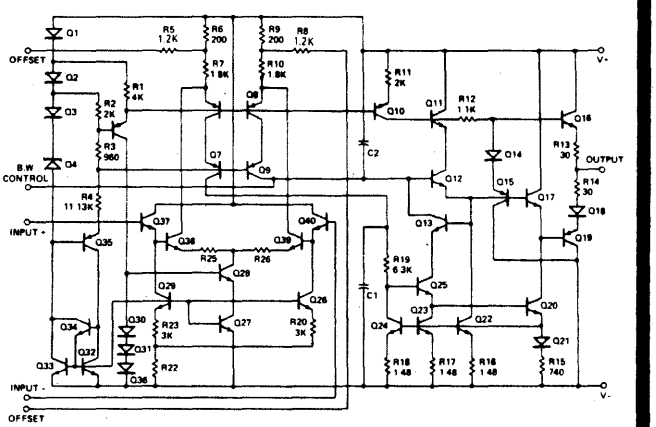
PINOUT

TO-99 **Package Code 2A**

Top View



SCHEMATIC



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow IC Handling Procedures.

SEE PAGES 1022-1025 FOR PACKAGE SELECTION GUIDE

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ABSOLUTE MAXIMUM RATINGS

Voltage Between V^+ and V^- Terminals	40.0V	Operating Temperature Range –	HA-2500/HA-2502	$-55^oC \leq T_A \leq +125^oC$
Differential Input Voltage	±15.0V		HA-2505	$0^oC \leq T_A \leq +75^oC$
Peak Output Current	50mA	Storage Temperature Range		$-65^oC \leq T_A \leq +150^oC$
Internal Power Dissipation	300mW			

ELECTRICAL CHARACTERISTICS

$V+ = +15V$ D.C., $V- = -15V$ D.C.

		HA-2500 -55°C to +125°C			HA-2502 -55°C to +125°C			HA-2505 0°C to +75°C			
		LIMITS			LIMITS			LIMITS			
PARAMETER	TEMP.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	UNITS
INPUT CHARACTERISTICS											
* Offset Voltage	+25°C		2	5		4	8		4	8	mV
	Full			8			10			10	mV
Offset Voltage Average Drift	Full		20			20			20		µV/°C
* Bias Current	+25°C		100	200		125	250		125	250	nA
	Full			400			500			500	nA
* Offset Current	+25°C		10	25		20	50		20	50	nA
	Full			50			100			100	nA
Input Resistance	+25°C	25	50		20	50		20	50		MΩ
Common Mode Range	Full	±10.0			±10.0			±10.0			V
TRANSFER CHARACTERISTICS											
* Large Signal Voltage Gain (Note 1,4)	+25°C	20K	30K		15K	25K		15K	25K		V/V
	Full	15K			10K			10K			V/V
* Common Mode Rejection Ratio (Note 2)	Full	80	90		74	90		74	90		dB
Gain Bandwidth Product (Note 3)	+25°C		12			12			12		MHz
OUTPUT CHARACTERISTICS											
Output Voltage Swing (Note 1)	Full	±10.0	±12.0		±10.0	±12.0		±10.0	±12.0		V
* Output Current (Note 4)	+25°C	±10	±20		±10	±20		±10	±20		mA
Full Power Bandwidth (Note 4)	+25°C	350	500		300	500		300	500		kHz
TRANSIENT RESPONSE											
Rise Time (Notes 1, 5, 6 & 8)	+25°C		25	50		25	50		25	50	ns
Overshoot (Notes 1, 5, 7 & 8)	+25°C		25	40		25	50		25	50	%
* Slew Rate (Notes 1,4,5 & 8)	+25°C	±25	±30		±20	±30		±20	±30		V/µs
Settling Time to 0.1% (Notes 1,4,5 & 8)	+25°C		0.33			0.33			0.33		µs
POWER SUPPLY CHARACTERISTICS											
* Supply Current	+25°C		4	6		4	6		4	6	mA
* Power Supply Rejection Ratio (Note 9)	Full	80	90		74	90		74	90		dB

NOTES:
1. $R_L = 2K$
2. $V_{CM} = \pm 5.0V$
3. $A_V > 10$
4. $V_O = \pm 10.0V$
5. $C_L = 50pF$
6. $V_O = \pm 400mV$
7. $V_O = \pm 600mV$
8. See transient response test circuits and waveforms page four.
9. $\Delta V = \pm 5.0V$

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HA-2510/2512/2515

High Slew Rate Operational Amplifiers

FEATURES

- HIGH SLEW RATE — 60V/μs
- FAST SETTLING — 250ns
- WIDE POWER BANDWIDTH — 1,000kHz
- HIGH GAIN BANDWIDTH — 12MHz
- HIGH INPUT IMPEDANCE — 100MΩ
- LOW OFFSET CURRENT — 10nA
- INTERNALLY COMPENSATED

APPLICATIONS

- DATA ACQUISITION SYSTEMS
- R.F. AMPLIFIERS
- VIDEO AMPLIFIERS
- SIGNAL GENERATORS
- PULSE AMPLIFICATION

DESCRIPTION

The HA-2510/2512/2515 are a series of high performance operational amplifiers which set the standards for maximum slew rate, highest accuracy and widest bandwidth for internally compensated monolithic devices. In addition to excellent dynamic characteristics, these dielectrically isolated amplifiers also offer low offset current and high input impedance.

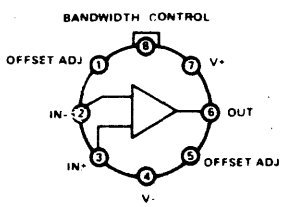
The ±60V/ μs slew rate and 250ns (0.1%) settling time of these amplifiers is ideally suited for high speed D/A, A/D, and pulse amplification designs. HA-2510/2512/2515's superior 12MHz gain bandwidth and 1000kHz power bandwidth is extremely useful in R.F. and video applications. For accurate signal conditioning these amplifiers also provide 10nA offset current, coupled with 100MΩ input impedance, and offset trim capability.

The HA-2510/2512 are available in metal can (TO-99) and 14-pin flat packages. HA-2510 and HA-2512 are specified from -55°C to +125°C. HA-2515 is specified over the 0°C to +75°C range, and is available in the TO-99 package.

PINOUT

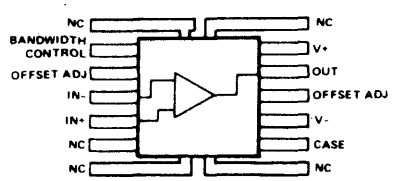
TO-99 TOP VIEW

Package Code 2A

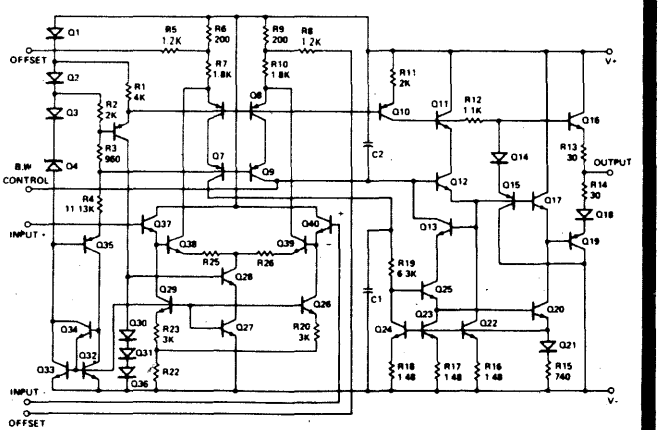


TO-86 TOP VIEW

Package Code 9V
(HA-2510/2512 Only)



SCHEMATIC



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow IC Handling Procedures.

SEE PAGES 1022-1025 FOR PACKAGE SELECTION GUIDE

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SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Voltage Between V^+ and V^- Terminals	40.0V	Peak Output Current	50mA
Differential Input Voltage	±15.0V	Internal Power Dissipation	300mW
Operating Temperature Range		Storage Temperature Range	$-65^oC \leq T_A \leq +150^oC$
HA-2510/HA-2512	$-55^oC \leq T_A \leq +125^oC$		
HA-2515	$0^oC \leq T_A \leq +75^oC$		

ELECTRICAL CHARACTERISTICS

V+ = +15V D.C., V– = 15V D.C.

PARAMETER	TEMP.	HA-2510 -55°C to +125°C LIMITS MIN.	TYP.	MAX.	HA-2512 -55°C to +125°C LIMITS MIN.	TYP.	MAX.	HA-2515 0°C to +75°C LIMITS MIN.	TYP.	MAX.	UNITS
INPUT CHARACTERISTICS											
* Offset Voltage	+25°C		4	8		5	10		5	10	mV
	Full			11			14			14	mV
Offset Voltage Average Drift	Full		20			25			30		µV/°C
* Bias Current	+25°C		100	200		125	250		125	250	nA
	Full			400			500			500	nA
* Offset Current	+25°C		10	25		20	50		20	50	nA
	Full			50			100			100	nA
Input Resistance	+25°C	50	100		40	100		40	100		MΩ
Common Mode Range	Full	±10.0			±10.0			±10.0			V
TRANSFER CHARACTERISTICS											
* Large Signal Voltage Gain (Note 1,4)	+25°C	10K	15K		7.5K	15K		7.5K	15K		V/V
	Full	7.5K			5K			5K			V/V
* Common Mode Rejection Ratio (Note 2)	Full	80	90		74	90		74	90		dB
Gain Bandwidth Product (Note 3)	+25°C		12			12			12		MHz
OUTPUT CHARACTERISTICS											
Output Voltage Swing (Note 1)	Full	±10.0	±12.0		±10.0	±12.0		±10.0	±12.0		V
* Output Current (Note 4)	+25°C	±10	±20		±10	±20		±10	±20		mA
Full Power Bandwidth (Note 4)	+25°C	750	1000		600	1000		600	1000		kHz
TRANSIENT RESPONSE											
Rise Time (Notes 1, 5, 6 & 8)	+25°C		25	50		25	50		25	50	ns
Overshoot (Notes 1, 5, 7 & 8)	+25°C		25	40		25	50		25	50	%
* Slew Rate (Notes 1, 4, 5 & 8)	+25°C	±50	±65		±40	±60		±40	±60		V/µs
Settling Time (Notes 1, 4, 5 & 8)	+25°C		0.25			0.25			0.25		µs
POWER SUPPLY CHARACTERISTICS											
* Supply Current	+25°C		4	6		4	6		4	6	mA
* Power Supply Rejection Ratio (Note 9)	Full	80	90		74	90		74	90		dB

NOTES:
1. R_L = 2K
2. V_{CM} = ±5.0V
3. $A_V > 10$
4. V_O = ±10.0V
5. C_L = 50pF
6. V_O = ±400mV
7. V_O = ±600mV
8. See transient response test circuits and waveforms page four.
9. Δ V = ±5.0V

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HA-2507/2517/2527

Epoxy-Packaged, High Slew Rate Operational Amplifier Series

Preliminary

FEATURES

	HA-2507	HA-2517	HA-2527	
• High Slew Rate	30	60	120	V/μs
• Fast Settling	330	250	200	ns
• Wide Power Bandwidth	0.5	1.0	1.6	MHz
• High Gain Bandwidth	12	12	20	MHz
• High Input Impedance	50	100	100	MΩ

APPLICATIONS

- Pulse Amplification
- Video Amplifiers
- High Speed Test Equipment
- Medical Instrumentation
- Data Acquisition Systems
- Signal Generators

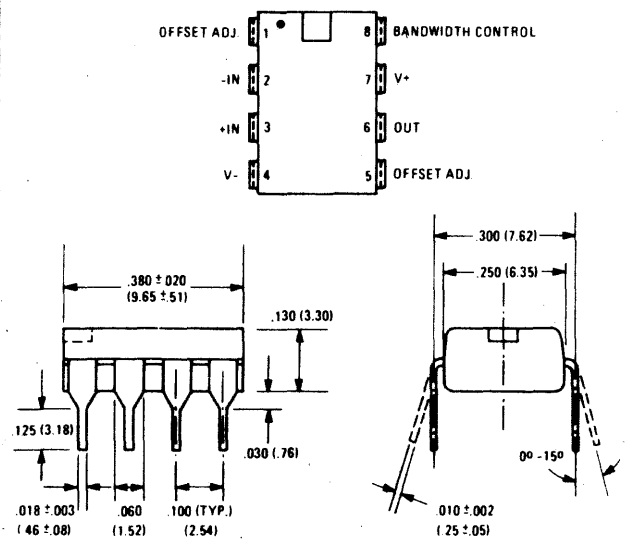
DESCRIPTION

HA-2507/2517/2527 operational amplifiers are a series of high-performance, epoxy-packaged monolithic IC's designed to deliver excellent slew rate, bandwidth and settling time specifications. Typical slew rate specifications for HA-2507, HA-2517 and HA-2527 are 30V/μsec, 60V/μsec and 120V/μsec respectively. Corresponding settling times (10V step to 0.1%) are 330ns, 250ns and 200ns for HA-2507, HA-2517 and HA-2527 respectively. Bandwidths range from 12MHz to 20MHz. This level of performance is achieved through the use of Harris's unique Dielectric Isolation processing techniques. HA-2507/2517/2527 are internally compensated; HA-2507 and HA-2517 are stable for closed loop gains (A_V) greater than or equal to unity. HA-2527 is stable for $A_V > 3$.

This series of op amps affords an economical means of designing high performance equipment for industrial and commercial use. Their slew rate and settling time performance makes them ideally suited for high speed D/A, A/D and pulse amplification designs. The wide bandwidth offered by these devices also makes them valuable components in RF and video applications. HA-2507/2517/2527 also deliver offset current, bias current and offset voltage specifications compatible with the requirements of accurate signal conditioning systems.

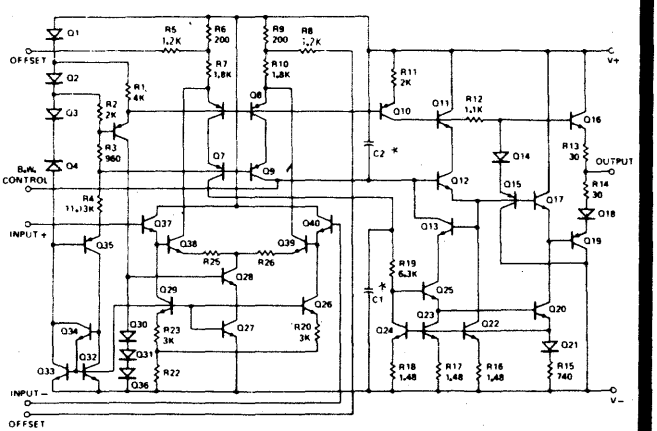
The HA-2507/2517/2527 are specified from 0°C to +75°C and are available in 8-lead epoxy DIP packages that have been extensively tested and qualified to deliver the high level of performance and reliability that are expected of Harris Semiconductor's operational amplifiers.

PINOUT



8 LEAD D.I.P. EPOXY

SCHEMATIC



*VALUES OF C1 AND C2 VARY DEPENDING ON DEVICE TYPE.

SEE PAGES 1022-1025 FOR PACKAGE SELECTION GUIDE

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ABSOLUTE MAXIMUM RATINGS

Voltage Between V^+ and V^- Terminals	40.0V	Operating Temperature Range – HA-2507/HA-2517	$0^oC \leq T_A \leq +75^oC$
Differential Input Voltage	±15.0V	HA-2527	
Peak Output Current	50mA	Storage Temperature Range	$-65^o \leq T_A \leq +150^oC$
Internal Power Dissipation	300mW		

ELECTRICAL CHARACTERISTICS

$V^+ = +15V$ D.C., $V^- = -15V$ D.C.

PARAMETER	TEMP.	HA-2507 0°C to +75°C LIMITS MIN.	HA-2507 TYP.	HA-2507 MAX.	HA-2517 0°C to +75°C LIMITS MIN.	HA-2517 TYP.	HA-2517 MAX.	HA-2527 0°C to +75°C LIMITS MIN.	HA-2527 TYP.	HA-2527 MAX.	UNITS
INPUT CHARACTERISTICS											
Offset Voltage	+25°C		5	10		5	10		5	10	mV
	Full			14			14			14	mV
Offset Voltage Average Drift	Full		25			30			30		µV/°C
Bias Current	+25°C		125	250		125	250		125	250	nA
	Full			500			500			500	nA
Offset Current	+25°C		20	50		20	50		20	50	nA
	Full			100			100			100	nA
Input Resistance	+25°C	20	50		40	100		40	100		MΩ
Common Mode Range	Full	±10.0			±10.0			±10.0			V
TRANSFER CHARACTERISTICS											
Large Signal Voltage Gain (Note 1, 4)	+25°C	15K	25K		7.5K	15K		7.5K	15K		V/V
	Full	10K			5K			5K			V/V
Common Mode Rejection Ratio (Note 2)	Full	74	90		74	90		74	90		dB
Gain Bandwidth Product (Note 3)	+25°C		12			12			20		MHz
OUTPUT CHARACTERISTICS											
Output Voltage Swing (Note 1)	Full	±10.0	±12.0		±10.0	±12.0		±10.0	±12.0		V
Output Current (Note 4)	+25°C	±10	±20		±10	±20		±10	±20		mA
Full Power Bandwidth (Note 4)	+25°C	220	500		450	1000		750	1600		kHz
TRANSIENT RESPONSE											
Rise Times (Notes 1, 5, 6 & 8)	+25°C		25	50		25	50		25	50	ns
Overshoot (Notes 1, 5, 7 & 8)	+25°C		25	50		25	50		25	50	%
Slew Rate (Notes 1, 4, 5 & 8)	+25°C	±15	± 30		±30	± 60		±60	±120		V/µs
Settling Time to 0.1% (Notes 1, 4, 5 & 8)	+25°C		0.33			0.25			0.20		µs
POWER SUPPLY CHARACTERISTICS											
Supply Current	+25°C		4	6		4	6		4	6	mA
Power Supply Rejection Ratio (Note 9)	Full	74	90		74	90		74	90		dB

NOTES:
1. $R_L = 2K$
2. $V_{CM} = +5.0V$
3. $A_V > 10$
4. $V_O = +10.0V$
5. $C_L = 50pF$
6. $V_O = +400mV$ for HA-2507 and HA-2517; $V_O = +200mV$ for HA-2527
7. $V_O = +600mV$
8. For HA-2507 and HA-2517, $A_V = 1$ For HA-2527, $A_V = 3$
9. $\Delta V = +5.0V$

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HA-2520/22/25

Uncompensated High Slew Rate Operational Amplifiers

FEATURES

- HIGH SLEW RATE — 120V/μs
- FAST SETTLING — 200ns
- WIDE POWER BANDWIDTH — 2,000kHz
- HIGH GAIN BANDWIDTH — 20MHz
- HIGH INPUT IMPEDANCE — 100MΩ
- LOW OFFSET CURRENT — 10nA

APPLICATIONS

- DATA ACQUISITION SYSTEMS
- R.F. AMPLIFIERS
- VIDEO AMPLIFIERS
- SIGNAL GENERATORS
- PULSE AMPLIFICATION

DESCRIPTION

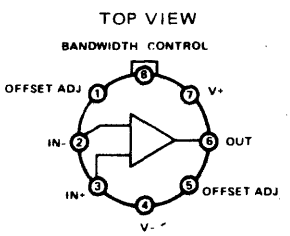
HA-2520/2522/2525 comprise a series of monolithic operational amplifiers delivering an unsurpassed combination of specifications for slew rate, bandwidth and settling time. These dielectrically isolated amplifiers are controlled at closed loop gains greater than 3 without external compensation. In additon, these high performance components also provide low offset current and high input impedance.

120V/μs slew rate and 200ns (0.1%) settling time of these amplifiers make them ideal components for pulse amplification and data acquisition designs. These devices are valuable components for R.F. and video circuitry requiring up to 20MHz gain bandwidth and 2MHz power bandwidth. For accurate signal conditioning designs the HA-2520/2522/2525's superior dynamic specifications are complimented by 10nA offset current, 100MΩ input impedance and offset trim capability.

The HA-2520/2522 are available in metal can (TO-99) and 14-pin flat packages. HA-2520 and HA-2522 are specified over -55°C to +125°C range. HA-2525 is specified from 0°C to +75°C, and is available in the TO-99 package.

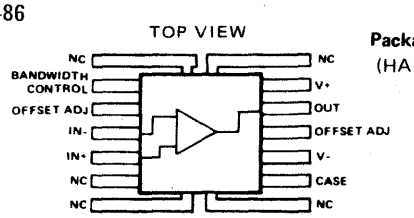
PINOUT

TO-99



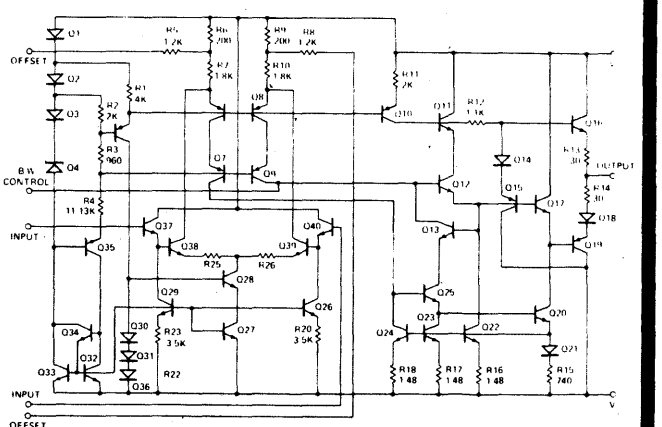
Package Code 2A

TO-86



Package Code 9V
(HA-2520/2522 Only)

SCHEMATIC



SEE PAGES 1022-1025 FOR PACKAGE SELECTION GUIDE

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ABSOLUTE MAXIMUM RATINGS

Voltage Between V^+ and V^- Terminals	40.0V	Peak Output Current	50mA
Differential Input Voltage	±15.0V	Internal Power Dissipation	300mW
Operating Temperature Range			
HA-2520/2522	$-55^oC \leq T_A \leq +125^oC$	Storage Temperature Range	$-65^oC \leq T_A \leq +150^oC$
HA-2525	$0^oC \leq T_A \leq +75^oC$		

ELECTRICAL CHARACTERISTICS

$V+ = +15V$ D.C., $V- = -15V$ D.C.

PARAMETER	TEMP.	HA-2520 -55°C to +125°C LIMITS MIN.	TYP.	MAX.	HA-2522 -55°C to +125°C LIMITS MIN.	TYP.	MAX.	HA-2525 0°C to +75°C LIMITS MIN.	TYP.	MAX.	UNITS
INPUT CHARACTERISTICS											
* Offset Voltage	+25°C Full		4	8 11		5	10 14		5	10 14	mV mV
Offset Voltage Average Drift	Full		20			25			30		µV/°C
* Bias Current	+25°C Full		100	200 400		125	250 500		125	250 500	nA nA
* Offset Current	+25°C Full		10	25 50		20	50 100		20	50 100	nA nA
Input Resistance	+25°C	50	100		40	100		40	100		MΩ
Common Mode Range	Full	±10.0			±10.0			±10.0			V
TRANSFER CHARACTERISTICS											
* Large Signal Voltage Gain (Note 1,4)	+25°C Full	10K 7.5K	15K		7.5K 5K	15K		7.5K 5K	15K		V/V V/V
* Common Mode Rejection Ratio (Note 2)	Full	80	90		74	90		74	90		dB
Gain Bandwidth Product (Note 3)	+25°C		20			20			20		MHz
OUTPUT CHARACTERISTICS											
Output Voltage Swing (Note 1)	Full	±10.0	±12.0		±10.0	±12.0		±10.0	±12.0		V
* Output Current (Note 4)	+25°C	±10	±20		±10	±20		±10	±20		mA
Full Power Bandwidth (Note 4)	+25°C	1500	2000		1200	1600		1200	1600		kHz
TRANSIENT RESPONSE ($A_V = +3$)											
Rise Time (Notes 1, 5, 6 & 8)	+25°C		25	50		25	50		25	50	ns
Overshoot (Notes 1, 5, 6 & 8)	+25°C		25	40		25	50		25	50	%
* Slew Rate (Notes 1, 4, 5 & 8)	+25°C	±100	±120		±80	±120		±80	±120		V/µs
Settling Time (Notes 1, 4, 5 & 8)	+25°C		0.20			0.20			0.20		µs
POWER SUPPLY CHARACTERISTICS											
* Supply Current	+25°C		4	6		4	6		4	6	mA
* Power Supply Rejection Ratio (Note 7)	Full	80	90		74	90		74	90		dB

NOTES:
1. $R_L = 2K$
2. $V_{CM} = \pm 5.0V$
3. $A_V > 10$
4. $V_O = \pm 10.0V$
5. $C_L = 50pF$
6. $V_O = \pm 200mV$
7. $\Delta V = \pm 5.0V$
8. See transient response test circuits and waveforms page four.

*100% Tested For DASH 8

HARRIS
SEMICONDUCTOR
PRODUCTS DIVISION
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HA-2530/2535

High Slew Rate, Wideband Inverting Amplifier

FEATURES

- HIGH SLEW RATE ±320V/μs
- FAST SETTLING TIME 550ns
- WIDE POWER BANDWIDTH 5MHz
- HIGH GAIN BANDWIDTH PRODUCT 70MHz
- LOW OFFSET VOLTAGE 0.8mV
- LOW POWER SUPPLY CURRENT 3.5mA

APPLICATIONS

- PULSE AMPLIFICATION
- SIGNAL CONDITIONING
- SIGNAL GENERATORS
- COAXIAL CABLE DRIVERS
- INTEGRATORS

DESCRIPTION

HA-2530 and HA-2535 are monolithic high speed inverting amplifiers which deliver superior slew rate, bandwidth, and accuracy specifications compared to any other amplifier in its class. Designs of these dielectrically isolated amplifiers utilize the feed forward amplifier technique to produce excellent dynamic and DC specifications coupled with low power consumption. These devices require no external compensation at closed loop gains greater than 10.

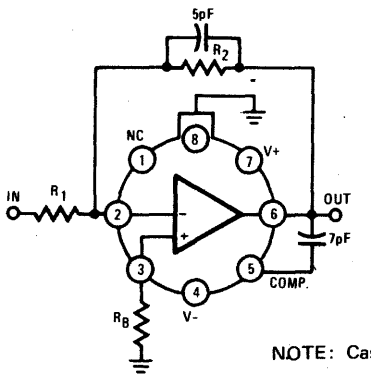
These amplifiers are excellent components for pulse circuits, data acquisition designs, and high speed integrators that can take advantage of the ±320V/μs slew rate and 550ns (0.1%) settling time. 70MHz gain bandwidth product, 5MHz power bandwidth coupled with 0.8mV offset voltage and ±50mA typical output current levels make these amplifiers ideally suited for signal conditioning, signal generation, and coaxial driver applications.

The HA-2530 and HA-2535 are available in metal can (TO-99) packages. HA-2530 is specified over the -55°C to +125°C range while HA-2535 is specified from 0°C to +75°C.

PINOUT

TO-99 **Package Code 2A**

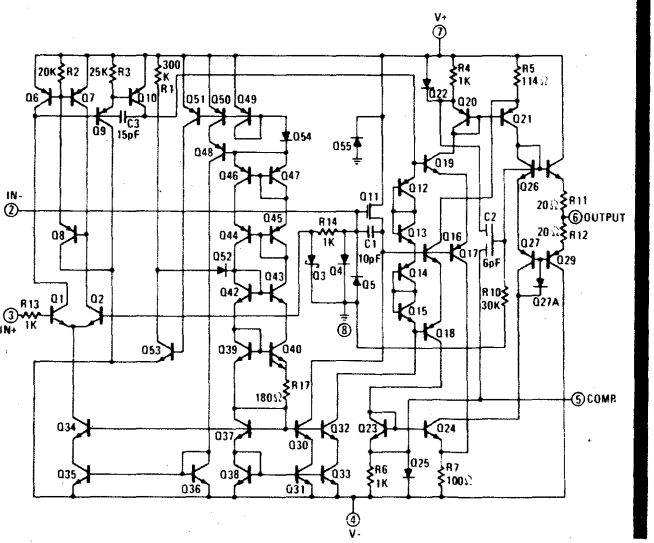
Top View



NOTE: Case tied to V-

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow IC Handling Procedures.

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SEE PAGES 1022-1025 FOR PACKAGE SELECTION GUIDE

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SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Voltage Between V+ and V- Terminals	40V	Internal Power Dissipation (Note 1)	550mW	
		Operating Temperature Range	$-55^{o}C \leq T_A \leq +125^{o}C$	(HA-2530)
Peak Output Current	±100mA		$0^{o}C \leq T_A \leq +75^{o}C$	(HA-2535)
		Storage Temperature Range	$-65^{o}C \leq T_A \leq +150^{o}C$	

ELECTRICAL CHARACTERISTICS

Test Conditions: V_{Supply} = ±15.0V Unless Otherwise Specified.

		HA-2530 -55°C to +125°C			HA-2535 0°C to +75°C			
		LIMITS			LIMITS			
PARAMETER	TEMP.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	UNITS
INPUT CHARACTERISTICS								
* Offset Voltage	+25°C		0.8			0.8		mV
	Full			3			5	mV
Average Offset Voltage Drift	Full		5			5		µV/°C
* Bias Current	+25°C		15			15		nA
	Full			100			200	nA
* Offset Current	+25°C		5			5		nA
	Full			20			20	nA
Input Resistance	+25°C		2			2		MΩ
Input Capacitance	+25°C		10			10		pF
TRANSFER CHARACTERISTICS								
Large Signal Voltage Gain (Notes 2,5)	+25°C		$2X10^6$			$2X10^6$		V/V
*	Full	10^5			10^5			V/V
* Common-Mode Rejection Ratio (Note 3)	Full	86	100		80	100		dB
Gain Bandwidth Product (Note 4)	+25°C		70			70		MHz
OUTPUT CHARACTERISTICS								
* Output Voltage Swing (Note 2)	Full	±10	±12		±10	±12		V
* Output Current (Note 5)	+25°C	±25	±50		±25	±50		mA
Full Power Bandwidth (Note 5)	+25°C	4	5		4	5		MHz
TRANSIENT RESPONSE (NOTES 6&7)								
* Rise Time	+25°C		20	40		20	40	ns
* Overshoot	+25°C		30	45		30	50	%
* Slew Rate	+25°C	±280	±320		±250	±320		V/µs.
Settling Time	+25°C		500			500		ns
POWER SUPPLY CHARACTERISTICS								
* Supply Current	+25°C		3.5	6		3.5	6	mA
* Power Supply Rejection Ratio (Note 8)	Full	86	100		80	100		dB

NOTES:
1. Derate at 5.5mW/°C for Operation at Ambient Temperature Above 75°C.
2. R_L = 2K
3. V_{CM} = ±5.0V
4. A_V >10
5. V_O = ±10V
6. C_L = 50pF
7. See Transient Response Test Circuit and Wave Forms, Page 4.
8. ΔV = ±5.0V

*100% Tested For DASH 8

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HA-2600/2602/2605

Wide Band, High Impedance Operational Amplifier

FEATURES

- WIDE BANDWIDTH — 12MHz
- HIGH INPUT IMPEDANCE — 500MΩ
- LOW INPUT BIAS CURRENT — 1nA
- LOW INPUT OFFSET CURRENT — 1nA
- LOW INPUT OFFSET VOLTAGE — 0.5mV
- HIGH GAIN — 150K V/V
- HIGH SLEW RATE — 7V/μs
- OUTPUT SHORT CIRCUIT PROTECTION

APPLICATIONS

- VIDEO AMPLIFIER
- PULSE AMPLIFIER
- AUDIO AMPLIFIERS AND FILTERS
- HIGH-Q ACTIVE FILTERS
- HIGH-SPEED COMPARATORS
- LOW DISTORTION OSCILLATORS

DESCRIPTION

HA-2600/2602/2605 are internally compensated bipolar operational amplifiers that feature very high input impedance (500 MΩ, HA-2600) coupled with wideband AC performance. The high resistance of the input stage is complemented by low offset voltage (0.5mV, HA-2600) and low bias and offset current (1nA, HA-2600) to facilitate accurate signal processing. Input offset can be reduced further by means of an external nulling potentiometer. 12MHz unity gain-bandwidth product, 7V/μs slew rate and 150,000V/V open-loop gain enables HA-2600/2602/2605 to perform high-gain amplification of fast, wideband signals. These dynamic characterisitics, coupled with fast settling times, make these amplifiers ideally suited to pulse amplification designs as well as high frequency (e.g. video) applications. The frequency response of the amplifier can be tailored to exact design requirements by means of an external bandwidth control capacitor.

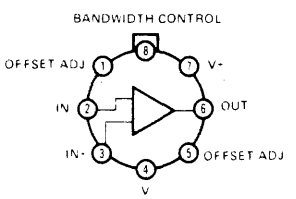
In addition to its application in pulse and video amplifier designs, HA-2600/2602/2605 is particularly suited to other high performance designs such as high-gain low distortion audio amplifiers, high-Q and wideband active filters and high-speed comparators.

HA-2600 and HA-2602 are guaranteed over -55°C to +125°C. HA-2605 is specified from 0°C to +75°C. All devices are available in TO-99 cans, and HA-2600/2602 are available in 10 lead flat packages.

PINOUT

TO-99 TOP VIEW

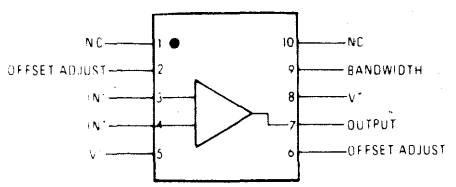
Package Code 2A



Case Connected to V-

TO-91 TOP VIEW

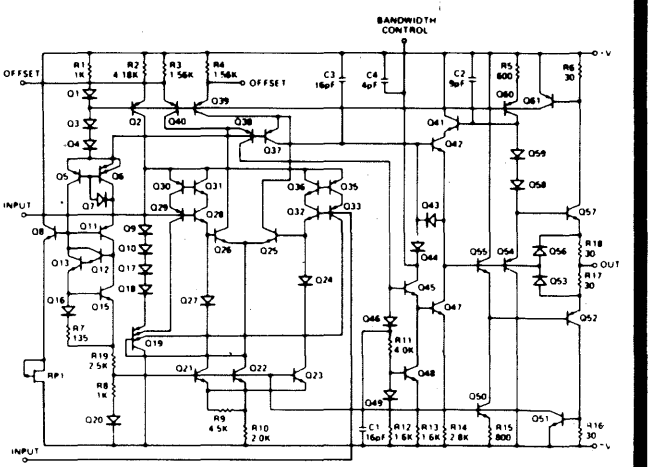
Package Code 9V
(HA-2600/2602 Only)



Case Connected to V-

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow IC Handling Procedures.

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ABSOLUTE MAXIMUM RATINGS

Voltage Between V^+ and V^- Terminals	45.0V
Differential Input Voltage	±12.0V
Peak Output Current	Full Short Circuit Protection
Internal Power Dissipation	300mW
Operating Temperature Range – HA-2600/HA-2602	$-55^oC \leq T_A \leq +125^oC$
HA-2605	$0^o \leq T_A \leq +75^oC$
Storage Temperature Range	$-65^oC \leq T_A \leq +150^oC$

ELECTRICAL CHARACTERISTICS V+=+15VDC, V- = -15VDC

PARAMETER	TEMP.	HA-2600 −55°C to +125°C LIMITS MIN.	HA-2600 TYP.	HA-2600 MAX.	HA-2602 −55°C to +125°C LIMITS MIN.	HA-2602 TYP.	HA-2602 MAX.	HA-2605 0°C to +75°C LIMITS MIN.	HA-2605 TYP.	HA-2605 MAX.	UNITS
INPUT CHARACTERISTICS											
* Offset Voltage	+25°C		0.5	4		3	5		3	5	mV
	Full		2	6			7			7	mV
Offset Voltage Average Drift	Full		5								µV/°C
* Bias Current	+25°C		1	10		15	25		5	25	nA
	Full		10	30			60			40	nA
* Offset Current	+25°C		1	10		5	25		5	25	nA
	Full		5	30			60			40	nA
Input Resistance	+25°C	100	500		40	300		40	300		MΩ
Common Mode Range	Full	±11.0			±11.0			±11.0			V
TRANSFER CHARACTERISTICS											
* Large Signal Voltage Gain (Notes 1, 4)	+25°C	100K	150K		80K	150K		80K	150K		V/V
	Full	70K			60K			70K			V/V
* Common Mode Rejection Ratio (Note 2)	Full	80	100		74	100		74	100		dB
Unity Gain Bandwidth (Note 3)	+25°C		12			12			12		MHz
OUTPUT CHARACTERISTICS											
Output Voltage Swing (Note 1)	Full	±10.0	±12.0		±10.0	±12.0		±10.0	±12.0		V
* Output Current (Note 4)	+25°C	±15	±22		±10	±18		±10	±18		mA
Full Power Bandwidth (Note 4)	+25°C	50	75		50	75		50	75		kHz
TRANSIENT RESPONSE											
Rise Time (Notes 1, 5, 6 & 8)	+25°C		30	60		30	60		30	60	ns
Overshoot (Notes 1, 5, 7 & 8)	+25°C		25	40		25	40		25	40	%
* Slew Rate (Notes 1, 4, 5 & 8)	+25°C	±4	±7		±4	±7		±4	±7		V/µs
Settling Time (Notes 1, 4, 5 & 8)	+25°C		1.5			1.5			1.5		µs
POWER SUPPLY CHARACTERISTICS											
* Supply Current	+25°C		3.0	3.7		3.0	4.0		3.0	4.0	mA
* Power Supply Rejection Ratio (Note 9)	Full	80	90		74	90		74	90		dB

TEST CONDITIONS

NOTES:
1. R_L = 2K
2. V_{CM} = ±5.0V
3. V_O < 90mV
4. V_O = ±10V
5. C_L = 100pF
6. V_O = ±200mV
7. V_O = ±400mV
8. See Transient response test circuits and waveforms page three.
9. V_S = ±9.0V to ±15V

*100% Tested For DASH 8

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HARRIS SEMICONDUCTOR PRODUCTS DIVISION
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HA-2607/2627

Epoxy-Packaged, Wide Band Operational Amplifier Series

Preliminary

FEATURES

	HA-2607	HA-2627	
● Wide Gain-Bandwidth	12	100	MHz
● High Slew Rate	7	35	V/μ S
● Wide Power Bandwidth	75	600	KHz
● High Gain	150KV/V		
● High Input Impedance	500M Ω		
● Output Short Circuit Protection			

APPLICATIONS

- Pulse Amplification
- Video Amplifiers
- Audio Amplifiers and Filters
- High Speed Test Equipment
- High Speed Comparators

DESCRIPTION

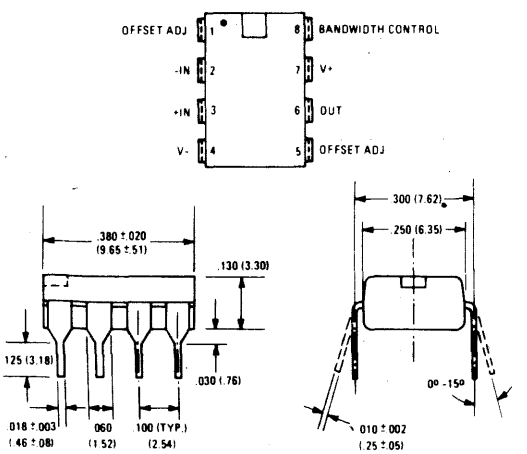
HA-2607/2627 bipolar operational amplifiers are high performance, epoxy-packaged monolithic IC's designed to deliver outstanding wideband AC performance. HA-2607 has a specified bandwidth of 12MHz while HA-2627 has a typical gain-bandwidth of 100MHz!* HA-2607 and HA-2627 also offer correspondingly high slew rates of 7V/μ Sec and 35V/μ Sec respectively. These dynamic characteristics, coupled with 150,000V/V open-loop gain enables HA-2607/2627 to perform high-gain amplification of very fast, wideband signals. This level of performance is achieved through the use of Harris' unique Dielectric Isolation processing techniques.

The HA-2607 and HA-2627 op amps afford an economical means of designing high performance equipment for industrial and commercial use. These amplifiers are ideally suited to pulse amplification designs as well as high frequency (e.g. RF, video) applications. The frequency response of both amplifiers can be tailored to exact design requirements by means of an external bandwidth control capacitor.

HA-2607/2627 are specified from 0°C to +75°C and are available in 8-lead epoxy DIP packages that have been extensively tested and qualified to deliver the high level of performance and reliability that are expected of Harris Semiconductor's operational amplifiers.

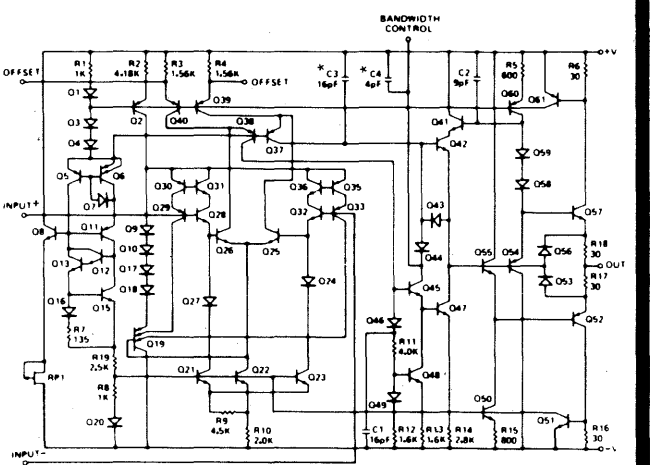
*HA-2607/2627 are internally compensated – HA-2607 is stable for $A_V \geq 1$, – HA- 2627 is stable for $A_V \geq 5$.

PINOUT



8 LEAD D.I.P. EPOXY

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*VALUES OF C3 AND C4 VARY DEPENDING ON DEVICE TYPE.

SEE PAGES 1022-1025 FOR PACKAGE SELECTION GUIDE

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ABSOLUTE MAXIMUM RATINGS

Voltage Between V^+ and V^- Terminals	45.0V
Differential Input Voltage	±12.0V
Peak Output Current	Full Short Circuit Protection
Internal Power Dissipation (Note 10)	300mW
Operating Temperature Range – HA-2607/HA-2627	$0^o \leq T_A \leq +75^oC$
Storage Temperature Range	$-65^oC \leq T_A \leq +150^oC$

ELECTRICAL CHARACTERISTICS

V+=+15VDC, V-= -15VDC

		HA-2607 0°C to +75°C LIMITS			HA-2627 0°C to +75°C			
PARAMETER	TEMP.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	UNITS
INPUT CHARACTERISTICS								
Offset Voltage	+25°C		4	6		4	6	mV
	Full			8			8	mV
Offset Voltage Average Drift	Full		5			5	30	nA
Bias Current	+25°C		5	30		5	30	nA
	Full			50			50	
Offset Current	+25°C		5	30		5	30	nA
	Full			50			50	nA
Input Resistance	+25°C	40	300		40	300		MΩ
Common Mode Range	Full	±10.0			±10.0			V
TRANSFER CHARACTERISTICS								
Large Signal Voltage Gain (Note 1)	+25°C	70	150K		70	150K		V/V
	Full	60			60			V/V
Common Mode Rejection Ratio (Note 2)	Full	74	100		74	100		dB
Gain Bandwidth Product (Note 3, 11)	+25°C		12			100		MHz
OUTPUT CHARACTERISTICS								
Output Voltage Swing (Note 1)	Full	±10.0	±12.0		±10.0	±12.0		V
Output Current (Note 4)	+25°C	±10	±18		±10	±18		mA
Full Power Bandwidth (Note 4)	+25°C	50	75		290	600		kHz
TRANSIENT RESPONSE								
Rise Time (Notes 1, 5, 6 & 8)	+25°C		30	60		17	45	ns
Overshoot (Notes 1, 5, 7 & 8)	+25°C		25	40		25	40	%
Slew Rate (Notes 1, 4, 5 & 8)	+25°C	±4	±7		±17	±35		V/μs
Settling Time (Notes 1, 4, 5 & 8)	+25°C		1.5			1.5		μs
POWER SUPPLY CHARACTERISTICS								
Supply Current	+25°C		3.0	4.0		3.0	4.0	mA
Power Supply Rejection Ratio (Note 9)	Full	74	90		74	90		dB

TEST CONDITIONS.

NOTES:
1. R_L = 2K
2. V_{CM} = + 5.0V
3. V_O < 90mV
4. V_O = + 10V
5. C_L = 100pF
6. V_L = + 200mV
7. V_O = + 400mV
8. For HA-2607, A_V = 1; For HA-2627, A_V = 5.
9. V_S = + 9.0V to +15V
10. Derate by 6.6mW/°C above 105°C
11. 40 dB gain setting used to measure Gain-Band width for HA-2627

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HARRIS SEMICONDUCTOR PRODUCTS DIVISION
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HA-2620/2622/2625

Very Wide Band, Uncompensated Operational Amplifiers

FEATURES

- GAIN BANDWIDTH PRODUCT(A_V = 5) 100MHz
- HIGH INPUT IMPEDANCE 500MΩ
- LOW INPUT BIAS CURRENT 1nA
- LOW INPUT OFFSET CURRENT 1nA
- LOW INPUT OFFSET VOLTAGE 0.5mV
- HIGH GAIN 150K V/V
- HIGH SLEW RATE 35V/μs
- OUTPUT SHORT CIRCUIT PROTECTION

APPLICATIONS

- VIDEO AND R.F. AMPLIFIERS
- PULSE AMPLIFIER
- AUDIO AMPLIFIERS AND FILTERS
- HIGH-Q ACTIVE FILTERS
- HIGH-SPEED COMPARATORS
- LOW DISTORTION OSCILLATORS

DESCRIPTION

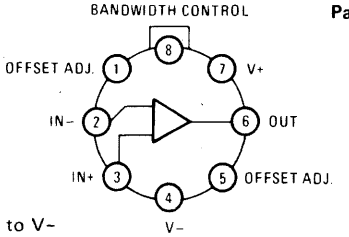
HA-2620/2622/2625 are bipolar operational amplifiers that feature very high input impedance (500MΩ. HA-2620) coupled with wideband AC performance. The high resistance of the input stage is complemented by low offset voltage (0.5mV, HA-2620) and low bias and offset current (1nA, HA-2620) to facilitate accurate signal processing. Input offset can be reduced further by means of an external nulling potentiometer. 100MHz gain-bandwidth product (HA-2620/2622/2625 are stable for closed loop gains greater than 5), 35V/ μs slew rate and 150,000V/V open-loop gain enables HA-2620/2622/2625 to perform high-gain amplification of very fast, wideband signals. These dynamic characterisitcs, coupled with fast settling times, make these amplifiers ideally suited to pulse amplification designs as well as high frequiency (e.g. video) applications. The frequency response of the amplifier can be tailored to exact design requirements by means of an external bandwidth control capacitor.

In addition to its application in pulse and video amplifier designs HA-2620/2622/2625 is particularly suited to other high performance designs such as high-gain low distortion audio amplifiers, high-Q and wideband active filters and high-speed comparators.

HA-2620 and HA-2622 are guaranteed over -55°C to +125°C. HA-2625 is specified from 0°C to +75°C. All devices are available in TO-99 cans, and 14 lead D.I.P. packages.

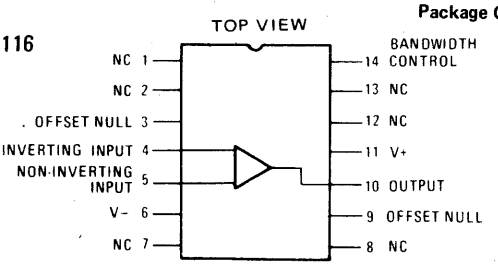
PINOUT

TO-99 — TOP VIEW — Package Code 2A



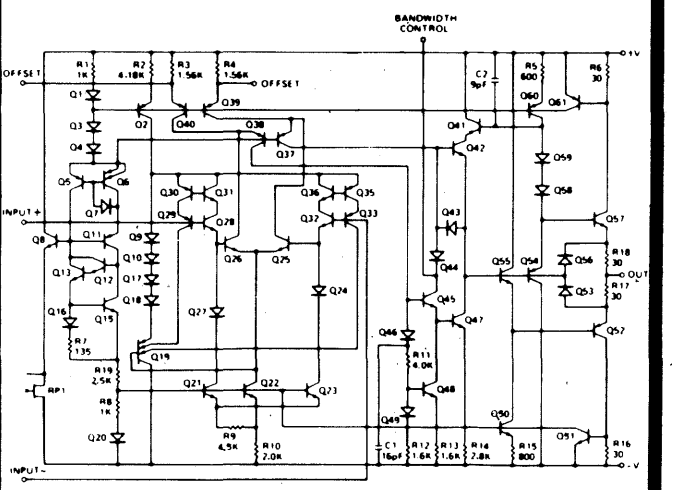
Case Connected to V-

TO-116 — TOP VIEW — Package Code 4U



Case Connected to V-

SCHEMATIC



SEE PAGES 1022-1025 FOR PACKAGE SELECTION GUIDE

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SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Voltage Between V^+ and V^- Terminals	45.0V
Differential Input Voltage	±12.0V
Peak Output Current	Full Short Circuit Protection
Internal Power Dissipation	300mW
Storage Temperature Range	$-65^oC \leq T_A \leq +150^oC$

ELECTRICAL CHARACTERISTICS

$V^+ = +15$ VDC, $V^- = -15$ VDC

PARAMETER	TEMPERATURE	HA-2620 −55°C to +125°C MIN.	HA-2620 TYP.	HA-2620 MAX.	HA-2622 −55°C to +125°C MIN.	HA-2622 TYP.	HA-2622 MAX.	HA-2625 0°C to +75°C MIN.	HA-2625 TYP.	HA-2625 MAX.	UNITS
INPUT CHARACTERISTICS											
* Offset Voltage (Note 1)	+25°C		0.5	4		3	5		3	5	mV
	Full			6			7			7	mV
* Bias Current	+25°C		1	15		5	25		5	25	nA
	Full		10	35			60			40	nA
* Offset Current	+25°C		1	15		5	25		5	25	nA
	Full		5	35			60			40	nA
Input Resistance	+25°C	65	500		40	300		40	300		MΩ
Common Mode Range	Full	±11.0			±11.0			±11.0			V
TRANSFER CHARACTERISTICS											
* Large Signal Voltage Gain (Notes 2 & 3)	+25°C	100K	150K		80K	150K		80K	150K		V/V
	Full	70K			60K			70K			V/V
* Common Mode Rejection Ratio (Note 4)	Full	80	100		74	100		74	100		dB
Gain Bandwidth Product (Notes 2, 5, &6)	+25°C		100			100			100		MHz
OUTPUT CHARACTERISTICS											
Output Voltage Swing (Note 2)	Full	±10.0	±12.0		±10.0	±12.0		±10.0	±12.0		V
* Output Current (Note 3)	+25°C	±15	±22		±10	±18		±10	±18		mA
Full Power Bandwidth (Notes 2, 3 & 7)	+25°C	400	600		320	600		320	600		kHz
TRANSIENT RESPONSE											
Rise Time (Notes 2, 5, 7 & 8)	+25°C		17	45		17	45		17	45	ns
* Slew Rate (Notes 2, 7, 8 & 10)	+25°C	±25	±35		± 20	±35		± 20	±35		V/μs
POWER SUPPLY CHARACTERISTICS											
* Supply Current	+25°C		3.0	3.7		3.0	4.0		3.0	4.0	mA
* Power Supply Rejection Ratio (Note 9)	Full	80	90		74	90		74	90		dB

NOTES:
1. Offset may be externally adjusted to zero.
2. $R_L = 2K\Omega$, $C_L = 50pF$
3. $V_O = \pm 10.0V$
4. $V_{CM} = \pm 5.0V$
5. $V_O < 90mV$
6. 40dB Gain
7. See transient response test circuits and waveforms page 3.
8. $A_V = 5.0V$ (The HA-2620 family is not stable at unity gain without external compensation.)
9. $V_{Sup} = \pm 9.0V$ to $\pm 15.0V$
10. $V_O = 5.0V$

*100% Tested For DASH 8

SEE PAGES 1022-1025 FOR PACKAGE SELECTION GUIDE

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HA-2630/2635

High Performance Current Booster

FEATURES

- OUTPUT CURRENT ±400mA
- SLEW RATE 500V/μs
- BANDWIDTH 8MHz
- FULL POWER BANDWIDTH 8MHz
- INPUT RESISTANCE $2.0 \times 10^6 \Omega$
- OUTPUT RESISTANCE 2.0Ω
- POWER SUPPLY RANGE ±5V to ±20V
- PACKAGE IS ELECTRICALLY ISOLATED

APPLICATIONS

- COAXIAL CABLE DRIVERS
- AUDIO OUTPUT AMPLIFIERS
- SERVO MOTOR DRIVERS
- POWER SUPPLIES (BIPOLAR)
- PRECISION DATA RECORDING

DESCRIPTION

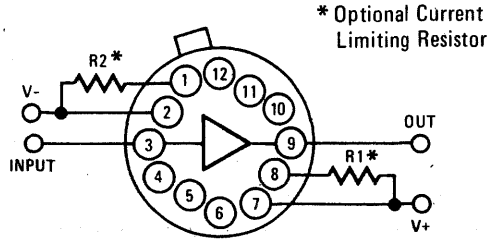
HA-2630 and HA-2635 are monolithic, unity voltage gain current amplifiers delivering extremely high slew rate, wide bandwidth, and full power bandwidth even under heavy output loading conditions. This dielectrically isolated current booster also offers high input impedance and low output resistance. These devices are intended to be used in series with an operational amplifier and inside the feedback loop whenever additional output current is required. Output current levels are programmable by selecting two optional external resistors.

These current amplifiers offer an exceptional 500V/μs slew rate and 8MHz bandwidth which allows them to be used with many high performance op amps in precision data recording and high speed coaxial cable driver designs. 2.0M ohm input resistance and 2 ohm output resistance coupled with ±400mA output current make HA-2630 and HA-2635 ideal components in high fidelity audio output amplifier designs.

HA-2630 and HA-2635 are available in an electrically isolated TO-8 type can for ease of mounting with or without a heat sink. HA-2630 is specified over the -55°C to +125°C range. HA-2635 is specified from 0°C to +75°C.

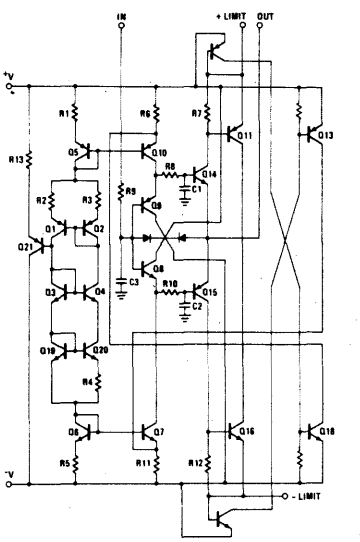
PINOUT

TO-8 **Package Code 2G**



Top View

SCHEMATIC



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow IC Handling Procedures.

SEE PAGES 1022-1025 FOR PACKAGE SELECTION GUIDE

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ABSOLUTE MAXIMUM RATINGS

Voltage Between V+ and V- Terminals	40V
Input Voltage Range	± V Supply
Output Current (Note 2)	±700mA
Internal Power Dissipation (Note 6) Free Air:	1W
In Heat Sink:	4W

Operating Temperature Range:
$-55^{o}C \leq T_A \leq +125^{o}C$ (HA-2630)
$0^{o}C \leq T_A \leq +75^{o}C$ (HA-2635)
Storage Temperature Range:
$-65^{o}C \leq T_A \leq +150^{o}C$

ELECTRICAL CHARACTERISTICS

$V_{Supply} = \pm 15$ Volts $R_L = 50$ Ohms $R_1 = R_2 = 0$ Ohms Unless otherwise specified.

PARAMETER	TEMP.	HA-2630 -55°C to +125°C MIN.	HA-2630 TYP.	HA-2630 MAX.	HA-2635 0°C to +75°C MIN.	HA-2635 TYP.	HA-2635 MAX.	UNITS
INPUT CHARACTERISTICS								
*Bias Current	+25°C		30	150		30	150	µA
	Full			200			200	µA
Input Resistance	+25°C		2.0			2.0		MΩ
Input Capacitance	+25°C		5.0			5.0		pF
TRANSFER CHARACTERISTICS								
Voltage Gain (Note 1)	Full	.85	.95		.85	.95		V/V
*Offset Voltage ($V_{OUT} - V_{IN}$)	+25°C		70	±200		70	±200	mV
	Full			±300			±300	mV
Bandwidth (-3dB)	+25°C		8.0			8.0		MHz
OUTPUT CHARACTERISTICS								
*Output Voltage Swing	Full	±10			±10			V
*Output Current (Note 1)	Full	±300	±400		±300	±400		mA
Output Resistance	+25°C		2.0			2.0		Ω
Full Power Bandwidth (Note 1)	+25°C		8.0			8.0		MHz
TRANSIENT RESPONSE								
Rise Time (Note 3)	+25°C		30			30		ns
Slew Rate (Note 4)	+25°C	200	500		200	500		V/µs
POWER SUPPLY CHARACTERISTICS								
*Supply Current	Full		15	20		15	23	mA
Supply Voltage Range	Full	±5		±20	±5		±20	V
Power Supply Rejection Ratio (Note 5)	Full		66			66		dB

NOTES:
1. $V_O = \pm 10V$
2. Heat sink is required for continuous short circuit protection, regardless of current limit setting.
3. $V_O = 0.4V$ p-p.
4. $V_O = 10V$ p-p.
5. $\Delta V_{SUPPLY} = \pm 5V$.
6. Without heat sink, derate by 14mW/°C ambient temperature above 100°C ambient, with heat sink, derate by 67mW/°C case temperature above 115°C case.

*100% Tested For DASH 8

HARRIS
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HA-2640/2645

High Voltage Operational Amplifier

FEATURES

- OUTPUT VOLTAGE SWING ±35V
- SUPPLY VOLTAGE ±10V TO ±40V
- OFFSET CURRENT 5nA
- BANDWIDTH 4MHz
- SLEW RATE 5V/μs
- COMMON MODE INPUT VOLTAGE SWING ±35V
- OUTPUT OVERLOAD PROTECTION

APPLICATIONS

- INDUSTRIAL CONTROL SYSTEMS
- POWER SUPPLIES
- HIGH VOLTAGE REGULATORS
- RESOLVER EXCITATION
- SIGNAL CONDITIONING

DESCRIPTION

HA-2640 and HA-2645 are monolithic operational amplifiers which are designed to deliver unprecedented dynamic specifications for a high voltage internally compensated device. These dielectrically isolated devices offer very low values for offset voltage and offset current coupled with large output voltage swing and common mode input voltage.

For maximum reliability, these amplifiers offer unconditional output overload protection through current limiting and a chip temperature sensing circuit. This sensing device turns the amplifier "off", when the chip reaches a certain temperature level.

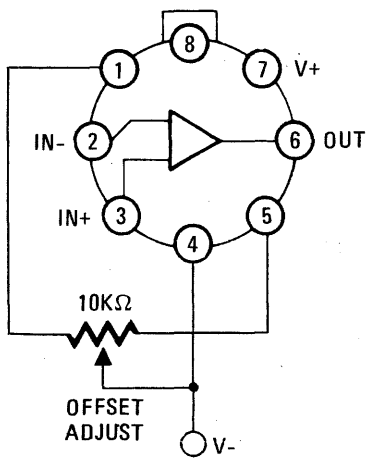
These amplifers deliver ±35V common mode input voltage swing, ±35V output voltage swing, and up to ±40V supply range for use in such designs as regulators, power supplies, and industrial control systems. 4MHz gain bandwidth and 5V/μs slew rate make these devices excellent components for high performance signal conditioning applications. Outstanding input and output voltage swings coupled with a low 5nA offset current make these amplifiers excellent components for resolver excitation designs.

HA-2640 and HA-2645 are available in metal can (TO-99) packages and can be used as high performance pin-to-pin replacements for many general purpose op amps. HA-2640 is specified from -55°C to +125°C and HA-2645 is specified over the 0°C to +75°C range.

PINOUT

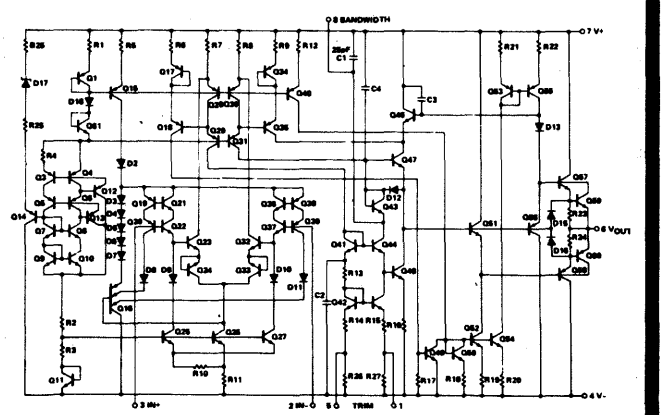
TO-99 **Package Code 2A**

Top View



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow IC Handling Procedures.

SCHEMATIC



SEE PAGES 1022-1025 FOR PACKAGE SELECTION GUIDE

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ABSOLUTE MAXIMUM RATINGS

Voltage Between V+ and V- Terminals 100V
Input Voltage Range ±37V
Output Current/Full Short Circuit Protection
Internal Power Dissipation 680mW*

*Derate by 4.6mW/°C above +25°C

Operating Temperature Range
$-55^{\circ}C \leq T_A \leq +125^{\circ}C$ (HA-2640)
$0^{\circ}C \leq T_A \leq +75^{\circ}C$ (HA-2645)
Storage Temperature Range
$-65^{\circ}C \leq T_A \leq +150^{\circ}C$

ELECTRICAL CHARACTERISTICS

$V_{Supply} = \pm 40V$, $R_L = 5K$, Unless Otherwise Specified.

PARAMETER	TEMP.	HA-2640 -55°C to +125°C MIN.	HA-2640 -55°C to +125°C TYP.	HA-2640 -55°C to +125°C MAX.	HA-2645 0°C to +75°C MIN.	HA-2645 0°C to +75°C TYP.	HA-2645 0°C to +75°C MAX.	UNITS
INPUT CHARACTERISTICS								
* Offset Voltage	+25°C		2	4		2	6	mV
	Full			6			7	mV
Offset Voltage Average Drift	Full		15			15		µV/°C
* Bias Current	+25°C		10	25		12	30	nA
	Full			50			50	nA
* Offset Current	+25°C		5	12		15	30	nA
	Full			35			50	nA
Input Resistance	+25°C	50	250		40	200		MΩ
Common Mode Range	Full	±35			±35			V
TRANSFER CHARACTERISTICS								
* Large Signal Voltage Gain (Note 8)	+25°C	100K	200K		100K	200K		V/V
	Full	75K			75K			V/V
* Common Mode Rejection Ratio (Note 1)	Full	80	100		74	100		dB
Unity Gain Bandwidth (Note 2)	+25°C		4			4		MHz
OUTPUT CHARACTERISTICS								
* Output Voltage Swing	Full	±35			±35			V
* Output Current (Note 9)	+25°C	±12	±15		±10	±12		mA
Output Resistance	+25°C		500			500		Ω
Full Power Bandwidth (Note 3)	+25°C		23			23		kHz
TRANSIENT RESPONSE (Note 7)								
Rise Time (Notes 4, 6)	+25°C		60			60		ns
Overshoot (Notes 4, 6)	+25°C		15			15		%
Slew Rate (Note 6)	+25°C		5			5		V/µs
POWER SUPPLY CHARACTERISTICS								
* Supply Current	+25°C		3.2	3.8		3.2	4.5	mA
Supply Voltage Range	Full	±10		±40	±10		±40	V
* Power Supply Rejection Ratio (Note 5)	Full	80	90		74	90		dB

*100% Tested For DASH 8

NOTES: 1. $V_{CM} = \pm 30V$
2. $V_O = 90mV$
3. $V_O = \pm 35V$
4. $V_O = \pm 200mV$
5. $V_S = \pm 10V$ to $\pm 40V$
6. $A_V = 1$
7. $C_L = 50pF$
8. $\Delta V_O =$
9. $R_L = 1K\Omega$

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HA-2650/2655

Dual High Performance Operational Amplifier

FEATURES

• SLEW RATE	5V/μs
• BANDWIDTH	8MHz
• BIAS CURRENT	35nA
• AV. OFFSET VOLTAGE DRIFT	8μV/°C
• POWER CONSUMPTION	75mW
• SUPPLY VOLTAGE RANGE	±2V TO ±20V

APPLICATIONS

- VIDEO AMPLIFIERS
- HIGH IMPEDANCE, WIDEBAND BUFFERS
- INTEGRATORS
- AUDIO AMPLIFIERS
- ACTIVE FILTERS

DESCRIPTION

HA-2650/2655 contains two internally compensated operational amplifiers offering high slew rate and high frequency performance combined with exceptional DC characteristics. 5V/μ sec slew rate and 8MHz bandwidth make these amplifiers suitable for processing fast, wideband signals extending into the video frequency spectrum. Signal processing accuracy is enhanced by front-end performance that includes 1.5mV offset voltage, 8 μ V/°C offset voltage drift and low offset and bias current (1nA and 35nA respectively). Offset voltage can be trimmed to zero on the devices offered in dual-in-line packages. Signal conditioning is further enhanced by 500MΩ input impedance.

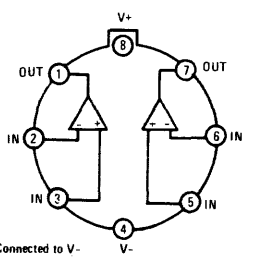
Applications for HA-2650/2655 include video circuit designs such as high impedance buffers, integrators, tone generators and filters. These amplifiers are also ideal components for active filtering of audio and voice signals.

HA-2650/2655 are offered in 14 pin D.I.P. and metal TO-99 packages and are also available in dice form. HA-2650 is specified from -55°C to +125°C. HA-2655 operates from 0°C to +75°C.

PINOUT

TO-99 — Package Code 2A

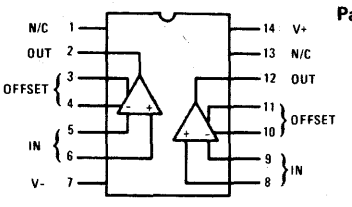
TOP VIEW



NOTE: Case Connected to V-

TO-116 — Package Code 4U

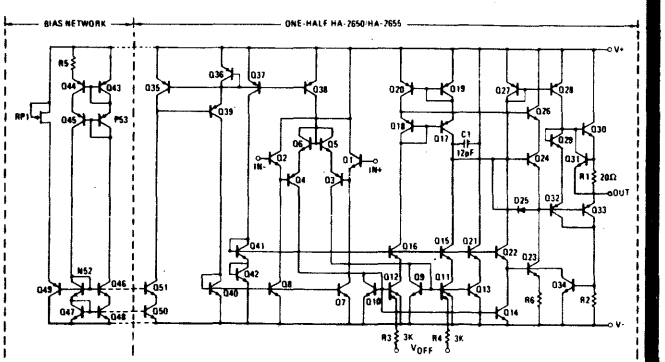
TOP VIEW



NOTE: Bottom of package is connected to V-.

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow IC Handling Procedures.

SCHEMATIC



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SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

T_A = +25°C Unless Otherwise Stated

Voltage Between V+ and V- Terminals	40.0V
Differential Input Voltage	±30.0V
Input Voltage (Note 1)	±15.0V
Output Short Circuit Duration	Indefinite

Power Dissipation (Note 2)	TO-99	300 mW
	TO-116	300 mW
Operating Temperature Range:		
HA-2650	$-55^oC \leq T_A \leq +125^oC$	
HA-2655	$0^oC \leq T_A \leq +75^oC$	
Storage Temperature Range	$-65^oC \leq T_A \leq +150^oC$	

ELECTRICAL CHARACTERISTICS

V+ = 15V V- = -15V

PARAMETER	TEMP.	HA-2650 -55°C to +125°C MIN.	HA-2650 TYP.	HA-2650 MAX.	HA-2655 0°C to +75°C MIN.	HA-2655 TYP.	HA-2655 MAX.	UNITS
INPUT CHARACTERISTICS								
*Offset Voltage	+25°C		1.5	3		2	5	mV
	Full			5			7	mV
Av. Offset Voltage Drift	Full		8			8		µV/°C
*Bias Current	+25°C		35	100		50	200	nA
	Full			200			300	nA
*Offset Current	+25°C		1	30		2	60	nA
	Full			60			100	nA
Common Mode Range	Full	±13			±13			V
Differential Input Resistance	+25°C	5	20		5	20		MΩ
Common Mode Input Resistance	+25°C		500			500		MΩ
Input Capacitance	+25°C		5			5		pF
TRANSFER CHARACTERISTICS								
*Large Signal Voltage Gain (Note 3ab)	+25°C	25K	40K		20K	40K		V/V
	Full	20K			15K			V/V
*Common Mode Rejection Ratio (Note 4)	+25°C	80	100		74	100		dB
	Full	80			74			dB
OUTPUT CHARACTERISTICS								
*Output Voltage Swing (Note 3c)	+25°C	±13	±14		±13	±14		V
	Full	±13			±13			V
Full Power Bandwidth (Note 5)	+25°C	30	80		30	80		KHz
Output Current (Note 3a)	+25°C		±20			±18		mA
Output Resistance	+25°C		100			100		Ω
TRANSIENT RESPONSE (Note 6)								
Rise Time (Note 7)	+25°C		40			40		ns
Overshoot (Note 7)	+25°C		15			15		%
Slew Rate	+25°C	±2	±5		±2	±5		V/µs
POWER SUPPLY CHARACTERISTICS								
*Supply Current	+25°C		2.5	3		3	4	mA
*Power Supply Rejection Ratio (Note 8)	+25°C	80	100		74	100		dB
	Full	80			74			dB

NOTES:
1. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
2. Derate at 4.7mW/°C at ambient temperatures above +110°C.
3. (a) V_O = ±10V (b) R_L = 2K (c) R_L = 10K
4. V_{CM} = ±5.0V
5. A_V = 1, R_L = 2K, V_O = $20V_{pp}$
6. See transient response/slew rate circuit.
7. V_{in} = 200mV
8. Δ V = ±5.0V

*100% Tested For DASH 8

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HA-2700/2704/2705

Low Power, High Performance Operational Amplifiers

FEATURES

- LOW POWER DISSIPATION — 2.24mW AT ±15.0V
- HIGH SLEW RATE — 20V/μs
- HIGH OPEN LOOP GAIN — 300K(R_L = 2KΩ)
- LOW INPUT BIAS CURRENT — 5nA
- LOW OFFSET VOLTAGE — 0.5mV
- HIGH CM_{rr} — 106dB
- WIDE POWER SUPPLY RANGE — ±5.5V TO ±20.0V

APPLICATIONS

- HIGH GAIN AMPLIFIER
- INSTRUMENTATION AMPLIFIERS
- ACTIVE FILTERS
- TELEMETRY SYSTEMS
- BATTERY-POWERED EQUIPMENT

DESCRIPTION

HA-2700/2704/2705 are ihternally compensated operational amplifiers which employ dielectric isolation to achieve excellent DC and dynamic performance with very low quiescent power consumption.

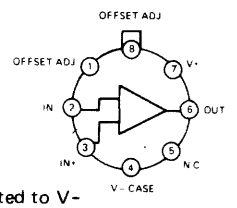
DC performance of the amplifier input is characterized by high CMRR (106dB), low offset voltage (0.5mV, HA-2700 and HA-2704; 1mV, HA-2705) along with low bias and offset current (5.0nA and 2.5nA respectively). These input specifications, in conjunction with offset null capability and open-loop gain of 300,000V/V, enable HA-2700/2704/2705 to provide accurate, high-gain signal amplification. Gain bandwidth 1MHz and slew rate of 20V/μs allow for processing of fast, wideband signals. Input and output signal amplitudes of at least ±11 volts can be accomodated while providing output drive capability of 10mA. For maximum reliability, the output is protected in the event of short circuits to ground.

These amplifiers operate from a wide range of supplies (±5.5V to ±20V) with a maximum quiescent supply drain of only 150μA. HA-2700/2704/2705 are, therefore, ideally suited to low-power instrumentation and filtering applications that require fast, accurate response over a wide range of signal frequency.

These amplifers are available in three performance grades: HA-2700 is rated for operation from -55°C to +125°C; HA-2704 is specified over -25°C to +85°C; HA-2705 is specified from 0°C to +75°C. All three devices are available in TO-99 cans or 14 lead D.I.P. packages.

PINOUT

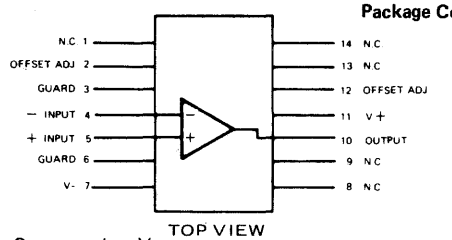
TO-99 — **Package Code 2A**



Case Connected to V-

TOP VIEW

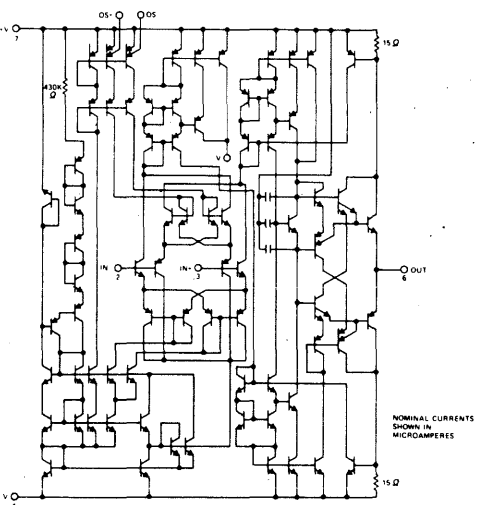
TO-116 — **Package Code 4U**



Case Connected to V-

TOP VIEW

SCHEMATIC



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow IC Handling Procedures.

SEE PAGES 1022-1025 FOR PACKAGE SELECTION GUIDE

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ABSOLUTE MAXIMUM RATINGS

Voltage Between V^+ and V^- Terminals	44.0V
Differential Input Voltage	±18.0V
Internal Power Dissipation (Note 7)	300mW
Storage Temperature	$-65^oC \leq T_A \leq +150^oC$

ELECTRICAL CHARACTERISTICS

$V^+ = +15.0$ V.D.C. $V^- = -15.0$ V.D.C.

PARAMETER	TEMP.	HA-2700 −55°C to +125°C			HA-2704 −25°C to +85°C			HA-2705 0°C to +75°C			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
INPUT CHARACTERISTICS											
* Offset Voltage (Note 1)	+25°C		0.5	3.0		0.5	3.0		1.0	5.0	mV
	Full			5.0			6.0			7.0	mV
* Bias Current	+25°C		5.0	20.0		5.0	20.0		5.0	40.0	nA
	Full			50.0			50.0			70.0	nA
* Offset Current	+25°C		2.5	10.0		2.5	10.0		2.5	15.0	nA
	Full			30.0			30.0			40.0	nA
Common Mode Range	Full	±11.0			±11.0			±11.0			V
TRANSFER CHARACTERISTICS											
* Large Signal Voltage Gain (Notes 2 & 3)	+25°C	200K	300K		200K	300K		200K	300K		V/V
	Full	100K			100K			100K			V/V
* Common Mode Rejection Ratio (Note 4)	Full	86	106		86	106		80	106		dB
Gain Bandwidth Product (Note 2)	+25°C		1.0			1.0			1.0		MHz
OUTPUT CHARACTERISTICS											
Output Voltage Swing (Note 2)	+25°C	±12.0	±13.0		±12.0	±13.0		±12.0	±13.0		V
	Full	±11.0			±11.0			±11.0			V
Output Current (Note 3)	+25°C		10			10			10		mA
TRANSIENT RESPONSE CHARACTERISTICS											
* Slew Rate (Notes 2 & 6)	+25°C	10	20		10	20		10	20		V/µs
POWER SUPPLY CHARACTERISTICS											
* Supply Current	+25°C		75	150		75	150		75	150	µA
* Power Supply Rejection Ratio (Note 5)	Full	86	100		86	100		80	100		dB

NOTES:
1. Can be adjusted to zero with 1 megohm pot between Pins 1 and 8 with the tap to Pin 7.
2. $R_L = 2K$, $C_L = 100pF$
3. $V_O = \pm 10.0V$
4. $V_{CM} = \pm 5.0V$
5. $V_S = \pm 10.0V$ to $\pm 20.0V$
6. $A_V = 5$
7. Derate by 6.6 mW/°C above 105°C.

*100% Tested For DASH 8

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HA-2720/25

Wide Range Programmable Operational Amplifier

FEATURES

WIDE PROGRAMMING RANGE

SLEW RATE	0.06 TO 6V/μs
BANDWIDTH	5kHz TO 10MHz
BIAS CURRENT	0.4 TO 50nA
SUPPLY CURRENT	1μA TO 1.5mA

- WIDE POWER SUPPLY RANGE ±1.2 TO ±18V
- CONSTANT AC PERFORMANCE OVER SUPPLY RANGE

APPLICATIONS

- ACTIVE FILTERS
- CURRENT CONTROLLED OSCILLATORS
- VARIABLE ACTIVE FILTERS
- MODULATORS
- BATTERY-POWERED EQUIPMENT

DESCRIPTION

HA-2720/2725 programmable amplifiers are internally compensated monolithic devices offering a wide range of performance, that can be controlled by adjusting the circuits' "set" current (I_{SET}). By means of adjusting an external resistor or current source, power dissipation, slew rate, bandwidth, output current and input noise can be programmed to desired levels. This versatile adjustment capability enables HA-2720/2725 to provide optimum design solutions by delivering the required level of performance with minimum possible power dissipation. HA-2720 and HA-2725 can, therefore, be utilized as the standard amplifier for a variety of designs simply by adjusting their programming current.

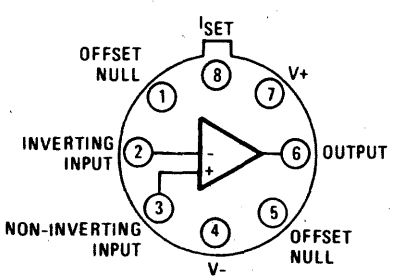
A major advantage of HA-2720/2725 is that operating characteristics remain virtually constant over a wide supply range (±1.2V to ±15V), allowing the amplifiers to offer maximum performance in almost any system including battery-operated equipment. A primary application for HA-2720/2725 is in active filters for a wide variety of signals that differ in frequency and amplitude. Also, by modulating the "set" current, HA-2720/2725 can be used for designs such as current controlled oscillators modulators, sample and hold circuits and variable active filters.

HA-2720 is guaranteed over -55°C to +125°C. HA-2725 is specified from 0°C to +75°C. Both parts are available in TO-99 cans or dice form.

PINOUT

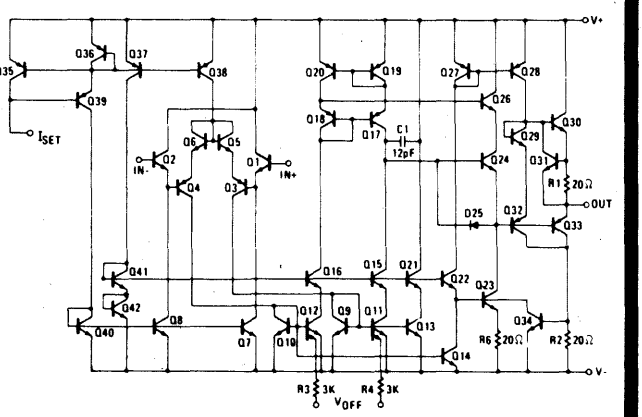
TO-99 **Package Code 2A**

Top View



NOTE: Case tied to V⁻

SCHEMATIC



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow IC Handling Procedures.

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ABSOLUTE MAXIMUM RATINGS

Voltage Between V+ and V- Terminals	45.0V
Differential Input Voltage	±30.0V
Input Voltage (Note 1)	±15.0V
I_{SET} (Current at I_{SET})	500μA
V_{SET} (Voltage to Gnd. at I_{SET})	$V+ - 2.0V \leq V_{SET} \leq V+$
Power Dissipation (Note 2)	300mW
Operating Temperature Range:	
HA-2720	$-55^{o}C \leq T_A \leq +125^{o}C$
HA-2725	$0^{o}C \leq T_A \leq +75^{o}C$
Storage Temperature Range	$-65^{o}C \leq T_A \leq +150^{o}C$

ELECTRICAL CHARACTERISTICS

V+ = +3.0V, V- = -3.0V

		HA-2720 -55°C to +125°C						HA-2725 0°C to +75°C						
		I_{SET} = 1.5μA			I_{SET} = 15μA			I_{SET} = 1.5μA			I_{SET} = 15μA			
PARAMETER	TEMP.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	UNITS
INPUT CHARACTERISTICS														
*Offset Voltage	25°C		2.0	3.0		2.0	3.0		2.0	5.0		2.0	5.0	mV
	Full			5.0			5.0			7.0			7.0	mV
Offset Current	25°C		0.5	3.0		1.0	10		0.5	5.0		1.0	10	nA
	Full			7.5			20			7.5			20	nA
Bias Current	25°C		2.0	5.0		8.0	20		2.0	10		8.0	30	nA
	Full			10			40			10			40	nA
Input Resistance	25°C		50			5			50			5		MΩ
Input Capacitance	25°C		3.0			3.0			3.0			3.0		pF
TRANSFER CHARACTERISTICS														
*Large Signal Voltage Gain (Note 9)	25°C	20K	40K		20K	40K		15K	40K		15K	40K		V/V
	Full	15K			15K			10K			10K			V/V
*Common Mode Rejection Ratio (Note 4)	Full	80			80			74			74			dB
OUTPUT CHARACTERISTICS														
*Output Voltage Swing (Note 3)	25°C	±2.0	±2.2		±2.0	±2.2		±2.0	±2.2		±2.0	±2.2		V
	Full	±2.0			±1.9			±2.0			±2.0			V
Output Current (Note 5)	25°C		±0.2			±2.0			±0.2			±2.0		mA
Output Resistance	25°C		2K			500			2K			500		Ω
Output Short-Circuit Current	25°C		2.8			14			2.8			14		mA
TRANSIENT RESPONSE														
Rise Time (Note 6)	25°C		2.5			0.25			2.5			0.25		μs
Overshoot (Note 6)	25°C		5			10			5			10		%
Slew Rate (Note 7)	25°C		0.07			0.70			0.07			0.70		V/μs
POWER SUPPLY CHARACTERISTICS														
Supply Current	25°C		15			170			15			170		μA
	Full			20			200			20			200	μA
*Power Supply Rejection Ratio (Note 8)	Full	100			100			150			150			μV/V

*100% Tested For DASH 8

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ELECTRICAL CHARACTERISTICS

V+ = +15.0V, V- = -15.0V

PARAMETER	TEMP.	HA-2720 -55°C to +125°C						HA-2725 0°C to +75°C						UNITS
		I_{SET} = 1.5μA			I_{SET} = 15μA			I_{SET} = 1.5μA			I_{SET} = 15μA			
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
INPUT CHARACTERISTICS														
*Offset Voltage	25°C		2.0	3.0		2.0	3.0		2.0	5.0		2.0	5.0	mV
	Full			5.0			5.0			7.0			7.0	mV
*Offset Current	25°C		0.5	3.0		1.0	10		0.5	5.0		1.0	10	nA
	Full			7.5			20			7.5			20	nA
*Bias Current	25°C		2.0	5.0		8.0	20		2.0	10		8.0	30	nA
	Full			10			40			10			40	nA
Input Resistance	25°C		50			5			50			5		MΩ
Input Capacitance	25°C		3.0			3.0			3.0			3.0		pF
TRANSFER CHARACTERISTICS														
*Large Signal Voltage Gain (Notes 3 & 9)	25°C	40K	100K		40K	120K		25K	100K		25K	120K		V/V
	Full	25K			25K			20K			20K			V/V
*Common Mode Rejection Ratio (Note 4)	25°C		90			90			90			90		dB
	Full	80			80			74			74			dB
OUTPUT CHARACTERISTICS														
*Output Voltage Swing (Note 3)	25°C	±12	±13.5		±12	±13.5		±12	±13.5		±12	±13.5		V
	Full	±10			±10			±10			±10			V
Output Current (Note 5)	25°C		±0.5			±5.0			±0.5			±5.0		mA
Output Resistance	25°C		2K			500			2K			500		Ω
Output Short-Circuit Current	25°C		3.7			19			3.7			19		mA
TRANSIENT RESPONSE														
Rise Time (Note 6)	25°C		2.0			0.2			2.0			0.2		μs
Overshoot (Note 6)	25°C		5			15			5			15		%
Slew Rate (Note 7)	25°C		0.1			0.8			0.1			0.8		V/μs
POWER SUPPLY CHARACTERISTICS														
*Supply Current	25°C		20			210			20			210		μA
	Full			25			250			25			250	μA
*Power Supply Rejection Ratio (Note 8)	Full	100			100			150			150			μV/V

NOTES:
1. For supply voltages less than ±15.0V, the absolute maximum input voltage is equal to supply voltage.
2. Derate at 6.8mW/°C for operation ambient temperatures above 75°C.

	V_{SUPPLY} = ±3.0V	V_{SUPPLY} = ±15.0V	I_{SET} = 1.5μA	I_{SET} = 15μA
3.	T = +25°C and Full	T = +25°C	R_L = 75KΩ	R_L = 5KΩ
	—	T = Full	R_L = 75KΩ	R_L = 75KΩ
4.	V_{CM} = ±1.5V	V_{CM} = ±5.0V		
5.	V_O = ±2.0V	V_O = ±10.0V		
6.	← A_V = +1, V_{IN} = 400mV, R_L = 5K, C_L = 100pF →			
7.	V_O = ±2.0V	V_O = ±10.0V	RR_L = 20K	R_L = 5K
8.	ΔV = ±1.5V	ΔV = ±5.0V		
9.	V_O = ±1.0V	V_O = ±10.0V		

*100% Tested For DASH 8

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HA-2730/35

Wide Range Dual Programmable Operational Amplifier

FEATURES

- WIDE PROGRAMMING RANGE

SET CURRENT	0.1 TO 100μA
SLEW RATE	0.06 TO 6V/μs
BANDWIDTH	5kHz TO 10MHz
BIAS CURRENT	0.4 TO 50nA
SUPPLY CURRENT	1μA TO 1.5mA

- WIDE POWER SUPPLY RANGE $^{+}$1.2 TO $^{+}$18V
- CONSTANT AC PERFORMANCE OVER SUPPLY RANGE

APPLICATIONS

- ACTIVE FILTERS
- CURRENT CONTROLLED OSCILLATORS
- VARIABLE ACTIVE FILTERS
- MODULATORS
- BATTERY-POWERED EQUIPMENT

DESCRIPTION

HA-2730/2735 Dual Programmable Amplifiers are internally compensated monolithic devices offering a wide range of performance, that can be controlled by adjusting the circuits' "set" current (I_{SET}). By means of adjusting an external resistor or current source, power dissipation, slew rate, bandwidth, output current and input noise can be programmed to desired levels. Each amplifier on the chip can be adjusted independently. This versatile adjustment capability enables HA-2730/2735 to provide optimum design solutions by delivering the required level of performance with minimum possible power dissipation. HA-2730/2735 can, therefore, be utilized as the standard amplifier for a variety of designs simply by adjusting their programming current.

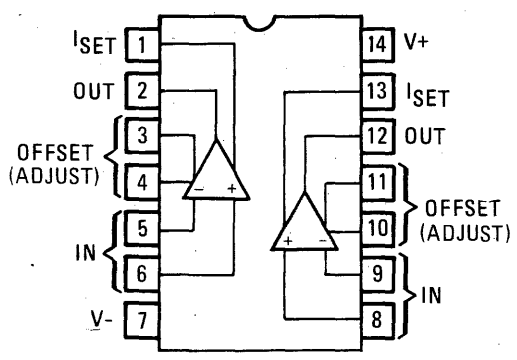
A major advantage of HA-2730/2735 is that operating characteristics remain virtually constant over a wide supply range (±1.2V to ±15V), allowing the amplifiers to offer maximum performance in almost any system including battery-operated equipement. A primary application for HA-2730/2735 is in active filters for a wide variety of signals that differ in frequency and amplitude. Also, by modulating the "set" current, HA-2730/2735 can be used for designs such as current controlled oscillators, modulators, sample and hold circuits and variable active filters.

HA-2730 is guaranteed over -55°C to +125°C. HA-2735 is specified from 0°C to +75°C. Both parts are available in 14 lead D.I.P. package or dice form.

PINOUT

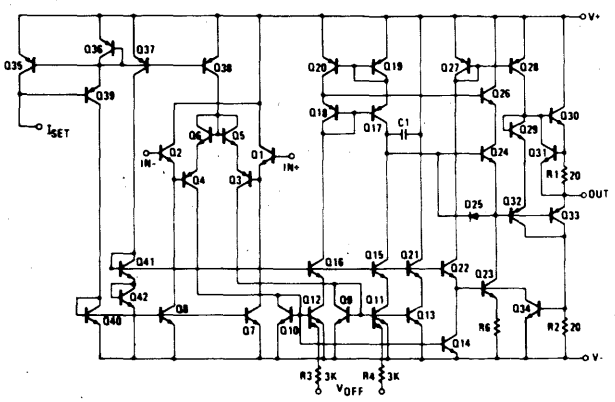
Package Code 4U

Top View



NOTE: Bottom of package is connected to V-.

SCHEMATIC



(ONE HALF ONLY)
HA-2730/35

CAUTION: These devices are sensitive to electrostatic discharge. Users should follow IC Handling Procedures.

SEE PAGES 1022-1025 FOR PACKAGE SELECTION GUIDE

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ABSOLUTE MAXIMUM RATINGS

Voltage Between V+ and V- Terminals	45.0V	Power Dissipation (Note 2)	500mW
Differential Input Voltage	±30.0V	Operating Temperature Range:	
Input Voltage (Note 1)	±15.0V	HA-2730	$-55^{o}C \leq T_A \leq +125^{o}C$
I_{SET} (Current at I_{SET})	500μA	HA-2735	$0^{o}C \leq T_A \leq +75^{o}C$
V_{SET} (Voltage to Gnd. at I_{SET})	$V+ - 2.0V \leq V_{SET} \leq V+$	Storage Temperature Range	$-65^{o}C \leq T_A \leq +150^{o}C$

ELECTRICAL CHARACTERISTICS (Each Side)

V+ = +3.0V, V- = -3.0V

		HA-2730 -55°C to +125°C						HA-2735 0°C to +75°C						
		I_{SET} = 1.5μA			I_{SET} = 15μA			I_{SET} = 1.5μA			I_{SET} = 15μA			
PARAMETER	TEMP.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	UNITS
INPUT CHARACTERISTICS														
*Offset Voltage	25°C		2.0	3.0		2.0	3.0		2.0	5.0		2.0	5.0	mV
	Full			5.0			5.0			7.0			7.0	mV
Offset Current	25°C		0.5	3.0		1.0	10		0.5	5.0		1.0	10	nA
	Full			7.5			20			7.5			20	nA
Bias Current	25°C		2.0	5.0		8.0	20		2.0	10		8.0	30	nA
	Full			10			40			10			40	nA
Input Resistance	25°C		50			5			50			5		MΩ
Input Capacitance	25°C		3.0			3.0			3.0			3.0		pF
TRANSFER CHARACTERISTICS														
*Large Signal Voltage Gain (Notes 3 & 9)	25°C	20K	40K		20K	40K		15K	40K		15K	40K		V/V
	Full	15K			15K			10K			10K			V/V
*Common Mode Rejection Ratio (Note 4)	Full	80			80			74			74			dB
OUTPUT CHARACTERISTICS														
*Output Voltage Swing (Note 3)	25°C	±2.0	±2.2		±2.0	±2.2		±2.0	±2.2		±2.0	±2.2		V
	Full	±2.0			±1.9			±2.0			±2.0			V
Output Current (Note 5)	25°C		±0.2			±2.0			±0.2			±2.0		mA
Output Resistance	25°C		2K			500			2K			500		Ω
Output Short-Circuit Current	25°C		2.8			14			2.8			14		mA
TRANSIENT RESPONSE														
Rise Time (Note 6)	25°C		2.5			0.25			2.5			0.25		μs
Overshoot (Note 6)	25°C		5			10			5			10		%
Slew Rate (Note 7)	25°C		0.07			0.70			0.07			0.70		V/μs
POWER SUPPLY CHARACTERISTICS														
*Supply Current (Each Amp)	25°C		15			170			15			170		μA
	Full			20			200			20			200	μA
*Power Supply Rejection Ratio (Note 8)	Full	100			100			150			150			μV/V

*100% Tested For DASH 8

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ELECTRICAL CHARACTERISTICS (Each Side)

V+ = +15.0V, V- = -15.0V

PARAMETER	TEMP.	HA-2730 -55°C to +125°C						HA-2735 0°C to +75°C						UNITS
		I_{SET} = 1.5μA			I_{SET} = 15μA			I_{SET} = 1.5μA			I_{SET} = 15μA			
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
INPUT CHARACTERISTICS														
*Offset Voltage	25°C		2.0	3.0		2.0	3.0		2.0	5.0		2.0	5.0	mV
	Full			5.0			5.0			7.0			7.0	mV
*Offset Current	25°C		0.5	3.0		1.0	10		0.5	5.0		1.0	10	nA
	Full			7.5			20			7.5			20	nA
*Bias Current	25°C		2.0	5.0		8.0	20		2.0	10		8.0	30	nA
	Full			10			40			10			40	nA
Input Resistance	25°C		50			5			50			5		MΩ
Input Capacitance	25°C		3.0			3.0			3.0			3.0		pF
TRANSFER CHARACTERISTICS														
* Large Signal Voltage Gain (Notes 3 & 9)	25°C	40K	100K		40K	120K		25K	100K		25K	120K		V/V
	Full	25K			25K			20K			20K			V/V
*Common Mode Rejection Ratio (Note 4)	25°C		90			90			90			90		dB
	Full	80			80			74			74			dB
OUTPUT CHARACTERISTICS														
*Output Voltage Swing (Note 3)	25°C	±12	±13.5		±12	±13.5		±12	±13.5		±12	±13.5		V
	Full	±10			±10			±10			±10			V
Output Current (Note 5)	25°C		±0.5			±5.0			±0.5			±5.0		mA
Output Resistance	25°C		2K			500			2K			500		Ω
Output Short-Circuit Current	25°C		3.7			19			3.7			19		mA
TRANSIENT RESPONSE														
Rise Time (Note 6)	25°C		2.0			0.2			2.0			0.2		μs
Overshoot (Note 6)	25°C		5			15			5			15		%
Slew Rate (Note 7)	25°C		0.1			0.8			0.1			0.8		V/μs
POWER SUPPLY CHARACTERISTICS														
*Supply Current (Each Amp)	25°C		20			210			20			210		μA
	Full			25			250			25			250	μA
*Power Supply Rejection Ratio (Note 8)	Full	100			100			150			150			μV/V

NOTES:
1. For supply voltages less than ±15.0V, the absolute maximum input voltage is equal to supply voltage.
2. Derate at 4.7mW/°C at ambient temperatures above 68°C.

	V_{SUPPLY} = ±3.0V	V_{SUPPLY} = ±15.0V	I_{SET} = 1.5μA	I_{SET} = 15μA
3.	T = +25°C and Full	T = +25°C	R_L = 75KΩ	R_L = 5KΩ
	—	T = Full	R_L = 75KΩ	R_L = 75KΩ
4.	V_{CM} = ±1.5V	V_{CM} = ±5.0V		
5.	V_O = ±2.0V	V_O = ±10.0V		
6.	← A_V = +1, V_{IN} = 400mV, R_L = 5K, C_L = 100pF →			
7.	V_O = ±2.0V	V_O = ±10.0V	RR$_L$ = 20K	R_L = 5K
8.	ΔV = ±1.5V	ΔV = ±5.0V		
9.	V_O = ±1.0V	V_O = ±10.0V		

*100% Tested For DASH 8

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HA-2900/04/05

Chopper Stabilized Operational Amplifier

FEATURES

- OFFSET VOLTAGE DRIFT 0.2 μV/°C
- OFFSET CURRENT DRIFT 1pA/°C
- OPEN LOOP GAIN 5×10^8
- BANDWIDTH 3MHz
- SLEW RATE 2.5V/μs
- TRUE DIFFERENTIAL INPUTS

APPLICATIONS

- HIGH-GAIN DC INSTRUMENTATION
- HIGH-ACCURACY WEIGHING EQUIPMENT
- BIOMEDICAL AMPLIFIERS
- PRECISION INTEGRATORS AND TIMERS

DESCRIPTION

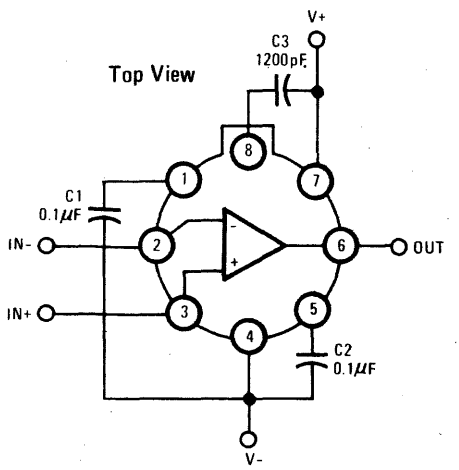
HA-2900/2904/2905 are monolithic chopper-stabilized operational amplifiers that employ dielectric isolation achieving superior offset drift, extremely low input currents and excellent AC performance. Input drift is characterized by offset voltage drift of 0.2 μV/°C and offset current drift of 1pA/°C. Initial offset voltage is only 20 μV while offset current is 50pA. These input specifications make HA-2900/2904/2905 ideally suited to high accuracy applications such as high-gain DC instrumentation, and precision integration. The amplifiers can be used to replace other op amps in designs where much lower errors are required without external adjustments. 3MHz gain-bandwidth product makes HA-2900/2904/2905 valuable for processing wide band signals as well as for low frequency measurements.

In addition to offering high-accuracy performance, these "choppers" also offer versatility by virtue of their symmetrical, differential inputs which permit operation in any op amp configuration – inverting, non-inverting or balanced. These devices require only three external capacitors for proper operation.

HA-2900 is guaranteed over -55°C to +125°C; HA-2904 operates from -25°C to +85°C; HA-2905 operates from 0°C to +75°C. All devices are available in a hermetically sealed metal can.

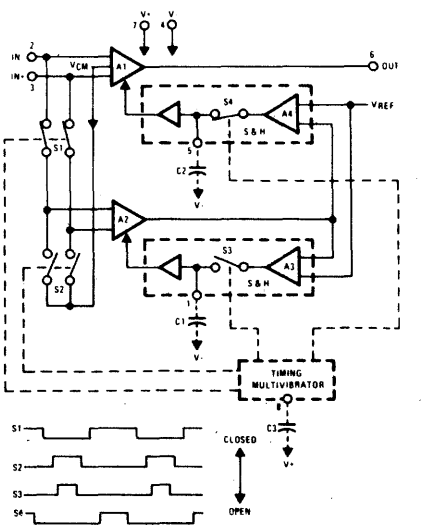
PINOUT AND SUGGESTED HOOKUP

TO-99 **Package Code 2E**



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow IC Handling Procedures.

FUNCTIONAL DIAGRAM



SEE PAGES 1022-1025 FOR PACKAGE SELECTION GUIDE

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ABSOLUTE MAXIMUM RATINGS

Voltage Between V+ and V- Terminals	42.0V	Operating Temperature Range	$-55^{o}C \leq T_A \leq +125^{o}C$ (HA-2900)
Differential Input Voltage (Note 1)	±15V		$-25^{o}C \leq T_A \leq +85^{o}C$ (HA-2904)
Output Current/Full Short Circuit Protection		Storage Temperature Range	$0^{o}C \leq T_A \leq +75^{o}C$ (HA-2905)
Internal Power Dissipation	300mW*		$-65^{o}C \leq T_A \leq +150^{o}C$
		*Derate by 6.6mW/^{o}C above +105^{o}C	

ELECTRICAL CHARACTERISTICS

Test Conditions: C1 = C2 = 0.1μF, C3 = 1500pF, V_{Supply} = ±15.0V unless otherwise specified.

PARAMETER	TEMP.	HA-2900 -55°C to +125°C MIN.	HA-2900 TYP.	HA-2900 MAX.	HA-2904 -25°C to +85°C MIN.	HA-2904 TYP.	HA-2904 MAX.	HA-2905 0°C to +75°C MIN.	HA-2905 TYP.	HA-2905 MAX.	UNITS
INPUT CHARACTERISTICS											
*Offset Voltage	+25°C		20			20			20		μV
	Full			60			50			80	μV
Offset Voltage Average Drift	Full		0.3	0.6		0.2	0.4		0.2		μV/°C
*Bias Current	+25°C		150			150			150		pA
	Full			1,000			1,000			1,000	pA
*Offset Current	+25°C		50			50			50		pA
	Full			500			500			500	pA
Offset Current Average Drift	Full		1	4		1	3		1		pA/°C
Input Resistance	+25°C		100			100			100		MΩ
Input Capacitance	+25°C		10			10			10		pF
Common Mode Range	Full	±10			±10			±10			V
TRANSFER CHARACTERISTICS											
*Large Signal Voltage Gain (Note 2)	+25°C		$5x10^8$			5×10^8			5×10^8		V/V
	Full	10^6			10^7			10^6			V/V
Chopper Frequency	+25°C		750			750			750		Hz
*Common Mode Rejection Ratio (Note 3)	Full	120	160		130	160		120	160		dB
Gain Bandwidth Product (Note 4)	+25°C		3			3			3		MHz
OUTPUT CHARACTERISTICS											
*Output Voltage Swing (Note 2)	Full	±10	±12		±10	±12		±10	±12		V
*Output Current	+25°C	±10			±10			±7			mA
Output Resistance	Full		200			200			200		Ω
Full Power Bandwidth (Note 5)	+25°C		40			40			40		kHz
TRANSIENT RESPONSE (NOTES 2, 8, and 9)											
Rise Time (Note 6)	+25°C		200			200			200		ns
Overshoot (Note 6)	+25°C		20			20			20		%
Slew Rate (Note 5)	+25°C		2.5			2.5			2.5		V/μs
POWER SUPPLY CHARACTERISTICS											
*Supply Current	+25°C		3.5	5.0		3.5	5.0		3.5	5.0	mA
*Supply Voltage Range	Full	±12		±20	±10		±20	±12		±20	V
*Power Supply Rejection Ratio (Note 7)	Full	120	160		130	160		120	160		dB

NOTES:
1. Input terminals should be protected against static discharge during handling and installation. Input voltage should never exceed supply voltages.
2. R_L = 2K
3. V_{CM} = ±5.0V
4. A_V = 10
5. V_O = ±10V
6. V_O = ±200mV
7. ΔV_S = ±5V
8. C_L = 50pF
9. A_V = +1 See transient response test circuits and waveforms, page 4.

*100% Tested For DASH 8

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HA-4602/4605

High Performance Quad Operational Amplifier

FEATURES

- LOW OFFSET VOLTAGE 0.3mV
- HIGH SLEW RATE ±4V/μs
- WIDE BANDWIDTH 8MHz
- LOW DRIFT 2μV/°C
- FAST SETTLING (0.01%, 10V STEP) 4.2μs
- LOW POWER CONSUMPTION 35mW/AMP
- SUPPLY RANGE ±5V TO ±20V

APPLICATIONS

- HIGH Q, WIDE BAND FILTERS
- INSTRUMENTATION AMPLIFIERS
- AUDIO AMPLIFIERS
- DATA ACQUISITION SYSTEMS
- INTEGRATORS
- ABSOLUTE VALUE CIRCUITS
- TONE DETECTORS

DESCRIPTION

The HA-4602 and HA-4605 are high performance dielectrically isolated monolithic quad operational amplifiers with superior specifications not previously available in a quad amplifier. These amplifiers offer excellent dynamic performance coupled with low values for offset voltage and drift, input noise voltage and power consumption.

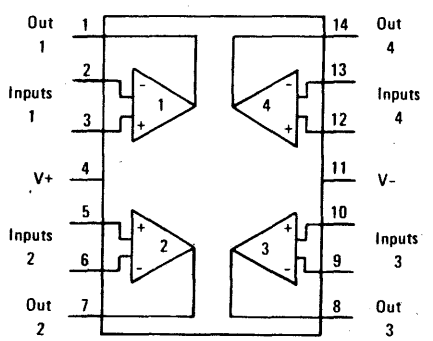
A wide range of applications can be achieved by using the features made available by the HA-4602/4605. With wide bandwidth (8MHz), low power (35mW/amp), and internal compensation, these devices are ideally suited for precision active filter designs. For audio applications these amplifiers offer low noise ($8nV/\sqrt{Hz}$) and excellent full power bandwidth (60kHz). The HA-4602/4605 is particularly useful in designs requiring low offset voltage (0.3mV) and drift (2 μV/°C), such as instrumentation and signal conditioning circuits. The high slew rate (4V/μs) and fast settling time (4.2 μs to 0.01%, 10V step) makes these amplifiers useful components in fast, accurate data acquisition systems.

The HA-4602 and 4605's are available in 14 pin CERDIP packages which are interchangeable with most other quad op amps. HA-4602 is specified from -55°C to +125°C, and HA-4605 is specified over 0°C to +75°C range.

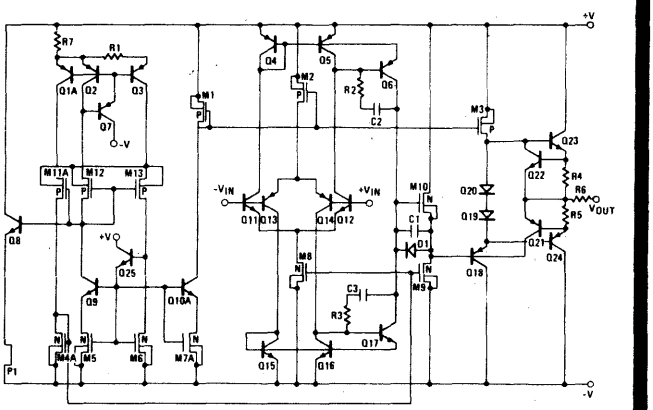
PINOUT

Package Code 4U

TOP VIEW



SCHEMATIC



ONE FOURTH ONLY (HA-4602/4605)

SEE PAGES 1022-1025 FOR PACKAGE SELECTION GUIDE

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ABSOLUTE MAXIMUM RATINGS (Note 1)

T_A = +25°C Unless Otherwise Stated

Voltage Between V+ and V- Terminals	40.0V	Power Dissipation (Note 4)	880mW
Differential Input Voltage	±7V	Operating Temperature Range	
Input Voltage (Note 2)	±15.0V	HA-4602-2	$-55^oC \leq T_A \leq +125^oC$
Output Short Circuit Duration (Note 3)	Indefinite	HA-4605-5	$0^oC \leq T_A \leq +75^oC$
		Storage Temperature Range	$-65^oC \leq T_A \leq +150^oC$

ELECTRICAL CHARACTERISTICS

V+ = 15V, V- = -15V

PARAMETER	TEMP.	HA-4602-2 -55°C to +125°C MIN.	TYP.	MAX.	HA-4605-5 0°C to +75°C MIN.	TYP.	MAX.	UNITS
INPUT CHARACTERISTICS								
* Offset Voltage	+25°C		0.3	2.5		0.5	3.5	mV
	Full			3.0			4.0	mV
Av. Offset Voltage Drift	Full		2			2		µV/°C
* Bias Current	+25°C		130	200		130	300	nA
	Full			325			400	nA
* Offset Current	+25°C		30	75		30	100	nA
	Full			125			120	nA
Common Mode Range	Full	±12			±12			V
Input Noise Voltage (f = 1KHz)	+25°C		8			8		$nV/\sqrt{Hz}$
Input Resistance			500			500		KΩ
TRANSFER CHARACTERISTICS								
* Large Signal Voltage Gain (Note 5)	Full	100K	250K		75K	250K		V/V
* Common Mode Rejection Ratio (Note 9)	Full	86			80			dB
Channel Separation (Note 6)	+25°C		-108			-108		dB
Small Signal Bandwidth	+25°C		8			8		MHz
OUTPUT CHARACTERISTICS								
* Output Voltage Swing (R_L = 10K)	Full	±12	±13		±12	±13		V
(R_L = 2K)	Full	±10	±12		±10	±12		V
Full Power Bandwidth (Note 5)	+25°C		60			60		KHz
Output Current (Note 7)	Full	±10	±15		±8	±15		mA
Output Resistance	+25°C		200			200		Ω
TRANSIENT RESPONSE (Note 8)								
Rise Time	+25°C		50			50		ns
Overshoot	+25°C		30			30		%
Slew Rate	+25°C		±4			±4		V/µs
Settling Time (Note 10)			4.2			4.2		µs
POWER SUPPLY CHARACTERISTICS								
* Supply Current (I^+ or I^-)	+25°C		4.6	5.5		5.0	6.5	mA
* Power Supply Rejection Ratio (Note 9)	Full	86			80			dB

*100% tested for HA1-4602-8

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PRELIMINARY

HA-4622/4625

Wide Band, High Performance Quad Operational Amplifier

FEATURES

- Wide Gain Bandwidth Product — 70MHz
- High Slew Rate — ±20V/μs
- Low Offset Voltage — 0.3V
- Fast Settling (0.01%, 10V Step) — 2.5μs
- Total Harmonic Distortion — <.01% to 30kHz
- Low Drift — 2μV/°C
- Low Power Consumption — 35mW/Amp
- Supply Range — ±5V to ±20V

APPLICATIONS

- High Q Wide Band Filters
- Pulse Amplifiers
- Audio Amplifiers
- Data Acquisition Systems
- Absolute Value Circuits
- Video and R.F. Amplifiers

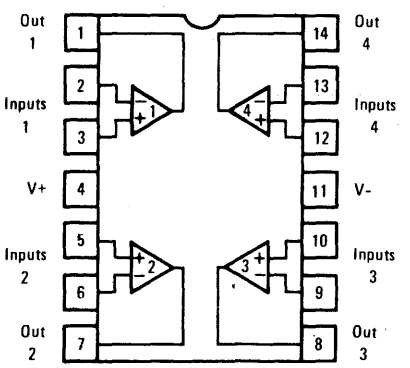
DESCRIPTION

The HA-4622 and HA-4625 are wide band quad operational amplifiers featuring high slew rate, wide bandwidth and fast settling time specifications complemented by low input offset voltage, low drift and input noise voltage.

These dielectrically isolated devices are optimized to offer excellent features suitable for applications where a gain of 10 or greater is to be used. The 35mW/amp and a 70MHz gain-bandwidth-product make these monolithic amplifiers valuable components for many active filter circuits. HA-4622/4625 offer 0.3mV offset voltages and 2 μV/°C offset voltage drift for very accurate signal conditioning designs. In high performance audio applications, these amplifiers deliver 260kHz full power bandwidth and 8nV/$\sqrt{\text{Hz}}$ noise voltage. For fast accurate data acquisition systems HA-4622/4625 offer 20V/μs settling time to 0.01% using a 10V output step.

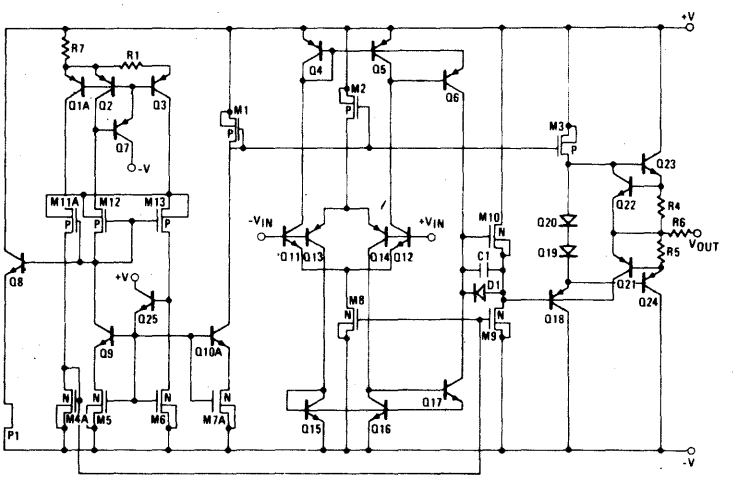
HA-4622 and HA-4625 are available in 14 pin CERDIP packages and are interchangeable with most other quad op amps. HA-4625 is also available in chip form. The HA-4622 specifications are given for operation from -55°C to +125°C while HA-4625 is specified for operation over the 0°C to +75°C range.

PINOUT



TOP VIEW

SCHEMATIC



ONE FOURTH ONLY - HA-4622/4625

SEE PAGES 1022-1025 FOR PACKAGE SELECTION GUIDE

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ABSOLUTE MAXIMUM RATINGS (Note 1)

T_A = +25°C Unless Otherwise Stated

Voltage Between V+ and V- Terminals	40.0V	Power Dissipation (Note 4)	880mW
Differential Input Voltage	±7V	Operating Temperature Range	
Input Voltage (Note 2)	±15.0V	HA-4622-2	-55°C T_A +125°C
Output Short Circuit Duration (Note 3)	Indefinite	HA-4625-5	0°C T_A +75°C
		Storage Temperature Range	-65°C T_A +150°C

ELECTRICAL CHARACTERISTICS

V+ = 15V, V- = -15V

		HA-4622-2 -55°C to +125°C			HA-4625-5 0°C to +75°C			
PARAMETER	TEMP	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
INPUT CHARACTERISTICS								
*Offset Voltage	+25°C		0.3	2.5		0.5	3.5	mV
	Full			3.0			4.0	mV
Av. Offset Voltage Drift	Full		2			2		µV/°C
*Bias Current	+25°C		130	200		130	300	nA
	Full			325			400	nA
*Offset Current	+25°C		30	75		30	100	nA
	Full			125			120	nA
Common Mode Range	Full	±12			±12			V
Input Noise Voltage (f = 1kHz)	+25°C		8			8		$nV/\sqrt{Hz}$
Input Resistance	+25°C		500			500		KΩ
TRANSFER CHARACTERISTICS								
*Large Signal Voltage Gain (Note 5)	Full	100K	250K		75K	250K		V/V
*Common Mode Rejection Ratio (Note 6)	Full	86			80			dB
Channel Separation (Note 7)	+25°C		-108			-108		dB
Gain Bandwidth Products (Note 8)	+25°C		70			70		MHz
OUTPUT CHARACTERISTICS								
*Output Voltage Swing (R_L = 10K)	Full	±12	±13		±12	±13		V
(R_L = 2K)	Full	±10	±12		±10	±12		V
Full Power Bandwidth (Note 5 & 9)	+25°C	150	260		130	260		kHz
Output Current (Note 10)	Full	±10	±15		±8	±15		mA
Output Resistance	+25°C		200			200		Ω
TRANSIENT RESPONSE (Note 11)								
Rise Time	+25°C		38			38		ns
Overshoot	+25°C		45			45		%
Slew Rate	+25°C	±12	±20		±11	±20		V/µs
Settling Time (Note 12)	+25°C		2.5			2.5		µs
POWER SUPPLY CHARACTERISTICS								
*Supply Current (I+ or I-)	+25°C		4.6	5.5		5.0	6.5	mA
*Power Supply Rejection Ratio (NOTE 6)	Full	86			80			dB

*100% tested for HA1-4622-8

NOTES:

1. Absolute maximum ratings are limiting values, applied individually, beyond which the serviceability of the circuit may be impaired. Functional operability under any of these conditions is not necessarily implied.
2. For supply voltages $< \pm 15V$, the absolute maximum input voltage is equal to the supply voltage.
3. Any one amplifier may be shorted to ground indefinitely.
4. Derate 5.8mW/°C above T_A = +25°C.
5. $V_{OUT} = \pm 10V$, R_L = 2K.
6. $V = \pm 5.0V$.
7. Channel separation value is referred to the input of the amplifier. Input test conditions are: f = 10kHz; V_{IN} = 200mV peak to peak; R_S = 1KΩ. (Refer to Channel Separation vs. Frequency Curve for test circuits.)
8. A_V = 10; R_L = 2K; $C_L \leq$ 10pF.
9. Full power bandwidth is guaranteed by equation:
   $$\text{Full power bandwidth} = \frac{\text{Slew Rate}}{2\pi\ V\text{Peak}}$$
10. Output current is measured with $V_{OUT} = \pm 5V$.
11. Refer to Test Circuits section of the data sheet.
12. Settling time is measured to 0.01% of final value for a 1 volt input step, and A_V = -10.

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HA-4741

Quad Operational Amplifier

FEATURES

- SLEW RATE 1.6V/μs (TYP.)
- BANDWIDTH 3.5MHz (TYP.)
- INPUT VOLTAGE NOISE 9nV/$\sqrt{Hz}$ (TYP.)
- INPUT OFFSET VOLTAGE 0.5mV (TYP.)
- INPUT BIAS CURRENT 60nA (TYP.)
- SUPPLY RANGE ±2V TO ±20V
- NO CROSSOVER DISTORTION
- STANDARD QUAD PIN-OUT

APPLICATIONS

- UNIVERSAL ACTIVE FILTERS
- D3 COMMUNICATIONS FILTERS
- AUDIO AMPLIFIERS
- BATTERY-POWERED EQUIPMENT

DESCRIPTION

The HA-4741, which contains four amplifiers on a monolithic chip, provides a new measure of performance for general purpose operational amplifiers. Each amplifier in the HA-4741 has operating specifications that equal or exceed those of the 741-type amplifier in all categories of performance.

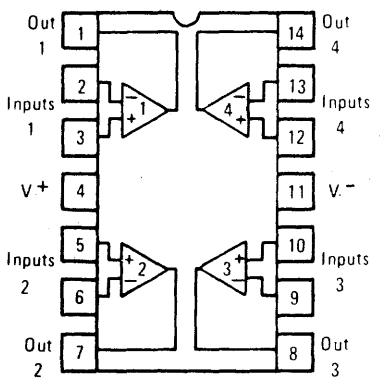
HA-4741 is well suited to applications requiring accurate signal processing by virtue of its low values of input offset voltage (0.5mV), input bias current (60nA) and input voltage noise (9nV/ $\sqrt{Hz}$ at 1kHz). 3.5MHz bandwidth, coupled with high open-loop gain, allow the HA-4741 to be used in designs requiring amplification of wide band signals, such as audio amplifiers. Audio application is further enhanced by the HA-4741's negligible output crossover distortion. These excellent dynamic characteristics also make the HA-4741 ideal for a wide range of active filter designs. Performance integrity of multi-channel designs is assured by a high level of amplifier-to-amplifier isolation (108dB at 1kHz).

A wide range of supply voltages (±2V to ±20V) can be used to power the HA-4741, making it compatible with almost any system including battery-powered equipment.

The HA-4741 has guaranteed operation over -55°C to +125°C and can be furnished to meet MIL-STD-883 (HA-4741-8). The HA-4741-5 is guaranteed over 0°C to +75°C and is available in ceramic and plastic dual-in-line packages and in dice form.

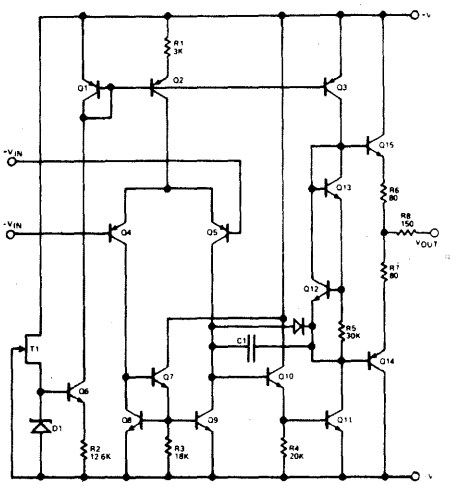
PINOUT

Package Code 4U
Package Code 3B (-5 Only)



QUAD OP AMP

SCHEMATIC



(¼) HA-4741

SEE PAGES 1022-1025 FOR PACKAGE SELECTION GUIDE

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ABSOLUTE MAXIMUM RATINGS

T_A = +25°C Unless Otherwise Stated

Voltage Between V+ and V− Terminals	40.0V	Power Dissipation (Note 3)	880mW
Differential Input Voltage	±30.0V	Operating Temperature Range	
Input Voltage (Note 1)	±15.0V	HA-4741-2	−55°C≤T_A≤+125°C
Output Short Circuit Duration (Note 2)	Indefinite	HA-4741-5	0°C≤T_A≤+75°C
		Storage Temperature Range	−65°C≤T_A≤+150°C

ELECTRICAL CHARACTERISTICS

V+ = 15V, V− = −15V

PARAMETER	TEMP.	HA-4741-2 −55°C to +125°C MIN.	TYP.	MAX.	HA-4741-5 0°C to +75°C MIN.	TYP.	MAX.	UNITS
INPUT CHARACTERISTICS								
* Offset Voltage	+25°C		0.5	3.0		1.0	5.0	mV
	Full		4.0	5.0		5.0	6.5	mV
Av. Offset Voltage Drift	Full		5			5		µV/°C
* Bias Current	+25°C		60	200		60	300	nA
	Full			325			400	nA
* Offset Current	+25°C		15	30		30	50	nA
	Full			75			100	nA
Common Mode Range	Full	±12			±12			V
Differential Input Resistance	+25°C		5			5		MΩ
Input Noise Voltage (f = 1KHz)	+25°C		9			9		$nV/\sqrt{Hz}$
TRANSFER CHARACTERISTICS								
* Large Signal Voltage Gain (Note 4)	+25°C	50K	100K		25K	50K		V/V
	Full	25K			15K			V/V
* Common Mode Rejection Ratio (Note 8)	+25°C	80			80			dB
	Full	74			74			dB
Channel Separation (Note 5)	+25°C		−108			−108		dB
Small Signal Bandwidth	+25°C		3.5			3.5		MHz
OUTPUT CHARACTERISTICS								
* Output Voltage Swing (R_L = 10K)	Full	±12	±13.7		±12	±13.7		V
(R_L = 2K)	Full	±10	±12.5		±10	±12.5		V
Full Power Bandwidth (Note 4)	+25°C		25			25		KHz
Output Current (Note 6)	Full	±5	±15		±5	±15		mA
Output Resistance	+25°C		300			300		Ω
TRANSIENT RESPONSE (Note 7)								
Rise Time	+25°C		75			75		ns
Overshoot	+25°C		25			25		%
Slew Rate	+25°C		±1.6			±1.6		V/µs
POWER SUPPLY CHARACTERISTICS								
* Supply Current (I^+ or I^-)	+25°C			5.0			7.0	mA
* Power Supply Rejection Ratio (Note 8)	Full	80			80			dB

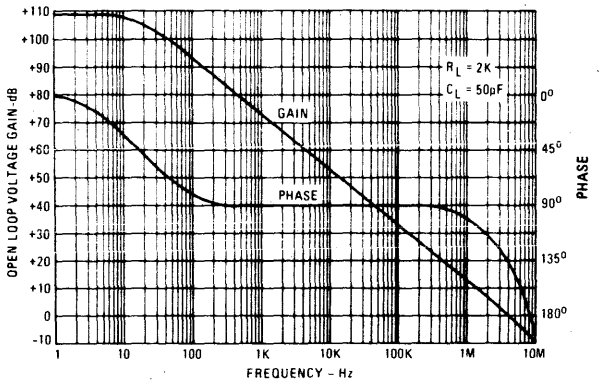
NOTES:
1. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
2. One amplifier may be shorted to ground indefinitely.
3. Derate 5.8mW/°C above T_A = +25°C.
4. V_{OUT} = ±10, R_L = 2K
5. Referred to input; f = 10KHz, R_S = 1K
6. V_{OUT} = ±10
7. See pulse response characteristics
8. ΔV = ±5.0V

*100% Tested for DASH 8.

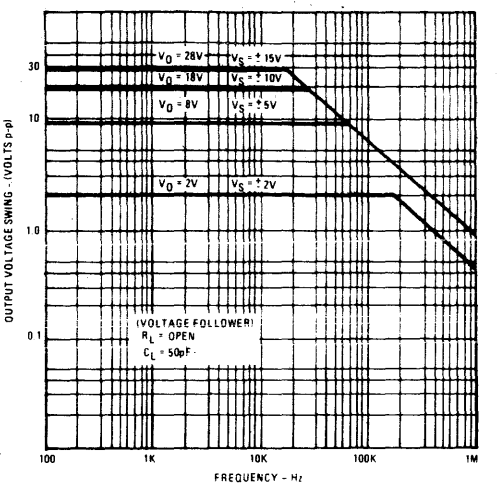
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$V+ = +15V$, $V^- = -15V$, $T_A = +25^oC$
Unless Otherwise Stated.

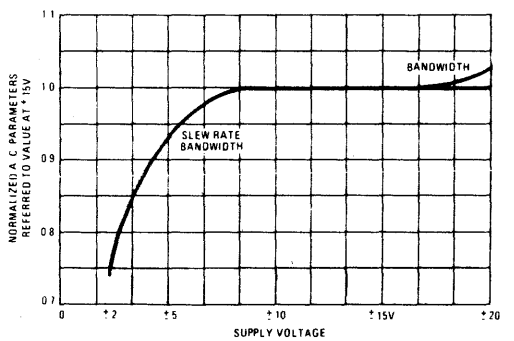
OPEN LOOP FREQUENCY RESPONSE



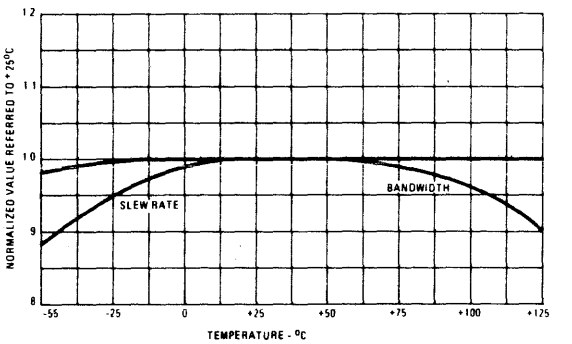
OUTPUT VOLTAGE SWING
VS. FREQUENCY



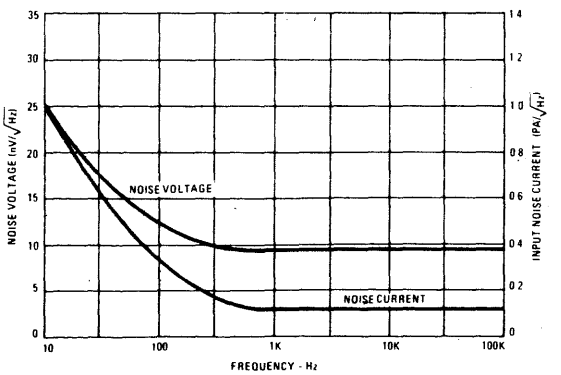
NORMALIZED AC PARAMETERS
VS. SUPPLY VOLTAGE



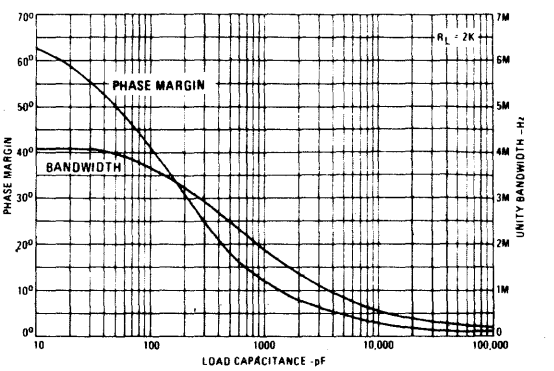
NORMALIZED AC PARAMETERS
VS. TEMPERATURE



INPUT NOISE VS. FREQUENCY

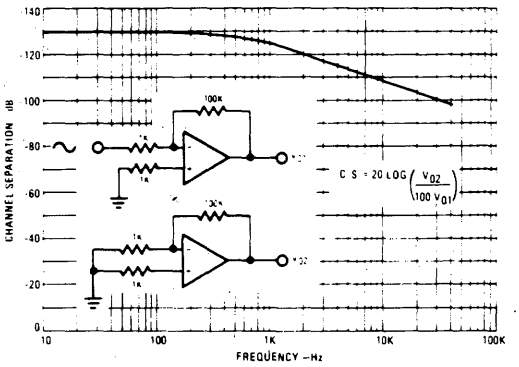


SMALL SIGNAL BANDWIDTH AND PHASE
MARGIN VS. LOAD CAPACITANCE

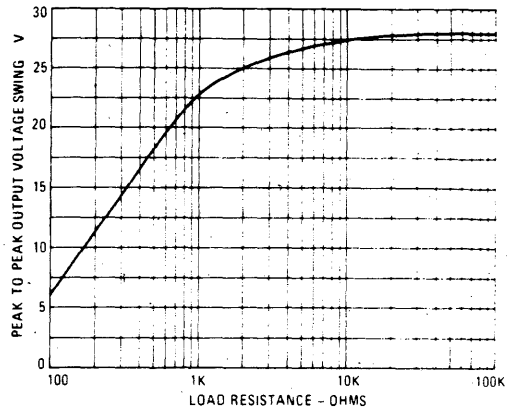


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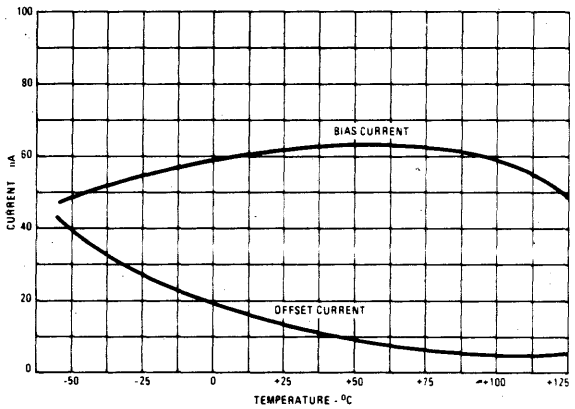
CHANNEL SEPARATION VS. FREQUENCY



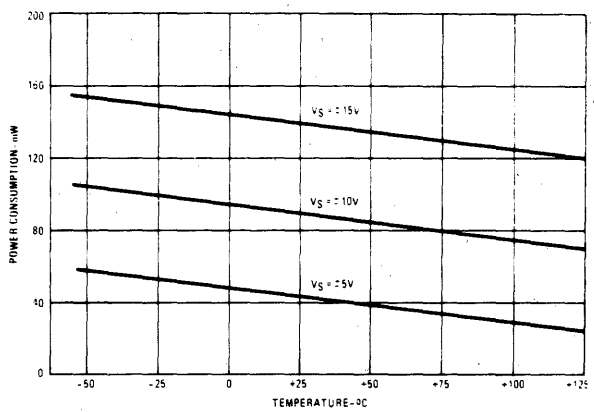
MAXIMUM OUTPUT VOLTAGE SWING VS. LOAD RESISTANCE



INPUT BIAS AND OFFSET CURRENT VS. TEMPERATURE

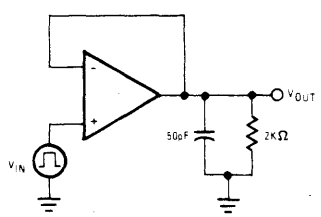


POWER CONSUMPTION VS. TEMPERATURE

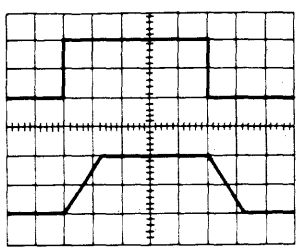


PULSE RESPONSE

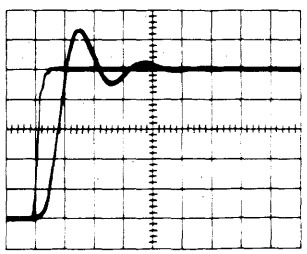
TRANSIENT RESPONSE/SLEW RATE CIRCUIT



SLEW RESPONSE (Volts: 5V/Div, Time: 5μs/Div)



TRANSIENT RESPONSE (Volts: 10mv/Div , Time: 100ns/Div)



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PRELIMINARY

HA-5100/5105

Wideband, JFET Input, Operational Amplifier

TYPICAL PERFORMANCE PARAMETERS

• Low Input Offset Voltage	0.5mV
• Low Offset Drift	5μV/°C
• Low Input Bias Current	50pA
• Large Voltage Gain	150K V/V
• Wide Bandwidth	18MHz
• High Slew Rate	8V/μsec
• Fast Large Signal Settling Time	1.7μsec

GENERAL DESCRIPTION

The HA-5100/5105 are monolithic wideband operational amplifiers manufactured with FET/Bipolar technologies and dielectric isolation. Precision laser trimming of the input stage complements the amplifier high frequency capabilities with excellent input characteristics.

These devices feature superior bandwidth, high slew rate, very low input offset voltage, very low input bias current, extremely high input impedance and fast settling time. Therefore, these amplifiers are most suitable for precision, high speed data acquisition system designs and for a wide variety of signal conditioning applications.*

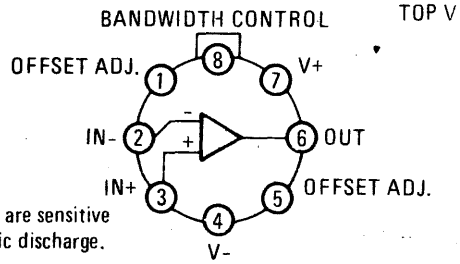
*-2 denotes a range of -55°C to 125°C and -5 denotes a 0°C to 70°C range.

APPLICATIONS

- Precision, High Speed, Data Acquisition Systems
- Precise Signal Generation
- Pulse Amplification

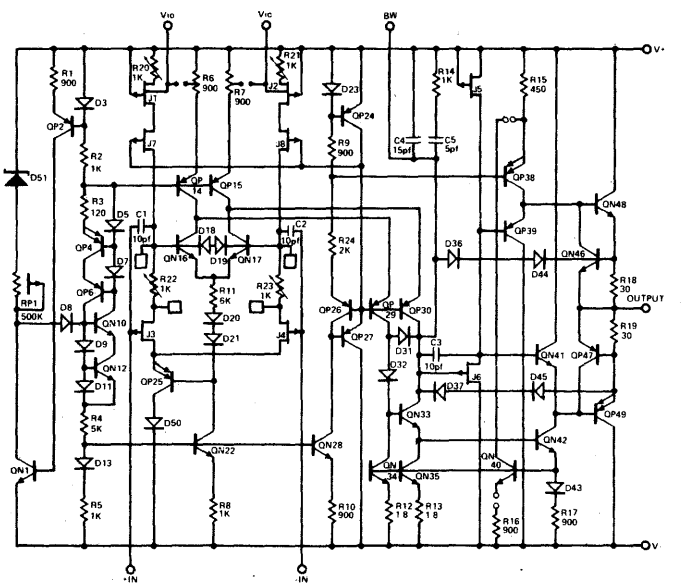
PINOUT

TO-99 TOP VIEW



CAUTION:
These devices are sensitive to electrostatic discharge.

SCHEMATIC DIAGRAM



SEE PAGES 1022-1025 FOR PACKAGE SELECTION GUIDE

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ABSOLUTE MAXIMUM RATINGS

Voltage Between V+ and V-	+40V
Differential Input Voltage	±40V
Peak Output Current	Full Short Circuit Protection
Internal Power Dissipation	300mW
Storage Temperature Range	-65°C to +150°C

ELECTRICAL CHARACTERISTICS

		HA-5100-2 -55°C to +125°C			HA-5100-5 0°C to +70°C			HA-5105-5 0°C to +70°C			
PARAMETER	TEMP	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
INPUT CHARACTERISTICS											
Offset Voltage	+25°C		0.5	1.0		0.5	1.0		0.5	1.5	mV
	Full		0.50	2.0		0.50	2.0		0.75	3.5	mV
Offset Voltage Average Drift	Full		5			10			15		µV/°C
Bias Current	+25°C		20	50		20	50		50	100	pA
	Full		5	10			10		10	20	nA
Offset Current	+25°C		2	10		2	10		5	50	pA
	Full		2	5		2	5		5	10	nA
Input Resistance	+25°C		10^{12}			10^{12}			10^{12}		Ω
Common Mode Range	Full	±10	±11		±10	±11		±10	±10.5		V
TRANSFER CHARACTERISTICS											
Large Signal Voltage Gain (Note 1)	+25°C	75K	150K		75K	150K		50K	100K		V/V
	Full	60K	100K		60K	100K		40K	80K		V/V
Common Mode Rejection Ratio	Full	86	94		86	94		80	86		dB
Gain Bandwidth Product at A_V = 10	Full		18			18			18		MHz
OUTPUT CHARACTERISTICS											
Output Voltage Swing (Note 2)	+25°C	±12	±13		±12	±13		±11	±12		V
	Full	±12	±13		±12	±13		±11	±12		V
Short Circuit Output Current (Note 3)	Full	±10	±15		±10	±15		±8	±15		mA
Full Power Bandwidth (Note 4)	+25°C	100	150		100	150		80	125		kHz
Output Resistance (Note 5)	+25°C		30			30			40		Ω
TRANSIENT RESPONSE											
Rise Time (Note 6)	+25°C		15			15			20		nsec
Slew Rate (Note 7)	+25°C	6	8		6	8		5	8		V/µsec
Settling Time (Note 8)	+25°C		1.7			1.7			2.0		µsec
POWER SUPPLY CHARACTERISTICS											
Supply Current	Full		5	7		5	7		6	8	mA
P.S.R.R.	Full	86	100		86	100		80	94		dB

NOTES: 1. R_L = 2KΩ
2. R_L = 10K
3. V_{OUT} = 0V
4. R_L = 2K
5. C_L = Open Loop
6. V_{IN} = 100mV, R_L = 2KΩ, C_L = 50pF
7. R_L = 2KΩ, C_L = 50pF
8. To 0.1%, V_{OUT} = 10V

*Full power bandwidth guarranteed based on slew rate measurement using FPBW = $S/R/2\pi V_{peak}$.

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HA-5110/5115

Wideband, JFET Input, Uncompensated, Operational Amplifier

PRELIMINARY

FEATURES

- WIDE GAIN BANDWIDTH 60MHz
- HIGH SLEW RATE 50V/μs
- SETTLING TIME 850ns
- POWER BANDWIDTH 800KHz
- OFFSET VOLTAGE 0.5mV
- BIAS CURRENT 50pA

APPLICATIONS

- VIDEO AND RF AMPLIFIERS
- DATA ACQUISITION
- PULSE AMPLIFIERS
- PRECISION SIGNAL GENERATION

DESCRIPTION

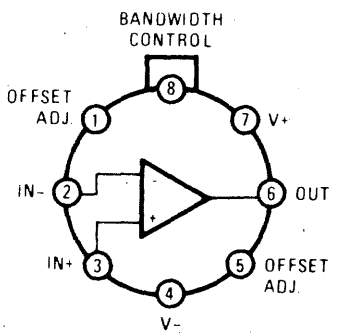
HA-5110/5115 are wideband, uncompensated, operational amplifiers manufactured with FET/Bipolar technologies and dielectric isolation. These monolithic amplifiers feature superior high frequency capabilities further enhanced by precision laser trimming of the input stage to provide excellent input characteristics. These devices are controlled at closed loop gains greater than 10 without compensation.

With excellent dynamic and input characteristics, HA-5110/5115 are well suited for many wideband, pulse, and video applications. These amplifiers are ideal components for video and RF circuitry requiring up to 60MHz gain-bandwidth-product and 800KHz power bandwidth. 50V/μs slew rate and 850ns settling time make these devices useful in pulse amplification and data acquisition designs. HA-5110/5115's 0.5mV offset voltage, 10pA offset current, and extremely high impedance coupled with excellent AC parameters make these amplifiers ideal selections for accurate signal conditioning designs. For applications requiring less critical input characteristics, HA-5115 is available in untrimmed form.

HA-5110/5115 are available in metal can (TO-99) packages. Suffix -2 denotes a range to -55°C to +125°C and -5 denotes a 0°C to +75°C range.

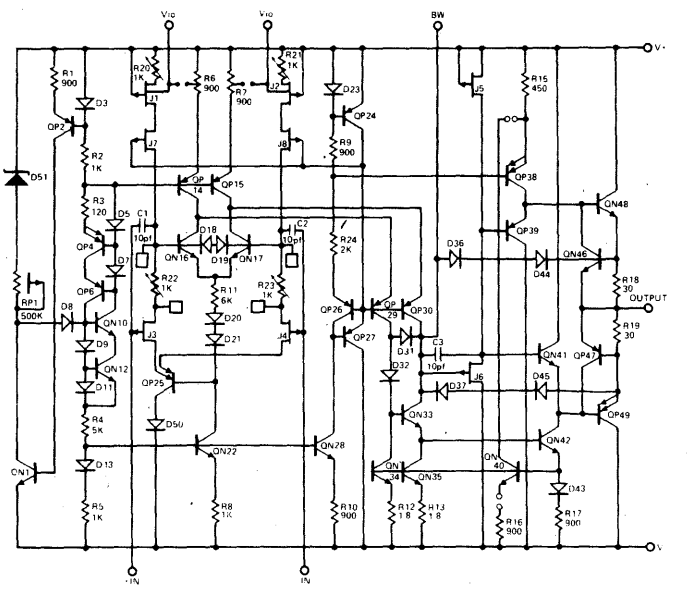
PINOUT

TOP VIEW



TO-99

SCHEMATIC



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ABSOLUTE MAXIMUM RATINGS

Voltage Between V^+ and V^-	40V	Internal Power Dissipation	300mW
Differential Input Voltage	+40V	Storage Temperature Range	-65°C to +150°C
Peak Output Current	Full Short Circuit Protection		

ELECTRICAL CHARACTERISTICS

		HA-5110-2 -55°C to +125°C			HA-5110-5 0°C to +70°C			HA-5115-5 0°C to +70°C			
		LIMITS			LIMITS			LIMITS			
PARAMETER	TEMP	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
INPUT CHARACTERISTICS											
Offset Voltage	+25°C		0.5	1.0		0.5	1.0		0.5	1.5	mV
	Full		0.50	2.0		0.50	2.0		0.75	3.5	mV
Offset Voltage Average Drift	Full		5			10			15		µV/°C
Bias Current	+25°C		20	50		20	50		50	100	pA
	Full		5	10			10		10	20	nA
Offset Current	+25°C		2	10		2	10		5	50	pA
	Full		2	5		2	5		5	10	nA
Input Resistance	+25°C		10^{12}			10^{12}			10^{12}		Ω
Common Mode Range	Full	±10	±11		±10	±11		±10	±10.5		V
TRANSFER CHARACTERISTICS											
Large Signal Voltage Gain (Note 1)	+25°C	75K	150K		75K	150K		50K	100K		V/V
	Full	60K	100K		60K	100K		40K	80K		V/V
Common Mode Rejection Ratio	Full	86	94		86	94		80	86		db
Gain Bandwidth Product	Full		60			60			50		MHz
OUTPUT CHARACTERISTICS											
Output Voltage Swing (Note 2)	+25°C	±12	±13		±12	±13		±11	±12		V
	Full	±12	±13		±12	±13		±11	±12		V
Output Current (Note 3)	+25°C	±10	±15		±10	±15		±8	±15		mA
Full Power Bandwidth (Note 4)	+25°C	625	800		625	800		550	625		KHz
Output Resistance (Note 5)	+25°C		30			30			40		Ω
TRANSIENT RESPONSE											
Rise Time (Note 6)	+25°C		20			20			20		nsec
Slew Rate (Note 7)	+25°C	40	50		40	50		35	40		v/µsec
Settling Time (Note 8)	+25°C		.85			.85			1.0		sec
POWER SUPPLY CHARACTERISTICS											
Supply Current P.S.R.R.	Full		5	7		5	7		6	8	mA
	+25°C	86	100		86	100		80	94		db

NOTES:

1. $R_L = 2K\Omega$; $V_{OUT} = 10V$
2. $R_L = 10K\Omega$
3. $V_{OUT} = 0V$
4. $R_L = 2K\Omega$; Full Bandwidth guaranteed based on slew rate measurement using
   $FPBW = \frac{\text{Slew Rate}}{2\pi V_{peak}}$
5. Open Loop
6. $V_{IN} = 10$ mV; $R_L = 2K\Omega$ $C_L = 50pF$; $A_V = 10$
7. $R_L = 2K\Omega$; $C_L = 50pF$ $A_V = 10$
8. To 0.1%; $V_{OUT} = 10V$; $A_V = 10$

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PRELIMINARY

HA-5190/5195

Wideband, Fast Settling Operational Amplifiers

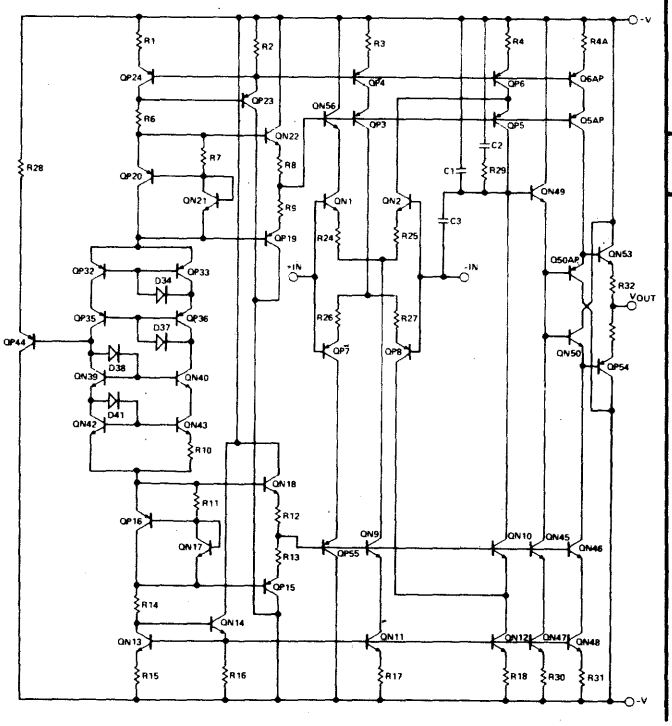
FEATURES

- FAST SETTLING — 70ns
- UNPARALLED SLEW RATE — 200V/μs
- WIDE GAIN-BANDWIDTH — 150MHz
- POWER BANDWIDTH — 6.5MHz
- LOW OFFSET VOLTAGE — 5mV
- INPUT VOLTAGE NOISE — 15nV/$\sqrt{Hz}$
- MONOLITHIC BIPOLAR CONSTRUCTION

APPLICATIONS

- FAST, PRECISE D/A CONVERTERS
- HIGH SPEED SAMPLE-HOLD CIRCUITS
- PULSE AMPLIFIERS
- WIDEBAND AMPLIFIERS

SCHEMATIC



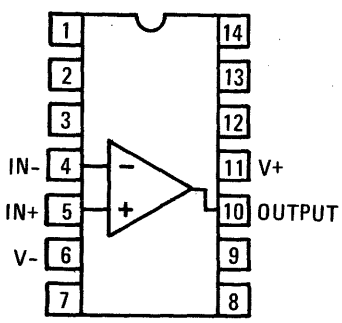
GENERAL DESCRIPTION

HA-5190/5195 are monolithic operational amplifiers featuring an ultimate combination of speed, precision, and bandwidth. Employing monolithic bipolar construction coupled with dielectric isolation, these devices are capable of delivering an unparalled 200V/μs slew rate with a settling time of 70ns (0.1%, 5V output step .) These truly differential amplifiers are designed to operate at gains $\geq$ 5 without the need for external compensation. Other outstanding HA-5190/5195 features are 150MHz gain-bandwidth-product and 6.5MHz full power bandwidth. In addition to these dynamic characteristics, these amplifiers also have excellent input characteristics such as 5mV offset voltage and 15nV input voltage noise (at 1kHz).

With 200V/μs slew rate and 70ns settling time, these devices make ideal output amplifiers for accurate, high speed D/A converters or the main components in high speed sample/hold circuits. 150MHz gain-bandwidth-product, 6.5MHz power bandwidth, and 5mV offset voltage make HA-5190/5195 ideally suited for a variety of pulse and wideband video amplifier applications.

In temperature applications above +75°C, a heat sink is required for HA-5190. THERMALLOY model 6011 or 6012 is recommended. HA-5190 is specified over the -55°C to +125°C range while HA-5195 is specified from 0°C to +75°C.

PINOUT



SEE PAGES 1022-1025 FOR PACKAGE SELECTION GUIDE

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ABSOLUTE MAXIMUM RATINGS

Voltage between V+ and V- Terminals	35V
Differential Input Voltage	6V
Output Current	50mA (Peak)
Internal Power Dissipation	1.5W (Peak)
Operating Temperature Range: (HA-5190)	$-55^{o}C \leq T_A \leq +125^{o}C$
(HA-5195)	$0^{o}C \leq T_A \leq +75^{o}C$
Storage Temperature Range	$-65^{o}C \leq T_A \leq +150^{o}C$

ELECTRICAL CHARACTERISTICS

$V_{SUPPLY} = \pm 15$ Volts; $R_L = 200$ ohms, Unless otherwise specified.

		HA-5190 -55°C to +125°C			HA-5195 0°C to +75°C			
PARAMETER	TEMP	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
INPUT CHARACTERISTICS								
Offset Voltage	+25°C		5.0	6.0		5.0	6.0	mV
	FULL			10.0			10.0	mV
Average Offset Voltage Drift	FULL		20			20		µV/°C
Bias Current	+25°C		5	15		5	15	µA
	FULL			20			20	µA
Offset Current	+25°C		2	4		2	4	µA
	FULL			6			6	µA
Input Resistance	+25°C		10			10		Kohms
Input Capacitance	+25°C		1.0			1.0		pF
Common Mode Range	FULL	±5			±5			V
Input Voltage Noise (f = 1kHz)	+25°C		15			15		nV/√Hz
TRANSFER CHARACTERISTICS								
Large Signal Voltage Gain (Note 1)	+25°C	15K	20K		10K	20K		V/V
	FULL	5K			5K			V/V
Common-Mode Rejection Ratio (Note 2)	FULL	74			74			dB
Gain-Bandwidth-Product (Notes 3 & 4)	+25°C		150			150		MHz
OUTPUT CHARACTERISTICS								
Output Voltage Swing (Note 1)	FULL	±5	±6		±5	±6		V
Output Current (Note 1)	+25°C	25	30		25	30		mA
Full Power Bandwidth (Notes 1 & 7)	+25°C		6.5			6.5		MHz
TRANSIENT RESPONSE								
Rise Time (Notes 5 & 6)	+25°C		11			11		ns
Overshoot (Notes 5 & 6)	+25°C		8			8		%
Slew Rate (Notes 1 & 5)	+25°C		200			200		V/µs
Settling Time: (Notes 1 &5)								
5V Step to 0.1%	+25°C		70			70		ns
5V Step to 0.01%	+25°C		100			100		ns
2.5V Step to 0.1%	+25°C		50			50		ns
2.5V Step to 0.01%	+25°C		80			80		ns
POWER REQUIREMENTS								
Supply Current	+25°C			33			33	mA
Power Supply Rejection Ratio	FULL	70			70			dB

NOTES:
1. $R_L = 200\Omega$, $C_L \leq 10$pF, $V_O = \pm 5$V
2. $V_{CM} = \pm 5$V
3. $V_O < 90$mV
4. 20 dB Gain
5. $A_V = 5$
6. $V_O = 100$mV
7. Full power bandwidth guaranteed based on slew rate measurement using $FPBW = S/R/2\pi V_{peak}$.

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HA-4900/4905

Precision Quad Comparator

FEATURES

- FAST RESPONSE TIME 130ns
- LOW OFFSET VOLTAGE 2.0mV
- LOW OFFSET CURRENT 10nA
- SINGLE OR DUAL-VOLTAGE SUPPLY OPERATION
- SELECTABLE OUTPUT LOGIC LEVELS
- ACTIVE PULL-UP/PULL-DOWN OUTPUT CIRCUIT - NO EXTERNAL RESISTORS REQUIRED

APPLICATIONS

- THRESHOLD DETECTOR
- ZERO-CROSSING DETECTOR
- WINDOW DETECTOR
- ANALOG INTERFACES FOR MICROPROCESSORS
- HIGH STABILITY OSCILLATORS
- LOGIC SYSTEM INTERFACES

DESCRIPTION

The HA-4900/4905 are monolithic, quad, precision comparators offering fast response time, low offset voltage, low offset current, and virtually no channel-to-channel crosstalk for applications requiring accurate, high speed, signal level detection. These comparators can sense signals at ground level while being operated from either a single +5 volt supply (digital systems) or from dual supplies (analog networks) up to ±15 volts. The HA-4900/4905 contains a unique current driven output stage which can be connected to logic system supplies (V_{Logic}^+ and V_{Logic}^-) to make the output levels directly compatible (no external components needed) with any standard logic or special system logic levels. In combination analog/digital systems, the design employed in the HA-4900/4905 input and output stages prevents troublesome ground coupling of signals between analog and digital portions of the system.

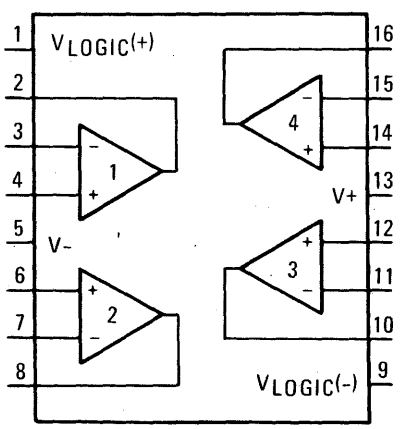
These comparators' combination of features makes them ideal components for signal detection and processing in data acquisition systems, test equipment, and microprocessor/analog signal interface networks.

Both devices are available in 16 pin dual-in-line ceramic packages. The HA-4900 operates from -55°C to +125°C and the HA-4905 operates over a 0°C to +75°C temperature range.

PIN OUT

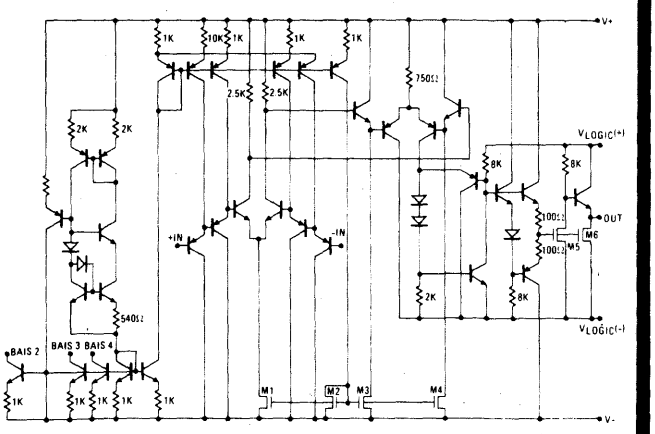
Package Code 4B

Top View



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow IC Handling Procedures

SCHEMATIC



One Fourth Only (HA-4900/4905)

SEE PAGES 1022-1025 FOR PACKAGE SELECTION GUIDE

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ABSOLUTE MAXIMUM RATINGS (Note 1)

Voltage Between V+ and V-	33V
Voltage Between $V_{Logic}(+)$ and $V_{Logic}(-)$	18V
Differential Input Voltage	±15V
Peak Output Current	±50mA
Internal Power Dissipation (Note 7, 8)	580mW
Storage Temperature Range	$-65^{o}C \leq T_A \leq 150^{o}C$

ELECTRICAL CHARACTERISTICS

V+ = +15.0V
V- = -15.0V
$V_{Logic}(+)$ = 5.0V
$V_{Logic}(-)$ = GND.

PARAMETER	TEMP.	HA-4900 -55°C to +125°C MIN.	HA-4900 -55°C to +125°C TYP.	HA-4900 -55°C to +125°C MAX.	HA-4905 0°C to +75°C MIN.	HA-4905 0°C to +75°C TYP.	HA-4905 0°C to +75°C MAX.	UNITS
INPUT CHARACTERISTICS								
* Offset Voltage (Note 2)	25°C		2.0	3.0		4.0	7.5	mV
	Full			4.0			10.0	mV
* Offset Current	25°C		10	25		25	50	nA
	Full			35			70	nA
* Bias Current (Note 3)	25°C		50	75		100	150	nA
	Full			150			300	nA
Input Sensitivity (Note 4)	25°C			3.1			7.6	mV
	Full			4.1			10.1	mV
* Common Mode Range	Full	V-		V+ -2.4	V-		V+ -2.4	V
TRANSFER CHARACTERISTICS								
Large Signal Voltage Gain	25°C		400K			400K		V/V
Response Time (T_{pd0})(Note 5)	25°C		130			130		ns
Response Time (T_{pd1})(Note 5)	25°C		180			180		ns
OUTPUT CHARACTERISTICS								
* Output Voltage Level								
Logic "Low State" (V_{OL})(Note6)	Full		0.2	0.4		0.2	0.4	V
Logic "High State" (V_{OH})(Note6)	Full	3.5	4.2		3.5	4.2		V
Output Current								
I_{Sink}	Full	3.5			3.5			mA
I_{Source}	Full	3.0			3.0			mA
POWER SUPPLY CHARACTERISTICS								
* Supply Current, $I_{ps}(+)$	25°C		6.5	12		7	13	mA
* Supply Current, $I_{ps}(-)$	25°C		4	6		5	7	mA
* Supply Current, I_{ps}(Logic)	25°C		1.7	2.0		1.7	2.5	mA
Supply Voltage Range								
V+	Full	+5.0		+15.0	+5.0		+15.0	V
V-	Full	-15.0		0	-15.0		0	V
$V_{Logic}(+)$ (Note 7)	Full	0		+15.0	0		+15.0	V
$V_{Logic}(-)$ (Note 7)	Full	-15.0		0	-15.0		0	V

*100% tested for HA1-4900-8.

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HA-4920/4925

High Speed Quad Comparator

Preliminary

FEATURES

- FAST RESPONSE TIME
- LOW OFFSET VOLTAGE
- STANDARD POWER SUPPLIES
- ACTIVE PULL-UP/PULL-DOWN OUTPUT CIRCUIT – NO EXTERNAL RESISTORS REQUIRED
- TTL AND ECL COMPATIBLE

APPLICATIONS

- A/D CONVERTERS
- THRESHOLD DETECTOR
- ZERO-CROSSING DETECTOR
- LOGIC SYSTEM INTERFACES
- HIGH FREQUENCY OSCILLATORS

DESCRIPTION

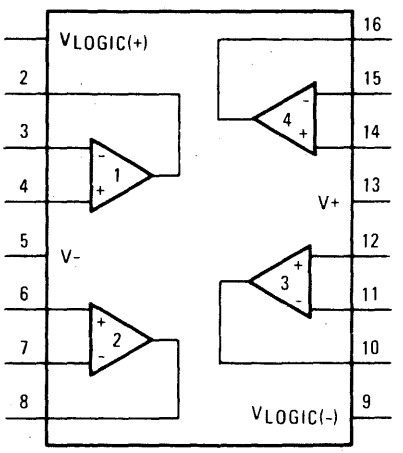
HA-4920/4925 are monolithic, quad, high speed comparators offering a combination of speed, precision, and flexibility never before available in a quad comparator. 40ns response time and 2.0mV offset voltage makes these comparators ideally suited for precise signal level detection and fast response times to large and small input signal levels. These dielectrically isolated devices employ unique input/output stages which prevent troublesome ground coupling inherent in combined analog/digital systems.

The flexibility/speed of HA-4920/4925 assures easy application in fast data acquisition systems, analog to logic interface networks, and test equipment.

Both devices are available in 16 pin dual-in-line ceramic packages. The HA-4920 operates from -55°C to +125°C and the HA-4925 operates over a 0°C to +75°C temperature range.

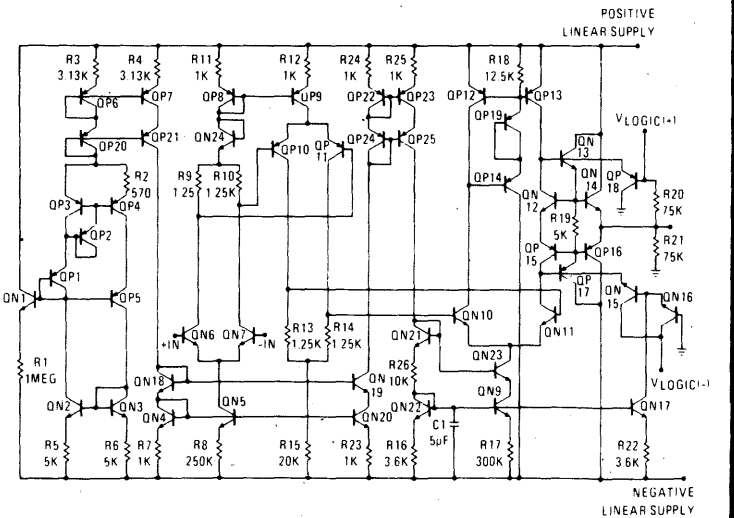
PINOUT

QUAD COMPARATOR



TOP VIEW

SCHEMATIC



SEE PAGES 1022-1025 FOR PACKAGE SELECTION GUIDE

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ABSOLUTE MAXIMUM RATINGS

Voltage between V+ and V-	40V
Voltage between $V_{Logic}(+)$ and $V_{Logic}(-)$	7V
Differential Input Voltage	±6V
Peak Output Current	50mA
Internal Power Dissipation (Note 1)	500mW
Storage Temperature Range	$-65^oC \leq T_A \leq 150^oC$

ELECTRICAL CHARACTERISTICS

V+ = +15.0V $V_{Logic}(+)$ = 5.0V
V- = -15.0V $V_{Logic}(-)$ = GND

		HA-4920: -55°C/+125°C			HA-4925: 0°C/+75°C			
PARAMETER	TEMP	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Input Offset Voltage (Note 2)	+25°C		2.0	3.0		4.0	6.0	mV
	Full			4.0			8.0	mV
Input Offset Current	+25°C		1.0	1.5		1.5	2.0	μa
	Full			2.0			3.0	
Input Bias Current	+25°C		5.0	6.0		6.0	8.0	μa
	Full			8.0			10.0	μa
Input Sensitivity (Note 3)	Full		0.6			0.6		mV
Common Mode Range (CMR)	Full	V_{CC} ±11			V_{CC} ±11		V_{CC} ±4.0	V
Large Signal Voltage Gain	+25°C		25K			25K		V/V
Response Time Tpd0 (Note 4)	+25°C		35			35		ns
Response Time Tpd1 (Note 4)	+25°C		30			30		ns
Output Voltage Level (Note 5)	Full		.2	.4		.2	.4	V
Output Voltage Level (Note 5)	Full	3.5	4.2		3.5	4.2		V
Output Current I_{Sink} (Note 6)	Full	3.2			3.2			mA
Output Current I_{Source} (Note 6)	Full	3.2			3.2			mA
Power Supply Current I_{CC+}	+25°C			22			22	mA
Power Supply Current I_{CC-}	+25°C			30			30	mA
Power Supply Current I_{Logic+}	+25°C			8.0			8.0	mA

1. Derate by 5.8mW/°C above T_A = +75°C.
2. Minimum differential input voltage required to ensure a defined output state.
3. Input sensivity is the differential voltage required at the input to make the output change state, after the offset has been nulled. Rs ≤ 10Ω.
4. Tpd (1) conditions; 100mV input step, -5mV overdrive. Tpd (0) conditions; -100mV input step, 5mV overdrive. Freq. ≃ 1KHz; Duty cycle ≃ 50%; TTL Fan Out = 1; Inverting Input Driven.
5. For V_{OH} and V_{OL}: 1 sink = 3.2mA, I_{Souce} = 3.2mA.
6. Per comparator.

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PRELIMINARY

HA-1600-5

Precision Voltage Reference

FEATURES

- MONOLITHIC CONSTRUCTION
- EXCELLENT TEMPERATURE STABILITY . . ±1ppm/°C
- LOW NOISE . . . . . 100μV_{p-p}
- WIDE INPUT RANGE . . . . . 12V to 20V

APPLICATIONS

- EXTERNAL VOLTAGE REFERENCE FOR DATA CONVERTERS (D/A OR A/D)
- COMPARATOR REFERENCE
- VOLTAGE REGULATOR REFERENCE

DESCRIPTION

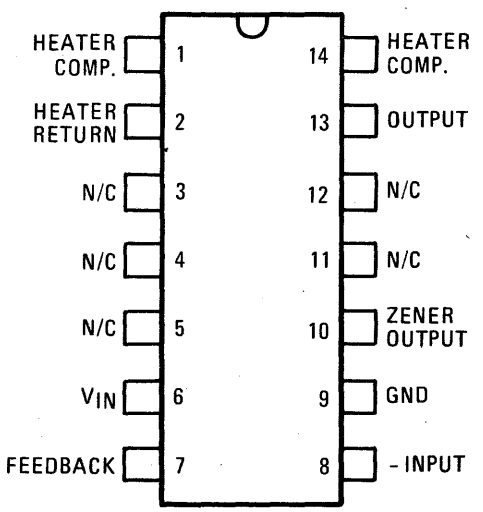
The Harris HA-1600 is a monolithic, temperature regulated +10V precision voltage reference, packaged in a 14 pin DIP. The chip temperature is sensed and regulated by a high gain differential amplifier to achieve a typical temperature coefficient of +1ppm/°C over the specified temperature range.

The I.C. chip is thermally isolated from the package to provide fast warm-up with minimum power drain. The output of the HA-1600 is laser trimmed to provide a precision +10V out.

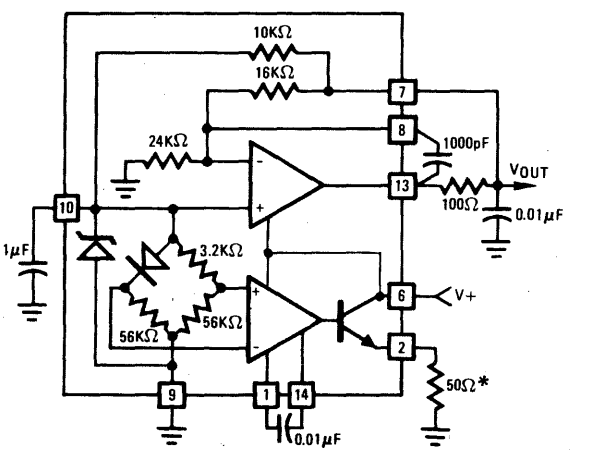
The HA-1600 accepts an unregulated 12V to 20V, DC input voltage and provides a very accurate +10V DC output at a maximum of 2mA load current. An external amplifier may be connected inside the feedback loop for higher output current. The characteristics of this voltage reference make it an ideal choice for applications where high precision and high stability is a necessity, such as the external voltage reference for a 12 bit D/A converter.

PINOUT

TOP VIEW



FUNCTIONAL DIAGRAM



*Current Limiting Resistor - See Note 2.

SEE PAGES 1022-1025 FOR PACKAGE SELECTION GUIDE

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SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS (Referred to Ground - Note 1)

Input Voltage	35V	Operating Temperature Range	0°C to 75°C
Power Dissipation	800mW	Storage Temperature	-65°C to 150°C

ELECTRICAL CHARACTERISTICS (Note 2)

V_{IN} = +15V; I_L = 0mA Unless Otherwise Specified.

PARAMETER	TEMP	HA-1600-5 0°C to +75°C MIN	TYP	MAX	UNITS
POWER INPUT CHARACTERISTICS					
V_{IN}, Input Voltage Range	25°C	12	15	20	Volts
I_Q, Quiescent Current	0°C		30	50	mA
	25°C		25	40	mA
	75°C		12	20	mA
REGULATED OUTPUT CHARACTERISTICS					
V_O, Output Voltage	25°C	9.998	10.000	10.002	Volts
I_L, Output Load Current	25°C			2	mA
e_n, Output Noise Voltage (0.1Hz to 1MHz)	Full		100	200	μV_{p-p}
Line Regulation V_{IN} = 13.5V to 16.5V	25°C		0.001	0.002	%/V
	Full		0.001	0.002	%/V
Load Regulation R_L = Open to 5KΩ	25°C		0.001	0.002	%/mA
	Full		0.001	0.002	%/mA
T_C, Output Voltage Temperature Coefficient, R_L = Open	Full		±1		ppm/°C
R_L = 5KΩ	Full		±1		ppm/°C
TURN-ON CHARACTERISTICS					
Turn-on Current (Note 3)	0°C		70		mA
	25°C		70		mA
	75°C		30		mA
Warm-up Time	0°C		60		sec.
	25°C		45		sec.

NOTES

1. Absolute maximum ratings are limiting values beyond which the serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied.
2. The specified electrical characteristics apply to suggested hookup only. The 50Ω heater current limiter is mandatory.
3. The maximum current drawn from the input supply that is required to heat the chip to its operating temperature at the specified conditions.

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HA-1610

+10V Precision Voltage Reference

Preliminary

FEATURES

- MONOLITHIC CONSTRUCTION
- INITIAL ACCURACY +10V ±0.01%
- EXCELLENT TEMPERATURE STABILITY ±5ppm/°C MAX
- LOW NOISE 100 μV_{p-p}
- WIDE INPUT RANGE 12V TO 30V
- OUTPUT SHORT CIRCUIT PROTECTION

APPLICATIONS

- EXTERNAL VOLTAGE REFERENCE FOR DATA CONVERTERS (D/A OR A/D)
- COMPARATOR REFERENCE
- VOLTAGE REGULATOR REFERENCE

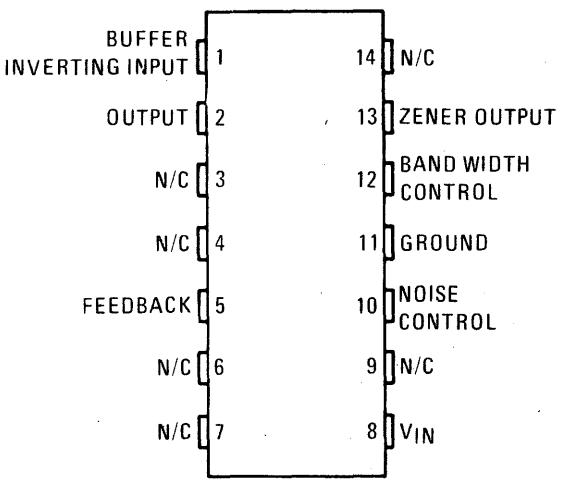
DESCRIPTION

The Harris HA-1610 is a monolithic +10V precision voltage reference packaged in a Hermetic Dual-in-Line package. The voltage output of the HA-1610 is held constant under varying external conditions by a reference zener and buffer amplifier. The feedback resistors and zener bias resistor are laser trimmed to provide the initial accuracy of 10 ± .01% and optimum T_C of ± 5ppm/°C (Max.) over the operating temperature range.

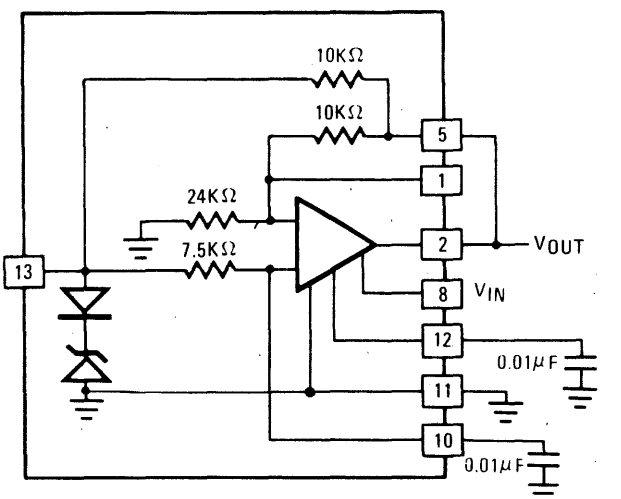
The HA-1610 accepts an unregulated 12V to 30V DC input and provides a accurate +10V DC output at a typical load current of 10mA. For higher current output, an external amplifer may be connected inside the feedback loop as a current booster. The high precision voltage output and low power dissipation (I_Q = 2mA Typ.) characteristics of HA-1610 make it an ideal choice for applications where high precision and high stability is a necessity, such as the voltage reference for 12 bit D/A or A/D converter.

PINOUT

TOP VIEW



FUNCTIONAL DIAGRAM



SEE PAGES 1022-1025 FOR PACKAGE SELECTION GUIDE

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ABSOLUTE MAXIMUM RATINGS NOTE 1

Input Voltage	40V	Operating Temperature Range	
		HA-1610-2	-55°C to +125°C
Output Short Circuit Duration	Indefinitely	HA-1610-5	0°C to +75°C
Power Dissipation	400mW	Storage Temperature Range	-65°C to +150°C

ELECTRICAL CHARACTERISTICS Note 2

(V_{IN} = +15V, I_L = 0mA, unless otherwise specified)

		HA-1610-2 -55°C to +125°C			HA-1610-5 0°C to +75°C			
PARAMETER	TEMP	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
POWER INPUT CHARACTERISTICS								
Input Voltage Range, V_{IN}	Full	12	15	30	12	15	30	V
Quiescent Current, I_Q	25°C		1.9			1.9		mA
	Full			3.0			3.0	
REGULATED OUTPUT CHARACTERISTICS								
Output Voltage, V_O	25°C		10.00			10.00		V
Output Load Current, I_L	Full		10			10		mA
Line Regulation (V_{IN} = 12V to 30V)	25°C		0.001			0.001		%/V
	Full			0.004			0.004	
Load Regulation (I_L = Open to 10mA)	25°C		0.0015			0.0015		%/mA
	Full			0.004			0.004	
Output Voltage Tempco, I_L = 0mA	Full		±3			±3		ppm/°C
I_L = 10mA	Full		±5			±5		
Output Noise Voltage, e_n	25°C		100			100		μV_{p-p}
(0.1Hz to 1MHz)	Full		150			150		
Dynamic Load Settling Time								
To ±0.1%	25°C		100			100		ns
To ±0.01%	25°C		400			400		
Warm-up Time (To ±0.01%)	25°C		1			1		sec
	Full		3			3		

NOTES

1. Absolute maximum ratings are limiting values beyond which the serviceability of the circuit may be impaired. Functional operation under any of these conditions is not necessarily implied.
2. The specified electrical characteristics apply to suggested hookup only.

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HA-2420/2425

Fast Sample and Hold Gated Operational Amplifier

FEATURES

- SAMPLE CURRENT/HOLD RATIO 10^6
- ACQUISITION TIME (0.01%) $5\mu s$
- SLEW RATE $5V/\mu s$
- BANDWIDTH 2MHz
- APERTURE DELAY 50ns
- LOW CHARGE TRANSFER 10pC
- DTL/TTL COMPATIBLE CONTROL INPUT

APPLICATIONS

- A TO D INPUT (TO 13 BITS)
- D TO A DEGLITCHER
- AUTO ZERO SYSTEMS
- PEAK DETECTOR
- GATED OP AMP

DESCRIPTION

The HA-2420/2425 is a monolithic circuit consisting of a high performance operational amplifier with its output in series with an ultra-low leakage analog switch and a MOSFET input unity gain amplifier.

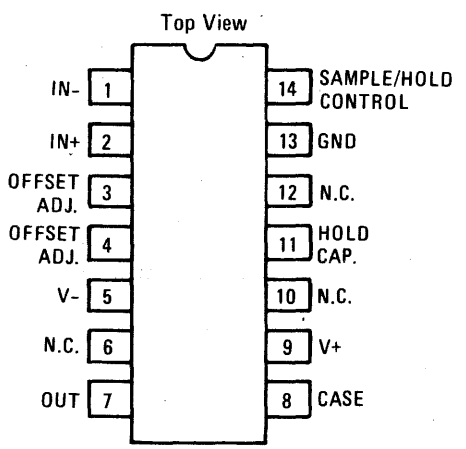
With an external holding capacitor connected to the switch output, a versatile, high performance sample-and-hold or track-and-hold circuit is formed. When the switch is closed, the device behaves as an operational amplifier, and any of the standard op amp feedback networks may be connected around the device to control gain, frequency response, etc. When the switch is opened the output will remain at its last level.

Performance as a sample-and-hold compares very favorably with other monolithic, hybrid, modular, and discrete circuits. Accuracy to better than 0.01% is achievable over the temperature range. Fast acquisition is coupled with superior droop characteristics, even at high temperatures. High slew rate, wide bandwidth, and low acquisition time produce excellent dynamic characteristics. The ability to operate at gains greater than 1 frequently eliminates the need for external scaling amplifiers.

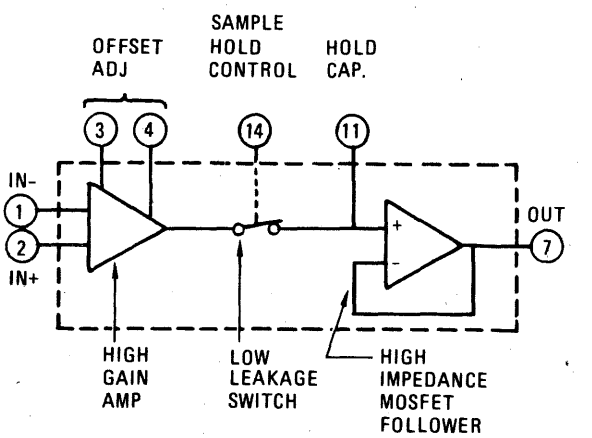
The device may also be used as a versatile operational amplifier with a gated output for applications such as analog switches, peak holding circuits, etc.

PINOUT

Package Code 4U



FUNCTIONAL DIAGRAM



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow IC Handling Procedures.

SEE PAGES 1022-1025 FOR PACKAGE SELECTION GUIDE

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SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Voltage Between V+ and V- Terminals	40V	Internal Power Dissipation	300mW (Note 7)
Differential Input Voltage	±30V	Operating Temperature Range	
Digital Input Voltage (Pin 14)	+8V, -15V	HA-2420	$-55^{o}C \leq T_A \leq +125^{o}C$
Output Current	Short Circuit Protected	HA-2425	$0^{o}C \leq T_A \leq +75^{o}C$
		Storage Temperature Range	$-65^{o}C \leq T_A \leq +150^{o}C$

ELECTRICAL CHARACTERISTICS

Test Conditions $V_{Supply} = \pm 15.0V$, $C_H = 1000pF$ Unless Otherwise Specified. Digital Input (Pin 14) $V_{IL} = +0.8V$ (Sample), $V_{IH} = +2.0V$ (Hold)

		HA-2420			HA-2425			
PARAMETER	TEMP.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	UNITS
INPUT CHARACTERISTICS								
* Offset Voltage	+25°C		2	4		3	6	mV
	Full		3	6		4	8	mV
*Bias Current	+25°C		50	200		50	200	nA
	Full			400			400	nA
* Offset Current	+25°C		10	50		10	50	nA
	Full			100			100	nA
Input Resistance	+25°C	5	10		5	10		MΩ
Common Mode Range	Full	±10			±10			V
TRANSFER CHARACTERISTICS								
* Large Signal Voltage Gain (Note 1, 4)	Full	25K	50K		25K	50K		V/V
*Common Mode Rejection (Note 2)	Full	80	90		74	90		dB
Gain Bandwidth Product (Note 3)	+25°C		2			2		MHz
OUTPUT CHARACTERISTICS								
* Output Voltage Swing (Note 1)	Full	±10			±10			V
Output Current	+25°C	±10			±10			mA
Full Power Bandwidth (Note 3, 4)	+25°C		70			70		kHz
Output Resistance	+25°C		5			5		Ω
TRANSIENT RESPONSE								
Rise Time (Note 3, 5)	+25°C		100			100		ns
Overshoot (Note 3, 5)	+25°C		20			20		%
Slew Rate (Note 3, 6)	+25°C		5			5		V/μs
DIGITAL INPUT CHARACTERISTICS								
Digital Input Current (V_{IN} = 0V)	Full			0.8			0.8	mA
Digital Input Current (V_{IN} = +5.0V)	Full			20			20	μA
Digital Input Voltage (Low)	Full			0.8			0.8	V
Digital Input Voltage (High)	Full	2.0			2.0			V
SAMPLE/HOLD CHARACTERISTICS								
Acquisition Time to .1% 10V Step (3)	+25°C		4			4		μs
Acquisition Time to .01% 10V Step (3)	+25°C		5			5		μs
Aperture Delay	+25°C		50			50		ns
Aperture Uncertainty	+25°C		5			5		ns
* Drift Current	+25°C		5			5		pA
	Full		0.5	10		.05	1.0	nA
* Charge Transfer	+25°C		10	20		10	20	pC
POWER SUPPLY CHARACTERISTICS								
* Supply Current	+25°C		2.5	5.0		2.5	5.0	mA
* Power Supply Rejection Ratio	Full	80	90		74	90		dB

NOTES:
1. $R_L = 2K\Omega$
2. $V_{CM} = \pm 10VDC$
3. $A_V = +1$, $R_L = 2K\Omega$, $C_L = 50pF$
4. $V_{OUT} = 20V$ peak-to-peak
5. $V_{OUT} = 400mV$ peak-to-peak
6. $V_{OUT} = 10.0V$ peak-to-peak
7. Derate Power Dissipation by 4.3mW/°C above +105°C Ambient Temperature.

*100% Tested For DASH 8

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HARRIS
SEMICONDUCTOR
PRODUCTS DIVISION
A DIVISION OF HARRIS CORPORATION

Harris Package Selection Guide

PART NUMBER	PACKAGE CODE (See Note)		
	CAN	FLATPACK	D.I.P.
HA-909/911	2A	9V	
HA-2050/2055/2050A/2055A	2A		
HA-2060/2065/2060A/2065A	2A		
HA-2400/2404/2405			4B
HA-2420/2425			4U
HA-2500/2502/2505	2A		
HA-2510/2512/2515	2A	9V*	
HA-2520/2522/2525	2A	9V*	
HA-2530/2535	2A		
HA-2600/2602/2605	2A	9W*	
HA-2620/2622/2625	2A		4U
HA-2630/2635	2G		
HA-2640/2645	2A		
HA-2650/2655	2A		4U
HA-2700/2704/2705	2A		4U
HA-2720/2725	2A		
HA-2730/2735			4U
HA-2820/2825			4U
HA-2900/2904/2905	2E		
HA-4602/4605			4U
HA-4741			4U, 3B†
HA-4900/4905			4B
HC-55516/55532		9R	4Q
HD-0165			4K
HD-245/545		9V	1S
HD-246/546/249/549		9V	1S
HD-248/548		9V	1S
HI-200	2D		
HI-201			4B
HI-506/507/506A/507A			1M
HI-508A/509A			4B
HI-562			1H
HI-1080/1085			4K
HI-1800A			4B
HI-1818A/1828A			4B
HI-1840			1M
HI-5040 thru HI-5051			4B

NOTE: "Package Code" references drawings on the following pages. Note that these do not correspond with the general package designations to be used in constructing the part number, which is explained in Ordering Information at the front of this book.

* Flatpack not available for commercial temperature range.

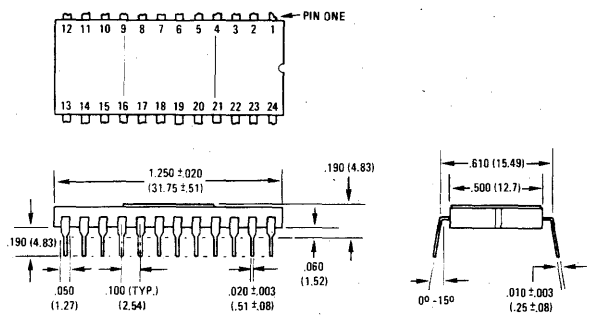
† 3B (Plastic D.I.P.) not available for military temperature range.

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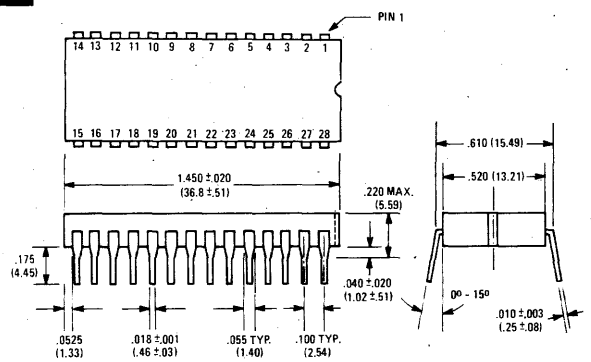
Package Dimensions

1. All dimensions in inches; millimeters are shown in parentheses.
2. All dimensions ±.010 (±0.25mm) unless otherwise shown.
3. Package codes are shown in black squares.

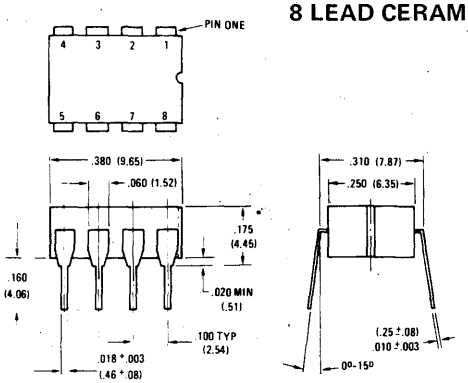
1H — 24 LEAD D.I.P.



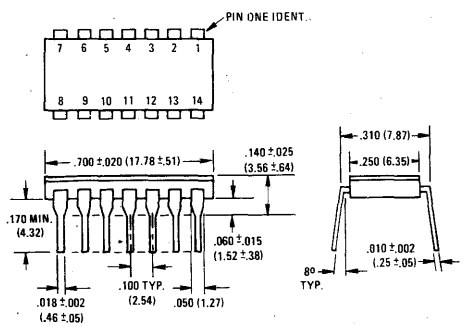
1M — 28 LEAD CERAMIC D.I.P.



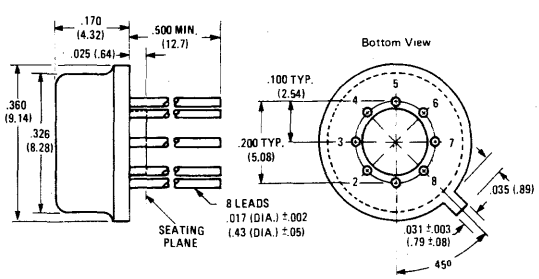
1N — 8 LEAD CERAMIC D.I.P.



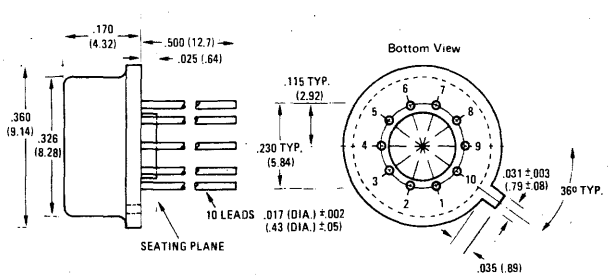
1S — 14 LEAD BRAZED D.I.P.



2A — TO-99 [.200 PC] (5.08 PC)

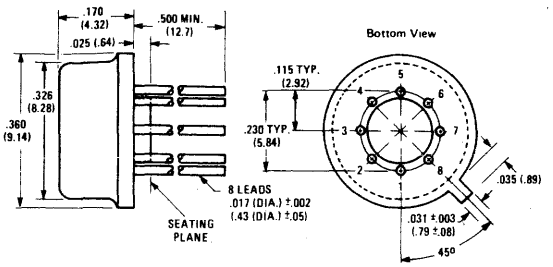


2D — TO-100 (10 LEAD)

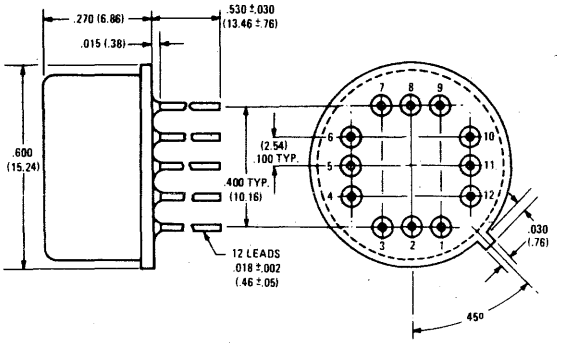


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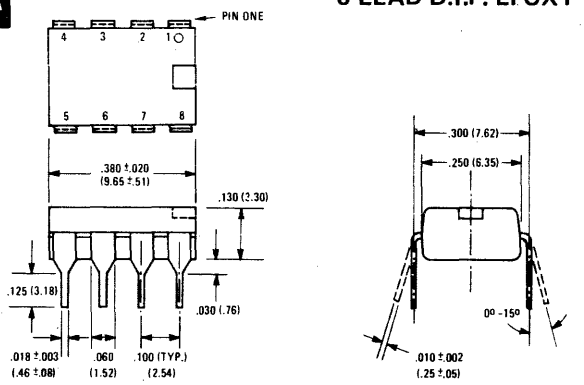
2E TO-99 [.230 PC] (5.84 PC)



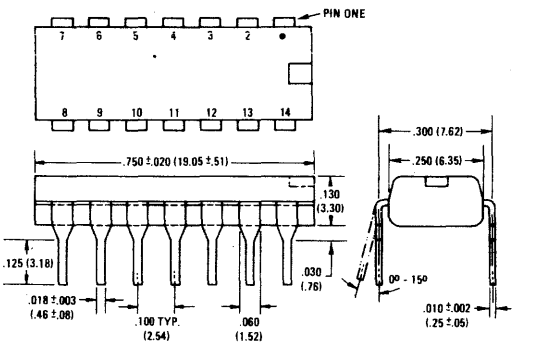
2G TO-8 (12 LEAD)



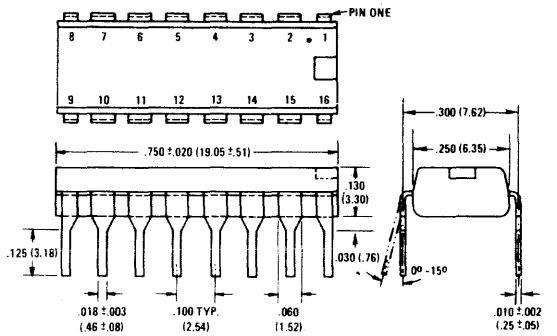
3A 8 LEAD D.I.P. EPOXY



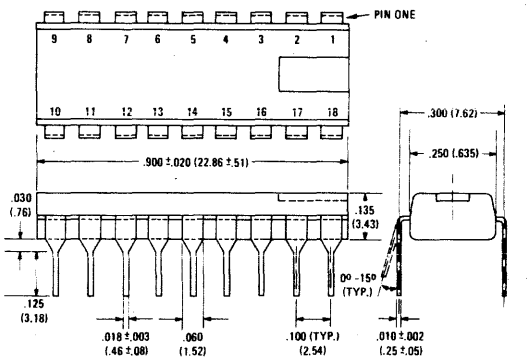
3B 14 LEAD D.I.P. EPOXY



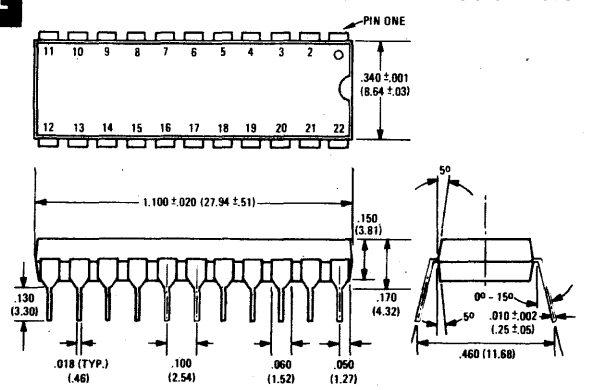
3C 16 LEAD D.I.P. EPOXY



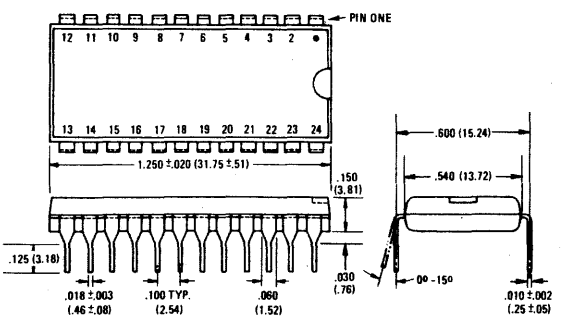
3D 18 LEAD D.I.P. EPOXY



3E 22 LEAD D.I.P. EPOXY

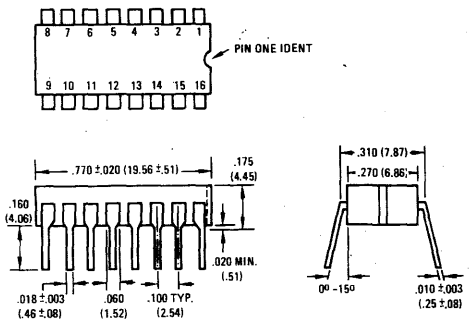


3F 24 LEAD D.I.P. EPOXY

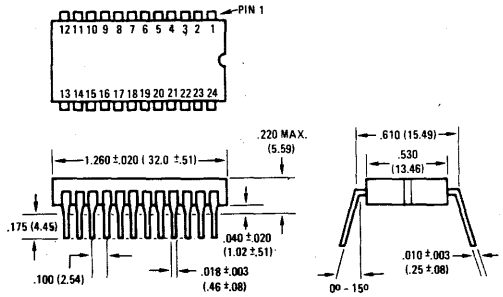


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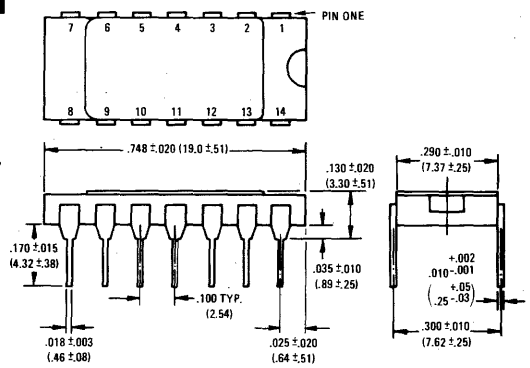
4B 16 LEAD CERAMIC D.I.P.



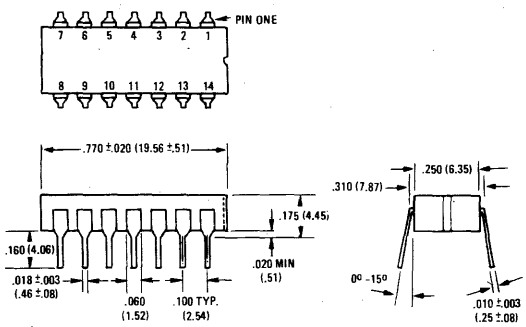
4K 24 LEAD CERAMIC D.I.P.



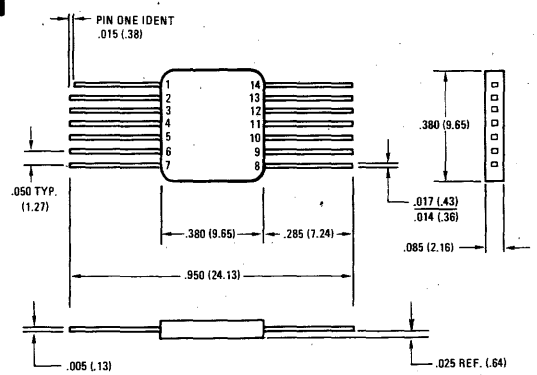
4Q 14 LEAD D.I.P. SIDE BRAZE



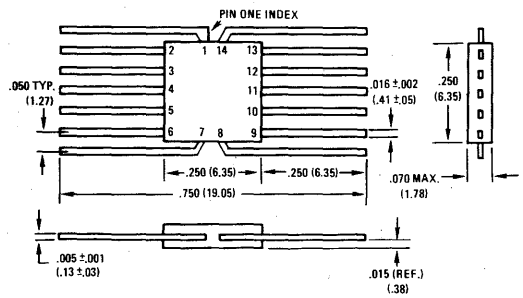
4U 14 LEAD CERAMIC D.I.P.



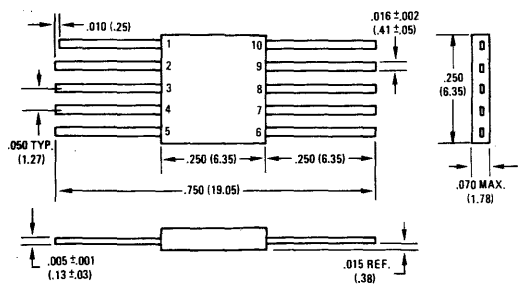
9R 14 LEAD METAL GLASS FLATPACK



9V TO-86 METAL BOTTOM



9W TO-91



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the first 16 bit, 8μs A/D (A-856);

the first 5½ digit dual slope A/D (109/110);

the first low cost 16 bit DAC (416);

the first 0.025% monolithic V/F (A-8400).

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282 Brokaw Road, Santa Clara, California 95050 Telephone (408) 244-0500 TWX 910 338-0254

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intech function modules

A-8400

Voltage-to-Frequency-to-Voltage Converter

DESCRIPTION

The A-8400 is a low-cost monolithic voltage-to-frequency converter that provides linear conversion of 0 to +10 V analog signals to a digital pulse train whose repetition rate is proportional to the analog voltage. This converter is designed to provide accurate and reliable performance, with versatile adjustment-free operation at low cost. A wide variety of input voltage scaling and output interfacing can be accomplished to satisfy many data acquisition and signal conditioning applications.

OPERATION

V/F Mode

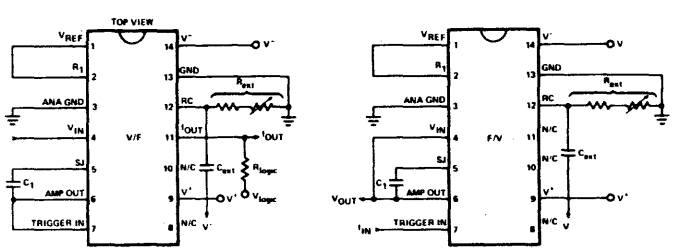
The analog input forces a current to flow through the input resistor into the integrating capacitor causing the output of the integrator to move in a negative direction. At a given voltage level, the comparator circuit triggers the timing reference network to turn the controlled current source on so that it discharges the integrating capacitor. As the capacitor discharges, the output of the integrator moves in a positive direction. When the timing reference has finished discharging the capacitor, the output of the integrator is positive and ready to start the process again for the next cycle. For current inputs into the summing junction (Pin 5), it is recommended for good temperature stability that an external R_{REF} be used between Pin 1 and $-V_{CC}$.

F/V Mode

As a frequency-to-voltage converter, the A-8400 accepts negative-going TTL pulses into the trigger circuit which starts the one-shot cycle (period=$T=R_{ext}\,C_{ext}$).

The current source forces current out of the summing junction for the one-shot period. The amplifier acts as a current-to-voltage integrator providing a voltage output proportional to the average current (also proportional to the input frequency). F/V linearity will be the same as in the V/F mode. Output ripple is controlled by the integrating capacitor (C_{INT}).

PIN CONNECTION



14 Pin DIP (Ceramic)

SPECIFICATIONS (Typical @ +25°C and ±15V Supplies Unless Otherwise Noted)

Parameter		A-8400
TRANSFER CHARACTERISTIC		$f_{out}=\frac{V_{IN}}{10}100kHz$
ACCURACY[6]		
Resolution		5 decades
Linearity, FS		
10kHz bandwidth		±0.025% max
100kHz bandwidth		±0.05% max
Monotonic		inherent
Scale Factor[1]		−0, +20%
Offset[1]		±10mV max
STABILITY[6]		
Scale Factor		
vs. Temperature	typ	±50ppm/°C
@ 10kHz	max	±100ppm/°C
vs. Power Supply		±300ppm/%
vs. Time/day		±100ppm
vs. Time/month		±200ppm
Offset		
vs. Temperature	typ	±3ppm/°C
	max	±10ppm/°C
vs. Power Supply		±100μV/%
vs. Time/day		±15ppm
vs. Time/month		±30ppm
RESPONSE – V/F Mode		
Settling Time, to 0.01%, FS Step		2 Cycles max[5]
Overload Recovery		10ms
RESPONSE – F/V Mode		Depends on C_{INT}/R_{IN} time constant
ANALOG INPUT (V/F)/OUTPUT (F/V)		
Voltage Range[2]		0 to +10V
Current Range		0 to +1mA
Overrange		Depends on external RC time constant
Configuration		Single-ended, referred to analog ground
Impedance (voltage input)		10kΩ nominal
Overvoltage Protection (V_{IN})		$\pm V_S$
OUTPUT (V/F)/INPUT (F/V)		
Frequency Range[2]		0 to 100kHz
Overrange		Depends on external RC time constant
Waveform[3]		Compatible with DTL, TTL & CMOS[7]
Fan Out[4] (V/F Mode)		1 TTL Load
Short Circuit Protection		Indefinite to GND
TEMPERATURE		
Rated		0 to +70°C
Operating		−25 to +85°C
Storage		−55 to +125°C
POWER SUPPLY		
Voltage – rated		±15V
– operate		±12 to ±18V
Current		±15mA @ ±15V

NOTES: 1. Adjustable to zero error. 2. Adjustable to other full scale input/output levels. 3. Output level determined by external pull-up resistor. 4. One TTL load unit is −1.6mA at LO (+0.4V) and +40μA at HI (+2.4V). 5. Of final frequency. 6. Applies to V/F & F/V modes. 7. Maximum output (V/F) = 6V.

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A-8402
Single Supply
Voltage-to-Frequency-to-Voltage Converter

DESCRIPTION

The A-8402 is a low-cost monolithic voltage-to-frequency converter that provides linear conversion of analog signals to a digital pulse train whose repetition rate is proportional to the analog signal.

Key features of the A-8402 V/F/V are its single power supply operation and the ability to be scaled over a 0 to +18V/0 to 100kHz range and virtually achieve 11 bit accuracy with a minimum number of components.

OPERATION

V/F Mode

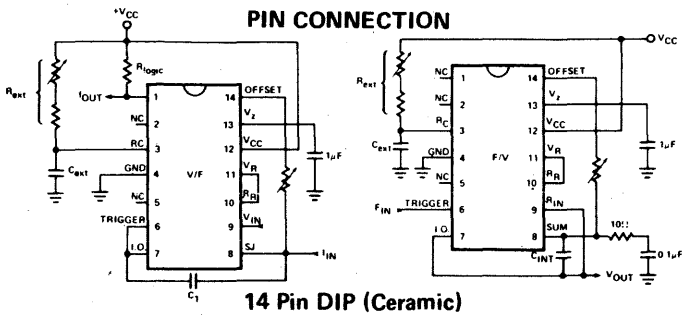
An improved form of the charge-balancing technique is used in the A-8402. The analog input forces a current to flow through the input resistor into the integrating capacitor causing the output of the integrator to move in a negative direction. At a nominal .7 volt level, the comparator circuit triggers the timing reference network to turn the controlled current source on so that it discharges the integrating capacitor. As the capacitor discharges, the output of the integrator moves in a positive direction. When the timing reference has finished discharging the capacitor, the output of the integrator is positive and ready to start the process again for the next cycle. For current inputs into the summing junction (Pin 8), it is recommended for good temperature stability that an external R_{REF} be used between Pin 11 and ground. It is also recommended that the internal R_{offset}, R_{REF} and the input resistor be used together for good TC performance. T_{OS} influences frequency stability; therefore low TC components should be used.

F/V Mode

As a frequency-to-voltage converter, the A-8402 accepts negative-going TTL-Level pulses into the trigger circuit which starts the one-shot cycle (period=$T_{OS}=R_{ext}\ C_{ext}$).

The current source forces current out of the summing junction for the one-shot period. The amplifier acts as a current-to-voltage integrator providing a voltage output proportional to the average current (also proportional to the input frequency). Output ripple is controlled by the integrating capacitor (C_{INT}). A low pass filter is recommended on Pin 8. Pin 13 may be used for external referencing (maximum current drain $<350\mu A$).

PIN CONNECTION



14 Pin DIP (Ceramic)

SPECIFICATIONS

(Typical @ +25°C and +12V Supplies, Unless Otherwise Noted)

Parameter		A-8402
TRANSFER CHARACTERISTIC		$f_{out}=\frac{V_{IN}}{10}F_{full\ scale}$
ACCURACY[1]		
Resolution		5 decades
Linearity, FS		
10kHz bandwidth		±0.05% max
100kHz bandwidth		±0.1% max
Monotonic		inherent
Scale Factor[2]		±15%
Offset		Note 2
STABILITY[1,8]		
Scale Factor		
vs. Temperature	typ	±50ppm/°C
@ 10kHz	max	±100ppm/°C
vs. Power Supply		±200ppm/%
vs. Time/day		±100ppm
vs. Time/month		±200ppm
Offset		
vs. Temperature	typ	±80ppm/°C
	max	±100ppm/°C
vs. Power Supply		±100µV/%
vs. Time/day		±15ppm
vs. Time/month		±30ppm
Bandgap Reference (V_Z=2.5V nom.)		±25ppm/°C
RESPONSE – V/F Mode		
Settling Time, to 0.01%, FS Step		2 cycles max[3]
Overload Recovery		10ms
RESPONSE – F/V Mode		Depends on $C_{INT}\cdot R_{IN}$ time constant
INPUT (V/F)/OUTPUT (F/V)		
Voltage Range[4,5]		0 to +10V
Current Range		0 to +1mA
Configuration		Single-ended
Impedance (voltage input)		17.8kΩ nominal
Overvoltage Protection (V_{IN})		$+V_{CC}$
OUTPUT (V/F)/INPUT (F/V)		
Frequency Range[4]		0 to 500kHz
Overrange		Depends on external RC time constant
Waveform[6]		Compatible with DTL, TTL & CMOS
Fan Out[7] – V_{sat}=0.4V		5 TTL Loads
– V_{sat}=1V		20mA
Short Circuit Protection		Indefinite to GND
TEMPERATURE		
Rated		0 to +70°C
Operating		–25 to +85°C
Storage		–55 to +125°C
POWER SUPPLY – V_{CC}		
Voltage – rated		+12V
– operate		+5 to +18V
Current		+20mA @ +12V

NOTES: 1. Applies to V/F & F/V modes. 2. Adjustable to zero error. 3. Of final frequency. 4. Adjustable to other full scale input/output levels. 5. F/V mode–min. V_{OUT}=0.4V. 6. Output level determined by external pull-up resistor. 7. One TTL load unit is –1.6mA at LO (+0.4V) and +40µA at HI (+2.4V). 8. Warm-up time = 5 min.

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Monolithic Voltage-Frequency Voltage Applications

Since the explosion of μP applications, many designers are looking for inexpensive, reliable multiplexed input sections that can be made compatible to their bussing system. The A-8402 is of particular interest here since it may operate from a single +5v supply and can be operated in a synchronous mode. Further advantages of the following scheme are increased TC performance, typically 25ppm/°C, and direct compatibility to microprocessor use.

Figure 1 details the hook-up of the A-8402. Note that the one shot is no longer a part of the circuit, deleting that portion of the TC error. C ext is deleted and R ext = 27K (this value is not critical). The clock cycle is not critical as long as it triggers the flip-flop.

Figure 2 shows the basic block diagram of an eight channel synchronous, multiplexed V/F system. It should be noted that the external clock frequency is dependent upon the number of input channels desired and is found from the equation:

$$Fce = (N)\ (F_{f.s.}),$$

where Fce = clock frequency

N = number of input channels

F_{fs} = full scale output of the A-8402.

Running many V/F converters synchronously from a single clock allows you to multiplex the outputs via parallel-to-serial transmission medium. After the falling edge of the divide-by-8 clock output, each V/F and its associated flip flop's Q output remain in their HIGH or LOW state until the next falling edge of the clock. At this time the MUX samples each V/F output in succession and transmits it to the demultiplexer, where it is decoded for parallel output. The one-shot clears the demultiplexer on the next falling edge of the clock, and the process repeats. In some cases you may have to strobe the demultiplexer's output into a latch.

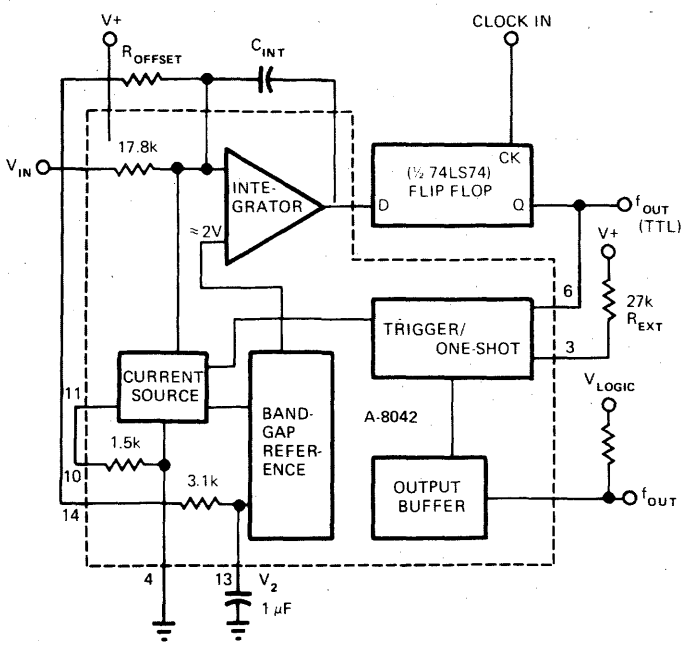


Fig. 1—In this synchronous operating scheme, the output frequency comes from either the A-8402's f_{OUT} pin or the flip flop's Q or $\overline{Q}$ outputs.

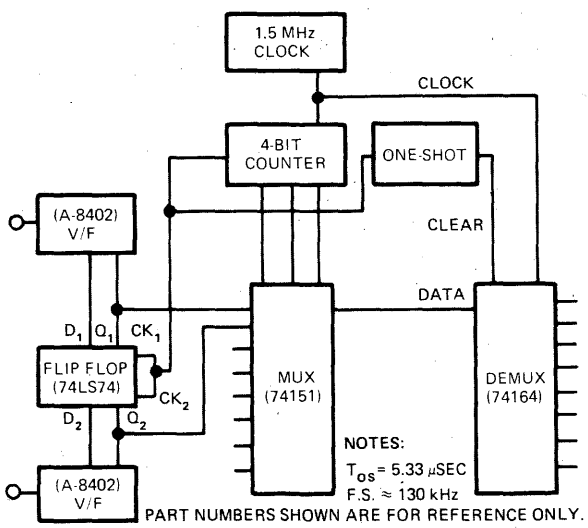


Fig. 2—By synchronizing several V/F's from a single clock, you can design a multiplexed data-transmission system.

MOTOROLA Semiconductors
3501 ED BLUESTEIN BLVD., AUSTIN, TEXAS 78721

MC14406
MC14407

Advanced Information

CMOS LSI

(LOW POWER COMPLEMENTARY MOS)

FULL DUPLEX 8-BIT
COMPANDED PCM CODEC

PULSE CODE MODULATION (PCM) CODEC

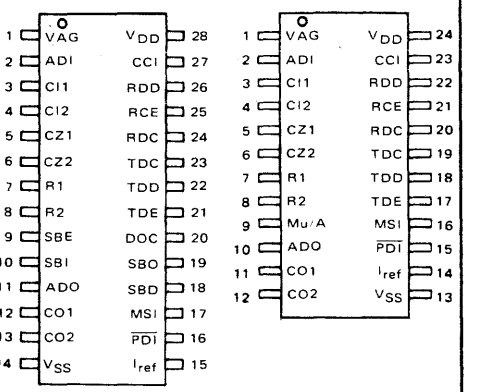
The MC14406 and MC14407 per channel PCM codecs are designed for 8000-samples-per-second, 8-bit-per-sample voice coding and decoding. These devices are full duplex and provide both Mu and A companding laws.

The transmit and receive data rates are independently selectable from 64 kHz to 3.088 MHz allowing direct interface to 24, 30, 32, and 48 channel digital frames.

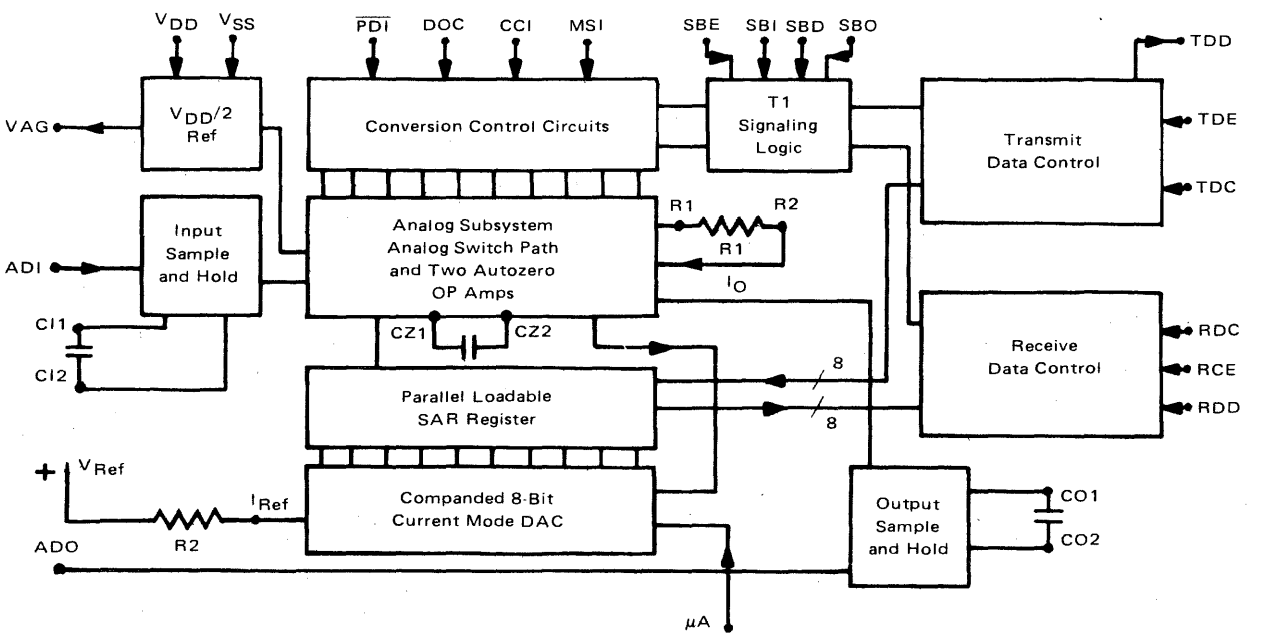
Both codecs are fabricated using CMOS technology for reliable low power performance. The MC14406 is the full feature device in a 28-pin package. The MC14407 provides a 24-pin package without signaling capabilites.

- Per Channel Full Duplex Capability
- Low Power Operation – 80 mW Typ
- Power Down Input (1.0 mW Max in Power Down Mode)
- Pin Selection of A-law and Mu-law Companding (MC14407)
- Single Power Supply Operation – 10 to 16 volts
- Zero Code Suppression
- Transmit and Receive Signaling Available (MC14406)
- Independent Transmit and Receive Clocks to 3.088 MHz
- Externally Selectable Full Scale
- On-Chip Auto Zero

PIN DESCRIPTION



BLOCK DIAGRAM



This is advance information and specifications are subject to change without notice. ©MOTOROLA INC., 1978

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DIGITAL ELECTRICAL CHARACTERISTICS

Characteristic		Symbol	V_{DD} Vdc	−40°C Min	−40°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit
Operating Current (R2 = 25 k)		I	12	–	–	–	8.0	–	–	–	mA
Power-Down Current ($\overline{PDI}$ = V_{SS})		I_{PD}	12	–	–	–	30	80	–	–	μA
Input Current											
CCI, RDD, RCE, RDC, TDC, $\overline{PDI}$		I_{in}	12	–	–	–	±0.00001	±0.3	–	–	μA
DOC, SBD, MSI, SBI, SBE		I_{inS}		–	–	–	+30	–	–	–	
(Internal Pull-Down Resistors)		I_{inD}		–	–	–	−0.00001	−0.3	–	–	
TDE, Mu/A-Law		I_{inS}		–	–	–	+0.00001	+0.3	–	–	
(Internal Pull-Up Resistors)		I_{inD}		–	–	–	−30	–	–	–	
Input Voltage	"0" Level	V_{IL}	12	–	–	–	5.25	3.60	–	–	V
			15	–	–	–	6.75	4.0	–	–	
	"1" Level	V_{IH}	12	–	–	8.4	6.75	–	–	–	V
			15	–	–	11	8.25	–	–	–	
Input Capacitance		C_{in}	12	–	–	–	5.0	7.5	–	–	pF
Output Drive Current	SBO										
V_{OH} = 11		I_{OH}	12	–	–	−2.0	−4.0	–	–	–	mA
V_{OH} = 13.5			15	–	–	−3.0	−8.8	–	–	–	
V_{OL} = 1.0		I_{OL}	12	–	–	2.0	4.0	–	–	–	mA
V_{OL} = 1.5			15	–	–	3.0	8.8	–	–	–	
Output Drive Current	TDD										
V_{OH} = 11		I_{OH}	12	–	–	−4.0	−8.0	–	–	–	mA
V_{OH} = 13.5			15	–	–	−6.0	−17.6	–	–	–	
V_{OL} = 1.0		I_{OL}	12	–	–	4.0	8.0	–	–	–	mA
V_{OL} = 15			15	–	–	6.0	17.6	–	–	–	

ANALOG ELECTRICAL CHARACTERISTICS (V_{DD} = 12 V)

Characteristic	Pin	−40°C Min	−40°C Max	+25°C Min	+25°C Typ	+25°C Max	+85°C Min	+85°C Max	Unit
Analog Ground Voltage	VAG	–	–	6.0	6.05	6.1	–	–	V
Source Current		–	–	–	200	–	–	–	μA
Sink Current		–	–	–	5.0	–	–	–	mA
Output Impedance		–	–	–	50	–	–	–	Ω
Reference Input Current	I_{ref}	–	–	50	100	200	–	–	μA
Input Offset Voltage		–	–	–	±10	+25	–	–	mV
Offset Voltage Drift		–	–	–	30	100	–	–	μV/°C
Input Impedance dc	ADI	–	–	1.0	10	–	–	–	MΩ
AC (Ω) CI = 0.002 nF, 1 kHz		–	–	–	80	–	–	–	kΩ
Lower Common Mode Ring		–	–	–	2.0	2.5	–	–	V
Upper Common Mode Ring		–	–	9.5	10	–	–	–	V
Sample Duty Cycle	ADO	–	–	–	3/16	–	–	–	–
Neutral Duty Cycle		–	–	–	13/16	–	–	–	–
Neutral Offset (From VAG)		–	–	−25	±25	+25	–	–	mV
Neutral Offset Drift		–	–	–	30	100	–	–	μV/°C
Source Current		–	–	–	200	–	–	–	mA
Sink Current		–	–	–	5.0	–	–	–	mA
Lower Common Mode Ring		–	–	–	2.0	2.5	–	–	V
Upper Common Mode Ring		–	–	9.5	10	–	–	–	V
Output Impedance		–	–	–	100	–	–	–	Ω
Settling Time to 3.0 V R and F		–	–	–	0.3	–	–	–	μs

MAXIMUM RATINGS (Voltages Referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	$V_{DD} - V_{SS}$	−0.5 to +18	Vdc
Voltage, Any Pin to V_{EE}	V	−0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin (Excluding V_{DD})	I	10	mAdc
Operating Temperature Range	T_A	−40 to +85	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

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RECOMMENDED OPERATING CONDITIONS

Parameter	Pin	Min	Typ	Max	Unit
DC Supply Voltage	$V_{DD} - V_{SS}$	10	12	16	Vdc
Convert Clock Freqency	CCI	128	128	512	kHz
Transmit Data Clock Frequency	TDC	128	2048	3088	kHz
Receive Data Clock Frequency	RDC	128	2048	3088	kHz
Input Sample Capacitor	CI1, CI2	0.001	0.002	0.010	μF
Output Sample Capacitor	CO1, CO2	0.001	0.002	0.010	μF
Unit Step Size = Full Scale/4096	ADO	0.36	0.85	1.2	mV
Full Scale Voltage (V_{DD} = 15 V)	ADO	1.5	3.5	5.0	Vp
Load Bias Resistor	VAG	2.0	–	–	kΩ
Bypass Capacitor	VAG	–	0.1	–	μF
Auto Zero Capacitor	CZ1, CZ2	–	0.002	–	μF

SYSTEM PERFORMANCE A-to-D through D-to-A (R1 = 25 kΩ, R2 = 2.27 kΩ, T_A = 25°C)

Characteristic		Min	Typ	Max	Unit
Signal to Noise Ratio	+3.0 to −30 dBm	33	36	–	dB
$\frac{S+N+D}{N+D}$	−40 dBm	27	30	–	
C Message at f = 1020 Hz	−45 dBm	22	25	–	dB
Deviation from Level Linearity	+3.0 to −35 dBm	−0.5	–	+0.5	dB
	−35 to −45 dBm	−0.10	–	+1.0	dB
Idle Channel Noise (ADI = VAG)		–	0	12	dBmC
Quiet Code		–	–	–	

VAG – Analog Ground Output (V_{DD}–V_{SS})/2. VAG is the output of the internal (V_{DD}–V_{SS})/2 voltage reference. A pull-up load resistor and bypass capacitor may be required if this output is to be used elsewhere in the system. This pin serves as the analog ground.

ADI – Analog Data Input. The band-limiting input filter between the channel unit hybrid and the codec drive pin 2. Driver source impedance should be 600 Ω or less. This is the voice input to the codec and will be sampled at 8.0 kHz.

CI1, CI2 – Input Sample Capacitor. The input sample capacitor is connected to these pins. A 2000 pF silver mica capacitor is recommended.

CZ1, CZ2 – Auto Zero Capacitor. The auto zero circuit requires a 2000 pF capacitor between these pins.

R1, R2 – Gain Resistor. The V-to-I conversion resistor is connected between these pins. Gain is established by the ratio of this resistor and the resistor at pin I_{ref}.

Mu/A – Mu-Law/A-Law Select (Internal Pull-Up). Selection of Mu-law or A-law coding is provided for logic control. An internal pull-up provides Mu-law output. An external connection to V_{SS} provides A-law operation.

SBE – Signal Bit Enable (Internal Pull-Down). SBE controls the insertion of transmit signaling bits into the transmit data register. When taken high, the next transmit word will contain the SBI pin level in the LSB position rather than the last bit of the PCM word. If kept high, the SBI data will be inserted in succeeding conversions until one conversion after it is brought low. It can be used for on-hook signaling or A and B signaling in D3 banks.

SBI – Signal Bit Input (Internal Pull-Down). SBI is the data input for transmitting signaling bits. The level of SBI will be latched on the leading edge of SBE, or by the internal latch data pulse if SBE is held high. If SBE is pulsed, the leading edge of SBE will latch SBI, and load it into the next transmit word.

ADO – Analog Data Output. ADO outputs the received PAM sample for three convert clock cycles beginning with MSI. It then returns to the output neutral voltage which may be a few millivolts different from VAG1.

CO1, CO2 – Output Sample Capacitor. The output sample capacitor is connected between these pins. A silver mica capacitor of 2000 pF is recommended.

V_{SS} – Most Negative Supply. This is the most negative supply pin, and the digital ground. All digital inputs and outputs will swing the full supply voltage.

I_{ref} – Current Reference Input. A reference current of 50 to 200 μA sets the full scale DAC current. An 80 μA input current corresponds to 1.28 mA full scale DAC current at pin R2.

$\overline{PDI}$ – Power-Down Input. $\overline{PDI}$ deactivates the codec when pulsed to V_{SS}. In the power-down mode the analog circuitry bias is turned off and the digital clock inputs are disabled. Power-down dissipation is less than 1.0 mW.

MSI – Master Sync Input (Internal Pull-Down). The MSI leading edge resets the entire chip to the initial cycle (0000). The chip continues operation on the next leading edge of data and convert clock. MSI also resets the output data multiplexer to the transmit word sign bit.

SBO – Signal Bit Output. SBO outputs the LSB of the receive data register. The LSB may be sampled externally during the first three convert clocks after MSI or used as a trigger pulse in off-hook applications.

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SBD — Signal Bit Decode (Internal Pull-Up). Signal bit decode allows the control of the 1/2 LSB or LSB centering required in sample decode cycles. It is loaded by the RCE edge in each cycle. If a zero is entered, the next decode cycle adds 1/2 LSB to the 8-bit received word to center the quantization error of the 8-bit received sample when the output sample capacitor is charged. If a 1 is loaded by RCE, the 1/2 LSB is not added, and the LSB is forced to a 1 to form a centered error 7-bit output, and the LSB is ignored and assumed to be signaling information. (For codes 1111111X or 0111111X, the LSB is disabled for SBD high.)

DOC — Decode Only Control (Internal Pull-Down). DOC is normally tied low. When high, it configures the device to skip the eight convert clocks used for A-to-D conversion. The operating cycle is then two clocks for PAM output at ADO and six clocks for charging the next output sample. The device may be used to do as many as four decode cycles in a 125 μs/period with an external transmission gate selector.

Received Data is loaded into the transmit data register at MSI when in DOC mode, so DOC can be used as a digital loop back control.

TDE — Transmit Data Enable (Internal Pull-Up). The Transmit Data Enable is a three-state control for the transmit digital output. A number of codec outputs can be interleaved into a serial stream by connecting the outputs and controlling TDE with a 1-of-N decoder. It will provide switching characteristics capable of 3.088 MHz operation.

TDD — Transmit Digital Data. The Transmit Digital Data rate is controlled by the data clock input, and is frame aligned with the Master Sync Input. If data clock is at 1.544 MHz, and convert clock is at 128 kHz, the new sign bit will be output beginning with the leading edge of convert clock 8, and the 8-bit word repeated throughout the convert cycle at the data clock rate. The data word is inverted offset binary with zero code suppression. See Conversion and Data Timing.

TDC — Transmit Data Clock. TDC sets the digital data rate of the codec. The transmit data stream will provide a continuous repetition of the current transmit data word at the TDC bit rate, beginning with MSB first and synchronized with the last MSI. The new data word is loaded and serially output at mid-cycle or on the leading edge of convert clock 8.

RDC — Receive Data Clock. RDC controls the receive data register. It clocks the receive-data register on the trailing edge under the control RCE. It is often connected to TDC.

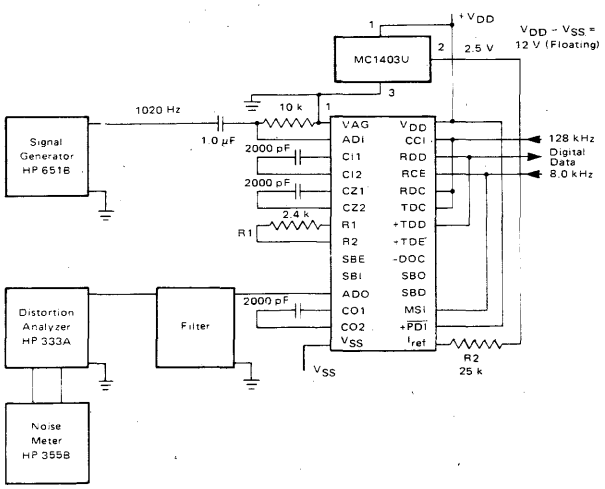
RCE — Receive Clock Enable. The rising edge of RCE triggers the receive data register to accept a new data input. After the rising edge of RCE, the data on RDD is loaded into the Receive Data Register on the next eight trailing edges of RDC. The ninth clock transfers the new 8-bit word to an internal intermediate register and frees the Receive Data Register for a new RCE.

RDD — Receive Digital Data. RDD is the input to the receive data shift register. It is controlled by RCE. The register is clocked on the trailing edge of RDC. The data format is sign bit first, inverted offset binary code.

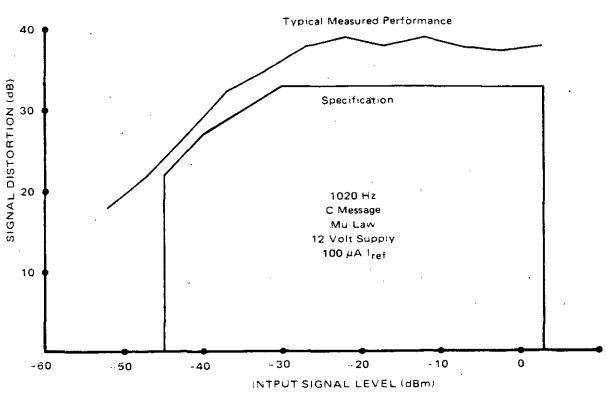
CCI — Convert Clock Input. CCI controls the conversion sequence. A 128 kHz clock will produce 64K-bits/s full duplex operation and a 256K-bits/s clock will produce 64K-bit operation for two channels. Sixteen clocks represent one chip cycle from MSI to MSI.

V_{DD} — Most Positive Supply. V_{DD} is typicallv 12 V with an operation range of 10 V to 16 V. All logic outputs swing the full supply voltage.

TEST CIRCUIT
MC14406 NOISE PERFORMANCE DATA



NOISE PERFORMANCE OF MC14406



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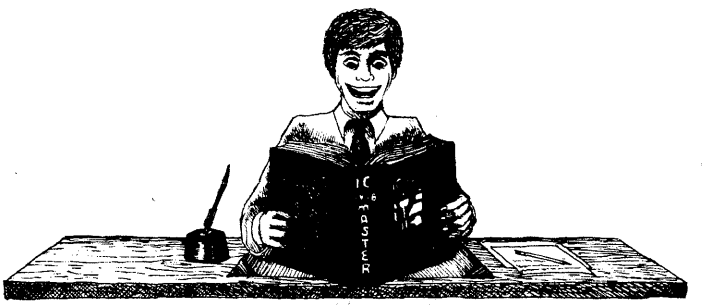
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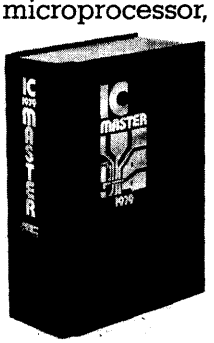
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BI-FET Technology
and Processing
Product Selection Guide
Ordering Information



Automatic Probe and Test Station for a linear 4 inch wafer.

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The BI-FET Process

What's New about BI-FETs?

The desire for a monolithic FET, to incorporate in linear circuit design, has been around for many years. In fact, many unsuccessful attempts were made using standard bipolar base and emitter diffusions. The major problem with this approach is the inability to control the all important pinch-off voltage, which is proportional to the concentration of the dopant in the channel.

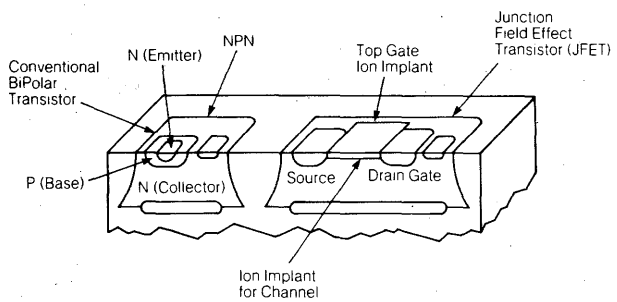
The key to the BI-FET process, which National pioneered six years ago, is the use of ion implantation of the channel and gate regions. By implanting the channel, very precise control of the channel dopant is achieved, and therefore the pinch-off voltage is maintained uniform in volume production. This breakthrough in semiconductor technology allowed the first BI-FET op amp family to be introduced in 1975.

BI-FET II

In addition to mastering the ion implant technology, National Semiconductor uses special processing techniques to reduce the input offset voltage, reduce the noise, and enhance the speed capabilities. One such process, which is now in full production, is the use of laser trimming of resistors at the input stage to reduce the input offset voltage down to 2.0 mV or less. This is BI-FET II.

Presently, at National, there are several new processing investigations which promise that the performance of future BI-FETs from National will be even more startling than the present devices. And it goes without saying, the development of these new techniques will be consistent with high volume production, resulting in another important feature—low cost to the user.

Ultra-matched JFETs and BiPolar Transistors



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The BI-FET Process

Advantages to Designers

Why use BI-FET and BI-FET II?

The chart below points out the major features of BI-FET op amps and advantages offered to designers:

Performance Features	Advantages to Designers
Low input bias current	Minimum current loss into amplifier inputs from feedback network or input signal source.
Low input offset current	Reduces concern for matching impedances on each amplifier input.
High input impedance	Allows use of high impedances for input and feedback networks and driving sources.
Low V_{os} options	Minimizes dc output errors in high gain configurations and can eliminate need for offset adjustments.
Low input noise voltage and current	Allows amplification of very small signals.
Internal compensation	Reduces component count by not requiring an external capacitor for stable, trouble free operation.
Wide bandwidth	Permits more gain at higher frequencies and reduces square wave rise times.
High slew rate	Allows large sinusoidal output voltage swings (±10V) at high frequencies (200 kHz) without slew distortion.
Low distortion	Low input stage gm and class AB output stage yield negligible distortion.
Fast settling time	Increases sampling rate in data acquisition system.
Ability to drive C loads	The amplifier can drive capacitors (filters, sample and holds) or relatively long lengths of cable without stability problems or ringing.
Short circuit protection	Will survive an output short indefinitely
Static discharge blowout proof	No special handling considerations necessary. JFETs are rugged, unlike CMOS.
Insensitive to RFI	Allows normal operation in RF systems and eliminates audio rectification problems.
Pin-for-pin compatibility	With all popular devices.
Low cost	One advantage every designer wants.

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Advantages of the BI-FET Process

The BI-FET process which combines bipolar transistors and junction FET's brings many advantages to design engineers. The most obvious advantage is the low input currents and corresponding high input impedance. In addition it can be shown that for an input stage running at the same current, a JFET input stage will be 20 times faster than the equivalent bipolar stage. Thus larger bandwidths and slew rates are obtained using JFET's.

Also, because a JFET does not have a "forward biased" junction as does a normal transistor, the JFET input stage is immune to rectification of spurious RFI which hampers some Bipolar small signal amplifier designs which must operate in an RFI environment.

In addition to the excellent input stage, National's LF355, LF356 and LF357 series use a JFET output stage. By eliminating the PNP transistor at the output, excellent settling time, low AC output impedance at high frequencies, and the ability to drive large capacitive loads results.

BI-FET II, the laser trimmed BI-FET op amp, attacks the other enemy of the circuit designers—offset voltage. Using laser trimming at the JFET input stage, offset voltage can be reduced to less than 2.0 mV, a remarkable achievement for a FET input amplifier.

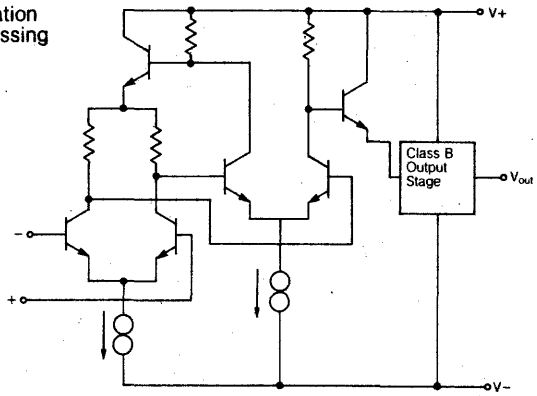
These features all combine to make BI-FET the future for all circuit designers using operational amplifiers.

Evolution of the Monolithic OP AMP

Innovations by National Semiconductor— The Linear Leader

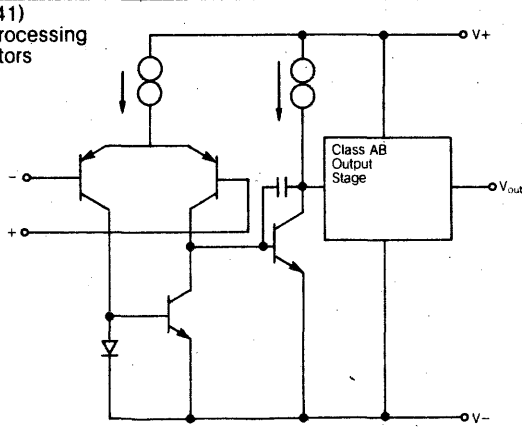
The Original—LM709

- ☐ First monolithic IC to be mass produced
- ☐ Required external compensation
- ☐ Used standard bipolar processing



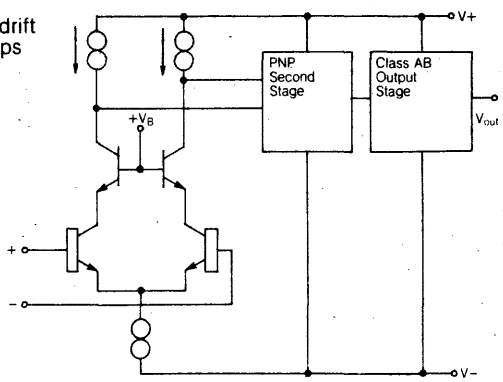
An Improvement—LM101 and LM741

- ☐ Internally compensated (LM741)
- ☐ Improved circuit design and processing
- ☐ First use of lateral PNP transistors



Super Beta—LM108 and 108A

- ☐ Innovative processing—first super beta transistors
- ☐ First to guarantee offset voltage drift
- ☐ Lowered bias current to nanoamps

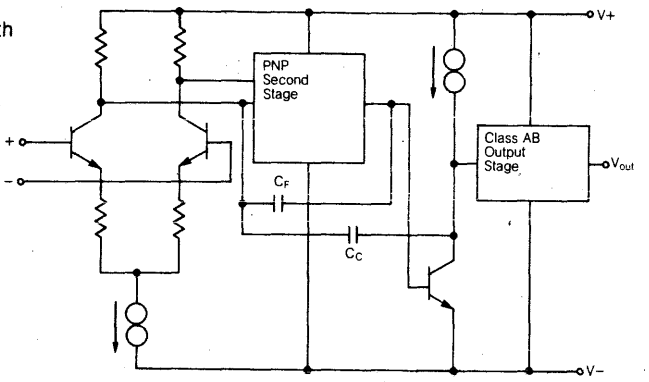


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Evolution of the Monolithic OP AMP

Wide Bandwidth—LM118

- ☐ First use of feedforward capacitors in a monolithic IC to improve speed
- ☐ High slew rate
- ☐ Wide bandwidth

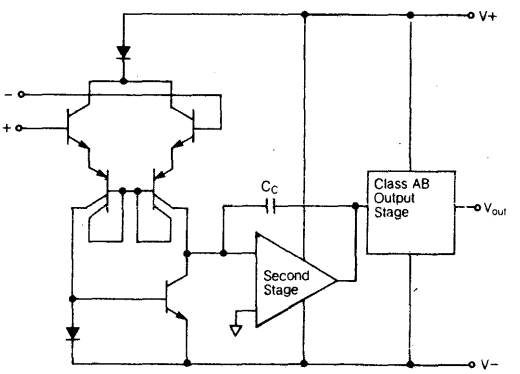


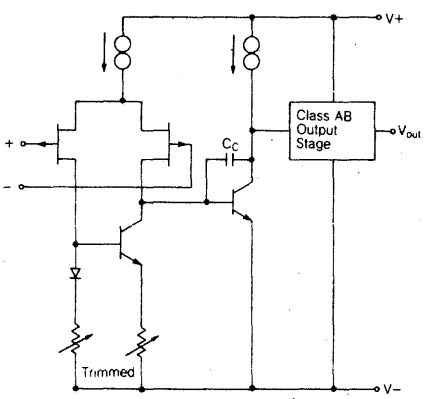
BI-FET II—Laser trimmed BI-FET op amps: LF351, LF353, LF347

- ☐ Complete family of singles, duals, and quads
- ☐ Small IC dies resulting in low cost
- ☐ Compatible pin-outs with existing duals and quads
- ☐ JFET inputs for withstanding input transients
- ☐ Laser trimming to obtain low offset voltage
- ☐ Fast slew rate
- ☐ Wide bandwidth and wide full power bandwidth
- ☐ Internal compensation
- ☐ Excellent RFI rejection
- ☐ Rugged handling capability
- ☐ Excellent noise voltage and noise current

Linear LSI—LM124, LM3900, LM148, LM146

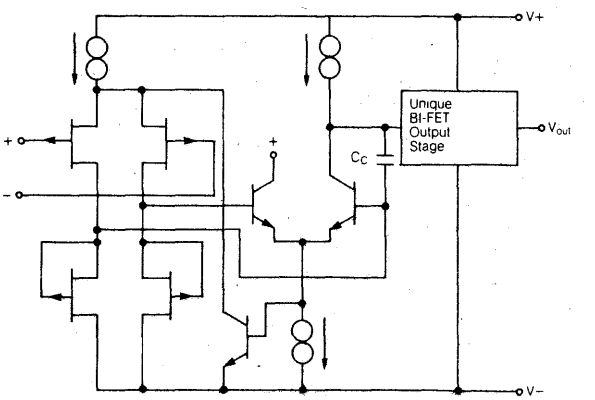
- ☐ First small die size cell enabling low cost dual and quad op amps to be manufactured
- ☐ Excellent general purpose perormance
- ☐ Performance programming capability (LM146)
- ☐ LM148 Amplifier cell shown



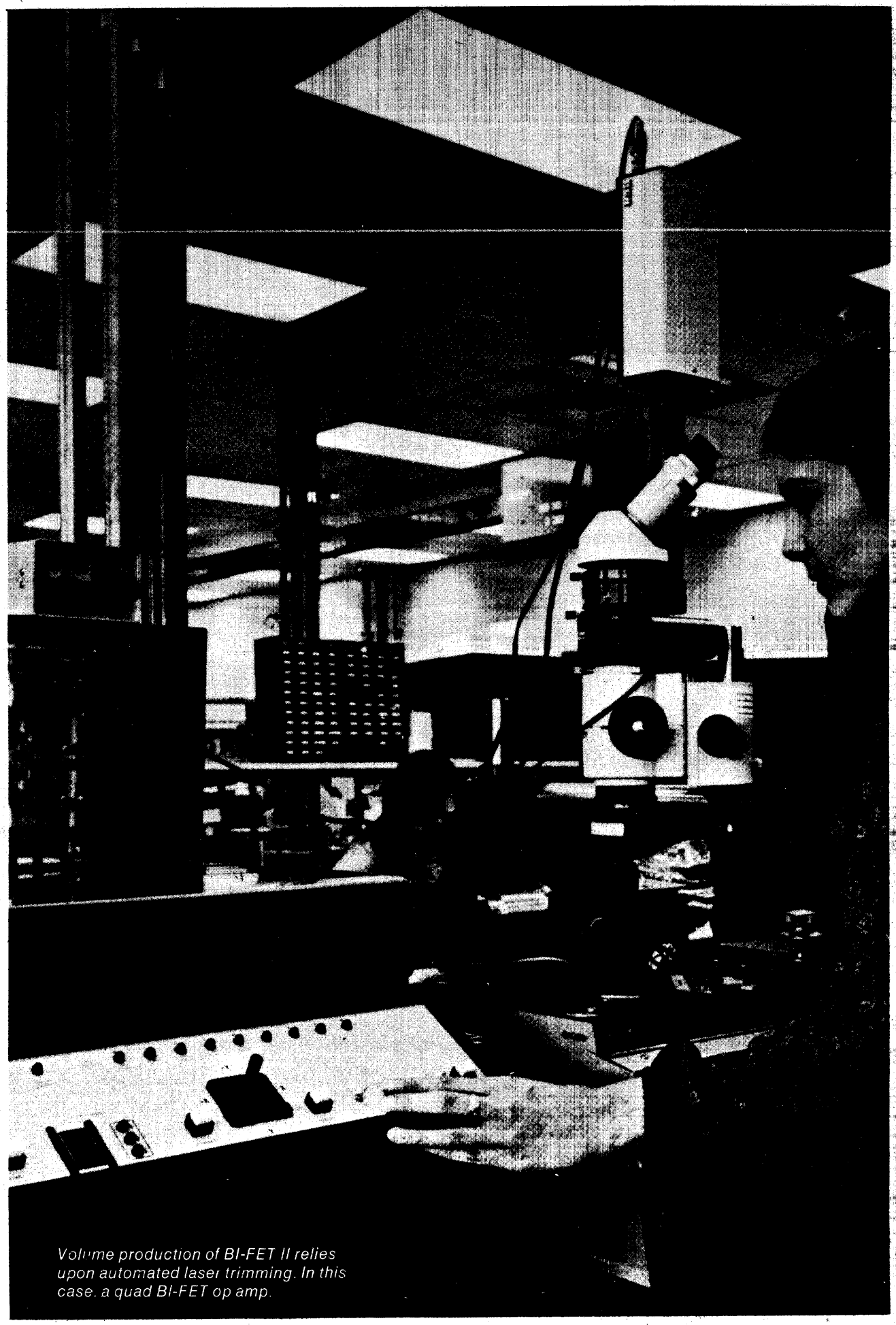


BI-FET—LF155, LF156, LF157

- ☐ First designs to combine bipolar transistors with high voltage junction FETs
- ☐ Innovation in processing and circuit design resulting in industry's lowest bias current, highest slew rates, highest capacitive load, drive capability and low cost for monolithic ICs.
- ☐ Very low noise voltage and current.

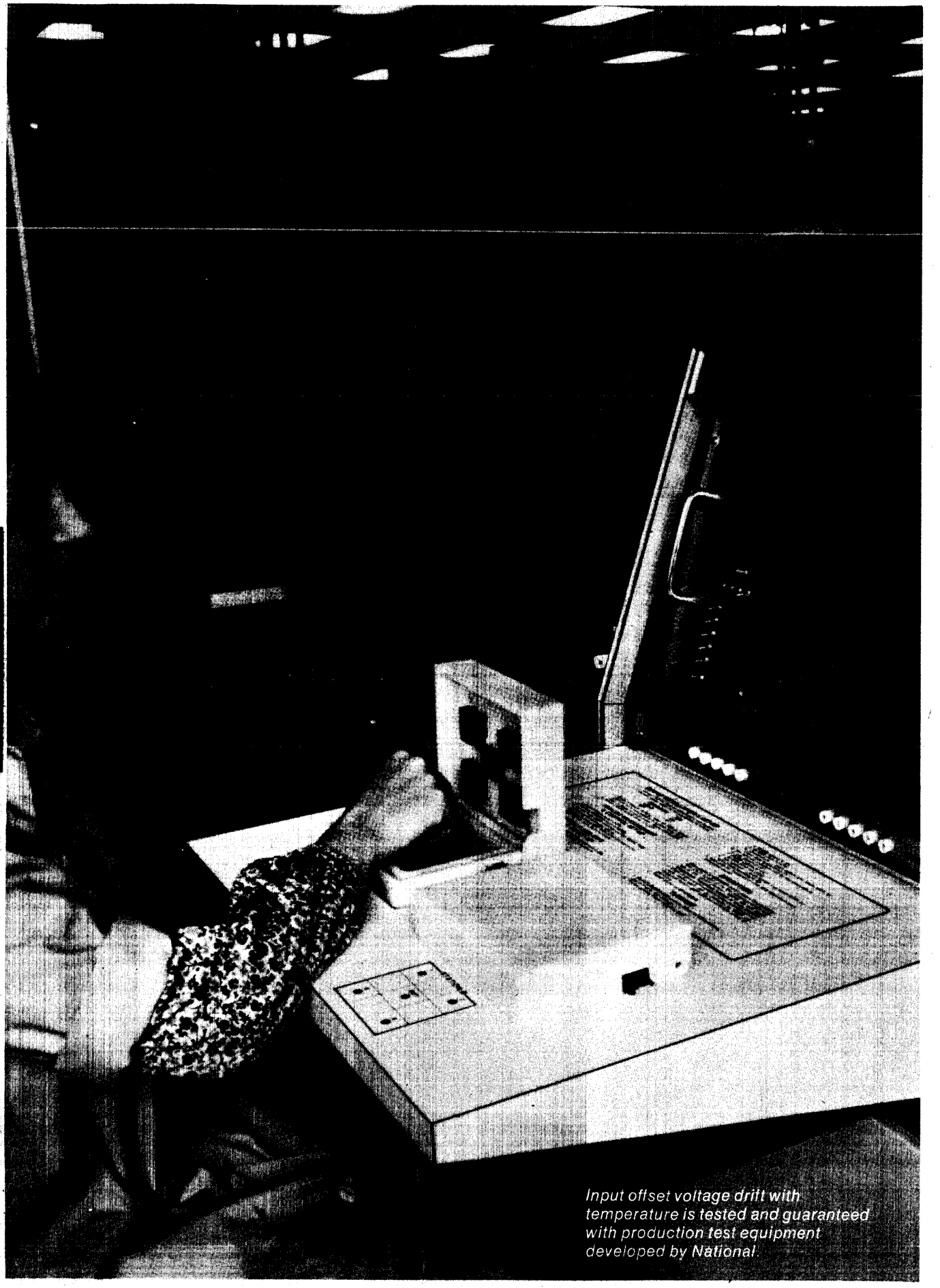


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Volume production of BI-FET II relies upon automated laser trimming. In this case, a quad BI-FET op amp.

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Input offset voltage dritt with temperature is tested and guaranteed with production test equipment developed by National.

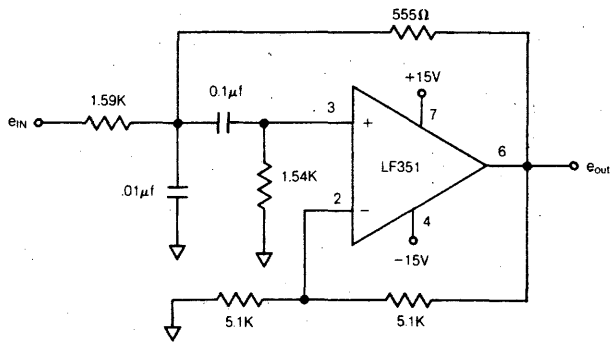
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Active Filters

National's high performance BI-FET op amps allow engineers to design RC active filters with fewer limitations on component selection. Some key performance features of interest to active filter designers are:

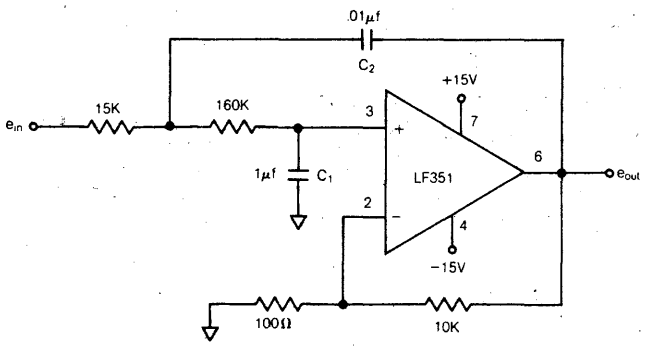
- ☐ BI-FET op amps, being very close to "ideal," allow the filter designer the ease of using less cumbersome filter design equations that rely upon the "ideal"op amp.
- ☐ The high input impedance and extremely low input bias current attendent with BI-FET permits the use of high value resistors, and consequently, low value capacitors. The use of low value capacitors is attractive due to their smaller size, lower cost, ease of availability, and precision.
- ☐ The low offset voltage, particularly with the BI-FET II series, and negligible offset current on all the National BI-FET devices, make them ideal for DC coupled filters such as lowpass sections.
- ☐ Low noise. Always a plus in any design, but particularly in bandpass and lowpass filter designs to maintain a high signal to noise ratio.
- ☐ Wide gain bandwidth product. This not only simplifies the filter design by allowing the designer to assume the "ideal" op amp case, but further extends the upper fxQ (frequency-Q product) previously obtainable. In any filter design, the fxQ product of any pole or zero should be less than five percent of the gain-bandwidth product of the op amp to assure a predictable filter response. The higher the gain-bandwidth product, the easier the design becomes.
- ☐ High slew rate. Not only does this feature allow for large sinusoidal output swings (±10 V) without slew limitations (distortion) up to 200 kHz, but it also relieves the problems associated with high Q sections and interstage connection where the signal swings may be large. This is particularly helpful when designing high Q notch or bandpass filters.
- ☐ Duals and Quad op amps. A real pc board space and money saver for multi-stage networks.

Single Amplifier Non-Inverting Bandpass



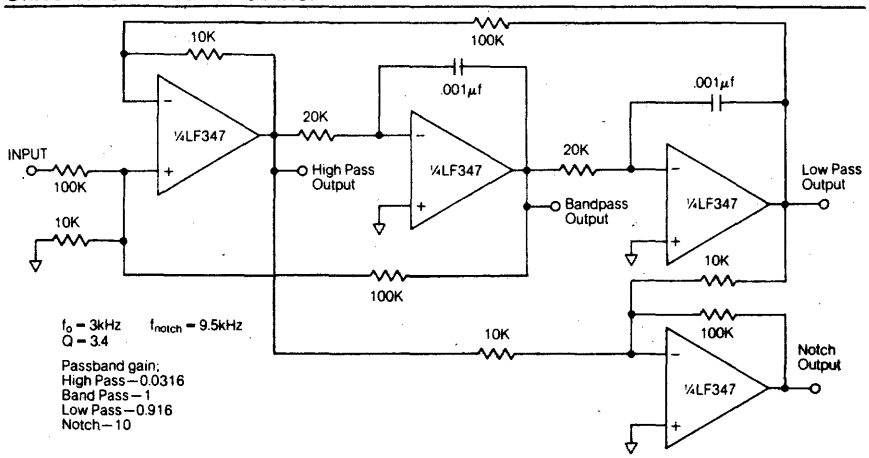
f_o = 20kHz, Q = 10, Av = +1

Single Amplifier High Gain-Lowpass



f_c = 10Hz, Q = .707 (maximally flat response)
Av = +100

Universal State Variable Filter



Specific Audio Applications

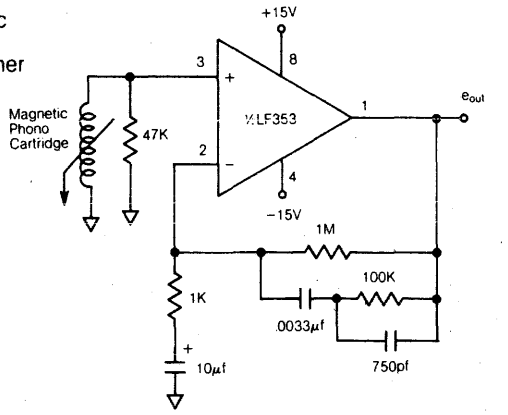
Audio

Audio systems require a frequency response bandwidth from 20Hz to 20kHz. All National BI-FET op amps possess the dynamic AC characteristics to provide both versatility and excellent performance over this frequency range. Some of the audio performance highlights are listed below:

- ☐ Wide bandwidth allows a closed loop gain of up to 200 for flat response over a 20kHz bandwidth
- ☐ No slew rate limitation problems.
- ☐ Low harmonic distortion as a result of a low gm input stage and class AB output stage.
- ☐ Low voltage and current noise provide quality sound reproduction.
- ☐ Ability to drive large capacitive loads—the LF356 can drive up to 0.01 μF without problems, making it an ideal amplifier for driving long cables.
- ☐ The input stage, being insensitive to RFI, eliminates the audio rectification dilemmas so often found when a pre amp detects and amplifies local radio signals.
- ☐ The high power supply ripple rejection and input common mode rejection eliminate hum problems.
- ☐ The availability of dual and quad devices simplifies stereo and four channel system designs.

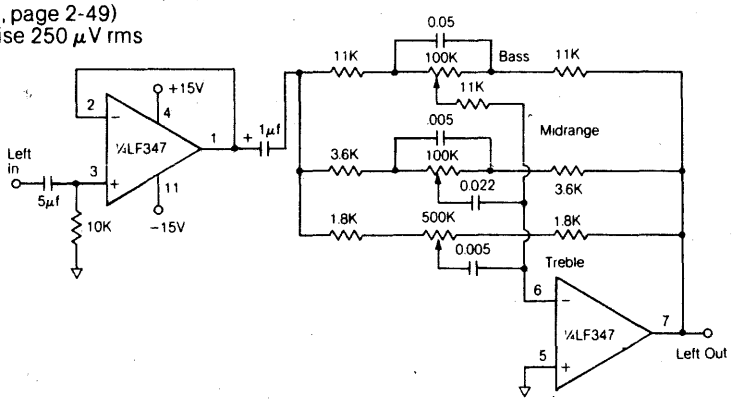
RIAA Equalization Preamp

- ☐ THD 0.05% from 20 Hz to 20 kHz
- ☐ Output noise voltage 220 μV rms (dc to 20 kHz)
- ☐ Duplicate for other channel using other half of LF353



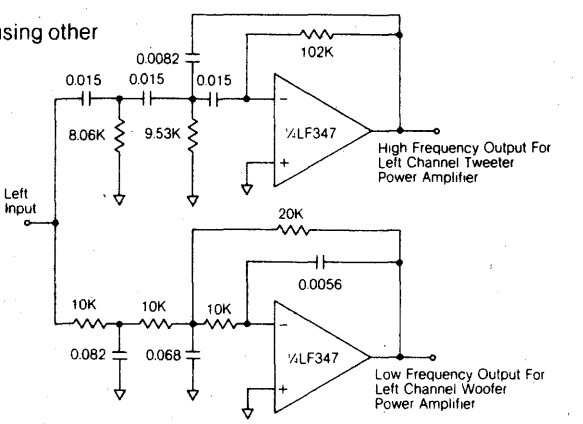
Three Band Tone Control

- ☐ Duplicate for right channel using other two amplifiers of the LF347
- ☐ Circuit performance curve (Audio Handbook, page 2-49)
- ☐ Output noise 250 μV rms



3rd Order Active Crossover Network

- ☐ Crossover frequency 500Hz
- ☐ Passband gain unity
- ☐ Duplicate for right channel using other half of the LF347



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Specific Data Acquisition Applications

Fast Sample and Hold

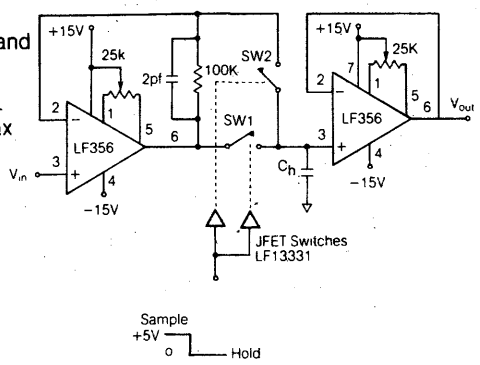
☐ Acquisition time (T_A) =

$$\left[\frac{2\,R_{on}\,V_{in}\,C_h}{S_r}\right]^{1/2}$$

where R_{on} is on resistance of SW 1 and S_r is slew rate provided that:

$$V_{in} < 2\,R_{on}\,C_h\,S_r \text{ and } T_A = \frac{V_{in}\,C_h}{I_{out}\,max}$$

if not: $T_A = \frac{V_{in}\,C_h}{20\ mA}$



Improved CMRR Instrumentation Amplifier

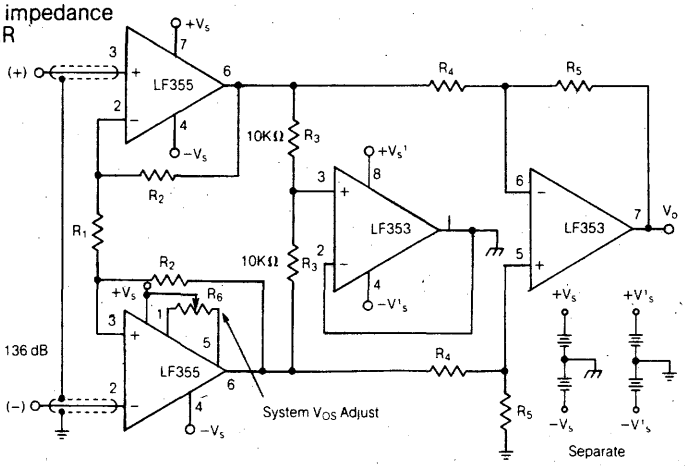
☐ Very high input impedance
☐ Very High CMRR

$A_V = \left(\frac{2R_2}{R_2} + 1\right)\frac{R_5}{R_4}$

And ⏚ Are Separate Isolated Grounds

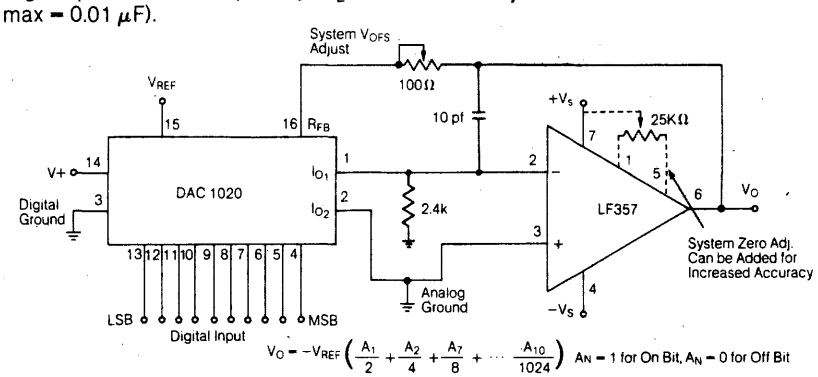
Matching of R_2s, R_4s and R_5s Control CMRR

With Av = 1400, Resistor Matching = .01%: CMRR = 136 dB



LF356 as Output Amplifier in D/A Systems

☐ Minimizes system errors due to bias current.
☐ Fast settling output.
☐ High capacitive drive capability (C_L max = 0.01 μF).



Data Acquisition

Operational amplifiers can perform well in a multitude of functions in data converters and complete data acquisition systems. In any of these systems, minimum error contribution by the amplifier is of maximum concern. National's line of BI-FET devices offers amplifiers suitable for use in high accuracy systems.

☐ Low input bias and offset currents useful in system output amplifiers or current-to-voltage converters for current mode DACs. Also ideal for sample and hold amplifiers used in data acquisition systems.
☐ Fast settling time where minimum conversion time is of prime importance.
☐ High common mode rejection for instrumentation amplifiers.
☐ High input impedance makes impedance translation easy.
☐ Low noise for signal conditioning.

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Specific Applications

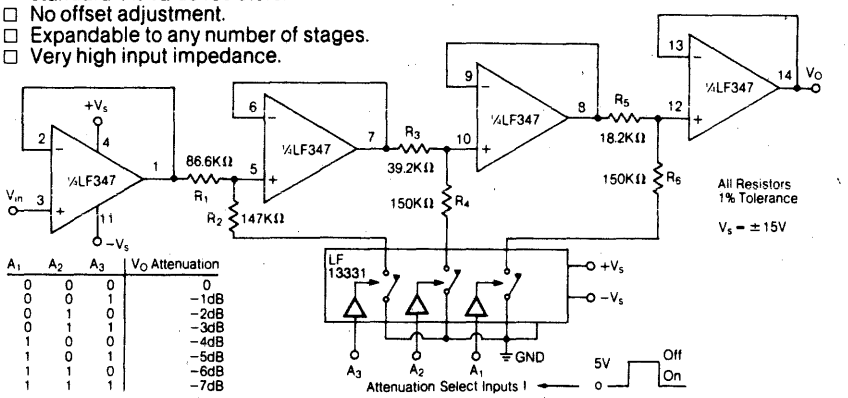
Instrumentation Circuits

Instrumentation circuits demand operational amplifiers with excellent characteristics in all areas of performance. Some of the major features of National's BI-FET line that apply to instrumentation needs are:

- ☐ High open loop gain combined with low noise at low frequencies results in high gain amplifiers with good signal-to-noise characteristics essential to all sensitive instrumentation applications.
- ☐ Low bias current. The requirement for precision long time integrators, logarithmic converters, and multipliers is easily satisfied with National BI-FETs.
- ☐ Wide bandwidth and fast slew rate op amps are needed to accurately amplify fast varying input signals.
- ☐ The high input impedance, large common mode range and power supply rejection inherent in National BI-FET op amps are especially useful for transducer amplifiers.
- ☐ Most instrumentation systems require more than one amplifier. This need is satisfied by National's complete line of single, dual and quad BI-FET op amps, covering all combinations of input offset voltage, bandwidth, low power, and more. A glance at the BI-FET selection guide will quickly find the correct device for your design.

Precision attenuator with attenuation digitally selected

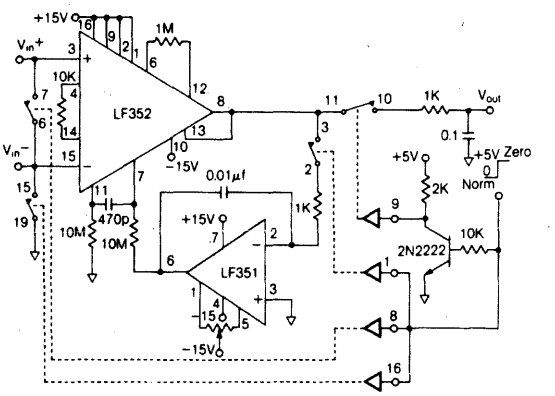
- ☐ Accuracy of better than 0.4% with standard 1% value resistors.
- ☐ No offset adjustment.
- ☐ Expandable to any number of stages.
- ☐ Very high input impedance.



A1	A2	A3	Vo Attenuation
0	0	0	0
0	0	1	-1dB
0	1	0	-2dB
0	1	1	-3dB
1	0	0	-4dB
1	0	1	-5dB
1	1	0	-6dB
1	1	1	-7dB

Auto Zeroed Instrumentation Amplifier

(Allow 500 μs for system to completely zero)

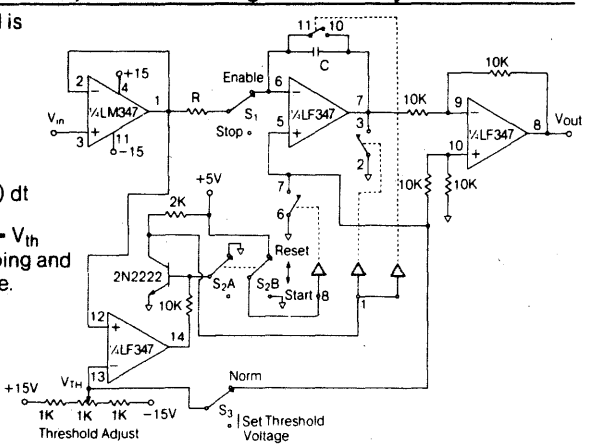


Long Time Integrator with Reset, Hold and Starting Threshold Adjustment

- ☐ V_{out} starts from zero and is equal to the integral of the input voltage with respect to the threshold voltage:

$$V_{out} = \frac{1}{RC}\int_0^t (V_{in} - V_{th})\,dt$$

- ☐ Output starts when $V_{in} = V_{th}$
- ☐ Switch S_1 permits stopping and holding any output value.
- ☐ Switch S_2 resets the system to zero.



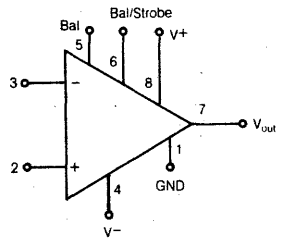
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BI-FET means more than Op Amps

In addition to op amps, here are other IC's built with this unique process:

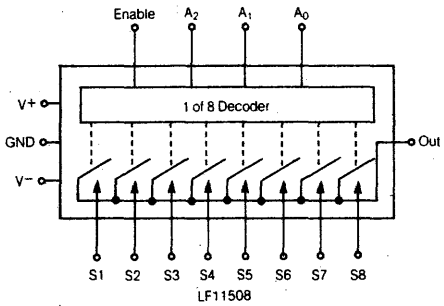
LF111 BI-FET input comparator

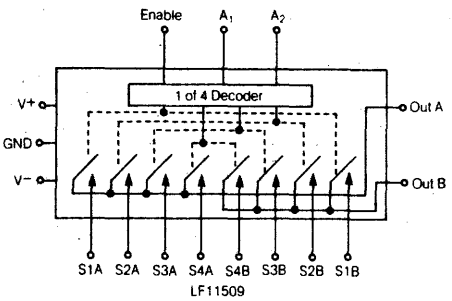
- ☐ Low bias current.
- ☐ High input impedance.



LF11508 and LF11509 8 Channel Single or Differential Multiplexers

- ☐ Low cost.
- ☐ Eliminate CMOS latch-up problem.

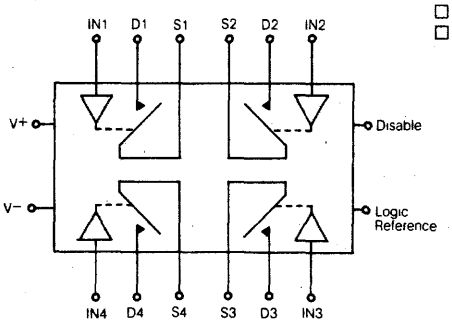




LF11331, LF11332, LF11333, LF11201, LF11202, QUAD SPST Analog Switches

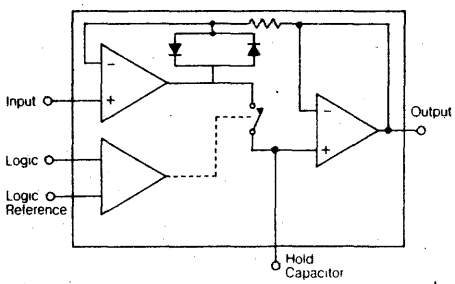
LF11331—4 normally open switches with disable.
LF11332—4 normally closed switches with disable.
LF11332—2 normally open and 2 normally closed switches with disable.
LF11201—4 normally closed switches.
LF11202—4 normally open switches.

- ☐ Low cost.
- ☐ Eliminate CMOS latch-up problems.



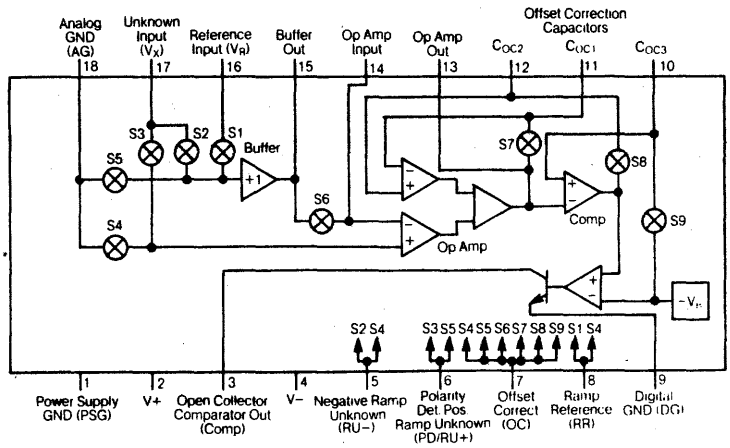
LF198 Sample and Hold Circuit

- ☐ First monolithic sample and hold.



LF13300 Dual Slope Integration A/D Analog Building Block

- ☐ Low cost 12-bit A/D and 4½ digit DVM.



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Product Selection Chart

Comparison of Electrical Characteristics

Part Number	DC Electrical Characteristics: V_{OS}—Max Offset Voltage (mV) (T_A = 25°C)	DC Electrical Characteristics: $\Delta V_{OS}/\Delta T$—T.C. OF V_{OS} ($\mu V/°C$) TYP	DC Electrical Characteristics: I_B—Max Bias Current (pA) (T_J = 25°C)	DC Electrical Characteristics: A_{VOL} Large Signal Voltage Gain (V/mV) Min (T_A = 25°C)	AC Electrical Characteristics: SR—Slew Rate (V/μs)	AC Electrical Characteristics: e_n—Equiv. Input Noise Voltage (nV/$\sqrt{Hz}$) (Note 2)
Military BI-FET OP AMP (Note 1)						
LF155	5	5	100	50	5	20
LF155A	2	5 (max)	50	50	5	20
LF156	5	5	100	50	12	12
LF156A	2	5 (max)	50	50	12	12
LF157	5	5	100	50	50	12
LF157A	2	5 (max)	50	50	50	12
LFT155	0.5	5 (max)	50	50	5	20
LFT156	0.5	5 (max)	50	50	12	12
Industrial BI-FET OP AMP (Note 1)						
LF255	5	5	100	50	5	20
LF256	5	5	100	50	12	12
LF257	5	5	100	50	50	12
Commercial BI-FET and BI-FET II OP AMP (Note 3)						
LF351	10	10	200	25	13	16
LF351A	2	10	100	25	13	16
LF351B	5	10	200	25	13	16
LF355	10	5	200	25	5	25
LF355A	2	5 (max)	50	25	5	25
LF355B	5	5	100	50	5	20
LF356	10	5	200	25	12	15
LF356A	2	5 (max)	50	25	12	15
LF356B	5	5	100	50	12	12
LF357	10	5	200	25	50	15
LF357A	2	5 (max)	50	25	50	15
LF357B	5	5	100	50	15	12
LFT355	0.5	5 (max)	50	50	5	20
LFT356	0.5	5 (max)	50	50	12	12
LF13741	15	10	200	25	0.5	37
BI-FET II Dual OP AMPS (Characteristics for Each Amplifier) (Note 3)						
LF353	10	10	200	25	13	16
LF353A	2	10	100	25	13	16
LF353B	5	10	200	25	13	16
BI-FET II Quad OP AMPS (Characteristics for Each Amplifier) (Note 3)						
LF347	10	10	200	25	13	16
LF347A	2	10	100	25	13	16
LF347B	5	10	200	25	13	16

BI-FET is a trademarked term by National Semiconductor who invented the technology in 1974.
Note 1: DC electrical characteristics are −55°C to +125°C for Military and −25° to +85°C for Industrial unless otherwise noted; AC electrical characteristics are T_A=25°C, typical specifications unless noted.
Note 2: f = 1000Hz
Note 3: DC electrical characteristics are 0°C to +70°C unless otherwise noted; AC electrical characteristics are T_A = 25°C, typical specifications unless noted.

Selection by Design Parameter

Max Input Offset Voltage (T_A = 25°C)	**0.5 mV** LFT155/LFT156 LFT355/LFT356	**2 mV** LF155A/LF355A LF156A/LF356A LF357A LF351A LF353A LF347A	**5 mV** LF351B LF347B LF353B LF155/LF156/LF157 LF255/LF256/LF257 LF355B/356B/357B	**10 mV** LF355/LF356/LF357 LF351 LF353 LF347	**15 mV** LF13741
Max Input Bias Current (T_J = 25°C)	**50 pA** LF155A/LF156A/LF157A LFT155/LFT156 LF355A/LF356A/LF357A	**100 pA** LF155/LF156/LF157 LF255/LF256/LF257 LF351A LF353A LF347A LF355B/356B/357B	**200 pA** LF355/LF356/LF357 LF351/LF351B LF347/LF347B LF353/LF353B LF13741		
Typ Equivalent Input Noise Voltage per $\sqrt{Hz}$, f = 1000 Hz, R_S = 100Ω	**12 nV or Less** LF156/LF156A LF157/LF157A LFT156/356 LF256/LF257 LF356B/357B	**15 nV to 20 nV** LF356 LF356A LF357 LF357A LF355B	LF351 LF351A LF351B LF347 LF347A LF347B	LF353 LF353A LF353B	**25 nV To 37 nV** LF155 LF155A LFT155 LF255	LF355 LF355A	LF13741
Typ Slew Rate	**0.5 V/μs** LF13741	**5 V/μs** LF155/LF155A LFT155 LF255 LF355/LF355A	LFT355 LF355B	**12 V/μs** LF156 LF156A LFT156 LF256 LF356	LF356A LFT356 LF256A LF356B	**13 V/μs** LF351 LF351A LF351B LF353 LF353A	LF353B LF347 LF347A LF347B	**50 V/μs** LF157 LF157A LF357 LF357A LF257	LF257A LF357B

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Ordering Information

National Semiconductor Part Number	Description	Package	Temperature Range
LF111H	BI-FET Comparator	TO-5	A
LF155AH	BI-FET Op Amp	TO-5	A
LF155H	BI-FET Op Amp	TO-5	A
LF156AH	BI-FET Op Amp, Low Power	TO-5	A
LF156H	BI-FET Op Amp	TO-5	A
LF157AH	BI-FET Op Amp, Low Power	TO-5	A
LF157H	BI-FET Op Amp	TO-5	A
LF198H	BI-FET Sample/Hold	TO-5	A
LF13741H	BI-FET 741 Op Amp	TO-5	C
LF13741N	BI-FET 741 Op p	8-pin DIP	C
LFT155H	BI-FET Op Amp, Low Power	TO-5	A
LFT156H	BI-FET Op Amp	TO-5	A
LF211H	BI-FET Comparator	TO-5	B
LF255H	BI-FET Op Emp	TO-5	B
LF256H	BI-FET Op Amp	TO-5	B
LF257H	BI-FET Op Amp	TO-5	B
LF298H	BI-FET Sample/Hold	TO-5	B
LFT355H	BI-FET Op Amp	TO-5	C
LFT356H	BI-FET Op Amp	TO-5	C
LF311H	BI-FET Comparator	TO-5	C
LF347N	BI-FET II Quad Op Amp	14-pin DIP	C
LF347AN	BI-FET II Quad Op Amp	14-pin DIP	C
LF347BN	BI-FET II Quad Op Amp	14-pin DIP	C
LF347J	BI-FET II Quad Op Amp	14-pin C-DIP	C
LF347AJ	BI-FET II Quad	14-pin C-DIP	C
LF347BJ	BI-FET II Quad Op Amp	14-pin C-DIP	C
LF351N	BI-FET II Op Amp	8-pin DIP	C
LF351AN	BI-FET II Op Amp	8-pin DIP	C
LF351BN	BI-FET II Op Amp	8-pin DIP	C
LF351H	BI-FET II Op Amp	TO-5	C
LF351AH	BI-FET II Op Amp	TO-5	C
LF351BH	BI-FET II Op Amp	TO-5	C
LF353N	BI-FET II Dual Op Amp	8-pin DIP	C
LF353AN	BI-FET II Dual Op Amp	8-pin DIP	C
LF353BN	BI-FET II Dual Op Amp	8-pin DIP	C
LF353H	BI-FET II Dual Op Amp	TO-5	C
LF353AH	BI-FET II Dual Op Amp	TO-5	C
LF353BH	BI-FET II Dual Op Amp	TO-5	C
LF354AN	BI-FET II Dual Op Amp	14-pin DIP	C
LF354BN	BI-FET II Dual Op Amp	14-pin DIP	C
LF354N	BI-FET II Dual Op Amp	14-pin DIP	C
LF355AH	BI-FET Op Amp	TO-5	C
LF355H	BI-FET Op Amp	TO-5	C
LF355N	BI-FET Op Amp	8-pin DIP	C
LF356AH	BI-FET Op Amp	TO-5	C
LF356H	BI-FET Op Amp	TO-5	C
LF356N	BI-FET Op Amp	8-pin DIP	C
LF357AH	BI-FET Op Amp	TO-5	C
LF357H	BI-FET Op Amp	TO-5	C
LF357N	BI-FET Op Amp	8-pin DIP	C
LF398H	BI-FET Sample/Hold	TO-5	C

Temperature Range:
A = −55 to +125°C
B = −25 to + 85°C
C = 0 to + 70°C

Additional National Semiconductor Products using BI-FET Technology

- ☐ LF111/LF311 Comparator
- ☐ LF11201/LF12201/LF13201 Quad Analog Switch Family
- ☐ LF11202/LF12202/LF13202 Quad Analog Switch Family
- ☐ LF11331/LF12331/LF13331 Quad Analog Switch Family
- ☐ LF11332/LF12332/LF13332 Quad Analog Switch Family
- ☐ LF11333/LF12333/LF13333 Quad Analog Switch Family
- ☐ LF11508/LF12508/LF13508 8 Channel Analog Multiplexer
  LF11509/LF12509/LF13509 9 Channel Differential Analog Multiplexer
- ☐ LF13300 Integrating A/D Building Block
- ☐ LF198/LF298/LF398 Sample and Hold Circuit

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National Semiconductor

LM13600/LM13600A/LM11600A Dual Operational Transconductance Amplifiers With Linearizing Diodes and Buffers

General Description

The LM13600 series consists of two current controlled transconductance amplifiers each with differential inputs and a push pull output. The two amplifiers share common supplies but otherwise operate independently. Linearizing diodes are provided at the inputs to reduce distortion and allow higher input levels. The results is a 10 dB signal-to-noise improvement referenced to 0.5 percent THD. Controlled impedance buffers are provided which are especially designed to complement the dynamic range of the amplifiers.

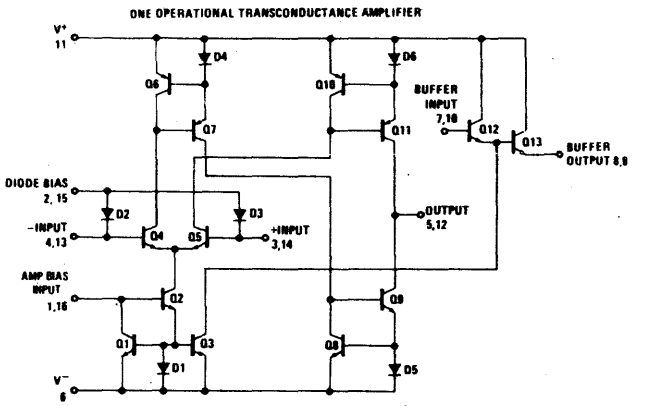
Features

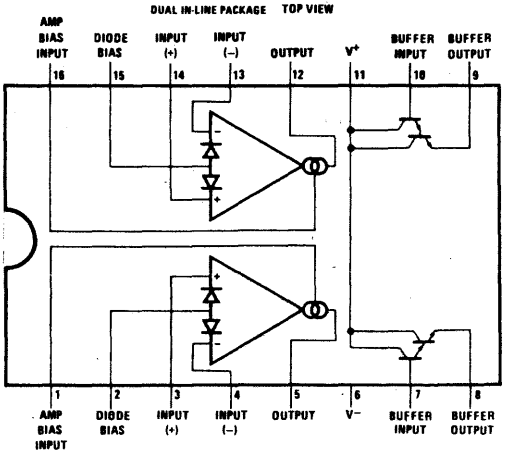
- gm adjustable over 6 decades
- Excellent gm linearity
- Excellent matching between amplifiers
- Linearizing diodes
- Controlled impedence buffers
- High output signal to noise ratio
- Wide supply range ± 2V to ± 22V.

Applications

- Current controlled amplifiers
- Current controlled impedances
- Current controlled filters
- Current controlled oscillators
- Multiplexers
- Timers
- Sample and hold circuits

Schematic and Connection Diagrams





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Absolute Maximum Ratings

Supply Voltage (Note 1)	
LM13600	36 V_{DC} or ± 18 V
LM13600A, LM11600A	44 V_{DC} or ± 22 V
Power Dissipation (Note 2) T_A = 25° C	
LM13600N, LM13600AN	570 mW
LM13600J, LM11600AJ	600mW
Differential Input Voltage	± 5 V
Diode Bias Current (I_D)	2 mA
Amplifier Bias Current (I_{ABC})	2 mA
Output Short Circuit Duration	Indefinite
Buffer Output Current (Note 3)	20 mA
Operating Temperature Range	
LM13600N, LM13600AN, LM13600J	0° C to + 70° C
LM11600AJ	-55° C to + 125° C
DC InputVoltage	+ V_S to -V_S
Storage Temperature Range	-65° C to + 150° C
Lead Temperature (Soldering, 10 Seconds)	300° C

Electrical Characteristics (Note 4)

Parameters	Conditions	LM13600 Min	LM13600 Typ	LM13600 Max	LM13600A Min	LM11600A Typ	LM11600A Max	Units
Input Offset Voltage (V_{OS})			0.4	5		0.4	2	mV
	Over Specified Temperature Range						5	mV
	I_{ABC} 5 μA		0.3	5		0.3	2	mV
V_{OS} Including Diodes	Diode Bias Current (I_D) = 500 μA		0.5	5		0.5	2	mV
Input Offset Change	5 μA ≤ I_{ABC} ≤ 500 μA		0.1			0.1	3	mV
Input Offset Current			0.1	0.6		0.1	0.6	μA
Input Bias Current			0.4	5		0.4	5	μA
	Over Specified Temperature Range		1	8		1	7	μA
Forward Transconductance(gm)		6700	9600	13000	7700	9600	12000	μmho
	Over specified Temp Range	5400			4000			μmho
gm Tracking			0.3			0.3		dB
Peak Output Current	RL = 0, I_{ABC} = 5 μA		5		3	5	7	μA
	RL = 0, I_{ABC} = 500 μA	350	500	650	350	500	650	μA
	RL = 0, Over Specified Temp Range	300			300			μA
Peak Output Voltage								
Positive	RL = ∞, 5 μA ≤ I_{ABC} ≤ 500 μA	+ 12	+ 14.2		+ 12	+ 14.2		V
Negative	RL = ∞, 5 μA ≤ I_{ABC} ≤ 500 μA	- 12	- 14.4		- 12	- 14.4		V
Supply Current	I_{ABC}=500μA,Both Channels		2.6			2.6		mA
V_{OS} Sensitivity								
Positive	Δ V_{OS}/Δ V +		20	150		20	150	μV/V
Negative	Δ V_{OS}/Δ V -		20	150		20	150	μV/V
CMRR		80	110		80	110		dB
Common Mode Range		± 12	± 13.5		± 12	± 13.5		V
Crosstalk	Referred to Input (Note 5) 20 Hz < f < 20 KHz		100			100		dB
Diff.Input Current	I_{ABC} = 0, Input = ± 4 V		0.02	100		0.02	10	nA
Leakage Current	I_{ABC} = 0 (Refer To Test Circuit)		0.2	100		0.2	5	nA
Input Resistance		10	26		10	26		KΩ
Open Loop Bandwith			2			2		MHz
Slew Rate	Unity Gain Compensated		50			50		V/μSec
Buff. Input Current	(Note 5)		0.4	5		0.4	5	μA
Peak Buffer Output Voltage	(Note 5)	10			10			V

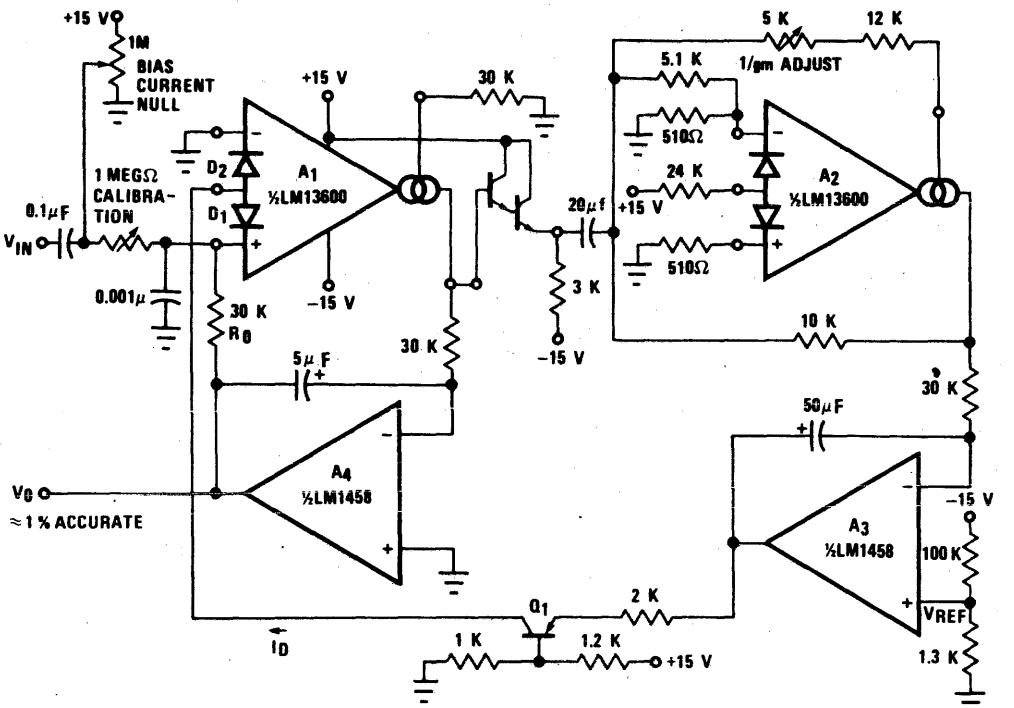
Note 1. For selections to a supply voltage above ± 22V, contact factory.

Note 2. For operating at high temperatures, the device must be derated based on a 150° C maximum junction temperature and a thermal resistance of 175° C/W which applies for the device soldered in a printed circuit board, operating in still air.

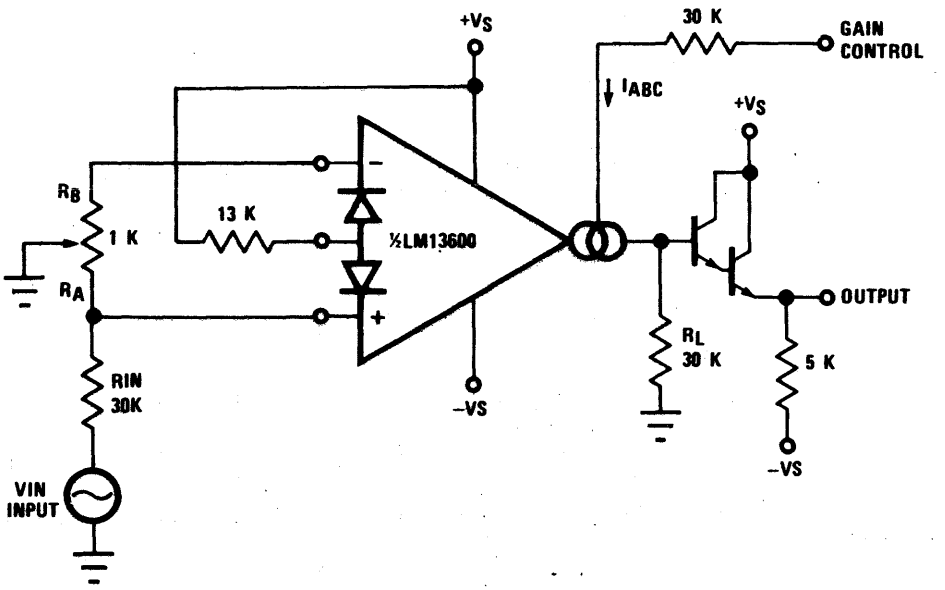
Note 3. Buffer output current should be limited so as to not exceed package dissipation.

Note 4. These specifications apply for V_S = ± 15 V, T_A = 25° C, amplifier bias current (I_{ABC}) = 500μA, pins 2 and 15 open unless otherwise specified. The inputs to the buffers are grounded and outputs are open.

Note 5. These specifications apply for V_S = ± 15V, I_{ABC} = 500 μA, R_{OUT} = 5 KΩ connected from the buffer output to - V_S and the input of the buffer is connected to the transconductance amplifier output.

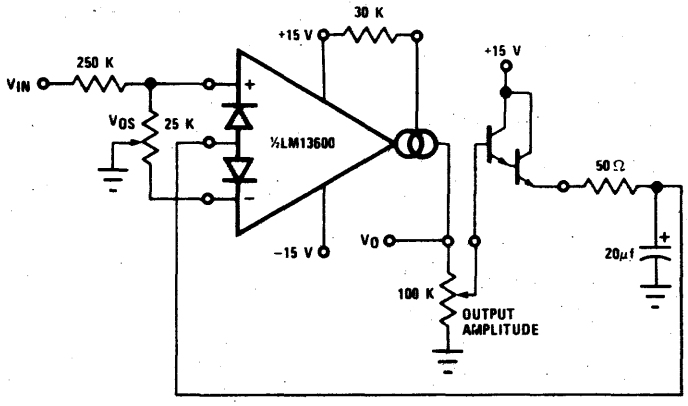


True RMS Converter

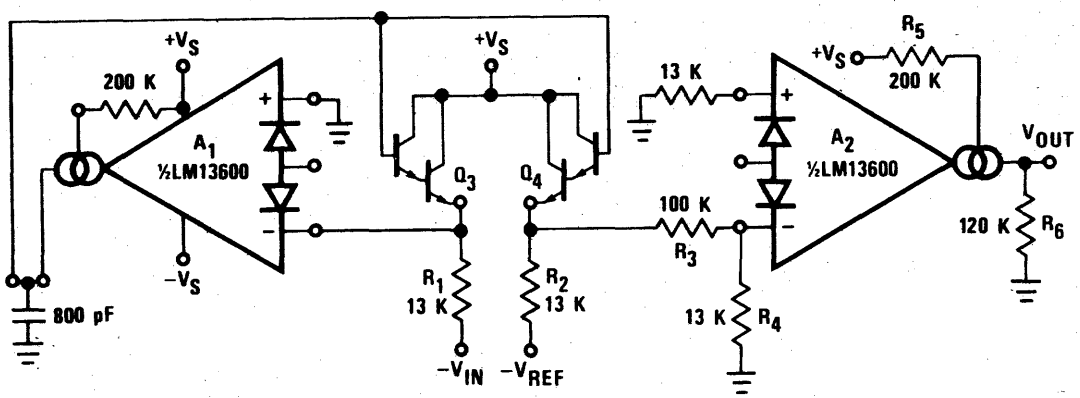


Voltage Controlled Amplifier

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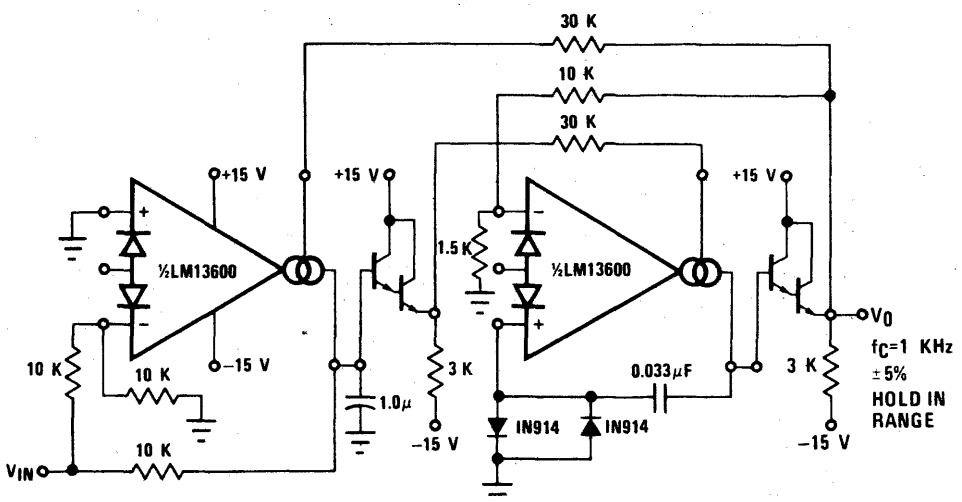


AGC Amplifier



$$V_{OUT} = \frac{(2\ V_S - 1.2\ V)\ (R_4)\ (R_6)}{(R_3 + R_4)\ (R_5)} \cdot \ln \frac{V_{IN}\ R_2}{V_{REF}\ R_1}$$

Log Amplifier



Phase Lock Loop

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JULY 1978

LM192/LM292/LM392, LM2924 Low Power Operational Amplifier/Voltage Comparator

General Description

The LM192 series consists of 2 independent building block circuits. One is a high gain, internally frequency compensated operational amplifier, and the other is a precision voltage comparator. Both the operational amplifier and the voltage comparator have been specifically designed to operate from a single power supply over a wide range of voltages. Both circuits have input stages which will common-mode input down to ground when operating from a single power supply. Operation from split power supplies is also possible and the low power supply current is independent of the magnitude of the supply voltage.

Application areas include transducer amplifier with pulse shaper, DC gain block with level detector, VCO, as well as all conventional operational amplifier or voltage comparator circuits. Both circuits can be operated directly from the standard 5 V_{DC} power supply voltage used in digital systems, and the output of the comparator will interface directly with either TTL or CMOS logic. In addition, the low power drain makes the LM192 extremely useful in the design of portable equipment.

Advantages

- Eliminates need for dual power supplies
- An internally compensated op amp and a precision comparator in the same package
- Allows sensing at or near ground
- Power drain suitable for battery operation
- Pin-out is the same as both the LM158 dual op amp and the LM193 dual comparator

Features

- Wide power supply voltage range
  - Single supply 3V to 32V
  - Dual supply ±1.5V to ±16V
- Low supply current drain—essentially independent of supply voltage 600 μA
- Low input biasing current 50 nA
- Low input offset voltage 2 mV
- Low input offset current 5 nA
- Input common-mode voltage range includes ground
- Differential input voltage range equal to the power supply voltage

ADDITIONAL OP AMP FEATURES

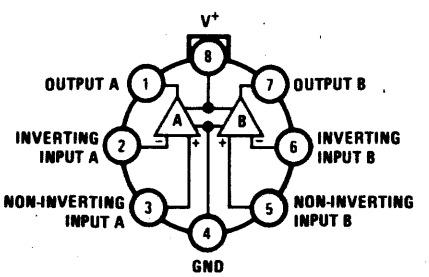
- Internally frequency compensated for unity gain
- Large DC voltage gain 100 dB
- Wide bandwidth (unity gain) 1 MHz
- Large output voltage swing 0V to $V^+ - 1.5V$

ADDITIONAL COMPARATOR FEATURES

- Low output saturation voltage 250 mV at 6 mA
- Output voltage compatible with all types of logic systems

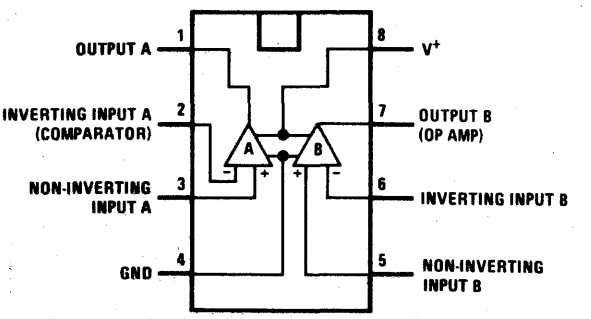
Connection Diagrams

Metal Can Package



TOP VIEW

Dual-In-Line Package



TOP VIEW

(Amplifier A = Comparator)
(Amplifier B = Operational Amplifier)

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IM-B25M78/Printed in U.S.A.

Absolute Maximum Ratings

	LM192/LM292/LM392	LM2924
Supply Voltage, V^+	32V or ±16V	26V or ±13V
Differential Input Voltage	32V	26V
Input Voltage	−0.3V to +32V	−0.3V to +26V
Power Dissipation (Note 1)		
Molded DIP (LM392N, LM2924N)	570 mW	570 mW
Metal Can (LM192H/LM292H/LM392H)	830 mW	
Output Short-Circuit to Ground (Note 2)	Continuous	Continuous
Input Current ($V_{IN} < -0.3\ V_{DC}$) (Note 3)	50 mA	50 mA
Operating Temperature Range		
LM392	0°C to +70°C	−40°C to +85°C
LM292	−25°C to +85°C	
LM192	−55°C to +125°C	
Storage Temperature Range	−65°C to +150°C	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C	300°C

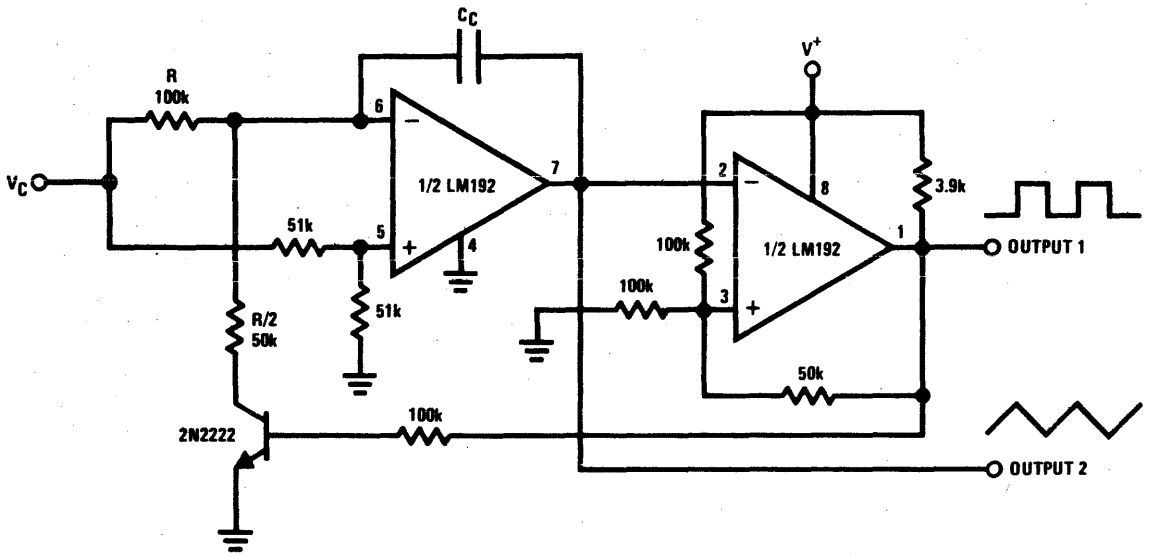
Electrical Characteristics ($V^+ = 5\ V_{DC}$; specifications apply to both amplifiers unless otherwise stated) (Note 4)

PARAMETER	CONDITIONS	LM192			LM292/LM392			LM2924			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	$T_A = 25°C$, (Note 5)		±2	±5		±2	±5		±2	±7	mV
Input Bias Current	IN(+) or IN(−), $T_A = 25°C$, (Note 6)		50	150		50	250		50	250	nA
Input Offset Current	IN(+) − IN(−), $T_A = 25°C$		±3	±25		±5	±50		±5	±50	nA
Input Common-Mode Voltage Range	$V^+ = 30\ V_{DC}$, $T_A = 25°C$, (Note 7)	0		$V^+-1.5$	0		$V^+-1.5$	0		$V^+-1.5$	V
Supply Current	$R_L = \infty$, $V_{CC} = 30V$, (LM2924, $V_{CC} = 26V$)		1	2		1	2		1	2	mA
Supply Current	$R_L = \infty$, $V_{CC} = 5V$		0.5	1		0.5	1		0.5	1	mA
Amplifier-to-Amplifier Coupling	f = 1 kHz to 20 kHz, $T_A = 25°C$, Input Referred, (Note 8)		−100			−100			−100		dB
Input Offset Voltage	(Note 5)			±7			±7			±10	mV
Input Bias Current	IN(+) or IN(−)			300			400			500	nA
Input Offset Current	IN(+) − IN(−)			100			150			200	nA
Input Common-Mode Voltage Range	$V^+ = 30\ V_{DC}$, (Note 7)	0		V^+-2	0		V^+-2	0		V^+-2	V
Differential Input Voltage	Keep All V_{IN}'s $\geq 0\ V_{DC}$ (or V^-, if Used), (Note 9)			V^+			V^+			V^+	V
OP AMP ONLY											
Large Signal Voltage Gain	$V^+ = 15\ V_{DC}$ (For Large V_o Swing), $R_L = 2\ k\Omega$, $T_A = 25°C$	50	100		25	100			100		V/mV
Output Voltage Swing	$R_L = 2\ k\Omega$, $T_A = 25°C$, (LM2924, $R_L \geq 10\ k\Omega$)	0		$V^+-1.5$	0		$V^+-1.5$	0		$V^+-1.5$	V
Common-Mode Rejection Ratio	DC, $T_A = 25°C$	70	85		65	70		50	70		dB
Power Supply Rejection Ratio	DC, $T_A = 25°C$	65	100		65	100		50	100		dB
Output Current Source	$V_{IN(+)} = 1\ V_{DC}$, $V_{IN(-)} = 0\ V_{DC}$, $V^+ = 15\ V_{DC}$, $T_A = 25°C$	20	40		20	40		20	40		mA
Output Current Sink	$V_{IN(-)} = 1\ V_{DC}$, $V_{IN(+)} = 0\ V_{DC}$, $V^+ = 15\ V_{DC}$; $V_o \geq 1\ V_{DC}$, $T_A = 25°C$	10	20		10	20		10	20		mA
	$V_{IN(-)} = 1\ V_{DC}$, $V_{IN(+)} = 0\ V_{DC}$, $V^+ = 15\ V_{DC}$, $V_o = 200\ mV$, $T_A = 25°C$	12	50		12	50		12	50		μA

Typical Applications

For many application ideas, please refer to the LM124, LM139, LM158 and LM193 data sheets.

Voltage Controlled Oscillator Circuit



Transducer Amplifier With Driver

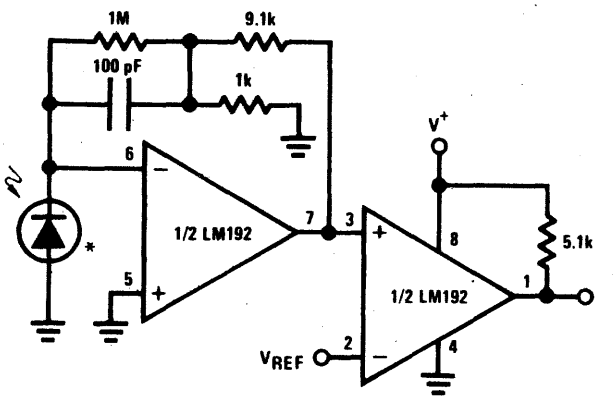


*Photo diode may be replaced with any type of transducer which converts some physical property to electrical energy.

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JUNE 1978

LM13080 Programmable Power Op Amp

General Description

The LM13080 is an internally compensated medium power operational amplifier designed for use in those applications requiring load currents of several hundred milliamperes. This amplifier has the added advantage of having an input stage programmed with an external resistor. The user is able to optimize the amplifier performance for each individual application with this feature. Applications include servo amplifiers and drivers, high input impedance audio amplifiers, DC-to-DC converters, precision power comparators which can either sink or source current and motor speed controls.

The LM13080 may be powered from either single or dual power supplies, and will operate from as little as 3V.

As a power operational amplifier, the LM13080 is capable of delivering 0.25A to a load. This feature allows the system designer to fulfill his medium power circuit requirements without having to add external current boost transistors to the output of a standard operational amplifier.

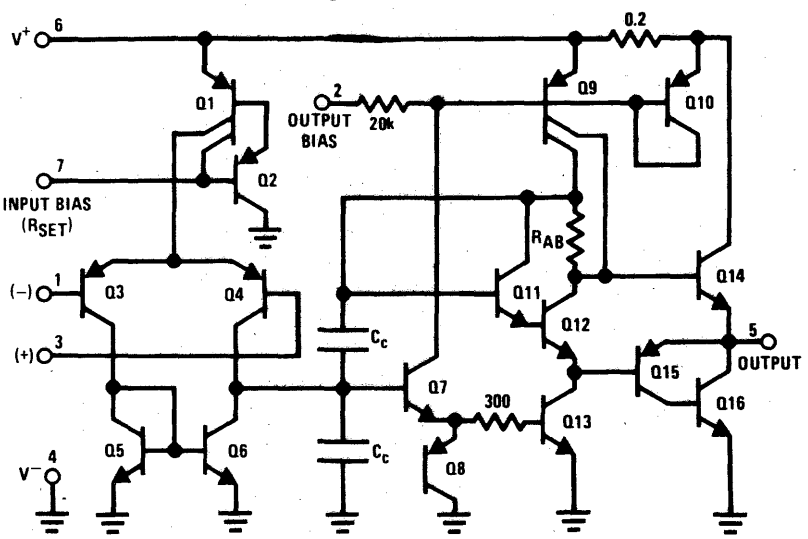
By selecting the proper input stage bias resistor it is possible to tailor the performance of the input stage to meet the needs of any particular system. Trade-offs between input offset voltage, input bias current and gain bandwidth are easily made.

An unusual feature of the LM13080 is an electronic shut-down capability.

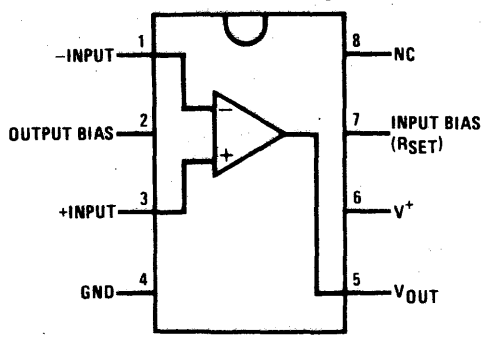
Features

- High output current—250 mA
- Externally programmable input stage
- Low power supply operation—3V
- Electronic shut-down capability
- Internally compensated for unity gain
- Low input bias current

Schematic and Connection Diagrams



Dual-In-Line Package



TOP VIEW

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Absolute Maximum Ratings

Supply Voltage Operation Range	3V to 15V or ±1.5V to ±7.5V	Input Voltage Range, (Note 3)	−0.3V to +15V
Power Dissipation, (Note 1)		Input Current ($V_{IN} \leq -0.3V$), (Note 4)	20 mA
Molded Dual-In-Line Package (LM13080N)	1000 mW	Operating Temperature Range	0°C to +70°C
Differential Input Voltage, (Note 2)	15V	Storage Temperature Range	−65°C to +150°C
		Lead Temperature (Soldering, 10 seconds)	300°C

Electrical Characteristics (V_S = 12V, R_{SET} = 680k, unless otherwise specified)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage	T_A = 25°C, (Note 5)		±3	±7	mV
Input Bias Current	$I_{IN(+)}$ or $I_{IN(-)}$, T_A = 25°C		100	400	nA
Input Offset Current	$I_{IN(+)} - I_{IN(-)}$, T_A = 25°C		±30	±75	nA
Supply Current	$R_L = \infty$, T_A = 25°C, (Note 6)		3	6	mA
Output Voltage Swing	V_S = ±6V, T_A = 25°C, (Note 1)				
V_{OH}	R_L = 50Ω	4.5	5		V
	R_L = 8Ω	2			V
V_{OL}	R_L = 50Ω		−5	−4.5	V
	R_L = 8Ω			−2	V
Large Signal Voltage Gain	V_S = ±6V, R_L = 50Ω, f = 100 Hz, T_A = 25°C	3	10		V/mV
Input Common-Mode Voltage Range	$V_S \leq$ 15V, T_A = 25°C, (Note 3)	1		V_S−1.5	V
Input Offset Voltage	(Note 5)			±10	mV
Input Offset Voltage Drift			5		μV/°C
Input Bias Current	$I_{IN(+)}$ or $I_{IN(-)}$			600	nA
Input Offset Current	$I_{IN(+)} - I_{IN(-)}$			±150	nA
Input Offset Current Drift			50		pA/°C
Supply Current	$R_L = \infty$, (Note 6)			8	mA
Output Voltage Swing	V_S = ±6V, (Note 1)				
V_{OH}	R_L = 50Ω			4	V
	R_L = 8Ω			1.6	V
V_{OL}	R_L = 50Ω	−4			V
	R_L = 8Ω	−1.6			V
Large Signal Voltage Gain	V_S = ±6V, R_L = 50Ω, f = 100 Hz	1			V/mV
Input Common-Mode Voltage Range	$V_S \leq$ 15V, (Note 3)	1.25		V_S−1.75	V
Common-Mode Rejection Ratio		63	85		dB
Total Harmonic Distortion	R_L = 8Ω, V_O = 2 Vrms, f = 1 kHz		0.5	5	%

Note 1: For operation at high temperatures the LM13080 must be derated based on a maximum junction temperature of 150°C and a thermal resistance of 120°C/W. The thermal resistance value is for a package soldered into a printed circuit board and operating in a still air ambient.

Note 2: Differential input voltages up to the magnitude of the power supply voltage will not damage the input circuitry. However, input voltages outside the input common-mode voltage range will not be able to properly control the output of the amplifier.

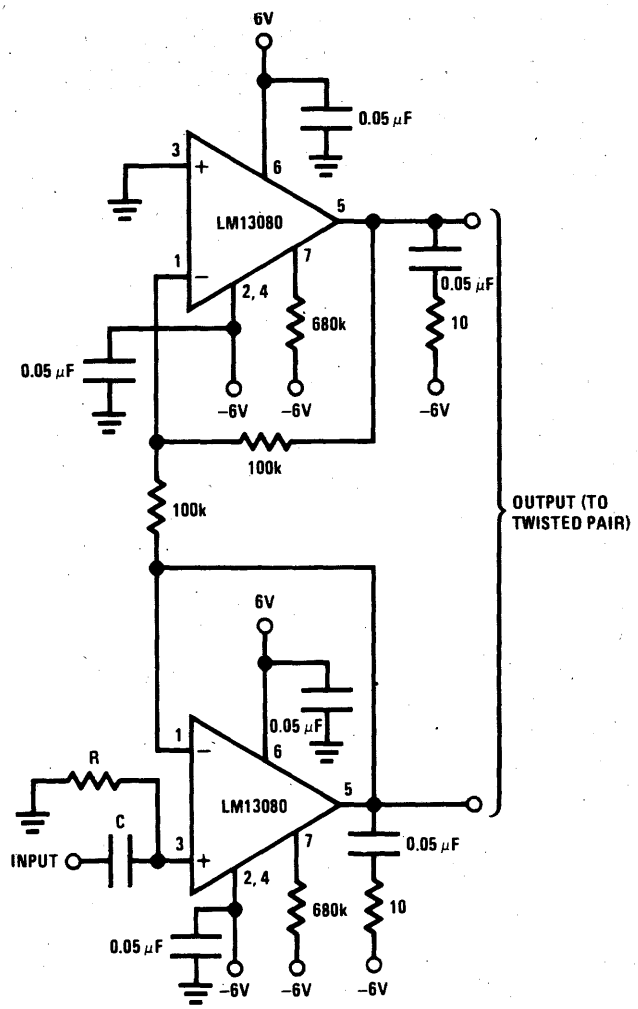
Note 3: The input voltage applied to either input should not be allowed to go more than 0.3V below the potential applied to pin 4; however, either input can be taken as high as 15V without causing damage to the circuit. Input voltages below the minimum common-mode voltage range may cause a phase reversal in the output.

Note 4: This input current will exist only when the voltage at either input lead is driven negative. It is due to the base-isolation junction of the PNP transistor tub becoming forward biased and thereby acting as an input diode clamp. In addition to this diode action, there is also lateral NPN parasitic action on the IC chip. This transistor action can cause the output to take an undefined state for the time duration that an input is driven negative.

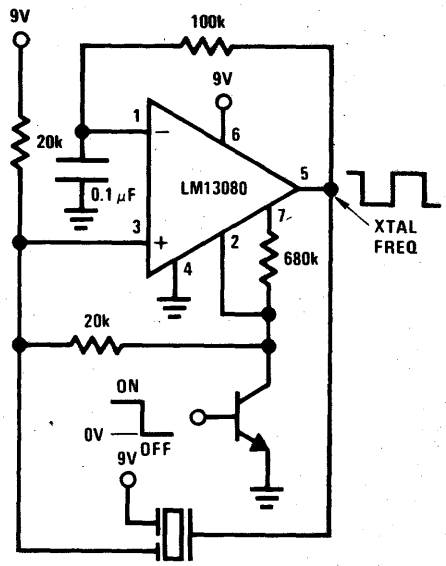
Note 5: V_O = 6V, R_S = 0Ω, and over the full input common-mode voltage range.

Note 6: Supply current is measured with the amplifier connected in a unity gain follower configuration and the positive input set to one-half of the supply voltage.

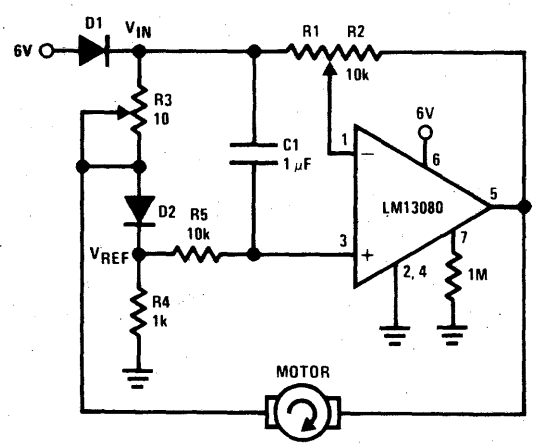
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Line Driver — Unbalanced Input to Balanced Output

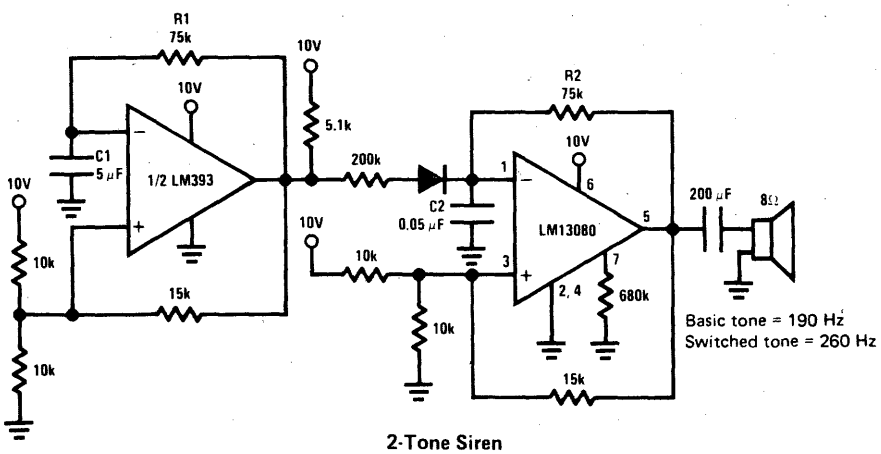


Piezoelectric Alarm



Motor Speed Control

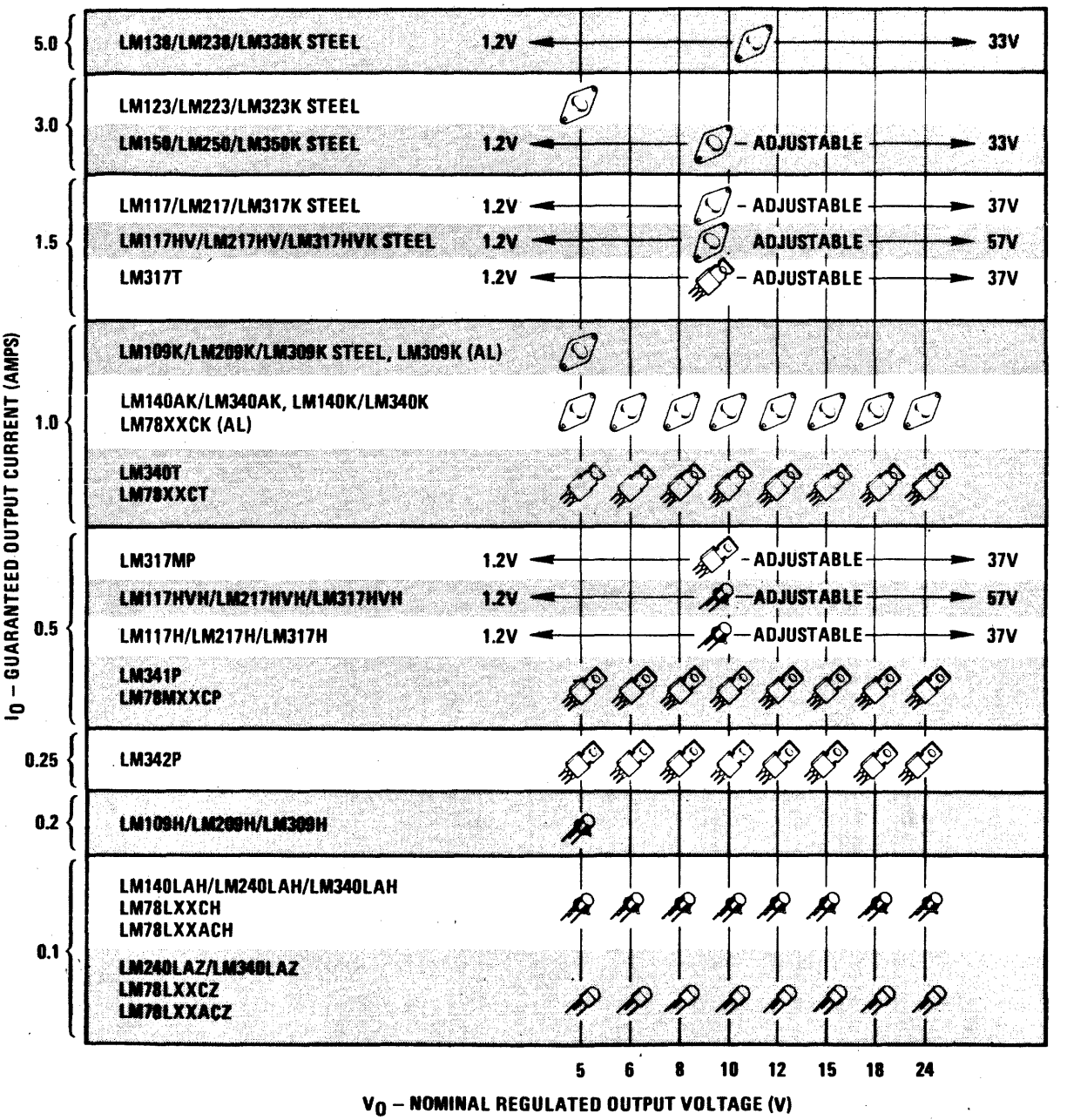
$$f_{SWITCH} = \frac{1}{1.4\ R1C1} = 1.9\ Hz$$



Basic tone = 190 Hz
Switched tone = 260 Hz

2-Tone Siren

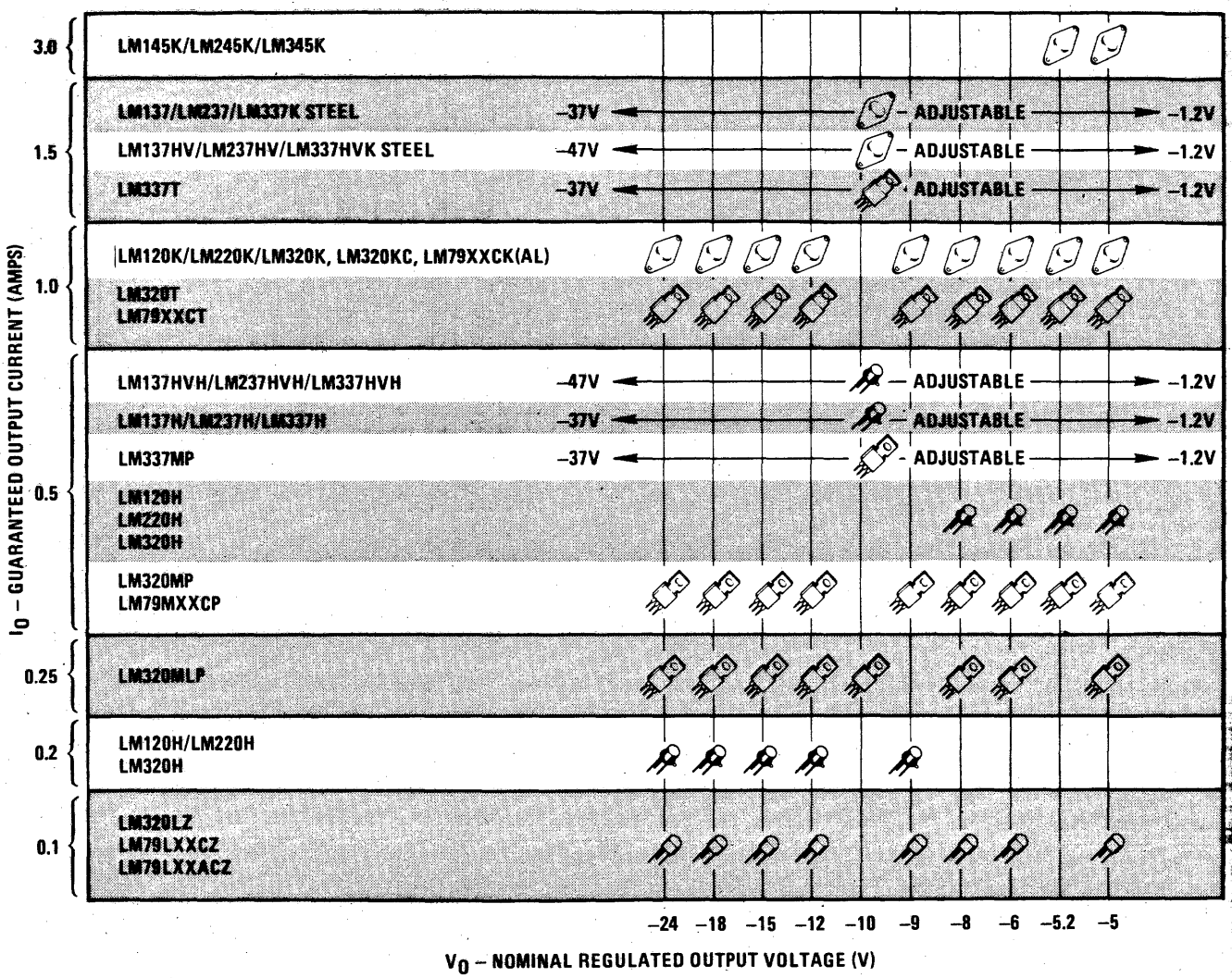
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	PACKAGE DESIGNATOR	PACKAGE TYPE
	K KC K STEEL	TO-3* HERMETIC
	T	TO-220 PLASTIC
	P	TO-202 PLASTIC
	H	TO-5, TO-39 HERMETIC
	Z	TO-99 PLASTIC

*All devices with TO-3 package designators (K or K STEEL) are supplied in steel TO-3 packages unless otherwise designated as (AL) aluminum TO-3 package. All KC designated devices are supplied in aluminum TO-3.

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REVERSE BREAKDOWN VOLTAGE V_R at I_R	DEVICE	VOLTAGE TOLERANCE MAX, T_A = 25°C	VOLTAGE TEMPERATURE DRIFT – ppm/°C MAX or mV MAX CHANGE OVER TEMPERATURE RANGE		CURRENT RANGE, I_R	DYNAMIC IMPEDANCE
			DRIFT (MAX)	TEMPERATURE RANGE		
1.22	LM113	±5%	100 (typ)	−55°C to +125°C	500 μA to 20 mA	0.3Ω
1.22	LM313	±5%	100 (typ)	0°C to +70°C	500 μA to 20 mA	0.3Ω
1.22	LM113-1	±1%	50 (typ)	−55°C to +125°C	500 μA to 20 mA	0.3Ω
1.22	LM113-2	±2%	50 (typ)	−55°C to +125°C	500 μA to 20 mA	0.3Ω
2.49	LM136	±2%	18 mV	−55°C to +125°C	400 μA to 10 mA	0.2Ω
2.49	LM136A	±1%	18 mV	−55°C to +125°C	400 μA to 10 mA	0.2Ω
2.49	LM236	±2%	9 mV	−25°C to +85°C	400 μA to 10 mA	0.2Ω
2.49	LM236A	±1%	9 mV	−25°C to +85°C	400 μA to 10 mA	0.2Ω
2.49	LM336	±4%	6 mV	0°C to +70°C	400 μA to 10 mA	0.2Ω
2.49	LM336B	±2%	6 mV	0°C to +70°C	400 μA to 10 mA	0.2Ω
5.0	LM136-5.0	±2%	36 mV	−55°C to +125°C	400 μA to 10 mA	0.2Ω
5.0	LM136A-5.0	±1%	36 mV	−55°C to +125°C	400 μA to 10 mA	0.2Ω
5.0	LM236-5.0	±2%	18 mV	−25°C to +85°C	400 μA to 10 mA	0.2Ω
5.0	LM236A-5.0	±1%	18 mV	−25°C to +85°C	400 μA to 10 mA	0.2Ω
5.0	LM336-5.0	±4%	12 mV	0°C to +70°C	400 μA to 10 mA	0.2Ω
5.0	LM336B-5.0	±2%	12 mV	0°C to +70°C	400 μA to 10 mA	0.2Ω
6.90	LM129A	+3%, −2%	10	−55°C to +125°C	0.6 mA to 15 mA	0.6Ω
6.90	LM129B	+3%, −2%	20	−55°C to +125°C	0.6 mA to 15 mA	0.6Ω
6.90	LM129C	+3%, −2%	50	−55°C to +125°C	0.6 mA to 15 mA	0.6Ω
6.90	LM329B	±5%	20	0°C to +70°C	0.6 mA to 15 mA	0.8Ω
6.90	LM329C	±5%	50	0°C to +70°C	0.6 mA to 15 mA	0.8Ω
6.90	LM329D	±5%	100	0°C to +70°C	0.6 mA to 15 mA	0.8Ω
6.95	LM199A	+1%, −2%	0.5	−55°C to +85°C	0.5 mA to 10 mA	0.5Ω
6.95	LM199A	+1%, −2%	10	85°C to +125°C	0.5 mA to 10 mA	0.5Ω
6.95	LM199	+1%, −2%	1	−55°C to +85°C	0.5 mA to 10 mA	0.5Ω
6.95	LM199	+1%, −2%	15	85°C to +125°C	0.5 mA to 10 mA	0.5Ω
6.95	LM299A	±1%, −2%	0.5	−25°C to +85°C	0.5 mA to 10 mA	0.5Ω
6.95	LM299	+1%, −2%	1	−25°C to +85°C	0.5 mA to 10 mA	0.5Ω
6.95	LM399A	±5%	1	0°C to +70°C	0.5 mA to 10 mA	0.5Ω
6.95	LM399	±5%	2	0°C to +70°C	0.5 mA to 10 mA	0.5Ω
6.95	LM3999	±5%	5	0°C to +70°C	0.6 mA to 10 mA	0.6Ω
10.00	LH0070-0	0.1%	20 mV	−25°C to +85°C	0 mA to 20 mA	0.2Ω
10.00	LH0070-1	0.1%	10 mV	−25°C to +85°C	0 mA to 20 mA	0.2Ω
10.00	LH0070-2	0.05%	4 mV	−25°C to +85°C	0 mA to 20 mA	0.2Ω
10.24	LH0071-0	0.1%	20 mV	−25°C to +85°C	0 mA to 20 mA	0.2Ω
10.24	LH0071-1	0.1%	10 mV	−25°C to +85°C	0 mA to 20 mA	0.2Ω
10.24	LH0071-2	0.05%	4 mV	−25°C to +85°C	0 mA to 20 mA	0.2Ω

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National Semiconductor

Voltage Regulators

LM1524/LM2524/LM3524
Regulating Pulse Width Modulator

General Description

The LM1524 series of regulating pulse width modulators contains all of the control circuitry necessary to implement switching regulators of either polarity, transformer coupled DC to DC converters, transformerless polarity converters and voltage doublers, as well as other power control applications. This device includes a 5V voltage regulator capable of supplying up to 50 mA to external circuitry, a control amplifier, an oscillator, a pulse width modulator, a phase splitting flip-flop, dual alternating output switch transistors, and current limiting and shutdown circuitry. Both the regulator output transistor and each output switch are internally current limited and, to limit junction temperature, an internal thermal shutdown circuit is employed. The LM1524 series will be available in the 16-pin dual-in-line J package with either a military, industrial or commercial temperature range.

Features

- Complete PWM power control circuitry
- Frequency adjustable to greater than 100 kHz
- 2% frequency stability with temperature
- Total quiescent current less than 10 mA
- Dual alternating output switches for both push-pull or single-ended applications
- Current limit amplifier provides external component protection
- On-chip protection against excessive junction temperature and output current—thermal limit
- 5V, 50 mA linear regulator output available to user

Typical Applications

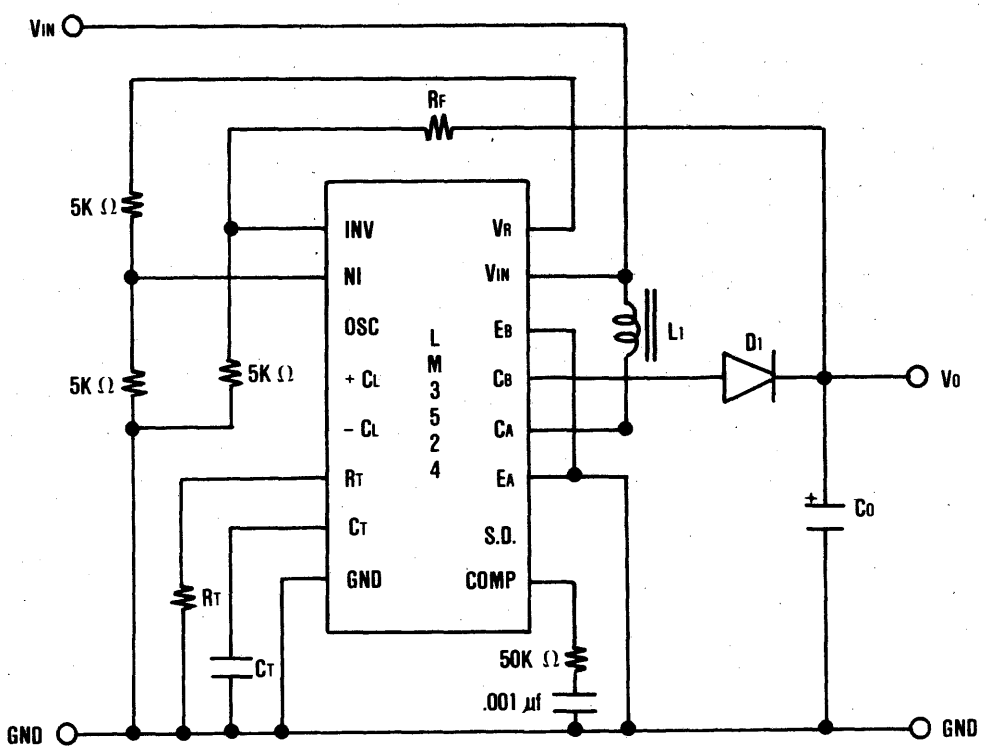


FIGURE 7: Positive Regulator, Set-Up Basic Configuration ($I_{IN\ MAX}$ = 80mA)

DESIGN EQUATIONS

$$R_F = 5K\left(\frac{V_O}{2.8} - 1\right)$$

$$f_{OSC} \simeq \frac{1}{(.5)\,R_T C_T}$$

$$L_1 = \frac{2.5 V_{IN}^2 (V_O - V_{IN})}{f\, I_O\, V_O^2}$$

$$C_O = \frac{I_O (V_O - V_{IN})}{f\ \Delta V_O\, V_O}$$

$$I_{O_{MAX}} = I_{IN}\frac{V_{IN}}{V_O}$$

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LM137/LM237/LM337 3-Terminal Adjustable Negative Regulators

General Description

The LM137/LM237/LM337 are adjustable 3-terminal negative voltage regulators capable of supplying in excess of −1.5A over an output voltage range of −1.2V to −37V. These regulators are exceptionally easy to apply, requiring only 2 external resistors to set the output voltage and 1 output capacitor for frequency compensation. The circuit design has been optimized for excellent regulation and low thermal transients. Further, the LM137 series features internal current limiting, thermal shutdown and safe-area compensation, making them virtually blowout-proof against overloads.

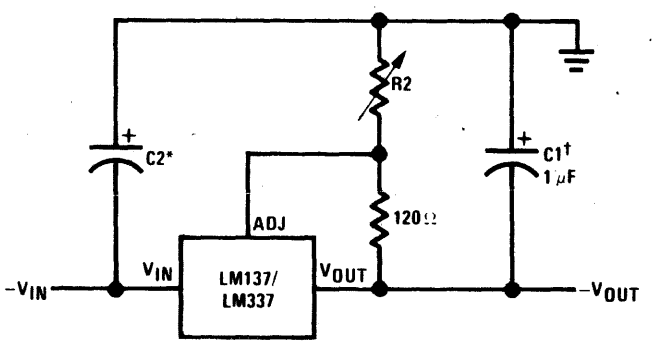
The LM137/LM237/LM337 serve a wide variety of applications including local on-card regulation, programmable-output voltage regulation or precision current regulation. The LM137/LM237/LM337 are ideal complements to the LM117/LM217/LM317 adjustable positive regulators.

Features

- Output voltage adjustable from −1.2V to −37V
- 1.5A output current guaranteed, −55°C to +150°C
- Line regulation typically 0.01%/V
- Load regulation typically 0.3%
- Excellent thermal regulation, 0.002%/W
- 77 dB ripple rejection
- Excellent rejection of thermal transients
- 50 ppm/°C temperature coefficient
- Temperature-independent current limit
- Internal thermal overload protection
- 100% electrical burn-in
- Standard 3-lead transistor package

Typical Applications

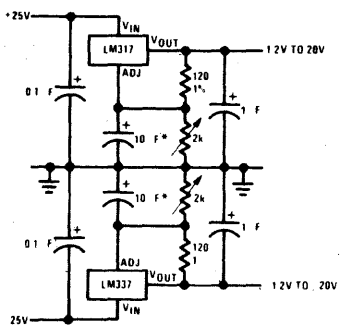
Adjustable Negative Voltage Regulator



$$-V_{OUT} = -1.25V\left(1 + \frac{R2}{120\Omega}\right)$$

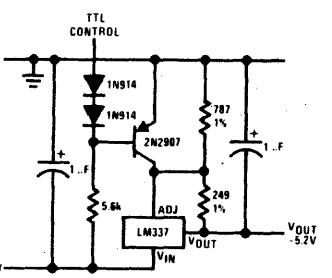
†C1 = 1 μF solid tantalum or 10 μF aluminum electrolytic required for stability
*C2 = 1 μF solid tantalum is required only if regulator is more than 4" from power-supply filter capacitor

Adjustable Lab Voltage Regulator



*The 10 μF capacitors are optional to improve ripple rejection

−5.2V Regulator with Electronic Shutdown*



*Minimum output ≈ −1.3V when control input is low

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National Semiconductor

OCTOBER 1977

LM150/LM250/LM350
3 Amp Adjustable Power Regulators

General Description

The LM150/LM250/LM350 are adjustable 3-terminal positive voltage regulators capable of supplying in excess of 3A over a 1.2V to 33V output range. They are exceptionally easy to use and require only 2 external resistors to set the output voltage. Further, both line and load regulation are comparable to discrete designs. Also, the LM150 is packaged in standard transistor packages which are easily mounted and handled.

In addition to higher performance than fixed regulators, the LM150 series offers full overload protection available only in IC's. Included on the chip are current limit, thermal overload protection and safe area protection. All overload protection circuitry remains fully functional even if the adjustment terminal is accidentally disconnected.

Normally, no capacitors are needed unless the device is situated far from the input filter capacitors in which case an input bypass is needed. An optional output capacitor can be added to improve transient response. The adjustment terminal can be bypassed to achieve very high ripple rejections ratios which are difficult to achieve with standard 3-terminal regulators.

Besides replacing fixed regulators or discrete designs, the LM150 is useful in a wide variety of other applications. Since the regulator is "floating" and sees only the input-to-output differential voltage, supplies of several hundred volts can be regulated as long as the maximum input to output differential is not exceeded.

Also, it makes an especially simple adjustable switching regulator, a programmable output regulator, or by connecting a fixed resistor between the adjustment and output, the LM150 can be used as a precision current regulator. Supplies with electronic shutdown can be achieved by clamping the adjustment terminal to ground which programs the output to 1.2V where most loads draw little current.

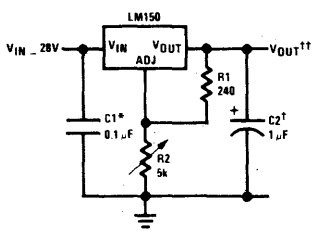
The LM150/LM250/LM350 are packaged in standard steel TO-3 transistor packages. The LM150 is rated for operation from −55°C to +150°C, the LM250 from −25°C to +150°C and the LM350 from 0°C to +125°C.

Features

- Adjustable output down to 1.2V
- Guaranteed 3A output current
- Line regulation typically 0.005%/V
- Load regulation typically 0.1%
- Guaranteed thermal regulation
- Current limit constant with temperature
- **100% electrical burn-in in thermal limit**
- Eliminates the need to stock many voltages
- Standard 3-lead transistor package
- 86 dB ripple rejection

Typical Applications

1.2V–25V Adjustable Regulator

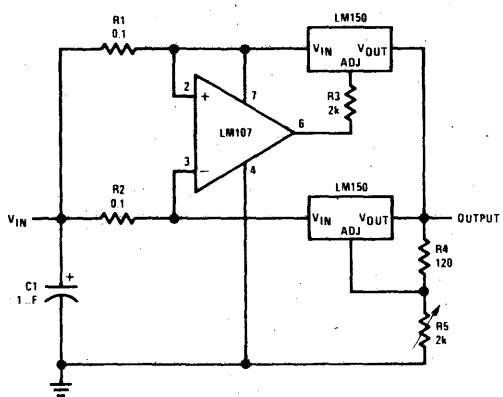


†Optional—improves transient response

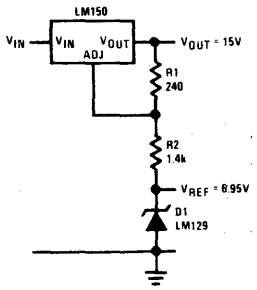
*Needed if device is far from filter capacitors

††$V_{OUT} = 1.25V \left(1 + \frac{R2}{R1}\right)$

6A Regulator



Regulator and Voltage Reference



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IM-B20M107/Printed in U.S.A.

The "NAKED-8"™

ADC 0801 8 Bit, μP Interfaced, Differential Input A/D

General Description

The ADC 0801 is a μP compatible, advanced CMOS/SiCr 8 Bit successive approximation A/D converter which uses a modified potentiometric ladder-similar to the 256 R products. It is designed to meet the NSC microbus™ standard to allow operation with the 8080 control bus. The "TRI-STATE"® output latches directly drive the data bus. This A/D appears like a memory location or an I/O port to the μP and no interfacing logic is needed.

A new differential analog voltage input allows many novel applications such as increasing the common-mode rejection and offsetting the analog "ZERO" input voltage value. In addition, the voltage reference input can be adjusted to allow encoding any smaller analog voltage span to the full 8 bits of resolution.

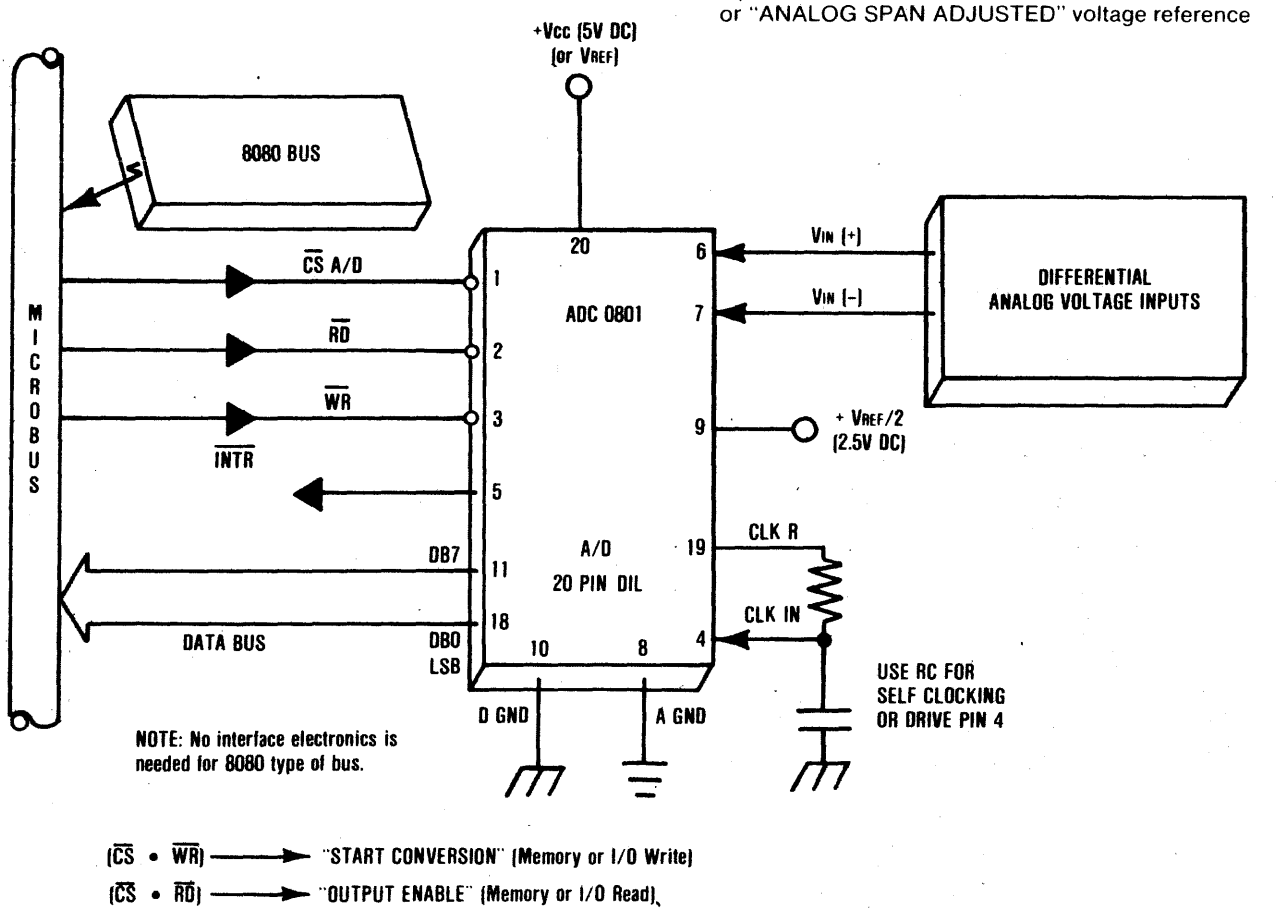
Features

- Microbus™ (8080) compatible—no interfacing logic needed
- Easy interface to all μP's
- New analog differential voltage inputs—has both VIN (+) & VIN (-) pins
- MOS logic inputs which meet T²L voltage level specifications
- Works with 5V or 2.5V (LM336) voltage reference
- On-chip clock generator. (with external R, C)
- 0 to 5V analog input voltage range with single 5V supply
- 0.3" std. width 20 pin DIL pkg.

Key Specification

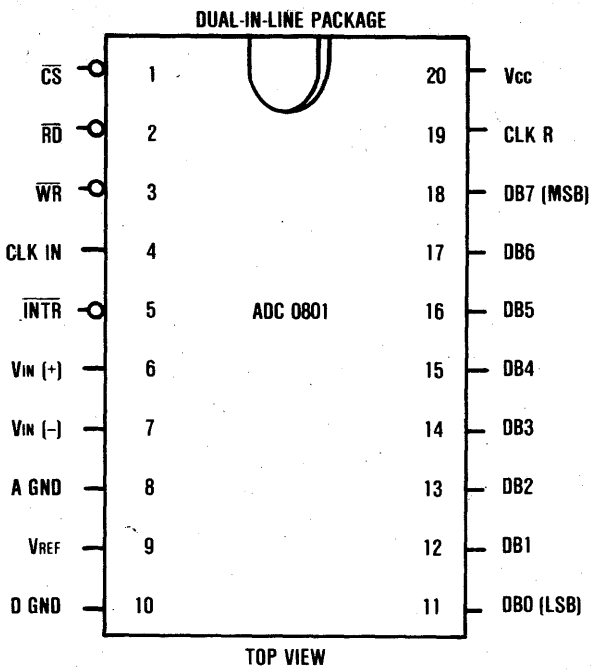
- Resolution: 8 Bits
- Linearity: ± 1/2 LSB
- Converstion time (Vcc = 6V): 50 μs
- Single supply: 5V DC
- Clock range 100 kHz to 1.28 MHz
- Operates ratiometric or with +5V DC, +2.5V DC, or "ANALOG SPAN ADJUSTED" voltage reference

TYPICAL APPLICATION



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CONNECTION DIAGRAM



20 PIN 0.3" WIDE DIL PACKAGE

Operation

The ADC 0801 contains a circuit equivalent of the 256R network. Analog switches are sequenced by successive approximation logic to match the analog difference input voltage [V_{IN} (+) - V_{IN} (-)] to a corresponding tap on the R network. The most significant bit is tested first and after 8 comparisons (64 clock cycles) a digital 8 bit binary code (1111 1111 = full scale) is transferred to an output latch and then an interrupt is asserted ($\overline{INTR}$ makes a high to low transition). The device may be operated in the free running mode by connecting $\overline{INTR}$ to the $\overline{WR}$ input with $\overline{CS}$ = 0. To insure start-up under all possible conditions, an external $\overline{WR}$ pulse is required during the first power up cycle. A conversion in process can be interrupted by issuing a second "start" command.

On the high to low transition of the $\overline{WR}$ input, the internal SAR latches and the shift register stages are reset. As long as the $\overline{CS}$ input and $\overline{WR}$ input remain low, the A/D will remain in a reset state. Conversion will not start until from 1 to 8 clock periods after at least one of these inputs makes a low to high transition.

Functional Description

DIGITAL CONTROL INPUTS

The digital control inputs ($\overline{CS}$, $\overline{RD}$, and $\overline{WR}$) have been designed to meet standard T^2L logic voltage levels. These signals have been re-named when compared to the "standard" A/D "START" and "OUTPUT ENABLE" labels. In addition, these inputs are active low to allow an easy interface to μP control busses. For non-μP based applications, the $\overline{CS}$ input (pin 1) can be grounded and the "standard" A/D "START" function is obtained by an active low pulse applied at the $\overline{WR}$ input (pin 3) and the "OUTPUT ENABLE" function is caused by an active low pulse at the $\overline{RD}$ input (pin 2).

THE ANALOG DIFFERENTIAL VOLTAGE INPUTS

This A/D has additional applications flexibility due to the unique analog differential voltage input feature. The V_{IN} (-) input (pin 7) can be used for "tare" correction to automatically subtract a fixed voltage value from the output reading. This is also useful in 4-20mA current loop conversion. In addition, "ground noise" problems can be reduced by making use of the differential input - especially when a dual sample and hold circuit is used (see applications section).

Finally, an analog input voltage with a reduced span and a relatively large "zero" offset can be easily handled by making use of the differential input (see the next section on the reference voltage).

The leads to the analog inputs (pins 6 and 7) should be kept as short as possible. Both noise and undesired digital clock coupling to these inputs can cause system errors. The source resistance for these inputs should be kept below 5 kΩ. If a low pass filter is required in the system, use a low valued series resistor ($\leq$ 5 kΩ) for a passive RC section or add an op amp RC active low pass filter. For low source resistance applications, a 0.1μF by-pass capacitor at the inputs will prevent pickup due to series lead inductance and a 1 kΩ series resistor can be used to isolate this capacitor from the output of an op amp (if used).

INPUT CURRENT

Due to the successive approximation switching action, currents will flow at the analog inputs. This is due to on-chip parasitic capacitance to ground. The voltage on this capacitor is switched and will result in currents entering or leaving the input pins which will depend on the analog input voltage levels. This "charge pumping" action is worse for continuous conversions with the analog input voltages at zero or full scale.

By-pass capacitors at the inputs will average these charges and cause a dc current to flow through the output resistances of the analog signal sources. For continuous conversions with a high clock frequency (fclk = MHz) with the analog inputs at zero volts, this dc current is at a maximum of approximately 1μA.

OFFSETTING ZERO

The zero of the A/D does not require adjustment. If the minimum analog input voltage value, VIN (min.), is above ground, a zero offset can be done. The converter can be made to output 0000 0000 digital code for this minimum input voltage by biasing the A/D VIN (-) input at this VIN (min.) value. This is making use of the differential mode operation of the A/D.

FULL SCALE ADJUSTMENT

The full scale adjustment can be made by applying a voltage which is 1-1/2 LSB of the desired analog voltage range to the VIN (+) input and then adjusting the magnitude of the VREF input (pin 9) for a digital output code which is just changing from "1111 1110" to "1111 1111".

REFERENCE VOLTAGE FLEXIBILITY

For maximum applications flexibility, the reference voltage has been designed to accommodate a +5VDC, +2.5VDC or an "adjusted" voltage level. This has been achieved in the design of the IC as shown in figure 1.

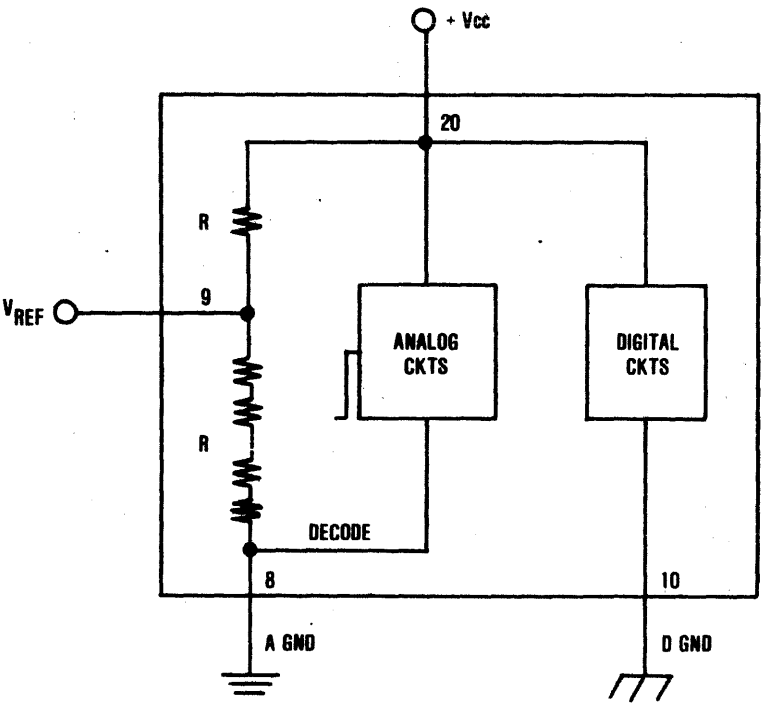


FIGURE 1: The $V_{REFERENCE}$ design on the IC

Notice that the reference voltage to the IC is either 1/2 of the voltage which is applied to the +Vcc supply pin, or is equal to the voltage which is externally "forced" to exist at the VREF pin. This allows for a ratiometric voltage reference using the +Vcc supply (where a capacitor can be connected from VREF to ground for noise rejection), a +5VDC reference voltage can be used for the +Vcc supply or any voltage can be applied to the VREF input for increased application flexibility. The internal "gain" to the VREF input is 2 to allow this factor of 2 reduction in the VREF voltage.

An example of the use of an "adjusted" reference voltage is to accommodate a reduced span - or dynamic voltage range of the analog input voltage. If the analog input voltage were to range from 0.5VDC to 3.5VDC, (instead of 0V to 5VDC) the span would be 3V. With +0.5VDC applied to the VIN (-) pin to absorb the "offset", the reference voltage can be made equal to 1/2 of the 3V span or +1.5VDC. The A/D now will encode the VIN (+) signal from 0.5V to 3.5V with the 0.5V input corresponding to "zero" and the +3.5VDC input corresponding to "full scale". The full 8 bits of resolution are therefore applied over this reduced analog input voltage range.

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SELF-CLOCKING OPTION

The clock for the A/D can be derived from the CPU clock or an external RC can be added to provide self-clocking. The "CLK IN" (pin 4) makes use of a Schmitt trigger as shown in figure 2.

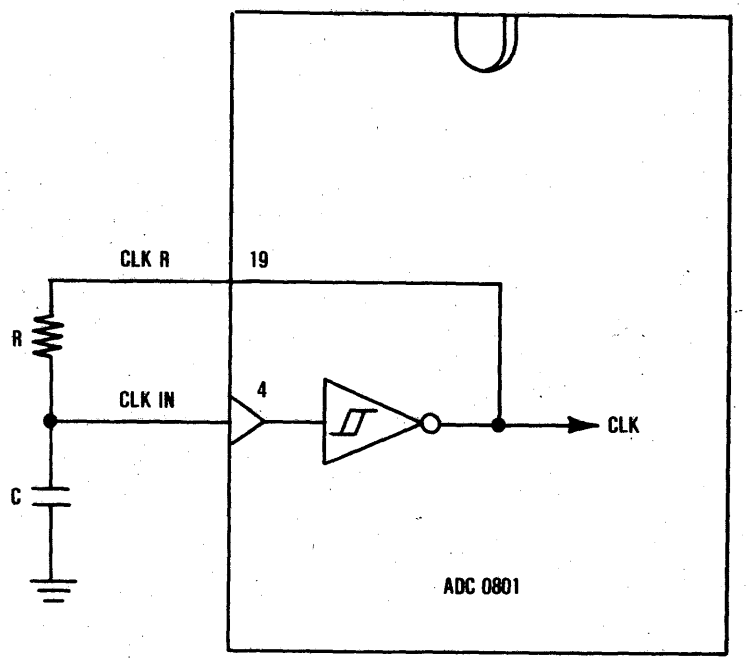


FIGURE 2: Self-clocking the A/D

Typical Applications

I. Interfacing 8080 μP Deviatives (8048, 8085)

This converter has been designed to directly interface with an 8080 A-2 μP (MICROBUS™ class 2). The A/D can be "mapped" into memory space (using standard memory address decoding for $\overline{CS}$ and the $\overline{MEMR}$ and $\overline{MEMW}$ strobes) or it can be controlled as an I/O device by using the $\overline{I/O\ R}$ and $\overline{I/O\ W}$ strobes and decoding the address bits $A_0 \rightarrow A_7$ (or address bits $A_8 \rightarrow A_{15}$ as they will contain the same 8 bit address information) to obtain the $\overline{CS}$ input. Using the I/O space provides 256 additional addresses and may allow a simpler 8 bit address decoder but the data can only be input to the accumulator, figure 3. To make use of the additional memory referenced instructions, the A/D should be "mapped" into memory space.

The standard control bus signals of the 8080 ($\overline{CS}$, $\overline{RD}$ and $\overline{WR}$) can be directly wired to the digital control inputs of the A/D and the bus timing requirements are met to allow both starting the converter and the outputting of the data onto the data bus. A bus driver should be used for larger μP systems where the data bus leaves the PC board and/or must drive capacitive loads larger than 100pF.

II. The Z-80 CPU

The Z-80 control bus is slightly different from that of the 8080. General $\overline{RD}$ and $\overline{WR}$ strobes are provided and separate memory request, $\overline{MREQ}$, and I/O request, $\overline{IORQ}$, signals are used which have to be combined with the generalized strobes to provide the equivalent 8080 signals. An advantage of operating the A/D in I/O space with the Z-80 is that the CPU will automatically insert one wait state (the $\overline{RD}$ and $\overline{WR}$ strobes are extended one clock period) to allow more time for the I/O devices to respond. Logic to map the A/D in I/O space is shown in figure 4.

III. Interfacing 6800 μP Derivatives (6502, etc.)

The control bus for the 6800 μP derivatives do not use $\overline{RD}$ and $\overline{WR}$ strobe signals. Instead they employ a single R/$\overline{W}$ line and additional synchronizing, if needed, could be derived from Ø2 clock. All I/O devices are memory mapped in the M6800 system and a special signal, VMA, indicates that the current address is valid. Figure 5 shows an interface schematic where the A/D is memory-mapped. Note that in many 6800 systems a decoded $\overline{4/5}$ line is brought out to the common bus at pin (21). This can be tied directly to the $\overline{CS}$ pin of the A/D provided that no other devices are addressed at ADDR : 4XXX or 5XXX.

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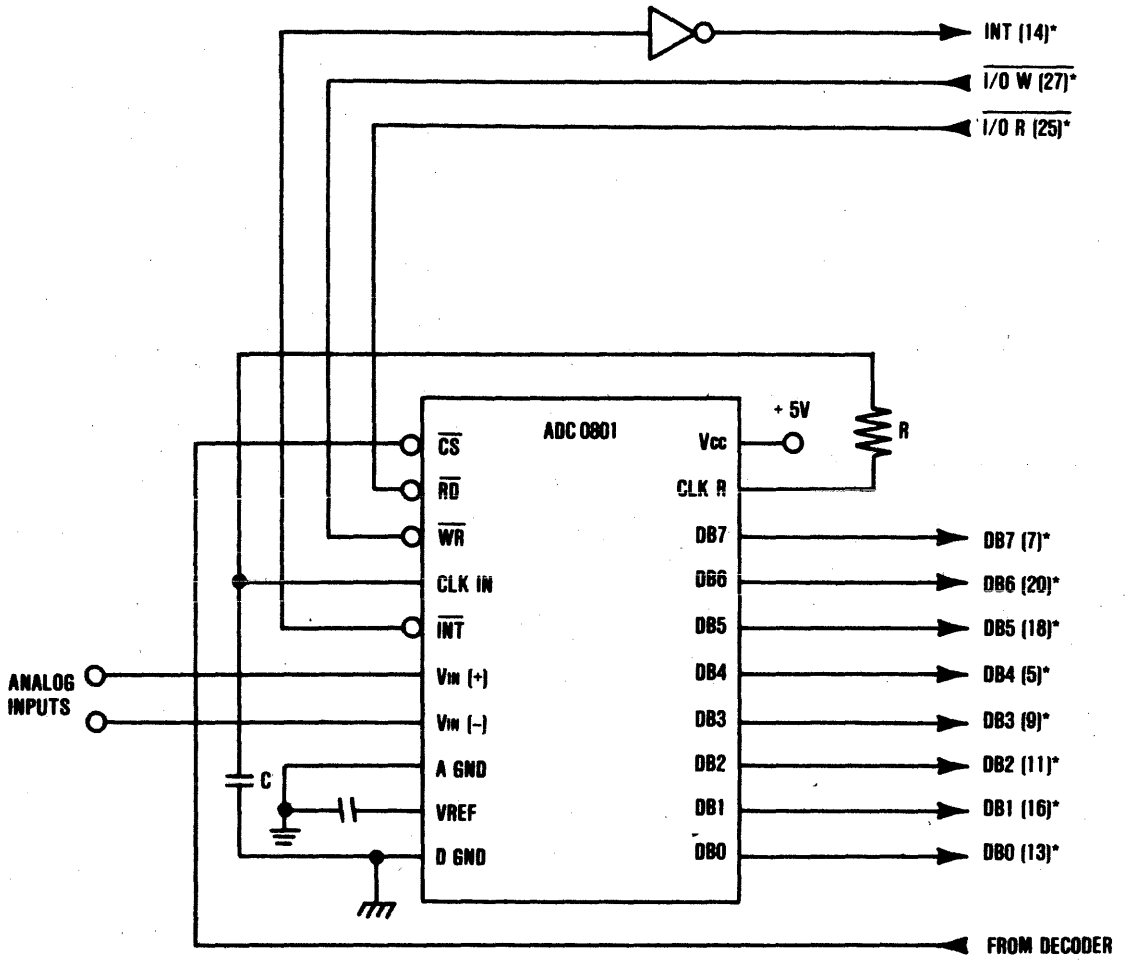


FIGURE 3: ADC0801 - INS8080A CPU Interface

Hardware Notes:
1. *Pin numbers for the INS8238 system controller.

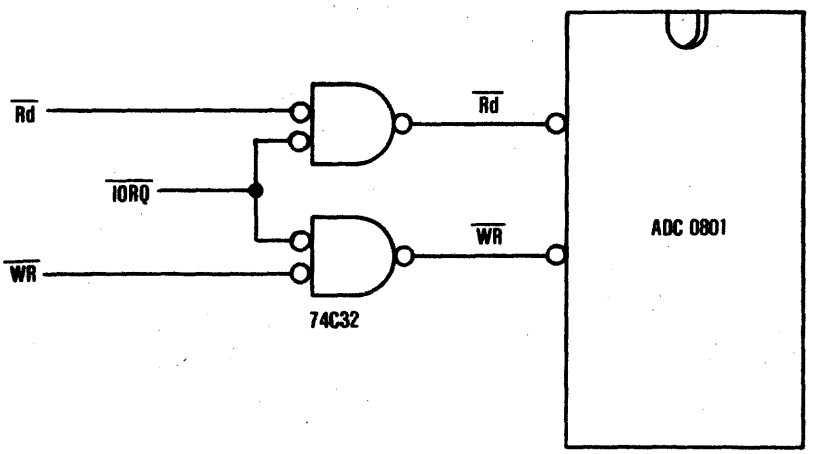
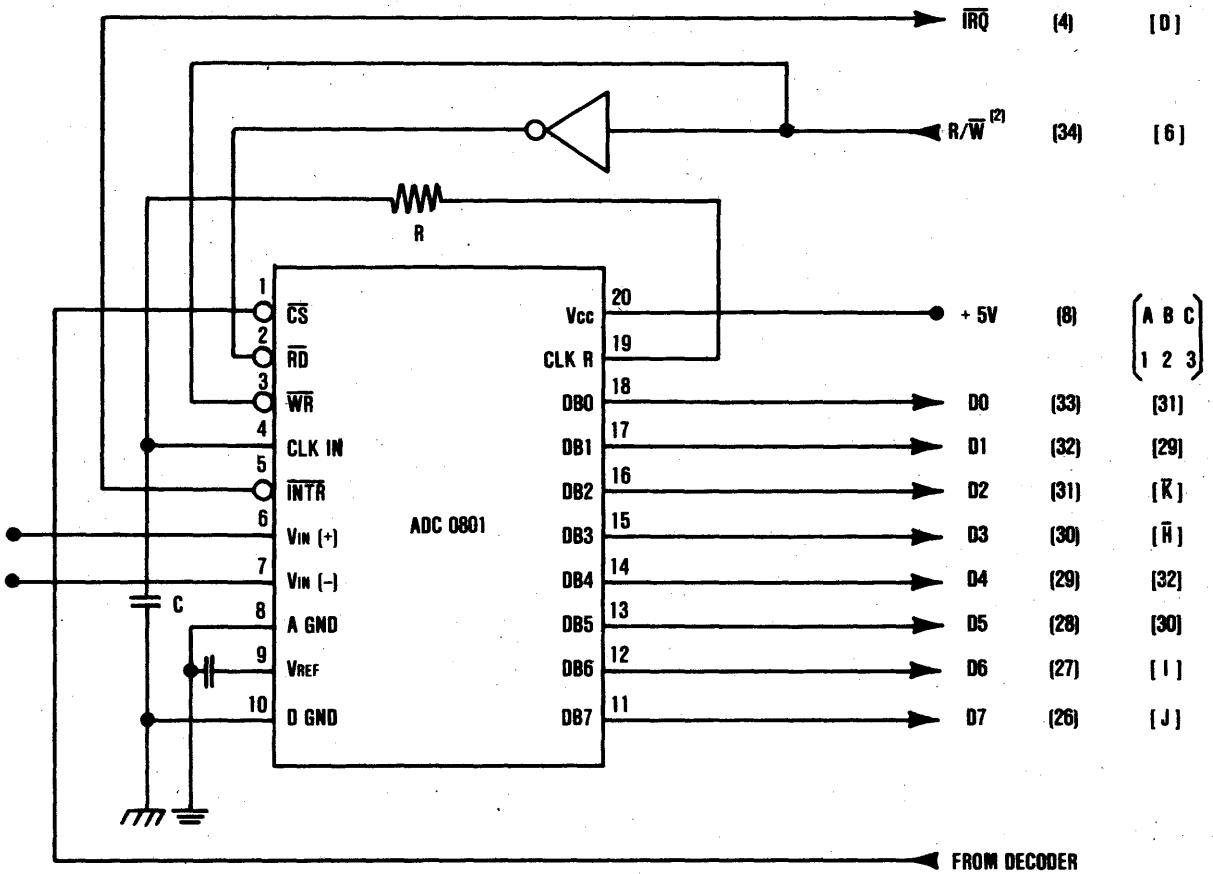


FIGURE 4: Mapping the A/D as an I/O device for use with the Z-80 CPU.

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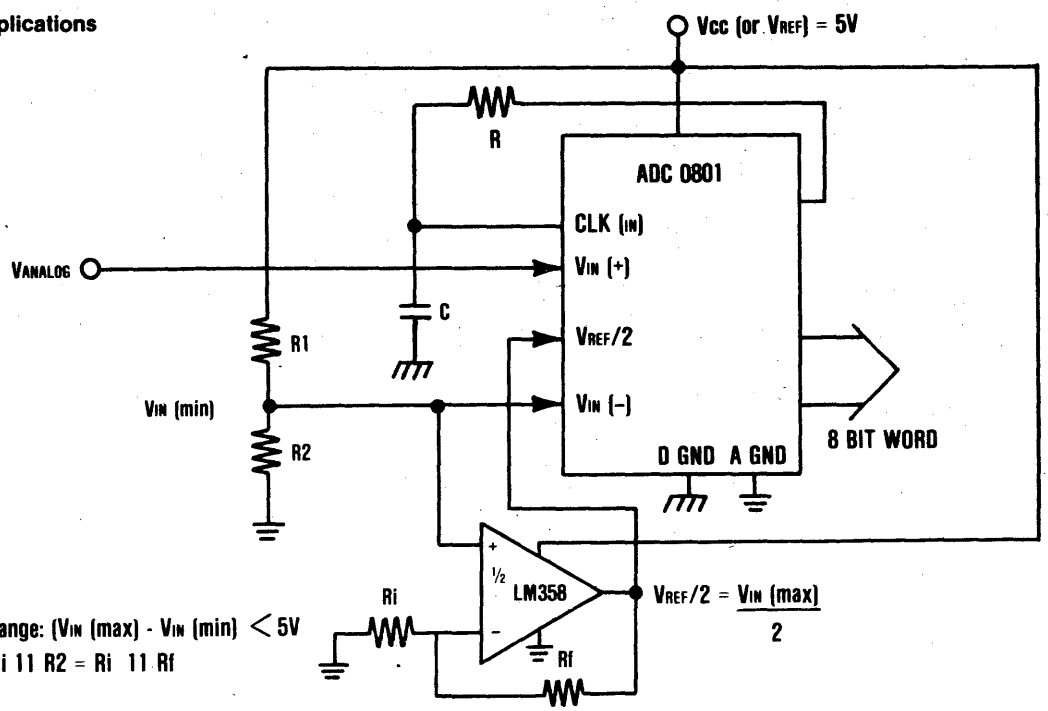


HARDWARE NOTES:

1. Numbers in parenthesis refer to MC6800 CPU unit. 2. Numbers or letters in brackets refer to standard M6800 system common bus code.

FIGURE 5: ADC0801 to MC6800 CPU Interface

IV. Miscellaneous Applications



- Analog input voltage range: (V_{IN} (max) - V_{IN} (min) $< 5V$
- $\frac{Rf}{Ri} + 1 = \frac{V_{IN}\text{ (max)}}{2\ V_{IN}\text{ (min)}}$; Ri 11 R2 = Ri 11 Rf
- If V_{IN} (min) is zero, the V_{IN} (-) pin of the A/D should be grounded, the LM358 should be connected as unity gain follower, and the center point of the R1, R2 divider should be = V_{IN} (max)/2.

FIGURE 6: Offsetting the zero, and accommodating the Naked 8™ for input voltage ranges less than 0 to 5V.

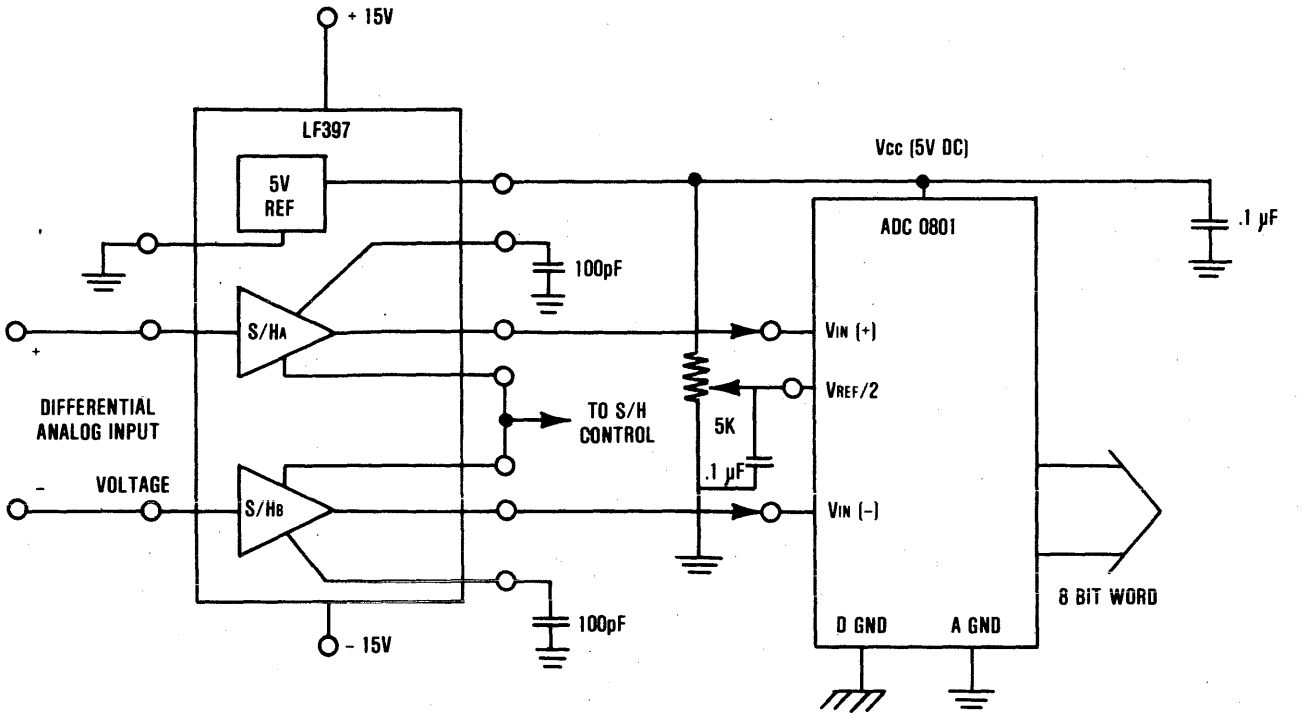


FIGURE 7: Interfacing the Naked 8™ with the LF397 data acquisition building block. The unique advantages of the Naked 8™ - DUAL S/H combination are very fast acquisition times, negligible hold mode errors and rejection of common mode signals.

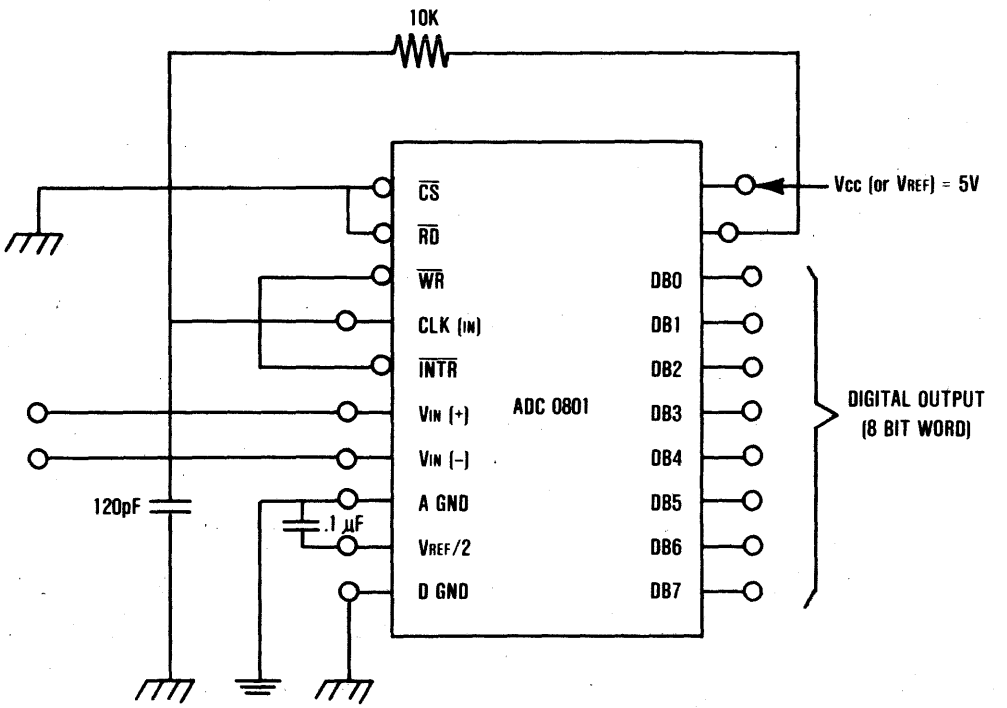
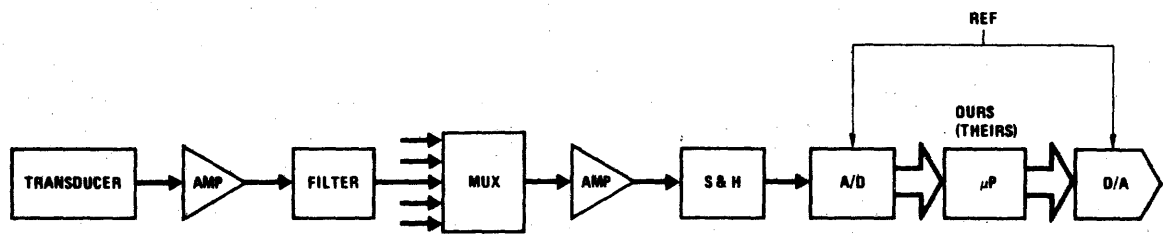


FIGURE 8: The Naked 8™ in a free running mode.

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General Data Acquisition System Block Diagram



PRESSURE
LX___
TEMPERATURE
LM334
LM335
LM3911
OTHERS
THERMOCOUPLE
RTD
AUDIO

LH0044
+RA201
LF352
LH0036
LH0037
LH0062

AF100
AF150
AF151

LF13508
LF13509
AM9709
AM97C09
LF13201
LF13333
AH5009

LF356
LF351
LF353
LF347

LF398
LH0023
LH0043
LH0053

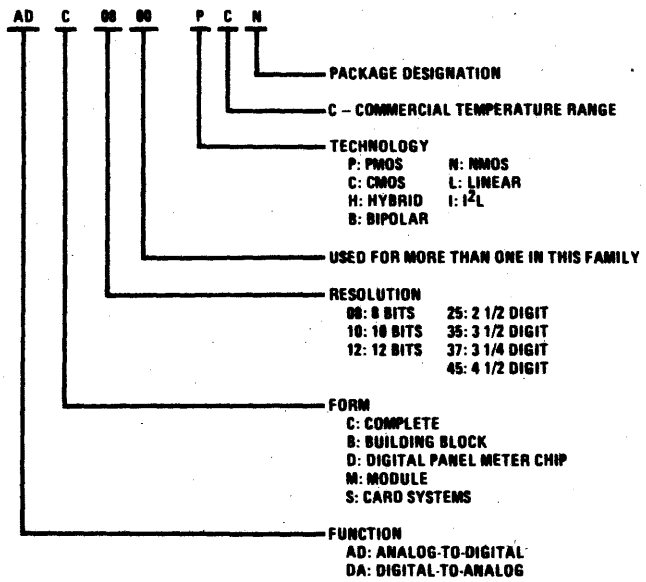
ADC0801
ADC0808
ADC0816
ADC0809
ADC1210
ADC3511
ADC3711
LF13300
+AD81200
DAC1200
+DM2504
OR 74C905
DAC0800
+DM2502/
DM2503

LM3900
LM329
LM336
LM336-5
LM399
LH0070/LH0071

DAC0800
DAC0808
DAC102X
DAC1280
DAC122X
DAC1280/
DAC1285
LM1408
AD7520
AD7521

OTHER DEVICES:
LM331 PRECISION VOLTAGE-TO-FREQUENCY CONVERTER
ADS1216 16-CHANNEL 12-BIT DATA ACQUISITION SYSTEM WITH MEMORY

A/D–D/A
Converter Products Part Numbering System



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A/D Converter/ DVM

RESOLUTION (BITS)	BASIC TYPE	LINEARITY @ 25°C (MAX) (%)	CONVERSION TIME (TYP)	OUTPUT LOGIC LEVELS	SUPPLIES (V)	TEMPERATURE RANGES AVAILABLE (°C)	COMMENTS
A/D CONVERTER							
8	ADC0800 (MM5357B)	0.8	100 μs	TTL TRI-STATE®	+5, −12	0 to +70, −55 to +125	
8	**ADC0801**	**0.2**	**100 μs**	**TTL TRI-STATE**	**+5**	**0 to +70, −40 to +85, −55 to +125**	**P, DIFF. INPUT (SPAN ADJ), .1% LIN AVAIL**
8	ADC0808	0.2	100 μs	TTL TRI-STATE	+5	−40 to +85, −55 to +125	Includes 8-Channel MUX
8	ADC0809	0.4	100 μs	TTL TRI-STATE	+5	−40 to +85, −55 to +125	Includes 8-Channel MUX
8	ADC0816	0.2	100 μs	TTL TRI-STATE	+5	−40 to +85, −55 to +125	16-Channel MUX, S and H Port
8	ADC0817	0.4	100 μs	TTL TRI-STATE	+5	−40 to +85, −55 to +125	16-Channel MUX, S and H Port
8†	TP3000	†	†	TTL	±12	0 to +70	†Companding Coder-Decoder
12	ADC1210	0.012	100 μs	CMOS	+5 to ±15	−25 to +85, −55 to +125	10-Bit Conversion in 30 μs
12 (10)	ADC1211	0.049	100 μs	CMOS	+5 to ±15	−25 to +85, −55 to +125	
12	LF13300	0.01	N/A	N/A	±15	0 to +70	Dual Slope ADC
	ADB1200	N/A	36 ms	TTL TRI-STATE	+5, −15	0 to +70	12-Bit Logic for LF13300
3 1/2-Digits	ADC3511	0.05	200 ms	TTL TRI-STATE	+5	0 to +70	Integrating μP ADC
3 3/4-Digits	ADC3711	0.05	400 ms	TTL TRI-STATE	+5	0 to +70	Integrating μP ADC
V-F	LM131	0.01	N/A	N/A	+5 to +40	0 to +70, −25 to +85, −55 to +125	Voltage-to-Frequency Converter, 100 kHz Max
DIGITAL VOLTMETER							
3 1/2-Digits	ADD3501	0.05	200 ms	7-Segment LED Drive	+5	0 to +70	3 1/2-Digit LED DPM
3 3/4-Digits	ADD3701	0.05	400 ms	7-Segment LED Drive	+5	0 to +70	3 3/4-Digit LED DPM

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RESOLUTION (BITS)	NATIONAL PART NUMBER	ALTERNATE SOURCE PART NUMBER	LINEARITY @ 25°C (MAX) (%)	INTERNAL REFERENCE	OUTPUT OP AMP	SUPPLIES (V)	TEMPERATURE RANGES AVAILABLE (°C)	COMMENTS
D/A CONVERTER								
8	DAC0802	DAC-08A, DAC-08H	0.1			±5 to ±15	0 to +70, −55 to +125	High Speed Multiplying
8	DAC0800	DAC-08, DAC-08E	0.19			±5 to ±15	0 to +70, −55 to +125	High Speed Multiplying
8	DAC0801	DAC-08C	0.39			±5 to ±15	0 to +70	High Speed Multiplying
8	DAC0806	MC1408-6	0.78			±5 to ±15	0 to +70	Multiplying
8	DAC0807	MC1408-7	0.39			±5 to ±15	0 to +70	Multiplying
8	DAC0808	MC1508-8/MC1408-8	0.19			±5 to ±15	0 to +70, −55 to +125	Multiplying
10	DAC1020	AD7520L/AD7530L	0.05			5 to 15	0 to +70, −55 to +125	4-Quadrant Multiplying
10	DAC1021	AD7520K/AD7530K	0.1			5 to 15	0 to +70, −55 to +125	4-Quadrant Multiplying
10	DAC1022	AD7520J/AD7530J	0.2			5 to 15	0 to +70, −55 to +125	4-Quadrant Multiplying
12	DAC1220	AD7521L/AD7531L	0.05			5 to 15	0 to +70, −55 to +125	4-Quadrant Multiplying
12	DAC1221	AD7521K/AD7531K	0.1			5 to 15	0 to +70, −55 to +125	4-Quadrant Multiplying
12	DAC1222	AD7521J/AD7531J	0.2			5 to 15	0 to +70, −55 to +125	4-Quadrant Multiplying
12	DAC1200		0.012	•	•	±15, 5	−25 to +85, −55 to +125	Complete DAC
12	DAC1201		0.049	•	•	±15, 5	−25 to +85, −55 to +125	Complete DAC
12	DAC1285	DAC85 (Binary)	0.012	•	•	±15, 5	−25 to +85, −55 to +125	Complete DAC
12	DAC1280	DAC80 (Binary)*	0.024	•	•	±15, 5	−25 to +85	Complete DAC
3-Digits	DAC1202		0.01	•	•	±15, 5	−25 to +85, −55 to +125	Complete BCD DAC
3-Digits	DAC1203		0.05	•	•	±15, 5	−25 to +85, −55 to +125	Complete BCD DAC
3-Digits	DAC1286	DAC85 (BCD)	0.05	•	•	+15, 5	−25 to +85, −55 to +125	Complete BCD DAC
3-Digits	DAC1287	DAC80 (BCD)*	0.1	•	•	±15, 5	−25 to +85	Complete BCD DAC

*Note. Minor specification differences

R_{ON} (Ω)	V_A/I (V)	PART NUMBER	LOGIC INPUT	V_S (V) TYP	t_{ON}/t_{OFF} TYP
Dual SPST					
10	±10	AH0141/DG141	TTL	−18, 12	0.8/1.1μs
30	±10	AH0133/DG133	TTL	−18, 12	0.5/0.9μs
80	±10	AH0134/DG134	TTL	−18, 12	0.5/0.9μs
15	±7.5	AH0151/DG151	TTL	±15	0.8/1.1μs
50	±7.5	AH0152/DG152	TTL	±15	0.5/0.9μs
*30	±7.5	AM181/DG181	TTL	±15, 5	180/150 ns
*75	±10	AM182/DG182	TTL	±15, 5	300/150 ns
Triple SPST					
*100	15 mA	AH5015	15V TTL		150/300 ns
*150	5 mA	AH5016	TTL		150/300 ns
Quad SPST					
200-600	±10	AH0015	TTL	−20, 10, 5	100/400 ns
*200	±10	LF11201	TTL	±15	90/500 ns
*200	±10	LF11202	TTL	±15	90/500 ns
*200	±10	LF11331	TTL	±15	90/500 ns
*200	±10	LF11332	TTL	±15	90/500 ns
*200	±10	LF11333	TTL	±15	90/500 ns
*250	±10	LF13201	TTL	±15	90/500 ns
*250	±10	LF13202	TTL	±15	90/500 ns
*250	±10	LF13331	TTL	±15	90/500 ns
*250	±10	LF13332	TTL	±15	90/500 ns
*250	±10	LF13333	TTL	±15	90/500 ns
280	±7.5	CD4066	CMOS	±7.5	
850	±7.5	CD4016	CMOS	±7.5	
*100	15 mA	AH5011/AM9711	15V TTL		150/300 ns
*100	10 mA	AM97C11	CMOS		150/300 ns
*150	5 mA	AH5012/AM9712	TTL		150/300 ns
*150	3 mA	AM97C12	CMOS		150/300 ns
*30	±7.5	AM193	TTL	±15, 5	180/150 ns
*75	±10	AM194	TTL	±15, 5	300/150 ns

R_{ON} (Ω)	V_A/I (V)	PART NUMBER	LOGIC INPUT	V_S (V) TYP	t_{ON}/t_{OFF} TYP
SPDT					
10	±10	AH0146/DG146	TTL	−18, 12	0.8/1.1μs
30	±10	AH0144/DG144	TTL	−18, 12	0.5/0.9μs
80	±10	AH0143/DG143	TTL	−18, 12	0.5/0.9μs
15	±7.5	AH0161/DG161	TTL	±15	0.8/1.1μs
50	±7.5	AH0162/DG162	TTL	±15	0.5/0.9μs
100	±9	AH2114 (Sw. 1)	15V TTL	±15	35/600 ns
		(Sw. 2)			1.2μs/50 ns
*30	±7.5	AM187/DG187	TTL	±15, 5	180/150 ns
*75	±10	AM188/DG188	TTL	±15, 5	300/150 ns
Dual SPDT					
*30	±7.5	AM190/DG190	TTL	±15, 5	180/150 ns
*75	±10	AM191/DG191	TTL	±15, 5	300/150 ns
Triple SPDT					
280	±7.5	CD4053	CMOS	±7.5	150/150 ns
Dual DPST					
10	±10	AH0140/DG140	TTL	−18, 12	0.8/1.1μs
30	±10	AH0129/DG129	TTL	−18, 12	0.5/0.9μs
80	±10	AH0126/DG126	TTL	−18, 12	0.5/0.9μs
15	±7.5	AH0153/DG153	TTL	±15	0.8/1.1μs
50	±7.5	AH0154/DG154	TTL	±15	0.5/0.9μs
200-600	±10	AH0019	TTL	−20, 10, 5	100/400 ns
*30	±7.5	AM184/DG184	TTL	±15.5	180/150 ns
*75	±10	AM185/DG185	TTL	±15.5	300/150 ns
Dual DPDT					
10	±10	AH0145/DG145	TTL	−18, 12	0.8/1.1μs
30	±10	AH0139/DG139	TTL	−18, 12	0.5/0.9μs
80	±10	AH0142/DG142	TTL	−18, 12	0.5/0.9μs
15	±7.5	AH0163/DG163	TTL	±15	0.8/1.1μs
50	±7.5	AH0164/DG164	TTL	±15	0.5/0.9μs
200-600	±10	AH0014	TTL	−20, 10, 5	350/400 ns

R_{ON} (Ω)	V_A/I (V)	PART NUMBER	LOGIC INPUT	V_S (V) TYP	t_{ON}/t_{OFF} TYP
MULTIPLEXERS					
3-Channel					
*100	15 mA	AH5013	15V TTL		150/300 ns
*150	5 mA	AH5014	TTL		150/300 ns
4-Channel					
*100	15 mA	AH5009/AM9709	15V TTL		150/300 ns
*100	10 mA	AM97C09	CMOS		150/300 ns
*150	5 mA	AH5010/AM9710	TTL		150/300 ns
*150	3 mA	AM97C10	CMOS		150/300 ns
4-Channel Differential					
280	±7.5	CD4052	CMOS	±7.5	150/150 ns
*350	12,−15	LF11509	TTL	±15	1/0.2μs
270	±7.5	CD4529B	CMOS	±7.5	50/50 ns
6-Channel					
250-1500	50 mA	AM2009/MM4504/ MM5504	TTL	−15, 5	
8-Channel					
250-400	±5	AM3705	TTL	−15, 5	300/600 ns
*350	12,−15	LF11508	TTL	±15	1/0.2μs
270	±7.5	CD4529B	CMOS	±7.5	50/50 ns
280	±7.5	CD4051	CMOS	±7.5	150/150 ns

Notes:

R_{ON} max @ T_A = 25°C

V_A/I = maximum voltage or current to be safely switched

Part number = basic number/alternate number (i.e., AM181/DG181). May be ordered by either number.

*Preferred devices

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National Semiconductor

JULY 1978

LM131A/LM131, LM231A/LM231, LM331A/LM331 Precision Voltage-to-Frequency Converters

General Description

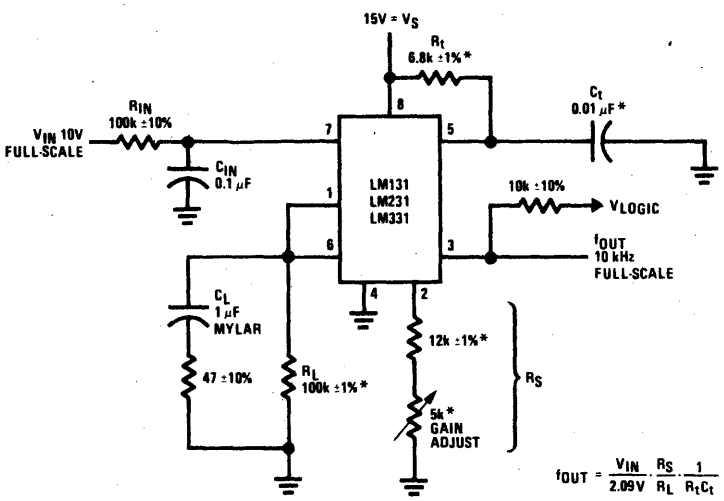
The LM131/LM231/LM331 family of voltage-to-frequency converters are ideally suited for use in simple low-cost circuits for analog-to-digital conversion, precision frequency-to-voltage conversion, long-term integration, linear frequency modulation or demodulation, and many other functions. The output when used as a voltage-to-frequency converter is a pulse train at a frequency precisely proportional to the applied input voltage. Thus, it provides all the inherent advantages of the voltage-to-frequency conversion techniques, and is easy to apply in all standard voltage-to-frequency converter applications. Further, the LM131A/LM231A/LM331A attains a new high level of accuracy versus temperature which could only be attained with expensive voltage-to-frequency modules. Additionally the LM131 is ideally suited for use in digital systems at low power supply voltages and can provide low-cost analog-to-digital conversion in microprocessor-controlled systems. And, the frequency from a battery powered voltage-to-frequency converter can be easily channeled through a simple photoisolator to provide isolation against high common mode levels.

The LM131/LM231/LM331 utilizes a new temperature-compensated band-gap reference circuit, to provide excellent accuracy over the full operating temperature range, at power supplies as low as 4.0V. The precision timer circuit has low bias currents without degrading the quick response necessary for 100kHz voltage-to-frequency conversion. And the output is capable of driving 3 TTL loads, or a high voltage output up to 40V, yet is short-circuit-proof against V_{CC}.

Features

- Guaranteed linearity 0.01% max
- Improved performance in existing voltage-to-frequency conversion applications
- Split or single supply operation
- Operates on single 5V supply
- Pulse output compatible with all logic forms
- Excellent temperature stability, ±50ppm/°C max
- Low power dissipation, 15mW typical at 5V
- Wide dynamic range, 100dB min at 10kHz full scale frequency
- Wide range of full scale frequency, 1Hz to 100kHz
- Low cost

Typical Applications



*Use stable components with low temperature coefficients. See applications notes.

FIGURE 1. Simple Stand-Alone Voltage-to-Frequency Converter with ±0.03% Typical Linearity (f = 10 Hz to 11 kHz)

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IM-B25M78/Printed in U.S.A.

Absolute Maximum Ratings

	LM131A/LM131	LM231A/LM231	LM331A/LM331
Supply Voltage	40V	40V	40V
Output Short Circuit to Ground	Continuous	Continuous	Continuous
Output Short Circuit to V_S	Continuous	Continuous	Continuous
Input Voltage	−0.2V to +V_S	−0.2V to +V_S	−0.2V to +V_S
	T_{MIN} T_{MAX}	T_{MIN} T_{MAX}	T_{MIN} T_{MAX}
Operating Ambient Temperature Range	−55°C to +125°C	−25°C to +85°C	0°C to +70°C

Electrical Characteristics

T_A = 25°C unless otherwise specified. (Note 1)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
VFC Non-Linearity (Note 2)	4.5V ≤ V_S ≤ 20V		±0.003	±0.01	% Full-Scale
	T_{MIN} ≤ T_A ≤ T_{MAX}		±0.006	±0.02	% Full-Scale
In Circuit of *Figure 1*	V_S = 15V, f = 10 Hz to 11 kHz		±0.024	±0.14	% Full-Scale
Conversion Accuracy Scale Factor (Gain)	V_{IN} = −10V, R_S = 14 kΩ				
LM131, LM131A, LM231, LM231A		0.95	1.00	1.05	kHz/V
LM331, LM331A		0.90	1.00	1.10	kHz/V
Temperature Stability of Gain	T_{MIN} ≤ T_A ≤ T_{MAX}, 4.5V ≤ V_S ≤ 20V				
LM131/LM231/LM331			±30	±150	ppm/°C
LM131A/LM231A/LM331A			±20	±50	ppm/°C
Change of Gain with V_S	4.5V ≤ V_S ≤ 10V		0.01	0.1	%/V
	10V ≤ V_S ≤ 40V		0.006	0.06	%/V
Rated Full-Scale Frequency	V_{IN} = −10V	10.0			kHz
Overrange (Beyond Full-Scale) Frequency	V_{IN} = −11V	10			%
INPUT COMPARATOR					
Offset Voltage			±3	±10	mV
LM131/LM231/LM331	T_{MIN} ≤ T_A ≤ T_{MAX}		±4	±14	mV
LM131A/LM231A/LM331A	T_{MIN} ≤ T_A ≤ T_{MAX}		±3	±10	mV
Bias Current			−80	−300	nA
Offset Current			±8	±100	nA
Common-Mode Range	T_{MIN} ≤ T_A ≤ T_{MAX}	−0.2		V_{CC}−2.0	V
TIMER					
Timer Threshold Voltage, Pin 5		0.63	0.667	0.70	x V_S
Input Bias Current, Pin 5	V_S = 15V				
All Devices	0V ≤ $V_{PIN\ 5}$ ≤ 9.9V		±10	±100	nA
LM131/LM231/LM331	$V_{PIN\ 5}$ = 10V		200	1000	nA
LM131A/LM231A/LM331A	$V_{PIN\ 5}$ = 10V		200	500	nA
$V_{SAT\ PIN\ 5}$ (Reset)	I = 5 mA		0.22	0.5	V
CURRENT SOURCE (Pin 1)					
Output Current	R_S = 14 kΩ, $V_{PIN\ 1}$ = 0				
LM131, LM131A, LM231, LM231A		126	135	144	μA
LM331, LM331A		116	136	156	μA
Change with Voltage	0V ≤ $V_{PIN\ 1}$ ≤ 10V		0.2	1.0	μA
Current Source OFF Leakage					
LM131, LM131A			0.01	1.0	nA
LM231, LM231A, LM331, LM331A			0.02	10.0	nA
All Devices	T_A = T_{MAX}		2.0	50.0	nA
Operating Range of Current (Typical)			(10 to 500)		μA
REFERENCE VOLTAGE (Pin 2)					
LM131, LM131A, LM231, LM231A		1.76	1.89	2.02	V_{DC}
LM331, LM331A		1.70	1.89	2.08	V_{DC}
Stability vs Temperature			±60		ppm/°C
Stability vs Time, 1000 Hours			±0.1		%

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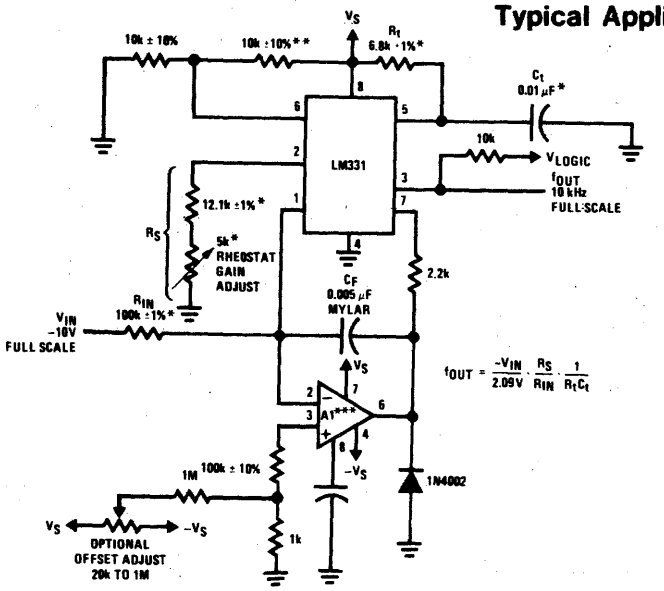
Electrical Characteristics (Continued) $T_A = 25°C$ unless otherwise specified (Note 1)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
LOGIC OUTPUT (Pin 3)					
V_{SAT}	I = 5 mA		0.15	0.50	V
	I = 3.2 mA (2 TTL Loads), $T_{MIN} \leq T_A \leq T_{MAX}$		0.10	0.40	V
OFF Leakage			±0.05	1.0	μA
SUPPLY CURRENT					
LM131, LM131A, LM231,	V_S = 5V	2.0	3.0	4.0	mA
LM231A	V_S = 40V	2.5	4.0	6.0	mA
LM331, LM331A	V_S = 5V	1.5	3.0	6.0	mA
	V_S = 40V	2.0	4.0	8.0	mA

Note 1: All specifications apply in the circuit of *Figure 3*, with $4.0V \leq V_S \leq 40V$, unless otherwise noted.

Note 2: Nonlinearity is defined as the deviation of f_{OUT} from V_{IN} x (10 kHz/−10 V_{DC}) when the circuit has been trimmed for zero error at 10 Hz and at 10 kHz, over the frequency range 1 Hz to 11 kHz. For the timing capacitor, C_T, use NPO ceramic, Teflon*, or polystyrene.

Typical Applications



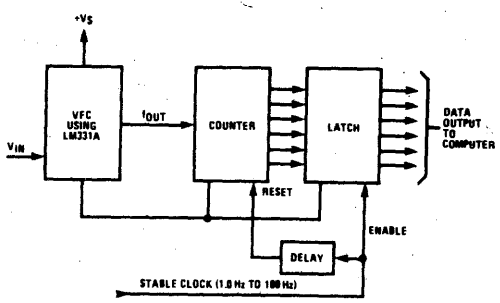
*Use stable components with low temperature coefficients. See applications notes.

**This resistor can be 5 kΩ or 10 kΩ for V_S = 8V to 22V, but must be 10 kΩ for V_S = 4.5V to 8V.

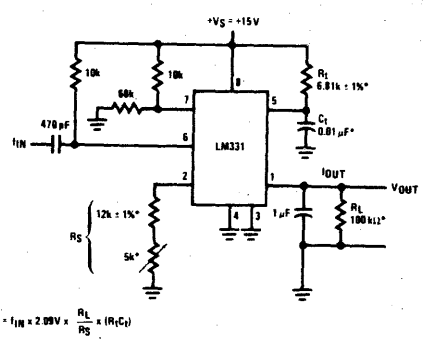
***Use low offset voltage and low offset current op amps for A1: recommended types LM108, LM308A, LF351B

Standard Test Circuit and Applications Circuit, Precision Voltage-to-Frequency Converter

Basic Analog-to-Digital Converter Using Voltage-to-Frequency Converter

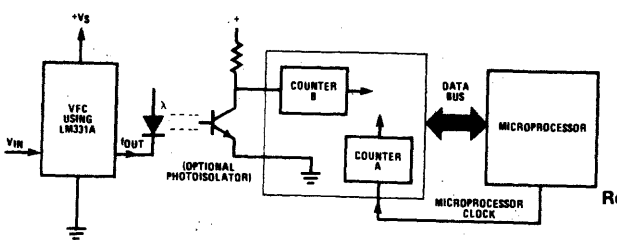


Simple Frequency-to-Voltage Converter, 10 kHz Full-Scale, ±0.06% Non-Linearity

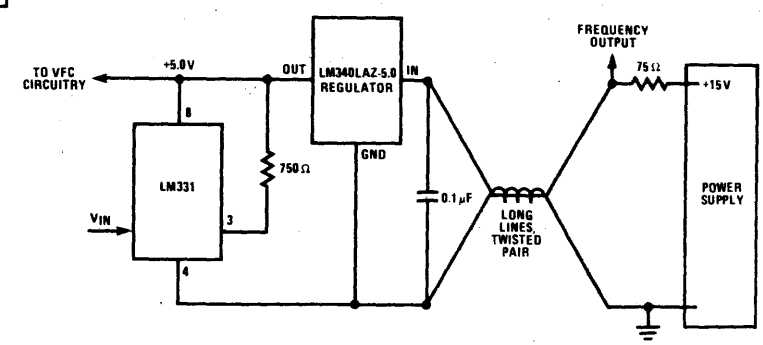


*Use stable components with low temperature coefficients.

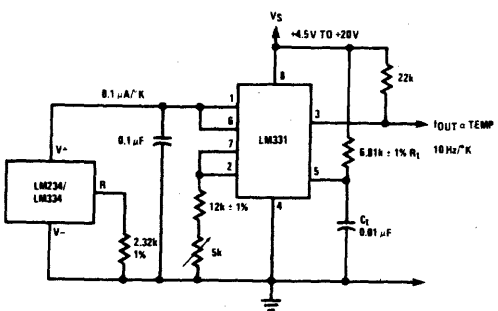
Analog-to-Digital Converter with Microprocessor



Remote Voltage-to-Frequency Converter with 2-Wire Transmitter and Receiver



Temperature to Frequency Converter



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National Semiconductor

DAC1020 10-Bit Binary Multiplying D/A Converter
DAC1220 12-Bit Binary Multiplying D/A Converter

General Description

The DAC1020 and the DAC1220 are, respectively, 10 and 12-bit binary multiplying digital-to-analog converters. A deposited thin film R-2R resistor ladder divides the reference current and provides the circuit with excellent temperature tracking characteristics (0.0002%/°C linearity error temperature coefficient maximum). The circuit uses CMOS current switches and drive circuitry to achieve low power consumption (30 mW max) and low output leakages (200 nA max). The digital inputs are compatible with DTL/TTL logic levels as well as full CMOS logic level swings. This part, combined with an external amplifier and voltage reference, can be used as a standard D/A converter; however, it is also very attractive for multiplying applications (such as digitally controlled gain blocks) since its linearity error is essentially independent of the voltage reference. All inputs are protected from damage due to static discharge by diode clamps to V^+ and ground.

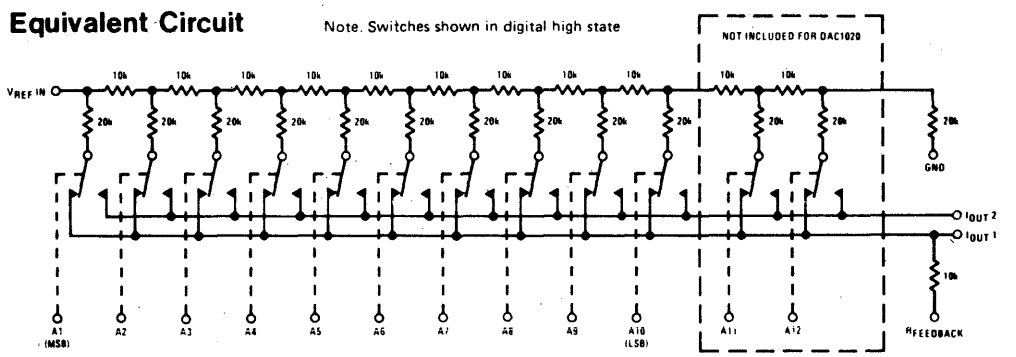
This part is available with 10-bit (0.05%), 9-bit (0.10%), and 8-bit (0.20%) non-linearity guarenteed over temperature (note 1 of electrical characteristics). The DAC1020, DAC1021, and DAC1022 are direct replacements for the 10-bit resolution AD7520 and AD7530 family. The DAC1220, DAC1221, and DAC1222 are direct replacements for the 12-bit resolution AD7521 and AD7531 family.

Features

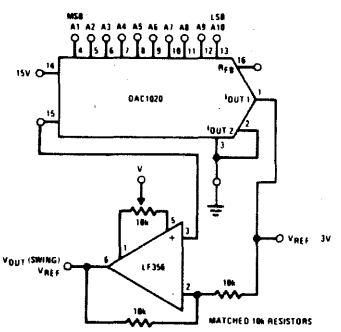
- Non-linearity guaranteed over temperature
- Integrated thin film on CMOS structure
- 10-bit or 12-bit resolution
- Low power dissipation 10 mW @ 15V typ
- Accepts variable or fixed reference $-25V \leq V_{REF} \leq +25V$
- 4-quadrant multiplying capability
- Interfaces directly with DTL, TTL and CMOS
- Fast settling time—500 ns typ
- Low feedthrough error—1/2 LSB @ 100 kHz typ

Equivalent Circuit

Note. Switches shown in digital high state



Typical Applications

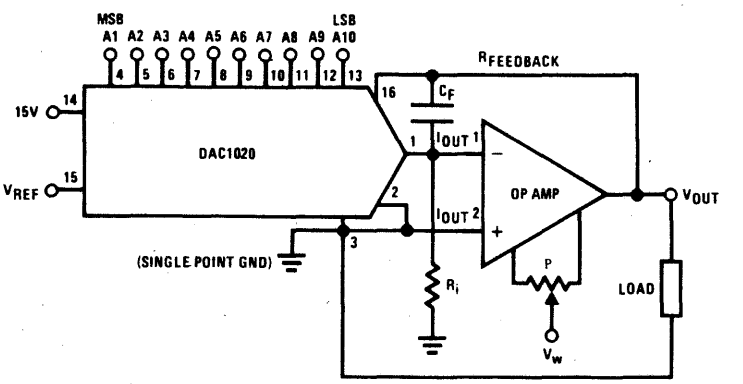


TRUE OFFSET BINARY OPERATION

DIGITAL INPUT										V_{OUT}
1	1	1	1	1	1	1	1	1	1	$V_{REF} \times 1022/1024$
1	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0	$-V_{REF}$

$t_S = 1.8\ \mu s$
use LM336 for a voltage reference

Bipolar Configuration with a Single Op Amp



$$V_{OUT} = -V_{REF}\left(\frac{A1}{2} + \frac{A2}{4} + \frac{A3}{8} + \ldots \frac{A10}{1024}\right)$$

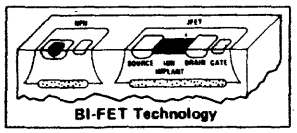
$-10V \leq V_{REF} \leq 10V$

$0 \leq V_{OUT} \leq -\frac{1023}{1024} V_{REF}$

where $A_N = 1$ if the A_N digital input is high
$A_N = 0$ if the A_N digital input is low

Basic Connection: Unipolar or 2-Quadrant Multiplying Configuration (Digital Attenuator)

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LF11508/LF12508/LF13508
8-channel analog multiplexer
LF11509/LF12509/LF13509
4-channel differential analog multiplexer

general description

The LF11508/LF12508/LF13508 is an 8-channel analog multiplexer which connects the output to 1 of the 8 analog inputs depending on the state of a 3-bit binary address. An enable control allows disconnecting the output, thereby providing a package select function.

This device is fabricated with National's BI-FET technology which provides ion-implanted JFETs for the analog switch on the same chip as the bipolar decode and switch drive circuitry. This technology makes possible low constant "ON" resistance with analog input voltage variations. This device does not suffer from latch-up problems or static charge blow-out problems associated with similar CMOS parts. The digital inputs are designed to operate from both TTL and CMOS levels while always providing a definite break-before-make action.

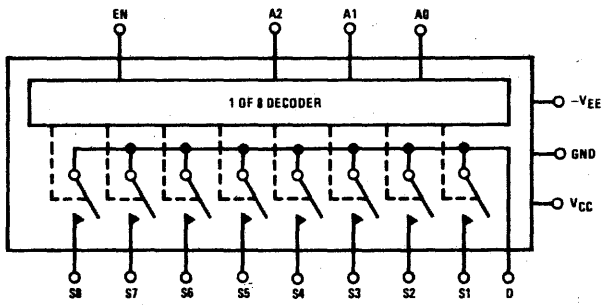
The LF11509/LF12509/LF13509 is a 4-channel differential analog multiplexer. A 2-bit binary address will connect a pair of independent analog inputs to one of any 4 pairs of independent analog outputs. The device has all the features of the LF11508 series and should be used whenever differential analog inputs are required.

features

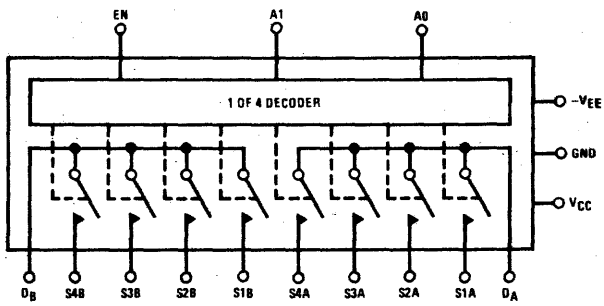
- JFET switches rather than CMOS
- No static discharge blow-out problem
- No SCR latch-up problems
- Analog signal range 11V, −15V
- Constant "ON" resistance for analog signals between −11V and 11V
- "ON" resistance 380 Ω typ
- Digital inputs compatible with TTL and CMOS
- Output enable control
- Break-before-make action: t_{OFF} = 0.2 μs; t_{ON} = 2 μs typ

functional diagrams

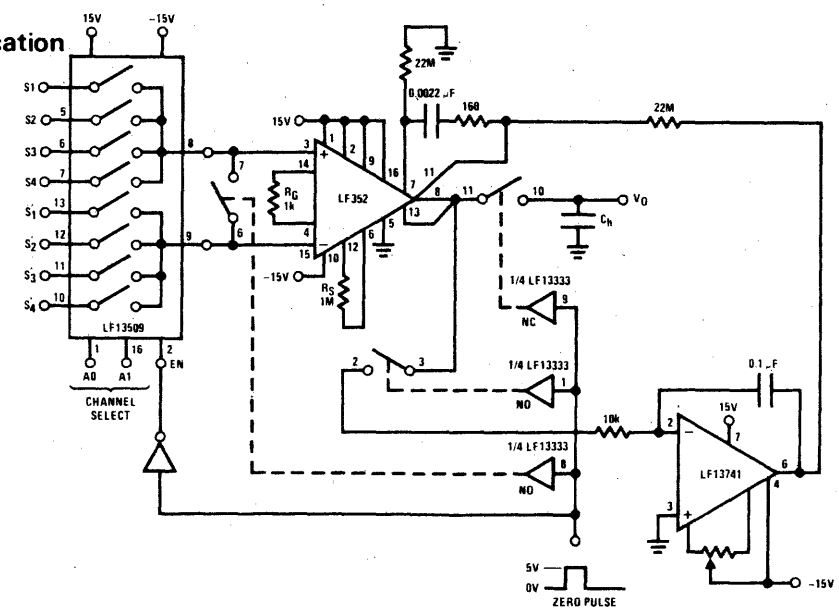
LF11508/LF12508/LF13508



LF11509/LF12509/LF13509

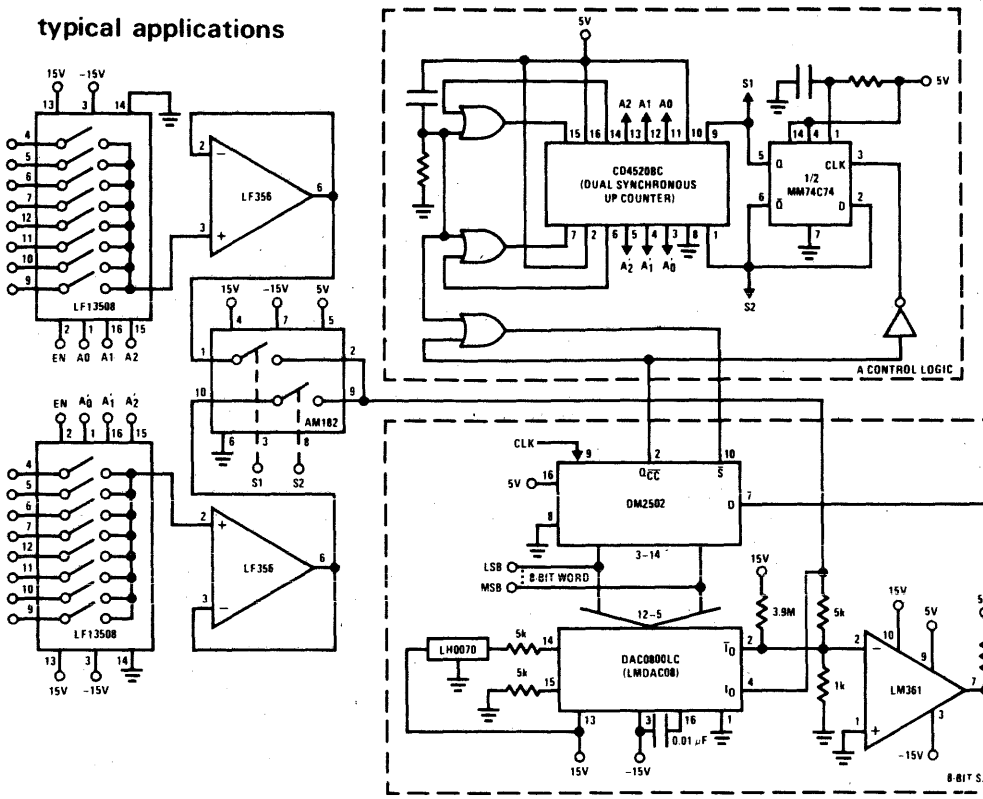


typical application

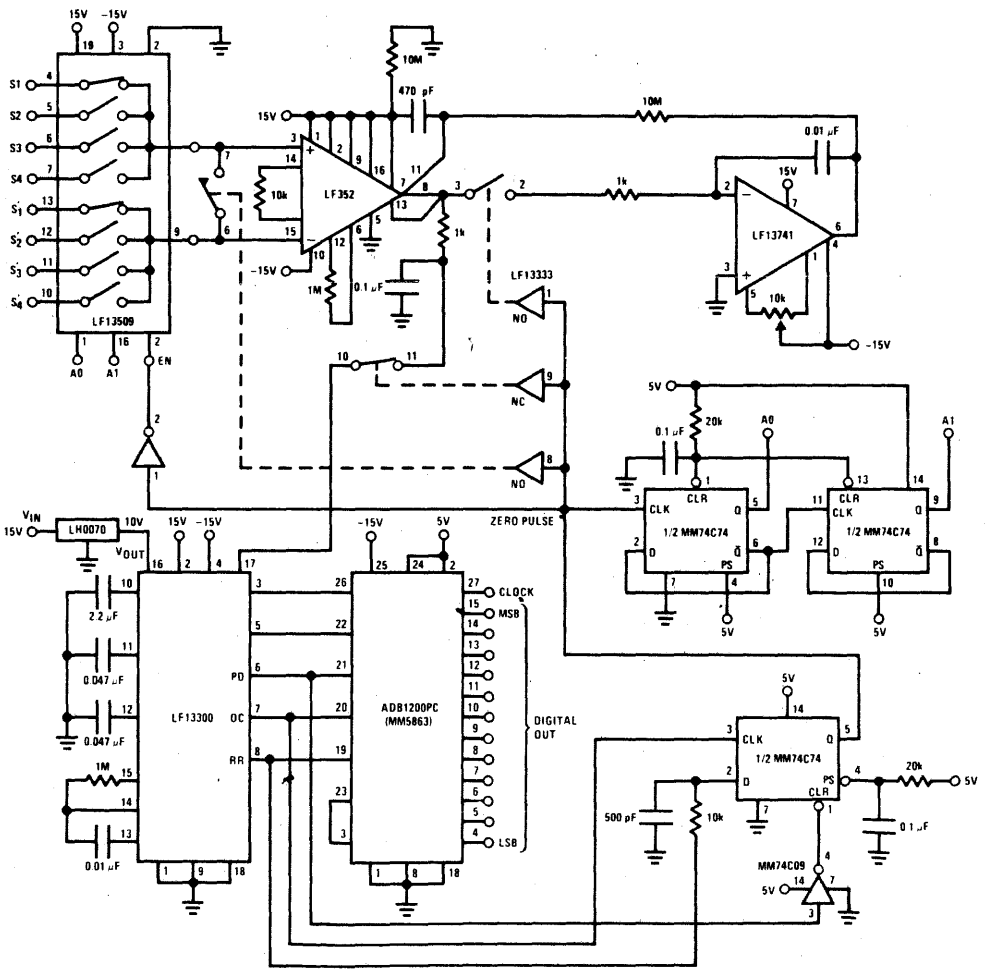


- Differential multiplexer disabled during auto zeroing
- Minimum zeroing pulse width will depend upon the integrator R1C
- This scheme provides input offset adjust especially useful with high gain connections. The device, LF352, provides pins for output offset adjust. For more details, see LF352 data sheet.

4-Channel Differential Multiplexer with Auto Zeroed Instrumentation Amplifier



A Fast 16-Channel DAU with Second Level Multiplexing



- f_{CLOCK} max = 200 kHz
- The LF352 instrumentation amplifier is auto zeroed during offset correction cycle of the LF13300 A/D
- The system accuracy will mostly depend on the instrumentation amplifier gain linearity

4-Channel Differential Multiplexer with Auto Zeroed Instrumentation Amplifier and 12-Bit A/D Converter

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National Semiconductor

Analog-to-Digital Converters

ADC0808, ADC0809 Single Chip Data Acquisition System

General Description

The ADC0808, ADC0809 data acquisition components are monolithic CMOS devices with an 8-bit analog-to-digital converter, 8-channel multiplexer and microprocessor compatible control logic. The 8-bit A/D converter uses successive approximation as the conversion technique. The converter features a high impedance chopper stablilzed comparator, a 256R voltage divider with analog switch tree and a successive approximation register. The 8-channel multiplexer can directly access any one of 8-single-ended analog signals.

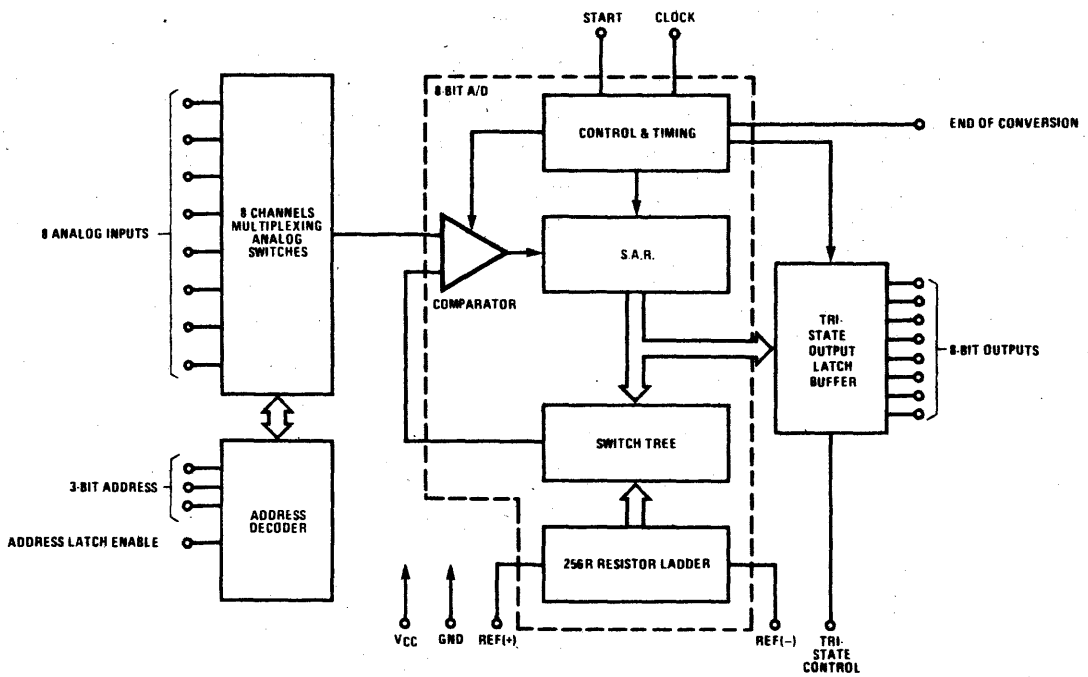
The device eliminates the need for external zero and full-scale adjustments and features an absolute accuracy $\leq$ 1 LSB including quantizing error. Easy interfacing to microprocessors is provided by the latched and decoded address inputs and latched TTL TRI-STATE® outputs.

The design of the ADC0808, ADC0809 has been optimized by incorporating the most desirable aspects of several A/D conversion techniques. The ADC0808, ADC0809 offers high speed, high accuracy, minimal temperature dependence, excellent long-term accuracy and repeatability, and consumes minimal power. These features make this device ideally suited to applications such as process control, industrial control, and machine control. For 16-channel multiplexer with common output (sample/hold port) see ADC0816 data sheet.

Features

- Total unadjusted error $<$ ±1/2 LSB
- Linearity error $<$ ±1/2 LSB
- No missing codes
- Guaranteed monotonicity
- No offset adjust required
- No scale adjust required
- Conversion time of 100 μs
- Easy microprocessor interface
- Latched TRI-STATE output
- Latched address input
- Ratiometric conversion
- Single 5V supply
- Low power consumption—15 mW
- Full −55°C to +125°C operation available

Block Diagram



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National Semiconductor

ADC0816/ADC0817 Single Chip Data Acquisition System

General Description

The ADC0816, ADC0817 (MM74C948) data acquisition components are monolithic CMOS devices with an 8-bit analog-to-digital converter, a 16-channel multiplexer and microprocessor compatible control logic. The 8-bit A/D converter uses successive approximation as the conversion technique. The converter features a high impedance chopper stabilized comparator, a 256R voltage divider with analog switch tree and a successive approximation register. The 16-channel multiplexer can directly access any one of 16 single-ended analog signals and provides the logic for additional channel expansion. Signal conditioning of any analog input signal is eased by direct access to the input of the 8-bit A/D converter.

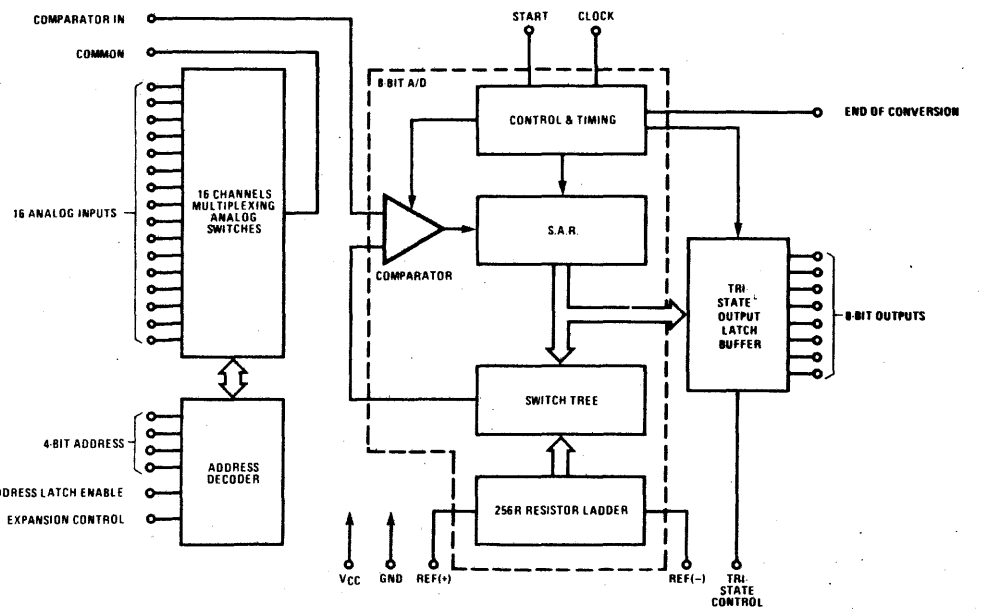
The device eliminates the need for external zero and full-scale adjustments and features an absolute accuracy $\leq$ 1 LSB including quantitizing error. Easy interfacing to microprocessors is provided by the latched and decoded address inputs and latched TTL TRI-STATE® outputs.

The design of the ADC0816, ADC0817 has been optimized by incorporating the most desirable aspects of several A/D conversion techniques. The ADC0816, ADC0817 offers high speed, high accuracy, minimal temperature dependence, excellent long-term accuracy and repeatability, and consumes minimal power. These features make this device ideally suited to applications such as process control, industrial control, and machine control.

Features

- Total unadjusted error $<\pm$1/2 LSB
- Linearity error $<\pm$1/2 LSB
- No missing codes
- Guaranteed monotonicity
- No offset adjust required
- No scale adjust required
- Conversion time of 100 μs
- Easy microprocessor interface
- Latched TRI-STATE output
- Latched address input
- Ratiometric conversion
- Single 5V supply
- Low power consumption—15 mW

Block Diagram



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Absolute Maximum Ratings (Notes 1 and 2)

Voltage at Any Pin Except Control Inputs	−0.3V to V_{CC} + 0.3V
Voltage at Control Inputs (Start, TRI-STATE, Clock, ALE, ADD A, ADD B, ADD C, ADD D, Expansion Control)	−0.3V to + 15V
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Package Dissipation (at 25°C)	500 mW
Operating V_{CC} Range	4.5V to 6V
Absolute Maximum V_{CC}	6.5V
Lead Temperature (Soldering, 10 seconds)	300°C

DC Electrical Characteristics

$4.75V \leq V_{CC} \leq 5.25V$, $-40°C \leq T_A \leq +85°C$ unless otherwise noted, (Note 2)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
$V_{IN(1)}$	Logical "1" Input Voltage	V_{CC} = 5V	V_{CC}−1.5			V
$V_{IN(0)}$	Logical "0" Input Voltage	V_{CC} = 5V			1.5	V
$V_{OUT(1)}$	Logical "1" Output Voltage	I_O = −360 μA	V_{CC}−0.4			V
$V_{OUT(0)}$	Logical "0" Output Voltage	I_O = 1.6 mA			0.45	V
$V_{OUT(0)}$	Logical "0" Output Voltage EOC	I_O = 1.2 mA			0.45	V
$I_{IN(1)}$	Logical "1" Input Current (The Control Inputs)	V_{IN} = 15V			1.0	μA
$I_{IN(0)}$	Logical "0" Input Current (The Control Inputs)	V_{IN} = 0	−1.0			μA
I_{CC}	Supply Current	Clock Frequency = 500 kHz		300	1000	μA
I_{OUT}	TRI-STATE Output Current	V_O = 5V			3	μA
		V_O = 0	−3			μA

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Electrical Characteristics" provides conditions for actual device operation.

Note 2: All voltages measured with respect to GND unless otherwise specified.

Note 3: Non-linearity error is the maximum deviation from a straight line through the end points of the A/D transfer characteristic, *(Figure 2)*.

Note 4: Zero error is the difference between the output of an ideal and the actual A/D for zero input voltage, *(Figure 2)*.

Note 5: Full-scale error is the difference between the output of an ideal and the actual A/D for full-scale input voltage, *(Figure 2)*.

Note 6: Total unadjusted error is the maximum sum of non-linearity, zero and full-scale errors, *(Figure 3)*.

Note 7: Quantization error is the ±1/2 LSB uncertainty caused by the converter's finite resolution, *(Figure 3)*.

Note 8: Absolute Accuracy describes the difference between the actual input voltage and the full-scale weighted equivalent of the binary output code; included are quantizing and all other errors. Although rarely provided on data sheets, it is the best indication of a converter's true performance, *(Figure 3)*.

Note 9: Supply rejection relates to the ability of an ADC to maintain accuracy as the supply voltage varies. The supply and $V_{REF(+)}$ are varied together and the change in accuracy is measured with respect to full-scale.

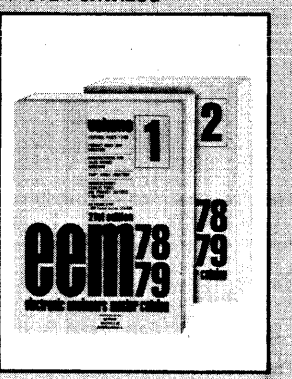
Note 10: Comparator input current is a bias current into or out of the chopper stabilized comparator. The bias current varies directly with clock frequency and has little temperature dependence, *(Figure 5)*.

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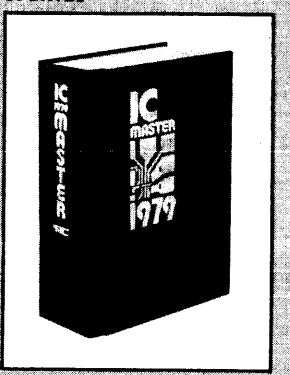
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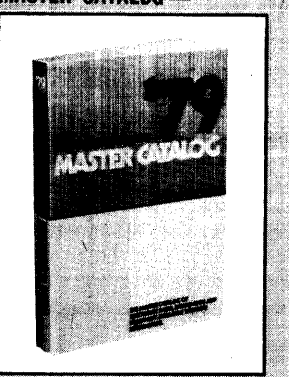
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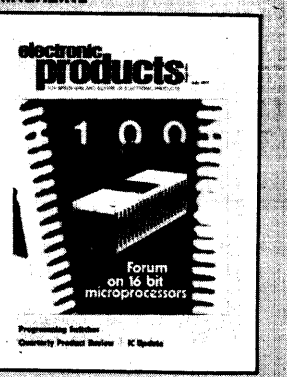
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SL445A
POWER CONTROL
ZERO VOLTAGE SWITCH

The SL445 is a triac controller providing a *complete* solution for temperature controlled electric panel heaters, cookers, film processing baths etc.

Switching occurs at the zero voltage point in order to minimise radio frequency interference.

The device is suitable for on-line operation and requires minimal external components.

SPECIAL FEATURES

1. Choice of proportional or on/off temperature control.
2. Controlled switching rate in order to limit 'lamp flicker'. A pulse integration technique eliminates the problems associated with electrolytic timing capacitors.
3. Very accurate temperature control is possible since switching jitter has been eliminated *without introducing hysteresis* to the servo amplifier.
4. Symmetrical burst control i.e. no half-wave firing.
5. LED drive circuit which responds directly to the temperature setting.
6. Over-temperature protection circuit using a 'fail-safe' PTC thermistor and having the option of automatic or manual reset.
7. LED/Buzzer drive circuit controlled by 6 above.
8. High immunity against spurious triac trigger pulses under noisy mains environment.
9. Spurious triac trigger pulses inhibited at 'switch-on'.
10. Potentiometer expansion circuit to improve resolution/reduce component count.

ABSOLUTE MAXIMUM RATINGS

Pin	Max.	Units
1. Applied voltage	V_4	V
3. Peak Repetitive Current in ($\pm I_{2M}$)	80	mA
3. Non-repetitive peak current (tp $<$ 250μS) $\pm I_{2SM}$	200	mA
5. Applied voltage	10	V
6. Applied Voltage	10	V
6. Output Current	10	mA
7. Applied Voltage	6	V
7. Output Current	10	mA
8. Applied Voltage	10	V
9. Applied Voltage	V_{11}	V
10. Applied Voltage	V_{11}	V
11. Output Current	10	mA
16 Applied Voltage	V_4	V

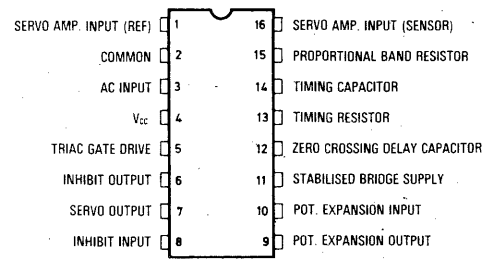


Fig. 1 Pin connections (top)

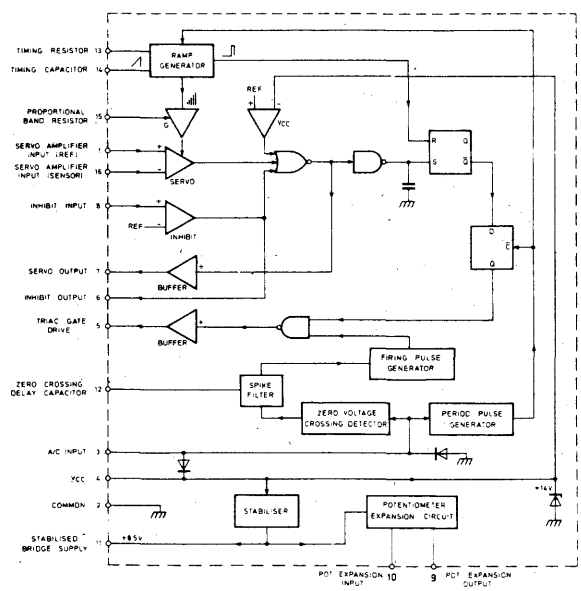


Fig. 2 SL445 block diagram

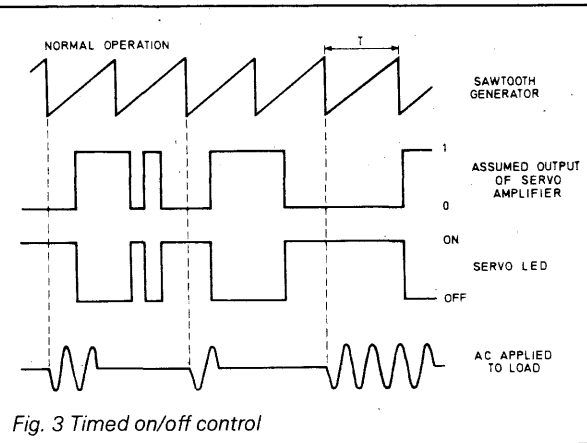


Fig. 3 Timed on/off control

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SL445A
POWER CONTROL CIRCUIT

ELECTRICAL CHARACTERISTICS

Operating temperature range −10°C to +85°C
Storage temperature range −55°C to +125°C
Test conditions (unless otherwise stated): Tamb = 25°C
All potentials measured with respect to common (pin 2)

	Value			Units	Conditions
	Min.	Typ.	Max.		
Shunt regulating voltage Pin 4		14.7		V	I_4 = 20mA average
Max. regulating voltage on Pin 4 at 85°C			16	V	I_4 = 20mA average
Supply sensing amplifier—minimum working voltage Pin 4		12.2		V	
*Quiescent current drain			8.2	mA	Less I_{11}, I7, I6, I_{5AV}
Stabilised bridge supply voltage Pin 11 @ 2mA	8.0	8.5	9.0	V	
Temperature coefficient Pin 11	−1		+1	mV/°C	
Triac gate drive Pin 5					See Fig. 6 for pulse timing
Open circuit OFF voltage			0.1	V	
Open circuit ON voltage		8.5		V	
Current drive into short circuit			200	mA	
Current drive into 2V drain	80	100		mA	
Current drive into 4V drain	50	70		mA	
Internal drain resistance Pin 5		800		Ω	
Servo amp. Pins 1 & 16					
Input bias current			1	μA	
Input working voltage range	0		10	V	
Servo amp. output voltage drive Pin 7	6.0	6.5	7.0	V	
Internal drain resistance Pin 7	10	25	60	kΩ	
Inhibit amp. input Pin 8					
Trip voltage	0.9	0.95	1.0	V	$V_{11} \div 9$
Input bias current			1	μA	
Input working voltage range	0		10	V	
Inhibit amp. output voltage drive Pin 6	5.8	6.4	6.8	V	
Internal drain resistance Pin 6	8	12	16	kΩ	
Inhibit voltage Pin 6		3.5		V	
Potentiometer expansion circuit input bias current Pin 10			10	μA	See Fig. 7
Potentiometer expansion circuit output resistance Pin 9	4	6	8	kΩ	See Fig. 7
Proportional control band (R_{15} = 220k)	60	100	140	mV	R_{15} = 220kΩ
Ramp generator period T	40	44	48	s	R_{13} = 100k, R_{14}= 1.0μF, 220V AC

* The supply current is 0.45 × (RMS current fed into Pin 3).

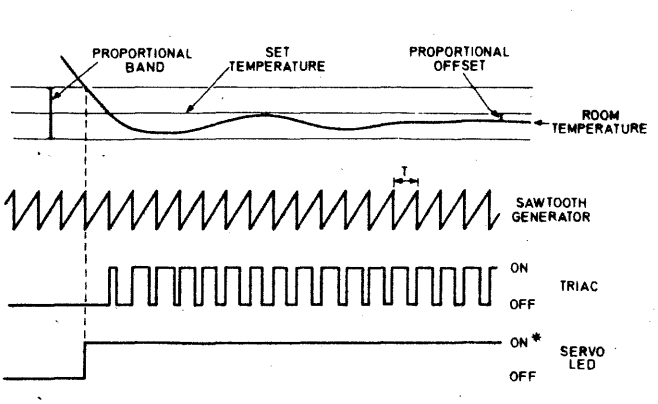


Fig. 4 Timed proportional control normal operation

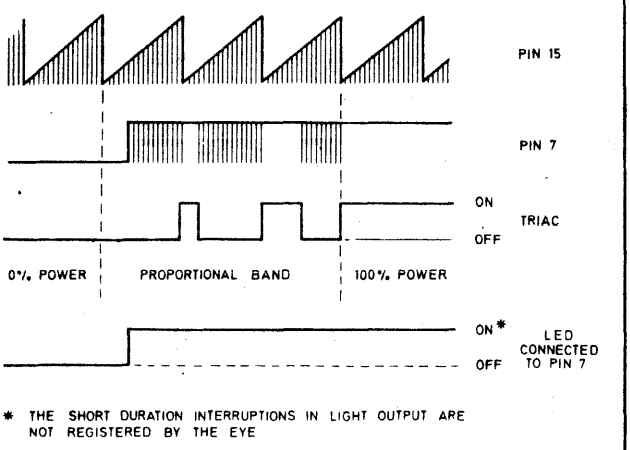


Fig. 5 Timed proportional control (expanded)

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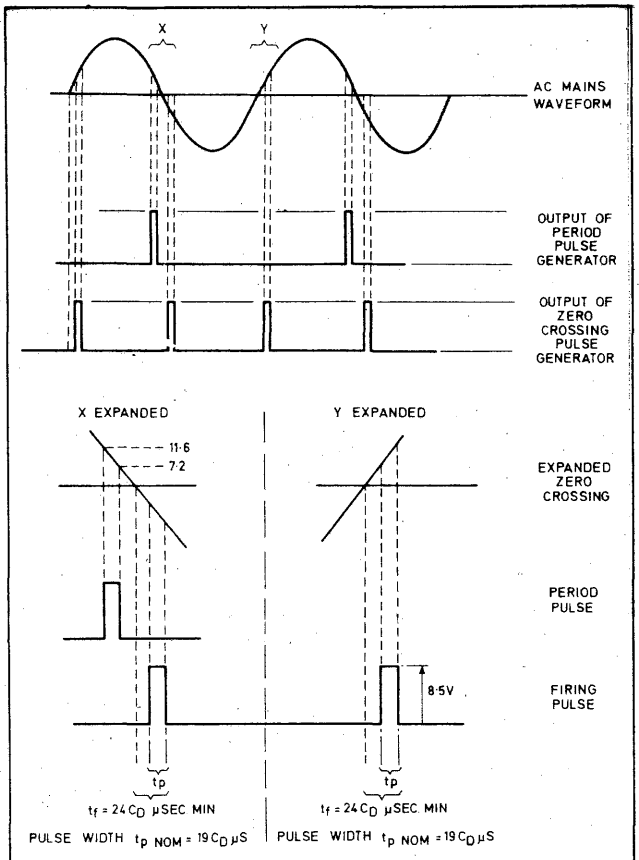


Fig. 6 Pulse timing

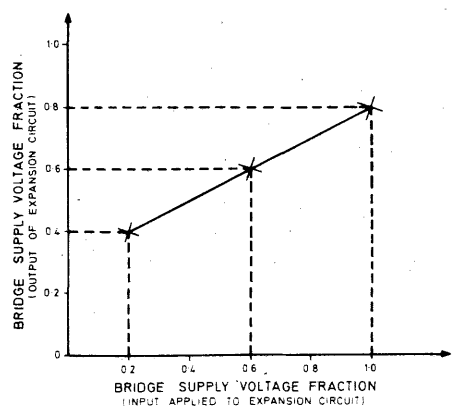
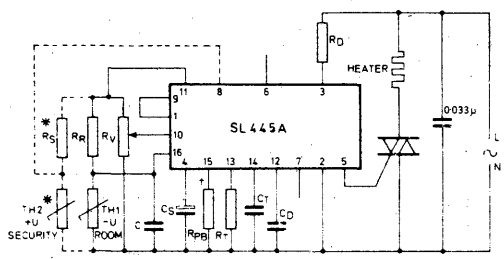


Fig. 7 Potentiometer expansion characteristic



* These two components may be omitted if the over-temperature trip facility is not required. Pin 8 should then be taken to common ie. Pin 2.

† This component may be omitted if proportional control is not required. The circuit will then provide times on/off control. Pin 15 should be taken to Pin 11.

C May be required to integrate input noise e.g. 47nF.

Fig. 8 Electric panel heater control with room thermostat and optional security thermostat

LED INDICATOR

Provides the following facilities

(a) In the case of timed proportional control, the LED will be lit continuously if any energy is supplied during the timing cycle, i.e. the LED will only be extinguished if the room temperature is being maintained without panel assistance.

(b) In the case of timed on/off control, the LED will be lit for the period that energy is being consumed, i.e. the LED will flash on and off as the room temperature varies about the set point.

(c) Room temperature may be ascertained by observing LED action whilst adjusting the temperature setting i.e. the LED is a substitute for the sound produced by electromechanical thermostats.

The LED facility may be added as shown in Fig. 9.

It is desirable to minimise LED drive current since this has a significant effect on the power rating of the mains dropping resistor R_D. If the LED is for facility 'a' or 'b', a high intensity, wide viewing angle LED will be required and a current of 5mA nominal is suggested i.e. $R_L = 1k\Omega$ ($V_{LED} = 1.5V$).

If the LED is only intended for facility 'c', a small, narrow viewing angle LED may be used and a current of 0.5mA nominal is sufficient i.e. $R_L = 10k\Omega$ ($V_{LED} = 1.5V$).

A small amount of positive feedback may be applied to the servo amplifier by inclusion of resistor Rf (Fig. 9b). This can ensure flicker free operation of the LED by increasing the immunity of the amplifier to noise etc. on its input connections. However, the level of feedback should be minimised since temperature regulation will necessarily be impaired. A typical value for Rf would be 4.7 MΩ and this results in a hysteresis of 13mV (0.13°C) if the bridge components are as given below.

SECURITY (OVERTEMPERATURE TRIP) INDICATION

Indication may be provided by LED or buzzer as shown in Fig. 10.

SECURITY (OVERTEMPERATURE TRIP) RESET

Hysteresis may be externally applied to the Inhibit Amplifier such that re-entry of the control circuit takes place automatically i.e.

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SL445A
POWER CONTROL CIRCUIT

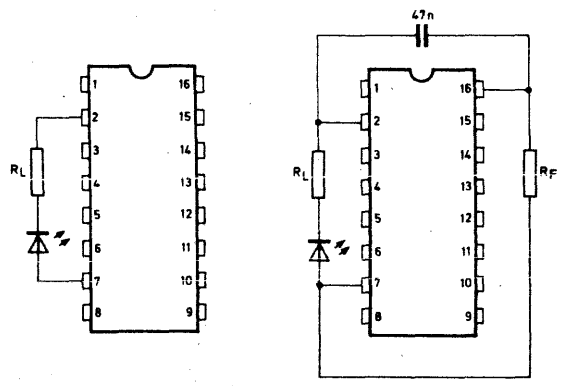


Fig. 9a Simple indicator

Fig. 9b Flicker-free indicator

Fig. 9 LED indicator connections

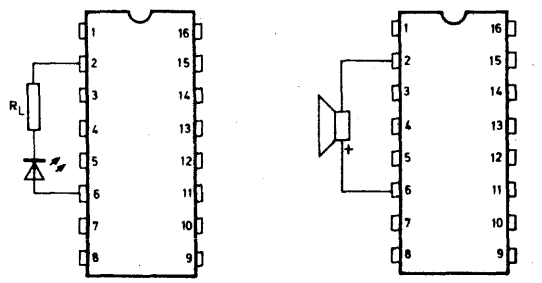


Fig. 10a LED (I_{LED} = 5mA, V_L = 1.5V, R_L = 1kΩ; I_{LED} = 0.5mA, V_L = 1.5V, R_L = 10kΩ)

Fig. 10b Buzzer (6V, 6mA)

Fig. 10 Security indicator circuits

when the panel temperature falls to a certain level below the trip point. Alternatively, it may be arranged that the trip circuit—when activated—can only be reset by manual intervention e.g. momentarily interrupting the mains supply. It is desirable to introduce some hysteresis to the system when using a buzzer, in order to ensure positive on/off operation. When the manual reset mode of operation is adopted, an additional capacitor is required to eliminate the possibility of a spurious spike tripping the circuit.

COMPONENT VALUES

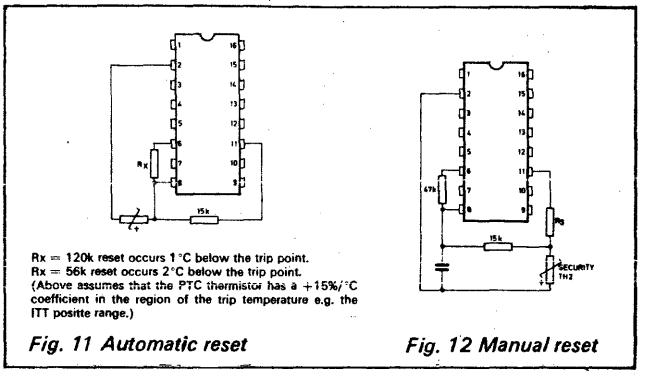
Room Temperature Sensing (R_R, TH1, R_V)

Rv = 22k or 25k linear control potentiometer.
R_R = 18k ±2%
THI = NTC thermistor, e.g. ITT type KQ223Y,
R_{25} = 22k ±10%, B = 4300 ±5%

Using these components, substantially linear temperature control is obtained over the range 5°C to 35°C. This range is covered by 69% of the potentiometer track when the I.C's expansion circuit is used as shown in figure 1. If the LED facility is used, calibration can be both accurate and rapid.

Controlled Switching rate (R_T, C_T)

The period of the ramp generator is dictated by the requirements of Cenelec EN50.006 concerning lamp flicker. The load can only be switched into circuit at the start of a ramp cycle i.e. if power is interrupted to the load at any point in the cycle, subsequent demands for power can only be met at the start of the next cycle.



Rx = 120k reset occurs 1°C below the trip point.
Rx = 56k reset occurs 2°C below the trip point.
(Above assumes that the PTC thermistor has a +15%/°C coefficient in the region of the trip temperature e.g. the ITT positte range.)

Fig. 11 Automatic reset

Fig. 12 Manual reset

The pulse integration technique employed in the ramp generator accounts for the mains voltage term in the formula:

Period of ramp = 0.2 x V_{RMS} x C_T seconds ± 10%

This assumes R_T = 100k. C_T is in μF, and V_{RMS} is in volts, e.g. a 1.0μF capacitor will provide a ramp period of 44 sec if the circuit is used with a 220V AC supply.

The capacitor should be of polyester or similar construction. Because of leakage and other considerations, electrolytic capacitors are not suitable.

Proportional Control (R_{PB})

Resistance R_{PB} controls the proportion of the ramp waveform which is applied internally to the offset facility of the servo amplifier. R_{PB} therefore, controls the width of the proportional control band.

If R_{PB} = 220k, the peak offset will be 100mV which is equivalent to a proportional control band of 1°C if the above bridge component values are used.

If R_{PB} = 100k, PB = 2.2°C
= 390k, PB = 0.55°C etc.

Overtemperature Control (Security) (Rs, TH2)

Rs = 15k

	Trip Temperature Min.	Max.
TH2 = ITT POSITTE PTC thermistor type YC080TB	82°C	90°C
=ITT POSITTE PTC thermistor type YC090TB	92°C	100°C
=ITT POSITTE PTC thermistor type YC100TB	102°C	110°C

Thermistors of alternative manufacture may be used although the value of R_S may then differ. Tripping takes place if the resistance of TH2 is greater than $R_S \div 8$.

The value of R_S should be kept high to minimise power loss in R_D.

Triac and C_D

Generally, the maximum gate firing voltage (V_{GT}) of a triac is 2.0V and the output stage of the IC has been designed to deliver a minimum of 80mA into such a load. The nominal current is 100mA and the triac is supplied with positive gate current. A wide range of suitable, low price triacs are available from several manufacturers. In order to minimise RFI, a triac should be chosen which has a low latching current IL. The triac cannot latch until the supply voltage V_L O (V_T + I_L x R_L) where

V_T = on-stage voltage of the device
R_L = resistance of the triac load

Therefore the triac requires a gate current

$$\frac{V_L \times 10^6}{V_{RMS} \times \sqrt{2} \times 2\pi f} \mu S$$

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after the zero crossing point in the supply cycle where f = the supply frequency.

e.g. for a 380V ±10%, 50HZ supply, 1kW load

MAX. V_T of triac = 1.2V (@ I_L)

MAX. I_L of triac = 50mA

we get $R_L = \frac{380^2}{10^3} = 144.4\Omega$

R_L MAX = 144.4 + 5% =152Ω

$V_L = I_L \times R_L + V_T = 0.05 \times 152 + 1.2 = 8.8V$ Max

The trailing edge of the firing pulse (Tf) must occur not sooner than

$\frac{V_L \times 10^6}{V_{RMS} \times \sqrt{2} \times 2nf}$ μs after the zero crossing point.

$Tf\ MIN. = \frac{8.8 \times 10^6}{0.9 \times 380 \times \sqrt{2} \times 2 \times \pi \times 50}$

$= 57.91\ \mu s = 24 \times C_D$

C_D MIN. = 57.91 = 2.41nf

C_D = 2.7 nF ±10%

The same triac could of course be used to control a higher power load. The load resistance and hence required V_L would fall, but for convenience the value of C_D need not be altered. Similarily, if the above calculations are repeated for a 220V supply, it will be established that C_D must exceed 1.77 nF and a value of 2.7 nF is again suitable. It may be convenient to use the same triac and value of C_D for 220, 240 and 380V applications. However, C_D should be kept as low as possible if power dissipation in the dropper resistor is to be minimised.

LINE DROPPING RESISTOR (R_D)

Table I indicates the value of resistor R_D as a function of mains supply voltage, facilities provided etc. It will be apparent that it is desirable when dealing with a 380V supply to reduce power dissipation in the dropper resistor by introducing a series diode.

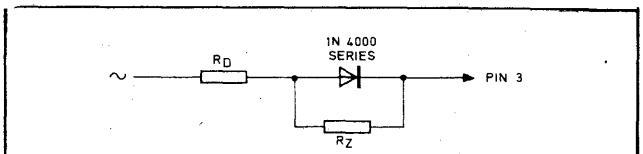


Fig. 13 Mains supply input circuit

	110V	220/240V	380V
R_Z ±10%	39k	82k	82k
Power dissipation in R_Z (max)	0.3W	0.4W	1W
Minimum value C_D	2.4 nf	1.9 nF	1.3 nF

Table 2 Max. value of R_Z for various supply voltages

The diode bypass resistor R_Z (see Table 2) is necessary to provide proper operation of the zero voltage crossing circuit. The values for R_D given in the table may be reduced for rationalization purposes if required (e.g. common value for 220/240V supplies) or where additional external circuitry is fed by the 8.3V or 14V supplies. This may necessitate an appropriate increase in the value of the smoothing capacitor Cs. Furthermore, consideration should be given to the possible increase in chip power dissipation particularly if the external load is dynamic.

SMOOTHING CAPACITOR (Cs)

A 220μF 16V Capacitor should be used except when dealing with the higher current appications i.e. 5mA LED, 6mA buzzer etc. Cs should then be increased to 330μF. The ripple voltage should be kept below 1V peak–to–peak.

Facilities used					Nominal R_D value (±5%)	Maximum R_D power dissipation	Maximum R_D power dissipation (with diode)	Nominal power supply voltage ±10%	Nominal C_D
Room temperature control	Serve LED 0.5mA	Over temperature trip (security)	Serve LED 5mA	Security buzzer (6V. 6mA)					
●					3.3K	4.7W	2.3W	110V	4.7nF
●					7.5k	8.2W	4.1W	220V	
●					8.2k	8.9W	4.4W	240V	2.7nF
●					12k	15.3W	7.6W	380V	
●	●				3.0k	5.1W	2.5W	110V	4.7nF
●	●				6.8k	9.1W	4.5W	220V	
●	●				7.5k	9.8W	4.9W	240V	2.7nF
●	●				12k	15.3W	7.6W	380V	
●		●			3.0k	5.1W	2.5W	110V	4.7nF
●		●			6.8k	9.1W	4.5W	220V	
●		●			7.5k	9.8W	4.9W	240V	2.7nF
●		●			12k	15.3W	7.6W	380V	
●	●	●			3.0k	5.1W	2.5W	110V	4.7nF
●	●	●			6.8k	9.1W	4.5W	220V	
●	●	●			7.5k	9.8W	4.9W	240V	2.7nF
●	●	●			12k	15.3W	7.6W	380V	
●			●		2.2k	7.0W	3.5W	110V	4.7nF
●			●		5.1k	12.1W	6.0W	220V	
●			●		6.2k	11.8W	5.9W	240V	2.7nF
●			●		9.1k	20.2W	10.1W	380V	
●		●	●	●	2.2k	7.0W	3.5W	110V	4.7nF
●		●	●	●	4.7k	13.1W	6.5W	220V	
●		●	●	●	5.1k	14.4W	7.2W	240V	2.7nF
●		●	●	●	8.2k	22.4W	11.2W	380V	

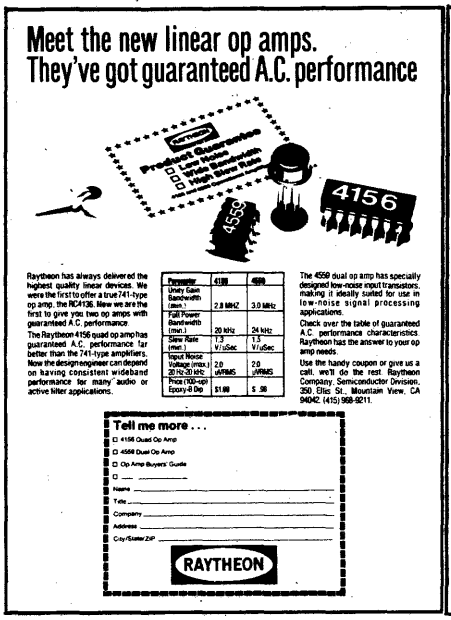
Table 1 Value of R_D (mains dropping resistor)

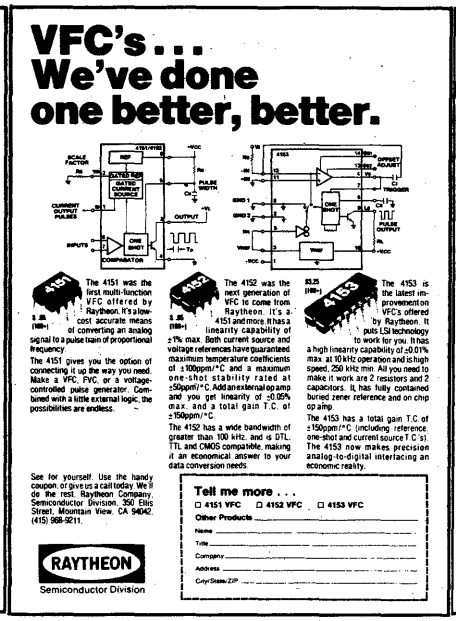
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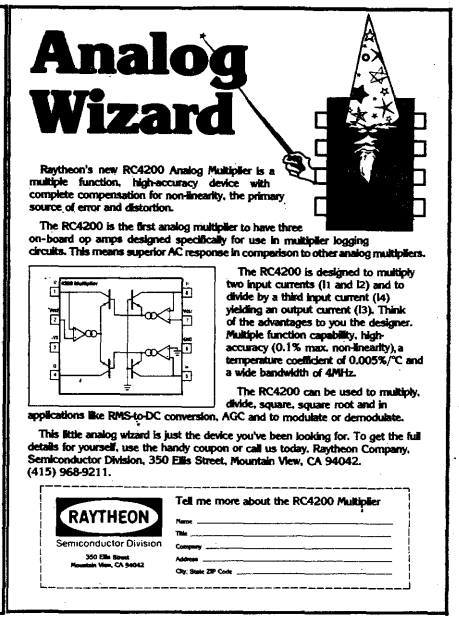
ABBREVIATIONS OF COMPANY NAMES

AD	Analog Devices
AMD	Advanced Micro Devices
AMI	American Microsystems, Inc.
Amperex	Amperex Electronics Corp.
Analogic	Analogic Corp.
Beckman	Beckman Instruments, Helipot Division
BEI	BEI Electronics
Burr-Brown	Burr-Brown Research
Cermetek	Cermetek
Cherry	Cherry Semiconductor
CMA	Consumer Microcircuits of America
Cybernetic	Cybernetic Micro Systems
Data General	Data General
Datel	Datel Systems
DDC	Data Devices Corp.
Delco	Delco Electronics
Dionics	Dionics Inc.
EA	Electronic Arrays
EMM/Semi	EMM Semi, Div. of Electronic Memories & Magnetics
Essex	Essex International
Exar	Exar Integrated Systems
Fairchild	Fairchild
Ferranti	Ferranti Electric
Fujitsu	Fujitsu
GI	General Instrument
Harris	Harris Semiconductor
Hitachi	Hitachi America Ltd.
Holt	Holt Inc.
Hughes	Hughes Aircraft Solid State Products
Hybrid Sys	Hybrid Systems
HyComp	HyComp
IMI	International Microcircuits, Inc.
Intech/FMI	Intech/Function Modules Inc.
Intel	Intel
Interdesign	Interdesign
Intersil	Intersil
IPI	Integrated Photomatrix, Inc.
Lambda	Lambda Electronics
LSI	LSI Computer Systems
Maruman	Maruman Integrated Circuits
Master Logic	Master Logic
Matrox	Matrox Electronics Systems
Micro Net	Micro Networks
Micropac	Micropac Industries
Micro Power	Micro Power Systems
Micro Tech	Microcircuits Technology
Mitel	Mitel Semiconductor
Mitsubishi	Mitsubishi Electric Co.
MMI	Monolithic Memories, Inc.
Monosil	Monosil
MOS	MOS Technology
Mostek	Mostek
Motorola	Motorola Semiconductor
National	National Semiconductor
NCR	NCR Corp., Microelectronics Division
NEC America	NEC America
NEC Micro	NEC Microcomputers
Nitron	Nitron
Nortec	Nortec Electronics
Novonics	Novonics
NPC	Nucleonic Products Co.
OEI	Optical Electronics, Inc.
OKI	OKI Semiconductor
Panasonic	Panasonic, Matsushita Electric Corp.
Photo Therm	Photo Therm
Plessey	Plessey Semiconductors
PMI	Precision Monolithics, Inc.
Raytheon	Raytheon Semiconductor
RCA	RCA Solid State Division
Reticon	Reticon
RIFA	RIFA
Rockwell	Rockwell Microelectronic Devices
RTC	Real Time Corp.
Sanken	Sanken Electric
Sanyo	Sanyo Electric
SGS	SGS-Ates Semiconductor
Siemens	Siemens
Signetics	Signetics (Philips)
Silicon G	Silicon General
Siliconix	Siliconix
Silicon Sys.	Silicon Systems, Inc.
Silitronics	Silitronics
SMC	Standard Microsystems
Solitron	Solitron Devices
Sprague	Sprague Electric Company
Supertex	Supertex, Inc.
SSM	Solid State Microtechnology for Music
SSS	Solid State Scientific
Synertek	Synertek
Telaris	Telaris
Teledyne C	Teledyne Crystalonics
Teledyne P	Teledyne Philbrick
Teledyne S	Teledyne Semiconductor
Telefunken	AEG-Telefunken
TI	Texas Instruments
TMX	TMX
Toshiba	Toshiba
Trans-Data	Trans-Data
TRW	TRW
Unitrode	Unitrode
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Zilog	Zilog

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DESCRIPTION

The RC4151 and RM4151 provide a simple low-cost method of analog-to-digital conversion. They have all the inherent advantages of the voltage-to-frequency conversion technique. The output of the 4151 is a series of pulses of constant duration. The frequency of the pulses is proportional to the applied input voltage. These converters are designed for use in a wide range of data conversion and remote sensing applications.

FEATURES

- Single supply operation (+8V to +22V)
- Pulse output compatible with all logic forms
- Programmable scale factor (K)
- Linearity ±0.05% typical - precision mode
- Temperature stability ±100% ppm/°C typical
- High noise rejection
- Inherent monotonicity
- Easily transmittable output
- Simple full scale trim
- Single-ended input, referenced to ground
- Also provides frequency-to-voltage conversion

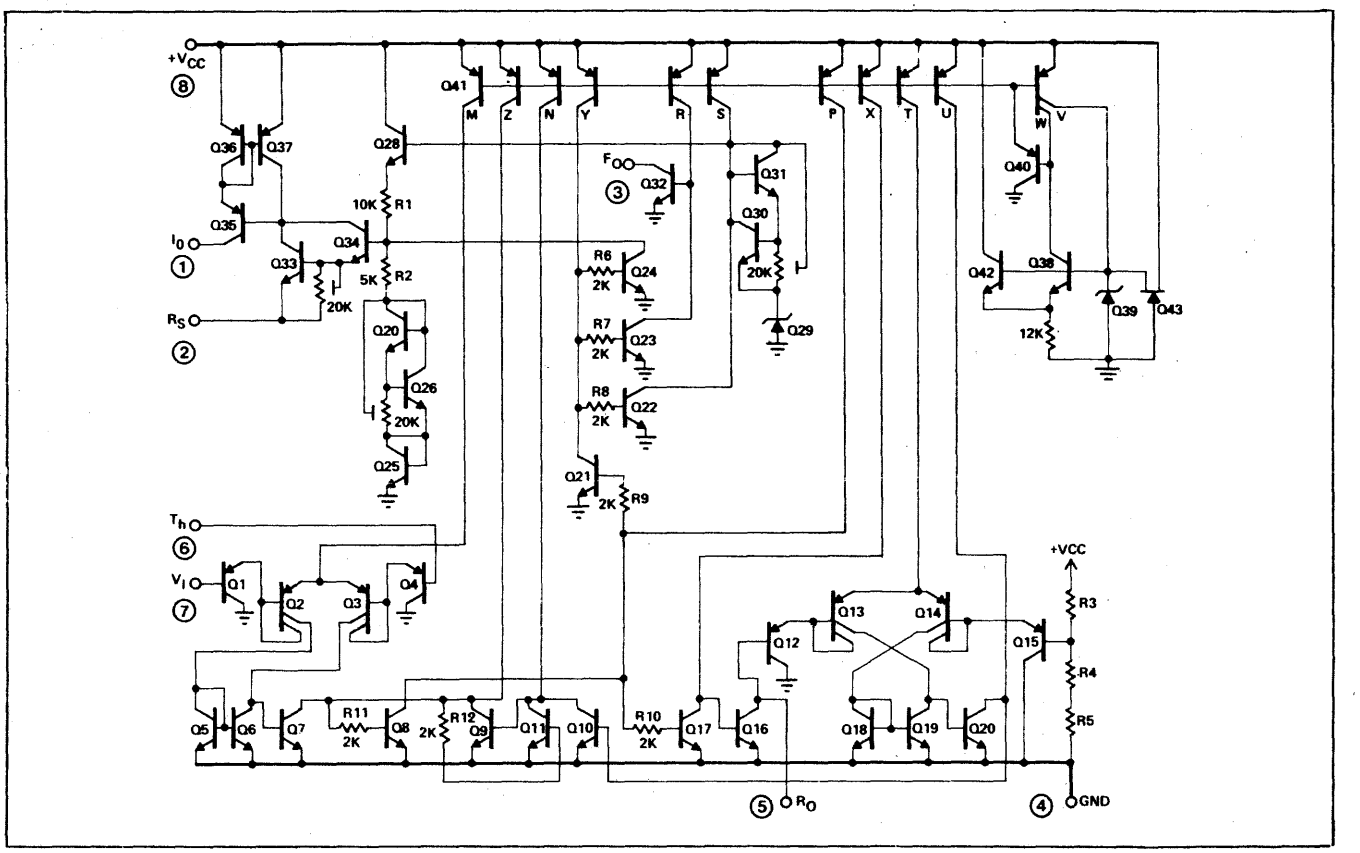
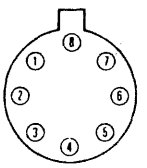


Figure 1. 4151 Schematic Diagram

TE (TO-99) METAL CAN

(Top View)

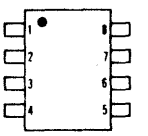


Order Part Nos.: RC4151T, RM4151T

NOTE: PIN 4 CONNECTED TO CASE

NB MINIATURE DUAL-IN-LINE

(Top View)



Order Part Nos.: RC4151NB, RV4151NB

PIN	FUNCTION
1	CURRENT SOURCE
2	SCALE FACTOR
3	LOGIC OUTPUT
4	GROUND
5	ONE-SHOT R, C
6	THRESHOLD
7	INPUT VOLTAGE
8	V_{CC}

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ABSOLUTE MAXIMUM RATINGS

Supply voltages	+8.0 to +22V
Output sink current	20mA
Internal power dissipation	500mW
Input voltage	-0.2V to +V_{CC}
Output short circuit to ground	Continuous

Temperature Range	Storage	Operating
RM4151:	-65°C to +150°C	-55°C to +125°C
RV4151:	-55°C to +125°C	-40°C to + 85°C
RC4151:	-55°C to +125°C	0°C to + 70°C

ELECTRICAL CHARACTERISTICS V_{CC} = +15V, T_A = +25°C, unless otherwise specified

PARAMETER	CONDITIONS	UNITS	MIN	TYP	MAX
SUPPLY CURRENT	8V < V_{cc} < 15V	mA	2.0	3.5	6.0
	15V < V_{cc} < 22V	mA	2.0	4.5	7.5
CONVERSION ACCURACY					
Scale Factor	Circuit Figure 3, V_I = 10V R_S = 14.0K	kHz/V	0.90	1.0	1.10
Drift with Temperature	Circuit Figure 3, V_I = 10V	ppM/°C	–	± 100	–
Drift with V_{cc}	Circuit Figure 3, V_I = 1.0V 8V < V_{cc} < 18V	%/V	–	0.2	1.0
INPUT COMPARATOR					
Offset Voltage		mV	–	5.0	10.0
Offset Current		nA	–	± 50.0	±100.0
Input Bias Current		nA	–	-100.0	-300
Common Mode Range (Note 1)		V	0	0 to V_{cc}-2	V_{cc} -3.0
ONE-SHOT					
Threshold Voltage, Pin 5		xV_{cc}	0.63	0.667	0.70
Input Bias Current, Pin 5		nA	–	-100.0	-500
Reset V_{SAT}	Pin 5, I = 2.2 mA	V	–	0.15	0.50
CURRENT SOURCE					
Output Current (R_S = 14.0kΩ)	Pin 1, Figure 3, V = 0	μA	–	138.7	–
Change with Voltage	Pin 1, V = 0V to V = 10V	μA	–	1.0	2.5
Off Leakage	Pin 1, V = 0V	nA	–	1.0	50.0
REFERENCE VOLTAGE	Pin 2, Figure 3	V	1.70	1.9	2.08
LOGIC OUTPUT					
V_{SAT}	Pin 3, I = 3.0 mA	V	–	0.15	0.50
V_{SAT}	I = 2.0 mA	V	–	0.10	0.35
Off Leakage		μA	–	0.1	1.0

Note 1: Input Common Mode Range includes ground.

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DESCRIPTION

The Raytheon 4152 consists of a comparator, a one-shot, a precise gated current-source output, an internal voltage reference, and an open-collector output . . . all on a single monolithic IC chip. These elements can be combined via external pin connections to perform a wide variety of circuit functions.

The versatility of this unique IC makes it easy to tailor the circuit operation to your needs. Pulse width, scale factor, and output drive are set by external resistors as shown in Figure 1. Combine the versatile 4152 with an op amp or two, some digital circuits, and the range of cost-effective applications becomes even greater.

The Raytheon 4152 provides a versatile, low-cost means of accurately converting an analog signal to a pulse train of proportional frequency, and vice versa. It can be imaginatively applied to a broad range of signal conditioning applications once the various functional blocks within the IC are understood.

The 4152 is directly interchangeable with the 4151, thereby allowing an upgrading of system accuracy at minimal cost.

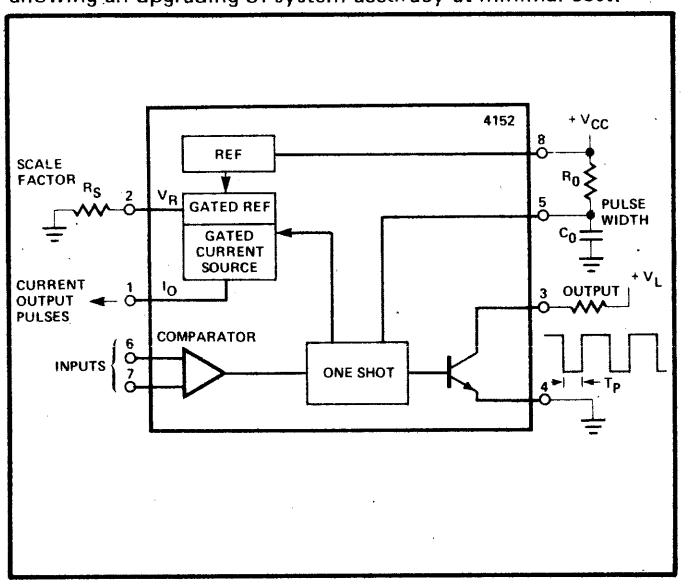


Figure 1. Functional Diagram of Raytheon 4152.

FEATURES

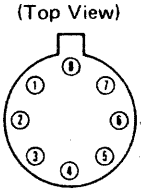
- Single supply operation (+7 V to +18 V)
- Pulse output compatible with all logic forms (DTL/TTL/CMOS)
- Programmable scale factor (K)
- High linearity ±0.05% max
- Temperature stability ±150 ppm/°C max
- Direct replacement for RM/RC4151
- High noise rejection
- Inherent monotonicity
- Easily transmittable output
- Simple full scale trim
- Single-ended input, referenced to ground
- V/F or F/V conversion
- Voltage or current input
- Wide dynamic range

APPLICATIONS

- Precision voltage-to-frequency-converters
- Pulse-width modulators
- Programmable pulse generators
- Frequency-to-voltage converters
- Integrating analog-to-digital converter
- Long-term analog integrator
- Signal conversion –
  - Current-to-frequency
  - Temperature-to-frequency
  - Pressure-to-frequency
  - Capacitance-to-frequency
  - Frequency-to-current
- Signal isolation
  - VFC → opto-isolation → FVC
  - ADC with opto-isolation
- Signal encoding
  - FSK modulation/demodulation
  - Pulse-width modulation
- Frequency scaling
- DC motor speed control

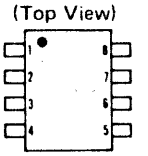
CONNECTION INFORMATION

TE (TO-99) Metal Can
(Top View)



Order Part Nos.: RC4152T, RM4152T
NOTE: PIN 4 CONNECTED TO CASE

DE and NB Miniature Dual In-line Packages
(Top View)



Order Part Nos.: RC4152NB, RV4152NB
RM4152DE, RV4152DE, RC4152DE

PIN	FUNCTION
1	CURRENT SOURCE
2	SCALE FACTOR
3	LOGIC OUTPUT
4	GROUND
5	ONE-SHOT R, C
6	THRESHOLD
7	INPUT VOLTAGE
8	V_{CC}

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ABSOLUTE MAXIMUM RATINGS

Supply Voltages . . . . . +22V
Output Sink Current 20mA
Internal Power Dissipation 500mW
Input Voltage . . . . . −0.2V to +V_{CC}
Output Short Circuit to Ground . . . . . Continuous

Storage Temperature Range
RM4152 . . . . . −65°C to +150°C
RV4152 . . . . . −55°C to +125°C
RC4152 . . . . . −55°C to +125°C
Operating Temperature Range
RM4152 . . . . . −55°C to +125°C
RV4152 . . . . . −40°C to +85°C
RC4152 . . . . . 0°C to +70°C

ELECTRICAL SPECIFICATIONS

Typical performance at V_{CC} = +15 V and T_A = +25°C unless otherwise noted.

CIRCUIT CHARACTERISTICS	MIN	TYP	MAX	UNITS
Input Comparator				
Input Offset Voltage @ 25°C		±2	±10	mV
vs. Temperature		±20		µV/°C
Input Offset Current		±30	±100	nA
Bias Current (Either Input)		-50	-300	nA
Input Voltage Range (Either Input)		0 to V_{CC} -3.0 Volts		V
Comparator Gain		10,000		—
One-Shot Pulse Circuit				
Pulse Width (See Fig. 1)		1.1 R_o C_o ± 3%		sec
Threshold Voltage (Pin 5)	0.65 V_{CC}	0.67 V_{CC}	0.69 V_{CC}	V
Input Bias Current (Pin 5)		-100	-500	nA
V_{sat} at Pin 5, I = 2.2 mA		0.10	0.5	V
Pulse Width Stability (T_p = 75 µs)				
vs. Temperature		±30	±50	ppm/°C
vs. Supply		±100		ppm/V
Gated Current Source				
Output of Gated Current Source		V_R/R_S ± 1%		—
vs. Temperature(1)		±50	±100	ppm/°C
vs. Supply		0.10		%/V
Compliance (Change with Voltage)		0.10	0.25	µA/V
Leakage in OFF State		10	50	nA
Rise Time		100		nsec
Fall Time		100		nsec
Reference Voltage				
Voltage V_R (Pin 2)	2.0	2.25	2.5	V
Temperature Coefficient		±50	±100	ppm/°C
Logic Output (Pin 3)				
V_{sat} @ I = 3 mA		0.1	0.5	V
@ I = 10 mA		0.8		V
Power Supply				
Voltage, Operating Range	+7	+15	+18	V
Quiescent Current Drain		2.5	6	mA

(1) Temperature coefficient of output current mirror (pin 1 output) exclusive of reference voltage drift.

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Description

The 4153 is a high speed, precision voltage-to-frequency converter utilizing Linear LSI technology to provide a fully contained 12 bit accurate data conversion element.

The 4153 converts an analog input signal to a proportional serial pulse train output with scaling selectable over a wide dynamic range (>100dB). Comparable performance is available in the frequency-to-voltage mode making the 4153 an ideal building block for accurate, wide bandwidth isolation amplifiers and 3-wire analog data links.

The speed, accuracy and temperature performance of the 4153 is achieved by incorporating on a single monolithic chip high speed ECL logic, a high gain, wide bandwidth op amp and an ion-implanted buried zener reference.

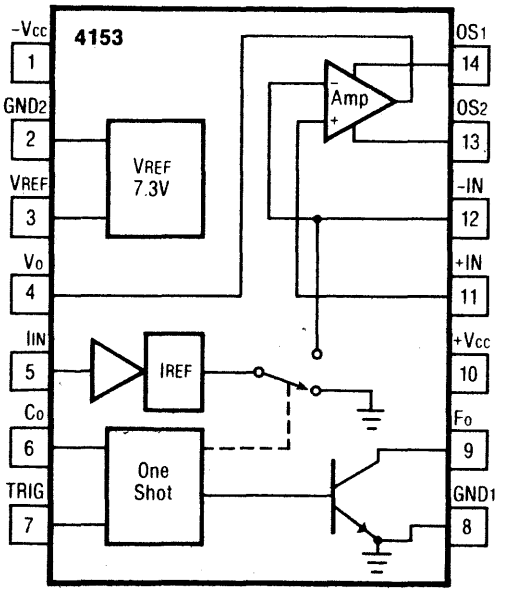
Features

- < .1Hz to > 250KHz dynamic range
- .01% F.S. max. nonlinearity error (.1Hz to 10KHz)
- 150ppm/° C max. gain tempco
- On board 7.3 volt reference

Applications

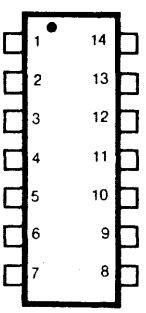
- Precision voltage-to-frequency-converters
- Pulse-width modulators
- Programmable pulse generators
- Frequency-to-voltage converters
- Integrating analog-to-digital converter
- Long-term analog integrator
- Signal Conversion—
  - Current-to-frequency
  - Temperature-to-frequency
  - Pressure-to-frequency
  - Capacitance-to-frequency
  - Frequency-to-current
- Signal isolation
  - VFC → opto-isolation → FVC
  - ADC with opto-isolation
- Signal encoding
  - FSK modulation/demodulation
  - Pulse-width modulation
- Frequency scaling
- DC motor speed control

4153 Functional Block Diagram



Connection Information

DC or DB Dual In-line Packages (Top View)



Pin	Function	Pin	Function
1	-Vcc	8	Circuit GND
2	REF GND	9	Frequency Output (open collector)
3	VREF Output		
4	VOUT (op amp)	10	+Vcc
5	IIN (REF voltage input)	11	(-) Op Amp Input
		12	(+) Op Amp Input
6	Co (Pulse Width)	13	Op Amp Offset Adjust
7	Trigger Input	14	

RAYTHEON
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Electrical Specifications (VCC = ±15V and TA = 25°C unless otherwise noted)

Parameters	Min.	Typ.	Max.	Units
Full Scale Frequency	250	500		KHz
Transfer Characteristics				
Nonlinearity Error:				
0.1Hz≤ F ≤ 10KHz		.006	.01	%FS
1.0Hz≤ F≤ 100KHz		.025	.05	%FS
5.0Hz≤ F≤ 250KHz		.05	.1	%FS
Scaling Factor Tolerance				
K = 2 VREF RIN CO		±3		%
Reference Voltage (VREF)		7.3		V
Output Current (steady state)			8.0	mA
IIN Current (pin 5)		1.0		mA
Temperature Stability (0°C to +70°C)				
Gain		±75	±150	ppm/°C
Gain (external REF)		±25	± 50	ppm/°C
Reference Voltage		±50	±100	ppm/°C
Frequency Output (open collector)				
Saturation Voltage				
IO = 4mA		.2	.4	V
IO = 10mA		.55	1.0	V
Time Base Error				
@ FMAX = 10KHz		1/8		LSB @ 10 Bits
Voltage Output (op amp)				
Output Resistance		230		Ohms
Output Short Circuit Current		25		mA
Gain-Bandwidth Product		2.5	3.0	MHz
Slew Rate	.5	.7		V/uSec
Output Voltage Swing (RL≥2K)	0 to +10	-.5 to +14.3		V
Power Supply Requirements				
Supply Range	±12	±15	±18	V
Supply Current (IO = 0)			7	mA
Inputs				
Analog (V-F)				
Current Range	0-1.5	0-1.8		mA
Input Bias Current		70	400	nA
Input Offset Voltage (adjustable to 0)		.5	3	mV
Input Offset Current		30	60	nA
Input Resistance		1.0		M Ohms
Digital (F-V)				
Logic "0"			.5	V
Logic "1"	2.0			V
Pulse Width	150			nSec
Trigger Current		-50		uA

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Quad High Performance Operational Amplifier

DESCRIPTION

The RM4156/RC4156 is a monolithic integrated circuit, consisting of four independent high performance operational amplifiers constructed with the planar epitaxial process.

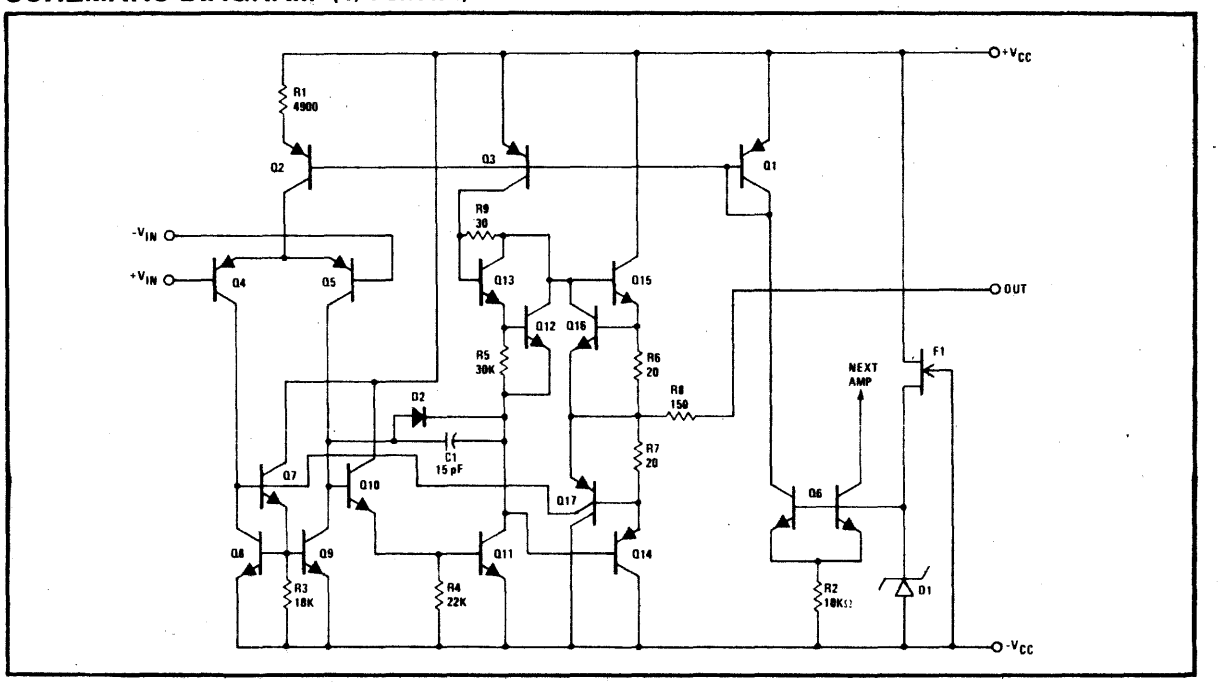
These amplifiers feature guaranteed A.C. performance which far exceeds that of the 741 type amplifiers. Also featured are excellent input characteristics and guaranteed low noise making this device the optimum choice for audio, active filter and instrumentation applications.

FEATURES

	Typical	Guaranteed
• Unity Gain Bandwidth	3.5 MHz	2.8 MHz
• High Slew Rate	1.6V/μS	1.3V/μS
• Low Noise Voltage	1.4μV	2.0μV

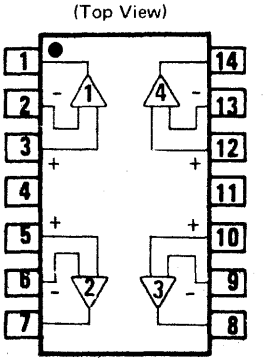
- Indefinite Short Circuit Protection
- No Crossover Distortion
- Low Input Offset and Bias Parameters
- Internal Compensation

SCHEMATIC DIAGRAM (1/4 Shown)



CONNECTION INFORMATION

DB and DC
Dual In-line Package
(Top View)



PIN	FUNCTION
1	OUTPUT A
2	$-V_{IN}$ A
3	$+V_{IN}$ A
4	V+
5	$+V_{IN}$ B
6	$-V_{IN}$ B
7	OUTPUT B
8	OUTPUT C
9	$-V_{IN}$ C
10	$+V_{IN}$ C
11	V-
12	$+V_{IN}$ D
13	$-V_{IN}$ D
14	OUTPUT D

Order Part Nos.:
RM4156DC, RV4156DB,
RV4156DC, RC4156DC,
RC4156DB

RAYTHEON

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ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±20V	Storage Temperature Range	-65 to +150°C
Internal Power Dissipation (Note 1)	880 mW	Operating Temperature Range RM4156	-55 to +125°C
Differential Input Voltage	±30V	RV4156	-40 to +85°C
Input Voltage (Note 2)	±15V	RC4156	0 to +70°C
Output Short Circuit Duration (Note 3)	Indefinite	Lead Soldering Temperature (10 sec)	300°C

ELECTRICAL CHARACTERISTICS V_{CC} ±15V T_A +25°C unless otherwise specified

PARAMETER	CONDITIONS	RM4156 MIN	RM4156 TYP	RM4156 MAX	RV4156/RC4156 MIN	RV4156/RC4156 TYP	RV4156/RC4156 MAX	UNITS
Input Offset Voltage	$R_S \leq 10$ KΩ		0.5	3.0		1.0	5.0	mV
Input Offset Current			15	30		30	50	nA
Input Bias Current			60	200		60	300	nA
Input Resistance			0.5			0.5		MΩ
Large Signal Voltage Gain	$R_L \geq 2$ KΩ V_{OUT} ±10V	50,000	100,000		25,000	100,000		V/V
Output Voltage Swing	$R_L \geq 10$ KΩ	±12	±14		±12	±14		V
	$R_L \geq 2$ KΩ	±10	±13		±10	±13		V
Input Voltage Range		±12	±14		±12	±14		V
Output Resistance			230			230		Ω
Output Short Circuit Current			25			25		mA
Common Mode Rejection Ratio	$R_S \leq 10$ KΩ	80			80			dB
Power Supply Rejection Ratio	$R_S \leq 10$ KΩ	80			80			dB
Supply Current (all amplifiers)	$R_L = \infty$		4.5	5.0		5.0	7.0	mA
Transient Response								
Rise Time			50			75		ns
Overshoot			25%			25%		%
Slew Rate		1.3	1.6		1.3	1.6		V/μs
Unity Gain Bandwidth		2.8	3.5		2.8	3.5		MHz
Phase Margin	R_L = 2 KΩ R_C = 50 pF		50			50		degrees
Full Power Bandwidth	V_O = 20V p-p	20	25		20	25		kHz
Input Noise Voltage	f = 20 Hz to 20 kHz		1.4	2.0		1.4	2.0	μV RMS
Input Noise Current	f = 20 Hz to 20 kHz		15			15		pA RMS
Channel Separation			-108			-108		dB
The following specifications apply for -55°C ≤ T_A ≤ +125°C for RM4156, -40°C ≤ T_A ≤ +85°C for RV4156, 0°C ≤ T_A ≤ +70°C for RC4156.								
Input Offset Voltage	$R_S \leq 10$ KΩ			5.0			6.5	mV
Input Offset Current				75			100	nA
Input Bias Current				325			400	nA
Large Signal Voltage Gain	$R_L \geq 2$ KΩ V_{OUT} ±10V	25,000			15,000			V/V
Output Voltage Swing	$R_L \geq 2$ KΩ	±10			±10			V
Supply Current			10			10		mA
Average Offset Voltage Drift			5			5		μV/°C

Notes: 1. Rating applies for case temperature of +25°C maximum; derate linearity at 6.4 mW/°C for temperatures above +25°C.
2. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
3. Short circuit to ground on one amplifier only.

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General Description

The Raytheon RC4200 is the industry's first integrated circuit multiplier to have complete compensation for non-linearity, the primary source of error and distortion. This is also the first IC multiplier to have three on-board operational amplifiers designed specifically for use in multiplier logging circuits. These specially-designed amplifiers are frequency compensated for optimum AC response in a logging circuit; the heart of a multiplier, and can therefore provide superior AC response in comparison to other analog multipliers.

Versatility is unprecedented; this is the first IC multiplier that can be used in a wide variety of applications without sacrificing accuracy. Four-quadrant multiplication, two-quadrant division, square-rooting, squaring and RMS conversion can all be easily implemented with predictable accuracy. The nonlinearity compensation is not just trimmed at a single temperature, it is designed to provide compensation over the full temperature range. This nonlinearity compensation combined with the low gain and offset drift inherent in a well-designed monolithic chip provides a very low accuracy tempco.

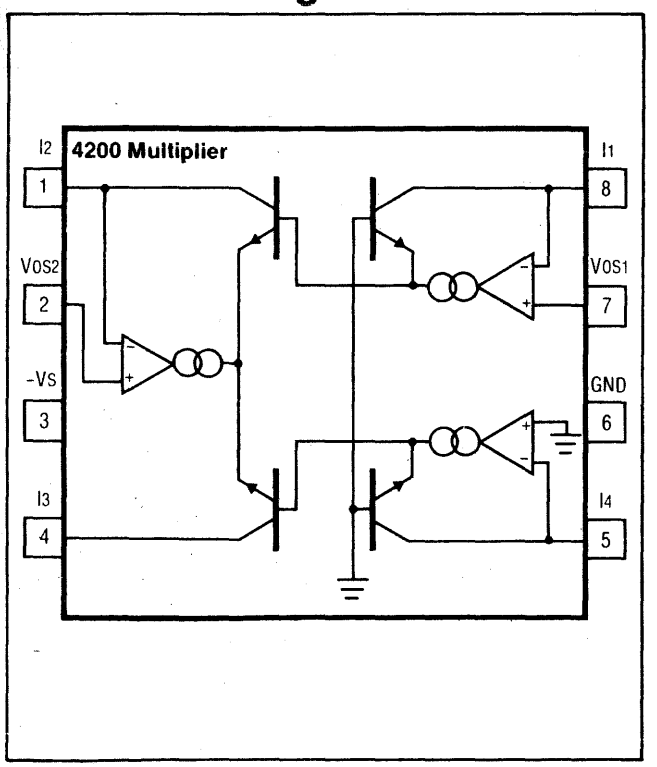
Design Features

- High accuracy
  Non-linearity—0.1% maximum
  Temperature coefficient—0.005%/°C maximum
- Multiple functions
  Multiply, divide, square, square root, RMS-to-DC conversion, AGC, and modulate/demodulate
- Wide bandwidth—4 MHz
- Feedthru Rejection 60dB @ 100 KHz
- Signal-to-noise ratio 94dB

The excellent linearity and versatility were achieved through circuit design rather than special grading to tweaking, therefore unit cost is very low. Analog multipliers can now be used in applications where price was previously an inhibiting factor.

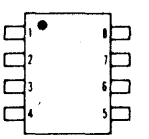
The Raytheon RC4200 is ideal for use in low-distortion audio modulation circuits, voltage-controlled active filters, and precision oscillators.

Functional Diagram



Connection Information

DE and NB Miniature Dual In-line Package
(Top View)



PIN	FUNCTION
1	I_2
2	V_{OS2}
3	-Vs
4	Output I_3
5	I_4
6	Gnd
7	V_{OS1}
8	I_1

Order Part Nos.: RC4200NB, RV4200NB, RC4200DE, RV4200DE, RM4200DE, RC4200ANB, RV4200ANB, RV4200ADE, RM4200ADE.

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Absolute Maximum Ratings (above which the useful life may be impaired)

Supply Voltage	-22V
Internal Power Dissipation	500 mW
Input Current	-5 mA
Storage Temperature Range	
RM4200/4200A	-65° C to +150° C
RV4200/4200A	-55° C to +125° C
RC4200/4200A	-55° C to +125° C
Operating Temperature Range	
RM4200/4200A	-55° C to +125° C
RV4200/4200A	-40° C to +85° C
RC4200/4200A	0° C to +70° C

Electrical Characteristics (over operating temperature range, Vs + -15V unless otherwise noted)

Parameter	Conditions	RC4200A			RC4200			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Input range (I1, I2 and I4)	(Note 1)	1.0		1000	1.0		1000	uA
Total error as multiplier	TA = 25° C							
Untrimmed				+2.0			+3.0	%
With external trim	(Note 2)			+2.0			+0.5	%
Vs temperature			+0.005			+0.005		%/°C
Vs supply (-9 to -18V)			+0.1			+0.1		%/V
Nonlinearity	50uA 1 250uA, TA = 25°C			+0.1			+0.3	%
Input offset voltage	I1 = I2 = I4 = 150uA, TA = 25°C			+5			+10	mV
Input bias current	I1 = I2 = I4 = 150uA, TA = 25°C			300			500	nA
Average temperature coefficient of input offset voltage	I1 = I2 = I4 = 150uA			+50			+100	uV/°C
Output current range (I3)	(Note 3)	1.0		1000	1.0		1000	uA
Frequency response, -3 dB			4			4		MHz
Supply voltage range		-9	-15	-18	-9	-15	-18	V
Quiescent current	I1 = I2 = I4 = 150uA, TA = 25°C			4			4	mA

Notes: 1. Refer to sec. E and sec. G for input current limitations.
2. Refer to Figure 6 for example.
3. These specifications apply with output (I3) connected to an op amp summing junction. If desired, the output (I3) at pin (4) can be used to drive a resistive load directly. The resistive load should be less than 700 ohms and must be pulled up to a positive supply such that the voltage on pin (3) stays within a range of 0 to +5V.

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GENERAL DESCRIPTION

The 4559 integrated circuit is a dual high performance operational amplifier internally compensated and constructed on a single silicon chip using the planar epitaxial process.

These amplifiers feature guaranteed AC performance which far exceeds that of the 741-type amplifiers. The specially designed low-noise input transistors allow the 4559 to be used in low-noise signal processing applications such as audio pre amplifiers and signal conditioners.

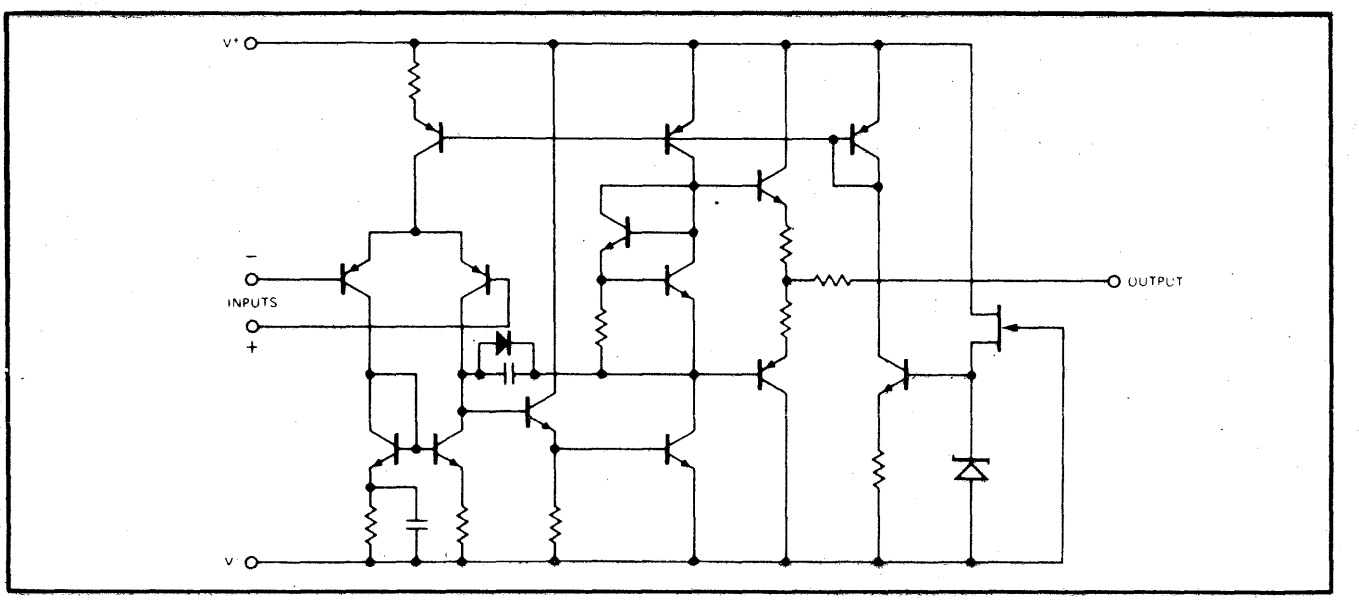
The 4559 also has more output drive than 741-type amplifiers and can be used to drive a 600 ohm load.

FEATURES

	Typical	Guaranteed
• Unity Gain Bandwidth	4.0 MHz	3.0 MHz
• Slew Rate	2.0 V/μsec	1.5 V/μsec
• Low Noise Voltage	1.4 μV_{RMS}	2.0 μV_{RMS}

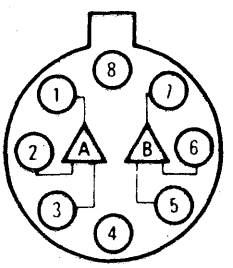
- Supply Voltage ±22V for RM4559 and ±18V for RC4559
- No Frequency Compensation Required
- No Latch Up
- Large Common Mode and Differential Voltage Ranges
- Low Power Consumption
- Parametric Tracking Over Temperature Range
- Gain and Phase Match Between Amplifiers

SCHEMATIC DIAGRAM (1/2 Shown)



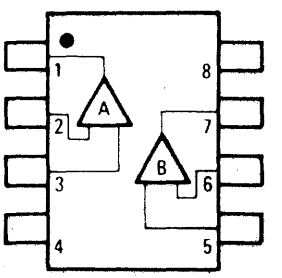
CONNECTION INFORMATION

TE (TO-99)
Metal Can Package
(Top View)



Order Part Nos.:
RC4559T, RM4559T

DE and NB
Dual In-line Packages
(Top View)



Order Part Nos.:
RC4559NB, RV4559NB
RC4559DE, RV4559DE
RM4559DE

PIN	FUNCTION
1	A OUTPUT
2	A -INPUT
3	A +INPUT
4	V^-
5	B +INPUT
6	B -INPUT
7	B OUTPUT
8	V^+

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ABSOLUTE MAXIMUM RATINGS

Supply Voltage	RM4559: ±22V RC4559: ±18V
Internal Power Dissipation (Note 1)	500mW
Differential Input Voltage	±30V
Input Voltage (Note 2)	±15V
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	
RM4559	−55°C to +125°C
RV4559	−40°C to +85°C
RC4559	0°C to +70°C
Lead Temperature (Soldering, 10 sec)	300°C
Output Short-Circuit Duration (Note 3)	Indefinite

ELECTRICAL CHARACTERISTICS (T_A = 25°C, V_{CC} = ±15 V unless otherwise specified.)

		RM4559			RV/RC4559			
PARAMETER	CONDITIONS	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
Input Offset Voltage	$R_S \leq 10k\Omega$		1.0	5.0		2.0	6.0	mV
Input Offset Current			5	100		5	100	nA
Input Bias Current			40	250		40	250	nA
Input Resistance		0.3	1.0		0.3	1.0		MΩ
Large Signal Voltage Gain	$R_L \geq 2k\Omega$, V_{out} = ±10V	50,000	300,000		20,000	300,000		V/V
Output Voltage Swing	$R_L \geq 3k\Omega$ $R_L \geq 600\Omega$	±12 ±9.5	±13 ±10		±12 ±9.5	±13 ±10		V V
Input Voltage Range		±12	±13		±12	±13		V
Common Mode Rejection Ratio	$R_S \leq 10k\Omega$	80	100		80	100		dB
Supply Voltage Rejection Ratio	$R_S \leq 10k\Omega$		10	75		10	75	μV/V
Supply Current	R_L = ∞ (All Amplifiers)		3.3	5.6		3.3	5.6	mA
Transient Response (unity gain) Rise Time	V_{IN} = 20mV, R_L = 2kΩ, $C_L \leq 100pf$		80			80		nsec
Overshoot			18			18		%
Slew Rate (unity gain)		1.5	2.0		1.5	2.0		V/μs
Unity Gain Bandwidth		3.0	4.0		3.0	4.0		MHz
Full Power Bandwidth	V_O = 20 V_{p-p}	24	32		24	32		kHz
Input Noise Voltage	f = 20 Hz to 20 kHz		1.4	2.0		1.4	2.0	μV_{RMS}
Input Noise Current	f = 20 Hz to 20 kHz		25			25		pA RMS
Channel Separation	Gain = 100 f = 10 kHz, R_S = 1kΩ		90			90		dB
The following specifications apply for −55°C ≤ T_A ≤ +125°C for RM4559; 0°C ≤ T_A ≤ +70°C for RC4559								
Input Offset Voltage	$R_S \leq 10k\Omega$			6.0			7.5	mV
Input Offset Current				300			200	nA
Input Bias Current				500			500	nA
Large-Signal Voltage Gain	$R_L \geq 2k\Omega$, V_{out} = ±10V	25,000			15,000			
Output Voltage Swing	$R_L \geq 2k\Omega$	±10			±10			V
Supply Current (All Amplifiers)	V_S = ±15 V, R_L = ∞ T_A = +125°C T_A = −55°C		3 4	5 6.6		3 4	5 6.6	mA

MATCHING CHARACTERISTICS (V_{CC} = ±15V, T_A = 25°C unless otherwise specified)

PARAMETER	CONDITIONS	RM4559 TYP	RC4559 TYP	UNITS
Voltage Gain	$R_L \geq 2k\Omega$	±0.5	±1.0	dB
Input Bias Current		±15	±15	nA
Input Offset Current		±7.5	±7.5	nA
Input Offset Voltage	$R_S \geq 10k\Omega$	±0.1	±0.2	mV

NOTES:
1. Rating applies for case temperatures to 125° C; derate linearly at 6.5mW/° C for ambient temperatures above ×75° C for RM4559
2. For supply voltages less than -15V, the absolute maximum input voltage is equal to the supply voltage.
3. Short circuit may be to ground on one amp only. Rating applies to +125° C case temperature or +75° C ambient temperature for RC4559 and to +85° C ambient temperature for RV4559.

RAYTHEON

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DESCRIPTION

The ST100 is a monolithic μ-255 law companded PCM Codec. This is a per channel device fabricated in I^2L technology. The ST100 has all the circuitry necessary to convert an analog signal into an 8 bit PCM digital data stream and vice versa. Asynchronous operation of transmit and receive is possible. A & B signaling and zero code suppression are also provided. Very few external components are required for its operation. The digital inputs are TTL compatible while the digital outputs are open collector, TTL compatible.

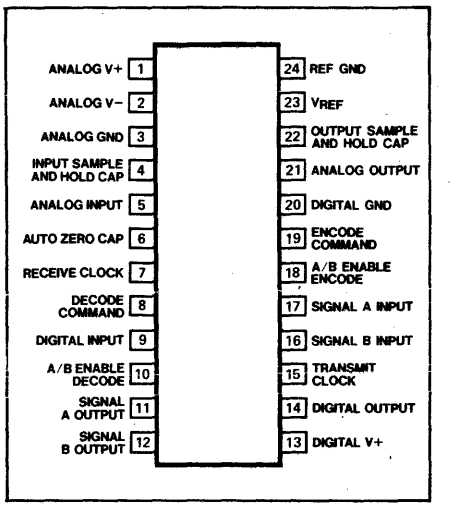
FEATURES

- **μ-255 law companding**
- **Serial data rates up to 2.048MHz**
- **Sampling rates up to 16kHz**
- **Asynchronous operation of transmit and receive**
- **A & B dual channel signaling**
- **Zero code suppression**
- **Low noise**
- **Fabricated with proven, reliable bipolar process**

APPLICATIONS

- **PCM channel banks**
- **EPABX'S**
- **Subscriber loop carrier systems**
- **Central office switches**

PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS*

PARAMETER	RATING	UNIT
Analog supply voltages		
Positive	13	V
Negative	−13	V
Digital supply voltage	+5±0.25	V
Maximum analog input	6V (Peak to Peak)	V
Operating temperature range	0 to +70	°C
Storage temperature range	−65 to +150	°C

*If any of these limits are exceeded more than momentarily, permanent damage to the device may occur.

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NE/SE527-F,K,N

DESCRIPTION

The SE/NE527 is a high speed analog voltage comparator which, in the first time mates state-of-the-art Schottky diode technology with the conventional linear process. This allows simultaneous fabrication of high speed T²L gates with a precision linear amplifier on a single monolithic chip. The SE/NE527 is similar in design to the Signetics SE/NE529 voltage comparator except that it incorporates a "Emitter Follower" input stage for extremely low input currents. This opens the door to a whole new range of applications for analog voltage comparators.

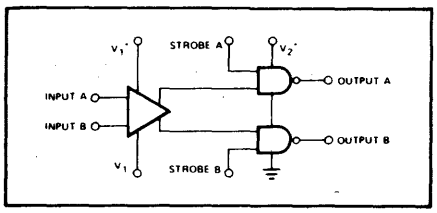
FEATURES

- **15ns propagation delay**
- **Complementary output gates**
- **TTL or ECL compatible outputs**
- **Wide common mode and differential voltage range**
- **Mil std 883A,B,C available**

APPLICATIONS

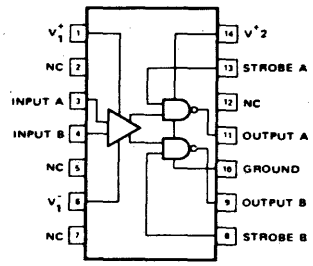
- **A/D conversion**
- **ECL to TTL interface**
- **TTL to ECL interface**
- **Memory sensing**
- **Optical data coupling**

BLOCK DIAGRAM

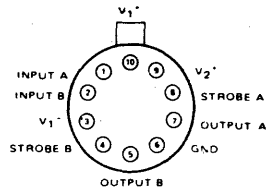


PIN CONFIGURATIONS

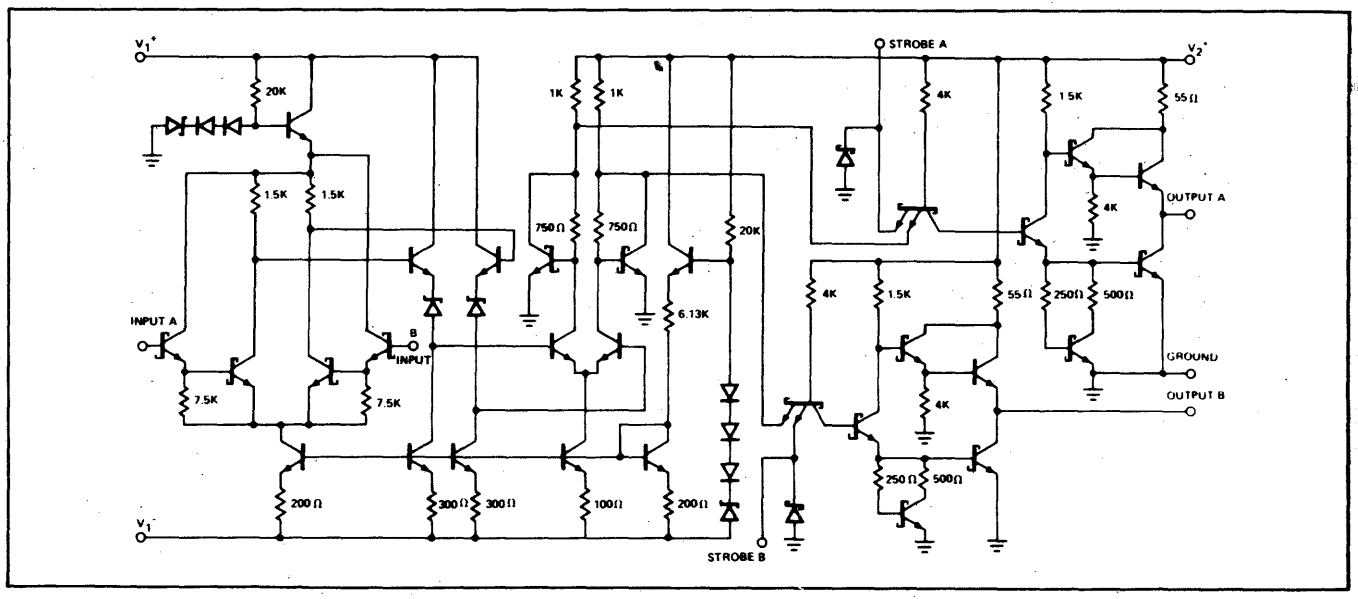
F,N PACKAGE



K PACKAGE



EQUIVALENT SCHEMATIC



NE/SE529-F,K,N

DESCRIPTION

The SE/NE529 is a high speed analog voltage comparator which, for the first time mates state-of-the-art Schottky diode technology with the conventional linear process. This allows simultaneous fabrication of high speed T²L gates with a precision linear amplifier on a single monolithic chip.

FEATURES

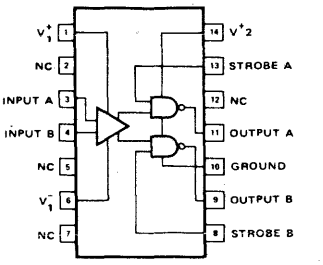
- **10ns propagation delay**
- **Complementary output gates**
- **TTL or ECL compatible outputs**
- **Wide common mode and differential voltage range**

APPLICATIONS

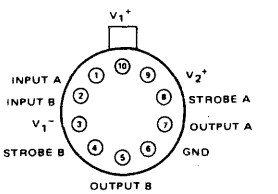
- **A/D conversion**
- **ECL to TTL interface**
- **TTL to ECL interface**
- **Memory sensing**
- **Optical data coupling**
- **Mil std 883A,B,C available**

PIN CONFIGURATION

F,N PACKAGE



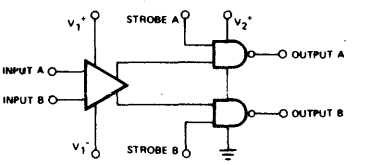
K PACKAGE



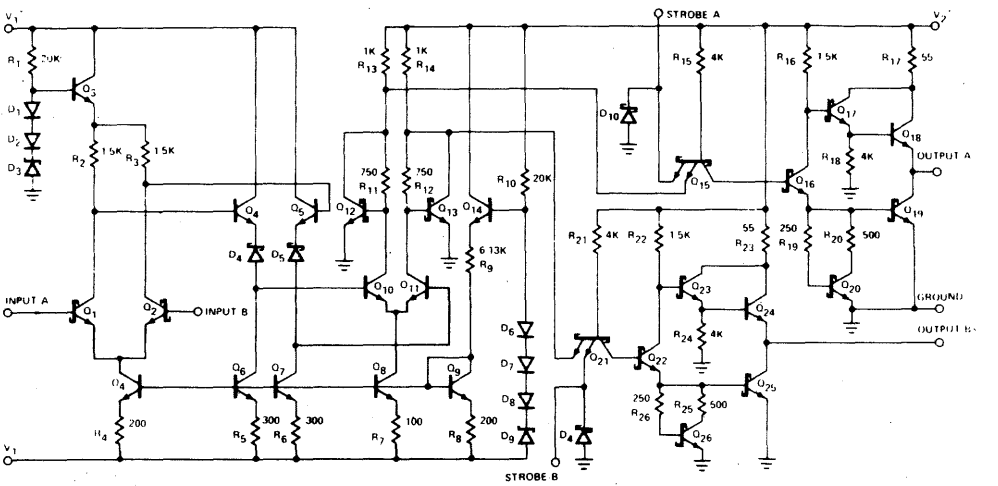
ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Positive supply voltage (V1+)	+15	V
Negative supply voltage (V1-)	-15	V
Gate supply voltage (V2+)	+7	V
Output voltage	+15	V
Differential input voltage	±5	V
Input common mode voltage	±6	V
Power dissipation	600	mW
Operating temperature range		
NE529	0 to +70	°C
SE529	-55 to +125	°C
Storage temperature range	-65 to +150	°C
Lead temperature (soldering, 60 sec)	+300	°C

BLOCK DIAGRAM



EQUIVALENT SCHEMATIC



signetics

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NE/SE532/532A/SA532-N,T

DESCRIPTION

The 532 consists of two independent, high gain, internally frequency compensated operational amplifiers designed specifically to operate from a single power supply over a wide range of voltages. Operation from dual power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage.

FEATURES

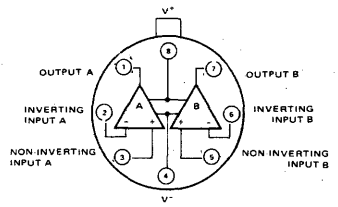
- **Internally frequency compensated for unity gain**
- **Large dc voltage gain—(100dB)**
- **Wide bandwidth (unity gain)—1MHz (temperature compensated)**
- **Wide power supply range**
  single supply—(3Vdc to 30Vdc)
  or dual supplies—(±1.5Vdc to ±15Vdc)
- **Very low supply current drain (400μA)—essentially independent of supply voltage (1mW/op amp at +5Vdc)**
- **Low input biasing current—(45nA dc temperature compensated)**
- **Low input offset voltage—(2mVdc) and offset current—(5nA dc)**
- **Differential input voltage range equal to the power supply voltage**
- **Large output voltage—(0Vdc to V+—-1.5Vdc swing)**
- **SE532 Mil std 883A,B,C available**

UNIQUE FEATURES

In the linear mode the input common-mode voltage range includes ground and the output voltage can also swing to ground, even though operated from only a single power supply voltage. The unity gain cross frequency is temperature compensated. The input bias current is also temperature compensated.

PIN CONFIGURATIONS

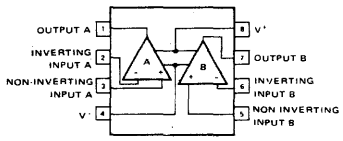
T PACKAGE
(Top View)



ORDER PART NO.

SE532T	NE532T
SE532AT	NE532AT
SA532T	

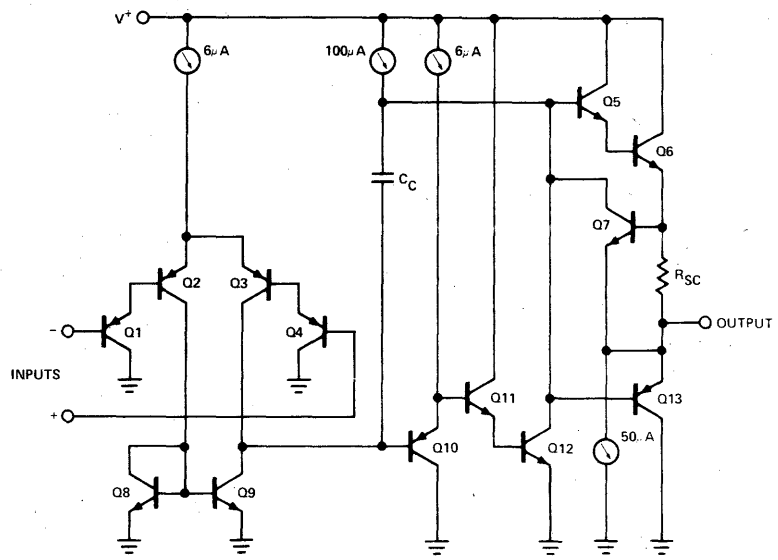
N PACKAGE
(Top View)



ORDER PART NO.

SE532N	NE532N
SA532N	
SE532AN	NE532AN

EQUIVALENT CIRCUIT



ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Supply voltage, V+	32 or ±16	Vdc
Differential input voltage	32	Vdc
Input voltage	-0.3 to +32	Vdc
Power dissipation		
T package	680	mW
N package	625	mW
Output short-circuit to GND		
V+ < 15 Vdc and T_A = 25°C	Continuous	
Operating temperature range		
NE532	0 to +70	°C
SA532	-40 to +85	°C
SE532	-55 to +125	°C
Storage temperature range	-65 to +150	°C
Lead temperature (soldering, 10sec)	300	°C

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NE/SE532/532A/SA532-N,T

DC ELECTRICAL CHARACTERISTICS

$T_A = 25°C$, $V+ = +5V$ unless otherwise specified (see Notes on following page).

PARAMETER	TEST CONDITIONS	SE532			NE532			UNIT
		Min	Typ	Max	Min	Typ	Max	
V_{OS} Offset voltage[1]	$R_S \leq 10k$		±2	±5		±2	±6	mV
	$R_S \leq 10k\Omega$, over temp.			±7			±7.5	mV
V_{OS} Drift	$R_S = 0\Omega$, over temp.		7			7		µV/°C
I_{OS} Offset current	$I_{IN}(+)$ or $I_{IN}(-)$		±3	±30		+5	±50	nA
I_{OS} Offset current	Over temp.			±100			±150	nA
I_{OS} Drift	Over temp.		10			10		pA/°C
I_{BIAS} Input current[2]	$I_{IN}(+)$ or $I_{IN}(-)$		45	150		45	250	nA
	Over temp., $I_{IN}(+)$ or $I_{IN}(-)$		40	300		40	500	nA
V_{CM} Common mode voltage range[3]	$V+ = 30V$	0		V+−1.5	0		V+−1.5	V
	Over temp., $V+ = 30V$			V+−2.0			V+−2.0	V
C_{MRR} Common mode rejection ratio	$R_S \leq 10k\Omega$	70	85		65	70		dB
V_{OUT} Output voltage swing (V_{OH})	$R_L \geq 2k\Omega$, $V+ = 30V$	26			26			V
	$R_L \geq 10k\Omega$, $V+ = 30V$	27	28		27	28		V
V_{OUT} Output voltage swing (V_{OL})	$R_L \leq 10k\Omega$, over temp.		5	20		5	20	mV
I_{CC} Supply current	$R_L = \infty$ on all amplifiers, over temp		0.5	1.2		0.5	1.2	mA
A_{VOL} Large signal voltage Gain	$R_L \geq 2k\Omega$, $V_{OUT} \pm 10V$, $V_S = \pm 15V$	50	100		25	100		V/mV
	Over temp.	25			15			V/mV
P_{SRR} Supply voltage rejection ratio	$R_S \leq 10k\Omega$	65	100		65	100		dB
Amplifier-to-amplifier coupling[4]	f = 1kHz to 20kHz (input referred)		−120			−120		dB
Output current source	$V_{IN}+ = 1Vdc$, $V_{IN}- = 0Vdc$, $V+ = 15Vdc$	20	40		20	40		mA
Output current sink	$V_{IN}- = 1Vdc$, $V_{IN} = 0Vdc$, $V+ = 15Vdc$	10	20		10	20		mA
	$V_{IN}- = 1Vdc$, $V_{IN} = 0Vdc$, $V_{OUT} = 200mVdc$	12	50		12	50		µA
I_{SC}[5]			40	60		40	60	mA

DC ELECTRICAL CHARACTERISTICS

(Cont'd) $T_A = 25°C$, $V+ = +5V$ unless otherwise specified (see Notes on following page).

PARAMETER	TEST CONDITIONS	SA532			SE532A			UNIT
		Min	Typ	Max	Min	Typ	Max	
V_{OS} Offset voltage[1]	$R_S \leq 10k$		±2	±6		1	2	mV
	$R_S \leq 10k\Omega$, over temp.			±7.5			4	mV
V_{OS} Drift	$R_S = 0\Omega$, over temp.		7			7	15	µV°C
I_{OS} Offset current	$I_{IN}(+)$ or $I_{IN}(-)$		±5	±50		2	10	nA
I_{OS} Offset current	Over temp.			±150			30	nA
I_{OS} Drift	Over temp.		10			10	200	pA/°C
I_{BIAS} Input current[2]	$I_{IN}(+)$ or $I_{IN}(-)$		45	250		20	50	nA
	Over temp., $I_{IN}(+)$ or $I_{IN}(-)$		40	500		40	100	nA
V_{CM} Common mode voltage range[3]	$V+ = 30V$	0		V+−1.5	0		V+−1.5	V
	Over temp., $V+ = 30V$			V+−2.0	0		V+−1.5	V
C_{MRR} Common mode rejection ratio	$R_S \leq 10k\Omega$	65	70		70	85		dB
V_{OUT} Output voltage swing (V_{OH})	$R_L \geq 2k\Omega$, $V+ = 30V$	26						V
	$R_L \geq 10k\Omega$, $V+ = 30V$	27	28					V
V_{OUT} Output voltage swing (V_{OL})	$R_L \leq 10k\Omega$, over temp.		5	20				mV
I_{CC} Supply current	$R_L = \infty$ on all amplifiers, over temp.		0.5	1.2		0.5	1.2	mA
A_{VOL} Large signal voltage Gain	$R_L \geq 2k\Omega$, $V_{OUT} \pm 10V$, $V_S = \pm 15V$	25	100		50	100		V/mV
	Over temp.	15			25			V/mV
P_{SRR} Supply voltage rejection ratio	$R_S \leq 10k\Omega$	65	100		65	100		dB
Amplifier-to-amplifier coupling[4]	f = 1kHz to 20kHz (input referred)		−120			−120		dB
Output current source	$V_{IN}+ = 1Vdc$, $V_{IN}- = 0Vdc$, $V+ = 15Vdc$	20	40		20	40		mA
Output current sink	$V_{IN}- = 1Vdc$, $V_{IN} = 0Vdc$, $V+ = 15Vdc$	10	20		10	20		mA
	$V_{IN}- = 1Vdc$, $V_{IN} = 0Vdc$, $V_{OUT} = 200mVdc$	12	50		12	50		µA
I_{SC}[5]			40	60		40	60	mA

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NE564-N

DESCRIPTION

The NE564 is a versatile, high frequency Phase Locked Loop designed for operation up to 50MHz. As shown in the block diagram, the NE564 consists of a VCO, limiter, phase comparator, and post detection processor.

APPLICATIONS

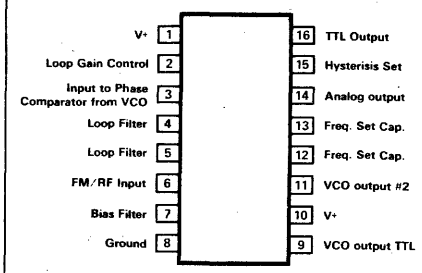
- **High speed modems**
- **FSK receivers and transmitters**
- **Frequency synthesizers**
- **Signal generators**

FEATURES

- **Operation with single 5V supply**
- **TTL compatible inputs and outputs**
- **Operation to 50MHz**
- **External loop gain control**
- **Reduced carrier feedthrough**
- **No elaborate filtering needed in FSK applications**
- **Can be used as a modulator**
- **Variable loop gain (Externally Controlled)**

PIN CONFIGURATION

N PACKAGE

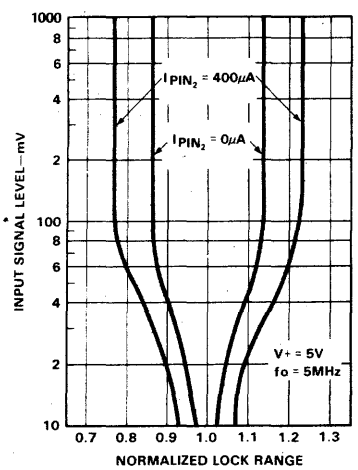


ABSOLUTE MAXIMUM RATINGS

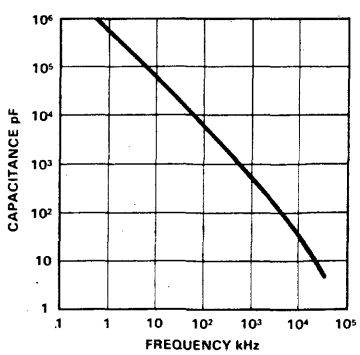
PARAMETER		RATING	UNIT
V+	Supply voltage		V
	Pin 1	14	
	Pin 10	6	
P_D	Power dissipation	400	mW
T_A	Operating temperature	0 to 70	°C
t_{stg}	Storage temperature	-65 to 150	°C

TYPICAL PERFORMANCE CHARACTERISTICS

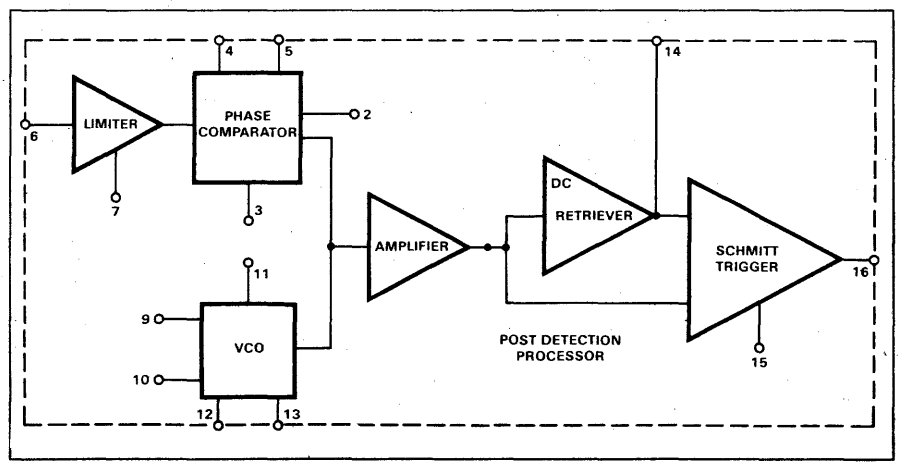
LOCK RANGE vs SIGNAL INPUT



VCO CAPACITOR vs FREQUENCY



BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

The NE564 is a monolithic phase locked loop with a post detection processor. The use of Schottky clamped transistors and optimized device geometries extends the frequency of operation to 50MHz. In addition to the classical PLL applications, the NE564 can be used as a modulator with a controllable frequency deviation.

The output voltage of the PLL can be written as shown in the following equation:

Equation 1

$$v_o = \frac{(f_{in} - f_o)}{K_{VCO}}$$

K_{VCO} = conversion gain of the VCO (see figure 7)
f_{in} = frequency of the input signal
f_o = free running frequency of the VCO

The process of recovering FSK signals involves the conversion of the PLL output into logic compatible signals.

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DESCRIPTION

The 570/571 is a versatile low cost dual gain control circuit in which either channel may be used as a dynamic range compressor or expandor. Each channel has a full wave rectifier to detect the average value of the signal; a linerarized, temperature compensated variable gain cell; and an operational amplifier.

The 570/571 is well suited for use in telephone subscriber and trunk carrier systems, communications systems and hi-fi audio systems.

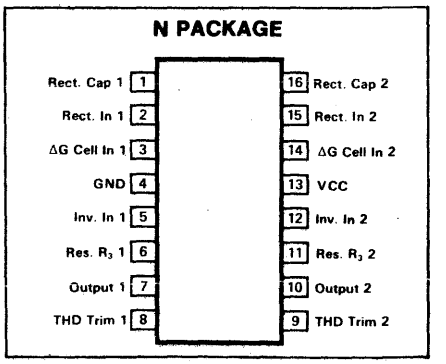
FEATURES

- **Complete compressor and expandor in 1 IC**
- **Temperature compensated**
- **Greater than 110dB dynamic range**
- **Operates down to 6Vdc**
- **System levels adjustable with external components**
- **Distortion may be trimmed out**

APPLICATIONS

- **Telephone trunk compandor—570**
- **Telephone subscriber compandor—571**
- **High level limiter**
- **Low level expandor—noise gate**
- **Dynamic noise reduction systems**
- **Voltage controlled amplifier**
- **Dynamic filters**

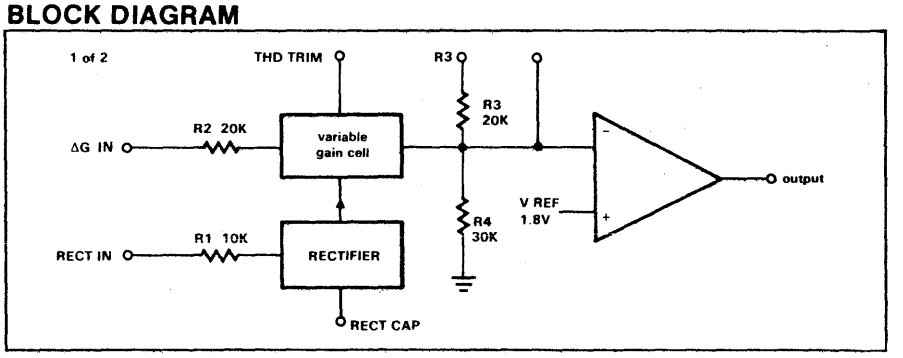
PIN CONFIGURATION



ABSOLUTE MAXIMUM RATINGS

	PARAMETER	RATING	UNIT
	Positive supply		Vdc
	570	24	
	571	18	
T_A	Operating temperature range	-40 to +70	°C
P_D	Power dissipation	400	mW

BLOCK DIAGRAM



CIRCUIT DESCRIPTION

The 570/571 compandor building blocks, as shown in the block diagram, are a full wave rectifier, a variable gain cell, an operational amplifier and a bias system. The arrangement of these blocks in the IC result in a circuit which can perform well with few external components, yet can be adapted to many diverse applications.

The full wave rectifier rectifies the input current which flows from the rectifier input, to an internal summing node which is biased at V_{REF}. The rectified current is averaged on an external filter capacitor tied to the C_{RECT} terminal, and the average value of the input current controls the gain of the variable gain cell. The gain will thus be proportional to the average value of the input signal for capacitively coupled voltage inputs as shown in the following equation. Note that for capacitively coupled inputs there is no offset voltage capable of producing a gain error. The only error will come from the bias current of the rectifier (supplied internally) which is less than .1μA.

$$G \propto \frac{|V_{IN} - V_{REF}|_{ave}}{R_1}$$

or

$$G \propto \frac{|V_{IN}|_{ave}}{R_1}$$

The speed with which gain changes to follow changes in input signal levels is determined by the rectifier filter capacitor. A small capacitor will yield rapid response but will not fully filter low frequency signals. Any ripple on the gain control signal will modulate the signal passing through the variable gain cell. In an expandor or compressor application, this would lead to third harmonic distortion, so there is a tradeoff to be made between fast attack and decay times, and distortion. For step changes in amplitude, the change in gain with time is shown by this equation.

$$G(t) = (G_{initial} - G_{final})\ e^{-t/\tau} + G_{final};\ \tau = 10K \times C_{RECT}$$

The variable gain cell is a current in, current out device with the ratio I_{OUT}/I_{IN} controlled by the rectifier. I_{IN} is the current which flows from the ΔG input to an internal summing node biased at V_{REF}. The following equation applies for capacitively coupled inputs. The output current, I_{OUT}, is fed to the summing node of the op amp.

$$I_{IN} = \frac{V_{IN} - V_{REF}}{R_2} = \frac{V_{IN}}{R_2}$$

A compensation scheme built into the ΔG cell compensates for temperature, and cancels out odd harmonic distortion. The only distortion which remains is even harmonics, and they exist only because of internal offset voltages. The THD trim terminal provides a means for nulling the internal offsets for low distortion operation.

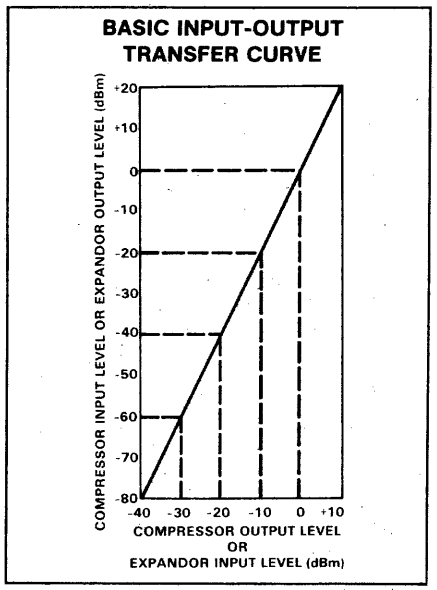
The operational amplifier (which is internally compensated) has the non-inverting input tied to V_{REF}, and the inverting input connected to the ΔG cell output as well as brought out externally. A resistor, R_3, is brought out from the summing node and allows compressor or expandor gain to be determined only by internal components. The output stage is capable of ±20mA output current. This allows a +13dBm (3.5V rms) output into a 300Ω load which, with a series resistor and proper transformer, can result in +13dBm with a 600Ω output impedance.

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A band gap reference provides the reference voltage for all summing nodes, a regulated supply voltage for the rectifier and ΔG cell, and a bias current for the ΔG cell. The low tempco of this type of reference provides very stable biasing over a wide temperature range.

The typical performance characteristics illustration shows the basic input-output transfer curve for basic compressor or expandor circuits.

TYPICAL PERFORMANCE CHARACTERISTICS



DC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_{CC} = 15V$[1]

PARAMETER	TEST CONDITIONS	NE570			NE571			UNIT
		Min	Typ	Max	Min	Typ	Max	
V_{CC} Supply voltage		6		24	6		18	V
I_{CC} Supply current	No signal		3.2	4.0				mA
Output current capability		±20						mA
Output slew rate			±.5					V/us
Gain cell distortion[2]	Untrimmed		.3	1.0		.5	2.0	%
	Trimmed		.05			.1		
Resistor tolerance			±5	±15				%
Internal reference voltage		1.7	1.8	1.9	1.65	1.8	1.95	V
Output dc shift[3]	Untrimmed		±20	±50		±30	±100	mV
Expandor output noise	No signal, 20Hz-20kHz		20					μV
			-15					dBRNC
Unity gain level		-1	0	+1	-1.5	0	+1.5	dBm
Gain change[2,4]	-40°C < T < 70°C		±.1	±.3		±.1	±.5	dB
	0°C < T < 70°C		±.1	±.2		±.1	±.4	
Reference drift[4]	-40°C < T < 70°C		+2, -25	-10, -40		+2, -25	+20, -50	mV
	0°C < T < 70°C		±5	±10		±5	±20	
Resistor drift[4]	-40°C < T < 70°C		+8,-0					%
	0°C < T < 70°C		+1,-0					
Tracking error[5]	Rectifier input=							dB
	+6dBm		±.2					
	-10dBm		+.2	-.2,+.4		+.2	-.2,+.5	
	-20dBm		+.2	-.3,+.6		+.2	-.4,+.7	
	-30dBm		+.2	-.5,+1		+.2	-1,+1.5	
	-40dBm		+.2,-.4			+.2,-.4		

NOTES

1. Except where indicated, the 571 specifications are identical to the 570
2. Measured at OdBm
3. Expandor ac input change from no signal to OdBm
4. Relative to value at $T_A = 25°C$
5. Relative to OdBm

DESCRIPTION

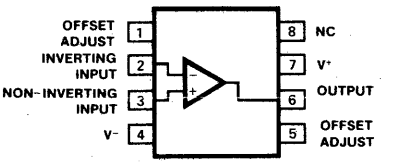
The 530/5530 are new generation operational amplifiers featuring high slew rates combined with improved input characteristics. Internally compensated, the SE530/5530 guarantee slew rates of 25V/μs with 2mV maximum offset voltage. Industry standard pinout and internal compensation allow the user to upgrade system performance by directly replacing general purpose amplifiers such as the 741, 747, 1458, 4558 and LF356 types.

FEATURES

- **Gain bandwidth product—3MHz**
- **35V/μs slew rate (Gain = -1)**
- **Internal frequency compensation**
- **Low input offset voltage 2mV max**
- **Low input bias current-60nA max**
- **Short circuit protection**
- **Offset null capability**
- **Large common mode and differential voltage ranges**

PIN CONFIGURATIONS

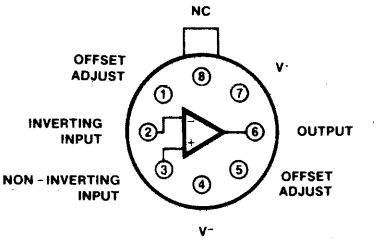
FE,N PACKAGE



ORDER PART NO.

SE530FE, SE530N
NE530FE, NE530N

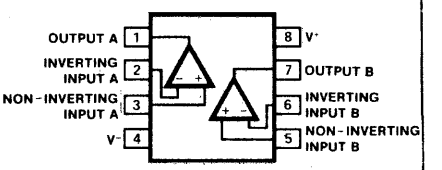
T PACKAGE



ORDER PART NO.

SE530T NE530T

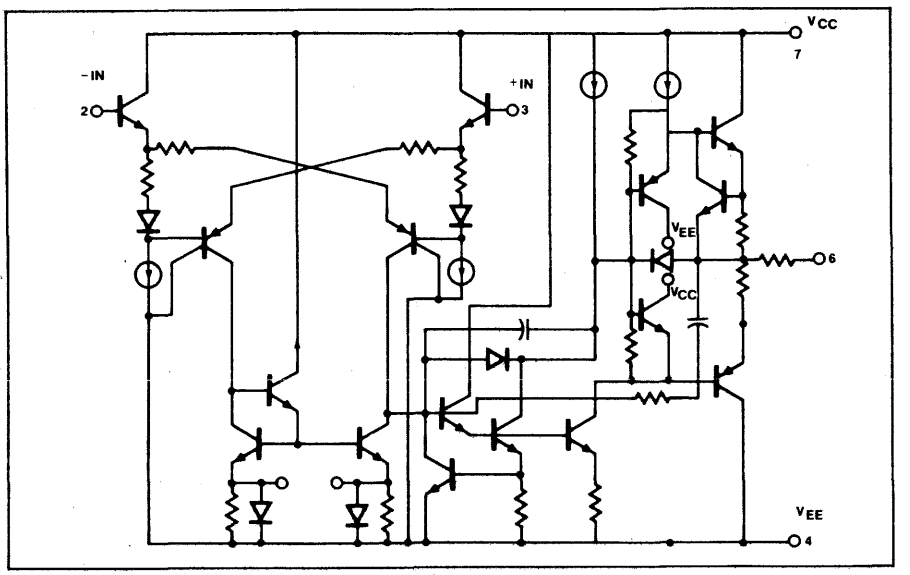
N PACKAGE



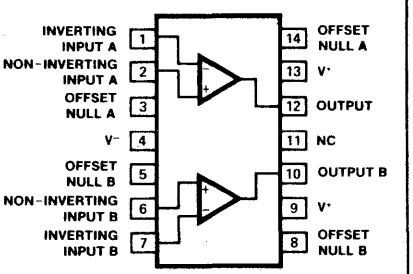
ORDER PART NO.

SE5530N
NE5530N

EQUIVALENT SCHEMATIC EACH AMPLIFIER



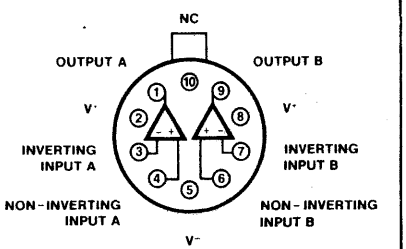
F , N-14 PACKAGE



ORDER PART NO.

SE5530F, SE5530N-14
NE5530F, NE5530N-14

K PACKAGE



ORDER PART NO.

SE5530K
NE5530K

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Supply voltage		
SE530/5530	±22	V
NE530/5530	±18	V
Internal power dissipation[1]		
N Package	500	mW
K/T Package	800	mW
F Package	1000	mW
Differential input voltage	±30	V
Input voltage[2]	±15	V
Operating temperature range		
SE530/5530	-55 to +125	°C
NE530/5530	0 to +70	°C
Storage temperature range	-65 to +150	°C
Lead temperature range (Solder, 60sec)	300	°C
Output short circuit[3]	Indefinite	

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DC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_{CC} = \pm 15V$ unless otherwise specified.[1]

PARAMETER	TEST CONDITIONS	SE530/5530			NE530/5530			UNIT
		Min	Typ	Max	Min	Typ	Max	
Input offset voltage	$R_S \leq 10k\Omega$ Over temperature		0.7	2.0 3.0		2.0	5.0 6.0	mV mV
Temperature coefficient of input offset voltage			3	15		6		$\mu V/°C$
Input offset current	 Over temperature		5	10 20		15	40 80	nA nA
Input bias current	 Over temperature		45	60 100		65	150 200	nA nA
Input resistance		3	10		1	6		$m\Omega$
Input voltage range		±12	±13		±12	±13		V
Large signal voltage gain	$R_L \geq 2k\Omega$, $V_0 = \pm 10V$ Over temperature	50 25	200		50 25	200		V/mV V/mV
Output voltage swing	$R_L \geq 10k\Omega$ $R_L \geq 2k\Omega$ $V_{CC} = \pm 5V$, $R_L \geq 2k\Omega$	±12 ±10 ±3.5	±14 ±13		±12 ±10 ±3.5	±14 ±13		V V V
Output short circuit current			25			25		mA
Output resistance			100			100		Ω
Supply current	Each amplifier Over temperature		2.0 2.2	3.0 3.6		2.0 2.2	3.0	mA mA
Common mode rejection ratio	$Rs \leq 10k\Omega$ Over temperature	70	90			90		dB
Power supply rejection ratio	$Rs \leq 10k\Omega$ Over temperature		30	150	70	30	150	$\mu V/V$

AC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_{CC} = \pm 15V$ unless otherwise specified.

PARAMETER	TEST CONDITIONS	SE530/5530			NE530/5530			UNIT
		Min	Typ	Max	Min	Typ	Max	
Transient response								
Small signal rise time			.06			.06		μs
Small signal overshoot			13			13		%
Settling time	TO 0.1% (10V step)		0.9			0.9		μs
Slew rate	$\pm 15V$ supply, $V_0 = \pm 10V$, $R_L \geq 2k\Omega$							
Unity gain inverting		25	35		20	35		$V/\mu s$
Unity gain non-inverting		18	25		12	25		$V/\mu s$
Power bandwidth	5% THD, $V_0 = \pm 10V$, $R_L \geq 2k\Omega$	360	500		280	500		kHz
Small signal bandwidth	Open loop		3			3		MHz
Channel separation				120		120		dB

NOTE

1. Operating temperature range for the SE530/5530 is -55°C to +125°C.
   Operating temperature range for the NE530/5530 is 0°C to +70°C.

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NE5532/5532A-FE,T

DESCRIPTION

The NE5532 is a dual high-performance low noise operational amplifier. Compared to most of the standard operational amplifiers, such as the 1458, it shows better noise performance, improved output drive capability and considerably higher small-signal and power bandwidths.

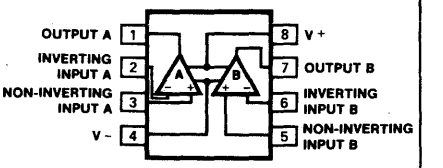
This makes the device especially suitable for application in high quality and professional audio equipment, instrumentation and control circuits, and telephone channel amplifiers. The op amp is internally compensated for gains equal to one. If very low noise is of prime importance, it is recommended that the NE5532A version be used which has guaranteed noise specifications.

FEATURES

- **Small-signal bandwidth: 10MHz**
- **Output drive capability: 600Ω, 10V (rms)**
- **Input noise voltage: 5nV/√Hz**
- **DC voltage gain: 50000**
- **AC voltage gain: 2200 at 10kHz**
- **Power bandwidth: 140kHz**
- **Slew-rate: 9V/μs**
- **Large supply voltage range: ±3 to ±20V**
- **Pin out 5532**
  MC1458
  TL072
  LF353

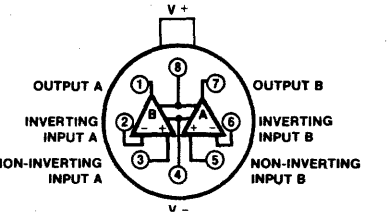
PIN CONFIGURATION

FE PACKAGE



ORDER PART NO.
NE5532FE
NE5532AFE

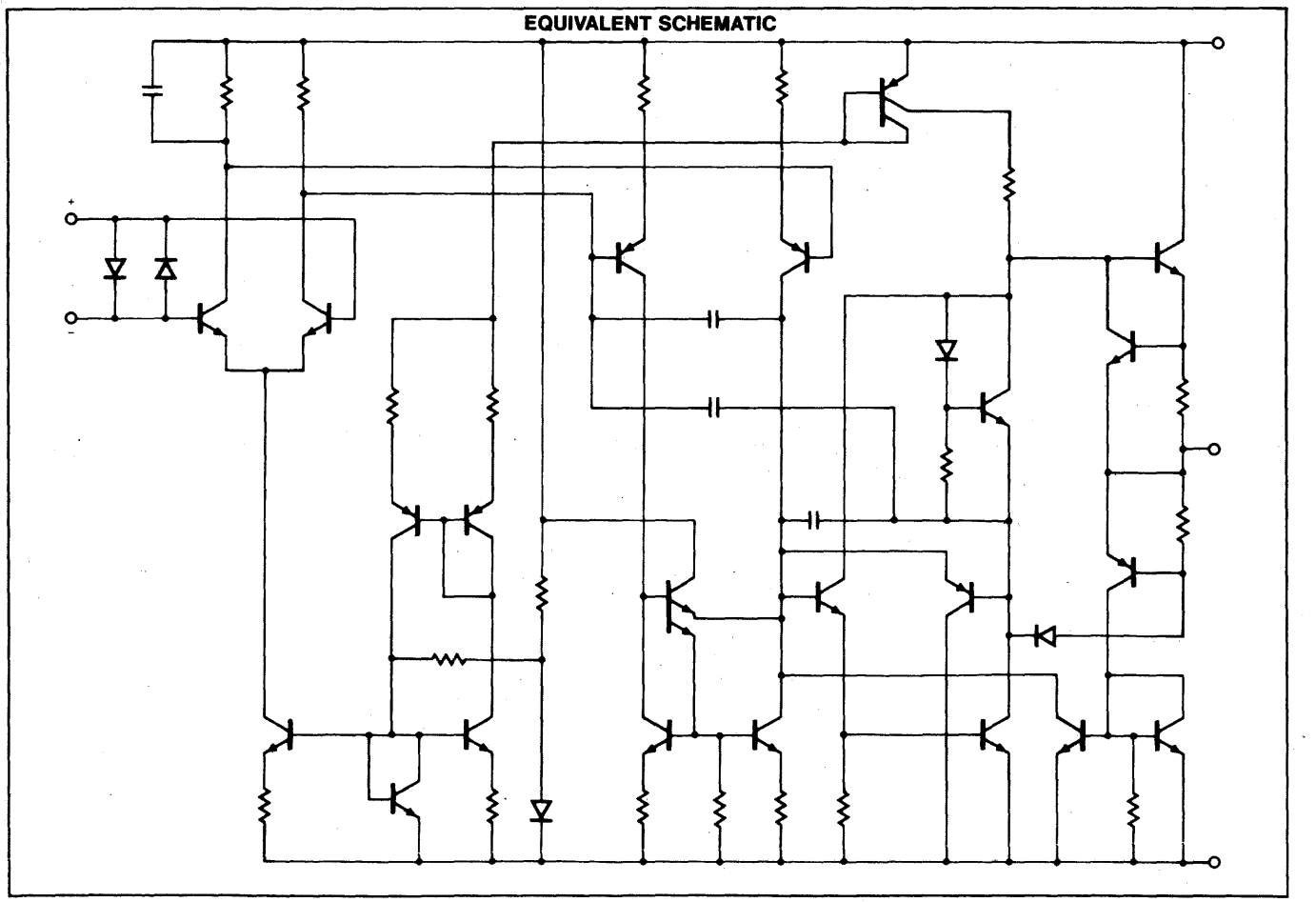
T PACKAGE



ORDER PART NO.
NE5532T
NE5532AT

EACH AMPLIFIER

EQUIVALENT SCHEMATIC



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NE/5533/5533A-N,F•NE/SE5534/5534A-N,T

DESCRIPTION

The 5533/5534 are single and dual high-performance low noise operational amplifiers. Compared to other operational amplifiers, such as TL083, they show better noise performance, improved output drive capability and considerably higher small-signal and power bandwidths.

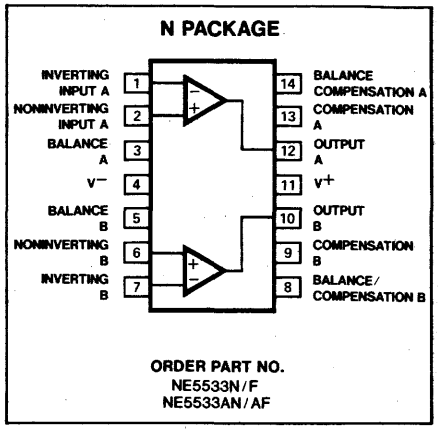
This makes the devices especially suitable for application in high quality and professional audio equipment, in instrumentation and control circuits and telephone channel amplifiers. The op amps are internally compensated for gain equal to, or higher than, three. The frequency response can be optimized with an external compensation capacitor for various applications (unity gain amplifier, capacitive load, slew-rate, low overshoot, etc.) If very low noise is of prime importance, it is recommended that the 5533A/5534A version be used which has guaranteed noise specifications.

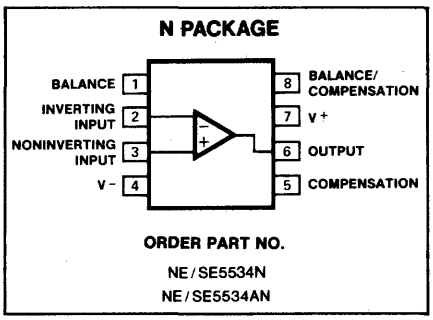
FEATURES

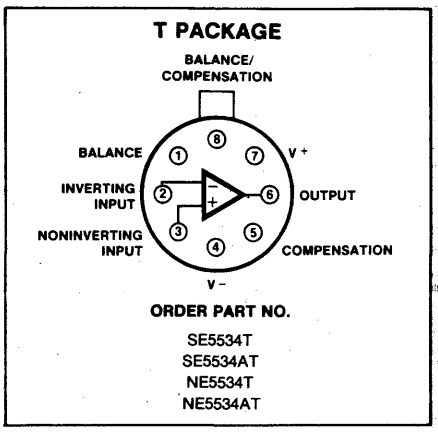
- **Small-signal bandwidth: 10MHz**
- **Output drive capability: 600Ω, 10V (rms) at $V_S = \pm 18V$**
- **Input noise voltage: 4nV/$\sqrt{Hz}$**
- **DC voltage gain: 100000**
- **AC voltage gain: 6000 at 10kHz**
- **Power bandwidth: 200kHz**
- **Slew-rate: 13V/μs**
- **Large supply voltage range: ±3 to ±20V**

	5534
• Pin out	741
• Configuration	Single

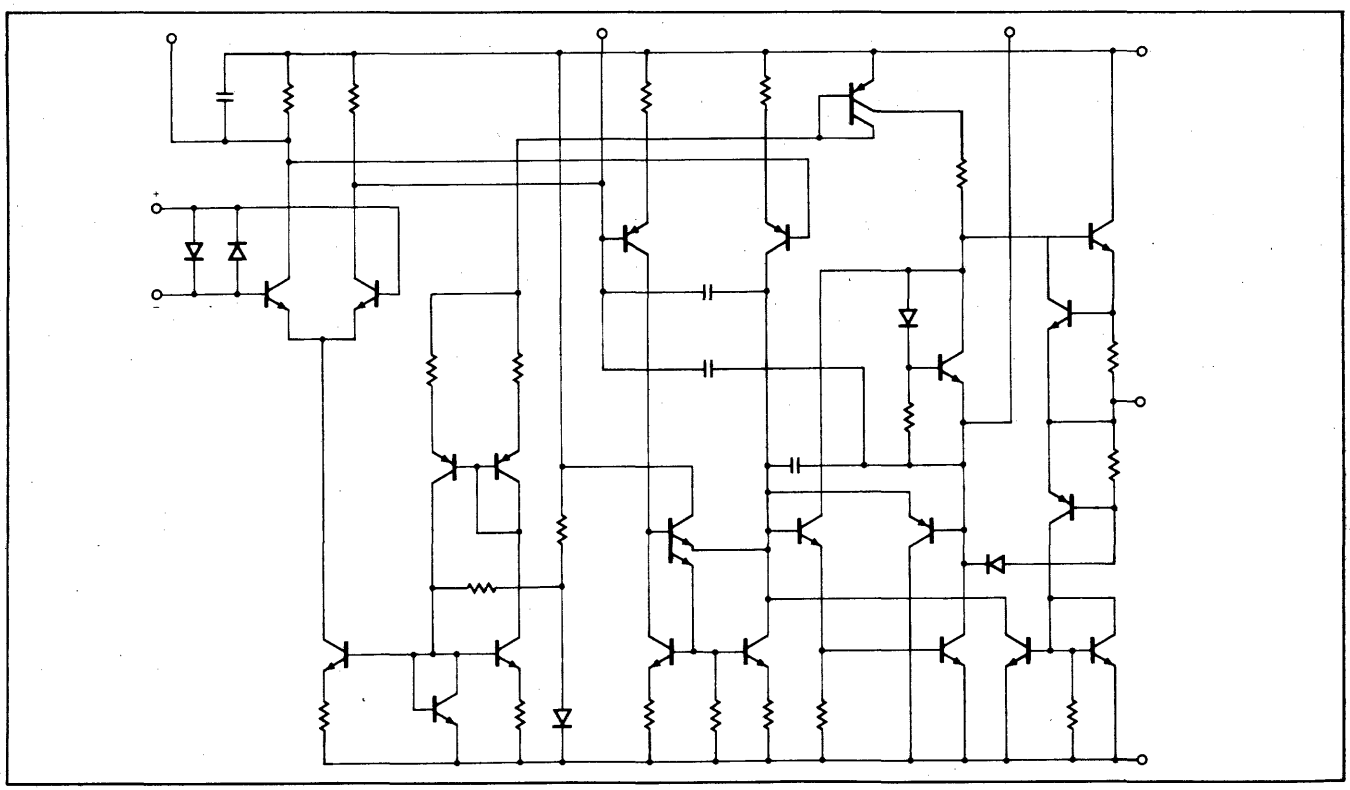
PIN CONFIGURATION







EQUIVALENT SCHEMATIC



ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
V_S	Supply voltage	±22	V
V_{IN}	Input voltage	±V supply	V
V_{DIFF}	Differential input voltage[1]	±.5	V
T_A	Operating temperature range		
	SE5534/5534A	-55 to +125	°C
	NE5533/5533A/5534/5534A	0 to 70	°C
T_{STG}	Storage temperature	-65 to +150	°C
T_J	Junction temperature	150	°C
P_D	Power dissipation at 25°C[2]		
	5533N 5534N	500	mW
	5534T	800	mW
	Output short circuit duration[3]	indefinite	
	Lead temperature (soldering 10 sec)	300	°C

NOTES

1. Diodes protect the inputs against over-voltage. Therefore, unless current-limiting resistors are used, large currents will flow if the differential input voltage exceeds 0.6V. Maximum current should be limited to ±10mA.
2. For operation at elevated temperature T package must be derated based on a thermal resistance of 150°C/W junction to ambient, 45°C/W junction to case. Thermal resistance of the N package is 240°C/W junction to ambient.
3. Output may be shorted to ground at $V_S = \pm 15V$, $T_A = 25°C$. Temperature and/or supply voltages must be limited to ensure dissipation rating is not exceeded.

DC ELECTRICAL CHARACTERISTICS

$T_A = 25°C$, $V_S = \pm 15V$ unless otherwise specified.[1,2]

PARAMETER		TEST CONDITIONS	SE5534/5534A			NE5533/5533A 5534/5534A			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OS}	Offset voltage			.5	2		5	4	mV
		Over temperature			3			5	mV
I_{OS}	Offset current			10	200		20	300	nA
		Over temperature			500			400	nA
I_B	Input current			400	800		500	1500	nA
		Over temperature			1500			2000	nA
I_{CC}	Supply current			4	6.5		4	8	mA
	Per op amp	Over temperature			9				mA
V_{CM}	Common mode input range		±12	±13		±12	±13		V
CMRR	Common mode rejection ratio		80	100		70	100		dB
PSRR	Power supply rejection ratio			10	50		10	100	μV/V
A_{VOL}	Large signal voltage gain	$R_L \geq 600\Omega$, $V_O = \pm 10V$	50	100		25	100		V/mV
		Over temperature	25			15			V/mV
V_{OUT}	Output swing	$R_L \geq 600\Omega$	±12	±13		±12	±13		V
		$R_L \geq 600\Omega$ $V_S = \pm 18V$	±15	±16		±15	±16		V
R_{IN}	Input resistance		50	100		30	100		kΩ
I_{SC}	Output short circuit current			38			38		mA

NOTES

1. For NE5533/5533A/5534/5534A, $T_{MIN} = 0°C$, $T_{MAX} = 70°C$
2. For SE5534/5534A, $T_{MIN} = -55°C$, $T_{MAX} = +125°C$

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DESCRIPTION

The NE5537 monolithic Sample and Hold amplifier combines the best features of ion implanted JFET's with bipolar devices to obtain high accuracy, fast acquisition time, and low droop rate. This device is pin compatible with the LF198, and features a superior performance in droop rate and output drive capability. The circuit, shown in Figure 1 contains two operational amplifiers which function as a unity gain amplifier in the sample mode. The first amplifier has bipolar input transistors which gives the system a low offset voltage. The second amplifier has JFET input transistors to achieve low leakage current from the hold capacitor. A unique circuit design for leakage current cancellation using current mirrors gives the NE5537 a low droop rate at higher temperature. The output stage has the capability to drive a 2K load. The logic input is compatible with TTL, PMOS or CMOS logic. The differential logic threshold is 1.4V with the sample mode occurring where the logic input is high.

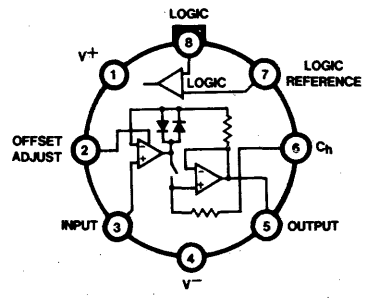
FEATURES

- **Operates from ±5V to ±18V supplies**
- **Hold leakage current 6pA @ T_j25°C**
- **Less than 10μs acquisition time**
- **TTL, PMOS, CMOS compatible logic input**
- **0.5mV typical hold step at C_h = 0.01μF**
- **Low input offset: 1MV (typical)**
- **0.002% gain accuracy with R_L = 2kΩ**
- **Low output noise in hold mode**
- **Input characteristics do not change during hold mode**
- **High supply rejection ratio in sample or hold**
- **Wide bandwidth**

Logic inputs on the 5537 are fully differential with low input current, allowing direct connection to TTL, PMOS, and CMOS. Differential threshold is 1.4V. The 5537 will operate from ±5V to ±18V supplies. It is available in an 8-lead TO-5 package.

PIN CONFIGURATION

T PACKAGE
Metal Can Package



TOP VIEW

ORDER PART NO.
NE/SE 5537-T

BLOCK DIAGRAM

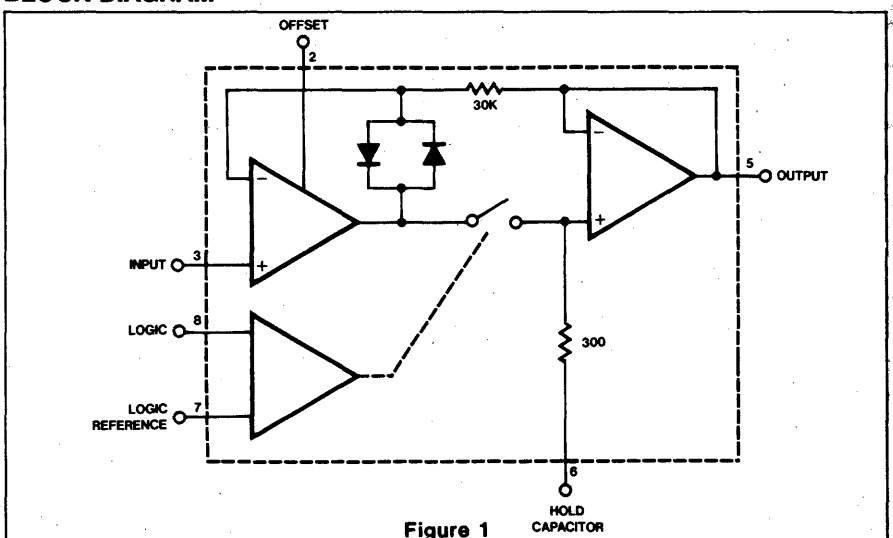
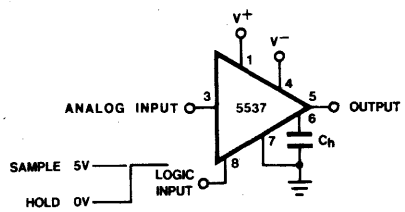


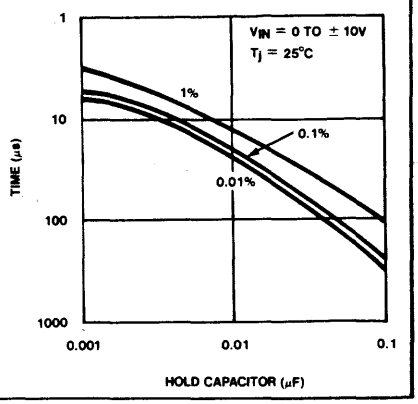
Figure 1

TYPICAL APPLICATIONS

TYPICAL CONNECTION



ACQUISITION TIME



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DESCRIPTION

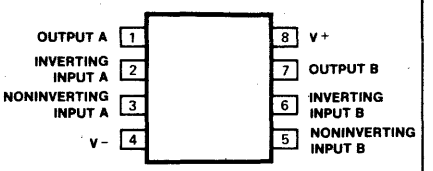
The 538/5538 are new generation operational amplifiers featuring high slew rates combined with improved input characteristics. Internally compensated for gains of 5 or larger, the SE538/SE5538 offer guaranteed minimum slew rates of 40V/μs or larger. Featuring 2mV max input offset voltage, the 538 is a single amplifier while the 5538 is a dual version. Industry standard pin out and internal compensation allow the user to upgrade system performance by directly replacing general purpose amplifiers, such as 748, 101A, 741, 747 and 1458.

FEATURES

- **2mV max input offset voltage**
- **60nA max input offset current**
- **Short circuit protected**
- **Offset null capability**
- **Large common mode and differential voltage ranges**
- **60V/μs slew rate (gain of +5, -4 min)**
- **6MHz gain bandwidth product (gain +5, -4 minimum)**
- **Internal frequency compensation (gain of +5, -4 minimum)**
- **Pin out: 538 same as 741 (single)**
  5538 same as 747, 1458 (dual)

PIN CONFIGURATIONS

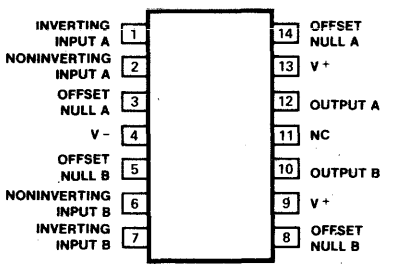
N PACKAGE



ORDER PART NO.

SE5538N, NE5538N

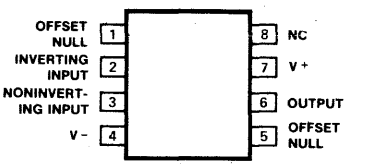
N-14, F PACKAGE



ORDER PART NO.

SE5538 N-14, F
NE5538 N-14, F

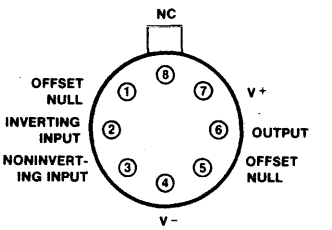
N PACKAGE



ORDER PART NO.

SE538N, NE538N

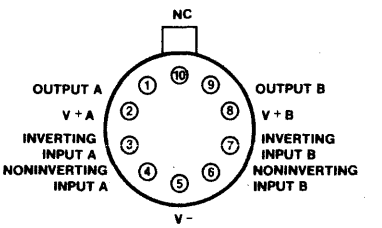
T PACKAGE



ORDER PART NO.

SE538T, NE538T

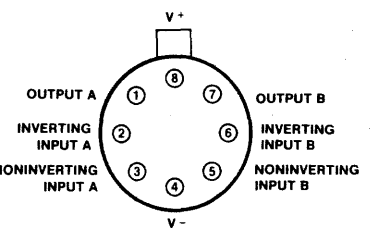
K PACKAGE



ORDER PART NO.

SE5538K, NE5538K

T PACKAGE



ORDER PART NO.

SE5538T, NE5538T

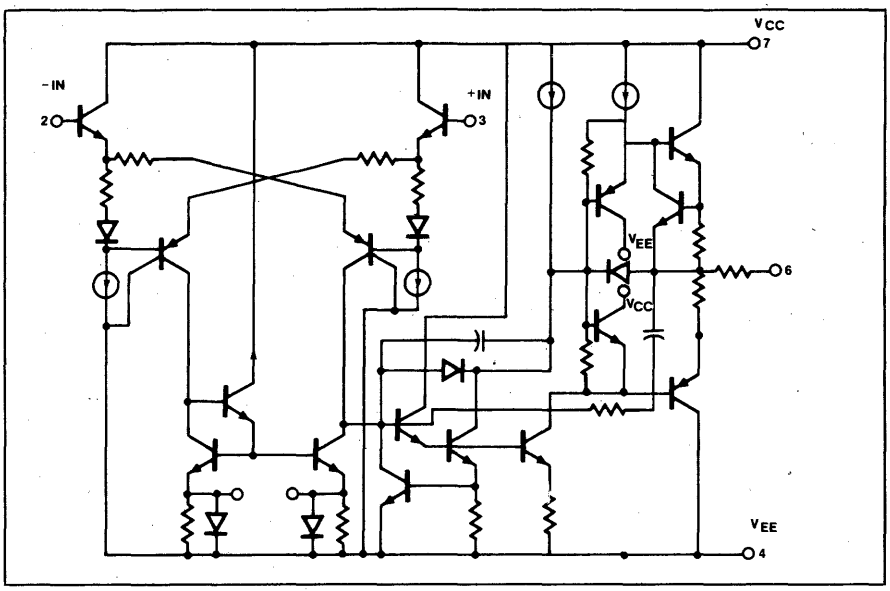
ABSOLUTE MAXIMUM RATINGS[1,2,3]

	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage		
	SE military grade	±22	V
	NE commercial grade	±18	V
P_D	Internal power dissipation F package	1000	mW
P_D	Internal power dissipation[1] N package	500	mW
P_D	Internal power dissipation[1] K, T package	800	mW
	Differential input voltage	±30	V
	Input voltage[2]	±15	V
	Operating temperature range		
	SE military grade	-55 to +125	°C
	NE commercial grade	0 to 70	°C
	Output short circuit[3]	indefinite	
	Storage temperature range	-65 to +150	°C
	Lead temperature (solder, 60sec.)	300	°C

NOTES

1. Rating applies for thermal resistances of 240°C/W and 150°C/W junction to ambient for N and K, T packages, respectively. Maximum chip temperature is 150°C.
2. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
3. Short circuit may be to ground or either supply. Rating applies to 125°C case temperature or 75°C ambient temperature.

EQUIVALENT SCHEMATIC (EACH AMPLIFIER)



DC ELECTRICAL CHARACTERISTICS

$T_A = 25°C$, $V_S = \pm 15V$ unless otherwise specified.

PARAMETER		TEST CONDITIONS	SE538/SE5538			NE538/NE5538			UNIT
			Min	Typ	Max	Min	Typ	Max	
V_{OS}	Input offset voltage	$R_S \leq 10k\Omega$		0.7	2.0		2.0	5.0	mV
V_{OS}	Input offset voltage	$R_S \leq 10k\Omega$, over temp.			3.0			6.0	mV
ΔV_{OS}	Input offset voltage drift	$R_S = 0\Omega$, over temp.		3.0	15		6.0		$\mu V/°C$
I_{OS}	Input offset current			5	10		15	40	nA
I_{OS}	Input offset current	Over temp.			20			80	nA
I_B	Input current			45	60		65	150	nA
I_B	Input current	Over temp.			100			200	nA
V_{CM}	Input common mode voltage range		±12	±13		±12	±13		V
C_{MRR}	Common mode rejection ratio	$R_S \leq 10k\Omega$, over temp.	70	90		70	90		dB
P_{SRR}	Power supply rejection	$R_S \leq 10k\Omega$, over temp.		30	150		30	150	$\mu V/V$
R_{IN}	Input resistance		3	10		1	6		MΩ
A_{VOL}	Large signal voltage gain	$R_L \geq 2k\Omega$, $V_{OUT} = \pm 10V$	50	200		50	200		V/mV
A_{VOL}	Large signal voltage gain	Over temp., $R_L \geq 2k\Omega$, $V_{OUT} = \pm 10V$	25			25			V/mV
V_{OUT}	Output voltage	Over temp., $R_L \geq 2k\Omega$	±10	±13		±10	±13		V
V_{OUT}	Output voltage	Over temp., $R_L \geq 10k\Omega$	±12	±14		±12	±14		V
I_{CC}	Supply current	Per amplifier		2	3		2	3	mA
I_{CC}	Supply current	Over temp., per amplifier		2.2	3.6		2.2		mA
P_D	Power dissipation	Per amplifier		60	90		60	90	mW
P_D	Power dissipation	Over temp., per amplifier		66	108		66		mW
I_{SC}	Output short circuit current			25			25		mA
R_{OUT}	Output resistance			100			100		Ω

NOTE

Temperature Range
SE Types $-55°C \leq T_A \leq 125°C$
NE Types $0°C \leq T_A \leq 70°C$

OBJECTIVE SPECIFICATION NE/SE5551/2/3/4/5-N,T

DESCRIPTION

The NE/SE5551, 2, 3, 4, 5 are dual polarity tracking regulators designed to produce balanced or unbalanced output voltages from 5 to 20 volts with up to 300 mA output current. Similar in specifications to the 78MXX and 79MXX fixed regulators, the 5551 series can be continuously adjusted, balanced or unbalanced. Standard fixed voltages available are ±5, ±6, ±12, ±15, and +5, -12 volts. Employing current limiting and thermal shutdown protection, these dual polarity regulators are ideal for local on-card regulation.

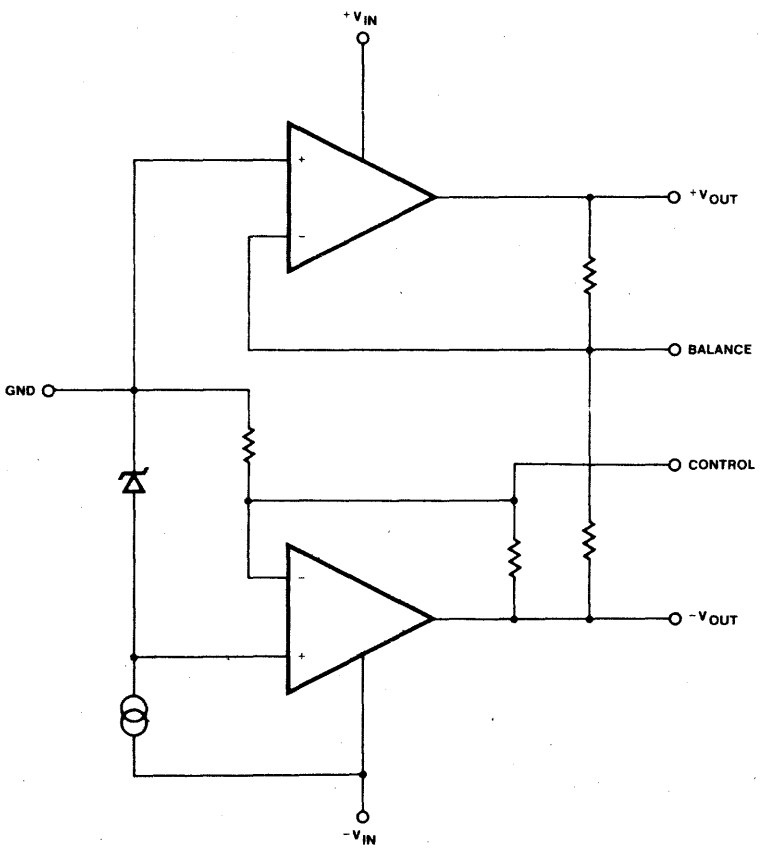
FEATURES

- **Output current to 300mA**
- **Internally current limited**
- **Thermal overload protected**
- **Input voltage to ±32V**
- **Output balance 1% typ.**
- **External balance control**
- **Continuously adjustable from 5 to 20 volts, balanced or unbalanced**
- **No external components required**
- **Short circuit current 400mA**
- **Heat sink available for increased power dissipation**

ABSOLUTE MAXIMUM RATINGS

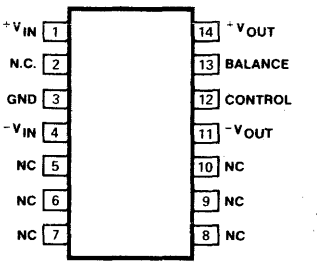
PARAMETER	RATING	UNIT
V_{IN} input voltage	±32	V
T_{SG} storage temperature	-65 to +150	°C
T_J operating junction temperature		
NE5551,2,3,4,5	0 to +125	°C
SE5551,2,3,4,5	-55 to +150	°C
Lead temperature 10 sec.	300	°C

BLOCK DIAGRAM



PIN CONFIGURATIONS

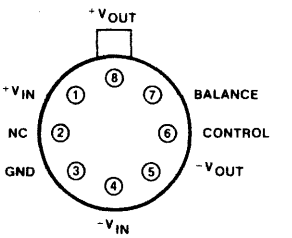
N PACKAGE



ORDER PART NUMBERS

VOLTAGE	PART NO.
±5V	SE/NE5551N
±6V	SE/NE5552N
±12V	SE/NE5553N
±15V	SE/NE5554N
+5, -12V	SE/NE5555N

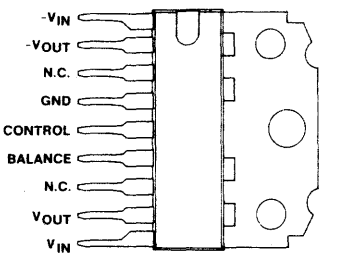
T PACKAGE



ORDER PART NUMBERS

VOLTAGE	PART NO.
±5V	SE/NE5551T
±6V	SE/NE5552T
±12V	SE/NE5553T
±15V	SE/NE5554T
+5, -12V	SE/NE5555T

U PACKAGE



ORDER PART NUMBERS

VOLTAGE	PART NO.
±5V	SE/NE 5551 U
±6V	SE/NE 5552 U
±12V	SE/NE 5553 U
±15V	SE/NE 5554 U
+5,-12V	SE/NE 5555 U

Power dissipation (without heat sink)
T Package
N Package
U Package

Signetics LINEAR

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DESCRIPTION

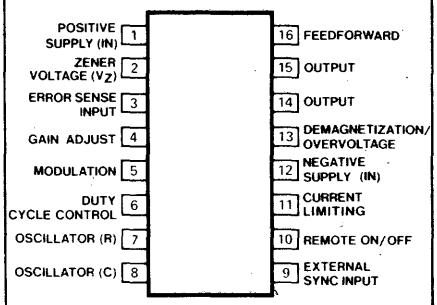
The NE/SE5560 is a control circuit for use in switched mode power supplies. This single monolithic chip incorporates all the control and housekeeping (protection) functions required in switched mode power supplies, including an internal temperature compensated reference source, internal Zener reference, sawtooth generator, pulse width modulator, output stage and various protection circuits.

FEATURES

- **Stabilized power supply**
- **Temperature compensated reference source**
- **Sawtooth generator**
- **Pulse width modulator**
- **Remote on/off switching**
- **Current limiting**
- **Low supply voltage protection**
- **Loop fault protection**
- **Demagnetization/overvoltage protection**
- **Maximum duty cycle adjustment**
- **Feed forward control**
- **External synchronization**

PIN CONFIGURATION

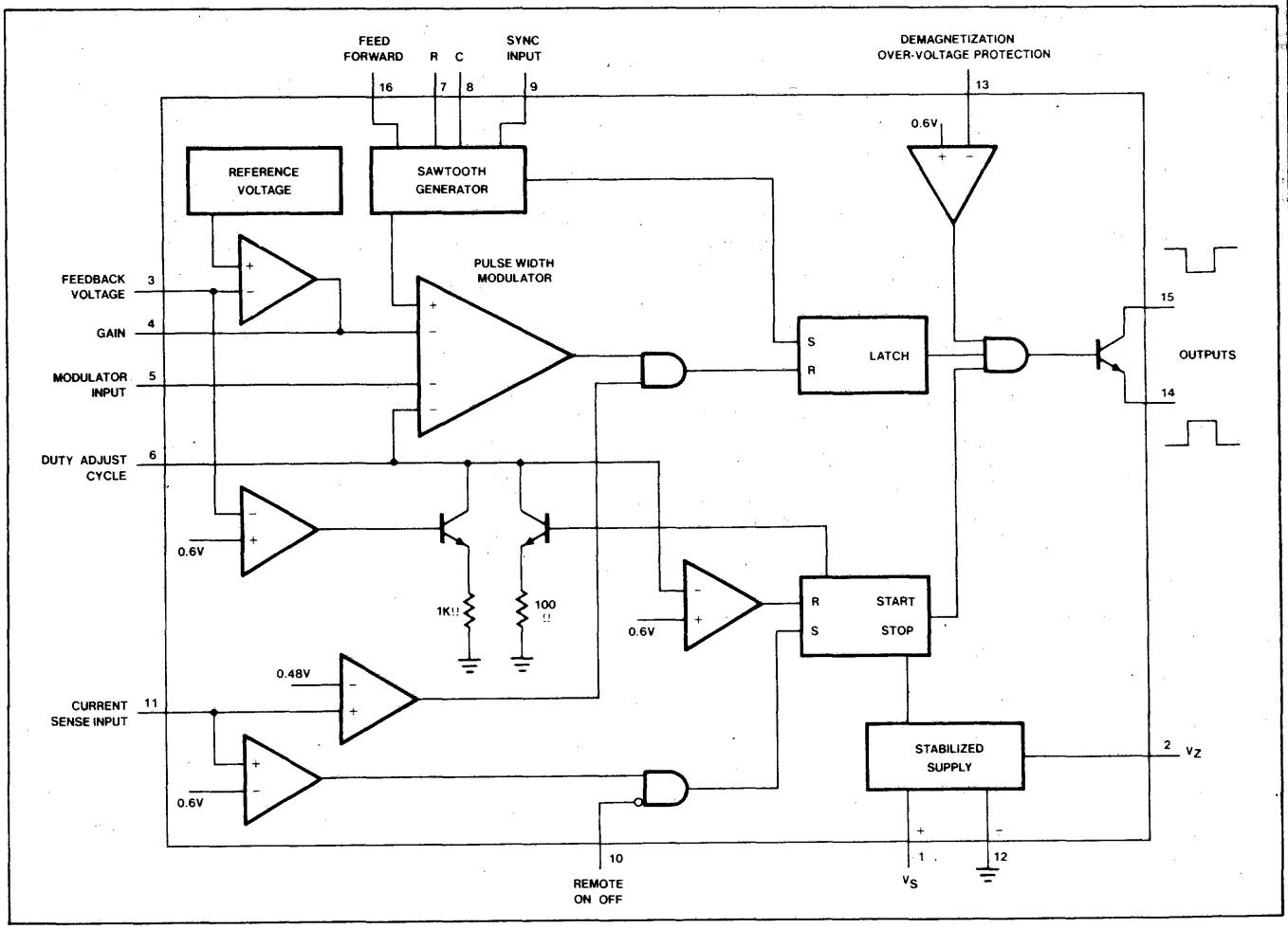
F,N PACKAGE



ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
Supply voltage (Voltage sourced)	+18	V
Supply current (Current sourced)	30	mA
Output current	40	mA
Operating temperature range	−55 to +125	°C
Storage temperature range	−65 to +150	°C

BLOCK DIAGRAM



8X08-F,XA

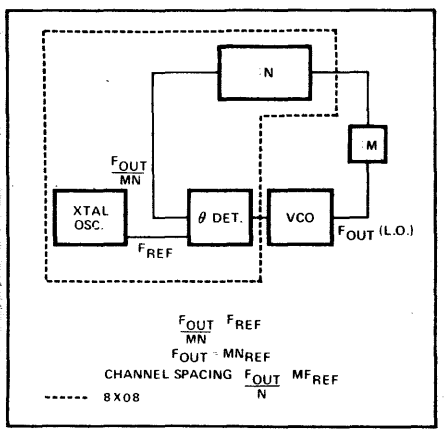
DESCRIPTION

This LSI integrated circuit performs the digital control functions required for generating AM/FM radio frequency local oscillator signals using digital phase locked loop techniques. By the use of low power Schottky and ECL technologies on the same substrate it is possible to operate at 80MHz input frequencies with an average system power of 1.6mW per gate typical.

FEATURES

- **80MHz input frequency**
- **ECL prescaler**
- **LS process**
- **Single 5V supply**
- **Power dissipation—600mW (max)**
- **External components—**
  - **1 crystal**
  - **2 capacitors**

PHASE LOCKED LOOP BLOCK DIAGRAM



PHASE LOCKED LOOP PRINCIPLES

Digital phase locked loops are comprised of 4 basic building blocks: A fixed reference frequency generator (crystal oscillator and divider), a phase comparator, a voltage controlled oscillator (VCO) and a programable counter (÷N).

In cases where very high frequencies must be generated, a fixed prescaler (÷M) is employed to divide the local oscillator frequency down to a frequency compatible with the programmable counter. Fout from the VCO is divided down by the prescaler and programmable counters and compared to the reference frequency by the phase detector. If $\frac{Fout}{MN}$ is not equal to Fref in phase and frequency, the phase detector generates a signal which causes the VCO frequency to increase or decrease until Fref = $\frac{Fout}{MN}$. When this occurs, the local oscillator is essentially as stable as the crystal reference oscillator.

The local oscillator frequency (Fout) is changed by programming a different number into the programmable counter. The distance between discrete frequencies or the channel spacing is determined by the reference frequency.

For the AM/FM circuit, up to 200 channels are possible with selectable channel spacing of 10kHz for AM operation and 2000 channels at 100kHz for FM operation.

AM/FM Frequency Synthesizer Circuit Description

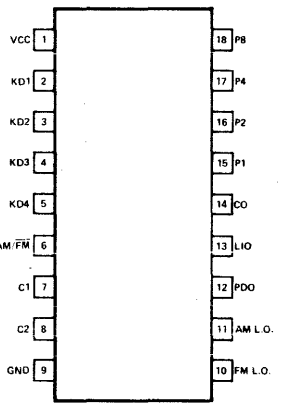
The frequency synthesizer circuit logic diagram is shown below. Following is a description of each of the major blocks.

Programmable Counter

The programmable counter consists of 3 stages of decade counter plus a divide by 1 or 0 counter to divide by numbers up to 1999. BCD programming data is presented to the dividers in parallel form, one digit at a time. Parallel data is strobed into internal latches via strobe signals; one strobe for each digit. A ÷ 5 80MHz ECL prescaler precedes the programmable counter for FM operation. This prescaler plus an external 160MHz ÷ 2 flip-flop provide a ÷ 10 160MHz prescaler (÷M) function to scale the programmable counter input frequency down to 16MHz maximum. A logic control circuit bypasses the ÷M prescaler and the first decade counter for AM operation. By this technique, the channel spacing is programmable to 10kHz for AM operation and 100kHz for FM operation.

PIN CONFIGURATION

F, XA PACKAGE



VCO

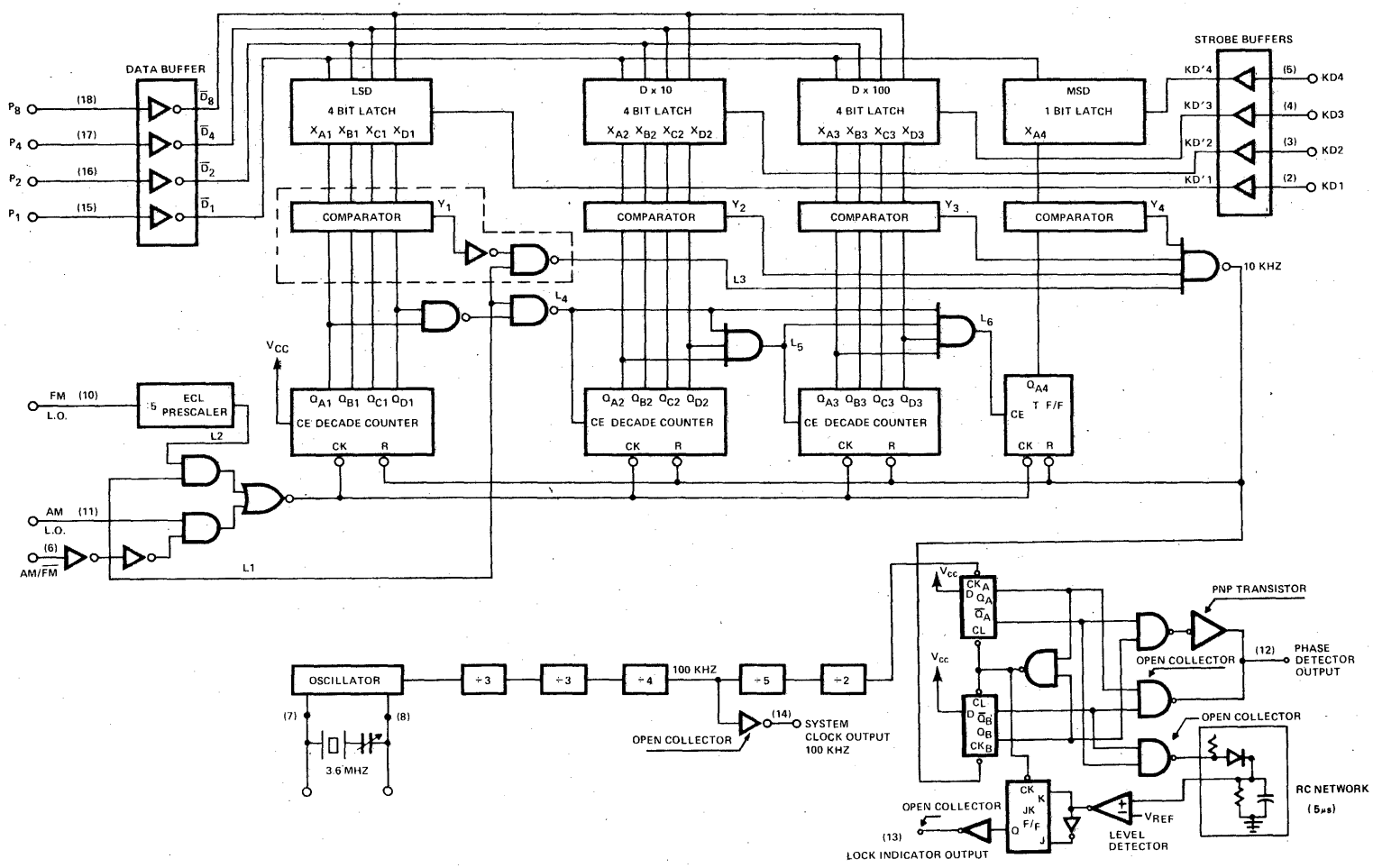
An externally provided integrator and voltage controlled oscillator must be provided to perform the complete frequency synthesizer function. The integrator converts the pulses that come from the phase detector into a dc signal that controls the output frequency of the voltage controlled oscillator. It is in the integrator part of the circuit that the critical loop constants are determined. The voltage controlled oscillator is normally a LC tuned oscillator with varactor diode tuning that is controlled by the dc signals from the integrator. In this case, two are required, one for the AM band and one for the FM band. The FM oscillator output must be +5V ECL compatible while the AM oscillator must be TTL compatible.

RECOMMENDED OPERATING CONDITIONS

PARAMETER		LIMITS			UNIT
		Min	Typ	Max	
T_A	Operating free air temperature	-40		+85	°C
V_{CC}	Supply voltage	4.75	5.0	5.25	V
	Max input voltage data, strobe			16	V
	Max AM local oscillator input operating frequency (Pin 11)		20		MHz
	Max FM local oscillator input operating frequency (Pin 10)		100	80	MHz
	Maximum reference frequency oscillator operating frequency		6		MHz

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LOGIC DIAGRAM



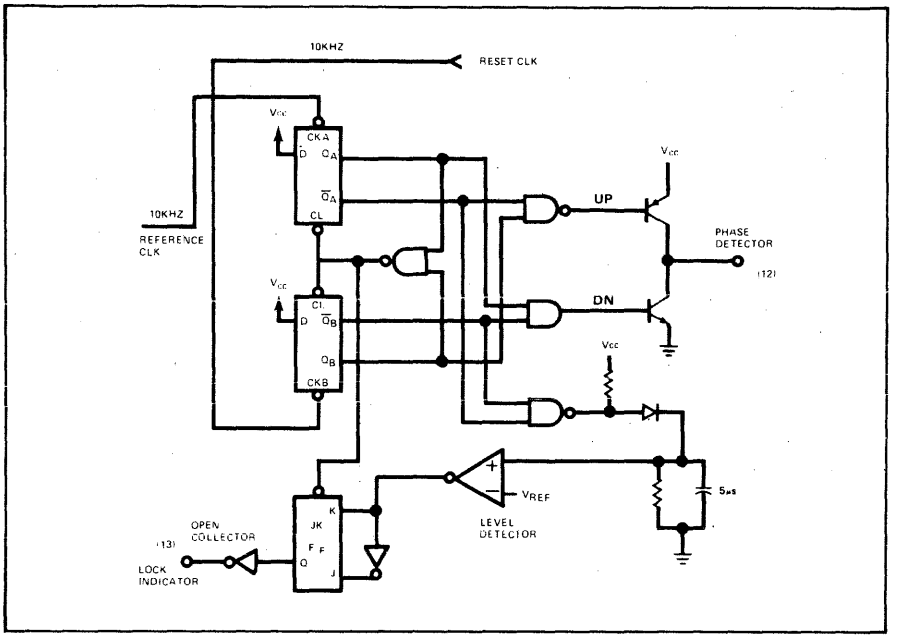
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Phase Detector Circuit

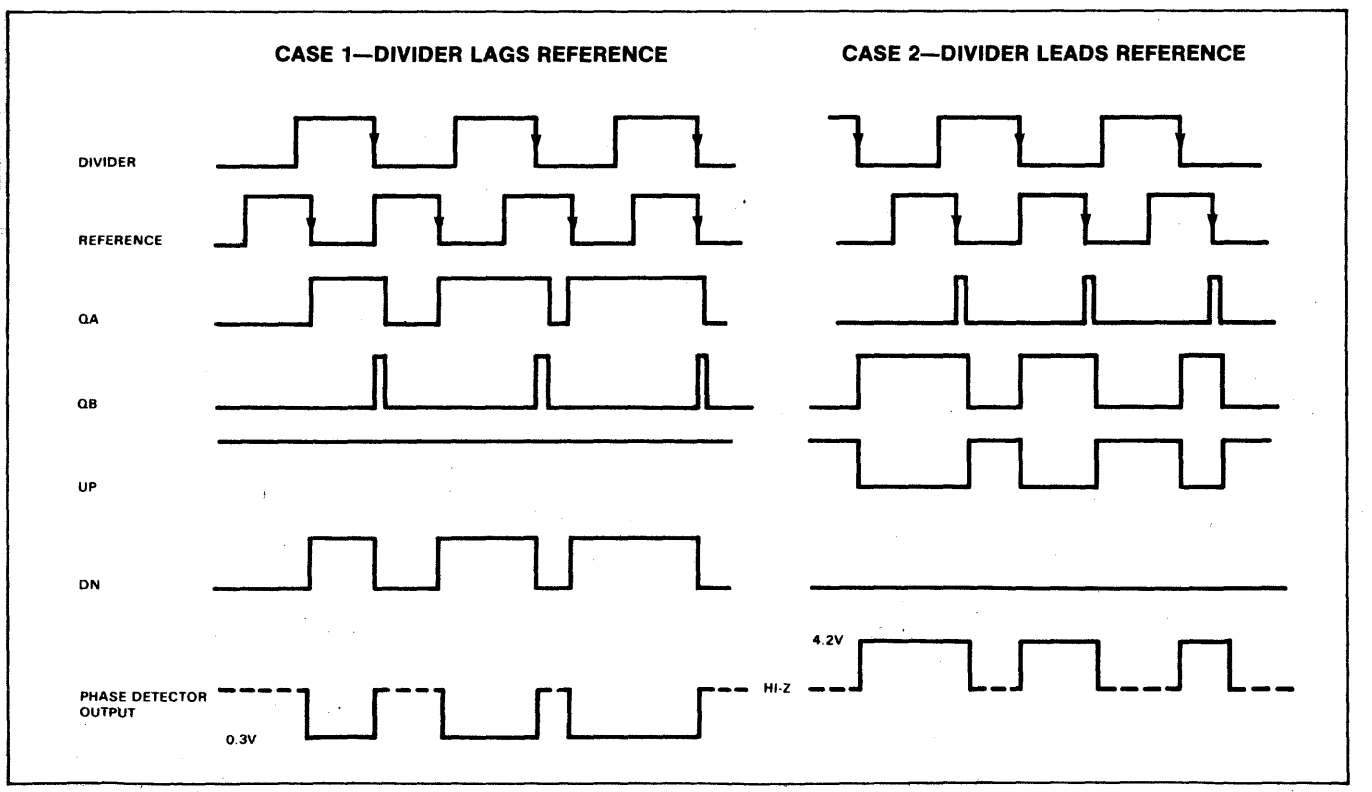
The phase detector is a digital edge-detecting device that provides an output three-state signal that is in a high impedance state when the 2 input signals are equal in phase and/or frequency. The output of the phase detector is a series of pulses that swing from the high impedance state to .3V typical or from the high impedance state to 4.2V typical. If the positive edge of the divider input leads the reference, the pulses will go to 4.2V. If it lags they will go to .3V.

The width of the output pulses is a function of the time between the positive edges (phase) of the 2 signals. An example of the operation of the device is shown where the reference signal is twice the frequency of the divider signal and has a phase lead of 270°. The output pulses are converted to a dc signal by integrating amplifiers causing the output frequency of the voltage controlled oscillator to increase or decrease (increase in this case) until the divider output and the reference output are equal in phase and frequency.

PHASE DETECTOR CIRCUIT



DIVIDER REFERENCE



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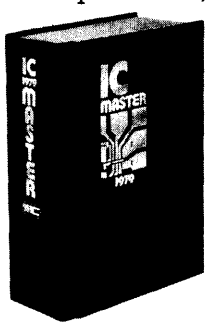
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SG1524/2524/3524 REGULATING PULSE WIDTH MODULATOR

DESCRIPTION

This monolithic integrated circuit contains all the control circuitry for a regulating power supply inverter or switching regulator. Included in a 16-pin dual-in-line package is the voltage reference, error-amplifier, oscillator, pulse width modulator, pulse steering flip-flop, dual alternating output switches and current limiting and shut-down circuitry. This device can be used for switching regulators of either polarity, transformer coupled DC to DC converters, transformerless voltage doublers and polarity converters, as well as other power control applications. The SG1524 is specified for operation over the full military temperature range of −55° C to +125° C, while the SG2524 and SG3524 are designed for commercial applications of 0° C to +70° C.

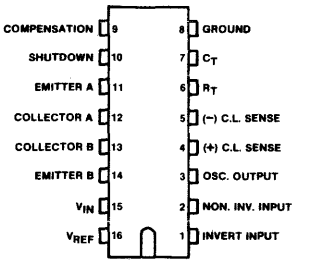
FEATURES

- **Complete PWM power control circuitry**
- **Single ended or push-pull outputs**
- **Line and load regulation of 0.2%**
- **1% maximum temperature variation**
- **Total supply current less than 10 mA**
- **Operation beyond 100kHz**

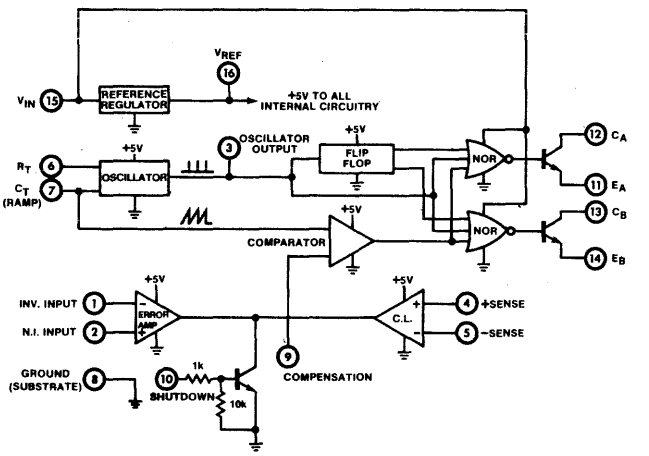
ABSOLUTE MAXIMUM RATINGS

Input Voltage	40V
Output Current (each output)	100 mA
Reference Output Current	50 mA
Oscillator Charging Current	5 mA
Power Dissipation (package limitation) Derate above 25° C	1000 mW 8mW/° C
Operating Temperature Range SG1524 SG2524/SG3524	 −55° C to +125° C 0° C to +70° C
Storage Temperature Range	−65° C to +150° C

CONNECTION DIAGRAMS



BLOCK DIAGRAM



SG1627/3627 DUAL HIGH-CURRENT OUTPUT DRIVER

DESCRIPTION

The SG1627 and SG3627 devices are monolithic, high-speed driver integrated circuits designed to interface digital control logic with high current loads. Each device contains two independent drivers which will either source or sink up to 500 mA of current. The sink transistor is designed as a saturating switch while the source transistor can be used either as a switch or as a constant current generator with external resistor programming.

Each half of this device contains both inverting and noninverting inputs which have two volt thresholds for high noise immunity. Either input can be used alone to switch the output, or one input can be strobed with the other. These units have been designed to directy interface with the SG1524 Regulating Pulse Width Modulator Circuit.

These devices are supplied in ceramic 16-pin D.I.L. packages. The SG1627 is specified for operation over a −55° C to +125° C temperature range while the SG3627 is intended for industrial applications of 0° C to +100° C.

FEATURES

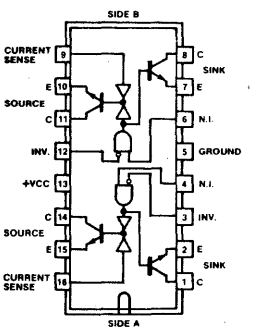
- **Two independent driver circuits**
- **Outputs will source or sink currents to 500 mA**
- **100 nSec response time**
- **Full compatibility with SG1524 PWM circuit**
- **Constant current drive capability**
- **Two volt threshold for high noise immunity**
- **Source and sink can be separated for complementary outputs**

ABSOLUTE MAXIMUM RATINGS

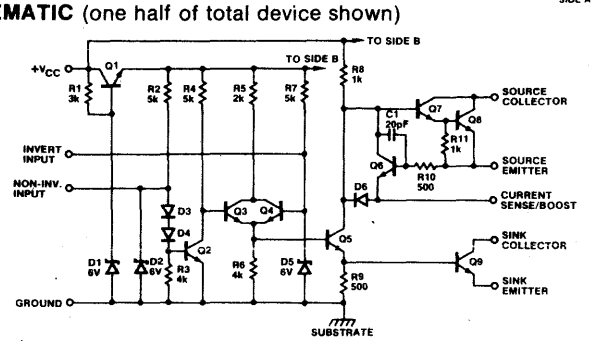
Supply Voltage, VCC	30V
Output Collector Voltage	30V
Source or Sink Current	500 mA
Input Voltage	5.5V
Input Current	10 mA
Avg. Total Power Dissipation (Note 1) Derate Above 55° C	1000 mW 10 mW/° C
Operating Temperature Range SG1627 SG3627	 −55° C to +125° C 0° C to +100° C
Storage Temperature Range	−65° C to +150° C

Note 1: Total power dissipation is the sum of the control logic power plus the power of each source and sink output transistor, factored for duty cycle.

CONNECTION DIAGRAMS



SCHEMATIC (one half of total device shown)



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SG1543/2543/3543 POWER SUPPLY OUTPUT SUPERVISORY CIRCUIT

DESCRIPTION

This monolithic integrated circuit contains all the functions necessary to monitor and control the output of a sophisticated power supply system. Over-voltage (O.V.) sensing with provision to trigger an external SCR "crowbar" shutdown; and under-voltage (U.V.) circuit which can be used to monitor either the output or to sample the input line voltage; and a third op amp/comparator usable for current sensing (C.L.) are all included in this IC, together with an independent, accurate reference generator.

Both over and under voltage sensing circuits can be externally programmed for minimum time duration of fault before triggering. All functions contain open collector outputs which can be used independently or wire-or'ed together, and although the SCR trigger is directly connected only to the over voltage sensing circuit, it may be optionally activated by any of the other outputs, or the outputs from additional external comparators like the SG139/239/339 for multiple-output monitoring. The O.V. circuit also includes an optional latch and external reset capability.

The current sense circuit may be used with external compensation as a linear amplifier or as a high-gain comparator. Although nominally set for zero input offset, a fixed threshold may be added with an external resistor. Instead of current limiting, this circuit may also be used as an additional voltage monitor.

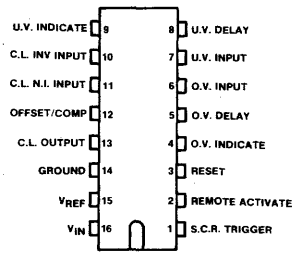
The reference generator circuit is internally trimmed to eliminate the need for external potentiometers and the entire circuit may be powered directly from either the output being monitored or from a separate bias voltage.

The SG1543 is specified for operation over the full military temperature range of −55° C to +125° C, while the SG2543 and SG3543 are designed for commercial applications of 0° C to +70° C.

FEATURES

- **Over-voltage, under-voltage, and current sensing circuits all included**
- **Reference voltage trimmed to 1% accuracy**
- **SCR "Crowbar" drive of 200 mA**
- **Programmable time delays**
- **Open-collector outputs and remote activation capability**
- **Total standby current less than 10 mA**

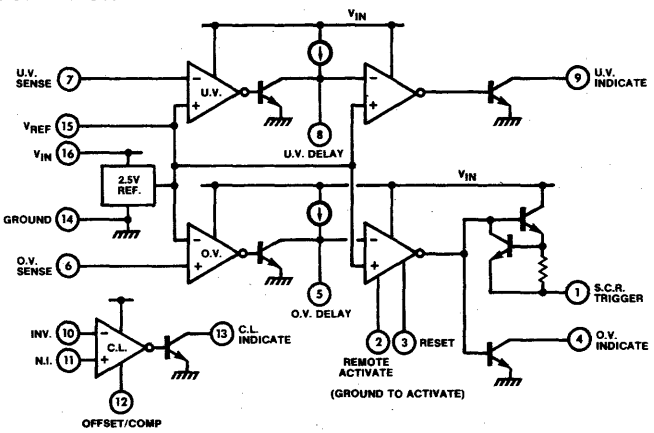
CONNECTION DIAGRAMS



ABSOLUTE MAXIMUM RATINGS

Input Supply Voltage	40V
Sense Inputs	VIN −1.5V
SCR Trigger Current	300 mA
Indicator Output Voltage	40V
Power Dissipation (Package Limitation) Derate Above 25° C	1000 mW 8.0 mW/° C
Operating Temperature Range SG1543 SG2543/3543	 −55° C to +125° C 0° C to +70° C
Storage Temperature Range	−65° C to +150° C

BLOCK DIAGRAM



SG1503/2503/3503 PRECISION 2.5 VOLT REFERENCE

DESCRIPTION

This monolithic integrated circuit is a fully self-contained precision voltage reference generator, interally trimmed for ±1% accuracy. Requiring less than 2 mA in quiescent current, this device can deliver in excess of 10 mA with total load and line induced tolerances of less than 0.5%. In addition to voltage accuracy, internal trimming achieves a temperature coefficient of output voltage of typically 10 ppm/° C. As a result, these references are excellent choices for application to critical instrumentation and D to A converter systems. The SG1503 is specified for operation over the full military temperature range of −55° C to +125° C, while the SG2503 and SG3503 are designed for commercial applications of 0° C to +70° C.

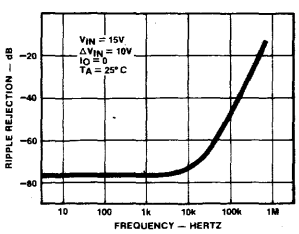
FEATURES

- **Output voltage trimmed to ±1%**
- **Input voltage range of 4.5 to 40V**
- **Temperature coefficient of 10 ppm/° C**
- **Quiescent current typically 1.5 mA**
- **Output current in excess of 10 mA**
- **Interchangeable with MC1503 and AD580**

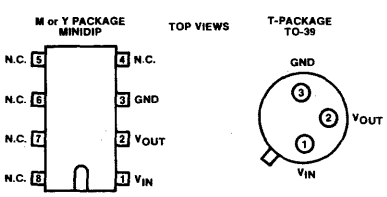
ABSOLUTE MAXIMUM RATINGS

Input Voltage	4.5 — 40V
Power Dissipation Derate Over 25° C	600 mW 4.8 mW/° C
Operating Temperature Range SG1503 SG2503/3503	 −55° C to 125° C 0° C to +70° C
Storage Temperature Range	−65° C to +150° C

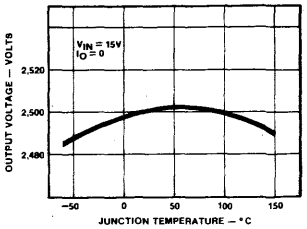
RIPPLE REJECTION



CONNECTION DIAGRAMS



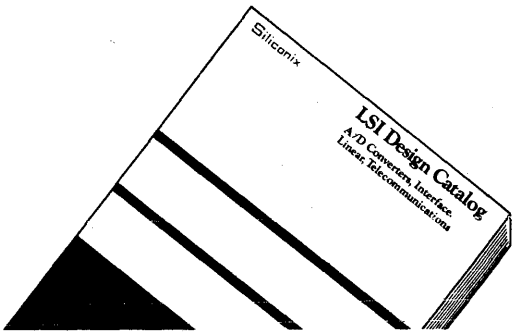
OUTPUT VOLTAGE vs. TEMPERATURE



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Siliconix
incorporated
2201 Laurelwood Road
Santa Clara, CA 95054
(408) 988-8000
TWX: 910-338-0227

Product Selector Guide



Send for Complete Information in the New LSI Design Catalog

PART NO.	FUNCTION/APPLICATION				
	A/D CONVERTERS, INDEX 1				
	DIGITS	SCALES	RESOLUTION	BASIC ACCURACY	
LD110/LD111	3 1/2	2 V, 200 mV	100 μV	0.05% ±1 count	
LD110/LD111A	3 1/2	2 V, 200 mV, 20 mV (2 mV with external preamp)	10 μV (1 μV with external preamp)	0.02% ±1 count	
LD111/LD114	3 1/2	2 V, 200 mV	100 μV	0.05% ±1 count	
LD120/LD121	4 1/2	2 V, 200 mV (20 mV with external preamp)	10 μV (1 μV with external preamp)	0.005% ±1 count	
LD130	±3	1.0 V	1 mV	0.1% ±1 count	
LD131	±3 1/3	1.500 V	1 mV	0.1% ±1 count	

	LINEAR, INDEX 2	
L144	**Triple Op Amp**/Low power amplification, voltage comparators, active filters, battery powered circuits	
L161	**Quad Comparator**/Low power voltage comparator, level detectors, CMOS line receivers, oscillators, phase comparators, battery powered circuits	
L911	**Detector Circuit**/Battery and line operated heat sensors, sound level detectors, smoke detectors, gas detectors	
LM3909	**LED Flasher**/Micropower indicators, emergency locators, electronic jewelry, warning indicators, oscillators, timers, micropower actuators	
SM110	**Ionization Smoke Detector**/Complete system block including direct interface to ionization chambers, low battery threshold sensing circuitry and output drive	
T100/T300	**Transducer Preamplifier**/Microphone, electret, condenser, ceramic, strain gauges, self-contained source follower amplifier	

	INTERFACE, INDEX 3	
D139	**Universal Logic Interface Circuit**/Level shifts TTL or CMOS logic input to any logic output at high speed	
D140	**Hex Digit Driver**/Ideal for low voltage LED display systems requiring very small switch losses	
DF411	**Decodes Four Digit Multiplexed BCD to LCD Display Driver**/Decodes up to 4 digits of multiplexed BCD information and derives the AC signals needed to drive a 4 digit LCD display	

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(Continued)

PART NO.	FUNCTION/APPLICATION	
	TELECOMMUNICATIONS, INDEX 4	
DF320/321/322	**Loop Disconnect Dialer (push button to conventional pulse dialer)**/ Allows conversion of telephone systems without touch-tone® capability to use a push button phone	
DF331/332	**μ255-Law CODEC**/Converts present analog voice channels into a PCM digital format with companding A to D characteristics and back to analog signals (coder-decoder set)	
DF341/342	**A-Law CODEC**/Same as DF331/332 except this part follows the Telecommunications Industry A-Law for companding	
	TIMING, INDEX 5	
DF213/214	**Stopwatches**/Two timing modes available: 59:59:99 minutes and seconds, 99.999 minutes. Has multiple split timing available.	
DF215	**Dual Set Point Timer**/Two programmable count points that determine time interval lengths. Two outputs to control systems for the interval length, includes seven segment LED output drivers.	
DF216	**Down-Up Counter**/Keyboard entry programs time interval, down counts to zero, outputting end of interval signal including timing the overtime length	

Touch-tone® is a registered trademark of Western Electric Co.

©IC MASTER 1979

CMOS μ-255 law companding converter set *designed for . . .*

- **Telecommunications Channel Banks**
- **Servo Control Systems**
- **Microprocessor Interface**
- **Remote Data Acquisition Systems**
- **Audio Delay Lines**

BENEFITS

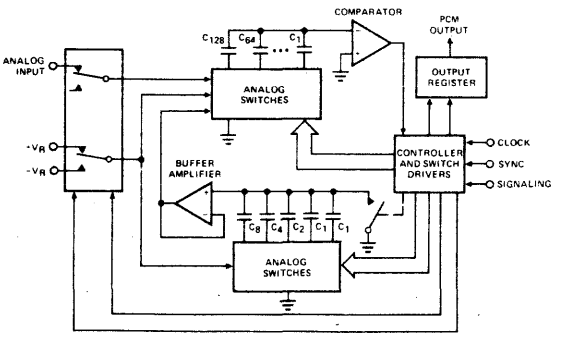
- Minimizes System Power Requirements
- Reduces External Component Requirements
- Reduces System Costs
- Easily Interfaced
- Eliminates Channel Crosstalk Problems
- Eliminates External Signalling Logic
- No External Zero Code Suppression Required
- Reduced System Noise Problems
- No External Sample and Hold or MUX Required
- No Additional Logic Required for Extended Bandwidth Applications
  - 3.5 to 9 KHz Bandwidth Possible With Clock Frequency From 1.25 to 3.0 MHz

DESCRIPTION

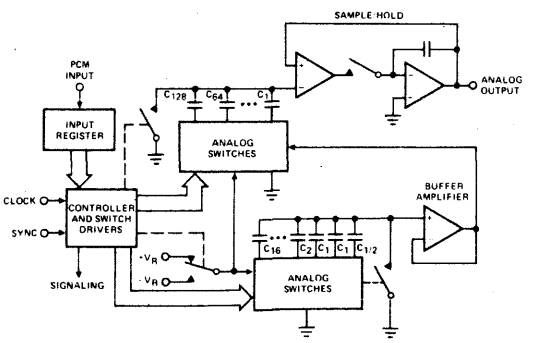
The DF331 (coder) is an analog-to-digital converter which has a transfer characteristic conforming to the telecommunication industry μ-255 law. Its counterpart, the DF332 or DF334 (decoder) is a digital-to-analog converter which also conforms to the μ-255 law.

Together the DF331 and DF332 or DF331 and DF334 form a CODEC (coder-decoder set) which is designed to meet the needs of the telecommunications industry for per channel voice frequency CODECs used in PCM Channel Bank and PBX systems. Digital output and input of the coder and decoder is in serial format. Actual transmission and reception of 8-bit data words containing the analog information is typically done at a 1.544 megabit/sec rate with analog signal sampling occurring at an 8 kHz rate. A sync pulse input pin is provided for synchronizing transmission and reception of multi-channel information being multiplexed over a single transmission line. The DF332 and DF334 differ in the output device for the A/B signal output pins, refer to the Functional Description.

FUNCTIONAL BLOCK DIAGRAMS



DF331

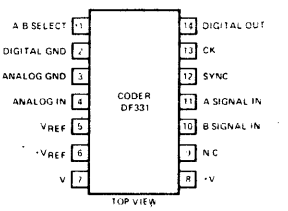


DF332, DF334

Figure 1

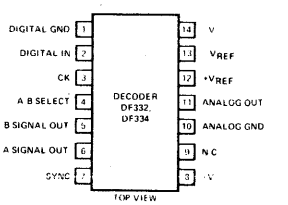
PIN CONFIGURATIONS

Dual In-Line Package



ORDER NUMBER: DF331CJ

Dual In-Line Package



ORDER NUMBER: DF332CJ, DF334CJ

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ABSOLUTE MAXIMUM RATINGS

V_{in} (Digital Inputs) . . . $-0.3\ V, \leq V_{in} \leq +V + 0.3\ V$
V_{in} (Analog Inputs) . . . $-V - 0.3\ V, \leq V_{in} \leq +V + 0.3\ V$
$+V$ . . . . . $0 \leq +V \leq 11\ V$
$-V$ . . . . . $-11\ V \leq -V \leq 0$
$+V_{ref}$ . . . . . $-V \leq +V_{ref} \leq +V$
$-V_{ref}$ . . . . . $-V \leq -V_{ref} \leq +V$

V_O (Digital Output) DF331, DF334 . . . . $V_O \leq 15\ V$
$V_{A/B}$ Signal Out DF332 . . . . . $V_O \geq -7.5\ V$
Operating Temperature . . . . . 0 to 70°C
Storage Temperature . . . . . −55 to +125°C
Power Dissipation . . . . . 450 mW
Derate 6.5 mW/°C above 25°C

ELECTRICAL CHARACTERISTICS

All DC parameters are 100% tested at 25°C. Lots are sample-tested for AC parameters to assure conformance with specifications.

		Characteristic		$T_A = 25°C$ Min	Typ	Max	Unit	Test Conditions, See Note 2 Clock = 1.544 MHz, Sample Rate = 8 KHz, $+V = 7.5\ V, -V_{ref} = -3.0\ V, -V = -7.5\ V,$ $+V_{ref} = 3.0\ V, R_L = 820\ \Omega, C_L = 12.5\ pF$
DC Characteristics DF331 (Coder)								
1	INPUTS	I_{in} (Analog)	Analog Input Current		0.5		mA	See Note 3
2		I_{inL} (Clock)	Clock Input Low Current		−0.1	−100	nA	$V_{IN} = 0$
3		I_{inL} (Sync)	Sync Input Low Current		−0.1	−100		
4		I_{inH} (Clock)	Clock Input High Current		0.1	100		$V_{IN} = 7.5\ V$
5		I_{inH} (Sync)	Sync Input High Current		0.2	100		
6		R_{in} (Analog)	Analog Input Series Resistance		1		KΩ	
7		C_{in} (Analog)	Analog Input Series Capacitance		200		pF	
8	OUT	V_{offset}	Analog Input Offset Voltage		5	10	mV	
9		C_o (Digital)	Digital Output Capacitance		3		pF	$V_O = 7.5\ V$
10		V_{OL}	Digital Output Low Voltage		0.3	0.5	V	$I_{OL} = 3\ mA$
11		V_{OH} (max)	Digital Output High Voltage			12		$I_{OH} = 10\ \mu A$
12	SUPPLY	I^+	Positive Supply Current		4	6	mA	Clock = 1.544 MHz Sample Rate = 8 KHz
13		I^-	Negative Supply Current		−3	−6		
14			Supply Tolerance		±10		%	
15		I_{ref}^+	Positive Reference Current		3.5		μA	Average Current — See Note 3
16		I_{ref}^-	Negative Reference Current		−3.5			
AC Characteristics DF331 (Coder)								
17		$\|t_{ds}\|$	Sync to Clock Delay Time			100	ns	See Figure 2
18		$t_{d(on)}$	Digital Output to Sync Delay Time		75	130		
19		$t_{d(off)}$	Digital Output to Sync Delay Time		165	220		
20		t_{dbr}	Digital Output to Clock Delay Time		65	130		
21		t_{dbf}	Digital Output to Clock Delay Time		70	130		
22		t_{fo}	Digital Output Fall Time		65	130		$C_L = 100\ pF$
23		t_{ro}	Digital Output Rise Time		175	250		
24		t_{ss} (min)	A/B Signaling Input Setup Time			200		See Figure 4
25		t_{scs} (min)	A/B Select Setup Time			1000		
26		DC_c	Clock Duty Cycle	30		70	%	

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ELECTRICAL CHARACTERISTICS (Cont'd)

All DC parameters are 100% tested at 25°C. Lots are sample-tested for AC parameters to assure conformance with specifications.

		Characteristic			T_A = 25°C Min	Typ	Max	Unit	Test Conditions, See Note 2 +V = 7.5 V, V = 7.5 V, V_{ref} = 3.0 V, V_{ref} = 3.0V, Clock = 1.544 MHz, Sync = 8 KHz Period, 8 Clock Pulses Wide
DC Characteristics DF332, DF334 (Decoder)									
1	IN	I_{inL} (Logic)	Digital Inputs Low Current			0.1	100	nA	V_{IN} = 0
2	IN	I_{inH} (Logic)	Digital Inputs High Current			0.1	100	nA	V_{IN} = 7.5 V
3	OUT	I_{OL} (Signaling)	A/B Output Low Current	DF332 Only		0.1	100	nA	V_{OL} = 0
4	OUT	I_{OH} (Signaling)	A/B Output High Current	DF332 Only	0.2	0.5		mA	V_{OH} = 6.5 V
5	OUT	V_{OH} (max) (Signaling)	A/B Output High Voltage	DF334 Only			12	V	I_{OH} = 10 μA
6	OUT	V_{OL} (Signaling)	A/B Output High Voltage	DF334 Only		0.3	0.5	V	I_{OL} = 1.5 mA
7	OUT	C_L (Analog)	Analog Output Load Capacitance				750	pF	
8	SUPPLY	R_O (Analog)	Analog Output Series Resistance			0.5	1.0	KΩ	See Input/Output Schematics, See Note 4
9	SUPPLY	V_{offset}	Analog Output Offset Voltage			50	100	mV	
10	SUPPLY	I^+	Positive Supply Current			6	8	mA	
11	SUPPLY	I^-	Negative Supply Current			5	7	mA	
12	SUPPLY		Supply Tolerance			±10		%	
13	SUPPLY	I_{ref}^+	Positive Reference Current			3.5		μA	Average Current See Note 3
14	SUPPLY	I_{ref}^-	Negative Reference Current			3.5		μA	Average Current See Note 3
AC Characteristics DF332, DF334 (Decoder)									
15		t'_{ds}	Sync to Clock Delay Time		25		450	ns	See Figure 3
16		t'_{dc}	Clock to Sync Delay Time		10			ns	See Figure 3
17		t'_{sd}	Data to Clock Setup Time		100			ns	See Figure 3
18		t'_{scs} (min)	A/B Select Setup Time				1000	ns	See Figure 5
		t'_{d}	A/B Output Delay Time			500	1000	ns	See Figure 5
19		t'_{do}	Analog Output to Sync Delay Time				15	μs	See Figure 3
20		$Slew^+$	3 V to +3 V Analog Output Slew Rate			5		V/μS	C_L = 100 pF
21		Slew	+3 V to −3 V Analog Output Slew Rate			5		V/μS	C_L = 100 pF
22		Droop	Analog Output Droop Rate			0.01		%/μs	
System Characteristics, DF331/DF332 Pair or DF331/DF334 Pair									
23		S/D	Signal to Distortion		35	37		dB	Pin = 0 to 30 dBmO; f_{in} = 1020 Hz
24		S/D	Signal to Distortion		30	33		dB	Pin = 40 dBmO; f_{in} = 1020 Hz
25		S/D	Signal to Distortion		25	28		dB	Pin = 45 dBmO; f_{in} = 1020 Hz
26		G_T	Gain Tracking		0.3		0.3	dB	Pin +3 to 40 dBmO; f_{in} = 1020 Hz
27		G_T	Gain Tracking		0.5		0.3	dB	Pin = 40 to 50 dBmO; f_{in} = 1020 Hz
28		G_T	Gain Tracking		2.0		1.0	dB	Pin = 50 to 55 dBmO; f_{in} = 1020 Hz
29			Idle Channel Noise			12	15	dBrnc0	V_{in} = 0, Z_o = 900 Ω
30		(DF332,DF334)	Quiet Code Output			10	12	dBrnc0	Digital In = All "Ones"

NOTES:

1. Typical values are for Design Aid only and not subject to production testing.
2. V_{in} ≥ +V − 1 V for logic "1", V_{in} ≤ 0.8 V for logic "0" for logic input levels.
3. Peak currents of up to 2 mA occur during reconstruction of Analog Output and during encoding of Analog Input.
4. Use of a load resistance ≥ 10K Ω is recommended to avoid output attenuation.

DF331 ICBL
DF332 ICBM-A
DF334 ICBM-B

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micropower comparator detector alarm circuit

designed for . . .

- **Burglar Alarm Systems**
- **Moisture Sensor Systems**
- **Temperature Detection Systems**
- **Emergency Lighting Detection Systems**
- **Excessive Noise Sound Level Detectors**
- **Remote Heat Sensor**

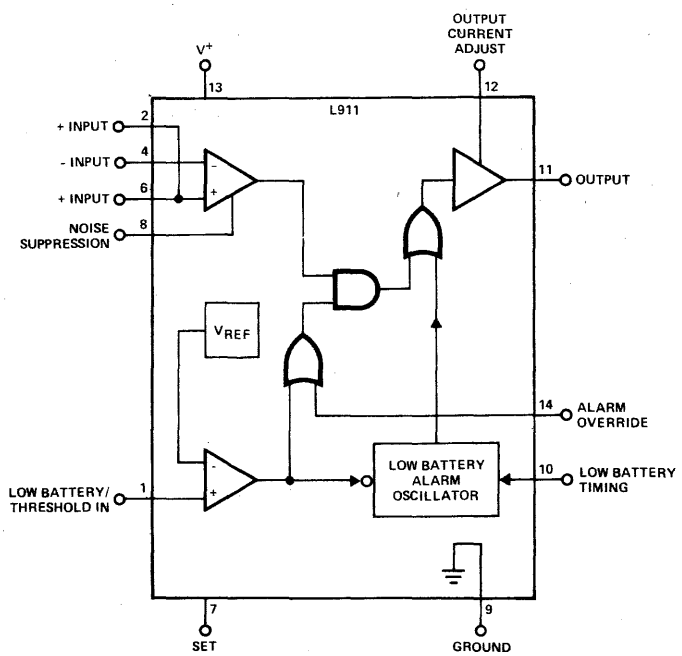
BENEFITS

- **Minimizes System Power Requirements**
  - Supply Current Less Than 10 μA
  - Allows Greater Than 1 Year of 9 V Alkaline Battery Life
- **Simple Maintenance of System**
  - Includes Weak Battery Threshold Voltage Detection Circuitry
  - Outputs Trouble Alarm Signal
- **Reduces External Component Requirements**
  - No Buffers Required for High Impedance Transducers ($R_{IN} > 1000M\ \Omega$)
  - Directly Interfaces to TTL or CMOS Logic
  - Directly Drives Power SCR's Transistors or VMOS
  - Built-In Reverse Battery Protection
- **Operation Similar to UL Recognized SM110 Smoke Detector IC**

DESCRIPTION

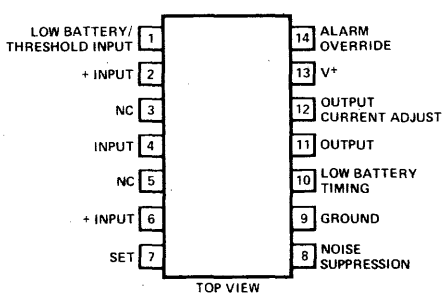
The L911 is a monolithic bipolar-PMOS integrated circuit intended to meet the system requirements of a micropower detector alarm or ON/OFF control system. The circuit will operate from a supply as low as 6 V and is tested for 15 V conditions. The alarm output can source sufficient current to activate an NPN or SCR buzzer alarm driver and can also interface to TTL or CMOS Logic. The L911 can easily operate with a standby supply current of less than 10 μA from a 9 V battery, and less than 17 μA at 15 V. The high input impedance MOSFET comparator easily interfaces to high impedance sensor devices.

FUNCTIONAL DIAGRAM



PIN CONFIGURATION

Dual-In-Line Package



ORDER NUMBER L911CJ

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ABSOLUTE MAXIMUM RATINGS

V^+ to GND . . . . . 16.5 V
Inputs (Pins 1, 2, 4, 6, 14) . . . . . $V^+ + 0.3$ V, −0.3 V
Output . . . . . 5 V
All Other Pins . . . . . V^+, 0 V
Current, Any Terminal . . . . . 30 mA

Operating Temperature . . . . . 0 to +70°C
Storage Temperature . . . . . −65 to 125°C
Power Dissipation** . . . . . 490 mW
**Device mounted with all leads welded or soldered to PC board. Derate 6.5 mW/°C above 25°C.

ELECTRICAL CHARACTERISTICS

All min/max parameters are tested at 25°C on either a 100% basis or on a sample basis to assure conformance with specifications

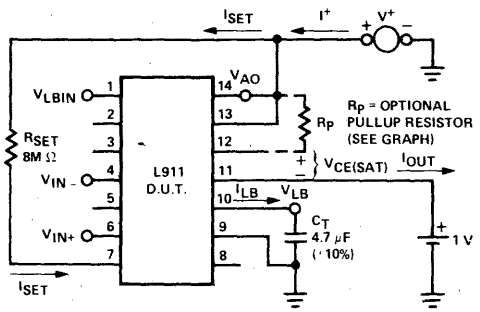
		Characteristic			Min/Max Limits Min	1 Typ	Max	Unit	Test Conditions Unless Otherwise Specified: T_A = 25°C, V^+ = 15 V, R_{SET} 8M Ω (From Pin 7 to V^+) See Test Circuit
1	SUPPLY	V^+	Operating Voltage		6.0			V	
2		I^+	Power Supply Current, Standby			4.5	10	μA	V^+ = 9 V
3						7.5	17		
4			Power Supply Current, Low Battery Condition (Excludes Output Pulse)			5	15		V^+ = 7 V
5						13	25		
6			Power Supply Current, Alarm ON			6	12	mA	V^+ = 9 V; V_{OUT} = 0 V, Pin 12 Open
7						15	28		
8	INPUTS	I_{BIAS}	Input Bias Current (Pins 1, 2, 4, 6, 14)			±0.1	±10	nA	0 V ≤ V_{IN} ≤ 15 V
9						2.3			V_{IN} = 0 V; T_A = 70°C
10						−0.5			V_{IN} = 15 V; T_A = 70°C
11		I_{OFFSET}	Input Offset Current, Pins 4 and 6			±0.1			
12		V_{OFFSET}	Input Offset Voltage, Pins 4 to 6			−20	-200	mV	
13						−20			T_A = 0°C and 70°C
14		CM	Input Common Mode Range		0		V^+−4	V	
15		V_{REF}	Internal Reference Voltage (Measured at Pin 1)		2.1	2.23	2.5		
16					2.0	2.11	2.4		V^+ = 7 V
17						1.7			T_A = 70°C
18						2.5			T_A = 0°C
19	OUTPUTS	I_{OUT}	Output Source Current		−0.5	−1.2		mA	V^+ = 6 V; Pin 12 Open (Note 2); V_{OUT} = 1 V
20					−8	−15			V^+ = 6 V; I_{OUT} = 25 mA; V_{OUT} = 1 V
21		$V_{CE(sat)}$	Output Saturation Voltage, Pins 12 to 11			0.1	0.5	V	
22		$V_{OUT(off)}$	Output OFF Voltage, Pin 11 to GND			0.01	0.2		
23		$V_{12(off)}$	Collector OFF Voltage, Pin 12 to V^+			0.6	1		
24		I_{LB}	Low Battery Timing Current (Pin 10)	OFF		−0.1	−1	nA	
25				ON		−0 32		μA	V^+ = 7 V
26					−0.5	−0.73	−1.1		
27	DYNAMIC	V_{LB}	Low Battery Timing Voltage (Pin 10)	HIGH		2.6		V	Timing Capacitor Charge Voltage; V^+ = 7 V, C_T = 4.7 μF, From Pin 10 to GND
28				LOW		0.7			Timing Capacitor Discharge Voltage
29		t_{on}	Low Battery Alarm Output ON Time			7.5		ms	
30		t_{off}	Low Battery Alarm Output OFF Time			30		sec	
31		d.c.	Low Battery Alarm Output Duty Cycle				$\frac{1}{1250}$		V^+ = 7 V
32		t_r	Response Time	Negative Output Transition		32		μs	100 mV Overdrive, C_L = 10 pF
33				Positive Output Transition		6			

NOTES:

1. Typical values are for design aid only, not guaranteed and not subject to production testing.
2. Use a pullup resistor from pin 12 to V^+ to increase the output current capability. Refer to the "pin function description" and the graph of Output Current vs Supply Voltage vs Pullup Resistor.

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TEST CIRCUIT



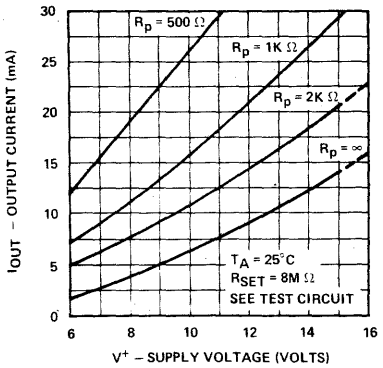
CONDITION CHART

CONDITION	INPUT VOLTAGES†		
	V_{LBI} (PIN 1)	V_{IN-} (PIN 4)	V_{IN+} (PINS 2, 6)
Standby (OFF)	2.5 V	3.5 V	3.0 V
Alarm ON	2.5 V	2.5 V	3.0 V
Low Battery/ Threshold Detector Alarm ON	1.9 V	3.5 V	3.0 V

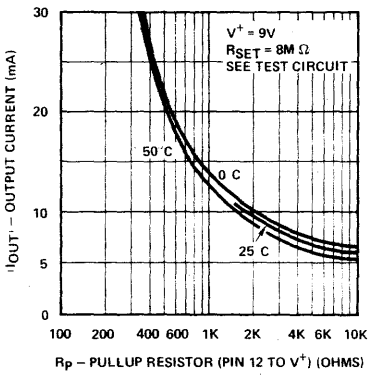
†These input voltages functionally test the system conditions noted. Exact electrical conditions are given in the electrical characteristics specifications table.

TYPICAL CHARACTERISTICS

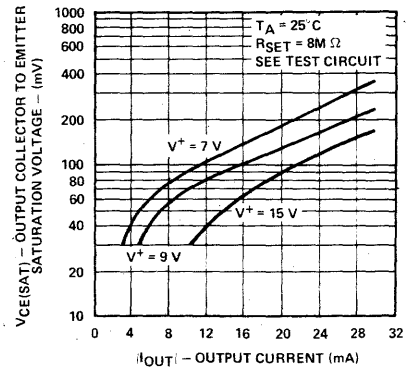
Output Current vs Supply Voltage and Pullup Resistor



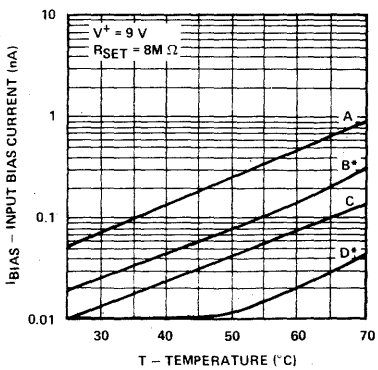
Output Current vs Pullup Resistor and Temperature



Output $V_{CE(SAT)}$ vs Pullup Resistor and Supply Voltage

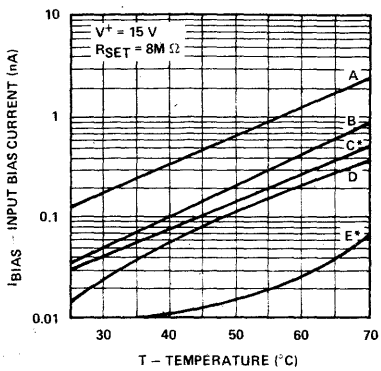


Input Bias Current vs Temperature (@ Low Supply Voltage)



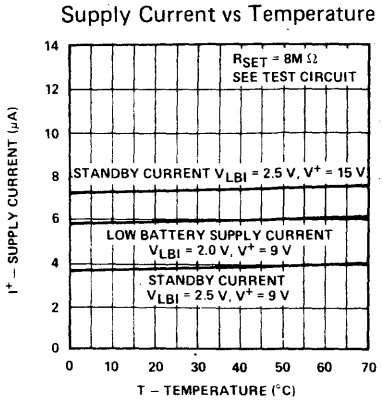
CONDITIONS
(Suffix refers to pin number)
A: I_{BIAS4} AND I_{BIAS6}. $V_{IN} = 0$ V
B: I_{BIAS4}, $V_{IN4} = 4.5$ V AND $-I_{BIAS6}$*, $V_{IN6} = 9$ V
C: I_{BIAS6}, $V_{IN6} = 4.5$ V
D: $-I_{BIAS4}$*, $V_{IN4} = 9$ V
*$-I_{BIAS}$ IS A NEGATIVE CURRENT (FLOWS OUT OF TERMINAL)

Input Bias Current vs Temperature (@ High Supply Voltage)

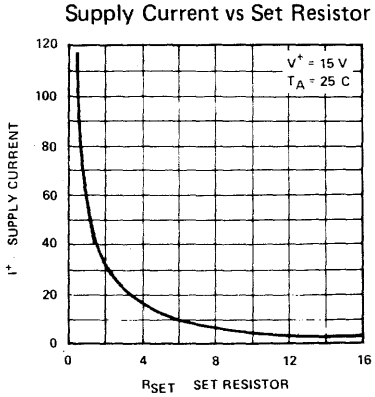


CONDITIONS
(Suffix refers to pin number)
A: I_{BIAS4} AND I_{BIAS6}. $V_{IN} = 0$ V
B: I_{BIAS4}, $V_{IN} = 7.5$ V
C: $-I_{BIAS6}$*, $V_{IN6} = 15$ V
D: I_{BIAS6}, $V_{IN6} = 7.5$ V
E: $-I_{BIAS4}$*, $V_{IN4} = 15$ V
*$-I_{BIAS}$ IS A NEGATIVE CURRENT (FLOWS OUT OF TERMINAL)

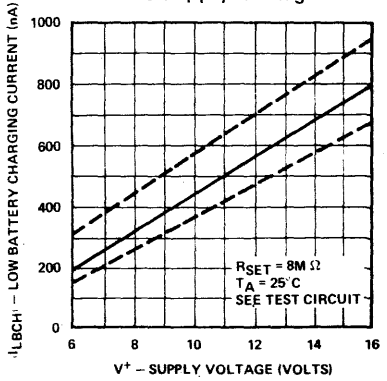
Supply Current vs Temperature



Supply Current vs Set Resistor



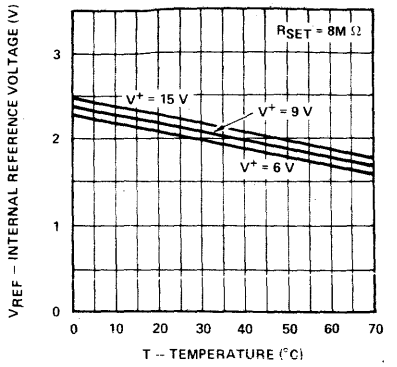
Low Battery Charge Current vs Supply Voltage



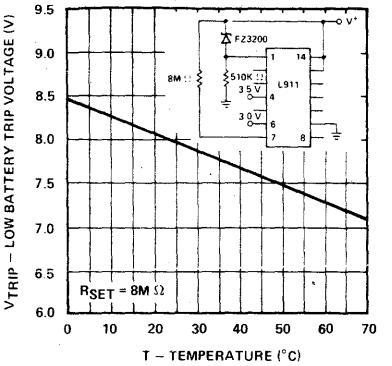
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TYPICAL CHARACTERISTICS (Continued)

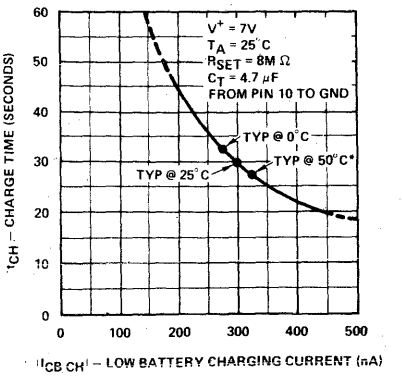
Reference Voltage vs Temperature and Supply Voltage



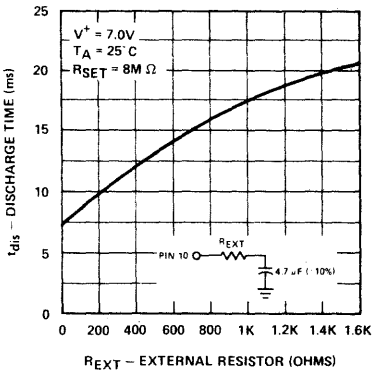
Low Battery Trip Voltage vs Temperature



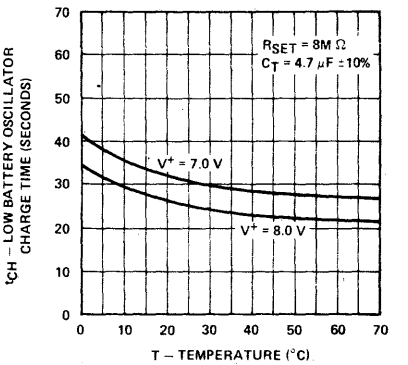
Low Battery Charge Time vs Charging Current



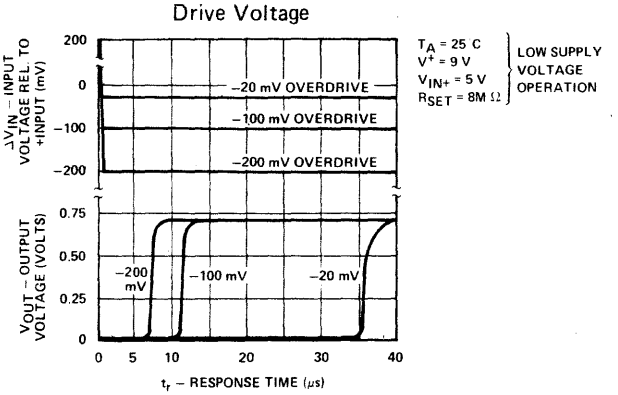
Low Battery Alarm ON Time vs External Resistance



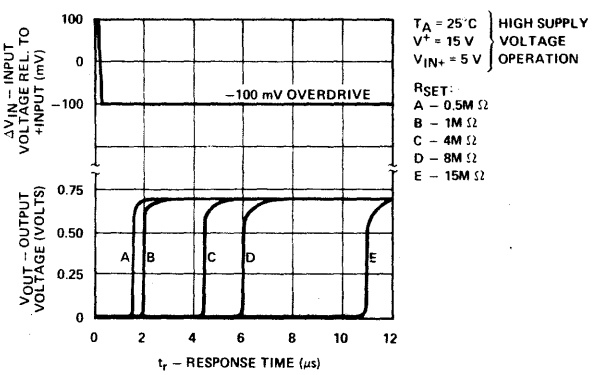
Low Battery Alarm Period vs Temperature and Supply Voltage



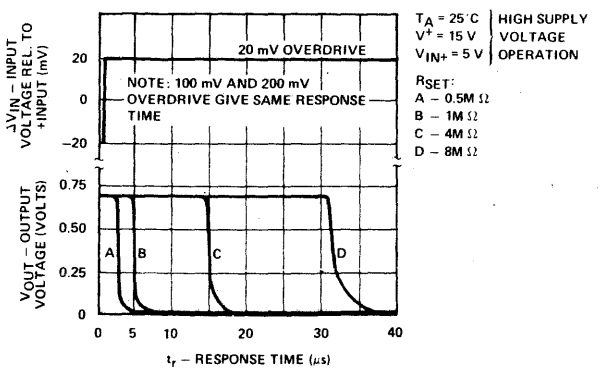
Response Time vs Input Over Drive Voltage



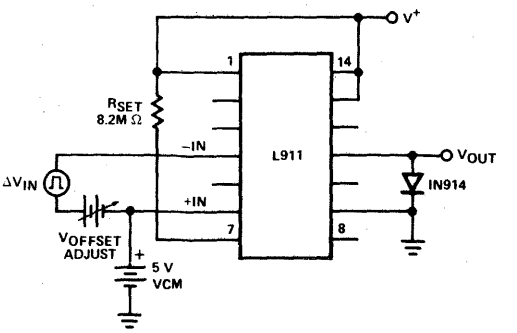
Positive Transition Response Time vs Set Resistor



Negative Transition Response Time vs Set Resistor



Response Time Test Circuit



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APPLICATION HINTS

Bias Control of Standby Supply Current

The current entering the "SET" input will program the supply standby current at follows:

$$I_{SET} = \frac{V^+ - 0.55\ V}{R_{SET}}$$

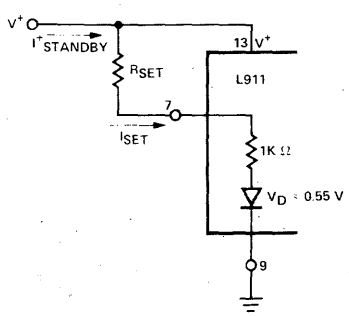
The supply current is:

$$I^+ \text{ STANDBY} \approx 4 \times I_{SET}$$

(includes I_{SET} into pin 7).

In the "Low Battery Alarm" condition (with $V^+ \approx 7$ V) the supply current becomes:

$$I^+ \text{ Low Battery Alarm (excluding output pulse)} \approx 7 \times \frac{V^+ \text{ LOW BATTERY} - 0.55\ V}{R_{SET}}$$



Low Battery Alarm Oscillator Timing

t_{ch} – charge time (oscillation OFF period)

$$t_{ch} = \frac{\Delta V_C}{I_{CH}} \times C_T \text{ where}$$

$\Delta V_C = V_{C\ HIGH} - V_{C\ LOW}$ (capacitor charge and discharge voltage levels).

$\Delta V_C \approx 2.6\ V - 0.7\ V = 1.9\ V$

$I_{CH} = 0.4 \times I_{SET} = 0.4 \times (V^+ - 0.55)/R_{SET}$

C_T = timing capacitor from Low Battery Timing to Ground.

In Figure 1, for $V^+ = 7$ V:

$$t_{ch} = \frac{1.9\ V}{0.32\ \mu A} \times 4.7\ \mu F \approx 28 \text{ sec.}$$

t_{DIS} – Discharge time (oscillation ON pulse).

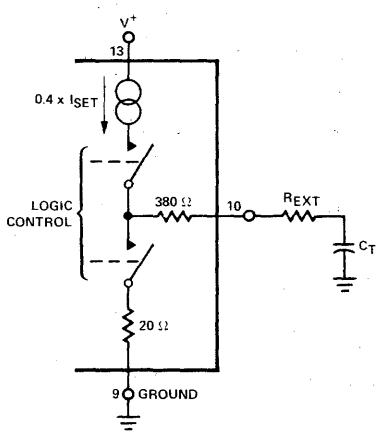
$$t_{DIS} = \left| \left[\ln \frac{I_{HOLD}\ R}{1.91} \right] \tau \right|$$

where I_{HOLD} = SCR Holding current $\approx 100\ \mu A$
R = Series Resistance $\approx 400\ \Omega$ ($R_{EXT} = 0\ \Omega$)
τ = RC Time constant

with C = 4.7 μF (as in Figure 1), $\tau = 400\ \Omega \times 4.7\ \mu F = 1.9$ msec.

$t_{DIS} = 7.3$ msec

To increase t_{DIS}, external resistance can be added in series with C_T (see the graph of typical Discharge Time vs External Resistance).



Input-Output Truth Table

Illustrating Alarm Output conditions for input conditions at Input, Low Battery Set, Alarm Override.

–Input voltage (pin 4) with respect to +input (pins 2 and 6)	H	L	H	L	L
Low Battery Input voltage with respect to internal V_{REF} (pin 1)	H	H	L	L	L
Alarm Override (pin 14)	–	–	–	H	L
Output State: ON – Alarm condition; OSC = ON/OFF oscillation controlled by Low Battery Timing (pin 11)	OFF	ON	OSC	ON	OSC

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TYPES TL431M, TL431I, TL431C
ADJUSTABLE PRECISION SHUNT REGULATORS

BULLETIN NO. DL-S 12644, JULY 1978

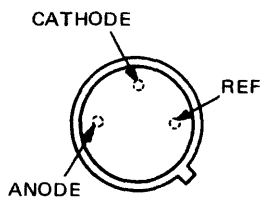
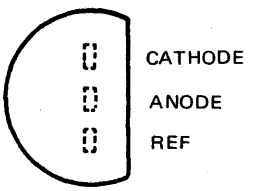
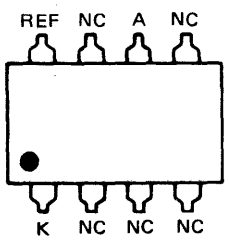
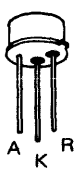
- Equivalent Full-Range Temperature Coefficient . . . 50 ppm/°C Typ
- Temperature Compensated for Operation Over Full Rated Operating Temperature Range
- Adjustable Output Voltage
- Fast Turn-On Response
- Sink Current Capability . . . 1 mA to 100 mA
- Low (0.2-Ω Typ) Dynamic Output Impedance
- Low Output Noise Voltage

description

The TL431 is a three-terminal adjustable regulator series with guaranteed thermal stability over applicable temperature ranges. The output voltage may be set to any value between V_{ref} (approximately 2.5 volts) and 36 volts with two external resistors (see Figure 2). These devices have a typical dynamic output impedance of 0.2 Ω. Active output circuitry provides a very sharp turn-on characteristic, making these devices excellent replacements for zener diodes in many applications.

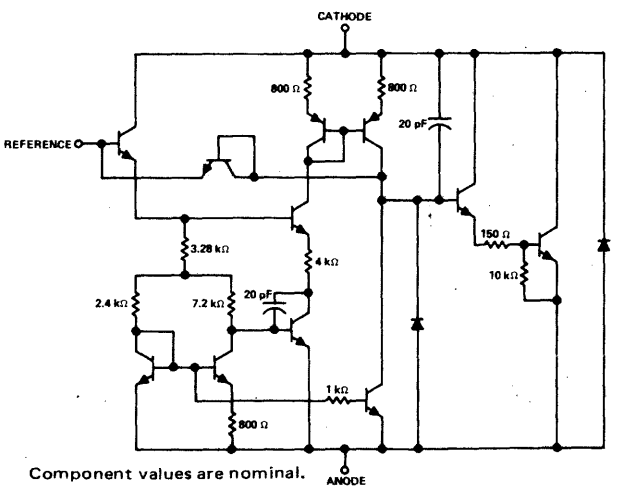
The TL431M is characterized for operation over the full military temperature range of −55°C to 125°C. The TL431I is characterized for operation from −40°C to 85°C, and the TL431C from 0°C to 70°C.

terminal assignments

TL431M, TL431I, TL431C . . . LA PLUG-IN PACKAGE	TL431I, TL431C . . . LP SILECT† PACKAGE	TL431I, TL431C . . . P DUAL-IN-LINE PACKAGE
(TOP VIEW)	(TOP VIEW)	(TOP VIEW)
		
		

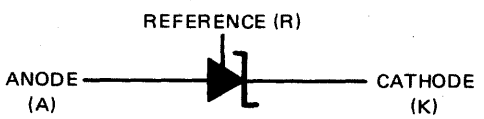
NC—No internal connection

schematic



Component values are nominal.

functional block diagram



†Trademark of Texas Instruments Incorporated

TENTATIVE DATA SHEET

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This document provides tentative information on a new product. Texas Instruments reserves the right to change specifications for this product in any manner without notice.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 225012 • DALLAS, TEXAS 75265

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Cathode voltage (see Note 1) . . . . . 37 V
Continuous cathode current range . . . . . −100 mA to 150 mA
Reference input current range . . . . . −50 μA to 10 mA
Continuous power dissipation at (or below) 25°C free-air temperature (see Note 2): LA package . . . . . 600 mW
LP package . . . . . 775 mW
P package . . . . . 1000 mW
Operating free-air temperature range: TL431C . . . . . 0°C to 70°C
TL431I . . . . . −40°C to 85°C
TL431M . . . . . −55°C to 125°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1/16 inch (1.6 mm) from case for 60 seconds: LA package . . . . . 300°C
Lead temperature 1/16 inch (1.6 mm) from case for 10 seconds: LP or P package . . . . . 260°C

NOTES: 1. Voltage values are with respect to the anode terminal unless otherwise noted.
2. For operation above 25°C free-air temperature, refer to the Dissipation Derating Table.

recommended operating conditions

	MIN	MAX	UNIT
Cathode voltage, V_{KA}	V_{ref}	36	V
Cathode current, I_K, (for regulation)	1	100	mA

DISSIPATION DERATING TABLE

PACKAGE	POWER RATING	DERATING FACTOR	ABOVE T_A
LA	600 mW	4.8 mW/°C	25°C
LP	775 mW	6.2 mW/°C	25°C
P	1000 mW	8.0 mW/°C	25°C

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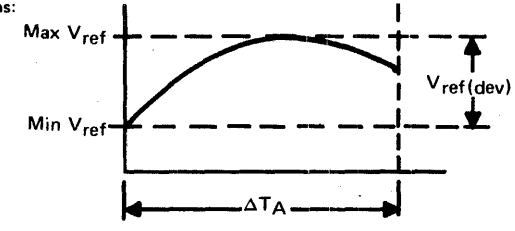
electrical characteristics at 25°C free-air temperature (unless otherwise noted)

PARAMETER		TEST CIRCUIT	TEST CONDITIONS		TL431M			TL431I			TL431C			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{ref}	Reference input voltage	1	$V_{KA} = V_{ref}$, I_K = 10 mA		2440	2495	2550	2440	2495	2550	2440	2495	2550	mV
$V_{ref(dev)}$	Deviation of reference input voltage over full temperature range‡	1	$V_{KA} = V_{ref}$, I_K = 10 mA, T_A = full range†			22	44		15	30		8	17	mV
$\frac{\Delta V_{ref}}{\Delta V_{KA}}$	Ratio of change in reference input voltage to the change in cathode voltage	2	I_K = 10 mA	ΔV_{KA} = 10 V − V_{ref}		−1.4	−2.7		−1.4	−2.7		−1.4	−2.7	mV/V
				ΔV_{KA} = 36 V − 10 V		−1	−2		−1	−2		−1	−2	
I_{ref}	Reference input current	2	I_K = 10 mA, R1 = 10 kΩ, R2 = ∞			2	4		2	4		2	4	μA
$I_{ref(dev)}$	Deviation of reference input current over full temperature range‡	2	I_K = 10 mA, R1 = 10 kΩ, R2 = ∞, T_A = full range†			1	3		0.8	2.5		0.4	1.2	μA
I_{min}	Minimum cathode current for regulation	1	$V_{KA} = V_{ref}$			0.4	1		0.4	1		0.4	1	mA
I_{off}	Off-state cathode current	3	V_{KA} = 36 V, V_{ref} = 0			0.1	1		0.1	1		0.1	1	μA
$\lvert z_{ka} \rvert$	Dynamic impedance§	1	$V_{KA} = V_{ref}$, I_K = 1 mA to 100 mA, f ≤ 1 kHz			0.2	0.5		0.2	0.5		0.2	0.5	Ω

†Full temperature range is −55°C to 125°C for the TL431M, −40°C to 85°C for the TL431I, and 0°C to 70°C for the TL431C.

‡The deviation parameters $V_{ref(dev)}$ and $I_{ref(dev)}$ are defined as the differences between the maximum and minimum values obtained over the rated temperature range. The equivalent full-range temperature coefficient of the reference input voltage, αV_{ref}, is defined as:

$$\left|\alpha V_{ref}\right| \left(\frac{ppm}{°C}\right) = \frac{\left(\frac{V_{ref(dev)}}{V_{ref\ @\ 25°C}}\right) \times 10^6}{\Delta T_A}$$



where ΔT_A is the rated operating free-air temperature range of the device.

αV_{ref} can be positive or negative depending on whether minimum V_{ref} or maximum V_{ref}, respectively, occurs at the lower temperature (see Figure 8).

Example: Max V_{ref} = 2500 mV @ 30°C, Min V_{ref} = 2492 mV @ 0°C, V_{ref} = 2495 mV @ 25°C, ΔT_A = 70°C for TL431C

$$\left|\alpha_{Vref}\right| = \frac{\left(\frac{8\ mV}{2495\ mV}\right) \times 10^6}{70°C} = 46\ ppm/°C$$

Because minimum V_{ref} occurs at the lower temperature, the coefficient is positive.

§The dynamic impedance is defined as:

$$\left|z_{ka}\right| = \frac{\Delta V_{KA}}{\Delta I_K}$$

When the device is operated with two external resistors (see Figure 2), the total dynamic impedance of the circuit is given by:

$$\left|z'\right| = \frac{\Delta V}{\Delta I} \approx \left|z_{ka}\right| \left(1 + \frac{R1}{R2}\right)$$

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PARAMETER MEASUREMENT INFORMATION

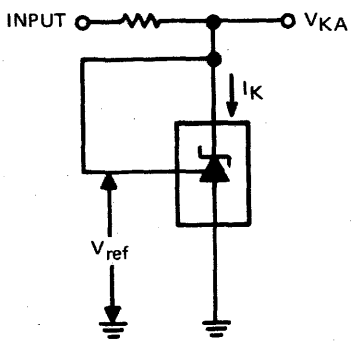


FIGURE 1–TEST CIRCUIT FOR $V_{KA} = V_{ref}$

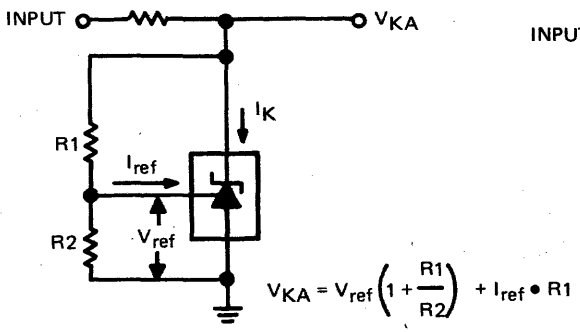


FIGURE 2–TEST CIRCUIT FOR $V_{KA} > V_{ref}$

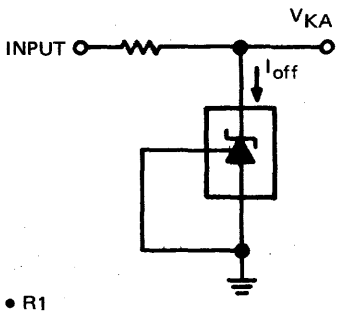


FIGURE 3–TEST CIRCUIT FOR I_{off}

TYPICAL CHARACTERISTICS

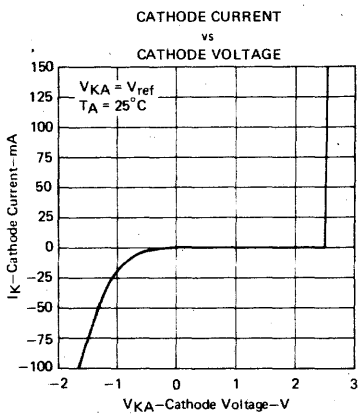


FIGURE 4

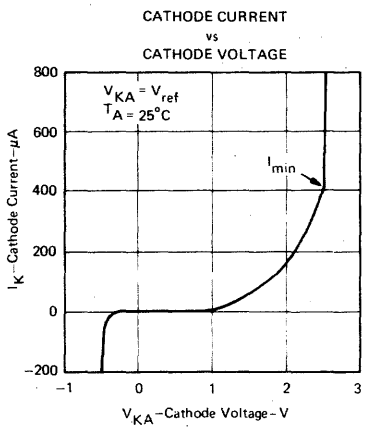


FIGURE 5

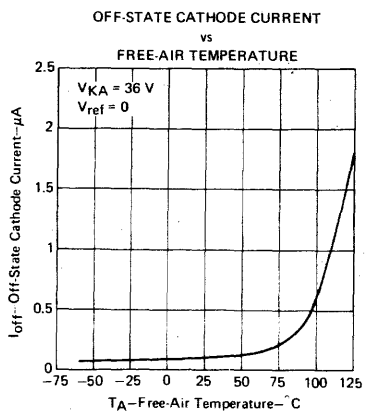


FIGURE 6

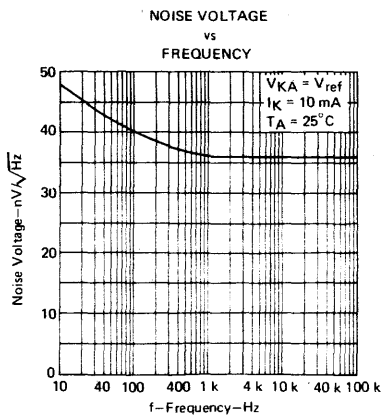


FIGURE 7

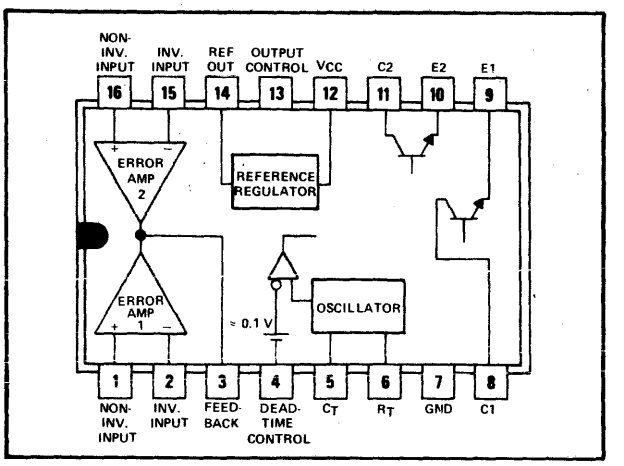
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TYPES TL494C, TL495C
PULSE-WIDTH-MODULATION CONTROL CIRCUITS

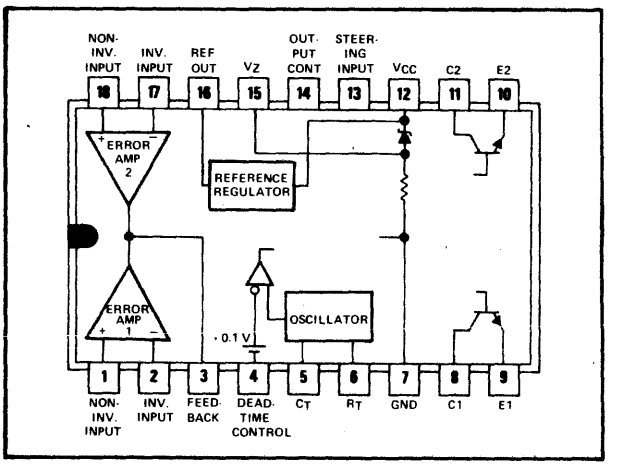
BULLETIN NO. DL-S 12620, JUNE 1978

- Complete PWM Power Control Circuitry
- Uncommitted Outputs for 200-mA Sink or Source
- Output Control Selects Single-Ended or Push-Pull Operation
- Internal Circuitry Prohibits Double Pulse at Either Output
- Variable Dead-Time Provides Control Over Total Range
- Internal Regulator Provides a Stable 5-V Reference Supply
- Circuit Architecture Provides Easy Synchronization
- On-Chip 39-V Zener (TL495 Only)
- External Control of Output Steering (TL495 Only)

TL494C . . . J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



TL495C . . . J OR N
DUAL-IN-LINE PACKAGE (TOP VIEW)



description

The TL494 incorporates on a single monolithic chip all the functions required in the construction of a pulse-width-modulation control circuit. Designed primarily for power supply control, the TL494 contains an on-chip 5-volt regulator, two error amplifiers, adjustable oscillator, dead-time control comparator, pulse-steering flip-flop, and output-control circuitry. The uncommitted output transistors provide either common-emitter or emitter-follower output capability. Push-pull or single-ended output operation may be selected through the output-control function. The architecture of the TL494 prohibits the possibility of either output being pulsed twice during push-pull operation. The internal amplifiers exhibit a common-mode voltage range from −0.2 volt to V_{CC} − 2 volts. The dead-time control comparator has a fixed offset that provides approximately 5% dead time unless externally altered. The on-chip oscillator may be bypassed by terminating R_T (pin 6) to the reference output and providing a sawtooth input to C_T (pin 5), or it may be used to drive the common TL494 circuitry and provide a sawtooth input for associated control circuitry in synchronous multiple-rail power supplies.

FUNCTION TABLE

INPUTS		OUTPUT FUNCTION
OUTPUT CONTROL	STEERING INPUT (TL495 only)	
Grounded	Open	Single-ended or parallel output
At V_{ref}	Open	Normal push-pull operation
At V_{ref}	$V_I < 0.4$ V	PWM Output at Q1
At V_{ref}	$V_I > 2.4$ V	PWM Output at Q2

The TL495 provides the identical functions found in the TL494. In addition the TL495 contains an on-chip 39-volt zener diode for high-voltage applications where V_{CC} is greater than 40 volts, and an output steering control that overrides the internal control of the pulse-steering flip-flop.

The TL494C and the TL495C are characterized for operation from 0°C to 70°C.

TENTATIVE DATA SHEET

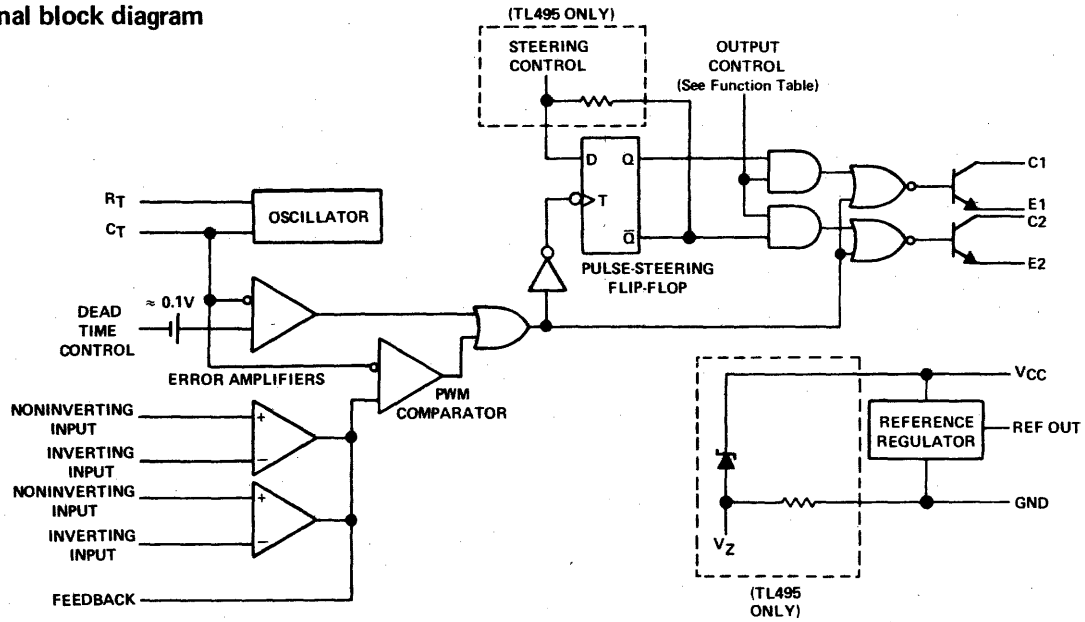
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functional block diagram



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	41 V
Amplifier input voltages	V_{CC} + 0.3 V
Collector output voltage	41 V
Collector output current	250 mA
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2)	1000 mW
Operating free-air temperature range	0°C to 70°C
Storage temperature range	−65°C to 150°C
Lead temperature 1/16 inch (1,6 mm) from case for 60 seconds: J package	300°C
Lead temperature 1/16 inch (1,6 mm) from case for 10 seconds: N package	260°C

NOTES: 1. All voltage values are with respect to network ground terminal.
2. For operation above 25°C free-air temperature, see Dissipation Derating Table.

DISSIPATION DERATING TABLE

PACKAGE	POWER RATING	DERATING FACTOR	ABOVE T_A
J	1000 mW	8.2 mW/°C	28°C
N	1000 mW	9.2 mW/°C	41°C

recommended operating conditions

	MIN	MAX	UNIT
Supply voltage, V_{CC}	7	40	V
Amplifier input voltages, V_I	−0.3	V_{CC} −2	V
Collector output voltage, V_O		40	V
Collector output current (each transistor)		200	mA
Current into feedback terminal		0.3	mA
Timing capacitor, C_T	0.47	10,000	nF
Timing resistor, R_T	1.8	500	kΩ
Oscillator frequency	1	300	kHz
Operating free-air temperature	0	70	°C

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electrical characteristics over recommended operating free-air temperature range, V_{CC} = 15 V, f = 10 kHz (unless otherwise noted)

reference section

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Output voltage (V_{ref})	I_O = 1 mA	4.75	5	5.25	V
Input regulation	V_{CC} = 7 V to 40 V, T_A = 25°C		2	25	mV
Output regulation	I_O = 1 to 10 mA, T_A = 25°C		1	15	mV
Output voltage change with temperature	T_A = 0°C to 70°C		0.2	1	%
Short-circuit output current‡	V_{ref} = 0		35		mA

oscillator section

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Frequency	C_T = 0.01 μF, R_T = 12 kΩ		10		kHz
Standard deviation of frequency§	All values of V_{CC}, C_T, R_T, T_A constant		10		%
Frequency change with voltage	V_{CC} = 7 V to 40 V, T_A = 25°C		0.1		%
Frequency change with temperature	C_T = 0.01 μF, R_T = 12 kΩ, T_A = 0°C to 70°C			2	%

dead-time control-section (see figure 1)

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Input bias current (pin 4)	V_I = 0 to 5.25 V		−2	−10	μA
Maximum duty cycle, each output	V_I (pin 4) = 0	45			%
Input threshold voltage (pin 4)	Zero duty cycle		3	3.3	V
	Maximum duty cycle	0			

error-amplifier sections

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Input offset voltage	V_O (pin 3) = 2.5 V		2	10	mV
Input offset current	V_O (pin 3) = 2.5 V		25	250	nA
Input bias current	V_O (pin 3) = 2.5 V		0.2	1	μA
Common-mode input voltage range	V_{CC} = 7 V to 40 V	−0.3 to V_{CC}−2			V
Open-loop voltage amplification	ΔV_O = 3 V, V_O = 0.5 V to 3.5 V	70	95		dB
Unity-gain bandwidth			800		kHz
Common-mode rejection ratio	V_{CC} = 40 V, T_A = 25°C	65	80		dB
Output sink current (pin 3)	V_{ID} = −15 mV to −5 V, $V_{(pin\ 3)}$ = 0.7 V	0.3	0.7		mA
Output source current (pin 3)	V_{ID} = 15 mV to 5 V, $V_{(pin\ 3)}$ = 3.5 V	−2			mA

output section

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Collector off-state current		V_{CE} = 40 V, V_{CC} = 40 V		2	100	μA
Emitter off-state current		V_{CC} = V_C = 40 V, V_E = 0			−100	μA
Collector-emitter saturation voltage	Common-emitter	V_E = 0, I_C = 200 mA		1.1	1.3	V
	Emitter follower	V_C = 15 V, I_E = −200 mA		1.5	2.5	
Output control input current		V_I = V_{ref}			3.5	mA

†All typical values except for temperature coefficients are at T_A = 25°C.
‡Duration of the short-circuit should not exceed one second.
§Standard deviation is a measure of the statistical distribution about the mean as derived from the formula $\sigma = \sqrt{\frac{\sum_{n=1}^{N} (x_n - \bar{x})^2}{N-1}}$

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electrical characteristics over recommended operating free-air temperature range, V_{CC} = 15 V, f = 10 kHz (unless otherwise noted)

pwm comparator section (see figure 1)

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Input threshold voltage (pin 3)	Zero duty cycle		4	4.5	V
Input sink current (pin 3)	$V_{(pin\ 3)}$ = 0.7 V	0.3	0.7		mA

steering control (TL495 only)

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
Input current	V_I = 0.4 V		−200	μA
	V_I = 2.4 V		200	

zener-diode circuit (TL495 only)

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Breakdown voltage	V_{CC} = 41 V, I_Z = 2 mA		39		V
Sink current	$V_{I(pin\ 15)}$ = 1 V		0.3		mA

total device

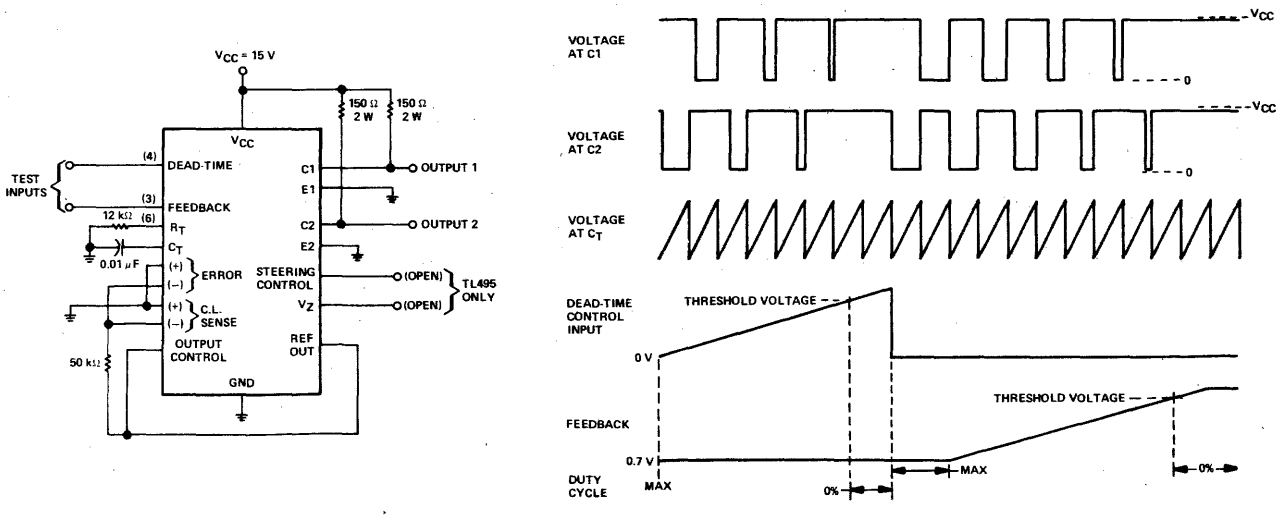
PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Standby supply current	Pin 6 at V_{ref}, All other inputs and outputs open		6	10	mA
Average supply current	$V_{(pin\ 4)}$ = 2 V, See Figure 1		7.5		mA

switching characteristics, T_A = 25°C

PARAMETER	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
Output voltage rise time	Common-emitter configuration, See Figure 3		100	200	ns
Output voltage fall time			25	100	ns
Output voltage rise time	Emitter-follower configuration, See Figure 4		100	200	ns
Output voltage fall time			40	100	ns

†All typical values except for temperature coefficients are at T_A = 25°C.

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT VOLTAGE WAVEFORMS

FIGURE 1–DEAD-TIME AND FEEDBACK CONTROL

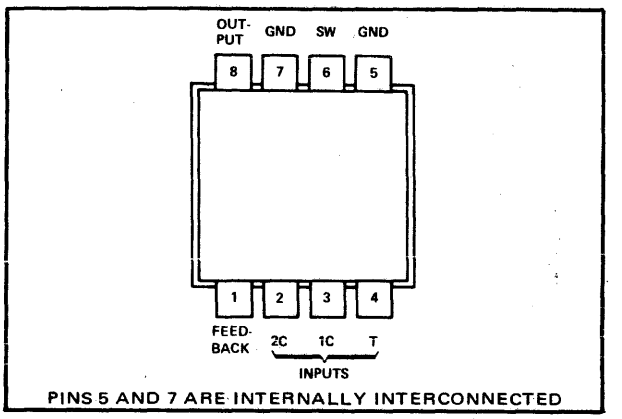
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TYPE TL496C
9-VOLT POWER-SUPPLY CONTROLLER

BULLETIN NO. DL-S 12657, AUGUST 1978

- Internal Step-Up Switching Regulator
- Fixed 9-Volt Output
- Charges Battery Source During Transformer-Coupled-Input Operation
- Minimum External Components Required (1 Inductor, 1 Capacitor, 1 Diode)
- 1- or 2-Cell-Input Operation

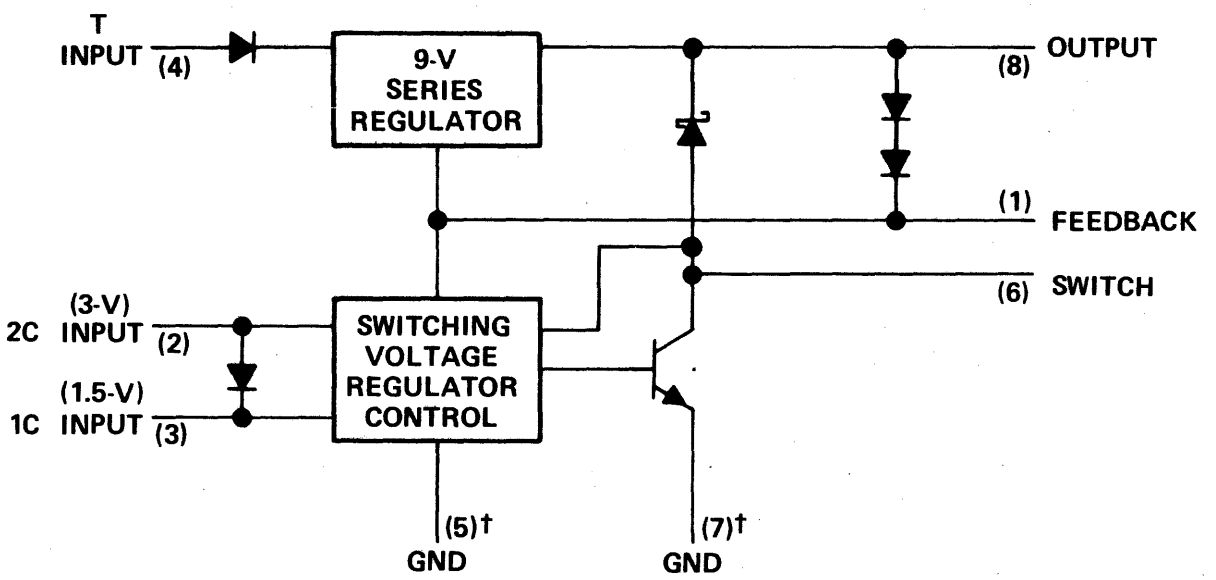
JG OR P
DUAL-IN-LINE PACKAGE
(TOP VIEW)



description

The TL496 power supply control circuit is designed to provide a 9-volt regulated supply from a variety of input sources. Operable from a 1- or 2-cell-battery input, the TL496 performs as a switching regulator with the addition of a single inductor and filter capacitor. When ac coupled with a step-down transformer, the TL496 operates as a series regulator to maintain the regulated output voltage and, with the addition of a single catch diode, time shares to recharge the input batteries.

functional block diagram



†Even though connected internally, pins 5 and 7 must both be terminated to ground to ensure proper circuit operation.

TENTATIVE DATA SHEET

This document provides tentative information on a new product. Texas Instruments reserves the right to change specifications for this product in any manner without notice.

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absolute maximum ratings

Input voltage:	
Pin 2	3.5 V
Pin 3	2.5 V
Pin 4	20 V
Output voltage (Pin 6)	12 V
Diode reverse voltage (Pin 8)	12 V
Switch current (Pin 6)	1.2 A
Diode current (Pin 8)	1.2 A
Operating free-air temperature range	0°C to 70°C
Storage temperature range	−65°C to 150°C
Lead temperature 1/16 inch (1.6 mm) from case for 10 seconds	260°C

electrical characteristics at 25°C free-air temperature

series regulator section (input is pin 4)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Dropout voltage	V_I = 5 V, I_O = −50 mA			1.5	2	V
Regulated output voltage	V_I = 20 V	I_O = −50 μA	9.5	10.1	11.2	V
		I_O = −80 mA	9.0	10.0	11.0	
	V_I = 20 V, Pin 1 shorted to pin 8	I_O = −50 μA	8.5	9.0	9.7	
		I_O = −80 mA	6.7	8.6	9.5	
Standby current (pin 4)	V_I = 20 V, Pin 8 at 12 V				400	μA
Reverse current thru pin 4	V_I = −1.5 V, 1 mA into Pin 8				−25	μA

output switch

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
$V_{CE(sat)}$ Collector-emitter saturation voltage	800 mA into Pin 6	Pin 2 at 2.25 V		0.35	0.6	V

diode (pin 6 to pin 8)

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_F Forward voltage	I_F = 1.5 A			1.6	2.5	V
I_R Reverse current thru pin 6	Pin 6 at 0 V	1 mA into Pin 8			−20	μA

control section

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
On-state current (pin 2)	Pins 1 and 8 at 0 V,	Pin 2 at 3 V		60	100	mA
Standby current (pin 1)	Pin 1 at 8.65 V,	Pins 2 and 6 at 3 V			40	μA
Standby current (pin 2 and 6)	Pin 1 at 8.65 V,	Pins 2 and 6 at 3 V			400	μA
Start-up current (current into pin 6 to initiate cycle)	Pins 1, 2, 6 and 8 at 2.25 V		16			mA

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TYPICAL APPLICATION DATA

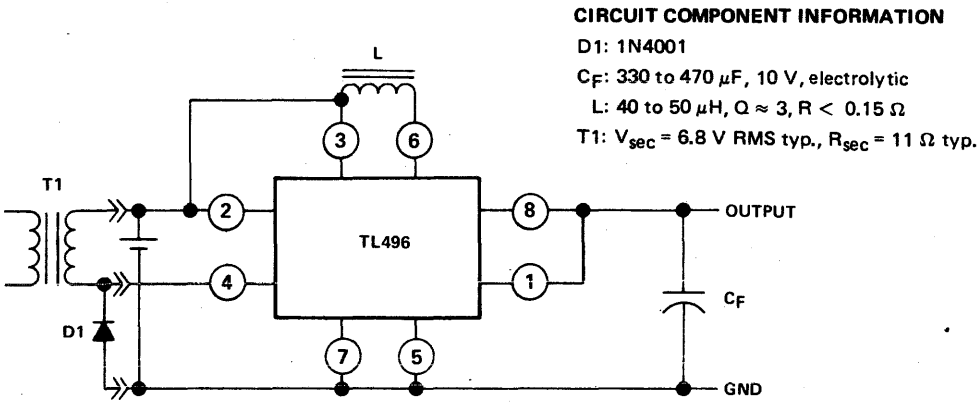


FIGURE 1–ONE-CELL OPERATION

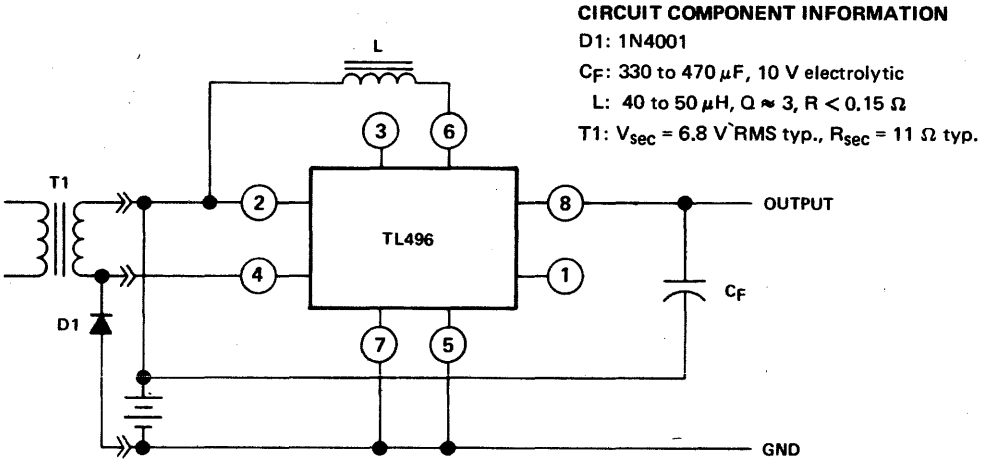


FIGURE 2–TWO-CELL OPERATION

recommended operating conditions

	MIN	MAX	UNIT
Input voltage, one-cell operation (pins 2 and 3 to ground)	1.1	1.5	V
Input voltage, two-cell operation (pin 2 to ground)	2.3	3	V
Input voltage, one-cell or two-cell operation (pin 4 to ground)	V_O+2	20	V

typical electrical characteristics for circuits above

PARAMETER		ONE-CELL OPERATION (FIGURE 1)	TWO-CELL OPERATION (FIGURE 2)
Input current	No load	125 uA	125 uA
	R_L = 120 Ω	525 mA	405 mA
Output voltage	Without T1	7.2 V	8.6 V
	With T1	8.6 V	10 V
Output current capability		40 mA	80 mA
Efficiency		66%	66%
Battery life (AA NiCad) no load		60 days	166 days

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functional description

The TL496 is designed to operate from either a single-cell or two-cell source. To operate the device from a single cell (1.1 V to 1.5 V) the source must be connected to both inputs 1C and 2C as shown in Figure 1. For two-cell operation (2.3 V to 3.0 V), the input is applied to the 2C input only and the 1C input is left open (see Figure 2).

battery operation

The TL496 operates as a switching regulator from a battery input. The cycle is initiated when a low voltage condition is sensed by the internal feedback (the thresholds at pin 1 and pin 8 are approximately 7.2 and 8.6 volts respectively). An internal latch is set and the output transistor is turned "on." This causes the current in the external inductor (L) to increase linearly until it reaches a peak value of approximately 1 ampere. When the peak current is sensed the internal latch is reset and the output transistor is turned "off." The energy developed in the inductor is then delivered to the output storage capacitor through the blocking diode. The latch remains in the off state until the feedback signal indicates the output voltage is again deficient.

transformer-coupled operation

The TL496 operates on alternate half cycles of the ac input during transformer-coupled operation to, first, sustain the output voltage and, second, recharge the batteries. The TL496 performs like a series regulator to supply charge to the output filter/storage capacitor during the first half cycle. The output voltage of the series regulator is slightly higher voltage than that created by the switching circuit; this maintains the feedback voltage above the switching regulator control circuit threshold. This effectively inhibits the switching control circuitry. During the second half cycle an external diode (1N4001) is used to clamp the negative going end of the transformer secondary to ground thus allowing the positive-going end (end connected to V+ side of battery) to pump charge into the stand-by batteries.

general

The design of the TL496 allows minimal supply current drain during stand-by operation (125 uA typical). With most battery sources this allows a constant bias to be maintained on the power supply. This allows instant power available to the system thus eliminating power-up sequencing problems.

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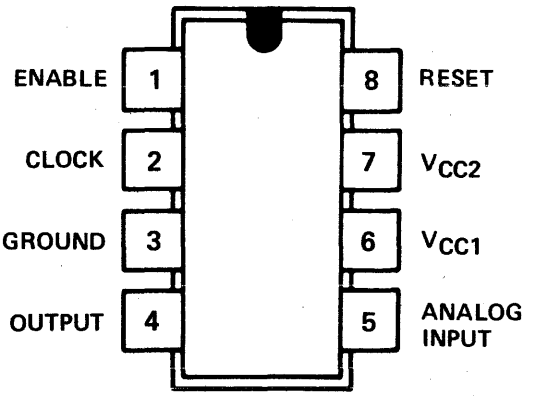
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TYPE TL507C ANALOG-TO-DIGITAL CONVERTER

SEPTEMBER 1978

- Low Cost
- 7-Bit Resolution
- Guaranteed Monotonicity
- Ratiometric Conversion
- Conversion Speed . . . approximately 1 ms
- Single-Supply Operation . . . Either Unregulated 8-V to 18-V V_{CC2} Input, or Regulated 3.5-V to 6-V V_{CC1} Input
- I^2L Technology
- Power Consumption at 5 V . . . 25 mW Typ

P DUAL-IN-LINE PACKAGE
(TOP VIEW)



description

The TL507C is a single-slope analog-to-digital converter designed for use with TMS 1000 type microprocessors. It contains a 7-bit synchronous counter, a binary weighted resistor ladder network, an operational amplifier, two comparators, a buffer amplifier, an internal regulator, and necessary logic circuitry. Integrated-injection logic (I^2L) technology makes it possible to offer this complex circuit at low cost in a small dual-in-line 8-pin package.

In continuous operation, it is possible to obtain conversion speeds up to 1000 per second. The TL507 requires external signals for clock, reset, and enable. Versatility and simplicity of operation coupled with low cost, makes this converter especially useful for a wide variety of applications.

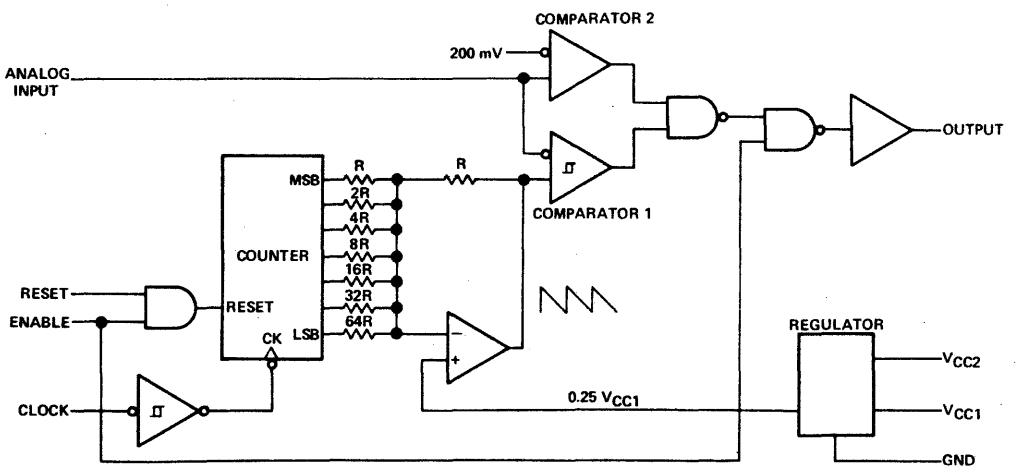
The TL507C is characterized for operation from 0°C to 70°C.

FUNCTION TABLE

ANALOG INPUT CONDITION	ENABLE	OUTPUT
X	L†	H
$V_I < 200$ mV	H	L
$V_{ramp} > V_I > 200$ mV	H	H
$V_I > V_{ramp}$	H	L

† Low level on enable also inhibits the reset function.
H = high level, L = low level, X = irrelevant

functional block diagram



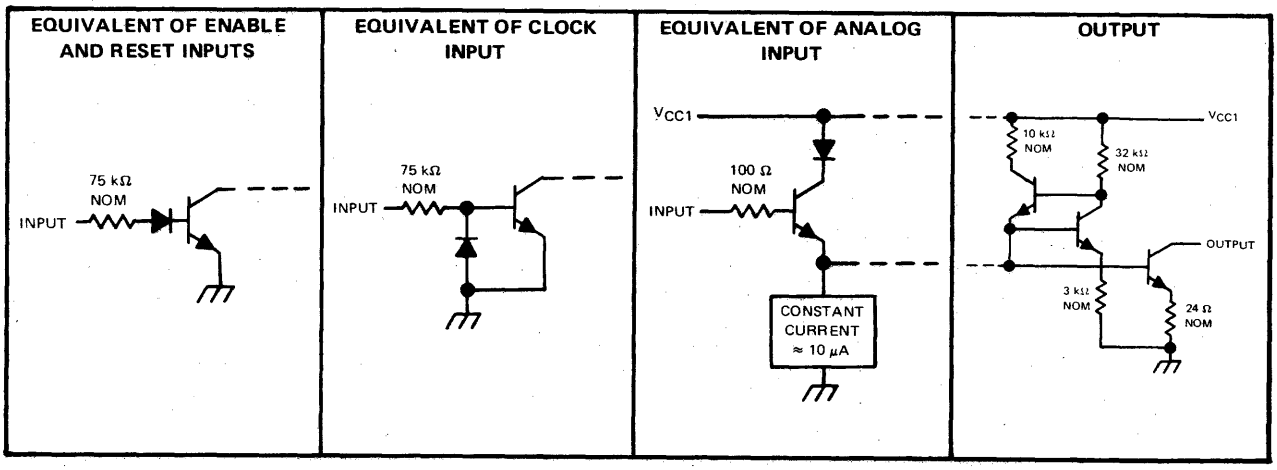
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schematics of inputs and outputs



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC1} (see Note 1) . . . . . 6.5 V
Supply voltage, V_{CC2} . . . . . 20 V
Input voltage at analog input . . . . . 6.5 V
Input voltage at enable, clock, and reset inputs . . . . . ±20 V
On-state output voltage . . . . . 6 V
Off-state output voltage . . . . . 20 V
Continuous total dissipation at (or below) 25°C free-air temperature (see Note 2) . . . . . 1000 mW
Operating free-air temperature range . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C
Lead temperature 1/16 inch (1,6 mm) from case for 10 seconds . . . . . 260°C

NOTES: 1. Voltage values are with respect to network ground terminal unless otherwise noted.
2. For operation above 25°C free-air temperature, derate linearly at 8 mW/°C.

recommended operating conditions

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC1}	3.5	5	6	V
Supply voltage, V_{CC2}	8	15	18	V
Input voltage at analog input	0		5.5	V
Input voltage at chip enable, clock, and reset inputs			±18	V
On-state output voltage			5.5	V
Off-state output voltage			18	V
Clock frequency, f_{clock}		125	150	kHz

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electrical characteristics over recommended operating free-air temperature range, $V_{CC1} = V_{CC2} = 5$ V (unless otherwise noted)

regulator section

PARAMETER		TEST CONDITIONS		MIN	TYP‡	MAX	UNIT
V_{CC1}	Supply voltage (output)	V_{CC2} = 8 V to 18 V,	I_{CC1} = 0 to −1 mA	5	5.6	6	V
I_{CC1}	Supply current	V_{CC1} = 5 V,	V_{CC2} open		5	8	mA
I_{CC2}	Supply current	V_{CC2} = 15 V,	V_{CC1} open		7	10	mA

inputs

PARAMETER			TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage	Reset and Enable		2			V
V_{IL}	Low-level input voltage					0.8	V
I_{IH}	High-level input current	Reset, Enable, and Clock	V_I = 2.4 V		17	35	μA
			V_I = 18 V	130	220	320	
I_{IL}	Low-level input current		V_I = 0			±10	μA
I_I	Analog input current		V_I = 4 V		10	300	nA
V_{T+}	Positive-going threshold voltage	Clock input		2.5	3.5	4.5	V
V_{T-}	Negative-going threshold voltage			0.4	0.9	1.2	V
$V_{T+} - V_{T-}$	Hysteresis			2	2.6	4	V

output section

PARAMETER		TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
V_{OL}	Low-level output voltage	I_{OL} = 1.6 mA		80	400	mV
I_{OH}	High-level output current	V_{OH} = 18 V		0.1	100	μA
I_{OL}	Low-level output current	V_{OL} = 5.5 V,	5	10	15	mA

operating characteristics over recommended operating free-air temperature range, $V_{CC1} = V_{CC2} = 5$ V

PARAMETER	TEST CONDITIONS	MIN	TYP‡	MAX	UNIT
Resolution		7			Bits
Overall error				±80	mV
Differential nonlinearity	See Figure 1			±1	LSB
Zero error	Binary count = 0			±80	mV
Scale error	Binary count = 127			±80	mV
Propagation delay time from reset or enable			2		μs

‡All typical values are at $T_A = 25°C$.

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PARAMETER MEASUREMENT INFORMATION

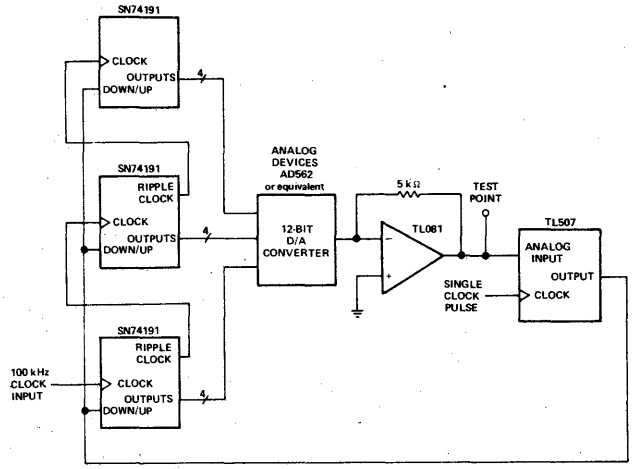


FIGURE 1—MONOTONICITY AND NONLINEARITY TEST CIRCUIT

PRINCIPLES OF OPERATION

The TL507 is a single-slope analog-to-digital converter. All single-slope converters are basically voltage-to-time or current-to-time converters. A study of the functional block diagram shows the versatility of the TL507.

An external clock signal is applied through a buffer to a negative-edge-triggered synchronous counter. Binary-weighted resistors from the counter are connected to an operational amplifier used as an adder. The operational amplifier generates a signal that ramps from $0.75 \cdot V_{CC1}$ down to $0.25 \cdot V_{CC1}$. Comparator 1 compares the ramp signal to the analog input signal. Comparator 2 functions as a fault defector. With the analog input voltage in the range $0.25 \cdot V_{CC1}$ to $0.75 \cdot V_{CC1}$, the duty cycle of the output signal is determined by the unknown analog input as shown in Figure 2 and the Function Table.

For illustration assume $V_{CC1} = 5.12$ V,

$$0.25 \cdot V_{CC1} = 1.28 \text{ V}$$

$$1 \text{ binary count} = \frac{(0.75 - 0.25)\, V_{CC1}}{128} = 20 \text{ mV}$$

$$0.75 \cdot V_{CC1} - 1 \text{ count} = 3.82 \text{ V}$$

The output is an open-collector n-p-n transistor capable of withstanding up to 18 volts in the off state. The output is current limited to the 8- to 12-milliampere range; however, care must be taken to ensure that the output does not exceed 5.5 volts in the on state.

The voltage regulator section allows operation from either an unregulated 8- to 18-volt V_{CC2} source or a regulated 3.5- to 6-volt V_{CC1} source. Regardless of which external power source is used, the internal circuitry operates at V_{CC1}. When operating from a V_{CC1} source, V_{CC2} may be connected to V_{CC1} or left open. When operating from a V_{CC2} source, V_{CC1} can be used as a reference voltage output.

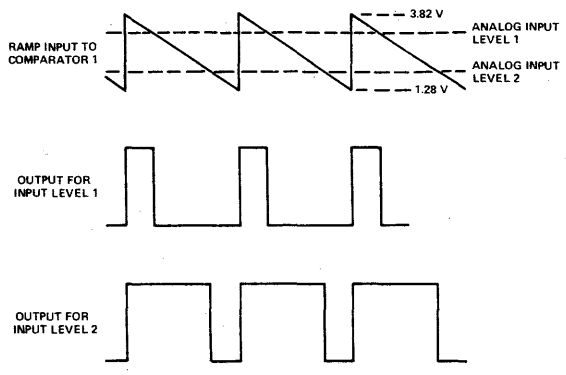


FIGURE 2

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INTRODUCTION TO MEMORY

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The manufacturers listed above are providing detailed information on their latest and most significant products.

MEMORY.....

The Master Selection Guide provides sufficient information to make initial product selections. It enables you to find the products which are most appropriate to fulfill your major requirements and then provides data for many of the more important products.

All devices that appear in this section, both in the initial selection guide and in the data pages, are included in all other indexes. These index listings lead to the page and the line on that page where each device appears.

The Memory Section provides initial selection information and data on PROMs, RAMs, and ROMs as well as other memory devices. In these particular sections, the devices are characterized by organization (words and bits/word) and by access times. In order to assure that the access times are comparable, whenever possible the values have been shown in nanoseconds over the full rated temperature range for the devices (i.e., 0° to 70°C for commercial units and −55°C to 125°C for military units). The full temperature nanosecond value is marked "nsF." When this value isn't specified, the guaranteed nanosecond value at room temperature is listed followed by "nsR." In some cases a guaranteed value has not yet been established; then the typical value is shown followed by "ns," "* ".."Typical" values are invariably much faster than the guaranteed ones so that such listings place these memories higher on the list than they otherwise would appear.

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MEMORY–Character Generators

Character Generators

Format	Number of Output Lines	Input Logic levels	Supply Voltage	Device	Source	Line
4 x 5	25	MOS	-12,14	4881	Nortec	
5 x 5	25	MOS	-12,14	4881	Nortec	
5 x 7	1	TTL	5	DM8678	National	
	5	MOS	±12	4481	Nortec	
		TTL	5	RO3-2513	GI	
				5055	†MMI	
				6055	MMI	
				5061	†MMI	
				6061	MMI	
				5155	†MMI	10
				6155	MMI	
				5161	†MMI	
				6161	MMI	
				MCM6670	**Motorola** (1490)	
				MCM6674	Motorola	
			-12,5	3258	Fairchild	
				32581	Fairchild	
				32582	Fairchild	
	7	MOS	-12(5-12)	MCS2027	MOS	
			±14	CG4100	SMC	20
				CG4103	SMC	
			-12,5	CG4103	SMC	
		TTL	5	5056	†MMI	
				6056	MMI	
				5062	†MMI	
				6062	MMI	
				5156	†MMI	
				6156	MMI	
				5162	†MMI	
				6162	MMI	30
			±12	EA40105	EA	
			-12,5	3257	Fairchild	
				RO5-2240S	GI	
				MK2302	Mostek	
	8	MOS	5	MK34073-3	Mostek	
				MSM575A	OKI	
		TTL	±5,12	TMS4710	TI	
	10	TTL	-12,5	MK2408	Mostek	
5 x 8	5	MOS	±12	MM4240	†National	
	8	MOS	5*	MK34073-3	Mostek	40
6 x 8	8	TTL	-12,5	MM4241	†National	
				MM5241	National	
7 x 8	4	TTL	5	N8228CB	Signetics	
	10	MOS	±12	EA4004	EA	
	35	MOS	-12,14	4881	Nortec	
7 x 9	1	TTL	5	DM8678	National	
			-12,5	MM4220	†National	
				MM5220	National	
	7	TTL	-12,5	S8564	AMI	
				3260	Fairchild	50
			5	5071	†MMI	
				6071	MMI	
				5072	†MMI	
				6072	MMI	
				5171	†MMI	
				6171	MMI	
				5172	†MMI	
				6172	MMI	
				5290	†MMI	

(Continued)

Character Generators (Cont'd.)

Format	Number of Output Lines	Input Logic levels	Supply Voltage	Device	Source	Line
7 x 9	7	TTL	5		(Cont'd.)	60
				6290	MMI	
				5291	†MMI	
				6291	MMI	
				MCM66700	**Motorola** (1495)	
				MCM66710	Motorola	
				MCM66714	Motorola	
				MCM66720	Motorola	
				MCM66730	Motorola	
				MCM66734	Motorola	
				MCM66740	Motorola	70
				MCM66750	Motorola	
				MCM66751	Motorola	
				MCM66760	Motorola	
				MCM66770	Motorola	
				MCM66780	Motorola	
				MCM66790	Motorola	
				2609	Signetics	
			-3,5,12*	MCM6570	Motorola	
				MCM6571A	Motorola	
				MCM6572	Motorola	80
				MCM6573	Motorola	
				MCM6573A	Motorola	
				MCM6574	Motorola	
				MCM6575	Motorola	
				MCM6576	Motorola	
				MCM6577	Motorola	
				MCM6578	Motorola	
				MCM6579	Motorola	
				NC6570	Nitron	
				NC6571	Nitron	90
				NC6571A	Nitron	
				NC6572	Nitron	
				NC6573	Nitron	
				NC6574	Nitron	
				NC6575	Nitron	
				NC6576	Nitron	
				NC6580	Nitron	
				NC6581	Nitron	
				NC6583	Nitron	
	9	MOS	-12,-24	EA3815	EA	100
			±12	EA4001	EA	
		TTL	5	5073	†MMI	
				6073	MMI	
				5074	†MMI	
				6074	MMI	
				5173	†MMI	
				6173	MMI	
				5174	†MMI	
				6174	MMI	
			-3,5,12	MCM6580	Motorola	110
				MCM6581	Motorola	
				MCM6583	Motorola	
				NC6580	Nitron	
				NC6581	Nitron	
				NC6583	Nitron	
7 x 10	7	TTL	±12	EA4016	EA	
7 x 11	1	TTL	5	CG5004L	SMC	
				CG8002	SMC	
9 x 9	9	TTL	-12,5	RO5-5184	GI	
			5	5292	†MMI	120
				6292	MMI	
				5293	†MMI	
				6293	MMI	

† Military Temperature Range (−55° to 125°C)

* Typical Values

MEMORY–Code Converters

Code Converters

Code Conversion From	To	Bits In	Bits Out	Process	Supply Voltage	Device	Source	Line
ASCII-BCDIC		6	6	PMOS	±12	MM4220LR	† National	
						MM5220LR	National	
ASCII-EBCDIC		6	7	PMOS	±12	MM4220EK	† National	
						MM5220EK	National	
		7	8	PMOS	±12	MM4220AE	† National	
						MM5220AE	National	
					-12,5	MM4221RR	† National	
						MM5221RR	National	
		8	8	PMOS	-12,5	MK2503	Mostek	
						MK2601	Mostek	10
					±12	MM4230QY	† National	
						MM5230QY	National	
			10	PMOS	±12	EA4015	EA	
ASCII-HOLLERITH								
		8	8	PMOS	±12	MM4231BUS	National	
						MM5231BUS	National	
		9	10	PMOS	-24	EA4035	EA	
ASCII-RS244A and Vice Versa								
		6	8	PMOS	-12,5	MM4221RQ	† National	
						MM5221RQ	National	20
ASCII-SELECTRIC								
		7	7	PMOS	±12	MM4230KP	† National	
						MM5230KP	National	
BCD-BINARY		6	6	Bipolar	5	SN54184	† TI	
						SN74184	TI	
BCDIC-ASCII		6	7	PMOS	±12	MM4220AP	† National	
						MM5220AP	National	
						MM4220LR	† National	
						MM5220LR	National	
BCDIC-EBCDIC		6	7	PMOS	±12	MM4220EK	† National	
						MM4230JT	† National	30
						MM5220EK	National	
						MM5230JT	National	
Baudot-ASCII		5	8	PMOS	±12	MM4220BL	† National	
						MM5220BL	National	
BINARY-BCD		6	6	Bipolar	5	SN54185A	† TI	
						SN74185A	TI	
EBCDIC-ASCII		8	8	Bipolar	5	N8204	Signetics	
				PMOS	-12,5	MK2503	Mostek	
						MK2601	Mostek	40
					±12	MM4230QX	† National	
						MM4231RP	† National	
						MM5230QX	National	
						MM5231RP	National	
			10	PMOS	±12	EA4015	EA	
		12	8	Bipolar	5	DM8576AAA	National	
EBCDIC-DCDIC		7	6	PMOS	±12	MM4230JT	† National	
						MM5230JT	National	
EBCDIC-HOLLERITH								
		9	10	MOS	-24	EA4034	EA	50
				PMOS	-24	EA4035	EA	
EBCDIC-SELECTRIC								
		8	8	PMOS	±12	MM4230FE	† National	
						MM5230FE	National	
HOLLERITH-ASCII								
		8	8	PMOS	±12	MM4230BO	† National	
						MM5230BO	National	
						MM4231BUS	† National	

(Continued)

Code Converters (Cont'd.)

Code Conversion From	To	Bits In	Bits Out	Process	Supply Voltage	Device	Source	Line
HOLLERITH-ASCII								
		8	8	PMOS	±12		(Cont'd.)	60
						MM5231BUS	† National	
HOLLERITH-EBCDIC								
		8	8	PMOS	±12	MM4230QW	† National	
						MM5230QW	National	
		9	10	PMOS	-24	EA4034	EA	
Multiple SELECTRIC, HOLLERITH-EBCDIC-ASCII and Vice Versa								
				NMOS	-3,5,12	MCM6561	Motorola	
						MCM6562	Motorola	
						NC6561	Nitron	70
Multiple ASCII-SELECTRIC, EBCDIC, HOLLERITH								
				NMOS	-3,5,12	MCM6591	Motorola	
						NC6591	Nitron	
					±5	MCM68316	Motorola	
SELECTRIC-EBCDIC								
		8	8	PMOS	±12	MM4230FE	† National	
						MM5230FE	National	

† Military Temperature Range (−55° to 125°C)

* Typical Values

Bold face indicates additional data is provided on the page noted.

MEMORY–EAROMs, FIFOs, LIFOs

Electrically Alterable ROMs

Words	Bits Per Word	Access Time (Max)	Output	Supply Voltage	Device	Source
1	1			±20	NOM201	Plessey
	2			±20	NOM202	Plessey
	4			±20	NOM204	Plessey
8	8			±20	NOM401	Plessey
21	16	10 µsF		-20,10	NC7033	Nitron
32	16	3 µsF	TS	-28,5	ER2051	GI
		4 µsF	TS	-29,5	NCR2051	NCR
					NC2051	Nitron
64	4	2 µsF		±15,5	NC7040	Nitron
	8	4 µsF	TS	-29,5	ER2055	GI
					NCR2055	NCR
					NC2055	Nitron
100	14	3.4 msF	Serial	-35	ER1400	GI
					NC1400	Nitron
128	8	850 nsF	TS	-15,-12,5,25		
					NC1721	Nitron
		1.2 µsF	TS	-25,±5	NC7053	Nitron
256	4	850 nsF	TS	-15,-12,5,25		
					ER1711	GI
					NCR1711	NCR
					NC1711	Nitron
		1.2 µsF	TS	-25,±5	NC7054	Nitron
		1.5 µsF	TS	-15,5	M58656	Mitsubishi
				-15,5	TMM142	Toshiba
		2 µsF		-24,±12,30		
					NCR1105	NCR
					NC1105	Nitron
	8	800 nsF	TS	-40,-5,-2,5, 12,26,36		
					µPD454	NEC Micro
		950 nsF	TS	-15,-12,5,25		
					NC1731	Nitron
	9	1 µsF	TS	-30,-12	MN1102	Panasonic
1024	4	900 nsF	TS	-30,-12,5	ER3400	GI
					NCR2450	NCR
					NC2450	Nitron
		2 µsF	TS	-23,-14,±5		
					ER2401A	GI
					M58561	Mitsubishi
					NCR2401	NCR
					NC2401	Nitron
		3 µsF	TS	5,-14,-19	M5G2401	Mitsubishi
	8	450 nsF	TS	-40,-5,-2,5,12,26,36		
					µPD458	NEC Micro
2048	4	1.65 µsF	TS	-23,-14,±5		
					ER2805	GI
					NCR2810	NCR
					NC2805	Nitron
					NC2810	Nitron
		2.6 µsF	TS	-23,-14,±5		
					ER2800	GI

First-In First-Out

Words	Bits/ Word	Data Rate MHz(max)	Supply Voltage	Device	Source
16	4	8.0*	3-15	CD40105B	†RCA
				CD40105BE	RCA
		10.0	5	**9403C**	**Fairchild (1893,1896)**
				9403M	**†Fairchild (1893,1896)**
		12.0	5	SN54LS222	†TI
				SN74LS222	TI
				SN54LS224	†TI
				SN74LS224	TI
	5	10.0	5	SN74S225	TI
24	4	2.5	5-16	MS618	†RTC
32	8	0.25	-12, 5	MP3812	Plessey
		0.5	-12,5	AM2812C	AMD
				AM2812L	AMD
		1.0	-12,5	AM2812AC	AMD
				AM2812AL	AMD
	9	0.5	-12,5	AM2813C	AMD
				AM2813L	AMD
		1.0	-12,5	AM2813AC	AMD
				AM2813AL	AMD
40	9	0.25	-12,5	FR1502E-02	Western
		0.5	-12,5	FR1502E-01	Western
		1.0	-12,5	33512	Fairchild
				FR1502E	Western
		2.0	-12,5	33511	Fairchild
64	4	0.7	-12,5	3341C	AMD
				3341	Fairchild
		1.0	-12,5	AM2841C	AMD
				AM2841M	†AMD
				3341A	Fairchild
		1.2	-12,5	2841A	AMD
		7.0	5	**57401**	**†MMI (1472)**
		8.0	5	**9423**	**Fairchild (1893)**
		10.0	5	**67401**	**MMI (1472)**
		15*	5	**57401A**	**†MMI (1476)**
				67401A	**MMI (1476)**
	5	15*	5	**57402A**	**†MMI (1476)**
				67402A	**MMI (1476)**

Last-In First-Out

Words	Bits/ Word	Data Rate MHz(max)	Supply Voltage	Device	Source
16	4	10.5	5	**9406C**	**Fairchild (1893)**
				9406M	**Fairchild (1893)**
81	4	1.0	5	SR5018	SMC
133	4	1.0	5	SR5017	SMC

† Military Temperature Range (−55° to 125°C) ns*—Nanoseconds Typical nsF—Nanoseconds over Full Temperature Range nsR—Nanoseconds at Room Temperature

OC—Open Collector TS—Three-State OE—Open Emitter

MEMORY–PLAs

PLAs

Organization	Propagation Time	Output	Supply Voltage	Device	Source		Line
48 Product Terms, 16 Inputs, Field Programmable							
	50 nsF	OC	5	**93458**	**Fairchild**	**(1269)**	
				82S101	MMI		
				MC29101C	Motorola		
				MC82101C	Motorola		
				N82S101	**Signetics**	**(1684)**	
		TS	5	**93459**	**Fairchild**	**(1269)**	
				82S100	MMI		
				MC29100C	Motorola		
				MC82100C	Motorola		10
				N82S100	**Signetics**	**(1684)**	
	80 nsF	OC	5	MC29101M	† Motorola		
				MC82101M	† Motorola		
				S82S101	**† Signetics**	**(1684)**	
		TS	5	MC29100M	† Motorola		
				MC82100M	† Motorola		
				S82S100	**† Signetics**	**(1684)**	
48 Product Terms, 16 Inputs, Factory Programmable							
	50 nsF	OC	5	N82S201	Signetics		
		TS	5	N82S200	Signetics		20
	80 nsF	OC	5	S82S201	† Signetics		
		TS	5	S82S200	† Signetics		
48 Product Terms, 14 Inputs, Field Programmable							
	100 nsF	OC	5	IM5200	Intersil		
50 Product Terms, 12 Inputs, 6 Outputs, Field Programmable							
	35 ns*	TS	5	SN54S330	† TI		
				SN74S330	TI		
		—	5	SN54S331	† TI		
				SN74S331	TI		30
96 Product Terms, 14 Inputs, Factory Programmable							
	150 nsF	—	5	DM7575	† National		
				DM7576	† National		
				DM8575	National		
				DM8576	National		
Field Programmable Array Logic; AND-OR Gate Array							
	25 ns*	TS	5	**PAL10H8C**	**MMI**	**(1479)**	
				PAL10H8M	**† MMI**	**(1479)**	
				PAL12H6C	**MMI**	**(1479)**	
				PAL12H6M	**† MMI**	**(1479)**	40
				PAL14H4C	**MMI**	**(1479)**	
				PAL14H4M	**† MMI**	**(1479)**	
				PAL16C1C	**MMI**	**(1479)**	
				PAL16C1M	**† MMI**	**(1479)**	
				PAL16H2C	**MMI**	**(1479)**	
				PAL16H2M	**† MMI**	**(1479)**	
				PAL10H8C	Raytheon		
				PAL10H8M	† Raytheon		
				PAL12H6C	Raytheon		
				PAL12H6M	† Raytheon		
				PAL14H4C	Raytheon		
				PAL14H4M	† Raytheon		
				PAL16C1C	Raytheon		
				PAL16C1M	† Raytheon		
				PAL16H2C	Raytheon		
				PAL16H2M	† Raytheon		
Field Programmable Array Logic; AND-OR INVERT Gate Array							
	25 ns*	TS	5	**PAL10L8C**	**MMI**	**(1479)**	
				PAL10L8M	**† MMI**	**(1479)**	
				PAL12L6C	**MMI**	**(1479)**	
				PAL12L6M	**† MMI**	**(1479)**	
				PAL14L4C	**MMI**	**(1479)**	
						(Continued)	

PLAs (Cont'd.)

Organization	Propagation Time	Output	Supply Voltage	Device	Source		Line
	25 ns*	TS	5			(Cont'd.)	
				PAL14L4M	**† MMI**	**(1479)**	
				PAL16L2C	**MMI**	**(1479)**	
				PAL16L2M	**† MMI**	**(1479)**	
				PAL16L8C	**MMI**	**(1479)**	
				PAL16L8M	**† MMI**	**(1479)**	70
				PAL10L8C	Raytheon		
				PAL10L8M	† Raytheon		
				PAL12L6C	Raytheon		
				PAL12L6M	† Raytheon		
				PAL14L4C	Raytheon		
				PAL14L4M	† Raytheon		
				PAL16L2C	Raytheon		
				PAL16L2M	† Raytheon		
				PAL16L8C	Raytheon		
				PAL16L8M	† Raytheon		80
Field Programmable Logic Array; AND-OR INVERT Gate Array with registers							
	25 ns*	TS	5	**PAL16R4C**	**MMI**	**(1479)**	
				PAL16R4M	**† MMI**	**(1479)**	
				PAL16R6C	**MMI**	**(1479)**	
				PAL16R6M	**† MMI**	**(1479)**	
				PAL16R8C	**MMI**	**(1479)**	
				PAL16R8M	**† MMI**	**(1479)**	
				PAL16R4C	Raytheon		
				PAL16R4M	† Raytheon		90
				PAL16R6C	Raytheon		
				PAL16R6M	† Raytheon		
				PAL16R8C	Raytheon		
				PAL16R8M	† Raytheon		
Field Programmable Array Logic; AND-OR-XOR Gate Array with registers							
	25 ns*	TS	5	**PAL16X4C**	**MMI**	**(1479)**	
				PAL16X4M	**† MMI**	**(1479)**	
				PAL16X4C	Raytheon		
				PAL16X4M	† Raytheon		100
Field Programmable Array Logic; AND-CARRY-OR-XOR Invert Gate Array with registers							
	25 ns*	TS	5	**PAL16A4C**	**MMI**	**(1479)**	
				PAL16A4M	**† MMI**	**(1479)**	
				PAL16A4C	Raytheon		
				PAL14A4M	† Raytheon		
Field Programmable Gate Array, 16 Inputs, 9 AND/NAND Gates, 9 Outputs, Field Programmable							
	40 nsF	OC	5	**N82S102**	**Signetics**	**(1687)**	
		TS	5	**N82S103**	**Signetics**	**(1687)**	110
	50 nsF	OC	5	**S82S102**	**† Signetics**	**(1687)**	
		TS	5	**S82S103**	**† Signetics**	**(1687)**	
Field Programmable Multiplexer, (10 inputs, four 10x8 programmable arrays, four 8:1 addressable multiplexers, four outputs)							
	55 nsF	TS	5	29693C	Raytheon		
	75 nsF	TS	5	29693M	† Raytheon		
Field Programmable ROM Patch, for correcting or changing the programs in large ROMs							
	—	OC	5	**N82S106**	**Signetics**	**(1696)**	120
		TS	5	**N82S107**	**Signetics**	**(1696)**	
Field Programmable Logic Sequencer, 48 Transition Terms, 16 Inputs, 8 Outputs							
	90 nsF	OC	5	**N82S104**	**Signetics**	**(1690)**	
		TS	5	**N82S105**	**Signetics**	**(1690)**	

† Military Temperature Range (−55° to 125°C) ns*—Nanoseconds Typical nsF—Nanoseconds over Full Temperature Range nsR—Nanoseconds at Room Temperature

OC—Open Collector TS—Three-State OE—Open Emitter

Bold face indicates additional data is provided on the page noted.

MEMORY–PROMs

PROMs

Organization	Access Time (Max)	Type	Output	No. Pins	Supply Voltage	Device	Source		Line
32x8	15 nsF	TTL	OC	16	5	**SM74S188**	**Supertex**	**(1704)**	
			TS	16	5	**SM74S288**	**Supertex**	**(1704)**	
	20 nsF	TTL	OC	16	5	**MM74S188**	**† Supertex**	**(1704)**	
			TS	16	5	**MM74S288**	**† Supertex**	**(1704)**	
	20 nsR	ECL	OE	16	-5.2	SN10139	TI		
	22 nsF	ECL	OE	16	-5.2	10139	Signetics		
	25 nsF	ECL	OE	16	-5.2	MCM10139	Motorola		
		TTL	OC	16	5	**63S080**	**MMI**	**(1453)**	
			TS	16	5	**63S081**	**MMI**	**(1453)**	
	35 nsF	TTL	OC	16	5	**53S080**	**† MMI**	**(1453)**	10
						63LS080	**MMI**	**(1458)**	
						DM74S188	National		
			TS	16	5	**53S081**	**† MMI**	**(1453)**	
						63LS081	**MMI**	**(1458)**	
						DM74S288	National		
	40 nsF	TTL	OC	16	5	AM27S18C	AMD		
						AM29750AC	AMD		
						HM7602-5	**Harris**	**(1284)**	
						DM54S188	† National		
						SN74S188	**TI**	**(1708)**	20
			TS	16	5	AM27S19C	AMD		
						AM29751AC	AMD		
						HM7603-5	**Harris**	**(1284)**	
						SN74S288	**TI**	**(1708)**	
	45 nsF	TTL	OC	16	5	**53LS080**	**† MMI**	**(1458)**	
			TS	16	5	**53LS081**	**† MMI**	**(1458)**	
						DM54S288	† National		
	50 nsF	TTL	OC	16	5	AM27S18M	† AMD		
						AM29750AM	† AMD		
						HM7602-2	**† Harris**	**(1284)**	30
						M54730	Mitsubishi		
						6330-1	**MMI**	**(1449)**	
						N82S23	**Signetics**	**(1680)**	
						SN54S188	**† TI**	**(1708)**	
			TS	16	5	AM27S19M	† AMD		
						AM29751AM	† AMD		
						HM7603-2	**† Harris**	**(1284)**	
						6331-1	**MMI**	**(1449)**	
						N82S123	**Signetics**	**(1680)**	
						SN54S288	**† TI**	**(1708)**	40
	50 nsR	TTL	OC	16	5	HPROM8256-2	† Harris		
						HPROM8256-5	Harris		
						IM5600C	Intersil		
						IM5600M	† Intersil		
						SN54188A	† TI		
						SN74188A	TI		
			TS	16	5	IM5610C	Intersil		
						IM5610M	† Intersil		
	60 nsF	TTL	OC	16	5	**5330-1**	**† MMI**	**(1449)**	
			TS	16	5	**5331-1**	**† MMI**	**(1449)**	50
	65 nsF	TTL	OC	16	5	**S82S23**	**† Signetics**	**(1680)**	
			TS	16	5	**S82S123**	**† Signetics**	**(1680)**	
	70 nsR	TTL	OC	16	5	IM5600CF	Intersil		
			TS	16	5	IM5610CF	Intersil		
	80 nsF	TTL	OC	16	5	MSL8515	OKI		
			TS	16	5	MSL8516	OKI		
64x8	75 nsR	TTL	OC	24	5	JAN38510/201	† Harris		
						HPROM0512-2	**† Harris**	**(1346)**	

(Continued)

PROMs (Cont'd.)

Organization	Access Time (Max)	Type	Output	No. Pins	Supply Voltage	Device	Source		Line
								(Cont'd.)	
64x8	75 nsR	TTL	OC	24	5	**HPROM0512-5**	**Harris**	**(1346)**	60
						SN54186	† TI		
						SN74186	TI		
	125 nsF	TTL	OC	24	5	MCM5003A	Motorola		
						MCM5303A	† Motorola		
			—	24	5	MCM5004A	Motorola		
						MCM5304A	† Motorola		
256x4	12 ns*	ECL	OE	16	-5.2	GXB1049	Siemens		
	15 ns*	ECL	OE	16	-5.2	F10416C	Fairchild		
	20 nsR	ECL	OE	16	-5.2	10149	Signetics		
	30 nsF	ECL	OE	16	-5.2	MCM10149	Motorola		70
	35 nsF	TTL	OC	16	5	63PS140	MMI		
			TS	16	5	63PS141	MMI		
	40 nsF	TTL	OC	16	5	**HM7610A-5**	**Harris**	**(1292)**	
						N82S27	Signetics		
			TS	16	5	**HM7611A-5**	**Harris**	**(1292)**	
	45 nsF	TTL	OC	16	5	AM27S20C	AMD		
						AM29760AC	AMD		
						93417C	**Fairchild**	**(1258)**	
						53PS140	† MMI		
						63S140	**MMI**	**(1453)**	80
			TS	16	5	AM27S21C	AMD		
						AM29761AC	AMD		
						93427C	**Fairchild**	**(1258)**	
						53PS141	† MMI		
						63S141	**MMI**	**(1453)**	
	50 nsF	TTL	OC	16	5	DM74S387	National		
						N82S126	**Signetics**	**(1680)**	
			TS	16	5	DM74S287	National		
						N82S129	**Signetics**	**(1680)**	
	55 nsF	TTL	OC	16	5	**53S140**	**† MMI**	**(1453)**	90
						6300-1	**MMI**	**(1449)**	
						63LS140	**MMI**	**(1458)**	
			TS	16	5	**53S141**	**† MMI**	**(1453)**	
						6301-1	**MMI**	**(1449)**	
						63LS141	**MMI**	**(1458)**	
	60 nsF	TTL	OC	16	5	AM27S20M	† AMD		
						AM29760AM	AMD		
						93417M	**† Fairchild**	**(1258)**	
						HM7610-5	**Harris**	**(1284)**	
						HM7610A-2	**† Harris**	**(1292)**	100
						M54700	Mitsubishi		
						DM54S387	† National		
						29662C	**Raytheon**	**(1665)**	
			TS	16	5	AM27S21M	† AMD		
						AM29761AM	† AMD		
						93427M	**† Fairchild**	**(1258)**	
						HM7611-5	**Harris**	**(1284)**	
						HM7611A-2	**† Harris**	**(1292)**	
						DM54S287	† National		
						29663C	**Raytheon**	**(1665)**	110
	60 nsR	TTL	OC	16	5	IM5603AC	Intersil		
						IM5603AM	† Intersil		
						μPB403	NEC Micro		
			TS	16	5	IM5623C	Intersil		
						IM5623M	† Intersil		
	65 nsF	TTL	OC	16	5	**53LS140**	**† MMI**	**(1458)**	
						SN74S387	**TI**	**(1708)**	

(Continued)

† Military Temperature Range (−55° to 125°C) ns*—Nanoseconds Typical nsF—Nanoseconds over Full Temperature Range nsR—Nanoseconds at Room Temperature

OC—Open Collector TS—Three-State OE—Open Emitter

MEMORY–PROMs (Cont'd)

PROMs (Cont'd.)

Organization	Access Time (Max)	Type	Output	No. Pins	Supply Voltage	Device	Source		Line
								(Cont'd.)	
256x4	65 nsF	TTL	TS	16	5	**53LS141**	**† MMI**	**(1458)**	
						SN74S287	**TI**	**(1708)**	
	70 nsF	TTL	OC	16	5	**29660C**	**Raytheon**	**(1664)**	
						S82S126	**† Signetics**	**(1680)**	
			TS	16	5	**29661C**	**Raytheon**	**(1664)**	
						S82S129	**† Signetics**	**(1680)**	
	70 nsR	TTL	OC	16	5	HPROM1024A-2	† Harris		
						HPROM1024A-5	Harris		
			TS	16	5	HPROM1024-2	† Harris		10
						HPROM1024-5	Harris		
	75 nsF	TTL	OC	16	5	**HM7610-2**	**Harris**	**(1284)**	
						5300-1	**† MMI**	**(1449)**	
						29662M	**† Raytheon**	**(1665)**	
						SN54S387	**† TI**	**(1708)**	
			TS	16	5	**HM7611-2**	**† Harris**	**(1284)**	
						5301-1	**† MMI**	**(1449)**	
						29663M	**† Raytheon**	**(1665)**	
						SN54S287	**† TI**	**(1708)**	
	80 nsF	TTL	OC	16	5	**29660M**	**† Raytheon**	**(1664)**	20
			TS	16	5	**29661M**	**† Raytheon**	**(1664)**	
	100 nsF	TTL	OC	16	5	MSL8520	OKI		
			TS	16	5	MSL8521	OKI		
	350 nsF	CMOS	TS	16	4-11	**HM6611A-2**	**† Harris**	**(1401)**	
						HM6611A-9	**Harris**	**(1401)**	
	450 nsF	CMOS	TS	16	5	**HM6611-2**	**† Harris**	**(1401)**	
						HM6611-9	**Harris**	**(1401)**	
				28	5	**HM6661**	**Harris**	**(1405)**	
	650 nsF	CMOS	TS	16	5	**HM6611D-5**	**Harris**	**(1401)**	
256x8	45 nsF	TTL	OC	20	5	**63S280**	**MMI**	**(1453)**	30
						63PS280	MMI		
			TS	20	5	**63S281**	**MMI**	**(1453)**	
						63PS281	MMI		
	55 nsF	TTL	OC	20	5	**53S280**	**† MMI**	**(1453)**	
						53PS280	† MMI		
			TS	20	5	**53S281**	**† MMI**	**(1453)**	
						53PS281	† MMI		
	60 nsF	TTL	TS	24	5	**HM7625R-5**	**Harris**	**(1300)**	
						N82S114	**Signetics**	**(1680)**	
	65 nsF	TTL	OC	20	5	**63LS280**	**MMI**	**(1458)**	40
			TS	20	5	**63LS281**	**MMI**	**(1458)**	
	70 nsF	TTL	OC	20	5	**6308-1**	**MMI**	**(1449)**	
						29602C	**Raytheon**	**(1653)**	
						SN74S470	**TI**	**(1708)**	
				24	5	**6335-1**	**† MMI**	**(1449)**	
			TS	20	5	**6309-1**	**MMI**	**(1449)**	
						29603C	**Raytheon**	**(1653)**	
						SN74S471	**TI**	**(1708)**	
				24	5	**HM7629-5**	**Harris**	**(1302)**	
						6336-1	**MMI**	**(1449)**	50
						63RA281	MMI		
						63RA283	MMI		
	75 nsF	TTL	OC	20	5	**53LS280**	**† MMI**	**(1458)**	
						29600C	**Raytheon**	**(1652)**	
			TS	20	5	**53LS281**	**† MMI**	**(1458)**	
						29601C	**Raytheon**	**(1652)**	

(Continued)

PROMs (Cont'd.)

Organization	Access Time (Max)	Type	Output	No. Pins	Supply Voltage	Device	Source		Line
								(Cont'd.)	
256x8	80 nsF	TTL	OC	20	5	**5308-1**	**† MMI**	**(1449)**	
						29602M	**† Raytheon**	**(1653)**	
						SN54S470	**† TI**	**(1708)**	60
				24	5	**5335-1**	**† MMI**	**(1449)**	
			TS	20	5	**5309-1**	**† MMI**	**(1449)**	
						29603M	**† Raytheon**	**(1653)**	
						SN54S471	**† TI**	**(1708)**	
				24	5	**HM7625R-2**	**† Harris**	**(1300)**	
						5336-1	**† MMI**	**(1449)**	
						53RA281	† MMI		
						53RA283	† MMI		
	90 nsF	TTL	OC	20	5	**29600M**	**† Raytheon**	**(1652)**	
				24	5	63135-1	MMI		70
			TS	20	5	**29601M**	**† Raytheon**	**(1652)**	
				24	5	**S82S114**	**† Signetics**	**(1680)**	
	500 nsF	TTL	TS	16	5	**HM76LS03-5**	**Harris**	**(1288)**	
	550 nsF	Erasable	TS	24	-9,5	1702A-1	AMD		
						1702AL-1	AMD		
	650 nsF	Erasable	TS	24	-9,5	1702A-2	AMD		
						1702AL-2	AMD		
						1702A-2	Intel		80
						1702AL-2	Intel		
	750 nsF	Erasable	TS	24	-9,5	9702-1	AMD		
						MM1702AQ-1	National		
	800 nsF	Electrically Erasable	TS	24	5,12	µPD454	NEC Micro		
						HM7611A-2	**† Harris**	**(1292)**	
	850 nsF	Erasable	TS	24	-9,5	M1702A	† Intel		
	1 µsF	Erasable	TS	24	-9,5	1702A	AMD		90
						1702AL	AMD		
						1702A	Intel		
						1702AL	Intel		
						M5L1702A	Mitsubishi		
						MM1702AQ	National		
						MSM2750-1A	OKI		
					-12,5	MM4203Q	National		
						MM5203Q	National		
	1.2 µsF	Erasable	TS	24	-9,5	MSM2750-2A	OKI		100
	1.3 µsF	Erasable	TS	24	-9,5	8702A	AMD		
						8702A	Intel		
						MM8702A	National		
	1.5 µsF	Erasable	TS	24	-9,5	1702A-6	AMD		
						1702A-6	Intel		
						M58563-1	Mitsubishi		
						MM1702AQ-6	National		110
	1.7 µsF	Erasable	TS	24	-10,5	4702A	AMD		
						4702A	Intel		
						MM4702A	National		

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† Military Temperature Range (−55° to 125°C) ns*—Nanoseconds Typical nsF—Nanoseconds over Full Temperature Range nsR—Nanoseconds at Room Temperature

OC—Open Collector TS—Three-State OE—Open Emitter

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MEMORY–PROMs (Cont'd)

Organization	Access Time (Max)	Type	Output	No. Pins	Supply Voltage	Device	Source	Line
PROMs							**(Cont'd.)**	
256x8							(Cont'd.)	
	2.3 µsF	Erasable						
			TS	24	-9,5	8702A-4 AMD MM8702A-4 National		
512x4	35 nsF	TTL	OC	16	5	63PS240 MMI		
			TS	16	5	63PS241 MMI		
	45 nsF	TTL	OC	16	5	**HM7620A-5 Harris (1298)** 53PS240 † MMI **63S240 MMI (1453)**		
			TS	16	5	**HM7621A-5 Harris (1298)** 53PS241 † MMI **63S241 MMI (1453)**		10
	50 nsF	TTL	OC	16	5	AM27S12C AMD AM29770C AMD **93436C Fairchild (1260)** **N82S130 Signetics (1680)**		
			TS	16	5	AM27S13C AMD AM29771C AMD **93446C Fairchild (1260)** **N82S131 Signetics (1680)**		
	55 nsF	TTL	OC	16	5	**53S240 † MMI (1453)** **63LS240 MMI (1458)** DM74S570 National **29610C Raytheon (1654)**		20
			TS	16	5	**53S241 † MMI (1453)** **63LS241 MMI (1458)** DM74S571 National **29611C Raytheon (1654)**		
	60 nsF	TTL	OC	16	5	AM27S12M † AMD AM29770M † AMD **93436M † Fairchild (1260)** **HM7620A-2 † Harris (1298)** **6305-1 MMI (1449)** **29612C Raytheon (1655)**		30
			TS	16	5	AM27S13M † AMD AM29771M † AMD **93446M † Fairchild (1260)** **HM7621A-2 † Harris (1298)** **6306-1 MMI (1449)** **29613C Raytheon (1655)**		
	65 nsF	TTL	OC	16	5	**53LS240 † MMI (1458)** DM54S570 † National		40
			TS	16	5	**53LS241 † MMI (1458)** DM54S571 † National		
	70 nsF	TTL	OC	16	5	MB7058 Fujitsu **HM7620-5 Harris (1284)** MCM7620C Motorola **S82S130 † Signetics (1680)**		
			TS	16	5	MB7053 Fujitsu **HM7621-5 Harris (1284)** MCM7621C Motorola **S82S131 † Signetics (1680)**		50
	70 nsR	TTL	OC	16	5	IM5604C Intersil IM5604M † Intersil **29610M † Raytheon (1654)**		
			TS	16	5	IM5624C Intersil IM5624M † Intersil **29611M † Raytheon (1654)**		
	75 nsF	TTL	OC	16	5	**5305-1 † MMI (1449)** **29612M † Raytheon (1655)**		
							(Continued)	

Organization	Access Time (Max)	Type	Output	No. Pins	Supply Voltage	Device	Source	Line
PROMs							**(Cont'd.)**	
512x4	75 nsF	TTL					(Cont'd.)	60
			TS	16	5	**5306-1 † MMI (1449)** **29613M † Raytheon (1655)**		
	85 nsF	TTL	OC	16	5	**HM7620-2 † Harris (1284)** MCM7620M † Motorola		
			TS	16	5	**HM7621-2 † Harris (1284)** MCM7621M † Motorola		
	1 µsF	Erasable						
			TS	24	-9,±5	TMM121-1 Toshiba		
	1 µsR	Erasable						
			TS	24	-12,5	MM4203Q National MM5203Q National		70
	1.5 µsF	Erasable						
			TS	24	-9,±5	TMM121 Toshiba		
512x8	45 nsF	TTL	OC	20	5	**N82S146 Signetics (1680)**		
			TS	20	5	**N82S147 Signetics (1680)**		
	50 nsF	TTL	OC	20	5	**63S480 MMI (1453)** 63PS480 MMI		
				24	5	**HM7640A-5 Harris (1304)** **63S482 MMI (1453)** 63PS482 MMI **29624C Raytheon (1658)**		80
			TS	20	5	**63S481 MMI (1453)** 63PS481 MMI		
				24	5	**HM7641A-5 Harris (1304)** **63S483 MMI (1453)** 63PS483 MMI **29625C Raytheon (1658)**		
	50 ns*	TTL	OC	22	5	AM27S26 AMD		
			TS	22	5	AM27S27 AMD		
	55 nsF	TTL	OC	20	5	9 AM27S28C AMD **29620C Raytheon (1656)**		90
				24	5	AM27S30C AMD **93438C Fairchild (1262)** **29626C Raytheon (1659)**		
			TS	20	5	AM27S29C AMD **29621C Raytheon (1656)**		
				24	5	AM27S31C AMD **93448C Fairchild (1262)** **29627C Raytheon (1659)**		
	60 nsF	TTL	OC	20	5	**HM7648-5 Harris (1320)** **53S480 † MMI (1453)** 53PS480 † MMI DM74S473 National		100
				24	5	**HM7640AR-5 Harris (1306)** 3604A-2 Intel **53S482 † MMI (1453)** 53PS482 † MMI **N82S140 Signetics (1680)**		
			TS	20	5	**HM7649-5 Harris (1320)** **53S481 † MMI (1453)** 53PS481 † MMI DM74S472 National		110
				24	5	AM27S15C AMD **HM7641AR-5 Harris (1306)** **HM7647R-5 Harris (1318)** 3624A-2 Intel **53S483 † MMI (1453)** 53PS483 † MMI		
							(Continued)	

† Military Temperature Range (−55° to 125°C)
ns*—Nanoseconds Typical
nsF—Nanoseconds over Full Temperature Range
nsR—Nanoseconds at Room Temperature
OC—Open Collector
TS—Three-State
OE—Open Emitter

MEMORY–PROMs (Cont'd)

PROMs (Cont'd.)

Organization	Access Time (Max)	Type	Output	No. Pins	Supply Voltage	Device	Source		Line
512x8	60 nsF	TTL	TS	24	5			(Cont'd.)	
						N82S115	**Signetics**	**(1680)**	
						N82S141	**Signetics**	**(1680)**	
	65 nsF	TTL	OC	20	5	AM27S28M	† AMD		
						63LS480	**MMI**	**(1458)**	
						29622C	**Raytheon**	**(1657)**	
				24	5	AM27S30M	† AMD		
						63LS482	**MMI**	**(1458)**	
						DM87S295	National		
			TS	20	5	AM27S29M	† AMD		10
						63LS481	**MMI**	**(1458)**	
						29623C	**Raytheon**	**(1657)**	
				24	5	AM27S31M	† AMD		
						63LS483	**MMI**	**(1458)**	
						DM87S296	National		
	70 nsF	TTL	OC	20	5	**6348-1**	**MMI**	**(1449)**	
						29620M	**† Raytheon**	**(1656)**	
				24	5	**93438M**	**† Fairchild**	**(1262)**	
						HM7640-5	**Harris**	**(1284)**	
						HM7640A-2	**† Harris**	**(1304)**	20
						3604	Intel		
						3604A	Intel		
						IM5605C	Intersil		
						6340-1	**MMI**	**(1449)**	
						MCM7640C	Motorola		
						29624M	**† Raytheon**	**(1658)**	
			TS	20	5	**6349-1**	**MMI**	**(1449)**	
						29621M	**† Raytheon**	**(1656)**	
				24	5	**93448M**	**† Fairchild**	**(1262)**	
						HM7641-5	**Harris**	**(1284)**	30
						HM7641A-2	**† Harris**	**(1304)**	
						3624	Intel		
						3624A	Intel		
						IM5625C	Intersil		
						6341-1	**MMI**	**(1449)**	
						63RA481	MMI		
						63RA483	MMI		
						MCM7641C	Motorola		
						μPB425	**NEC Micro**	**(1621)**	
						29625M	**† Raytheon**	**(1658)**	40
	75 nsF	TTL	OC	20	5	**53LS480**	**† MMI**	**(1458)**	
						DM54S473	† National		
						SN74S473	**TI**	**(1708)**	
				24	5	**53LS482**	**† MMI**	**(1458)**	
						DM77S295	† National		
						29626M	**† Raytheon**	**(1659)**	
						SN74S475	**TI**	**(1708)**	
			TS	20	5	**53LS481**	**† MMI**	**(1458)**	
						DM54S472	† National		
						SN74S472	**TI**	**(1708)**	50
				24	5	**53LS483**	**† MMI**	**(1458)**	
						DM77S296	† National		
						29627M	**† Raytheon**	**(1659)**	
						SN74S474	**TI**	**(1708)**	
	80 nsF	TTL	OC	20	5	**HM7648-2**	**Harris**	**(1320)**	
						5348-1	**† MMI**	**(1449)**	
						29622M	**† Raytheon**	**(1657)**	
				24	5	**HM7640AR-2**	**† Harris**	**(1306)**	
						IM5605M	† Intersil		
						5340-1	**† MMI**	**(1449)**	60
			TS	20	5	**HM7649-2**	**Harris**	**(1320)**	
						5349-1	**† MMI**	**(1449)**	

(Continued)

PROMs (Cont'd.)

Organization	Access Time (Max)	Type	Output	No. Pins	Supply Voltage	Device	Source		Line
512x8	80 nsF	TTL	TS	20	5			(Cont'd.)	
						29623M	**† Raytheon**	**(1657)**	
				24	5	**HM7641AR-2**	**† Harris**	**(1306)**	
						HM7647R-2	**† Harris**	**(1318)**	
						IM5625M	† Intersil		
						5341-1	**† MMI**	**(1449)**	
						53RA481	† MMI		
						53RA483	† MMI		70
	85 nsF	TTL	OC	20	5	**SN54S473**	**TI**	**(1708)**	
				24	5	**HM7640-2**	**† Harris**	**(1284)**	
						MCM7640M	† Motorola		
						SN54S475	**TI**	**(1708)**	
			TS	20	5	**SN54S472**	**TI**	**(1708)**	
				24	5	**HM7641-2**	**† Harris**	**(1284)**	
						MCM7641M	† Motorola		
						SN54S474	**TI**	**(1708)**	
	90 nsF	TTL	OC	24	5	3604-4	Intel		
						3604L-6	Intel		80
						3604AL	Intel		
						M3604	† Intel		
						63137-1	MMI		
						63139-1	MMI		
						S82S140	**† Signetics**	**(1680)**	
			TS	24	5	AM27S15M	† AMD		
						3624-4	Intel		
						M3624	† Intel		
						S82S141	**† Signetics**	**(1680)**	
						S82S115	**† Signetics**	**(1680)**	90
	100 nsF	TTL	OC	24	5	**μPB405-E**	**NEC Micro**	**(1621)**	
			TS	24	5	**μPB425-E**	**NEC Micro**	**(1621)**	
	450 nsF	Erasable							
			TS	24	±5,12	EA2704C	EA		
						2704	Intel		
						M2704	SGS		
	500 nsF	CMOS Erasable							
			TS	24	4-11	IM6604	Intersil		
		Erasable							
			TS	24	±5,12	EA2704L	EA		100
						MSM3754A	OKI		
	550 nsF	Erasable							
			TS	24	±5,12	EA2704M	† EA		
	575 nsF	Erasable							
			TS	24	-12,5	**S6834**	**AMI**	**(1809)**	
	700 nsF	Erasable							
			TS	24	-12,5	MM5204Q-1	National		
	750 nsF	Erasable							
			TS	24	-12,5	**S5204A**	**AMI**	**(1221)**	
						S6834-1	**AMI**	**(1809)**	110
	1 μsF	Erasable							
			TS	24	-12,5	MM5204Q	National		
	1.25 μsF	Erasable							
			TS	24	-12,5	MM4204Q	National		
1024x4	35 nsR	TTL	OC	18	5	**SN54S477**	**† TI**	**(1713)**	
						SN74S477	**TI**	**(1713)**	
			TS	18	5	**SN54S476**	**† TI**	**(1713)**	
						SN74S476	**TI**	**(1713)**	
	50 nsF	TTL	OC	18	5	**HM7642A-5**	**Harris**	**(1308)**	
						HM7642P-5	**Harris**	**(1310)**	120
						63S440	**MMI**	**(1453)**	

(Continued)

† Military Temperature Range (−55° to 125°C) ns*—Nanoseconds Typical nsF—Nanoseconds over Full Temperature Range nsR—Nanoseconds at Room Temperature

OC—Open Collector TS—Three-State OE—Open Emitter

Bold face indicates additional data is provided on the page noted.

MEMORY–PROMs (Cont'd)

PROMs (Cont'd.)

Organization	Access Time (Max)	Type	Output	No. Pins	Supply Voltage	Device	Source		Line
								(Cont'd.)	
1024x4	50 nsF	TTL	OC	18	5	63PS440	MMI		
			TS	18	5	**HM7643A-5**	**Harris**	**(1308)**	
						HM7643P-5	**Harris**	**(1310)**	
						63S441	**MMI**	**(1453)**	
						63PS441	MMI		
				20	5	**HM7645-5**	**Harris**	**(1314)**	
						HM7645P-5	**Harris**	**(1316)**	
			—	16	5	**HM7644A-5**	**Harris**	**(1312)**	
	55 nsF	TTL	OC	18	5	AM27S32C	AMD		10
						93452C	**Fairchild**	**(1264)**	
			TS	18	5	AM27S33C	AMD		
						93453C	**Fairchild**	**(1264)**	
	60 nsF	TTL	OC	18	5	**HM7642A-2**	**† Harris**	**(1308)**	
						HM7642P-2	**† Harris**	**(1310)**	
						3605A-1	Intel		
						6350-1	**MMI**	**(1449)**	
						6352-1	**MMI**	**(1449)**	
						53S440	**† MMI**	**(1453)**	
						53PS440	† MMI		20
						DM74S572	National		
						N82S136	**Signetics**	**(1680)**	
			TS	18	5	**HM7643A-2**	**† Harris**	**(1308)**	
						HM7643P-2	**† Harris**	**(1310)**	
						3625A-1	Intel		
						6351-1	**MMI**	**(1449)**	
						6353-1	**MMI**	**(1449)**	
						53S441	**† MMI**	**(1453)**	
						53PS441	† MMI		
						DM74S573	National		30
						DM74S574	National		
						N82S137	**Signetics**	**(1680)**	
			—	16	5	**HM7644A-2**	**† Harris**	**(1312)**	
	65 nsF	TTL	OC	18	5	AM27S32M	† AMD		
						63LS440	**MMI**	**(1458)**	
			TS	18	5	AM27S33M	† AMD		
						63LS441	**MMI**	**(1458)**	
						63RA441	**MMI**	**(1462)**	
						63RS441	**MMI**	**(1462)**	
	70 nsF	TTL	OC	18	5	**93452M**	**† Fairchild**	**(1264)**	40
						MB7059	Fujitsu		
						HM7642-5	**Harris**	**(1284)**	
						3605A	Intel		
						MCM7642C	Motorola		
						μPB406	**NEC Micro**	**(1625)**	
			TS	18	5	**93453M**	**† Fairchild**	**(1264)**	
						MB7054	Fujitsu		
						HM7643-5	**Harris**	**(1284)**	
						3625A	Intel		
						MCM7643C	Motorola		50
						μPB426	**NEC Micro**	**(1625)**	
				20	5	**HM7645-2**	**† Harris**	**(1314)**	
						HM7645P-2	**† Harris**	**(1316)**	
			—	16	5	**HM7644-5**	**Harris**	**(1284)**	
	75 nsF	TTL	OC	18	5	**5350-1**	**† MMI**	**(1449)**	
						5352-1	**† MMI**	**(1449)**	
						53LS440	**† MMI**	**(1458)**	
						DM54S572	† National		
			TS	18	5	**5351-1**	**† MMI**	**(1449)**	
						5353-1	**† MMI**	**(1449)**	60
						53LS441	**† MMI**	**(1458)**	
								(Continued)	

PROMs (Cont'd.)

Organization	Access Time (Max)	Type	Output	No. Pins	Supply Voltage	Device	Source		Line
								(Cont'd.)	
1024x4	75 nsF	TTL	TS	18	5	**53RA441**	**† MMI**	**(1462)**	
						53RS441	**† MMI**	**(1462)**	
						DM54S573	† National		
						DM54S574	† National		
	80 nsF	TTL	OC	18	5	**S82S136**	**† Signetics**	**(1680)**	
			TS	18	5	**S82S137**	**† Signetics**	**(1680)**	
	85 nsF	TTL	OC	18	5	**HM7642-2**	**† Harris**	**(1284)**	
						MCM7642M	† Motorola		70
			TS	18	5	**HM7643-2**	**† Harris**	**(1284)**	
						MCM7643M	† Motorola		
			—	16	5	**HM7644-2**	**† Harris**	**(1284)**	
	90 nsF	TTL	OC	18	5	M54740	Mitsubishi		
			TS	18	5	M54741	Mitsubishi		
	100 nsF	TTL	OC	18	5	**μPB406-E**	**NEC Micro**	**(1625)**	
			TS	18	5	**μPB426-E**	**NEC Micro**	**(1625)**	
	500 nsF	CMOS Erasable							
			TS	24	4-11	IM6603	Intersil		
1024x8	50 nsF	TTL	OC	24	5	63PS880	MMI		80
			TS	24	5	63PS881	MMI		
	55 nsF	TTL	OC	24	5	**93450C**	**Fairchild**	**(1266)**	
			TS	24	5	**93451C**	**Fairchild**	**(1266)**	
	60 nsF	TTL	OC	24	5	**HM7680-5**	**Harris**	**(1322)**	
						HM7680P-5	**Harris**	**(1326)**	
						HM7680R-5	**Harris**	**(1324)**	
						HM7680RP-5	**Harris**	**(1328)**	
						53PS880	† MMI		
						63S880	**MMI**	**(1453)**	
						N82S182	Signetics		90
						SN74S451	TI		
						SN74S479	**TI**	**(1713)**	
						SN74S3708	TI		
			TS	24	5	**HM7608-5**	**Harris**	**(1290)**	
						HM7681-5	**Harris**	**(1322)**	
						HM7681P-5	**Harris**	**(1326)**	
						HM7681R-5	**Harris**	**(1324)**	
						HM7681RP-5	**Harris**	**(1328)**	
						53PS881	† MMI		
						63S881	**MMI**	**(1453)**	100
						N82S183	Signetics		
			OC	24	5	SN74S450	TI		
						SN74S478	**TI**	**(1713)**	
						SN74S2708	TI		
			—	24	5	**HM7683-5**	**Harris**	**(1331)**	
	70 nsF	TTL	OC	24	5	**93450M**	**† Fairchild**	**(1266)**	
						53S880	**† MMI**	**(1453)**	
						MCM7680C	Motorola		
						MCM82707C	Motorola		
						DM87S229	National		110
						N82S180	**Signetics**	**(1680)**	
			TS	24	5	**93451M**	**† Fairchild**	**(1266)**	
						53S881	**† MMI**	**(1453)**	
						MCM7681C	Motorola		
						MCM82708C	Motorola		
						DM87S228	National		
						N82S181	**Signetics**	**(1680)**	
						N82S2708	**Signetics**	**(1702)**	
	75 nsF	TTL	OC	24	5	**63LS880**	**MMI**	**(1458)**	
						SN54S451	† TI		120
								(Continued)	

† Military Temperature Range (−55° to 125°C) ns*—Nanoseconds Typical nsF—Nanoseconds over Full Temperature Range nsR—Nanoseconds at Room Temperature

OC—Open Collector TS—Three-State OE—Open Emitter

MEMORY–PROMs (Cont'd)

Organization	Access Time (Max)	Type	Output	No. Pins	Supply Voltage	Device	Source		Line
PROMs								**(Cont'd.)**	
1024x8	75 nsF	TTL	OC	24	5			(Cont'd.)	
						SN54S479	**† TI**	**(1713)**	
						SN54S3708	† TI		
			TS	24	5	**63LS881**	**MMI**	**(1458)**	
						63RA881	MMI		
						63RA883	MMI		
						SN54S450	† TI		
						SN54S478	**† TI**	**(1713)**	
						SN54S2708	† TI		
	80 nsF	TTL	OC	24	5	**HM7680-2**	**† Harris**	**(1322)**	10
						HM7680P-2	**† Harris**	**(1326)**	
						HM7680R-2	**† Harris**	**(1324)**	
						HM7680RP-2	**† Harris**	**(1328)**	
						3608	Intel		
						29630C	**Raytheon**	**(1660)**	
			TS	24	5	HM7608-2	† Harris		
						HM7681-2	**† Harris**	**(1322)**	
						HM7681P-2	**† Harris**	**(1326)**	
						HM7681R-2	**† Harris**	**(1324)**	
						HM7681RP-2	**† Harris**	**(1328)**	20
						3628	Intel		
						29631C	**Raytheon**	**(1660)**	
			—	20	5	**HM7683-2**	**† Harris**	**(1331)**	
	80 ns*	TTL	OC	24	5	**SN54LS479**	**† TI**	**(1713)**	
						SN74LS479	**TI**	**(1713)**	
			TS	24	5	**SN54LS478**	**† TI**	**(1713)**	
						SN74LS478	**TI**	**(1713)**	
	85 nsF	TTL	OC	24	5	**53LS880**	**† MMI**	**(1458)**	
						MCM7680M	† Motorola		
						MCM82707M	† Motorola		30
			TS	24	5	**53LS881**	**† MMI**	**(1458)**	
						MCM7681M	† Motorola		
						MCM82708M	† Motorola		
	90 nsF	TTL	OC	22	5	6386-1	MMI		
				24	5	**6380-1**	**MMI**	**(1449)**	
						6384-1	**MMI**	**(1449)**	
						DM77S229	† National		
						29634C	**Raytheon**	**(1662)**	
						29636C	**Raytheon**	**(1663)**	
						S82S180	**† Signetics**	**(1680)**	40
						S82S182	† Signetics		
			TS	22	5	6387-1	MMI		
				24	5	**6381-1**	**MMI**	**(1449)**	
						6385-1	**MMI**	**(1449)**	
						53RA881	† MMI		
						53RA883	† MMI		
						DM77S228	† National		
						29635C	**Raytheon**	**(1662)**	
						29637C	**Raytheon**	**(1663)**	
						S82S181	**† Signetics**	**(1680)**	50
						S82S183	† Signetics		
						S82S2708	**† Signetics**	**(1702)**	
	95 nsF	TTL	OC	24	5	**29632C**	**Raytheon**	**(1661)**	
			TS	24	5	**29633C**	**Raytheon**	**(1661)**	
	100 nsF	TTL	OC	24	5	3608-4	Intel		
			TS	24	5	3628-4	Intel		
	110 nsF	TTL	OC	24	5	**29630M**	**† Raytheon**	**(1660)**	
			TS	24	5	**29631M**	**† Raytheon**	**(1660)**	
	120 nsF	TTL	TS	24	5	µPB427	NEC Micro		
								(Continued)	

Organization	Access Time (Max)	Type	Output	No. Pins	Supply Voltage	Device	Source		Line
PROMs								**(Cont'd.)**	
1024x8								(Cont'd.)	60
	125 nsF	TTL	OC	22	5	5386-1	† MMI		
				24	5	**5380-1**	**† MMI**	**(1449)**	
						5384-1	**† MMI**	**(1449)**	
						29632M	**† Raytheon**	**(1661)**	
						29634M	**† Raytheon**	**(1662)**	
						29636M	**† Raytheon**	**(1663)**	
			TS	22	5	5387-1	† MMI		
				24	5	**5381-1**	**† MMI**	**(1449)**	
						5385-1	**† MMI**	**(1449)**	
						29633M	**† Raytheon**	**(1661)**	70
						29635M	**† Raytheon**	**(1662)**	
						29637M	**† Raytheon**	**(1663)**	
	175 nsF	TTL	OC	24	5	**N82LS180**	**Signetics**	**(1700)**	
			TS	24	5	**N82LS181**	**Signetics**	**(1700)**	
	200 nsF	TTL	TS	24	5	**µPB417**	**NEC Micro**	**(1629)**	
	225 nsF	TTL	OC	24	5	**S82LS180**	**† Signetics**	**(1700)**	
			TS	24	5	**S82LS181**	**† Signetics**	**(1700)**	
	250 nsF	TTL	OC	24	5	MB7060	Fujitsu		
			TS	24	5	MB7055	Fujitsu		
	300 nsF	Erasable							80
			TS	24	±5,12	MCM27A08L	Motorola		
						MCM68A708L	Motorola		
	350 nsF	Erasable							
			TS	24	5	TMS2508-35	TI		
					±5,12	2708-1	AMD		
						2708-1	**Fairchild**	**(1282)**	
						2708-1	Intel		
						MM2708-1	National		
						TMS2708-35	TI		
	450 nsF	Electrically Erasable							90
			TS	28	5,12	µPD458	NEC Micro		
		Erasable							
			TS	24	5	2758	Intel		
						TMS2508-45	TI		
					±5,12	2708	AMD		
						AM9708	† AMD		
						EA2708C	EA		
						2708	**Fairchild**	**(1282)**	
						F68708	**Fairchild**	**(1887)**	
						MB8518H	Fujitsu		100
						HN462708	Hitachi		
						2708	Intel		
						2708L	Intel		
						M2708	† Intel		
						M5L2708	**Mitsubishi**	**(1441)**	
						MCM2708L	Motorola		
						MCM68708ML	† Motorola		
						MCM68708L	Motorola		
						MM2708	National		
						M2708	SGS		110
						2708	Signetics		
						TMS27L08	TI		
						TMS2708	TI		
						TMM322	Toshiba		
		NMOS	TS	24	±5,12	MCM2708P	Motorola		
	500 nsF	Erasable							
			TS	24	±5,12	EA2708L	EA		
	550 nsF	Erasable							
			TS	24	±5,12	EA2708M	† EA		
								(Continued)	

† Military Temperature Range (–55° to 125°C) ns*—Nanoseconds Typical nsF—Nanoseconds over Full Temperature Range nsR—Nanoseconds at Room Temperature

OC—Open Collector TS—Three-State OE—Open Emitter

Bold face indicates additional data is provided on the page noted.

MEMORY–PROMs (Cont'd)

PROMs (Cont'd.)

Organization	Access Time (Max)	Type	Output	No. Pins	Supply Voltage	Device	Source		Line
1024x8	550 nsF	Erasable						(Cont'd.)	
			TS	24	±5,12	MSM3758	OKI		
	650 nsF	Erasable							
			TS	24	±5,12	MB8518E	Fujitsu		
2048x4	45 ns*	TTL	OC	18	5	**SN54S455**	**† TI**	**(1193)**	
						SN74S455	**TI**	**(1713)**	
			TS	18	5	**SN54S454**	**† TI**	**(1713)**	
						SN74S454	**TI**	**(1713)**	
						M5L2708-65	**Mitsubishi**	**(1441)**	10
	50 nsF	TTL	OC	18	5	63PS840	MMI		
			TS	18	5	63PS841	MMI		
						M5L2708-65	**Mitsubishi**	**(1441)**	
	60 nsF	TTL	OC	18	5	**HM7684-5**	**Harris**	**(1333)**	
						HM7684P-5	**Harris**	**(1335)**	
						53PS840	† MMI		
						63S840	**MMI**	**(1453)**	
				20	5	**HM7686-5**	**Harris**	**(1337)**	
						HM7686P-5	**Harris**	**(1341)**	
						HM7686R-5	**Harris**	**(1339)**	20
						HM7686RP-5	**Harris**	**(1343)**	
			TS	18	5	**HM7685-5**	**Harris**	**(1333)**	
						HM7685P-5	**Harris**	**(1335)**	
						53PS841	† MMI		
						63S841	**MMI**	**(1453)**	
				20	5	**HM7687-5**	**Harris**	**(1337)**	
						HM7687P-5	**Harris**	**(1341)**	
						HM7687R-5	**Harris**	**(1339)**	
						HM7687RP-5	**Harris**	**(1343)**	
	70 nsF	TTL	OC	18	5	**53S840**	**† MMI**	**(1453)**	30
			TS	18	5	**53S841**	**† MMI**	**(1453)**	
	75 nsF	TTL	OC	18	5	**63LS840**	**MMI**	**(1458)**	
			TS	18	5	**63LS841**	**MMI**	**(1458)**	
				20	5	**63RA841**	**MMI**	**(1462)**	
						63RS841	**MMI**	**(1462)**	
	80 nsF	TTL	OC	18	5	**HM7684-2**	**† Harris**	**(1333)**	
						HM7684P-2	**† Harris**	**(1335)**	
				20	5	**HM7686-2**	**† Harris**	**(1337)**	
						HM7686P-2	**† Harris**	**(1341)**	
						HM7686R-2	**† Harris**	**(1339)**	40
						HM7686RP-2	**† Harris**	**(1343)**	
			TS	18	5	**HM7685-2**	**† Harris**	**(1333)**	
						HM7685P-2	**† Harris**	**(1335)**	
				20	5	**HM7687-2**	**† Harris**	**(1337)**	
						HM7687P-2	**† Harris**	**(1341)**	
						HM7687R-2	**† Harris**	**(1339)**	
						HM7687RP-2	**† Harris**	**(1343)**	
	85 nsF	TTL	OC	18	5	**53LS840**	**† MMI**	**(1458)**	
			TS	18	5	**53LS841**	**† MMI**	**(1458)**	
				20	5	**53RA841**	**† MMI**	**(1462)**	50
						53RS841	**† MMI**	**(1462)**	
	100 nsF	TTL	OC	18	5	**N82S184**	**Signetics**	**(1680)**	
			TS	18	5	**N82S185**	**Signetics**	**(1680)**	
	125 nsF	TTL	OC	18	5	**S82S184**	**† Signetics**	**(1680)**	
			TS	18	5	**S82S185**	**† Signetics**	**(1680)**	
2048x8	50 ns*	TTL	OC	24	5	**SN54S453**	**† TI**	**(1713)**	

(Continued)

PROMs (Cont'd.)

Organization	Access Time (Max)	Type	Output	No. Pins	Supply Voltage	Device	Source		Line
2048x8	50 ns*	TTL	OC	24	5			(Cont'd.)	
						SN74S453	**TI**	**(1713)**	
			TS	24	5	**SN54S452**	**† TI**	**(1713)**	
						SN74S452	**TI**	**(1713)**	60
	60 nsF	TTL	OC	24	5	**HM76160-5**	**Harris**	**(1296)**	
						63S1680	**MMI**	**(1453)**	
						63PS1680	MMI		
						SM82S190	**Supertex**	**(1705)**	
			TS	24	5	**HM7616-5**	**Harris**	**(1294)**	
						HM76161-5	**Harris**	**(1296)**	
						63S1681	**MMI**	**(1453)**	
						63PS1681	MMI		
						SM82S191	**Supertex**	**(1705)**	
	70 nsF	TTL	OC	24	5	**53S1680**	**† MMI**	**(1453)**	70
						53PS1680	† MMI		
			TS	24	5	**53S1681**	**† MMI**	**(1453)**	
						53PS1681	† MMI		
	80 nsF	TTL	OC	24	5	**HM76160-2**	**† Harris**	**(1296)**	
						63LS1680	**MMI**	**(1458)**	
						N82S190	**Signetics**	**(1680)**	
						MM82S190	**† Supertex**	**(1706)**	
			TS	24	5	**HM7616-2**	**† Harris**	**(1294)**	
						HM76161-2	**† Harris**	**(1296)**	
						63LS1681	**MMI**	**(1458)**	80
						N82S191	**Signetics**	**(1680)**	
						MM82S191	**† Supertex**	**(1705)**	
	85 nsF	TTL	TS	24	5	63RA1681	MMI		
						63RA1683	MMI		
	90 nsF	TTL	OC	24	5	**53LS1680**	**† MMI**	**(1458)**	
			TS	24	5	**53LS1681**	**† MMI**	**(1458)**	
	100 nsF	TTL	OC	24	5	**S82S190**	**† Signetics**	**(1680)**	
			TS	24	5	53RA1681	† MMI		
						53RA1683	† MMI		
						S82S191	**† Signetics**	**(1680)**	90
	250 nsF	VMOS	TS	24	5	**S4716**	**AMI**	**(1220)**	
	300 nsF	Erasable							
			TS	24	±5,12	TMS27A16L	Motorola		
	350 nsF	Erasable							
			TS	24	5	2716-1	Intel		
						MCM27A16L	**Motorola**	**(1493)**	
	390 nsF	Erasable							
			TS	24	5	2716-2	Intel		
	450 nsF	Erasable							
			TS	24	5	2716	AMD		100
						EA2716	EA		
						EA2716M	† EA		
						2716	Fairchild		
						F68716	**Fairchild**	**(1887)**	
						HN42716	Hitachi		
						MBM2716	Fujitsu		
						2716	Intel		
						MIC2716	Maruman		
						MK2716	Mostek		
						MCM2716L	**Motorola**	**(1493)**	110
						MM2716	National		
						μPD2716	**NEC Micro**	**(1617)**	
						2716	Signetics		
						SY2716	Synertek		
						TMS2516	TI		
						TMM323	Toshiba		

(Continued)

† Military Temperature Range (−55° to 125°C)
ns*—Nanoseconds Typical
nsF—Nanoseconds over Full Temperature Range
nsR—Nanoseconds at Room Temperature
OC—Open Collector
TS—Three-State
OE—Open Emitter

MEMORY–PROMs (Cont'd)

Organization	Access Time (Max)	Type	Output	No. Pins	Supply Voltage	Device	Source	Line
PROMs						**(Cont'd.)**		
2048x8	450 nsF	Erasable						
			TS	24				(Cont'd.)
					±5,12	**TMS2716**	**Motorola**	**(1486)**
						TMS2716	TI	
4096x4	60 nsF	TTL	OC	20	5	**63S1640**	**MMI**	**(1453)**
						63PS1640	MMI	
			TS	20	5	**63S1641**	**MMI**	**(1453)**
						63PS1641	MMI	
	70 nsF	TTL	OC	20	5	**53S1640**	**† MMI**	**(1453)**
						53PS1640	† MMI	
			TS	20	5	**53S1641**	**† MMI**	**(1453)**
						53PS1641	† MMI	
	80 nsF	TTL	OC	20	5	**63LS1640**	**MMI**	**(1458)**
			TS	20	5	**63LS1641**	**MMI**	**(1458)**
	85 nsF	TTL	TS	20	5	**63RA1641**	**MMI**	**(1462)**
						63RS1641	**MMI**	**(1462)**
	90 nsF	TTL	OC	20	5	**53LS1640**	**† MMI**	**(1458)**
			TS	20	5	**53LS1641**	**† MMI**	**(1458)**
	100 nsF	TTL	TS	20	5	**53RA1641**	**† MMI**	**(1462)**
						53RS1641	**† MMI**	**(1462)**
4096x8	250 nsF	VMOS	TS	24	5	**S4532**	**AMI**	**(1219)**
	450 nsF	Erasable						
			TS	24	5	2732	Intel	
						TMS2532	TI	
8192x8	450 nsF	Erasable						
			TS	24	5	TMS2564	TI	

† Military Temperature Range (−55° to 125°C) ns*—Nanoseconds Typical nsF—Nanoseconds over Full Temperature Range nsR—Nanoseconds at Room Temperature

OC—Open Collector TS—Three-State OE—Open Emitter

Bold face indicates additional data is provided on the page noted.

MEMORY–RAMs

Organization	Access Time (Max)	Type	Output	No. Pins	Supply Voltage	Device	Source	Line
Dynamic								
1024x1	130 nsF	PMOS	—	18	20,22.5,7	TMS4063	TI	
				22	20,22.5,7	TMS4062	TI	
	145 nsF	PMOS	—	18	19,22.5	S1103A-1	AMI	
						1103A-1	Intel	
						1103A-2	Intel	
	150 nsF	PMOS	—	18	19,22.5	1103-1	Intel	
						1103-1	Nortec	10
				22	20,22.5,7	IM6002-11	Intersil	
						6002	Nortec	
	205 nsF	PMOS	—	18	16,19.5	S1103A	AMI	
						1103A	Intel	
					19,22.5	S146	AMI	
						1103-146	Nortec	
	300 nsF	PMOS	—	18	16,19.5	S1103	AMI	
						1103	Intel	
						M58533	Mitsubishi	20
						1103	Nortec	
						MN1003	Panasonic	
	400 nsF	PMOS	—	16	-12,5	S4006	AMI	
						MK4006	Mostek	
	500 nsF	PMOS	—	16	-12,5	S4008	AMI	
						MK4008	Mostek	
	800 nsF	PMOS	—	16	-12,5	S4008-9	AMI	
2048x1	350 nsF	PMOS	—	22	35,8,5,-15,-20	IM6003-11	Intersil	
						600311	Nortec	30
	460 nsF	PMOS	—	22	35,8,5,-15,-20	IM6003-10	Intersil	
						600314	Nortec	
2048x8	120 nsF	NMOS	TS	28	5	MK4816-1	Mostek	
	150 nsF	NMOS	TS	28	5	MK4816-2	Mostek	
	200 nsF	NMOS	TS	28	5	MK4816-3	Mostek	
4096x1	80 nsF	I²L	TS	16	5	93481B	Fairchild	
	100 nsF	I²L	TS	16	5	93481A	Fairchild	
		NMOS	—	22	±5,12	HM4710	Hitachi	
	120 nsF	I²L	TS	16	5	93481	Fairchild	40
		NMOS	TS	16	±5,12	IM7027-1	Intersil	
						MK4027-1	Mostek	
	125 nsR	NMOS	TS	22	±5,12	**MM5280A-2**	**National** (270)	
	130 nsF	NMOS	TS	22	±5,15	HM4711-1	Hitachi	
	135 nsF	NMOS	TS	22	±5,15	**μPD411-4**	**NEC Micro** (1547)	
	140 nsF	NMOS	TS	18	-5,12	MM5271	National	
	150 nsF	NMOS	TS	16	±5,12	MB8227H	Fujitsu	
						HM4704L-2	Hitachi	
						2104A-1	Intel	
						MK4027-2	Intersil	50
						MK4027-2	Mostek	
						MCM4027-2	**Motorola** (1522)	
						M4027-2	SGS	
						4027-2	**Signetics** (1677)	
						TMS4027-15	TI	
				22	±5,12	MB8107Y	Fujitsu	
						HM4711-2	Hitachi	
						2107C-1	Intel	
							(Continued)	

Organization	Access Time (Max)	Type	Output	No. Pins	Supply Voltage	Device	Source	Line
Dynamic							**(Cont'd.)**	
4096x1	150 nsF	NMOS	TS	22	±5,12		(Cont'd.)	
						M58155-3	Mitsubishi	60
						MCM6605A-1	Motorola	
						μPD411-3	**NEC Micro** (1547)	
	200 nsF	NMOS	TS	16	±5,12	MB8227E	Fujitsu	
						HM4704L-3	Hitachi	
						2104A-2	Intel	
						MK4027-3	Intersil	
						M5L2107	Mitsubishi	
						MK4027-3	Mostek	
						MK4027-83	Mostek	
						MCM4027-3	**Motorola** (1522)	70
						μPD414-2	NEC Micro	
						M4027-3	SGS	
						4027-3	**Signetics** (1677)	
						TMS4027-20	TI	
						TMM415-3	Toshiba	
				18	-5,12	9050E	AMD	
						90L50E	AMD	
						MM5270	National	
						MM5271	National	
						TMS4050-2	TI	80
				22	±5,12	9060E	AMD	
						90L60E	AMD	
						MB8107H	Fujitsu	
						HM4711-3	Hitachi	
						2107C-2	Intel	
						M58755-1	Mitsubishi	
						MCM6605A-2	Motorola	
						MM5280	**National** (270)	
						μPD411A-2	**NEC Micro** (1554)	
						μPD411-2	**NEC Micro** (1547)	90
						MSM3743A	OKI	
						MN1001-2	Panasonic	
						M340A	SGS	
						M2107	SGS	
						TMS4060-2	TI	
						TMM414	Toshiba	
	250 nsF	NMOS	TS	16	±5,12	MB8227N	Fujitsu	
						HM4704L-4	Hitachi	
						2104A-3	Intel	
						MK4027-4	Intersil	100
						MK4015	Mostek	
						MK4027-4	Mostek	
						MK4027-84	Mostek	
						MK4096-6	Mostek	
						MK4096-77	Mostek	
						MCM4027-4	**Motorola** (1522)	
						MCM4096-6	Motorola	
						MCM6604A-2	Motorola	
						μPD414-1	NEC Micro	
						M4027-4	SGS	110
						4027-4	**Signetics** (1677)	
						TMM415-4	Toshiba	
						TMS4027-25	TI	
				18	-5,12	9050D	AMD	
						90L50D	AMD	
						MM5271	National	
						TMS4050-1	TI	
						TMS4051-1	TI	
				22	±5,12	9060D	AMD	
						90L60D	AMD	120
						EA4122-1	EA	
						2107C	Intel	
						μPD411-1	**NEC Micro** (1547)	
							(Continued)	

† Military Temperature Range (−55° to 125°C) ns*—Nanoseconds Typical nsF—Nanoseconds over Full Temperature Range nsR—Nanoseconds at Room Temperature

OC—Open Collector TS—Three-State OE—Open Emitter

MEMORY–RAMs (Cont'd)

Dynamic (Cont'd.)

Organization	Access Time (Max)	Type	Output	No. Pins	Supply Voltage	Device	Source	Line
4096x1	250 nsF	NMOS	TS	22	±5,12		(Cont'd.)	
						μPD411A-1	**NEC Micro (1554)**	
						MN1001-1	Panasonic	
						TMS4060-1	TI	
						TMM414-1	Toshiba	
	270 nsF	NMOS	TS	18	-5,12	MM4270	National	
						MM5270-5	National	
				22	±5,12	M58755-2	Mitsubishi	
						MM4280	National	
						MM5280-5	**National (270)**	10
						M340B	SGS	
						M2107-4	SGS	
	280 nsF	NMOS	TS	22	±5,12	2107A-1	Intel	
	300 nsF	NMOS	TS	16	±5,12	2104A-4	Intel	
						M5L2104	Mitsubishi	
						M58756	Mitsubishi	
						MK4096-16	Mostek	
						MK4096-86	Mostek	
						MK4200-16	Mostek	
						MCM4096-16	Motorola	20
						MCM6604A-4	Motorola	
						μPD414	NEC Micro	
				18	-5,12	9050C	AMD	
						90L50C	AMD	
						TMS4050	TI	
						TMS4051	TI	
				22	±5,12	9060C	AMD	
						90L60C	AMD	
						MB8107N	Fujitsu	
						HM4503-1	Hitachi	30
						HM4507	Hitachi	
						2107C-4	Intel	
						MCM6605A	Motorola	
						μPD411	**NEC Micro (1547)**	
						μPD411A	**NEC Micro (1554)**	
						MSM3741A	OKI	
						MN1001	Panasonic	
						HYB4060	Siemens	
						TMS4060	TI	
	330 nsF	NMOS	TS	22	±5, 12	MSM3741-1A	OKI	40
	350 nsF	NMOS	TS	16	±5,12	HM4704L-6	Hitachi	
						2104A	Intel	
						MK4096-11	Mostek	
						MK4096-85	Mostek	
						MK4200-11	Mostek	
						MCM4096-11	Motorola	
						MCM6604A	Motorola	
						μPD414-E	NEC Micro	
				18	-5,12	IM7270-14	Intersil	
				22	±5,12	**μPD411-E**	**NEC Micro (1547)**	50
						μPD411A-E	**NEC Micro (1554)**	
						M340C	SGS	
						M2107-6	SGS	
	380 nsF	NMOS	TS	22	±5,12	MSM3741-2A	OKI	
	400 nsF	NMOS	TS	18	±5,12	HM4503	Hitachi	
	420 nsF	NMOS	TS	22	±5,12	9107-6	AMD	
8192x1	150 nsF	NMOS	TS	22	±5,12	IM7008-10	Intersil	
	200 nsF	NMOS	TS	16	±5,12	2109-2	Intel	
						MK4108	Mostek	
						MM5298-3	National	60
				22	±5,12	IM7008-11	Intersil	
							(Continued)	

Dynamic (Cont'd.)

Organization	Access Time (Max)	Type	Output	No. Pins	Supply Voltage	Device	Source	Line
8192x1							(Cont'd.)	
	250 nsF	NMOS	TS	16	±5,12	MK4115	Mostek	
						MM5298-4	National	
	300 nsF	NMOS	TS	16	±5,12	2109-4	Intel	
16384x1	80 nsF	NMOS	TS	16	5	**2118-2**	**Intel (1417)**	
	100 nsF	NMOS	TS	16	5	HM4816	Hitachi	
						2118-3	**Intel (1417)**	
	120 nsF	NMOS	TS	16	5	**2118-4**	**Intel (1417)**	
					±5,12	MB8116Y	Fujitsu	70
						μPD416-5	**NEC Micro (1562)**	
	150 nsF	NMOS	TS	16	5	**2118-7**	**Intel (1417)**	
					±5,12	**F16K-2**	**Fairchild (1272)**	
						MB8116H	Fujitsu	
						HM4716A-2	Hitachi	
						2117-2	Intel	
						M5K4116-2	**Mitsubishi (1420)**	
						MCM4116-15	**Motorola (1505)**	
						MK4116-2	Mostek	
						MM5290-2	**National (1544,270,278)**	80
						μPD416-3	**NEC Micro (1562)**	
						MSM3716-2	OKI	
						2690-2	**Signetics (1676)**	
						TMS4116-15	TI	
						TMM416-2	Toshiba	
						Z6116-2	Zilog	
	160 nsF	NMOS	TS	16	±5,12	9016D	AMD	
	200 nsF	NMOS	TS	16	±5,12	9016E	AMD	
						F16K-3	**Fairchild (1272)**	90
						MB8116E	Fujitsu	
						HM4716A-3	Hitachi	
						2117-3	Intel	
						ICM7116-3	Intersil	
						M5K4116-3	**Mitsubishi (1420)**	
						MK4116-3	Mostek	
						MK4116-83	†Mostek	
						MCM6616-20	Motorola	
						MM5290-3	**National (1544,270,278)**	100
						μPD416-2	**NEC Micro (1562)**	
						MSM3716-3	OKI	
						HYB4116-3	Siemens	
						2690-3	**Signetics (1676)**	
						TMS4116-20	TI	
						TMM416-3	Toshiba	
						Z6116-3	Zilog	
	250 nsF	NMOS	TS	16	±5,12	9016D	AMD	
						F16K-4	**Fairchild (1272)**	
						MB8116N	Fujitsu	110
						HM4716A-4	Hitachi	
						2117-4	Intel	
						IM7116-4	Intersil	
						M5K4116-4	**Mitsubishi (1420)**	
						MK4116-4	Mostek	
						MK4116-84	†Mostek	
						MK4215	Mostek	
						MCM4116-25	**Motorola (1505)**	
						MM5290-4	**National (1544,270,278)**	120
						μPD416-1	**NEC Micro (1562)**	
						MSM3716-4	OKI	
						HYB4116-4	Siemens	
						2690-4	**Signetics (1676)**	
						TMS4116-25	TI	
							(Continued)	

† Military Temperature Range (−55° to 125°C)
ns*—Nanoseconds Typical
nsF—Nanoseconds over Full Temperature Range
nsR—Nanoseconds at Room Temperature
OC—Open Collector
TS—Three-State
OE—Open Emitter

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MEMORY–RAMs (Cont'd)

Dynamic (Cont'd.)

Organization	Access Time (Max)	Type	Output	No. Pins	Supply Voltage	Device	Source
							(Cont'd.)
16384x1	250 nsF	NMOS	TS	16	±5,12	TMM416-4	Toshiba
						Z6116-4	Zilog
	300 nsF	NMOS	TS	16	±5,12	9016C	AMD
						F16K-5	**Fairchild (1272)**
						2117-4	Intel
						MCM4116-30	**Motorola (1505)**
						μPD416	**NEC Micro (1562)**
						HYB4116-5	Siemens
32768x1	150 nsF	NMOS	—	16	-2.5,7	MB8132H	Fujitsu
	200 nsF	NMOS	—	16	-2.5,7	MB8132E	Fujitsu
			TS	18	±5,12	MK4332D-3	Mostek
	250 nsF	NMOS	—	16	-2.5,7	MB8132N	Fujitsu
65536x1	100 nsF	NMOS	TS	16	5	TMS4164-10	TI
	150 nsF	NMOS	TS	16	5	TMS4164-15	TI
			—	16	-2.5,7	MB8164H	Fujitsu
	200 nsF	NMOS	TS	16	5	TMS4164-20	TI
			—	16	-2.5,7	MB8164E	Fujitsu
	250 nsF	NMOS	—	16	-2.5, 7	MB8164N	Fujitsu

Bubble Memories

92,304-Bits (641x144x1)				16		TIB0203	TI
254,688-Bits (1137x224x1)				20		TIB0303	TI
266500-Bits (1025x260x1)				18		RBM256	Rockwell
290560-Bits (1135x256x1)				20		H4701B	Hitachi

CCD Memories

910-Bits (455x2)				16		CCD321	Fairchild
16,384-Bits (256x64x1)				18		SY2416	Synertek
65,536-Bits(4096x16x1)				16		**F464**	**Fairchild (1276)**
						MCM0464	**Motorola (1514)**
						μPD3064	**NEC Micro (1643)**
						TMS3064	TI
						TMS3064-1	TI

Static

4x4	20 nsR	TTL	OC	16	5	25LS170C	Raytheon
						25LS170M	† Raytheon
			TS	16	5	25LS670C	Raytheon
						25LS670M	† Raytheon
	30 nsF	TTL	OC	24	5	3104	Intel
	30 nsR	TTL	OC	16	5	54LS170	† Raytheon
						74LS170	Raytheon
	40 nsR	TTL	OC	16	5	54170	† Fairchild
						74170	Fairchild
						54LS170	† Fairchild
						74LS170	Fairchild
						ZN54170	† Ferranti
						ZN74170	Ferranti

(Continued)

Static (Cont'd.)

Organization	Access Time (Max)	Type	Output	No. Pins	Supply Voltage	Device	Source
							(Cont'd.)
4x4	40 nsR	TTL	OC	16	5	SN54LS170	† Motorola
						SN74LS170	Motorola
						DM54170	† National
						DM74170	National
						DM54LS170	† National
						DM74LS170	National
						54LS170	† Signetics
						74LS170	Signetics
						SN54170	† TI
						SN74170	TI
						SN54LS170	† TI
						SN74LS170	TI
			TS	16	5	54LS670	† Fairchild
						74LS670	Fairchild
						SN54LS670	† Motorola
						SN74LS670	Motorola
						DM54LS670	† National
						DM74LS670	National
						54LS670	† Raytheon
						74LS670	Raytheon
						54LS670	† Signetics
						74LS670	Signetics
						SN54LS670	† TI
						SN74LS670	TI
	1 μsR	CMOS	—	24	4.5-15	MC14580BA	† Motorola
	1.5 μsR	CMOS	—	24	3-15	MC14580BC	Motorola
4x8	1 μsR	CMOS	—	24	3-15	CD4036A	† RCA
						CD4039A	† RCA
						CM4036A	† Solitron
						CM4039A	† Solitron
8x2	12 nsF	ECL	OE	18	-5.2	10155	Signetics
	15 nsF	ECL	—	24	-5.2	MCM10143	Motorola
	50 nsR	TTL	TS	24	5	74S172	Signetics
						SN74172	TI
8x4	40 nsF	TTL	OC	24	5	**N82S12**	**Signetics (1678)**
			TS	24	5	**N82S112**	**Signetics (1678)**
						F464-2	**Fairchild (1276)**
						F464-3	**Fairchild (1276)**
						F464-4	**Fairchild (1276)**
16x1	20 nsR	TTL	OC	14	5	SN5481A	† TI
						SN7481A	TI
				16	5	SN5484A	† TI
						SN7484A	TI
	35 nsR	TTL	OC	14	5	MC4004	Motorola
						MC4005	Motorola
						MC4304	† Motorola
						MC4305	† Motorola
16x4	6 nsR	ECL	OE	16	-5.2	F10145	Fairchild
	10 ns*	ECL	OE	16	-5.2	HD10145	Hitachi
	15 nsF	ECL	OE	16	-5.2	MCM10145	† Motorola
	15 nsR	ECL	OE	16	-5.2	10145	Signetics
	20 nsF	TTL	TS	18	5	**9410C**	**Fairchild (1893)**
	25 nsF	TTL	OC	16	5	AM27S02AC	AMD
						AM27S06C	AMD
						AM29700C	AMD
						AM29702C	AMD
						27S02AC	MMI
						29700C	MMI
						29702C	MMI

(Continued)

† Military Temperature Range (−55° to 125°C) ns*—Nanoseconds Typical nsF—Nanoseconds over Full Temperature Range nsR—Nanoseconds at Room Temperature

OC—Open Collector TS—Three-State OE—Open Emitter

MEMORY–RAMs (Cont'd)

Static (Cont'd.)

Organization	Access Time (Max)	Type	Output	No. Pins	Supply Voltage	Device	Source	Line
16x4	25 nsF	TTL				(Cont'd.)		
			TS	16	5	AM27S03AC	AMD	
						AM27S07C	AMD	
						AM29701C	AMD	
						AM29703C	AMD	
						27S03AC	MMI	
						29701C	MMI	
						29703C	MMI	
	30 nsF	TTL	OC	16	5	AM27S02AM	† AMD	
						AM27S06M	† AMD	10
						AM29700M	† AMD	
						AM29702M	† AMD	
						27S02AM	† MMI	
						29700M	† MMI	
						29702M	† MMI	
			TS	16	5	AM27S03AM	† AMD	
						AM27S07M	† AMD	
						AM29701M	† AMD	
						AM29703M	† AMD	
						27S03AM	† MMI	20
						29701M	† MMI	
						29703M	† MMI	
	35 nsF	TTL	OC	16	5	AM27S02C	AMD	
						SN74S289	AMD	
						74S289	Fairchild	
						HD74S289	Hitachi	
						3101A	Intel	
						DM74S289	National	
						µPB2289	NEC America	
						N3101A	**Signetics (1678)**	30
						SN74S289	TI	
			TS	16	5	AM27S03C	AMD	
						SN74S189	AMD	
						74S189	Fairchild	
						HD74S189	Hitachi	
						DM74S189	National	
						74S189	**Signetics (1678)**	
						SN74S189	TI	
	40 nsF	TTL	TS	18	5	85S68	MMI	
						DM85S68	National	40
	45 nsF	TTL	OC	16	5	AM27S02M	† AMD	
			TS	16	5	AM27S03M	† AMD	
	45 ns*	TTL	OC	16	5	SN74LS89	Motorola	
			TS	16	5	SN74LS189	Motorola	
						SN74LS289	Motorola	
						74LS189	**Fairchild (485)**	
	50 nsF	TTL	OC	16	5	SN54S289	† AMD	
						6560	MMI	
						DM54S289	† National	
						N82S25	**Signetics (1678)**	50
						S3101A	**† Signetics (1678)**	
						74S89	**Signetics (1678)**	
						SN54S289	† TI	
			TS	16	5	SN54S189	† AMD	
						6561	MMI	
						DM54S189	† National	
						DM8599	National	
						54S189	**† Signetics (1678)**	
						SN54S189	† TI	
	53 nsF	TTL	TS	28	5	AM29705C	AMD	60
	55 nsF	TTL	OC	16	5	AM27LS02AC	AMD	
						AM27LS06C	AMD	
							(Continued)	

Static (Cont'd.)

Organization	Access Time (Max)	Type	Output	No. Pins	Supply Voltage	Device	Source	Line
16x4	55 nsF	TTL	OC	16	5	(Cont'd.)		
						27LS02C	MMI	
			TS	16	5	AM27LS03AC	AMD	
						AM27LS07C	AMD	
						27LS03C	MMI	
	55 ns*	TTL	OC	16	5	SN54LS89	† Motorola	
						SN54LS289	† Motorola	
			TS	16	5	SN54LS189	† Motorola	70
	58 nsF	TTL	TS	28	5	AM29705M	† AMD	
	60 nsF	TTL	OC	16	5	AM27LS06M	† AMD	
						3101	AMD	
						3101	Intel	
						DM7489	National	
						µPB2089	NEC America	
						S82S25	**† Signetics (1678)**	
						SN54LS289	† TI	
						SN74LS289	TI	
						SN54LS319	† TI	80
						SN74LS319	TI	
			TS	16	5	AM27LS07M	† AMD	
						SN54LS189A	† TI	
						SN74LS189A	TI	
						SN54LS219	† TI	
						SN74LS219	TI	
	60 nsR	TTL	OC	16	5	SN7489	AMD	
						7489	Fairchild	
						HD7489	Hitachi	
						M53289	Mitsubishi	90
						MC4064	Motorola	
						SN7489	TI	
	61 nsF	TTL	OC	28	5	AM29704C	AMD	
	65 nsF	TTL	OC	16	5	AM27LS02M	† AMD	
						27LS02M	† MMI	
						54S89	**† Signetics (1678)**	
			TS	16	5	AM27LS03M	† AMD	
						27LS03M	† MMI	
	68 nsF	TTL	OC	28	5	AM29704M	† AMD	
	70 nsF	TTL	OC	16	5	AM27LS02C	AMD	100
			TS	16	5	AM27LS03C	AMD	
						DM7599	† National	
	75 nsF	TTL	OC	16	5	31013	† AMD	
						5560	† MMI	
			TS	16	5	5561	† MMI	
	80 nsF	TTL	OC	16	5	DM5489	† National	
			TS	16	5	DM74LS189	National	
	85 nsF	TTL	OC	16	5	AM27LS02M	† AMD	
			TS	16	5	AM27LS03M	† AMD	
	90 nsF	TTL	OC	16	5	DM74LS289	National	110
	100 nsF	TTL	OC	16	5	L6560	MMI	
			TS	16	5	L6561	MMI	
						DM54LS189	† National	
	110 nsF	TTL	OC	16	5	DM54LS289	† National	
	110 nsR	TTL	OC	16	5	31L01C	AMD	
						31L01M	† AMD	
	120 nsF	TTL	OC	16	5	L5560	† MMI	
			TS	16	5	L5561	† MMI	
	120 nsR	CMOS	TS	18	4.5-12.5	F4710BC	Fairchild	
							(Continued)	

† Military Temperature Range (−55° to 125°C)
ns*—Nanoseconds Typical
nsF—Nanoseconds over Full Temperature Range
nsR—Nanoseconds at Room Temperature
OC—Open Collector
TS—Three-State
OE—Open Emitter

Bold face indicates additional data is provided on the page noted.

MEMORY–RAMs (Cont'd)

Organization	Access Time (Max)	Type	Output	No. Pins	Supply Voltage	Device	Source
Static							**(Cont'd.)**
16x4	120 nsR	CMOS	TS	18	4.5-12.5		(Cont'd.)
						F4710BM	† Fairchild
	280 nsR	CMOS	TS	16	3-15	MM54C89	† National
						MM74C89	National
						CD40114B	† RCA
						CD40114BE	RCA
32x2	50 nsF	TTL	OC	16	5	**N82S21**	**Signetics (1678)**
32x8	200 ns*	CMOS	TS	18	4-6	SCP1824L	† SSS
	300 ns*	CMOS	TS	18	10	HCMP1824	† Hughes
						CDP1824	† RCA
	400 ns*	CMOS	TS	18	4-12	SCP1824	† SSS
	600 ns*	CMOS	TS	18	5	HCMP1824C	† Hughes
						CDP1824C	† RCA
64x1	10 nsR	ECL	OE	16	-5.2	SN10142	TI
	12 nsF	ECL	OE	16	-5.2	μPB10142	NEC America
	15 nsF	ECL	OE	16	-5.2	μPB10148	NEC America
	15 nsR	ECL	OE	16	-5.2	HD10148	Hitachi
						10140	Signetics
						10148	Signetics
						10151	Signetics
						SN10140	TI
						SN10148	TI
	270 nsR	CMOS	—	14	3-18	MCM14505A	† Motorola
	350 nsR	CMOS	—	14	4.5-16	MCM14505C	Motorola
64x4	6 ns*	ECL	OE	24	-5.2	GXB100473	Siemens
	200 ns*	CMOS	TS	24	5-15	SCM5555	SSS
	700 nsF	CMOS	TS	16	5	MM74C910	National
	860 nsF	CMOS	TS	16	5	MM54C910	† National
	1.05 μsR	CMOS	TS	24	5-15	MCM14552A	† Motorola
	2.1 μsR	CMOS	TS	24	5-15	MCM14552C	Motorola
64x9	45 nsF	TTL	OC	28	5	**93419C**	**Fairchild (1255)**
						MBM93419	Fujitsu
						N82S09	**Signetics (1678)**
	60 nsF	TTL	OC	28	5	**93419M**	**† Fairchild (1255)**
	80 nsF	TTL	OC	28	5	**S82S09**	**† Signetics (1678)**
64x12	150 nsF	CMOS	TS	18	3-11	IM6512A	Intersil
	180 nsF	CMOS	TS	18	5	HM6511-2	† Harris
						HM6511-9	Harris
	250 nsF	CMOS	TS	18	5	HM6511C-9	Harris
	280 nsF	CMOS	TS	18	5	HM6512-2	† Harris
						HM6512-9	Harris
	460 nsF	CMOS	TS	18	3-7	**HM6512C-9**	**Harris (1370)**
						IM6512	Intersil
	600 nsF	CMOS	TS	18	3-7	IM6512C	Intersil
128x1	12 nsR	ECL	OE	16	-5.2	HD10147	Hitachi
						GXB10147	Siemens
	14 nsF	ECL	OE	16	-5.2	MB7047	Fujitsu
	15 nsF	ECL	OE	16	-5.2	F10405C	Fairchild
						MCM10147	Motorola
	15 nsR	ECL	OE	16	-5.2	10147	Signetics
						SN10147	TI
128x8	200 ns*	CMOS	TS	24	10	CDP1823	RCA
	250 ns*	NMOS	TS	24	5	**F68B10**	**Fairchild (1887)**
						MCM68B10	Motorola
							(Continued)

Organization	Access Time (Max)	Type	Output	No. Pins	Supply Voltage	Device	Source
Static							**(Cont'd.)**
128x8							(Cont'd.)
	350 nsF	NMOS	TS	24	5	MCM6810A	Motorola
	350 ns*	CMOS	TS	24	5	CDP1823C	RCA
	360 nsF	NMOS	TS	24	5	**F68A10**	**Fairchild (1887)**
						HM468A10	Hitachi
						MCM68A10	Motorola
	450 nsF	NMOS	TS	24	5	**F6810**	**Fairchild (1887,1888)**
						HM46810	Hitachi
						MCM6810A-1	Motorola
	1 μsF	NMOS	TS	24	5	**S6810**	**AMI (1790)**
128x9	500 nsF	CMOS	TS	22	5	MN1101	Panasonic
256x1	12 nsF	ECL	OE	16	-5.2	MB7042H	Fujitsu
	15 nsF	ECL	OE	16	-5.2	F100414	Fairchild
						F10414	Fairchild
						MB7042	Fujitsu
						HM2106	Hitachi
						MCM10152	Motorola
	25 nsF	ECL	OE	16	-5.2	μPB10144	NEC America
	26 nsF	ECL	OE	16	-5.2	MCM10144	Motorola
	30 nsF	ECL	OE	16	-5.2	F10410C	Fairchild
						10144	Signetics
	30 nsR	ECL	OE	16	-5.2	SP10144	Plessey
	35 nsF	ECL	OE	16	-4.25	F10411C	Fairchild
					-5.2	MBM10410	Fujitsu
						HM2105	Hitachi
		TTL	TS	16	5	AM27LS00AC	AMD
	35 nsR	ECL	OE	16	-5.2	SN10144	TI
	40 nsF	ECL	OE	16	-5.2	RI10144	Raytheon
		TTL	OC	16	5	**N82S117**	**Signetics (1678)**
			TS	16	5	93421AC	Fairchild
						N82S116	**Signetics (1678)**
	45 nsF	TTL	OC	16	5	AM27LS01C	AMD
						AM29720C	AMD
						93410AC	Fairchild
						93411AC	Fairchild
						HM2504-1	Hitachi
			TS	16	5	AM27LS00C	AMD
						AM27LS00AM	† AMD
						AM29721C	AMD
						93L420C	**Fairchild (1252)**
	50 nsF	TTL	OC	16	5	μPB2206	NEC America
						N82S17	**Signetics (1678)**
						74S301	**Signetics (1678)**
			TS	16	5	**93421C**	**Fairchild (1252)**
						DM74S200	National
						μPB2200	NEC America
						RC5340	Raytheon
						N82S16	**Signetics (1678)**
						74S200	**Signetics (1678)**
						74S201	**Signetics (1678)**
	55 nsF	TTL	OC	16	5	AM27LS01M	† AMD
						AM29720M	† AMD
						93411C	Fairchild
						HM2504	Hitachi
						6530	MMI
						RC5330	Raytheon
			TS	16	5	AM27LS00M	† AMD
							(Continued)

† Military Temperature Range (−55° to 125°C) ns*—Nanoseconds Typical nsF—Nanoseconds over Full Temperature Range nsR—Nanoseconds at Room Temperature

OC—Open Collector TS—Three-State OE—Open Emitter

MEMORY–RAMs (Cont'd)

Static (Cont'd.)

Organization	Access Time (Max)	Type	Output	No. Pins	Supply Voltage	Device	Source	Line
							(Cont'd.)	
256x1	55 nsF	TTL	TS	16	5	AM29721M	† AMD	
						93L420M	**† Fairchild (1252)**	
						6531	MMI	
	60 nsF	TTL	OC	16	5	93410C	Fairchild	
						DM74S206	National	
			TS	16	5	**93421M**	**† Fairchild (1252)**	
	65 nsF	TTL	OC	16	5	93411M	† Fairchild	
						SN74S301	† TI	
			TS	16	5	HM2505	Hitachi	10
						µPB2202	NEC America	
						SN74S201	TI	
	70 nsF	TTL	OC	16	5	93410M	† Fairchild	
						5530	† MMI	
						S82S17	**† Signetics (1678)**	
						54S301	**† Signetics (1678)**	
			TS	16	5	5531	† MMI	
						DM54S200	† National	
						RM5340	† Raytheon	
						S82S16	**† Signetics (1678)**	20
						54S200	**† Signetics (1678)**	
						54S201	**† Signetics (1678)**	
	75 nsF	TTL	OC	16	5	RM5330	† Raytheon	
	80 nsF	TTL	OC	16	5	AM27LS01LC	AMD	
						DM54S206	† National	
			TS	16	5	AM27LS00LC	AMD	
	90 nsF	TTL	TS	16	5	**93L421C**	**Fairchild (1252)**	
	95 nsF	TTL	OC	16	5	AM27LS01LM	† AMD	
			TS	16	5	AM27LS00LM	† AMD	
	100 nsF	TTL	TS	16	5	**93L421M**	**† Fairchild (1252)**	30
	115 nsF	TTL	OC	16	5	L6530	MMI	
			TS	16	5	L6531	MMI	
	130 nsF	TTL	OC	16	5	L5530	† MMI	
			TS	16	5	L5531	† MMI	
	150 ns*	CMOS	TS	16	10	CD40061A	† RCA	
	200 ns*	CMOS	TS	16	4.5-12.5	F4720C	Fairchild	
						F4720M	† Fairchild	
					3-15	F4720AC	Fairchild	
	300 ns*	CMOS	TS	16	5	CD40061	RCA	
	380 nsR	CMOS	TS	16	3-15	CD4061A	† RCA	40
	400 nsR	CMOS	TS	16	3-15	MM54C200	† National	
						MM74C200	National	
	500 nsR	CMOS	—	16	3-7	IM6523M	† Intersil	
		PMOS	TS	16	-9,5	MM1101A2	National	
	650 nsF	PMOS	TS	16	-9,5	MM4250	† National	
	800 nsF	CMOS	—	16	3-7	IM6523C	Intersil	
	900 nsF	PMOS	—	16	-12,5	MK4007	Mostek	
						MK4007-4	Mostek	
	1.5 µsF	CMOS	TS	16	5	MSM4061A	OKI	
	1 µsF	PMOS	TS	16	-9.5	MM1101A1	National	50
	1 µsR	PMOS	TS	16	-9,5	1101A1	AMD	
	1.4 µsR	CMOS	—	16	3-15	MCM14537A	† Motorola	
	1.5 µsF	PMOS	TS	16	-9,5	1101A	AMD	
						1101AM	† AMD	

(Continued)

Static (Cont'd.)

Organization	Access Time (Max)	Type	Output	No. Pins	Supply Voltage	Device	Source	Line
							(Cont'd.)	
256x1	1.5 µsF	PMOS	TS	16	-9,5	M58531	Mitsubishi	
						MM1101A	National	
	2 µsR	CMOS	—	16	3-15	MCM14537C	Motorola	
256x4	10 nsF	ECL	OE	24	-5.2	MB7071H	Fujitsu	
	12 nsF	ECL	OE	22	-5.2	MB7072E	Fujitsu	60
				24	-5.2	MB7071E	Fujitsu	
	15 nsF	ECL	OE	22	-5.2	MB7072N	Fujitsu	
				24	-5.2	MB7071N	Fujitsu	
	40 nsR	TTL	TS	16	5	SN54S207	† TI	
						SN74S207	TI	
				20	5	SN54S208	† TI	
						SN74S208	TI	
	45 nsF	TTL	OC	22	5	93412C	Fairchild	
						MCM93412C	Motorola	
			TS	22	5	**93422C**	**Fairchild (1249)**	70
						MCM93422C	Motorola	
	60 nsF	TTL	OC	22	5	93L412C	Fairchild	
						93412M	† Fairchild	
						MCM93412M	† Motorola	
			TS	22	5	**93L422C**	**Fairchild (1249)**	
						93422M	**† Fairchild (1249)**	
						MCM93422M	† Motorola	
	75 nsF	TTL	OC	22	5	93L412M	† Fairchild	
			TS	22	5	**93L422M**	**† Fairchild (1249)**	
	75 nsR	TTL	TS	16	5	SN74LS207	† TI	80
				20	5	SN74LS208	† TI	
	175 nsF	NMOS	TS	16	5	SY21H12	Synertek	
				18	5	SY21H11	Synertek	
				22	5	SY21H01	Synertek	
	180 nsF	CMOS	TS	18	10	IM6551AC	Intersil	
	180 nsR	CMOS	TS	22	10	IM6551AM	† Intersil	
						IM6561A	Intersil	
	200 nsF	NMOS	TS	16	5	SY21H12-2	Synertek	
				18	5	SY21H11-2	Synertek	
				22	5	SY21H01-2	Synertek	90
	220 nsF	CMOS	TS	16	5	**HM6562B-2**	**† Harris (1397)**	
						HM6562B-9	**Harris (1397)**	
				18	5	**HM6561B-2**	**† Harris (1389)**	
						HM6561B-9	**Harris (1389)**	
				22	5	**HM6501B-2**	**† Harris (1356)**	
						HM6501B-9	**Harris (1356)**	
						HM6551B-2	**† Harris (1389)**	
						HM6551B-9	**Harris (1389)**	
	250 nsF	CMOS	TS	18	5	MM74C921	National	
				22	5	MM74C920	National	100
					10	CDP1822	RCA	
						MWS5101DL1	† RCA	
						MWS5101EL1	RCA	
						MWS5101DL2	† RCA	
						MWS5101EL2	RCA	
		NMOS	TS	16	5	9112D	AMD	
						M5L2112A-2	Mitsubishi	
						MM2112A-2	National	
						MM2112A-2L	National	

(Continued)

† Military Temperature Range (–55° to 125°C) ns*—Nanoseconds Typical nsF—Nanoseconds over Full Temperature Range nsR—Nanoseconds at Room Temperature

OC—Open Collector TS—Three-State OE—Open Emitter

Bold face indicates additional data is provided on the page noted.

MEMORY–RAMs (Cont'd)

Static (Cont'd.)

Organization	Access Time (Max)	Type	Output	No. Pins	Supply Voltage	Device	Source	Line
256x4	250 nsF	NMOS	TS	16	5	(Cont'd.)		
						SY2112A-2	Synertek	
				18	5	9111D	AMD	
						M5L2111A-2	Mitsubishi	
						MM2111A-2	National	
						MM2111A-2L	National	
						μPD2111AL-2	**NEC Micro (1595)**	
						SY2111A-2	Synertek	
				22	5	9101D	AMD	
						M5L2101A-2	Mitsubishi	10
						MM2101A-2	National	
						μPD2101AL-2	**NEC Micro (1586)**	
						SY2101A-2	Synertek	
	275 nsF	CMOS	TS	18	5	MM54C921	† National	
				22	5	MM54C920	† National	
	300 nsF	CMOS	TS	16	5	**HM6562-2**	**† Harris (1397)**	
						HM6562-9	**Harris (1397)**	
				18	5	**HM6561-2**	**† Harris (1389)**	
						HM6561-9	**Harris (1389)**	
				22	5	**HM6501-2**	**† Harris (1356)**	20
						HM6501-9	**Harris (1356)**	
						HM6551-2	**† Harris (1389)**	
						HM6551-9	**Harris (1389)**	
		NMOS	TS	16	5	91L12C	AMD	
						91L12CM	† AMD	
						9112C	AMD	
						9112CM	† AMD	
				18	5	91L11C	AMD	
						91L11CM	† AMD	
						9111C	AMD	30
						9111CM	† AMD	
				22	5	91L01C	AMD	
						91L01CM	† AMD	
						9101C	AMD	
						9101CM	† AMD	
	350 nsF	CMOS	TS	22	5	MWS5101DL3	† RCA	
						MWS5101EL3	RCA	
		NMOS	TS	16	5	M5L2112A	Mitsubishi	
						MM2112A-L	National	
						2112A	Signetics	40
						SY2112A	Synertek	
				18	5	M5L2111A	Mitsubishi	
						MM2111	National	
						MM2111A-L	National	
						μPD2111AL	**NEC Micro (1595)**	
						2111A	Signetics	
						SY2111A	Synertek	
				22	5	3538F	Fairchild	
						M5L2101A	Mitsubishi	
						MM2101A	National	50
						MM2101A-L	National	
						μPD2101AL	**NEC Micro (1586)**	
						2101A	Signetics	
						SY2101A	Synertek	
	360 nsF	CMOS	TS	16	5	HM6562D-5	Harris	
				18	5	HM6561D-5	Harris	
					10	IM6561	Intersil	
				22	5	HM6501D-5	Harris	
						HM6551D-5	Harris	
						IM6551C	Intersil	60
							(Continued)	

Static (Cont'd.)

Organization	Access Time (Max)	Type	Output	No. Pins	Supply Voltage	Device	Source	Line
256x4	360 nsF	CMOS	TS	22	5	(Cont'd.)		
						IM6551M	† Intersil	
	400 nsF	CMOS	TS	22	5	HCM1822	† Hughes	
						CDP1822C	RCA	
		NMOS	TS	16	5	91L12B	AMD	
						91L12BM	† AMD	
						9112B	AMD	
						9112BM	† AMD	
				18	5	91L11B	AMD	
						91L11BM	† AMD	70
						9111B	AMD	
						9111BM	† AMD	
				22	5	91L01B	AMD	
						91L01BM	† AMD	
						9101B	AMD	
						9101BM	† AMD	
	450 nsF	CMOS	TS	22	5	**S5101L-1**	**AMI (1206)**	
						S5101L-2	**AMI (1206)**	
						S5101-1	**AMI (1206)**	
						S5101-2	**AMI (1206)**	80
						HM435101-1	Hitachi	
						5101-1	Intel	
						5101L-1	Intel	
						M5L5101L-1	Mitsubishi	
						MCM145101-1	**Motorola (1536)**	
						PD5101L-1	**NEC Micro (1562)**	
						MWS5101DL8	† RCA	
						MWS5101EL8	RCA	
						SCM5101-1	SSS	
						TC5501	Toshiba	90
		NMOS	TS	16	5	M5L2112A-4	Mitsubishi	
						MM2112A-4	National	
						MM2112A-4L	National	
						2112A-4	Signetics	
						SY2112A-4	Synertek	
				18	5	M2111A	† Intel	
						M5L2111A-4	Mitsubishi	
						MM2111A-4	National	
						μPD2111AL-4	**NEC Micro (1595)**	
						2111A-4	Signetics	100
						SY2111A-4	Synertek	
				22	5	3538-1	Fairchild	
						2101A-4	Intel	
						M5L2101A-4	Mitsubishi	
						MM2101A-4	National	
						MM2101A-4L	National	
						μPD2101AL-4	**NEC Micro (1586)**	
						2101A-4	Signetics	
						SY2101A-4	Synertek	
	500 nsF	NMOS	TS	16	5	2112-1	AMD	110
						91L12A	AMD	
						91L12AM	† AMD	
						9112A	AMD	
						9112AM	† AMD	
						2606-1	Signetics	
						SY2112-1	Synertek	
				18	5	2111-1	AMD	
						91L11A	AMD	
						91L11AM	† AMD	
						9111A	AMD	120
						9111AM	† AMD	
						SY2111-1	Synertek	
				22	5	2101-1	AMD	
							(Continued)	

† Military Temperature Range (−55° to 125°C) ns*—Nanoseconds Typical nsF—Nanoseconds over Full Temperature Range nsR—Nanoseconds at Room Temperature

OC—Open Collector TS—Three-State OE—Open Emitter

MEMORY–RAMs (Cont'd)

Static (Cont'd.)

Organization	Access Time (Max)	Type	Output	No. Pins	Supply Voltage	Device	Source	Line
256x4	500 nsF	NMOS	TS	22	5		(Cont'd.)	
						91L01A	AMD	
						91L01AM	†AMD	
						9101A	AMD	
						9101AM	†AMD	
						MM5269-1	National	
						SY2101-1	Synertek	
				24	5	RA3-4256	GI	
	650 nsF	CMOS	TS	22	5	**S5101**	**AMI (1206)**	
						S5101-3	**AMI (1206)**	10
						S5101L	**AMI (1206)**	
						S5101L-3	**AMI (1206)**	
						HM435101	Hitachi	
						HM435101V	Hitachi	
						5101	Intel	
						5101L	Intel	
						5101-3	Intel	
						5101L-3	Intel	
						MCM145101	**Motorola (1536)**	
						MCM145101-3	**Motorola (1536)**	20
						μPD5101L	**NEC Micro (1562)**	
						MSM573A	OKI	
						SCM5101	SSS	
						SCM5101-3	SSS	
						SY5101	Synertek	
						TC5501-1	Toshiba	
		NMOS	TS	16	5	2112-2	AMD	
						MM2112A-6	National	
						MM2112A-6L	National	
						2112A-6	Signetics	30
						SY2112-2	Synertek	
						TMM312-1	Toshiba	
				18	5	2111-2	AMD	
						MM2111A-6	National	
						MM2111A-6L	National	
						2111A-6	Signetics	
						SY2111-2	Synertek	
						TMM311-1	Toshiba	
				22	5	2101-2	AMD	
						3538-2	Fairchild	40
						RA3-4256B	GI	
						MM2101A-6	National	
						MM2101A-6L	National	
						2101A-6	Signetics	
						SY2101-2	Synertek	
				24	5	RA3-4256A	GI	
	750 nsF	NMOS	TS	16	5	2606	Signetics	
	800 nsF	CMOS	TS	22	5	**S5101-8**	**AMI (1206)**	
						M5101-4	Intel	
						M5101L-4	Intel	50
						MCM145101-8	**Motorola (1536)**	
						SCM5101-8	SSS	
	1 μsF	NMOS	TS	16	5	2112	AMD	
						2112A-1	Signetics	
						SY2112	Synertek	
				18	5	2111	AMD	
						2111A-1	Signetics	
						SY2111	Synertek	
				22	5	2101	AMD	
						RA3-4256B	EMM/Semi	60
						2101A-1	Signetics	
						SY2101	Synertek	
256x8	40 nsF	TTL	TS	22	5	**N8X350**	**Signetics (1678)**	
							(Continued)	

Static (Cont'd.)

Organization	Access Time (Max)	Type	Output	No. Pins	Supply Voltage	Device	Source	Line
256x8							(Cont'd.)	
	60 nsF	TTL	TS	22	5	**N82S208**	**Signetics (1678)**	
	400 nsF	NMOS	TS	22	5	**3539-1**	**EMM/Semi (1226)**	
	500 nsF	NMOS	TS	22	5	**3539-2**	**EMM/Semi (1226)**	
						3539-2	Fairchild	
	650 nsF	NMOS	TS	22	5	**3539**	**EMM/Semi (1226)**	
						3539	Fairchild	70
256X9	45 nsF	TTL	TS	22	5	**N82S212**	**Signetics (1678)**	
256x9	60 nsF	TTL	TS	24	5	**N82S210**	**Signetics (1678)**	
512x1	200 nsF	CMOS	—	16	10	S2222	AMI	
						2222	Nortec	
						SCM5522	SSS	
	400 nsF	CMOS	—	16	10	S2222A	AMI	
						2222A	Nortec	
512X4	320 nsF	CMOS	TS	18	5	**HM6513-9**	**Harris (1373)**	
	370 nsF	CMOS	TS	18	5	**HM6513-5**	**Harris (1373)**	
1024x1	20 nsF	ECL	OE	16	-5.2	**F10415AC**	**Fairchild (1246)**	80
						MBM10415AH	Fujitsu	
						HM2110-2	Hitachi	
	25 nsF	ECL	OE	16	-5.2	HM2110-1	Hitachi	
						GXB10415	Siemens	
	29 nsF	ECL	OE	16	-5.2	MCM10146	Motorola	
	30 nsF	TTL	OC	16	5	93415AC	Fairchild	
						MBM93415AH	Fujitsu	
						N82S110	**Signetics (1678)**	
						N93415A	Signetics	
			TS	16	5	93425AC	Fairchild	90
						N82S111	**Signetics (1678)**	
						N93425A	Signetics	
	35 nsF	ECL	OE	16	-5.2	MBM10415A	Fujitsu	
						HM2110	Hitachi	
		TTL	OC	16	5	HM2510-2	Hitachi	
	35 nsR	ECL	—	24	-4.5	**F100415C**	**Fairchild (1246)**	
			OE	16	-5.2	**F10415C**	**Fairchild (1246)**	
	35 ns*	TTL	OC	16	5	RM5500	†Raytheon	
						RC5500	Raytheon	
	40 nsF	TTL	OC	16	5	**N82S10**	**Signetics (1678)**	100
			TS	16	5	N82S11	Signetics	
	45 nsF	NMOS	OC	16	5	**2115A**	**Intel (1416)**	
						2115AL	**Intel (1416)**	
			TS	16	5	**2125A**	**Intel (1416)**	
						2125AL	**Intel (1416)**	
		TTL	OC	16	5	93415C	AMD	
						93415C	**Fairchild (1240)**	
						MBM93415A	Fujitsu	
						HM2510-1	Hitachi	
						MCM93415C	Motorola	110
						N82LS10	Signetics	
						N93415A	Signetics	
			TS	16	5	93425C	AMD	
						93425C	**Fairchild (1240)**	
						HM2511-1	Hitachi	
						MCM93425C	Motorola	
						N82LS11	Signetics	
						N93425	Signetics	
	50 nsF	TTL	OC	16	5	μPB2205	NEC America	
						SN74S314A	TI	120
							(Continued)	

† Military Temperature Range (−55° to 125°C) ns*—Nanoseconds Typical nsF—Nanoseconds over Full Temperature Range nsR—Nanoseconds at Room Temperature

OC—Open Collector TS—Three-State OE—Open Emitter

Bold face indicates additional data is provided on the page noted.

MEMORY–RAMs (Cont'd)

Static (Cont'd.)

Organization	Access Time (Max)	Type	Output	No. Pins	Supply Voltage	Device	Source	Line
1024x1	50 nsF	TTL					(Cont'd.)	
			TS	16	5	SN74S214A	TI	
	55 nsF	NMOS	OC	16	5	**M2115A**	**† Intel (1416)**	
			TS	16	5	**M2125A**	**† Intel (1416)**	
	60 nsF	NMOS	—	22	-3,7,15	IM7001-12	Intersil	
						7001	Nortec	
		TTL	OC	16	5	93L415C	AMD	
						93415M	† AMD	
						93L415C	**Fairchild (1240)**	
						93415M	**† Fairchild (1240)**	10
						MCM93415M	† Motorola	
						N93L415	Signetics	
			TS	16	5	93L425C	AMD	
						93425M	† AMD	
						93L425C	**Fairchild (1240)**	
						93425M	**† Fairchild (1240)**	
						MCM93425M	† Motorola	
						N93L425	Signetics	
	70 nsF	NMOS	OC	16	5	**S4015-2**	**AMI (1203)**	
						2115A-2	**Intel (1416)**	20
						2115AL-2	**Intel (1416)**	
			TS	16	5	**S4025-2**	**AMI (1203)**	
						2125A-2	**Intel (1416)**	
						2125AL-2	**Intel (1416)**	
			—	22	-3,7,15	IM7001-15	Intersil	
		TTL	OC	16	5	93L415M	† AMD	
						93L415M	**† Fairchild (1240)**	
						HM2510	Hitachi	
						S82LS10	† Signetics	
						S82S10	**† Signetics (1678)**	30
						S93L415	† Signetics	
						SN74S314	TI	
			TS	16	5	93L425M	† AMD	
						93L425M	**† Fairchild (1240)**	
						HM2511	Hitachi	
						S82LS11	† Signetics	
						S82S11	**† Signetics (1678)**	
						S93L425	† Signetics	
						SN74S214	TI	
	75 nsF	NMOS	OC	16	5	**M2115AL**	**† Intel (1416)**	40
			TS	16	5	**M2125AL**	**† Intel (1416)**	
		TTL	OC	16	5	93415M	† AMD	
	75 ns*	TTL	OC	16	5	SN54LS315	† TI	
						SN74LS315	TI	
			TS	16	5	SN54LS215	† TI	
						SN74LS215	TI	
	80 nsF	NMOS	—	22	-3,7,15	IM7001-16	Intersil	
	95 nsF	NMOS	OC	16	5	**S4015**	**AMI (1203)**	
			TS	16	5	**S4025**	**AMI (1203)**	
		TTL	OC	16	5	SN74LS314	TI	50
			TS	16	5	SN74LS214	TI	
	95 nsR	CMOS	TS	16	10	IM6508A-1	Intersil	
				18	10	IM6518A-1	Intersil	
	140 nsF	TTL	OC	16	5	SN54LS314	† TI	
			TS	16	5	SN54LS214	† TI	
	150 nsF	NMOS	TS	16	5	3542	Fairchild	
	150 nsR	CMOS	TS	16	10	IM6508A	Intersil	

(Continued)

Static (Cont'd.)

Organization	Access Time (Max)	Type	Output	No. Pins	Supply Voltage	Device	Source	Line
1024x1	150 nsR	CMOS	TS				(Cont'd.)	
				18	10	IM6518A	Intersil	
	150 ns*	CMOS	TS	16	5	MWS5001	RCA	60
	175 nsF	NMOS	TS	16	5	SY21H02	Synertek	
	200 nsF	CMOS	TS	16	4-11	S6508A-1	AMI	
		NMOS	TS	16	5	3542A	Fairchild	
						SY21H02-2	Synertek	
	200 ns*	CMOS	TS	16	10	CDP1821S	RCA	
	250 nsF	CMOS	TS	16	3-10	IM6508C	Intersil	
						IM6508M	† Intersil	
						μPD6508-1	**NEC Micro (1562)**	
					5	MM74C929	National	
				18	3-10	IM6518C	Intersil	70
						IM6518M	† Intersil	
					5	MM74C930	National	
		NMOS	TS	16	5	9102D	AMD	
						2102H	**Fairchild (1275)**	
						2102HM	**† Fairchild (1275)**	
						2102LH	**Fairchild (1275)**	
						2102LHM	**† Fairchild (1275)**	
						21L02H	Fairchild	
						2102A-2	Intel	
						2102AL-2	Intel	80
						MM2102A-2	National	
						MM2102A-2L	National	
						μPD2102AL-2	**NEC Micro (1591)**	
						2102A-2	Signetics	
						M2102A-2	SGS	
						M2102AL-2	SGS	
						TMM313-1	Toshiba	
	275 nsF	CMOS	TS	16	5	MM54C929	† National	
				18	5	MM54C930	† National	
	300 nsF	CMOS	TS	16	5	**S6508-1**	**AMI (1207)**	90
						IM6508-1	Intersil	
						MCM146508-1	**Motorola (1534)**	
						MCM146508-2	**† Motorola (1534)**	
						μPD6508	**NEC Micro (1562)**	
				18	5	**S6518-1**	**AMI (1208)**	
						S6518A-1	**AMI (1208)**	
						IM6518-1	Intersil	
						MCM146518-1	**Motorola (1534)**	
						MCM146518-2	**† Motorola (1534)**	
		NMOS	TS	16	5	91L02C	AMD	100
						91L02CM	† AMD	
						9102C	AMD	
						9102CM	† AMD	
	300 ns*	CMOS	TS	16	5	CDP1821C	RCA	
	305 nsF	CMOS	TS	16	5	**HM6508B-2**	**† Harris (1366)**	
						HM6508B-9	**Harris (1366)**	
				18	5	**HM6518B-2**	**† Harris (1379)**	
						HM6518B-9	**Harris (1379)**	
	350 nsF	CMOS	TS	16	4-11	**S6508A**	**AMI (1207)**	
		NMOS	TS	16	5	**2102F**	**Fairchild (1275)**	110
						2102FM	**† Fairchild (1275)**	
						2102LFM	† Fairchild	
						21L02F	Fairchild	
						2102A	Intel	
						2102AL	Intel	
						MM2102A	National	

(Continued)

† Military Temperature Range (−55° to 125°C) ns*—Nanoseconds Typical nsF—Nanoseconds over Full Temperature Range nsR—Nanoseconds at Room Temperature

OC—Open Collector TS—Three-State OE—Open Emitter

MEMORY–RAMs (Cont'd)

Static

Organization	Access Time (Max)	Type	Output	No. Pins	Supply Voltage	Device	Source	Line
1024x1	350 nsF	NMOS	TS	16	5		(Cont'd.)	
						MM2102AL	National	
						μPD2102AL	**NEC Micro (1591)**	
						2102A	Signetics	
						2102AL	Signetics	
						M2102A	SGS	
						M2102AL	SGS	
						SY2102A	Synertek	
						SYMC2102A	† Synertek	
	370 nsF	CMOS	TS	16	5	TC5508	Toshiba	10
	400 nsF	NMOS	TS	16	5	91L02B	AMD	
						91L02BM	† AMD	
						9102B	AMD	
						9102BM	† AMD	
						SY21L02B	Synertek	
						SYMC21L02B	† Synertek	
	425 nsF	CMOS	TS	16	5	**HM6508-9**	**Harris (1366)**	
				18	5	**HM6518-9**	**Harris (1379)**	
	450 nsF	CMOS	TS	16	5	SCM5102-1	SSS	
		NMOS	TS	16	5	**21021**	**Fairchild (1275)**	20
						21021M	**† Fairchild (1275)**	
						2102L1	**Fairchild (1275)**	
						2102L1M	**† Fairchild (1275)**	
						21L021	Fairchild	
						2102A-4	Intel	
						M2102A-4	† Intel	
						2102AL-4	Intel	
						M5L2102A-4	Mitsubishi	
						MM2102A-4	National	
						MM2102AL-4	National	30
						μPD2102AL-4	**NEC Micro (1591)**	
						2102A-4	Signetics	
						2102AL-4	Signetics	
						M2102A-4	SGS	
						M2102AL-4	SGS	
						TMM313-4	Toshiba	
	460 nsF	CMOS	TS	16	5	**S6508**	**AMI (1207)**	
						MCM146508	**Motorola (1534)**	
				18	5	**S6518**	**AMI (1208)**	
						S6518A	**AMI (1208)**	40
						MCM146518	**Motorola (1534)**	
	465 nsF	CMOS	TS	16	5	**HM6508-2**	**† Harris (1366)**	
				18	5	**HM6518-2**	**† Harris (1379)**	
	500 nsF	NMOS	TS	16	5	2102-1	AMD	
						9102A	AMD	
						9102AM	† AMD	
						91L02A	AMD	
						91L02AM	† AMD	
						SY21L02-1	Synertek	
						SYMC21L02-1	† Synertek	50
	550 nsF	CMOS	TS	16	5	TC5508-1	Toshiba	
	600 nsF	CMOS	TS	16	5	IM6508	Intersil	
				18	5	IM6518	Intersil	
	650 nsF	CMOS	TS	16	5	HM6508D-5	Harris	
						SCM5102	SSS	
						SY5102-3	Synertek	
				18	5	HM6518D-5	Harris	
		NMOS	TS	16	5	2102-2	AMD	
						9102	AMD	
						9102M	† AMD	60
						91L02	AMD	

(Continued)

Static (Cont'd.)

Organization	Access Time (Max)	Type	Output	No. Pins	Supply Voltage	Device	Source	Line
1024x1	650 nsF	NMOS	TS	16	5		(Cont'd.)	
						91L02M	† AMD	
						21022	**Fairchild (1275)**	
						21022M	**† Fairchild (1275)**	
						2102L2	**Fairchild (1275)**	
						2102L2M	**† Fairchild (1275)**	
						21L022	Fairchild	
						2102A-6	Intel	
						MM2102A-6	National	70
						MM2102AL-6	National	
						MSM3750-6A	OKI	
						M2102A-6	SGS	
						2102A-6	Signetics	
	800 nsF	CMOS	TS	16	5	SIL1902A	Mitel	
						SIL1902AF	† Mitel	
						SCM5102-3	SSS	
						SCM5102-8	SSS	
	850 nsF	NMOS	TS	16	5	MSM3750-8A	OKI	
	1 μsF	CMOS	TS	16	5	MSM574	OKI	80
		NMOS	TS	16	5	2102	AMD	
						SY2102	Synertek	
						SY21L02	Synertek	
1024x4	20 ns*	ECL	DE	24	-5.2	GXB100475	Siemens	
	25 nsF	ECL	—	22	-5.2	MB7077	Fujitsu	
	35 nsF	TTL	—	22	5	MB7067	Fujitsu	
	70 nsF	VMOS	TS	18	5	**S2114H**	**AMI (1196)**	
	150 nsF	CMOS	TS	18	5	MD4114	Mitel	
		NMOS	TS	18	5	MB8114H	Fujitsu	
						HM472114A-1	Hitachi	90
						2614-15	**Signetics (1669)**	
						TMS4045-15	TI	
				20	5	TMS4047-15	TI	
				22	±5,12	4104B	EMM/Semi	
		VMOS	TS	18	5	**S2114-1**	**AMI (1196)**	
						S2114A-1	**AMI (1196)**	
						S2114L-1	**AMI (1196)**	
	200 nsF	NMOS	TS	18	5	9114E	AMD	
						91L14E	AMD	
						9124E	AMD	100
						91L24E	AMD	
						2114-2	**EMM/Semi (1222)**	
						L2114-2	**EMM/Semi (1222)**	
						2114-2	**Fairchild (1281)**	
						2114L-2	**Fairchild (1281)**	
						MB8114E	Fujitsu	
						MB8114EL	Fujitsu	
						HM472114A-2	Hitachi	
						2114-2	Intel	
						2114L-2	Intel	110
						2114-2	Intersil	
						2114L-2	Intersil	
						IM7114A-2	Intersil	
						IM7114L-2	Intersil	
						MIC2114-2	Maruman	
						MIC2114L-2	Maruman	
						M5L2114L-2	**Mitsubishi (1438)**	
						MCM2114-20	**Motorola (1528)**	
						MCM21L14-20	Motorola	
						MM2114-2	National	120
						MM2114L-2	National	
						2614-20	**Signetics (1669)**	
						SY2114-2	Synertek	

(Continued)

† Military Temperature Range (−55° to 125°C) ns*—Nanoseconds Typical nsF—Nanoseconds over Full Temperature Range nsR—Nanoseconds at Room Temperature

OC—Open Collector TS—Three-State OE—Open Emitter

Bold face indicates additional data is provided on the page noted.

MEMORY–RAMs (Cont'd)

Organization	Access Time (Max)	Type	Output	No. Pins	Supply Voltage	Device	Source	Line
Static							**(Cont'd.)**	
1024x4	200 nsF	NMOS	TS	18	5		(Cont'd.)	
						SY2114L-2	Synertek	
						SY2114LV-2	Synertek	
						TMS4045-20	TI	
						TMS40L45-20	TI	
						TMM314A-1	Toshiba	
						TMM314AL-1	Toshiba	
				20	5	9142E	AMD	
						91L42E	AMD	
						2142-2	Intel	10
						2142L-2	Intel	
						SY2142-2	Synertek	
						SY2142L-2	Synertek	
						TMS4047-20	TI	
						TMS40L47-20	TI	
				22	5	9130EC	AMD	
					±5,12	4104A	EMM/Semi	
						4104US	† EMM/Semi	
						M4104US	† EMM/Semi	
		VMOS	TS	18	5	**S2114-2**	**AMI (1196)**	20
						S2114A-2	**AMI (1196)**	
						S2114L-2	**AMI (1196)**	
	250 nsF	CMOS	TS	18	5	**μPD444**	**NEC Micro (1580)**	
		NMOS	TS	18	5	**MCM2114-25**	**Motorola (1528)**	
						MCM21L14-25	Motorola	
						μPD2114L-2	**NEC Micro (1604)**	
						2614-25	**Signetics (1669)**	
						TMS4045-25	TI	
						TMS40L45-25	TI	
				20	5	TMS4047-25	TI	30
						TMS40L47-25	TI	
				22	5	9130DC	AMD	
						91L30DC	AMD	
					±5,12	M4104UM	† EMM/Semi	
						4104UM	† EMM/Semi	
	300nsF	CMOS	TS	18	5	MBM6514	Fujitsu	
						M58981-30	**Mitsubishi (1435)**	
		NMOS	TS	18	5	9114C	AMD	
						9114CM	† AMD	
						91L14C	AMD	40
						91L14CM	† AMD	
						9124C	AMD	
						9124CM	† AMD	
						91L24C	AMD	
						91L24CM	† AMD	
						2114-3	**EMM/Semi (1222)**	
						L2114-3	**EMM/Semi (1222)**	
						2114-3	**Fairchild (1281)**	
						2114L-3	**Fairchild (1281)**	
						MB8114N	Fujitsu	50
						MB8114NL	Fujitsu	
						HM472114-3	Hitachi	
						2114-3	Intel	
						2114L-3	Intel	
						2114-3	Intersil	
						2114L-3	Intersil	
						IM7114L-3	Intersil	
						MIC2114-3	Maruman	
						MIC2114L-3	Maruman	
						M5L2114L-3	**Mitsubishi (1438)**	60
						MCM2114-30	**Motorola (1528)**	
						MCM21L14-30	Motorola	
						MM2114-3	National	
							(Continued)	

Organization	Access Time (Max)	Type	Output	No. Pins	Supply Voltage	Device	Source	Line
Static							**(Cont'd.)**	
1024x4	300nsF	NMOS	TS	18	5		(Cont'd.)	
						MM2114L-3	National	
						μPD2114L-1	**NEC Micro (1604)**	
						SY2114-3	Synertek	
						SY2114L-3	Synertek	
						SY2114LV-3	Synertek	
						SYM2114-3	† Synertek	70
				20	5	9142C	AMD	
						91L42C	AMD	
						2142-3	Intel	
						2142L-3	Intel	
						SY2142-3	Synertek	
						SY2142L-3	Synertek	
				22	5	91L30CC	AMD	
						91L30CM	† AMD	
						9130CC	AMD	
						9130CM	† AMD	80
		VMOS	TS	18	5	**S2114-3**	**AMI (1196)**	
						S2114A-3	**AMI (1196)**	
						S2114L-3	**AMI (1196)**	
	320 nsF	CMOS	TS	18	5	**HM6514-2**	**† Harris (1376)**	
						HM6514-9	**Harris (1376)**	
	350 nsF	SOS/CMOS	TS	18	10	CDP1825	† RCA	
	370 nsF	CMOS	TS	18	5	**HM6514-5**	**Harris (1376)**	
	400 nsF	CMOS	TS	22	5	**HM6533-2**	**† Harris (1383)**	
						HM6533-9	**Harris (1383)**	90
		NMOS	TS	18	5	4804B	EMM/Semi	
				22	5	91L30BC	AMD	
						91L30BM	† AMD	
						9130BC	AMD	
						9130BM	† AMD	
	450 nsF	CMOS	TS	18	5	HM4334	Hitachi	
						M58981-45	**Mitsubishi (1435)**	
				20	5	**μPD445L**	**NEC Micro (1581)**	
				22	5	**HM6533C-9**	**Harris (1383)**	
		NMOS	TS	18	5	9114B	AMD	100
						9114BM	† AMD	
						91L14B	AMD	
						91L14BM	† AMD	
						9124B	AMD	
						9124BM	† AMD	
						91L24B	AMD	
						91L24BM	† AMD	
						2114	**EMM/Semi (1222)**	
						L2114U	**EMM/Semi (1222)**	
						4804A	EMM/Semi	110
						2114	**Fairchild (1281)**	
						2114L	**Fairchild (1281)**	
						HM472114-4	Hitachi	
						2114	Intel	
						2114L	Intel	
						M2114A	† Intel	
						2114	Intersil	
						2114L	Intersil	
						IM7114L	Intersil	
						MIC2114	Maruman	120
						MIC2114L	Maruman	
						M5L2114L	**Mitsubishi (1438)**	
						MCM2114-45	**Motorola (1528)**	
						MCM21L14-45	Motorola	
						MM2114	National	
							(Continued)	

† Military Temperature Range (−55° to 125°C) ns*—Nanoseconds Typical nsF—Nanoseconds over Full Temperature Range nsR—Nanoseconds at Room Temperature

OC—Open Collector TS—Three-State OE—Open Emitter

MEMORY–RAMs (Cont'd)

Static

Organization	Access Time (Max)	Type	Output	No. Pins	Supply Voltage	Device	Source	Line
1024x4	450 nsF	NMOS	TS	18	5	(Cont'd.)		
						MM2114L	National	
						μPD2114L	**NEC Micro (1604)**	
						R2114	Rockwell	
						2614-45	**Signetics (1669)**	
						SY2114	Synertek	
						SY2114L	Synertek	
						SY2114LV	Synertek	
						SYM2114	† Synertek	
						TMS4045-45	TI	10
						TMS40L45-45	TI	
						TMM314A	Toshiba	
						TMM314AL	Toshiba	
				20	5	9142B	AMD	
						91L42B	AMD	
						2142	Intel	
						2142L	Intel	
						M2142	† Intel	
						SY2142	Synertek	
						SY2142L	Synertek	20
						TMS4047-25	TI	
						TMS40L47-45	TI	
	500 nsF	NMOS	TS	22	5	91L30AC	AMD	
						91L30AM	† AMD	
						9130AC	AMD	
						9130AM	† AMD	
	550 nsF	CMOS	TS	20	5	TC5047-1	Toshiba	
	600 nsF	NMOS	TS	18	5	4804U	EMM/Semi	
	650 nsF	CMOS	TS	20	5	**μPD445L-1**	**NEC Micro (1581)**	
		SOS/CMOS						
			TS	18	5	CDP1825C	† RCA	30
	800 nsF	CMOS	TS	20	5	TC5047-2	Toshiba	
1024x8	55 nsF	NMOS	TS	24	5	MK4801-55	Mostek	
	70 nsF	NMOS	TS	24	5	MK4801-70	Mostek	
	85 nsF	NMOS	TS	22	5	**μPD8108**	**NEC Micro (1616)**	
	90 nsF	NMOS	TS	24	5	MK4801-90	Mostek	
	120 nsF	NMOS	TS	24	5	MK4118-1	Mostek	
	150 nsF	NMOS	TS	24	5	MK4118-2	Mostek	
	200 nsF	NMOS	TS	24	5	MK4118-3	Mostek	
	250 nsF	NMOS	TS	24	5	MK4118-4	Mostek	40
	300 nsF	NMOS	TS	22	5	**8108-3**	**EMM/Semi (1232)**	
	500 nsF	NMOS	TS	22	5	**8108-5**	**EMM/Semi (1232)**	
2048x1	320 nsF	CMOS	TS	18	5	**HM6503-9**	**Harris (1360)**	
	370 nsF	CMOS	TS	18	5	**HM6503-5**	**Harris (1360)**	
2048x8	150 nsF	NMOS	TS	24	5	TMS4016-15	TI	
	200 nsF	VMOS	TS	24	5	**S4028**	**AMI (1205)**	
	250 nsF	NMOS	TS	24	5	TMS4016-20	TI	
	300 nsF	NMOS	TS	24	5	TMS4016-25	TI	
4096x1	25 nsF	ECL	—	22	-5.2	MB7078	Fujitsu	
	30ns*	ECL	—	18	-5.2	**F10470C**	**Fairchild (1238)**	50
	35 nsF	ECL	OE	18	-4.5	**F100470**	**Fairchild (1238)**	
					-5.2	**F10470C**	**Fairchild (1238)**	
		TTL	—	22	5	MB7068	Fujitsu	
	40 ns*	TTL	OC	18	5	**93L470C**	**Fairchild (1234)**	
						93L470M	**† Fairchild (1234)**	

(Continued)

Static (Cont'd.)

Organization	Access Time (Max)	Type	Output	No. Pins	Supply Voltage	Device	Source	Line
4096x1	40 ns*	TTL				(Cont'd.)		
			TS	18	5	**93L471C**	**Fairchild (1234)**	
						93L471M	**† Fairchild (1234)**	
	45 nsF	NMOS	TS	18	5	HM4847-2	Hitachi	
		TTL	OC	18	5	**N82S400A**	**Signetics (1678)**	60
			TS	18	5	**N82S401A**	**Signetics (1678)**	
	50 nsF	TTL	OC	18	5	**93470C**	**Fairchild (1234)**	
			TS	18	5	**93471C**	**Fairchild (1234)**	
	55 nsF	NMOS	TS	18	5	9147-3	AMD	
						MBM2147H	Fujitsu	
						HM4847-3	Hitachi	
						2147-3	**Intel (1419)**	
						MCM2147-55	**Motorola (1510)**	
						MM2147-3	National	
						μPD2147-3	**NEC Micro (1609)**	70
						2147-3	Synertek	
						TMM315-1	Toshiba	
		VMOS	TS	18	5	**S2147-3**	**AMI (1200)**	
						S4017-3	**AMI (1204)**	
	60 nsF	TTL	OC	18	5	**93470M**	**Fairchild (1234)**	
			TS	18	5	**93471M**	**† Fairchild (1234)**	
	65 nsF	NMOS	TS	22	-5,12	4502	EMM/Semi	
	70 nsF	CMOS	TS	18	5	HM6147	Hitachi	
		NMOS	TS	18	5	9147	AMD	
						2147	**Intel (1419)**	80
						91L47	AMD	
						MBM2147E	Fujitsu	
						HM4847	Hitachi	
						2147L	**Intel (1419)**	
						MCM2147-70	**Motorola (1510)**	
						MM2147	National	
						μPD2147	**NEC Micro (1609)**	
						μPD2147L	NEC Micro	
						2147	Synertek	
						2147L	Synertek	90
						TMM315	Toshiba	
		TTL	OC	18	5	μPB2400	NEC America	
						N82S400	**Signetics (1678)**	
			TS	18	5	μPB2401	NEC America	
						N82S401	**Signetics (1678)**	
		VMOS	TS	18	5	**S2147**	**AMI (1200)**	
						S4017	**AMI (1204)**	
	80 nsF	NMOS	TS	22	±5,12	μPD410-5	NEC Micro	
	85 nsF	NMOS	TS	18	5	M2147	† Intel	
						MCM2147-85	**Motorola (1510)**	100
						μPD4104-6	**NEC Micro (1610)**	
						μPD4104-36	**NEC Micro (1610)**	
	90 nsF	NMOS	TS	22	±5,12	**μPD410-3**	**NEC Micro (1600)**	
	95 nsF	NMOS	TS	18	5	MBM2147N	Fujitsu	
	100 nsF	NMOS	TS	18	5	**MCM2147-100**	**Motorola (1510)**	
				22	±5,12	**μPD410-2**	**NEC Micro (1600)**	
					-5,12	4402B	EMM/Semi	
	120 nsF	NMOS	TS	18	5	2141-2	EMM/Semi	
						2141-2	**Intel (1418)**	
						μPD4104-5	**NEC Micro (1610)**	110
						μPD4104-35	**NEC Micro (1610)**	
				22	±5,12	**4300A**	**EMM/Semi (1230)**	

(Continued)

† Military Temperature Range (−55° to 125°C) ns*—Nanoseconds Typical nsF—Nanoseconds over Full Temperature Range nsR—Nanoseconds at Room Temperature

OC—Open Collector TS—Three-State OE—Open Emitter

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MEMORY–RAMs (Cont'd)

Static (Cont'd.)

Organization	Access Time (Max)	Type	Output	No. Pins	Supply Voltage	Device	Source	Line
4096x1								(Cont'd.)
	150 nsF	NMOS	TS	18	5	4044-15	AMD	
						4244-15	AMD	
						2141-3	EMM/Semi	
						2141-3	**Intel (1418)**	
						2141L-3	**Intel (1418)**	
						μPD4104-3	**NEC Micro (1610)**	
						μPD4104-33	**NEC Micro (1610)**	
						2613-15	**Signetics (1668)**	
						TMS4044-15	TI	10
						Z6104-2	Zilog	
				20	5	TMS4046-15	TI	
				22	-5,12	4402A	EMM/Semi	
					±5,12	4200B	EMM/Semi	
						μPD410-1	**NEC Micro (1600)**	
	200 nsF	CMOS	TS	18	5	IM6504	Intersil	
						IM6505	Intersil	
		NMOS	TS	18	5	4044-20	AMD	
						4244-20	AMD	
						2141-4	EMM/Semi	20
						MBM4044E	Fujitsu	
						2141-4	**Intel (1418)**	
						2141L-4	**Intel (1418)**	
						IM7141-2	Intersil	
						IM7141L-2	Intersil	
						M5T4044-20	**Mitsubishi (1432)**	
						MK4104-3	Mostek	
						MK4104-33	Mostek	
						MCM6641-20	Motorola	
						MCM66L41-20	Motorola	30
						MM5257-2	National	
						MM5257-2L	National	
						μPD4104-2	**NEC Micro (1610)**	
						μPD4104-32	**NEC Micro (1610)**	
						2613-20	**Signetics (1668)**	
						TMS4044-20	TI	
						TMS40L44-20	TI	
						Z6104-3	Zilog	
				20	5	TMS4046-20	TI	
						TMS40L46-20	TI	40
				22	5	9140EC	AMD	
					±5,12	4200A	EMM/Semi	
						4200US	EMM/Semi	
						M4200US	† EMM/Semi	
						μPD410	**NEC Micro (1600)**	
	250 nsF	NMOS	TS	18	5	4044-25	AMD	
						4244-25	AMD	
						2141-5	**Intel (1418)**	
						2141L-5	**Intel (1418)**	
						MK4104-4	Mostek	50
						MK4104-34	Mostek	
						MCM6641-25	Motorola	
						MCM66L41-25	Motorola	
						MM5257-25	National	
						MM5257-25L	National	
						μPD4104-1	**NEC Micro (1610)**	
						μPD4104-31	**NEC Micro (1610)**	
						2613-25	**Signetics (1668)**	
						TMS4044-25	TI	
						TMS40L44-25	TI	60
						Z6104-4	Zilog	
						TMS40L46-25	TI	
				22	5	9140 DC	AMD	
						91L40DC	AMD	

(Continued)

Static (Cont'd.)

Organization	Access Time (Max)	Type	Output	No. Pins	Supply Voltage	Device	Source	Line
4096x1	250 nsF	NMOS	TS	22	±5,12			(Cont'd.)
						M4200UM	† EMM/Semi	
						4200UM	† EMM/Semi	
	300 nsF	NMOS	TS	18	5	4044-30	AMD	
						4244-30	AMD	
						4044-3	**EMM/Semi (1228)**	70
						MBM4044N	Fujitsu	
						IM7141-3	Intersil	
						IM7141L-3	Intersil	
						M5T4044-30	**Mitsubishi (1432)**	
						MK4104-5	Mostek	
						MK4104-35	Mostek	
						MK4104-86	† Mostek	
						MCM6641-30	Motorola	
						MCM66L41-30	Motorola	
						MM5257-3	National	80
						MM5257-3L	National	
						μPD4104	**NEC Micro (1610)**	
						μPD4104-30	**NEC Micro (1610)**	
						Z6104-5	Zilog	
				22	5	91L40CC	AMD	
						91L40CM	† AMD	
						9140CC	AMD	
						9140CM	† AMD	
	320 nsF	CMOS	TS	18	5	MBM6504	Fujitsu	
						HM6504-2	**† Harris (1363)**	90
						HM6504-9	**Harris (1363)**	
	350 nsF	NMOS	TS	18	5	MK4104-6	Mostek	
						MK4104-86	† Mostek	
	370 nsF	CMOS	TS	18	5	**HM6504-5**	**Harris (1363)**	
	400 nsF	CMOS	TS	22	5	**HM6543-2**	**† Harris (1386)**	
						HM6543-9	**Harris (1386)**	
		NMOS	TS	18	5	4801B	EMM/Semi	
				22	5	91L40BC	AMD	
						91L40BM	† AMD	
						9140BC	AMD	100
						9140BM	† AMD	
	450 nsF	CMOS	TS	18	5	HM4315	Hitachi	
						MCM146504	Motorola	
				22	5	**HM6543C-9**	**Harris (1386)**	
		NMOS	TS	18	5	4044-45	AMD	
						4244-45	AMD	
						4044	**EMM/Semi (1228)**	
						L4044	**EMM/Semi (1228)**	
						4801A	EMM/Semi	
						IM7141	Intersil	110
						IM7141L	Intersil	
						M5T4044-45	**Mitsubishi (1432)**	
						MCM6641-45	Motorola	
						MCM66L41-45	Motorola	
						MM5257	National	
						MM5257L	National	
						2613-45	**Signetics (1668)**	
						TMS4044-45	TI	
						TMS40L44-45	TI	
				20	5	TMS4046-45	TI	120
						TMS40L46-45	TI	
	500 nsF	NMOS	TS	22	5	91L40AC	AMD	
						91L40AM	† AMD	
						9140AC	AMD	
						9140AM	† AMD	
	550 nsF	CMOS	TS	18	5	TC5504-1	Toshiba	

(Continued)

† Military Temperature Range (−55° to 125°C) ns*—Nanoseconds Typical nsF—Nanoseconds over Full Temperature Range nsR—Nanoseconds at Room Temperature

OC—Open Collector TS—Three-State OE—Open Emitter

MEMORY–RAMs (Cont'd)

Static (Cont'd.)

Organization	Access Time (Max)	Type	Output	No. Pins	Supply Voltage	Device	Source	Line
4096x1							(Cont'd.)	
	600 nsF	NMOS	TS	18	5	4801U	EMM/Semi	
	800 nsF	CMOS	TS	18	5	TC5504-2	Toshiba	

† Military Temperature Range (−55° to 125°C)
ns*—Nanoseconds Typical
nsF—Nanoseconds over Full Temperature Range
nsR—Nanoseconds at Room Temperature
OC—Open Collector
TS—Three-State
OE—Open Emitter

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MEMORY–ROMs

Organization	Access Time (Max)	Type	Output	No. Pins	Supply Voltage	Device	Source	Line
Dynamic								
512x8	4 µsF	CMOS	TS	24	5	MSM575	OKI	
512x10	450 nsF	PMOS	TS	28	-12,5	S8771	AMI	
1024x5	450 nsF	PMOS	TS	28	-12.5	S8771	AMI	
1024x12	3.6 µsF	PMOS	TS	28	-12,-24	EA3800	EA	
2048x4	1.3 µsF	PMOS	TS	28	-12,5	S8865	AMI	
	1.6 µsF	PMOS	—	24	-12,5	RO5-8192	GI	
2048x8	1.8 µsF	PMOS	TS	24	-12,5	S9996	AMI	
4096x4	1.8 µsF	PMOS	TS	28	-12,5	S8996	AMI	
Static								
32x8	45 nsR	TTL	OC	16	5	SN5488A	†TI	
						SN7488A	TI	10
	50 nsF	TTL	OC	16	5	**6230-1**	**MMI** (1466)	
						DM7488	National	
			TS	16	5	**6231-1**	**MMI** (1466)	
	50 nsR	TTL	OC	16	5	MCM4002L	† Motorola	
						MCM4002P	Motorola	
	60 nsF	TTL	OC	16	5	**5230-1**	**MMI** (1466)	
			TS	16	5	**5231-1**	**† MMI** (1466)	
	70 nsF	TTL	OC	16	5	DM5488	† National	
128x8	650 nsR	PMOS	—	24	±12	MM4220	† National	
						MM5220	National	20
	950 nsR	PMOS	—	24	-12,5	MM4221	† National	
						MM5221	National	
	4 µsR	PMOS	—	24	-13,-27	MM3501	National	
256x4	45 nsF	TTL	OC	16	5	93457C	Fairchild	
						6200-1	**MMI** (1466)	
			TS	16	5	93467C	Fairchild	
						6201-1	**MMI** (1466)	
	50 nsF	TTL	OC	16	5	DM74S187	National	
						N82S226	Signetics	
			TS	16	5	DM85S97	National	30
						N82S229	Signetics	
	60 nsF	TTL	OC	16	5	93457M	† Fairchild	
						5200-1	**† MMI** (1466)	
						DM54S187	† National	
						SN54187	†TI	
						SN74187	TI	
			TS	16	5	93467M	† Fairchild	
						5201-1	**† MMI** (1466)	
						DM75S97	† National	
	60 nsR	TTL	OC	16	5	DM54187	† National	
						DM74187	National	40
	70 nsF	TTL	OC	16	5	S82S226	† Signetics	
			TS	16	5	S82S229	† Signetics	
	650 nsR	PMOS	—	16	±12	MM4210	† National	
						MM5210	National	
				24	±12	MM4220	† National	
						MM5220	National	
	950 nsR	PMOS	—	16	-12,5	MM4211	† National	
						MM5211	National	
				24	-12,5	MM4221	† National	
						MM5221	National	50
	1.8 µsR	CMOS	—	16	3-15	MCM14524A	† Motorola	
						MCM14524C	Motorola	

Organization	Access Time (Max)	Type	Output	No. Pins	Supply Voltage	Device	Source	Line
Static							**(Cont'd.)**	
256x5	100 nsF	TTL	OC	16	5	**6210-1**	**MMI** (1466)	
	175 nsF	TTL	OC	16	5	**5210-1**	**† MMI** (1466)	
256x8	60 nsF	TTL	TS	24	5	N82S214	Signetics	
	70 nsF	TTL	OC	20	5	**6208-1**	**MMI** (1466)	
						SN74S271	TI	
			TS	20	5	**6209-1**	**MMI** (1466)	
						SN74S371	TI	60
	80 nsF	TTL	OC	20	5	**5208-1**	**† MMI** (1466)	
			TS	20	5	**5209-1**	**† MMI** (1466)	
	90 nsF	TTL	TS	24	5	S82S214	† Signetics	
	95 nsF	TTL	OC	20	5	SN54S271	†TI	
			TS	20	5	SN54S371	†TI	
	100 nsF	TTL	OC	24	5	**6235-1**	**MMI** (1466)	
			TS	24	5	**6236-1**	**MMI** (1466)	
	175 nsF	TTL	OC	24	5	**5235-1**	**† MMI** (1466)	
			TS	24	5	**5236-1**	**MMI** (1466)	
	180 nsR	TTL	OC	16	5	DM54L187A	† National	
						DM74L187A	National	70
	450 nsF	NMOS	TS	24	5,12	µPD464	NEC Micro	
	750 nsR	PMOS	—	24	±12	MM4230	National	
						MM5230	National	
	850 nsR	PMOS	—	24	-12,5	MM4213	† National	
						MM5213	National	
	950 nsR	PMOS	—	24	-12,5	MM4231	† National	
						MM5231	National	
						MM4252	† National	
						MM5253	National	80
	1 µsF	PMOS	TS	24	±9,-5	MM1742	National	
256x10	600 nsF	PMOS	—	24	-12,5	MK2400	Mostek	
				28	-12,5	MK2400	Mostek	
256x12	1.4 µsF	PMOS	—	28	-12,5	MM4229	† National	
						MM5229	National	
320x7	1 µsF	PMOS	—	24	-12,5	MK2300	Mostek	
384x8	900 nsR	PMOS	TS	24	-12,5	MM4241	† National	
						MM5251	National	
512x4	50 nsF	TTL	OC	16	5	93431C	Fairchild	
						N82S230	Signetics	90
			TS	16	5	93441C	Fairchild	
						N82S231	Signetics	
	55 nsF	TTL	OC	16	5	DM74S270	National	
	60 nsF	TTL	OC	16	5	93431M	† Fairchild	
						6205-1	**MMI** (1466)	
			TS	16	5	93441M	† Fairchild	
						6206-1	**MMI** (1466)	
	70 nsF	TTL	OC	16	5	S82S230	† Signetics	
						SN74S270	TI	
			TS	16	5	S82S231	† Signetics	
						SN74S370	TI	100
	75 nsF	TTL	OC	16	5	**5205-1**	**† MMI** (1466)	
			TS	16	5	**5206-1**	**† MMI** (1466)	
	95 nsF	TTL	OC	16	5	SN54S270	†TI	
			TS	16	5	SN54S370	†TI	
	725 nsR	PMOS	—	24	±12	MM4230	† National	
						MM5230	National	

(Continued)

† Military Temperature Range (−55° to 125°C) ns*—Nanoseconds Typical nsF—Nanoseconds over Full Temperature Range nsR—Nanoseconds at Room Temperature

OC—Open Collector TS—Three-State OE—Open Emitter

MEMORY–ROMs (Cont'd)

Static (Cont'd.)

Organization	Access Time (Max)	Type	Output	No. Pins	Supply Voltage	Device	Source		Line
512x4								(Cont'd.)	
	850 nsR	PMOS	TS	24	-12,5	MM4213	† National		
						MM5213	National		
	950 nsR	PMOS	—	24	-12,5	MM4231	† National		
						MM5231	National		
	1 μsR	PMOS	TS	24	-12,5	MM4243	National		
						MM5243	National		
512x5	100 nsF	TTL	OC	18	5	**6225-1**	**MMI**	**(1466)**	
	175 nsF	TTL	OC	18	5	**5225-1**	**† MMI**	**(1466)**	
	450 nsF	NMOS	TS	18	5	RO3-2560	GI		10
	500 nsR	PMOS	TS	24	±12	MM4240	† National		
						MM5240	National		
512x8	55 nsF	TTL	OC	24	5	93432C	Fairchild		
			TS	24	5	93442C	Fairchild		
	60 nsF	TTL	OC	24	5	N82S240	Signetics		
			TS	24	5	N82S215	Signetics		
						N82S241	Signetics		
	65 nsF	TTL	OC	24	5	DM87S95	National		
			TS	24	5	DM87S96	National		
	70 nsF	TTL	OC	24	5	93432M	† Fairchild		20
						6248-1	**MMI**	**(1466)**	
			TS	24	5	93442M	† Fairchild		
						6249-1	**MMI**	**(1466)**	
	75 nsR	TTL	OC	24	5	3304AL-6	Intel		
	80 nsF	TTL	OC	24	5	**5248-1**	**† MMI**	**(1466)**	
						DM77S95	† National		
			TS	24	5	**5249-1**	**† MMI**	**(1466)**	
						DM77S96	† National		
	90 nsF	TTL	OC	24	5	S82S240	† Signetics		
			TS	24	5	S82S215	† Signetics		30
						S82S241	† Signetics		
	100 nsF	TTL	OC	24	5	**6240-1**	**MMI**	**(1466)**	
			TS	24	5	**6241-1**	**MMI**	**(1466)**	
	175 nsF	TTL	OC	24	5	**5240-1**	**† MMI**	**(1466)**	
			TS	24	5	**5241-1**	**† MMI**	**(1466)**	
	350 ns*	CMOS	TS	24	4-12	SCP1832	† SSS		
	400 ns*	CMOS	TS	24	10	CDP1831	† RCA		
						CDP1832	† RCA		
						HCMP1831	† Hughes		
						HCMP1832	† Hughes		40
	500 nsF	NMOS	TS	22	5	RO3-4096	GI		
				24	5	9214C	AMD		
						9214M	† AMD		
						SY2530	Synertek		
						SY3515	Synertek		
	600 nsF	PMOS	TS	24	-12,5	3515	Fairchild		
	700 nsF	PMOS	TS	24	5	3514	AMD		
					-12,5	MK2500	Mostek		
						MK2600	Mostek		
	850 nsF	PMOS	TS	24	-12,5	3514	Fairchild		50
	850 ns*	CMOS	TS	24	5	HCMP1831C	† Hughes		
						HCMP1832C	† Hughes		
						CDP1831C	RCA		
						CDP1832C	† RCA		
						SCP1832L	† SSS		

(Continued)

Static (Cont'd.)

Organization	Access Time (Max)	Type	Output	No. Pins	Supply Voltage	Device	Source		Line
512x8								(Cont'd.)	
	1 μsF	PMOS	TS	24	-12,5	S3514	AMI		
						S5232	AMI		
						MM5244	National		
	1 μsR	PMOS	TS	24	-12,5	MM4214	† National		60
						MM5214	National		
						MM4232	† National		
						MM5232	National		
						MM4233	† National		
						MM5233	National		
	1.25 μsF	PMOS	TS	24	-12,5	MM4244	National		
512x10	500 nsF	NMOS	TS	24	5	RO3-5120	GI		
	725 nsF	PMOS	—	24	±12	EA4000	EA		
864x12 (9x96x12)									
	10 μs	PMOS		28	-12,5	S607	Siemens		70
1024x4	60 nsF	TTL	OC	18	5	**6250-1**	**MMI**	**(1466)**	
						6252-1	**MMI**	**(1466)**	
			TS	18	5	**6251-1**	**MMI**	**(1466)**	
						6253-1	**MMI**	**(1466)**	
	70 nsF	TTL	—	16	5	N8228	Signetics		
	75 nsF	TTL	OC	18	5	**5250-1**	**† MMI**	**(1466)**	
						5252-1	**† MMI**	**(1466)**	
			TS	18	5	**5251-1**	**† MMI**	**(1466)**	
						5253-1	**† MMI**	**(1466)**	
	700 nsF	PMOS	TS	24	-12,5	MK2500	Mostek		80
						MK2600	Mostek		
	1 μsF	PMOS	TS	24	-12,5	S5232	AMI		
	1 μsR	PMOS	TS	24	-12,5	MM4232	† National		
						MM5232	National		
1024x8	45 nsF	TTL	OC	24	5	93454C	Fairchild		
			TS	24	5	93464C	Fairchild		
	55 nsF	TTL	OC	22	5	**6286-2**	**MMI**	**(1469)**	
				24	5	**6280-2**	**MMI**	**(1469)**	
			TS	22	5	**6287-2**	**MMI**	**(1469)**	
			—	20	5	**6289-2**	**MMI**	**(1469)**	90
			TS	24	5	**6281-2**	**MMI**	**(1469)**	
	60 nsF	TTL	OC	24	5	93454M	† Fairchild		
			TS	24	5	93464M	† Fairchild		
	70 nsF	TTL	OC	24	5	DM85S29	National		
						N82S280	Signetics		
			TS	24	5	DM85S28	National		
						N82S281	Signetics		
	75 nsF	TTL	OC	22	5	**5286-2**	**† MMI**	**(1469)**	
				24	5	**5280-2**	**† MMI**	**(1469)**	
			TS	22	5	**5287-2**	**† MMI**	**(1469)**	100
			—	20	5	**5289-2**	**† MMI**	**(1469)**	
			TS	24	5	**5281-2**	**† MMI**	**(1469)**	
	90 nsF	TTL	OC	24	5	DM75S29	† National		
			TS	24	5	DM75S28	† National		
	100 nsF	TTL	OC	22	5	**6286-1**	**MMI**	**(1469)**	
				24	5	**6280-1**	**MMI**	**(1466)**	
						6282-1	**MMI**	**(1469)**	
						6284-1	**MMI**	**(1469)**	
						S82S280	† Signetics		

(Continued)

† Military Temperature Range (−55° to 125°C) ns*—Nanoseconds Typical nsF—Nanoseconds over Full Temperature Range nsR—Nanoseconds at Room Temperature

OC—Open Collector TS—Three-State OE—Open Emitter

Bold face indicates additional data is provided on the page noted.

MEMORY–ROMs (Cont'd)

Static (Cont'd.)

Organization	Access Time (Max)	Type	Output	No. Pins	Supply Voltage	Device	Source	Line
1024x8	100 nsF	TTL						(Cont'd.)
			TS	22	5	**6287-1**	**MMI**	**(1469)**
				24	5	**6281-1**	**MMI**	**(1466)**
						6283-1	**MMI**	**(1469)**
						6285-1	**MMI**	**(1469)**
						S82S281	†Signetics	
			—	20	5	**6289-1**	**MMI**	**(1469)**
	175 nsF	TTL	OC	22	5	**5286-1**	**†MMI**	**(1469)**
				24	5	AM27S80C	AMD	
						5280-1	**†MMI**	**(1466)**
						5282-1	**†MMI**	**(1469)**
						5284-1	**†MMI**	**(1469)**
			TS	22	5	**5287-1**	**†MMI**	**(1469)**
				24	5	AM27S81C	AMD	
						5281-1	**†MMI**	**(1466)**
						5283-1	**†MMI**	**(1469)**
						5285-1	**†MMI**	**(1469)**
			—	20	5	**5289-1**	**†MMI**	**(1469)**
	250 nsF	NMOS	TS	24	5	**F68B308**	**Fairchild**	**(1887)**
						MCM68B30A	Motorola	
						MCM68B308	Motorola	
					5,12	9208D	AMD	
	275 nsF	TTL	OC	24	5	AM27S80M	†AMD	
			TS	24	5	AM27S81M	†AMD	
	300 nsF	NMOS	TS	24	5,12	9208CC	AMD	
	350 nsF	NMOS	TS	24	5	**F68A308**	**Fairchild**	**(1887)**
						MK30000	Mostek	
						MCM68A30A	**Motorola**	**(1530)**
					±5,12	**MCM68A308**	**Motorola**	**(1530)**
						MCM68A308P7	**Motorola**	**(1530)**
					-3,5,12	MCM6560	Motorola	
						NC6560	Nitron	
	350 ns*	CMOS	TS	24	10	HCMP1833	†Hughes	
						HCMP1834	†Hughes	
						CDP1833	†RCA	
						CDP1834	†RCA	
						SCP1834	†SSS	
	400 nsF	NMOS	TS	24	5	ER2308AC	EA	
						EA8308AC	EA	
					5,12	9208BC	AMD	
						9208BM	†AMD	
	450 nsF	NMOS	TS	24	5	2607	Signetics	
						2608-1	Signetics	
					±5,12	8308	AMD	
						2308	Intel	
						2608	Intel	
						8308	Intel	
						μPD2308	NEC Micro	
						TMS4700	TI	
	500 nsF	NMOS	TS	24	5	F6830	Fairchild	
						F68308	**Fairchild** **(1887,1889)**	
						HN46830	Hitachi	
	550 nsF	NMOS	TS	24	5	EA2308AL	EA	
						EA8308AL	EA	
						2608	Signetics	
	575 nsF	NMOS	TS	24	5	MM4242	National	
	600 nsF	NMOS	TS	24	±5,12	MSM3770A	OKI	

(Continued)

Static (Cont'd.)

Organization	Access Time (Max)	Type	Output	No. Pins	Supply Voltage	Device	Source	Line
1024x8								(Cont'd.)
	850 nsF	NMOS	TS	24	±5,12	M58730	Mitsubishi	
	850 ns*	CMOS	TS	24	5	CDP1833C	†RCA	
						CDP1834C	†RCA	
						HCMP1833C	†Hughes	
						HCMP1834C	†Hughes	
						SCP1834L	†SSS	
1024x9	100 nsF	TTL	OC	24	5	**6260-1**	**MMI**	**(1469)**
			TS	24	5	**6261-1**	**MMI**	**(1469)**
	150 nsF	TTL	OC	24	5	**5260-1**	**†MMI**	**(1469)**
			TS	24	5	**5261-1**	**†MMI**	**(1469)**
1024x10	100 nsF	TTL	OC	24	5	**6255-1**	**MMI**	**(1469)**
			TS	24	5	**6256-1**	**MMI**	**(1469)**
	150 nsF	TTL	OC	24	5	**5255-1**	**†MMI**	**(1469)**
			TS	24	5	**5256-1**	**†MMI**	**(1469)**
1024x12	250 nsR	CMOS	TS	18	10	IM6312A	Intersil	
					4-11	**HM6312A-2**	**†Harris**	**(1348)**
						HM6312A-9	**Harris**	**(1348)**
	400 nsF	CMOS	TS	18	5	IM6312	Intersil	
	500 nsR	CMOS	TS	18	5	**HM6312-2**	**†Harris**	**(1348)**
						HM6312-9	**Harris**	**(1348)**
	640 nsF	CMOS	TS	18	5	**HM6312C-9**	**Harris**	**(1348)**
	3 μsR	PMOS	—	28	±12	MM5215	National	
	5 μsR	PMOS	—	28	-12,5	MM5212	National	
2048x4	125 nsF	TTL	OC	18	5	**S82S184**	**†Signetics**	**(1680)**
			TS	18	5	**S82S185**	**†Signetics**	**(1680)**
	350 nsF	NMOS	TS	24	-3,5,12	MCM6560	Motorola	
						NC6560	Nitron	
2048x8	80 nsF	TTL	OC	24	5	N82S290	Signetics	
			TS	24	5	N82S291	Signetics	
	110 nsF	TTL	OC	24	5	**6275-1**	**MMI**	**(1469)**
			TS	24	5	**6276-1**	**MMI**	**(1469)**
	120 nsF	TTL	OC	24	5	**5275-1**	**†MMI**	**(1469)**
			TS	24	5	**5276-1**	**†MMI**	**(1469)**
	125 nsF	VMOS	TS	24	5	**S4216B-1**	**AMI**	**(1209)**
						S4216D-1	AMI	
	150 ns*	I²L	OC/TTL					
				24	ma	SBP9818C	TI	
						SBP9818M	†TI	
	200 nsF	VMOS	TS	24	5	**S4216B-2**	**AMI**	**(1209)**
						S4216D-2	AMI	
	300 nsF	NMOS	TS	24	5,12	9216C	AMD	
					5	2600-1	Signetics	
						SY2316B-3	Synertek	
	350 nsF	NMOS	TS	24	5	9218C	AMD	
						RO3-9316C	GI	
						MK34000-3	Mostek	
						MCM68A316A	**Motorola**	**(1530)**
						MCM68A316E	Motorola	
						MCM68A316EP91	Motorola	
						2616-1	**Signetics**	**(1670)**
						2617-1	Signetics	
	350 ns*	I²L	OC/TTL					
				24	5	SBP8316C	TI	
						SBP8316M	†TI	

(Continued)

† Military Temperature Range (−55° to 125°C) ns*—Nanoseconds Typical nsF—Nanoseconds over Full Temperature Range nsR—Nanoseconds at Room Temperature

OC—Open Collector TS—Three-State OE—Open Emitter

MEMORY–ROMs (Cont'd)

Static (Cont'd.)

Organization	Access Time (Max)	Type	Output	No. Pins	Supply Voltage	Device	Source	Line
2048x8							(Cont'd.)	
	400 nsF	NMOS	TS	24	5	9216BC	AMD	
						9216BM	†AMD	
	450 nsF	CMOS	TS	24	5	**CM3200**	**Supertex** (1706)	
		NMOS	TS	24	5	9217BC	AMD	
						9217BM	†AMD	
						9218BC	AMD	
						9218BM	†AMD	
						S6831A	**AMI** (1215,1806)	10
						S6831B	**AMI** (1215,1806)	
						S6831C	AMI	
						S8316	AMI	
						EA8316EC	EA	
						3516	Fairchild	
						RO3-8316B	GI	
						RO3-9316B	GI	
						2316E	Intel	
						2616	Intel	20
						2616-11	Intersil	
						MIC2316E	Maruman	
						MK34000-84	†Mostek	
						MM2316A	National	
						µPD2316A	NEC Micro	
						µPD2316E	**NEC Micro** (1633)	
						R2316B	Rockwell	
						M2316	SGS	
						SAB8316	Siemens	
						2616	**Signetics** (1670)	30
						2617	Signetics	
						SY2316B	Synertek	
						TMM331A	Toshiba	
						TMM334	Toshiba	
	450 ns*	CMOS	TS	24	5	SCM5316	SSS	
	500 nsF	NMOS	TS	24	5	**S6831**	**AMI** (1215,1806)	
						F68316	Motorola	
						2600	Signetics	
					±5,12	MCM6832	Motorola	40
	525 nsF	NMOS	TS	24	5	EA8316EL	EA	
	550 nsF	NMOS	TS	24	5	9217AC	AMD	
						9217AM	†AMD	
						MK31000-3	Mostek	
						R2316A	Rockwell	
						SY4600	Synertek	
						SY8316A	Synertek	
					±5,12	MCM6832	Motorola	
	600 nsF	NMOS	TS	24	5	EA2316E	EA	
		PMOS	—	24	-12,5	MK28000	Mostek	50
	800 nsF	NMOS	TS	24	-3,5,12	MCM6590	Motorola	
						NC6590	Nitron	
	850 nsF	NMOS	TS	24	5	RO3-8316A	GI	
						RO3-9316A	GI	
						2316A	Intel	
						M58731	Mitsubishi	
	950 nsF	PMOS	—	24	-12,5	EA4900C	EA	
	1 µsF	NMOS	TS	24	5	MSM3870	OKI	
	1.35 µsF	PMOS	—	24	-12,5	EA4900L	EA	
2048x10	500 nsF	NMOS	TS	28	5	RO3-9500	GI	60
				40	5	RO3-9501	GI	
							(Continued)	

Static (Cont'd.)

Organization	Access Time (Max)	Type	Output	No. Pins	Supply Voltage	Device	Source	Line
2048x10	500 nsF	NMOS	TS	40	5		(Cont'd.)	
						RO3-9502	GI	
4096x4	550 nsF	NMOS	TS	24	5	SY4600	Synertek	
	600 nsF	PMOS	—	24	-12,5	MK28000	Mostek	
	1 µsF	NMOS	TS	24	5	RO3-16384	GI	
4096x5	450 nsF	NMOS	TS	22	5	2620	Signetics	
4096x8	300 nsF	NMOS	TS	24	5	9232C	AMD	
						9233C	AMD	
						2332	Intel	70
						R2332-3	Rockwell	
	350 nsF	NMOS	TS	24	5	RO3-9332C	GI	
						MCM68A332	Motorola	
						MCM68A332P2	Motorola	
				28	5	EA3200	EA	
	450 nsF	NMOS	TS	24	5	9232BC	AMD	
						9232BM	†AMD	
						9233BC	AMD	
						9233BM	†AMD	
						S68332	**AMI** (1216)	80
						EA2332C	EA	
						RO3-9332B	GI	
						MIC2332	Maruman	
						M58333	Mitsubishi	
						MM5235	National	
						µPD2332	**NEC Micro** (1637)	
						R2332	Rockwell	
						SAB8332	Siemens	
						2632	**Signetics** (1672)	
						ROM4732	SMC	90
						SY2332	Synertek	
						TMS4732	TI	
						TMM333	Toshiba	
	600 nsF	NMOS	TS	28	5	HN46532-3	Hitachi	
	850 nsF	NMOS	TS	24	5	RO3-9332A	GI	
8192x8	250 nsF	NMOS	TS	24	5	MK36000-4	Mostek	
						MCM68B364	Motorola	
	300 nsF	NMOS	TS	24	5	2364	Intel	
	350 nsF	NMOS	TS	24	5	**MCM68A364**	**Motorola** (1530)	
						MCM68A364P3	**Motorola** (1530)	100
		VMOS	TS	24	5	**S4264**	**AMI** (1212)	
	450 nsF	NMOS	TS	24	5	RO3-9364B	GI	
						µPD2364	**NEC Micro** (1640)	
						2664	**Signetics** (1674)	
						SY2364	Synertek	
	550 nsF	CMOS	TS	24	5	**HM6388**	**†Harris** (1352)	
				28	5	**HM6389**	**†Harris** (1354)	
	800 nsF	NMOS	TS	28	5	MM4235	†National	
						MM5235	National	
16384x4	450 nsF	NMOS	TS	22	5	2666	Signetics	110
16384x8	450 nsF	NMOS	TS	28	5	26128	Signetics	

† Military Temperature Range (−55° to 125°C) ns*—Nanoseconds Typical nsF—Nanoseconds over Full Temperature Range nsR—Nanoseconds at Room Temperature

OC—Open Collector TS—Three-State OE—Open Emitter

Bold face indicates additional data is provided on the page noted.

MEMORY–Shift Registers

Dynamic

Bits Per Register	No. of Reg.	Operation	Process	Frequency (Hz - Spec)	Supply Voltage	Device	Source	Line
16	4	SS	PMOS	3.0 M	-28	EA1208	EA	
32	4	SS	PMOS	1.0 M	-28	EA1201	EA	
				3.0 M	-28	EA1200	EA	
64	1	SS	PMOS	1.0 M	-14,-28	EA1203	EA	
				3.0 M	-14,-28	EA1202	EA	
	2	SS	PMOS	0.1 M	-14	HD3213	Hitachi	
					-14,9	HD3214	Hitachi	
				10.0 M	-17	HDSR2164	Hughes	
	3	SS	PMOS	0.1 M	-14	HD3214	Hitachi	
	4	SS	PMOS	5.0 M	-12,5	TMS3417	TI	10
					±5	HD3508	Hitachi	
72	3	SS	PMOS	5.0 M	±5	HD3523	Hitachi	
						HD3524	Hitachi	
80	4	SS	PMOS	2.5 M	-12,5	MK1007	Mostek	
				5.0 M	-12,5	TMS3409	TI	
100	2	SS	PMOS	1.0 M	±5	HD3506	Hitachi	
						HD3507	Hitachi	
				2.0 M	±5	1406	†AMD	
						1407	†AMD	
						1506	AMD	20
						1507	AMD	
				2.5 M	-12,5	MM4006	†National	
						MM5006	National	
128	2	SS	PMOS	5.0 M	±5	HD3509	Hitachi	
200	1	SS	CMOS	2.5 M	3-15	CD4062A	†RCA	
			PMOS	1.0 M	-28	EA1221	EA	
256	1	SS	PMOS	1.0 M	-28	EA1205	EA	
				2.5 M	±5	HD3510	Hitachi	
				3.0 M	-14	EA1204	EA	
	2	SS	PMOS	2.5 M	-14	EA1210	EA	30
	4	SS	PMOS	2.5 M	±5	SY1402B	Synertek	
						SY1402BR	Synertek	
				3.0 M	±5	HDSR1026	Hughes	
						M58502	Mitsubishi	
				5.0 M	±5	1402AC	AMD	
						1402AM	†AMD	
						HD3502	Hitachi	
						1402A	Intel	
						MM1402A	National	
						1402	Nortec	40
						1402A	Nortec	
						SY1402A	Synertek	
						SY1402AR	Synertek	
				10.0 M	±5	AM2802C	AMD	
						AM2802M	†AMD	
						SY2802	Synertek	
32-678	2	SS	PMOS	2.5 M	-12,5	MM4104	†National	
						MM5104	National	
455	2	SS	CCD	20.0 M	17	CCD321	Fairchild	
512	1	SS	PMOS	2.0 M	±5	1405A	AMD	50
						1405A	Intel	
				2.5 M	-12,5	MM4016	†National	
						MM5016	National	
				3.0 M	±5	AM2805M	†AMD	
						AM2807M	†AMD	

(Continued)

Dynamic (Cont'd.)

Bits Per Register	No. of Reg.	Operation	Process	Frequency (Hz - Spec)	Supply Voltage	Device	Source	Line
512	1	SS	PMOS	3.0 M			(Cont'd.)	
					-14	EA1212	EA	
				4.0 M	±5	AM2805C	AMD	
						AM2807C	AMD	
				5.0 M	±5	HD3505	Hitachi	60
					-27	EA1206	EA	
	2	SS	PMOS	2.5 M	±5	SY1403B	Synertek	
				3.0 M	±5	M58503	Mitsubishi	
				5.0 M	±5	1403AC	AMD	
						1403AM	†AMD	
						HD3503	Hitachi	
						1403A	Intel	
						MM1403A	National	
						1403A	Nortec	
						SY1403A	Synertek	70
				8.0 M	±5	HDSR1025	Hughes	
				10.0 M	±5	AM2803C	AMD	
						AM2803M	†AMD	
						SY2803	Synertek	
1024	1	SS	NMOS	1.0 M	5	2405	Intel	
						SY2405	Synertek	
			PMOS	3.0 M	±5	AM2806M	†AMD	
						AM2808M	†AMD	
						M58504	Mitsubishi	
						2512	Nortec	80
				4.0 M	±5	AM2806C	AMD	
						AM2808C	AMD	
						2512	Nortec	
				5.0 M	±5	1404AC	AMD	
						1404AM	†AMD	
						HD3504	Hitachi	
						1404A	Intel	
						MM1404A	National	
						MM5024A	National	
						1404A	Nortec	90
					5	SY1404A	Synertek	
				8.0 M	±5	HDSR1024	Hughes	
						M130	SGS	
				10.0 M	±5	AM2804C	AMD	
						AM2804M	†AMD	
						SY2804	Synertek	
	2	SS	NMOS	1.0 M	5	AM2401	AMD	
						2401	Intel	
						SY2401	Synertek	
				2.0 M	5	9401C	AMD	100
						9401M	†AMD	
				2.5 M	5	SY2401-1	Synertek	
			PMOS	2.0 M	-12,5	MM4025	†AMD	
						MM4026	†AMD	
						MM4025	†National	
						MM4026	†National	
				2.5 M	-12,5	MM5025	National	
						MM5026	National	
				4.0 M	-10.5,5	AM2825M	†AMD	
						AM2826M	†AMD	110
				6.0 M	-10.5,5	AM2825C	AMD	
						AM2826C	AMD	
						SY2825A	Synertek	
						SY2826A	Synertek	

(Continued)

† Military Temperature Range (−55° to 125°C)

SS = Serial In, Serial Out

PP = Parallel In, Parallel Out

* Typical Values

MEMORY–Shift Registers (Cont'd)

Bits Per Register	No. of Reg.	Operation	Process	Frequency (Hz - Spec)	Supply Voltage	Device	Source	Line
Dynamic							**(Cont'd.)**	
1024	2	SS	PMOS				(Cont'd.)	
				8.0 M	±5	HDSR2048	Hughes	
2048	1	SS	PMOS	2.0 M	-12,5	MM4027	† AMD	
						MM4027	† National	
				2.5 M	-12,5	MM5027	National	
				4.0 M	-10.5,5	AM2827M	† AMD	
				6.0 M	-10.5,5	AM2827C	AMD	
						SY2827	Synertek	
4096	4	PP	CCD	5.0 M	±5,12	CCD460	Fairchild	
65536	1	SS	CCD	25 M	±5,12	**F464**	**Fairchild (1276)**	10
						TMS3064	TI	
Static								
4	1	PP	Bipolar	25 M	5	SN54L95	TI	
						SN54L99	† TI	
				3 M	5	SN74L99	TI	
						SN74L95	TI	
					12	375A/C	Teledyne S	
					15	375B/M	Teledyne S	
				5 M	5	93L00C	† AMD	
						93L00M	† AMD	
				6 M	5	DM54L95	† National	20
						DM74L95	National	
				15 M	5	9300C	AMD	
						9300M	† AMD	
						93L00C	Fairchild	
						93L00M	† Fairchild	
						M5395	Mitsubishi	
						M53295	Mitsubishi	
						MC8300	Motorola	
						MC9300	† Motorola	
						RC9300	Raytheon	30
						RM9300	† Raytheon	
						N8270	Signetics	
						S8270	† Signetics	
						N8271	Signetics	
						S8271	† Signetics	
				20 M	5	HD2534	Hitachi	
						MC7270	Motorola	
						MC7271	Motorola	
						MC8270	Motorola	
						MC8271	Motorola	40
						RC8270	Raytheon	
						RM8270	† Raytheon	
						RC8271	Raytheon	
						RM8271	† Raytheon	
						74LS295A	Signetics	
						9LS95BC	Raytheon	
						9LS95BM	† Raytheon	
						54LS95B	† Raytheon	
						74LS95B	Raytheon	
				25 M	5	SN54194	† AMD	50
						SN74194	AMD	
						SN54LS194A	† AMD	
						SN74LS194A	AMD	
						5495	† Fairchild	
						7495	Fairchild	
						54178	† Fairchild	
						74178	Fairchild	
						54179	† Fairchild	
						74179	Fairchild	
							(Continued)	

Bits Per Register	No. of Reg.	Operation	Process	Frequency (Hz - Spec)	Supply Voltage	Device	Source	Line
Static							**(Cont'd.)**	
4	1	PP	Bipolar	25 M	5		(Cont'd.)	60
						54194	† Fairchild	
						74194	Fairchild	
						ZN5495A	† Ferranti	
						ZN7495A	Ferranti	
						ZN54194	† Ferranti	
						ZN74194	Ferranti	
						HD74194	Hitachi	
						HD74LS194A	Hitachi	
						MC54194	† Motorola	
						MC74194	Motorola	70
						DM5495	† National	
						DM7495	National	
						DM54194	† National	
						DM74194	National	
						μPB74LS194	NEC America	
						9LS395C	Raytheon	
						9LS395M	† Raytheon	
						54LS395	† Raytheon	
						74LS395	Raytheon	
						5495A	† Signetics	80
						7495A	Signetics	
						74LS95B	Signetics	
						54194	† Signetics	
						74194	Signetics	
						74LS194	Signetics	
						SN5495A	† TI	
						SN7495A	TI	
						SN54LS95B	† TI	
						SN74LS95B	TI	
						SN54178	† TI	90
						SN74178	TI	
						SN54179	† TI	
						SN74179	TI	
						SN54194	TI	
						SN74194	TI	
						SN54LS194A	† TI	
						SN74LS194A	TI	
				30 M	5	SN54195	† AMD	
						SN74195	AMD	
						SN54LS195A	† AMD	100
						SN74LS195A	AMD	
						9LS95C	Fairchild	
						9LS95M	† Fairchild	
						54LS95B	† Fairchild	
						74LS95B	Fairchild	
						9LS194C	Fairchild	
						9LS194M	† Fairchild	
						54LS194A	Fairchild	
						74LS194A	Fairchild	
						9LS195C	Fairchild	110
						9LS195M	† Fairchild	
						54195	† Fairchild	
						74195	Fairchild	
						54LS195A	† Fairchild	
						74LS195A	Fairchild	
						9LS295C	Fairchild	
						9LS295M	† Fairchild	
						54LS295A	† Fairchild	
						74LS295A	Fairchild	
						9LS395C	Fairchild	120
						9LS395M	† Fairchild	
						54LS395	† Fairchild	
						74LS395	Fairchild	
						9300C	Fairchild	
						9300M	† Fairchild	
						HD74195	Hitachi	
							(Continued)	

† Military Temperature Range (−55° to 125°C)

SS = Serial In, Serial Out

PP = Parallel In, Parallel Out

* Typical Values

Bold face indicates additional data is provided on the page noted.

MEMORY–Shift Registers (Cont'd)

Bits Per Register	No. of Reg.	Operation	Process	Frequency (Hz - Spec)	Supply Voltage	Device	Source	Line
Static							**(Cont'd.)**	
4	1	PP	Bipolar	30 M	5		(Cont'd.)	
						HD74LS195A	Hitachi	
						SN54LS95B	† Motorola	
						SN74LS95B	Motorola	
						SN54LS194A	† Motorola	
						SN74LS194A	Motorola	
						MC54195	† Motorola	
						MC74195	Motorola	
						SN54LS195A	† Motorola	
						SN74LS195A	Motorola	10
						SN54LS295A	† Motorola	
						SN74LS295A	Motorola	
						SN54LS395	† Motorola	
						SN74LS395	Motorola	
						DM5495	† National	
						DM7495	National	
						DM54195	† National	
						DM74195	National	
						DM8300	National	
						DM9300	† National	20
						μPB74195	NEC America	
						μPB74LS195	NEC America	
						μPB74LS295	NEC America	
						μPB74LS395	NEC America	
						9LS194AC	Raytheon	
						9LS194AM	† Raytheon	
						SN54LS194A	† Raytheon	
						SN74LS194A	Raytheon	
						9LS195AC	Raytheon	
						9LS195AM	† Raytheon	30
						54LS195A	† Raytheon	
						74LS195A	Raytheon	
						9LS295AC	Raytheon	
						9LS295AM	† Raytheon	
						54LS295A	† Raytheon	
						74LS295A	Raytheon	
						54195	† Signetics	
						74195	Signetics	
						54LS195A	† Signetics	
						74LS195A	Signetics	40
						74LS395	Signetics	
						S9300	Signetics	
						SN54195	† TI	
						SN74195	TI	
						SN54LS195A	† TI	
						SN74LS195A	TI	
						SN54LS295B	† TI	
						SN74LS295B	TI	
						SN54LS395A	† TI	
						SN74LS395A	TI	50
				31 M	5	MC5495A	† Motorola	
						MC7495A	Motorola	
				35 M	5	AM25LS194AC	AMD	
						AM25LS194AM	† AMD	
						MC4012	Motorola	
						MC4312	† Motorola	
						25LS194AC	Raytheon	
						25LS194AM	† Raytheon	
						25LS195AC	Raytheon	
						25LS195AM	† Raytheon	60
				38 M	5	9300C	Fairchild	
						9300M	† Fairchild	
				40 M	5	N82S70	Signetics	
						N82S71	† Signetics	
						74S178	Signetics	
						74S179	Signetics	
							(Continued)	

Bits Per Register	No. of Reg.	Operation	Process	Frequency (Hz - Spec)	Supply Voltage	Device	Source	Line
Static							**(Cont'd.)**	
4	1	PP	Bipolar				(Cont'd.)	
				45 M	5	93H00C	† Fairchild	
						93H00M	† Fairchild	
						93H72C	Fairchild	70
						93H72M	† Fairchild	
				70 M	5	SN54S194	† AMD	
						SN74S194	AMD	
						SN54S195	† AMD	
						SN74S195	AMD	
						93S00C	Fairchild	
						93S00M	† Fairchild	
						54S194	† Fairchild	
						74S194	Fairchild	
						74S194	Signetics	80
						74S195	Signetics	
						SN54S194	† TI	
						SN74S194	TI	
						SN54S195	† TI	
						SN74S195	TI	
				140 M	-5.2	95H00C	Fairchild	
				150 M	-5.2	F10000C	Fairchild	
					-5.2	F95000	Fairchild	
					-5.2	MC10141	Motorola	
						MC10541	† Motorola	90
						10141	Signetics	
				250 M	-5.2	F10141	Fairchild	
		PS	Bipolar	10 M	5	5494	† Fairchild	
						7494	Fairchild	
						ZN5494	† Ferranti	
						ZN7494	Ferranti	
						HD2533	Hitachi	
						MC5494	† Motorola	
						MC7494	Motorola	
						5494	Signetics	100
						7494	Signetics	
						SN5494	† TI	
						SN7494	TI	
		SP		325 M	-5.2	MC1694	† Motorola	
		SS		0.5 M	15	MC686	Motorola	
		PP	CMOS	2 M	3-15	F4035BM	† Fairchild	
						F40194BM	† Fairchild	
						F40195BM	† Fairchild	
						HD14035B	Hitachi	
						MC14035BC	Motorola	110
						CD4035BC	National	
						MM54C195	† National	
						μPD4035B	NEC America	
						MSM4035	OKI	
						SCL4035BE	† SSS	
						CD4035BE	RCA	
						SCL4035B	SSS	
						CM4035AE	Solitron	
						TC4035	Toshiba	
				3 M	3-15	F4035BC	Fairchild	120
						F40194BC	Fairchild	
						F40195BC	Fairchild	
						SIL4035B	† Mitel	
						SIL4035BE	Mitel	
						MC14035BA	† Motorola	
						CD4035BM	† National	
						MM74C195	National	
						CD4035B	† RCA	
						CM4035A	† Solitron	
							(Continued)	

† Military Temperature Range (−55° to 125°C)

SS = Serial In, Serial Out

PP = Parallel In, Parallel Out

* Typical Values

MEMORY–Shift Registers (Cont'd)

Bits Per Register	No. of Reg.	Operation	Process	Frequency (Hz - Spec)	Supply Voltage	Device	Source	Line
Static							**(Cont'd.)**	
4	1	PP	CMOS	3 M	3-15		(Cont'd.)	
						TP4035B	TI	
				4.5 M	3-15	MC14194BA	† Motorola	
						µPD4194B	NEC America	
						MSM40194	OKI	
						CD40194B	† RCA	
						CD40194BE	RCA	
				6.5 M	3-15	MM54C95	† National	
						MM74C95	National	
				9 M*	3-15	MSM40104	OKI	10
						CD40104B	† RCA	
						CD40104BE	RCA	
	2	SP	CMOS	1 M	5	CM4015AE	Solitron	
				1.5 M	5	CM4015A	† Solitron	
					3-15	TP4015A/B	TI	
				2.5 M	3-15	F4015BC	Fairchild	
						HD14015B	Hitachi	
						MC14015BC	Motorola	
						CD4015AC	National	
						µPD4015B	NEC America	20
						CD4015BE	RCA	
						TC4015	Toshiba	
				3 M	3-15	F4015BM	† Fairchild	
						SIL4015B	† Mitel	
						SIL4015BE	Mitel	
					3-18	MC14015BA	† Motorola	
					3-15	CD4015AM	† National	
						CD4015B	† RCA	
						SCL4015B	† SSS	
						SCL4015BE	SSS	30
5	1	PP	Bipolar	10 M	5	5496	† Fairchild	
						7496	Fairchild	
						ZN5496	† Ferranti	
						ZN7496	Ferranti	
						HD7496	Hitachi	
						M53296	Mitsubishi	
						M54403	Mitsubishi	
						MC5496	† Motorola	
						MC7496	Motorola	
						DM5496	† National	40
						DM7496	National	
						5496	† Signetics	
						7496	Signetics	
						54LS96	Signetics	
						74LS96	Signetics	
						SN5496	† TI	
						SN7496	TI	
				25	5	SN54LS96	† TI	
						SN74LS96	TI	
	4	SS	CMOS	1.2 M	5	CM4006AE	Solitron	50
				1.5 M	5	CM4006AD	† Solitron	
				2 M	3-15	F4006BC	Fairchild	
						CD4006AC	National	
						µPD4006	NEC America	
						CD4006BE	RCA	
						CM4006A	† Solitron	
						CM4006AE	Solitron	
				2.5 M	3-15	F4006M	† Fairchild	
						CD4006A	† National	
						CD4006B	† RCA	60
				3 M	3-15	SCL4006B	† SSS	

(Continued)

Bits Per Register	No. of Reg.	Operation	Process	Frequency (Hz - Spec)	Supply Voltage	Device	Source	Line
Static							**(Cont'd.)**	
5	4	SS	CMOS	3 M	3-15		(Cont'd.)	
						SCL4006BE	SSS	
				4 M	5-15	MC14006BC	Motorola	
				7 M	5-15	MC14006BA	† Motorola	
8	1	PP	Bipolar	15 M	5	DM7546	† National	
						DM8546	National	
				25 M	5	SN54LS299	† AMD	
						SN74LS299	AMD	
						54198	† Fairchild	70
						74198	Fairchild	
						54199	† Fairchild	
						74199	Fairchild	
						HD74198	Hitachi	
						HD74199	Hitachi	
						M53398	Mitsubishi	
						M53399	Mitsubishi	
						DM54198	† National	
						DM74198	National	
						DM54199	† National	80
						DM74199	National	
						µPB74198	NEC America	
						54198	† Signetics	
						74198	Signetics	
						54199	† Signetics	
						74199	Signetics	
						SN54198	† TI	
						SN74198	TI	
						SN54199	† TI	
						SN74199	† TI	90
				30 M	5	AM25LS299C	AMD	
						AM25LS299M	† AMD	
				35 M	5	AM25LS23C	AMD	
						AM25LS23M	† AMD	
						SN54LS323	† AMD	
						SN74LS323	AMD	
						54LS299	† Fairchild	
						74LS299	Fairchild	
						54LS323	† Fairchild	
						74LS323	Fairchild	100
						54LS299	† MMI	
						74LS299	MMI	
						54LS323	† MMI	
						74LS323	MMI	
						25LS299C	**Raytheon** (533)	
						25LS299M	**† Raytheon** (533)	
						25LS23C	Raytheon	
						25LS23M	† Raytheon	
						9LS299C	**Raytheon** (533)	
						9LS299M	**† Raytheon** (533)	110
						9LS323C	**Raytheon** (540)	
						9LS323M	**† Raytheon** (540)	
						54LS323	**† Raytheon** (540)	
						74LS323	**Raytheon** (540)	
						SN54LS299	† TI	
						SN74LS299	TI	
						SN54LS323	† TI	
						SN74LS323	TI	
				50 M	5	SN54S299	† TI	
						SN74S299	TI	120
		PS	Bipolar	14 M	5	DM7590	† National	
						DM8590	National	
				20 M	5	54165	† Fairchild	
						74165	Fairchild	
						ZN54165	† Ferranti	

(Continued)

† Military Temperature Range (−55° to 125°C)

SS = Serial In, Serial Out

PP = Parallel In, Parallel Out

* Typical Values

Bold face indicates additional data is provided on the page noted.

MEMORY–Shift Registers (Cont'd)

Bits Per Register	No. of Reg.	Operation	Process	Frequency (Hz - Spec)	Supply Voltage	Device	Source	Line
Static							**(Cont'd.)**	
8	1	PS	Bipolar	20 M	5		(Cont'd.)	
						ZN74165	Ferranti	
						M53365	Mitsubishi	
						MC54165	†Motorola	
						MC74165	Motorola	
						DM54165	†National	
						DM74165	National	
						54165	†Signetics	
						74165	Signetics	
						SN54165	†TI	10
						SN74165	TI	
				25 M	5	74LS165	Fairchild	
						54166	†Fairchild	
						74166	Fairchild	
						ZN54166	†Ferranti	
						ZN74166	Ferranti	
						HD74166	Hitachi	
						M53366	Mitsubishi	
						SN54LS165	†Motorola	
						SN74LS165	Motorola	20
						DM54166	†National	
						DM74166	National	
						54166	†Signetics	
						74166	Signetics	
						SN54LS165	†TI	
						SN74LS165	TI	
						SN54166	†TI	
						SN74166	TI	
						SN54LS166	†TI	
						SN74LS166	TI	30
		SP	Bipolar	6 M	5	DM54L164A	†National	
						DM74L164A	National	
				12 M	5	SN54L164	†TI	
						SN74L164	TI	
				25 M	5	SN54164	†AMD	
						SN74164	AMD	
						SN54LS164	†AMD	
						SN74LS164	AMD	
						54164	†Fairchild	
						74164	Fairchild	40
						54LS164	†Fairchild	
						74LS164	Fairchild	
						ZN54164	†Ferranti	
						ZN74164	Ferranti	
						HD74164	Hitachi	
						HD74LS164	Hitachi	
						M53364	Mitsubishi	
						SN54LS164	†Motorola	
						SN74LS164	Motorola	
						DM7570	†National	50
						DM8570	National	
						DM54164	†National	
						DM74164	National	
						DM54LS164	†National	
						DM74LS164	National	
						μPB74164	NEC America	
						μPB74LS164	NEC America	
						9LS164C	Raytheon	
						9LS164M	†Raytheon	
						54LS164	†Raytheon	60
						74LS164	Raytheon	
						54164	†Signetics	
						74164	Signetics	
						54LS164	†Signetics	
						74LS164	Signetics	
						SN54164	†TI	

(Continued)

Bits Per Register	No. of Reg.	Operation	Process	Frequency (Hz - Spec)	Supply Voltage	Device	Source	Line
Static							**(Cont'd.)**	
8	1	SP	Bipolar	25 M	5		(Cont'd.)	
						SN74164	TI	
						SN54LS164	†TI	
						SN74LS164	TI	70
						TD3503	Toshiba	
				35 M	5	AM25LS164C	AMD	
						AM25LS164M	†AMD	
				350 M	-5.2	F10041	Fairchild	
		SS	Bipolar	3 M	5	SN54L91	†TI	
						SN74L91	TI	
				4 M	5	DM54L91	†National	
						DM74L91	National	
				10 M	5	5491	†Fairchild	
						7491	Fairchild	80
						ZN5491	†Ferranti	
						ZN7491	Ferranti	
						HD2524	Hitachi	
						M5391	Mitsubishi	
						M53291	Mitsubishi	
						MC5491A	†Motorola	
						MC7491A	Motorola	
						SN5491A	†National	
						SN7491A	National	
						μPB7491	NEC America	90
						9LS91C	Raytheon	
						9LS91M	†Raytheon	
						54LS91	†Raytheon	
						74LS91	Raytheon	
						5491	†Signetics	
						7491	Signetics	
						SN5491A	†TI	
						SN7491A	TI	
						SN54LS91	†TI	
						SN74LS91	TI	100
						TD3491	Toshiba	
				15 M	5	N8276	Signetics	
		PP	CMOS	2.5 M	3-18	MC14034BC	Motorola	
					3-15	SCL4034BE	SSS	
					5	CM4034AE	Solitron	
				3 M	3-18	HD14034B	Hitachi	
						MC14034BA	Motorola	
					3-15	CD4034BC	National	
						CD4034BM	National	
						μPD4034	NEC America	110
						CD4034B	†RCA	
						SCL4034B	†SSS	
					5	CM4034A	†Solitron	
					3-15	TC4034	Toshiba	
		PS	CMOS	1 M	3-15	F4014BC	Fairchild	
						F4021BC	Fairchild	
						CM4014A	†Solitron	
				1.3 M	3-15	TP4021A	TI	
				2.5 M	3-15	HD14021B	Hitachi	
						MC14021BC	Motorola	120
						CD4014AC	National	
						CD4021AC	National	
						μPD4014	NEC America	
						μPD4021	NEC America	
						CD4014BE	RCA	
						CD4021BE	RCA	
						SCL4014BE	SSS	

(Continued)

† Military Temperature Range (−55° to 125°C)

SS = Serial In, Serial Out

PP = Parallel In, Parallel Out

* Typical Values

MEMORY–Shift Registers (Cont'd)

Bits Per Register	No. of Reg.	Oper-ation	Process	Frequency (Hz - Spec)	Supply Voltage	Device	Source	Line
Static							**(Cont'd.)**	
8	1	PS	CMOS	2.5 M	3-15		(Cont'd.)	
						SCL4021BE	SSS	
						CM4018AE	Solitron	
						CM4021AE	Solitron	
						TC4014	Toshiba	
						TC4021	Toshiba	
						TP4014A	TI	
				3 M	3-15	F4014BM	† Fairchild	
						F4021BM	† Fairchild	
						SIL4014B	† Mitel	10
						SIL4014BE	Mitel	
						SIL4021B	† Mitel	
						SIL4021BE	Mitel	
						MC14014BA	† Motorola	
						MC14021BA	† Motorola	
						CD4014AM	† National	
						CD4021AM	† National	
						CD4014B	† RCA	
						CD4021B	† RCA	
						SCL4014B	† SSS	20
						SCL4021B	† SSS	
						CM4014A	† Solitron	
						CM4021A	† Solitron	
				5 M	3-15	MM54C165	† National	
						MM74C165	National	
		SP	CMOS	5.5 M	3-15	MM54C164	† National	
						MM74C164	National	
		SS	CMOS	2.5 M	3-15	MC14094BA	† Motorola	
						MC14094BC	Motorola	
						µPD4094B	NEC America	30
						CD4094B	† RCA	
						CD4094BE	RCA	
						SCL4094B	† SSS	
						SCL4094BE	SSS	
	2	SS	Bipolar	10 M	5	93L28C	AMD	
						93L28M	† AMD	
						93L28C	Fairchild	
						93L28M	† Fairchild	
						MC8328	Motorola	
						MC9328	† Motorola	40
				15 M	5	RC8277	Raytheon	
						RM8277	† Raytheon	
						N8277	Signetics	
				20 M	5	9328C	AMD	
						9328M	† AMD	
						9328C	Fairchild	
						9328M	† Fairchild	
10	1	PP	Bipolar	25 M	5	RC8274	Raytheon	
						RM8274	† Raytheon	
						N8274	Signetics	50
						S8274	† Signetics	
		SP	Bipolar	25 M	5	RC8273	Raytheon	
						RM8273	† Raytheon	
						N8273	Signetics	
						S8273	† Signetics	
16	2	SS	CMOS	2 M	5-10	HSSR0321	† Hughes	
						HSSR0351	† Hughes	
			PMOS	2 M	-12,5	SS5-8211	GI	
						SS5-8212	GI	
						SS6-8211	† GI	60
						SS6-8212	† GI	
	4	SS	PMOS	2 M	-12,5	SL5-4016	GI	
24	4	SS	CMOS	2.5 M	5-16	MS618	† RTC	
25	4	SS	PMOS	1 M	-12,5	SL5-4025	GI	
						SL6-4025	† GI	
30	1	SS	CMOS	1M	3-15	MD4330B	Mitel	
						MD4330BE	Mitel	
32	1	SS	PMOS	1 M	-12,5	SS5-1032	GI	
						SS6-1032	† GI	
	2	SS	PMOS	1.5 M	-28	EA1003	EA	70
						EA1007	EA	
	4	SS	PMOS	1 M	-12,5	SL5-4032	GI	
						SL6-4032	† GI	
	6	SS	PMOS	1 M	-12,5	3348	Fairchild	
						3349	Fairchild	
				2 M	-12,5	TMS3112	TI	
33	1	SP	PMOS	0.25 M	–10,–20	MM5559	National	
50	2	SS	PMOS	1 M	-12,5	SL5-2050	GI	
						SL6-2050	† GI	
				1.5 M	-14,12	EA1013	EA	80
				3 M	-14,12	EA1012	EA	
64	1	SS	CMOS	1 M	3-15	F4031BC	Fairchild	
						CD4031BE	RCA	
				2 M	3-15	F4031BM	† Fairchild	
						CD4031B	† RCA	
				2.7 M	3-15	F4557BM	† Fairchild	
					3-16	MC1455BC	Motorola	
				4 M	3-15	CD4031BC	National	
						CD4031BM	† National	
				5 M	3-15	F4557BC	Fairchild	90
					3-18	MC14557BA	† Motorola	
				10 M	5-16	MS612	RTC	
	2	SS	Bipolar	30 M	5	TDC1005J	TRW	
			CMOS	4 M	3-15	MC14517BC	Motorola	
						µPD4517B	NEC America	
						SCL4517	SSS	
				5 M	3-15	MC14517BA	† Motorola	
			PMOS	1 M	-12,5	SL5-2064	GI	
						SL6-2064	† GI	
	4	SS	CMOS	4 M	4.5-12.5	F4731BC	Fairchild	100
						F4731BM	† Fairchild	
			PMOS	1.5 M	-12,5	3342	Fairchild	
80	2	SS	PMOS	1.5 M	-14,12	EA1009	EA	
					-12,5	3341C	Fairchild	
						3341M	† Fairchild	
				1.6 M	-12,5	MM4052	National	
				2.2 M	-12,5	MM5052	National	
				3 M	-14,12	EA1008	EA	
	4	SS	NMOS	1 M	5	SR5015-80	SMC	
				3 M	5	M142	SGS	110
			PMOS	1.5 M	-12,5	3347	AMD	
						3347	Fairchild	
				2 M	-12,5	3357-2	Fairchild	
				2.5 M	-12,5	AM2847M	† AMD	
						TMS3120	TI	
				3 M	-12,5	AM2847C	AMD	

(Continued)

† Military Temperature Range (–55° to 125°C)

SS = Serial In, Serial Out

PP = Parallel In, Parallel Out

* Typical Values

Bold face indicates additional data is provided on the page noted.

MEMORY–Shift Registers (Cont'd)

Bits Per Register	No. of Reg.	Operation	Process	Frequency (Hz - Spec)	Supply Voltage	Device	Source	Line
Static							**(Cont'd.)**	
							(Cont'd.)	
80	4	SS	PMOS	4 M	-12,5	3357-1	Fairchild	
64,72,80	2	SS	PMOS	1.5 M	-12,5	MM5054	National	
81	4	SS	NMOS	1 M	5	SR5015-81	SMC	
						SR5018	SMC	
96	2	SS	PMOS	2.5 M	-12,5	TMS3126	TI	
	4	SS	PMOS	2.5 M	-12,5	AM2896M	† AMD	
				3 M	-12,5	AM2896C	AMD	
100	1	SS	PMOS	1.5 M	-14,12	EA1005	EA	10
				3 M	-14,12	EA1004	EA	
	2	SS	PMOS	1.6 M	-12,5	MM4053	National	
						MM5053	National	
				2 M	-12,5	SL5-C2100	GI	
				2.5 M	-12,5	TMS3127	TI	
	4	SS	PMOS	2.2 M	-12,5	MM5061	National	
20-100	2	SS	PMOS	2.5 M	-12,5	MM4007	National	
128	1	SS	CMOS	5 M	12	MS625	RTC	
	2	SS	PMOS	1 M	-12,5	MK1002	AMD	
						MK1002	Mostek	20
						SL5-2128	GI	
				1.5 M	-12,5	MM5060AA	National	
				2 M	-12,5	AM2809M	† AMD	
						AM2810C	AMD	
						AM2810M	† AMD	
						TMS3114	AMD	
						SL5-C2128	GI	
						TMS3114	TI	
				2.5 M	-12,5	AM2809C	AMD	
						AM2814C	AMD	30
						AM2814M	† AMD	
						TMS3128	TI	
	4	SS	PMOS	1 M	-12,5	MM4055	† National	
				1.5 M	-12,5	MM5055	National	
				2.5 M	-12,5	AM2855	AMD	
						AM4055	† AMD	
						AM5055	AMD	
16-128	1	SS	CMOS	1.5 M	3-15	MC14562BC	Motorola	
				3 M	3-15	MC14562BA	† Motorola	
132	2	SS	PMOS	1.5 M	-12,5	MM5060AB	National	40
				2.5 M	-12,5	TMS3129	TI	
133	2	SS	PMOS	1.5 M	-12,5	MM5060AC	National	
				2 M	-12,5	TMS3113	TI	
				2.5 M	-12,5	TMS3130	TI	
	4	SS	NMOS	1 M	5	SR5015-133	SMC	
						SR5017	SMC	
1-134	4	SS	NMOS	1 M	5	SR5015	SMC	
125-144	2	SS	PMOS	1.5 M	-12,5	MM5060	National	
144	2	SS	PMOS	1.5 M	-12,5	MM5060AD	National	50
				2.5 M	-12,5	TMS3132	TI	
256	1	SS	Bipolar	30M	5	TDC1006J	TRW	
	2	SS	PMOS	1 M	-12,5	MM4056	† National	
							(Continued)	

Bits Per Register	No. of Reg.	Operation	Process	Frequency (Hz - Spec)	Supply Voltage	Device	Source	Line
Static							**(Cont'd.)**	
							(Cont'd.)	
256	2	SS	PMOS	1.5 M	-12,5	MM5056	National	
				2.5 M	-12,5	AM2856	AMD	
						AM4056	† AMD	
						AM5056	AMD	
288	1	SS	CMOS	20 M	1.5-10	MD6703A	† Mitel	
						MD6703AE	Mitel	60
480	2	SS	NMOS	1.5 M	5	SY2535	Synertek	
				3 M	5	SY2535A	Synertek	
512	1	SS	PMOS	1.0 M	-12,5	MM4057	† National	
				1.5 M	-12,5	MM5057	National	
				2.5 M	-12,5	AM2857C	AMD	
						AM4057	† AMD	
						AM5057	AMD	
	2	SS	NMOS	1.5 M	5	SY2534	Synertek	
				3 M	5	SY2534A	Synertek	
1024	1	SS	NMOS	1.5 M	5	SY2533	Synertek	70
				2 M	5	SY2833	Synertek	
				3 M	5	SY2833A	Synertek	
				4 M	5	SY2833B	Synertek	
				5 M	5	SY2833C	Synertek	
			PMOS	1.5 M	-12,5	AM2533	AMD	
						MM5058	National	
				2 M	-12,5	AM2833C	AMD	
						AM2833M	† AMD	
92304	1	SS	Bubble	0.1 M	—	TIB0203	TI	
254688	1	SS	Bubble	0.1 M	—	TIB0303	TI	80
266500	1	SS	Bubble		—	RBM256	Rockwell	
290560	1	SS	Bubble		—	H4701B	Hitachi	

† Military Temperature Range (−55° to 125°C)

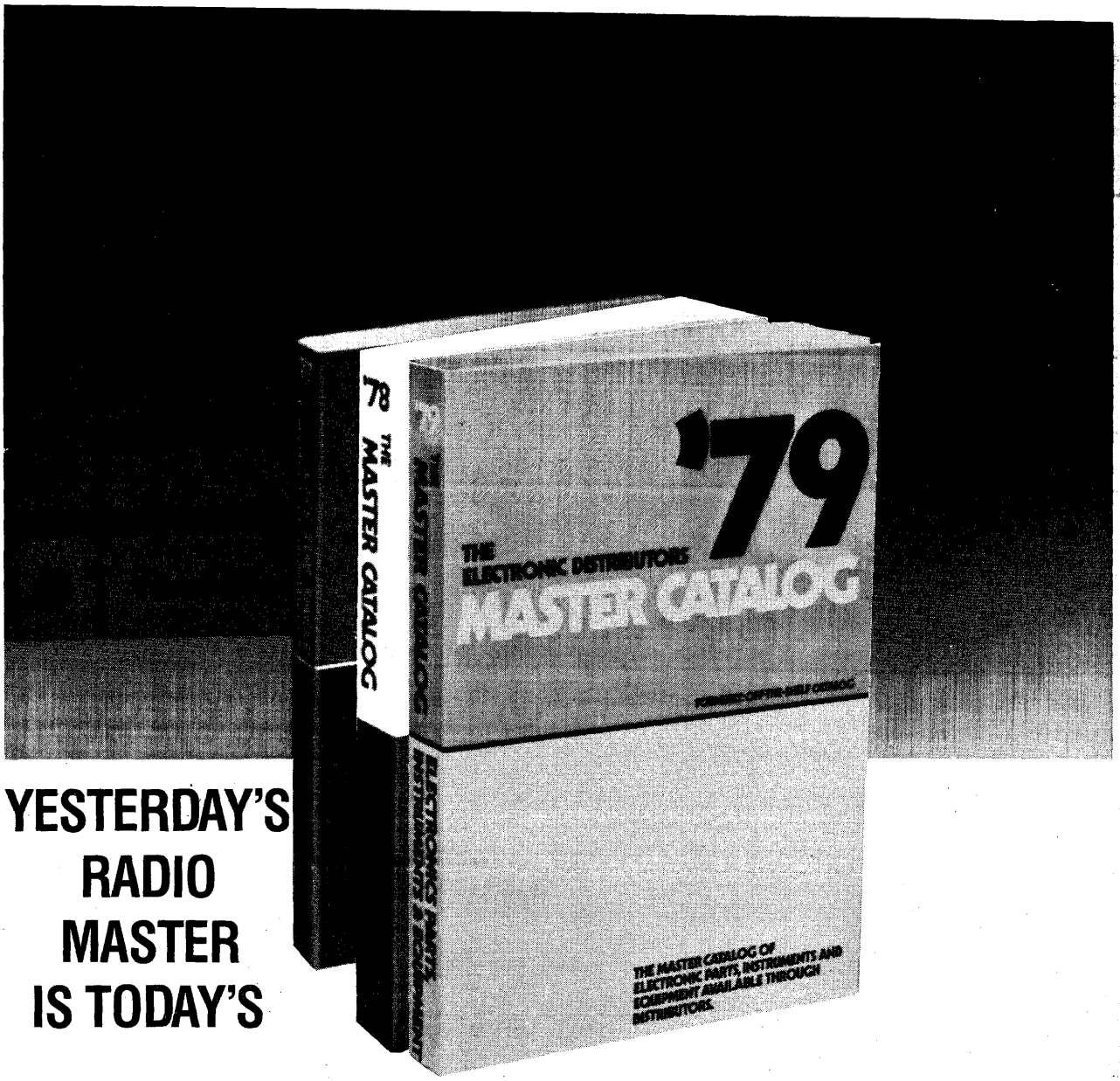
SS = Serial In, Serial Out

PP = Parallel In, Parallel Out

* Typical Values

ABBREVIATIONS OF COMPANY NAMES

AD	Analog Devices
AMD	Advanced Micro Devices
AMI	American Microsystems, Inc.
Amperex	Amperex Electronics Corp.
Analogic	Analogic Corp.
Beckman	Beckman Instruments, Helipot Division
BEI	BEI Electronics
Burr-Brown	Burr-Brown Research
Cermetek	Cermetek
Cherry	Cherry Semiconductor
CMA	Consumer Microcircuits of America
Cybernetic	Cybernetic Micro Systems
Data General	Data General
Datel	Datel Systems
DDC	Data Devices Corp.
Delco	Delco Electronics
Dionics	Dionics Inc.
EA	Electronic Arrays
EMM/Semi	EMM Semi, Div. of Electronic Memories & Magnetics
Essex	Essex International
Exar	Exar Integrated Systems
Fairchild	Fairchild
Ferranti	Ferranti Electric
Fujitsu	Fujitsu
GI	General Instrument
Harris	Harris Semiconductor
Hitachi	Hitachi America Ltd.
Holt	Holt Inc.
Hughes	Hughes Aircraft Solid State Products
Hybrid Sys	Hybrid Systems
HyComp	HyComp
IMI	International Microcircuits, Inc.
Intech/FMI	Intech/Function Modules Inc.
Intel	Intel
Interdesign	Interdesign
Intersil	Intersil
IPI	Integrated Photomatrix, Inc.
Lambda	Lambda Electronics
LSI	LSI Computer Systems
Maruman	Maruman Integrated Circuits
Master Logic	Master Logic
Matrox	Matrox Electronics Systems
Micro Net	Micro Networks
Micropac	Micropac Industries
Micro Power	Micro Power Systems
Micro Tech	Microcircuits Technology
Mitel	Mitel Semiconductor
Mitsubishi	Mitsubishi Electric Co.
MMI	Monolithic Memories, Inc.
Monosil	Monosil
MOS	MOS Technology
Mostek	Mostek
Motorola	Motorola Semiconductor
National	National Semiconductor
NCR	NCR Corp., Microelectronics Division
NEC America	NEC America
NEC Micro	NEC Microcomputers
Nitron	Nitron
Nortec	Nortec Electronics
Novonics	Novonics
NPC	Nucleonic Products Co.
OEI	Optical Electronics, Inc.
OKI	OKI Semiconductor
Panasonic	Panasonic, Matsushita Electric Corp.
Photo Therm	Photo Therm
Plessey	Plessey Semiconductors
PMI	Precision Monolithics, Inc.
Raytheon	Raytheon Semiconductor
RCA	RCA Solid State Division
Reticon	Reticon
RIFA	RIFA
Rockwell	Rockwell Microelectronic Devices
RTC	Real Time Corp.
Sanken	Sanken Electric
Sanyo	Sanyo Electric
SGS	SGS-Ates Semiconductor
Siemens	Siemens
Signetics	Signetics (Philips)
Silicon G	Silicon General
Siliconix	Siliconix
Silicon Sys.	Silicon Systems, Inc.
Silitronics	Silitronics
SMC	Standard Microsystems
Solitron	Solitron Devices
Sprague	Sprague Electric Company
Supertex	Supertex, Inc.
SSM	Solid State Microtechnology for Music
SSS	Solid State Scientific
Synertek	Synertek
Telaris	Telaris
Teledyne C	Teledyne Crystalonics
Teledyne P	Teledyne Philbrick
Teledyne S	Teledyne Semiconductor
Telefunken	AEG-Telefunken
TI	Texas Instruments
TMX	TMX
Toshiba	Toshiba
Trans-Data	Trans-Data
TRW	TRW
Unitrode	Unitrode
Western	Western Digital
Zilog	Zilog



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MOS STATIC RANDOM ACCESS MEMORIES

PART NO.	ORGANIZATION	PROCESS	MAX. ACCESS TIME (ns)	MAX. ACTIVE POWER (mW)	MAX. STANDBY POWER (mW)	POWER SUPPLIES	PACKAGE
S68B10	128 x 8	NMOS	250	420	N/A	+5V	24 PIN
S68A10	128 x 8	NMOS	360	420	N/A	+5V	24 PIN
S4015-2	1024 x 1	VMOS	60	660	N/A	+5V	16 PIN
S4025-2	1024 x 1	VMOS	60	660	N/A	+5V	16 PIN
S2114H[3]	1024 x 4	VMOS	70	790	N/A	+5V	18 PIN
S2114A-1	1024 x 4	VMOS	150	265	N/A	+5V	18 PIN
S2114L-1	1024 x 4	VMOS	150	370	N/A	+5V	18 PIN
S2114-1	1024 x 4	VMOS	150	525	N/A	+5V	18 PIN
S2114A-2	1024 x 4	VMOS	200	265	N/A	+5V	18 PIN
S2114L-2	1024 x 4	VMOS	200	370	N/A	+5V	18 PIN
S2114-2	1024 x 4	VMOS	200	525	N/A	+5V	18 PIN
S2114A-3	1024 x 4	VMOS	300	265	N/A	+5V	18 PIN
S2114L-3	1024 x 4	VMOS	300	370	N/A	+5V	18 PIN
S2114-3	1024 x 4	VMOS	300	525	N/A	+5V	18 PIN
S4017-3	4096 x 1	VMOS	55	660	N/A	+5V	18 PIN
S4017	4096 x 1	VMOS	70	660	N/A	+5V	18 PIN
S2147-3[3]	4096 x 1	VMOS	55	945	160	+5V	18 PIN
S2147[3]	4096 x 1	VMOS	70	840	105	+5V	18 PIN
S4028[3]	2048 x 8	VMOS	200	525	N/A	+5V	24 PIN

CMOS STATIC RANDOM ACCESS MEMORIES

PART NO.	ORGANIZATION	MAX. ACCESS TIME (ns)	MAX. ACTIVE POWER (mW)	MAX. STANDBY POWER (mW)	POWER SUPPLIES	PACKAGE
S2222[1]	512 x 1	350	25	.05	+10V	16 PIN
S2222A[1]	512 x 1	700	25	.25	+10V	16 PIN
S5101L-1	256 x 4	450	115	.055	+5V	22 PIN
S5101L	256 x 4	650	115	.055	+5V	22 PIN
S5101L-3	256 x 4	650	115	.735	+5V	22 PIN
S5101L-8	256 x 4	800	115	2.7	+5V	22 PIN
S5101-8	256 x 4	800	115	2.7	+5V	22 PIN
S6508-1	1024 x 1	300	13	.055	+5V	16 PIN
S6508	1024 x 1	460	13	.55	+5V	16 PIN
S6508A-1	1024 x 1	275/115[2]	12.5/50[2]	1.1	+4V to +11V	16 PIN
S6508A	1024 x 1	460/185[2]	12.5/50[2]	5.5	+4V to +11V	16 PIN
S6518-1	1024 x 1	300	13	.055	+5V	18 PIN
S6518	1024 x 1	460	13	.55	+5V	18 PIN
S6518A-1	1024 x 1	275/115[2]	12.5/50[2]	1.1	+4V to +11V	18 PIN
S6518A	1024 x 1	460/185[2]	12.5/50[2]	5.5	+4V to +11V	18 PIN

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MOS DYNAMIC RANDOM ACCESS MEMORIES

PART NO.	ORGANIZATION	PROCESS	MAX. ACCESS TIME (ns)	MAX. ACTIVE POWER (mW)	MAX. STANDBY POWER (mW)	POWER SUPPLIES	PACKAGE
S1103A[1]	1024 x 1	PMOS	205	425	2.0	+16/+19	18 PIN
S4006[1]	1024 x 1	PMOS	400	450	50	−12/+5	16 PIN
S4008-9[1]	1024 x 1	PMOS	800	450	50	−12/+5	16 PIN

UV ERASABLE ELECTRICALLY PROGRAMMABLE READ ONLY MEMORIES

PART NO.	ORGANIZATION	PROCESS	MAX. ACCESS TIME (ns)	MAX. ACTIVE POWER (mW)	MAX. STANDBY POWER (mW)	POWER SUPPLIES	PACKAGE
S6834	512 x 8	PMOS	575	750	N/A	+5/−12	24 PIN
S6834-1	512 x 8	PMOS	750	750	N/A	+5/−12	24 PIN
S5204A	512 x 8	PMOS	750	750	N/A	+5/−12	24 PIN
S4716[3]	2048 x 8	VMOS	250	525	132	+5	24 PIN
S4532[3]	4096 x 8	VMOS	250	525	132	+5	24 PIN

MOS READ ONLY MEMORIES

PART NO.	DESCRIPTION	ORGANIZATION	PROCESS	MAX. ACCESS TIME (ns)	MAX. ACTIVE POWER (mW)	POWER SUPPLIES	PACKAGE
S8773[1]	2560 Bit Static ROM	256 x 10 or 512 x 5	PMOS	600	600	+5/−12	24/28 PIN
S8564[1]	64 x 7 x 9 Charac. Gen.	64 Words	PMOS	450	1100	+5/−12	28 PIN
S3514[1]	4096 Bit Static ROM	512 x 8 or 1024 x 4	PMOS	1000	500	+5/−12	24 PIN
S5232[1]	4096 Bit Static ROM	512 x 8 or 1024 x 4	PMOS	1000	500	+5/−12	24 PIN
S8771[1]	5120 Bit Static ROM	512 x 10 or 1024 x 5	PMOS	450	1000	+5/−12	28 PIN
S6830[1]	8192 Bit Static ROM	1024 x 8	NMOS	575	680	+5	24 PIN
S8865[1]	8192 Bit Dynamic ROM	1024 x 8	PMOS	1700	635	+5/−12	24 PIN
S4216B	16,384 Bit Static ROM	2048 x 8	VMOS	250	500	+5	24 PIN
S6831[1]	16,384 Bit Static ROM	2048 x 8	NMOS	450	420	+5	24 PIN
S6831A	16,384 Bit Static ROM	2048 x 8	NMOS	450	420	+5	24 PIN
S6831B	16,384 Bit Static ROM	2048 x 8	NMOS	450	420	+5	24 PIN
S6831C[1]	16,384 Bit Static ROM	2048 x 8	NMOS	450	420	+5	24 PIN
S8996[1]	16,384 Bit Dynamic ROM	4096 x 4	PMOS	1800	370	+5/−12	24 PIN
S8996[1]	16,384 Bit Dynamic ROM	2048 x 8	PMOS	1800	370	+5/−12	24 PIN
S68332	32,768 Bit Static ROM	4096 x 8	NMOS	450	630	+5	24 PIN
S4264	65,536 Bit Static ROM	8192 x 8	VMOS	350	800	+5	24 PIN

[1] NOT RECOMMENDED FOR NEW DESIGNS
[2] FIRST NUMBER IS AT +5V. SECOND IS AT +10V
[3] TO BE ANNOUNCED

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4096 BIT (1024x4) STATIC VMOS RAM

Features

- ☐ High Speed Operation: Access Time: 150ns Maximum (-1)
- ☐ High Density 18 Pin Package
- ☐ Single +5 Volt Power Supply
- ☐ Completely Static Operation: No Clocks Required
- ☐ Completely TTL Compatible
- ☐ Common Data I/O: Three-State Outputs
- ☐ Fan-Out of 5 TTL: I_{OL} = 8mA @ 0.4V

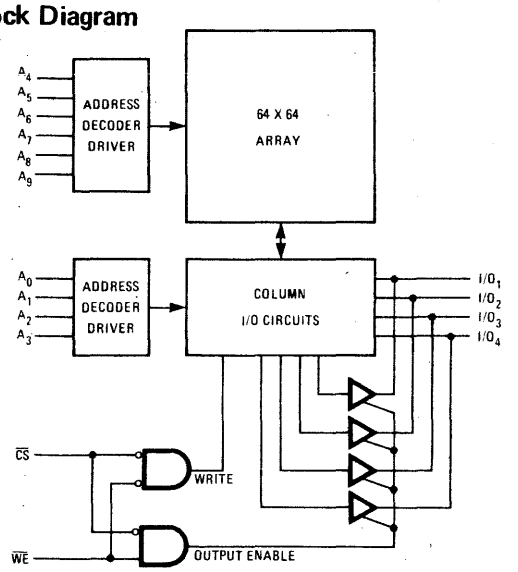
General Description

The AMI S2114 is a 4096 bit fully static RAM organized as 1024 words by 4 bits. The device is fully TTL compatible on all inputs and outputs and has a single +5V supply. The common data input/output pins facilitate interface with systems utilizing a bidirectional data bus. The stored data is read out non-destructively and is the same polarity as the original input data.

The S2114 is fully static requiring no clocks or refreshing for operation. This simplifies device operation as no address setup times are required. The chip select function facilitates memory system expansion by allowing the input/output pins to be OR-tied to other devices.

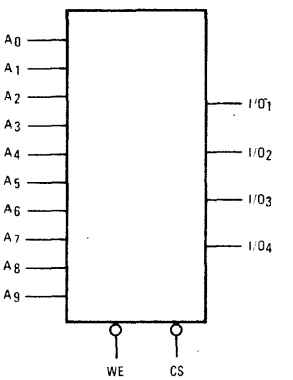
The S2114 is fabricated using AMI's proprietary VMOS technology. This process permits the manufacture of high performance memory devices suitable for high volume production.

Block Diagram



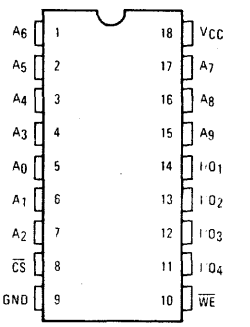
877308

Logic Symbol



877309

Pin Configuration



877310

Pin Names

A_0 - A_{11}	Address Inputs	$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select	V_{CC}	+5V Power
I/O_1 - I/O_4	Data Input/Output		

Truth Table

Inputs			Outputs	Mode
$\overline{CS}$	$\overline{WE}$	D_{IN}	D_{OUT}	
H	X	X	Hi - Z	Not Selected
L	L	L	Hi - Z	Write "0"
L	L	H	Hi - Z	Write "1"
L	H	X	D_{OUT}	Read

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Absolute Maximum Ratings*

Ambient Temperature Under Bias ..... -10°C to 80°C
Storage Temperature ..... -65°C to 150°C
Voltage on Any Pin With Respect to Ground ..... -0.5V to 7V
Power Dissipation 1W

*COMMENT: Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may effect device reliability.

D.C. Operating Conditions (V_{CC} = 5V ±5%; T_A = 0°C to 70°C)

Symbol	Parameter	S2114A-1 S2114A-2 S2114A-3		S2114L-1 S2114L-2 S2114L-3		S2114-1 S2114-2 S2114-3		Units	Conditions
		Min.	Max.	Min.	Max.	Min.	Max.		
I_{LI}	Input Leakage Current		10		10		10	μA	V_{IN} = 0V to 5.25V
$\|I_{LO}\|$	I/O Leakage Current		10		10		10	μA	CS = 2.4 V; $V_{I/O}$ = 0.4V to V_{CC}
I_{CC}	Power Supply Current		45		65		95	mA	V_{IN} = 5.25V; T_A = 25°C
			50		70		100	mA	V_{IN} = 5.25V; T_A = 0°C
V_{IL}	Input LOW Voltage	-0.5	0.8	-0.5	0.8	-0.5	0.8	V	
V_{IH}	Input HIGH Voltage	2.0	V_{CC}	2.0	V_{CC}	2.0	V_{CC}	V	
V_{OL}	Output LOW Voltage		0.4		0.4		0.4	V	I_{OL} = 8mA
V_{OH}	Output HIGH Voltage	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	I_{OH} = -1mA
I_{OS}	Output Short Circuit Current		100		100		100	mA	Duration not to exceed 30 sec.

Capacitance (T_A = 25°C; f = 1.0MHz)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
$C_{I/O}$	Input/Output Capacitance			10	pF	$V_{I/O}$ = 0V
C_{IN}	Input Capacitance			5	pF	V_{IN} = 0V

A.C. Characteristics (V_{CC} = 5V ±5%; T_A = 0°C to 70°C)
Read Cycle

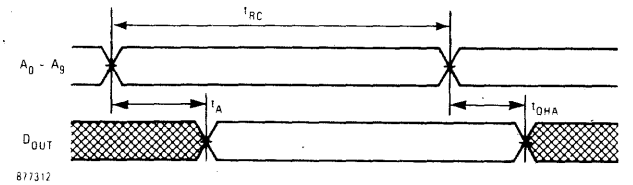
Symbol	Parameter	S2114A-1 S2114L-1 S2114-1		S2114A-2 S2114L-2 S2114-2		S2114A-3 S2114L-3 S2114-3		Units	Conditions
		Min.	Max.	Min.	Max.	Min.	Max.		
t_{RC}	Read Cycle Time	150		200		300		ns	See Test Circuit and Waveforms
t_A	Access Time		150		200		300	ns	
t_{CO}	Chip Selection to Output Valid		70		70		100	ns	
t_{CX}	Chip Selection to Output Active	15		15		15		ns	
t_{OTD}	Output 3-State from Deselection		40		60		80	ns	
t_{OHA}	Output Hold from Address Change	30		30		30		ns	

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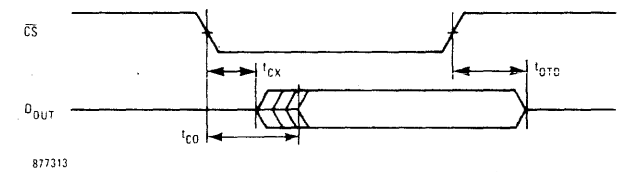
A.C. Characteristics (Continued)
Write Cycle

Symbol	Parameter	S2114A-1 S2114L-1 S2114-1		S2114A-2 S2114L-2 S2114-2		S2114A-3 S2114L-3 S2114-3		Units	Conditions
		Min.	Max.	Min.	Max.	Min.	Max.		
t_{WC}	Write Cycle Time	150		200		300		ns	See Test Circuit and Waveforms
t_W	Write Time	90		120		150		ns	
t_{WR}	Write Release Time	0		0		0		ns	
t_{OTW}	Output 3-State from Write		40		60		80	ns	
t_{DW}	Data to Write Time Overlap	90		120		150		ns	
t_{DH}	Data Hold from Write Time	0		0		0		ns	

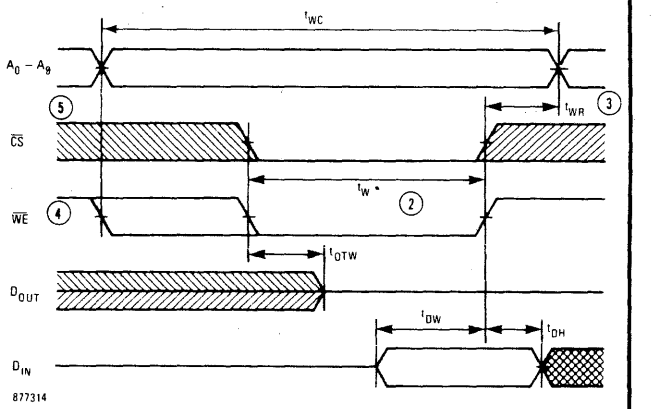
Read Cycle (note 1)
Propagation Delay From Address Inputs



Propagation Delay From Chip Select



Write Cycle (note 2)

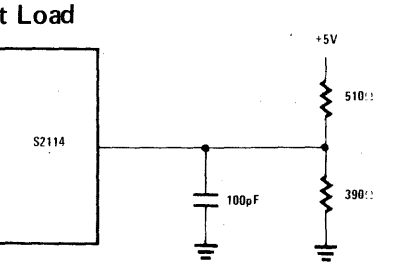


NOTES:
1. A read occurs during the overlap of a LOW $\overline{CS}$ and a HIGH $\overline{WE}$.
2. A write occurs during the overlap of a LOW $\overline{CS}$ and a LOW WE.
3. t_{WR} is referenced to the positive transition of $\overline{WE}$.
4. $\overline{WE}$ must be HIGH during all address transitions.
5. If the $\overline{CS}$ LOW transition occurs simultaneously with the $\overline{WE}$ LOW transition, then the output buffers remain in the high impedance state.

A.C. Test Conditions

Input Pulse Levels ..... 0.8V to 2.4V
Input Rise & Fall Times 10ns
Input and Output Timing Level 1.5V

A.C. Test Load



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4096 BIT (1024x4) HIGH SPEED STATIC VMOS RAM

Features

- ☐ High Speed Operation: Access Time: 70ns Maximum
- ☐ High Density 18 Pin Package
- ☐ Single +5 Volt Power Supply
- ☐ Completely Static Operation: No Clocks Required
- ☐ Completely TTL Compatible
- ☐ Common Data I/O: Three-State Outputs
- ☐ Fan-Out of 5 TTL: I_{OL}= 8mA @0.45V

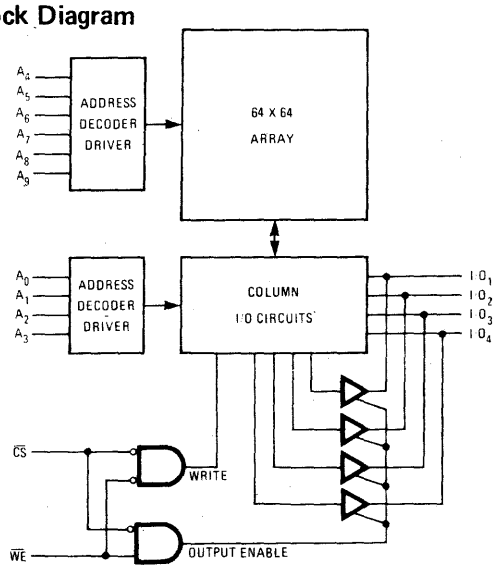
General Description

The AMI S2114H is a 4096 bit fully static RAM organized as 1024 words by 4 bits. The device is fully TTL compatible on all inputs and outputs and has a single +5V supply. The common data input/output pins facilitate interface with systems utilizing a bidirectional data bus. The stored data is read out non-destructively and is the same polarity as the original input data.

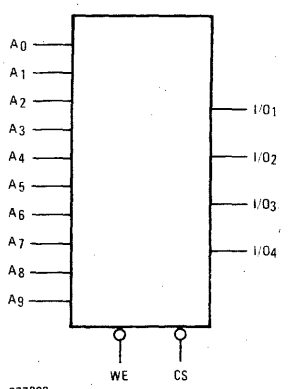
The S2114H is fully static requiring no clocks or refreshing for operation. This simplifies device operation as no address setup times are required. The chip select function facilitates memory system expansion by allowing the input/output pins to be OR-tied to other devices.

The S2114H is fabricated using AMI's proprietary VMOS technology. This process permits the manufacture of high performance memory devices suitable for high volume production.

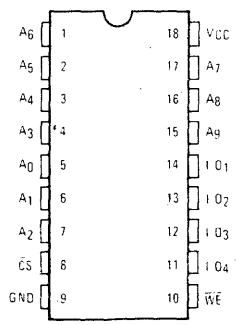
Block Diagram



Logic Symbol



Pin Configuration



Pin Names

A_0 - A_{11}	Address Inputs	$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select	V_{CC}	+5V Power
I/O_1 - I/O_4	Data Input/Output		

Truth Table

Inputs			Outputs	Mode
$\overline{CS}$	$\overline{WE}$	D_{IN}	D_{OUT}	
H	X	X	Hi - Z	Not Selected
L	L	L	Hi - Z	Write "0"
L	L	H	Hi - Z	Write "1"
L	H	X	D_{OUT}	Read

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4096 BIT (4096×1) HIGH SPEED STATIC VMOS RAM

Features

- ☐ High Speed Operation: Access Time: 55ns Max. (-3)
- ☐ Automatic Power-Down
- ☐ High Density 18 Pin Package
- ☐ Single +5V Power Supply
- ☐ Completely Static Operation
- ☐ Completely TTL Compatible Inputs
- ☐ Three-State TTL Compatible Output
- ☐ Fan-Out of 5 TTL: I_{OL} = 8mA @ 0.45V

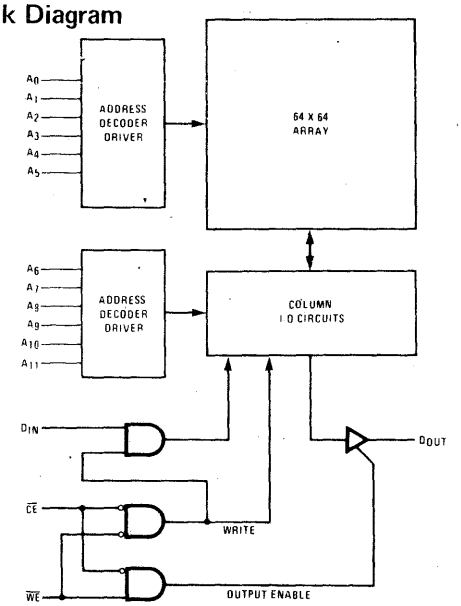
General Description

The AMI S2147 is a high speed 4096 bit fully static RAM organized as 4096 one-bit words. The device is fully TTL compatible and has a single +5V power supply. It has separate data input and output pins for maximum design flexibility. The three-state output facilitates memory expansion by allowing the output to be OR-tied to other devices. The stored data is read out non-destructively and is the same polarity as the input data.

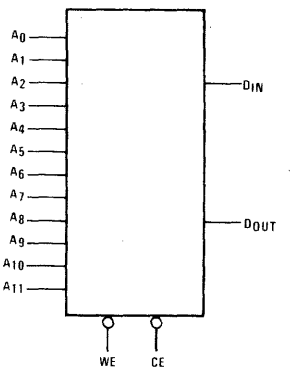
The automatic power down feature offers significant system power savings. This feature causes no performance degradation, as chip enable access and address access are equal. The S2147 is fully static eliminating the need for clocks or address set up and hold times as well as maximizing data rates since access times and cycle times are equal.

The S2147 is fabricated using AMI's proprietary VMOS technology. The process permits the manufacture of high performance memory devices suitable for high volume production.

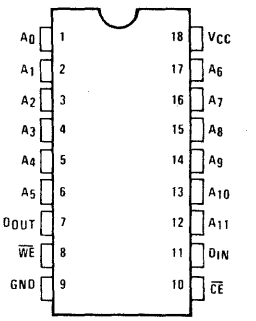
Block Diagram



Logic Symbol



Pin Configuration



Pin Names

A_0-A_{11}	Address Inputs	D_{IN}	Data Input
$\overline{CE}$	Chip Enable	D_{OUT}	Data Output
$\overline{WE}$	Write Enable	V_{CC}	+5V Power

Truth Table

Inputs			Output	Mode	Power
$\overline{CE}$	$\overline{WE}$	D_{IN}	D_{OUT}		
H	X	X	H-Z	Deselected	Standby
L	L	L	H-Z	Write "0"	Active
L	L	H	H-Z	Write "1"	Active
L	H	X	D_{OUT}	Read	Active

AMI

MEMORY

ADVANCED PRODUCT DESCRIPTION

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Absolute Maximum Ratings*

Ambient Temperature Under Bias	-10°C to 80°C
Storage Temperature	-65°C to 150°C
Voltage on Any Pin With Respect to Ground	-0.5V to 7V
Power Dissipation	1W

*COMMENT: Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may effect device reliability.

D.C. Characteristics: V_{CC} = 5V ± 5%, T_A = 0°C to 70°C

Symbol	Parameter		Min.	Typ.	Max.	Units	Conditions
V_{OL}	Output LOW Voltage				0.45	V	I_{OL} = 8mA
V_{OH}	Output HIGH Voltage		2.4			V	I_{OH} = -4.0mA
V_{IL}	Input LOW Voltage				0.8	V	
V_{IH}	Input HIGH Voltage		2.1			V	
I_{LI}	Input Leakage Current				10	μA	V_{CC} = Max., V_{IN} = 0 to V_{CC}
$\|I_{LO}\|$	Output Leakage Current				50	μA	$\overline{CS}$ = 2.1V, V_{CC} = Max. V_{OUT} = 0.4 to 4.5V
I_{OS}	Output Current Short Circuit to Ground				-100	mA	V_{CC} = Max., for not more than one second.
I_{CC}	Operating Current	S2147			160	mA	V_{CC} = Max., $\overline{CE}$ = V_{IL}, T_A = 0°C, Outputs Open
		S2147-3			180	mA	
I_{SB}	Standby Current	S2147			20	mA	V_{CC} = Max., $\overline{CE}$ = V_{IH}
		S2147-3			30	mA	

Capacitance: T_A = 25°C, f = 1.0MHz

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
C_{IN}	Input Capacitance			5	pF	V_{IN} = 0V
C_{OUT}	Output Capacitance			10	pF	V_{OUT} = 0V

A.C. Characteristics: T_A = 0°C to 75°C, V_{CC} = +5V ± 5%

Read Cycle

		S2147-3		S2147			
Symbol	Parameter	Min.	Max.	Min.	Max.	Units	Conditions
t_{RC}	Read Cycle Time	55		70		ns	See A.C. Test Conditions and Waveform
t_{AA}	Address Access Time		55		70	ns	
t_{AC}	Chip Enable Access Time		55		70	ns	
t_{OH}	Output Hold from Address Change	10		10		ns	
t_{LZ}	Chip Enable to Output LZ	10		10		ns	
t_{HZ}	Chip Enable to Output HZ		30		30	ns	
t_{PU}	Chip Enable to Power Up Time	0		0		ns	
t_{PD}	Chip Disable to Power Down Time		40		50	ns	

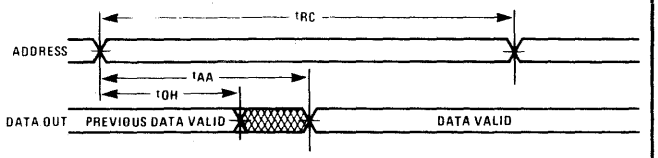
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Write Cycle

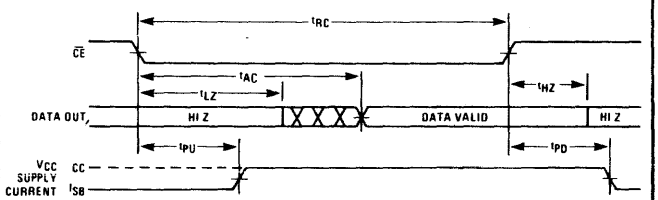
Symbol	Parameter	S2147-3 Min.	S2147-3 Max.	S2147 Min.	S2147 Max.	Units	Conditions
t_{WC}	Write Cycle Time	55		70		ns	
t_{CW}	Chip Enable to End of Write	45		55		ns	
t_{AW}	Address Valid to End of Write	45		55		ns	See A.C. Test Conditions and Waveforms
t_{AS}	Address Setup Time	5		5		ns	
t_{WP}	Write Pulse Width	35		40		ns	
t_{WR}	Write Recovery Time	10		15		ns	
t_{DW}	Data Valid to End of Write	25		30		ns	
t_{DH}	Data Hold Time	10		10		ns	
t_{WZ}	Write Enable to Output HZ	0	25	0	30	ns	
t_{OW}	Output Active from End of Write	0	25	0	30	ns	

READ CYCLE

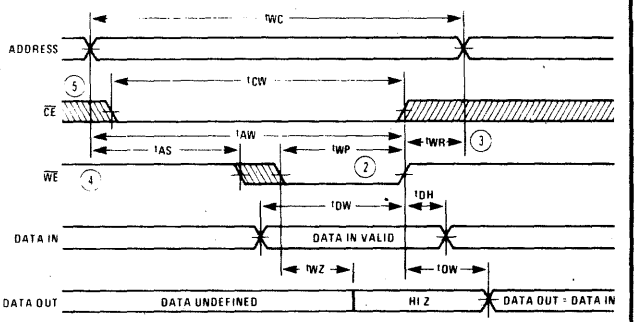
Propogation Delay From Address Inputs



Propagation Delay From Chip Enable

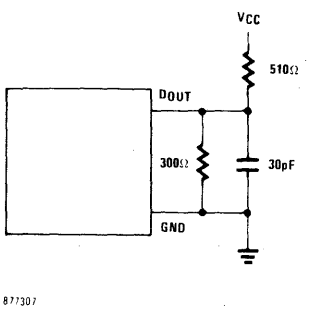


WRITE CYCLE

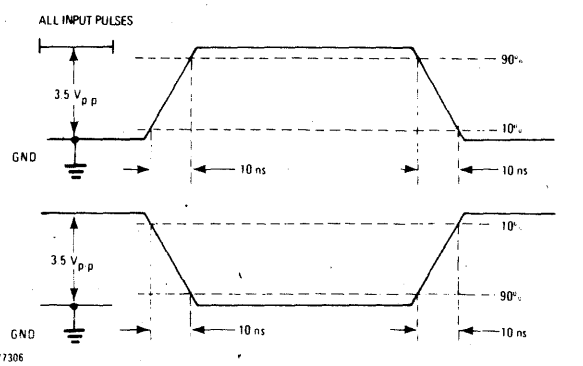


NOTES:
1. A read occurs during the overlap of a LOW $\overline{CE}$ and a HIGH $\overline{WE}$.
2. A write occurs during the overlap of a LOW $\overline{CE}$ and a LOW $\overline{WE}$.
3. t_{WR} is referenced to the positive transition of $\overline{WE}$.
4. $\overline{WE}$ must be HIGH during all address transitions.
5. If the $\overline{CE}$ LOW transition occurs simultaneously with the $\overline{WE}$ LOW transition, then output buffers remain in the high impedance state.

A.C. Test Load



A.C. Test Conditions



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1024 BIT (1024x1)
HIGH SPEED STATIC VMOS RAM

Features

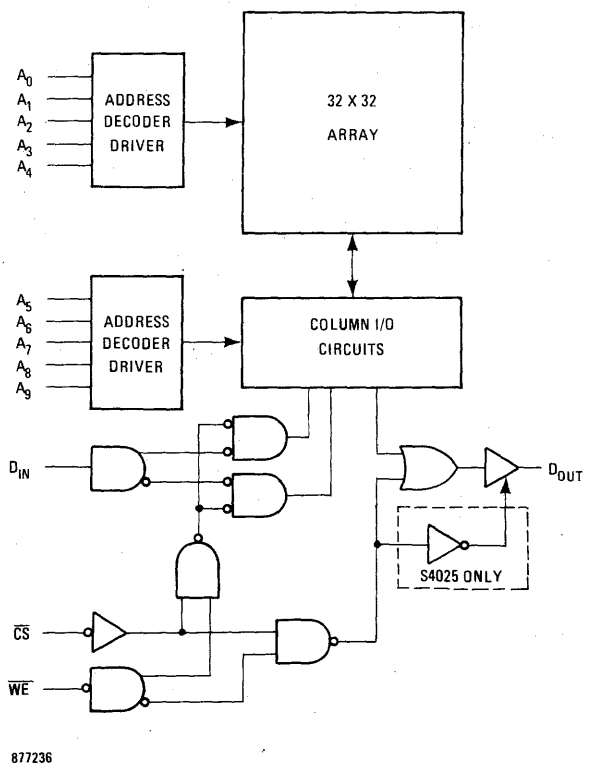
- ☐ **Pin Compatible with 93415 (S4015) and 93425 (S4025)**
- ☐ **Single +5V Power Supply**
- ☐ **Completely TTL Compatible**
- ☐ **Open Collector Output — S4015**
- ☐ **Three-State Output — S4025**
- ☐ **Fan-Out of 10 TTL — I_{OL} = 16mA @0.45V**
- ☐ **Completely Static — no Clocks or Refreshing**

General Description

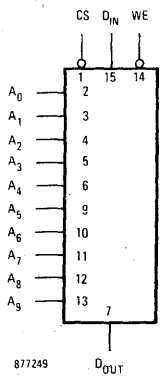
The AMI S4015/S4025 family of 1024x1 bit high speed VMOS RAMs offers fully static operation with a single 5V supply. The device is completely TTL compatible on inputs and output. The family is available in two output configurations. The S4015 has an open collector (open drain) output and the S4025 has a three-state output. The stored data is read out nondestructively and is the same polarity as the original input data.

The family is completely static requiring no clocks or refreshing for operation. Chip Select ($\overline{CS}$) controls the output and simplifies memory system expan-sion. The fast chip select time allows decoding the chip select from the address without increasing address access time.

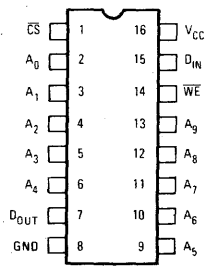
Block Diagram



Logic Symbol



Pin Configuration



Pin Names

$\overline{CS}$	Chip Select	D_{IN}	Data Input
$A_0 - A_9$	Address Inputs	D_{OUT}	Data Output
$\overline{WE}$	Write Enable		

Truth Table

Inputs			Output (D_{OUT})		Mode
$\overline{CS}$	$\overline{WE}$	D_{IN}	S4015	S4025	
H	X	X	H	H — Z	Not selected
L	L	L	H	H — Z	Write "0"
L	L	H	H	H — Z	Write "1"
L	H	X	D_{OUT}	D_{OUT}	Read

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4096 BIT (4096x1) HIGH SPEED STATIC VMOS RAM

Features

- ☐ High Speed Operation:
  - Address Access Time: 55ns Maximum
  - Chip Select Access Time: 30ns Maximum
- ☐ Fast Chip Select Optimizes Access Time
- ☐ High Density 18 Pin Package
- ☐ Single +5V Power Supply
- ☐ Completely Static Operation
- ☐ Completely TTL Compatible Inputs
- ☐ Three-State TTL Compatible Output
- ☐ Fan-Out of 5 TTL: I_{OL} = 8mA @ 0.45V

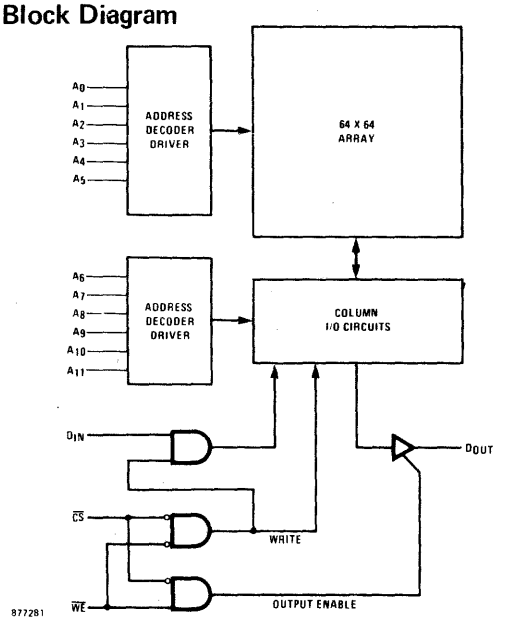
General Description

The AMI S4017 is a high speed 4096 bit fully static RAM organized as 4096 one-bit words. The device is fully TTL compatible and has a single + 5V power supply. It has separate data input and output pins for maximum design flexibility. The three-state output facilitates memory expansion by allowing the output to be OR-tied to other devices. The stored data is read out non-destructively and is the same polarity as the original input data.

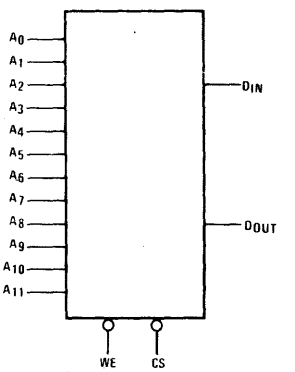
The fast chip select access time offers a significant performance advantage. As the chip select is normally decoded from the address, the time required to decode the chip select will not impact the overall access time.

The S4017 is fabricated using AMI's proprietary VMOS technology. The process permits the manufacture of high performance memory devices suitable for high volume production.

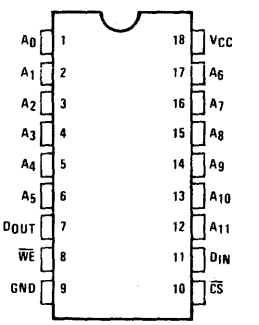
Block Diagram



Logic Symbol



Pin Configuration



Pin Names

A_0-A_{11}	Address Inputs	D_{IN}	Data Input
$\overline{CS}$	Chip Select	D_{OUT}	Data Output
$\overline{WE}$	Write Enable	V_{CC}	+5V Power

Truth Table

Inputs			Output	Mode
$\overline{CS}$	$\overline{WE}$	D_{IN}	D_{OUT}	
H	X	X	H-Z	Not Selected
L	L	L	H-Z	Write "0"
L	L	H	H-Z	Write "1"
L	H	X	D_{OUT}	Read

AMI

MEMORY

PRELIMINARY

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16,384 BIT (2048 X 8) STATIC VMOS RAM

Features

- ☐ **High Speed Operation: Access Time: 200ns Max.**
- ☐ **Single +5V Power Supply**
- ☐ **Pin Compatible with 16K EPROM/ROM**
- ☐ **Fully Static Operation**
- ☐ **Completely TTL Compatible**
- ☐ **Common Data Input/Output: Three-State Outputs**
- ☐ **Output Enable Function for Easy Control of Data Output**

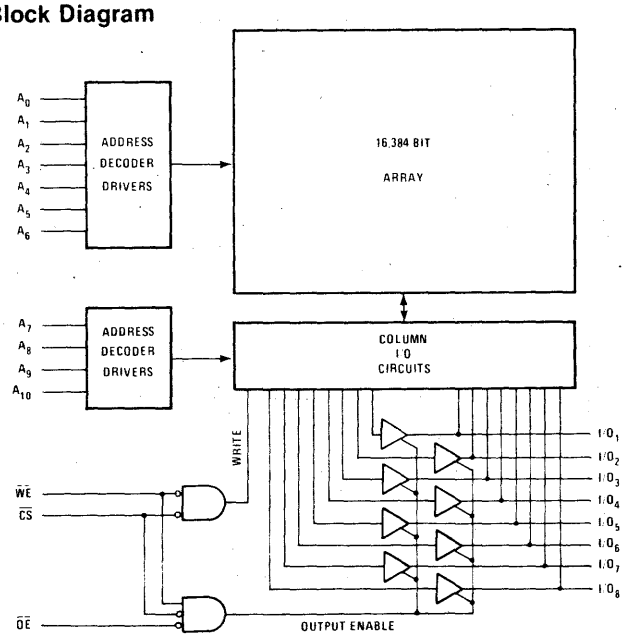
General Description

The AMI S4028 is a 16,384 bit fully static VMOS random access memory organized as 2048 words by 8 bits. The device is fully TTL compatible on all inputs and outputs and has a single +5V power supply. The common data input/output pins and output enable function facilitate interface with systems utilizing a bi-directional data bus. Data is read out non-destructively and is the same polarity as the input data.

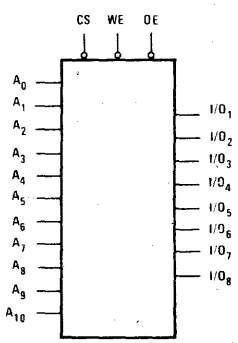
The S4028 is fully static requiring no clocks or refreshing for operation. This simplifies device operation as no address setup or hold times are required. The chip select and output enable functions facilitate memory expansion by allowing the input/output pins to be OR-tied to other devices.

The S4028 is fabricated using AMI's proprietary VMOS technology. This permits the manufacture of high performance memory devices suitable for high volume production.

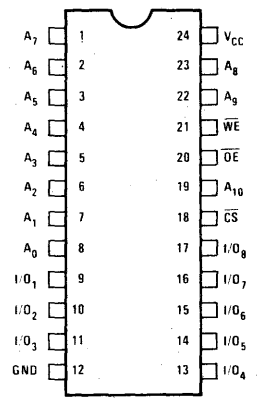
Block Diagram



Logic Symbol



Pin Configuration



Pin Names

$A_0 - A_{10}$	Address Inputs	$\overline{OE}$	Output Enable
$I/O_1 - I/O_8$	Data Inputs/Outputs	$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select	V_{CC}	+5V Power Supply

Truth Table

MODE	$\overline{CS}$	$\overline{OE}$	$\overline{WE}$	Data In	Data Out
Deselected	H	X	X	X	Hi-Z
Read	L	L	H	Hi-Z	Data Out
Write	L	H	L	Data In	Hi-Z
Write	L	L	L	Data In	Hi-Z
Selected, Output Hi-Z	L	H	H	X.	Hi-Z

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1024 BIT (256x4) STATIC CMOS RAM

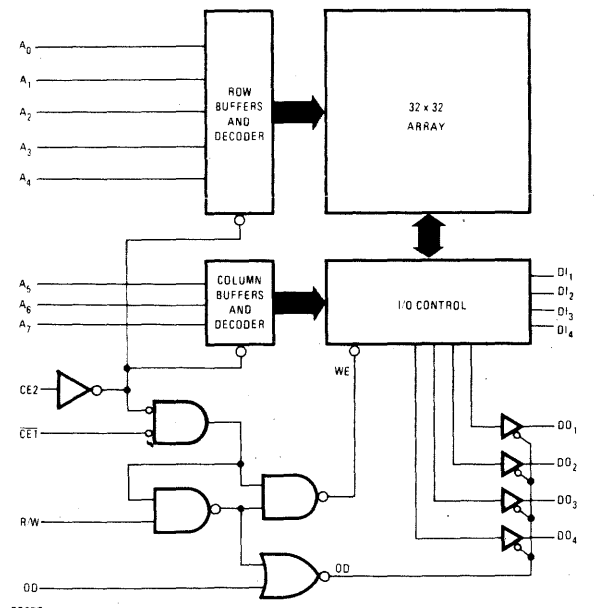
Features

- ☐ Ultra Low Standby Power
- ☐ Data Retention at 2V (L Version)
- ☐ Single +5 Volt Power Supply
- ☐ Completely Static Operation
- ☐ Completely TTL Compatible Inputs
- ☐ Three-State TTL Compatible Outputs

General Description

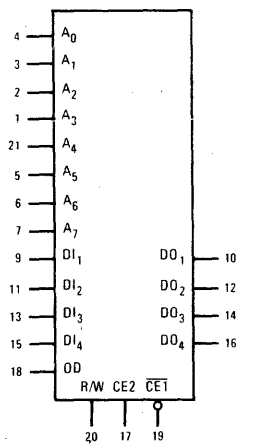
The AMI S5101 family of 256 x 4-bit ultra low power CMOS RAMs offers fully static operation with a single + 5 volt power supply. All inputs and outputs are directly TTL compatible. With data inputs and outputs on adjacent pins, either separate or common data I/O operations can easily be implemented for maximum design flexibility. The three-state outputs will drive one full TTL load and are disabled (high impedance state) by output disable (OD), either chip enable ($\overline{CE1}$ or CE2), or in a write cycle (R/W = LOW). This facilitates the control of common data I/O systems.

Block Diagram



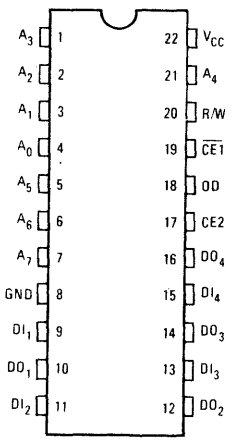
77678

Logic Symbol



877302

Pin Configuration



877301

Truth Table

$\overline{CE1}$	CE2	OD	R/W	DIN	Output	Mode
H	X	X	X	X	High Z	Not selected
X	L	X	X	X	High Z	Not Selected
X	X	H	H	X	High Z	Output Disabled
L	H	H	L	X	High Z	Write
L	H	L	L	X	High Z	Write
L	H	L	H	X	Dout	Read

Pin Names

A_0 - A_7	Address Inputs	$\overline{CE1}$	Chip Enable
DI_1 - DI_4	Data Inputs	CE2	Chip Enable
DO_1 - DO_4	Data Outputs	R/W	Read/Write Input
OD	Output Disable	V_{CC}	+5 Volt Power Supply

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1024 BIT (1024 x 1) STATIC CMOS RAM

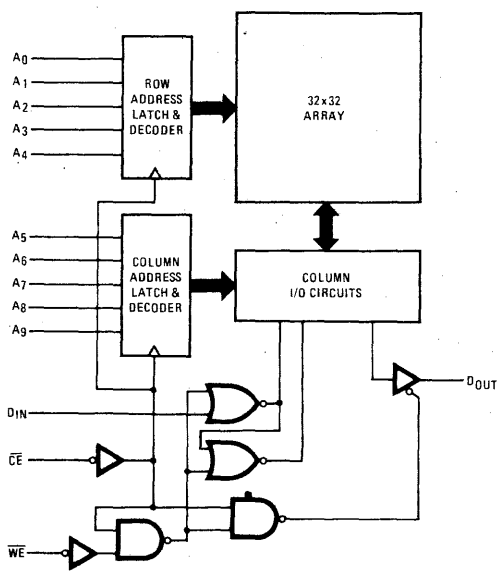
Features

- ☐ Ultra Low Standby Power
- ☐ S6508 Completely TTL Compatible
- ☐ S6508A Completely CMOS Compatible
- ☐ 4V to 11V Operation (S6508A)
- ☐ Data Retention at 2V
- ☐ Three-State Output
- ☐ Low Operating Power: 10mW @ 1MHz (5V)
- ☐ Fast Access Time: 115ns @ 10V

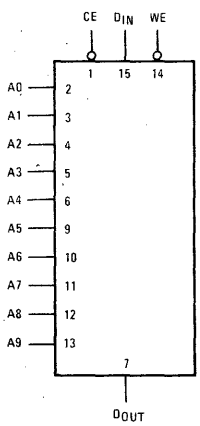
General Description

The AMI S6508 family of 1024x1 bit static CMOS RAMs offers ultra low power dissipation with a single power supply. The device is available in two versions. The basic part (S6508) operates on 5V and is directly TTL compatible on all inputs and the three-state output. The S6508 "A" operates from 4V to 11V and is fully CMOS compatible. The data is stored in ultra low power CMOS static RAM cells (six transistor). The stored data is read out nondestructively and is the same polarity as the original input data. The address is buffered by on-chip address registers. These internal registers are latched by the HIGH to LOW transition of chip enable ($\overline{CE}$). The write enable and chip enable functions are designed such that either separate or common data I/O operations can be easily implemented for maximum design flexibility.

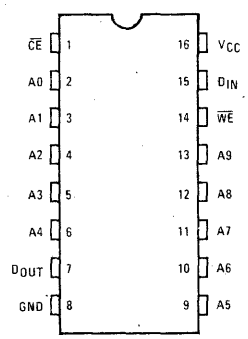
Block Diagram



Logic Symbol



Pin Configuration



Pin Names

A0-A9	Address Inputs	$\overline{CE}$	Chip Enable
D_{IN}	Data Input	$\overline{WE}$	Write Enable
D_{OUT}	Data Output	V_{CC}	Power Supply

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1024 BIT (1024x1) STATIC CMOS RAM

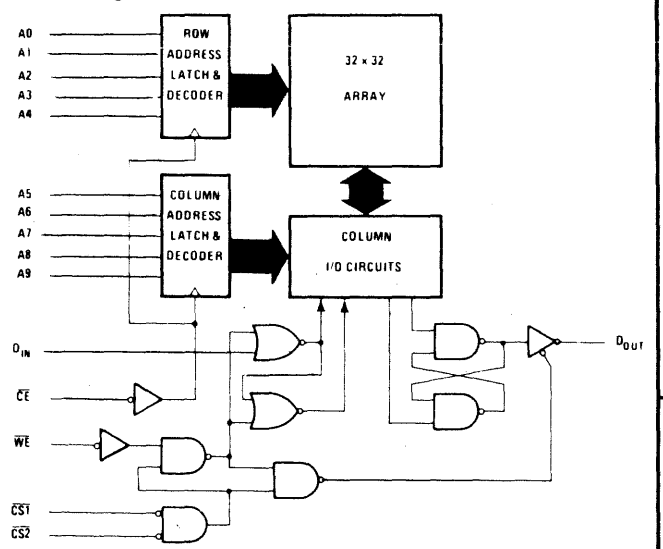
Features

- ☐ Ultra Low Standby Power
- ☐ S6518 Completely TTL Compatible
- ☐ S6518A Completely CMOS Compatible
- ☐ 4V to 11V Operation (S6518A)
- ☐ Data Retention at 2V
- ☐ Three-State Output
- ☐ Low Operating Power: 10mW @1MHz (5V)
- ☐ Fast Access Time: 115ns @10V

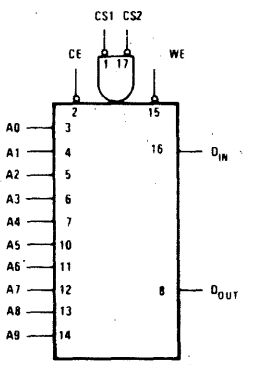
General Description

The AMI S6518 family of 1024x1 bit static CMOS RAMs offers ultra low power dissipation with a single power supply. The device is available in two versions. The basic part (S6518) operates on +5V and is directly TTL compatible on all inputs and the three-state output. The S6518 "A" operates from +4V to +11V and is fully CMOS compatible. The data is stored in ultra low power CMOS six transistor static RAM cells. The data is read out non-destructively (into a data latch) and is the same polarity as the original input data. The address is buffered by on-chip address registers. These internal registers are latched by the HIGH to LOW transition of chip enable ($\overline{CE}$). In addition, there are two chip selects ($\overline{CS1}$ and $\overline{CS2}$) which facilitate memory expansion. The write enable, chip enable and chip select functions are designed such that either separate or common data I/O operations can be easily implemented.

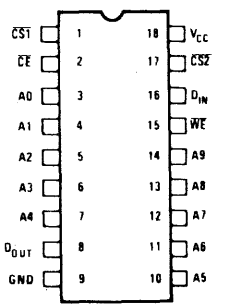
Block Diagram



Logic Symbol



Pin Configuration



Pin Names

$A_0 - A_9$	Address Inputs	$\overline{CS1}$, $\overline{CS2}$	Chip Selects
D_{IN}	Data Input	$\overline{WE}$	Write Enable
D_{OUT}	Data Output	V_{CC}	Power Supply
$\overline{CE}$	Chip Enable		

Truth Table

Inputs					Output	Mode
$\overline{CE}$	$\overline{CS1}$	$\overline{CS2}$	$\overline{WE}$	D_{IN}	D_{OUT}	
L	L	L	L	L	Hi-Z	Write "0"
L	L	L	L	H	Hi-Z	Write "1"
L	L	L	H	X	D_{OUT}	Read
X	H	X	X	X	Hi-Z	Deselected
X	X	H	X	X	Hi-Z	Deselected
H	X	X	L	X	Hi-Z	Deselected
H	L	L	H	X	D_{OUT}	Output Latched To Last Data

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16,384 BIT (2048 x 8) STATIC VMOS ROM

Features

- ☐ Fast Access Time: 250ns Maximum
- ☐ Fully Static Operation
- ☐ Single +5V ± 10% Power Supply
- ☐ Directly TTL Compatible Inputs
- ☐ Three-State TTL Compatible Outputs
- ☐ Three Programmable Chip Selects
- ☐ EPROM Pin Compatible
- ☐ Fan-Out of 5 TTL: I_{OL} = 8mA @ 0.4V

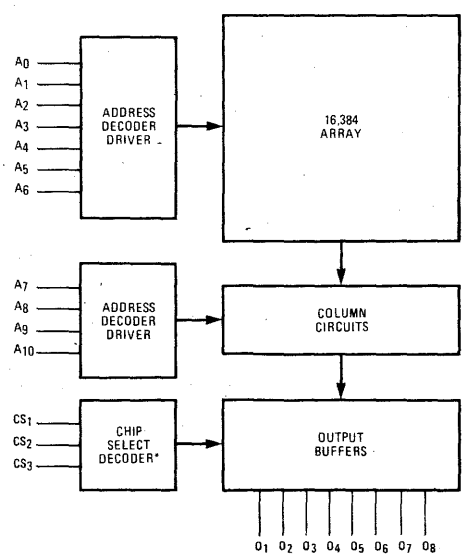
General Description

The AMI S4216B is a 16,384 bit static mask programmable VMOS ROM organized as 2048 words by 8 bits. The device is fully TTL compatible on all inputs and outputs and has single + 5V power suply. The three-state outputs facilitate memory expansion by allowing the outputs to be OR-tied to other devices.

The S4216B is fully compatible with 16K UV EPROMs (+ 5V version) making system development much easier and more cost effective. It is fully static, requiring no clocks for operation. The three chip selects are mask programmable, the active level for each being specified by the user.

The S4216B is fabricated using AMI's proprietary N-Channel VMOS technology. This permits the manufacture of very high density, high performance mask programmable ROMs.

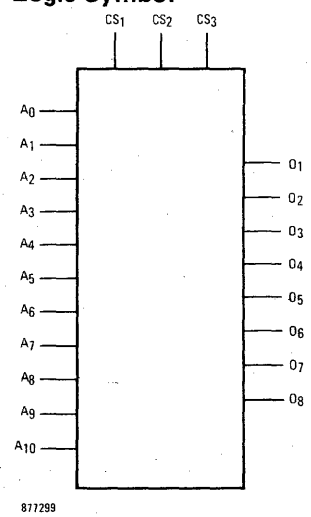
Block Diagram



*PROGRAMMABLE CHIP SELECTS

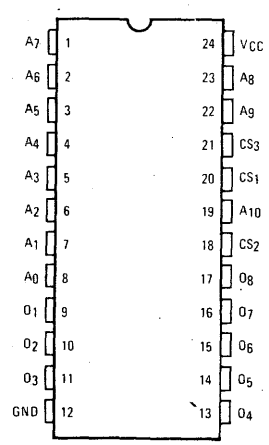
877273

Logic Symbol



877299

Pin Configuration



877300

Pin Names

A_0 - A_{10}	Address Inputs
O_1 - O_8	Data Outputs
CS_1 - CS_3	Chip Select Inputs
V_{CC}	+5V Power Supply

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Absolute Maximum Ratings*

Ambient Temperature Under Bias	-10°C to 80°C
Storage Temperature	-65°C to 150°C
Output or Supply Voltage	-0.5V to 7V
Input Voltage	-0.5V to 5.5V
Power Dissipation	1W

*Comment:

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. Characteristics: T_A = 0°C to 70°C, V_{CC} = 5V ± 10%

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
V_{OL}	Output LOW Voltage			0.4	V	I_{OL} = 8 mA
V_{OH}	Output HIGH Voltage	2.4			V	I_{OH} = -800μA
V_{IL}	Input LOW Voltage	-0.3		0.8	V	
V_{IH}	Input HIGH Voltage	2.2		V_{CC}	V	
I_{LI}	Input Leakage Current			10	μA	V_{IN} = 0 to 5.5V
I_{LO}	Output Leakage Current			10	μA	V_O = 0.4 to 5.5V, Chip Deselected
I_{CC}	Power Supply Current			90	mA	V_{CC} = Max., T_A = 0°C, Outputs Open

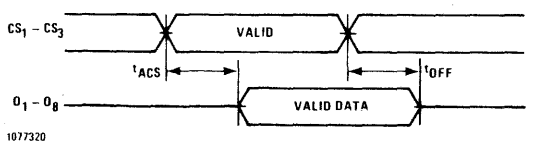
Capacitance: T_A = 25°C, f = 1Mhz

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
C_{IN}	Input Capacitance			8	pF	V_{IN} = 0V
C_{OUT}	Output Capacitance			10	pF	V_{OUT} = 0V

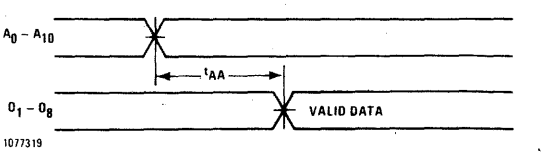
A.C. Characteristics: T_A = 0 to 70°C, V_{CC} = 5V ± 10%

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
t_{AA}	Address Access Time			250	ns	See A.C. Test
t_{ACS}	Chip Select Access Time			100	ns	Conditions
t_{OFF}	Chip Select Turn-off Time			100	ns	& Waveforms

Waveforms



Propagation From Chip Select



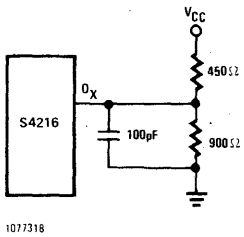
Propagation From Address

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A.C. Test Conditions

Input Pulse Levels	0.8V to 2.2V
Input Rise and Fall Times	10ns
Input/Output Timing Levels	1.5V

A.C. Test Load



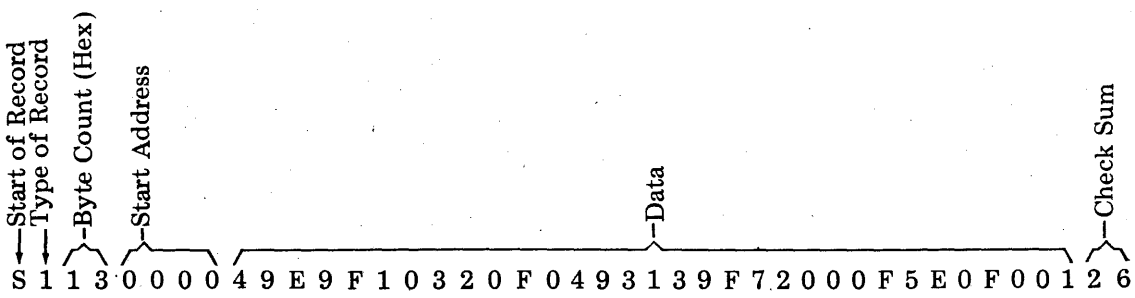
Custom Programming

The preferred method of pattern submission is the AMI Hex format as described below, with its built-in address space mapping and error checking. This is the format produced by the AMI Assembler. The format is as follows and may be on paper tape, punched cards or other media readable by AMI.

Position	Description
1	**Start of record (Letter S)**
2	**Type of record** 0 — Header record (comments) 1 — Data record 9 — End of file record
3, 4	**Byte Count** Since each data byte is represented as two hex characters, the byte count must be multiplied by two to get the number of characters to the end of the record. (This includes checksum and address data.) Records may be of any length defined in each record by the byte count.
5, 6, 7, 8	**Address Value** The memory location where the first data byte of this record is to be stored. Addresses should be in ascending order.
9, . . ., N	**Data** Each data byte is represented by two hex characters. Most significant character first.
N+1, N+2	**Checksum** The one's complement of the additive summation (without carry) of the data bytes, the address, and the byte count.

Example:

```
S 1 1 3 0 0 0 0 4 9 E 9 F 1 0 3 2 0 F 0 4 9 3 1 3 9 F 7 2 0 0 0 F 5 E 0 F 0 0 1 2 6
S 9 0 3 0 0 0 0 F C
```



NOTES:
1. Only positive logic formats for E_0, E_1, E_2 are accepted. 1 = V_{HIGH}; 0 = V_{LOW}
2. A "0" indicates the chip is enabled by a logic 0.
   A "1" indicates the chip is enabled by a logic 1.
3. Paper tape format is the same as the card format above except:
   a. The record should be a maximum of 80 characters.
   b. Carriage return and line feed after each record followed by another record.
   c. There should NOT be any extra line feed between records at all.
   d. After the last record, four (4) $$$$ (dollar) signs should be punched with carriage return and line feed indicating end of file.

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65,536 BIT (8192 x 8) STATIC VMOS ROM

Features

- ☐ Single +5V ± 10% Power Supply
- ☐ High Performance:
  Maximum Access Time: 350ns
- ☐ EPROM Compatible for Cost Effective System Development
- ☐ Completely Static Operation
- ☐ Directly TTL Compatible Inputs
- ☐ Three-State TTL Compatible Outputs
- ☐ Fan-out of 5 TTL: I_{OL} = 8mA @0.4V

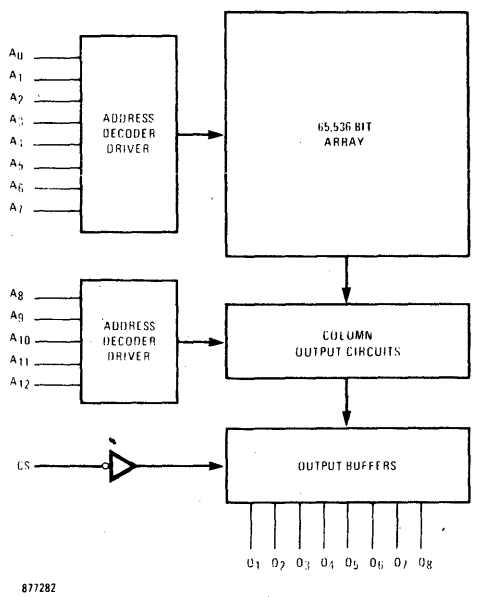
General Description

The AMI S4264 is a 65,536 bit fully static VMOS mask programmable ROM organized as 8192 words by 8 bits. The device is fully TTL compatible on all inputs and outputs and has a single +5V power supply. The three-state outputs facilitate memory expansion by allowing the outputs to be OR-tied to other devices.

The S4264 is fully static requiring no clocks for operation. Data access is simple as no address setup times are required. The byte organization of the S4264 makes it ideal for microprocessor applications.

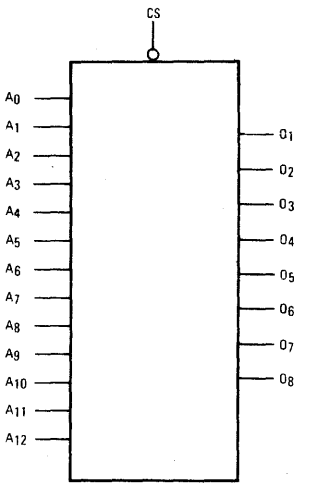
The S4264 is fabricated using AMI's proprietary VMOS technology. This permits the manufacture of very high density, high performance mask programmable ROMs.

Block Diagram



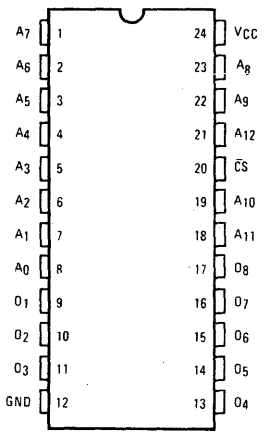
877282

Logic Symbol



877297

Pin Configuration



877298

Pin Names

A_0 - A_{12}	Address Inputs	$\overline{CS}$	Chip Select
O_1 - O_8	Data Outputs	V_{CC}	+5V Power

Truth Table

Input	Outputs	Mode
$\overline{CS}$	O_1-O_8	
L	D_{OUT}	Read
H	Hi-Z	Deselected

PRELIMINARY

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Absolute Maximum Ratings*

Ambient Temperature Under Bias	-10°C to 80°C
Storage Temperature	-65°C to 150°C
Output or Supply Voltages	-0.5V to 7V
Input Voltages	-0.5V to 5.5V
Power Dissipation	1W

*COMMENT: Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. Characteristics: T_A = 0°C to 70°C, V_{CC} = +5V ± 10%.

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
V_{OL}	Output LOW Voltage			0.4	V	I_{OL} = 8 mA
V_{OH}	Output HIGH Voltage	2.4			V	I_{OH} = -400μA
V_{IL}	Input LOW Voltage	-0.3		0.8	V	
V_{IH}	Input HIGH Voltage	2.2		V_{CC}	V	
I_{LI}	Input Leakage Current			10	μA	V_{IN} = 0 to 5.5V
I_{LO}	Output Leakage Current			50	μA	$\overline{CS} \geq$ 2.4V, V_O = 0.4V to 5.5V
I_{CC}	Power Supply Current			145	mA	V_{CC} = Max., T_A = 0°C, Outputs Open

Capacitance: T_A = 25°C, f = 1 MHz.

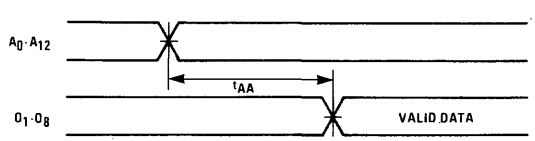
Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
C_{IN}	Input Capacitance			8	pF	V_{IN} = 0V
C_{OUT}	Output Capacitance			10	pF	V_{OUT} = 0V

A.C. Characteristics: T_A = 0°C to 70°C, V_{CC} = +5V ± 10%.

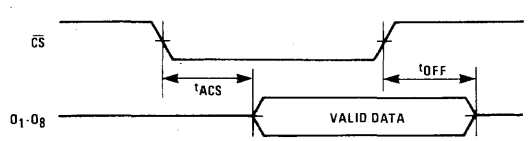
Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
t_{AA}	Address Access Time			350	ns	See Test Circuit & Waveforms
t_{ACS}	Chip Select Access Time			150	ns	
t_{OFF}	Chip Deselect Time	0		150	ns	

Wave Forms

Propagation Delay From Address



Propagation Delay From Chip Select

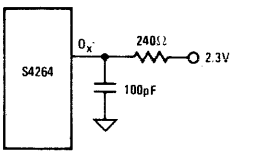


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A.C. Test Conditions

Input Pulse Levels	0.8V to 2.2V
Input Rise and Fall Times	10ns
Input/Output Timing Levels	1.5V

A.C. Test Load



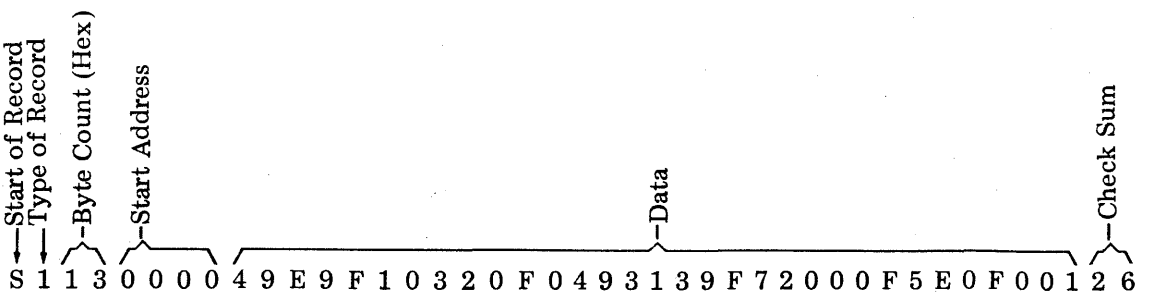
Custom Programming

The preferred method of pattern submission is the AMI Hex format as described below, with its built-in address space mapping and error checking. This is the format produced by the AMI Assembler. The format is as follows and may be on paper tape, punched cards or other media readable by AMI.

Position	Description
1	**Start of record (Letter S)**
2	**Type of record** 0 — Header record (comments) 1 — Data record 9 — End of file record
3, 4	**Byte Count** Since each data byte is represented as two hex characters, the byte count must be multiplied by two to get the number of characters to the end of the record. (This includes checksum and address data.) Records may be of any length defined in each record by the byte count.
5, 6, 7, 8	**Address Value** The memory location where the first data byte of this record is to be stored. Addresses should be in ascending order.
9, . . ., N	**Data** Each data byte is represented by two hex characters. Most significant character first.
N+1, N+2	**Checksum** The one's complement of the additive summation (without carry) of the data bytes, the address, and the byte count.

Example:

```
S 1 1 3 0 0 0 0 4 9 E 9 F 1 0 3 2 0 F 0 4 9 3 1 3 9 F 7 2 0 0 0 F 5 E 0 F 0 0 1 2 6
S 9 0 3 0 0 0 0 F C
```



NOTES:

1. Paper tape format is the same as the card format above except:
   a. The record should be a maximum of 80 characters.
   b. Carriage return and line feed after each record followed by another record.
   c. There should NOT be any extra line feed between records at all.
   d. After the last record, four (4) $$$$ (dollar) signs should be punched with carriage return and line feed indicating end of file.

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16,384 BIT (2048x8) STATIC NMOS ROM

Features

- ☐ Single +5V Power Supply
- ☐ Directly TTL Compatible Inputs
- ☐ Three-State TTL Compatible Outputs
- ☐ Three Programmable Enables
- ☐ Access Time: 450ns Maximum
- ☐ S6831A: Intel 2316A Pin Compatible
- ☐ S6831B: 2716 EPROM Pin Compatible
- ☐ Low Power: Supply Current is 80mA Maximum

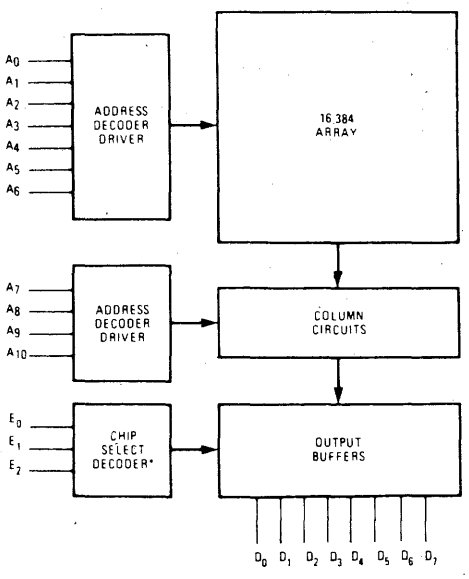
General Description

The AMI 6831 family of 16,384 bit mask programmable Read-Only-Memories offers fully static operation with a single + 5V power supply. The device is fully TTL compatible on all inputs and three-state outputs. The three enables are mask programmable, the active level is specified by the user.

The S6831 family is available in two pin configurations. One of these, the S6813A, is the pin configuration of a popular ROM: the Intel 2316A. The second pin configuration, the S6813B, is pin compatible with the 2708 and 2716 EPROMs. Software developed in EPROMs can be put in low cost ROM for high volume production.

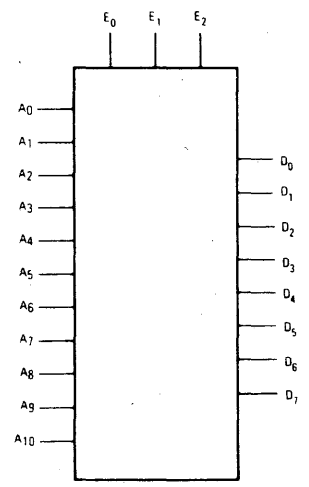
The device is organized as 2048 words by 8 bits, a configuration particularly suitable for microprocessors. The S6831 family is manufactured with an N-channel silicon gate depletion load technology.

Block Diagram



*PROGRAMMABLE CHIP SELECTS

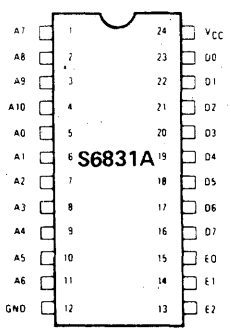
Logic Symbol



Pin Names

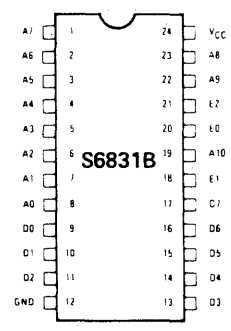
$A_0 - A_{10}$	Address Inputs
$D_0 - D_7$	Data Outputs
$E_0 - E_2$	Chip Select Inputs
V_{CC}	+5V Power Supply

Pin Configurations



Pin Compatible with:

AMD	AM9217
EA	EA2316A/8316A
GI	RO-3-8316
INTEL	2316A/8316A
MOSTEK	MK31000
NATIONAL	MM2316A
NEC	μPD2316A
SYNERTEK	SY2316A



Pin Compatible with:

AMD	AM9218
EA	EA2316E/8316E
FSC	68316E
GI	RO-3-9316
INTEL	2316E/8316E
MOTOROLA	MCM68316E
MOSTEK	MK-34000
NATIONAL	MM2316E
NEC	μPD2316E
SIGNETICS	2616
SYNERTEK	SY2316B

AMI MEMORY

32,768 BIT (4096x8) STATIC NMOS ROM

Features

- ☐ Fast Access Time: 450ns Maximum
- ☐ Fully Static Operation
- ☐ Single +5V ± 10% Power Supply
- ☐ Directly TTL Compatible Inputs
- ☐ Three-State TTL Compatible Outputs
- ☐ Two Programmable Chip Selects
- ☐ EPROM Pin Compatible

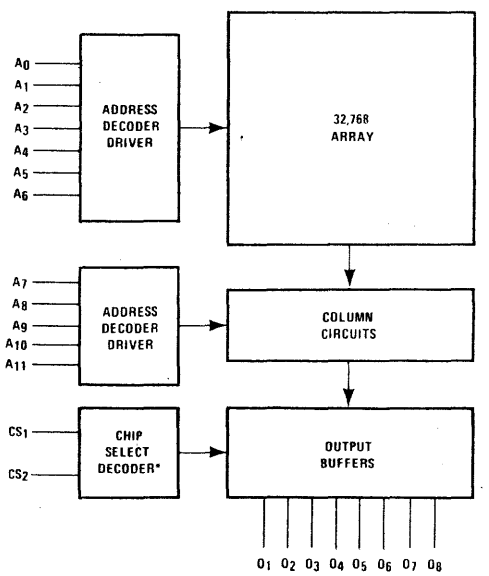
General Description

The AMI S68332 is a 32,768 bit static mask programmable NMOS ROM organized as 4096 words by 8 bits. The device is fully TTL compatible on all inputs and outputs and has a single +5V power supply. The three state outputs facilitate memory expansion by allowing the outputs to be OR-tied to other devices.

The S68332 is pin compatible with UV EPROMs making system development much easier and more cost effective. It is fully static, requiring no clocks for operation. The two chip selects are mask programmable, the active level for each being specified by the user.

The S68332 is fabricated using AMI's N-Channel MOS technology. This permits the manufacture of very high density, high performance mask programmable ROMs.

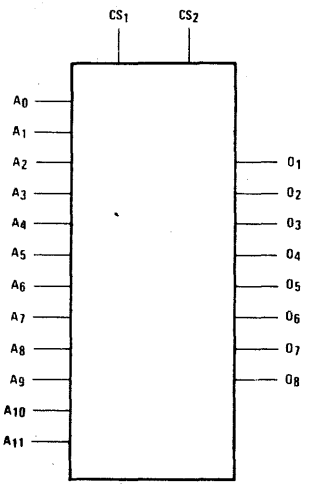
Block Diagram



*PROGRAMMABLE CHIP SELECTS

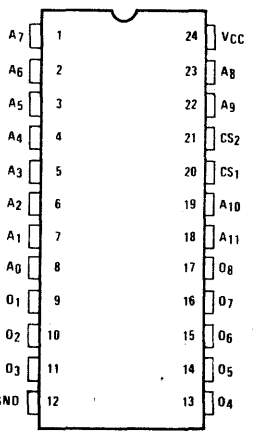
877273

Logic Symbol



877299

Pin Configuration



877300

Pin Names

A_0 - A_{11}	Address Inputs
O_1 - O_8	Data Outputs
CS_1 - CS_2	Chip Select Inputs
V_{CC}	+5V Power Supply

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Absolute Maximum Ratings*

Ambient Temperature Under Bias	-10°C to 80°C
Storage Temperature	-65°C to 150°C
Output or Supply Voltages	-0.5V to 7V
Input Voltages	-0.5V to 5.5V
Power Dissipation	1W

*COMMENT: Stresses above those listed under "Absolute Maximum Rating" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. Characteristics: T_A = 0°C to 70°C, V_{CC} = +5V ± 10%.

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
V_{OL}	Output LOW Voltage			0.4	V	I_{OL} = 2.1mA
V_{OH}	Output HIGH Voltage	2.4			V	I_{OH} = -200μA
V_{IL}	Input LOW Voltage	-0.5		0.8	V	
V_{IH}	Input HIGH Voltage	2.0		V_{CC}	V	
I_{LI}	Input Leakage Current			10	μA	V_{IN} = 0 to 5.5V
I_{LO}	Output Leakage Current			50	μA	V_O = 0.4V to 5.5V, Chip Deselected
I_{CC}	Power Supply Current			100	mA	V_{CC} = Max, T_A = 0°C

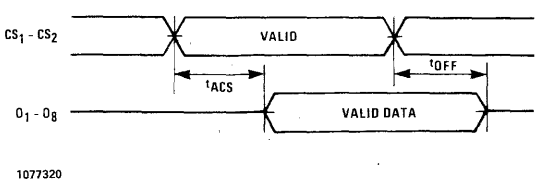
Capacitance: T_A = 25°C, f = 1 MHz.

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
C_{IN}	Input Capacitance			7	pF	V_{IN} = 0V
C_{OUT}	Output Capacitance			10	pF	V_{OUT} = 0V

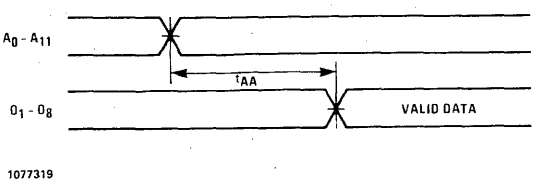
A.C. Characteristics: T_A = 0°C to 70°C, V_{CC} = +5V ± 10%.

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
t_{AA}	Address Access Time			450	ns	See Test Circuit
t_{ACS}	Chip Select Access Time			150	ns	&
t_{OFF}	Chip Deselect Time	0		150	ns	Waveforms

Waveforms



Propagation From Chip Select



Propagation From Address

A.C. Test Conditions

Input Pulse Levels	0.8V to 2.0V
Input Rise and Fall Times	10ns
Input/Output Timing Levels	1.5V
Output Load	1 TTL Load and 100pF

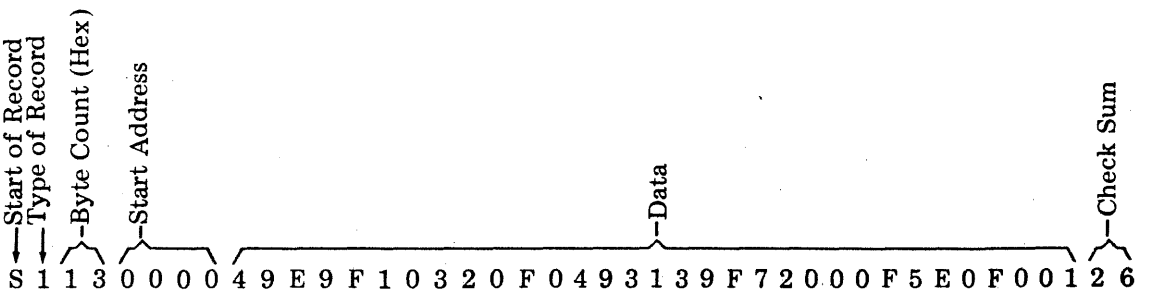
Custom Programming

The preferred method of pattern submission is the AMI Hex format as described below, with its built-in address space mapping and error checking. This is the format produced by the AMI Assembler. The format is as follows and may be on paper tape, punched cards or other media readable by AMI.

Position	Description
1	Start of record (Letter S)
2	Type of record 0 — Header record (comments) 1 — Data record 9 — End of file record
3, 4	Byte Count Since each data byte is represented as two hex characters, the byte count must be multiplied by two to get the number of characters to the end of the record. (This includes checksum and address data.) Records may be of any length defined in each record by the byte count.
5, 6, 7, 8	Address Value The memory location where the first data byte of this record is to be stored. Addresses should be in ascending order.
9, . . ., N	Data Each data byte is represented by two hex characters. Most significant character first.
N+1, N+2	Checksum The one's complement of the additive summation (without carry) of the data bytes, the address, and the byte count.

Example:

```
S 1 1 3 0 0 0 0 4 9 E 9 F 1 0 3 2 0 F 0 4 9 3 1 3 9 F 7 2 0 0 0 F 5 E 0 F 0 0 1 2 6
S 9 0 3 0 0 0 0 F C
```



NOTES:

1. Only positive logic formats for CS_1 and CS_2 are accepted. 1 = V_{HIGH}; 0 = V_{LOW}
2. A "0" indicates the chip is enabled by a logic 0.
   A "1" indicates the chip is enabled by a logic 1.
3. Paper tape format is the same as the card format above except:
   a. The record should be a maximum of 80 characters.
   b. Carriage return and line feed after each record followed by another record.
   c. There should NOT be any extra line feed between records at all.
   d. After the last record, four (4) $$$$ (dollar) signs should be punched with carriage return and line feed indicating end of file.

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32, 768 BIT (4096 X 8) UV ERASABLE VMOS EPROM

Features

- ☐ **Single +5 Volt Power Supply**
- ☐ **Fast Access Time: 250ns Maximum**
- ☐ **Automatic Power Down**
- ☐ **Pin Compatible with AMI's 32K ROM: S68332**
- ☐ **Fully TTL Compatible During Read and Program**
- ☐ **+15V Programming Power Supply: Easy On-Board Programming**

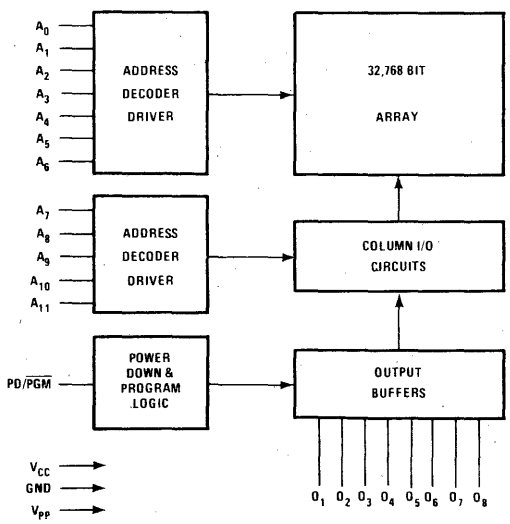
General Description

The S4532 is a 32,768 bit ultraviolet light erasable, electrically programmable read-only memory (EPROM) organized as 4096 words by 8 bits. It is fabricated using AMI's proprietary N-channel VMOS technology. The device is fully static requiring no clocks for operation. All the inputs and outputs are fully TTL compatible during both the read and program modes. The S4532 operates from a single +5V supply (read mode) and has a static power down feature that significantly reduces power dissipation.

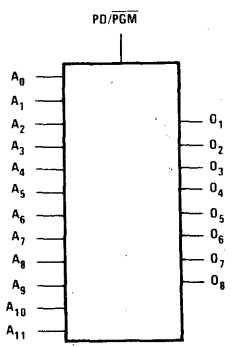
The S4532 is pin compatible with AMI's 32K ROM, the S68332. Thus for volume production, the user can switch to lower cost ROM.

The S4532 requires a +15V supply for programming but all the programming signals are TTL compatible. This considerably eases on-board programming.

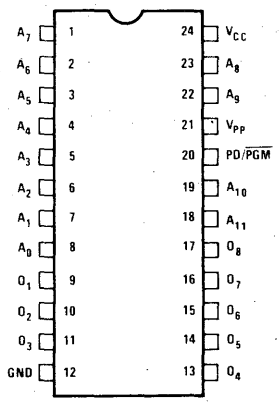
Block Diagram



Logic Symbol



Pin Configuration



Pin Names

$A_0 - A_{11}$	Address Inputs	VCC	+5V Power Supply
$O_1 - O_8$	Data Outputs	VPP	+15V Power Supply
PD/PGM	Power Down Program		

Truth Table

Mode	PD/PGM	Vcc	Vpp	Outputs
Read	V_{IL}	+5V	+ 5V	Data Out
Power Down	V_{IH}	+5V	+5V	High Z
Program	Pulsed V_{IH} to V_{IL} to V_{IH}	+5V	+15V	Data In
Program Inhibit	V_{IH}	+5V	+15V	High Z

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16,384 BIT (2048 X 8) UV ERASABLE VMOS EPROM

Features

- ☐ **Single +5 Volt Power Supply**
- ☐ **Fast Access Time: 250ns Maximum**
- ☐ **Pin Compatible with AMI's 16K, 32K and 64K ROMs**
- ☐ **Low Power Dissipation**
  525mA Maximum Active Power
  132mW Maximum Standby Power
- ☐ **Fully TTL Compatible During Read and Program**
- ☐ **+15V Programming Power Supply: Easy On-Board Programming**

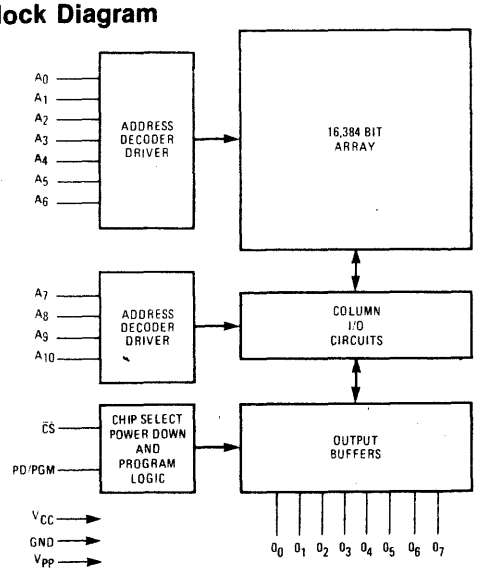
General Description

The S4716 is a 16,384 bit ultraviolet light erasable, electrically programmable read-only memory (EPROM) organized as 2048 words by 8 bits. It is fabricated using AMI's proprietary N-Channel VMOS technology. The device is fully static requiring no clocks for operation. All the inputs and outputs are fully TTL compatible during both the read and program modes. The S4716 operates from a single +5V power supply and has a static power down feature that significantly reduces power dissipation.

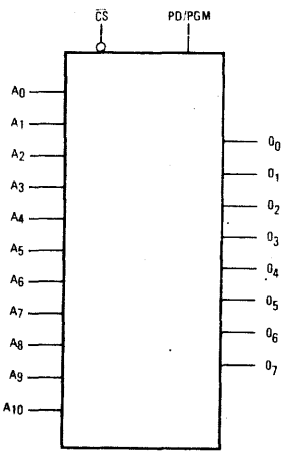
The S4716 is fully pin compatible with the S4216B and S6831B 16K ROMs, the S68332 32K ROM and the S4264 64K ROM. Thus for volume production, the user can switch to a lower cost ROM.

The S4716 requires a +15V supply for programming but all the programming signals are TTL. This considerably eases on-board programming.

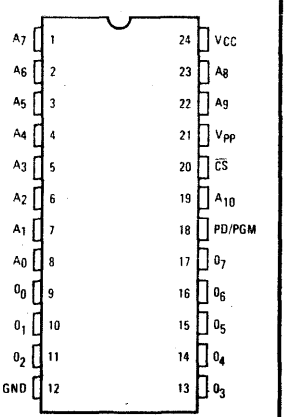
Block Diagram



Logic Symbol



Pin Configuration



Pin Names

$A_0 - A_{10}$	Addresses	PD/PGM	Power Down Program
$O_0 - O_7$	Data Outputs	$\overline{CS}$	Chip Select

Truth Table

MODE	PD/PGM	$\overline{CS}$	V_{CC}	V_{PP}	OUTPUTS
Read	V_{IL}	V_{IL}	+5V	+5V	Data Out
Deselect	Don't Care	V_{IH}	+5V	+5V	High Z
Power Down	V_{IH}	Don't Care	+5V	+5V	High Z
Program	Pulsed V_{IH} to V_{IH} to V_{IL}	V_{IH}	+5V	+15V	Data In
Program Verify	V_{IL}	V_{IL}	+5V	+15V	Data Out
Program Inhibit	V_{IL}	V_{IH}	+5V	+15V	High Z

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512 × 8 BIT ERASABLE AND ELECTRICALLY REPROGRAMMABLE READ ONLY MEMORY

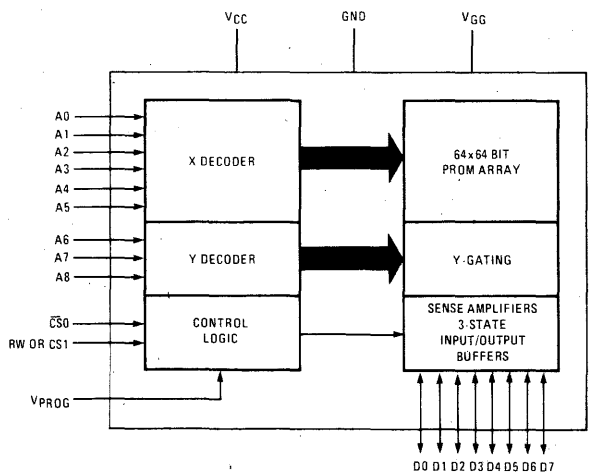
Features

- ☐ On-Board Programmability
- ☐ Fast Access Time — 750ns Max.
- ☐ High Speed Programming — Less than 1 Minute for all 4096 Bits
- ☐ Programmed with R/W, CS and V_{PROG} Pins
- ☐ Completely TTL Compatible — Excluding the V_{PROG} Pin during Read or Write
- ☐ Ultraviolet Light Erasable — Less than 10 Minutes
- ☐ Static Operation — No Clocks Required
- ☐ Three-State Data I/O
- ☐ Standard Power Supplies — +5V and - 12V
- ☐ Mature P-Channel Process

General Description

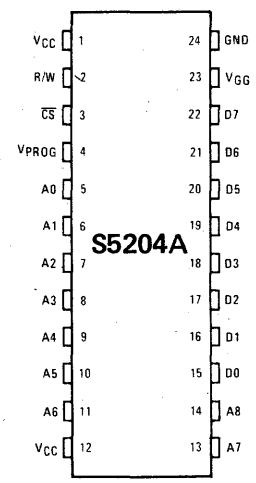
The S5204A is a high speed, static, 512x8 bit, erasable and electrically programmable read only memory designed for use in bus-organized systems. Both input and output are TTL compatible during both read and write modes. Packaged in a 24-pin hermetically sealed dual in-line package, the bit pattern can be erased by exposing the chip to an ultraviolet light source through the transparent lid, after which a new pattern can be written.

Block Diagram



77675

Pin Configuration



877254

Typical Applications

- ☐ ROM Program Debugging
- ☐ Code Translation
- ☐ Microprogramming
- ☐ Look-up Tables
- ☐ Random Logic Replacement
- ☐ Programmable Waveforms
- ☐ Character Generation
- ☐ Electronic Keyboards

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EMM 2114

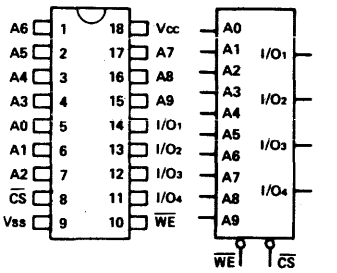
SEMI 2114 200NSEC, STATIC, TTL IN/OUT 1024x4 N-MOS RAM

FEATURES

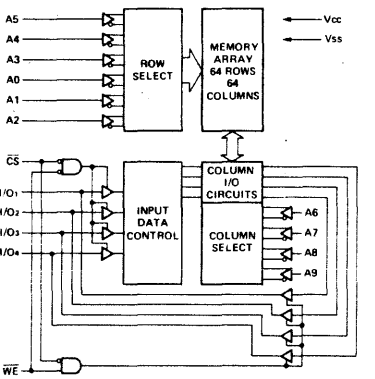
- 1024 words x 4 bits
- 200 or 300 nSec maximum access time
- Common output bus
- Three-state output drivers
- Fully STATIC — no clock or refresh
- Low power — 240 MW MAX
- Single +5V power supply
- TTL compatible interface
- 18-pin ceramic, plastic or cerdip package
- N-MOS, SILICON-GATE construction

PIN CONFIGURATION AND LOGIC SYMBOL

AN	Address Inputs
I/ON	Data Input/Output
$\overline{CS}$	Chip Select
$\overline{WE}$	Write Enable
Vss	Ground
Vcc	+5 V Power Supply



BLOCK DIAGRAM



TRUTH TABLE

$\overline{CS}$	$\overline{WE}$	DI/DO	STATUS	MODE
H	Don't Care	High Z	Deselect	Standby
L	H	Data	Selected	Read
L	L	L	Selected	Write 0
L	L	H	Selected	Write 1

ORDERING INFORMATION

DEVICE	ACCESS TIME	MAXIMUM POWER DISSIPATION	PACKAGE	TEMP. RANGE
2114-3CA	300ns	475mw	18-pin Ceramic	0° C to 70° C
2114-3CB	300ns	475mw	18-pin Plastic	0° C to 70° C
2114-3CE	300ns	475mw	18-pin Cerdip	0° C to 70° C
L2114-3CA	300ns	240mw	18-pin Ceramic	0° C to 70° C
L2114-3CB	300ns	240mw	18-pin Plastic	0° C to 70° C
L2114-3CE	300ns	240mw	18-pin Cerdip	0° C to 70° C
2114-2CA	200ns	475mw	18-pin Ceramic	0° C to 70° C
2114-2CB	200ns	475mw	18-pin Plastic	0° C to 70° C
2114-2CE	200ns	475mw	18-pin Cerdip	0° C to 70° C
L2114-2CA	200ns	240mw	18-pin Ceramic	0° C to 70° C
L2114-2CB	200ns	240mw	18-pin Plastic	0° C to 70° C
L2114-2CE	200ns	240mw	18-pin Cerdip	0° C to 70° C

RECOMMENDED OPERATING CONDITIONS (T_{AMB} = 0° C to 70° C)

PARAMETER	SYMBOL	MIN	NOM	MAX	UNITS
Supply Voltage	V_{CC}	4.75	5.0	5.25	V
Input High Level	V_{IH}	2.0	—	5.25	V
Input Low Level	V_{IL}	-0.5	—	0.8	V

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DC ELECTRICAL CHARACTERISTICS (Full Operating Voltage and Temperature Range)

CHARACTERISTIC	SYMBOL	MIN	TYP	MAX	UNIT	CONDITIONS
Input Leakage Current						
Input Low	I_{IL}	-10	—	+10	μA	V_{IN} = -0.5 to 0.8 V
Input Hi	I_{IH}	-10	—	+10	μA	V_{IN} = 2.0 to 5.25V
Output Leakage Current	I_{OL}	-10	—	+10	μA	$V_{I/O}$ = 0.4 to 5.25 V, CS = 2.4V
Output Voltage High	V_{OH}	2.4	—	—	V	I_O = -1.0 ma
Output Voltage Low	V_{OL}	—	—	0.4	V	I_O = 2.1 ma
Power Supply Current						
2114	I_{CC}	—	50	70	ma	T_{AMB} = 25°C
	I_{CC}	—	—	135	ma	T_{AMB} = 70°C
L2114	I_{CC}	—	35	65	ma	T_{AMB} = 25°C
	I_{CC}	—	—	70	ma	T_{AMB} = 70°C

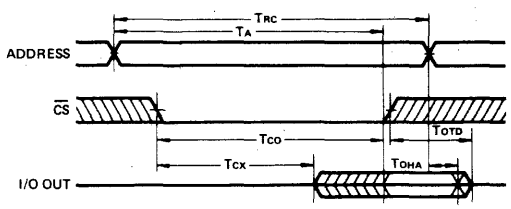
READ CYCLE — AC CHARACTERISTICS

		2114-2, L2114-2			2114-3, L2114-3				
PARAMETER	SYMBOL	MIN	TYP	MAX	MIN	TYP	MAX	UNITS	CONDITIONS
Read Cycle Time	T_{RC}	200	—	∞	300	—	∞	ns	Full Operating Voltage and Temperature Range
Access Time	T_A	—	—	200	—	—	300	ns	
Chip Select-to-Output, Valid	T_{CO}	—	—	70	—	—	100	ns	
Chip Select-to-Output, Active	T_{CX}	20	—	—	20	—	—	ns	
Output Hold After Address Change	T_{OHA}	50	—	—	50	—	—	ns	
Output Disable After Chip Deselection	T_{OTD}	—	—	60	—	—	80	ns	

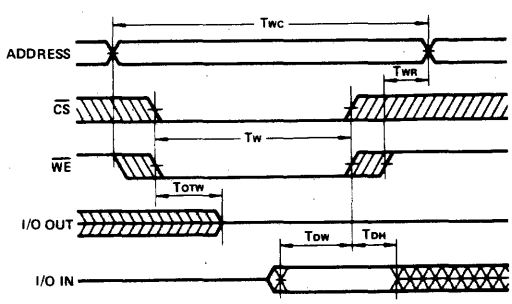
WRITE CYCLE — AC CHARACTERISTICS

		2114-2, L2114-2			2114-3, L2114-3				
PARAMETER	SYMBOL	MIN	TYP	MAX	MIN	TYP	MAX	UNIT	CONDITIONS
Write Cycle Time	T_{WC}	200	—	∞	300	—	∞	ns	Full Operating Voltage and Temperature Range
Write Pulse Width	T_W	120	—	—	150	—	—	ns	
Write Recovery Time	T_{WR}	0	—	—	0	—	—	ns	
Data Setup Time	T_{DW}	120	—	—	150	—	—	ns	
Data Hold Time	T_{DH}	0	—	—	0	—	—	ns	
Output Disable From Write or Chip Enable Time	T_{OTW}	—	—	60	—	—	80	ns	

READ CYCLE TIMING



WRITE CYCLE TIMING



NOTES:
1. WE is high for a Read Cycle.
2. Tw is measured from the latter of CS or WE going low to the earlier of CS or WE going high.
3. WE or CS must be high prior to a write cycle to prevent an erroneous write during the address transitions.

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EMM 2114

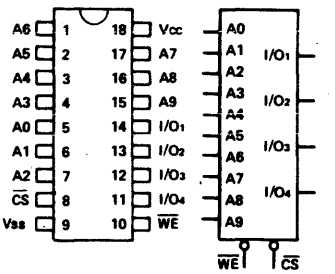
SEMI 2114 450NSEC, STATIC, TTL IN/OUT 1024x4 N-MOS RAM

FEATURES

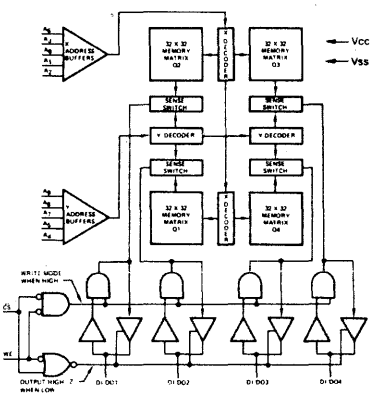
- 1024 words x 4 bits
- 450 nSec maximum access time
- Common output bus
- Three-state output drivers
- Fully STATIC — no clock or refresh
- Low power — 315 MW MAX
- Single +5V power supply
- TTL compatible interface
- 18-pin ceramic, plastic or cerdip package

PIN CONFIGURATION AND LOGIC SYMBOL

AN	Address Inputs
I/ON	Data Input/Output
$\overline{CS}$	Chip Select
$\overline{WE}$	Write Enable
Vss	Ground
Vcc	+5 V Power Supply



BLOCK DIAGRAM



TRUTH TABLE

$\overline{CS}$	$\overline{WE}$	DI/DO	STATUS	MODE
H	Don't Care	High Z	Deselect	Standby
L	H	Data	Selected	Read
L	L	L	Selected	Write 0
L	L	H	Selected	Write 1

ORDERING INFORMATION

DEVICE	ACCESS TIME	MAXIMUM POWER DISSIPATION	PACKAGE	TEMP. RANGE
2114-UCA	450ns	500mw	18-pin Ceramic	0° C to 70° C
2114-UCB	450ns	500mw	18-pin Plastic	0° C to 70° C
2114-UCE	450ns	500mw	18-pin Cerdip	0° C to 70° C
L2114-UCA	450ns	315mw	18-pin Ceramic	0° C to 70° C
L2114-UCB	450ns	315mw	18-pin Plastic	0° C to 70° C
L2114-UCE	450ns	315mw	18-pin Cerdip	0° C to 70° C

RECOMMENDED OPERATING CONDITIONS (T_{AMB} = 0°C to 70°C)

PARAMETER	SYMBOL	MIN	NOM	MAX	UNITS
Supply Voltage	V_{CC}	4.75	5.0	5.25	V
Input High Level	V_{IH}	2.4	—	5.25	V
Input Low Level	V_{IL}	-0.5	—	0.8	V

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DC ELECTRICAL CHARACTERISTICS (Full Operating Voltage and Temperature Range)

CHARACTERISTIC	SYMBOL	MIN	TYP	MAX	UNIT	CONDITIONS
Input Leakage Current						
Input Low	I_{IL}	-10	—	+10	μA	V_{IN} = -0.5 to 0.8 V
Input Hi	I_{IH}	-10	—	+10	μA	V_{IN} = 2.4 to 5.25V
Output Leakage Current	I_{OL}	-10	—	+10	μA	$V_{I/O}$ = 0.4 to 5.25V, $\overline{CS}$ = 2.4V
Output Voltage High	V_{OH}	2.4	—	—	V	I_O = -1.0 ma
Output Voltage Low	V_{OL}	—	—	0.4	V	I_O = 2.1 ma
Power Supply Current						
2114	I_{CC}	—	45	75	ma	T_{AMB} = 0° C
	I_{CC}	—	45	75	ma	T_{AMB} = 25° C
	I_{CC}	—	65	100	ma	T_{AMB} = 70° C
L2114	I_{CC}	—	30	40	ma	T_{AMB} = 0° C
	I_{CC}	—	35	45	ma	T_{AMB} = 25° C
	I_{CC}	—	40	60	ma	T_{AMB} = 70° C

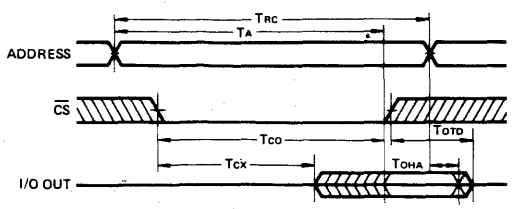
READ CYCLE — AC CHARACTERISTICS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	CONDITIONS
Read Cycle Time	T_{RC}	450	—	∞	ns	Full Operating Voltage and Temperature Range
Access Time	T_A	—	—	450	ns	
Chip Select-to-Output, Valid	T_{CO}	—	—	100	ns	
Chip Select-to-Output, Active	T_{Cx}	0	—	—	ns	
Output Hold After Address Change	T_{OHA}	50	—	—	ns	
Output Disable After Chip Deselection	T_{OTD}	25	—	100	ns	

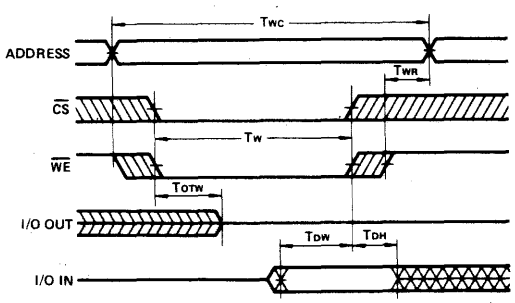
WRITE CYCLE — AC CHARACTERISTICS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT	CONDITIONS
Write Cycle Time	T_{WC}	450	—	∞	ns	Full Operating Voltage and Temperature Range
Write Pulse Width	T_W	200	—	—	ns	
Write Recovery Time	T_{WR}	0	—	—	ns	
Data Setup Time	T_{DW}	200	—	—	ns	
Data Hold Time	T_{DH}	0	—	—	ns	
Output Disable From Write or Chip Enable Time	T_{OTW}	—	—	100	ns	

READ CYCLE TIMING



WRITE CYCLE TIMING



NOTES:
1. $\overline{WE}$ is high for a Read Cycle.
2. Tw is measured from the latter of $\overline{CS}$ or $\overline{WE}$ going low to the earlier of $\overline{CS}$ or $\overline{WE}$ going high.
3. $\overline{WE}$ or $\overline{CS}$ must be high prior to a write cycle to prevent an erroneous write during the address transitions.

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EMM3539

SEMI 3539 400NSEC, STATIC, TTL IN/OUT 256x8 N-MOS RAM

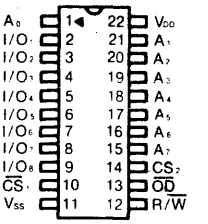
FEATURES

- 256 x 8 with Common I/O Bus
- Standard 22-Pin Dip
- Single +5V Power Supply
- Completely Static — No Clocks or Refresh
- Totally TTL Compatible
- 400 ns Maximum Access Time
- Less than 400 mW Power Dissipation
- Two Separate Chip Select Inputs
- Separate Output Disable Function

PIN CONFIGURATION

A_n	Address Inputs
$\overline{CS}_n$	Chip Select Inputs
$\overline{OD}$	Output Disable
$R/\overline{W}$	Read/Write Control Input
I/O_n	Data Bus Pins
V_{DD}	+5 V Power Supply
V_{SS}	0 V Power Supply

TOP VIEW

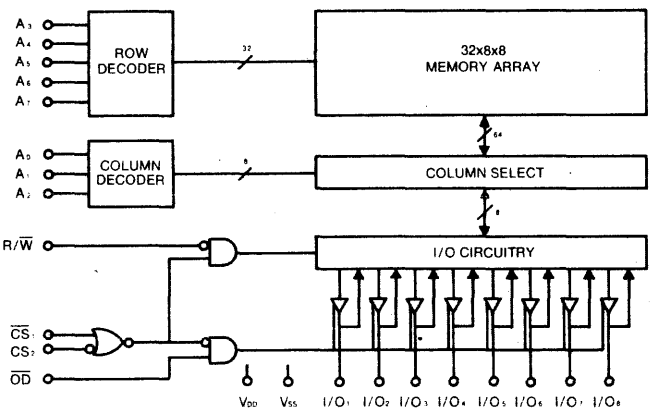


TRUTH TABLE

$\overline{CS_1}$	CS_2	$\overline{OD}$	$R/\overline{W}$	STATUS	I/O BUS MODE
H	X	X	X	DESELECTED	HI Z
X	L	X	X	DESELECTED	HI Z
L	H	L	L	WRITE MODE	OUTPUT DISENABLE DATA CAN BE WRITTEN
L	H	H	L	WRITE MODE	OUTPUT ENABLED DATA CAN NOT BE WRITTEN
L	H	L	H	READ MODE	OUTPUT DISABLED DATA CAN NOT BE READ
L	H	H	H	READ MODE	OUTPUT ENABLED DATA CAN BE READ

X = IRRELEVENT STATE

BLOCK DIAGRAM



ORDERING INFORMATION

Part Number	Access Time	Package	Temperature Range
3539UCD	650ns	Cerdip	0°C to +70°C
3539UCP	650ns	Plastic	0°C to +70°C
35392CD	500ns	Cerdip	0°C to +70°C
35392CP	500ns	Plastic	0°C to +70°C
35391CD	400ns	Cerdip	0°C to +70°C
35391CP	400ns	Plastic	0°C to +70°C

RECOMMENDED OPERATING CONDITIONS AMB = 0°C to +70°C

PARAMETER	SYMBOL	MIN	NOM	MAX	UNIT
Supply Voltage	V_{DD}	4.75	5.0	5.25	Vdc
Input High Level	V_{IH}	2.4		Vcc	Vdc
Input Low Level	V_{IL}	−0.5		0.8	Vdc

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DC CHARACTERISTICS (Full Operating Voltage & Temperature Range Unless Otherwise Noted)

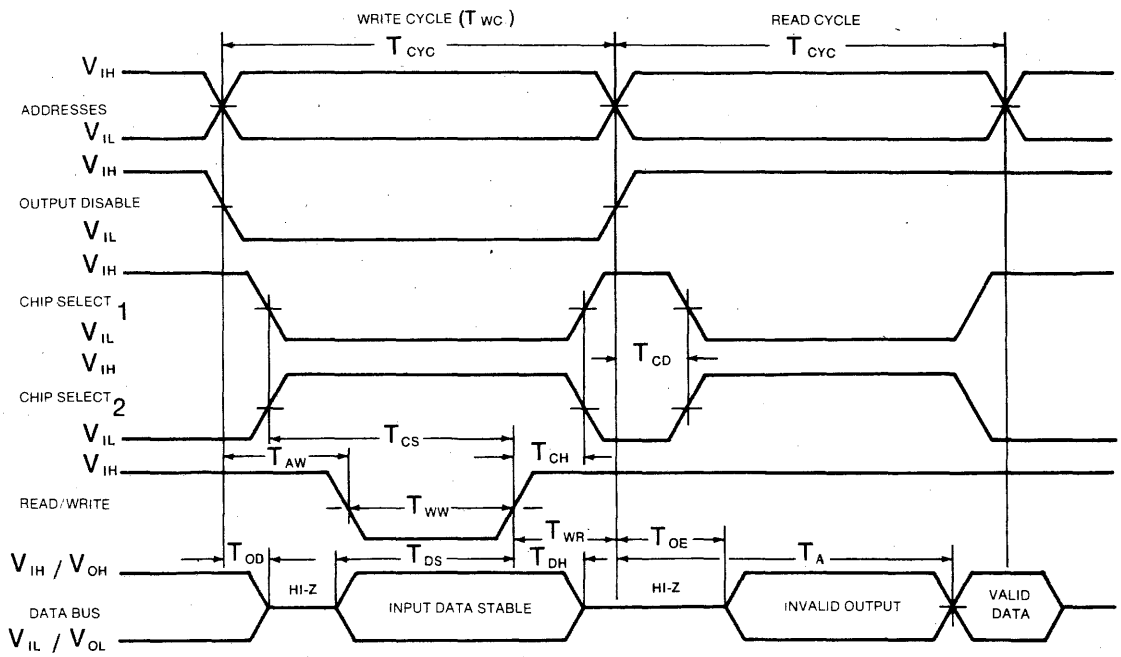
SYMBOL	PARAMETER	35391		35392		3539		UNITS	CONDITIONS
		MIN	MAX	MIN	MAX	MIN	MAX		
V_{IH}	Input HIGH Voltage	2.2		2.2		2.2		V	
V_{IL}	Input LOW Voltage		0.65		0.65		0.65	V	
V_{OH}	Output HIGH Voltage	2.2		2.2		2.2		V	$I_{OH} = -100\ \mu A$
V_{OL}	Output LOW Voltage		0.4		0.4		0.4	V	$I_{OL} = 1.6$ mA
I_{BH}	Bus HIGH Current		10		10		10	μA	$V_{IN} = V_{DD}$, Chip Deselected
I_{BL}	Bus LOW Current		−10		−10		−10	μA	$V_{DD} = 0$ V, Chip Deselected
I_{IN}	Input Leakage Current		10		10		10	μA	$V_{SS} \leq V_{IN} \leq V_{DD}$
I_{DD}	Power Supply Current		75		75		75	mA	$V_{DD} = 5.25$ V
PD	Power Dissipation		394		394		394	mW	$V_{DD} = 5.25$ V

AC CHARACTERISTICS (Full Operating Voltage & Temperature Range Unless Otherwise Noted)

SYMBOL	PARAMETER	35391		35392		3539		UNITS	CONDITIONS
		MIN	MAX	MIN	MAX	MIN	MAX		
T_{CYC}*	Read Cycle Time	400		500		650		ns	
T_A	Read Access Time		400		500		650	ns	
T_{AW}	Address to Write Delay	25		25		25		ns	
T_{DS}	Data Set-Up Time	200		250		275		ns	
T_{DH}	Data Hold Time	0		0		0		ns	
T_{WR}	Write Recovery Time	0		0		0		ns	
T_{WW}	Write Pulse Width	150		175		225		ns	
T_{CS}	Chip select to write set-up time	125		150		200		ns	
T_{CD}	Chip Select Delay Time		100		100		100	ns	
T_{CH}	Chip select to write hold time	0		0		0		ns	
T_{OD}	Output Disable Time		150		150		150	ns	
T_{OE}	Output Enable Time		200		225		250	ns	

*$T_{WC} = (T_{AW} + T_{WW} + T_{WR})$ or $(T_{OD} + T_{DS})$, whichever is relevant.

3539 TIMING DIAGRAM



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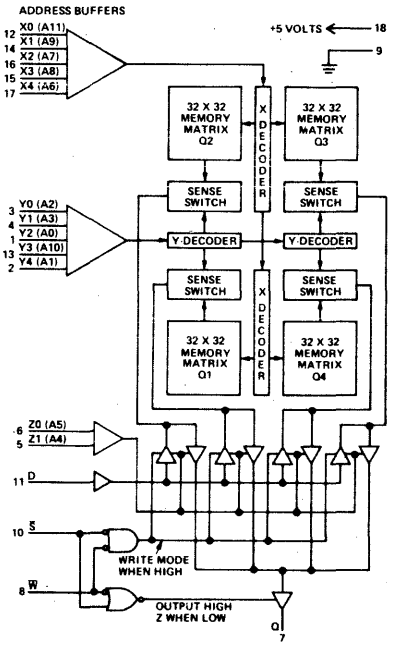
EMM4044

SEMI 4044 450NSEC, STATIC, TTL IN/OUT, 4096x1 N-MOS RAM

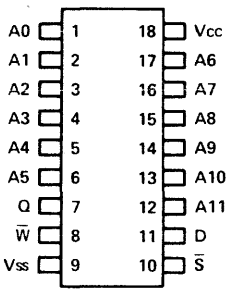
FEATURES

- 4096 words X 1 bit RAM
- High speed 450 ns ACCESS and CYCLE time
- Fully STATIC memory—no clock or refresh required
- Single +5V ±5% power supply
- 18-pin CERDIP or plastic package
- Low power dissipation—265 mw max @ 70° C
- Three-State, high impedance output
- TTL compatible interface
- Replaces 4 1024 x 1 static RAMs

BLOCK DIAGRAM



PIN CONFIGURATION



AN	Address Inputs
D	Data Input
Q	Data Output
S	Chip Select
W	Write Enable
Vss	Ground
Vcc	+5 V Power Supply

TRUTH TABLE

S	W	D	Q	STATUS	MODE
H	Don't Care	Don't Care	High Z	Deselect	Standby
L	H	Don't Care	Data	Selected	READ
L	L	L	High Z	Selected	Write 0
L	L	H	High Z	Selected	Write 1

ORDERING INFORMATION

Part Number	Access Time	Maximum Power Dissipation	Package	Temperature Range
4044-UCE	450 ns	475 mw	18-Pin Cerdip	0° C to 70° C
L4044-UCE	450 ns	265 mw	18-Pin Cerdip	0° C to 70° C
4044-UCB	450 ns	475 mw	18-Pin Plastic	0° C to 70° C
L4044-UCB	450 ns	265 mw	18-Pin Plastic	0° C to 70° C

RECOMMENDED OPERATING CONDITIONS (T_{AMB} = 0° C to 70° C)

PARAMETER	SYMBOL	MIN	NOM	MAX	UNIT
Supply Voltage	Vcc	4.75	5.0	5.25	Vdc
Input High Level	VIH	2.0		5.25	Vdc
Input Low Level	VIL	-0.5		0.8	Vdc

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DC ELECTRICAL CHARACTERISTICS (Full Operating Voltage and Temperature Range)

CHARACTERISTIC	SYMBOL	MIN	TYP	MAX	UNIT	CONDITIONS
Input Leakage Current	I_{LI}	-10	—	+10	μA	V_{IN} = 0.0 to +5.25V
Output Leakage Current	I_{LO}	-10	—	+10	μA	V_{OUT} = 0.0 to +5.25V $\overline{S}$ = 2.0Vdc, or $\overline{W}$ = 0.8Vdc
Output Voltage High	V_{OH}	2.4	—	—	Vdc	I_{OH} = -1.0 ma, V_{CC} = +4.75V
Output Voltage Low	V_{OL}	—	—	0.4	Vdc	I_{OL} = 3.2 ma
Power Supply Current						
4044 V_{CC} = +5.25Vdc	I_{CC}	—	50	70	ma	T_{AMB} = 25° C
	I_{CC}	—	—	90	ma	T_{AMB} = 70° C (Worst Case)
L4044 V_{CC}= +5.25Vdc	I_{CC}	—	35	40	ma	T_{AMB} = 25° C
	I_{CC}	—	—	50	ma	T_{AMB} = 70° C (Worst Case)

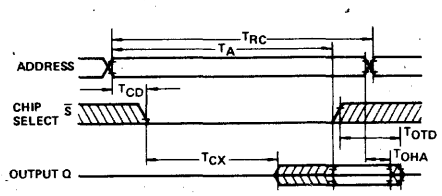
READ CYCLE—AC CHARACTERISTICS

CHARACTERISTIC	SYMBOL	MIN	TYP	MAX	UNIT	CONDITIONS
Read Cycle Time	T_{RC}	450	—	∞	ns	Full Operating Voltage and Temperature Range
Access Time	T_A	—	—	450	ns	
Chip Enable Delay Time	T_{CD}	—	—	300	ns	
Data Valid After Address	T_{OHA}	10	—	—	ns	
Output Disable From Deselection	T_{OTD}	—	—	100	ns	
Chip Select to Output Active	T_{CX}	20	—	—	ns	

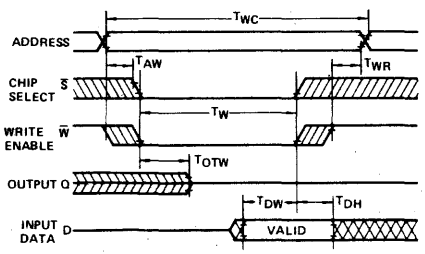
WRITE CYCLE — AC CHARACTERISTICS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT	CONDITIONS
Write Cycle Time	T_{WC}	450	—	∞	ns	Full Operating Voltage and Temperature Range
Address To Write Time	T_{AW}	0	—	—	ns	
Write Pulse Width	T_W	200	—	—	ns	
Write Recovery Time	T_{WR}	0	—	—	ns	
Data Set Up Time	T_{DW}	200	—	—	ns	
Data Hold Time	T_{DH}	0	—	—	ns	
Output Disable From Write or Chip Enable	T_{OTW}	—	—	100	ns	
Output Enabled After Write Disabled	T_{OE}	—	—	150	ns	
Read, Modify-Write Cycle	T_{RWC}	650	—	—	ns	

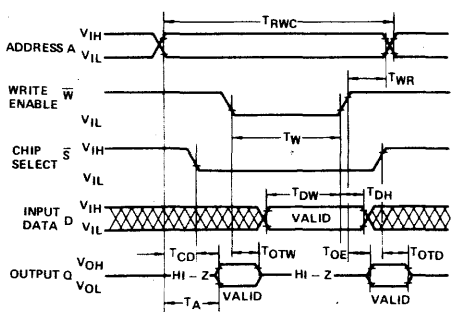
READ CYCLE TIMING



WRITE CYCLE TIMING



READ/MODIFY-WRITE CYCLE TIMING



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EMM 4300

SEMI 4300 120NSEC, STATIC, TTL IN/OUT, 4096x1 N-MOS RAM

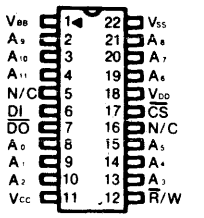
FEATURES

- Completely Static
- Access Time as low as 120 nsec max
- Cycle Time as low as 250 nsec max
- Typical Operating Power Under 450 mw.
- Typical Standby Power Under 30 mw.
- Data Retention with Low V_{DD}
- Pin and Voltage Compatible with Standard 22 Pin 4K Dynamic Rams
- TTL Compatible Three-State Outputs
- Fully Decoded
- Active Low Chip Select

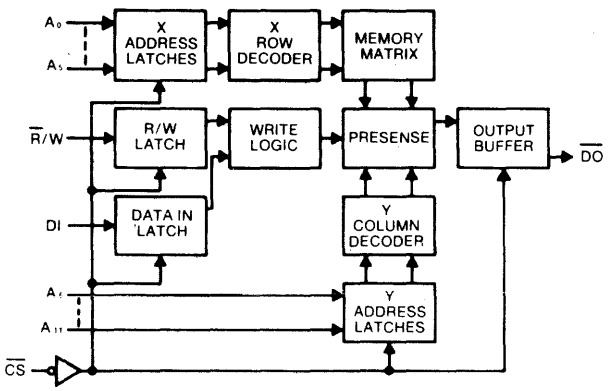
PIN CONFIGURATION

A_N	Address Inputs
DI	Data Input
$\overline{DO}$	Data Output
$\overline{CS}$	Chip Select Input
$\overline{R}/W$	Read/Write Input
N/C	No Internal Connection
V_{SS}	Ground
V_{BB}	Supply Voltage (−5V)
V_{CC}	Supply Voltage (+5V)
V_{DD}	Supply Voltage (+12V)

TOP VIEW



BLOCK DIAGRAM



ORDERING INFORMATION

Part Number	Access	Cycle	Package	Temperature Range
4300ACC	120	250	Ceramic	0°C to +70°C
4300ACP	120	250	Plastic	0°C to +70°C
4300ACD	120	250	Cerdip	0°C to +70°C

RECOMMENDED OPERATING CONDITIONS T_{AMB} = 0°C to 70°C

PARAMETER	SYMBOL	MIN	NOM	MAX	UNIT
Supply Voltage	V_{DD}	11.4	12.0	12.6	Vdc
Output Reference Voltage	V_{CC}	4.75	5.0	5.25	Vdc
Substrate Voltage	V_{BB}	−4.5	−5	−5.5	Vdc
Input High Level	V_{IH}	2.4	—	5.25	Vdc
Input Low Level	V_{IL}	−0.1	—	0.8	Vdc
Chip Select High Level	V_{CH}	8	—	15	Vdc
Chip Select Low Level	V_{CL}	−1	—	0.5	Vdc

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DC ELECTRICAL CHARACTERISTICS (Full Operating Voltage and Temperature Range Unless Otherwise Noted)

CHARACTERISTICS	SYMBOL	MIN	TYP	MAX	UNIT	CONDITIONS
Input Current	I_{IN}	−20	—	+20	μA	V_{IN} = 0.5V or 5V
Chip Select Input Current	I_{CS}	−20	—	+20	μA	V_{CS} = 0.5V or 12V
Output "Low" Voltage	V_{OL}	—	0.3	0.5	Vdc	I_{OL} = 2.0mA Fig. 5
Output "High" Voltage	V_{OH}	2.4	3.5	V_{CC}	Vdc	I_{OH} = -500 μA Fig.5
Output Current (Unselected)	I_{DO}	−20	—	+20	μA	V_{OUT} = 2.7V, V_{CS} = 12V
Supply Current (Selected and Averaged Over One Cycle) 4300 T_{CSW} 140 T_C 250 For Other Conditions	I_{DD}	—	—	45	mA	T_{AMB} = 25°C V_{DD} = 12V V_{CC} = 5V V_{BB} = −5V V_{CS} = 0.5V
Supply Current (Unselected) T_{AMB} = 25°C	I_{DD}	—	—	4	mA	V_{DD} = 12V V_{CC} = 5V V_{BB} = −5V V_{CS} = 12V
Supply Current (Unselected) T_{AMB} = 70°C	I_{DD}	—	—	8	mA	
Reference Supply Current	I_{CC}	—	50	100	μA	
Substrate Current	I_{BB}	—	—	-2	mA	V DD = 12V V CC = 5V V BB = -5V V CS = 0V or 12V
Standby Current At Reduced Voltages T_{AMB} = 25°C	I_{DDS}	—	0.8	2	mA	V_{CS} = 4V to 15V V_{DD} = 4V V_{BB} = −4V V_{CC} = 0V
Standby Current At Reduced Voltages T_{AMB} = 70°C	I_{DDS}	—	1.8	6	mA	

READ CYCLE — AC CHARACTERISTICS

CHARACTERISTICS	SYMBOL	MIN	TYP	MAX	UNIT	CONDITIONS
Chip Select Read Pulse Width	T_{CSR}	120	—	∞	ns	FULL OPERATING VOLTAGE AND TEMPERATURE RANGE
Chip Select Rise and Fall Time*	T_{CR} ,T_{CF}	—	10	100	ns	
Set Up Time	T_P	0	—	—	ns	
Access Time	T_A	—	—	120	ns	
Cycle Time, T_{CR}=T_{CF} = 10ns	T_C	250	—	—	ns	
Data Hold Time	T_H	75	—	—	ns	
Output Recovery Time	T_{DR}	10	15	—	ns	
Read Recovery Time	T_{CRR}	90	—	—	ns	

WRITE CYCLE — AC CHARACTERISTICS

CHARACTERISTICS	SYMBOL	MIN	TYP	MAX	UNIT	CONDITIONS
Chip Select Write Pulse Width	T_{CSW}	140	—	∞	ns	FULL OPERATING VOLTAGE AND TEMPERATURE RANGE
Chip Select Rise and Fall Time*	T_{CR} ,T_{CF}	—	10	100	ns	
Set Up Time	T_P	0	—	—	ns	
Cycle Time, T_{CR}=T_{CF} = 10ns	T_C	250	—	—	ns	
Data Hold Time	T_H	75	—	—	ns	
Write Recovery Time	T_{CWR}	90	—	—	ns	

*Typical Chip Select Rise and Fall Time (T_{CR} and T_{CF}) is 10 ns For Read and Write Cycle

Figure 1 — READ CYCLE

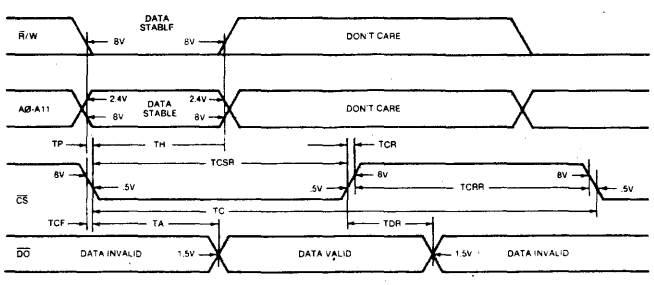
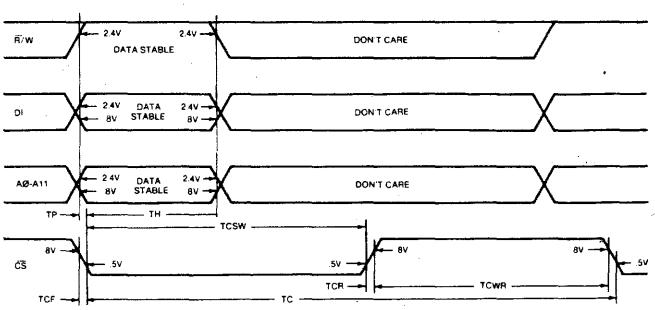


Figure 2 — WRITE CYCLE



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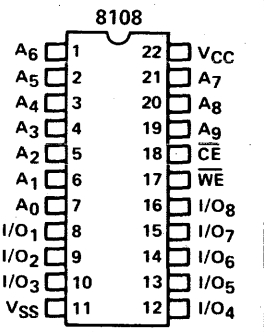
EMM8108

SEMI 8108 300NSEC, STATIC, TTL IN/OUT 1024 x 8 N-MOS RAM
SEMI 8108 500NSEC, STATIC, TTL IN/OUT 1024 x 8 N-MOS RAM

FEATURES

- 1024 words X 8 bits
- EPROM, PROM, ROM pinout compatible
- Common I/O bus
- Single +5V power supply
- No maximum limit on Chip Enable ($\overline{CE}$) pulse width
- 300 or 500 nSEC maximum access time
- Less than 60 mW power (disabled)
- Less than 270 mW power (enabled)

PIN CONFIGURATION

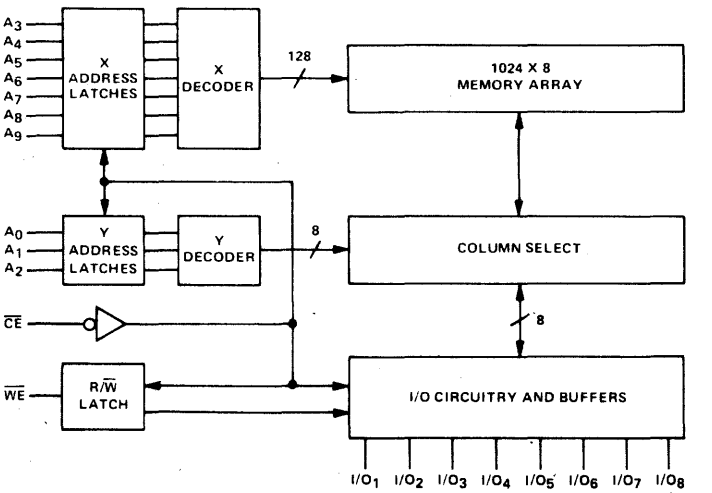


PIN NAMES

A_n	Address Inputs
$\overline{CE}$	Chip Enable Input
$\overline{WE}$	Write Enable Control Input
I/O_n	Data Bus Input/Output Pins
V_{CC}	+5V Power Supply
V_{SS}	0V Power Supply

$\overline{CE}$	$\overline{WE}$	I/O_n	STATUS	MODE
H	Don't Care	High Z	Disabled	Standby
L	H	Data	Enabled	Read
L	L	L	Enabled	Write 0
L	L	H	Enabled	Write 1

BLOCK DIAGRAM



ORDERING INFORMATION

DEVICE	ACCESS TIME	CYCLE TIME	PACKAGE	TEMP. RANGE
8108-3CD	300	450	Cerdip	0°C to 70°C
8108-5CD	500	700	Cerdip	0°C to 70°C

RECOMMENDED OPERATING CONDITIONS: (T_{AMB} = 0°C to 70°C)

PARAMETER	SYMBOL	MIN	NOM	MAX	UNIT
Supply Voltage	V_{CC}	4.75	5.0	5.25	V
Input High Level	V_{IH}	2.4	–	5.25	V
Input Low Level	V_{IL}	-0.5	–	0.8	V

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DC CHARACTERISTICS: T_A = 0°C to +70°C. V_{CC} = +5V ± +5%, unless otherwise noted.

PARAMETER	SYMBOL	8108		UNITS	CONDITIONS
		MIN	MAX		
Output HIGH Voltage	V_{OH}	2.4	5.25	V	I_{OH} = -200 μA
Output LOW Voltage	V_{OL}	–	0.4	V	I_{OL} = 2.1 mA
Output Leakage Current	I_{LO}	-10	+10	μA	$V_{I/O}$ = 0.4 V to V_{CC}, CE = 2.4 V
Input Leakage Current	I_{LI}	-10	+10	μA	V_{IN} = 0 to 5.25 V
Power Supply Current (Device Enabled)	I_{CC1}	–	50	mA	CE ⩽ 0.8 V, V_{CC} = 5V
Power Supply Current (Device Disabled)	I_{CC2}	–	10	mA	CE ⩾ 2.4 V, V_{CC} = 5 V

READ CYCLE – AC CHARACTERISTICS

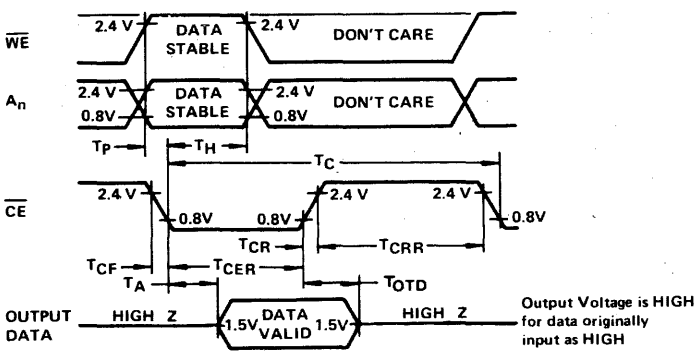
CHARACTERISTICS	SYMBOL	8108-3		8108-5		UNIT	CONDITIONS
		MIN	MAX	MIN	MAX		
Chip Enable Read Pulse Width	T_{CER}	300	∞	500	∞	nS	Full Operating Voltage and Temperature Range
Chip Enable Rise and Fall Time*	T_{CR}, T_{CF}	–	100	–	100	nS	
Set Up Time	T_P	0	–	0	–	nS	
Access Time	T_A	–	300	–	500	nS	
Cycle Time, T_{CR} = T_{CF} = 10 nS	T_C	450	–	700	–	nS	
Data Hold Time	T_H	100	–	100	–	nS	
Output Recovery Time	T_{DR}	–	75	–	75	nS	
Read Recovery Time	T_{CRR}	130	–	180	–	nS	

WRITE CYCLE – AC CHARACTERISTICS

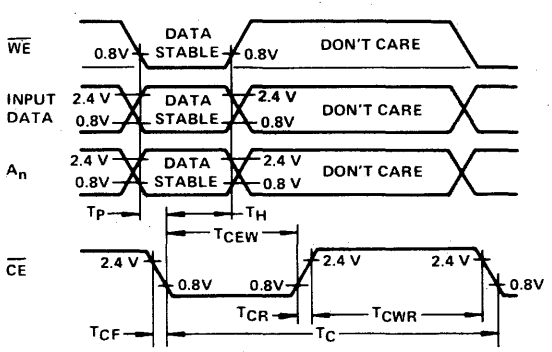
CHARACTERISTICS	SYMBOL	8108-3		8108-5		UNIT	CONDITIONS
		MIN	MAX	MIN	MAX		
Chip Enable Write Pulse Width	T_{CEW}	300	∞	500	∞	nS	Full Operating Voltage and Temperature Range
Chip Enable Rise and Fall Time*	T_{CR}, T_{CF}	–	100	–	100	nS	
Set Up Time	T_P	0	–	0	–	nS	
Cycle Time, T_{CR} = T_{CF} = 10 nS	T_C	450	–	700	–	nS	
Data Hold Time	T_H	100	–	100	–	nS	
Write Recovery Time	T_{CWR}	130	–	180	–	nS	

*Typical Chip Select Rise and Fall Time (T_{CR} and T_{CF}) is 10 nS For Read and Write Cycle

READ CYCLE – AC CHARACTERISTICS



WRITE CYCLE – AC CHARACTERISTICS



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93470 • 93471 • 93L470 • 93L471

TTL ISOPLANAR MEMORY

4096 x 1-BIT FULLY DECODED RANDOM ACCESS MEMORY

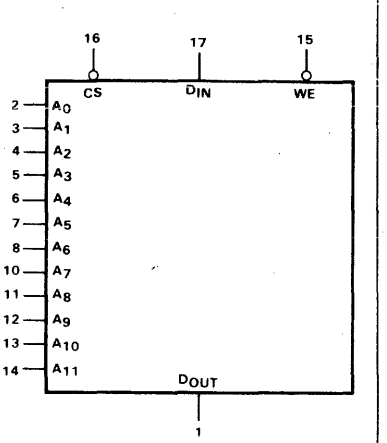
DESCRIPTION — These devices are 4096-bit TTL Read/Write Random Access Memories organized 4096 words by one bit. The devices are identical except for the output stage. The 93470 and 93L470 have an uncommitted collector output, while the 93471 and 93L471 have a 3-state output. The devices have full decoding on chip, separate Data Input and Data Output lines and active LOW Chip Select lines. They are designed for high performance main memory application and can be used to replace four 1024-bit RAMs The 93L470 and 93L471 are appropriate for systems requiring low power.

- **FULL MIL AND COMMERCIAL TEMPERATURE RANGES**
- **ORGANIZATION — 4096 WORDS x 1 BIT**
- **READ ACCESS TIME — 40 ns TYP FOR 93L470/71, 30 ns TYP FOR 93470/71**
- **CHIP SELECT ACCESS TIME — 20 ns TYP FOR 93L470/71, 15 ns TYP FOR 73470/71**
- **UNCOMMITTED COLLECTOR OUTPUT — 93L470, 93470**
- **3-STATE OUTPUT — 93L471, 93471**
- **NON-INVERTING DAA OUTPUT**
- **POWER DISSIPATION — 0.09 mW/BIT TYP — 93L470/71**
- **POWER DISSIPATION — 0.15 mW/BIT TYP — 93470/71**
- **REPLACES FOUR 1024 BY ONE RAMs**

PIN NAMES

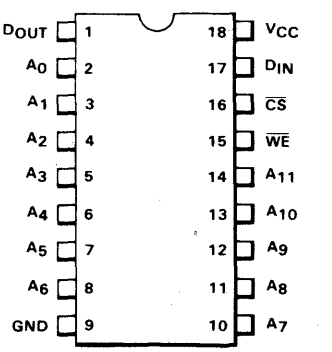
$\overline{CS}$	Chip Select Input
A_0-A_{11}	Address Inputs
$\overline{WE}$	Write Enable
D_{IN}	Data Input
D_{OUT}	Data Output

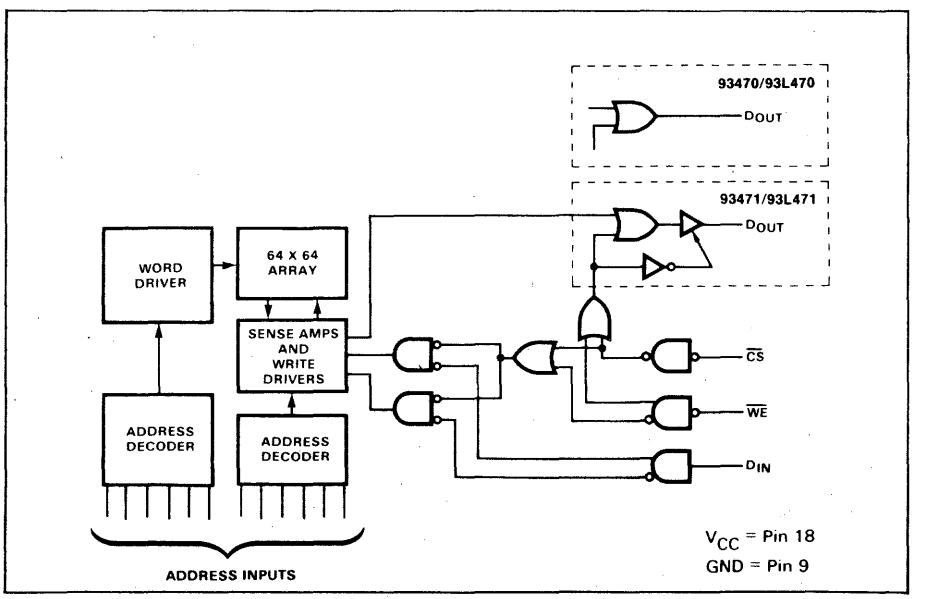
LOGIC SYMBOL



V_{CC} = Pin 18
GND = Pin 9

CONNECTION DIAGRAM
DIP (TOP VIEW)





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FAIRCHILD

Fairchild

MEMORY

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93470/71 ONLY AC CHARACTERISTICS: Over Guaranteed Operating Ranges (Notes 1–6)

SYMBOL	CHARACTERISTIC	93470/71XC			93470/71XM			UNITS	CONDITIONS
		MIN	TYP (Note 3)	MAX	MIN	TYP (Note 3)	MAX		
READ MODE	DELAY TIMES								
t_{ACS}	Chip Select Access Time		15	30		15	35		
t_{RCS}	Chip Select Recovery Time (93470)		25	35		25	45		
t_{ZRCS}	Chip Select to HIGH Z (93471)		25	35		25	45	ns	See Test Circuit
t_{AA}	Address Access Time		30	45		30	60		and Waveforms
WRITE MODE	DELAY TIMES								
t_{WS}	Write Disable Time (93470)		25	35		25	45		
t_{ZWS}	Write Disable to HIGH Z (93471)		25	35		25	45	ns	
t_{WR}	Write Recovery Time		25	35		25	45		
	INPUT TIMING REQUIREMENTS								See Test Circuit
t_W	Write Pulse Width (to guarantee write)	30	20		45	20			and Waveforms
t_{WSD}	Data Set-Up Time Prior to Write	10	5		15	5			
t_{WHD}	Data Hold Time After Write	5	0		10	0			
t_{WSA}	Address Set-Up Time	10	5		15	5		ns	
t_{WHA}	Address Hold Time	5	0		10	0			
t_{WSCS}	Chip Select Set-Up Time	5	0		10	0			
t_{WHCS}	Chip Select Hold Time	5	0		10	0			
C_I	Input Pin Capacitance		4	5		4	5	pF	Measure with
C_O	Output Pin Capacitance		7	8		7	8		Pulse Technique

NOTES:
1. Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
2. The specified LIMITS represents the "worst case" value for the parameters. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
3. Typical values are at V_{CC} = 5.0 V, T_A = 25°C, and MAX loading.
4. The Temperature Ranges are guaranteed with transverse air flow exceeding 400 linear feet per minute and a two minute warm-up. Temperature range of operation refers to case temperature for Flatpaks and ambient temperature for all other packages. Typical thermal resistance values of the package at maximum temperature are:

   θ_{JA} (Junction to Ambient) (at 400 fpm air flow) = 50°C/Watt, Ceramic DIP; 65°C/Watt, Plastic DIP, NA, Flatpak.
   θ_{JA} (Junction to Ambient) (still air) = 90°C, Watt, Ceramic DIP; 110°C/Watt, Plastic DIP, NA, Flatpak.
   θ_{JC} (Junction to Case) = 25°C/Watt, Ceramic DIP; 25°C/Watt, Plastic DIP; 15°C/Watt, Flatpak.

5. The MAX address access time is guaranteed to be the "worst case" bit in the memory using a pseudo random testing pattern.
6. t_W measured at t_{WSA} = MIN, t_{WSA} measured at t_W = MIN.
7. Duration of short circuit should not exceed one second.

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FUNCTIONAL DESCRIPTION — These devices are fully decoded 4096-bit Random Access Memories organized 4096 words by one bit. Word selection is achieved by means of a 12-bit address, A_0 through A_{11}.

The Chip Select input is provided for logic flexibility. For larger memories, the fast Chip Select access time permits the decoding of Chip Select, $\overline{CS}$, from the address without increasing address access time.

The read and write operations are controlled by the state of the active LOW Write Enable, $\overline{WE}$ (pin 15). With $\overline{WE}$ held LOW and the chip selected, the data at D_{IN} is written into the addressed location. To read, $\overline{WE}$ is held HIGH and the chip selected. Data in the specified location is presented at the Data Output.

The 93471 and 93L471 have 3-state outputs which provide drive capability for higher speeds with high capacitive load systems. The third state (high impedance) allows bus organized systems where multiple outputs are connected to a common bus.

The 93470 and 93L470 have uncommitted collector outputs to allow maximum flexibility in output connection. In many applications, such as memory expansion, the outputs of several 93470s or 93L470s can be tied together. In other applications the wired-OR is not used. In either case an external pull-up resistor of value R_L must be used to provide a HIGH at the output when it is off. Any value of R_L within the range specified below may be used.

$$\frac{V_{CC(max)}}{I_{OL} - F.O.\ (1.6)} \leq R_L \leq \frac{V_{CC(min)} - V_{OH}}{N\ (I_{CEX}) + F.O.\ (0.04)}$$

R_L is in kΩ
N = number of wired-OR outputs tied together
F.O. = number of TTL Unit Loads (U.L.) driven
I_{CEX} = Memory Output Leakage Current in mA
V_{OH} = Required Output HIGH level at Output Node
I_{OL} = Output Low Current

The minimum value of R_L is limited by output current sinking ability. The maximum value of R_L is determined by the output and input leakage current which must be supplied to hold the output at V_{OH}.

TRUTH TABLE

INPUTS			OUTPUTS		MODE
$\overline{CS}$	$\overline{WE}$	D_{IN}	O.C.	3-STATE	
H	X	X	H	HIGH Z	Not Selected
L	L	L	H	HIGH Z	Write "0"
L	L	H	H	HIGH Z	Write "1"
L	H	X	D_{OUT}	D_{OUT}	Read

H = HIGH Voltage, L = LOW Voltage; X = Don't Care (HIGH or LOW)
HIGH Z = High Impedance, OC = Open Collector

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
Input Voltage (dc)*	−0.5 V to +5.5 V
Input Current (dc)*	−12 mA to +5.0 mA
Voltage Applied to Outputs (output HIGH)**	−0.5 V to +5.50 V
Output Current (dc)	−20 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.
**Output Current Limit Required.

GUARANTEED OPERATING RANGES

PART NUMBER	SUPPLY VOLTAGE (V_{CC})			AMBIENT TEMPERATURE Note 4
	MIN	TYP	MAX	
93470XC/93471XC 93L470XC/93L471XC	4.75 V	5.0 V	5.25 V	0° C to +75° C
93L470XM/93L471XM 93470XM/93471XM	4.50 V	5.0 V	5.50 V	-55° C to +125° C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

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DC CHARACTERISTICS: Over Operating Temperature Ranges (Notes 1-4)

SYMBOL	CHARACTERISTIC		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	CONDITIONS
V_{OL}	Output LOW Voltage			0.3	0.50	V	V_{CC} = MIN; I_{OL} = 16mA
V_{IH}	Input HIGH Voltage		2.1	1.6		V	Guaranteed Input HIGH Voltage for all Inputs
V_{IL}	Input LOW Voltage			1.5	0.8	V	Guaranteed Input LOW Voltage for all Inputs
I_{IL}	Input LOW Current			−250	−400	μA	V_{CC} = MAX, V_{IN} = 0.4 V
I_{IH}	Input HIGH Current			1.0	40 1.0	μA mA	V_{CC} = MAX, V_{IN} = 4.5 V V_{CC} = MAX, V_{IN} = 5.25 V
V_{CD}	Input Diode Clamp Voltage			−1.0	−1.5	V	V_{CC} = MAX, I_{IN} = −10 mA
I_{CEX}	Output Leakage Current	93471/93L471		1.0	100	μA	V_{CC} = MAX, V_{OUT} = 4.5 V
I_{OFF}	Output Current (HIGH Z)	93471/93L471			50 −50	μA	V_{CC} = MAX, V_{OUT} = 2.4 V V_{CC} = MAX, V_{OUT} = 0.5 V
V_{OH}	Output HIGH Voltage	93470/93L470	2.4			V	V_{CC} = MIN, I_{OH} = −5.2 mA
I_{OS}	Output Current Short Circuit to Ground	93470/93L470			−100	mA	V_{CC} = MAX, Note 7
I_{CC}	Power Supply Current	93L470/71XC		67		mA	T_A = +75°C, V_{CC} = MAX, All Inputs and Outputs Open
		93L470/71XC		80			T_A = 0°C
		93L470/71XM		63			T_A = +125°C
		93L470/71XM		86			T_A = −55°C
		93470/71XC		110			T_A = 75°C
		93470/71XC		130	170		T_A = 0°C
		93470/71XM		100			T_A = 125°C
		93470/71XM		140	180		T_A = −55°C

93L470/71 ONLY AC CHARACTERISTICS: Over Guaranteed Operating Ranges (Notes 1-6)

SYMBOL	CHARACTERISTIC	93L470/71XC MIN	93L470/71XC TYP (Note 3)	93L470/71XC MAX	93L470/71XM MIN	93L470/71XM TYP (Note 3)	93L470/71XM MAX	UNITS	CONDITIONS
READ MODE	DELAY TIMES								
t_{ACS}	Chip Select Access Time		20			20		ns	See Test Circuit and Waveforms
t_{RCS}	Chip Select Recovery Time (93L470)		30			30			
t_{ZRCS}	Chip Select to HIGH Z (93L471)		30			30			
t_{AA}	Address Access Time		40			40			
WRITE MODE	DELAY TIMES								
t_{WS}	Write Disable Time (93L470)		30			30		ns	
t_{ZWS}	Write Disable to HIGH Z (93L471)		30			30			
t_{WR}	Write Recovery Time		30			30			
	INPUT TIMING REQUIREMENTS								
t_W	Write Pulse Width (to guarantee write)		25			25		ns	See Test Circuit and Waveforms
t_{WSD}	Data Set-Up Time Prior to Write		5			5			
t_{WHD}	Data Hold Time After Write		0			0			
t_{WSA}	Address Set-Up Time		5			5			
t_{WHA}	Address Hold Time		0			0			
t_{WSCS}	Chip Select Set-Up Time		0			0			
t_{WHCS}	Chip Select Hold Time		0			0			
C_I	Input Pin Capacitance		4	5		4	5	pF	Measure with Pulse Technique
C_O	Output Pin Capacitance		7	8		7	8		

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F10470 • F100470

ECL ISOPLANAR MEMORY

4096 x 1-BIT FULLY DECODED RANDOM ACCESS MEMORY

DESCRIPTION — These devices are 4096-bit Read/Write Random Access Memories organized 4096 words by one bit. They are designed for high-speed scratchpad, control and buffer storage applications.

The F10470 is compatible with the F10K and uncompensated 10K ECL logic series and includes on-chip voltage compensation for improved noise margin. The F10470 is specified to operate over the 0° C to 75° C temperature range.

The F100470 has on-chip voltage and temperature compensation and is compatible with the F100K and 95K series of ECL logic. The device is specified to operate over the 0° C to 85° C temperature range.

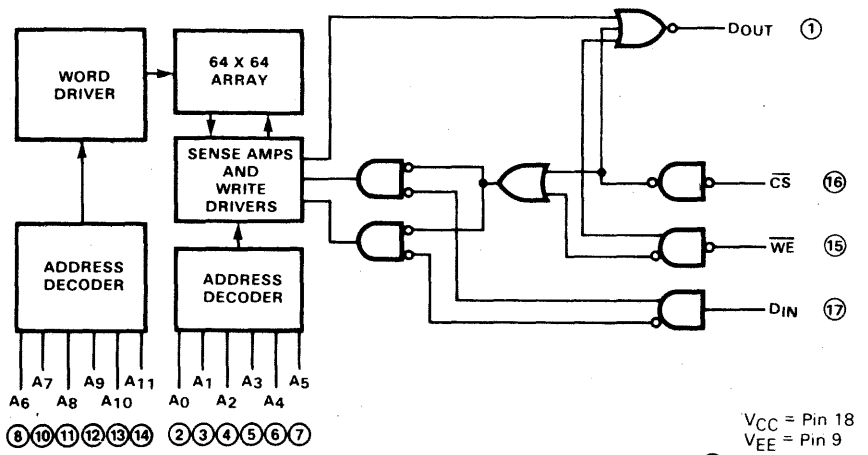
Features common to both devices are full address decoding on chip, separate Data In and non-inverting Data Out lines and an active LOW Chip Select line. The devices are packaged in a hermetic ceramic 18-pin dual in-line package.

- **ORGANIZED 4096 WORDS BY ONE BIT**
- **OPEN EMITTER OUTPUT FOR EASE OF MEMORY EXPANSION**
- **READ ACCESS TIME — 25 ns TYP**
- **POWER DISSIPATION — 0.2 mW/BIT**
- **F10470 — COMPATIBLE WITH F10K AND UNCOMPENSATED 10K ECL LOGIC**
- **F100470 — COMPATIBLE WITH F100K AND 95K ECL LOGIC**

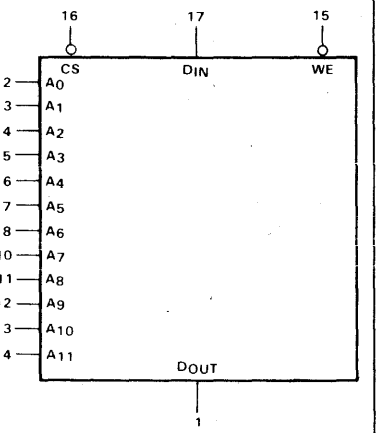
PIN NAMES

$\overline{CS}$	Chip Select Input
A_0 — A_{11}	Address Inputs
$\overline{WE}$	Write Enable
D_{IN}	Data Input
D_{OUT}	Data Output

LOGIC DIAGRAM

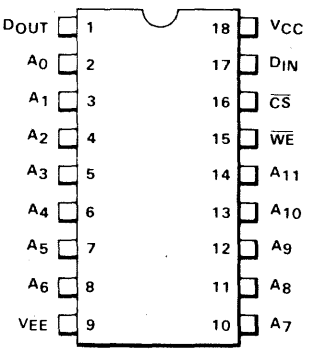


LOGIC SYMBOL



V_{CC} = Pin 18
V_{EE} = Pin 9

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

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464 ELLIS STREET, MOUNTAIN VIEW, CALIFORNIA 94042 (415) 962-5011/TWX 910-379-6435

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FUNCTIONAL DESCRIPTION — These devices are fully decoded 4096-bit Random Access Memories organized 4096 words by one bit. Word selection is achieved by means of a 12-bit address, A_0 thru A_{11}.

One chip Select input is provided for memory array expansion up to 8192 words without the need for external decoding. For larger memories, the fast Chip Select access time permits the decoding of Chip Select, $\overline{CS}$, from the address without increasing address access time.

The read and write operations are controlled by the state of the active LOW Write Enable, $\overline{WE}$ (Pin 15). With $\overline{WE}$ held LOW and the chip selected, the data at D_{IN} is written into the addressed location. To read, $\overline{WE}$ is held HIGH and the chip selected. Data in the specified location is presented at D_{OUT} and is non-inverted.

An unterminated emitter-follower output is provided to allow maximum flexibility i output connection. In many applications such as memory expansion, the outputs of many F10470s or F100470s can be tied together. In other applications the wired-OR is not used. In either case an external 50 Ω pull down resistor to -2 V or an equivalent network must be used to provide a LOW at the output when it is off.

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{EE} Pin Potential to Ground Pin	−7.0 V to +0.5 V
Input Voltage (dc)	V_{EE} to +0.5 V
Output Current (dc Output HIGH)	−30 mA to +0.1 mA

TABLE 1 – TRUTH TABLE

INPUTS			OUTPUT	MODE
$\overline{CS}$	$\overline{WE}$	D_{IN}	OPEN EMITTER	
H	X	X	L	Not Selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	X	D_{OUT}	Read

L LOW Voltage Levels 1.7 V
H HIGH Voltage Levels 0.9 V
(Nominal values)
X Don't Care

GUARANTEED OPERATING RANGES

PART NUMBER	SUPPLY VOLTAGE (V_{EE})			AMBIENT TEMPERATURE (T_A)
	MIN	TYP	MAX	(Note 4)
F10470	−5.46 V	−5.2 V	−4.94 V	0°C to +75°C
F100470	-5.7 V	-4.5 V	-4.2 V	0°C to +85°C

F10470 ONLY DC CHARACTERISTICS: V_{EE} = −5.2 V, V_{CC} = GND, Output Load = 50 Ω and 30 pF to −2.0 V, T_A = 0°C to 75°C (Note 4)

SYMBOL	CHARACTERISTIC	B LIMIT	TYP (Note 3)	A LIMIT	UNITS	T_A	CONDITIONS	
V_{OH}	Output Voltage HIGH	−1000		−840	mV	0°C	$V_{IN} = V_{IHA}$ or V_{ILB}	Loading is 50 Ω to −2.0 V
		−960		−810		25°C		
		−900		−720		75°C		
V_{OL}	Output Voltage LOW	−1870		−1665	mV	0°C		
		−1850		−1650		25°C		
		−1830		−1625		75°C		
V_{OHC}	Output Voltage HIGH	−1020			mV	0°C	$V_{IN} = V_{IHB}$ or V_{ILA}	
		−980				25°C		
		−920				75°C		
V_{OLC}	Output Voltage LOW			−1645	mV	0°C		
				−1630		25°C		
				−1605		75°C		
V_{IH}	Input Voltage HIGH	−1145		−840	mV	0°C	Guaranteed Input Voltage HIGH for All Inputs	
		−1105		−810		25°C		
		−1045		−720		75°C		
V_{IL}	Input Voltage LOW	−1870		−1490	mV	0°C	Guaranteed Input Voltage LOW for All Inputs	
		−1850		−1475		25°C		
		−1830		−1450		75°C		
I_{IH}	Input Current HIGH			220	μA	0 to 75°C	$V_{IN} = V_{IHA}$	
I_{IL}	Input Current LOW, $\overline{CS}$	0.5		170	μA	25°C	$V_{IN} = V_{ILB}$	
	All others	−50						
I_{EE}	Power Supply Current		−145		mA	75°C	All Inputs and Output Open	
	(Pin 9)	-200	−160			0°C		

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F100470 ONLY DC CHARACTERISTICS: V_{EE} = −4.5 V, V_{CC} = GND, Output Load = 50 Ω and 30 pF to −2.0 V, T_A = 0°C to +85°C (Note 4)

SYMBOL	CHARACTERISTIC	LIMITS (Note 6) B	LIMITS (Note 6) TYP (Note 3)	LIMITS (Note 6) A	UNITS	CONDITIONS	
V_{OH}	Output Voltage HIGH	1025	955	−880	mV	V_{IN} = V_{IHA} or V_{ILB}	Loading is 50 Ω to −2.0 V
V_{OL}	Output Voltage LOW	1810	−1715	−1620	mV		
V_{OHC}	Output Voltage HIGH	1035			mV	V_{IN} = V_{IHB} or V_{ILA}	
V_{OLC}	Output Voltage LOW			−1610	mV		
V_{IH}	Input Voltage HIGH	1165		−880	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input Voltage LOW	1810		−1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IH}	Input Current HIGH			220	μA	V_{IN} = V_{IHA}	
I_{IL}	Input Current LOW, $\overline{CS}$ All others	0.5 50		170	μA	V_{IN} = V_{ILB}	
I_{EE}	Power Supply Current	−195	−160		mA	All Inputs and Output open	

NOTES:
1. Conditions for testing, not shown in the tables are chosen to guarantee operation under "worst case" conditions.
2. The specified Limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
3. Typical values are V_{EE} = −4.5 V for F100470, V_{EE} = −5.2 V for F10470, T_A = 25°C and maximum loading unless otherwise specified.
4. Guaranteed with transverse air flow exceeding 400 linear F.P.M. and 2 minute warm-up period. Typical resistance values of the package are:
   θ_{JA} (Junction to Ambient) = 90°C/Watt (still air)
   θ_{JA} (Junction to Ambient) = 50°C/Watt (at 400 F.P.M. air flow)
   θ_{JC} (Junction to Case) = 25°C/Watt
5. The maximum address access time is guaranteed to be the worst case bit in the memory using a pseudorandom testing pattern.
6. DEFINITION OF SYMBOLS AND TERMS USED IN THIS DATA SHEET:
   The symbols and terms used in this data sheet have been chosen to agree with the latest standards of the Electronics Industries Association and the International Electrotechnical Commission. The relative values of the specified conditions and limits will be referenced to an algebraic scale. The extremities of the scale are: "A" the value closest to positive infinity, "B" the value closest to negative infinity.

AC CHARACTERISTICS: F10470: V_{EE} = −5.2 V ±5%, T_A = 0°C to 75°C, Output Load = 50 Ω, 30 pF to −2.0 V
F100470: V_{EE} = −4.5 V ±5%, T_A = 0°C to 85°C, Output Load = 50 Ω, 30 pF to −2.0 V

SYMBOL	PARAMETER	MIN	TYP (Note 3)	MAX	UNITS	CONDITIONS
t_{ACS}	Chip Select Access Time		10	15	ns	measured at 50% of input to valid output (V_{ILA} for V_{OL} or V_{IHB} or V_{OH})
t_{RCS}	Chip Select Recovery Time		10	15	ns	
t_{AA}	Address Access Time		25	35	ns	
t_W	Write Pulse Width (to Guarantee writing)	25	18		ns	
t_{WSD}	Data Set-up Time Prior to Write	5	1		ns	
t_{WHD}	Data Hold Time After Write	5	1		ns	
t_{WSA}	Address Set-up Time Prior to Write	10	5		ns	
t_{WHA}	Address Hold Time After Write	5	1		ns	
t_{WSCS}	Chip Select Set-up Time Prior to Write	5	1		ns	
t_{WHCS}	Chip Select Hold Time After Write	5	1		ns	measured at 50% of input to valid output (V_{ILA} for V_{OL} or V_{IHB} for V_{OH})
t_{WS}	Write Disable Time		7	15	ns	
t_{WR}	Write Recovery Time		10	20	ns	
t_r	Output Rise Time		5		ns	Measured between 20% and 80% points.
t_f	Output Fall Time		5		ns	
C_{IN}	Input Pin Capacitance		4		pF	Measure with a Pulse Technique
C_{OUT}	Output Pin Capacitance		7		pF	

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93415 • 93L415 • 93425 • 93L425

TTL ISOPLANAR MEMORY

1024 x 1-BIT FULLY DECODED RANDOM ACCESS MEMORIES

DESCRIPTION — These devices are 1024-Bit Read/Write Random Access Memories organized 1024 words by one bit and are designed for buffer control storage and high performance main memory applications. The typical access time ranges from 25 ns to 40 ns depending upon the device type. The 93L415 and 93L425 are appropriate for systems requiring low power.

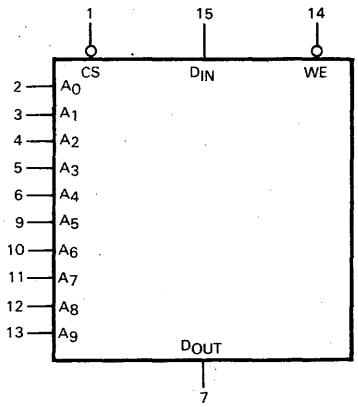
Each 1024-bit memory has full decoding on chip, separate Data Input and Data Output lines and an active LOW Chip Select line. The 93425 and 93L425 have a 3-state output to drive bus organized systems and/or highly capacitive loads and the 93415 and 93L415 have an uncommitted collector output for ease of memory expansion. All of the devices are fully compatible with standard DTL and TTL logic families.

- **FULL MIL AND COMMERCIAL RANGES**
- **3-STATE OUTPUT — 93425 AND 93L425**
- **UNCOMMITTED COLLECTOR OUTPUT — 93415 AND 93L415**
- **NON-INVERTING DATA OUTPUT**
- **ORGANIZED 1024 WORDS x 1 BIT**
- **POWER DISSIPATION 250 mW TYP — 93L415 AND 93L425**
- **POWER DISSIPATION 0.5 mW TYP — 93415 AND 93425**
- **TTL INPUTS AND OUTPUT**
- **POWER DISSIPATION DECREASES WITH INCREASING TEMPERATURE**

PIN NAMES

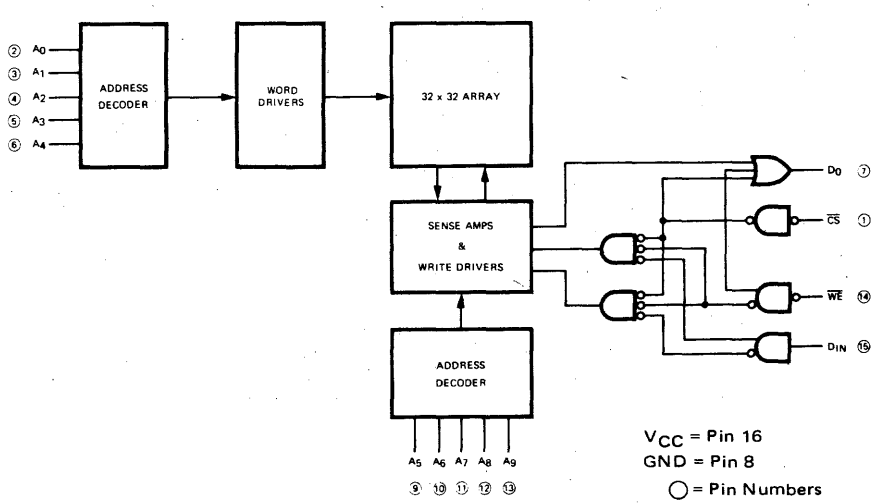
$\overline{CS}$	Chip Select Input
$A_0 - A_9$	Address Inputs
$\overline{WE}$	Write Enable Input
D_{IN}	Data Input
D_{OUT}	Data Output

LOGICAL SYMBOL



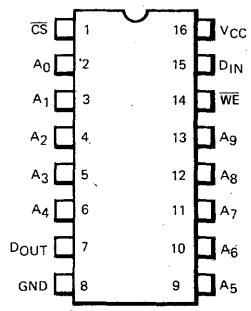
V_{CC} = Pin 16
GND = Pin 8

93415/93L415 LOGIC DIAGRAM



V_{CC} = Pin 16
GND = Pin 8
◯ = Pin Numbers

CONNECTION DIAGRAMS
DIP (TOP VIEW)



Note:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

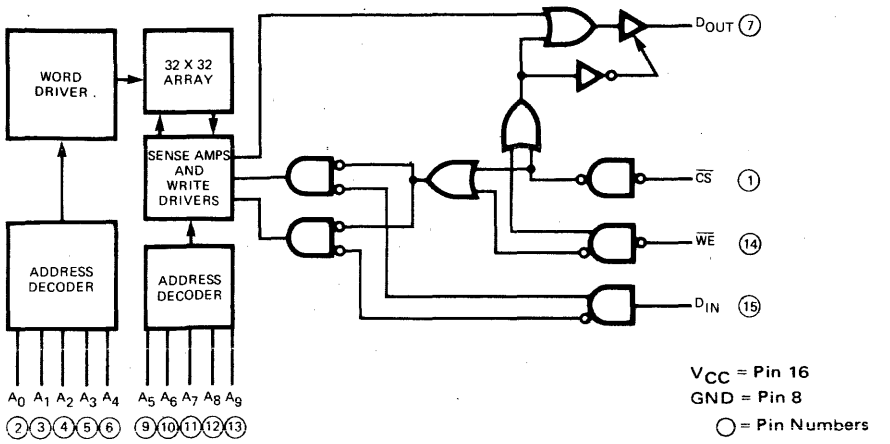
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93425/93L425 LOGIC DIAGRAM



FUNCTIONAL DESCRIPTION — These devices are fully decoded 1024-Bit Random Access Memories organized 1024 words by one bit. Word selection is achieved by means of a 10-bit address, A_0-A_9. The Chip Select input allows memory array expansion. For large memories, the fast chip select access time permits decoding of the Chip Select ($\overline{CS}$) from the address without affecting system performance. The read and write operations are controlled by the state of the active LOW Write Enable ($\overline{WE}$). With $\overline{WE}$ held LOW and the chip selected, the data at D_{IN} is written into the addressed location. To read, $\overline{WE}$ is held HIGH and the chip selected. Data in the specified location is presented at D_{OUT} and is non-inverted.

93425 and 93L425 Only

The 93425 and 93L425 3-state outputs provide drive capability for higher speeds with high capacitive load systems. The third state (high impedance) allows bus organized systems where multiple outputs are connected to a common bus. During writing, the output is held in the high impedance state.

93415 and 93L415 Only

The 93415 and 93L415 uncommitted collector outputs are provided to allow maximum flexibility in output connection. In many applications such as memory expansion, the outputs of many 93415s or 93L415s can be tied together. In other applications, the wired-OR is not used. In either case, an external pull-up resistor of R_L value must be used to provide a HIGH at the output when it is off. Any R_L value within the range specified below may be used. The minimum R_L value is limited by output current sinking ability. The maximum R_L value is determined by the output and input leakage current which must be supplied to hold the output at V_{OH}. One Unit Load = 40 μA HIGH/1.6 mA LOW.

$$\frac{V_{CC}\,(min)}{I_{OL} - FO\,(1.6)} \leq R_L \leq \frac{V_{CC}\,(min) - V_{OH}}{n\,(I_{CEX}) + FO\,(0.04)}$$

R_L is in kΩ
n = number of wired-OR outputs tied together
FO = number of TTL Unit Loads (UL) driven
I_{CEX} = Memory Output Leakage Current
V_{OH} = Required Output HIGH Level at Output Node
I_{OL} = Output LOW Current

93415/93L415 – TRUTH TABLE

INPUTS			OUTPUT	MODE
$\overline{CS}$	$\overline{WE}$	D_{IN}	Open Collector	
H	X	X	H	NOT SELECTED
L	L	L	H	WRITE "0"
L	L	H	H	WRITE "1"
L	H	X	D_{OUT}	READ

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care (HIGH or LOW)

93425/93L425 – TRUTH TABLE

INPUTS			OUTPUT	MODE
$\overline{CS}$	$\overline{WE}$	D_{IN}	D_{OUT}	
H	X	X	HIGH Z	Not Selected
L	L	L	HIGH Z	Write "0"
L	L	H	HIGH Z	Write "1"
L	H	X	D_{OUT}	Read

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care (HIGH or LOW)

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ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +5.5 V
*Input Current (dc)	−12 mA to +5.0 mA
**Voltage Applied to Outputs (output HIGH)	0.5 V to +5.50 V
Output Current (dc) (output LOW)	+20 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.
**Output Current Limit Required.

GUARANTEED OPERATING RANGES

PART NUMBER	SUPPLY VOLTAGE (V_{CC})			AMBIENT TEMPERATURE (T_A) (Note 4)
	MIN	TYP	MAX	
93415XC, 934L15XC 93425XC, 934L25XC	4.75 V	5.0 V	5.25 V	0°C to +75°C
93415XM, 93415XM 93425XM, 934L25XM	4.50 V	5.0 V	5.50 V	−55°C to +125°C

X = package type; F for Flatpak, D for Ceramic DIP, P for Plastic DIP. See Packaging Information Section for packages available on this product.

93415 DC CHARACTERISTICS: Over Operating Temperature Ranges (Notes 1, 2, 4)

SYMBOL	CHARACTERISTIC	LIMITS			UNITS	CONDITIONS	
		MIN	TYP (Note 3)	MAX			
V_{OL}	Output LOW Voltage		0.3	0.45	V	V_{CC} = MIN, I_{OL} = 16 mA	
V_{IH}	Input HIGH Voltage	2.1	1.6		V	Guaranteed Input HIGH Voltage for all Inputs	
V_{IL}	Input LOW Voltage		1.5	0.8	V	Guaranteed Input LOW Voltage for all Inputs	
I_{IL}	Input LOW Current		−250	−400	μA	V_{CC} = MAX, V_{IN} = 0.4 V	
I_{IH}	Input HIGH Current		1.0	40	μA	V_{CC} = MAX, V_{IN} = 4.5 V	
				1.0	mA	V_{CC} = MAX, V_{IN} = 5.25 V	
I_{CEX}	Output Leakage Current		1.0	100	μA	V_{CC} = MAX, V_{OUT} = 4.5 V	
V_{CD}	Input Diode Clamp Voltage		−1.0	−1.5	V	V_{CC} = MAX, I_{IN} = −10 mA	
I_{CC}	Power Supply Current		95	130	mA	$T_A \geq 75°C$	V_{CC} = MAX, All Inputs Grounded
				155	mA	T_A = 0°C	
				170	mA	T_A = −55°C	

93L415 DC CHARACTERISTICS: Over Operating Temperature Ranges (Notes 1, 2, 4)

SYMBOL	CHARACTERISTIC	LIMITS			UNITS	CONDITIONS	
		MIN	TYP (Note 3)	MAX			
V_{OL}	Output LOW Voltage		0.35	0.50	V	V_{CC} = MIN, I_{OL} = 16 mA	
V_{IH}	Input HIGH Voltage	2.1	1.6		V	Guaranteed Input HIGH Voltage for all Inputs	
V_{IL}	Input LOW Voltage		1.5	0.8	V	Guaranteed Input LOW Voltage for all Inputs	
I_{IL}	Input LOW Current		−150	−300	μA	V_{CC} = MAX, V_{IN} = 0.4 V	
I_{IH}	Input HIGH Current		1.0	40	μA	V_{CC} = MAX, V_{IN} = 4.5 V	
				1.0	mA	V_{CC} = MAX, V_{IN} = 5.25 V	
I_{CEX}	Output Leakage Current		1.0	100	μA	V_{CC} = MAX, V_{OUT} = 4.5 V	
V_{CD}	Input Diode Clamp Voltage		−1.0	−1.5	V	V_{CC} = MAX, I_{IN} = −10 mA	
I_{CC}	Power Supply Current			55	mA	$T_A \geq 75°C$	V_{CC} = MAX, All Inputs Grounded
			45	65	mA	T_A = 0°C	
				75	mA	T_A = −55°C	

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93425 DC CHARACTERISTICS: Over Operating Temperature Ranges (Notes 1, 2, 4)

SYMBOL	CHARACTERISTIC		LIMITS MIN	LIMITS TYP (Note 3)	LIMITS MAX	UNITS	CONDITIONS	
V_{OL}	Output LOW Voltage			0.3	0.45	V	V_{CC} = MIN, I_{OL} = 16 mA	
V_{IH}	Input HIGH Voltage		2.1	1.6		V	Guaranteed Input HIGH Voltage for all Inputs	
V_{IL}	Input LOW Voltage			1.5	0.8	V	Guaranteed Input LOW Voltage for all Inputs	
I_{IL}	Input LOW Current			−250	−400	μA	V_{CC} = MAX, V_{IN} = 0.4 V	
I_{IH}	Input HIGH Current			1.0	40	μA	V_{CC} = MAX, V_{IN} = 4.5 V	
					1.0	mA	V_{CC} = MAX, V_{IN} = 5.25 V	
I_{OFF}	Output Current (HIGH Z)				50	μA	V_{CC} = MAX, V_{OUT} = 2.4 V	
					−50		V_{CC} = MAX, V_{OUT} = 0.5 V	
I_{OS}	Output Current Short Circuit to Ground				−100	mA	V_{CC} = MAX, Note 7	
V_{OH}	Output HIGH Voltage	93425XC	2.4			V	I_{OH} = −10.3 mA, V_{CC} = 5.0 V ±5%	
		93425XM	2.4			V	I_{OH} = −5.2 mA	
V_{CD}	Input Diode Clamp Voltage			−1.0	−1.5	V	V_{CC} = MAX, I_{IN} = −10 mA	
I_{CC}	Power Supply Current				130	mA	$T_A \geq 75°C$	V_{CC} = MAX, All Inputs Grounded
				95	155	mA	T_A = 0°C	
					170	mA	T_A = −55°C	

93L425 DC CHARACTERISTICS: Over Operating Temperature Ranges. Notes 1, 2 and 4

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP (Note 3)	LIMITS MAX	UNITS	CONDITIONS	
V_{OL}	Output LOW Voltage			0.35	0.50	V	V_{CC} = MIN, I_{OL} = 16 mA	
V_{IH}	Input HIGH Voltage		2.1	1.6		V	Guaranteed Input HIGH Voltage for all Inputs	
V_{IL}	Input LOW Voltage			1.5	0.8	V	Guranteed Input LOW Voltage for all Inputs	
I_{IL}	Input LOW Current			−150	−300	μA	V_{CC} = MAX, V_{IN} = 0.4 V	
I_{IH}	Input HIGH Current			1.0	40	μA	V_{CC} = MAX, V_{IN} = 4.5 V	
					1.0	mA	V_{CC} = MAX, V_{IN} = 5.25 V	
I_{OFF}	Output Current (HIGH Z)				50	μA	V_{CC} = MAX, V_{OUT} = 2.4 V	
					−50		V_{CC} = MAX, V_{OUT} = 0.5 V	
I_{OS}	Output Current Short Circuit to Ground				−100	mA	V_{CC} = MAX, Note 7	
V_{OH}	Output HIGH Voltage	93L425XC	2.4			V	I_{OH} = −5.2 mA, V_{CC} = 5.0 V ±5%	
		93L425XM	2.4			V	I_{OH} = −5.2 mA, V_{CC} = 5.0 V ±10%	
V_{CD}	Input Clamp Diode Voltage			−1.0	−1.5	V	V_{CC} = MAX, I_{IN} = −10 mA	
I_{CC}	Power Supply Current				55	mA	$T_A \geq 75°C$	V_{CC} = MAX, All Inputs Grounded
				45	65	mA	T_A = 0°C	
					75	mA	T_A = −55°C	

NOTES:
1. Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
2. The specified LIMITS represents the "worst case" value for the parameters. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
3. Typical limits are at V_{CC} = 5.0 V, T_A = +25°C, and MAX loading.
4. The Temperature Ranges are guaranteed with transverse air flow exceeding 400 linear feet per minute. For military range an additional requirement of a two minute warm-up. Typical thermal resistance values of the package at maximum temperature are:
   θ_{JA} (Junction to Ambient) (at 400 fpm air flow) = 50°C/Watt, Ceramic DIP; 65°CC/Watt, Plastic DIP; NA, Flatpak.
   θ_{JA} (Junction to Ambient) (still air) = 90°C/Watt, Ceramic DIP; 110°C/Watt, Plastic DIP, NA, Flatpak.
   θ_{JC} (Junction to Case) = 25°C/Watt, Ceramic DIP; 25°C/Watt, Plastic DIP; 10°C/Watt, Flatpak.
5. The MAX address access time is guaranteed to be the "worst case" bit in the memory using a pseudo random testing pattern.
6. t_W measured at t_{WSA} = MIN, t_{WSA} measured at t_W = MIN.
7. Duration of short circuit should not exceed one second.

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AC CHARACTERISTICS: Over Guaranteed Operating Ranges (Notes 1, 2, 4, 5, 6)

SYMBOL	CHARACTERISTIC	93415/25AXC			93415/25XC			93415/25XM			UNITS	CONDITIONS
		MIN	TYP (Note 3)	MAX	MIN	TYP (Note 3)	MAX	MIN	TYP (Note 3)	MAX		
READ MODE	DELAY TIMES											
t_{ACS}	Chip Select Time		15	20		15	35		15	45	ns	See Test Circuit and Waveforms
t_{RCS}	Chip Select Recovery Time		15	20		20	35		20	50		
t_{AA}	Address Access Time		25	30		30	45		40	60		
WRITE MODE	DELAY TIMES											
t_{WS}	Write Disable Time		15	20		20	35		20	45	ns	
t_{WR}	Write Recovery Time		20	25		25	40		45	50		
	INPUT TIMING REQUIREMENTS											
t_W	Write Pulse Width (to guarantee write)	20	15		30	25		40	25		ns	See Test Circuit and Waveforms
t_{WSD}	Data Set-Up Time Prior to Write	5	0		5	0		5	0			
t_{WHD}	Data Hold Time After Write	5	0		5	0		5	0			
t_{WSA}	Address Set-Up Time	5	0		10	0		15	0			
t_{WHA}	Address Hold Time	5	0		5	0		5	0			
t_{WSCS}	Chip Select Set-Up Time	5	0		5	0		5	0			
t_{WHCS}	Chip Select Hold Time	5	0		5	0		5	0			
C_I	Input Pin Capacitance		4	5		4	5		4	5	pF	Measure with Pulse Technique
C_O	Output Pin Capacitance		7	8		7	8		7	8		

AC CHARACTERISTICS: Over Guaranteed Operating Ranges. Notes 1, 2, 4, 5, 6

SYMBOL	CHARACTERISTIC	93L415/25XC			93L415/25XM			UNITS	CONDITIONS
		MIN	TYP (Note 3)	MAX	MIN	TYP (Note 3)	MAX		
READ MODE	DELAY TIMES								
t_{ACS}	Chip Select Access Time		20	40		20	45		See Test Circuit
t_{ZRCS}	Chip Select to HIGH Z		20	40		20	50	ns	and Waveforms
t_{AA}	Address Access Time		35	60		35	70		
WRITE MODE	DELAY TIMES								
t_{ZWS}	Write Disable to HIGH Z		20	45		20	45		
t_{WR}	Write Recovery Time		20	45		20	55		
	INPUT TIMING REQUIREMENTS								
t_W	Write Pulse Width (to guarantee write)	45	25		50	25		ns	See Test Circuit and Waveforms
t_{WSD}	Data Set-Up Time Prior to Write	5	0		10	0			
t_{WHD}	Data Hold Time After Write	5	0		10	0			
t_{WSA}	Address Set-Up Time	10	0		10	0			
t_{WHA}	Address Hold Time	5	0		10	0			
t_{WSCS}	Chip Select Set-Up Time	5	0		10	0			
t_{WHCS}	Chip Select Hold Time	5	0		10	0			
C_I	Input Pin Capacitance		4	5		4	5	pF	
C_O	Output Pin Capacitance		7	8		7	8		

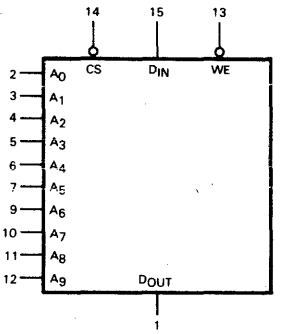
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ECL ISOPLANAR MEMORY
F10415 / F10415A / F100415
1024 x 1-BIT FULLY DECODED RANDOM ACCESS MEMORIES

GENERAL DESCRIPTION — These devices are 1024-bit Read/Write Random Access Memories organized 1024 words by one bit. They are designed for high speed scratch pad, control and buffer storage applications. Both include full address decoding on the chip, have separate Data In and non-inverted Data Out lines, and active LOW Chip Select lines.

- **TYPICAL READ ACCESS TIME**
  F10415 – 25 ns
  F10415A and F100415 – 12 ns
- **TYPICAL CHIP SELECT ACCESS TIME**
  F10415 – 7 ns
  F10415A and 100415 – 5 ns
- **ORGANIZED 1024 WORDS X 1 BIT**
- **OPEN EMITTER OUTPUT FOR EASE OF MEMORY EXPANSION**
- **POWER DISSIPATION: 0.5m W/BIT**
- **F10415/10415 COMPATIBLE WITH F10K AND UNCOMPENSATED 10K ECL LOGIC**
- **F100415 COMPATIBLE WITH F100K AND F95K ECL LOGIC**

LOGIC SYMBOL



V_{CC} = Pin 16
V_{EE} = Pin 8

PIN NAMES

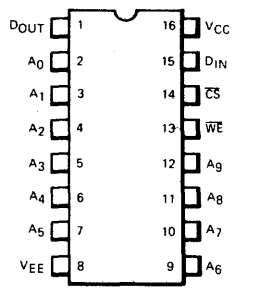
$\overline{CS}$	Chip Select Input
A_0 to A_9	Address Inputs
D_{IN}	Data Input
D_{OUT}	Data Output
$\overline{WE}$	Write Enable Input

TABLE 1 – TRUTH TABLE

INPUTS			OUTPUT	MODE
$\overline{CS}$	$\overline{WE}$	D_{IN}	OPEN EMITTER	
H	X	X	L	NOT SELECTED
L	L	L	L	WRITE "0"
L	L	H	L	WRITE "1"
L	H	X	D_{OUT}	READ

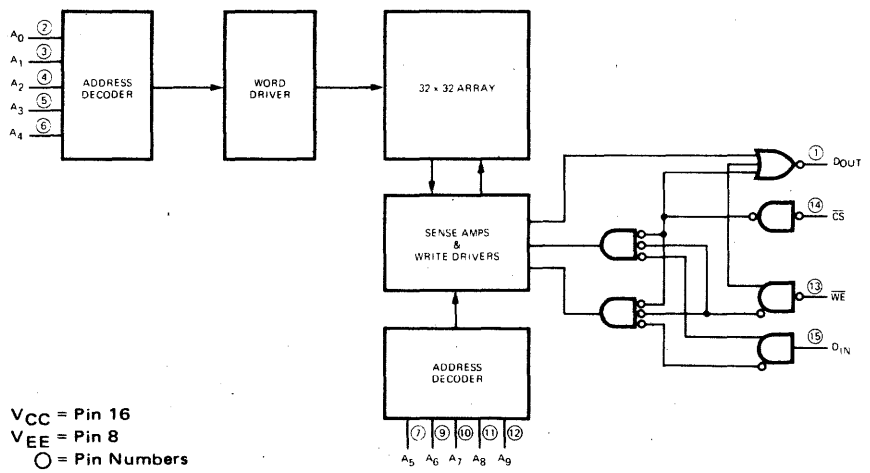
L = LOW Voltage Levels = −1.7 V
H = HIGH Voltage Levels = −0.9 V
(Nominal values)
X = Don't Care

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

LOGIC DIAGRAM



V_{CC} = Pin 16
V_{EE} = Pin 8
○ = Pin Numbers

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464 ELLIS STREET, MOUNTAIN VIEW, CALIFORNIA, 94042 (415) 962-5011/TWX 910-379-6435

FAIRCHILD

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FUNCTIONAL DESCRIPTION – The F10415, F10415A and F100415 are fully decoded 1024-bit Read/Write Random Access Memories organized 1024 words by one bit. Bit selection is acheived by means of a 10-bit address, A_0 to A_9. One Chip Select input is provided for memory array expansion up to 2048 words without the need for external decoding. For larger memories, the fast chip select access time permits the decoding of Chip Select ($\overline{CS}$) from the address without increasing address access time. The read and write operations are controlled by the state of the active LOW Write Enable ($\overline{WE}$). With $\overline{WE}$ and $\overline{CS}$ held LOW, the data at D_{in} is written into the addressed location. To read, $\overline{WE}$ is held HIGH and $\overline{CS}$ held LOW. Data in the specified location is presented at D_{OUT} and is non-inverted.

An unterminated emitter-follower output is provided to allow maximum flexibility in output connection. In many applications such as memory expansion, the outputs of many F10415s, F10415As or 100415s can be tied together. In other applications the wired-OR is not used. In either case an external 50 Ω pull down resistor to –2 V or an equivalent network must be used to provide a LOW at the output when it is off.

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	–65°C to +150°C
Temperature (Ambient) Under Bias	–55°C to +125°C
V_{EE} Pin Potential to Ground Pin	–7.0 V to +0.5 V
Input Voltage (dc)	V_{EE} to +0.5 V
Output Current (dc Output HIGH)	–30 mA to +0.1 mA

GUARANTEED OPERATING RANGES

PART NUMBER	SUPPLY VOLTAGE (V_{EE})			AMBIENT TEMPERATURE
	MIN	TYP	MAX	See Note 4
F10415DC, F10415ADC	–5.46 V	–5.2 V	–4.94 V	0°C to 75°C
F100415DC	–5.7 V	–4.5 V	–4.2 V	0°C to 85°C

10415 and 10415A Only
DC CHARACTERISTICS: V_{EE} = –5.2 V, Output Load = 50 Ω and 30 pF to –2.0 V, T_A = 0°C to 75°C (Note 4)

SYMBOL	CHARACTERISTIC	B LIMIT	TYP (Note 3)	A LIMIT	UNITS	T_A	CONDITIONS	
V_{OH}	Output Voltage HIGH	–1000		–840	mV	0°C	$V_{IN} = V_{IHA}$ or V_{ILB}	
		–960		–810		+25°C		
		–900		–720		+75°C		
V_{OL}	Output Voltage LOW	–1870		–1665	mV	0°C		
		–1850		–1650		+25°C		
		–1830		–1625		+75°C		Loading is 50 Ω to –2.0 V
V_{OHC}	Output Voltage HIGH	–1020			mV	0°C	$V_{IN} = V_{IHB}$ or V_{ILA}	
		–980				+25°C		
		–920				+75°C		
V_{OLC}	Output Voltage LOW			–1645	mV	0°C		
				–1630		+25°C		
				–1605		+75°C		
V_{IH}	Input Voltage HIGH	–1145		–840	mV	0°C	Guaranteed Input Voltage HIGH for All Inputs	
		–1105		–810		+25°C		
		–1045		–720		+75°C		
V_{IL}	Input Voltage LOW	–1870		–1490	mV	0°C	Guaranteed Input Voltage LOW for All Inputs	
		–1850		–1475		+25°C		
		–1830		–1450		+75°C		
I_{IH}	Input Current HIGH			220	μA	0 to +75°C	$V_{IN} = V_{IHA}$	
I_{IL}	Input Current LOW, $\overline{CS}$	0.5		170	μA	+25°C	$V_{IN} = V_{ILB}$	
	All others	–50						
I_{EE}	Power Supply Current		–90		mA	+75°C	All Inputs and Outputs Open	
	(Pin 8)	–150	–105			0°C		

NOTES:
1. Conditions for testing, not shown in the tables are chosen to guarantee operation under "worst case" conditions.
2. The specified Limits represent the "worst case" value for the parameter. Since these "worst case" values normally occur at the temperature extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
3. Typical values are at V_{EE} = –5.2V for F10415/10415A, V_{EE} = –4.5V for F100415, T_A = 25°C and maximum loading.
4. Guaranteed with transverse air flow exceeding 400 linear F.P.M. and 2-minute warm-up period. Typical resistance values of the package are:
   θ_{JA} (Junction to Ambient) = 90°C/Watt (still air)
   θ_{JA} (Junction to Ambient) = 50°C/Watt (at 400 F.P.M. air flow)
   θ_{JC} (Junction to Case) = 25°C/Watt
5. The maximum address access time is guaranteed to be the worst case bit in the memory using a pseudorandom testing pattern.
6. DEFINITION OF SYMBOLS AND TERMS USED IN THIS DATA SHEET:
   The symbols and terms used in this data sheet have been chosen to agree with the latest standards of the Electronics Industries Association and the International Electrotechnical Commission. The relative values of the specified conditions and limits will be referenced to an algebraic scale. The extremities of the scale are: "A" the value closest to positive infinity, "B" the value closest to negative infinity.

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100415 Only

DC CHARACTERISTICS: V_{EE} = −4.5V, V_{CC} = GND, T_A = 0°C to +85°C (Note A)

SYMBOL	CHARACTERISTIC	LIMITS (Note 6) B	LIMITS (Note 6) TYP (Note 3)	LIMITS (Note 6) A	UNITS	CONDITIONS	
V_{OH}	Output Voltage HIGH	−1025	−955	−880	mV	V_{IN} = V_{IHA} or V_{ILB}	Loading is 50 Ω to −2.0 V
V_{OL}	Output Voltage LOW	−1810	−1705	−1620	mV		
V_{OHC}	Output Voltage HIGH	−1035			mV	V_{IN} = V_{IHB} or V_{ILA}	
V_{OLC}	Output Voltage LOW			−1610	mV		
V_{IH}	Input Voltage HIGH	−1165		−880	mV	Guaranteed HIGH Signal for All Inputs	
V_{IL}	Input Voltage LOW	−1810		−1475	mV	Guaranteed LOW Signal for All Inputs	
I_{IH}	Input Current HIGH			220	μA	V_{IN} = V_{IHA}	
I_{IL}	Input Current LOW, $\overline{CS}$ All others	0.5 −50		170	μA	V_{IN} = V_{ILB}	
I_{EE}	Power Supply Current	−150	−105		mA	All Inputs and Output open	

AC CHARACTERISTICS: V_{EE} = −5.2 V ± 5%, Output Load = 50 Ω, 30 pF to −2.0 V, T_A = 0°C to 75°C

SYMBOL	PARAMETER	F10415ADC/100415 MIN	F10415ADC/100415 TYP (Note 3)	F10415ADC/100415 MAX	F10415DC MIN	F10415DC TYP (Note 3)	F10415DC MAX	UNITS	CONDITIONS
READ MODE									Fig 1a & b measured at
t_{ACS}	Chip Select Access Time		5			7	10	ns	50 % of inpur to valid
t_{RCS}	Chip Select Recovery Time		5			7	10	ns	output (V_{ILA} for V_{OL}
t_{AA}	Address Access Time		12	20		25	35	ns	or V_{IHB} for V_{OH})
WRITE MODE									
t_W	Write Pulse Width (to Guarantee writing)	12	9		25	20		ns	F10415A t_{WSA} = 8 ns; F10415 t_{WSA} = 20 ns
t_{WSD}	Data Set-up Time Prior to Write		0		5	0		ns	
t_{WHD}	Data Hold Time After Write		0		5	0			
t_{WSA}	Address Set-up Time Prior to Write		5		8	5		ns	F10415A t_W = 12 ns; F10415 t_W = 25 ns
t_{WHA}	Address Hold Time After Write		0		4	1		ns	
t_{WSCS}	Chip Select Set-up Time Prior to Write		0		5	0		ns	Fig. 2 measured at 50 % of input to valid output (V_{ILA} for V_{OL} or V_{IHB} for V_{OH})
t_{WHCS}	Chip Select Hold Time After Write		0		5	0		ns	
t_{WS}	Write Disable Time		5			7	10	ns	
t_{WR}	Write Recovery Time		7			7	10	ns	
RISE TIME AND FALL TIME - 10415/10415A ONLY									
t_r	Output Rise Time		5			5		ns	Measured between 20 % and 80 % points. (Fig. 1a)
t_f	Output Fall Time		5			5		ns	
RISE TIME AND FALL TIME - 100415 Only									
t_r	Output Rise Time		4.5					ns	
t_f	Output Fall Time		5.5					ns	
CAPACITANCE									
C_{IN}	Input Pin Capacitance		4	5		4	5	pF	Measure with a Pulse
C_{OUT}	Output Pin Capacitance		7	8		7	8	pF	Technique

*Note: The F10415A Ac limits are preliminary

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93422 • 93L422

TTL ISOPLANAR MEMORY

256 x 4-BIT FULLY DECODED RANDOM ACCESS MEMORY

DESCRIPTION - The 93422 and 93L422 are 1024-bit Read/Write Access Memories organized 256 words by four bits per words by four bits per word. The devices 3-state outputs, and is designed primarily for buffer control storage and high performance main memory applications.

- **ISOPLANAR TECHNOLOGY**
- **ORGANIZED — 256 WORDS X 4 BITS**
- **3-STATE OUTPUTS**
- **STANDARD 22-PIN DUAL & IN-LINE PACKAGE**
- **TWO CHIP SELECT INPUTS PROVIDE EASY MEMORY EXPANSION**
- **POWER DISSIPATION: 93L422 .027m W/BIT 93422 .045m W/BIT**

TYPICAL READ ACCESS TIME: 93L422 — 45ns 93422 — 30ns

PIN NAMES

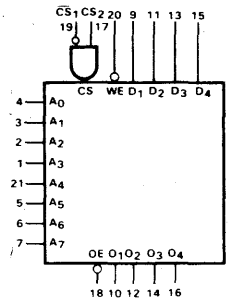
$A_0 - A_7$	Address Inputs
$D_1 - D_4$	Data Inputs
$\overline{CS}_1$, CS_2	Chip Select Inputs
$\overline{WE}$	Write Enable Input
$O_1 - O_4$	Data Outputs
$\overline{O}_E$	Output Enable

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +5.5 V
*Input Current (dc)	−12 mA to +5.0 mA
**Voltage Applied to Outputs (output HIGH)	−0.5 V to +5.50 V
Output Current (dc)	+20 mA

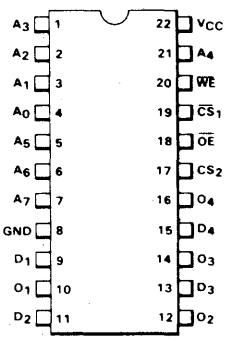
*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.
**Output Current Limit Required.

LOGIC SYMBOL

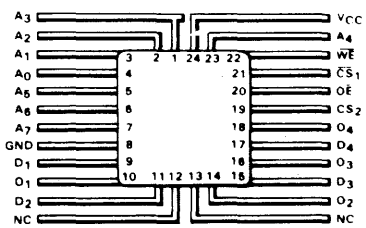


V_{CC} = Pin 22
GND = Pin 8

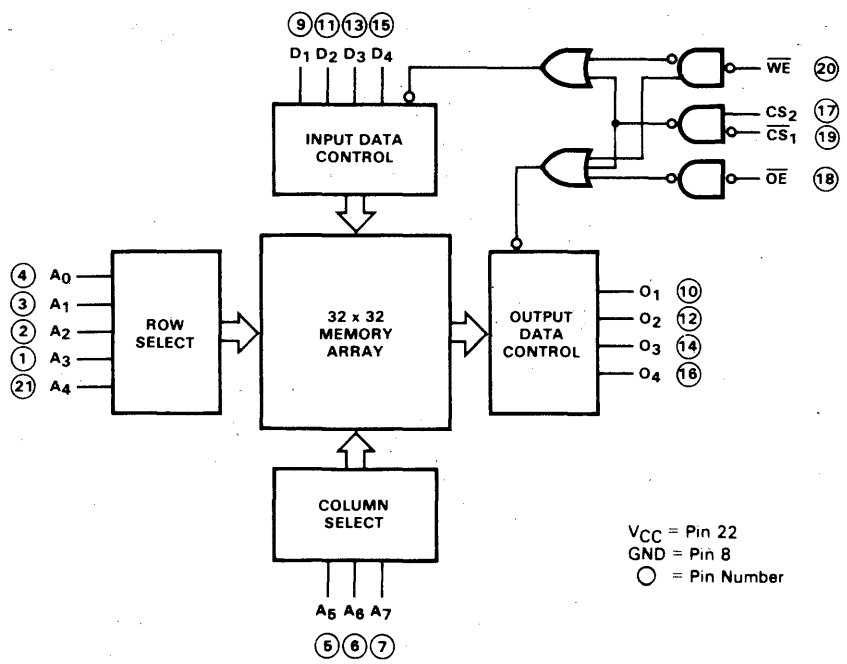
CONNECTION DIAGRAMS
DIP (TOP VIEW)



FLATPAK (TOP VIEW)



LOGIC DIAGRAM



V_{CC} = Pin 22
GND = Pin 8
○ = Pin Number

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FAIRCHILD

FUNCTIONAL DESCRIPTION – The 93422 is a fully decoded 1024-bit Random Access Memory organized 256 words by four bits. Word selection is achieved by means of an 8-bit address, A_0 thru A_7. Two Chip Select inputs are provided for logic flexibility. For larger memories, the fast chip select access time permits the decoding of Chip Select, CS, from the address without increasing address access time. The read and write operations are controlled by the state of the active LOW Write Enable, WE (pin 20). With WE held LOW and the chip selected, the data at D_{IN} is written into the addressed location. To read, WE is held HIGH and the chip selected. Data in the specified location is presented at D_{OUT}.

TRUTH TABLE

INPUTS					OUTPUTS	
$\overline{OE}$ PIN 18	$\overline{CS_1}$ PIN 19	CS_2 PIN 17	$\overline{WE}$ PIN 20	$D_1 - D_4$ PINS 9, 11,13, 15	93422 3-STATE	MODE
X	H	X	X	X	HIGH Z	Not Selected
X	X	L	X	X	HIGH Z	Not Selected
L	L	H	H	X	$O_1 - O_4$	Read Stored Data
X	L	H	L	L	HIGH Z	Write "0"
X	L	H	L	H	HIGH Z	Write "1"
H	L	H	H	X	HIGH Z	Output Disabled
H	L	H	L	L	HIGH Z	Write "0" (Output Disabled)
H	L	H	L	H	HIGH Z	Write "1" (Output Disabled)

H = HIGH Voltage, L = LOW Voltage, X = Don't Care (HIGH or LOW), HIGH Z = High Impedance

GUARANTEED OPERATING RANGES

PART NUMBER	SUPPLY VOLTAGE (V_{CC})			AMBIENT TEMPERATURE Note 4
	MIN	TYP	MAX	
93422XC, 93L422XC	4.75 V	5.0 V	5.25 V	0°C to +75°C
93422XM, 93L422XM	4.5 V	5.0 V	5.5 V	−55°C to +125°C

X=package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS: Over Operating Temperature Ranges (Notes 1, 2, 4)

SYMBOL	CHARACTERISTIC		LIMITS MIN	LIMITS TYP (Note 3)	LIMITS MAX	UNITS	CONDITIONS	
V_{OL}	Output LOW Voltage			0.3	0.45	V	V_{CC} = MIN, I_{OL} = 8 mA	
V_{IH}	Input HIGH Voltage		2.1	1.6		V	Guaranteed Input HIGH Voltage for all Inputs	
V_{IL}	Input LOW Voltage			1.5	0.8	V	Guaranteed Input LOW Voltage for all Inputs	
I_{IL}	Input LOW Current			−150	−300	μA	V_{CC} = MAX, V_{IN} = 0.4 V	
I_{IH}	Input HIGH Current			1.0	40	μA	V_{CC} = MAX, V_{IN} = 4.5 V	
					1.0	mA	V_{CC} = MAX, V_{IN} = 5.25 V	
V_{CD}	Input Diode Clamp Voltage			−10	−1.5	V	V_{CC} = MAX, IN = −10 mA	
I_{OFF}	Output Current (HIGH Z)				50	μA	V_{CC} = MAX, V_{OUT} = 2.4 V	
					−50		V_{CC} = MAX, V_{OUT} = 0.5 V	
V_{OH}	Output HIGH Voltage		2.4			V	V_{CC} = MIN, I_{OH} = −5.2 mA	
I_{OS}	Output Current Short Circuit to Ground				−70	mA	V_{CC} = MAX, Note 7	
I_{CC}	Power Supply Current	93422XC		95	130	mA	T_A = +75°C	V_{CC} = MAX, All Inputs and Outputs Open
		93422XC			155		T_A = 0°C	
		93422XM			120		T_A = +125°C	
		93422XM			170		T_A = −55°C	
I_{CC}	Power Supply Current	93L422XC		55	75	mA	T_A = +75°C	
		93L422XC		60	80		T_A = 0°C	
		93L422XM		50	70		T_A = +125°C	
		93L422XM		65	90		T_A = −55°C	

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93422 AC CHARACTERISTICS: Over Guaranteed Operating Ranges (Notes 1, 2, 4, 5, 6)

SYMBOL	CHARACTERISTIC	93422XC			93422XM			UNITS	CONDITIONS
		MIN	TYP (Note 3)	MAX	MIN	TYP (Note 3)	MAX		
READ MODE	DELAY TIMES								
t_{ACS}	Chip Select Time		20	30		20	45		
t_{ZRCS}	Chip Select to HIGH Z		20	30		20	45	ns	See Test Circuit
t_{AOS}	Output Enable Time		20	30		20	45		and Waveforms
t_{ZROS}	Output Enable to HIGH Z		20	30		20	45		
t_{AA}	Address Access Time		30	45		40	60		
WRITE MODE	DELAY TIMES								
t_{ZWS}	Write Disable to HIGH Z		20	35		20	45	ns	
t_{WR}	Write Recovery Time		25	40		25	50		
	INPUT TIMING REQUIREMENTS								See Test Circuit
t_W	Write Pulse Width (to guarantee write)	30	20		40	30			and Waveforms
t_{WSD}	Data Set-Up Time Prior to Write	5	0		5	0			
t_{WHD}	Data Hold Time After Write	5	0		5	0			
t_{WSA}	Address Set-Up Time	10	0		10	0		ns	
t_{WHA}	Address Hold Time	5	0		10	0			
t_{WSCS}	Chip Select Set-Up Time	5	0		5	0			
t_{WHCS}	Chip Select Hold Time	5	0		10	0			
C_I	Input Pin Capacitance		3	5		3	5	pF	Measure with
C_O	Output Pin Capacitance		5	8		5	8		Pulse Technique

93L422 AC CHARACTERISTICS: Over Guaranteed Operating Ranges (Notes 1, 2, 4, 5, 6)

SYMBOL	CHARACTERISTIC	93L422XC*			93L422XM			UNITS	CONDITIONS
		MIN	TYP (Note 3)	MAX	MIN	TYP (Note 3)	MAX		
READ MODE	DELAY TIMES								
t_{ACS}	Chip Select Time		20	35		20	45		
t_{ZRCS}	Chip Select to HIGH Z		20	35		20	45	ns	See Test Circuit
t_{AOS}	Output Enable Time		20	35		20	45		and Waveforms
t_{ZROS}	Output Enable to HIGH Z		20	35		20	45		
t_{AA}	Address Access Time		45	60		45	75		
WRITE MODE	DELAY TIMES								
t_{ZWS}	Write Disable to HIGH Z		20	40		20	45	ns	
t_{WR}	Write Recovery Time		25	45		25	50		
	INPUT TIMING REQUIREMENTS								See Test Circuit
t_W	Write Pulse Width (to guarantee write)	45	30		55	35			and Waveforms
t_{WSD}	Data Set-Up Time Prior to Write	5	0		5	0			
t_{WHD}	Data Hold Time After Write	5	0		5	0			
t_{WSA}	Address Set-Up Time	10	0		10	0		ns	
t_{WHA}	Address Hold Time	5	0		10	0			
t_{WSCS}	Chip Select Set-Up Time	5	0		5	0			
t_{WHCS}	Chip Select Hold Time	5	0		10	0			
C_I	Input Pin Capacitance		3	5		3	5	pF	Measure with
C_O	Output Pin Capacitance		5	8		5	8		Pulse Technique

NOTES:

1. Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
2. The specified LIMITS represents the "worst case" value for the parameters. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
3. Typical values are at V_{CC} = 5.0 V, T_A = +25°C, and MAX loading.
4. The Temperature Ranges are guaranteed with transverse air flow exceeding 400 linear feet per minute. For military range an additional requirement of a two minute warm-up. Temperature range of operation refers to case temperature for Flatpaks and ambient temperature for all other packages. Typical thermal resistance values of the package at maximum temperature are:
   θ_{JA} (Junction to Ambient) (at 400 fpm air flow) = 50°C/Watt, Ceramic DIP; 65°C/Watt, Plastic DIP; NA, Flatpak.
   θ_{JA} (Junction to Ambient) (still air) = 90°C/Watt, Ceramic DIP; 110°C/Watt, Plastic DIP; NA, Flatpak.
   θ_{JC} (Junction to Case) = 25°C/Watt, Ceramic DIP; 25°C/Watt, Plastic DIP; 10°C/Watt, Flatpak.
5. The MAX address access time is guaranteed to be the "worst case" bit in the memory using a pseudo random testing pattern.
6. t_W measured at t_{WSA} = MIN, t_{WSA} measured at t_W = MIN.
7. Duration of short circuit should not exceed one second.

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93421/93421A • 93L420 • 93L421

TTL ISOPLANAR MEMORY

256 x 1-BIT FULLY DECODED RANDOM ACCESS MEMORY

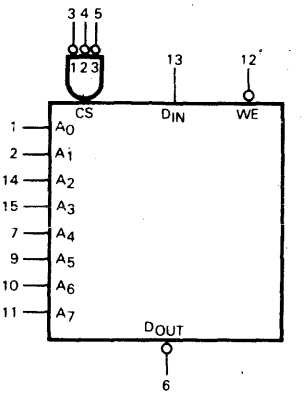
DESCRIPTION — These devices are high speed 256-bit TTL Random Access Memories with full decoding on chip. They are organized 256 words by one bit and are designed for scratchpad, buffer and distributed main memory applications. The devices have three Chip Select lines to simplify their use in larger memory systems. Address input pin locations are specifically chosen to permit maximum packaging density and for ease of PC board layout. A 3-state output is provided to drive bus organized systems and/or highly capacitive loads. The 93L420 and 93L421 are appropriate for systems requiring low power.

- **3-STATE OUTPUT**
- **REPLACEMENT FOR 54/74S200 AND EQUIVALENT DEVICES**
- **ORGANIZATION — 256 WORDS x 1 BIT**
- **THREE HIGH SPEED CHIP SELECT INPUTS**
- **TYPICAL READ ACCESS TIME**

93421A	Commercial	30 ns	93L420	40 ns
93421	Commercial	35 ns	93L421	45 ns
93421	Military	35 ns		

- **ON CHIP DECODING**
- **POWER DISSIPATION — 1.8 mW/BIT — 93421 AND 93421A**
- **POWER DISSIPATION — 250 mW TYP — 93L420, 93L421**
- **POWER DISSIPATION DECREASES WITH TEMPERATURE**
- **INVERTED DATA OUTPUT**

LOGIC SYMBOL

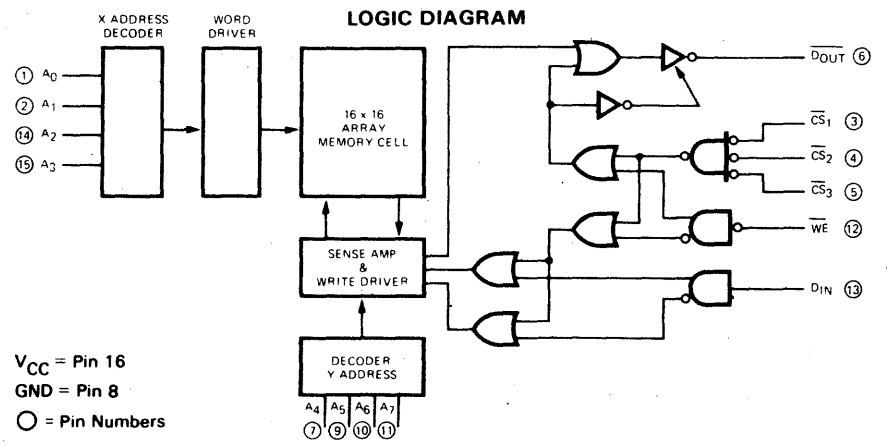


V_{CC} Pin 16
GND Pin 8

PIN NAMES		LOADING (Notes a, b)
$\overline{CS}_1$, $\overline{CS}_2$, $\overline{CS}_3$	Chip Select Inputs	0.5 U.L.
$A_0 - A_7$	Address Inputs	0.5 U.L.
D_{IN}	Data Input	0.5 U.L.
$\overline{D_{OUT}}$	Data Output	10 U.L.
$\overline{WE}$	Write Enable	0.5 U.L.

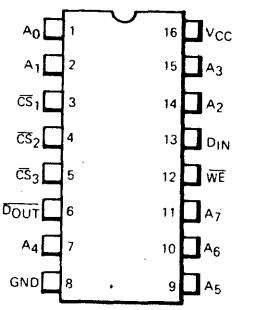
NOTES:
a. 1 Unit Load (U.L.) = 40 μA HIGH / 1.6 mA LOW
b. 10 U.L. is the output LOW drive factor. This output will sink a maximum of 16 mA at V_{OUT} = 0.45 V, and will source a minimum of 10 mA at 2.4 V.

LOGIC DIAGRAM



V_{CC} = Pin 16
GND = Pin 8
○ = Pin Numbers

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

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MEMORY

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FUNCTIONAL DESCRIPTION — These devices are fully decoded 256-bit Random Access Memory organized 256 words by one bit. Word selection is achieved by means of an 8-bit address, A_0 thru A_7.

Three Chip Select inputs are provided for logic flexibility. For larger memories, the fast chip select access time permits the decoding of Chip Select, $\overline{CS}$, from the address without increasing address access time.

The read and write operations are controlled by the state of the active LOW Write Enable ($\overline{WE}$, pin 12). With $\overline{WE}$ held LOW and the chip selected, the data at D_{IN} is written into the addressed location. To read, $\overline{WE}$ is held HIGH and the chip selected. Data in the specified location is presented at $\overline{D_{OUT}}$.

The 3-state output provides drive capability for higher speeds with high capacitive load systems. The third state (high impedance) allows bus organized systems where multiple outputs are connected to a common bus.

During writing, the output is held in the high impedance state.

TABLE I – TRUTH TABLE

INPUTS					OUTPUT	
$\overline{CS}_1$	$\overline{CS}_2$	$\overline{CS}_3$	$\overline{WE}$	D_{IN}	$\overline{D_{OUT}}$	MODE
H	X	X	X	X	HIGH Z	Not Selected
X	H	X	X	X	HIGH Z	Not Selected
X	X	H	X	X	HIGH Z	Not Selected
L	L	L	L	L	HIGH Z	Write "0"
L	L	L	L	H	HIGH Z	Write "1"
L	L	L	H	X	$\overline{D_{OUT}}$	Read inverted data from addressed location

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care (HIGH or LOW)
HIGH Z = HIGH Impedance

TABLE 2 – FUNCTION TABLE

FUNCTION	INPUTS		OUTPUT
	CHIP SELECT	WRITE ENABLE	
Write	L	L	HIGH Z
Read	L	H	$\overline{\text{Stored Data}}$
Not Selected	H	X	HIGH Z

ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +5.5 V
*Input Current (dc)	−12 mA to +5.0 mA
**Voltage Applied to Outputs (output HIGH)	−0.5 V to +5.50 V
Output Current (dc) (output LOW)	+20 mA

*Either Input Voltage limit or Input Current limit is sufficient to protect the inputs.
**Output Current Limit Required.

GUARANTEED OPERATING RANGES

PART NUMBER	SUPPLY VOLTAGE (V_{CC})			AMBIENT TEMPERATURE Note 4
	MIN	TYP	MAX	
93420XC/93421AXC 93L420XC/93L421XC	4.75 V	5.0 V	5.25 V	0° C to +75° C
93L420XM/93L421XM 93421XM	4.50 V	5.0 V	5.50 V	-55° C to +125° C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

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DC CHARACTERISTICS: Over Operating Temperature Ranges. Notes 1, 2 and 4

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP (Note 3)	LIMITS MAX	UNITS	CONDITIONS
V_{OL}	Output LOW Voltage			0.3	0.45	V	V_{CC} = MIN, I_{OL} = 16 mA
V_{IH}	Input HIGH Voltage		2.0	1.6		V	Guaranteed Input Logical HIGH Voltage for all Inputs
V_{IL}	Input LOW Voltage			1.5	0.85	V	Guaranteed Input Logical LOW Voltage for all Inputs
I_{IL}	Input LOW Current			−530	−800	μA	V_{CC} = MAX, V_{IN} = 0 V
I_{IH}	Input HIGH Current			1.0	20	μA	V_{CC} = MAX, V_{IN} = 4.5 V
I_{OFF}	Output Current (HIGH Z)				50 −50	μA	V_{CC} = MAX, V_{OUT} = 2.4 V V_{CC} = MAX, V_{OUT} = 0.5 V
V_{CD}	Input Clamp Diode Voltage			−1.0	−1.5	V	V_{CC} = MAX, I_{IN} = −10 mA
I_{CC}	Power Supply Current	93421XC		90	124	mA	T_A = +75°C; V_{CC} = MAX, WE Grounded, all other inputs @ 4.5 V, see Power Supply vs Temp. Curve
		93421AXC		100	135		T_A = 0°C
		93421XM		90	117		T_A = +125°C
				100	143		T_A = −55°C
V_{OH}	Output HIGH Voltage	93421XC,AXC	2.4			V	I_{OH} = −10.3 mA
		93421XM	2.4			V	I_{OH} = −5.2 mA
I_{OS}	Output Current Short Circuit to Ground				−100	mA	V_{CC} = MAX, Note 7

AC CHARACTERISTICS: Over Guaranteed Operating Ranges. Notes 1, 2, 4, 5, 6 **93421/93421A ONLY**

SYMBOL	CHARACTERISTIC	93421AXC MIN	93421AXC TYP (Note 3)	93421AXC MAX	93421XC MIN	93421XC TYP (Note 3)	93421XC MAX	93421XM MIN	93421XM TYP (Note 3)	93421XM MAX	UNITS	CONDITIONS
READ MODE	DELAY TIMES											
t_{ACS}	Chip Select Access Time		20	30		20	30		25	40		See Test Circuit
t_{ZRCS}	Chip Select to HIGH Z		20	30		20	30		20	40	ns	and Waveforms
t_{AA}	Address Access Time		30	40		35	50		35	60		Note 5
WRITE MODE	DELAY TIMES											
t_{ZWS}	Write Disable to HIGH Z	10	20	35	10	20	35	10	20	45	ns	
t_{WR}	Write Recovery Time		25	40		25	40		25	50		
	INPUT TIMING REQUIREMENTS											
t_W	Minimum Write Pulse Width	30	10		30	10		40	10			See Test Circuit
t_{WSD}	Data Set-Up Time Prior to Write	0	0		0	0		0	0			and Waveforms
t_{WHD}	Data Hold Time After Write	5	0		5	0		5	0			Note 6
t_{WSA}	Address Set-Up Time	0	0		0	0		0	0		ns	
t_{WHA}	Address Hold Time	5	0		5	0		5	0			
t_{WSCS}	Chip Select Set-Up Time	0	0		0	0		0	0			
t_{WHCS}	Chip Select Hold Time	5	0		5	0		5	0			
C_I	Input Capacitance		2.5	3.5		2.5	3.5		2.5	3.5	pF	Measured with
C_O	Output Capacitance		5	7		5	7		5	7		pulse technique

NOTES:

1. Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
2. The specified LIMITS represents the "worst case" value for the parameters. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
3. Typical values are at V_{CC} = 5.0 V, T_A = 25°C, and MAX loading.
4. The Temperature Ranges are guaranteed with transverse air flow exceeding 400 linear feet per minute. For military range an additional requirement of a two minute warm-up. Temperature range of operation refers to case temperature for Flatpaks and ambient temperature for all other packages. Typical thermal resistance values of the package at maximum temperature are

   θ_{JA} (Junction to Ambient) (at 400 fpm air flow) = 50°C/Watt, Ceramic DIP; 65°C/Watt, Plastic DIP; NA, Flatpak.
   θ_{JA} (Junction to Ambient) (still air) = 90°C/Watt, Ceramic DIP; 110°C/Watt, Plastic DIP; NA, Flatpak.
   θ_{JC} (Junction to Case) = 25°C/Watt, Ceramic DIP; 25°C/Watt, Plastic DIP; 10°C/Watt, Flatpak.

5. The MAX address access time is guaranteed to be the "worst case" bit in the memory using a pseudo random testing pattern.
6. t_W measured at t_{WSA} = MIN, t_{WSA} measured at t_W = MIN.
7. Duration of short circuit should not exceed one second.

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TTL ISOPLANAR MEMORY 93419

64×9-BIT FULLY DECODED RANDOM ACCESS MEMORY

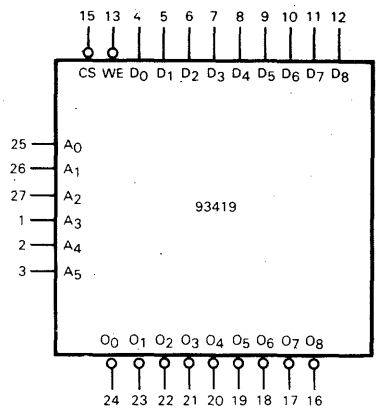
DESCRIPTION – The 93419 is a 576-bit Read/Write Random Access Memory organized 64 words by nine bits per word with uncommitted collector outputs. It is ideally suited for scratchpad, small buffer and other applications where the number of required words is small and where the number of required bits per word is relatively large. The ninth bit can provide parity for 8-bit word systems.

- **UNCOMMITTED COLLECTOR OUTPUTS**
- **TTL INPUTS AND OUTPUTS**
- **ISOPLANAR TECHNOLOGY**
- **ORGANIZATION – 64 WORDS X 9 BITS**
- **STANDARD 28-PIN DUAL IN-LINE PACKAGE**
- **DATA OUTPUT IS THE COMPLEMENT OF DATA INPUT**
- **POWER DISSIPATION – 1.3 mW/BIT**

PIN NAMES

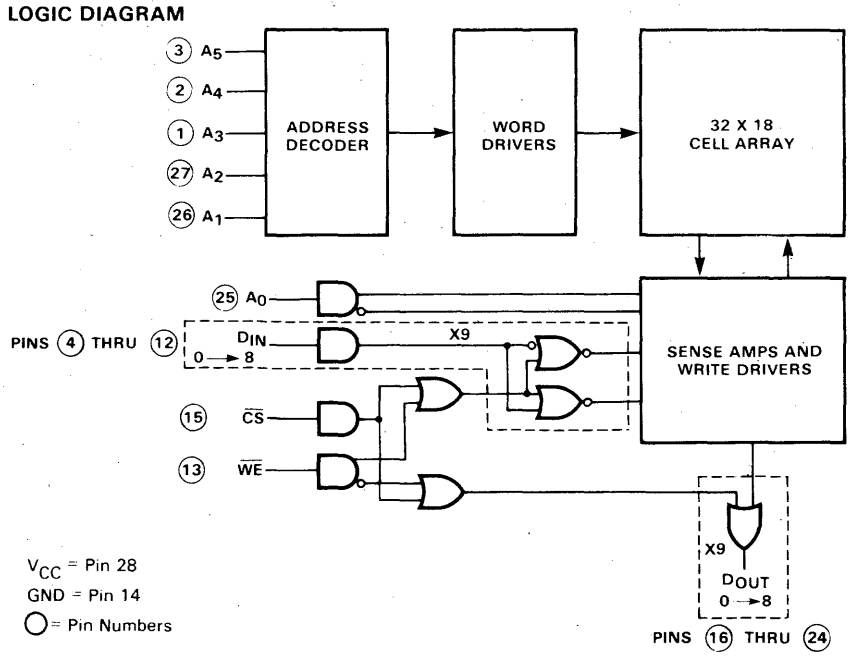
$A_0 - A_5$	Address Inputs
$D_0 - D_8$	Data Inputs
$\overline{O}_0 - \overline{O}_8$	Outputs
$\overline{WE}$	Write Enable Input
$\overline{CS}$	Chip Select Input

LOGIC SYMBOL



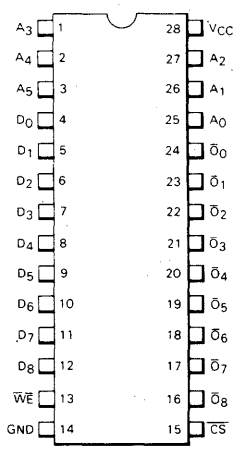
V_{CC} = Pin 28
GND = Pin 14

LOGIC DIAGRAM



V_{CC} = Pin 28
GND = Pin 14
◯ = Pin Numbers

CONNECTION DIAGRAM
DIP (TOP VIEW)



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FAIRCHILD

FUNCTIONAL DESCRIPTION – The 93419 is a fully decoded 576-bit Random Access Memory organized 64 words by nine bits. Word selection is achieved by means of a 6-bit address, A_0 to A_5.

The Chip Select input provides for memory array expansion. For large memories, the fast chip select access time permits the decoding of chip select ($\overline{CS}$) from the address without affecting system performance.

The read and write operations are controlled by the state of the active LOW Write Enable ($\overline{WE}$, pin 13). With $\overline{WE}$ held LOW and the chip selected, the data at D_{IN} is written into the addressed location. To read, $\overline{WE}$ is held HIGH and the chip selected. Data in the specified location is presented at $\overline{D_{OUT}}$ and is inverted from Data In to Data Out.

Uncommitted collector outputs are provided to allow maximum flexibility in output connection. In many applications such as memory expansion, the outputs of many 93419s can be tied together. In other applications the wired-OR is not used. In either case an external pull-up resistor of R_L value must be used to provide a HIGH at the output when it is off. Any R_L value within the range specified below may be used.

$$\frac{V_{CC(MAX)}}{I_{OL} - FO\ (1.6)} \leqslant R_L \leqslant \frac{V_{CC}\ (MIN) - V_{OH}}{n\ (I_{CEX}) + FO\ (0.04)}$$

R_L is in kΩ (limited to 8 mA)
n = number of wired-OR outputs tied together
FO = number of TTL Unit Loads (UL) driven
I_{CEX} = Memory Output Leakage Current
V_{OH} = Required Output HIGH Level at Output Node
I_{OL} = Output LOW Current

The minimum R_L value is limited by output current sinking ability. The maximum R_L value is determined by the output and input leakage current which must be supplied to hold the output at V_{OH}. One Unit Load = 40 μA HIGH/1.6 mA LOW. FO_{MAX} = 5 UL.

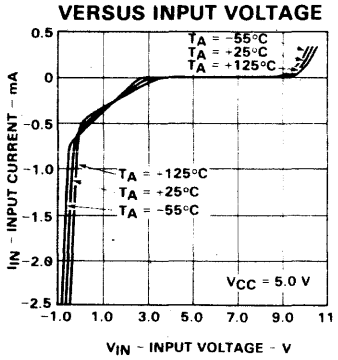
TABLE I – TRUTH TABLE

INPUTS			OUTPUT	MODE
$\overline{CS}$	$\overline{WE}$	D_{IN}	Open Collector	
H	X	X	H	NOT SELECTED
L	L	L	H	WRITE "0"*
L	L	H	H	WRITE "1"*
L	H	X	$\overline{D_{OUT}}$*	READ

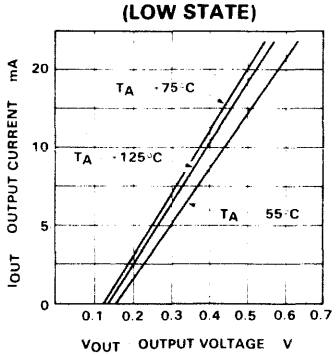
H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care (HIGH or LOW)
* Memory inverts from Data In to Data Output

TYPICAL INPUT AND OUTPUT CHARACTERISTICS

INPUT CURRENT VERSUS INPUT VOLTAGE



OUTPUT CURRENT VERSUS OUTPUT VOLTAGE (LOW STATE)



ABSOLUTE MAXIMUM RATINGS (above which the useful life may be impaired)

Storage Temperature	−65°C to +150°C
Temperature (Ambient) Under Bias	−55°C to +125°C
V_{CC} Pin Potential to Ground Pin	−0.5 V to +7.0 V
*Input Voltage (dc)	−0.5 V to +5.5 V
*Input Current (dc)	−12 mA to +5.0 mA
Voltage Applied to Outputs (Output HIGH)	−0.5 V to +5.5 V
Output Current (dc) (Output LOW)	+10 mA

*Either input voltage or input current limit is sufficient to protect the input.

GUARANTEED OPERATING RANGES

PART NUMBER	SUPPLY VOLTAGE (V_{CC})			AMBIENT TEMPERATURE (Note 4)
	MIN	TYP	MAX	
93419XC	4.75 V	5.0 V	5.25 V	0°C to +75°C
93419XM	4.50 V	5.0 V	5.50 V	−55°C to +125°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

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DC CHARACTERISTICS: Over Operating Temperature Ranges (Notes 1, 2 and 4)

SYMBOL	PARAMETER	LIMITS MIN	LIMITS TYP (Note 3)	LIMITS MAX	UNITS	CONDITIONS	
V_{OL}	Output LOW Voltage		0.3	0.50	V	V_{CC} = MIN, I_{OL} = 8 mA	
V_{IH}	Input HIGH Voltage	2.1	1.6		V	Guaranteed Input HIGH Voltage for all Inputs	
V_{IL}	Input LOW Voltage		1.5	0.8	V	Guaranteed Input LOW Voltage for all Inputs	
I_{IL}	Input LOW Current		−250	−400	μA	V_{CC} = MAX, V_{IN} = 0.4 V	
I_{IH}	Input HIGH Current		1.0	40	μA	V_{CC} = MAX, V_{IN} = 4.5 V	
				1.0	mA	V_{CC} = MAX, V_{IN} = 5.25 V	
I_{CEX}	Output Leakage Current		1.0	100	μA	V_{CC} = MAX, V_{OUT} = 4.5 V	
V_{CD}	Input Clamp Diode Voltage		−1.0	−1.5	V	V_{CC} = MAX, I_{IN} = −10 mA	
I_{CC}	Power Supply Current			165	mA	T_A = 125°C	V_{CC} = MAX, All Inputs Grounded Outputs LOW
			145	200	mA	T_A = 25°C	
				210	mA	T_A = −55°C	

AC CHARACTERISTICS: Over Guaranteed Operating Ranges (Notes 1, 2, 4, 5, 6)

SYMBOL	CHARACTERISTIC	93419XC MIN	93419XC TYP (Note 3)	93419XC MAX	93419XM MIN	93419XM TYP (Note 3)	93419XM MAX	UNITS	CONDITIONS
READ MODE	DELAY TIMES								
t_{ACS}	Chip Select Access Time		15	40		15	40		See Test Circuit
t_{RCS}	Chip Select Recovery Time		20	40		20	40	ns	and Waveforms
t_{AA}	Address Access Time		35	45		40	60		
WRITE MODE	DELAY TIMES								
t_{WS}	Write Disable Time		20	40		20	45	ns	
t_{WR}	Write Recovery Time		25	45		45	55		
	INPUT TIMING REQUIREMENTS								
t_W	Write Pulse Width (to guarantee write)	35	20		45	25			See Test Circuit and Waveforms
t_{WSD}	Data Set-Up Time Prior to Write	5	0		5	0			
t_{WHD}	Data Hold Time After Write	5	0		5	0			
t_{WSA}	Address Set-Up Time	5	0		10	0		ns	
t_{WHA}	Address Hold Time	5	0		5	0			
t_{WSCS}	Chip Select Set-Up Time	5	0		5	0			
t_{WHCS}	Chip Select Hold Time	5	0		5	0			
C_{IN}	Input Pin Capacitance		4	5		4	5	pF	
C_{OUT}	Output Pin Capacitance		7	8		7	8		

NOTES:

1. Conditions for testing, not shown in the Table, are chosen to guarantee operation under "worst case" conditions.
2. The specified LIMITS represents the "worst case" value for the parameters. Since these "worst case" values normally occur at the temperature and supply voltage extremes, additional noise immunity and guard banding can be achieved by decreasing the allowable system operating ranges.
3. Typical limits are at V_{CC} = 5.0 V, T_A = +25°C, and MAX loading.
4. The Temperature Ranges are guaranteed with transverse air flow exceeding 400 linear feet per minute. For military range an additional requirement of a two minute warm-up. Temperature range of operation refers to case temperature for Flatpaks and ambient temperature for all other packages. Typical thermal resistance values of the package at maximum temperature are:

   θ_{JA} (Junction to Ambient) (at 400 fpm air flow) = 50°C/Watt, Ceramic DIP; 65°CC/Watt, Plastic DIP; NA, Flatpak.
   θ_{JA} (Junction to Ambient) (still air) = 90°C/Watt, Ceramic DIP; 110°C/Watt, Plastic DIP; NA, Flatpak.
   θ_{JC} (Junction to Case) = 25°C/Watt, Ceramic DIP; 25°C/Watt, Plastic DIP; 10°C/Watt, Flatpak.

5. The MAX address access time is guaranteed to be the "worst case" bit in the memory using a pseudo random testing pattern.
6. t_W measured at t_{WSA} = MIN, t_{WSA} measured at t_W = MIN.

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93417•93427
ISOPLANAR SCHOTTKY TTL MEMORY
256×4-BIT PROGRAMMABLE READ ONLY MEMORY

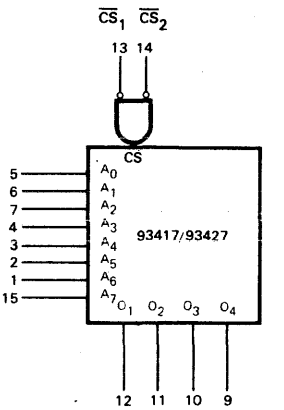
DESCRIPTION – The 93417 and 93427 are fully decoded high speed 1024-bit field Programmable ROMs organized 256 words by four bits per word. The devices are identical except for the output stage. The 93417 has uncommitted collector outputs, while the 93427 has 3-state outputs. In either case, the outputs are disabled when either $\overline{CS}_1$ or $\overline{CS}_2$ are in the HIGH state. The 93417 and 93427 are supplied with all bits stored as logic "1"s and can be programmed to logic "0"s by following the field programming procedure.

- **FULL MIL AND COMMERCIAL RANGES**
- **FIELD PROGRAMMABLE**
- **ORGANIZED 256 x 4 BITS PER WORD**
- **UNCOMMITTED COLLECTORS – 93417**
- **3-STATE OUTPUTS – 93427**
- **FULLY DECODED – ON-CHIP ADDRESS DECODER AND BUFFER**
- **CHIP SELECT INPUTS PROVIDE EASY MEMORY EXPANSION**
- **WIRED-OR CAPABILITY**
- **STANDARD 16-PIN DUAL IN-LINE PACKAGE**
- **NICHROME FUSE LINKS – FOR HIGH RELIABILITY**

PIN NAMES

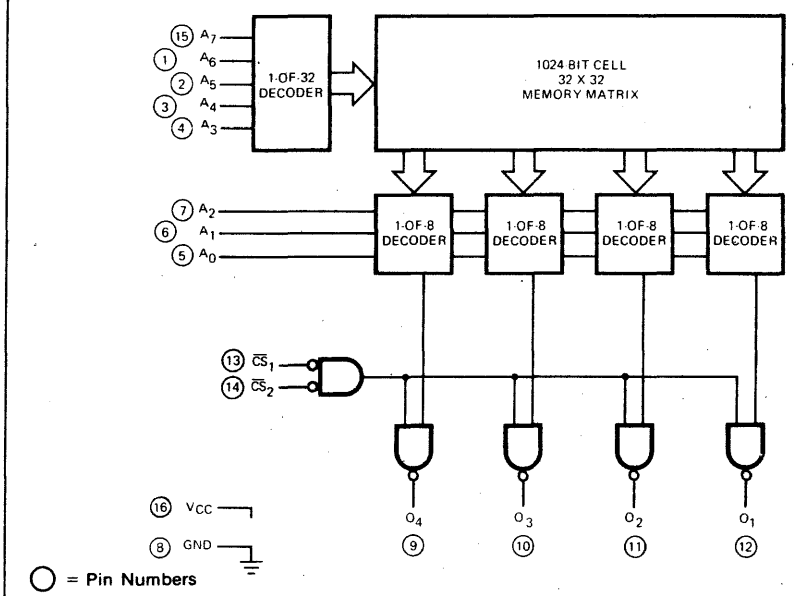
$A_0 - A_7$	Address Inputs
$\overline{CS}_1, \overline{CS}_2$	Chip Select Inputs (Active LOW)
$O_1 - O_4$	Data Outputs

LOGIC SYMBOL



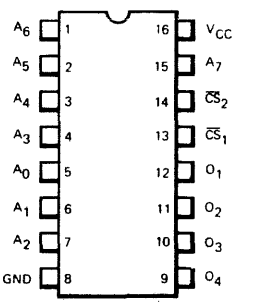
V_{CC} = Pin 16
GND = Pin 8

LOGIC DIAGRAM



○ = Pin Numbers

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

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MEMORY

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GUARANTEED OPERATING RANGES

PART NUMBER	SUPPLY VOLTAGE (V_{CC})			AMBIENT TEMPERATURE
	MIN	TYP	MAX	
93417XC, 93427XC	4.75 V	5.0 V	5.25 V	0°C to +75°C
93417XM, 93427XM	4.50 V	5.0 V	5.50 V	−55°C to +125°C

X = package type; F for Flatpak, D for Ceramic DIP, P for Plastic DIP. See Package Information on this data sheet.

DC CHARACTERISTICS: Over guaranteed operating ranges unless otherwise noted.

SYMBOL	CHARACTERISTIC	LIMITS MIN	LIMITS TYP (Note 1)	LIMITS MAX	UNITS	CONDITIONS	
I_{CEX}	Output Leakage Current (93417 only)			50	μA	V_{CC} = 5.25 V, V_{CEX} = 4.95 V, 0°C to +75°C Address any HIGH Output	
I_{CEX}	Output Leakage Current (93417 only)			100	μA	V_{CC} = 5.5 V, V_{CEX} = 5.2 V, −55°C to +125°C Address any HIGH Output	
V_{OL}	Output LOW Voltage		0.30	0.45	V	V_{CC} = MIN, I_{OL} = 16 mA, A_0 = +10.8 V A_1 through A_7 = HIGH	
V_{OH}	Output HIGH Voltage (93427 only)	2.4			V	V_{CC} = MIN, I_{OH} = −2.0 mA	
I_{off}	Output Leakage Current for HIGH Impedance State (93427 only)			50 −50	μA μA	V_{OH} = 2.4 V V_{OL} = 0.4 V	0°C to +75°C
I_{off}	Output Leakage Current for HIGH Impedance State (93427 only)			100 −50	μA μA	V_{OH} = 2.4 V V_{OL} = 0.4 V	−55°C to +125°C
V_{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage			0.8	V	Guaranteed Input LOW Voltage for All Inputs	
I_F	Input LOW Current I_{FA} (Address Inputs) I_{FCS} (Chip Select Inputs)		−160 −160	−250 −250	μA μA	V_{CC} = MAX, V_F = 0.45 V	
I_R	Input HIGH Current I_{RA} (Address Inputs) I_{RCS} (Chip Select Input)			40 40	μA μA	V_{CC} = MAX, V_R = 2.4 V	
I_{CC}	Power Supply Current		85	110	mA	V_{CC} = MAX, Outputs open Inputs Grounded and Chip Selected	
C_O	Output Capacitance		7		pF	V_{CC} = 5.0 V, V_O = 4.0 V, f = 1.0 MHz	
C_{IN}	Input Capacitance		4		pF	V_{CC} = 5.0 V, V_O = 4.0 V, f = 1.0 MHz	
V_C	Input Clamp Diode Voltage			−1.2	V	V_{CC} = MIN, I_A = −18 mA	

AC CHARACTERISTICS: T_A = 0°C to +75°C, V_{CC} = 5.0 V ± 5%.

SYMBOL	CHARACTERISTIC	LIMITS MIN	LIMITS TYP (Note 1)	LIMITS MAX	UNITS	CONDITIONS
t_{AA-} t_{AA+}	Address to Output Access Time		25 25	45 45	ns ns	See Figure 1A and 1B
t_{ACS-} t_{ACS+}	Chip Select Access Time		12 12	20 20	ns ns	

AC CHARACTERISTICS: T_A = −55°C to +125°C, V_{CC} = 5.0 V ± 10%.

SYMBOL	CHARACTERISTIC	LIMITS MIN	LIMITS TYP (Note 1)	LIMITS MAX	UNITS	CONDITIONS
t_{AA-} t_{AA+}	Address to Output Access Time		25 25	60 60	ns ns	See Figure 1A and 1B
t_{ACS-} t_{ACS+}	Chip Select Access Time		12 12	30 30	ns ns	

Note 1. Typical limits are at V_{CC} = 5.0 V, +25°C and max loading.

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93436/93446
ISOPLANAR SCHOTTKY TTL MEMORY
512×4-BIT PROGRAMMABLE READ ONLY MEMORY

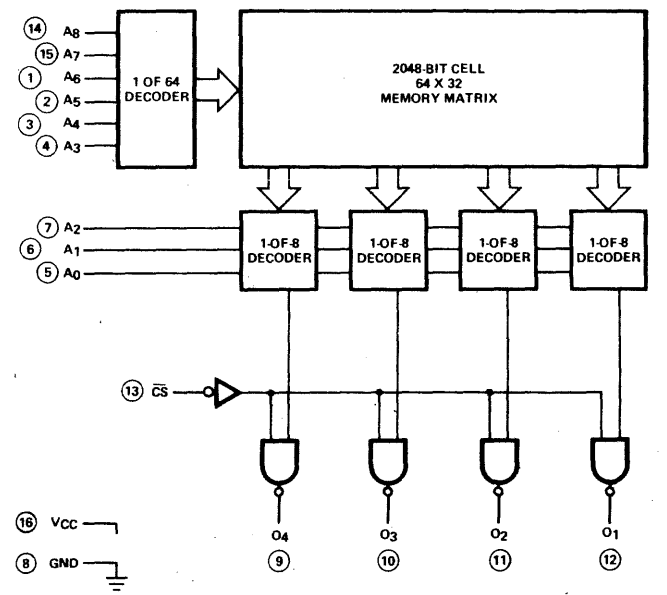
DESCRIPTION – The 93436 and 93446 are fully decoded high speed 2048-bit field Programmable ROMs organized 512 words by four bits per word. The devices are identical except for the output stage. The 93436 has uncommitted collector outputs, while the 93446 has 3-state outputs. In either case, the outputs are off when the $\overline{CS}$ input is in the HIGH state. The 93436 and 93446 are supplied with all bits stored as logic "1"s and can be programmed to logic "0"s by following the field programming procedure.

- **FAST CYCLE TIME – 30 ns TYP**
- **FULL MIL AND COMMERCIAL RANGES**
- **FIELD PROGRAMMABLE**
- **ORGANIZATION – 512 WORDS x 4 BITS**
- **UNCOMMITTED COLLECTORS – 93436**
- **3-STATE OUTPUTS – 93446**
- **FULLY DECODED – ON-CHIP ADDRESS DECODER AND BUFFER**
- **CHIP SELECT INPUT PROVIDES EASY MEMORY EXPANSION**
- **WIRED-OR CAPABILITY**
- **STANDARD 16-PIN DUAL IN-LINE PACKAGE**
- **NICHROME FUSE LINKS FOR HIGH RELIABILITY**
- **REPLACES TWO 256 x 4 PROMS – DOUBLE DENSITY WITH SAME SPACE AND POWER**

PIN NAMES

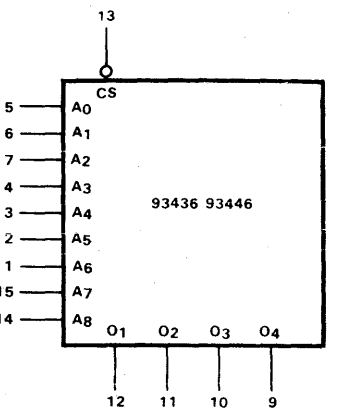
$A_0 - A_8$	Address Inputs
$\overline{CS}$	Chip Select Input
$O_1 - O_4$	Data Outputs

LOGIC DIAGRAM



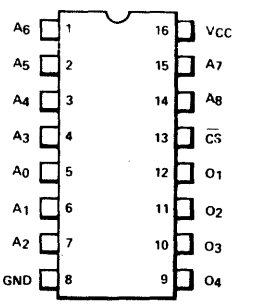
○ = Pin Numbers

LOGIC SYMBOL



V_{CC} = Pin 16
GND = Pin 8

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-Line Package.

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GUARANTEED OPERATING RANGES

PART NUMBER	SUPPLY VOLTAGE (V_{CC})			AMBIENT TEMPERATURE
	MIN	TYP	MAX	
93436XC, 93446XC	4.75 V	5.0 V	5.25 V	0°C to +75°C
93436XM, 93446XM	4.50 V	5.0 V	5.50 V	−55°C to +125°C

X = package type; F for Flatpak, D for Ceramic DIP, P for Plastic DIP. See Package Information on this data sheet.

DC CHARACTERISTICS: Over guaranteed operating ranges unless otherwise noted.

SYMBOL	CHARACTERISTIC	LIMITS MIN	LIMITS TYP (Note 1)	LIMITS MAX	UNITS	CONDITIONS
I_{CEX}	Output Leakage Current (93436 only)			50	μA	V_{CC} = MAX, V_{CEX} = 4.0 V, 0°C to +75°C Address any HIGH Output
I_{CEX}	Output Leakage Current (93436 only)			100	μA	V_{CC} = MAX, V_{CEX} = 4.0 V, −55°C to +125°C Address any HIGH Output
V_{OL}	Output LOW Voltage		0.30	0.45	V	V_{CC} = MIN, I_{OL} = 16 mA, A_0 = +10.8 V A_1 through A_8 = HIGH
V_{OH}	Output HIGH Voltage (93446 only)	2.4			V	V_{CC} = MIN, I_{OH} = −2.0 mA
I_{off}	Output Leakage Current for HIGH Impedance State (93446 only)			50 −50	μA μA	V_{OH} = 2.4 V V_{OL} = 0.4 V 0°C to +75°C
I_{off}	Output Leakage Current for HIGH Impedance State (93446 only)			100 −50	μA μA	V_{OH} = 2.4 V V_{OL} = 0.4 V −55°C to +125°C
V_{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V_{IL}	Input LOW Voltage			0.8	V	Guaranteed Input LOW Voltage for All Inputs
I_F	Input LOW Current I_{FA} (Address Inputs) I_{FCS} (Chip Select Inputs)		−160 −160	−250 −250	μA μA	V_{CC} = MAX, V_F = 0.45 V
I_R	Input HIGH Current I_{RA} (Address Inputs) I_{RCS} (Chip Select Input)			40 40	μA μA	V_{CC} = MAX, V_R = 2.4 V
I_{CC}	Power Supply Current		95	130	mA	V_{CC} = MAX, Outputs open Inputs Grounded and Chip Selected
C_O	Output Capacitance		7		pF	V_{CC} = 5.0 V, V_O = 4.0 V, f = 1.0 MHz
C_{IN}	Input Capacitance		4		pF	V_{CC} = 5.0 V, V_O = 4.0 V, f = 1.0 MHz
V_C	Input Clamp Diode Voltage			−1.2	V	V_{CC} = MIN, I_A = −18 mA

AC CHARACTERISTICS: T_A = 0°C to +75°C, V_{CC} = 5.0 V ± 5%.

SYMBOL	CHARACTERISTIC	LIMITS MIN	LIMITS TYP (Note 1)	LIMITS MAX	UNITS	CONDITIONS
t_{AA-}	Address to Output Access Time		30	50	ns	See Waveforms and Test Circuits
t_{AA+}			30	50	ns	
t_{ACS-}	Chip Select Access Time		15	25	ns	
t_{ACS+}			15	25	ns	

AC CHARACTERISTICS: T_A = −55°C to +125°C, V_{CC} = 5.0 V ± 10%

SYMBOL	CHARACTERISTIC	LIMITS MIN	LIMITS TYP (Note 1)	LIMITS MAX	UNITS	CONDITIONS
t_{AA-}	Address to Output Access Time		30	60	ns	See Waveforms and Test Circuits
t_{AA+}			30	60	ns	
t_{ACS-}	Chip Select Access Time		15	30	ns	
t_{ACS+}			15	30	ns	

Note 1: Typical values are at V_{CC} = 5.0 V, +25°C and max loading.

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93438/93448
ISOPLANAR SCHOTTKY TTL MEMORY
512×8-BIT PROGRAMMABLE READ ONLY MEMORY

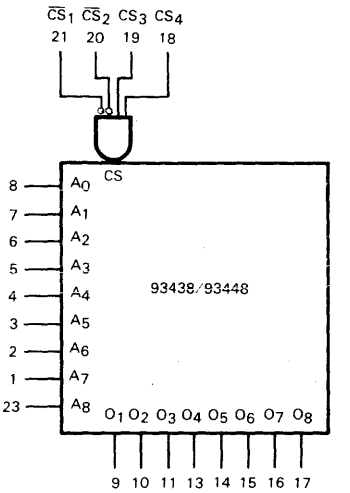
DESCRIPTION – The 93438 and 93448 are fully decoded 4096-bit field Programmable ROMs organized 512 words by eight bits per word. The devices are identical except for the output stage. The 93438 has uncommitted collector outputs, while the 93448 has 3-state outputs. Either device is enabled when $\overline{CS}_1$ and $\overline{CS}_2$ are LOW and CS_3 and CS_4 are HIGH. The 93438/48 is supplied with all bits stored as logic "1's" and may be programmed to logic "0's" by following the field programming procedure.

- FAST CYCLE TIME – 35ns TYP
- FULL MIL AND COMMERCIAL RANGES
- FIELD PROGRAMMABLE
- ORGANIZATION – 512 WORDS X 8 BITS
- UNCOMMITTED COLLECTORS – 93438
- 3-STATE OUTPUTS – 93448
- FULLY DECODED – ON-CHIP ADDRESS DECODER AND BUFFER
- CHIP SELECT INPUTS PROVIDE EASY MEMORY EXPANSION
- WIRED-OR CAPABILITY
- STANDARD 24-PIN DUAL IN-LINE PACKAGE
- NICHROME FUSE LINKS FOR HIGH RELIABILITY

PIN NAMES

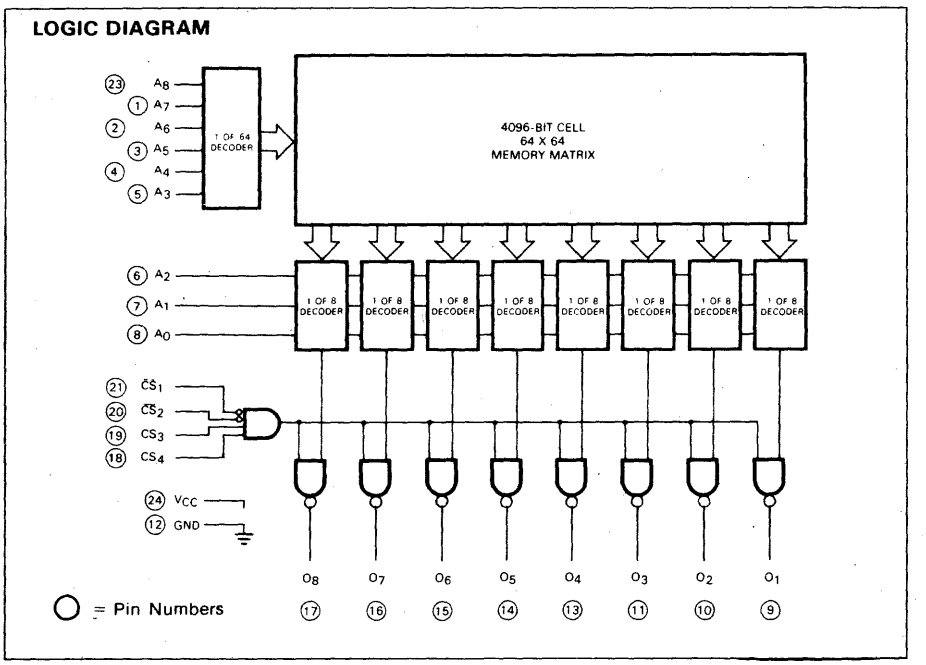
$\overline{A_0} - \overline{A_8}$	Address Inputs
$\overline{CS}_1, \overline{CS}_2, CS_3, CS_4$	Chip Select Inputs
$O_1 - O_8$	Data Outputs

LOGIC SYMBOL

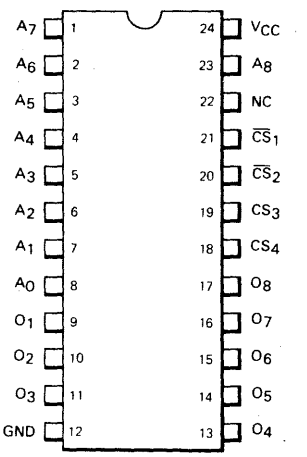


V_{CC} = Pin 24
GND = Pin 12

LOGIC DIAGRAM



CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE: The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package.

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GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE (V_{CC})			AMBIENT TEMPERATURE
	MIN	TYP	MAX	
93438XC, 93448XC	4.75 V	5.0 V	5.25 V	0°C to +75°C
93438XM, 93448XM	4.50 V	5.0 V	5.50 V	−55°C to +125°C

X = package type; F for Flatpak, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

DC CHARACTERISTICS: Over guaranteed operating ranges unless otherwise note.

SYMBOL	CHARACTERISTIC	LIMITS MIN	LIMITS TYP (Note 1)	LIMITS MAX	UNITS	CONDITIONS	
I_{CEX}	Output Leakage Current (93438 only)			50	μA	V_{CC} = MAX, V_{CEX} = 4.0 V, 0°C to +75°C Address any HIGH Output	
I_{CEX}	Output Leakage Current (93438 only)			100	μA	V_{CC} = MAX, V_{CEX} = 4.0 V, −55°C to +125°C Address any HIGH Output	
V_{OL}	Output LOW Voltage		0.30	0.45	V	V_{CC} = MIN, I_{OL} = 16 mA A_0 = +10.8 V, $A_1 - A_8$ = HIGH	
V_{OH}	Output HIGH Voltage (93448 only)	2.4			V	V_{CC} = MIN, I_{OH} = −2.0 mA	
I_{off}	Output Leakage Current for HIGH Impedance State (93448 only)			50 −50	μA μA	V_{OH} = 2.4 V V_{OL} = 0.4 V	0°C to +75°C
I_{off}	Output Leakage Current for HIGH Impedance State (93448 only)			100 −50	μA μA	V_{OH} = 2.4 V V_{OL} = 0.4 V	−55°C to +125°C
V_{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs	
V_{IL}	Input LOW Voltage			0.8	V	Guaranteed Input LOW Voltage for All Inputs	
I_F	Input LOW Current I_{FA} (Address Inputs) I_{FCS} (Chip Select Inputs)		 −160 −160	 −250 −250	 μA μA	V_{CC} = MAX, V_F = 0.45 V	
I_R	Input HIGH Current I_{RA} (Address Inputs) I_{RCS} (Chip Select Input)			 40 40	 μA μA	V_{CC} = MAX, V_R = 2.4 V	
I_{CC}	Power Supply Current		130	175	mA	V_{CC} = MAX, Outputs Open Inputs Grounded and Chip Selected	
C_O	Output Capacitance		7		pF	V_{CC} = 5.0 V, V_O = 4.0 V, f = 1.0 MHz	
C_{IN}	Input Capacitance		4		pF	V_{CC} = 5.0 V, V_O = 4.0 V, f = 1.0 MHz	
V_C	Input Clamp Diode Voltage			−1.2	V	V_{CC} = MIN, I_A = −18 mA	

AC CHARACTERISTICS: T_A = 0°C to +75°C, V_{CC} = 5.0 V ±5%

SYMBOL	CHARACTERISTIC	LIMITS MIN	LIMITS TYP (Note 1)	LIMITS MAX	UNITS	CONDITIONS
t_{AA-} t_{AA+}	Address to Output Access Time		35 35	55 55	ns ns	See Figure 3A and 3B
t_{ACS-} t_{ACS+}	Chip Select Access Time		15 15	25 25	ns ns	

AC CHARACTERISTICS: T_A = −55°C to +125°C, V_{CC} = 5.0 V ±10%

SYMBOL	CHARACTERISTIC	LIMITS MIN	LIMITS TYP (Note 1)	LIMITS MAX	UNITS	CONDITIONS
t_{AA-} t_{AA+}	Address to Output Access Time		35 35	70 70	ns ns	See Figure 3A and 3B
t_{ACS-} t_{ACS+}	Chip Select Access Time		15 15	30 30	ns ns	

Note (1): Typical values are at V_{CC} = 5.0 V, +25°C and max loading.

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93452•93453

ISOPLANAR SCHOTTKY TTL MEMORY

1024X 4-BIT PROGRAMMABLE READ ONLY MEMORY

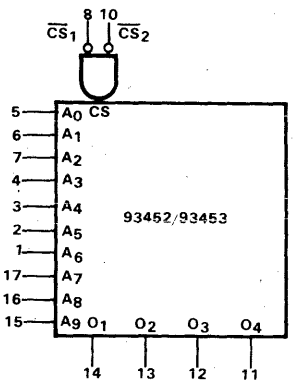
DESCRIPTION – The 93452 and 93453 are fully decoded high speed 4096-bit field Programmable Read Only Memories organized 1024 words by four bits per word. The devices are identical except for the output stages. The 93452 has uncommitted collector outputs, while the 93453 has 3-state outputs. In either case, the outputs are enabled when $\overline{CS}_1$ and $\overline{CS}_2$ are LOW.

- **FULL MIL AND COMMERCIAL RANGES**
- **FAST CYCLE TIME – 35 ns TYP**
- **ORGANIZATION – 1024 WORDS X 4 BITS**
- **UNCOMMITTED COLLECTOR OUTPUTS – 93452**
- **3-STATE OUTPUTS – 93453**
- **FULLY DECODED – ON-CHIP ADDRESS DECODER AND BUFFER**
- **CHIP SELECT INPUTS PROVIDE EASY MEMORY EXPANSION**
- **WIRED-OR CAPABILITY**
- **18-PIN DUAL IN-LINE PACKAGE**
- **REPLACES FOUR 256 X 4 PROMs**

PIN NAMES

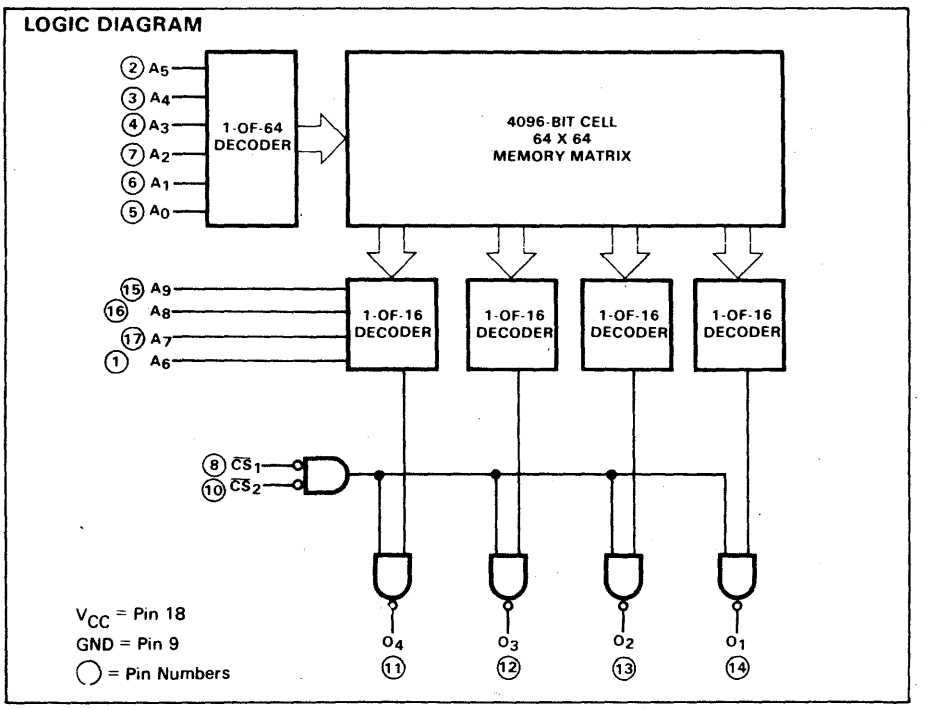
A_0 to A_9	Address Inputs
$\overline{CS}_1$, $\overline{CS}_2$	Chip Select Inputs
O_1 to O_4	Data Outputs

LOGIC SYMBOL



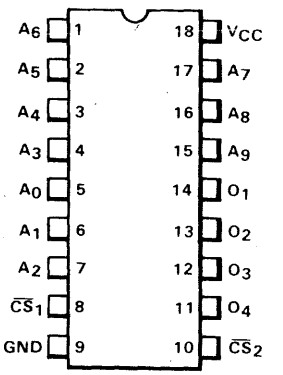
V_{CC} = Pin 18
GND = Pin 9

LOGIC DIAGRAM



V_{CC} = Pin 18
GND = Pin 9
◯ = Pin Numbers

CONNECTION DIAGRAM
DIP (TOP VIEW)



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GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN	TYP	MAX	
93452XC, 93453XC	4.75 V	5.0 V	5.25 V	0°C to +75°C
93452XM, 93453XM	4.50 V	5.0 V	5.50 V	−55°C to +125°C

X = package type; F for Flatpak, D for Ceramic DIP, P for Plastic DIP. See Package Information on this data sheet.

DC CHARACTERISTICS: Over guaranteed operating ranges unless otherwise noted.

SYMBOL	CHARACTERISTIC	LIMITS MIN	LIMITS TYP (Note 1)	LIMITS MAX	UNITS	CONDITIONS
I_{CEX}	Output Leakage Current (93452 only)			50	μA	V_{CC} = 5.25 V, V_{CEX} = 4.95 V, 0°C to +75°C Address any HIGH Output
I_{CEX}	Output Leakage Current (93452 only)			100	μA	V_{CC} = 5.5 V, V_{CEX} = 5.2 V, −55°C to +125°C Address any HIGH Output
V_{OL}	Output LOW Voltage		0.30	0.45	V	V_{CC} = MIN, I_{OL} = 16 mA A_9 = +10.8 V, A_2 = 10.8 V
V_{OH}	Output HIGH Voltage (93453 only)	2.4			V	V_{CC} = MIN, I_{OH} = −2.0 mA
I_{off}	Output Leakage Current for HIGH Impedance State (93453 only)			50 −50	μA μA	V_{OH} = 2.4 V V_{OL} = 0.4 V 0°C to +75°C
I_{off}	Output Leakage Current for HIGH Impedance State (93453 only)			100 −50	μA μA	V_{OH} = 2.4 V V_{OL} = 0.4 V −55°C to +125°C
V_{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V_{IL}	Input LOW Voltage			0.8	V	Guaranteed Input LOW Voltage for All Inputs
I_F	Input LOW Current I_{FA} (Address Inputs) I_{FCS} (Chip Select Inputs)		 −160 −160	 −250 −250	 μA μA	V_{CC} = MAX, V_F = 0.45 V
I_R	Input HIGH Current I_{RA} (Address Inputs) I_{RCS} (Chip Select Input)			 40 40	 μA μA	V_{CC} = MAX, V_R = 2.4 V
I_{CC}	Power Supply Current		120	170	mA	V_{CC} = MAX, Outputs Open Inputs Grounded and Chip Selected
C_O	Output Capacitance		7		pF	V_{CC} = 5.0 V, V_O = 4.0 V, f = 1.0 MHz
C_{IN}	Input Capacitance		4		pF	V_{CC} = 5.0 V, V_O = 4.0 V, f = 1.0 MHz
V_C	Input Clamp Diode Voltage			−1.2	V	V_{CC} = MIN, I_A = −18 mA

AC CHARACTERISTICS: T_A = 0°C to +75°C, V_{CC} = 5.0 V ±5%

SYMBOL	CHARACTERISTIC	LIMITS MIN	LIMITS TYP (Note 1)	LIMITS MAX	UNITS	CONDITIONS
t_{AA-} t_{AA+}	Address to Output Access Time		30 30	55 55	ns ns	S See Waveforms and Test Circuits B
t_{ACS-} t_{ACS+}	Chip Select Access Time		15 15	25 25	ns ns	

AC CHARACTERISTICS: T_A = −55°C to +125°C, V_{CC} = 5.0 V ±10%

SYMBOL	CHARACTERISTIC	LIMITS MIN	LIMITS TYP (Note 1)	LIMITS MAX	UNITS	CONDITIONS
t_{AA-} t_{AA+}	Address to Output Access Time		30 30	70 70	ns ns	S See Waveforms and Test Circuits B
t_{ACS-} t_{ACS+}	Chip Select Access Time		15 15	30 30	ns ns	

Note 1: Typical limits are at V_{CC} = 5.0 V, +25°C and max loading.

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93450/93451

ISOPLANAR SCHOTTKY TTL MEMORY

1024x8-BIT PROGRAMMABLE READ ONLY MEMORY

DESCRIPTION — The 93450 and 93451 are fully decoded 8192-bit field Programmable ROMs organized 1024 words by eight bits per word. The devices are identical except for the output stage. The 93450 has uncommitted collector outputs, while the 93451 has 3-state outputs. Either device is enabled when $\overline{CS}_1$ and $\overline{CS}_2$ are LOW and CS_3 and CS_4 are HIGH. The 93450/51 is supplied with all bits stored as logic "1's" and may be programmed to logic "0's" by following the field programming procedure.

- **FAST CYCLE TIME — 35 ns TYP**
- **FULL MIL AND COMMERCIAL RANGES**
- **FIELD PROGRAMMABLE**
- **ORGANIZATION — 1024 WORDS X 8 BITS**
- **UNCOMMITTED COLLECTORS — 93450**
- **3-STATE OUTPUTS — 93451**
- **FULLY DECODED — ON-CHIP ADDRESS DECODER AND BUFFER**
- **CHIP SELECT INPUTS PROVIDE EASY MEMORY EXPANSION**
- **WIRED-OR CAPABILITY**
- **STANDARD 24-PIN DUAL IN-LINE PACKAGE**
- **NICHROME FUSE LINKS FOR HIGH RELIABILITY**

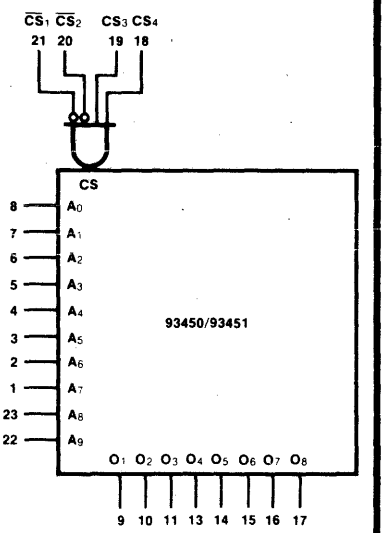
PIN NAMES

A_0 — A_9	Address Inputs
$\overline{CS}_1$, $\overline{CS}_2$, CS_3, CS_4	Chip Select Inputs
O_1 — O_8	Data Outputs

ABSOLUTE MAXIMUM RATINGS

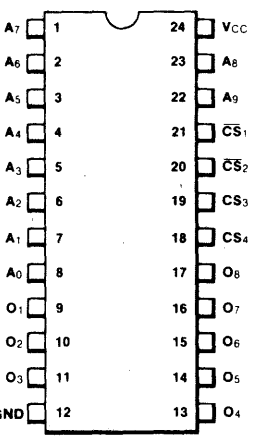
Storage Temperature	-65° C to +150° C
Temperature (Ambient) Under Bias	-55° C to +125° C
V_{CC}	-0.5 V to +7.0 V
Input Voltage	-0.5 V to +5.5 V
Current into Output Terminal	100 mA
Output Voltages	-0.5 V to +5.5 V

LOGIC SYMBOL



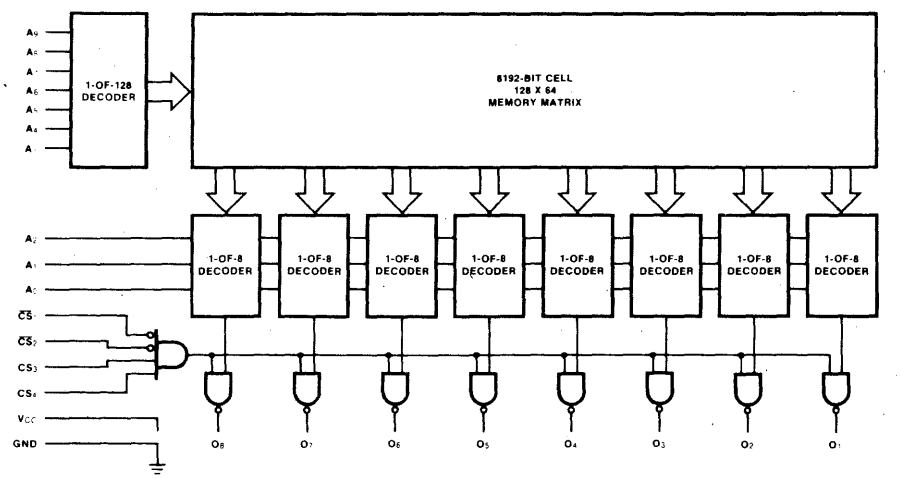
V_{CC} = Pin 24
GND = Pin 12

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE: The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package.

LOGIC DIAGRAM



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DC CHARACTERISTICS: Over guaranteed operating ranges unless otherwise noted.

SYMBOL	CHARACTERISTIC	LIMITS MIN	LIMITS TYP (Note 1)	LIMITS MAX	UNITS	CONDITIONS
I_{CEX}	Output Leakage Current (93450 only)			50	μA	V_{CC} = 5.25, V_{CEX} = 4.95 V, 0°C to +75°C Address any HIGH Output
I_{CEX}	Output Leakage Current (93450 only)			100	μA	V_{CC} = 5.5, V_{CEX} = 5.2 V, -55°C to +125°C Address any HIGH Output
V_{OL}	Output LOW Voltage		0.30	0.45	V	V_{CC} = MIN, I_{OL} = 16 mA, A_0 = +10.8 V, A_9 = +10.8 V, A_1 - A_8 = Don't Care
V_{OH}	Output HIGH Voltage (93451 only)	2.4			V	V_{CC} = MIN, I_{OH} = -2.0 mA
I_{off}	Output Leakage Current for HIGH Impedance State (93541 only)			50 -50	μA μA	V_{OH} = 2.4 V, V_{OL} = 0.4 V — 0°C to +75°C
I_{off}	Output Leakage Current for HIGH Impedance State (93451 only)			100 -50	μA μA	V_{OH} = 2.4 V, V_{OL} = 0.4 V — -55°C to +125°C
V_{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for all Inputs
V_{IL}	Input LOW Voltage			0.8	V	Guaranteed Input LOW Voltage for All Inputs
I_F	Input LOW Current I_{FA} (Address Inputs) I_{FCS} (Chip Select Inputs)		 -160 -160	 -250 -250	 μA μA	V_{CC} = MAX, V_F = 0.45 V
I_R	Input HIGH Current I_{RA} (Address Inputs) I_{RCS} (Chip Select Input)			 40 40	 μA μA	V_{CC} = MAX, V_R = 2.4 V
I_{CC}	Power Supply Current		130	175	mA	V_{CC} = MAX, Outputs Open Inputs Grounded and Chip Selected
C_O	Output Capacitance		7		pF	V_{CC} = 5.0 V, V_O = 4.0 V, f = 1.0 MHz
C_{IN}	Input Capacitance		4		pF	V_{CC} = 5.0 V, V_O = 4.0 V, f = 1.0 MHz
V_C	Input Clamp Diode Voltage			-1.2	V	V_{CC} = MIN, I_A = -18 mA

AC CHARACTERISTICS: T_A = 0°C to +75°C, V_{CC} = 5.0 V ±5%

SYMBOL	CHARACTERISTIC	LIMITS MIN	LIMITS TYP (Note 1)	LIMITS MAX	UNITS	CONDITIONS
t_{AA-} t_{AA+}	Address to Output Access Time		35 35	55 55	ns ns	See Figure 2A and 2B
t_{ACS-} t_{ACS+}	Chip Select Access Time		15 15	25 25	ns ns	

AC CHARACTERISTICS: T_A = -55°C to +125°C, V_{CC} = 5.0 V ±10%

SYMBOL	CHARACTERISTIC	LIMITS MIN	LIMITS TYP (Note 1)	LIMITS MAX	UNITS	CONDITIONS
t_{AA-} t_{AA+}	Address to Output Access Time		35 35	70 70	ns ns	See Figure 2A and 2B
t_{ACS-} t_{ACS+}	Chip Select Access Time		15 15	30 30	ns ns	

Note (1): Typical values are at V_{CC} = 5.0 V, +25°C and max loading.

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GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE (V_{CC})			AMBIENT
	MIN	TYP	MAX	TEMPERATURE
93450XC, 93451XC	4.75 V	5.0 V	5.25 V	0°C to +75°C
93450XM, 93451XM	4.50 V	5.0 V	5.50 V	-55°C to +125°C

X = package type; F for Flatpack, D for Ceramic Dip, P for Plastic Dip. See Packaging Information Section for packages available on this product.

FUNCTIONAL DESCRIPTION — The 93450 and 93451 are bipolar field Programmable Read Only Memories (PROMs) organized 1024 words by eight bits per word. Open Collector outputs are provided on the 93450 for use in wired-OR systems. The 93451 has 3-state outputs which provide active pull-ups when enabled and high output impedance when disabled. Chip Select for both devices follows the logic equation: $\overline{CS}_1 \bullet \overline{CS}_2 \bullet CS_3 \bullet CS_4 = CS$; i.e., if $\overline{CS}_1$ and $\overline{CS}_2$ are both active LOW and CS_3 and CS_4 are both active HIGH, all eight outputs are enabled; for any other condition all eight outputs are disabled.

The read function is identical to that of a conventional bipolar ROM. That is, a binary address is applied to the A_0 through A_9 inputs, the chip is selected, and data is valid at the outputs after t_{AA} nanoseconds.

Programming (selectively opening nichrome fuse links) is accomplished by following the sequence outlined under the table of PROGRAMMING SPECIFICATIONS.

PROGRAMMING — The 93450 and 93451 are manufactured with all bits in the logic "1" state. Any desired bit (output) can be programmed to a logic "0" state by following the procedure shown below. One may build a programmer to satisfy the specifications or purchase any of the commercially available programmers which meet these specifications.

PROGRAMMING SPECIFICATIONS

PARAMETER	SYMBOL	MIN	RECOMMENDED VALUE	MAX	UNITS	COMMENTS	
Address Input	V_{IH}	2.4	5.0	5.0	V	Do not leave inputs open	
	V_{IL}	0	0	0.4	V		
Chip Select	$\overline{CS}_1$, $\overline{CS}_2$	2.4	5.0	5.0	V	Pin 20 or 21 or both	Either or both
	CS_3, CS_4	0	0	0.4	V	Pin 18 or 19 or both	
Programming Voltage Pulse	V_{OP}	20	20.5	21	V	Applied to output to be programmed	
Programming Pulse Width	t_{pw}	0.05	0.18	50	ms	All bits can be programmed in ≤ 8.2 s	
Duty Cycle Programming Pulse			20	*	%	*Maximum duty cycle to maintain $T_C < 85°$ C	
Programming Pulse Rise Time	t_r	0.5	1.0	3.0	μs		
Number of Pulses Required		1	4	8			
Power Supply Voltage	V_{CC}	4.9	5.0	5.1	V		
Case Temperature	T_C		25	85	°C		
Programming Pulse Current Limit	I_{OP}			100	mA	If pulse generator is used, set current limit to this max value.	
Low V_{CC} Read	V_{CC}		4.4	5.0	V	Programming Read Verify	

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93458/93459
ISOPLANAR SCHOTTKY TTL FPLA
16 × 48 × 8 FIELD PROGRAMMABLE LOGIC ARRAY

DESCRIPTION — The 93458 and 93459 are high-speed bipolar field Programmable Logic arrays organized with 16 inputs, 48 product terms and 8 outputs. The 16 inputs and their complements are fuse linked to the inputs of 48 AND gates (48 product terms). Each of the 48 AND gates are fuse linked to 8 48-input OR gates (8 summing terms). Each output may be programmed active HIGH or active LOW. The devices are identical except for the output stage. The 93458 has uncommitted collector outputs while the 93459 has 3-state outputs. In either case, the outputs are enabled when $\overline{CS}$ is LOW.

- **FIELD PROGRAMMABLE (NICHROME FUSE LINKS)**
- **FULL MIL AND COMMERCIAL RANGES**
- **FAST CYCLE TIME — 25 ns TYP**
- **ORGANIZATION — 16 INPUTS x 48 PRODUCT TERMS x 8 OUTPUTS**
- **UNCOMMITTED COLLECTOR OUTPUTS — 93458**
- **3-STATE OUTPUTS — 93459**
- **CHIP SELECT PROVIDES EASY MEMORY EXPANSION**
- **28-PIN PACKAGE**

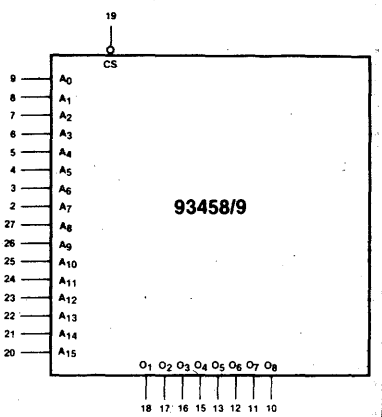
ABSOLUTE MAXIMUM RATINGS

Storage Temperature	-65°C to +150°C
Temperature (Ambient) Under Bias	-55°C to +125°C
V_{CC} Pin Potential to Ground	-0.5 V to +7.0 V
Input Voltage	-0.5 V to +5.5 V
Current Into Output Terminal	100 mA
Output Voltages	−0.5 V to 5.5 V

PIN NAMES

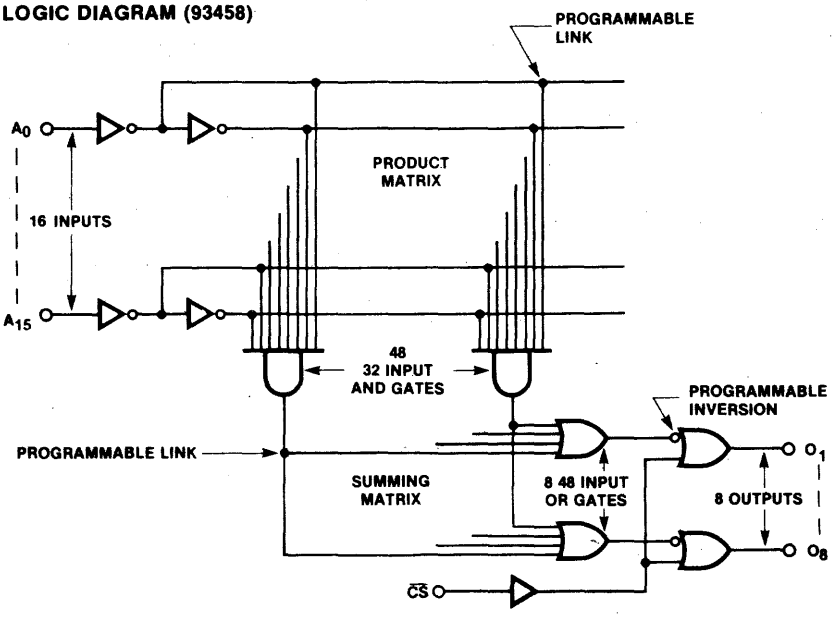
$A_0 - A_{15}$	Address Inputs
$\overline{CS}$	Chip Select Input
$O_1 - O_8$	Data Outputs

LOGIC SYMBOL

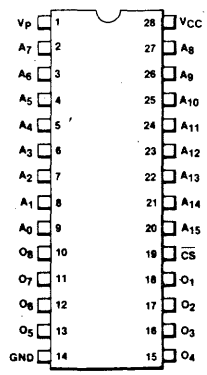


V_{CC} = Pin 28
GND = Pin 14
V_P = Pin 1

LOGIC DIAGRAM (93458)



CONNECTION DIAGRAM
DIP (TOP VIEW)



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GUARANTEED OPERATING RANGES

PART NUMBERS	SUPPLY VOLTAGE (V_{CC})			TEMPERATURE
	MIN	TYP	MAX	
93458DC, 93459DC	4.75 V	5.0 V	5.25 V	0°C to +75°C
93458DM, 93459DM	4.50 V	5.0 V	5.50 V	-55°C to +125°C

LOGIC RELATIONSHIPS

Input Term A_n — $n = 0, \ldots, 15$, one of 16 inputs

Product Term $P_m = \Pi_0^{15} (i_n A_n + j_n \overline{A_n})$ — $m = 0, \ldots, 47$, one of 48 product terms where:
a) $i_n = j_n = 0$ for unprogrammed input
b) $i_n = \overline{j_n}$ for programmed input
c) $i_n = j_n = 1$ for don't care input

$F_r = \Sigma_0^{47} P_m$ — $r = 1, \ldots, 8$, the OR function of the 48 products terms

Summing Term $S_r = \Sigma_0^{47} k_m P_m$ — where $k_m = 0$ for product term inactive (programmed)
$k_m = 1$ for product term active (unprogrammed)

MODE	$\overline{CS}$	F_r	S_r	OUTPUT ACTIVE HIGH	OUTPUT ACTIVE LOW
READ	0	1	0	0	1
	0	1	1	1	0
	0	0	X	0	1
DISABLE	1	X	X	1 (93458)	1 (93458)
	1	X	X	HI Z (93459)	HI Z (93459)

Example — By programming, the 8 outputs of an FPLA can be made to relate to the 16 inputs as given by the following example:

8 outputs total

$$O_1 = A_0 \overline{A_6} A_{14} + \overline{A_2}\,\overline{A_{15}} + \underbrace{\overline{A_0} A_1 \ldots A_{15}}_{\text{16 input terms max}} + \overline{A_8} A_{10} \overline{A_{13}}$$

48 product terms max

$O_2 = A_0 \overline{A_6} A_{14} + \overline{A_2}\,\overline{A_{15}}$ (Output polarity programmed, active high.)

.
.
.

$$O_8 = \overline{(\overline{A_8} A_{10} \overline{A_{13}} + A_4 \overline{A_7} \overline{A_9} A_{11} \overline{A_{12}})}$$ (Output polarity not programmed, active low.)

FUNCTIONAL DESCRIPTION — The 93458 and 93459 are bipolar field Programmable Logic Arrays (FPLA) organized 16 inputs by 48 product terms by 8 outputs. Open collector outputs are provided on the 93458 for use in wired-OR systems. The 93459 has 3-state outputs which provide active pull ups when enabled and high output impedance when disabled. Chip Select for both devices is active LOW; i.e., a HIGH (logic "1") on the $\overline{CS}$ pin will disable all outputs.

The read function is identical to that of a conventional bipolar ROM. That is, a binary address is applied to the A_0 through A_{15} inputs, the chip is selected, and data is valid at the outputs after t_{AA} nanoseconds.

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DC CHARACTERISTICS: Over guaranteed operating ranges unless otherwise noted.

SYMBOL	CHARACTERISTIC	LIMITS MIN	LIMITS TYP (Note 1)	LIMITS MAX	UNITS	CONDITIONS
I_{CEX}	Output Leakage Current (93458 only)			50	µA	V_{CC} = MAX, V_{CEX} = V_{CC}, 0°C to +75°C Address any HIGH Output
I_{CEX}	Output Leakage Current (93458 only)			100	µA	V_{CC} = MAX, V_{CEX} = V_{CC}, −55°C to +125°C Address any HIGH Output
V_{OL}	Output LOW Voltage		0.30	0.45	V	V_{CC} = MIN, I_{OL} = 16 mA V_P, $\overline{CS}$ = 0 V; A_0—A_5, A_{13}, A_{15} = 5 V; and A_6—A_{12}, A_{14} = 10.8 V
V_{OH}	Output HIGH Voltage (93459 only)	2.4			V	V_{CC} = MIN, I_{OH} = -2.0 mA
I_{off}	Output Leakage Current for HIGH Impedance State (93459 only)			50 -50	µA µA	V_{OH} = 2.4 V V_{OL} = 0.4 V — 0°C to +75°C
I_{off}	Output Leakage Current for HIGH Impedance State (93459 only)			100 µA	µA µA	V_{OH} = 2.4 V V_{OL} = 0.4 V — −55°C to +125°C
I_{OS}	Short Circuit Current	−10		−70	mA	V_{OUT} = 0V; Chip Enabled
V_{IH}	Input HIGH Voltage	2.0			V	Guaranteed Input HIGH Voltage for All Inputs
V_{IL}	Input LOW Voltage			0.8	V	Guaranteed Input LOW Voltage for All Inputs
I_F	Input LOW Current I_{FA} (Address Inputs) I_{FCS} (Chip Select Inputs)		 −160 −160	 −250 −250	 µA µA	V_{CC} = MAX, V_F = 0.45 V
I_R	Input HIGH Current I_{RA} (Address Inputs) I_{RCS} (Chip Select Input)			 40 40	 µA µA	V_{CC} = MAX, V_R = 2.4 V
I_{CC}	Power Supply Current		105	140	mA	V_{CC} = MAX, Outputs Open Inputs Grounded and Chip Selected (See Note 2)
C_O	Output Pin Capacitance		7		pF	V_{CC} = 5.0 V, V_O = 4.0 V, f = 1.0 MHz
C_I	Input Pin Capacitance		4		pF	V_{CC} = 5.0, V_O = 4.0 V, f = 1.0 MHz
V_C	Input Clamp Diode Voltage			−1.2	V	V_{CC} = MIN, I_A = −18 mA

AC CHARACTERISTICS: T_A = 0°C to +75°C, V_{CC} = 5.0 V ±5%

SYMBOL	CHARACTERISTIC	LIMITS MIN	LIMITS TYP (Note 1)	LIMITS MAX	UNITS	CONDITIONS
t_{AA-} t_{AA+}	Address to Output Access Time		25 25	45 45	ns ns	See Figure 1A and 1B
t_{ACS-} t_{ACS+}	Chip Select Access Time		15 15	25 25	ns ns	

AC CHARACTERISTICS: T_A = −55°C to +125°C, V_{CC} = 5.0 V ±10%

SYMBOL	CHARACTERISTIC	LIMITS MIN	LIMITS TYP (Note 1)	LIMITS MAX	UNITS	CONDITIONS
t_{AA-} t_{AA+}	Address to Output Access Time		25 25	65 65	ns ns	See Figure 1A and 1B
t_{ACS-} t_{ACS+}	Chip Select Access Time		15 15	30 30	ns ns	

NOTES: 1. Typical values are at V_{CC} = 5.0 V, +25°C and max loading.
2. For programmed part, add .45 mA typical, .60 mA max per selected programmed product terms and add 2.9 mA typical, 3.9 mA max per enabled low output or 33 mA typical, 44 mA max for disabled states.

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F16K

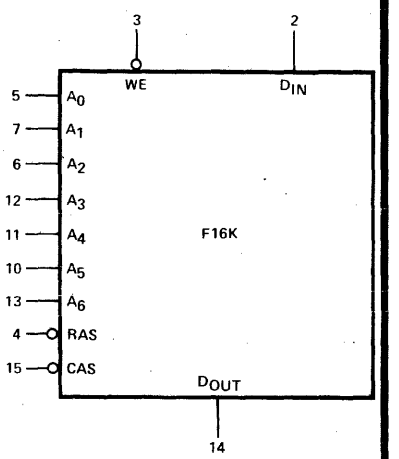
16,384 x 1 DYNAMIC RANDOM ACCESS MEMORY

FAIRCHILD ISOPLANAR SILICON GATE MOS

GENERAL DESCRIPTION — The F16K is a 16,384-bit MOS Dynamic Random Access Memory configured as 16,384 one-bit words, and which is manufactured using Fairchild's n-channel silicon gate, double-poly Isoplanar process. The use of the single-transistor memory cell along with address multiplexing techniques permits the packaging of the F16K in a standard 16-pin dual in-line package. The use of this package allows construction of highly dense memory systems utilizing widely available automated testing and insertion equipment. Furthermore, the pinout, timing and organizational characteristics of the F16K are essentially the same 16-pin 4K dynamic RAMs. Thus the F16K is ideally suited for easy upgrading of 4K-RAM-based systems.

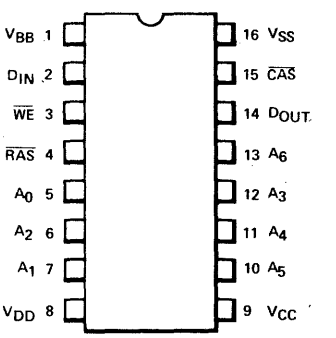
- INDUSTRY STANDARD 16-PIN DUAL IN-LINE PACKAGE
- LOW CAPACITANCE, TTL-COMPATIBLE INPUTS (INCLUDING CLOCKS)
- ON-CHIP ADDRESS AND INPUT DATA LATCHES
- 3-STATE TTL-COMPATIBLE OUTPUT WITH DATA VALID TIME CONTROLLED BY $\overline{CAS}$
- COMMON I/O CAPABILITY
- TWO DIMENSIONAL SELECTION BY DECODING BOTH $\overline{RAS}$ AND $\overline{CAS}$
- STANDARD 10% SUPPLIES (+12 V, +5 V, and −5 V)
- FLEXIBLE TIMING WITH PAGE-MODE AND EXTENDED PAGE BOUNDARIES
- 128-CYCLE $\overline{RAS}$-ONLY REFRESH
- PINOUT AND SPECIFICATION COMPATIBLE WITH INDUSTRY-STANDARD 16K RAMs

LOGIC SYMBOL

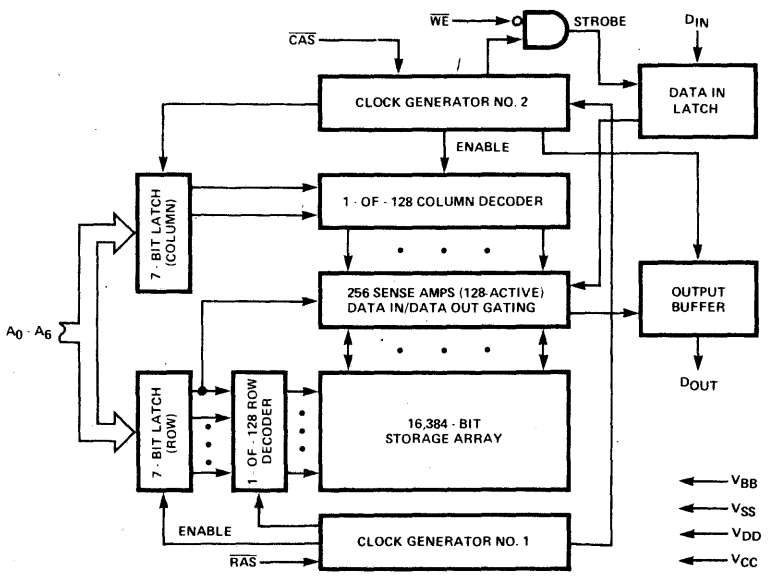


V_{SS} = Pin 16
V_{CC} = Pin 9
V_{DD} = Pin 8
V_{BB} = Pin 1

CONNECTION DIAGRAM
DIP (TOP VIEW)



BLOCK DIAGRAM



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FAIRCHILD

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FUNCTIONAL DESCRIPTION

ADDRESSING – The 14 address bits required to decode one-of-16, 384 cell locations in the F16K are entered using a 2-phase multiplexing operation in which first the 7-bit Row Address is entered followed by the 7-bit Column Address. First the 7-bit Row Address is applied to the seven address inputs of the F16K and latched into the chip by Row Address Strobe ($\overline{RAS}$) which is the first of two externally applied TTL-level clocks. The second clock, Column Address Strobe ($\overline{CAS}$), subsequently latches the seven column address bits into the chip. Each of these signals $\overline{RAS}$ and $\overline{CAS}$, trigger on-chip clock generators which control the internal sequencing of events on the chip. Advanced techniques used in handling the row and column address information allow the address multiplexing operation to be performed without lengthening the critical timing path governing the access time. The activation of $\overline{CAS}$ strobes the column address latch but this event as well as other internal events governed by the $\overline{CAS}$ clock generator may be inhibited until certain prerequisite events controlled by the $\overline{RAS}$ clock generator have occured.

More specifically, a "window" of time exists, extending from $t_{RCD(min)}$ to $t_{RCD(max)}$ during which $\overline{CAS}$ may become active without impacting the access time. Stated another way, as long as $\overline{CAS}$ occurs during this window, the access time will be specified by t_{RAC}. If $\overline{CAS}$ occurs a certain delay after this window of time, the $\overline{RAS}$ clock generator no longer inhibits the $\overline{CAS}$ clock generator and the magnitude of this delay will add directly to the overall access time. This lengthened access time is now referenced to $\overline{CAS}$ rather than $\overline{RAS}$ and is lengthened by the amount of time that t_{RCD} exceeds the $t_{RCD(max)}$ limit. This "gated-$\overline{CAS}$" feature allows greater flexibility since the $\overline{CAS}$ clock may be externally activated as soon as the Hold Time for the Row Address has been met and the address inputs have been changed from Row Address to Column Address information.

PAGE MODE OPERATION – The Page-Mode feature of the F16K allows successive memory cycles accessing the same row in the memory matrix to be concatenated together in such a way that the common Row Address need be supplied only once - resulting in faster access times with no corresponding increase in power. The page-mode option may be used in conjunction with any of the defined memory operations, and is accomplished by supplying the Row Address to the chip and holding $\overline{RAS}$ LOW throughout all subsequent memory cycles for which the Row Address is common.

Since $\overline{RAS}$ makes its initial negative transition only once, no additional dynamic power is dissipated due to $\overline{RAS}$ on any subsequent cycles performed within that row. The access and cycle times are also shortened since the time required to supply a Row Address is eliminated.

DATA INPUT – In a write operation, the data to be input into memory is strobed into an on-chip register during $\overline{RAS}$ by a combination of $\overline{CAS}$ and Write Enable ($\overline{WE}$). The strobe is formed by whichever is the latter of these two signals to make its negative transistion. This presents several possibilities in how a write cycle may be performed. In an "early-write" cycle ($\overline{WE}$ active LOW before $\overline{CAS}$ goes LOW), Data In (D_{IN}) is strobed by $\overline{CAS}$ and thus the set-up and hold times are referenced to this signal edge. If D_{IN} is not yet valid at the time $\overline{CAS}$ becomes active (or if the cycle is a read-write or read-modify-write) then $\overline{WE}$ must be delayed. In this delayed-write mode, the D_{IN} set-up and hold times are referenced to $\overline{WE}$ rather than $\overline{CAS}$. (See the timing diagrams).

DATA OUTPUT – The Data Out (D_{OUT}) latch and buffer unconditionally assume the high-impedance state whenever $\overline{CAS}$ is HIGH, i.e. inactive. If the cycle being performed is a read, read-modify-write, or a delayed write cycle then the D_{OUT} latch and buffer will remain high impedance until the access time, after which D_{OUT} will assume the value of the data read from the selected cell. This output data is of the same polarity (not inverted) as the input data and will remain valid as long as $\overline{CAS}$ is kept active, i.e. LOW. However, if the cycle is an "early-write" cycle or if the chip fails to receive both $\overline{RAS}$ and $\overline{CAS}$, then D_{OUT} will remain high impedance throughout the cycle. This feature allows systems which write employing the early write mode exclusively, to common D_{IN} and D_{OUT} directly together.

Another advantage of this "unlatched output" feature is that OR-tied outputs in a memory matrix require no special action to be turned off. Unlike other types of RAMs which require a negative transition of $\overline{CAS}$ to become high impedance, the F16K's output is already high impedance whenever $\overline{CAS}$ is HIGH, i.e. inactive. This means that $\overline{CAS}$ need not be supplied to unused devices and therefore may be used for device selection. Thus a reduction in external decoding logic is possible by using both $\overline{RAS}$ and $\overline{CAS}$ in a 2 dimensional decoding/selection scheme. (see Table 1 below).

$\overline{RAS}$ active during cycle?	$\overline{CAS}$ active during cycle?	RESULT (after t_{OFF} delay)
Yes	Yes	Device active
Yes	No	Device deselected, refresh
No	Yes	Device deselected
No	No	Device deselected

TABLE 1

EXTENDED PAGE BOUNDARY – A further implication of using both $\overline{RAS}$ and $\overline{CAS}$ for device decoding/selection is in extending page boundaries for page-mode operation. If only $\overline{RAS}$ is decoded, then any given "page" is limited to only 128 different column addresses within that page, (i.e. seven column address bits correspond to $2^7 = 128$ column addresses). Therefore, for memory systems using more than 16K words of data, page boundaries may be extended from 128 addresses per page up to any multiple of 128 addresses merely by decoding which 16K memory bank also gets a $\overline{CAS}$

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(subject to $t_{RAS(max)}$ limitation). This is accomplished by supplying $\overline{RAS}$ to all devices in order to latch in the Row Address information and then decoding which bank of 16K words is to also get $\overline{CAS}$. Only those devices which receive both $\overline{RAS}$ and $\overline{CAS}$ will respond with a valid memory cycle.

INPUT/OUTPUT LEVELS – All inputs, including the two address strobes, interface directly with TTL. The high-impedance, low-capacitance input characteristics simplify input driver selection by allowing use of standard logic elements rather than specially designed driver elements. Termination resistors are normally required in a system to prevent ringing due to line inductance and reflections. In high-speed memory systems, transmission line techniques must be employed on the signal lines to achieve optimum system speeds. Series termination may be employed at some degradation of system speed.

The 3-state output buffer is a low impedance to V_{CC} for logic "1" and low impedance to V_{SS} for logic "0". The effective resistance to V_{CC} is 420 Ω maximum and 135 Ω typically. The effective resistance to V_{SS} is 95 Ω maximum and 35 Ω typically.

REFRESH – The matrix of 128 X 128 memory cells in the F16K is refreshed by executing a memory cycle at each of the 128 Row Addresses within each interval of 2 milliseconds or less. Although any cycle in which $\overline{RAS}$ occurs accomplishes a refresh operation, the refresh is most easily accomplished in the $\overline{RAS}$-only-refresh mode. This type of refresh operation results in decreased power dissipation since $\overline{CAS}$ remains inactive.

POWER DISSIPATION/STANDBY – Since the F16K uses dynamic memory cells, this means that most of the dissipated power is a result of an address strobe edge. There is, however, a small dc component of dissipated power that is associated with the precharging of the sense amplifiers. Thus, the total power dissipated is a function of both operating frequency and duty cycle. Typically, the power is 350 mW at 1μs cycle time with a worst case power of less than 462 mW at 375 μs cycle time. To reduce overall system power during standby, $\overline{RAS}$-only-refresh cycles should be performed with $\overline{CAS}$ held HIGH.

The V_{CC} supply is not used in the internal memory operations of the F16K, but rather used only at the output buffer and thus, for some applications, may be powered from the supply voltage of the logic to which the chip's output is interfaced. This means that I_{CC}, the current drawn from the V_{CC} supply, is a function of output loading. During battery standby operation, the V_{CC} pin may be unpowered, if desired, without affecting the refresh operation. This allows all system logic, except the $\overline{RAS}$ timing circuitry and the refresh address logic, to be turned off during battery standby to conserve power.

PIN NAMES

A_n	Address Inputs	D_{OUT}	Data Output
D_{IN}	Data Input	V_{CC}	+5 V Power Supply
$\overline{WE}$	Write Enable Input (Active LOW)	V_{SS}	0 V Power Supply
$\overline{RAS}$	Row Address Strobe (Clock) Input (Active LOW)	V_{BB}	−5 V Power Supply
$\overline{CAS}$	Column Address Strobe (Clock) Input (Active LOW)	V_{DD}	+12 V Power Supply

ABSOLUTE MAXIMUM RATINGS

Voltage of any pin relative to V_{BB} ($V_{SS} - V_{BB} \geq 4.5$ V)	−0.5 V to + 20 V
Operating Temperature (Ambient)	0°C to 70°C
Storage Temperature (Ambient)	−55°C to 150°C
Power Dissipation	1 W

Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

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2102 • 2102L • 21L02

1024 X 1 STATIC RANDOM ACCESS MEMORY

FAIRCHILD ISOPLANAR SILCON GATE MOS INTEGRATED CIRCUIT

GENERAL DESCRIPTION — The 2102 family consists of 1024-word by 1-bit Static Random Access Read/Write Memories which requires only a single 5 V supply, have fully TTL compatible inputs and output, and require no clocking or refresh. Chip Select (CS) permits a 3-state output allowing the outputs to be wired-OR. Special features include low power dissipation (2102L) and a power-down capability (21L02).

The 2102, 2102L and 21L02 series are manufactured employing the n-channel Isoplanar process and are available in a 16-pin dual in-line package or flatpak.

- **FAST ACCESS – 250 ns**
- **SINGLE +5 V SUPPLY**
- **TTL COMPATIBLE INPUTS AND OUTPUT**
- **TOTALLY STATIC – NO CLOCKS OR REFRESH**
- **3-STATE OUTPUT**
- **LOW POWER (2102L)**
- **POWER-DOWN CAPABILITY (21L02)**
- **FULLY EXPANDABLE**
- **FULLY DECODED**
- **16-PIN DUAL IN-LINE PACKAGE**

POWER/ACCESS TIME GUIDE

	PART NUMBER	ACCESS TIME	$I_{DD(MAX)}$	
			C	L, M
POWER DOWN	21L02H	250 ns	30 mA	— — —
	21L02F	350 ns	30 mA	— — —
	21L021	450 ns	30 mA	— — —
	21L022	650 ns	30 mA	— — —
LOW POWER	2102LH	250 ns	30 mA	40 mA
	2102LF	350 ns	30 mA	40 mA
	2102L1	450 ns	30 mA	40 mA
	2102L2	650 ns	30 mA	40 mA
STANDARD	2102H	250 ns	55 mA	70 mA
	2102F	350 ns	55 mA	70 mA
	21021	450 ns	55 mA	70 mA
	21022	650 ns	55 mA	70 mA

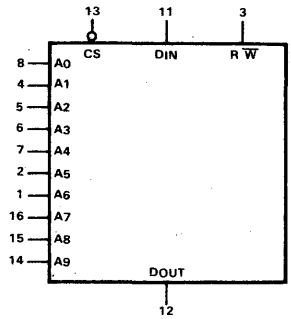
PIN NAMES

A_{0-9}	Address Inputs
D_{OUT}	Data Output
D_{IN}	Data Input
R/$\overline{W}$	Read/Write
$\overline{CS}$	Chip Select (active LOW)

ABSOLUTE MAXIMUM RATINGS

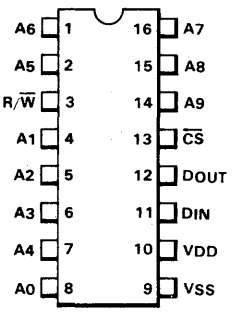
Any Pin with Respect to V_{SS}		−0.5 V to +7.0 V
Storage Temperature		−55°C to +150°C
Operating Temperature	C	0°C to +70°C
	L	−55°C to +85°C
	M	−55°C to +125°C

LOGIC SYMBOL

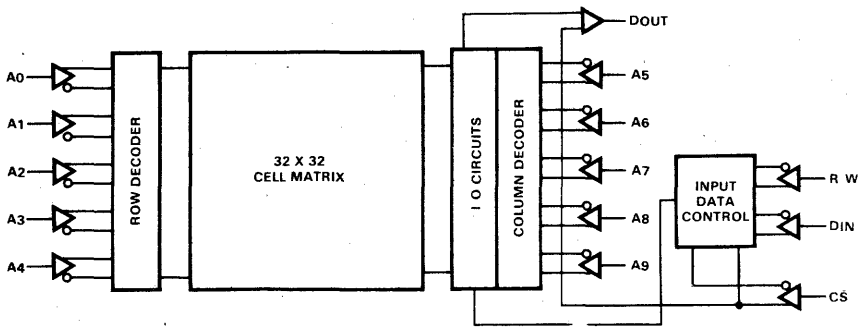


V_{SS} Pin 9
V_{DD} Pin 10

CONNECTION DIAGRAM
DIP (TOP VIEW)



BLOCK DIAGRAM



TRUTH TABLE

$\overline{CS}$	R/$\overline{W}$	D_{IN}	D_{OUT}	Comments
H	X	X	*	Chip Deselected
L	L	H	H	Write "1" †
L	L	L	L	Write "0" †
L	H	X	D_n	Read †

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
* = Output High Impedance State
D_n = Data at Address Location
† = Chip Selected

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FAIRCHILD

F464

65,536 X 1 DYNAMIC SERIAL MEMORY

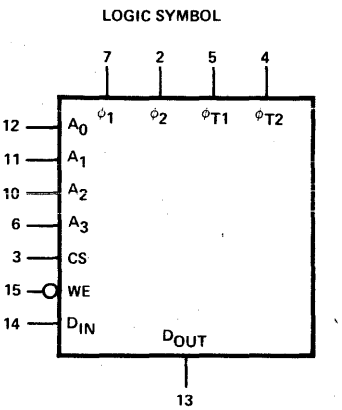
FAIRCHILD CHARGE COUPLED DEVICE

GENERAL DESCRIPTION – The F464 is a 65,536-bit dynamic serial memory configured as 16 randomly accessible shift registers, each 4096 bits long. Each of these shift registers is designed utilizing Charge Coupled Device (CCD) techniques with the interlaced Serial-Parallel-Serial (SPS) register structure which features both low power and high density characteristics. The high density of the F464 is further enhanced through the use of an electrode-per-bit memory cell approach. The high density permits packaging the memory in a standard 16-pin (0.3"-wide) dual in-line package which allows the construction of highly dense memory systems using widely available automated testing and insertion equipment.

Furthermore, this buried-channel CCD memory is fabricated using Fairchild's double-poly n-channel Isoplanar process. This process allows the F464 to be a high performance, state-of-the-art memory circuit which is manufacturable in large volume.

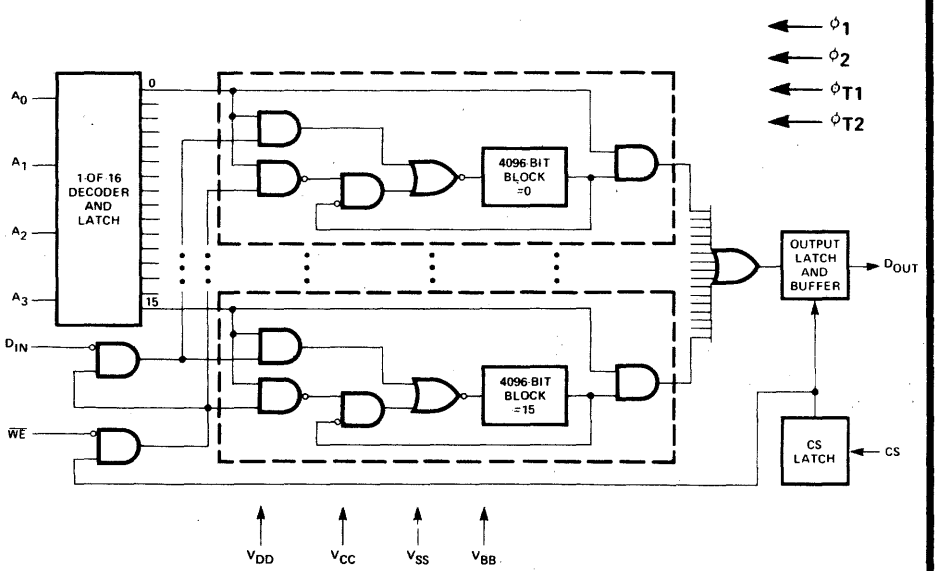
- **INDUSTRY STANDARD 16 PIN (0.3"-WIDE) DUAL IN-LINE PACKAGE.**
- **OPERATING FREQUENCY RANGE: 1 MHz TO 5 MHz.**
- **15 μs HALT TIME AT 2.0 MHz**
- **LOW CAPACITANCE TTL-COMPATIBLE INPUTS (EXCEPT CLOCKS).**
- **3-STATE, TTL-COMPATIBLE, LATCHED DATA OUTPUT.**
- **OUTPUT DRIVE CAPABILITY: 3.5 mA**
- **LOW CAPACITANCE 12 V CLOCKS:**
  - **ϕ_1 AND ϕ_2: 100 pF (TYP)**
  - **ϕ_{T1} AND ϕ_{T2}: 30 pF (TYP)**
- **LOW POWER**
  - **NORMAL OPERATION: <336 mW (MAX) @ f_{max}**
  - **STANDBY: <66 mW (MAX) @ f_{min}**
- **STANDARD POWER SUPPLIES (+12 V, +5 V, AND −5 V)**

LOGIC SYMBOL

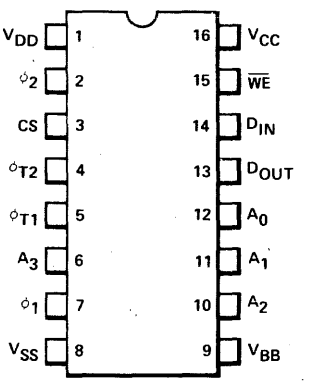


V_{DD} = PIN 1
V_{CC} = PIN 16
V_{SS} = PIN 8
V_{BB} = PIN 9

BLOCK DIAGRAM



CONNECTION DIAGRAM
DIP (TOP VIEW)



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PIN NAMES

ϕ_1, ϕ_2	Serial Clocks	D_{IN}	Data Input
ϕ_{T1}, ϕ_{T2}	Transfer Clocks	D_{OUT}	Data Output
A_n	Address Inputs	V_{CC}	+5 V Power Supply
CS	Chip Select Input	V_{SS}	0 V Power Supply, GND
$\overline{WE}$	Write Enable Input (Active LOW)	V_{BB}	−5 V Power Supply
		V_{DD}	+12 V Power Supply

FUNCTIONAL DESCRIPTION

ORGANIZATION – The F464 is a 65,536 x 1 bit dynamic serial memory organized internally as 16 dynamic shift registers (or blocks) of 4096 bits each in length. These 16 shift register blocks are randomly accessible through four internally decoded Address inputs (A_0 – A_3). When a given register is selected, its input and output are internally connected (as needed) to the D_{IN} and D_{OUT} pins, respectively, thus permitting simultaneous read and write operations.

ARCHITECTURE – Each of the sixteen shift register blocks is implemented using a Serial-Parallel-Serial (SPS) register architecture. In this approach N data bits are sequentially shifted into a "serial" input register. When full, the entire N-bit word is shifted in parallel into N "parallel" registers of M bits in length, as illustrated in Figure 1. At the other end of this parallel register structure, bits are loaded in parallel into an N-bit serial output register. Bits in this register are then shifted out toward the sense amplifier at the output and are automatically recirculated back to the input serial register unless a WRITE operation is specified.

The primary advantages of this type of architecture include very high density, low power, and low clock capacitance. These features all result from the fact that in the SPS architecture the parallel registers which encompass most of the total storage capacity within each block are shifted at a considerably slower rate (f_{IN}/N) than the clock rate of the input or output serial registers (f_{IN}).

In actuality, each 4096-bit block of the F464 is implemented using an "interlaced" SPS structure in which each bit of the input serial register services two parallel registers rather than just one. The same is true for the output serial register. In addition, "electrode-per-bit" design techniques are used to reduce the effective cell size by minimizing the number of electrodes used to store each bit of information. These techniques obviously enhance the memory density considerably. The dimensions of the F464's interlaced SPS structure are 32-bit input and output serial registers and 64 parallel registers, each 63 bits in length. See Figure 2. These dimensions were chosen in order to optimize the power/density/latency tradeoffs inherent in the CCD memory approach.

CLOCKS – The F464 requires four MOS level clocks: two high frequency (1 to 5 MHz) serial clocks and two low frequency transfer clocks. The serial clocks, ϕ_1 and ϕ_2, control the movement of data within the input and output serial registers of each 4096-bit block and have a frequency equal to the data rate. The transfer clock ϕ_{T1} is used to transfer data from the input serial register to the parallel registers while the transfer clock ϕ_{T2} is used to transfer data from the parallel registers to the output serial register of each block. The data present in the parallel registers is shifted by internally generated ripple clocks. This ripple clock technique allows a high bit-packing density approaching one electrode per bit.

To achieve proper transfer phasing, the two transfer clocks are asymetrical about a 32-cycle interval (31.5 and 32.5 cycles) but symmetrical about a 64-cycle interval. The phasing between these transfer clocks alternates in order to achieve correct bit storage in each block. When ϕ_{T1} occurs during ϕ_1 time, ϕ_{T2} occurs during ϕ_2 time 1.5 cycles prior to ϕ_{T1}. When ϕ_{T1} occurs during ϕ_2 time, ϕ_{T2} occurs during ϕ_1 time 2.5 cycles prior to ϕ_{T1}. Figure 3 illustrates the clock phase relationships.

The clocking operation may be momentarily halted for as long as 15 μs once each interval of 64 or more clock cycles provided that the clock frequency is at least 2.0 MHz or higher. During this "halt time" it is recommended that all clock signals be in the LOW state in order to limit power dissipation.

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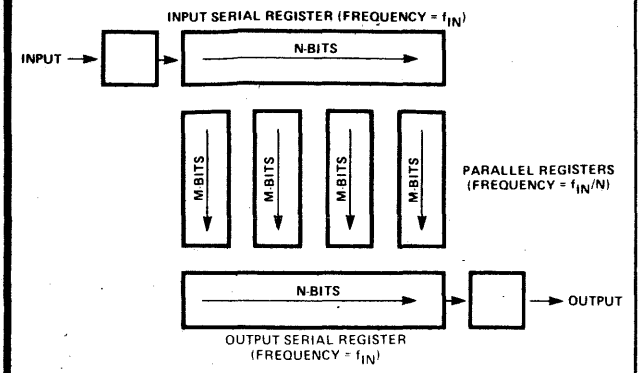


Fig. 1 SIMPLIFIED SPS EXAMPLE WITH N = 4

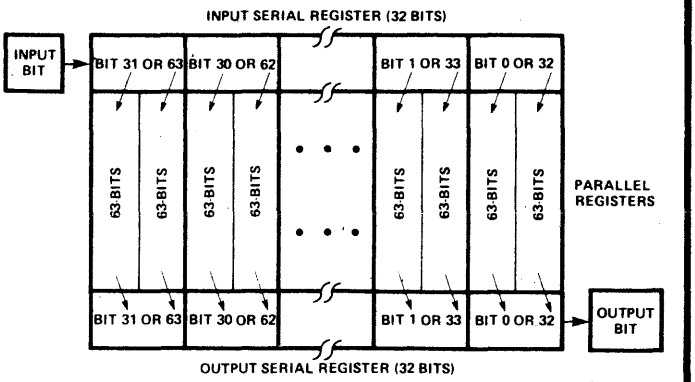
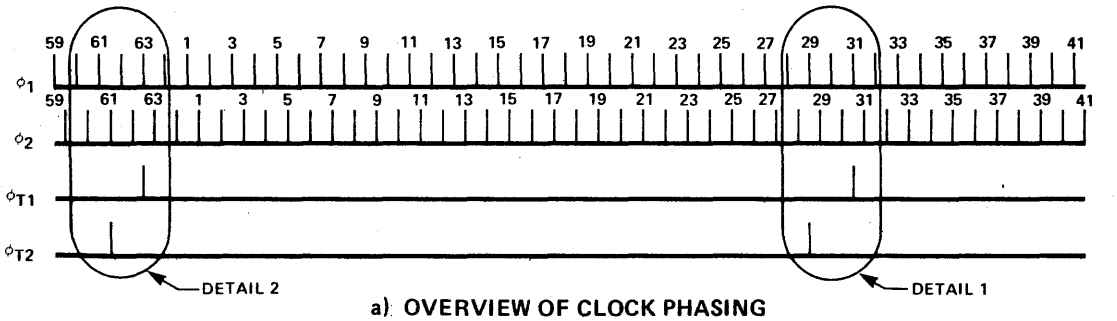
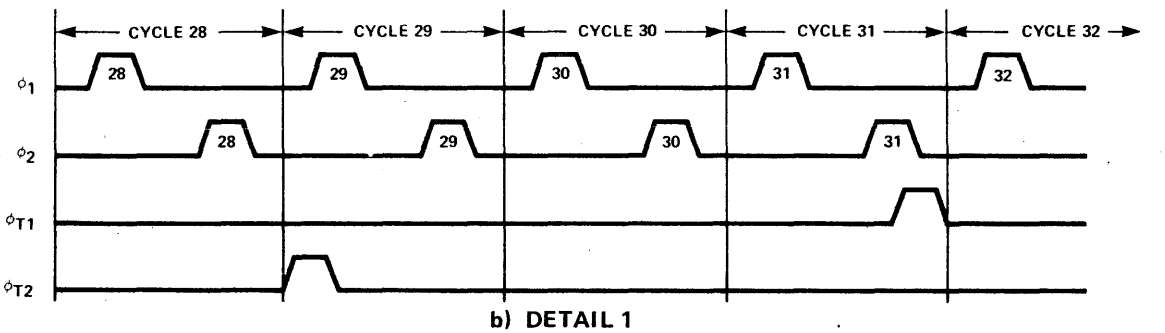


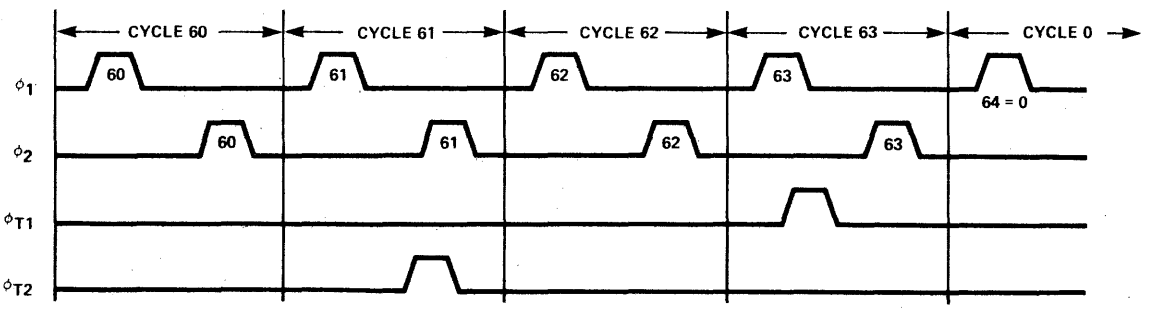
Fig. 2 INTERLACED SPS ARCHITECTURE



a) OVERVIEW OF CLOCK PHASING



b) DETAIL 1



c) DETAIL 2

Fig. 3 F464 CLOCK RELATIONSHIPS

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CONTROLS

In addition to the four Address inputs (A_0 through A_3), other TTL level control signals available on the F464 include Write Enable ($\overline{WE}$) and Chip Select (CS). The CS input, along with the address information, is presented during ϕ_1 HIGH time and dynamically latched with the trailing edge of ϕ_1 which simultaneously disables both the address and CS buffers. This action prevents changes that occur on the external pins from entering the internal circuitry when ϕ_1 is LOW. The $\overline{WE}$ control signal determines whether new data from the D_{IN} pin, or recirculated output data, is presented to the input of the addressed block. The non-addressed blocks are automatically recirculated.

MODES OF OPERATION

STANDBY (Recirculate-only cycle)

In Standby mode (CS LOW), the contents of all 16 blocks are recirculated automatically, and the device disregards the $\overline{WE}$, Address, and D_{IN} inputs. The output latch goes into the high impedance state after the trailing edge of the ϕ_1 clock. Minimum power dissipation results when the device is operated in the recirculate mode with minimum ϕ_1 and ϕ_2 pulse widths at the lowest allowed frequency.

READ-RECIRCULATE MODE

In this mode of operation ($\overline{WE}$ HIGH and CS HIGH) the data from the selected block is presented to the output buffer immediately following the leading edge of ϕ_2 and appears at the output, D_{OUT}, after a delay equal to the access time t_{ACC}. Thus, the access time is referenced from the leading edge of the ϕ_2 pulse and is independent of the duration of ϕ_2. The output data is latched and remains valid at the D_{OUT} pin until the end of the ϕ_1 clock pulse in the next cycle. The data present in all 16 blocks automatically recirculates from the output back to the input regardless of the address inputs, provided that $\overline{WE}$ remains inactive throughout the cycle.

READ AND WRITE MODE

In the Read and Write mode ($\overline{WE}$ LOW and CS HIGH), the output data from the selected block is available at the output pin as in the read-recirculate mode; however, the recirculate path of that particular block is disabled. Input data present at the D_{IN} pin during ϕ_2 is written into the selected block by the falling edge of ϕ_2, while the other 15 blocks automatically recirculate their contents. This form of an "early-write" cycle ($\overline{WE}$ LOW prior to the falling edge of ϕ_1) requires that both $\overline{WE}$ and D_{IN} have set-up times with respect to the trailing edge of ϕ_1. In fact, for successive write operations handled in this mode, $\overline{WE}$ may be held LOW continuously without returning it to the HIGH state between cycles. A "delayed-write" cycle ($\overline{WE}$ goes LOW after the trailing edge of the ϕ_1 clock pulse) is also possible and is discussed in the next paragraph as a subset of the RMW operating mode.

READ-MODIFY-WRITE MODE

The Read-Modify-Write mode (CS HIGH, $\overline{WE}$ HIGH goes LOW) is simplified by the fact that the F464 is always in the read mode whenever it is selected (CS HIGH). Since the access time is referenced to the leading edge of ϕ_2 and the setup times of $\overline{WE}$ and D_{IN} are referenced to the trailing edge of ϕ_2, this mode of operation requires an extended ϕ_2 HIGH time in order to provide the required modify time. This "stretched" ϕ_2 HIGH time may be determined by the following relationship:

$$t_{\phi 2H} = t_{ACC} + t_{MOD} + t_{DS} + t_{WCL} + t_T$$

The modify time, t_{MOD}, is determined by the user and is dependent on the delays of the external logic used to modify the output data. The Read-Modify-Write (RMW) cycle time then, is given by:

$$t_{CYC} = t_{\phi 1H} + t_{UL1} + t_{\phi 2H} + t_{UL2} + 4t_{TC}$$

where $t_{\phi 2H}$ is the new "stretched" version of the ϕ_2 clock pulse.

If no modification of output data is required, then this operating mode reduces to a "delayed-write" mode in which D_{IN} and $\overline{WE}$ may occur after the ϕ_1 clock pulse.

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MEMORY START-UP

When the F464 is initially powered up, the V_{BB} supply (i.e., the –5 volt supply) should be applied to the memory before and removed after the other supplies. This action results in greater protection against accidental violation of the voltage limits specified in the Absolute Maximum Ratings section and, in general, enhances the long term reliability of the memory.

In order to clear the memory of extraneous charge following power-up or after a clock stoppage of greater than 15 μs, the F464 must be clocked through a minimum of 20,000 clock cycles of any type before a valid memory cycle should be attempted.

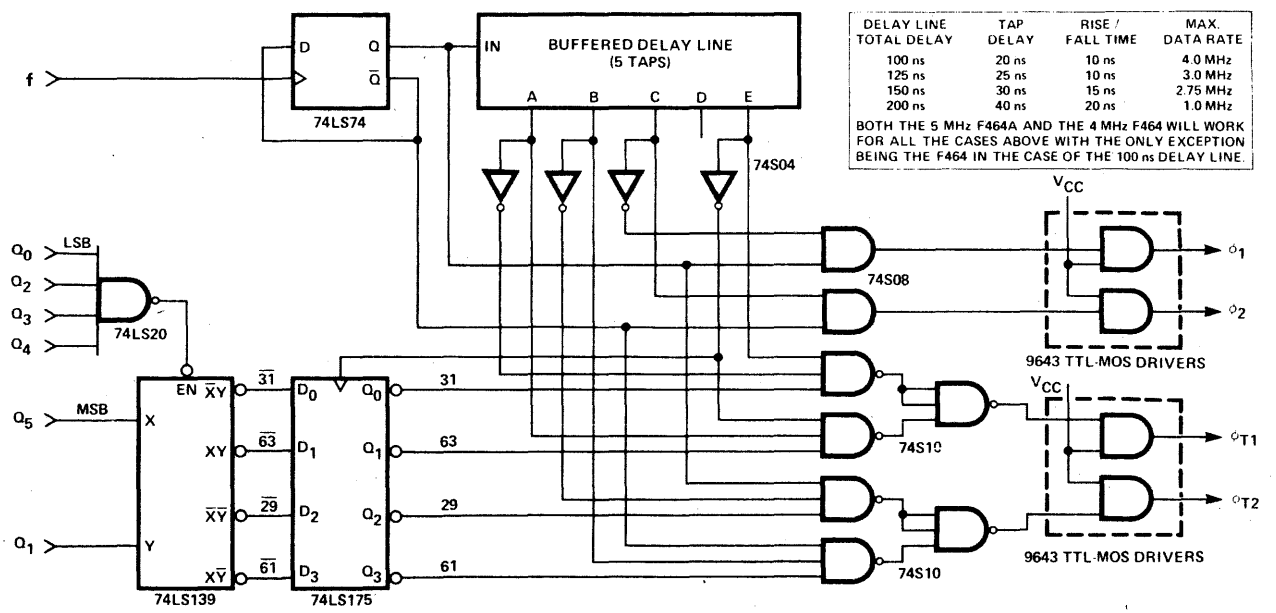
CLOCK GENERATION CIRCUIT –

The circuit shown below may be used to generate the four MOS-level clocks required of the F464 from a single master clock. In this circuit, the master clock frequency f, must be twice the desired data rate at the F464 output pin. Since the input clock frequency is "squared-up" with a divide-by-two flip-flop, the duty cycle of this clock is non-critical. A pulse edge at the input of the buffered delay line produces a sequence of delayed pulse edges from the A, B, C, D and E output taps. These delayed pulse edges are ANDed together to produce the required ϕ_1 and ϕ_2 clocks as well as the ϕ_{T1} and ϕ_{T2} transfer clocks. Since the transfer clocks occur in a symmetrical fashion every 64 clock cycles, a 6-bit, modulo 64 counter is required. The outputs of this 6-bit counter are decoded to enable the appropriate transfer clock gates at counts of 29, 31, 61 and 63. Thus, ϕ_{T1} is passed along to the clock drivers only during cycles 31 and 63, while ϕ_{T2} is gated through only during cycles 29 and 61. These four counts are easily decoded with only a 2-to-4 decoder and one 4-input NAND gate. The 6 bits of the modulo 64 counter comprise the 6 low order bits of the 12-bit, modulo 4096 loop counter. This counter is required to define address locations within each 4K block and will, in most cases, be already present in the system.

One major advantage of using a delay line is that since the clock pulses are generated from delayed edges, the pulse width in all cases is fixed and does not vary as a function of the input master frequency f. Thus minimum pulse widths are always generated regardless of cycle and data rates. This translates directly into lower power dissipation since I_{DD} is a function of clock pulse width.

The maximum clock rates for which this circuit will operate properly depends on the clock transition times (both rise and fall) at the output of the TTL-to-MOS drivers and, the delay between adjacent taps on the delay line. The maximum data rates possible for this circuit are given in the table. Faster and/or more efficient clock generation circuits may be realized by using different types of delay lines (e.g. more taps or unequal tap delays).

SERIAL AND TRANSFER CLOCK GENERATION CIRCUIT



DELAY LINE TOTAL DELAY	TAP DELAY	RISE / FALL TIME	MAX. DATA RATE
100 ns	20 ns	10 ns	4.0 MHz
125 ns	25 ns	10 ns	3.0 MHz
150 ns	30 ns	15 ns	2.75 MHz
200 ns	40 ns	20 ns	1.0 MHz

BOTH THE 5 MHz F464A AND THE 4 MHz F464 WILL WORK FOR ALL THE CASES ABOVE WITH THE ONLY EXCEPTION BEING THE F464 IN THE CASE OF THE 100 ns DELAY LINE.

Fairchild cannot assume responsibility for use of any circuitry described other than circuitry entirely embodied in a Fairchild product. No other circuit patent licenses are implied.

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F2114

1024 x 4-BIT STATIC RANDOM ACCESS MEMORY

FAIRCHILD ISOPLANAR SILICON GATE MOS INTEGRATED CIRCUIT

GENERAL DESCRIPTION – The Fairchild F2114 is a 4096-bit static Random Access Memory organized as 1024 words by four bits each. Since the operation of the F2114 is entirely static, there is no clocking or refreshing required. It operates from a single +5 V supply and is directly TTL compatible at all inputs and outputs including the four bi-directional data I/O pins.

It is designed for memory applications in which static operation, large bit capacity, and simple interfacing are important design considerations.

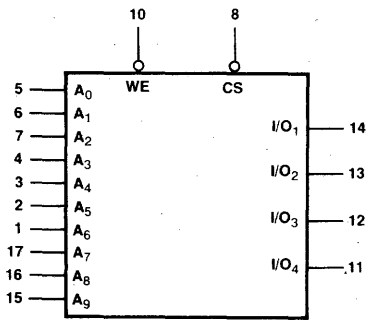
The F2114 is manufactured using Fairchild's n-channel silicon gate Isoplanar process. The innovative use of polysilicon resistors in the static memory cell design permit a high bit packing density and insures low-power characteristics. It is available in standard 18-pin dual in-line packages in either plastic or ceramic.

- **1024 X 4 BIT ORGANIZATION**
- **STANDARD 18-PIN DIP PACKAGE**
- **SINGLE +5 V SUPPLY**
- **COMPLETELY STATIC – NO CLOCKS OR REFRESH**
- **TOTALLY TTL COMPATIBLE**
- **COMMON DATA I/O PINS WITH 3-STATE CAPABILITY**
- **IDENTICAL CYCLE AND ACCESS TIMES**
- **SIMPLE BUS INTERFACING USING CHIP SELECT AND WRITE ENABLE**

PIN NAMES

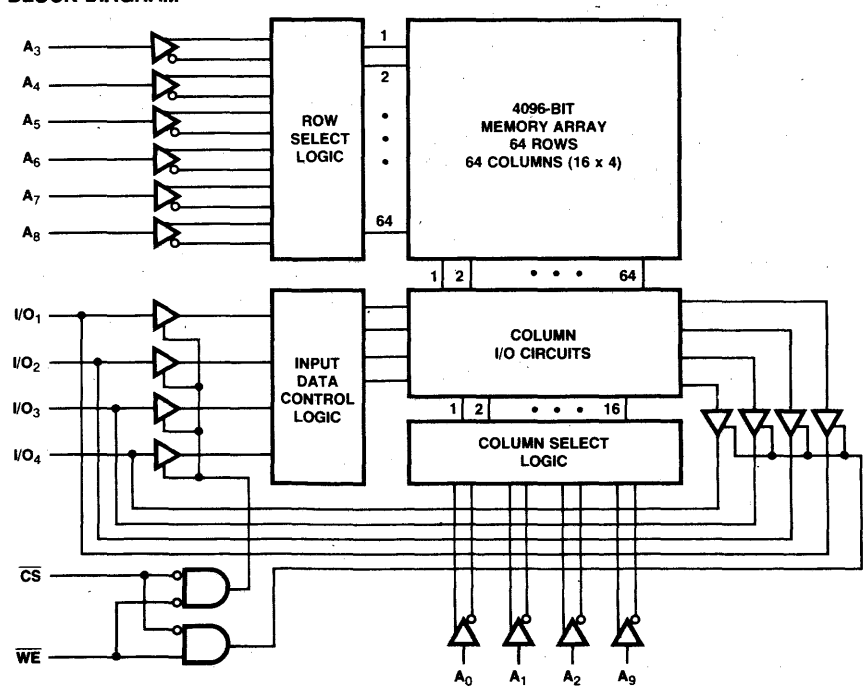
A_0-A_9	Address Inputs
$\overline{CS}$	Chip Select (Active LOW)
$\overline{WE}$	Write Enable (Active LOW)
I/O_1-I/O_4	Data Input/Output
V_{CC}	+5 V Power Supply
GND	Ground

LOGIC SYMBOL

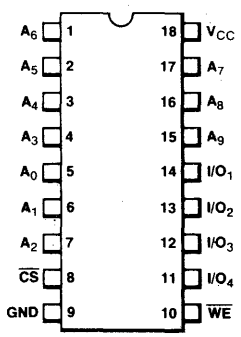


V_{CC} = Pin 18
GND = Pin 9

BLOCK DIAGRAM



CONNECTION DIAGRAM
DIP (TOP VIEW)



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FAIRCHILD

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F2708

1024 x 8 UV ERASABLE PROM

FAIRCHILD ISOPLANAR SILICON GATE NMOS

GENERAL DESCRIPTION — The Fairchild F2708 is an 8,192-bit ultraviolet light erasable and electrically reprogrammable Read Only Memory manufactured using the Isoplanar n-channel silicon gate technology. Organized 1024 x 8, the F2708 is ideally suited for non-volatile data storage in applications such as 8-bit microprocessor systems, where reprogrammability, high bit density, maximum performance, and simple interfacing are essential parameters. All inputs and outputs are TTL compatible. The 3-state outputs become high impedance when the F2708 is deselected, allowing a direct interface capability which is useful in many computer bus structures.

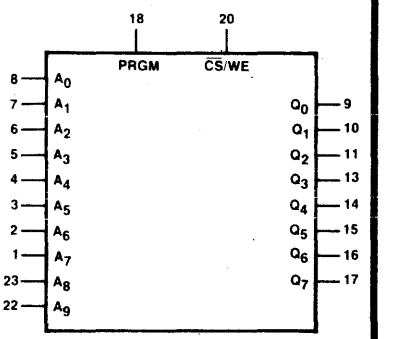
The F2708, which is pin-for-pin compatible with industry-standard 8K-bit ROMs, provides inexpensive, non-volatile storage of data/program code in applications where fast turn-around and data/program code experimentation are important requirements. Thus, the F2708 provides the system development vehicle whereby system prototypes using the F2708 may be released into volume production by directly substituting ROM devices for F2708 devices.

- **1024 x 8 BITS ORGANIZATION**
- **FAST ACCESS TIME: 350 nx MAX (F2708-1)**
- **TTL COMPATIBLE ON INPUTS AND OUTPUTS**
- **3-STATE OUTPUTS FOR OR-TIE CAPABILITY**
- **STANDARD POWER SUPPLIES +12V, +5V, −5V**
- **CHIP SELECT INPUT FOR MEMORY EXPANSION**
- **STATIC OPERATION**
- **PIN COMPATIBLE TO 8K AND 16K ROMs FOR LOW COST PRODUCTION**
- **LOW POWER DURING PROGRAMMING**
- **CONTENTS ERASABLE WITH ULTRAVIOLET LIGHT**

PIN NAMES

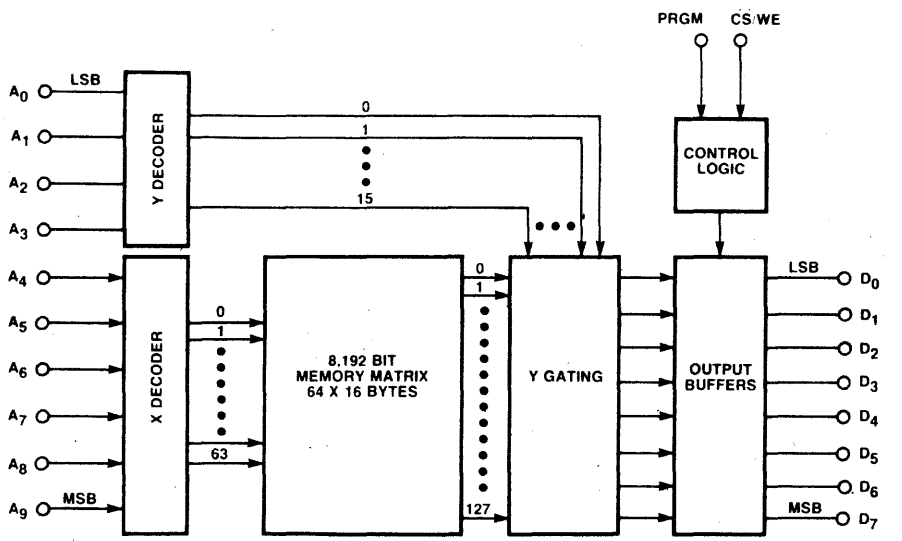
A_n	Address Inputs (10)
Q_n	Output Data (8)
PRGM	Program Pulse Input
$\overline{CS}$/WE	Chip Select/Write Enable
V_{DD}	+12 V Supply
V_{CC}	+5 V Supply
V_{SS}	Ground
V_{BB}	−5 V Supply

LOGIC SYMBOL

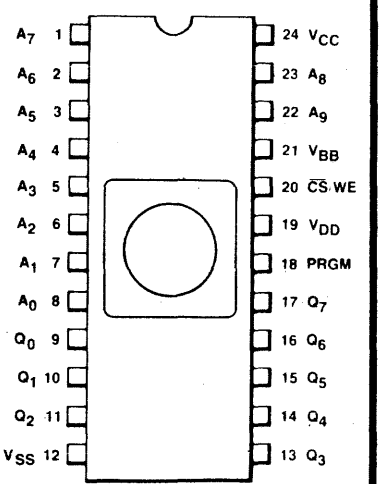


V_{DD} = Pin 19
V_{CC} = Pin 24
V_{BB} = Pin 21
V_{SS} = Pin 12

BLOCK DIAGRAM



CONNECTION DIAGRAM
DIP (TOP VIEW)



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FAIRCHILD

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MEMORY

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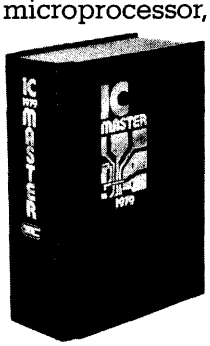
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HM-76XX

GENERIC PROM FAMILY

Features

- COMMON D.C. ELECTRICAL CHARACTERISTICS AND PROGRAMMING PROCEDURE
- SIMPLE, HIGH SPEED PROGRAMMING PROCEDURE, ONE PULSE/BIT
- EXPANDABLE - "OPEN COLLECTOR" OR "THREE STATE" OUTPUTS AND CHIP ENABLE INPUTS
- INPUTS AND OUTPUTS TTL COMPATIBLE
  - LOW INPUT CURRENT – 250μA LOGIC "0", 40μA LOGIC "1"
  - FULL OUTPUT DRIVE – 16 mA SINK, 2mA SOURCE
- FAST ACCESS TIME – GUARANTEED FOR WORST CASE N^2 SEQUENCING, OVER COMMERCIAL AND MILITARY TEMPERATURE AND VOLTAGE RANGES
- PIN COMPATIBLE WITH INDUSTRY STANDARD PROMs AND ROMs

Organizations

PART NUMBER	*OUTPUT	TOTAL BITS	WORDS x BITS/WORD
HM-7602 HM-7603	OC TS	256	32 x 8
HM-7610 HM-7611	OC TS	1024	256 x 4
HM-7620 HM-7621	OC TS	2048	512 x 4
HM-7640 HM-7641	OC TS	4096	512 x 8
HM-7642 HM-7643 HM-7644	OC TS APU	4096	1024 x 4

*OC Open Collector
*TS *Three State*
*APU Active Pull-Up

Description

The HM-76XX Generic PROMs comprise a completely compatible family having common D.C. electrical characteristics and identical programming requirements. They are fully decoded, high speed, field programmable ROMs and are available in all commonly used organizations, with both open-collector and "Three State" outputs. All bits are manufactured storing a logical "1" (outputs high), and can be selectively programmed for a logical "0" (outputs low).

The nichrome fuse technology is the same as is used in the JAN approved MIL-STD-38510/201 PROM and in all other Harris PROMs.

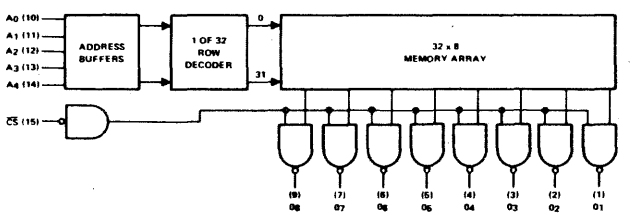
The field programmable PROM can be custom programmed to any pattern using a simple programming procedure. Schottky Bipolar circuitry provides fast access time, and features temperature and voltage compensation to minimize access time variation.

All pinouts are compatible to industry standard PROMs and ROMs.

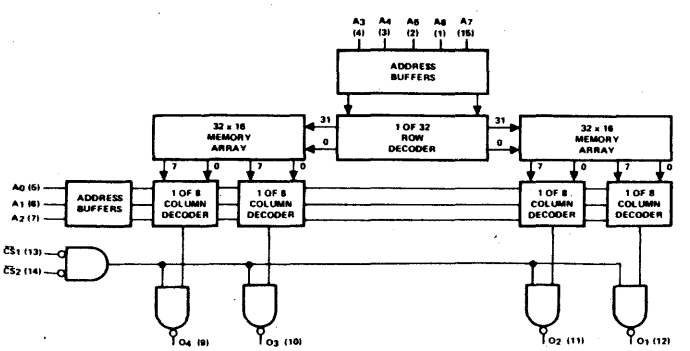
In addition to the conventional storage array, extra test rows and columns are included to assure high programmability, and guarantee parametric and A.C. performance. Fuses in these test rows and columns are blown prior to shipment.

Block Diagrams

HM-7602/03
32 x 8



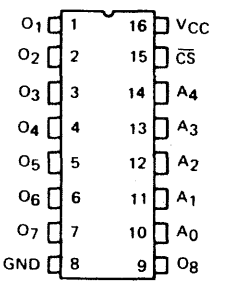
HM-7610/11
256 x 4



Pinouts

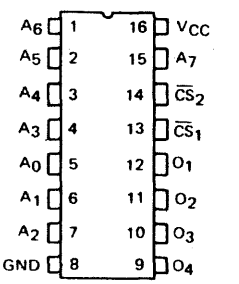
HM-7602/03
32 x 8

TOP VIEW



HM-7610/11
256 x 4

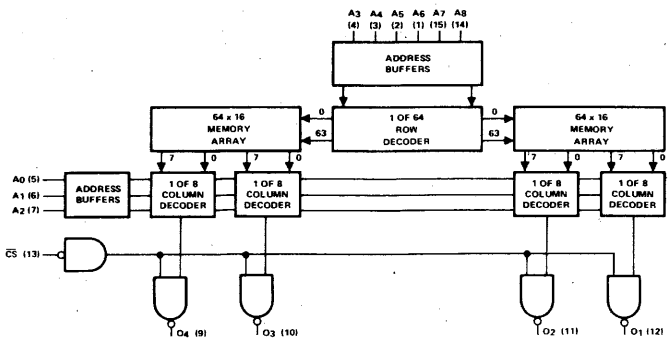
TOP VIEW



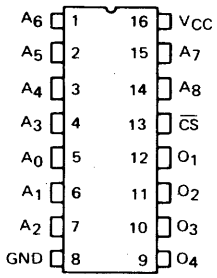
"SEE PAGES 1409-1415 FOR PACKAGE SELECTION GUIDE"

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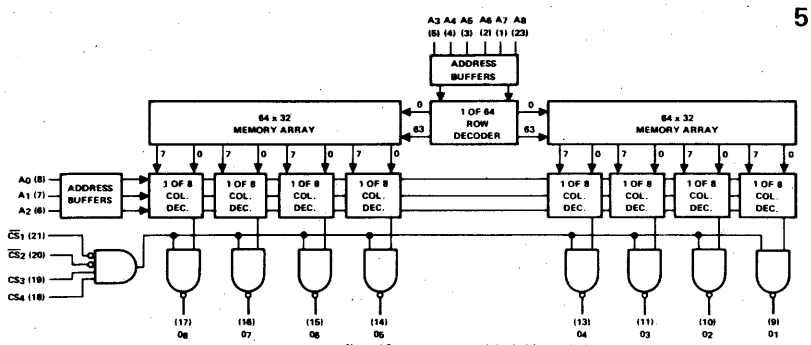
HM-7620/21
512 x 4



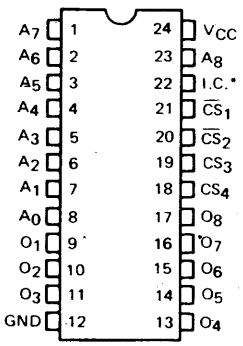
TOP VIEW



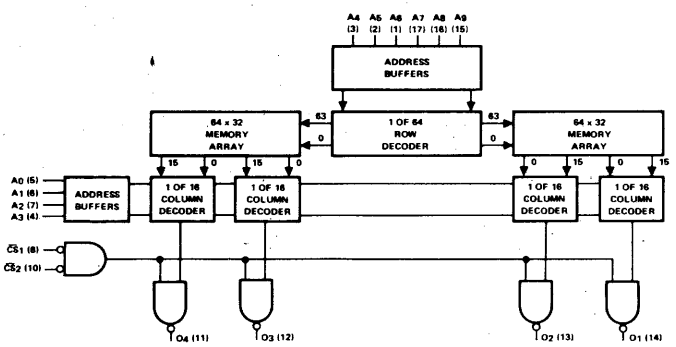
HM-7640/41
512 x 8



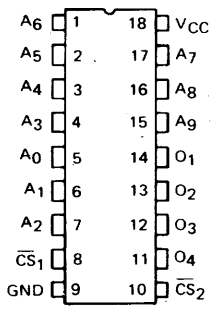
TOP VIEW



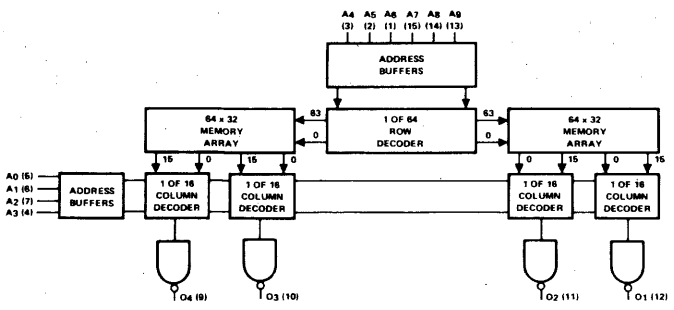
HM-7642/43
1024 x 4



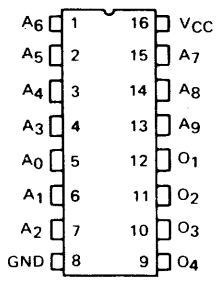
TOP VIEW



HM-7644
1024 x 4



TOP VIEW



ABSOLUTE MAXIMUM RATINGS

Output or Supply Voltage (Operating)	-0.3 to +7.0V	Storage Temperature	-65°C to +150°C
Address/Enable Input Voltage	5.5V	Operating Temperature (Ambient)	-55°C to +125°C
Address/Enable Input Current	-20mA	Maximum Junction Temperature	+175°C
Output Sink Current	100mA		

CAUTION: Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied. (While programming, follow the programming specifications.)

D.C. ELECTRICAL CHARACTERISTICS (Operating)

HM-76XX-5 (V_{CC} = 5.0V ±5%, T_A = 0°C to +75°C)
HM-76XX-2, HM-76XX-8 (V_{CC} = 5.0V ±10%, T_A = -55°C to +125°C)
Typical Measurements are at T_A = 25°C, V_{CC} = +5V

SYMBOL	PARAMETER	OPEN COLLECTOR OUTPUT MIN	OPEN COLLECTOR OUTPUT TYP	OPEN COLLECTOR OUTPUT MAX	THREE STATE OUTPUT MIN	THREE STATE OUTPUT TYP	THREE STATE OUTPUT MAX	UNITS	TEST CONDITIONS
I_{IH} I_{IL}	Address/Enable Input Current (1) "1" "0"	– –	 -50.0	40 -250	– –	 -50.0	40 -250	µA µA	V_{IH} = V_{CC} Max. V_{IL} = 0.45V
V_{IH} V_{IL}	Input Threshold Voltage "1" "0"	2.0 –	– –	 0.8	2.0 –	– –	 0.8	V V	V_{CC} = V_{CC} Min. V_{CC} = V_{CC} Max.
V_{OH} V_{OL}	Output Voltage "1" "0"	N/A 	 0.35	 0.45	2.4 	3.4 0.35	 0.45	V V	I_{OH} = -2.0mA, V_{CC} = V_{CC} Min. I_{OL} = +16mA, V_{CC} = V_{CC} Min.
I_{OHE} I_{OLE}	Output Disabled Current (2) "1" "0"	– –	– –	100 N/A	– –	– –	100 -100	µA µA	V_{OH}, V_{CC} = V_{CC} Max. V_{OL} = +0.3V, V_{CC} = V_{CC} Max.
I_{OH}	Output Leakage (1) "1"	–	–	100	–	–	N/A	µA	V_{OH}, V_{CC} = V_{CC} Max.
V_{CL}	Input Clamp Voltage	–	–	-1.2	–	–	-1.2	V	I_{IN} = -18mA
I_{OS}	Output Short Circuit Current	N/A	–	N/A	-15	–	-100	mA	V_{OUT} = 0.0V One Output Only for a Max. of 1 sec.
I_{CC}	Power Supply Current HM-7602/7603 HM-7610/7611 HM-7620/7621	– –	90 90	105 130	– –	90 90	105 130	mA	V_{CC} = V_{CC} Max. All Inputs Grounded
	HM-7640/7641	–	125	170	–	125	170	mA	
	HM-7642/7643/7644	–	100	140	–	100	140	mA	

NOTE: (1) Enable current measured using only one enable input to disable the device.
(2) N/A for HM-7644, Active Pull-Up Output.

A.C. ELECTRICAL CHARACTERISTICS (Operating)

SYMBOL	PARAMETER	HM-76XX-5 V_{CC} – 5V ±5% T_A – 0° to +75°C TYPICAL	HM-76XX-5 MAXIMUM	HM-76XX-2 HM-76XX-8 V_{CC} – 5V ± 10% T_A – -55°C to +125°C TYPICAL	HM-76XX-2 HM-76XX-8 MAXIMUM	UNITS
T_{AA} T_{EA}	HM-7602/7603	30 20	40 30	30 20	50 40	ns ns
T_{AA} T_{EA}	HM-7610/7611	40 15	60 25	40 15	75 30	ns ns
T_{AA} T_{EA}	HM-7620/7621	45 15	70 25	45 15	85 30	ns ns
T_{AA} T_{EA}	HM-7640/7641	45 30	70 40	45 30	85 50	ns ns
T_{AA} T_{EA}	HM-7642/7643 HM-7644	45 15	60 25	45 15	85 30	ns ns

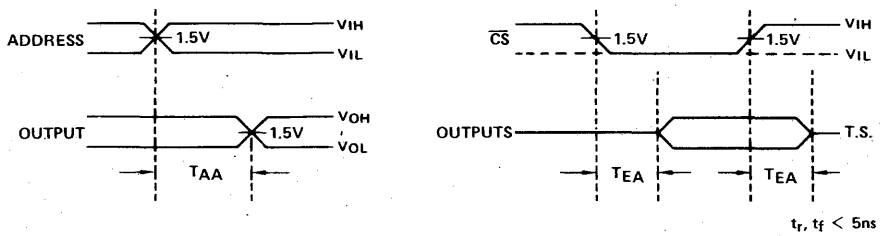
T_{AA} – Address to Output Access Time
T_{EA} – Chip Enable Access Time (N/A HM-7644)
A.C. Limits Guaranteed for Worst Case N^2 Sequencing

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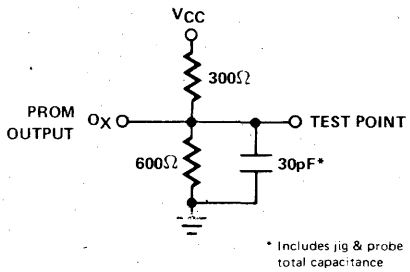
CAPACITANCE: $T_A = 25^oC$

SYMBOL	PARAMETER	MAXIMUM	UNITS	TEST CONDITIONS
CINA, CINCS	Input Capacitance	12	pF	VCC = 5V, VIN = 2.0V, f = 1MHz
COUT	Output Capacitance	12	pF	VCC = 5V, VOUT = 2.0V, f = 1MHz

SWITCHING TIME DEFINITIONS

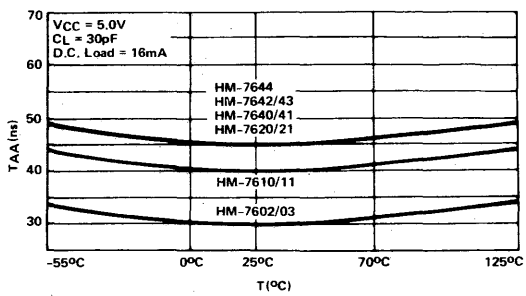


A.C. TEST LOAD

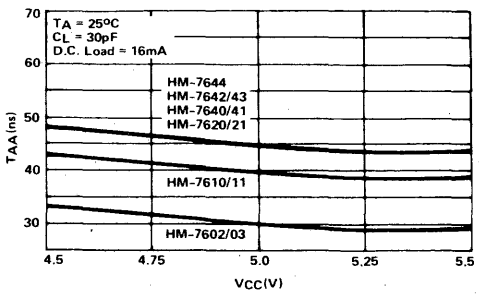


TYPICAL A.C. CHARACTERISTICS

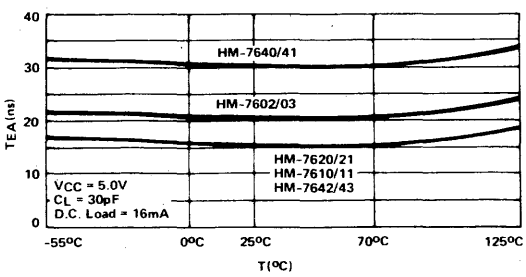
ADDRESS TO OUTPUT DELAY VS. TEMPERATURE



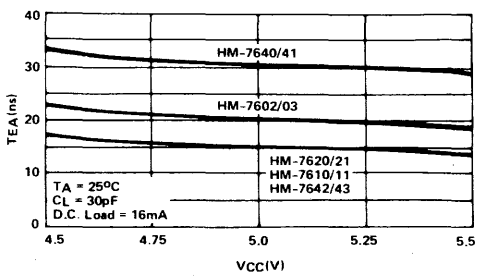
ADDRESS TO OUTPUT DELAY VS. SUPPLY VOLTAGE



CHIP SELECT TO OUTPUT DELAY VS. TEMPERATURE



CHIP SELECT TO OUTPUT DELAY VS. SUPPLY VOLTAGE



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HM-76LS03

32 x 8 PROM
"Three State" Outputs

Preliminary

Features

- ULTRA LOW POWER - 60mW TYPICAL
- SIMPLE HIGH SPEED PROGRAMMING PROCEDURE - ONE PULSE/BIT TYPICAL, ASSURES FAST PROGRAMMING AND SUPERIOR RELIABILITY.
- INDUSTRY'S HIGHEST PROGRAMMING YIELD.
- PIN COMPATIBLE WITH THE STANDARD 7603 PINOUT.

Description

The HM-76LS03 is an ultra low power version of the standard 7603 PROM, designed to be MOS compatible with it's low ICC specification. The HM-76LS03 is a fully decoded high speed Schottky TTL 256-Bit Field Programmable ROM in a 32 word by 8 bit/word format with "Three State" outputs. This PROM is available in a 16 pin DIP (ceramic or epoxy).

All bits are manufactured storing a logical "1" (positive logic) and can be selectively programmed for a logical "0" in any bit position.

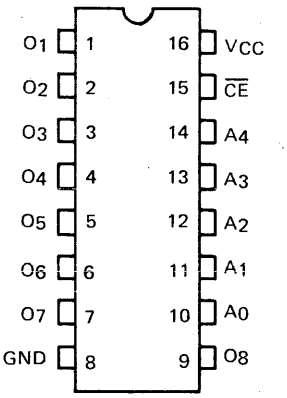
Nichrome fuse technology is used on this and all other Harris Bipolar PROMs.

The HM-76LS03 contains test rows and columns which are in addition to the storage array to assure high programmability and guarantee parametric and A.C. performance. The fuses in these test rows and columns are blown prior to shipment.

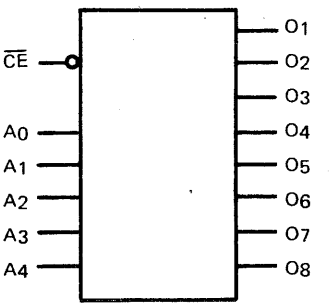
There is a Chip Enable on the HM-76LS03, $\overline{CE}$ low enables the device.

Pinout

TOP VIEW—DIP



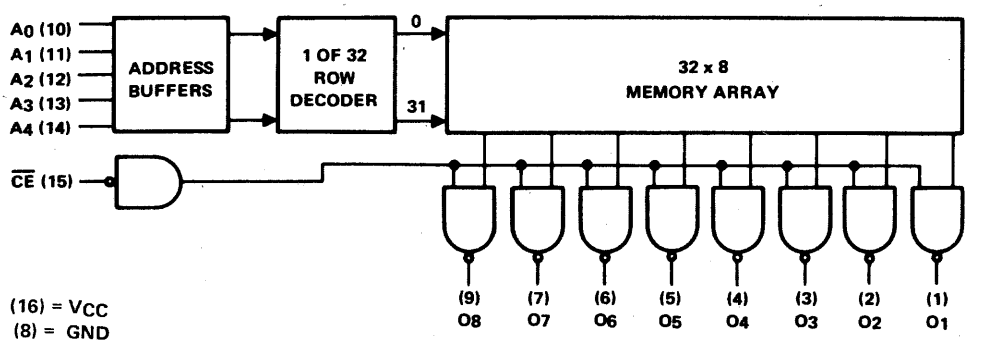
Logic Symbol



PIN NAMES

A0 - A4	Address Inputs
O1 - O8	Data Outputs
$\overline{CE}$	Chip Enable Input

Functional Diagram



"SEE PAGES 1409-1415 FOR PACKAGE SELECTION GUIDE"

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ABSOLUTE MAXIMUM RATINGS

Output or Supply Voltage Ratings (Operating)	-0.3 to +7.0V	Storage Temperature	-65°C to +150°C
Address/Enable Input Voltage	+5.5V	Operating Temperature (Ambient)	0°C to +75°C
Address/Enable Input Current	-20mA	Maximum Junction Temperature	+175°C
Output Sink Current	100mA		

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied. (While programming, follow the programming specifications)

D.C. ELECTRICAL CHARACTERISTICS (Operating)

HM-76LS03-5 (V_{CC} = 5.0V ± 5%, T_A = 0°C to +75°C)

SYMBOL	PARAMETER		MIN	TYP	MAX	UNITS	TEST CONDITIONS
I_{IH} I_{IL}	Address/Enable Input Current	"1" "0"	— —	— —	+40 -50	uA uA	V_{IH} = V_{CC} max V_{IL} = 0.45V
V_{IH} V_{IL}	Input Threshold Voltage	"1" "0"	2.0 —	1.5 1.5	— 0.80	V V	V_{CC} = V_{CC} min V_{CC} = V_{CC} max
V_{OH} V_{OL}	Output Voltage	"1" "0"	2.4 —	3.4 0.34	— 0.45	V V	I_{OH} = -0.20mA V_{CC} = V_{CC} min. I_{OL} = +1.0mA V_{CC} = V_{CC} min.
I_{OHE} I_{OLE}	Output Disable Current	"1" "0"	— —	— —	+100 -100	uA uA	V_{OH}, V_{CC} = V_{CC} max V_{OL} = +0.3V V_{CC} = V_{CC} max
V_{CL}	Input Clamp Voltage		—	—	-1.2	V	I_{IN} = -18mA
I_{OS}	Output Short Circuit Current		-2	—	-20	mA	V_{OUT} = 0.0V one output only for a max of one second.
I_{CC}	Power Supply Current		—	12	25	mA	V_{CC} = V_{CC} max all inputs grounded

Typical measurements are at T_A = 25°C, V_{CC} = +5V
NOTE: Positive current defined as into the device terminals.

A.C. ELECTRICAL CHARACTERISTICS (Operating)

		HM-76LS03-5 5V ± 5% 0°C to +75°C			
SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
T_{AA} T_{EA}	Address Access Time Chip Enable Access Time	— —	300 300	500 500	ns ns

A.C. limits guaranteed for worst case N^2 sequencing.

CAPACITANCE: T_A = 25°C

SYMBOL	PARAMETER	MAX	UNIT	TEST CONDITIONS
C_{INA}, C_{INCE} C_{OUT}	Input Capacitance Output Capacitance	12 12	pF pF	V_{CC} = 5V, V_{IN} = 2.0, f = 1MHz V_{CC} = 5V, V_{OUT} = 2.0, f = 1MHz

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HM-7608

1K x 8 PROM

Preliminary

Features

- 60ns MAXIMUM ADDRESS ACCESS TIME
- "THREE STATE" OUTPUTS WITH A CHIP ENABLE INPUT
- SIMPLE, HIGH SPEED PROGRAMMING PROCEDURE – ONE PULSE/BIT. ASSURES FAST PROGRAMMING AND SUPERIOR RELIABILITY.
- FAST ACCESS TIME – GUARANTEED FOR WORST CASE N^2 SEQUENCING OVER COMMERCIAL AND MILITARY TEMPERATURE AND VOLTAGE RANGES.
- INDUSTRY'S HIGHEST PROGRAMMING YIELD
- PIN COMPATIBLE WITH THE 2708 WITH:
  - ONLY ONE 5 VOLT SUPPLY
  - SUPERIOR ACCESS TIME
  - FASTER PROGRAMMING TIME

Description

The HM-7608 is a fully decoded high speed Schottky TTL 8192-Bit Field Programmable ROM in a 1K word by 8 bit/word format and is available in a 24 pin D.I.P. (ceramic or epoxy) and a 24 pin flat pack.

All bits are manufactured storing a logical "1" (Positive Logic) and can be selectively programmed for a logical "0" in any bit position, the HM-7608 has "Three State" outputs.

Nichrome fuse technology is used on this and all other Harris Bipolar PROM's.

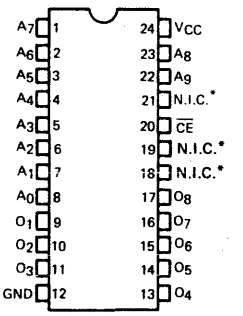
The HM-7608 contains test rows and columns which are in addition to the storage array to assure high programmability and guarantee parametric and A.C. performance. The fuses in these test rows and columns are blown prior to shipment.

This PROM is a plug in replacement for the 2708 where the V_{SS} pin on the 2708 becomes GND on the HM-7608. The V_{BB}, VDD, and program pins on the 2708 are all N.C. on the HM-7608.

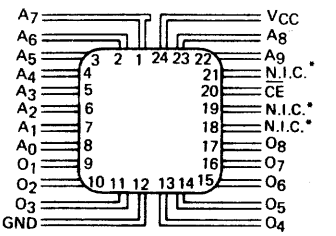
There is a chip enable input on the HM-7608 where $\overline{CE}$ low enables the device.

Pinouts

TOP VIEW – DIP



TOP VIEW – FLATPACK

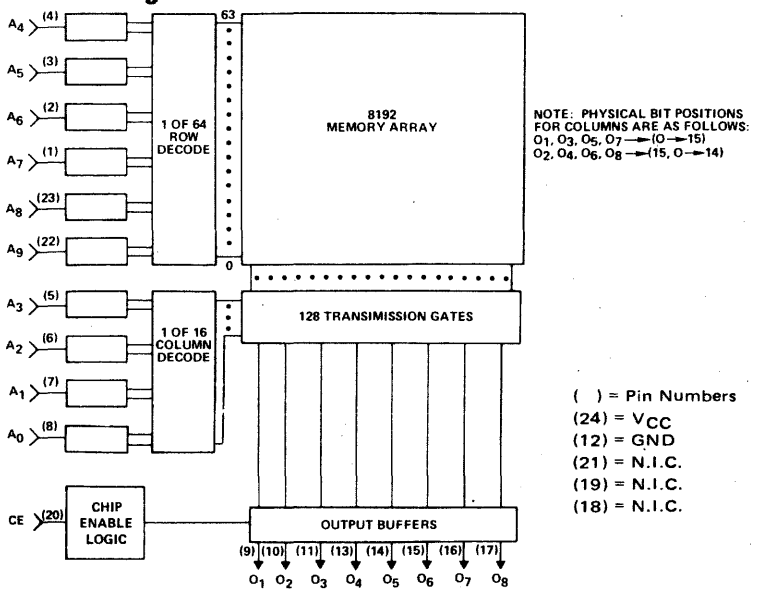


PIN NAMES

$A_0 - A_9$	Address Inputs
$O_1 - O_8$	Data Outputs
$\overline{CE}$	Chip Enable Input

*No Internal Connect

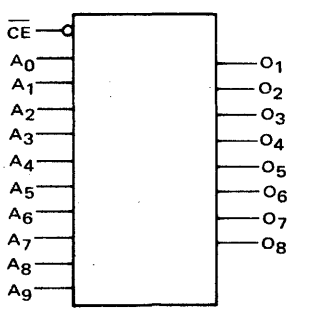
Functional Diagram



NOTE: PHYSICAL BIT POSITIONS FOR COLUMNS ARE AS FOLLOWS:
$O_1, O_3, O_5, O_7 \rightarrow (0 \rightarrow 15)$
$O_2, O_4, O_6, O_8 \rightarrow (15, 0 \rightarrow 14)$

( ) = Pin Numbers
(24) = V_{CC}
(12) = GND
(21) = N.I.C.
(19) = N.I.C.
(18) = N.I.C.

Logic Symbol



"SEE PAGES 1409-1415 FOR PACKAGE SELECTION GUIDE"

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ABSOLUTE MAXIMUM RATINGS

Output or Supply Voltage (Operating)	-0.3 to +7.0V	Storage Temperature	-65°C to +150°C
Address/Enable Input Voltage	5.5V	Operating Temperature (Ambient)	-55°C to +125°C
Address/Enable Input Current	-20mA	Maximum Junction Temperature	+175°C
Output Sink Current	100mA		

CAUTION: Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied. (While programming, follow the programming specifications.)

D.C. ELECTRICAL CHARACTERISTICS (Operating)

HM-7608-5 (V_{CC} = 5.0V ±5%, T_A = 0°C to +75°C)
HM-7608-2 (V_{CC} = 5.0V ±10%, T_A = -55°C to +125°C)
Typical measurements are at T_A = 25°C, V_{CC} = +5V

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
I_{IH}	Address/enable "1"	–	–	+40	µA	V_{IH} = V_{CC} Max.
I_{IL}	Input Current "0"	–	-50.0	-100	µA	V_{IL} = 0.45V
V_{IH}	Input Threshold "1"	2.0	1.5	–	V	V_{CC} = V_{CC} Min.
V_{IL}	Voltage "0"	–	1.5	0.8	V	V_{CC} = V_{CC} Max.
V_{OH}	Output "1"	2.4	3.2	–	V	I_{OH} = -2.0mA, V_{CC} = V_{CC} Min.
V_{OL}	Voltage "0"	–	0.35	0.45	V	I_{OL} = +16mA, V_{CC} = V_{CC} Min.
I_{OHE}	Output Disable "1"	–	–	+40	µA	V_{OH}, V_{CC} = V_{CC} Max.
I_{OLE}	Current "0"	–	–	-40	µA	V_{OL} = 0.3V, V_{CC} = V_{CC} Max.
V_{CL}	Input Clamp Voltage	–	–	-1.2	V	I_{IN} = -18mA
I_{OS}	Output S.C. Current	-15	–	-100	mA	V_{OUT} = 0.0V One Output Only for a Max. of 1 Second
I_{CC}	Power Supply Current	–	130	170	mA	V_{CC} = V_{CC} Max. All Inputs Grounded

NOTE: Positive current defined as into device terminals.

A.C. ELECTRICAL CHARACTERISTICS (Operating)

		HM-7608-5 5V ±5% 0°C to + 75°C			HM-7608-2 5V ±10% -55°C to +125°C			
SYMBOL	PARAMETER	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
T_{AA}	Address Access Time	–	45	60	–	–	80	ns
T_{EA}	Chip Enable Access Time	–	30	40	–	–	50	ns

A.C. limits guaranteed for worst case N^2 sequencing.

CAPACITANCE : T_A = 25°C

SYMBOL	PARAMETER	MAXIMUM	UNITS	TEST CONDITIONS
C_{INA}, C_{INCE}	Input Capacitance	8	pF	V_{CC} = 5V, V_{IN} = 2.0V, f = 1MHz
C_{OUT}	Output Capacitance	10	pF	V_{CC} = 5V, V_{OUT} = 2.0V, f = 1MHz

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HM-7610A/11A

256 x 4 PROM

HM-7610A - Open Collector Outputs
HM-7611A - "Three State" Outputs

Features

- 40ns MAXIMUM ADDRESS ACCESS TIME
- "THREE STATE" OR OPEN COLLECTOR OUTPUTS
- SIMPLE, HIGH SPEED PROGRAMMING PROCEDURE USING SINGLE PULSES, ASSURES FAST PROGRAMMING AND SUPERIOR RELIABILITY
- INPUTS AND OUTPUTS TTL COMPATIBLE
- FAST ACCESS TIME – GUARANTEED FOR WORST CAST N^2 SEQUENCING OVER COMMERCIAL AND MILITARY TEMPERATURE AND VOLTAGE RANGES.
- INDUSTRY'S HIGHEST PROGRAMMING YIELD
- PIN COMPATIBLE WITH INDUSTRY STANDARD PROM's AND ROM's

Description

The HM-7610A/11A are fully decoded high speed Schottky TTL 1024-Bit Field Programmable ROMs in a 256 word by 4 bit/word format with open collector (HM-7610A) or "three state" (HM-7611A) outputs. These PROMs are available in 16 pin D.I.P. (ceramic or epoxy) and a 16 pin flatpack.

All bits are manufactured storing a logical "1" (positive logic) and can be selectively programmed for a logical "0" in any bit position.

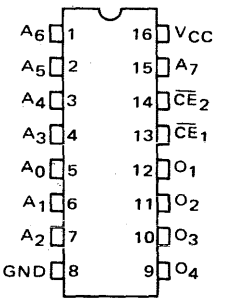
The HM-7610A/11A contain test rows and columns which are in addition to the storage array to assure high programmability and guarantee parametric and A.C. performance. The fuses in these test rows and columns are blown prior to shipment.

This PROM is intended for use in state of the art ultra high speed logic systems.

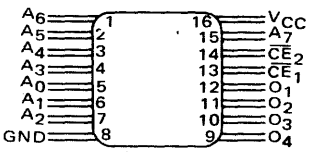
Nichrome fuse technology is used on these and all other Harris Bipolar PROM's.

Pinouts

TOP VIEW–DIP



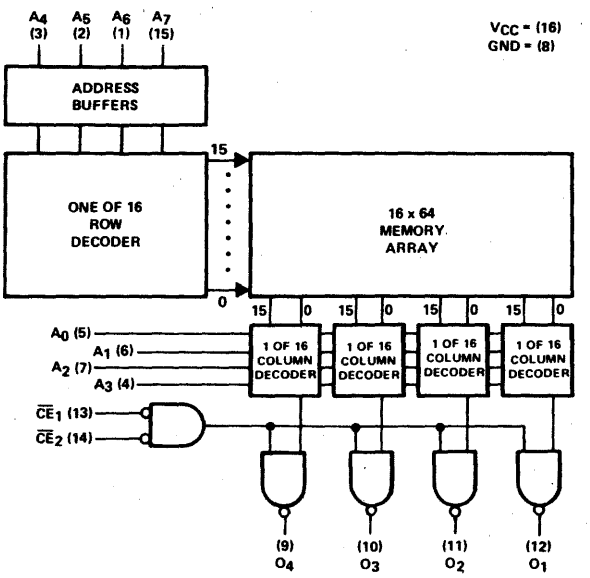
TOP VIEW–FLAT PACK



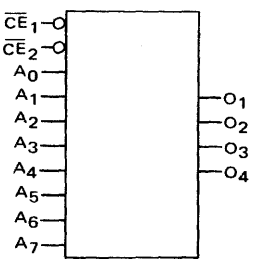
PIN NAMES

$A_0 - A_7$	Address Inputs
$O_1 - O_4$	Data Outputs
$\overline{CE}_1, \overline{CE}_2$	Chip Enable Inputs

Functional Diagram



Logic Symbol



"SEE PAGES 1409-1415 FOR PACKAGE SELECTION GUIDE"

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ABSOLUTE MAXIMUM RATINGS

Output or Supply Voltage (Operating)	-0.3 to +7.0V	Storage Temperature	-65°C to +150°C
Address/Enable Input Voltage	5.5V	Operating Temperature (Ambient)	-55°C to +125°C
Address/Enable Input Current	-20mA	Maximum Junction Temperature	+175°C
Output Sink Current	100mA		

CAUTION: Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied. (While programming, follow the programming specifications.)

D.C. ELECTRICAL CHARACTERISTICS (Operating)

HM-7610A/11A-5 (V_{CC} = 5.0V ±5%, T_A = 0°C to +75°C)
HM-7610A/11A-2 (V_{CC} = 5.0V ±10%, T_A = -55°C to +125°C)
Typical measurements are at T_A = 25°C, V_{CC} = +5V

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
I_{IH}	Address/Enable "1"	–	–	+40	μA	V_{IH} = V_{CC} Max.
I_{IL}	Input Current "0"	–	-50.0	-250	μA	V_{IL} = 0.45V
V_{IH}	Input Threshold "1"	2.0	1.5	–	V	V_{CC} = V_{CC} Min.
V_{IL}	Voltage "0"	–	1.5	0.8	V	V_{CC} = V_{CC} Max.
V_{OH}	Output "1"	2.4*	3.2*	–	V	I_{OH} = -2.0mA, V_{CC} = V_{CC} Min.
V_{OL}	Voltage "0"	–	0.35	0.45	V	I_{OL} = +16mA, V_{CC} = V_{CC} Min.
I_{OHE}	Output Disable "1"	–	–	+40	μA	V_{OH}, V_{CC} = V_{CC} Max.
I_{OLE}	Current "0"	–	–	-40*	μA	V_{OL} = 0.3V, V_{CC} = V_{CC} Max.
V_{CL}	Input Clamp Voltage	–	–	-1.2	V	I_{IN} = -18mA
I_{OS}	Output S.C. Current *	-15*	–	-100*	mA	V_{OUT} = 0.0V One Output Only for a Max. of 1 Second
I_{CC}	Power Supply Current	–	–	130	mA	V_{CC} = V_{CC} Max. All Inputs Grounded

*Not applicable to open collector.
NOTE: Positive current defined as into device terminals.

A.C. ELECTRICAL CHARACTERISTICS (Operating)

		HM-7610A/11A-5 5V ±5% 0°C to + 75°C			HM-7610A/11A-2 5V ±10% -55°C to +125°C			
SYMBOL	PARAMETER	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
T_{AA}	Address Access Time	–	–	40	–	–	60	ns
T_{EA}	Chip Enable Access Time	–	–	25	–	–	40	ns

A.C. limits guaranteed for worst case N^2 sequencing.

CAPACITANCE: T_A = 25°C

SYMBOL	PARAMETER	MAXIMUM	UNITS	TEST CONDITIONS
C_{INA}, C_{INCE}	Input Capacitance	8	pF	V_{CC} = 5V, V_{IN} = 2.0V, f = 1MHz
C_{OUT}	Output Capacitance	10	pF	V_{CC} = 5V, V_{OUT} = 2.0V, f = 1MHz

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HM-7616
2K x 8 PROM

Preview

Features

- 60ns MAXIMUM ADDRESS ACCESS TIME
- "THREE STATE" OUTPUTS AND A CHIP ENABLE INPUT
- SIMPLE HIGH SPEED PROGRAMMING PROCEDURE – ONE PULSE/BIT TYPICAL
- FAST ACCESS TIME – GUARANTEED FOR WORST CASE N^2 SEQUENCING OVER COMMERCIAL AND MILITARY TEMPERATURE AND VOLTAGE RANGES
- INDUSTRY'S HIGHEST PROGRAMMING YIELD
- PIN COMPATIBLE WITH THE 2716

Description

HM-7616 is a fully decoded high speed Schottky TTL, 16,384 bit Field Programmable ROM in a 2K word by 8 bit/word format with "Three State" outputs. This PROM is available in a 24 pin DIP.

All bits are manufactured storing a logical "1" (Positive Logic) and can be selectively programmed for a logical "0" in any bit position.

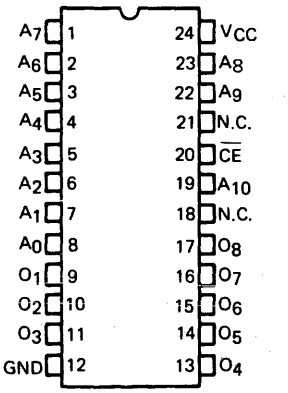
The nichrome fuse technology used is the same as all other Harris Bipolar PROMs and the JAN approved MIL-M-38510/201 PROM.

The HM-7616 contains test rows and columns which are in addition to the storage array to assure high programmability and guarantee parametrics and A.C. performance. The fuses in these test rows and columns are blown prior to shipment.

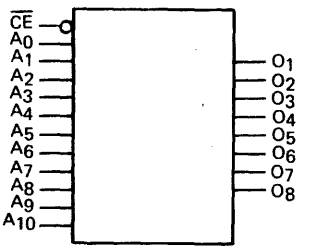
There is a chip enable input on the HM-7616. $\overline{CE}$ low enables the device.

Pinout

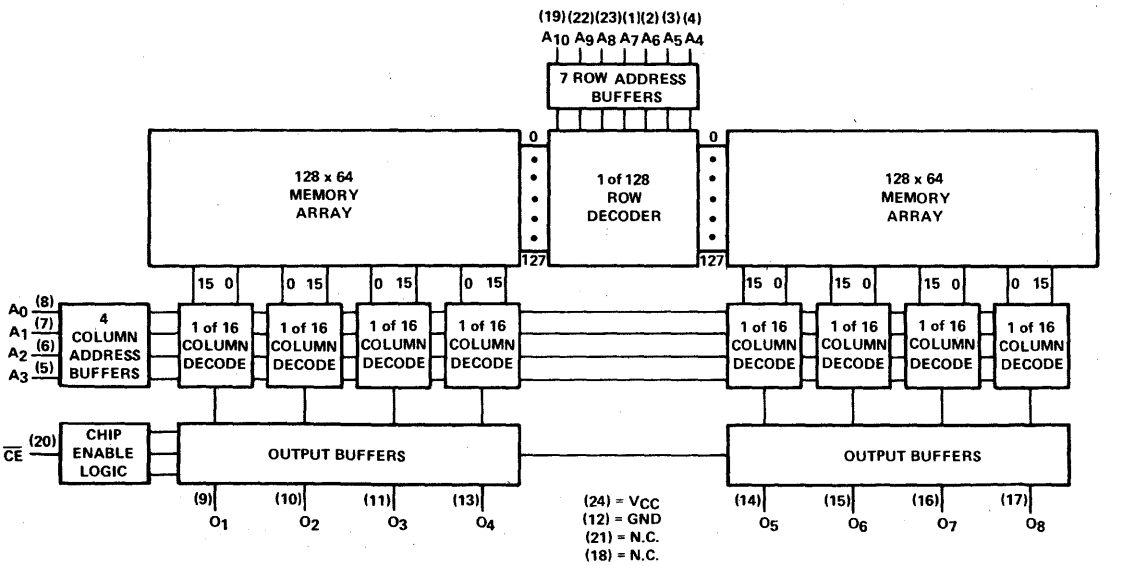
TOP VIEW - D I P



Logic Symbol



Functional Diagram



"SEE PAGES 1409-1415 FOR PACKAGE SELECTION GUIDE"

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ABSOLUTE MAXIMUM RATINGS

Output or Supply Voltage (Operating)	-0.3 to +7.0V	Storage Temperature	-65°C to +150°C
Address/Enable Input Voltage	5.5V	Operating Temperature (Ambient)	-55°C to +125°C
Address/Enable Input Current	-20mA	Maximum Junction Temperature	+175°C
Output Sink Current	100mA		

CAUTION: Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied. (While programming, follow the programming specifications.)

D.C. ELECTRICAL CHARACTERISTICS (Operating)

HM-7616-5 (V_{CC} = 5.0V ±5%, T_A = 0°C to +75°C)
HM-7616-2 (V_{CC} = 5.0V ±10%, T_A = -55°C to +125°C)
Typical Measurements are at T_A = 25°C, V_{CC} = +5V

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
I_{IH} I_{IL}	Address/Enable "1" Input Current "0"	– –	– -50.0	+40 -250	μA μA	V_{IH} = V_{CC} Max. V_{IL} = 0.45V
V_{IH} V_{IL}	Input Threshold "1" Voltage "0"	2.0 –	1.5 1.5	– 0.8	V V	V_{CC} = V_{CC} Min. V_{CC} = V_{CC} Max.
V_{OH} V_{OL}	Output "1" Voltage "0"	2.4* –	3.2 0.35	– 0.50	V V	I_{OH} = -2.0mA, V_{CC} = V_{CC} Min. I_{OL} = +16mA, V_{CC} = V_{CC} Min.
I_{OHE} I_{OLE}	Output Disable "1" Current "0"	– –	– –	+40 -40*	μA μA	V_{OH}, V_{CC} = V_{CC} Max. V_{OL} = 0.3V, V_{CC} = V_{CC} Max.
V_{CL}	Input Clamp Voltage	–	–	-1.2	V	I_{IN} = -18mA
I_{OS}	Output Short Circuit Current	-15	–	-100	mA	V_{OUT} = 0.0V, One Output at a Time for a Max. of 1 Second
I_{CC}	Power Supply Current	–	–	180	mA	V_{CC} = V_{CC} Max., All Inputs Grounded.

NOTE: Positive current defined as into device terminals.

A.C. ELECTRICAL CHARACTERISTICS (Operating)

		HM-7616-5 5V ±5% 0°C to +75°C			HM-7616-2 5V ±10% -55°C to +125°C			
SYMBOL	PARAMETER	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
T_{AA}	Address Access Time	–	45	60	–	–	80	ns
T_{EA}	Chip Enable Access Time	–	30	40	–	–	50	ns

A.C. limits guaranteed for worst case N^2 sequencing.

CAPACITANCE: T_A = 25°C

SYMBOL	PARAMETER	MAXIMUM	UNITS	TEST CONDITIONS
C_{INA}, C_{INCE}	Input Capacitance	8	pF	V_{CC} = 5V, V_{IN} = 2.0V, f = 1MHz
C_{OUT}	Output Capacitance	10	pF	V_{CC} = 5V, V_{OUT} = 2.0V, f = 1MHz

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Preview

HM-76160/161

2K x 8 PROMS

HM-76161 — "Three State" Outputs
HM-76160 — Open Collector Outputs

Features

- 60ns MAXIMUM ADDRESS ACCESS TIME
- "THREE STATE" OR OPEN COLLECTOR OUTPUTS AND THREE CHIP ENABLE INPUTS
- SIMPLE HIGH SPEED PROGRAMMING PROCEDURE – ONE PULSE/BIT TYPICAL
- FAST ACCESS TIME – GUARANTEED FOR WORST CASE N^2 SEQUENCING OVER COMMERCIAL AND MILITARY TEMPERATURE AND VOLTAGE RANGES
- INDUSTRY'S HIGHEST PROGRAMMING YIELD

Description

The HM-76160/161 are fully decoded high speed Schottky TTL 16,384 bit Field Programmable ROMs in a 2K word by 8 bit/word format with open collector (HM-76160) or "Three State" (HM-76161) outputs. These PROMs are available in a 24 pin DIP.

All bits are manufactured storing a logical "1" (Positive Logic) and can be selectively programmed for a logical "0" in any bit position.

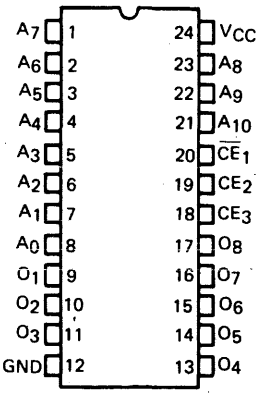
The nichrome fuse technology used is the same as all other Harris Bipolar PROMs and the JAN approved MIL-M-38510/201 PROM.

The HM-76160/161 contain test rows and columns which are in addition to the storage array to assure high programmability and guarantee parametrics and A.C. performance. The fuses in these test rows and columns are blown prior to shipment.

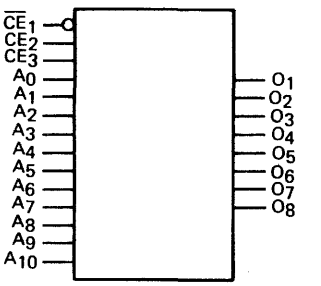
There are three chip enable inputs on the HM-76160/161. $\overline{CE}_1$ low, CE_2 high, and CE_3 high enables the device.

Pinout

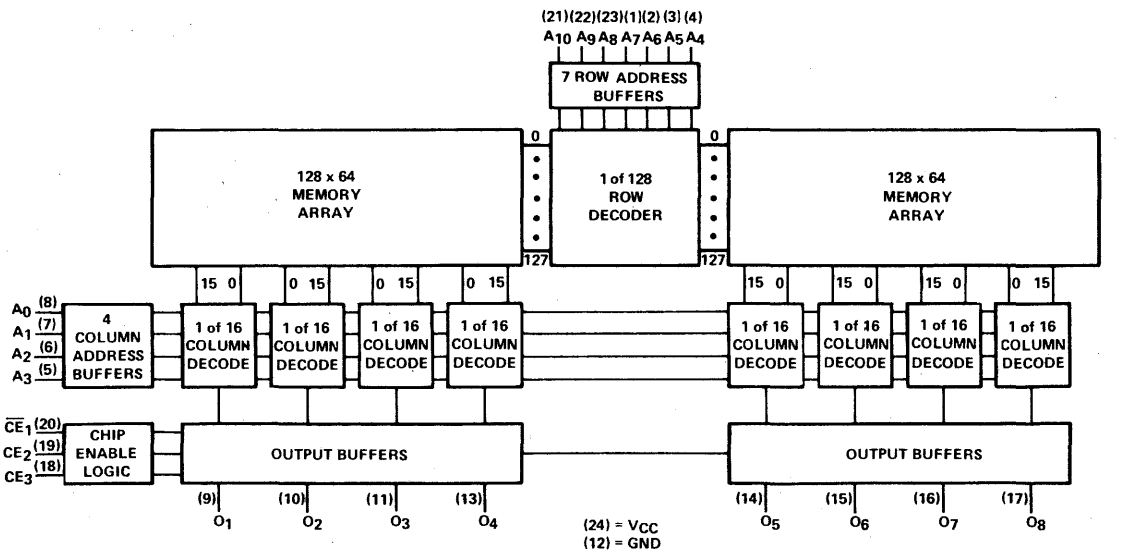
TOP VIEW - D I P



Logic Symbol



Functional Diagram



"SEE PAGES 1409-1415 FOR PACKAGE SELECTION GUIDE"

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ABSOLUTE MAXIMUM RATINGS

Output or Supply Voltage (Operating)	-0.3 to +7.0V	Storage Temperature	-65°C to +150°C
Address/Enable Input Voltage	5.5V	Operating Temperature (Ambient)	-55°C to +125°C
Address/Enable Input Current	-20mA	Maximum Junction Temperature	+175°C
Output Sink Current	100mA		

CAUTION: Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied. (While programming, follow the programming specifications.)

D.C. ELECTRICAL CHARACTERISTICS (Operating)

HM-76160/161-5 (V_{CC} = 5.0V ±5%, T_A = 0°C to +75°C)
HM-76160/161-2 (V_{CC} = 5.0V ±10%, T_A = -55°C to +125°C)
Typical Measurements are at T_A = 25°C, V_{CC} = +5V

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
I_{IH} I_{IL}	Address/Enable "1" Input Current "0"	– –	– -50.0	+40 -250	µA µA	V_{IH} = V_{CC} Max. V_{IL} = 0.45V
V_{IH} V_{IL}	Input Threshold "1" Voltage "0"	2.0 –	1.5 1.5	– 0.8	V V	V_{CC} = V_{CC} Min. V_{CC} = V_{CC} Max.
V_{OH} V_{OL}	Output "1" Voltage "0"	2.4* –	3.2* 0.35	– 0.50	V V	I_{OH} = -2.0mA, V_{CC} = V_{CC} Min. I_{OL} = +16mA, V_{CC} = V_{CC} Min.
I_{OHE} I_{OLE}	Output Disable "1" Current "0"	– –	– –	+40 -40*	µA µA	V_{OH}, V_{CC} = V_{CC} Max. V_{OL} = 0.3V, V_{CC} = V_{CC} Max.
V_{CL}	Input Clamp Voltage	–	–	-1.2	V	I_{IN} = -18mA
I_{OS}	Output Short Circuit Current	-15*	–	-100*	mA	V_{OUT} = 0.0V, One Output at a Time for a Max. of 1 Second
I_{CC}	Power Supply Current	–	–	180	mA	V_{CC} = V_{CC} Max., All Inputs Grounded.

NOTE: Positive current defined as into device terminals.
*"Three State" only

A.C. ELECTRICAL CHARACTERISTICS (Operating)

		HM-76160/161-5 5V ±5% 0°C to +75°C			HM-76160/161-2 5V ±10% -55°C to +125°C			
SYMBOL	PARAMETER	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
T_{AA}	Address Access Time	–	45	60	–	–	80	ns
T_{EA}	Chip Enable Access Time	–	30	40	–	–	50	ns

A.C. limits guaranteed for worst case N^2 sequencing.

CAPACITANCE: T_A = 25°C

SYMBOL	PARAMETER	MAXIMUM	UNITS	TEST CONDITIONS
C_{INA}, C_{INCE}	Input Capacitance	8	pF	V_{CC} = 5V, V_{IN} = 2.0V, f = 1MHz
C_{OUT}	Output Capacitance	10	pF	V_{CC} = 5V, V_{OUT} = 2.0V, f = 1MHz

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HARRIS SEMICONDUCTOR PRODUCTS DIVISION
A DIVISION OF HARRIS CORPORATION

HM-7620A/21A

512 x 4 PROM

HM-7620A - Open Collector Outputs
HM-7621A - "Three State" Outputs

Features

- 45ns MAXIMUM ADDRESS ACCESS TIME
- "THREE STATE" OR OPEN COLLECTOR OUTPUTS
- SIMPLE, HIGH SPEED PROGRAMMING PROCEDURE USING SINGLE PULSES, ASSURES FAST PROGRAMMING AND SUPERIOR RELIABILITY.
- INPUTS AND OUTPUTS TTL COMPATIBLE
- FAST ACCESS TIME – GUARANTEED FOR WORST CASE N^2 SEQUENCING OVER COMMERCIAL AND MILITARY TEMPERATURE AND VOLTAGE RANGES.
- INDUSTRY'S HIGHEST PROGRAMMING YIELD
- PIN COMPATIBLE WITH INDUSTRY STANDARD PROM's AND ROM's.

Description

The HM-7620A/21A are fully decoded high speed Schottky TTL 2048-Bit Field Programmable ROM's in a 512 word by 4 bit/word format with open collector (HM-7620A) or "three state" (HM-7621A) outputs. These PROMs are available in 16 pin D.I.P. (ceramic or epoxy) and a 16 pin flatpack.

All bits are manufactured storing a logical "1" (positive logic) and can be selectively programmed for a logical "0" in any bit position.

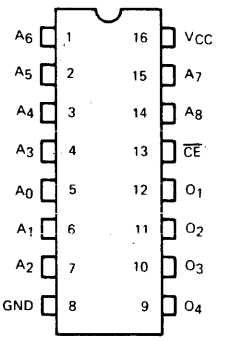
The HM-7620A/21A contain test rows and columns which are in addition to the storage array to assure high programmability and guarantee parametric and A.C. performance. The fuses in these test rows and columns are blown prior to shipment.

This PROM is intended for use in state of the art ultra high speed logic systems.

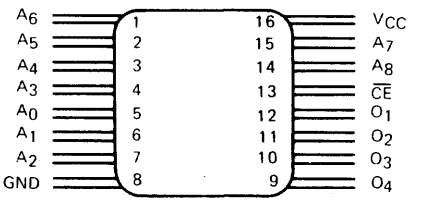
Nichrome fuse technology is used on these and all other Harris Bipolar PROM's.

Pinouts

TOP VIEW - DIP



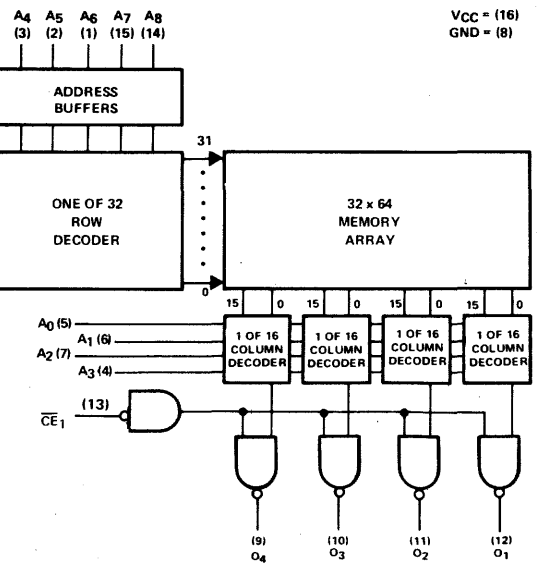
TOP VIEW – FLATPACK



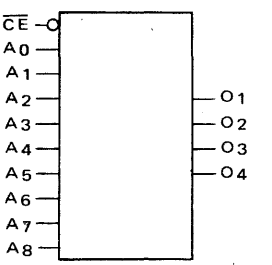
PIN NAMES

$A_0 - A_8$	Address Inputs
$\overline{CE}$	Chip Enable Input
$O_1 - O_4$	Data Outputs

Functional Diagram



Logic Symbol



"SEE PAGES 1409-1415 FOR PACKAGE SELECTION GUIDE"

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ABSOLUTE MAXIMUM RATINGS

Output or Supply Voltage (Operating)	-0.3 to +7.0V	Storage Temperature	-65°C to +150°C
Address/Enable Input Voltage	5.5V	Operating Temperature (Ambient)	-55°C to +125°C
Address/Enable Input Current	-20mA	Maximum Junction Temperature	+175°C
Output Sink Current	100mA		

CAUTION: Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied. (While programming, follow the programming specifications.)

D.C. ELECTRICAL CHARACTERISTICS (Operating)

HM-7620A/21A-5 (V_{CC} = 5.0V ±5%, T_A = 0°C to +75°C)
HM-7620A/21A-2 (V_{CC} = 5.0V ±10%, T_A = -55°C to +125°C)
Typical measurements are at T_A = 25°C, V_{CC} = +5V

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
I_{IH}	Address/enable "1"	–	–	+40	μA	V_{IH} = V_{CC} Max.
I_{IL}	Input Current "0"	–	-50.0	-250	μA	V_{IL} = 0.45V
V_{IH}	Input Threshold "1"	2.0	1.5	–	V	V_{CC} = V_{CC} Min.
V_{IL}	Voltage "0"	–	1.5	0.8	V	V_{CC} = V_{CC} Max.
V_{OH}	Output "1"	2.4*	3.2*	–	V	I_{OH} = -2.0mA, V_{CC} = V_{CC} Min.
V_{OL}	Voltage "0"	–	0.35	0.45	V	I_{OL} = +16mA, V_{CC} = V_{CC} Min.
I_{OHE}	Output Disable "1"	–	–	+40	μA	V_{OH}, V_{CC} = V_{CC} Max.
I_{OLE}	Current "0"	–	–	-40*	μA	V_{OL} = 0.3V, V_{CC} = V_{CC} Max.
V_{CL}	Input Clamp Voltage	–	–	-1.2	V	I_{IN} = -18mA
I_{OS}	Output S.C. Current	-15*	–	-100*	mA	V_{OUT} = 0.0V One Output Only for a Max. of 1 Second
I_{CC}	Power Supply Current	–	90	130	mA	V_{CC} = V_{CC} Max. All Inputs Grounded

*"Three State" only
NOTE: Positive current defined as into device terminals.

A.C. ELECTRICAL CHARACTERISTICS (Operating)

		HM-7620A/21A - 5 5V ±5% 0°C to + 75°C			HM-7620A/21A -2 5V ±10% -55°C to +125°C			
SYMBOL	PARAMETER	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
T_{AA}	Address Access Time	–	–	45	–	–	60	ns
T_{EA}	Chip Enable Access Time	–	–	25	–	–	40	ns

A.C. limits guaranteed for worst case N^2 sequencing.

CAPICITANCE: T_A = 25°C

SYMBOL	PARAMETER	MAXIMUM	UNITS	TEST CONDITIONS
C_{INA}, C_{INCE}	Input Capacitance	8	pF	V_{CC} = 5V, V_{IN} = 2.0V, f = 1MHz
C_{OUT}	Output Capacitance	10	pF	V_{CC} = 5V, V_{OUT} = 2.0V, f = 1MHz

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HM-7625R

256 x 8 PROM

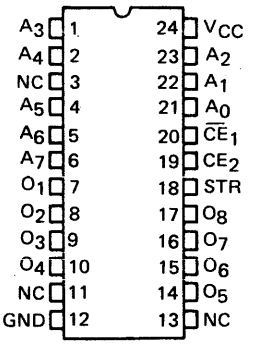
"Three State" Outputs

Features

- 60ns MAXIMUM ADDRESS ACCESS TIME.
- "THREE STATE" OUTPUTS WITH TWO CHIP ENABLE INPUTS.
- SIMPLE HIGH SPEED PROGRAMMING PROCEDURE-ONE PULSE/BIT TYPICAL. ASSURES FAST PROGRAMMING AND SUPERIOR RELIABILITY.
- FAST ACCESS TIME - GUARANTEED FOR WORST CASE N^2 SEQUENCING OVER COMMERCIAL AND MILITARY TEMPERATURE AND VOLTAGE RANGES.
- INDUSTRY'S HIGHEST PROGRAMMING YIELD.

Pinout

TOP VIEW – DIP



PIN NAMES

$A_0 - A_7$	Address Inputs
$O_1 - O_8$	Data Outputs
CE_1, CE_2	Chip Enable Inputs
STR	Strobe Input

Description

The HM-7625R is a fully decoded high speed Schottky TTL 2048-Bit Field Programmable ROM in a 256 word by 8 bit/word format and is available in a 24 pin DIP (ceramic or epoxy).

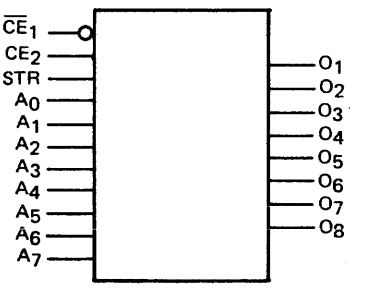
All bits are manufactured storing a logical "1" (positive logic) and can be selectively programmed for a logical "0" in any bit position.

Nichrome fuse technology is used on this and all other Harris Bipolar PROMs.

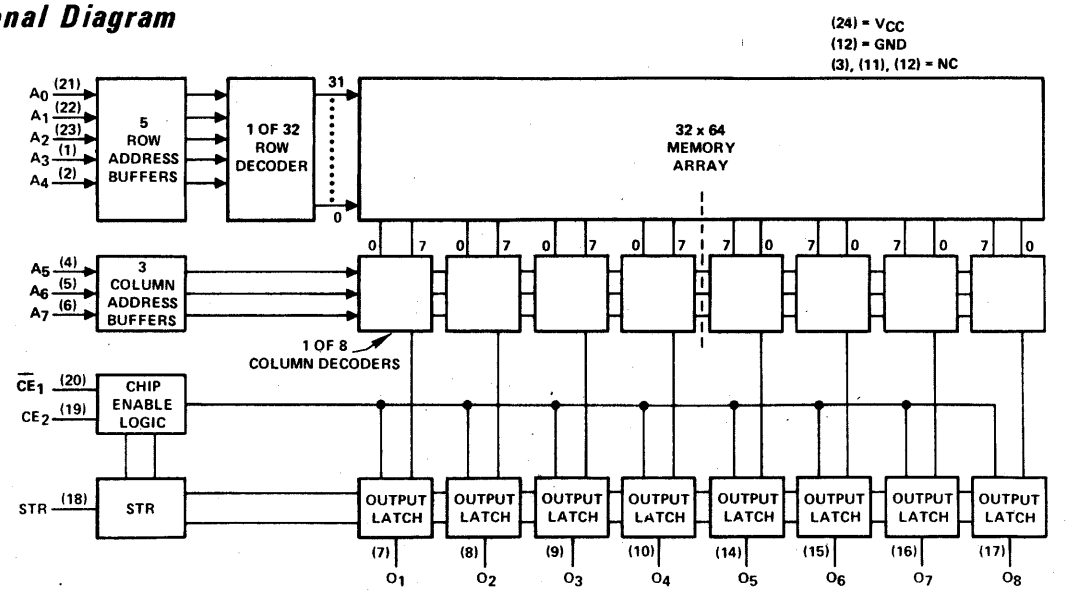
The HM-7625R contains test rows and columns which are in addition to the storage array to assure high programmability and guarantee parametric and A.C. performance. The fuses in these test rows and columns are blown prior to shipment.

There are two chip enables on the HM-7625R. $\overline{CE}_1$ low and CE_2 high enables the chip.

Logic Symbol



Functional Diagram



"SEE PAGES 1409-1415 FOR PACKAGE SELECTION GUIDE"

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ABSOLUTE MAXIMUM RATINGS

Output or Supply Voltage (Operating)	-0.3 to +7.0V	Storage Temperature	-65°C to +150°C
Address/Enable Input Voltage	5.5V	Operating Temperature (Ambient)	-55°C to +125°C
Address/Enable Input Current	-20mA	Maximum Junction Temperature	+175°C
Output Sink Current	100mA		

CAUTION: Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied. (While programming, follow the programming specifications.)

D.C. ELECTRICAL CHARACTERISTICS (Operating)

HM-7625R-5 (V_{CC} = 5.0V ± 5%, T_A = 0°C to +75°C)
HM-7625R-2 (V_{CC} = 5.0V ± 10%, T_A = -55°C to +125°C)
Typical measurements are at T_A = 25°C, V_{CC} = +5V

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
I_{IH} I_{IL}	Address/Enable "1" Input Current "0"	– –	– -50.0	+25 -100(1)	μA μA	V_{IH} = V_{CC} Max. V_{IL} = 0.45V
V_{IH} V_{IL}	Input Threshold "1" Voltage "0"	2.0 –	1.5 1.5	– 0.85	V V	V_{CC} = V_{CC} Min. V_{CC} = V_{CC} Max.
V_{OH} V_{OL}	Output "1" Voltage "0"	2.7(2) –	3.3 0.35	– 0.50	V V	I_{OH} = -2.0mA, V_{CC} = V_{CC} Min. I_{OL} = +16mA, V_{CC} = V_{CC} Min.
I_{OHE} I_{OLE}	Output Disable "1" Current "0"	– –	– –	+40 -40	μA μA	V_{OH}, V_{CC} = V_{CC} Max. V_{OL} = 0.3V, V_{CC} = V_{CC} Max.
V_{CL}	Input Clamp Voltage	–	–	-1.2	V	I_{IN} = -18mA
I_{OS}	Output Short Circuit Current	-20	–	-70	mA	V_{OUT} = 0.0V, One Output at a Time for a Max. of 1 Second
I_{CC}	Power Supply Current	–	135	185	mA	V_{CC} = V_{CC} Max., All Inputs Grounded.

NOTE: Positive current defined as into device terminals.
NOTE(1): I_{IL} = -150μA for -2
NOTE(2): V_{OH} = 2.4V for -2

A.C. ELECTRICAL CHARACTERISTICS (Operating)

		HM-7625R-5 5V ±5% 0°C to +75°C			HM-7625R-2 5V ±10% -55°C to +125°C				
SYMBOL	PARAMETER	MIN	TYP	MAX	MIN	TYP	MAX	UNITS	TEST CONDIT.
T_{AA} T_{EA}	Address Access Time Chip Enable Access Time	– –	40 30	60 40	– –	50 40	80 50	ns ns	Latched or Transparent
T_{ADH} T_{CDH} T_{SW} T_{SL} T_{DL} T_{CDS}	Address Hold Time Chip Enable Hold Time Strobe Pulse Width Strobe Latch Time Strobe Delatch Time Chip Enable Set-Up Time	0 10 30 60 – 40	-10 0 15 35 – –	– – – – 40 –	0 10 40 80 – 50	-10 0 15 45 – –	– – – – 50 –	ns ns ns ns ns ns	Latched Only

A.C. limits guaranteed for worst case N^2 sequencing.

CAPACITANCE (1): T_A = 25°C

SYMBOL	PARAMETER	MAXIMUM	UNITS	TEST CONDITIONS
C_{INA}, C_{INCE}	Input Capacitance	8	pF	V_{CC} = 5V, V_{IN} = 2.0V, f = 1MHz
C_{OUT}	Output Capacitance	10	pF	V_{CC} = 5V, V_{OUT} = 2.0V, f = 1MHz

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HM-7629

256 x 8 PROM

"Three State" Outputs

Features

- 70ns MAXIMUM ADDRESS ACCESS TIME.
- "THREE STATE" OUTPUTS WITH FOUR CHIP ENABLE INPUTS.
- SIMPLE HIGH SPEED PROGRAMMING PROCEDURE - ONE PULSE/BIT TYPICAL. ASSURES FAST PROGRAMMING AND SUPERIOR RELIABILITY.
- FAST ACCESS TIME - GUARANTEED FOR WORST CASE N^2 SEQUENCING OVER COMMERCIAL AND MILITARY TEMPERATURE AND VOLTAGE RANGES.
- INDUSTRY'S HIGHEST PROGRAMMING YIELD.

Description

The HM-7629 is a fully decoded high speed Schottky TTL 2048-Bit Field Programmable ROM in a 256 word by 8 bit/word format and is available in a 24 pin DIP (ceramic or epoxy).

All bits are manufactured storing a logical "1" (positive logic) and can be selectively programmed for a logical "0" in any bit position.

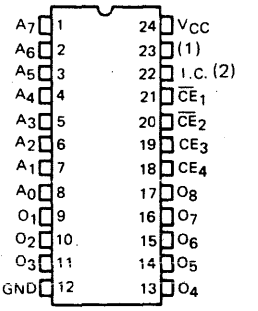
Nichrome fuse technology is used on this and all other Harris Bipolar PROMs.

The HM-7629 contains test rows and columns which are in addition to the storage array to assure high programmability and guarantee parametric and A.C. performance. The fuses in these test rows and columns are blown prior to shipment.

There are four chip enables on the HM-7629. $\overline{CE}_1$ low, $\overline{CE}_2$ low, CE_3 high , and CE_4 high enables the chip.

Pinout

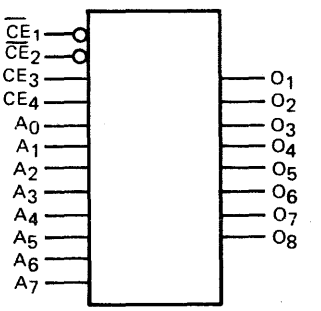
TOP VIEW – DIP



PIN NAMES

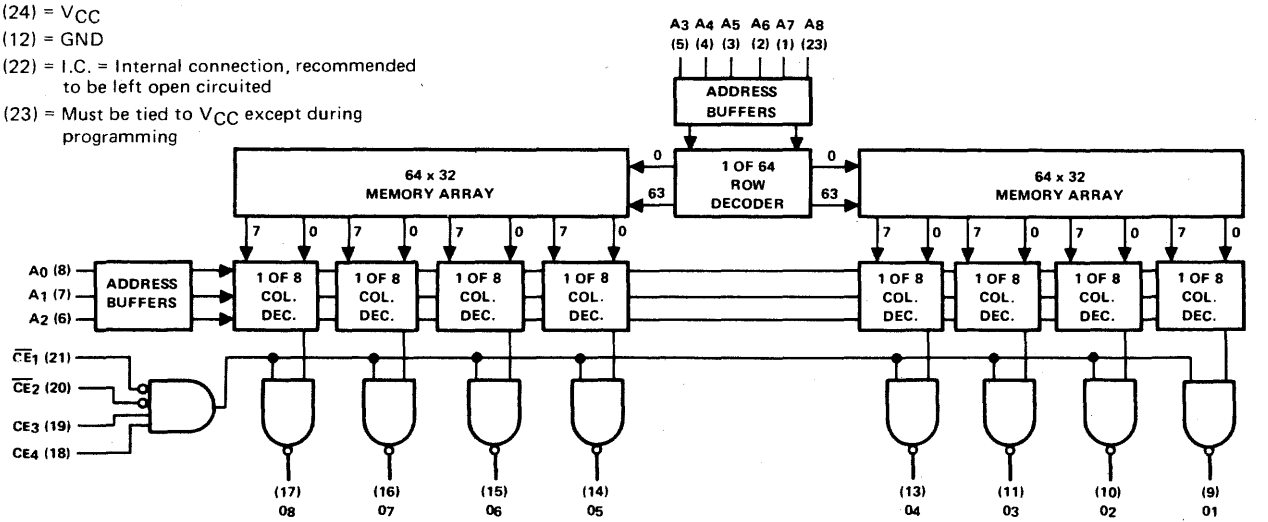
A_0 - A_7 Address Inputs
O_1 - O_8 Data Outputs
$\overline{CE}_1$, $\overline{CE}_2$, CE_3, CE_4 Chip Enable Inputs
(1) Pin 23 must be tied to V_{CC} except during programming
(2) Internal Connection

Logic Symbol



Functional Diagram

(24) = V_{CC}
(12) = GND
(22) = I.C. = Internal connection, recommended to be left open circuited
(23) = Must be tied to V_{CC} except during programming



"SEE PAGES 1409-1415 FOR PACKAGE SELECTION GUIDE"

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ABSOLUTE MAXIMUM RATINGS

Output or Supply Voltage (Operating)	-0.3 to +7.0V	Storage Temperature	-65°C to +150°C
Address/Enable Input Voltage	5.5V	Operating Temperature (Ambient)	0°C to +75C
Address/Enable Input Current	-20mA	Maximum Junction Temperature	+175°C
Output Sink Current	100mA		

CAUTION: Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied. (While programming, follow the programming specifications.)

D.C. ELECTRICAL CHARACTERISTICS (Operating)

HM-7629-5 (V_{CC} = 5.0V + 5%, T_A = 0°C to +75°C)
Typical measurements are at T_A = 25°C, V_{CC} = +5V

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
I_{IH}	Address/Enable*"1"	–	–	+40	μA	V_{IH} = V_{CC} Max.
I_{IL}	Input Current "0"	–	-50.0	-250	μA	V_{IL} = 0.45V
V_{IH}	Input Threshold "1"	2.0	1.5	–	V	V_{CC} = V_{CC} Min.
V_{IL}	Voltage "0"	–	1.5	0.80	V	V_{CC} = V_{CC} Max.
V_{OH}	Output "1"	2.4	3.4	–	V	I_{OH} = -2.0mA, V_{CC} = V_{CC} Min.
V_{OL}	Voltage "0"	–	0.35	0.45	V	I_{OL} = +16mA, V_{CC} = V_{CC} Min.
I_{OHE}	Output Disable "1"	–	–	+100	μA	V_{OH}, V_{CC} = V_{CC} Max.
I_{OLE}	Current "0"	–	–	-100	μA	V_{OL} = 0.3V, V_{CC} = V_{CC} Max.
V_{CL}	Input Clamp Voltage	–	–	-1.2	V	I_{IN} = -18mA
I_{OS}	Output Short Circuit Current	-15	–	-100	mA	V_{OUT} = 0.0V, One Output at a Time for a Max. of 1 Second
I_{CC}	Power Supply Current	–	125	170	mA	V_{CC} = V_{CC} Max., All Inputs Grounded.

NOTE: Positive current defined as into device terminals.
*Enable current measured using only one enable input at a time to disable the device.

A.C. ELECTRICAL CHARACTERISTICS (Operating)

		HM-7629-5 5V ± 5% 0°C to +75°C			
SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
T_{AA}	Address Access Time	–	45	70	ns
T_{EA}	Chip Enable Access Time	–	30	40	ns

A.C. limits guaranteed for worst case N^2 sequencing.

CAPACITANCE: T_A = 25°C

SYMBOL	PARAMETER	MAXIMUM	UNITS	TEST CONDITIONS
C_{INA}, C_{INCE}	Input Capacitance	12	pF	V_{CC} = 5V, V_{IN} = 2.0V, f = 1MHz
C_{OUT}	Output Capacitance	12	pF	V_{CC} = 5V, V_{OUT} = 2.0V, f = 1MHz

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HARRIS
SEMICONDUCTOR
PRODUCTS DIVISION
A DIVISION OF HARRIS CORPORATION

HM-7640A/41A

512 x 8 PROM

HM-7640A - Open Collector Outputs
HM-7641A - "Three State" Outputs

Features

- 50ns MAXIMUM ADDRESS ACCESS TIME
- "THREE STATE" OR OPEN COLLECTOR OUTPUTS AND FOUR CHIPS ENABLE INPUTS.
- SIMPLE HIGH SPEED PROGRAMMING PROCEDURE — ONE PULSE/BIT. ASSURES FAST PROGRAMMING AND SUPERIOR RELIABILITY.
- FAST ACCESS TIME – GUARANTEED FOR WORST CASE N^2 SEQUENCING OVER COMMERCIAL AND MILITARY TEMPERATURE AND VOLTAGE RANGES.
- INDUSTRY'S HIGHEST PROGRAMMING YIELD
- LOW INPUT LOADING

Description

The HM-7640A/41A are fully decoded high speed Schottky TTL 4096-Bit Field Programmable ROMs in a 512 word by 8 bit/word format and are available in a 24 pin DIP (ceramic or epoxy) and a 24 pin flatpack.

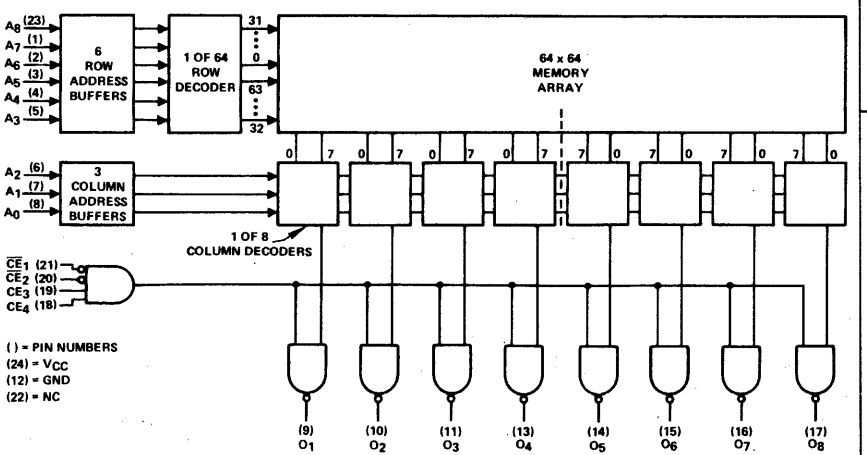
All bits are manufactured storing a logical "1" (positive logic) and can be selectively programmed for a logical "0" in any bit position.

Nichrome fuse technology is used on this and all other Harris Bipolar PROM's.

The HM-7640A/41A contain test rows and columns which are in addition to the storage array to assure high programmability and guarantee parametric and A.C. performance. The fuses in these test rows and columns are blown prior to shipment.

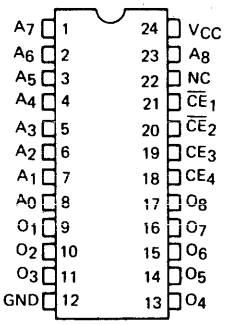
There are four chip enable inputs on the HM-7640A/41A where $\overline{CE}_1$, and $\overline{CE}_2$ low and CE_3 and CE_4 high enables the chip.

Functional Diagram

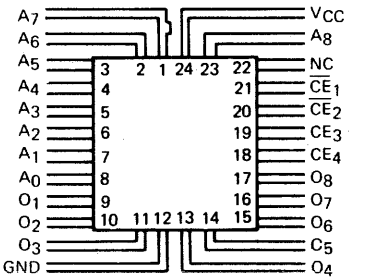


Pinouts

TOP VIEW – DIP



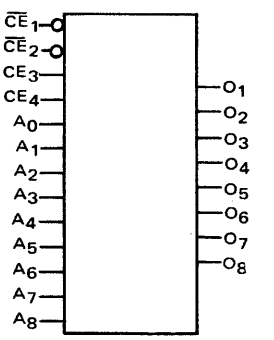
TOP VIEW – FLATPACK



PIN NAMES

$A_0 - A_8$	Address Inputs
$O_1 - O_8$	Data Outputs
$\overline{CE}_1, \overline{CE}_2, CE_3, CE_4$	Chip Enable Inputs

Logic Symbol



"SEE PAGES 1409-1415 FOR PACKAGE SELECTION GUIDE"

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ABSOLUTE MAXIMUM RATINGS

Output or Supply Voltage (Operating)	-0.3 to +7.0V	Storage Temperature	-65°C to +150°C
Address/Enable Input Voltage	5.5V	Operating Temperature (Ambient)	-55°C to +125°C
Address/Enable Input Current	-20mA	Maximum Junction Temperature	+175°C
Output Sink Current	100mA		

CAUTION: Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied. (While programming, follow the programming specifications.)

D.C. ELECTRICAL CHARACTERISTICS (Operating)

HM-7640A/41A-5 (V_{CC} = 5.0V ± 5%, T_A = 0°C to +75°C)
HM-7640A/41A-2 (V_{CC} = 5.0V ± 10%, T_A = -55°C to +125°C)
Typical measurements are at T_A = 25°C, V_{CC} = +5V

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
I_{IH} I_{IL}	Address/Enable "1" Input Current "0"	– –	– -50.0	+40 -250	µA µA	V_{IH} = V_{CC} Max. V_{IL} = 0.45V
V_{IH} V_{IL}	Input Threshold "1" Voltage "0"	2.0 –	1.5 1.5	– 0.8	V V	V_{CC} = V_{CC} Min. V_{CC} = V_{CC} Max.
V_{OH} V_{OL}	Output "1" Voltage "0"	2.4* –	3.2* 0.35	– 0.45	V V	I_{OH} = -2.0mA, V_{CC} = V_{CC} Min. I_{OL} = +16mA, V_{CC} = V_{CC} Min.
I_{OHE} I_{OLE}	Output Disable "1" Current "0"	– –	– –	+40 -40*	µA µA	V_{OH}, V_{CC} = V_{CC} Max. V_{OL} = 0.3V, V_{CC} = V_{CC} Max.
V_{CL}	Input Clamp Voltage	–	–	-1.2	V	I_{IN} = -18mA
I_{OS}	Output Short Circuit Current	-15*	–	-100*	mA	V_{OUT} = 0.0V, One Output at a Time for a Max. of 1 Second
I_{CC}	Power Supply Current	–	125	170	mA	V_{CC} = V_{CC} Max., All Inputs Grounded.

NOTE: Positive current defined as into device terminals.
*"Three State" only

A.C. ELECTRICAL CHARACTERISTICS (Operating)

		HM-7640A/41A 5V ±5% 0°C to +75°C			HM-7640A/41A 5V ±10% -55°C to +125°C			
SYMBOL	PARAMETER	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
T_{AA}	Address Access Time	–	35	50	–	–	70	ns
T_{EA}	Chip Enable Access Time	–	30	40	–	–	50	ns

A.C. limits guaranteed for worst case N^2 sequencing.

CAPACITANCE: T_A = 25°C

SYMBOL	PARAMETER	MAXIMUM	UNITS	TEST CONDITIONS
C_{INA}, C_{INCE}	Input Capacitance	8	pF	V_{CC} = 5V, V_{IN} = 2.0V, f = 1MHz
C_{OUT}	Output Capacitance	10	pF	V_{CC} = 5V, V_{OUT} = 2.0V, f = 1MHz

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HARRIS SEMICONDUCTOR PRODUCTS DIVISION
A DIVISION OF HARRIS CORPORATION

HM-7640AR/41AR

512 x 8 PROM

HM-7640AR - Open Collector Outputs
HM-7641AR - "Three State" Outputs

Preview

Features

- 50ns MAXIMUM ADDRESS ACCESS TIME.
- "THREE STATE" OR OPEN COLLECTOR OUTPUTS WITH THREE CHIP ENABLE INPUTS.
- SIMPLE HIGH SPEED PROGRAMMING PROCEDURE - ONE PULSE/BIT. ASSURES FAST PROGRAMMING AND SUPERIOR RELIABILITY.
- FAST ACCESS TIME - GUARANTEED FOR WORST CASE N^2 SEQUENCING OVER COMMERCIAL AND MILITARY TEMPERATURE AND VOLTAGE RANGES.
- INDUSTRY'S HIGHEST PROGRAMMING YIELD.
- LATCHED OUTPUTS.
- LOW INPUT LOADING.

Description

The HM-7640AR/41AR are fully decoded high speed Schottky TTL 4096 Bit Field Programmable ROMs in a 512 word by 8 bit/word format and are available in a 24-pin DIP (ceramic or epoxy) and a 24-pin flat pack.

All bits are manufactured storing a logical "1" (positive logic) and can be selectively programmed for a logical "0" in any bit position.

Nichrome fuse technology is used on this and all other Harris Bipolar PROMs.

The HM-7640AR/41AR contain test rows and columns which are in addition to the storage array to assure high programmability and guarantee parametrics and A.C. performance. The fuses in these test rows and columns are blown prior to shipment.

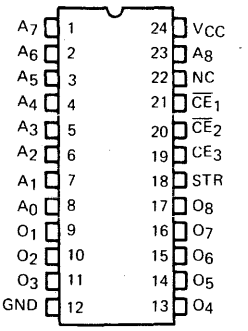
There are three chip enable inputs on the HM-7640AR/41AR, $\overline{CE}_1$, $\overline{CE}_2$ low and CE_3 high enables the chip.

HM-7640AR/41AR are operated in the Transparent Read Mode by holding the strobe input high throughout the read operation. This is the normal read mode where the three chip enable inputs will control the outputs.

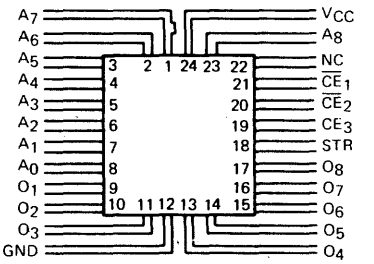
In Latched Read Mode, bringing the strobe input low will latch the outputs and chip enable inputs. If the device is disabled, when the strobe input goes low the outputs will be latched in the high impedance state. If the device is in the latched mode the strobe input must be brought high to allow the outputs to respond to new address or chip enable conditions.

Pinouts

TOP VIEW – DIP



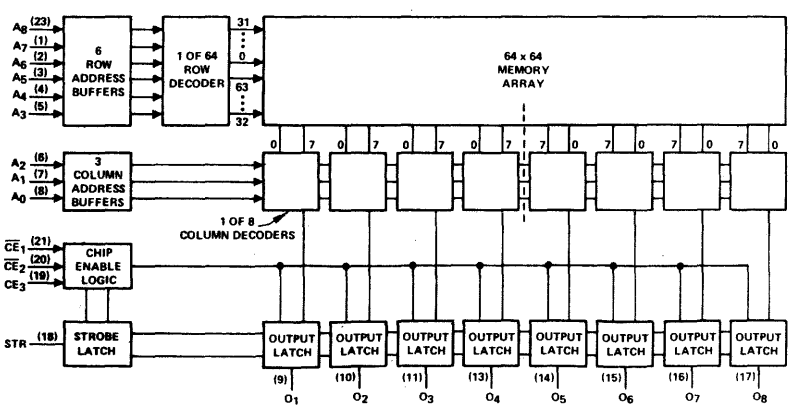
TOP VIEW – FLATPACK



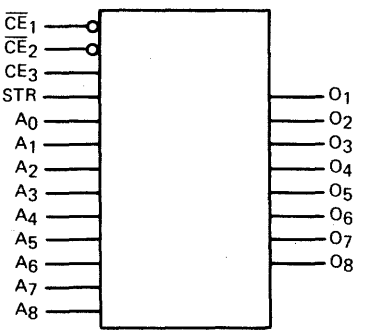
PIN NAMES

$A_0 - A_8$	Address Inputs
$O_1 - O_8$	Data Outputs
$\overline{CE}_1, \overline{CE}_2, CE_3$	Chip Enable Inputs
STR	Latch Input

Functional Diagram



Logic Symbol



"SEE PAGES 1409-1415 FOR PACKAGE SELECTION GUIDE"

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ABSOLUTE MAXIMUM RATINGS

Output or Supply Voltage (Operating)	-0.3 to +7.0V	Storage Temperature	-65°C to +150°C
Address/Enable Input Voltage	5.5V	Operating Temperature (Ambient)	-55°C to +125°C
Address/Enable Input Current	-20mA	Maximum Junction Temperature	+175°C
Output Sink Current	100mA		

CAUTION: Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied. (While programming, follow the programming specifications.)

D.C. ELECTRICAL CHARACTERISTICS (Operating)

HM-7640AR/41AR-5 (V_{CC} = 5.0V ± 5%, T_A = 0°C to +75°C)
HM-7640AR/41AR-2 (V_{CC} = 5.0V ± 10%, T_A = -55°C to +125°C)
Typical measurements are at T_A = 25°C, V_{CC} = +5V

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
I_{IH} I_{IL}	Address/Enable "1" Input Current "0"	– –	– -50.0	+40 -250	µA µA	V_{IH} = V_{CC} Max. V_{IL} = 0.45V
V_{IH} V_{IL}	Input Threshold "1" Voltage "0"	2.0 –	1.5 1.5	– 0.8	V V	V_{CC} = V_{CC} Min. V_{CC} = V_{CC} Max.
V_{OH} V_{OL}	Output "1" Voltage "0"	2.4* –	3.2* 0.35	– 0.45	V V	I_{OH} = -2.0mA, V_{CC} = V_{CC} Min. I_{OL} = +16mA, V_{CC} = V_{CC} Min.
I_{OHE} I_{OLE}	Output Disable "1" Current "0"	– –	– –	+40 -40*	µA µA	V_{OH}, V_{CC} = V_{CC} Max. V_{OL} = 0.3V, V_{CC} = V_{CC} Max.
V_{CL}	Input Clamp Voltage	–	–	-1.2	V	I_{IN} = -18mA
I_{OS}	Output Short Circuit Current	-15*	–	-100*	mA	V_{OUT} = 0.0V, One Output at a Time for a Max. of 1 Second
I_{CC}	Power Supply Current	–	–	180	mA	V_{CC} = V_{CC} Max., All Inputs Grounded.

NOTE: Positive current defined as into device terminals.
*"Three State" only

A.C. ELECTRICAL CHARACTERISTICS (Operating)

		HM-7640AR/41AR-5 5V ±5% 0°C to +75°C			HM-7640AR/41AR-2 5V ±10% -55°C to +125°C				
SYMBOL	PARAMETER	MIN	TYP	MAX	MIN	TYP	MAX	UNITS	TEST CONDIT.
T_{AA}	Address Access Time	–	35	50	–	–	70	ns	Latched or
T_{EA}	Chip Enable Access Time	–	30	40	–	–	50	ns	Transparent
T_{ADH}	Address Hold Time	0	-10	–	0	-10	–	ns	Latched Only
T_{CDH}	Chip Enable Hold Time	10	0	–	10	0	–	ns	
T_{SW}	Strobe Pulse Width	30	15	–	40	15	–	ns	
T_{SL}	Strobe Latch Time	60	35	–	80	45	–	ns	
T_{DL}	Strobe Delatch Time	–	–	40	–	–	50	ns	
T_{CDS}	Chip Enable Set-Up Time	40	–	–	50	–	–	ns	

A.C. limits guaranteed for worst case N^2 sequencing.

CAPACITANCE: T_A = 25°C

SYMBOL	PARAMETER	MAXIMUM	UNITS	TEST CONDITIONS
C_{INA}, C_{INCE}	Input Capacitance	8	pF	V_{CC} = 5V, V_{IN} = 2.0V, f = 1MHz
C_{OUT}	Output Capacitance	10	pF	V_{CC} = 5V, V_{OUT} = 2.0V, f = 1MHz

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HARRIS SEMICONDUCTOR PRODUCTS DIVISION
A DIVISION OF HARRIS CORPORATION

HM-7642A/43A

1K x 4 PROM

HM-7642A - Open Collector Outputs
HM-7643A - "Three State" Outputs

Features

- 50ns MAXIMUM ADDRESS ACCESS TIME.
- "THREE STATE" OR OPEN COLLECTOR OUTPUTS AND TWO CHIP ENABLE INPUTS
- SIMPLE HIGH SPEED PROGRAMMING PROCEDURE ONE PULSE/BIT. ASSURES FAST PROGRAMMING AND SUPERIOR RELIABILITY.
- FAST ACCESS TIME - GUARANTEED FOR WORST CASE N^2 SEQUENCING OVER COMMERCIAL AND MILITARY TEMPERATURE AND VOLTAGE RANGES.
- INDUSTRY'S HIGHEST PROGRAMMING YIELD.

Description

The HM-7642A/43A are fully decoded high speed Schottky TTL 4096-Bit Field Programmable ROMs in a 1K words by 4 Bit/word format with open collector(HM-7642A) or "Three State" (HM-7643A) outputs. These PROM's are available in an 18–pin DIP (ceramic or epoxy) and an 18–pin flat pack.

All bits are manufactured storing a logical "1" (positive logic) and can be selectively programmed for a logical "0" in any bit position.

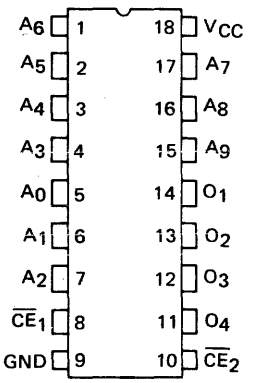
Nichrome fuse technology is used on this and all other Harris Bipolar PROMs.

The HM-7642A/43A contains test rows and columns which are in addition to the storage array to assure high programmability and guarantee parametrics and A.C. performance. The fuses in these test rows and columns are blown prior to shipment.

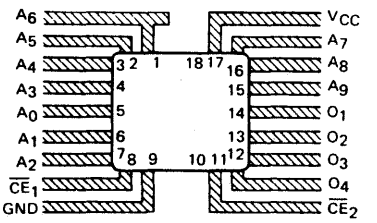
There are two chip enable inputs on the HM-7642A/43A. $\overline{CE}_1$ and $\overline{CE}_2$ low enables the chip.

Pinout

TOP VIEW–DIP



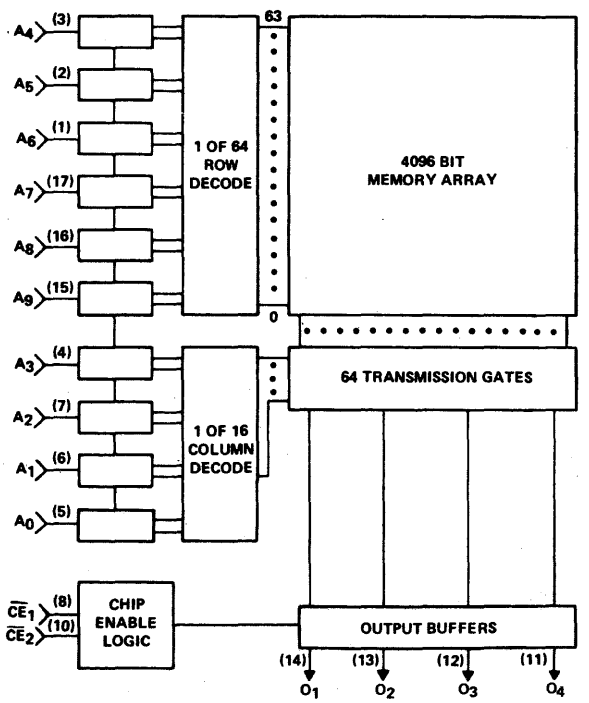
TOP VIEW–FLAT PACK



PIN NAMES

$A_0 - A_9$	ADDRESS INPUTS
$O_1 - O_4$	DATA OUTPUTS
$\overline{CE}_1, \overline{CE}_2$	CHIP ENABLE INPUTS

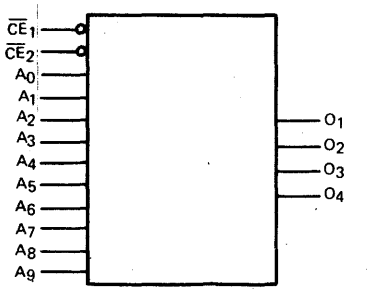
Functional Diagram



NOTE: Physical bit positions for columns are as follows:
O_2, O_4 = (0 → 15)
O_1, O_3 = (15, 0 → 14)

( ) = PIN NUMBERS
(18) = V_{CC}
(9) = GND

Logic Symbol



"SEE PAGES 1409-1415 FOR PACKAGE SELECTION GUIDE"

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ABSOLUTE MAXIMUM RATINGS

Output or Supply Voltage (Operating)	-0.3 to +7.0V	Storage Temperature	-65°C to +150°C
Address/Enable Input Voltage	5.5V	Operating Temperature (Ambient)	-55°C to +125°C
Address/Enable Input Current	-20mA	Maximum Junction Temperature	+175°C
Output Sink Current	100mA		

CAUTION: Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied. (While programming, follow the programming specifications.)

D.C. ELECTRICAL CHARACTERISTICS (Operating)

HM-7642A/43A-5 V_{CC} = 5.0V ±5%, T_A = 0°C to +75°C)
HM-7642A/43A-2 V_{CC} = 5.0V ±10%, T_A = -55°C to +125°C)
Typical Measurements are at T_A = 25°C, V_{CC} = +5V

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
I_{IH} I_{IL}	Address/Enable "1" Input Current "0"	– –	– -50.0	+40 -250	µA µA	V_{IH} = V_{CC} Max. V_{IL} = 0.45V
V_{IH} V_{IL}	Input Threshold "1" Voltage "0"	2.0 –	1.5 1.5	– 0.8	V V	V_{CC} = V_{CC} Min. V_{CC} = V_{CC} Max.
V_{OH} V_{OL}	Output "1" Voltage "0"	2.4* –	3.2* 0.35	– 0.45	V V	I_{OH} = -2.0mA, V_{CC} = V_{CC} Min. I_{OL} = +16mA, V_{CC} = V_{CC} Min.
I_{OHE} I_{OLE}	Output Disable "1" Current "0"	– –	– –	+40 -40*	µA µA	V_{OH}, V_{CC} = V_{CC} Max. V_{OL} = 0.3V, V_{CC} = V_{CC} Max.
V_{CL}	Input Clamp Voltage	–	–	-1.2	V	I_{IN} = -18mA
I_{OS}	Output Short Circuit Current	-15*	–	-100*	mA	V_{OUT} = 0.0V, One Output at a Time for a Max. of 1 Second
I_{CC}	Power Supply Current	–	100	140	mA	V_{CC} = V_{CC} Max., All Inputs Grounded.

NOTE: Positive current defined as into device terminals.
*"Three State" only

A.C. ELECTRICAL CHARACTERISTICS (Operating)

		HM-7642A/43A 5V ±5% 0°C to +75°C			HM-7642A/43A 5V ±10% -55°C to +125°C			
SYMBOL	PARAMETER	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
T_{AA}	Address Access Time	–	35	50	–	–	70	ns
T_{EA}	Chip Enable Access Time	–	25	30	–	–	40	ns

A.C. limits guaranteed for worst case N^2 sequencing.

CAPACITANCE: T_A = 25°C

SYMBOL	PARAMETER	MAXIMUM	UNITS	TEST CONDITIONS
C_{INA}, C_{INCE}	Input Capacitance	8	pF	V_{CC} = 5V, V_{IN} = 2.0V, f = 1MHz
C_{OUT}	Output Capacitance	10	pF	V_{CC} = 5V, V_{OUT} = 2.0V, f = 1MHz

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HM-7642P/43P

1K x 4 PROM

HM-7642P - Open Collector Outputs
HM-7643P - "Three State" Outputs

Preview

Features

- 50ns MAXIMUM ADDRESS ACCESS TIME.
- "THREE STATE" OR OPEN COLLECTOR OUTPUTS, A POWER DOWN INPUT, AND A CHIP ENABLE INPUT.
- SIMPLE HIGH SPEED PROGRAMMING PROCEDURE - ONE PULSE/BIT. ASSURES FAST PROGRAMMING AND SUPERIOR RELIABILITY.
- FAST ACCESS TIME FOR WORST CASE N^2 SEQUENCING OVER COMMERCIAL AND MILITARY TEMPERATURE AND VOLTAGE RANGES.
- INDUSTRY'S HIGHEST PROGRAMMING YIELD.

Description

The HM-7642P/43P are fully decoded high speed SchottkyTTL 4096-Bit Field Programmable ROMs in a 1K words by 4 bit/word format with open collector (HM-7642P) or "Three State" (HM-7643P) outputs. These PROMs are available in an 18-pin DIP (ceramic or epoxy) and an 18-pin flat pack.

All bits are manufactured storing a logical "1" (positive logic) and can be selectively programmed for a logical "0" in any bit position.

Nichrome fuse technology is used on these and all other Harris Bipolar PROMs.

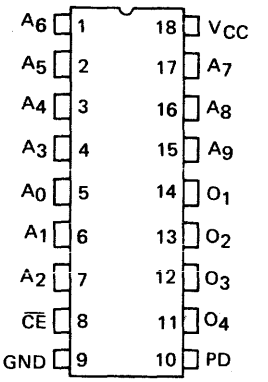
The HM-7642P/43P contains test rows and columns which are in addition to the storage array to assure high programmability and guarantee parametrics and A.C. performance. The fuses in these test rows and columns are blown prior to shipment.

There is a power down input on the HM-7642P/43P which is similar to a chip enable. The chip can be enabled or disabled using the power down input where a powered down chip dissipates 25% of nominal power and the outputs go to a high impedance state. The chip is powered up when PD_1 is low.

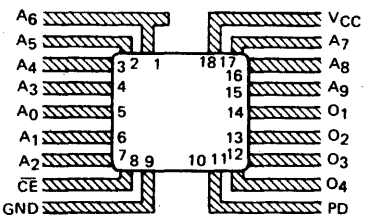
There is also the conventional chip enable input on this device, $\overline{CE}$ low and PD_1 low enables the device.

Pinout

TOP VIEW – DIP



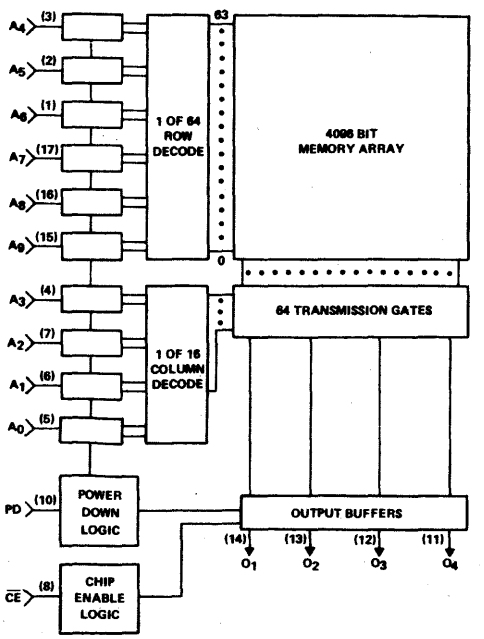
TOP VIEW – FLAT PACK



PIN NAMES

$A_0 - A_9$	ADDRESS INPUTS
$O_1 - O_4$	DATA OUTPUTS
PD	POWER DOWN INPUT
$\overline{CE}$	CHIP ENABLE INPUT

Functional Diagram

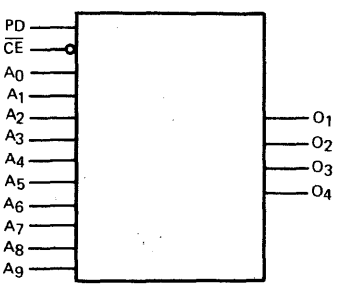


NOTE: Physical bit positions for columns are as follows:

O_1, O_3 = (15, 0 ⟶ 14)
O_2, O_4 = (0 ⟶ 15)

( ) = Pin Numbers
(18) = V_{CC}
(9) = GND

Logic Symbol



"SEE PAGES 1409-1415 FOR PACKAGE SELECTION GUIDE"

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ABSOLUTE MAXIMUM RATINGS

Output or Supply Voltage (Operating)	-0.3 to +7.0V	Storage Temperature	-65°C to +150°C
Address/Enable Input Voltage	5.5V	Operating Temperature (Ambient)	-55°C to +125°C
Address/Enable Input Current	-20mA	Maximum Junction Temperature	+175°C
Output Sink Current	100mA		

CAUTION: Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied. (While programming, follow the programming specifications.)

D.C. ELECTRICAL CHARACTERISTICS (Operating)

HM-7642P/43P-5 (V_{CC} = 5.0V ±5%, T_A = 0°C to +75°C)
HM-7642P/43P-2 (V_{CC} = 5.0V ±10%, T_A = -55°C to +125°C)
Typical Measurements are at T_A = 25°C, V_{CC} = +5V

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
I_{IH} I_{IL}	Address/Enable "1" Input Current "0"	– –	– -50.0	+40 -250	μA μA	V_{IH} = V_{CC} Max. V_{IL} = 0.45V
V_{IH} V_{IL}	Input Threshold "1" Voltage "0"	2.0 –	1.5 1.5	– 0.8	V V	V_{CC} = V_{CC} Min. V_{CC} = V_{CC} Max.
V_{OH} V_{OL}	Output "1" Voltage "0"	2.4* –	3.2* 0.35	– 0.45	V V	I_{OH} = -2.0mA, V_{CC} = V_{CC} Min. I_{OL} = +16mA, V_{CC} = V_{CC} Min.
I_{OHE} I_{OLE}	Output Disable "1" Current "0"	– –	– –	+40 -40*	μA μA	V_{OH}, V_{CC} = V_{CC} Max. V_{OL} = 0.3V, V_{CC} = V_{CC} Max.
V_{CL}	Input Clamp Voltage	–	–	-1.2	V	I_{IN} = -18mA
I_{OS}	Output Short Circuit Current	-15*	–	-100*	mA	V_{OUT} = 0.0V, One Output at a Time for a Max. of 1 Second
I_{CC}	Power Supply Current	–	100	140	mA	V_{CC} = V_{CC} Max., All Inputs Grounded.

NOTE: Positive current defined as into device terminals.
*"Three State" only

A.C. ELECTRICAL CHARACTERISTICS (Operating)

		HM-7642P/43P-5 5V ± 5% 0°C to +75°C			HM-7642P/43P-2 5V ± 10% -55°C to +125°C			
SYMBOL	PARAMETER	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
T_{AA}	Address Access Time	-	35	50	-	-	70	ns
T_{DA}	Chip Disable Access Time	-	25	30	-	-	40	ns
T_{PU}	Chip Power-Up Access Time	-	80	100	-	-	150	ns

A.C. limits guaranteed for worst case N^2 sequencing.

CAPACITANCE: T_A = 25°C

SYMBOL	PARAMETER	MAXIMUM	UNITS	TEST CONDITIONS
C_{INA}, C_{INCE}	Input Capacitance	8	pF	V_{CC} = 5V, V_{IN} = 2.0V, f = 1MHz
C_{OUT}	Output Capacitance	10	pF	V_{CC} = 5V, V_{OUT} = 2.0V, f = 1MHz

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HM-7644A

1K x 4 PROM

Active Pull-up Outputs

Features

- 50ns MAXIMUM ADDRESS ACCESS TIME
- ACTIVE PULL-UP OUTPUTS
- SIMPLE HIGH SPEED PROGRAMMING PROCEDURE ONE PULSE/BIT ASSURES FAST PROGRAMMING AND SUPERIOR RELIABILITY
- FAST ACCESS TIME - GUARANTEED FOR WORST CASE N^2 SEQUENCING OVER COMMERCIAL AND MILITARY TEMPERATURE AND VOLTAGE RANGES
- INDUSTRY'S HIGHEST PROGRAMMING YIELD
- LOW PIN COUNT FOR MAXIMUM DENSITY

Description

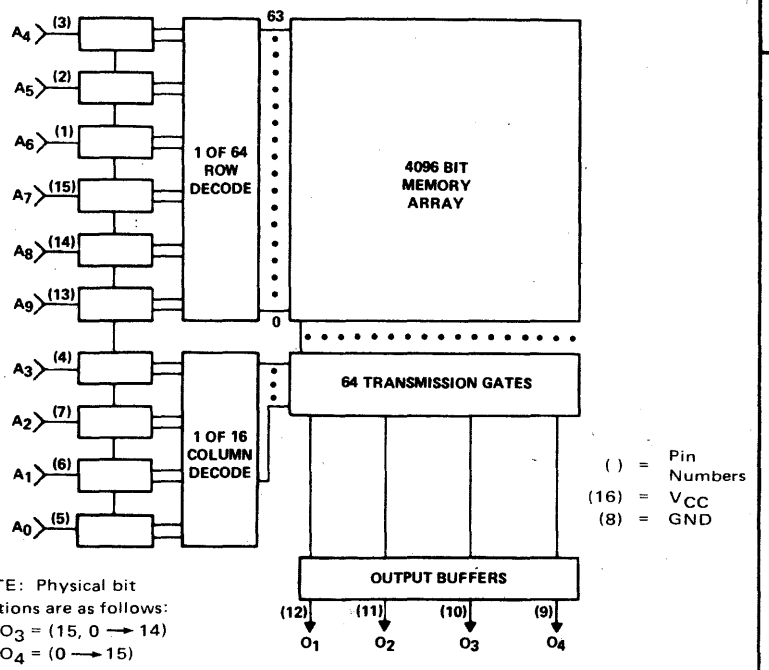
The HM-7644A is a fully decoded high speed Schottky TTL 4096-Bit Field Programmable ROM in a 1K word by 4 bit/word format with active pull-up outputs. This PROM is available in a 16 pin DIP (ceramic or epoxy) and a 16 pin flatpack.

All bits are manufactured storing a logical "1" (positive logic) and can be selectively programmed for a logical "0" in any bit position.

Nichrome fuse technology is used on this and all other Harris Bipolar PROMs.

The HM-7644A contains test rows and columns which are in addition to the storage array to assure high programmability and guarantee parametrics and A.C. performance. The fuses in these test rows and columns are blown prior to shipment.

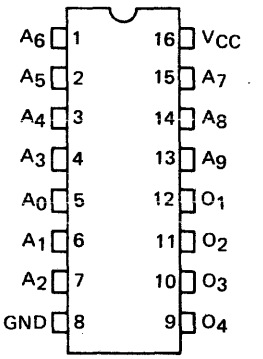
Functional Diagram



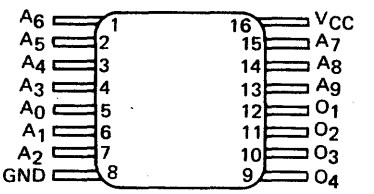
NOTE: Physical bit positions are as follows:
O_1, O_3 = (15, 0 → 14)
O_2, O_4 = (0 → 15)

Pinouts

TOP VIEW – DIP



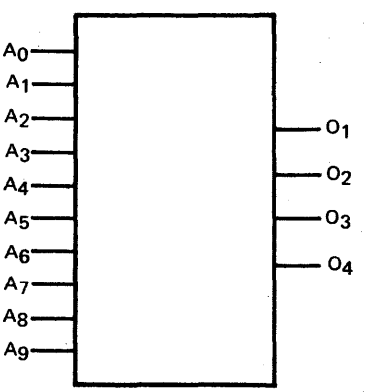
TOP VIEW – FLATPACK



PIN NAMES

A_0-A_9 Address Inputs
O_1-O_4 Outputs

Logic Symbol



"SEE PAGES 1409-1415 FOR PACKAGE SELECTION GUIDE"

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ABSOLUTE MAXIMUM RATINGS

Output or Supply Voltage (Operating)	-0.3 to +7.0V	Storage Temperature	-65°C to +150°C
Address/Enable Input Voltage	5.5V	Operating Temperature (Ambient)	-55°C to +125°C
Address/Enable Input Current	-20mA	Maximum Junction Temperature	+175°C
Output Sink Current	100mA		

CAUTION: Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied. (While programming, follow the programming specifications.)

D.C. ELECTRICAL CHARACTERISTICS (Operating)

HM-7644A-5 (V_{CC} = 5.0V ± 5%, T_A = 0°C to +75°C)
HM-7644A-2 (V_{CC} = 5.0V ± 10%, T_A = -55°C to +125°C)
Typical measurements are at T_A = 25°C, V_{CC} = +5V

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
I_{IH} I_{IL}	Address Input "1" Current "0"	– –	– -50.0	+40 -250	µA µA	V_{IH} = V_{CC} Max. V_{IL} = 0.45V
V_{IH} V_{IL}	Input Threshold "1" Voltage "0"	2.0 –	1.5 1.5	– 0.8	V V	V_{CC} = V_{CC} Min. V_{CC} = V_{CC} Max.
V_{OH} V_{OL}	Output "1" Voltage "0"	2.4 –	3.2 0.35	– 0.45	V V	I_{OH} = -2.0mA, V_{CC} = V_{CC} Min. I_{OL} = +16mA, V_{CC} = V_{CC} Min.
V_{CL}	Input Clamp Voltage	–	–	-1.2	V	I_{IN} = -18mA
I_{OS}	Output Short Circuit Current	-15	–	-100	mA	V_{OUT} = 0.0V, One Output at a Time for a Max. of 1 Second
I_{CC}	Power Supply Current	–	100	140	mA	V_{CC} = V_{CC} Max., All Inputs Grounded.

NOTE: Positive current defined as into device terminals.

A.C. ELECTRICAL CHARACTERISTICS (Operating)

		HM-7644A-5 5V ± 5% 0°C to +75°C			HM-7644A-2 5V ± 10% -55°C to +125°C			
SYMBOL	PARAMETER	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
T_{AA}	Address Access Time	–	35	50	–	–	60	ns

A.C. limits guaranteed for worst case N^2 sequencing.

CAPACITANCE: T_A = 25°C

SYMBOL	PARAMETER	MAXIMUM	UNITS	TEST CONDITIONS
C_{INA}	Input Capacitance	8	pF	V_{CC} = 5V, V_{IN} = 2.0V, f = 1MHz
C_{OUT}	Output Capacitance	10	pF	V_{CC} = 5V, V_{OUT} = 2.0V, f = 1MHz

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HARRIS SEMICONDUCTOR PRODUCTS DIVISION
A DIVISION OF HARRIS CORPORATION

HM-7645

1K x 4 PROM

"Three State" Outputs

Preview

Features

- 50ns MAXIMUM ADDRESS ACCESS TIME
- "THREE STATE" OUTPUTS AND FOUR CHIP ENABLE INPUTS
- SIMPLE HIGH SPEED PROGRAMMING PROCEDURE ONE PULSE/BIT. ASSURES FAST PROGRAMMING AND SUPERIOR RELIABILITY.
- FAST ACCESS TIME – GUARANTEED FOR WORST CASE N^2 SEQUENCING OVER COMMERCIAL AND MILITARY TEMPERATURE AND VOLTAGE RANGES.
- INDUSTRY'S HIGHEST PROGRAMMING YIELD.
- 2142 PINOUT

Description

The HM-7645 is a fully decoded high speed Schottky TTL 4096 Bit Field Programmable PROM in a 1K word by 4 bit/word format with "Three State" outputs. This PROM is available in a 20 pin DIP (ceramic or epoxy) and a 20 pin flat pack.

All bits are manufactured storing a logical "1" (positive logic) and can be selectively programmed for a logical "0" in any bit position.

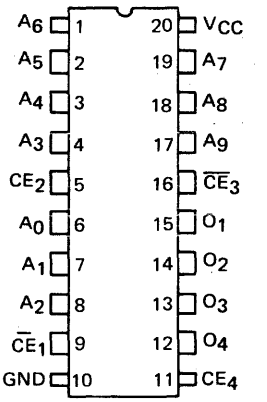
Nichrome fuse technology is used on this and all other Harris Bipolar PROMs.

The HM-7645 contains test rows and columns which are in addition to the storage array to assure high programmability and guarantee parametrics and A.C. performance. The fuses in these test rows and columns are blown prior to shipment.

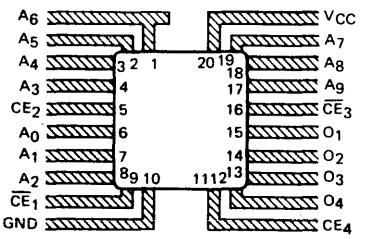
There are four chip enable inputs on the HM-7645. $\overline{CE}_1$, $\overline{CE}_3$ low and CE_2, CE_4 high enables the chip.

Pinout

TOP VIEW–DIP



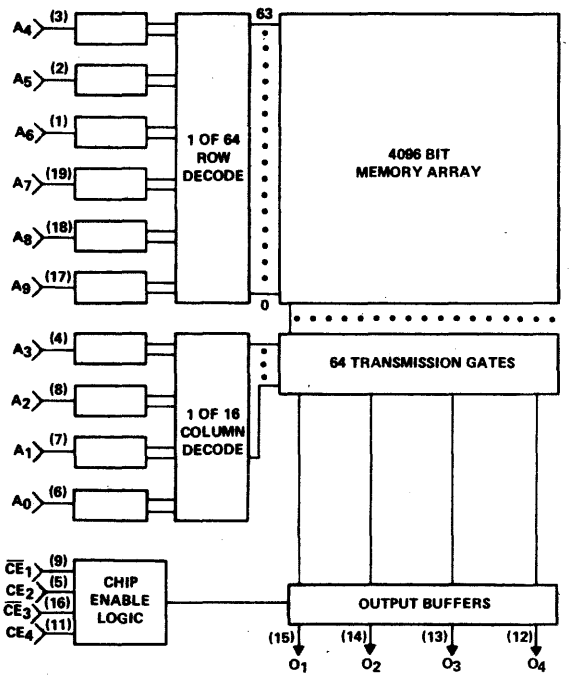
TOP VIEW–FLAT PACK



PIN NAMES

A_0 - A_9	ADDRESS INPUTS
O_1 - O_4	DATA OUTPUTS
$\overline{CE}_1$, $\overline{CE}_3$	CHIP ENABLE INPUTS
CE_2, CE_4	

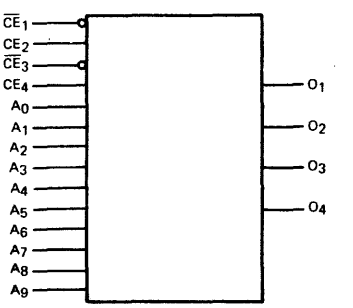
Functional Diagram



NOTE: Physical bit positions for columns are as follows:
O_1, O_3 = (15, 0 ⟶ 14)
O_2, O_4 = (0 ⟶ 15)

( ) = Pin Numbers
(20) = V_{CC}
(10) = GND

Logic Symbol



"SEE PAGES 1409-1415 FOR PACKAGE SELECTION GUIDE"

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ABSOLUTE MAXIMUM RATINGS

Output or Supply Voltage (Operating)	-0.3 to +7.0V	Storage Temperature	-65°C to +150°C
Address/Enable Input Voltage	5.5V	Operating Temperature (Ambient)	-55°C to +125°C
Address/Enable Input Current	-20mA	Maximum Junction Temperature	+175°C
Output Sink Current	100mA		

CAUTION: Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied. (While programming, follow the programming specifications.)

D.C. ELECTRICAL CHARACTERISTICS (Operating)

HM-7645-5 (V_{CC} = 5.0V ± 5%, T_A = 0°C to +75°C)
HM-7645-2 (V_{CC} = 5.0V ± 10%, T_A = -55°C to +125°C)
Typical Measurements are at T_A = 25°C, V_{CC} = +5V

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
I_{IH}	Address/Enable "1"	–	–	+40	μA	V_{IH} = V_{CC} Max.
I_{IL}	Input Current "0"	–	-50.0	-250	μA	V_{IL} = 0.45V
V_{IH}	Input Threshold "1"	2.0	1.5	–	V	V_{CC} = V_{CC} Min.
V_{IL}	Voltage "0"	–	1.5	0.8	V	V_{CC} = V_{CC} Max.
V_{OH}	Output "1"	2.4	3.2	–	V	I_{OH} = -2.0mA, V_{CC} = V_{CC} Min.
V_{OL}	Voltage "0"	–	0.35	0.50	V	I_{OL} = +16mA, V_{CC} = V_{CC} Min.
I_{OHE}	Output Disable "1"	–	–	+40	μA	V_{OH}, V_{CC} = V_{CC} Max.
I_{OLE}	Current "0"	–	–	-40	μA	V_{OL} = 0.3V, V_{CC} = V_{CC} Max.
V_{CL}	Input Clamp Voltage	–	–	-1.2	V	I_{IN} = -18mA
I_{OS}	Output Short Circuit Current	-15	–	-100	mA	V_{OUT} = 0.0V, One Output at a Time for a Max. of 1 Second
I_{CC}	Power Supply Current	–	100	140	mA	V_{CC} = V_{CC} Max., All Inputs Grounded.

NOTE: Positive current defined as into device terminals.

A.C. ELECTRICAL CHARACTERISTICS (Operating)

		HM-7645-5 5V ±5% 0°C to +75°C			HM-7645-2 5V ±10% -55°C to +125°C			
SYMBOL	PARAMETER	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
T_{AA}	Address Access Time	–	35	50	–	–	70	ns
T_{EA}	Chip Enable Access Time	–	25	30	–	–	40	ns

A.C. limits guaranteed for worst case N^2 sequencing.

CAPACITANCE: T_A = 25°C

SYMBOL	FARAMETER	MAXIMUM	UNITS	TEST CONDITIONS
C_{INA}, C_{INCE}	Input Capacitance	8	pF	V_{CC} = 5V, V_{IN} = 2.0V, f = 1MHz
C_{OUT}	Output Capacitance	10	pF	V_{CC} = 5V, V_{OUT} = 2.0V, f = 1MHz

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HM-7645P

1K x 4 PROM

"Three State" Outputs

Preview

Features

- 50ns MAXIMUM ADDRESS ACCESS TIME
- "THREE STATE" OUTPUTS AND FOUR POWER DOWN INPUTS
- SIMPLE HIGH SPEED PROGRAMMING PROCEDURE - ONE PULSE/BIT ASSURES FAST PROGRAMMING AND SUPERIOR RELIABILITY
- FAST ACCESS TIME - FOR WORST CASE N^2 SEQUENCING OVER COMMERCIAL AND MILITARY TEMPERATURE AND VOLTAGE RANGES
- INDUSTRY'S HIGHEST PROGRAMMING YIELD
- 2142 PINOUT

Description

The HM-7645P is a fully decoded high speed Schottky TTL 4096-Bit Field Programmable ROM in a 1K by 4 bit/word format with "Three State" outputs. This PROM is available in a 20 pin DIP (ceramic or epoxy) and a 20 pin flatpack.

All bits are manufactured storing a logical "1" (positive logic) and can be selectively programmed for a logical "0" in any bit position.

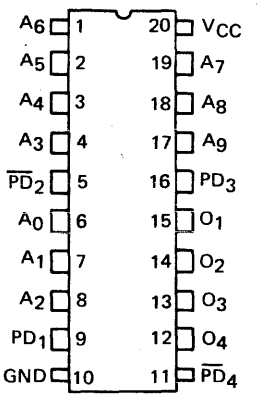
Nichrome fuse technology is used on these and all other Harris Bipolar PROM's.

The HM-7645P contains test rows and columns which are in addition to the storage array to assure high programmability and guarantee parametrics and A.C. performance. The fuses in these test rows and columns are blown prior to shipment.

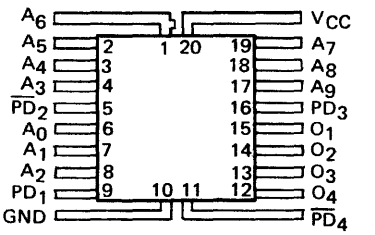
There are four power down inputs on the HM-7645P which are similar to chip enables. The chip is enabled or disabled using the power down inputs where a disabled chip dissipates 30% of nominal power and the outputs go to a high impedance state. The chip is powered up (enabled) when PD_1, PD_3 are low, and $\overline{PD}_2$, $\overline{PD}_4$ are high.

Pinouts

TOP VIEW - DIP



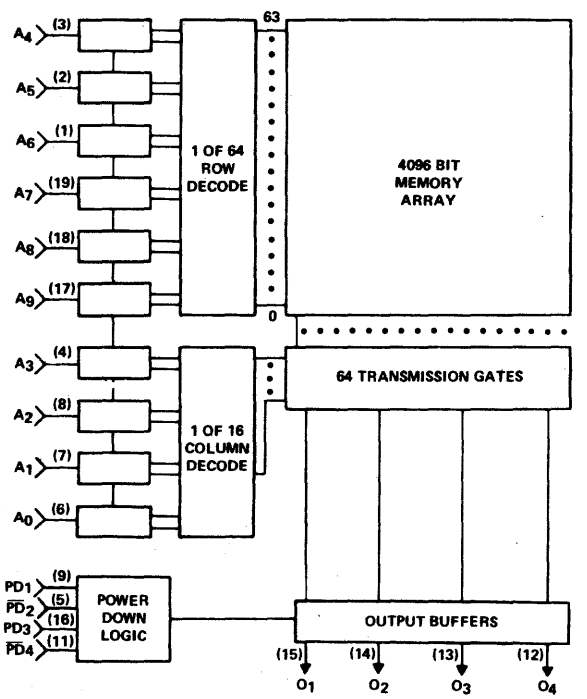
TOP VIEW - FLATPACK



PIN NAMES

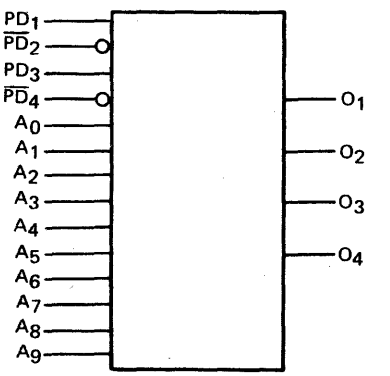
A_0-A_9	Address Inputs
O_1-O_4	Data Outputs
PD_1, $\overline{PD}_2$, PD_3, $\overline{PD}_4$	Power Down Inputs

Functional Diagram



NOTE: Physical bit positions for columns are as follows:
O_1, O_3 = (15, 0 → 14)
O_2, O_4 = (0 → 15)

Logic Diagram



"SEE PAGES 1409-1415 FOR PACKAGE SELECTION GUIDE"

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ABSOLUTE MAXIMUM RATINGS

Output or Supply Voltage (Operating)	-0.3 to +7.0V	Storage Temperature	-65°C to +150°C
Address/Enable Input Voltage	5.5V	Operating Temperature (Ambient)	-55°C to +125°C
Address/Enable Input Current	-20mA	Maximum Junction Temperature	+175°C
Output Sink Current	100mA		

CAUTION: Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied. (While programming, follow the programming specifications.)

D.C. ELECTRICAL CHARACTERISTICS (Operating)

HM-7645P-5 (V_{CC} = 5.0V ± 5%, T_A = 0°C to +75°C)
HM-7645P-2 (V_{CC} = 5.0V ± 10%, T_A = -55°C to +125°C)
Typical measurements are at T_A = 25°C, V_{CC} = +5V

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
I_{IH} I_{IL}	Address/Enable "1" Input Current "0"	– –	– -50.0	+40 -250	μA μA	V_{IH} = V_{CC} Max. V_{IL} = 0.45V
V_{IH} V_{IL}	Input Threshold "1" Voltage "0"	2.0 –	1.5 1.5	– 0.8	V V	V_{CC} = V_{CC} Min. V_{CC} = V_{CC} Max.
V_{OH} V_{OL}	Output "1" Voltage "0"	2.4 –	3.2 0.35	– 0.50	V V	I_{OH} = -2.0mA, V_{CC} = V_{CC} Min. I_{OL} = +16mA, V_{CC} = V_{CC} Min.
I_{OHE} I_{OLE}	Output Disable "1" Current "0"	– –	– –	+40 -40	μA μA	V_{OH}, V_{CC} = V_{CC} Max. V_{OL} = 0.3V, V_{CC} = V_{CC} Max.
V_{CL}	Input Clamp Voltage	–	–	-1.2	V	I_{IN} = -18mA
I_{OS}	Output Short Circuit Current	-15	–	-100	mA	V_{OUT} = 0.0V, One Output at a Time for a Max. of 1 Second
I_{CC}	Power Supply Current	–	100	140	mA	V_{CC} = V_{CC} Max., All Inputs Grounded.

NOTE: Positive current defined as into device terminals.

A.C. ELECTRICAL CHARACTERISTICS (Operating)

		HM-7645P-5 5V ± 5% 0°C to +75°C			HM-7645P-2 5V ± 10% -55°C to +125°C			
SYMBOL	PARAMETER	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
T_{AA}	Address Access Time	-	35	50	-	-	70	ns
T_{PD}	Chip Power-Down Access Time	-	25	30	-	-	40	ns
T_{PU}	Chip Power-Up Access Time	-	80	100	-	-	150	s

A.C. limits guaranteed for worst case N^2 sequencing.

CAPACITANCE: T_A = 25°C

SYMBOL	PARAMETER	MAXIMUM	UNITS	TEST CONDITIONS
C_{INA}, C_{INCE}	Input Capacitance	8	pF	V_{CC} = 5V, V_{IN} = 2.0V, f = 1MHz
C_{OUT}	Output Capacitance	10	pF	V_{CC} = 5V, V_{OUT} = 2.0V, f = 1MHz

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HM-7647R

512 x 8 PROM

Features

- 60ns MAXIMUM ADDRESS ACCESS TIME
- "THREE STATE" OUTPUTS WITH TWO CHIP ENABLE INPUTS
- SIMPLE HIGH SPEED PROGRAMMING PROCEDURE – ONE PULSE/BIT. ASSURES FAST PROGRAMMING AND SUPERIOR RELIABILITY.
- FAST ACCESS TIME – GUARANTEED FOR WORST CASE N^2 SEQUENCING OVER COMMERCIAL AND MILITARY TEMPERATURE AND VOLTAGE RANGES.
- INDUSTRY'S HIGHEST PROGRAMMING YIELD
- PIN COMPATIBLE WITH THE 82S115
- LATCHED OUTPUTS
- INPUT LOADING IS – 100 μA MAXIMUM

Description

The HM-7647R is a fully decoded high speed Schottlky TTL 4096-Bit Field Programmable ROM in a 512 word by 8 bit/word format and is available in a 24 pin D.I.P. (ceramic or epoxy) and a 24 pin flatpack.

All bits are manufactured storing a logical "1" (positive logic) and can be selectively programmed for a logical "0" in any position. The HM-7647R has "Three State" outputs.

Nichrome fuse technology is used on this and all other Harris Bipolar PROMs.

The pinout is identical to the 82S115 PROM.

The HM-7647R contains test rows and columns which are in addition to the storage array to assure high programmability and guarantee parametric and A.C. performance. The fuses in these test rows and columns are blown prior to shipment.

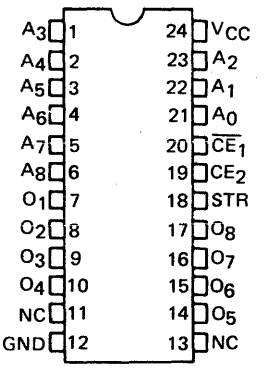
There are two chip enable inputs on the HM-7647R. $\overline{CE}_1$ low and CE_2 high enables the chip.

HM-7647R is operated in the Transparent Read Mode by holding the strobe input high throughout the read operation. This is the normal read mode where the two chip enable inputs will control the outputs.

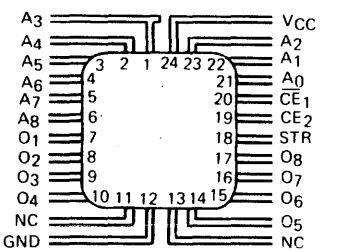
In Latched Read Mode, bringing the strobe input low will latch the outputs and chip enable inputs. If the device is disabled when the strobe input goes low the outputs will be latched in the high impedance state. If the device is in the latched mode the strobe input must be brought high to allow the outputs to respond to new address or chip enable conditions.

Pinout

TOP VIEW – D.I.P.



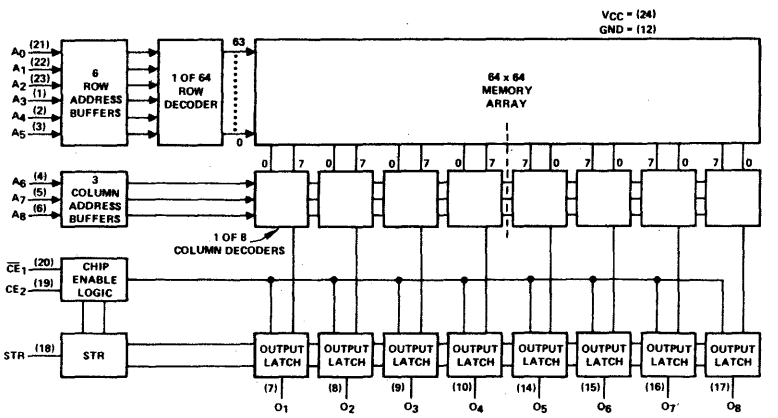
TOP VIEW – FLATPACK



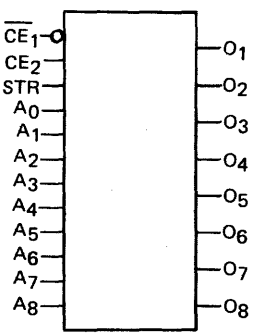
PIN NAMES

$A_0 - A_8$	Address Inputs
$O_1 - O_8$	Data Outputs
$\overline{CE}_1 - CE_2$	Chip Enable Inputs
STR	Latch Input

Functional Diagram



Logic Symbol



"SEE PAGES 1409-1415 FOR PACKAGE SELECTION GUIDE"

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ABSOLUTE MAXIMUM RATINGS

Output or Supply Voltage (Operating)	-0.3 to +7.0V	Storage Temperature	-65°C to +150°C
Address/Enable Input Voltage	5.5V	Operating Temperature (Ambient)	-55°C to +125°C
Address/Enable Input Current	-20mA	Maximum Junction Temperature	+175°C
Output Sink Current	100mA		

CAUTION: Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied. (While programming, follow the programming specifications.)

D.C. ELECTRICAL CHARACTERISTICS (Operating)

HM-7647R-5 (V_{CC} = 5.0V ±5%, T_A = 0°C to +75°C)
HM-7647R-2 (V_{CC} = 5.0V ±10%, T_A = -55°C to +125° C)
Typical measurements are at T_A = 25°C, V_{CC} = +5V

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
I_{IH}	Address/Enable "1"	–	–	+25	μA	V_{IH} = V_{CC} Max.
I_{IL}	Input Current "0"	–	-50	-100(1)	μA	V_{IL} = 0.45V
V_{IH}	Input Threshold "1"	2.0	1.5	–	V	V_{CC} = V_{CC} Min.
V_{IL}	Voltage "0" "0"	–	1.5	0.85	V	V_{CC} = V_{CC} Max.
V_{OH}	Output "1" "1"	2.7(2)	3.3	–	V	I_{OH} = -2.0mA, V_{CC} = V_{CC} Min.
V_{OL}	Voltage "0" "0"	–	0.35	0.50	V	I_{OL} = +16mA, V_{CC} = V_{CC} Min.
I_{OHE}	Output Disable "1"	–	–	+40	μA	V_{OH}, V_{CC} = V_{CC} Max.
I_{OLE}	Current "0" "0"	–	–	-40	μA	V_{OL} = 0.3V, V_{CC} = V_{CC} Max.
V_{CL}	Input Clamp Voltage	–	–	-1.2	V	I_{IN} = -18mA
I_{OS}	Output S.C. Current	-20	–	-70	mA	V_{OUT} = 0.0V One Output Only for a Max. of 1 Second
I_{CC}	Power Supply Current	–	135	185	mA	V_{CC} = V_{CC} Max. All Inputs Grounded

*Positive current defined as into device terminals.

NOTE(1): I_{IL} = -150 μA for -2

NOTE(2): V_{OH} = 2.4V for -2

A.C. ELECTRICAL CHARACTERISTICS (Operating)

		HM-7647R-5 5V ± 5% 0°C to +75°C			HM-7647R-2 5V ± 10% -55°C to +125°C				
SYMBOL	PARAMETER	MIN	TYP	MAX	MIN	TYP	MAX	UNITS	TEST CONDIT.
T_{AA}	Address Access Time	–	40	60	–	50	80	ns	
T_{EA}	Chip Enable Access Time	–	30	40	–	40	50	ns	Transparent
T_{ADH}	Address Hold Time	0	-10	–	0	-10	–	ns	Latched
T_{CDH}	Chip Enable Hold Time	10	0	–	10	0	–	ns	
T_{SW}	Strobe Pulse Width	30	15	–	40	15	–	ns	
T_{SL}	Strobe Latch Time	60	35	–	80	45	–	ns	
T_{DL}	Strobe Delatch Time	–	–	40	–	–	50	ns	
T_{CDS}	Chip Enable Set-Up Time	40	–	–	50	–	–	ns	

A.C. limits guaranteed for worst case N^2 sequencing.

CAPACITANCE: T_A = 25°C

SYMBOL	PARAMETER	MAXIMUM	UNITS	TEST CONDITIONS
C_{INA}, C_{INCE}	Input Capacitance	8	pF	V_{CC} = 5V, V_{IN} = 2.0V, f = 1MHz
C_{OUT}	Output Capacitance	10	pF	V_{CC} = 5V, V_{OUT} = 2.0V, f = 1MHz

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HARRIS SEMICONDUCTOR PRODUCTS DIVISION
A DIVISION OF HARRIS CORPORATION

HM-7648/49

512 x 8 PROM

HM-7648 - Open Collector Outputs
HM-7649 - "Three State" Outputs

Features

- 60ns MAXIMUM ADDRESS ACCESS TIME
- "THREE STATE" OR OPEN COLLECTOR OUTPUTS AND A CHIP ENABLE INPUT
- SIMPLE HIGH SPEED PROGRAMMING PROCEDURE - ONE PULSE/BIT ASSURES FAST PROGRAMMING AND SUPERIOR RELIABILITY.
- FAST ACCESS TIME - GUARANTEED FOR WORST CASE N^2 SEQUENCING OVER COMMERCIAL AND MILITARY TEMPERATURE AND VOLTAGE RANGES.
- INDUSTRY'S HIGHEST PROGRAMMING YIELD
- PIN COMPATIBLE WITH THE 74S472/73
- LOW INPUT LOADING

Description

The HM-7648/49 is a fully decoded high speed Schottky TTL 4096-Bit Field Programmable ROM in a 512 word by 8 bit/word format with open collector (HM-7648) or "Three State" (HM-7649) outputs. These PROMs are available in a 24 pin D.I.P. (ceramic or epoxy) and a 24 pin flat pack.

All bits are manufactured storing a logical "1" (positive logic) and can be selectively programmed for a logical "0" in any bit position.

Nichrome fuse technology is used on this and all other Harris Bipolar PROMs.

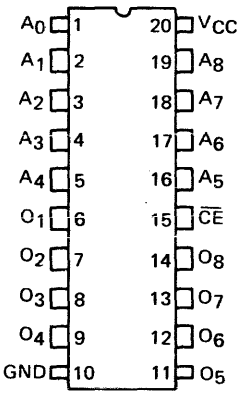
The pinout is identical to the 74S472/73 PROM.

The HM-7648/49 contains test rows and columns which are in addition to the storage array to assure high programmability and guarantee parametic and A.C. performance. The fuses in these test rows and columns are blown prior to shipment.

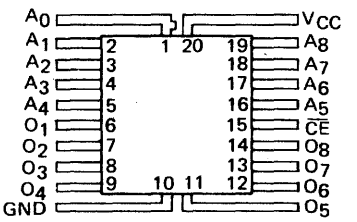
There is a chip enable input on the HM-7648/49 where $\overline{CE}$ low enables the device.

Pinouts

TOP VIEW - D.I.P.



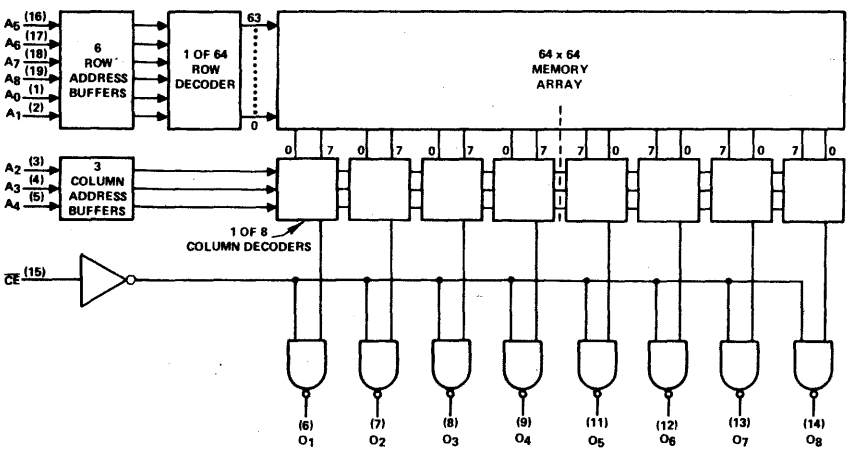
TOP VIEW - FLATPACK



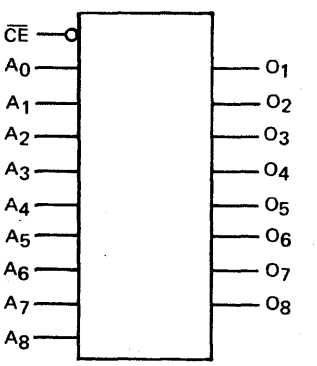
PIN NAMES

$A_0 - A_8$	Address Inputs
$O_1 - O_8$	Data Outputs
$\overline{CE}$	Chip Enable Input

Functional Diagram



Logic Symbol



"SEE PAGES 1409-1415 FOR PACKAGE SELECTION GUIDE"

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ABSOLUTE MAXIMUM RATINGS

Output or Supply Voltage (Operating)	-0.3 to +7.0V	Storage Temperature	-65°C to +150°C
Address/Enable Input Voltage	5.5V	Operating Temperature (Ambient)	-55°C to +125°C
Address/Enable Input Current	-20mA	Maximum Junction Temperature	+175°C
Output Sink Current	100mA		

CAUTION: Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied. (While programming, follow the programming specifications.)

D.C. ELECTRICAL CHARACTERISTICS (Operating)

HM-7648/49-5 (V_{CC} = 5.0V ± 5%, T_A = 0°C to +75°C)
HM-7648/49-2 (V_{CC} = 5.0V ± 10%, T_A = -55°C to +125°C)
Typical measurements are at T_A = 25°C, V_{CC} = +5V

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
I_{IH} I_{IL}	Address/Enable "1" Input Current "0"	– –	– -50	+25 -250	µA µA	V_{IH} = V_{CC} Max. V_{IL} = 0.45V
V_{IH} V_{IL}	Input Threshold "1" Voltage "0"	2.0 –	1.5 1.5	– 0.80	V V	V_{CC} = V_{CC} Min. V_{CC} = V_{CC} Max.
V_{OH} V_{OL}	Output "1" Voltage "0"	2.4 * –	3.2* 0.35	– 0.50	V V	I_{OH} = -2.0mA, V_{CC} = V_{CC} Min. I_{OL} = +16mA, V_{CC} = V_{CC} Min.
I_{OHE} I_{OLE}	Output Disable "1" Current "0"	– –	– –	+50 -50 *	µA µA	V_{OH}, V_{CC} = V_{CC} Max. V_{OL} = 0.3V, V_{CC} = V_{CC} Max.
V_{CL}	Input Clamp Voltage	–	–	-1.2	V	I_{IN} = -18mA
I_{OS}	Output S.C. Current	-20*	–	-100*	mA	V_{OUT} = 0.0V One Output Only for a Max. of 1 Second
I_{CC}	Power Supply Current	–	120	170	mA	V_{CC} = V_{CC} Max. All Inputs Grounded

* "Three State" only
NOTE: Positive current defined as into device terminals.

A.C. ELECTRICAL CHARACTERISTICS (Operating)

		HM-7648/49-5 5V ±5% 0°C to + 75°C			HM-7648/49-2 5V ±10% -55°C to +125°C			
SYMBOL	PARAMETER	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
T_{AA}	Address Access Time	–	55	60	–	50	80	ns
T_{EA}	Chip Enable Access Time	–	20	40	–	30	50	ns

A.C. limits guaranteed for worst case N^2 sequencing.

CAPACITANCE: T_A = 25°C

SYMBOL	PARAMETER	MAXIMUM	UNITS	TEST CONDITIONS
C_{INA}, C_{INCE}	Input Capacitance	8	pF	V_{CC} = 5V, V_{IN} = 2.0V, f = 1MHz
C_{OUT}	Output Capacitance	10	pF	V_{CC} = 5V, V_{OUT} = 2.0V, f = 1MHz

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HM-7680/81

1K x 8 PROM

HM-7680 - Open Collector Outputs
HM-7681 - "Three State" Outputs

Preliminary

Features

- 60ns MAXIMUM ADDRESS ACCESS TIME
- "THREE STATE" OR OPEN COLLECTOR OUTPUTS AND FOUR CHIP ENABLE INPUTS
- SIMPLE HIGH SPEED PROGRAMMING PROCEDURE ONE PULSE/BIT. ASSURES FAST PROGRAMMING AND SUPERIOR RELIABILITY.
- FAST ACCESS TIME – GUARANTEED FOR WORST CASE N^2 SEQUENCING OVER COMMERCIAL AND MILITARY TEMPERATURE AND VOLTAGE RANGES.
- INDUSTRY'S HIGHEST PROGRAMMING YIELD

Description

The HM-7680/81 is a fully decoded high speed Schottky TTL 8192/Bit Field Programmable ROM in a 1K word by 8 bit/word format with open collector (HM-7680) or "Three State" (HM-7681) outputs. These PROM's are available in a 24 pin D.I.P. (ceramic or epoxy) and a 24 pin flat pack.

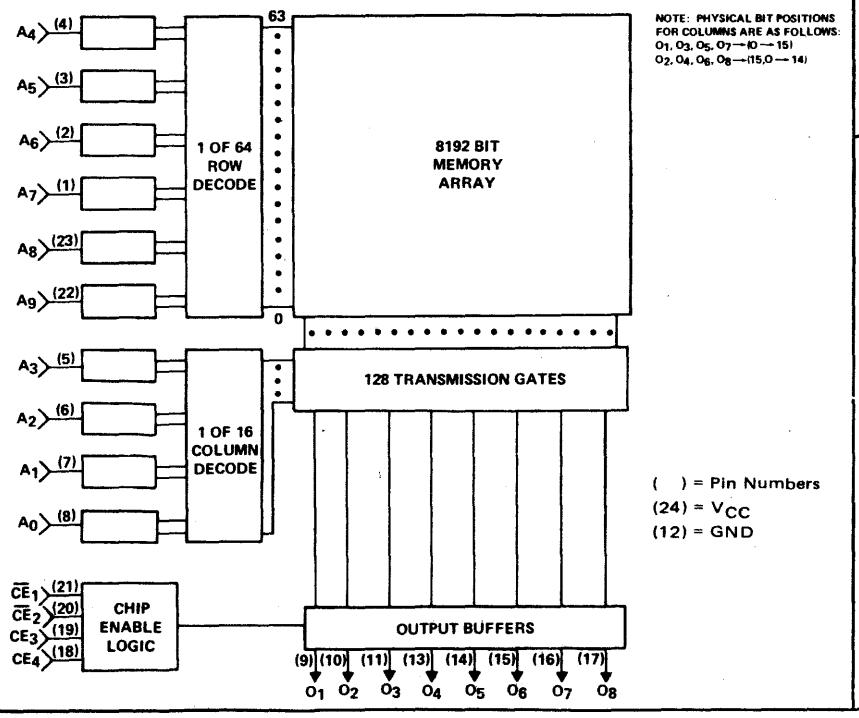
All bits are manufactured storing a logical "1" (Positive Logic) and can be selectively programmed for a logical "0" in any one bit position.

Nichrome fuse technology is used on this and all other Harris Bipolar PROMs.

The HM-7680/81 contains test rows and columns which are in addition to the storage array to assure high programmability and guarantee parametric and A.C. performance. The fuses in these test rows and columns are blown prior to shipment.

There are four chip enable inputs on the HM-7680/81. $\overline{CE}_1$, $\overline{CE}_2$ low, and CE_3, CE_4 high enables the chip.

Functional Diagram

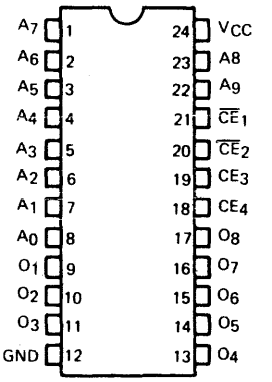


NOTE: PHYSICAL BIT POSITIONS FOR COLUMNS ARE AS FOLLOWS:
O_1, O_3, O_5, O_7 — (0 — 15)
O_2, O_4, O_6, O_8 — (15,0 — 14)

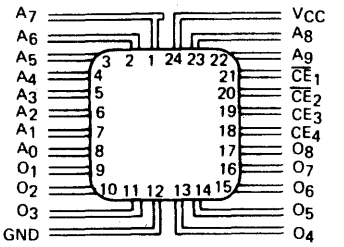
( ) = Pin Numbers
(24) = V_{CC}
(12) = GND

Pinouts

TOP VIEW—DIP



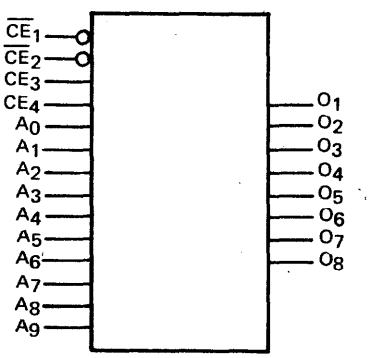
TOP VIEW – FLATPACK



PIN NAMES

$A_0 - A_9$	Address Inputs
$O_1 - O_8$	Data Outputs
$\overline{CE}_1, \overline{CE}_2, CE_3, CE_4$	Chip Enable Inputs

Logic Symbol



"SEE PAGES 1409-1415 FOR PACKAGE SELECTION GUIDE"

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ABSOLUTE MAXIMUM RATINGS

Output or Supply Voltage (Operating)	-0.3 to +7.0V	Storage Temperature	-65°C to +150°C
Address/Enable Input Voltage	5.5V	Operating Temperature (Ambient)	-55°C to +125°C
Address/Enable Input Current	-20mA	Maximum Junction Temperature	+175°C
Output Sink Current	100mA		

CAUTION: Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied. (While programming, follow the programming specifications.)

D.C. ELECTRICAL CHARACTERISTICS (Operating)

HM-7680/81-5 (V_{CC} = 5.0V ±5%, T_A = 0°C to +75°C)
HM-7680/81-2 (V_{CC} = 5.0V ±10%, T_A = -55°C to +125°C)
Typical measurements are at T_A = 25°C, V_{CC} = +5V

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
I_{IH} I_{IL}	Address/enable "1" Input Current "0"	– –	– -50.0	+40 -250	µA µA	V_{IH} = V_{CC} Max. V_{IL} = 0.45V
V_{IH} V_{IL}	Input Threshold "1" Voltage "0"	2.0 –	1.5 1.5	– 0.8	V V	V_{CC} = V_{CC} Min. V_{CC} = V_{CC} Max.
V_{OH} V_{OL}	Output "1" Voltage "0"	2.4 * –	3.2* 0.35	– 0.50	V V	I_{OH} = -2.0mA, V_{CC} = V_{CC} Min. I_{OL} = +16mA, V_{CC} = V_{CC} Min.
I_{OHE} I_{OLE}	Output Disable "1" Current "0"	– –	– –	+40 -40*	µA µA	V_{OH}, V_{CC} = V_{CC} Max. V_{OL} = 0.3V, V_{CC} = V_{CC} Max.
V_{CL}	Input Clamp Voltage	–	–	-1.2	V	I_{IN} = -18mA
I_{OS}	Output S.C. Current	-15*	–	-100*	mA	V_{OUT} = 0.0V One Output Only for a Max. of 1 Second
I_{CC}	Power Supply Current	–	130	170	mA	V_{CC} = V_{CC} Max. All Inputs Grounded

NOTE: Positive current defined as into device terminals.
* "Three State" only

A.C. ELECTRICAL CHARACTERISTICS (Operating)

		HM-7680/81-5 5V ±5% 0°C to + 75°C			HM-7680/81-2 5V ±10% -55°C to +125°C			
SYMBOL	PARAMETER	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
T_{AA}	Address Access Time	–	45	60	–	–	80	ns
T_{EA}	Chip Enable Access Time	–	30	40	–	–	50	ns

A.C. limits guaranteed for worst case N^2 sequencing.

CAPACITANCE : T_A = 25°C

SYMBOL	PARAMETER	MAXIMUM	UNITS	TEST CONDITIONS
C_{INA}, C_{INCE}	Input Capacitance	8	pF	V_{CC} = 5V, V_{IN} = 2.0V, f = 1MHz
C_{OUT}	Output Capacitance	10	pF	V_{CC} = 5V, V_{OUT} = 2.0V, f = 1MHz

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HARRIS SEMICONDUCTOR PRODUCTS DIVISION
A DIVISION OF HARRIS CORPORATION

HM-7680R/81R

1K x 8 PROM

HM-7680R - Open Collector Outputs
HM-7681R - "Three State" Outputs

Preliminary

Features

- 60ns MAXIMUM ADDRESS ACCESS TIME
- "THREE STATE" OR OPEN COLLECTOR OUTPUTS AND THREE CHIP ENABLE INPUTS
- SIMPLE HIGH SPEED PROGRAMMING PROCEDURE - ONE PULSE/BIT ASSURES FAST PROGRAMMING AND SUPERIOR RELIABILITY
- FAST ACCESS TIME - GUARANTEED FOR WORST CASE N^2 SEQUENCING OVER COMMERCIAL AND MILITARY TEMPERATURES AND VOLTAGE RANGES
- INDUSTRY'S HIGHEST PROGRAMMING YIELD
- LATCHED OUTPUTS

Description

The HM-7680R/81R is a fully decoded high speed Schottky TTL 8192-Bit Field Programmable ROM in a 1K word by 8 bit/word format with open collector (HM-7680R) or "Three State" (HM-7681R) outputs. These PROMs are available in a 24 pin D.I.P. (ceramic or epoxy) and a 24 pin flatpack.

All bits are manufactured storing a logical "1" (positive logic) and can be selectively programmed for a logical "0" in any bit position.

Nichrome fuse technology is used on these and all other Harris Bipolar PROMs.

The HM-7680R/81R contains test rows and columns which are in addition to the storage array to assure high programmability and guarantee parametric and A.C. performance. The fuses in these test rows and columns are blown prior to shipment.

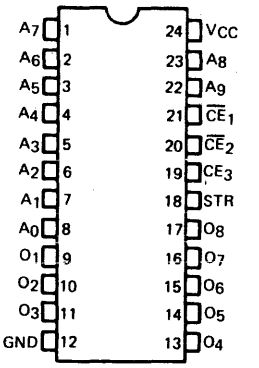
There are three chip enable inputs on the HM-7680R/81R. $\overline{CE}_1$, $\overline{CE}_2$ low and CE_3 high enables the chip.

The HM-7680R/81R is operated in the Transparent Read Mode by holding the strobe input high throughout the read operation. This is the normal read mode where the three chip enable inputs will control the outputs.

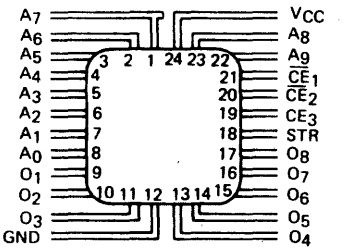
In Latched Read Mode, bringing the strobe input low will latch the outputs and chip enable inputs. If the device is disabled when the strobe input goes low, the outputs will be latched in the high impedance state. If the device is in the latched mode the strobe input must be brought high to allow the outputs to respond to new address or chip enable conditions.

Pinouts

TOP VIEW—DIP



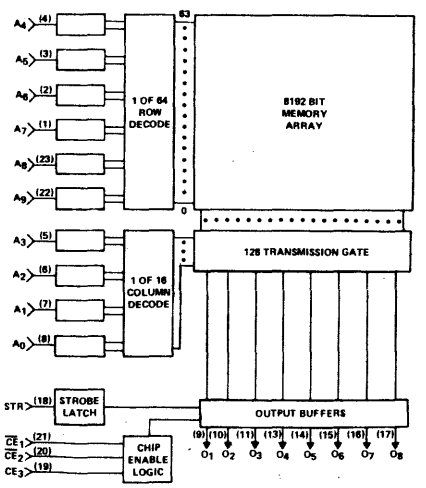
TOP VIEW – FLATPACK



PIN NAMES

A0 – A9	Address Inputs
O1 – O8	Data Outputs
CE1, CE2, CE3	Chip Enable Inputs
STR	Strobe

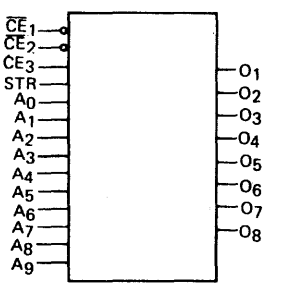
Functional Diagram



NOTE: Physical bit positions for columns are as follows:
$O_1, O_3, O_5, O_7 \rightarrow (0 \rightarrow 15)$
$O_2, O_4, O_6, O_8 \rightarrow (15, 0 \rightarrow 14)$

( ) = Pin Numbers
(24) = V_{CC}
(12) = GND

Logic Symbol



"SEE PAGES 1409-1415 FOR PACKAGE SELECTION GUIDE"

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ABSOLUTE MAXIMUM RATINGS

Output or Supply Voltage (Operating)	-0.3 to +7.0V	Storage Temperature	-65°C to +150°C
Address/Enable Input Voltage	5.5V	Operating Temperature (Ambient)	-55°C to +125°C
Address/Enable Input Current	-20mA	Maximum Junction Temperature	+175°C
Output Sink Current	100mA		

CAUTION: Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied. (While programming, follow the programming specifications.)

D.C. ELECTRICAL CHARACTERISTICS (Operating)

HM-7680R/81R-5 (V_{CC} = 5.0V ±5%, T_A = 0°C to +75°C)
HM-7680R/81R-2 (V_{CC} = 5.0V ±10%, T_A = -55°C to +125°C)
Typical measurements are at T_A = 25°C, V_{CC} = +5V

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
I_{IH} I_{IL}	Address/Enable "1" Input Current "0"	– –	– -50.0	+40 -250	µA µA	V_{IH} = V_{CC} Max. V_{IL} = 0.45V
V_{IH} V_{IL}	Input Threshold "1" Voltage "0"	2.0 –	1.5 1.5	– 0.8	V V	V_{CC} = V_{CC} Min. V_{CC} = V_{CC} Max.
V_{OH} V_{OL}	Output "1" Voltage "0"	2.4*	3.2* 0.35	– 0.50	V V	I_{OH} = -2.0mA, V_{CC} = V_{CC} Min. I_{OL} = +16mA, V_{CC} = V_{CC} Min.
I_{OHE} I_{OLE}	Output Disable "1" Current "0"	– –	– –	+40 -40*	µA µA	V_{OH}, V_{CC} = V_{CC} Max. V_{OL} = 0.3V, V_{CC} = V_{CC} Max.
V_{CL}	Input Clamp Voltage	–	–	-1.2	V	I_{IN} = -18mA
I_{OS}	Output S.C. Current	-15*	-2.5	-100*	mA	V_{OUT} = 0.0V One Output Only for a Max. of 1 Second
I_{CC}	Power Supply Current	–	130	170	mA	V_{CC} = V_{CC} Max. All Inputs Grounded

NOTE: Positive current defined as into device terminals.
*"Three State" only

A.C. ELECTRICAL CHARACTERISTICS (Operating)

		HM-7680R/81R-5 5V ±5% 0°C to +75°C			HM-7680R/81R-2 5V ±10% -55°C to +125°C				
SYMBOL	PARAMETER	MIN	TYP	MAX	MIN	TYP	MAX	UNITS	TEST CONDIT.
T_{AA} T_{EA}	Address Access Time Chip Enable Access Time	– –	45 30	60 40	– –	– –	80 50	ns ns	Latched or Transparent
T_{ADH} T_{CDH} T_{SW} T_{SL} T_{DL} T_{CDS}	Address Hold Time Chip Enable Hold Time Strobe Pulse Width Strobe Latch Time Strobe Delatch Time Chip Enable Set-Up Time	0 10 30 60 – 40	-10 0 10 40 – –	– – – – 40 –	0 10 40 80 – 50	-10 0 10 40 – –	– – – – 50 –	ns ns ns ns ns ns	Latched Only

A.C. limits guaranteed for worst case N^2 sequencing.

CAPACITANCE: T_A = 25°C

SYMBOL	PARAMETER	MAXIMUM	UNITS	TEST CONDITIONS
C_{INA}, C_{INCE}	Input Capacitance	8	pF	V_{CC} = 5V, V_{IN} = 2.0V, f = 1MHz
C_{OUT}	Output Capacitance	10	pF	V_{CC} = 5V, V_{OUT} = 2.0V, f = 1MHz

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HM-7680P/81P

1K x 8 PROM

HM-7680P - Open Collector Outputs
HM-7681P - "Three State" Outputs

Preview

Features

- 60ns MAXIMUM ADDRESS ACCESS TIME
- "THREE STATE" OR OPEN COLLECTOR OUTPUTS AND FOUR POWER DOWN INPUTS.
- SIMPLE HIGH SPEED PROGRAMMING PROCEDURE – ONE PULSE/BIT. ASSURES FAST PROGRAMMING AND SUPERIOR RELIABILITY.
- FAST ACCESS TIME – FOR WORST CASE N^2 SEQUENCING OVER COMMERCIAL AND MILITARY TEMPERATURE VOLTAGE RANGES.
- INDUSTRY'S HIGHEST PROGRAMMING YIELD.

Description

The HM-7680P/81P is a fully decoded high speed Schottky TTL 8192-Bit Field Programmable ROM in a 1K word by 8 bit/word format with open collector (HM-7680P) or "three state" (HM-7681P) outputs. These PROM's are available in a 24 pin D.I.P. (ceramic or epoxy) and a 24 pin flatpack.

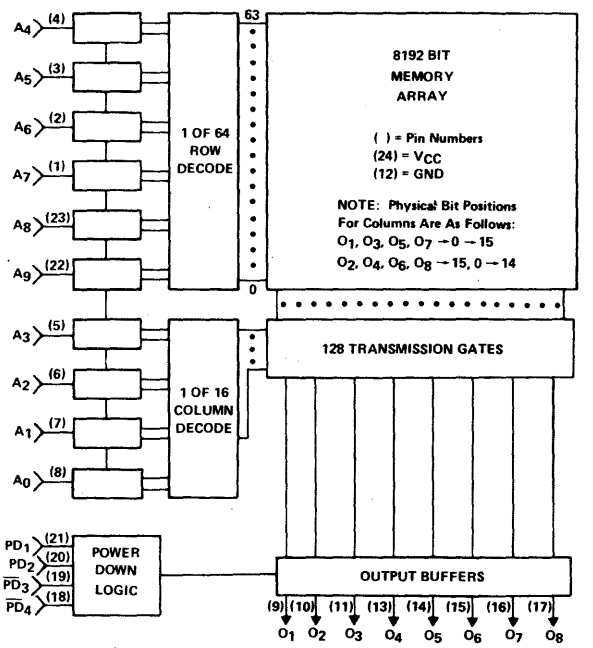
All bits are manufactured storing a logical "1" (positive logic) and can be selectively programmed for a logical "0" in any bit position.

Nichrome fuse technology is used on these and all other Harris Bipolar PROM's.

The HM-7680P/81P contains test rows and columns which are in addition to the storage array to assure high programmability and guarantee parametric and A.C. performance. The fuses in these test rows and columns are blown prior to shipment.

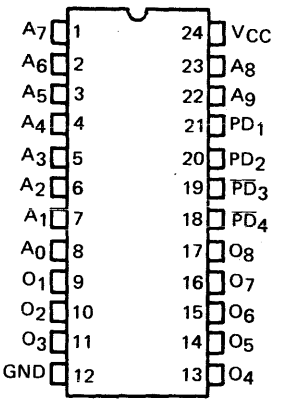
There are four power down inputs on the HM-7680P/81P which are similar to chip enables. The chip is enabled or disabled using the power down inputs where a disabled chip dissipates 30% of nominal power and the outputs go to a high impedance state. The chip is powered up (enabled) when PD_1 and PD_2 are low and $\overline{PD}_3$ and $\overline{PD}_4$ are high.

Functional Diagram

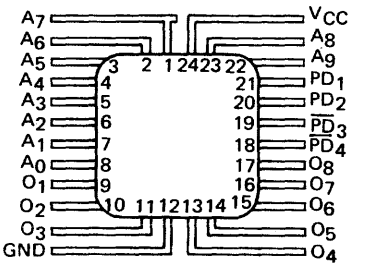


Pinouts

TOP VIEW - DIP



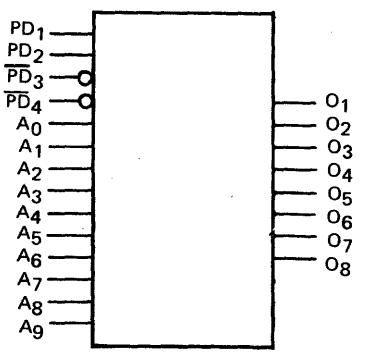
TOP VIEW - FLATPACK



PIN NAMES

A_0 - A_9	Address Inputs
O_1 - O_8	Address Outputs
PD_1, PD_2, $\overline{PD}_3$, $\overline{PD}_4$	Power Down Inputs

Logic Symbol



"SEE PAGES 1409-1415 FOR PACKAGE SELECTION GUIDE"

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ABSOLUTE MAXIMUM RATINGS

Output or Supply Voltage (Operating)	-0.3 to +7.0V	Storage Temperature	-65°C to +150°C
Address/Enable Input Voltage	5.5V	Operating Temperature (Ambient)	-55°C to +125°C
Address/Enable Input Current	-20mA	Maximum Junction Temperature	+175°C
Output Sink Current	100mA		

CAUTION: Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied. (While programming, follow the programming specifications.)

D.C. ELECTRICAL CHARACTERISTICS (Operating)

HM-7680P/81P-5 (V_{CC} = 5.0V ± 5%, T_A = 0°C to +75°C)
HM-7680P/81P-2 (V_{CC} = 5.0V ± 10%, T_A = -55°C to +125°C)
Typical measurements are at T_A = 25°C, V_{CC} = +5V

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
I_{IH}	Address/Enable "1"	–	–	+40	μA	V_{IH} = V_{CC} Max.
I_{IL}	Input Current "0"	–	-50.0	-250	μA	V_{IL} = 0.45V
V_{IH}	Input Threshold "1"	2.0	1.5	–	V	V_{CC} = V_{CC} Min.
V_{IL}	Voltage "0"	–	1.5	0.8	V	V_{CC} = V_{CC} Max.
V_{OH}	Output "1"	2.4*	3.2*	–	V	I_{OH} = -2.0mA, V_{CC} = V_{CC} Min.
V_{OL}	Voltage "0"	–	0.35	0.50	V	I_{OL} = +16mA, V_{CC} = V_{CC} Min.
I_{OHE}	Output Disable "1"	–	–	+40	μA	V_{OH}, V_{CC} = V_{CC} Max.
I_{OLE}	Current "0"	–	–	-40*	μA	V_{OL} = 0.3V, V_{CC} = V_{CC} Max.
V_{CL}	Input Clamp Voltage	–	–	-1.2	V	I_{IN} = -18mA
I_{OS}	Output Short Circuit Current	-15*	–	-100*	mA	V_{OUT} = 0.0V, One Output at a Time for a Max. of 1 Second
I_{CC}	Power Supply Current	–	130	170	mA	V_{CC} = V_{CC} Max., All Inputs Grounded.

NOTE: Positive current defined as into device terminals.
*"Three State" only

A.C. ELECTRICAL CHARACTERISTICS (Operating)

		HM-7680P/81P-5 5V ± 5% 0°C to +75°C			HM-7680P/81P-2 5V ± 10% -55°C to +125°C			
SYMBOL	PARAMETER	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
T_{AA}	Address Access Time	-	45	60	-	-	80	ns
T_{PD}	Chip Power-Down Access Time	-	30	40	-	-	50	ns
T_{PU}	Chip Power-Up Access Time	-	80	100	-	-	150	ns

A.C. limits guaranteed for worst case N^2 sequencing.

CAPACITANCE: T_A = 25°C

SYMBOL	PARAMETER	MAXIMUM	UNITS	TEST CONDITIONS
C_{INA}, C_{INCE}	Input Capacitance	8	pF	V_{CC} = 5V, V_{IN} = 2.0V, f = 1MHz
C_{OUT}	Output Capacitance	10	pF	V_{CC} = 5V, V_{OUT} = 2.0V, f = 1MHz

HM-7680RP/81RP

1K x 8 PROM

HM-7680RP - Open Collector Outputs
HM-7681RP - "Three State" Outputs

Preview

Features

- 60ns MAXIMUM ADDRESS ACCESS TIME.
- "THREE STATE" OR OPEN COLLECTOR OUTPUTS AND TWO CHIP ENABLE INPUTS.
- SIMPLE HIGH SPEED PROGRAMMING PROCEDURE - ONE PULSE/BIT. ASSURES FAST PROGRAMMING AND SUPERIOR RELIABILITY.
- FAST ACCESS TIME - GUARANTEED FOR WORST CASE N^2 SEQUENCING OVER COMMERCIAL AND MILITARY TEMPERATURE AND VOLTAGE RANGES.
- INDUSTRY'S HIGHEST PROGRAMMING YIELD.
- LATCHED OUTPUTS.
- A POWER DOWN INPUT ALLOWING 70% REDUCTION IN NOMINAL POWER DISSIPATION.

Description

The HM-7680RP/81RP are fully decoded high speed Schottky TTL 8192-Bit Field Programmable ROMs in a 1K words by 8 bit/word format with open collector (HM-7680RP) or "Three State" (HM-7681RP) outputs. These PROMs are available in a 24 pin DIP (ceramic or epoxy) and a 24 pin flatpack.

All bits are manufactured storing a logical "1" (positive logic) and can be selectively programmed for a logical "0" in any bit position.

Nichrome fuse technology is used on these and all other Harris Bipolar PROMs.

The HM-7680RP/81RP contains test rows and columns which are in addition to the storage array to assure high programmability and guarantee parametrics and A.C. performance. The fuses in these test rows and columns are blown prior to shipment.

There are two chip enable inputs on the HM-7680RP/81RP. $\overline{CE}_1$ and $\overline{CE}_2$ low enables the device.

There is also a power down input on this device. A powered down device has 70% reduction in nominal power dissipation if the outputs are not latched and 50% reduction in nominal power if the outputs are latched.

The HM-7680RP/81RP is operated in the Transparent Read Mode by holding the the strobe input high and the $\overline{PD}$ input high throughout the read operation. This is the normal read mode where the two chip enables and the power down inputs will control the outputs.

In Latched Read Mode, bringing the strobe input low will latch the outputs and the chip enable inputs. However, the power down input is independent of the latch function and can be changed while in the latched mode. If the device is disabled when the strobe input goes low, the outputs will be latched in the high impedance state. If the device is in the latched mode, the strobe input must be brought high to allow the outputs to respond to new address or chip enable conditions.

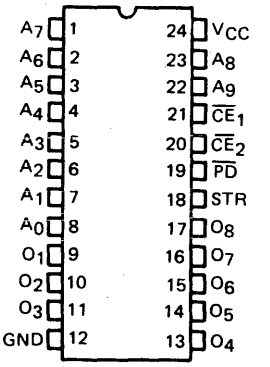
The following is a summary of the functional dependencies of the operating modes:

1. Chip enabled, transparent, powered up - normal mode where the power down input is effectively a chip enable with the I_{CC} reduction function.
2. Chip enabled, latched, power up - this is normal latched mode where the outputs remain latched regardless of address and chip enable switching.
3. Chip enabled, latched, power down - this is the powered down latched mode where the output data remains latched while power is reduced to 50% of its nominal value. If the latch strobe changes state while in this mode, the outputs will go to a high impedance state and power will reduce to 30% of nominal power. This is because the $\overline{PD}$ input becomes an effective chip enable in the Transparent Mode.
4. Chip disabled, transparent, power down - this is the normal powered down mode where the outputs are in a high impedance state and the power is reduced to 30% of the nominal power.

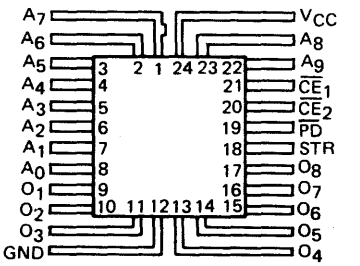
On the following page is a table to clarify the operational interdependencies.

Pinouts

TOP VIEW—DIP



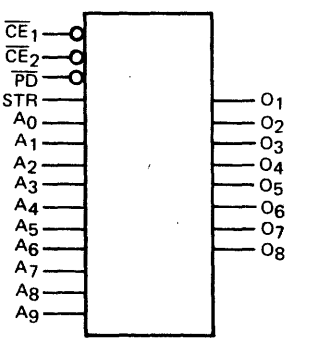
TOP VIEW—FLATPACK



PIN NAMES

A_0-A_9	Address Inputs
O_1-O_8	Data Outputs
$\overline{CE}_1$, $\overline{CE}_2$	Chip Enable Inputs
$\overline{PD}$	Power Down Input
STR	Strobe Input

Logic Symbol



"SEE PAGES 1409-1415 FOR PACKAGE SELECTION GUIDE"

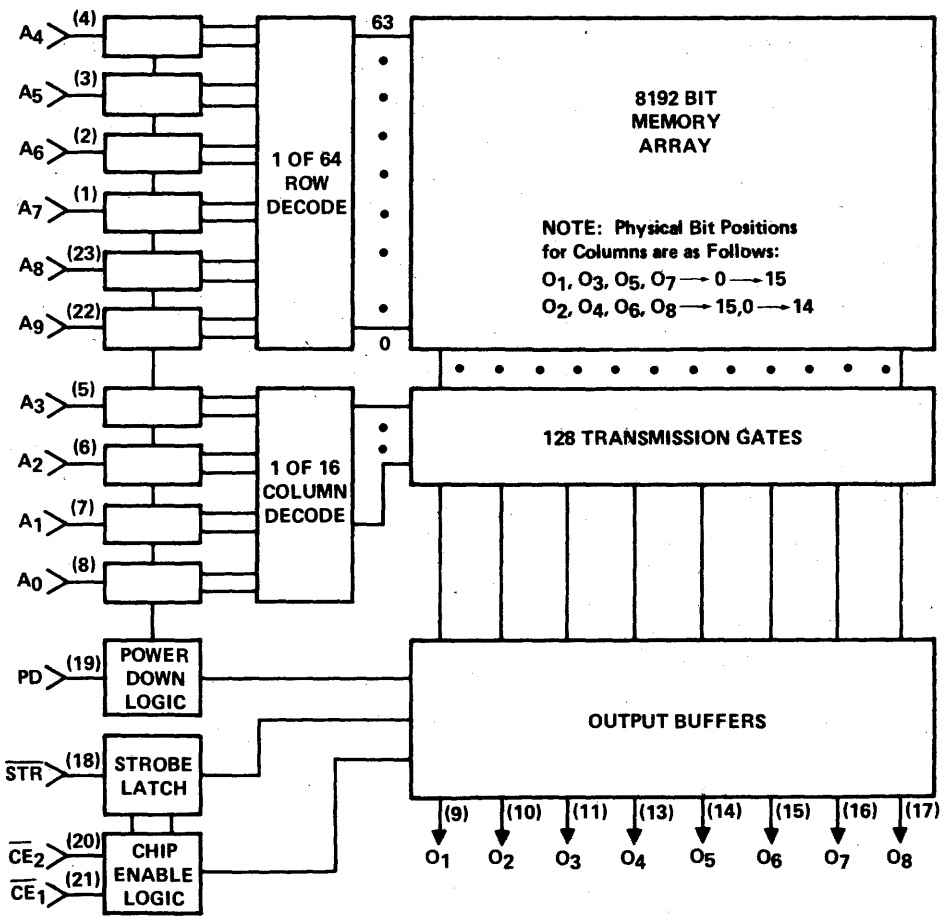
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TRUTH TABLE for HM-7680RP/81RP

$\overline{PD}$	STR	$\overline{CE}_2$	$\overline{CE}_1$	OUTPUTS	POWER
0	0	0	0	Latched Data	50%
0	0	0	1	Latched "Three State"	50%
0	0	1	0	Latched "Three State"	50%
0	0	1	1	Latched "Three State"	50%
0	1	0	0	Unlatched "Three State"	30%
0	1	0	1	Unlatched "Three State"	30%
0	1	1	0	Unlatched "Three State"	30%
0	1	1	1	Unlatched "Three State"	30%
1	0	0	0	Latched Data	100%
1	0	0	1	Latched "Three State"	100%
1	0	1	0	Latched "Three State"	100%
1	0	1	1	Latched "Three State"	100%
1	1	0	0	Unlatched Data	100%
1	1	0	1	Unlatched "Three State"	100%
1	1	1	0	Unlatched "Three State"	100%
1	1	1	1	Unlatched "Three State"	100%

Assume that the sequence of transitions is: 1) Chip Enables, 2) STR, 3) $\overline{PD}$ and the initial state is Unlatched Data.

Functional Diagram



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ABSOLUTE MAXIMUM RATINGS

Output or Supply Voltage (Operating)	-0.3 to +7.0V	Storage Temperature	-65°C to +150°C
Address/Enable Input Voltage	5.5V	Operating Temperature (Ambient)	-55°C to +125°C
Address/Enable Input Current	-20mA	Maximum Junction Temperature	+175°C
Output Sink Current	100mA		

CAUTION: Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied. (While programming, follow the programming specifications.)

D.C. ELECTRICAL CHARACTERISTICS (Operating)

HM-7680RP/81RP-5 (V_{CC} = 5.0V ± 5%, T_A = 0°C to +75°C)
HM-7680RP/81RP-2 (V_{CC} = 5.0V ± 10%, T_A = -55°C to +125°C)
Typical measurements are at T_A = 25°C, V_{CC} = +5V

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
I_{IH}	Address/Enable "1"	–	–	+40	µA	V_{IH} = V_{CC} Max.
I_{IL}	Input Current "0"	–	-50.0	-250	µA	V_{IL} = 0.45V
V_{IH}	Input Threshold "1"	2.0	1.5	–	V	V_{CC} = V_{CC} Min.
V_{IL}	Voltage "0"	–	1.5	0.8	V	V_{CC} = V_{CC} Max.
V_{OH}	Output "1"	2.4*	3.2*	–	V	I_{OH} = -2.0mA, V_{CC} = V_{CC} Min.
V_{OL}	Voltage "0"	–	0.35	0.50	V	I_{OL} = +16mA, V_{CC} = V_{CC} Min.
I_{OHE}	Output Disable "1"	–	–	+40	µA	V_{OH}, V_{CC} = V_{CC} Max.
I_{OLE}	Current "0"	–	–	-40*	µA	V_{OL} = 0.3V, V_{CC} = V_{CC} Max.
V_{CL}	Input Clamp Voltage	–	–	-1.2	V	I_{IN} = -18mA
I_{OS}	Output Short Circuit Current	-15*	-2.5	-100*	mA	V_{OUT} = 0.0V, One Output at a Time for a Max. of 1 Second
I_{CC}	Power Supply Current	–	120	170	mA	V_{CC} = V_{CC} Max., All Inputs Grounded.

NOTE: Positive current defined as into device terminals.
*"Three State" only

A.C. ELECTRICAL CHARACTERISTICS (Operating)

		HM-7680RP/81RP-5 5V ± 5% 0°C to +75°C			HM-7680RP/81RP-2 5V ± 10% -55°C to +125°C				
SYMBOL	PARAMETER	MIN	TYP	MAX	MIN	TYP	MAX	UNITS	TEST COND.
T_{AA}	Address Access Time	–	45	60	–	–	80	ns	Latched or
T_{DA}	Chip Disable Access Time	–	30	40	–	–	50	ns	Transparent
T_{EA}	Chip Enable Access Time	–	30	40	–	–	50	ns	
T_{PU}	Chip Power-Up Access Time	–	80	100	–	–	150	ns	
T_{ADH}	Address Hold Time	0	-10	–	0	-10	–	ns	Latched Only
T_{CDH}	Chip Enable Hold Time	10	0	–	10	0	–	ns	
T_{SW}	Strobe Pulse Width	30	10	–	40	10	–	ns	
T_{SL}	Strobe Latch Time	60	40	–	80	40	–	ns	
T_{DL}	Strobe Delatch Time	–	–	40	–	–	50	ns	
T_{CDS}	Chip Enable Set-Up Time	40	–	–	50	–	–	ns	

A.C. limits guaranteed for worst case N^2 sequencing.

CAPACITANCE: T_A = 25°C

SYMBOL	PARAMETER	MAXIMUM	UNITS	TEST CONDITIONS
CINA, CINCE	Input Capacitance	8	pF	V_{CC} = 5V, V_{IN} = 2.0V, f = 1MHz
COUT	Output Capacitance	10	pF	V_{CC} = 5V, V_{OUT} = 2.0V, f = 1MHz

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PRODUCTS DIVISION
A DIVISION OF HARRIS CORPORATION

HM-7683

1K x 8 PROM

Active Pull-up Outputs

Preliminary

Features

- 60ns MAXIMUM ADDRESS ACCESS TIME
- SIMPLE, HIGH SPEED PROGRAMMING PROCEDURE - ONE PULSE/BIT ASSURES FAST PROGRAMMING AND SUPERIOR RELIABILITY.
- FAST ACCESS TIME - GUARANTEED FOR WORST CASE N^2 SEQUENCING OVER COMMERCIAL AND MILITARY TEMPERATURE AND VOLTAGE RANGES.
- INDUSTRY'S HIGHEST PROGRAMMING YIELD
- LOW PIN COUNT FOR MAXIMUM DENSITY

Description

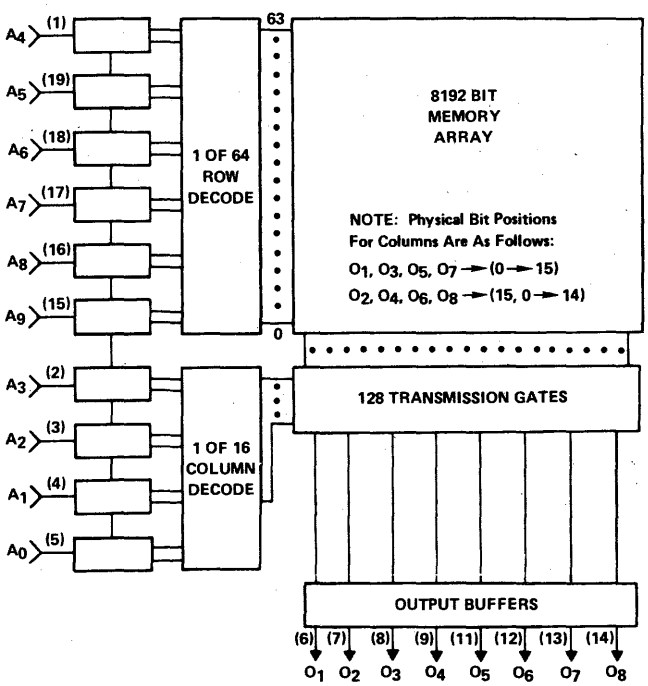
The HM-7683 is a fully decoded high speed Schottky TTL 8192-Bit Field Programmable ROM in a 1K word by 8 bit/word format and is available in a 20 pin DIP (ceramic or epoxy) and a 20 pin flatpack.

All bits are manufactured storing a logical "1" (positive logic) and can be selectively programmed for a logical "0" in any bit position.

Nichrome fuse technology is used on this and all other Harris Bipolar PROMs.

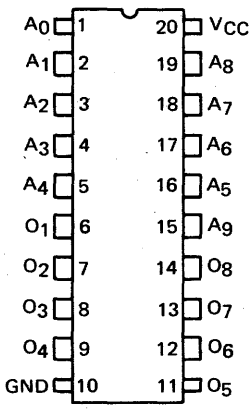
The HM-7683 contains test rows and columns which are in addition to the storage array to assure high programmability and guarantee parameterics and A.C. performance. The fuses in these test rows and columns are blown prior to shipment.

Functional Diagram

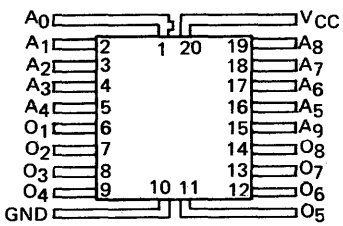


Pinouts

TOP VIEW - DIP



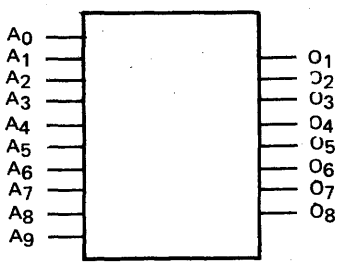
TOP VIEW - FLATPACK



PIN NAMES

$A_0 - A_9$	Address Outputs
$O_1 - O_8$	Data Outputs

Logic Symbol



"SEE PAGES 1409-1415 FOR PACKAGE SELECTION GUIDE"

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ABSOLUTE MAXIMUM RATINGS

Output or Supply Voltage (Operating)	-0.3 to +7.0V	Storage Temperature	-65°C to +150°C
Address/Enable Input Voltage	5.5V	Operating Temperature (Ambient)	-55°C to +125°C
Address/Enable Input Current	-20mA	Maximum Junction Temperature	+175°C
Output Sink Current	100mA		

CAUTION: Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied. (While programming, follow the programming specifications.)

D.C. ELECTRICAL CHARACTERISTICS (Operating)

HM-7683-5 (V_{CC} = 5.0V ± 5%, T_A = 0° to +75°C)
HM-7683-2 (V_{CC} = 5.0V ± 10%, T_A = -55°C to +125°C)
Typical Measurements are at T_A = 25°C, V_{CC} = +5V

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
I_{IH}	Address Input "1"	–	–	+40	μA	V_{IH} = V_{CC} Max.
I_{IL}	Current "0"	–	-50.0	-250	μA	V_{IL} = 0.45V
V_{IH}	Input Threshold "1"	2.0	1.5	–	V	V_{CC} = V_{CC} Min.
V_{IL}	Voltage "0"	–	1.5	0.8	V	V_{CC} = V_{CC} Max.
V_{OH}	Output "1"	2.4	3.2	–	V	I_{OH} = -2.0mA, V_{CC} = V_{CC} Min.
V_{OL}	Voltage "0"	–	0.35	0.50	V	I_{OL} = +16mA, V_{CC} = V_{CC} Min.
V_{CL}	Input Clamp Voltage	–	–	-1.2	V	I_{IN} = -18mA
I_{OS}	Output Short Circuit Current	-15	–	-100	mA	V_{OUT} = 0.0V, One Output at a Time for a Max. of 1 Second
I_{CC}	Power Supply Current	–	130	170	mA	V_{CC} = V_{CC} Max., All Inputs Grounded.

NOTE: Positive current defined as into device terminals.

A.C. ELECTRICAL CHARACTERISTICS (Operating)

		HM-7683-5 5V ± 5% 0°C to +75°C			HM-7683-2 5V ± 10% -55°C to +125°C			
SYMBOL	PARAMETER	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
T_{AA}	Address Access Time	–	45	60	–	–	80	ns

A.C. limits guaranteed for worst case N^2 sequencing.

CAPACITANCE: T_A = 25°C

SYMBOL	PARAMETER	MAXIMUM	UNITS	TEST CONDITIONS
C_{INA}	Input Capacitance	8	pF	V_{CC} = 5V, V_{IN} = 2.0V, f = 1MHz
C_{OUT}	Output Capacitance	10	pF	V_{CC} = 5V, V_{OUT} = 2.0V, f = 1MHz

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HARRIS
SEMICONDUCTOR
PRODUCTS DIVISION
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HM-7684/85

2K x 4 PROM

HM-7684 - Open Collector Outputs
HM-7685 - "Three State" Outputs

Preliminary

Features

- 60ns MAXIMUM ADDRESS ACCESS TIME
- "THREE STATE" OR OPEN COLLECTOR OUTPUTS AND A CHIP ENABLE INPUT
- SIMPLE HIGH SPEED PROGRAMMING PROCEDURE - ONE PULSE/BIT ASSURES FAST PROGRAMMING AND SUPERIOR RELIABILITY
- FAST ACCESS TIME - GUARANTEED FOR WORST CASE N^2 SEQUENCING OVER COMMERCIAL AND MILITARY TEMPERATURE AND VOLTAGE RANGES
- INDUSTRY'S HIGHEST PROGRAMMING YIELD

Description

The HM-7684/85 are a fully decoded high speed Schottky TTL 8192-Bit Field Programmable ROM in a 2K word by a 4 bit/word format with open collector (HM-7684) or "Three State" (HM-7685) outputs. These PROMs are available in an 18 pin DIP (ceramic or epoxy) and an 18 pin flatpack.

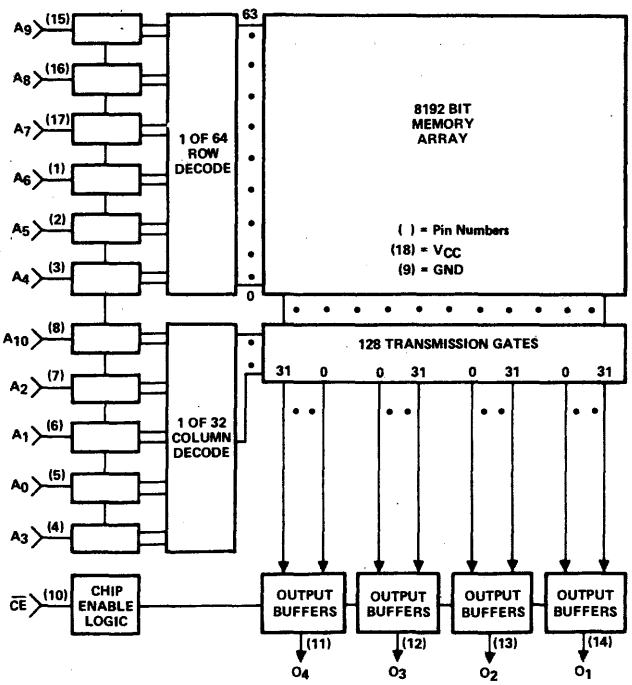
All bits are manufactured storing a logical "1"(positive logic) and can be selectively programmed for a logical "0" in any bit position.

Nichrome fuse technology is used on this and all other Harris Bipolar PROMs.

The HM-7684/85 contains test rows and columns which are in addition to the storage array to assure high programmability and guarantee parametrics and A.C. performance. The fuses in these test rows and columns are blown prior to shipment.

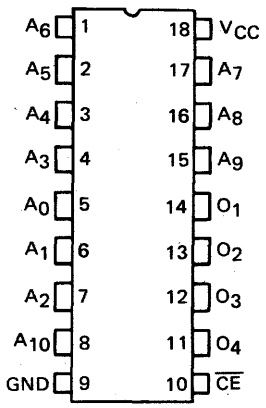
There is a chip enable on the HM-7684/85. $\overline{CE}$ low enables the chip.

Functional Diagram

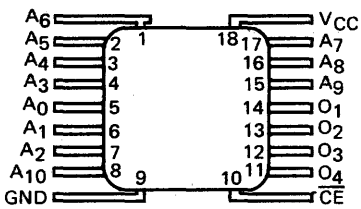


Pinouts

TOP VIEW - DIP



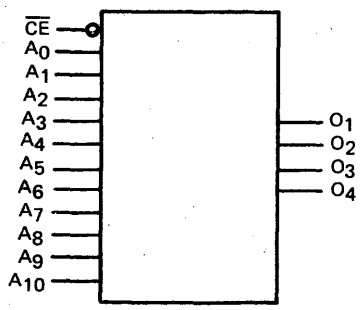
TOP VIEW - FLATPACK



PIN NAMES

$A_0 - A_{10}$	Address Inputs
$O_1 - O_4$	Data Outputs
$\overline{CE}$	Chip Enable Input

Logic Symbol



"SEE PAGES 1409-1415 FOR PACKAGE SELECTION GUIDE"

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ABSOLUTE MAXIMUM RATINGS

Output or Supply Voltage (Operating)	-0.3 to +7.0V	Storage Temperature	-65°C to +150°C
Address/Enable Input Voltage	5.5V	Operating Temperature (Ambient)	-55°C to +125°C
Address/Enable Input Current	-20mA	Maximum Junction Temperature	+175°C
Output Sink Current	100mA		

CAUTION: Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied. (While programming, follow the programming specifications.)

D.C. ELECTRICAL CHARACTERISTICS (Operating)

HM-7684/85-5 (V_{CC} = 5.0V ± 5%, T_A = 0°C to +75°C)
HM-7684/85-2 (V_{CC} = 5.0V ± 10%, T_A = -55°C to +125°C)
Typical measurements are at T_A = 25°C, V_{CC} = +5V

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
I_{IH} I_{IL}	Address/Enable "1" Input Current "0"	– –	– -50.0	+40 -250	µA µA	V_{IH} = V_{CC} Max. V_{IL} = 0.45V
V_{IH} V_{IL}	Input Threshold "1" Voltage "0"	2.0 –	1.5 1.5	– 0.8	V V	V_{CC} = V_{CC} Min. V_{CC} = V_{CC} Max.
V_{OH} V_{OL}	Output "1" Voltage "0"	2.4* –	3.2* 0.35	– 0.50	V V	I_{OH} = -2.0mA, V_{CC} = V_{CC} Min. I_{OL} = +16mA, V_{CC} = V_{CC} Min.
I_{OHE} I_{OLE}	Output Disable "1" Current "0"	– –	– –	+40 -40*	µA µA	V_{OH}, V_{CC} = V_{CC} Max. V_{OL} = 0.3V, V_{CC} = V_{CC} Max.
V_{CL}	Input Clamp Voltage	–	–	-1.2	V	I_{IN} = -18mA
I_{OS}	Output Short Circuit Current	-15*	–	-100*	mA	V_{OUT} = 0.0V, One Output at a Time for a Max. of 1 Second
I_{CC}	Power Supply Current	–	120	170	mA	V_{CC} = V_{CC} Max., All Inputs Grounded.

NOTE: Positive current defined as into device terminals.
*"Three State" only

A.C. ELECTRICAL CHARACTERISTICS (Operating)

		HM-7684/85-5 5V ± 5% 0°C to +75°C			HM-7684/85-2 5V ± 10% -55°C to +125°C			
SYMBOL	PARAMETER	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
T_{AA}	Address Access Time	–	45	60	–	–	80	ns
T_{EA}	Chip Enable Access Time	–	30	40	–	–	50	ns

A.C. limits guaranteed for worst case N^2 sequencing.

CAPACITANCE: T_A = 25°C

SYMBOL	PARAMETER	MAXIMUM	UNITS	TEST CONDITIONS
C_{INA}, C_{INCE}	Input Capacitance	8	pF	V_{CC} = 5V, V_{IN} = 2.0V, f = 1MHz
C_{OUT}	Output Capacitance	10	pF	V_{CC} = 5V, V_{OUT} = 2.0V, f = 1MHz

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HARRIS SEMICONDUCTOR PRODUCTS DIVISION
A DIVISION OF HARRIS CORPORATION

HM-7684P/85P

2K x 4 PROM

HM-7684P - Open Collector Outputs
HM-7685P - "Three State" Outputs

Preview

Features

- 60ns MAXIMUM ADDRESS ACCESS TIME
- "THREE STATE" OR OPEN COLLECTOR OUTPUTS AND A POWER DOWN INPUT
- SIMPLE HIGH SPEED PROGRAMMING PROCEDURE - ONE PULSE/BIT ASSURES FAST PROGRAMMING AND SUPERIOR RELIABILITY
- FAST ACCESS TIME - GUARANTEED FOR WORST CASE N^2 SEQUENCING OVER COMMERCIAL AND MILITARY TEMP. AND VOLT. RANGES
- INDUSTRY'S HIGHEST PROGRAMMING YIELD

Description

The HM-7684P/85P are fully decoded high speed Schottky TTL 8192-Bit Field Programmable ROMs in a 2K words by 4 bit/word format with open collector (HM-7684P) or "Three State" (HM-7685P) outputs. These PROMs are available in an 18 pin DIP (ceramic or epoxy) and an 18 pin flatpack.

All bits are manufactured storing a logical "1" (positive logic) and can be selectively programmed for a logical "0" in any bit position.

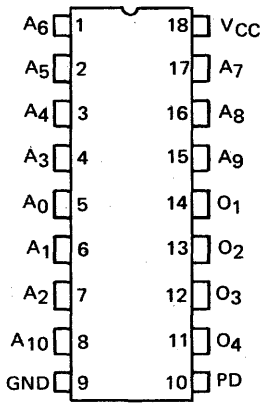
Nichrome fuse technology is used on these and all other Harris Bipolar PROMs.

The HM-7684P/85P contains test rows and columns which are in addition to the storage array to assure high programmability and guarantee parametrics and A.C. performance. The fuses in these test rows and columns are blown prior to shipment.

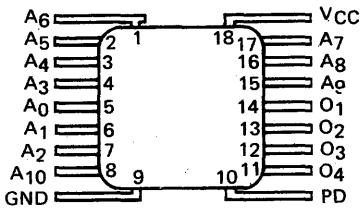
There is a power down input on the HM-7684P/85P which is similar to a chip enable. The chip is enabled or disabled using the power down input where a disabled chip dissipates 30% of nominal power and the outputs go to a high impedance state. The chip is powered up (enabled) when PD_1 is low.

Pinouts

TOP VIEW - DIP



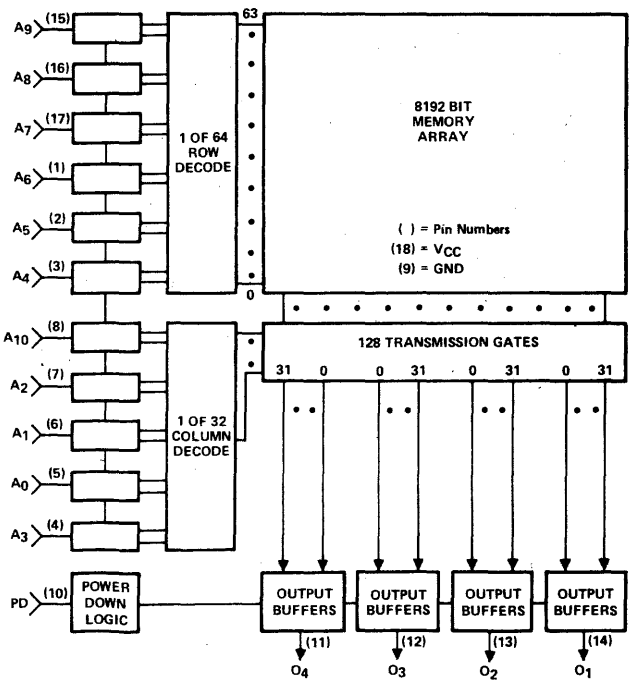
TOP VIEW - FLATPACK



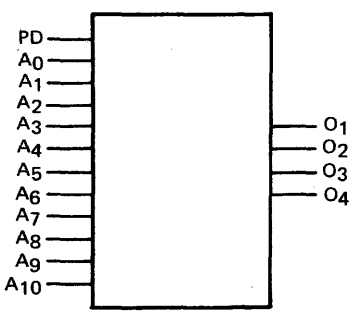
PIN NAMES

$A_0 - A_{10}$	Address Inputs
$O_1 - O_4$	Data Outputs
PD	Power Down Input

Functional Diagram



Logic Symbol



"SEE PAGES 1409-1415 FOR PACKAGE SELECTION GUIDE"

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ABSOLUTE MAXIMUM RATINGS

Output or Supply Voltage (Operating)	-0.3 to +7.0V	Storage Temperature	-65°C to +150°C
Address/Enable Input Voltage	5.5V	Operating Temperature (Ambient)	-55°C to +125°C
Address/Enable Input Current	-20mA	Maximum Junction Temperature	+175°C
Output Sink Current	100mA		

CAUTION: Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied. (While programming, follow the programming specifications.)

D.C. ELECTRICAL CHARACTERISTICS (Operating)

HM-7684P/85P-5 (V_{CC} = 5.0V ± 5%, T_A = 0°C to +75°C)
HM-7684P/85P-2 (V_{CC} 5.0V ± 10%, T_A = -55°C to +125°C)
Typical measurements are at T_A = 25°C, V_{CC} = +5V

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
I_{IH} I_{IL}	Address/Enable "1" Input Current "0"	– –	– -50.0	+40 -250	µA µA	V_{IH} = V_{CC} Max. V_{IL} = 0.45V
V_{IH} V_{IL}	Input Threshold "1" Voltage "0"	2.0 –	1.5 1.5	– 0.8	V V	V_{CC} = V_{CC} Min. V_{CC} = V_{CC} Max.
V_{OH} V_{OL}	Output "1" Voltage "0"	2.4 * –	3.2* 0.35	– 0.50	V V	I_{OH} = -2.0mA, V_{CC} = V_{CC} Min. I_{OL} = +16mA, V_{CC} = V_{CC} Min.
I_{OHE} I_{OLE}	Output Disable "1" Current "0"	– –	– –	+40 -40 *	µA µA	V_{OH}, V_{CC} = V_{CC} Max. V_{OL} = 0.3V, V_{CC} = V_{CC} Max.
V_{CL}	Input Clamp Voltage	–	–	-1.2	V	I_{IN} = -18mA
I_{OS}	Output Short Circuit Current	-15*	–	-100*	mA	V_{OUT} = 0.0V, One Output at a Time for a Max. of 1 Second
I_{CC}	Power Supply Current	–	120	170	mA	V_{CC} = V_{CC} Max., All Inputs Grounded.

NOTE: Positive current defined as into device terminals.
*"Three State" only

A.C. ELECTRICAL CHARACTERISTICS (Operating)

		HM-7684P/85P-5 5V ± 5% 0°C to +75°C			HM-7684P/85P-2 5V ± 10% -55°C to +125°C			
SYMBOL	PARAMETER	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
T_{AA}	Address Access Time	-	45	60	-	-	80	ns
T_{PD}	Chip Power Down Access Time	-	30	40	-	-	50	ns
T_{PU}	Chip Power-Up Access Time	-	80	100	-	-	150	ns

A.C. limits guaranteed for worst case N^2 sequencing.

CAPACITANCE: T_A = 25°C

SYMBOL	PARAMETER	MAXIMUM	UNITS	TEST CONDITIONS
C_{INA}, C_{INCE}	Input Capacitance	8	pF	V_{CC} = 5V, V_{IN} = 2.0V, f = 1MHz
C_{OUT}	Output Capacitance	10	pF	V_{CC} = 5V, V_{OUT} = 2.0V, f = 1MHz

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Preview

HM-7686/87

2K x 4 PROM

HM-7686 - Open Collector Outputs
HM-7687 - "Three State" Outputs

Features

- 60ns MAXIMUM ADDRESS ACCESS TIME.
- "THREE STATE" OR OPEN COLLECTOR OUTPUTS AND THREE CHIP ENABLE INPUTS.
- SIMPLE HIGH SPEED PROGRAMMING PROCEDURE - ONE PULSE/BIT. ASSURES FAST PROGRAMMING AND SUPERIOR RELIABILITY.
- FAST ACCESS TIME - GUARANTEED FOR WORST CASE N^2 SEQUENCING OVER COMMERCIAL AND MILITARY TEMPERATURE AND VOLTAGE RANGES.
- INDUSTRY'S HIGHEST PROGRAMMING YIELD.

Description

The HM-7686/87 are fully decoded high speed Schottky TTL 8192-Bit Field Programmable Roms in a 2K word by 4 bit/word format with open collector (HM-7686) or "Three State" (HM-7687) outputs. These PROMs are available in a 20 pin DIP (ceramic or epoxy) and a 20 pin flatpack.

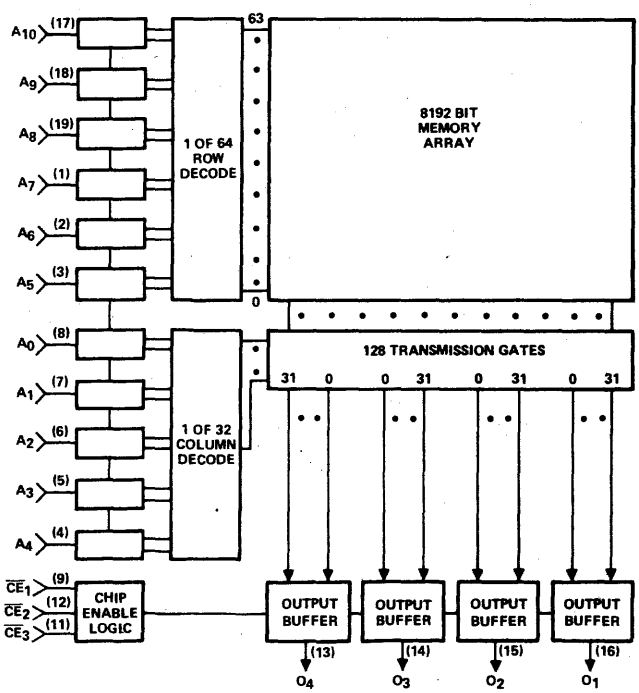
All bits are manufactured storing a logical "1" (positive logic) and can be selectively programmed for a logical "0" in any bit position.

Nichrome fuse technology is used on these and all other Harris Bipolar PROMs.

The HM-7686/87 contains test rows and columns which are in addition to the storage array to assure high programmability and guarantee parametrics and A.C. performance. The fuses in test rows and columns are blown prior to shipment.

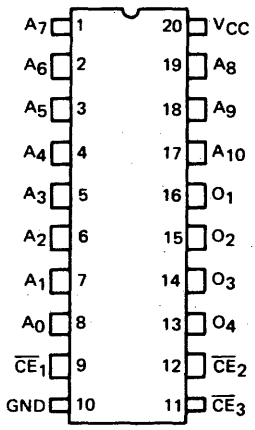
There are three chip enable inputs on the HM-7686/87. $\overline{CE}_1$, $\overline{CE}_2$, and $\overline{CE}_3$ low enables the chip.

Functional Diagram

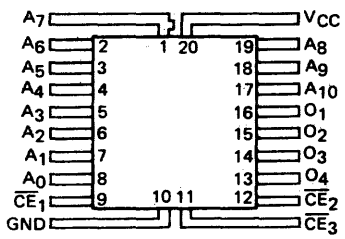


Pinouts

TOP VIEW – DIP



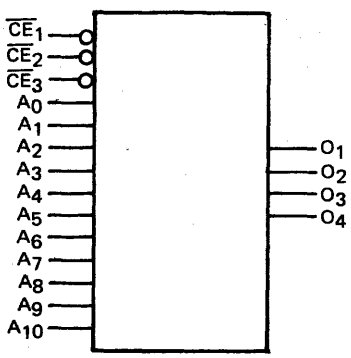
TOP VIEW – FLATPACK



PIN NAMES

$A_0 - A_{10}$	Address Inputs
$O_1 - O_4$	Data Outputs
$\overline{CE}_1, \overline{CE}_2, \overline{CE}_3$	Chip Enable Inputs

Logic Symbol



"SEE PAGES 1409-1415 FOR PACKAGE SELECTION GUIDE"

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ABSOLUTE MAXIMUM RATINGS

Output or Supply Voltage (Operating)	-0.3 to +7.0V	Storage Temperature	-65°C to +150°C
Address/Enable Input Voltage	5.5V	Operating Temperature (Ambient)	-55°C to +125°C
Address/Enable Input Current	-20mA	Maximum Junction Temperature	+175°C
Output Sink Current	100mA		

CAUTION: Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied. (While programming, follow the programming specifications.)

D.C. ELECTRICAL CHARACTERISTICS (Operating)

HM-7686/87-5 (V_{CC} = 5.0V ± 5%, T_A = 0°C to +75°C)
HM-7686/87-2 (V_{CC} = 5.0V ± 10%, T_A = -55°C to +125°C)
Typical measurements are at T_A = 25°C, V_{CC} = +5V

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
I_{IH}	Address/Enable "1"	–	–	+40	μA	V_{IH} = V_{CC} Max.
I_{IL}	Input Current "0"	–	-50.0	-250	μA	V_{IL} = 0.45V
V_{IH}	Input Threshold "1"	2.0	1.5	–	V	V_{CC} = V_{CC} Min.
V_{IL}	Voltage "0"	–	1.5	0.8	V	V_{CC} = V_{CC} Max.
V_{OH}	Output "1"	2.4*	3.2*	–	V	I_{OH} = -2.0mA, V_{CC} = V_{CC} Min.
V_{OL}	Voltage "0"	–	0.35	0.50	V	I_{OL} = +16mA, V_{CC} = V_{CC} Min.
I_{OHE}	Output Disable "1"	–	–	+40	μA	V_{OH}, V_{CC} = V_{CC} Max.
I_{OLE}	Current "0"	–	–	-40*	μA	V_{OL} = 0.3V, V_{CC} = V_{CC} Max.
V_{CL}	Input Clamp Voltage	–	–	-1.2	V	I_{IN} = -18mA
I_{OS}	Output Short Circuit Current	-15*	–	-100*	mA	V_{OUT} = 0.0V, One Output at a Time for a Max. of 1 Second
I_{CC}	Power Supply Current	–	120	170	mA	V_{CC} = V_{CC} Max., All Inputs Grounded.

NOTE: Positive current defined as into device terminals.
*"Three State" only

A.C. ELECTRICAL CHARACTERISTICS (Operating)

		HM-7686/87-5 5V ± 5% 0°C to +75°C			HM-7686/87-2 5V ± 10% -55°C to +125°C			
SYMBOL	PARAMETER	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
T_{AA}	Address Access Time	–	45	60	–	–	80	ns
T_{EA}	Chip Enable Access Time	–	30	40	–	–	50	ns

A.C. limits guaranteed for worst case N^2 sequencing.

CAPACITANCE: T_A = 25°C

SYMBOL	PARAMETER	MAXIMUM	UNITS	TEST CONDITIONS
C_{INA}, C_{INCE}	Input Capacitance	8	pF	V_{CC} = 5V, V_{IN} = 2.0V, f = 1MHz
C_{OUT}	Output Capacitance	10	pF	V_{CC} = 5V, V_{OUT} = 2.0V, f = 1MHz

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Preview

HM-7686R/87R

2K x 4 PROM

HM-7686R - Open Collector Outputs
HM-7687R - "Three State" Outputs

Features

- 60ns MAXIMUM ADDRESS ACCESS TIME
- "THREE STATE" OR OPEN COLLECTOR OUTPUTS AND TWO CHIP ENABLE INPUTS
- SIMPLE HIGH SPEED PROGRAMMING PROCEDURE - ONE PULSE/BIT ASSURES FAST PROGRAMMING AND SUPERIOR RELIABILITY
- FAST ACCESS TIME - GUARANTEED FOR WORST CASE N^2 SEQUENCING OVER COMMERCIAL AND MILITARY TEMPERATURE AND VOLTAGE RANGES
- INDUSTRY'S HIGHEST PROGRAMMING YIELD
- LATCHED OUTPUTS

Description

The HM-7686R/87R are fully decoded high speed Schottky TTL 8192-Bit Field Programmable ROMs in a 2K words by 4 bit/word format with open collector (HM-7686R) or "Three State" (HM-7687R) outputs. These PROMs are available in a 20 pin DIP (ceramic or epoxy) and 20 pin flatpack.

All bits are manufactured storing a logical "1" (positive logic) and can be selectively programmed for a logical "0" in any bit position.

Nichrome fuse technology is used on these and all other Harris Bipolar PROMs.

The HM-7686R/87R contains test rows and columns which are in addition to the storage array to assure high programmability and guarantee parametrics and A.C. performance. The fuses in these test rows and columns are blown prior to shipment.

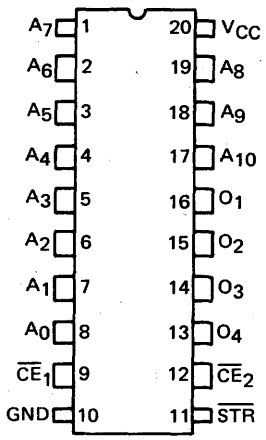
There are two chip enable inputs on the HM-7686R/87R. $\overline{CE}_1$, $\overline{CE}_2$ low enables the chip.

The HM-7686R/87R is operated in the Transparent Read Mode by holding the strobe input low throughout the read operation. This is the normal read mode where the two chip enable inputs will control the outputs.

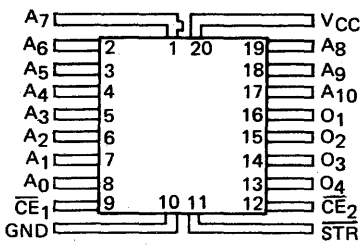
In Latched Read Mode, bringing the strobe input high will latch the outputs and chip enable inputs. If the device is disabled when the strobe input goes high, the outputs will be latched in the high impedance state. If the device is in the latched mode, the strobe input must be brought low to allow the outputs to respond to new address or chip enable conditions.

Pinouts

TOP VIEW-DIP



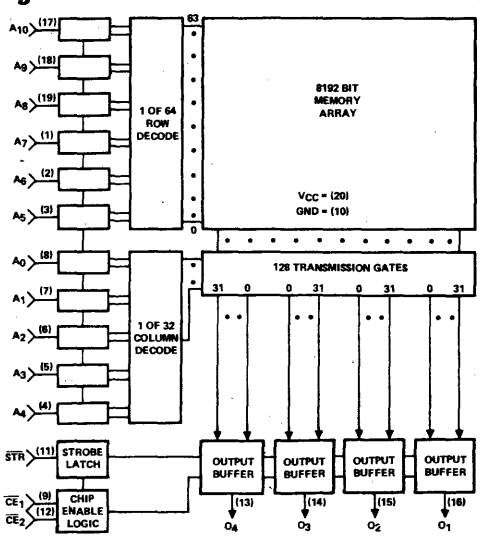
TOP VIEW-FLAT PACK



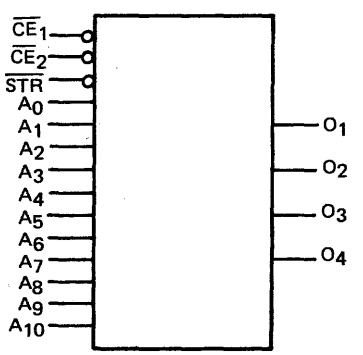
PIN NAMES

A_0-A_{10}	Address Inputs
O_1-O_4	Data Outputs
$\overline{CE}_1$, $\overline{CE}_2$	Chip Enable Inputs
$\overline{STR}$	Strobe Input

Functional Diagram



Logic Symbol



"SEE PAGES 1409-1415 FOR PACKAGE SELECTION GUIDE"

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ABSOLUTE MAXIMUM RATINGS

Output or Supply Voltage (Operating)	-0.3 to +7.0V	Storage Temperature	-65°C to +150°C
Address/Enable Input Voltage	5.5V	Operating Temperature (Ambient)	-55°C to +125°C
Address/Enable Input Current	-20mA	Maximum Junction Temperature	+175°C
Output Sink Current	100mA		

CAUTION: Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied. (While programming, follow the programming specifications.)

D.C. ELECTRICAL CHARACTERISTICS (Operating)

HM-7686R/87R-5 (V_{CC} = 5.0V ± 5%, T_A = 0°C to +75°C)
HM-7686R/87R-2 (V_{CC} = 5.0V ± 10%, T_A = -55°C to +125°C)
Typical measurements are at T_A = 25°C, V_{CC} = +5V

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
I_{IH}	Address/Enable "1"	–	–	+40	μA	V_{IH} = V_{CC} Max.
I_{IL}	Input Current "0"	–	-50.0	-250	μA	V_{IL} = 0.45V
V_{IH}	Input Threshold "1"	2.0	1.5	–	V	V_{CC} = V_{CC} Min.
V_{IL}	Voltage "0"	–	1.5	0.8	V	V_{CC} = V_{CC} Max.
V_{OH}	Output "1"	2.4 *	3.2*	–	V	I_{OH} = -2.0mA, V_{CC} = V_{CC} Min.
V_{OL}	Voltage "0"	–	0.35	0.50	V	I_{OL} = +16mA, V_{CC} = V_{CC} Min.
I_{OHE}	Output Disable "1"	–	–	+40	μA	V_{OH}, V_{CC} = V_{CC} Max.
I_{OLE}	Current "0"	–	–	-40 *	μA	V_{OL} = 0.3V, V_{CC} = V_{CC} Max.
V_{CL}	Input Clamp Voltage	–	–	-1.2	V	I_{IN} = -18mA
I_{OS}	Output Short Circuit Current	-15*	-2.5	-100*	mA	V_{OUT} = 0.0V, One Output at a Time for a Max. of 1 Second
I_{CC}	Power Supply Current	–	120	170	mA	V_{CC} = V_{CC} Max., All Inputs Grounded.

NOTE: Positive current defined as into device terminals.
*"Three State" only

A.C. ELECTRICAL CHARACTERISTICS (Operating)

		HM-7686R/87R-5 5V ± 5% 0°C to +75°C			HM-7686R/87R-2 5V ± 10% -55°C to +125°C				
SYMBOL	PARAMETER	MIN	TYP	MAX	MIN	TYP	MAX	UNITS	TEST CONDIT.
T_{AA}	Address Access Time	–	45	60	–	–	80	ns	Latched or
T_{EA}	Chip Enable Access Time	–	30	40	–	–	50	ns	Transparent
T_{ADH}	Address Hold Time	0	-10	–	0	-10	–	ns	Latched Only
T_{CDH}	Chip Enable Hold Time	10	0	–	10	0	–	ns	
T_{SW}	Strobe Pulse Width	30	10	–	40	10	–	ns	
T_{SL}	Strobe Latch Time	60	40	–	80	40	–	ns	
T_{DL}	Strobe Delatch Time	–	–	40	–	–	50	ns	
T_{CDS}	Chip Enable Set-Up Time	40	–	–	50	–	–	ns	

A.C. limits guaranteed for worst case N^2 sequencing.

CAPACITANCE: T_A = 25°C

SYMBOL	PARAMETER	MAXIMUM	UNITS	TEST CONDITIONS
C_{INA}, C_{INCE}	Input Capacitance	8	pF	V_{CC} = 5V, V_{IN} = 2.0V, f = 1MHz
C_{OUT}	Output Capacitance	10	pF	V_{CC} = 5V, V_{OUT} = 2.0V, f = 1MHz

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Preview

HM-7686P/87P

2K x 4 PROM

HM-7686P - Open Collector Outputs
HM-7687P - "Three State" Outputs

Features

- 60ns MAXIMUM ADDRESS ACCESS TIME.
- "THREE STATE" OR OPEN COLLECTOR OUTPUTS AND THREE POWER DOWN INPUTS.
- SIMPLE HIGH SPEED PROGRAMMING PROCEDURE - ONE PULSE/BIT. ASSURES FAST PROGRAMMING AND SUPERIOR RELIABILITY.
- FAST ACCESS TIME - FOR WORST CASE N^2 SEQUENCING OVER COMMERCIAL AND MILITARY TEMPERATURE AND VOLTAGE RANGES.
- INDUSTRY'S HIGHEST PROGRAMMING YIELD.

Description

The HM-7686P/87P are fully decoded high speed Schottky TTL 8192-Bit Field Programmable ROMs in a 2K word by 4 bit/word format with open collector (HM-7686P) or "Three State" (HM-7687P) outputs. These PROMs are available in a 20 pin DIP (ceramic or epoxy) and a 20 pin flatpack.

All bits are manufactured storing a logical "1" (positive logic) and can be selectively programmed for a logical "0" in any bit position.

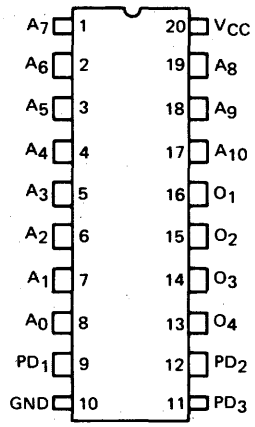
Nichrome fuse technology is used on these and all other Harris Bipolar PROMs.

The HM-7686P/87P contains test rows and columns which are in addition to the storage array to assure high programmability and guarantee parametrics and A.C. performance. The fuses in these test rows and columns are blown prior to shipment.

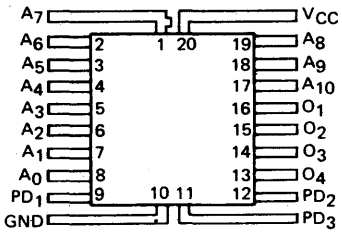
There are three power down inputs on the HM-7686P/87P which are similar to chip enables. The chip is enabled or disabled using the power down inputs where a disabled chip dissipates 30% of nominal power and the outputs go to a high impedance state. The chip is powered up (enabled) when PD_1, PD_2 and PD_3 are low.

Pinouts

TOP VIEW - DIP



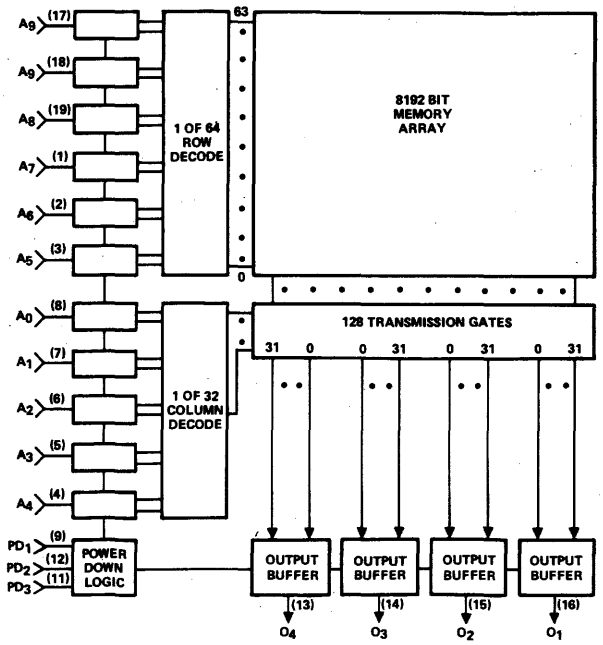
TOP VIEW - FLATPACK



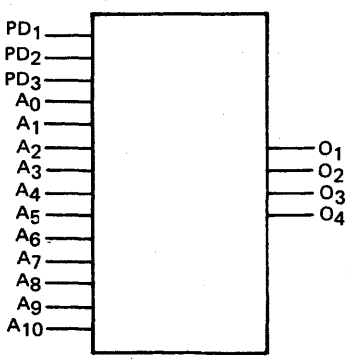
PIN NAMES

A_0 - A_{10}	Address Inputs
O_1 - O_4	Data Outputs
PD_1, PD_2, PD_3	Power Down Inputs

Functional Diagram



Logic Symbol



"SEE PAGES 1409-1415 FOR PACKAGE SELECTION GUIDE"

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ABSOLUTE MAXIMUM RATINGS

Output or Supply Voltage (Operating)	-0.3 to +7.0V	Storage Temperature	-65°C to +150°C
Address/Enable Input Voltage	5.5V	Operating Temperature (Ambient)	-55°C to +125°C
Address/Enable Input Current	-20mA	Maximum Junction Temperature	+175°C
Output Sink Current	100mA		

CAUTION: Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress only ratings and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied. (While programming, follow the programming specifications.)

D.C. ELECTRICAL CHARACTERISTICS (Operating)

HM-7686P/87P-5 (V_{CC} = 5.0V ± 5%, T_A = 0°C to +75°C)
HM-7686P/87P-2 (V_{CC} = 5.0V ± 10%, T_A = -55°C to +125°C)
Typical measurements are at T_A = 25°C, V_{CC} = +5V

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
I_{IH} I_{IL}	Address/Enable "1" Input Current "0"	– –	– -50.0	+40 -250	µA µA	V_{IH} = V_{CC} Max. V_{IL} = 0.45V
V_{IH} V_{IL}	Input Threshold "1" Voltage "0"	2.0 –	1.5 1.5	– 0.8	V V	V_{CC} = V_{CC} Min. V_{CC} = V_{CC} Max.
V_{OH} V_{OL}	Output "1" Voltage "0"	2.4* –	3.2* 0.35	– 0.50	V V	I_{OH} = -2.0mA, V_{CC} = V_{CC} Min. I_{OL} = +16mA, V_{CC} = V_{CC} Min.
I_{OHE} I_{OLE}	Output Disable "1" Current "0"	– –	– –	+40 -40*	µA µA	V_{OH}, V_{CC} = V_{CC} Max. V_{OL} = 0.3V, V_{CC} = V_{CC} Max.
V_{CL}	Input Clamp Voltage	–	–	-1.2	V	I_{IN} = -18mA
I_{OS}	Output Short Circuit Current	-15*	–	-100*	mA	V_{OUT} = 0.0V, One Output at a Time for a Max. of 1 Second
I_{CC}	Power Supply Current	–	120	170	mA	V_{CC} = V_{CC} Max., All Inputs Grounded.

NOTE: Positive current defined as into device terminals.
*"Three State" only

A.C. ELECTRICAL CHARACTERISTICS (Operating)

		HM-7686P/87P-5 5V ± 5% 0°C to +75°C			HM-7686P/87P-2 5V ± 10% -55°C to +125°C			
SYMBOL	PARAMETER	MIN	TYP	MAX	MIN	TYP	MAX	UNITS
T_{AA}	Address Access Time	-	45	60	-	-	80	ns
T_{PD}	Chip Power Down Access Time	-	30	40	-	-	50	ns
T_{PU}	Chip Power-Up Access Time	-	80	100	-	-	150	ns

A.C. limits guaranteed for worst case N^2 sequencing.

CAPACITANCE: T_A = 25°C

SYMBOL	PARAMETER	MAXIMUM	UNITS	TEST CONDITIONS
CINA, CINCE	Input Capacitance	8	pF	V_{CC} = 5V, V_{IN} = 2.0V, f = 1MHz
COUT	Output Capacitance	10	pF	V_{CC} = 5V, V_{OUT} = 2.0V, f = 1MHz

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Preview

HM-7686RP/87RP

2K x 4 PROM

HM-7686RP - Open Collector Outputs
HM-7687RP - "Three State" Outputs

Features

- 60ns MAXIMUM ADDRESS ACCESS TIME.
- "THREE STATE" OR OPEN COLLECTOR OUTPUTS AND A CHIP ENABLE INPUT.
- SIMPLE HIGH SPEED PROGRAMMING PROCEDURE - ONE PULSE/BIT. ASSURES FAST PROGRAMMING AND SUPERIOR RELIABILITY.
- FAST ACCESS TIME - GUARANTEED FOR WORST CASE N^2 SEQUENCING OVER COMMERCIAL AND MILITARY TEMPERATURE AND VOLTAGE RANGES.
- INDUSTRY'S HIGHEST PROGRAMMING YIELD.
- LATCHED OUTPUTS.
- A POWER DOWN INPUT ALLOWING 70% REDUCTION IN NOMINAL POWER DISSIPATION.

Description

The HM-7686RP/87RP are fully decoded high speed Schottky TTL 8192-Bit Field Programmable ROMs in a 2K words by 4 bit/word format with open collector (HM-7686RP) or "Three State" (HM-7687RP) outputs. These PROMs are available in a 20 pin DIP (ceramic or epoxy) and a 20 pin flatpack.

All bits are manufactured storing a logical "1" (positive logic) and can be selectively programmed for a logical "0" in any bit position.

Nichrome fuse technology is used on these and all other Harris Bipolar PROMs.

The HM-7686RP/87RP contains test rows and columns which are in addition to the storage array to assure high programmability and guarantee parametrics and A.C. performance. The fuses in these test rows and columns are blown prior to shipment.

There is a chip enable input on the HM-7686RP/87RP. $\overline{CE}$ low enables the device.

There is also a power down input on this device. A powered down device has 70% reduction in nominal power dissipation if the outputs are not latched and 50% reduction in nominal power if the outputs are latched.

The HM-7686RP/87RP is operated in the Transparent Read Mode by holding the the strobe input low and the PD input low throughout the read operation. This is the normal read mode where the chip enable and the power down input will control the outputs.

In Latched Read Mode, bringing the strobe input high will latch the outputs and the chip enable input. However, the power down input is independent of the latch function and can be changed while in the latched mode. If the device is disabled when the strobe input goes high, the outputs will be latched in the high impedance state. If the device is in the latched mode, the strobe input must be brought low to allow the outputs to respond to new address or chip enable conditions.

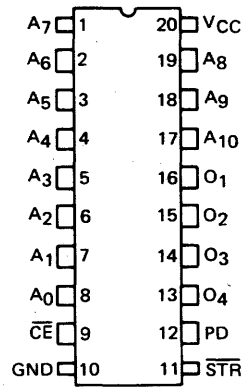
The following is a summary of the functional dependencies of the operating modes:

1. Chip enabled, transparent, powered up - normal mode where the power down input is effectively a chip enable with the I_{CC} reduction function.
2. Chip enabled, latched, power up - this is normal latched mode where the output remains latched regardless of address and chip enable switching.
3. Chip enabled, latched, power down - this is the powered down latched mode where the output data remains latched while power is reduced to 50% of its nominal value. If the latch strobe changes state while in this mode, the outputs will go to a high impedance state and power will reduce to 30% of nominal power. This is because the PD input becomes an effective chip enable in the Transparent Mode.
4. Chip disabled, transparent, power down - this is the normal powered down mode where the outputs are in a high impedance state and the power is reduced to 30% of the nominal power.

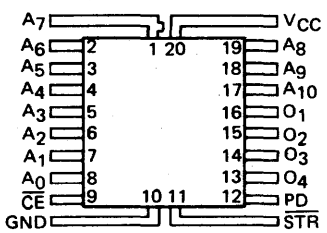
On the following page is a table to clarify the operational interdependencies.

Pinouts

TOP VIEW—DIP



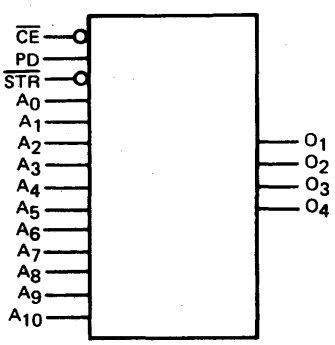
TOP VIEW—FLATPACK



PIN NAMES

A_0-A_{10}	Address Inputs
O_1-O_4	Data Ouputs
PD	Power Down Input
$\overline{STR}$	Strobe Input
$\overline{CE}$	Chip Enable Input

Logic Symbol



"SEE PAGES 1409-1415 FOR PACKAGE SELECTION GUIDE"

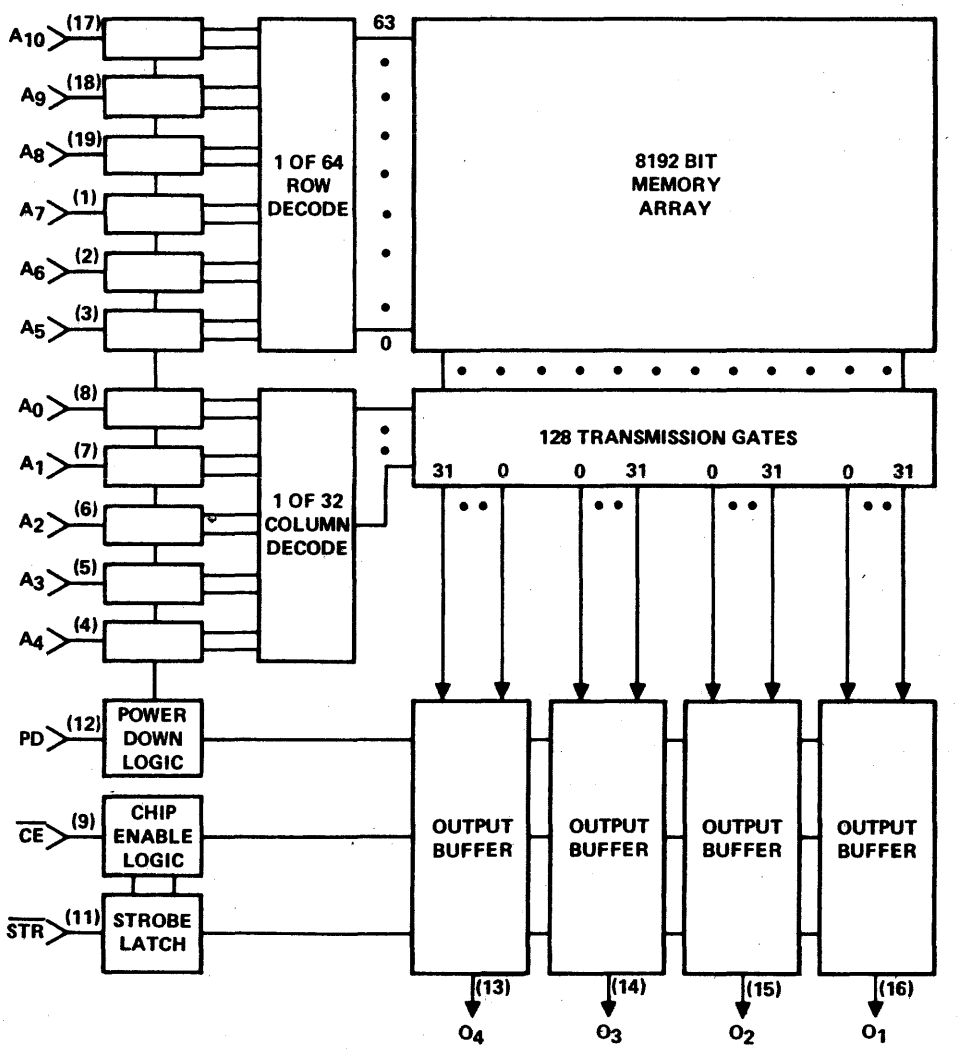
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TRUTH TABLE for HM-7686RP/87RP

PD	$\overline{STR}$	$\overline{CE}$	OUTPUTS	POWER
0	0	0	Unlatched Data	100%
0	0	1	Unlatched "Three State"	100%
0	1	0	Latched Data	100%
0	1	1	Latched "Three State"	100%
1	0	0	Unlatched "Three State"	30%
1	1	0	Latched Data	50%
1	1	1	Latched "Three State"	50%

Assume that the sequence of transitions is: 1) Chip Enable, 2) $\overline{STR}$, 3) PD, and the initial state is Unlatched Data.

Functional Diagram



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ABSOLUTE MAXIMUM RATINGS

Output or Supply Voltage (Operating)	-0.3 to +7.0V	Storage Temperature	-65°C to +150°C
Address/Enable Input Voltage	5.5V	Operating Temperature (Ambient)	-55°C to +125°C
Address/Enable Input Current	-20mA	Maximum Junction Temperature	+175°C
Output Sink Current	100mA		

CAUTION: Stresses above those listed under the "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and functional operation of the device at these or at any other conditions above those indicated in the operational sections of this specification is not implied. (While programming, follow the programming specifications.)

D.C. ELECTRICAL CHARACTERISTICS (Operating)

HM-7686RP/87RP-5 (V_{CC} = 5.0V + 5%, T_A = 0°C to +75°C)
HM-7686RP/87RP-2 (V_{CC} = 5.0V + 10%, T_A = -55°C to +125°C)
Typical measurements are at T_A = 25°C, V_{CC} = +5V

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
I_{IH} I_{IL}	Address/Enable "1" Input Current "0"	– –	– -50.0	+40 -250	µA µA	V_{IH} = V_{CC} Max. V_{IL} = 0.45V
V_{IH} V_{IL}	Input Threshold "1" Voltage "0"	2.0 –	1.5 1.5	– 0.8	V V	V_{CC} = V_{CC} Min. V_{CC} = V_{CC} Max.
V_{OH} V_{OL}	Output "1" Voltage "0"	2.4* –	3.2* 0.35	– 0.50	V V	I_{OH} = -2.0mA, V_{CC} = V_{CC} Min. I_{OL} = +16mA, V_{CC} = V_{CC} Min.
I_{OHE} I_{OLE}	Output Disable "1" Current "0"	– –	– –	+40 -40*	µA µA	V_{OH}, V_{CC} = V_{CC} Max. V_{OL} = 0.3V, V_{CC} = V_{CC} Max.
V_{CL}	Input Clamp Voltage	–	–	-1.2	V	I_{IN} = -18mA
I_{OS}	Output Short Circuit Current	-15*	-2.5	-100*	mA	V_{OUT} = 0.0V, One Output at a Time for a Max. of 1 Second
I_{CC}	Power Supply Current	–	120	170	mA	V_{CC} = V_{CC} Max., All Inputs Grounded.

NOTE: Positive current defined as into device terminals.
*"Three State" only

A.C. ELECTRICAL CHARACTERISTICS (Operating)

		HM-7686RP/87RP-5 5V ± 5% 0°C to +75°C			HM-7686RP/87RP-2 5V ± 10% -55°C to +125°C				
SYMBOL	PARAMETER	MIN	TYP	MAX	MIN	TYP	MAX	UNITS	TEST COND.
T_{AA}	Address Access Time	–	45	60	–	–	80	ns	Latched or
T_{DA}	Chip Disable Access Time	–	30	40	–	–	50	ns	Transparent
T_{EA}	Chip Enable Access Time	–	30	40	–	–	50	ns	
T_{PU}	Chip Power-Up Access Time	–	80	100	–	–	150	ns	
T_{ADH}	Address Hold Time	0	-10	–	0	-10	–	ns	Latched Only
T_{CDH}	Chip Enable Hold Time	10	0	–	10	0	–	ns	
T_{SW}	Strobe Pulse Width	30	10	–	40	10	–	ns	
T_{SL}	Strobe Latch Time	60	40	–	80	40	–	ns	
T_{DL}	Strobe Delatch Time	–	–	40	–	–	50	ns	
T_{CDS}	Chip Enable Set-Up Time	40	–	–	50	–	–	ns	

A.C. limits guaranteed for worst case N^2 sequencing.

CAPACITANCE: T_A = 25°C

SYMBOL	PARAMETER	MAXIMUM	UNITS	TEST CONDITIONS
C_{INA}, C_{INCE}	Input Capacitance	8	pF	V_{CC} = 5V, V_{IN} = 2.0V, f = 1MHz
C_{OUT}	Output Capacitance	10	pF	V_{CC} = 5V, V_{OUT} = 2.0V, f = 1MHz

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JAN-0512

512 BIT, BIPOLAR PROM
MIL/M38510/20101

Features

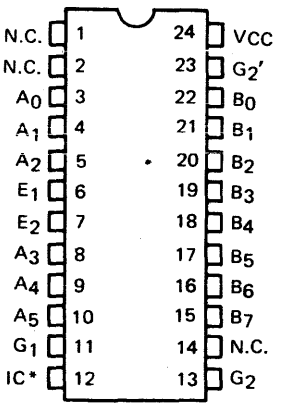
- FIELD PROGRAMMABLE
- 64 WORDS/8 BITS PER WORD
- FULLY DECODED
- DTL/TTL COMPATIBLE
- 55ns ACCESS TIME

Description

The JAN-0512 is a field programmable 64 word by 8 bit PROM. In an unprogrammed memory, all "Memory Elements" are short circuits so that logical "zeros" appear at each output bit position for any address input. "Electronic Programming" involves the alteration of specific "Memory Elements" to create logical "ones" in selected bit positions. This alteration is irreversible and cannot be accomplished under normal operating conditions.

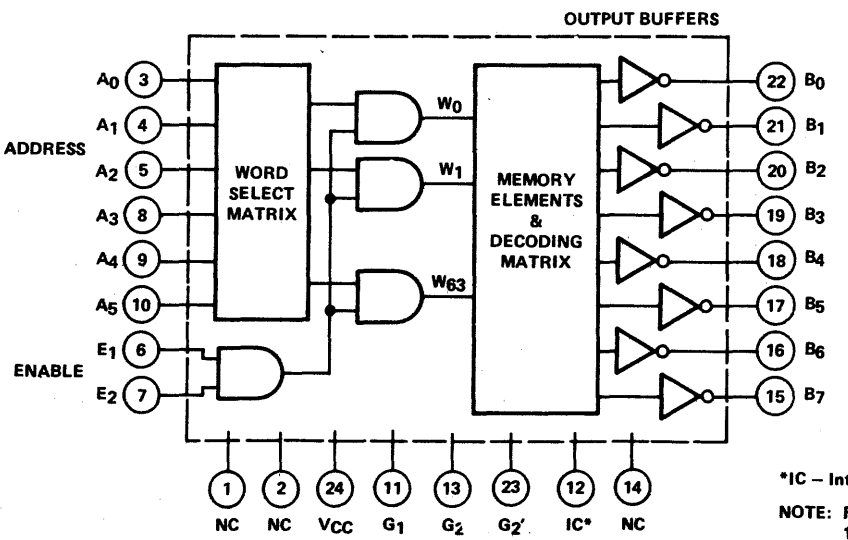
Pinout

TOP VIEW – D.I.P.



*Must be left open circuit

Block Diagram



*IC – Internal Connection must be left open

NOTE: For operational condition, return pins 11, 13, and 23 to system ground.

"SEE PAGES 1409-1415 FOR PACKAGE SELECTION GUIDE"

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ABSOLUTE MAXIMUM RATINGS

Supply Voltage Range	-0.5 V_{DC} to 7.0 V_{DC}
Input Voltage Range	-1.5 V_{DC} at -12mA to 5.5V_{DC}
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering 10 Seconds)	300°C
Thermal Resistance, Junction-to-Case	JC' Case J = 30°C/w
Output Supply Voltage	-0.5V_{DC} to 7.0V_{DC}
Output Sink Current	+30mA
Maximum Power Dissipation, P_D	575mWdc
Maximum Junction Temperature, T_J	175°C

RECOMMENDED OPERATING CONDITIONS

Supply Voltage	4.75 V_{DC} Min. to 5.25V_{DC} Maximum
Minimum High Level Input Voltage	2.0V_{DC}
Maximum Low Level Input Voltage	0.8V_{DC}
Normalized Fanout (Each Output)	6 Maximum (10mA)
Ambient Operating Temperature Range	-55°C to +125°C

ELECTRICAL CHARACTERISTICS

The electrical characteristics are as specified in the table and apply over the full recommended ambient operating temperature range, unless otherwise specified.

SYMBOL	TEST	LIMITS MIN	LIMITS MAX	UNITS	TEST CONDITIONS
V_{OH}	High Level Output Voltage	2.4		Volts	V_{CC} = 4.75V V_{IN} = 0.8V I_{OH} = -500μA
V_{OL}	Low Level Output Voltage		0.45	Volts	V_{CC} = 4.75V V_{IN} = 2.0V I_{OL} = 10mA
V_{IC}	Input Clamp Voltage		-1.5	Volts	V_{CC} = 4.75V I_{IN} = -12mA T_A = 25°C
I_{CEX1}	Maximum Collector Cut-Off Current		100	μA	V_{CC} = 5.25V V_{OH} = 2.8V V_{IN} = 0.8V
I_{CEX2}			200	μA	V_{CC} = 5.25V V_{OH} = 5.25V V_{IN} = 0.8V
I_{IH1}	High Level Input Current		60	μA	V_{CC} = 5.25V V_{IN} = 2.4V;
I_{IH2}			100	μA	V_{CC} = 5.25V V_{IN} = 5.25; ①
I_{IL}	Low Level Input Current	-0.2	-1.6	mA	V_{CC} = 5.25V V_{IN} = 0.4V; ②
I_{CC}	Supply Current		100	mA	V_{CC} = 5.25V V_{IN} = 0
t_{PHL}	Propagation Delay Time High-to-Low Level Logic	25	140	ns	V_{CC} = 5.0V C_L = 30pF Min. R_1 = 470Ω ±5%
t_{PLH}	Propagation Delay Time Low-to-High Level Logic	25	140	ns	

NOTES: 1. When testing one E input, apply 5.25V to the other.
2. When testing one E input, apply GND to the other.

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HM-6312/6312A

CMOS ROM
1024 Word x 12 Bit

Features

- HM-6100 COMPATIBLE
- LOW POWER - TYPICAL < 5.0μW STANDBY
- 4 - 11 VOLT VCC OPERATION
- HIGH SPEED
- STATIC OPERATION

Description

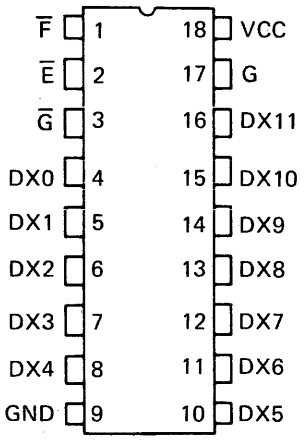
The HM-6312 and HM-6312A are high speed, low power, silicon gate CMOS static ROM's, organized 1024 words by 12 bits. In all static states these units exhibit the microwatt power requirements typical of CMOS. The basic part operates at 4 - 7 volts with a typical 5 volt 25°C access time of 350ns. Higher operating voltages, 4 - 11 volts, are available with the A version. Signal polarities and functions are specified for interfacing with the HM-6100 Microprocessor.

Operation

Addresses and data out are multiplexed on 12 lines, DX0 - DX11. Addresses are loading into an on chip register by falling edge of CE. Data out, corresponding to the latched address, is enabled when CE, OEL and OEH are true. The RSEL output defines an area in the 4096 word addressing space dedicated to RAM. It can be programmed by DX0, DX1, DX2 and DX3. This output eliminates a four bit register and decoder for the high order address bits to select RAM.

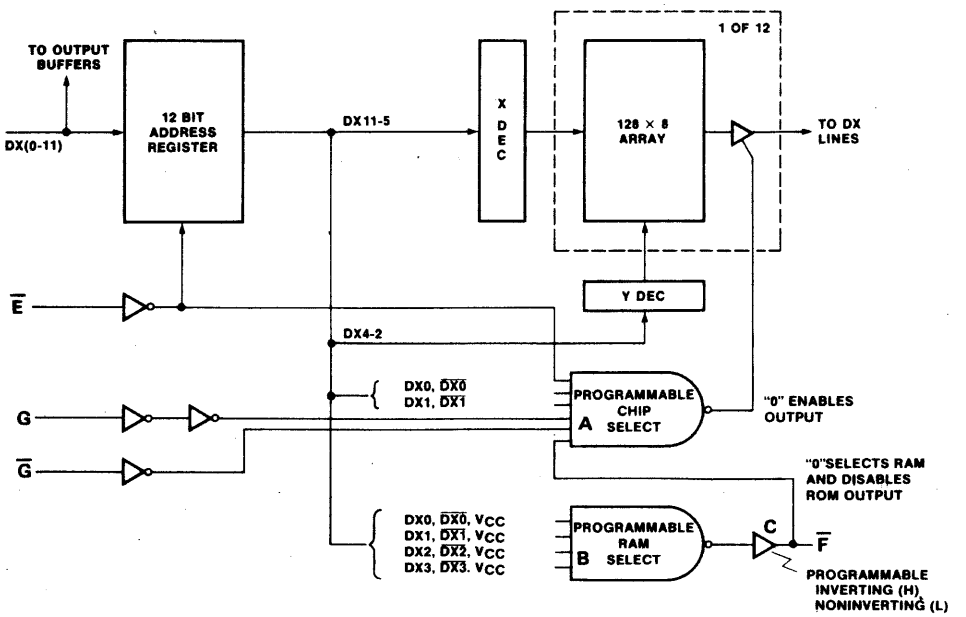
Pinout

TOP VIEW – DIP



DX - Address Input and Data Out
Ē - Chip Enable
G - Output Enable
Ḡ - Output Enable
F̄ - RAM Field Select

Functional Diagram



"SEE PAGES 1409-1415 FOR PACKAGE SELECTION GUIDE"

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ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+12.0V
Applied Input or Output Voltage	GND -0.3V to VCC + 0.3V
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	
Industrial-9	-40°C to +85°C
Military-2	-55°C to +125°C

ELECTRICAL CHARACTERISTICS VCC = 10 ± 5%

D.C.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
VIH	Logical "1" Input Voltage	70% VCC			V	
VIL	Logical "0" Input Voltage			20% VCC	V	
IIL	Input Leakage	-1.0		+1.0	μA	0V ≤ VIN ≤ VCC
VOH	Logical "1" Output Voltage	VCC -0.1			V	IOUT = 0
VOL	Logical "0" Output Voltage			GND + .01	V	IOUT = 0
IO	Output Leakage	-1.0		1.0	μA	0V ≤ VO ≤ VCC
ICCSB	Standby Supply Current			800	μA	VIN = 0 or VCC
ICCOP	Operating Current ①			10	mA	f = 1MHz, IO = 0
CI	Input Capacitance* ②		5.0	7.0	pF	VI = VCC or GND
CIO	I/O Capacitance* ②		6.0	10.0	pF	

*Guaranteed and sampled, but not 100% tested.

See Switching Waveforms page 3-9

A.C.

		INDUSTRIAL		MILITARY			
SYMBOL	PARAMETER	MIN	MAX	MIN	MAX	UNITS	TEST CONDITIONS ③
TELQV	Access Time From $\overline{E}$		200		220	ns	VCC = 10 ± 5%
TGHQV	Output Enable Time		160		175	ns	
TGLQZ	Output Disable Time		160		175	ns	
TEHEL	Strobe Pos. Pulse Width	125		140		ns	
TELEL	Cycle Time	325		360		ns	
TAVEL	Address Set-Up Time	30		35		ns	
TELAX	Address Hold Time	55		60		ns	
TELFV	Propagation to $\overline{F}$		100		110	ns	

NOTES: ① Operating Supply Current (ICCOP) is proportional to operating frequency, example typical ICCOP = 10mA/MHz.
② Capacitance sampled and guaranteed - not 100% tested.
③ A.C. test conditions: Inputs - TRise = TFall = 20ns; Outputs - ITTL Load and 50pF.

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ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+8 .0V
Applied Input or Output Voltage	GND -0.3V to VCC + 0.3V
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	
Industrial-9	-40°C to +85°C
Military-2	-55°C to +125°C

ELECTRICAL CHARACTERISTICS VCC = 5 ± 10%

D.C.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
VIH	Logical "1" Input Voltage	70% VCC			V	
VIL	Logical "0" Input Voltage			20% VCC	V	
IIL	Input Leakage	-1.0		+1.0	μA	0V≤VIN≤VCC
VOH	Logical "1" Output Voltage	VCC -0.1			V	IOUT = 0
VOL	Logical "0" Output Voltage			GND + .01	V	IOUT = 0
IO	Output Leakage	-1.0		1.0	μA	0V≤VO≤VCC
ICCSB	Standby Supply Current			100	μA	VI = 0 or VCC
ICCOP	Operating Current ①			5	mA	f = 1MHz, IO = 0
CI	Input Capacitance* ②		5.0	7.0	pF	VI = VCC or GND
CIO	I/O Capacitance* ②		6.0	10.0	pF	

*Guaranteed and sampled, but not 100% tested.

See Switching Waveforms page 3-9

A.C.

		INDUSTRIAL		MILITARY			
SYMBOL	PARAMETER	MIN	MAX	MIN	MAX	UNITS	TEST CONDITIONS ③
TELQV	Access Time From $\overline{E}$		510		560	ns	VCC = 5 ± 10%
TGHQV	Output Enable Time		290		320	ns	
TGLQZ	Output Disable Time		290		320	ns	
TEHEL	Strobe Pos. Pulse Width	260		285		ns	
TELEL	Cycle Time	770		845		ns	
TAVEL	Address Set-Up Time	75		85		ns	
TELAX	Address Hold Time	120		135		ns	
TELFV	Propagation to $\overline{F}$		220		240	ns	

NOTES: ① Operating Supply Current (ICCOP) is proportional to operating frequency, example typical ICCOP = 5mA/MHz.
② Capacitance sampled and guaranteed - not 100% tested.
③ A.C. test conditions: Inputs - TRise = TFall = 20ns; Outputs - ITTL Load and 50pF.

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ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+8 .0V
Applied Input or Output Voltage	GND -0.3V to VCC + 0.3V
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	-40°C to +85°C

ELECTRICAL CHARACTERISTICS VCC = 5 ± 10%

D.C.

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
VIH	Logical "1" Input Voltage	70% VCC			V	
VIL	Logical "0" Input Voltage			20% VCC	V	
IIL	Input Leakage	-10		+10	μA	$0V \leq VIN \leq VCC$
VOH	Logical "1" Output Voltage	VCC -.01			V	IOUT = 0
VOL	Logical "0" Output Voltage			GND + .01	V	IOUT = 0
IO	Output Leakage	-10		+10	μA	$0V \leq VO \leq VCC$
ICCSB	Standby Supply Current			500	μA	VI = 0 or VCC
ICCOP	Operating Current ①			5	mA	f = 1MHz, IO = 0
CI	Input Capacitance* ②		5.0	7.0	pF	VI = VCC or GND
CIO	I/O Capacitance* ②		6.0	10.0	pF	

*Guaranteed and sampled, but not 100% tested.

See Switching Waveforms page 3-9

A.C.

		INDUSTRIAL					
SYMBOL	PARAMETER	MIN	MAX	MIN	MAX	UNITS	TEST CONDITIONS ③
TELQV	Access Time From $\overline{E}$		640			ns	VCC = 5 ± 10%
TGHQV	Output Enable Time		390			ns	↓
TGLQZ	Output Disable Time		390			ns	
TEHEL	Strobe Pos. Pulse Width	300				ns	
TELEL	Cycle Time	940				ns	
TAVEL	Address Set-Up Time	75				ns	
TELAX	Address Hold Time	140				ns	
TELFV	Propagation to $\overline{F}$		250			ns	

NOTES: ① Operating Supply Current (ICCOP) is proportional to operating frequency, example typical ICCOP = 5mA/MHz.
② Capacitance sampled and guaranteed - not 100% tested.
③ A.C. test conditions: Inputs - TRise = TFall = 20ns; Outputs - ITTL Load and 50pF.

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Preview

HM-6388

8192 x 8 CMOS ROM

Features

- 8K WORD BY 8 BIT MEMORY
- MASK PROGRAMMED, NON-VOLATILE
- QUICK ACCESS OVER MIL TEMP. . . . . 550nsec MAX
- LOW STANDBY CURRENT OVER MIL TEMP. . . . . 100μA MAX
- SINGLE 5V POWER SUPPLY
- ON CHIP ADDRESS REGISTERS
- COMPACT 24 PIN PACKAGE
- PINOUT LIKE HM-6389 FOR EASY UPGRADE
- TTL COMPATIBLE INPUT/OUTPUT
- MILITARY, INDUSTRIAL AND COMMERCIAL TEMPERATURE RANGES

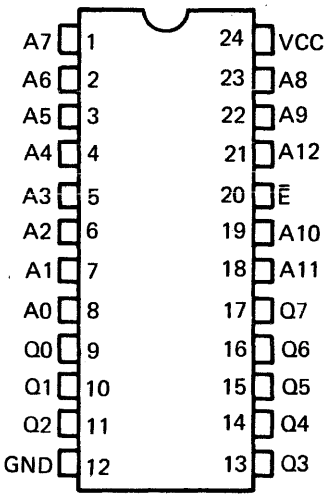
Description

The HM-6388 is a mask programmed Read Only Memory featuring quick access and extremely low power consumption. The 6388 contains internal address registers to allow simple implementation in common bus systems. Because of the similarity of pinouts a system utilizing this device can be easily modified to use the HM-6389 for added control flexibility.

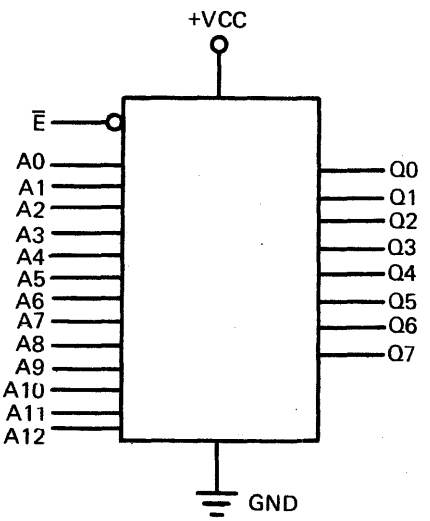
Because of the large memory matrix, 65,536 bits, this device can be used for non-volatile storage of operating systems, control stores, assemblers, compilers, loaders, editors, high accuracy look up tables, and a vast number of other unique and otherwise unsatisfied applications.

Pinout

TOP VIEW



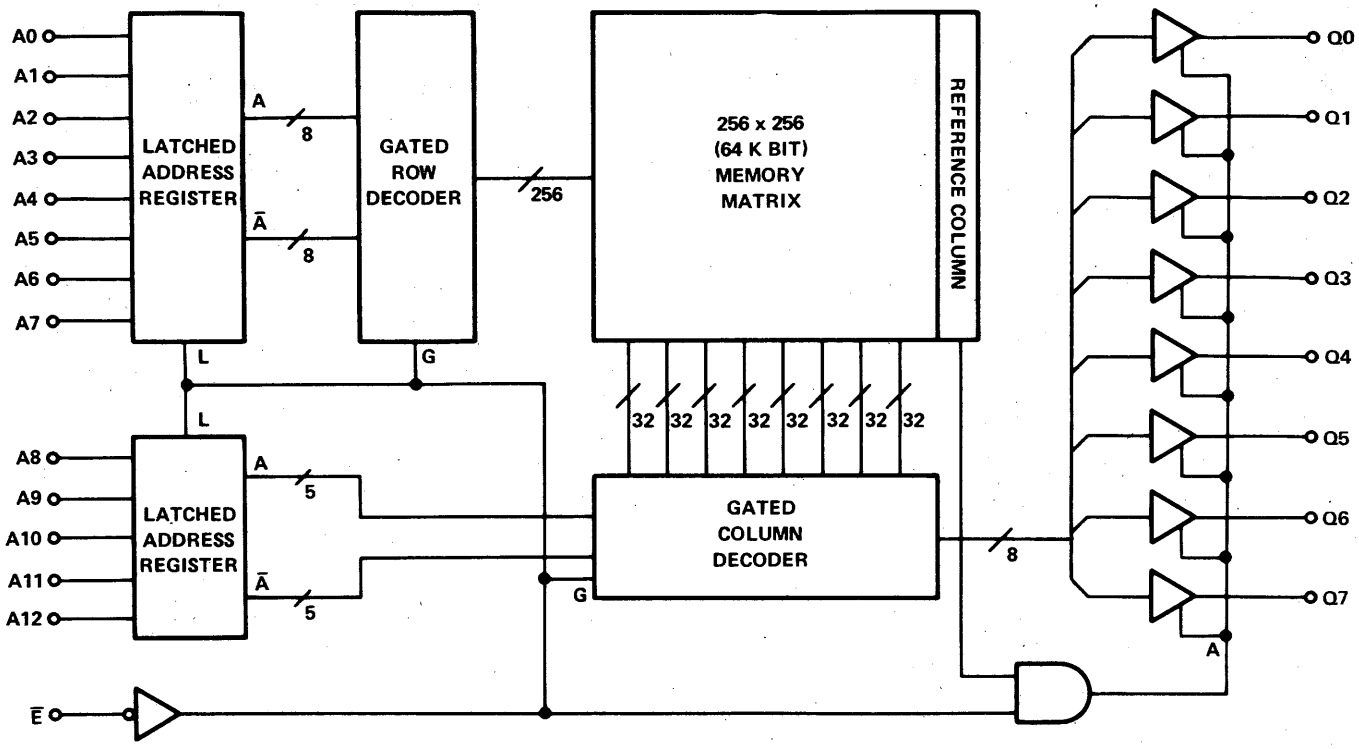
Logic Symbol



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Functional Diagram



LATCHED ADDRESS REGISTER LATCH ON RISING L
GATED DECODERS GATE ON RISING G
THREE STATE DRIVERS ACTIVE WHEN A = HIGH

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HM-6389

8192 x 8 CMOS ROM

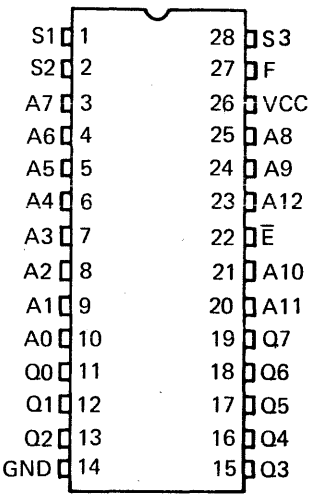
Preview

Features

- 8K WORD BY 8 BIT MEMORY
- MASK PROGRAMMED, NON-VOLATILE
- QUICK ACCESS OVER MIL TEMP. . . . . 550nsec MAX
- LOW STANDBY CURRENT OVER MIL TEMP. . . . . 100μA MAX
- SINGLE 5V POWER SUPPLY
- ON CHIP ADDRESS REGISTERS
- INTERNAL PLA FOR RAM FIELD SELECT OUTPUT
- CHIP SELECT POLARITY OPTIONS
- CHIP SELECT LATCHED/UNLATCHED OPTIONS
- DATA OUTPUT LATCHED/NONLATCHED OPTIONS
- TTL COMPATIBLE INPUT/OUTPUT
- MILITARY, INDUSTRIAL AND COMMERCIAL TEMP. RANGES

Pinout

TOP VIEW



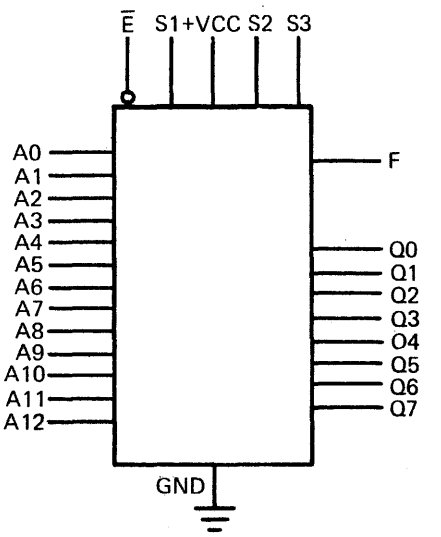
Description

The HM-6389 is a mask programmed Read Only Memory featuring quick access and extremely low power consumption. The HM-6389 contains internal address registers for ease of use in common bus systems. In addition to the 65,536 bit (6K) user defined memory matrix, there are a variety of user defined control options.

These options include a Programmable Logic Array (PLA) for RAM field select allowing internal address decoding for RAM over ROM overlay memory array applications. The polarity of the RAM Field Select output is also an user option. The chip select inputs are individually definable to be active high or low, and to be latched by chip enable or nonlatched. This feature can be used to eleminate address decoding for arrays as large as 64K words. Another user defined option determines whether the data outputs will be latched by the chip enable ($\overline{E}$), or is nonlatched mode is chosen, the chip enable signal is used to disable the three state output drivers.

Because of the large data storage matrix and the versatility of the control options, this device can be used for non-volitile storage of operating systems, assemblers, compilers, loaders, editors, high accuracy look up tables, and a wide variety of otherwise unsatisfied applications.

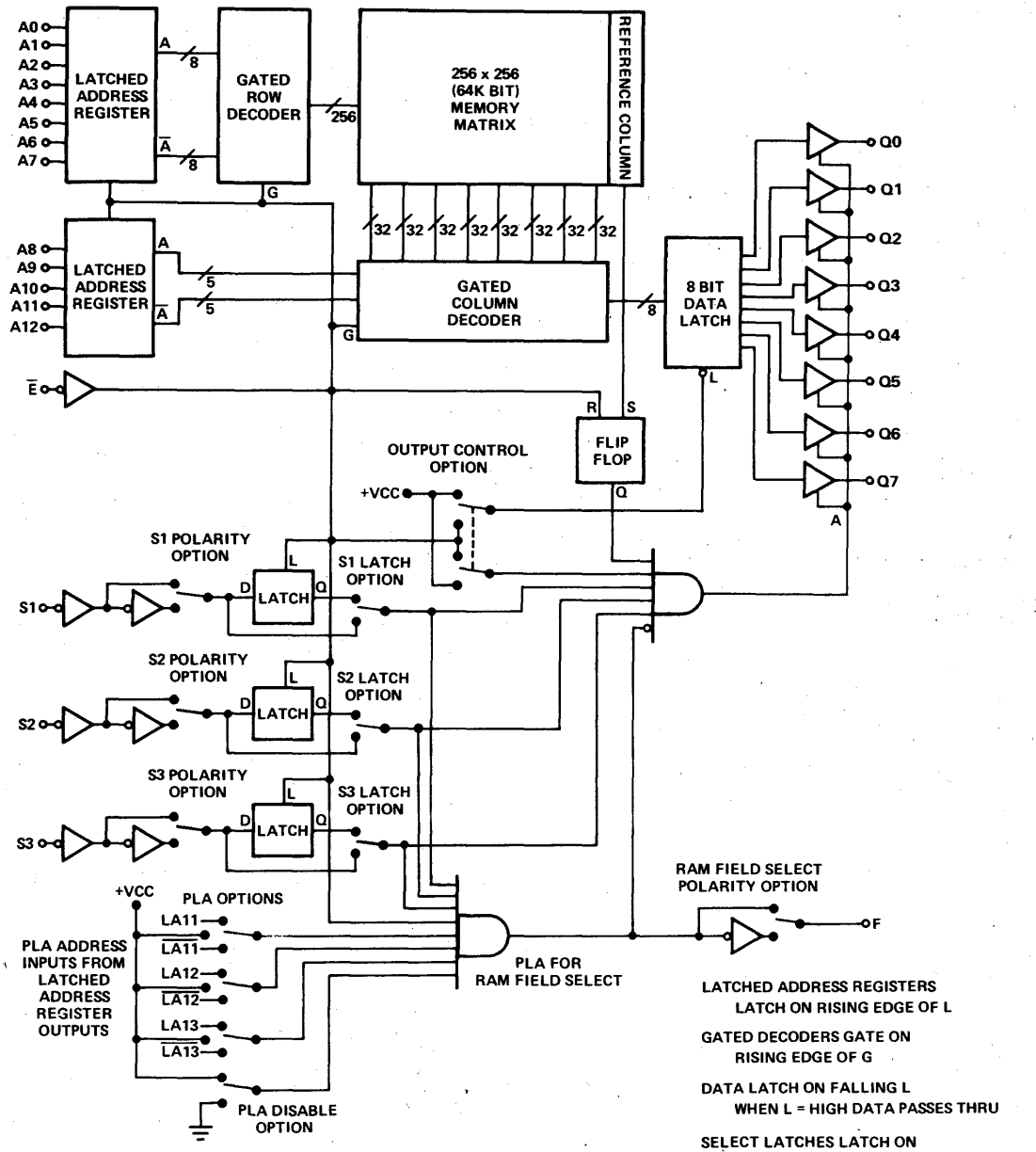
Logic Symbol



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Functional Diagram



LATCHED ADDRESS REGISTERS LATCH ON RISING EDGE OF L

GATED DECODERS GATE ON RISING EDGE OF G

DATA LATCH ON FALLING L WHEN L = HIGH DATA PASSES THRU

SELECT LATCHES LATCH ON RISING EDGE OF L

THREE STATE OUTPUTS ACTIVE IF A = HIGH

ALL SWITCHES ILLUSTRATE USER DEFINED MASK PROGRAMMED OPTIONS. ONCE MANUFACTURED ALL OPTIONS ARE INTERNALLY FIXED AND CAN NOT BE CHANGED.

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HM-6501

256 x 4 CMOS RAM

Features

- LOW STANDBY POWER . . . . . 55μW MAX
- LOW OPERATING POWER. . . . . 22mW/MHz MAX
- FAST ACCESS TIME . . . . . 220nsec MAX
- DATA RETENTION VOLTAGE . . . . . 2.0 VOLTS MIN.
- TTL COMPATIBLE IN/OUT
- HIGH OUTPUT DRIVE - 2 TTL LOADS
- HIGH NOISE IMMUNITY
- ON CHIP ADDRESS REGISTERS
- THREE STATE OUTPUTS
- EASY MICROPROCESSOR INTERFACING
- LATCHED OUTPUTS
- MILITARY AND INDUSTRIAL TEMPERATURE RANGES

Description

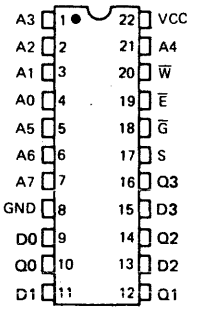
The HM-6501 is a 256 by 4 static CMOS RAM fabricated using self-aligned silicon gate technology. Synchronous circuit design techniques are employed to achieve high performance and low power operation.

On chip latches are provided for address and data outputs allowing efficient interfacing with microprocessor systems. The data output buffers can be forced to a high impedance state for use in expanded memory arrays.

The HM-6501 is a fully static RAM and may be maintained in any state for an indefinite period of time. Data retention supply voltage and supply current are guaranteed over temperature.

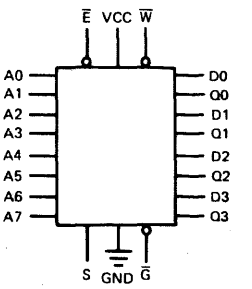
Pinout

TOP VIEW

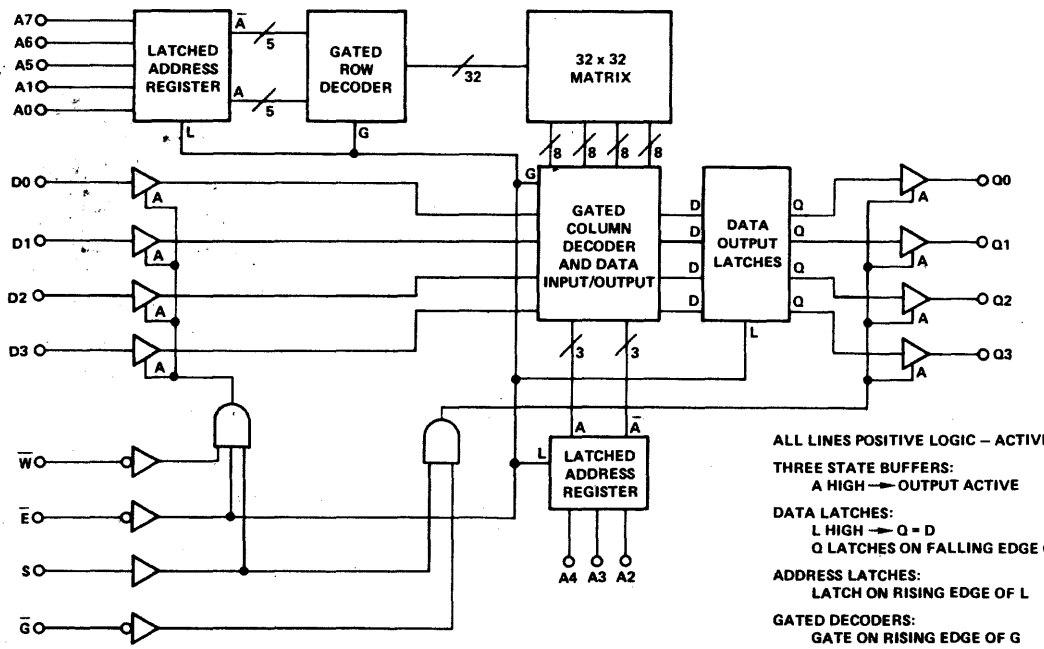


A - ADDRESS INPUT
E - CHIP ENABLE
W - WRITE ENABLE
G - OUTPUT ENABLE
S - CHIP SELECT
D - DATA INPUT
Q - DATA OUTPUT

Logic Symbol



Functional Diagram



ALL LINES POSITIVE LOGIC – ACTIVE HIGH

THREE STATE BUFFERS:
A HIGH → OUTPUT ACTIVE

DATA LATCHES:
L HIGH → Q = D
Q LATCHES ON FALLING EDGE OF L

ADDRESS LATCHES:
LATCH ON RISING EDGE OF L

GATED DECODERS:
GATE ON RISING EDGE OF G

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ABSOLUTE MAXIMUM RATINGS

Supply Voltage -VCC	+8.0V
Applied Input or Output Voltage	GND -0.3V VCC +0.3V
Storage Temperature	-65°C to +150°C

OPERATING RANGE

Operating Supply Voltage -VCC	
Military (-2)	4.5V to 5.5V
Industrial (-9)	4.5V to 5.5V
Operating Temperature	
Military (-2)	-55°C to +125°C
Industrial (-9)	-40°C to +85°C

ELECTRICAL CHARACTERISTICS

	SYMBOL	PARAMETER	TEMP. & VCC = OPERATING RANGE		TEMP. = 25°C ① VCC = 5.0V			UNITS	TEST CONDITIONS
			MIN	MAX	MIN	TYP	MAX		
D.C.	ICCSB	Standby Supply Current		10 1(+25°C)		0.1	1	μA	IO = 0 VI = VCC or GND
	ICCOP	Operating Supply Current ②		4		1.5	2.5	mA	f = 1MHz, IO = 0 VI = VCC or GND
	ICCDR	Data Retention Supply Current		10		0.01	1	μA	VCC = 3.0, IO = 0 VI = VCC or GND
	VCCDR	Data Retention Supply Voltage	2.0		2.0	1.4		V	
	II	Input Leakage Current	-1.0	+1.0	-0.5	0.0	+0.5	μA	GND ≤ VI ≤ VCC
	IOZ	Output Leakage Current	-1.0	+1.0	-0.5	0.0	+0.5	μA	GND ≤ VO ≤ VCC
	VIL	Input Low Voltage	-0.3	0.8	-0.3	2.0	1.5	V	
	VIH	Input High Voltage	VCC -2.0	VCC +0.3	2.5	2.0	5.3	V	
	VOL	Output Low Voltage		0.4		0.2	0.35	V	IOL = 3.2mA
	VOH	Output High Voltage	2.4		3.0	4.5		V	IOH = -0.4mA
	CI	Input Capacitance ③		6		4	6	pF	VI = VCC or GND f = 1MHz
	CO	Output Capacitance ③		10		6	10	pF	VO = VCC or GND f = 1MHz
A.C.	TELQV	Chip Enable Access Time		220		120	170	ns	④
	TAVQV	Address Access Time		220		110	170	ns	④
	TSHQX	Chip Select Output Enable Time		130		50	90	ns	④
	TGLQX	Output Enable Output Enable Time		130		50	90	ns	④
	TSLQZ	Chip Select Output Disable Time		130		50	90	ns	④
	TGHQZ	Output Enable Output Disable Time		130		50	90	ns	④
	TELEH	Chip Enable Pulse Negative Width	220		170	120		ns	④
	TEHEL	Chip Enable Pulse Positive Width	100		70	50		ns	④
	TAVEL	Address Setup Time	0		0	-10		ns	④
	TELAX	Address Hold Time	40		30	20		ns	④
	TDVWH	Data Setup Time	100		80	50		ns	④
	TWHDX	Data Hold Time	0		0	-10		ns	④
	TWLSL	Chip Select Write Pulse Setup Time	120		100	60		ns	④
	TWLEH	Chip Enable Write Pulse Setup Time	120		100	60		ns	④
	TSHWH	Chip Select Write Pulse Hold Time	120		100	60		ns	④
	TELWH	Chip Enable Write Pulse Hold Time	120		100	60		ns	④
	TWLWH	Write Enable Pulse Width	120		100	60		ns	④
	TELEL	Read or Write Cycle Time	320		240	170		ns	④

NOTES:
1. All devices tested at worst case limits. Room temp., 5 volt data provided for information — not guaranteed.
2. Operating Supply Current (ICCOP) is proportional to Operating Frequency. Example: Typical ICCOP = 1.5mA/MHz.
3. Capacitance sampled and guaranteed — not 100% tested.
4. AC Test Conditions: Inputs — TRISE = TFALL = 20nsec; Outputs — 1 TTL load and 50pF. All timing measurements at 1/2 VCC.

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ABSOLUTE MAXIMUM RATINGS

Supply Voltage -VCC	+8.0V
Applied Input or Output Voltage	GND -0.3V VCC +0.3V
Storage Temperature	-65°C to +150°C

OPERATING RANGE

Operating Supply Voltage -VCC	
Military (-2)	4.5V to 5.5V
Industrial (-9)	4.5V to 5.5V
Operating Temperature	
Military (-2)	-55°C to +125°C
Industrial (-9)	-40°C to +85°C

ELECTRICAL CHARACTERISTICS

	SYMBOL	PARAMETER	TEMP. & VCC = OPERATING RANGE MIN	TEMP. & VCC = OPERATING RANGE MAX	TEMP. = 25°C ① VCC = 5.0V MIN	TEMP. = 25°C ① VCC = 5.0V TYP	TEMP. = 25°C ① VCC = 5.0V MAX	UNITS	TEST CONDITIONS
D.C.	ICCSB	Standby Supply Current		10 1(+25°C)		1.0	1	μA	IO = 0 VI = VCC or GND
	ICCOP	Operating Supply Current ②		4		1.5	2.5	mA	f = 1MHz, IO = 0 VI = VCC or GND
	ICCDR	Data Retention Supply Current		10		0.1	1	μA	VCC = 3.0, IO = 0 VI = VCC or GND
	VCCDR	Data Retention Supply Voltage	2.0		2.0	1.4		V	
	II	Input Leakage Current	-1.0	+1.0	-0.5	0.0	+0.5	μA	GND ≤ VI ≤ VCC
	IOZ	Output Leakage Current	-1.0	+1.0	-0.5	0.0	+0.5	μA	GND ≤ VO ≤ VCC
	VIL	Input Low Voltage	-0.3	0.8	-0.3	2.0	1.5	V	
	VIH	Input High Voltage	VCC -2.0	VCC +0.3	2.5	2.0	5.3	V	
	VOL	Output Low Voltage		0.4		0.2	0.35	V	IOL = 3.2mA
	VOH	Output High Voltage	2.4		3.0	4.5		V	IOH = -0.4mA
	CI	Input Capacitance ③		6		4	6	pF	VI = VCC or GND f = 1MHz
	CO	Output Capacitance ③		10		6	10	pF	VO = VCC or GND f = 1MHz
A.C.	TELQV	Chip Enable Access Time		300		160	240	ns	④
	TAVQV	Address Access Time		300		150	240	ns	④
	TSHQX	Chip Select Output Enable Time		150		60	120	ns	④
	TGLQX	Output Enable Output Enable Time		150		60	120	ns	④
	TSLQZ	Chip Select Output Disable Time		150		60	120	ns	④
	TGHQZ	Output Enable Output Disable Time		150		60	120	ns	④
	TELEH	Chip Enable Pulse Negative Width	300		240	160		ns	④
	TEHEL	Chip Enable Pulse Positive Width	100		70	50		ns	④
	TAVEL	Address Setup Time	0		0	-10		ns	④
	TELAX	Address Hold Time	50		40	30		ns	④
	TDVWH	Data Setup Time	150		120	100		ns	④
	TWHDX	Data Hold Time	0		0	-10		ns	④
	TWLSL	Chip Select Write Pulse Setup Time	180		150	120		ns	④
	TWLEH	Chip Enable Write Pulse Setup Time	180		150	120		ns	④
	TSHWH	Chip Select Write Pulse Hold Time	180		150	120		ns	④
	TELWH	Chip Enable Write Pulse Hold Time	180		150	120		ns	④
	TWLWH	Write Enable Pulse Width	180		150	120		ns	④
	TELEL	Read or Write Cycle Time	400		310	210		ns	④

NOTES:
1. All devices tested at worst case limits. Room temp., 5 volt data provided for information — not guaranteed.
2. Operating Supply Current (ICCOP) is proportional to Operating Frequency. Example: Typical ICCOP = 1.5mA/MHz.
3. Capacitance sampled and guaranteed — not 100% tested.
4. AC Test Conditions: Inputs — TRISE = TFALL = 20nsec; Outputs — 1 TTL load and 50pF. All timing measurements at 1/2 VCC.

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ABSOLUTE MAXIMUM RATINGS

Supply Voltage -VCC	+8.0V
Applied Input or Output Voltage	GND -0.3V VCC +0.3V
Storage Temperature	-65°C to +150°C

OPERATING RANGE

Operating Supply Voltage -VCC Commercial	4.75V to 5.25V
Operating Temperature Commercial	0°C to 75°C

ELECTRICAL CHARACTERISTICS

	SYMBOL	PARAMETER	TEMP. & VCC = OPERATING RANGE MIN	TEMP. & VCC = OPERATING RANGE MAX	TEMP. = 25°C ① VCC = 5.0V MIN	TEMP. = 25°C ① VCC = 5.0V TYP	TEMP. = 25°C ① VCC = 5.0V MAX	UNITS	TEST CONDITIONS
D.C.	ICCSB	Standby Supply Current		100		10	100	μA	IO = 0 VI = VCC or GND
	ICCOP	Operating Supply Current ②		4		1.5	2.5	mA	f = 1MHz, IO = 0 VI = VCC or GND
	VCCDR	Data Retention Supply Voltage	2.0		2.0			V	
	II	Input Leakage Current	-1.0	+1.0	-0.5	0.0	+0.5	μA	GND ⩽ VI ⩽ VCC
	IOZ	Output Leakage Current	-1.0	+1.0	-0.5	0.0	+0.5	μA	GND ⩽ VO ⩽ VCC
	VIL	Input Low Voltage	-0.3	0.8	-0.3	2.0	1.5	V	
	VIH	Input High Voltage	VCC -2.0	VCC +0.3	2.5	2.0	5.3	V	
	VOL	Output Low Voltage		0.4		0.2	0.35	V	IOL = 1.6mA
	VOH	Output High Voltage	2.4		3.0	4.5		V	IOH = -0.2mA
	CI	Input Capacitance ③		6		4	6	pF	VI = VCC or GND f = 1MHz
	CO	Output Capacitance ③		10		6	10	pF	VO = VCC or GND f = 1MHz
A.C.	TELQV	Chip Enable Access Time		350		200	300	ns	④
	TAVQV	Address Access Time		360		200	310	ns	④
	TSHQX	Chip Select Output Enable Time		180		80	160	ns	④
	TGLQX	Output Enable Output Enable Time		180		80	160	ns	④
	TSLQZ	Chip Select Output Disable Time		180		80	160	ns	④
	TGHQZ	Output Enable Output Disable Time		180		80	160	ns	④
	TELEH	Chip Enable Pulse Negative Width	350		300	200		ns	④
	TEHEL	Chip Enable Pulse Positive Width	150		130	90		ns	④
	TAVEL	Address Setup Time	10		10	0		ns	④
	TELAX	Address Hold Time	70		50	40		ns	④
	TDVWH	Data Setup Time	170		140	120		ns	④
	TWHDX	Data Hold Time	0		0	-10		ns	④
	TWLSL	Chip Select Write Pulse Setup Time	210		170	150		ns	④
	TWLEH	Chip Enable Write Pulse Setup Time	210		170	150		ns	④
	TSHWH	Chip Select Write Pulse Hold Time	210		170	150		ns	④
	TELWH	Chip Enable Write Pulse Hold Time	210		170	150		ns	④
	TWLWH	Write Enable Pulse Width	210		170	150		ns	④
	TELEL	Read or Write Cycle Time	500		430	290		ns	④

NOTES:
1. All devices tested at worst case limits. Room temp., 5 volt data provided for information — not guaranteed.
2. Operating Supply Current (ICCOP) is proportional to Operating Frequency. Example: Typical ICCOP = 1.5mA/MHz.
3. Capacitance sampled and guaranteed — not 100% tested.
4. AC Test Conditions: Inputs — TRISE = TFALL = 20nsec; Outputs — 1 TTL load and 50pF. All timing measurements at 1/2 VCC.

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HM-6503

2048 x 1 CMOS RAM

Features

- LOW POWER STANDBY . . . . . ≪1mW MAX.
- LOW POWER OPERATION. . . . . 35mW/MHz MAX.
- EXTREMELY LOW SPEED POWER PRODUCT
- DATA RETENTION . . . . . @ 2.0V MIN.
- TTL COMPATIBILITY INPUT/OUTPUT
- THREE STATE OUTPUT
- FAST ACCESS TIME . . . . . 300nsec MAX.
- INDUSTRIAL OR COMMERCIAL TEMPERATURE RANGE
- 18 PIN PACKAGE FOR HIGH DENSITY
- ON CHIP ADDRESS REGISTER
- PINOUT ALLOWS UPGRADE TO 6504

Description

The HM-6503 is a 2048 x 1 static CMOS RAM fabricated using self aligned silicon gate technology. The device utilizes synchronous circuitry to achieve high performance and low power operation.

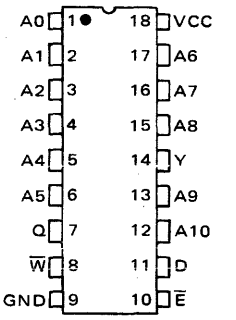
On chip latches are provided for addresses, data input and data output allowing efficient interfacing with microprocessor systems. The data output can be forced to a high impedance for use in expanded memory arrays.

The HM-6503 is a truly static RAM and may be maintained in any state for an indefinite period of time. Data retention supply voltage and supply current are guaranteed over temperature.

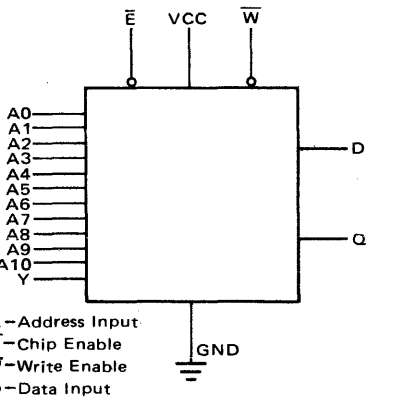
The HM-6503 is supplied in two versions, the HM-6503H and the HM-6503L. The H or L is used to designate the logic level to be connected to the Y input. If a HM-6503H is procured the user must connect the Y input to VCC in the system. If a HM-6503L is used the Y input must be connected to system ground.

Pinout

TOP VIEW

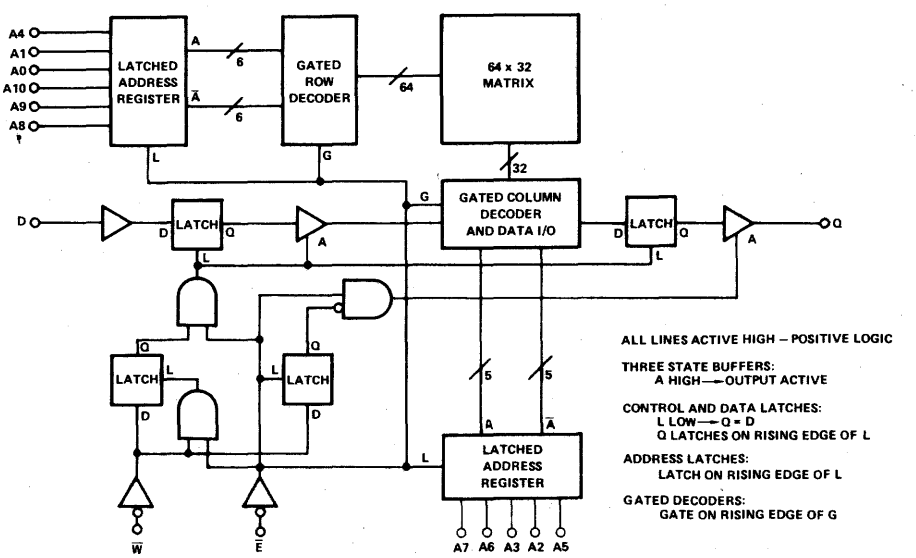


Logic Symbol



A–Address Input
Ē–Chip Enable
W̄–Write Enable
D–Data Input
Q–Data Output
Y–Hard Wired Input

Functional Diagram



ALL LINES ACTIVE HIGH – POSITIVE LOGIC

THREE STATE BUFFERS:
A HIGH—OUTPUT ACTIVE

CONTROL AND DATA LATCHES:
L LOW—Q = D
Q LATCHES ON RISING EDGE OF L

ADDRESS LATCHES:
LATCH ON RISING EDGE OF L

GATED DECODERS:
GATE ON RISING EDGE OF G

"SEE PAGES 1409-1415 FOR PACKAGE SELECTION GUIDE"

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ABSOLUTE MAXIMUM RATINGS

Supply Voltage – VCC	+8.0V
Input or Output Voltage Applied	GND -0.3V to VCC +0.3V
Storage Temperature	-65°C to +150°C

OPERATING RANGE

Operating Supply Voltage	
Industrial (-9)	4.5V to 5.5V
Operating Temperature	
Industrial (-9)	-40°C to +85°C

ELECTRICAL CHARACTERISTICS

			TEMP. & VCC = OPERATING RANGE		TEMP = 25°C ① VCC = 5.0V				
	SYMBOL	PARAMETER	MIN	MAX	MIN	TYP	MAX	UNITS	TEST CONDITIONS
D.C.	ICCSB	Standby Supply Current		50		0.1	10	μA	IO = 0 VI = VCC or GND
	ICCOP	Operating Supply Current ②		7		5	6	mA	f = 1MHz, IO = 0 VI = VCC or GND
	ICCDR	Data Retention Supply Current		25		0.01	5	μA	IO = 0 VCC = 3.0 VI = VCC or GND
	VCCDR	Data Retention Supply Voltage	2.0		2.0	1.4		V	
	II	Input Leakage Current	-1.0	+1.0	-0.5	0.0	+0.5	μA	GND≤VI≤VCC
	IOZ	Output Leakage Current	-1.0	+1.0	-0.5	0.0	+0.5	μA	GND≤VO≤VCC
	VIL	Input Low Voltage	-0.3	0.8	-0.3	2.0	1.5	V	
	VIH	Input High Voltage	VCC -2.0	VCC +0.3	2.5	2.0	5.3	V	
	VOL	Output Low Voltage		0.4		0.25	0.35	V	IO = 2.0mA
	VOH	Output High Voltage	2.4		3.5	4.0		V	IO = -1.0mA
	CI	Input Capacitance ③		8.0		5.0	8.0	pF	f = 1MHz VI = VCC or GND
	CO	Output Capacitance ③		10.0		6.0	10.0	pF	f = 1MHz VO=VCC or GND
A.C.	TELQV	Chip Enable Access Time		300		170	250	ns	④
	TAVQV	Address Access Time		320		170	270	ns	④
	TELQX	Chip Enable Output Enable Time		100		50	80	ns	④
	TEHQZ	Chip Enable Output Disable Time		100		50	80	ns	④
	TELEH	Chip Enable Pulse Negative Width	300		250	170		ns	④
	TEHEL	Chip Enable Pulse Positive Width	120		100	70		ns	④
	TAVEL	Address Setup Time	20		20	0		ns	④
	TELAX	Address Hold Time	50		50	20		ns	④
	TWLWH	Write Enable Pulse Width	80		60	40		ns	④
	TWLEH	Write Enable Pulse Setup Time	200		150	130		ns	④
	TWLEL	Early Write Pulse Setup Time	0		0	-10		ns	④
	TWHEL	Write Enable Read Mode Setup Time	0		0	-10		ns	④
	TELWH	Early Write Pulse Hold Time	80		60	40		ns	④
	TDVWL	Data Setup Time	0		0	-10		ns	④
	TDVEL	Early Write Data Setup Time	0		0	-10		ns	④
	TWLDX	Data Hold Time	80		60	40		ns	④
	TELDX	Early Write Data Hold Time	80		60	40		ns	④
	TELWL	Early Write Output Hi-Z Time	0		0	-10		ns	④
	TQVWL	Data Valid to Write Time	0		0	0		ns	④
	TELEL	Read or Write Cycle Time	420		350	240		ns	④

NOTES:
1. All devices tested at worst case limits. Room temp., 5 volt data provided for information – not guaranteed.
2. Operating Supply Current (ICCOP) is proportional to Operating Frequency. Example: Typical ICCOP = 5mA/MHz.
3. Capacitance sampled and guaranteed – not 100% tested.
4. AC test conditions: Inputs – TRISE = TFALL = 20nsec; Output – 1 TTL load and 50pF; All timing measured at ½ VCC.

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ABSOLUTE MAXIMUM RATINGS

Supply Voltage – VCC	+8.0V
Input or Output Voltage Applied	GND -0.3V to VCC +0.3V
Storage Temperature	-65°C to +150°C

OPERATING RANGE

Operating Supply Voltage Commercial	4.75V to 5.25V
Operating Temperature Commercial	0°C to +75°C

ELECTRICAL CHARACTERISTICS

			TEMP. & VCC = OPERATING RANGE		TEMP = 25°C ① VCC = 5.0V				
	SYMBOL	PARAMETER	MIN	MAX	MIN	TYP	MAX	UNITS	TEST CONDITIONS
D.C.	ICCSB	Standby Supply Current		500		100	500	μA	IO = 0 VI = VCC or GND
	ICCOP	Operating Supply Current ②		7		5	6	mA	f = 1MHz, IO = 0 VI = VCC or GND
	II	Input Leakage Current	-10.0	+10.0	-7.0	±0.5	+7.0	μA	GND ≤ VI ≤ VCC
	IOZ	Output Leakage Current	-10.0	+10.0	-7.0	±0.5	+7.0	μA	GND ≤ VO ≤ VCC
	VIL	Input Low Voltage	-0.3	0.8	-0.3	2.0	1.5	V	
	VIH	Input High Voltage	VCC -2.0	VCC +0.3	2.5	2.0	5.3	V	
	VOL	Output Low Voltage		0.4		0.25	0.35	V	IO = 1.6mA
	VOH	Output High Voltage	2.4		3.5	4.0		V	IO = -0.4mA
	CI	Input Capacitance ③		8.0		5.0	8.0	pF	f = 1MHz VI = VCC or GND
	CO	Output Capacitance ③		10.0		6.0	10.0	pF	f = 1MHz VO=VCC or GND
A.C.	TELQV	Chip Enable Access Time		350		200	300	ns	④
	TAVQV	Address Access Time		370		200	320	ns	④
	TELQX	Chip Enable Output Enable Time		100		50	80	ns	④
	TEHQZ	Chip Enable Output Disable Time		100		50	80	ns	④
	TELEH	Chip Enable Pulse Negative Width	350		300	200		ns	④
	TEHEL	Chip Enable Pulse Positive Width	150		120	100		ns	④
	TAVEL	Address Setup Time	20		20	0		ns	④
	TELAX	Address Hold Time	50		50	20		ns	④
	TWLWH	Write Enable Pulse Width	100		80	60		ns	④
	TWLEH	Write Enable Pulse Setup Time	250		200	100		ns	④
	TWLEL	Early Write Pulse Setup Time	.0		0	-10		ns	④
	TWHEL	Write Enable Read Setup Time	0		0	-10		ns	④
	TELWH	Early Write Pulse Hold Time	100		80	60		ns	④
	TDVWL	Data Setup Time	30		20	0		ns	④
	TDVEL	Early Write Data Setup Time	30		20	0		ns	④
	TWLDX	Data Hold Time	100		80	60		ns	④
	TELDX	Early Write Data Hold Time	100		80	80		ns	④
	TELWL	Early Write Output Hi-Z Time	0		0	-10		ns	④
	TQVWL	Data Valid to Write Time	0		0	0		ns	④
	TELEL	Read or Write Cycle Time	500		420	300		ns	④

NOTES:
1. All devices tested at worst case limits. Room temp., 5 volt data provided for information – not guaranteed.
2. Operating Supply Current (ICCOP) is proportional to Operating Frequency. Example: Typical ICCOP = 5mA/MHz.
3. Capacitance sampled and guaranteed – not 100% tested.
4. AC test conditions: Inputs – TRISE = TFALL = 20nsec; Output – 1 TTL load and 50pF; All timing measured at ½ VCC.

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HARRIS
SEMICONDUCTOR
PRODUCTS DIVISION
A DIVISION OF HARRIS CORPORATION

HM-6504

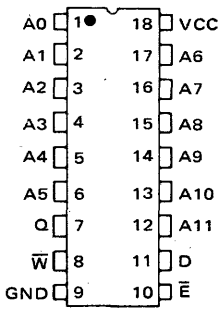
4096 x 1 CMOS RAM

Features

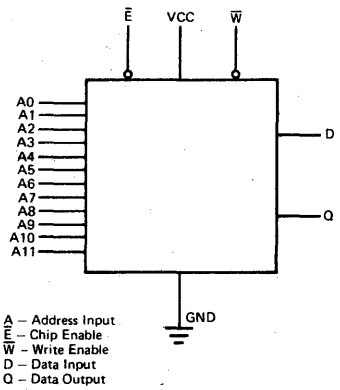
- LOW POWER STANDBY . . . . . ≪ 1mW MAX.
- LOW POWER OPERATION . . . . . 35mW/MHz MAX.
- EXTREMELY LOW SPEED POWER PRODUCT
- DATA RETENTION . . . . . @ 2.0V MIN.
- TTL COMPATIBLE INPUT/OUTPUT
- THREE-STATE OUTPUT
- STANDARD JEDEC PINOUT
- FAST ACCESS TIME . . . . . 300nsec MAX.
- MILITARY TEMPERATURE RANGE
- INDUSTRIAL TEMPERATURE RANGE
- 18 PIN PACKAGE FOR HIGH DENSITY
- ON CHIP ADDRESS REGISTER

Pinout

TOP VIEW



Logic Symbol



A – Address Input
E – Chip Enable
W – Write Enable
D – Data Input
Q – Data Output

Description

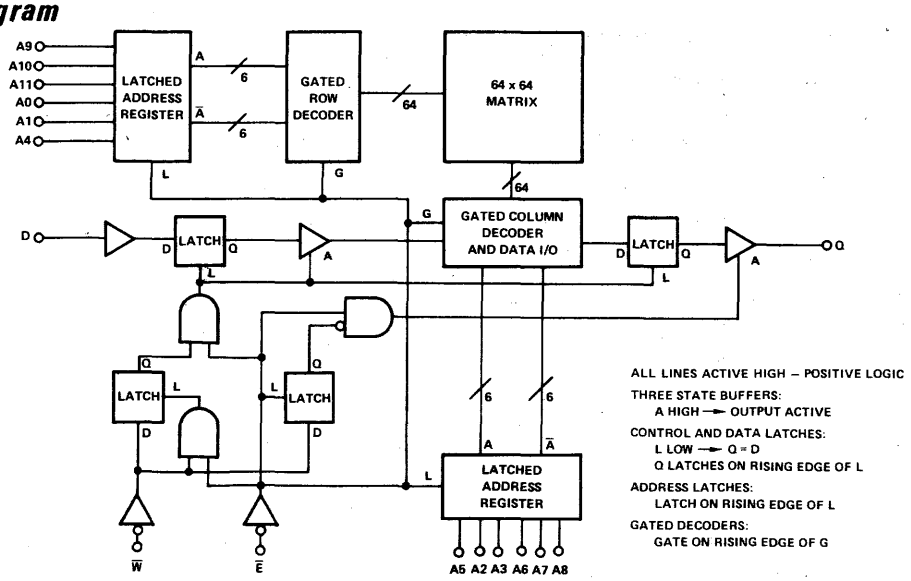
The HM-6504 is a 4096 x 1 static CMOS RAM fabricated using self aligned silicon gate technology. The device utilizes synchronous circuitry to achieve high performance and low power operation.

On chip latches are provided for addresses, data input and data output allowing efficient interfacing with microprocessor systems. The data output can be forced to a high impedance for use in expanded memory arrays.

The HM-6504 is a truly static RAM and may be maintained in any state for an indefinite period of time.

Data retention supply voltage and supply current are guaranteed over temperature.

Functional Diagram



"SEE PAGES 1409-1415 FOR PACKAGE SELECTION GUIDE"

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ABSOLUTE MAXIMUM RATINGS

Supply Voltage – VCC	+8.0V
Input or Output Voltage Applied	GND -0.3V to VCC +0.3V
Storage Temperature	-65°C to +150°C

OPERATING RANGE

Operating Supply Voltage	
Military (-2)	4.5V to 5.5V
Industrial (-9)	4.5V to 5.5V
Operating Temperature	
Military (-2)	-55°C to +125°C
Industrial (-9)	-40°C to +85°C

ELECTRICAL CHARACTERISTICS

	SYMBOL	PARAMETER	TEMP. & VCC = OPERATING RANGE MIN	TEMP. & VCC = OPERATING RANGE MAX	TEMP = 25°C ① VCC = 5.0V MIN	TEMP = 25°C ① VCC = 5.0V TYP	TEMP = 25°C ① VCC = 5.0V MAX	UNITS	TEST CONDITIONS
D.C.	ICCSB	Standby Supply Current		50		0.1	10	μA	IO = 0 VI = VCC or GND
	ICCOP	Operating Supply Current ②		7		5	6	mA	f = 1MHz, IO = 0 VI = VCC or GND
	ICCDR	Data Retention Supply Current		25		0.01	5	μA	IO = 0 VCC = 3.0 VI = VCC or GND
	VCCDR	Data Retention Supply Voltage	2.0		2.0	1.4		V	
	II	Input Leakage Current	-1.0	+1.0	-0.5	0.0	+0.5	μA	GND≤VI≤VCC
	IOZ	Output Leakage Current	-1.0	+1.0	-0.5	0.0	+0.5	μA	GND≤VO≤VCC
	VIL	Input Low Voltage	-0.3	0.8	-0.3	2.0	1.5	V	
	VIH	Input High Voltage	VCC -2.0	VCC +0.3	2.5	2.0	5.3	V	
	VOL	Output Low Voltage		0.4		0.25	0.35	V	IO = 2.0mA
	VOH	Output High Voltage	2.4		3.5	4.0		V	IO = -1.0mA
	CI	Input Capacitance ③		8.0		5.0	8.0	pF	f = 1MHz VI = VCC or GND
	CO	Output Capacitance ③		10.0		6.0	10.0	pF	f = 1MHz VO = VCC or GND
A.C.	TELQV	Chip Enable Access Time		300		170	250	ns	④
	TAVQV	Address Access Time		320		170	270	ns	④
	TELQX	Chip Enable Output Enable Time		100		50	80	ns	④
	TEHQZ	Chip Enable Output Disable Time		100		50	80	ns	④
	TELEH	Chip Enable Pulse Negative Width	300		250	170		ns	④
	TEHEL	Chip Enable Pulse Positive Width	120		100	70		ns	④
	TAVEL	Address Setup Time	20		20	0		ns	④
	TELAX	Address Hold Time	50		50	20		ns	④
	TWLWH	Write Enable Pulse Width	80		60	40		ns	④
	TWLEH	Write Enable Pulse Setup Time	200		150	130		ns	④
	TWLEL	Early Write Pulse Setup Time	0		0	-10		ns	④
	TWHEL	Write Enable Read Mode Setup Time	0		0	-10		ns	④
	TELWH	Early Write Pulse Hold Time	80		60	40		ns	④
	TDVWL	Data Setup Time	0		0	0		ns	④
	TDVEL	Early Write Data Setup Time	0		0	0		ns	④
	TWLDX	Data Hold Time	80		60	40		ns	④
	TELDX	Early Write Data Hold Time	80		60	40		ns	④
	TELWL	Early Write Output Hi-Z Time	0		0	-10		ns	④
	TQVWL	Data Valid to Write Time	0		0	0		ns	④
	TELEL	Read or Write Cycle Time	420		350	240		ns	④

NOTES:
1. All devices tested at worst case limits. Room temp., 5 volt data provided for information – not guaranteed.
2. Operating Supply Current (ICCOP) is proportional to Operating Frequency. Example: Typical ICCOP = 5mA/MHz.
3. Capacitance sampled and guaranteed – not 100% tested.
4. AC test conditions: Inputs – TRISE = TFALL = 20nsec; Output – 1 TTL load and 50pF; All timing measured at ½ VCC.

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ABSOLUTE MAXIMUM RATINGS

Supply Voltage – VCC	+8.0V
Input or Output Voltage Applied	GND -0.3V to VCC +0.3V
Storage Temperature	-65°C to +150°C

OPERATING RANGE

Operating Supply Voltage Commercial	4.75V to 5.25V
Operating Temperature Commercial	0°C to +75°C

ELECTRICAL CHARACTERISTICS

			TEMP. & VCC = OPERATING RANGE		TEMP = 25°C① VCC = 5.0V				
	SYMBOL	PARAMETER	MIN	MAX	MIN	TYP	MAX	UNITS	TEST CONDITIONS
D.C.	ICCSB	Standby Supply Current		500		100	500	μA	IO = 0 VI = VCC or GND
	ICCOP	Operating Supply Current ②		7		5	6	mA	f = 1MHz, IO = 0 VI = VCC or GND
	II	Input Leakage Current	-10.0	+10.0	-7.0	±0.5	+7.0	μA	GND ≤ VI ≤ VCC
	IOZ	Output Leakage Current	-10.0	+10.0	-7.0	±0.5	+7.0	μA	GND ≤ VO ≤ VCC
	VIL	Input Low Voltage	-0.3	0.8	-0.3	2.0	1.5	V	
	VIH	Input High Voltage	VCC -2.0	VCC +0.3	2.5	2.0	5.3	V	
	VOL	Output Low Voltage		0.4		0.25	0.35	V	IO = 1.6mA
	VOH	Output High Voltage	2.4		3.5	4.0		V	IO = -0.4mA
	CI	Input Capacitance ③		8.0		5.0	8.0	pF	f = 1MHz VI = VCC or GND
	CO	Output Capacitance ③		10.0		6.0	10.0	pF	f = 1MHz VO = VCC or GND
A.C.	TELQV	Chip Enable Access Time		350		200	300	ns	④
	TAVQV	Address Access Time		370		200	320	ns	④
	TELQX	Chip Enable Output Enable Time		100		50	80	ns	④
	TEHQZ	Chip Enable Output Disable Time		100		50	80	ns	④
	TELEH	Chip Enable Pulse Negative Width	350		300	200		ns	④
	TEHEL	Chip Enable Pulse Positive Width	150		120	100		ns	④
	TAVEL	Address Setup Time	20		20	0		ns	④
	TELAX	Address Hold Time	50		50	20		ns	④
	TWLWH	Write Enable Pulse Width	100		80	60		ns	④
	TWLEH	Write Enable Pulse Setup Time	250		200	100		ns	④
	TWLEL	Early Write Pulse Setup Time	0		0	-10		ns	④
	TWHEL	Write Enable Read Setup Time	0		0	-10		ns	④
	TELWH	Early Write Pulse Hold Time	100		80	60		ns	④
	TDVWL	Data Setup Time	30		20	0		ns	④
	TDVEL	Early Write Data Setup Time	30		20	0		ns	④
	TWLDX	Data Hold Time	100		80	60		ns	④
	TELDX	Early Write Data Hold Time	100		80	80		ns	④
	TELWL	Early Write Output Hi-Z Time	0		0	-10		ns	④
	TQVWL	Data Valid to Write Time	0		0	0		ns	④
	TELEL	Read or Write Cycle Time	500		420	300		ns	④

NOTES:
1. All devices tested at worst case limits. Room temp., 5 volt data provided for information – not guaranteed.
2. Operating Supply Current (ICCOP) is proportional to Operating Frequency. Example: Typical ICCOP = 5mA/MHz.
3. Capacitance sampled and guaranteed – not 100% tested.
4. AC test conditions: Inputs – TRISE = TFALL = 20nsec; Output – 1 TTL load and 50pF; All timing measured at ½ VCC.

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HM-6508

1024 x 1 CMOS RAM

Features

- LOW STANDBY POWER . . . . . 55μW MAX
- LOW OPERATING POWER . . . . . 22mW/MHz MAX
- FAST ACCESS TIME . . . . . 180nsec MAX
- DATA RETENTION VOLTAGE . . . . . 2.0 VOLTS MIN
- TTL COMPATIBLE IN/OUT
- HIGH OUTPUT DRIVE – 2 TTL LOADS
- HIGH NOISE IMMUNITY
- ON CHIP ADDRESS REGISTER
- MILITARY TEMPERATURE RANGE
- INDUSTRIAL TEMPERATURE RANGE
- THREE-STATE OUTPUTS
- 16 PIN PACKAGE FOR HIGH DENSITY

Description

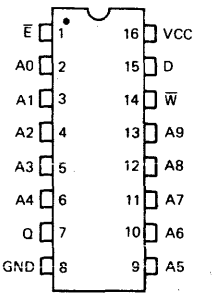
The HM-6508 is a 1024 by 1 static CMOS RAM fabricated using self-aligned silicon gate technology. Synchronous circuit design techniques are employed to achieve high performance and low power operation.

On chip latches are provided for address allowing efficient interfacing with microprocessor systems. The data output buffers can be forced to a high impedance state for use in expanded memory arrays.

The HM-6508 is a fully static RAM and may be maintained in any state for an indefinite period of time. Data retention supply voltage and supply current are guaranteed over temperature.

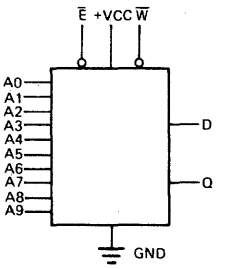
Pinout

TOP VIEW

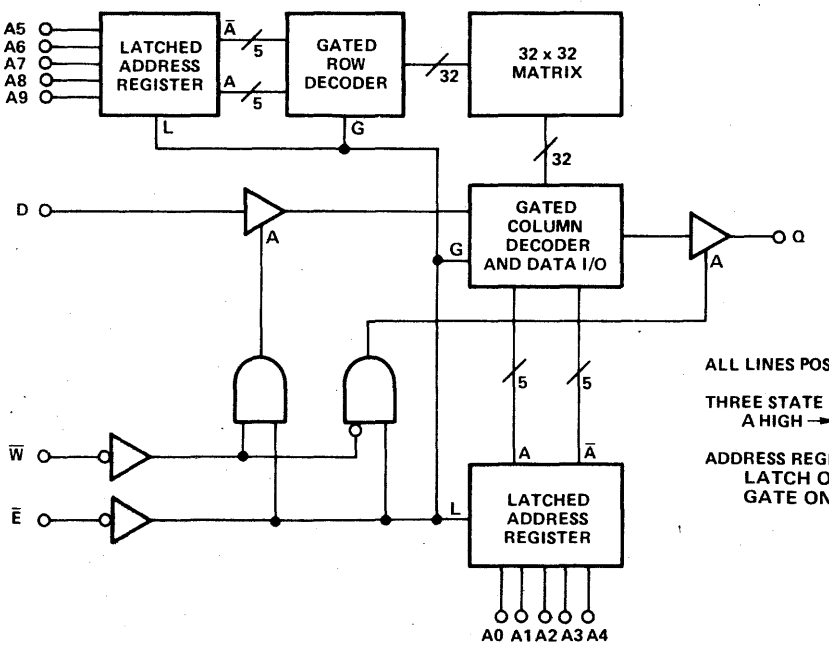


A – Address Input
Ē – Chip Enable
W̄ – Write Enable
D – Data Input
Q – Data Output

Logic Symbol



Functional Diagram



ALL LINES POSITIVE LOGIC – ACTIVE HIGH

THREE STATE BUFFERS:
A HIGH → OUTPUT ACTIVE

ADDRESS REGISTER AND DECODERS:
LATCH ON RISING EDGE OF L
GATE ON RISING EDGE OF G

"SEE PAGES 1409-1415 FOR PACKAGE SELECTION GUIDE"

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ABSOLUTE MAXIMUM RATINGS

Supply Voltage -VCC	+8.0V
Input or Output Voltage Applied	GND -0.3V to VCC +0.3V
Storage Temperature	-65°C to +150°C

OPERATING RANGE

Operating Supply Voltage -VCC	
Military (-2)	4.5V to 5.5V
Industrial (-9)	4.5V to 5.5V
Operating Temperature	
Military (-2)	-55°C to +125°C
Industrial (-9)	-40°C to +85°C

ELECTRICAL CHARACTERISTICS

	SYMBOL	PARAMETER	TEMP. & VCC = OPERATING RANGE MIN	TEMP. & VCC = OPERATING RANGE MAX	TEMP. = 25°C ① VCC = 5.0V MIN	TEMP. = 25°C ① VCC = 5.0V TYP	TEMP. = 25°C ① VCC = 5.0V MAX	UNITS	TEST CONDITIONS
D.C.	ICCSB	Standby Supply Current		10 1(+25°C)		0.1	1	μA	IO = 0 VI = VCC or GND
	ICCOP	Operating Supply Current ②		4		1.5	2.5	mA	f = 1MHz, IO = 0 VI = VCC or GND
	ICCDR	Data Retention Supply Current		10		0.01	1	μA	VCC = 3.0, IO = 0 VI = VCC or GND
	VCCDR	Data Retention Supply Voltage	2.0		2.0	1.4		V	
	II	Input Leakage Current	-1.0	+1.0	-0.5	0.0	+0.5	μA	GND ⩽ VI ⩽ VCC
	IOZ	Output Leakage Current	-1.0	+1.0	-0.5	0.0	+0.5	μA	GND ⩽ VO ⩽ VCC
	VIL	Input Low Voltage	-0.3	0.8	-0.3	2.0	1.5	V	
	VIH	Input High Voltage	VCC -2.0	VCC +0.3	2.5	2.0	5.3	V	
	VOL	Output Low Voltage		0.4		0.2	0.35	V	IOL = 3.2mA
	VOH	Output High Voltage	2.4		3.0	4.5		V	IOH = -0.4mA
	CI	Input Capacitance ③		6		4	6	pF	VI = VCC or GND f = 1MHz
	CO	Output Capacitance ③		10		6	10	pF	VO=VCC or GND f = 1MHz
A.C.	TELQV	Chip Enable Access Time		180		100	140	ns	④
	TAVQV	Address Access Time		180		90	140	ns	④
	TELQX	Chip Enable Output Enable Time		120		40	80	ns	④
	TWLQZ	Write Enable Output Disable Time		120		40	80	ns	④
	TEHQZ	Chip Enable Output Disable Time		120		40	80	ns	④
	TELEH	Chip Enable Pulse Negative Width	180		140	100		ns	④
	TEHEL	Chip Enable Pulse Positive Width	100		80	50		ns	④
	TAVEL	Address Setup Time	0		0	-10		ns	④
	TELAX	Address Hold Time	40		30	20		ns	④
	TDVWH	Data Setup Time	80		60	40		ns	④
	TWHDX	Data Hold Time	0		0	0		ns	④
	TWLEH	Chip Enable Write Pulse Setup Time	100		80	50		ns	④
	TELWH	Chip Enable Write Pulse Hold Time	100		80	50		ns	④
	TWLWH	Write Enable Pulse Width	100		80	50		ns	④
	TELEL	Read or Write Cycle Time	280		220	150		ns	④

NOTES:
1. All devices tested at worst case limits. Room temp., 5 volt data provided for information – not guaranteed.
2. Operating Supply Current (ICCOP) is proportional to Operating Frequency. Example: Typical ICCOP = 1.5mA/MHz.
3. Capacitance sampled and guaranteed – not 100% tested.
4. AC Test Conditions: Inputs – TRISE = TFALL = 20nsec; Outputs – 1 TTL load and 50pF. All timing measurements at 1/2 VCC.

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ABSOLUTE MAXIMUM RATINGS

Supply Voltage -VCC	+8.0V
Input or Output Voltage Applied	GND -0.3V to VCC +0.3V
Storage Temperature	-65°C to +150°C

OPERATING RANGE

Operating Supply Voltage -VCC	
Military (-2)	4.5V to 5.5V
Industrial (-9)	4.5V to 5.5V
Operating Temperature	
Military (-2)	-55°C to +125°C
Industrial (-9)	-40°C to +85°C

ELECTRICAL CHARACTERISTICS

	SYMBOL	PARAMETER	TEMP. & VCC = OPERATING RANGE MIN	TEMP. & VCC = OPERATING RANGE MAX	TEMP. = 25°C ① VCC = 5.0V MIN	TEMP. = 25°C ① VCC = 5.0V TYP	TEMP. = 25°C ① VCC = 5.0V MAX	UNITS	TEST CONDITIONS
D.C.	ICCSB	Standby Supply Current		10 1(+25°C)		1.0	1	μA	IO = 0 VI = VCC or GND
	ICCOP	Operating Supply Current ②		4		1.5	2.5	mA	f = 1MHz, IO = 0 VI = VCC or GND
	ICCDR	Data Retention Supply Current		10		0.1	1	μA	VCC = 3.0, IO = 0 VI = VCC or GND
	VCCDR	Data Retention Supply Voltage	2.0		2.0	1.4		V	
	II	Input Leakage Current	-1.0	+1.0	-0.5	0.0	+0.5	μA	GND ≤ VI ≤ VCC
	IOZ	Output Leakage Current	-1.0	+1.0	-0.5	0.0	+0.5	μA	GND ≤ VO ≤ VCC
	VIL	Input Low Voltage	-0.3	0.8	-0.3	2.0	1.5	V	
	VIH	Input High Voltage	VCC -2.0	VCC +0.3	2.5	2.0	5.3	V	
	VOL	Output Low Voltage		0.4		0.2	0.35	V	IOL = 3.2mA
	VOH	Output High Voltage	2.4		3.0	4.5		V	IOH = -0.4mA
	CI	Input Capacitance ③		6		4	6	pF	VI = VCC or GND f = 1MHz
	CO	Output Capacitance ③		10		6	10	pF	VO = VCC or GND f = 1MHz
A.C.	TELQV	Chip Enable Access Time		250		110	200	ns	④
	TAVQV	Address Access Time		250		100	200	ns	④
	TELQX	Chip Enable Output Enable Time		160		60	130	ns	④
	TWLQZ	Write Enable Output Disable Time		160		60	130	ns	④
	TEHQZ	Chip Enable Output Disable Time		160		60	130	ns	④
	TELEH	Chip Enable Pulse Negative Width	250		200	110		ns	④
	TEHEL	Chip Enable Pulse Positive Width	100		80	50		ns	④
	TAVEL	Address Setup Time	0		0	-10		ns	④
	TELAX	Address Hold Time	50		40	30		ns	④
	TDVWH	Data Setup Time	110		80	50		ns	④
	TWHDX	Data Hold Time	0		0	0		ns	④
	TWLEH	Chip Enable Write Pulse Setup Time	130		100	60		ns	④
	TELWH	Chip Enable Write Pulse Hold Time	130		100	60		ns	④
	TWLWH	Write Enable Pulse Width	130		100	60		ns	④
	TELEL	Read or Write Cycle Time	350		280	160		ns	④

NOTES:
1. All devices tested at worst case limits. Room temp., 5 volt data provided for information — not guaranteed.
2. Operating Supply Current (ICCOP) is proportional to Operating Frequency. Example: Typical ICCOP = 1.5mA/MHz.
3. Capacitance sampled and guaranteed — not 100% tested.
4. AC Test Conditions: Inputs — TRISE = TFALL = 20nsec; Outputs — 1 TTL load and 50pF. All timing measurements at 1/2 VCC.

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ABSOLUTE MAXIMUM RATINGS

Supply Voltage -VCC	+8.0V
Input or Output Voltage Applied	GND -0.3V to VCC +0.3V
Storage Temperature	-65°C to +150°C

OPERATING RANGE

Operating Supply Voltage -VCC Commercial	4.75V to 5.25V
Operating Temperature Commercial	0°C to +75°C

ELECTRICAL CHARACTERISTICS

	SYMBOL	PARAMETER	TEMP. & VCC = OPERATING RANGE MIN	TEMP. & VCC = OPERATING RANGE MAX	TEMP. = 25°C ① VCC = 5.0V MIN	TEMP. = 25°C ① VCC = 5.0V TYP	TEMP. = 25°C ① VCC = 5.0V MAX	UNITS	TEST CONDITIONS
D.C.	ICCSB	Standby Supply Current		100		10	100	μA	IO = 0 VI = VCC or GND
	ICCOP	Operating Supply Current ②		4		1.5	2.5	mA	f = 1MHz, IO = 0 VI = VCC or GND
	VCCDR	Data Retention Supply Voltage	2.0		2.0			V	
	II	Input Leakage Current	-1.0	+1.0	-0.5	0.0	+0.5	μA	GND ≤ VI ≤ VCC
	IOZ	Output Leakage Current	-1.0	+1.0	-0.5	0.0	+0.5	μA	GND ≤ VO ≤ VCC
	VIL	Input Low Voltage	-0.3	0.8	-0.3	2.0	1.5	V	
	VIH	Input High Voltage	VCC -2.0	VCC +0.3	2.5	2.0	5.3	V	
	VOL	Output Low Voltage		0.4		0.2	0.35	V	IOL = 1.6mA
	VOH	Output High Voltage	2.4		3.0	4.5		V	IOH = -0.2mA
	CI	Input Capacitance ③		6		4	6	pF	VI = VCC or GND f = 1MHz
	CO	Output Capacitance ③		10		6	10	pF	VO = VCC or GND f = 1MHz
A.C.	TELQV	Chip Enable Access Time		300		160	250	ns	④
	TAVQV	Address Access Time		310		160	260	ns	④
	TELQX	Chip Enable Output Enable Time		200		60	170	ns	④
	TWLQZ	Write Enable Output Disable Time		200		60	170	ns	④
	TEHQZ	Chip Enable Output Disable Time		200		60	170	ns	④
	TELEH	Chip Enable Pulse Negative Width	300		250	160		ns	④
	TEHEL	Chip Enable Pulse Positive Width	150		130	90		ns	④
	TAVEL	Address Setup Time	10		10	0		ns	④
	TELAX	Address Hold Time	70		50	40		ns	④
	TDVWH	Data Setup Time	130		100	80		ns	④
	TWHDX	Data Hold Time	0		0	0		ns	④
	TWLEH	Chip Enable Write Pulse Setup Time	160		130	100		ns	④
	TELWH	Chip Enable Write Pulse Hold Time	160		130	100		ns	④
	TWLWH	Write Enable Pulse Width	160		130	100		ns	④
	TELEL	Read or Write Cycle Time	450		380	250		ns	④

NOTES:
1. All devices tested at worst case limits. Room temp., 5 volt data provided for information — not guaranteed.
2. Operating Supply Current (ICCOP) is proportional to Operating Frequency. Example: Typical ICCOP = 1.5mA/MHz.
3. Capacitance sampled and guaranteed — not 100% tested.
4. AC Test Conditions: Inputs — TRISE = TFALL = 20nsec; Outputs — 1 TTL load and 50pF. All timing measurements at 1/2 VCC.

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HM-6512

64 x 12 CMOS RAM

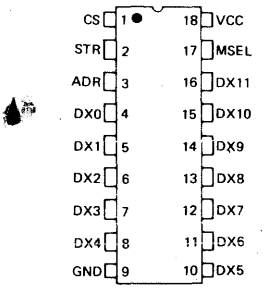
Preliminary

Features

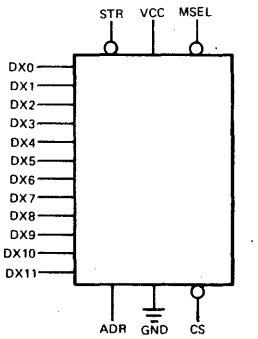
- LOW POWER STANDBY . . . . . 1mW MAX.
- LOW POWER OPERATION. . . . . .22mW/MHz MAX.
- DATA RETENTION . . . . . @ 2.0V MIN.
- TTL COMPATIBLE INPUT/OUTPUT
- TWO HM-6512's CAN BE USED WITH HM-6100 AND HM-6312 WITHOUT ADDITIONAL COMPONENTS
- THREE STATE OUTPUTS
- FAST ACCESS TIME . . . . . .250nsec MAX.
- MILITARY AND INDUSTRIAL TEMPERATURE RANGE
- 18 PIN PACKAGE FOR HIGH DENSITY
- ON CHIP ADDRESS REGISTER

Pinout

TOP VIEW



Logic Symbol



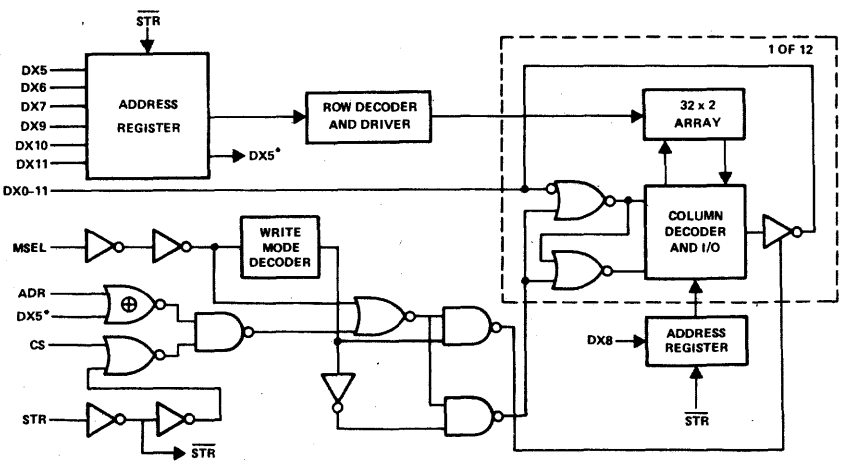
CS — Chip Select
STR — Chip Enable
MSEL — Enable and R/W Decode
ADR — Address Decode
DX — Address Input and Data I/O

Description

The HM-6512 is a high speed, low power, silicon gate CMOS 768 bit static RAM organized 64 words by 12 bits. In all static states these units exhibit the microwatt power requirements typical of CMOS. Inputs and three state outputs are TTL compatible. The basic part operates at 4-7 volts with a typical 5 volt, 25°C access time of 150ns.

Signal polarities and functions are specified for direct interfacing with the HM-6100 microprocessor. The device is ideally suited for minimum system all CMOS applications where low power, minimum cost, or non-volatility is required.

Functional Diagram



"SEE PAGES 1409-1415 FOR PACKAGE SELECTION GUIDE"

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ABSOLUTE MAXIMUM RATINGS

Supply Voltage	8.0V
Input or Output Voltage Applied	GND -0.3V to VCC +0.3V
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	
Industrial HM-6512-9	-40°C to +85°C
Military HM-6512-2	-55°C to +125°C

ELECTRICAL CHARACTERISTICS VCC = 5.0V ±10%, TA = Industrial or Military

	SYMBOL	PARAMETER	MINIMUM	TYPICAL	MAXIMUM	UNITS	TEST CONDITIONS
D.C.	VIH	Logical "1" Input Voltage	VCC -2.0			V	
	VIL	Logical "0" Input Voltage			0.8	V	
	IIL	Input Leakage	-1.0		+1.0	μA	0V ≤ VIN ≤ VCC
	VOH	Logical "1" Output Voltage	2.4			V	IOH = -0.2mA
	VOL	Logical "0" Output Voltage			0.45	V	IOL = 2.0mA
	IO	Output Leakage	-1.0		+1.0	μA	0V ≤ VO ≤ VCC
	ICCSB	Supply Current Standby		1.0	100	μA	STR = VCC = 5.5V VIN = VCC or GND
	ICCDR	Supply Current Data Retention		0.1	50	μA	STR = VCC = 3.0V VIN = VCC or GND
	CI	Input Capacitance		5.0	7.0	pF	
	CIO*	Input/Output Capacitance		6.0	10.0	pF	
A.C.	TAC	Access Time from STR			250	ns	CL = 50pF See Figures 1 & 2
	TEN	Output Enable Time			200	ns	
	TDIS	Output Disable Time			200	ns	
	TSTR	STR Pulse Width (Positive)	200			ns	
	$\overline{\text{TSTR}}$	STR Pulse Width (Negative)	250			ns	
	TC	Cycle Time	450			ns	
	TWP	Write Pulse Width (Negative)	130			ns	
	TAS	Address Setup Time	30			ns	
	TAH	Address Hold Time	50			ns	
	TDS	Data Setup Time	130			ns	
	TDH	Data Hold Time	0			ns	
	TPS	MSEL Pulse Separation	150			ns	
	TMS	MSEL Setup Time	50			ns	
	TMH	MSEL Hold Time	50			ns	

*Guaranteed but not 100% tested.

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ABSOLUTE MAXIMUM RATINGS

Supply Voltage	7.0V
Input or Output Voltage Applied	GND -0.3V to VCC +0.3V
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	
Industrial HM-6512C-9	-40°C to +85°C

ELECTRICAL CHARACTERISTICS VCC = 5.0V ±5%, TA = Industrial

	SYMBOL	PARAMETER	MINIMUM	TYPICAL	MAXIMUM	UNITS	TEST CONDITIONS
D.C.	VIH	Logical "1" Input Voltage	VCC -1.5			V	
	VIL	Logical "0" Input Voltage			0.8	V	
	IIL	Input Leakage	-5.0		+5.0	μA	0V ≤ VIN ≤ VCC
	VOH	Logical "1" Output Voltage	2.4			V	IOH = -0.2mA
	VOL	Logical "0" Output Voltage			0.45	V	IOL = 1.6mA
	IO	Output Leakage	-5.0		+5.0	μA	0V ≤ VO ≤ VCC
	ICCSB	Supply Current Standby			800	μA	STR = VCC = 5.25V VIN = VCC or GND
	CIN*	Input Capacitance		5.0	7.0	pF	
	CIO*	Input/Output Capacitance		6.0	10.0	pF	
A.C.	TAC	Access Time from STR			400	ns	CL = 50pF See Figures 1 & 2
	TEN	Output Enable Time			300	ns	
	TDIS	Output Disable Time			300	ns	
	TSTR	STR Pulse Width (Positive)	250			ns	
	$T\overline{STR}$	STR Pulse Width (Negative)	400			ns	
	TC	Cycle Time	650			ns	
	TWP	Write Pulse Width (Negative)	200			ns	
	TAS	Address Setup Time	60			ns	
	TAH	Address Hold Time	100			ns	
	TDS	Data Setup Time	200			ns	
	TDH	Data Hold Time	0			ns	
	TPS	MSEL Pulse Separation	150			ns	
	TMS	MSEL Setup Time	100			ns	
	TMH	MSEL Hold Time	100			ns	

*Guaranteed but not 100% tested.

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HM-6513

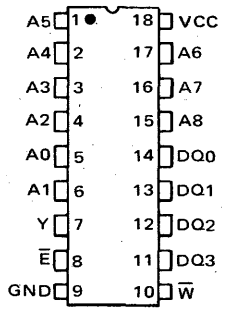
512 x 4 CMOS RAM

Features

- LOW POWER STANDBY . . . . . ≪1mW MAX.
- LOW POWER OPERATION. . . . . 35mW/MHz MAX.
- DATA RETENTION . . . . . @ 2.0V MIN.
- TTL COMPATIBILITY INPUT/OUTPUT
- COMMON DATA IN/OUT
- THREE STATE OUTPUTS
- FAST ACCESS TIME . . . . . 300nsec MAX.
- INDUSTRIAL OR COMMERCIAL TEMPERATURE RANGE
- 18 PIN PACKAGE FOR HIGH DENSITY
- ON CHIP ADDRESS REGISTER
- PINOUT ALLOWS UPGRADE TO HM-6514

Pinout

TOP VIEW



Description

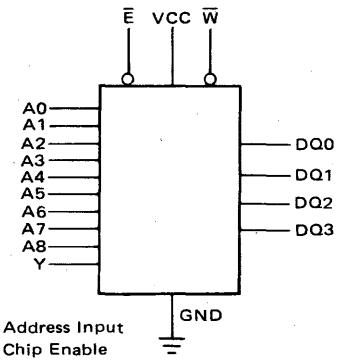
The HM-6513 is a 512 x 4 static CMOS RAM fabricated using self aligned silicon gate technology. The device utilizes synchronous circuitry to achieve high performance and low power operation.

On chip latches are provided for the addresses allowing efficient interfacing with microprocessor systems. The data output can be forced to a high impedance state for use in expanded memory systems.

The HM-6513 is a fully static RAM and may be maintained in any state for an indefinite period of time. Data retention supply voltage and supply current are guaranteed over temperature.

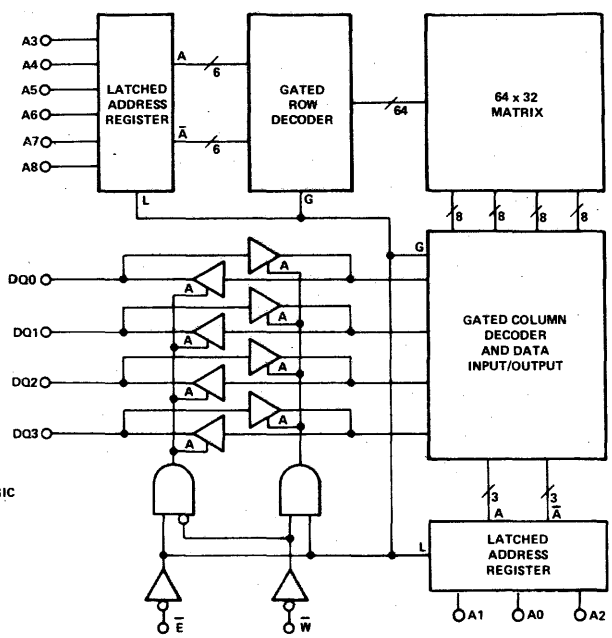
The HM-6513 is supplied in two versions, the HM-6513H and the HM-6513L. The H or L is used to designate the logic level to be connected to the Y input. If a HM-6513H is procured the user must connect the input to VCC in the system. If a HM-6513L is used the Y input must be connected to system ground.

Logic Symbol



A – Address Input
$\overline{E}$ – Chip Enable
$\overline{W}$ – Write Enable
DQ – Data In/Out
Y – Hard Wired Input

Functional Diagram



ALL LINES ACTIVE HIGH – POSITIVE LOGIC

THREE STATE BUFFERS:
A HIGH → OUTPUT ACTIVE

ADDRESS REGISTERS:
LATCH ON RISING EDGE OF L

GATED DECODERS:
GATE ON RISING EDGE OF G

"SEE PAGES 1409-1415 FOR PACKAGE SELECTION GUIDE"

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ABSOLUTE MAXIMUM RATINGS

Supply Voltage – VCC	+8.0V
Input or Output Voltage Applied	GND -0.3V to VCC +0.3V
Storage Temperature	-65°C to +150°C

OPERATING RANGE

Operating Supply Voltage Industrial (-9)	4.5V to 5.5V
Operating Temperature Industrial (-9)	-40°C to +85°C

ELECTRICAL CHARACTERISTICS

			TEMP. & VCC = OPERATING RANGE		TEMP = 25°C ① VCC = 5.0V				
	SYMBOL	PARAMETER	MIN	MAX	MIN	TYP	MAX	UNITS	TEST CONDITIONS
D.C.	ICCSB	Standby Supply Current		50		0.1	10	μA	IO = 0 VI = VCC or GND
	ICCOP	Operating Supply Current ②		7		5	6	mA	f = 1MHz, IO = 0 VI = VCC or GND
	ICCDR	Data Retention Supply Current		25		0.01	5	μA	IO = 0 VCC = 3.0 VI = VCC or GND
	VCCDR	Data Retention Supply Voltage	2.0		2.0	1.4		V	
	II	Input Leakage Current	-1.0	+1.0	-0.5	0.0	+0.5	μA	GND ≤ VI ≤ VCC
	IIOZ	Input/Output Leakage Current	-1.0	+1.0	-0.5	0.0	+0.5	μA	GND ≤ VIO ≤ VCC
	VIL	Input Low Voltage	-0.3	0.8	-0.3	2.0	1.5	V	
	VIH	Input High Voltage	VCC -2.0	VCC +0.3	2.5	2.0	5.3	V	
	VOL	Output Low Voltage		0.45		0.35	0.4	V	IO = 2.0mA
	VOH	Output High Voltage	2.4		3.5	4.0		V	IO = -1.0mA
	CI	Input Capacitance ③		8.0		5.0	8.0	pF	VI = VCC or GND f = 1MHz
	CIO	Input/Output Capacitance ③		10.0		6.0	10.0	pF	VIO = VCC or GND f = 1MHz
A.C.	TELQV	Chip Enable Access Time		300		170	250	ns	④
	TAVQV	Address Access Time		320		170	270	ns	④
	TELQX	Chip Enable Output Enable Time		100		50	80	ns	④
	TWLQZ	Write Enable Output Disable Time		100		50	80	ns	④
	TEHQZ	Chip Enable Output Disable Time		100		50	80	ns	④
	TELEH	Chip Enable Pulse Negative Width	300		250	170		ns	④
	TEHEL	Chip Enable Pulse Positive Width	120		100	70		ns	④
	TAVEL	Address Setup Time	20		20	0		ns	④
	TELAX	Address Hold Time	50		50	20		ns	④
	TWLWH	Write Enable Pulse Width	300		240	150		ns	④
	TWLEH	Write Enable Pulse Setup Time	300		240	150		ns	④
	TELWH	Write Enable Pulse Hold Time	300		240	150		ns	④
	TDVWH	Data Setup Time	200		160	100		ns	④
	TWHDZ	Data Hold Time	0		0	-10		ns	④
	TWHEL	Write Enable Read Setup Time	0		0	-10		ns	④
	TQVWL	Data Valid to Write Time	0		0	-10		ns	④
	TWLDV	Write Data Delay Time	100		80	50		ns	④
	TWLEL	Early Output High-Z Time	0		0	−10		ns	④
	TEHWH	Late Output High-Z Time	0		0	−10		ns	④
	TELEL	Read or Write Cycle Time	420		350	240		ns	④

NOTES:
1. All devices tested at worst case limits. Room temp., 5 volt data provided for information – not guaranteed.
2. Operating Supply Current (ICCOP) is proportional to Operating Frequency. Example: Typical ICCOP = 5mA/MHz.
3. Capacitance sampled and guaranteed – not 100% tested.
4. AC test conditions: Inputs – TRISE = TFALL = 20nsec; Outputs – 1 TTL load and 50pF; All timing measured at ½ VCC.

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ABSOLUTE MAXIMUM RATINGS

Supply Voltage – VCC	+8.0V
Input or Output Voltage Applied	GND -0.3V to VCC +0.3V
Storage Temperature	-65°C to +150°C

OPERATING RANGE

Operating Supply Voltage Commercial	4.75V to 5.25V
Operating Temperature Commercial	0°C to +75°C

ELECTRICAL CHARACTERISTICS

			TEMP. & VCC = OPERATING RANGE		TEMP = 25°C ① VCC = 5.0V				
	SYMBOL	PARAMETER	MIN	MAX	MIN	TYP	MAX	UNITS	TEST CONDITIONS
D.C.	ICCSB	Standby Supply Current		500		100	500	μA	VI = VCC or GND
	ICCOP	Operating Supply Current ②		7		5	6	mA	f = 1MHz, IO = 0 VI = VCC or GND
	II	Input Leakage Current	-10.0	+10.0	-7.0	±0.5	+7.0	μA	GND ≤ VI ≤ VCC
	IIOZ	Input/Output Leakage Current	-10.0	+10.0	-7.0	±0.5	+7.0	μA	GND ≤ VIO ≤ VCC
	VIL	Input Low Voltage	-0.3	0.8	-0.3	2.0	1.5	V	
	VIH	Input High Voltage	VCC -2.0	VCC +0.3	2.5	2.0	5.3	V	
	VOL	Output Low Voltage		0.45		0.35	0.4	V	IO = 1.6mA
	VOH	Output High Voltage	2.4		3.5	4.0		V	IO = -0.4mA
	CI	Input Capacitance ③		8.0		5.0	8.0	pF	VI = VCC or GND f = 1MHz
	CIO	Input/Output Capacitance ③		10.0		6.0	10.0	pF	VIO = VCC or GND f = 1MHz
A.C.	TELQV	Chip Enable Access Time		350		200	300	ns	④
	TAVQV	Address Access Time		370		200	320	ns	④
	TELQX	Chip Enable Output Enable Time		100		50	80	ns	④
	TWLQZ	Write Enable Output Disable Time		100		50	80	ns	④
	TEHQZ	Chip Enable Output Disable Time		100		50	80	ns	④
	TELEH	Chip Enable Pulse Negative Width	350		300	200		ns	④
	TEHEL	Chip Enable Pulse Positive Width	150		120	100		ns	④
	TAVEL	Address Setup Time	20		20	0		ns	④
	TELAX	Address Hold Time	50		50	20		ns	④
	TWLWH	Write Enable Pulse Width	350		300	200		ns	④
	TWLEH	Write Enable Pulse Setup Time	350		300	200		ns	④
	TELWH	Write Enable Pulse Hold Time	350		300	200		ns	④
	TDVWH	Data Setup Time	250		220	150		ns	④
	TWHDZ	Data Hold Time	0		0	-10		ns	④
	TWHEL	Write Enable Read Setup Time	0		0	-10		ns	④
	TDVWL	Output Data Valid to Write Time	0		0	-10		ns	④
	TWLDV	Write Data Delay Time	100		80	50		ns	④
	TWLEL	Early Output High-Z Time	0		0	–10		ns	④
	TEHWH	Late Output High-Z Time	0		0	–10		ns	④
	TELEL	Read or Write Cycle Time	500		420	320		ns	④

NOTES:
1. All devices tested at worst case limits. Room temp., 5 volt data provided for information – not guaranteed.
2. Operating Supply Current (ICCOP) is proportional to Operating Frequency. Example: Typical ICCOP = 5mA/MHz.
3. Capacitance sampled and guaranteed – not 100% tested.
4. AC test conditions: Inputs – TRISE = TFALL = 20nsec; Outputs – 1 TTL load and 50pF; All timing measured at ½ VCC.

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HM-6514

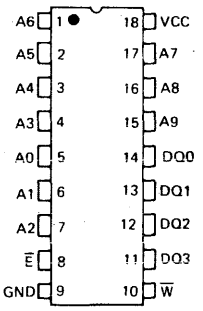
1024 x 4 CMOS RAM

Features

- LOW POWER STANDBY . . . . . ≪ 1mW MAX.
- LOW POWER OPERATION. . . . . 35mW/MHz MAX.
- DATA RETENTION . . . . . @ 2.0V MIN.
- TTL COMPATIBLE INPUT/OUTPUT
- COMMON DATA IN/OUT
- THREE-STATE OUTPUTS
- STANDARD JEDEC PINOUT
- FAST ACCESS TIME . . . . . 300nsec MAX.
- MILITARY TEMPERATURE RANGE
- INDUSTRIAL TEMPERATURE RANGE
- 18 PIN PACKAGE FOR HIGH DENSITY
- ON CHIP ADDRESS REGISTER

Pinout

TOP VIEW



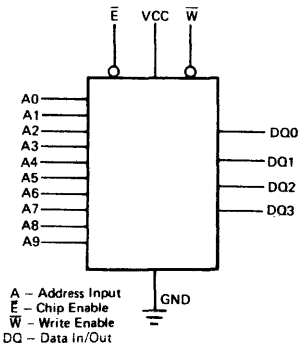
Description

The HM-6514 is a 1024 x 4 static CMOS RAM fabricated using self aligned silicon gate technology. The device utilizes synchronous circuitry to achieve high performance and low power operation.

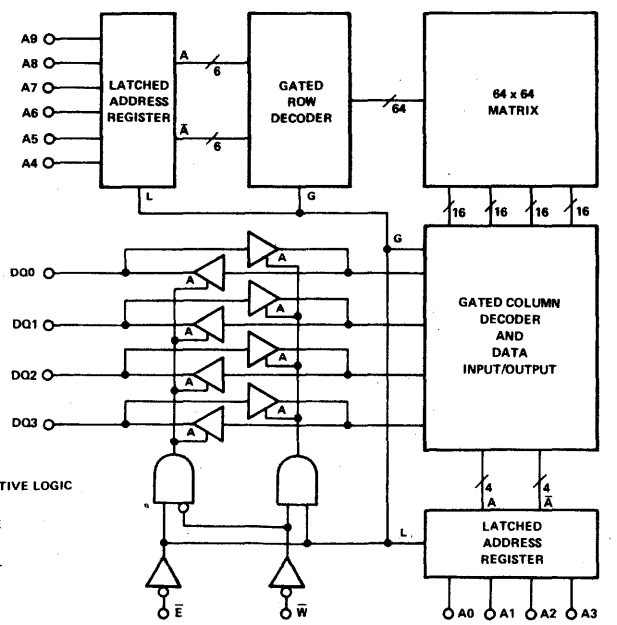
On chip latches are provided for the addresses allowing efficient interfacing with microprocessor systems. The data output can be forced to a high impedance state for use in expanded memory systems.

The HM-6514 is a fully static RAM and may be maintained in any state for an indefinite period of time. Data retention supply voltage and supply current are guaranteed over temperature.

Logic Symbol



Functional Diagram



ALL LINES ACTIVE HIGH – POSITIVE LOGIC
THREE STATE BUFFERS:
A HIGH → OUTPUT ACTIVE
ADDRESS REGISTERS:
LATCH ON RISING EDGE OF L
GATED DECODERS:
GATE ON RISING EDGE OF G

"SEE PAGES 1409-1415 FOR PACKAGE SELECTION GUIDE"

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ABSOLUTE MAXIMUM RATINGS

Supply Voltage – VCC	+8.0V
Input or Output Voltage Applied	GND -0.3V to VCC +0.3V
Storage Temperature	-65°C to +150°C

OPERATING RANGE

Operating Supply Voltage	
Military (-2)	4.5V to 5.5V
Industrial (-9)	4.5V to 5.5V
Operating Temperature	
Military (-2)	-55°C to +125°C
Industrial (-9)	-40°C to +85°C

ELECTRICAL CHARACTERISTICS

	SYMBOL	PARAMETER	TEMP. & VCC = OPERATING RANGE MIN	TEMP. & VCC = OPERATING RANGE MAX	TEMP = 25°C ① VCC = 5.0V MIN	TEMP = 25°C ① VCC = 5.0V TYP	TEMP = 25°C ① VCC = 5.0V MAX	UNITS	TEST CONDITIONS
D.C.	ICCSB	Standby Supply Current		50		0.1	10	μA	IO = 0 VI = VCC or GND
	ICCOP	Operating Supply Current ②		7		5	6	mA	f = 1MHz, IO = 0 VI = VCC or GND
	ICCDR	Data Retention Supply Current		25		0.01	5	μA	IO = 0 VCC = 3.0 VI = VCC or GND
	VCCDR	Data Retention Supply Voltage	2.0		2.0	1.4		V	
	II	Input Leakage Current	-1.0	+1.0	-0.5	0.0	+0.5	μA	GND ≤ VI ≤ VCC
	IIOZ	Input/Output Leakage Current	-1.0	+1.0	-0.5	0.0	+0.5	μA	GND ≤ VO ≤ VCC
	VIL	Input Low Voltage	-0.3	0.8	-0.3	2.0	1.5	V	
	VIH	Input High Voltage	VCC -2.0	VCC +0.3	2.5	2.0	5.3	V	
	VOL	Output Low Voltage		0.45		0.35	0.4	V	IO = 2.0mA
	VOH	Output High Voltage	2.4		3.5	4.0		V	IO = -1.0mA
	CI	Input Capacitance ③		8.0		5.0	8.0	pF	VI = VCC or GND f = 1MHz
	CIO	Input/Output Capacitance ③		10.0		6.0	10.0	pF	VO = VCC or GND f = 1MHz
A.C.	TELQV	Chip Enable Access Time		300		170	250	ns	④
	TAVQV	Address Access Time		320		170	270	ns	④
	TELQX	Chip Enable Output Enable Time		100		50	80	ns	④
	TWLQZ	Write Enable Output Disable Time		100		50	80	ns	④
	TEHQZ	Chip Enable Output Disable Time		100		50	80	ns	④
	TELEH	Chip Enable Pulse Negative Width	300		250	170		ns	④
	TEHEL	Chip Enable Pulse Positive Width	120		100	70		ns	④
	TAVEL	Address Setup Time	20		20	0		ns	④
	TELAX	Address Hold Time	50		50	20		ns	④
	TWLWH	Write Enable Pulse Width	300		240	150		ns	④
	TWLEH	Write Enable Pulse Setup Time	300		240	150		ns	④
	TELWH	Write Enable Pulse Hold Time	300		240	150		ns	④
	TDVWH	Data Setup Time	200		160	100		ns	④
	TWHDZ	Data Hold Time	0		0	0		ns	④
	TWHEL	Write Enable Read Setup Time	0		0	0		ns	④
	TQVWL	Data Valid to Write Time	0		0	0		ns	④
	TWLDV	Write Data Delay Time	100		80	50		ns	④
	TWLEL	Early Output High-Z Time	0		0	-10		ns	④
	TEHWH	Late Output High-Z Time	0		0	-10		ns	④
	TELEL	Read or Write Cycle Time	420		350	240		ns	④

NOTES:
1. All devices tested at worst case limits. Room temp., 5 volt data provided for information – not guaranteed.
2. Operating Supply Current (ICCOP) is proportional to Operating Frequency. Example: Typical ICCOP = 5mA/MHz.
3. Capacitance sampled and guaranteed – not 100% tested.
4. AC test conditions: Inputs – TRISE = TFALL = 20nsec; Outputs – 1 TTL load and 50pF; All timing measured at ½ VCC.

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ABSOLUTE MAXIMUM RATINGS

Supply Voltage – VCC	+8.0V
Input or Output Voltage Applied	GND -0.3V to VCC +0.3V
Storage Temperature	-65°C to +150°C

OPERATING RANGE

Operating Supply Voltage Commercial	4.75V to 5.25V
Operating Temperature Commercial	0°C to +75°C

ELECTRICAL CHARACTERISTICS

			TEMP. & VCC = OPERATING RANGE		TEMP = 25°C ① VCC = 5.0V				
	SYMBOL	PARAMETER	MIN	MAX	MIN	TYP	MAX	UNITS	TEST CONDITIONS
D.C.	ICCSB	Standby Supply Current		500		100	500	μA	VI = VCC or GND
	ICCOP	Operating Supply Current ②		7		5	6	mA	f = 1MHz, IO = 0 VI = VCC or GND
	II	Input Leakage Current	-10.0	+10.0	-7.0	±0.5	+7.0	μA	GND ≤ VI ≤ VCC
	IIOZ	Input/Output Leakage Current	-10.0	+10.0	-7.0	±0.5	+7.0	μA	GND ≤ VO ≤ VCC
	VIL	Input Low Voltage	-0.3	0.8	-0.3	2.0	1.5	V	
	VIH	Input High Voltage	VCC -2.0	VCC +0.3	2.5	2.0	5.3	V	
	VOL	Output Low Voltage		0.45		0.35	0.4	V	IO = 1.6mA
	VOH	Output High Voltage	2.4		3.5	4.0		V	IO = -0.4mA
	CI	Input Capacitance ③		8.0		5.0	8.0	pF	VI = VCC or GND f = 1MHz
	CIO	Input/Output Capacitance ③		10.0		6.0	10.0	pF	VO = VCC or GND f = 1MHz
A.C.	TELQV	Chip Enable Access Time		350		200	300	ns	④
	TAVQV	Address Access Time		370		200	320	ns	④
	TELQX	Chip Enable Output Enable Time		100		50	80	ns	④
	TWLQZ	Write Enable Output Disable Time		100		50	80	ns	④
	TEHQZ	Chip Enable Output Disable Time		100		50	80	ns	④
	TELEH	Chip Enable Pulse Negative Width	350		300	200		ns	④
	TEHEL	Chip Enable Pulse Positive Width	150		120	100		ns	④
	TAVEL	Address Setup Time	20		20	0		ns	④
	TELAX	Address Hold Time	50		50	20		ns	④
	TWLWH	Write Enable Pulse Width	350		300	200		ns	④
	TWLEH	Write Enable Pulse Setup Time	350		300	200		ns	④
	TELWH	Write Enable Pulse Hold Time	350		300	200		ns	④
	TDVWH	Data Setup Time	250		220	150		ns	④
	TWHDZ	Data Hold Time	0		0	0		ns	④
	TWHEL	Write Enable Read Setup Time	0		0	0		ns	④
	TDVWL	Output Data Valid to Write Time	0		0	0		ns	④
	TWLDV	Write Data Delay Time	100		80	50		ns	④
	TWLEL	Early Output High-Z Time	0		0	-10		ns	④
	TEHWH	Late Output High-Z Time	0		0	-10		ns	④
	TELEL	Read or Write Cycle Time	500		420	320		ns	④

NOTES:
1. All devices tested at worst case limits. Room temp., 5 volt data provided for information – not guaranteed.
2. Operating Supply Current (ICCOP) is proportional to Operating Frequency. Example: Typical ICCOP = 5mA/MHz.
3. Capacitance sampled and guaranteed – not 100% tested.
4. AC test conditions: Inputs – TRISE = TFALL = 20nsec; Outputs – 1 TTL load and 50pF; All timing measured at ½ VCC.

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HM-6518

1024 x 1 CMOS RAM

Features

- LOW STANDBY POWER . . . . . 55μW MAX
- LOW OPERATING POWER . . . . . 22mW/MHz MAX
- FAST ACCESS TIME . . . . . 180nsec MAX
- DATA RETENTION VOLTAGE . . . . . 2.0 VOLTS MIN
- TTL COMPATIBLE IN/OUT
- HIGH OUTPUT DRIVE - 2 TTL LOADS
- HIGH NOISE IMMUNITY
- ON CHIP ADDRESS REGISTER
- TWO CHIP SELECTS FOR EASY ARRAY EXPANSION
- THREE STATE OUTPUTS
- MILITARY TEMPERATURE RANGE
- INDUSTRIAL TEMPERATURE RANGE

Description

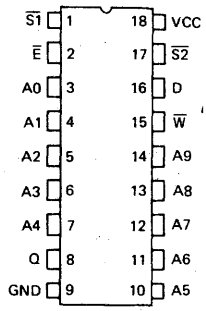
The HM-6518 is a 1024 by 1 static CMOS RAM fabricated using self-aligned silicon gate technology. Synchronous circuit design techniques are employed to achieve high performance and low power operation.

On chip latches are provided for address and data outputs allowing efficient interfacing with microprocessor systems. The data output buffers can be forced to a high impedance state for use in expanded memory arrays.

The HM-6518 is a fully static RAM and may be maintained in any state for an indefinite period of time. Data retention supply voltage and supply current are guaranteed over temperature.

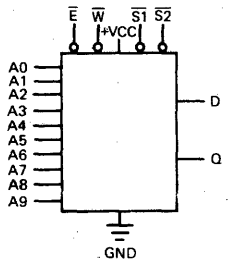
Pinout

TOP VIEW

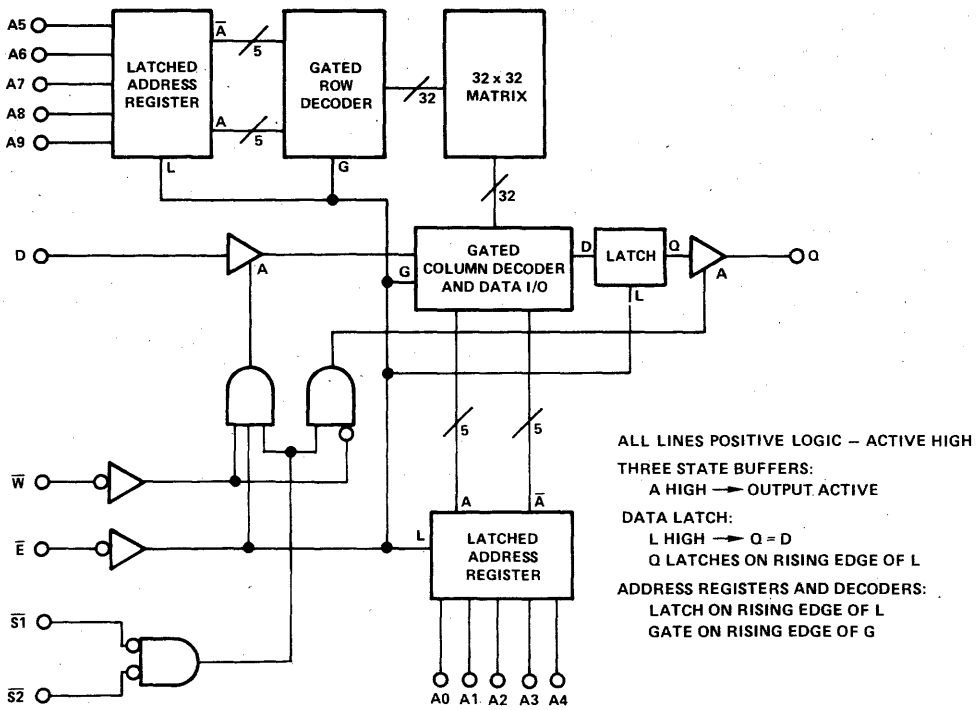


A - ADDRESS INPUT
E - CHIP ENABLE
S - CHIP SELECT
W - WRITE ENABLE
D - DATA INPUT
Q - DATA OUTPUT

Logic Symbol



Functional Diagram



ALL LINES POSITIVE LOGIC – ACTIVE HIGH

THREE STATE BUFFERS:
A HIGH → OUTPUT ACTIVE

DATA LATCH:
L HIGH → Q = D
Q LATCHES ON RISING EDGE OF L

ADDRESS REGISTERS AND DECODERS:
LATCH ON RISING EDGE OF L
GATE ON RISING EDGE OF G

"SEE PAGES 1409-1415 FOR PACKAGE SELECTION GUIDE"

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ABSOLUTE MAXIMUM RATINGS

Supply Voltage -VCC	+8.0V
Input or Output Voltage Applied	GND -0.3V to VCC +0.3V
Storage Temperature	-65°C to +150°C

OPERATING RANGE

Operating Supply Voltage -VCC	
Military (-2)	4.5V to 5.5V
Industrial (-9)	4.5V to 5.5V
Operating Temperature	
Military (-2)	-55°C to +125°C
Industrial (-9)	-40°C to +85°C

ELECTRICAL CHARACTERISTICS

	SYMBOL	PARAMETER	TEMP. & VCC = OPERATING RANGE MIN	TEMP. & VCC = OPERATING RANGE MAX	TEMP. = 25°C ① VCC = 5.0V MIN	TEMP. = 25°C ① VCC = 5.0V TYP	TEMP. = 25°C ① VCC = 5.0V MAX	UNITS	TEST CONDITIONS
D.C.	ICCSB	Standby Supply Current		10 1(+25°C)		0.1	1	μA	IO = 0 VI = VCC or GND
	ICCOP	Operating Supply Current ②		4		1.5	2.5	mA	f = 1MHz, IO = 0 VI = VCC or GND
	ICCDR	Data Retention Supply Current		10		0.01	1	μA	VCC = 3.0, IO = 0 VI = VCC or GND
	VCCDR	Data Retention Supply Voltage	2.0		2.0	1.4		V	
	II	Input Leakage Current	-1.0	+1.0	-0.5	0.0	+0.5	μA	GND ≤ VI ≤ VCC
	IOZ	Output Leakage Current	-1.0	+1.0	-0.5	0.0	+0.5	μA	GND ≤ VO ≤ VCC
	VIL	Input Low Voltage	-0.3	0.8	-0.3	2.0	1.5	V	
	VIH	Input High Voltage	VCC -2.0	VCC +0.3	2.5	2.0	5.3	V	
	VOL	Output Low Voltage		0.4		0.2	0.35	V	IOL = 3.2mA
	VOH	Output High Voltage	2.4		3.0	4.5		V	IOH = -0.4mA
	CI	Input Capacitance ③		6		4	6	pF	VI = VCC or GND f = 1MHz
	CO	Output Capacitance ③		10		6	10	pF	VO= VCC or GND f = 1MHz
A.C.	TELQV	Chip Enable Access Time		180		100	140	ns	④
	TAVQV	Address Access Time		180		90	140	ns	④
	TSLQX	Chip Select Output Enable Time		120		40	80	ns	④
	TWLQX	Write Enable Output Disable Time		120		40	80	ns	④
	TSHQX	Chip Select Output Disable Time		120		40	80	ns	④
	TELEH	Chip Enable Pulse Negative Width	180		140	100		ns	④
	TEHEL	Chip Enable Pulse Positive Width	100		80	50		ns	④
	TAVEL	Address Setup Time	0		0	-10		ns	④
	TELAX	Address Hold Time	40		30	20		ns	④
	TDVWH	Data Setup Time	80		50	30		ns	④
	TWHDX	Data Hold Time	0		0	0		ns	④
	TWLSH	Chip Select Write Pulse Setup Time	100		80	50		ns	④
	TWLEH	Chip Enable Write Pulse Setup Time	100		80	50		ns	④
	TSLWH	Chip Select Write Pulse Hold Time	100		80	50		ns	④
	TELWH	Chip Enable Write Pulse Hold Time	100		80	50		ns	④
	TWLWH	Write Enable Pulse Width	100		80	50		ns	④
	TELEL	Read or Write Cycle Time	280		220	150		ns	④

NOTES
1. All devices tested at worst case limits. Room temp., 5 volt data provided for information — not guaranteed.
2. Operating Supply Current (ICCOP) is proportional to Operating Frequency. Example: Typical ICCOP = 1.5mA/MHz.
3. Capacitance sampled and guaranteed — not 100% tested.
4. AC Test Conditions: Inputs — TRISE = TFALL = 20nsec; Outputs — 1 TTL load and 50pF. All timing measurements at 1/2 VCC.

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ABSOLUTE MAXIMUM RATINGS		OPERATING RANGE	
Supply Voltage -VCC	+8.0V	Operating Supply Voltage -VCC	
Input or Output Voltage Applied	GND -0.3V to VCC +0.3V	Military (-2)	4.5V to 5.5V
		Industrial (-9)	4.5V to 5.5V
Storage Temperature	-65°C to +150°C	Operating Temperature	
		Military (-2)	-55°C to +125°C
		Industrial (-9)	-40°C to +85°C

ELECTRICAL CHARACTERISTICS

	SYMBOL	PARAMETER	TEMP. & VCC = OPERATING RANGE MIN	TEMP. & VCC = OPERATING RANGE MAX	TEMP. = 25°C ① VCC = 5.0V MIN	TEMP. = 25°C ① VCC = 5.0V TYP	TEMP. = 25°C ① VCC = 5.0V MAX	UNITS	TEST CONDITIONS
D.C.	ICCSB	Standby Supply Current		10 1(+25°C)		1.0	1	μA	IO = 0 VI = VCC or GND
	ICCOP	Operating Supply Current ②		4		1.5	2.5	mA	f = 1MHz, IO = 0 VI = VCC or GND
	ICCDR	Data Retention Supply Current		10		0.1	1	μA	VCC = 3.0, IO = 0 VI = VCC or GND
	VCCDR	Data Retention Supply Voltage	2.0		2.0	1.4		V	
	II	Input Leakage Current	-1.0	+1.0	-0.5	0.0	+0.5	μA	GND ⩽ VI ⩽ VCC
	IOZ	Output Leakage Current	-1.0	+1.0	-0.5	0.0	+0.5	μA	GND ⩽ VO ⩽ VCC
	VIL	Input Low Voltage	-0.3	0.8	-0.3	2.0	1.5	V	
	VIH	Input High Voltage	VCC -2.0	VCC +0.3	2.5	2.0	5.3	V	
	VOL	Output Low Voltage		0.4		0.2	0.35	V	IOL = 3.2mA
	VOH	Output High Voltage	2.4		3.0	4.5		V	IOH = -0.4mA
	CI	Input Capacitance ③		6		4	6	pF	VI = VCC or GND f = 1MHz
	CO	Output Capacitance ③		10		6	10	pF	VO = VCC or GND f = 1MHz
A.C.	TELQV	Chip Enable Access Time		250		110	200	ns	④
	TAVQV	Address Access Time		250		100	200	ns	④
	TSLQX	Chip Select Output Enable Time		160		60	130	ns	④
	TWLQX	Write Enable Output Disable Time		160		60	130	ns	④
	TSHQX	Chip Select Output Disable Time		160		60	130	ns	④
	TELEH	Chip Enable Pulse Negative Width	250		200	110		ns	④
	TEHEL	Chip Enable Pulse Positive Width	100		80	50		ns	④
	TAVEL	Address Setup Time	0		0	-10		ns	④
	TELAX	Address Hold Time	50		40	30		ns	④
	TDVWH	Data Setup Time	110		80	50		ns	④
	TWHDX	Data Hold Time	0		0	0		ns	④
	TWLSH	Chip Select Write Pulse Setup Time	130		100	60		ns	④
	TWLEH	Chip Enable Write Pulse Setup Time	130		100	60		ns	④
	TSLWH	Chip Select Write Pulse Hold Time	130		100	60		ns	④
	TELWH	Chip Enable Write Pulse Hold Time	130		100	60		ns	④
	TWLWH	Write Enable Pulse Width	130		100	60		ns	④
	TELEL	Read or Write Cycle Time	350		280	160		ns	④

NOTES:
1. All devices tested at worst case limits. Room temp., 5 volt data provided for information — not guaranteed.
2. Operating Supply Current (ICCOP) is proportional to Operating Frequency. Example: Typical ICCOP = 1.5mA/MHz.
3. Capacitance sampled and guaranteed — not 100% tested.
4. AC Test Conditions: Inputs — TRISE = TFALL = 20nsec; Outputs — 1 TTL load and 50pF. All timing measurements at 1/2 VCC.

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ABSOLUTE MAXIMUM RATINGS		OPERATING RANGE	
Supply Voltage -VCC	+8.0V	Operating Supply Voltage -VCC Commercial	4.75V to 5.25V
Input or Output Voltage Applied	GND -0.3V VCC +0.3V	Operating Temperature Commercial	0°C to 75°C
Storage Temperature	-65°C to +150°C		

ELECTRICAL CHARACTERISTICS

	SYMBOL	PARAMETER	TEMP. & VCC = OPERATING RANGE MIN	TEMP. & VCC = OPERATING RANGE MAX	TEMP. = 25°C ① VCC = 5.0V MIN	TEMP. = 25°C ① VCC = 5.0V TYP	TEMP. = 25°C ① VCC = 5.0V MAX	UNITS	TEST CONDITIONS
D.C.	ICCSB	Standby Supply Current		100		10	100	μA	IO = 0 VI = VCC or GND
	ICCOP	Operating Supply Current ②		4		1.5	2.5	mA	f = 1MHz, IO = 0 VI = VCC or GND
	VCCDR	Data Retention Supply Voltage	2.0		2.0			V	
	II	Input Leakage Current	-1.0	+1.0	-0.5	0.0	+0.5	μA	GND ⩽ VI ⩽ VCC
	IOZ	Output Leakage Current	-1.0	+1.0	-0.5	0.0	+0.5	μA	GND ⩽ VO ⩽ VCC
	VIL	Input Low Voltage	-0.3	0.8	-0.3	2.0	1.5	V	
	VIH	Input High Voltage	VCC -2.0	VCC +0.3	2.5	2.0	5.3	V	
	VOL	Output Low Voltage		0.4		0.2	0.35	V	IOL = 1.6mA
	VOH	Output High Voltage	2.4		3.0	4.5		V	IOH = -0.2mA
	CI	Input Capacitance ③		6		4	6	pF	VI = VCC or GND f = 1MHz
	CO	Output Capacitance ③		10		6	10	pF	VO = VCC or GND f = 1MHz
A.C.	TELQV	Chip Enable Access Time		300		160	250	ns	④
	TAVQV	Address Access Time		310		160	260	ns	④
	TSLQX	Chip Select Output Enable Time		200		60	170	ns	④
	TWLQX	Write Enable Output Disable Time		200		60	170	ns	④
	TSHQX	Chip Select Output Disable Time		200		60	170	ns	④
	TELEH	Chip Enable Pulse Negative Width	300		250	160		ns	④
	TEHEL	Chip Enable Pulse Positive Width	150		130	90		ns	④
	TAVEL	Address Setup Time	10		10	0		ns	④
	TELAX	Address Hold Time	50		50	30		ns	④
	TDVWH	Data Setup Time	130		100	80		ns	④
	TWHDX	Data Hold Time	0		0	0		ns	④
	TWLSH	Chip Select Write Pulse Setup Time	160		130	100		ns	④
	TWLEH	Chip Enable Write Pulse Setup Time	160		130	100		ns	④
	TSLWH	Chip Select Write Pulse Hold Time	160		130	100		ns	④
	TELWH	Chip Enable Write Pulse Hold Time	160		130	100		ns	④
	TWLWH	Write Enable Pulse Width	160		130	100		ns	④
	TELEL	Read or Write Cycle Time	450		380	250		ns	④

NOTES:
1. All devices tested at worst case limits. Room temp., 5 volt data provided for information — not guaranteed.
2. Operating Supply Current (ICCOP) is proportional to Operating Frequency. Example: Typical ICCOP = 1.5mA/MHz.
3. Capacitance sampled and guaranteed — not 100% tested.
4. AC Test Conditions: Inputs — TRISE = TFALL = 20nsec; Outputs — 1 TTL load and 50pF. All timing measurements at 1/2 VCC.

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HARRIS
SEMICONDUCTOR
PRODUCTS DIVISION
A DIVISION OF HARRIS CORPORATION

HM-6533

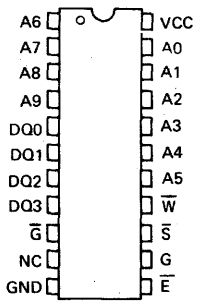
1024 x 4 CMOS RAM

Features

- LOW POWER STANDBY 1mW
- LOW POWER OPERATION. . . . . 35mW/MHz MAX
- DATA RETENTION @ 2.0 VOLTS.
- TTL COMPATIBLE INPUT/OUTPUT.
- "THREE STATE" OUTPUT.
- SEPARATE CHIP SELECT FOR EASE OF MEMORY EXPANSION.
- FULL MILITARY AND INDUSTRIAL TEMPERATURE RANGES.
- ON CHIP ADDRESS REGISTER.
- AVAILABLE IN 22 PIN DIP AND IN CHIP FORM FOR HYBRID FABRICATION.

Pinout

TOP VIEW



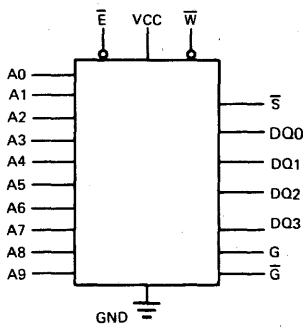
Description

The HM-6533 is a 1024 x 4 clocked static CMOS RAM designed specifically to interface with the HM-6100 Microprocessor. The device is manufactured utilizing self-aligned silicon gate technology. Extremely low power drain makes the HM-6533 an ideal candidate for battery powered systems.

On chip latching address registers and "Three State" I/O buffers enable the HM-6533 to operate in a multiplexed bus system with a minimum of support circuitry. Separate chip select and output disable pins allow for easy expansion. The output buffers can be disabled by the G, $\overline{G}$, or S pins (see Truth Table).

Wide supply voltage range and high noise immunity offer the system designer a large degree of flexability. Data retention is guaranteed down to 2.0V VCC making non-volitile memory systems simple to implement.

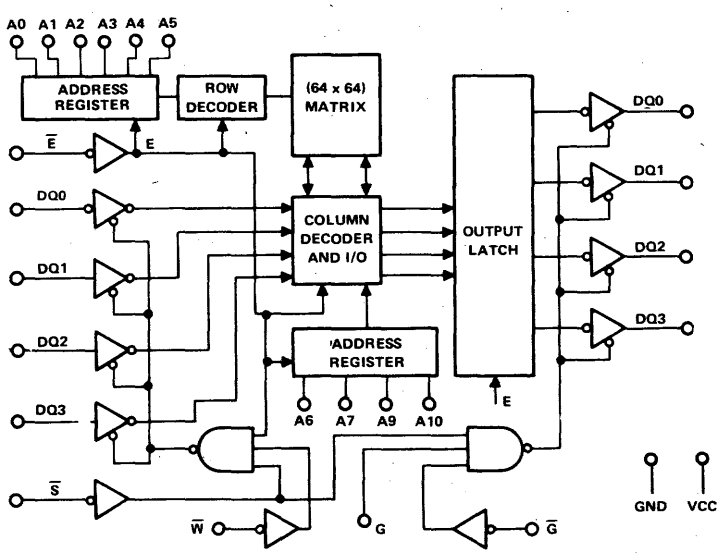
Logic Symbol



PIN NAMES

A	Address Input
$\overline{E}$	Chip Enable
$\overline{W}$	Write Enable
DQ	Data In/Out
S	Chip Select
G	Output Enable

Functional Diagram



"SEE PAGES 1409-1415 FOR PACKAGE SELECTION GUIDE"

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ABSOLUTE MAXIMUM RATINGS

Supply Voltage-VCC	+8.0V
Applied Input or Output Voltage	GND-0.3V VCC+0.3V
Storage Temperature Range	-65°C to +150°C

OPERATING RANGE

Operating Supply Voltage-VCC	4.5V to 5.5V
Operating Temperature Range	
Military (-2)	-55°C to +125°C
Industrial (-9)	-40°C to +85°C

ELECTRICAL CHARACTERISTICS

			VCC & TEMP = OPERATING RANGE		TEMP = 25°C VCC = 5.0V (1)				
	SYMBOL	PARAMETER	MIN	MAX	MIN	TYP	MAX	UNIT	TEST CONDITIONS
D.C.	ICCSB	Standby Supply Current		100		0.1	1.0	μA	IO = 0, VI = VCC or GND
	ICCOP	Operating Current (2)		8		6	7	mA	F = 1MHz, IO = 0
	ICCDR	Data Retention Supply Current		50		1.0	5.0	μA	VCC = 3.0, IO = 0 VI = VCC or GND
	VCCDR	Data Retention Supply Voltage		2.0		2.0	1.4	V	
	II	Input Leakage Current	-1.0	+1.0	-0.5	0.0	+0.5	μA	GND<VI<VCC
	IOZ	Output Leakage Current	-1.0	+1.0	-0.5	0.0	+0.5	μA	GND<VO<VCC
	VIL	Input Low Voltage	-0.3	0.8	-0.3	2.0	1.5	V	
	VIH	Input High Voltage	VCC -2.0	VCC +0.3	2.5	2.0	5.3	V	
	VOL	Output Low Voltage		0.4		0.2	0.35	V	IOL = 2.0mA
	VOH	Output High Voltage	2.4		3.0	4.5		V	IOH = -2.0mA
	CI	Input Capacitance (3)		6		4	6	pF	VI, VIO=VCC or GND F = 1MHz
	CIO	Output Capacitance (3)		10		6	10	pF	VI, VIO=VCC or GND F = 1MHz
A.C.	TELQV	Chip Enable Access Time		400		300	350	ns	(4)
	TSLQX	Chip Select Output Enable Time		200		110	150	ns	(4)
	TSHQZ	Chip Select Output Disable Time		200		110	150	ns	(4)
	TGLQX	Output Enable Time		200		110	150	ns	(4)
	TGHQX	Output Disable Time		200		110	150	ns	(4)
	TELEL	Read or Write Cycle Time		600		475	550	ns	(4)
	TEHEL	Chip Enable Positive Pulse Width	200		200	175		ns	(4)
	TELEH	Chip Enable Negative Pulse Width	400		350	300		ns	(4)
	TAVEL	Address Setup Time	25		25	10		ns	(4)
	TELAX	Address Hold Time	75		75	60		ns	(4)
	TWLWH	Write Enable Pulse Width	220		130	110		ns	(4)
	TWLEH	Write Enable Pulse Setup Time	220		130	110		ns	(4)
	TELWH	Chip Enable Write Pulse Hold Time	220		130	110		ns	(4)
	TWLSH	Chip Select Write Pulse Setup Time	220		130	110		ns	(4)
	TSLWH	Chip Select Write Pulse Hold Time	220		130	110		ns	(4)
	TDVWH	Data Setup Time	130		100	70		ns	(4)
	TWHDX	Data Hold Time	50		50	40		ns	(4)
	TDVSH	Data to Chip Select Setup Time	130		100	70		ns	(4)
	TSHDX	Data to Chip Select Hold Time	50		50	40		ns	(4)
	TSLSH	Chip Select Write Setup Time	220		130	100		ns	(4)

NOTES:
1. All devices tested at worst case limits. Room temperature, 5V data provided for information - not guaranteed.
2. Operating supply current (ICCOP) is proportional to operating frequency. Example: Typical ICCOP = 6mA/MHz.
3. Capacitance sampled and guaranteed - not 100% tested.
4. AC test conditions: Inputs – Trise = Tfall = 20ns.
   Outputs – 1 TTL Load and 50pF.

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ABSOLUTE MAXIMUM RATINGS

Supply Voltage-VCC	+8.0V
Applied Input or Output Voltage	GND-0.3V VCC+0.3V
Storage Temperature Range	-65°C to +150°C

OPERATING RANGE

Operating Supply Voltage-VCC	4.5V to 5.5V
Operating Temperature Range	-40°C to +85°C

ELECTRICAL CHARACTERISTICS

			VCC & TEMP = OPERATING RANGE		TEMP = 25°C VCC = 5.0V (1)				
	SYMBOL	PARAMETER	MIN	MAX	MIN	TYP	MAX	UNIT	TEST CONDITIONS
D.C.	ICCSB	Standby Supply Current		1.0		0.1	1.0	mA	IO = 0, VI = VCC or GND
	ICCOP	Operating Current (2)		8		6	+7	mA	F = 1MHz, IO = 0
	II	Input Leakage Current	-10	+10		± 0.5	+7	μA	GND < VI < VCC
	IOZ	Output Leakage Current	-10	+10	-7	± 0.5	+7	μA	GND < VO < VCC
	VIL	Input Low Voltage	-0.3	0.8	-0.3	2.0	1.5	V	
	VIH	Input High Voltage	VCC -2.0	VCC +0.3	2.5	2.0	5.3	V	
	VOL	Output Low Voltage		0.4		0.2	0.35	V	IOL = 1.6mA
	VOH	Output High Voltage	2.4		3.0	4.5		V	IOH = -1.6mA
	CI	Input Capacitance (3)		6		4	6	pF	VI, VIO=VCC or GND F = 1MHz
	CIO	Output Capacitance (3)		10		6	10	pF	VI, VIO=VCC or GND F = 1MHz
A.C.	TELQV	Chip Enable Access Time		450		350	400	ns	(4)
	TSLQX	Chip Select Output Enable Time		300		130	180	ns	(4)
	TSHQZ	Chip Select Output Disable Time		300		130	180	ns	(4)
	TGLQX	Output Enable Time		250		130	180	ns	(4)
	TGHQX	Output Disable Time		250		130	180	ns	(4)
	TELEL	Read or Write Cycle Time	700		650	560		ns	(4)
	TEHEL	Chip Enable Positive Pulse Width	250		250	210		ns	(4)
	TELEH	Chip Enable Negative Pulse Width	450		400	350		ns	(4)
	TAVEL	Address Setup Time	50		50	30		ns	(4)
	TELAX	Address Hold Time	100		100	75		ns	(4)
	TWLWH	Write Enable Pulse Width	300		200	175		ns	(4)
	TWLEH	Write Enable Pulse Setup Time	300		200	175		ns	(4)
	TELWH	Chip Enable Write Pulse Hold Time	300		200	175		ns	(4)
	TWLSH	Chip Select Write Pulse Setup Time	300		200	175		ns	(4)
	TSLWH	Chip Select Write Pulse Hold Time	300		200	175		ns	(4)
	TDVWH	Data Setup Time	200		150	120		ns	(4)
	TWHDX	Data Hold Time	75		50	25		ns	(4)
	TDVSH	Data to Chip Select Setup Time	220		150	120		ns	(4)
	TSHDX	Data to Chip Select Hold Time	75		50	25		ns	(4)
	TSLSH	Chip Select Write Setup Time	300		200	175		ns	(4)

NOTES:
1. All devices tested at worst case limits. Room temperature, 5V data provided for information - not guaranteed.
2. Operating supply current (ICCOP) is proportional to operating frequency. Example: Typical ICCOP = 6mA/MHz.
3. Capacitance sampled and guaranteed - not 100% tested.
4. AC test conditions: Inputs – Trise = Tfall = 20ns.
   Outputs – 1 TTL Load and 50pF.

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HM-6543

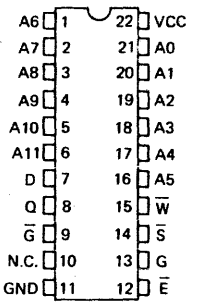
4096 x 1 CMOS RAM

Features

- LOW POWER STANDBY . . . . . 1mW MAX
- LOW POWER OPERATION . . . . . 35mW/MHz MAX
- DATA RETENTION . . . . . @ 2.0 VOLTS
- TTL COMPATIBLE INPUT/OUTPUT
- THREE STATE OUTPUT
- SEPARATE CHIP SELECT FOR EASE OF MEMORY EXPANSION
- FULL MILITARY AND INDUSTRIAL TEMPERATURE RANGE
- ON CHIP ADDRESS REGISTER
- AVAILABLE IN 22 PIN DIP AND IN CHIP FORM FOR HYBRID FABRICATION

Pinout

TOP VIEW



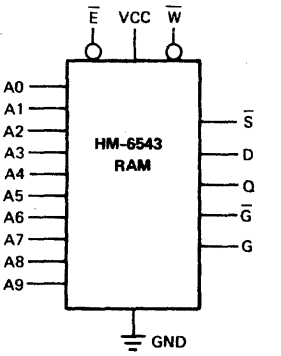
Description

The HM-6543 is a 4096 x 1 static CMOS RAM fabricated with self-aligned silicon gate technology. The device is designed to interface directly with the HM-6100, 12 bit Microprocessor.

On chip latches are provided for addresses and output data. The chip provides a three state output buffer for ease of use on a common bus.

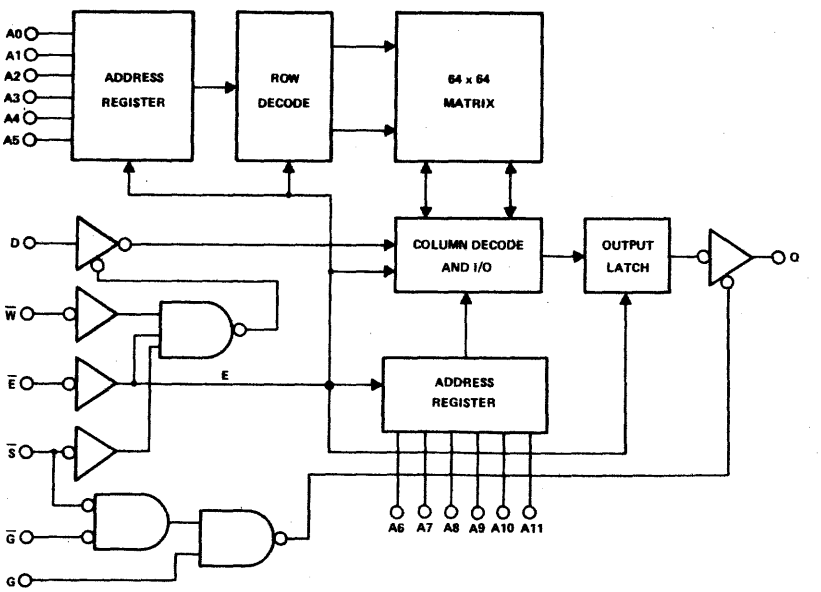
The HM-6543 is a fully static RAM and may be maintained in any state for an indefinite period of time. Data retention, supply voltage and supply current are guaranteed over temperature.

Logic Symbol



A – Address Input
$\overline{E}$ – Chip Enable
$\overline{W}$ – Write Enable
$\overline{G}$ – Output Enable
$\overline{S}$ – Chip Select
D – Data Input
Q – Data Output
G – Output Enable

Functional Diagram



"SEE PAGES 1409-1415 FOR PACKAGE SELECTION GUIDE"

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ABSOLUTE MAXIMUM RATINGS		OPERATING RANGE	
Supply Voltage -VCC	+8.0V	Operating Supply Voltage -VCC	4.5V to 5.5V
Applied Input or Output Voltage	GND -0.3V to VCC +0.3V	Operating Temperature	
		Military (-2)	-55°C to +125°C
Storage Temperature	-65°C to +150°C	Industrial (-9)	-40°C to +85°C

ELECTRICAL CHARACTERISTICS

	SYMBOL	PARAMETER	TEMP. & VCC = OPERATING RANGE MIN	TEMP. & VCC = OPERATING RANGE MAX	TEMP. = 25°C ① VCC = 5.0V MIN	TEMP. = 25°C ① VCC = 5.0V TYP	TEMP. = 25°C ① VCC = 5.0V MAX	UNITS	TEST CONDITIONS
D.C.	ICCSB	Standby Supply Current		100		2	10	μA	IO = 0 VI = VCC or GND
	ICCOP	Operating Current ②		8		6	7	mA	f = 1MHz, IO = 0 VI = VCC or GND
	ICCDR	Data Retention Supply Current		50		1	5	μA	VCC = 3.0, IO = 0 VI = VCC or GND
	VCCDR	Data Retention Supply Voltage		2.0		2.0	1.4	V	
	II	Input Leakage Current	-1.0	+1.0	-0.5	0.0	+0.5	μA	GND ≤ VI ≤ VCC
	IOZ	Output Leakage Current	-1.0	+1.0	-0.5	0.0	+0.5	μA	GND ≤ VO ≤ VCC
	VIL	Input Low Voltage	-0.3	0.8	-0.3	2.0	1.5	V	
	VIH	Input High Voltage	VCC -2.0	VCC +3.0	2.5	2.0	5.3	V	
	VOL	Output Low Voltage		0.4		0.2	0.35	V	IOL = 2.0mA
	VOH	Output High Voltage	2.4		3.0	4.5		V	IOH = -2.0mA
	CI	Input Capacitance ③		6		4	6	pF	VI = VCC or GND f = 1MHz
	CO	Output Capacitance ③		10		6	10	pF	VO= VCC or GND f = 1MHz
A.C.	TELQV	Chip Enable Access Time		400		300	350	ns	④
	TSLQX	Chip Select Output Enable Time		200		110	150	ns	④
	TSHQZ	Chip Select Output Disable Time		200		110	150	ns	④
	TGLQX	Output Enable Time		200		110	150	ns	④
	TGHQZ	Output Disable Time		200		110	150	ns	④
	TELEL	Read or Write Cycle Time		600		475	550	ns	④
	TEHEL	Chip Enable Positive Pulse Width	200		200	175		ns	④
	TELEH	Chip Enable Negative Pulse Width	400		350	300		ns	④
	TAVEL	Address Setup Time	25		25	10		ns	④
	TELAX	Address Hold Time	75		75	60		ns	④
	TWLWH	Write Enable Pulse Width	220		130	110		ns	④
	TWLEH	Write Enable Pulse Setup Time	220		130	110		ns	④
	TELWH	Chip Enable Write Pulse Hold Time	220		130	110		ns	④
	TWLSH	Chip Select Write Pulse Setup Time	220		130	110		ns	④
	TSWLH	Chip Select Write Pulse Hold Time	220		130	110		ns	④
	TDVWH	Data Setup Time	130		100	70		ns	④
	TWHDX	Data Hold Time	50		50	40		ns	④
	TDVSH	Data to Chip Select Setup Time	130		100	70		ns	④
	TSHDX	Data to Chip Select Hold Time	50		50	40		ns	④
	TSLSH	Chip Select Write Setup Time	220		130	100		ns	④

NOTES:
1. All devices tested at worst case limits. Room temp., 5 volt data provided — not guaranteed.
2. Operating Supply Current (ICCOP) is proportional to Operating Frequency. Example Typical ICCOP = 6mA/MHz.
3. Capacitance sampled and guaranteed — not 100% tested.
4. A.C. Test Conditions: Inputs — TRISE = TFALL = 20ns; Outputs — 1TTL load and 50pF.

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ABSOLUTE MAXIMUM RATINGS		OPERATING RANGE	
Supply Voltage -VCC	+8.0V	Operating Supply Voltage -VCC	4.5V to 5.5V
Applied Input or Output Voltage	GND -0.3V to VCC +0.3V	Operating Temperature	-40°C to +85°C
Storage Temperature	-65°C to +150°C		

ELECTRICAL CHARACTERISTICS

	SYMBOL	PARAMETER	TEMP. & VCC = OPERATING RANGE MIN	TEMP. & VCC = OPERATING RANGE MAX	TEMP. = 25°C ① VCC = 5.0V MIN	TEMP. = 25°C ① VCC = 5.0V TYP	TEMP. = 25°C ① VCC = 5.0V MAX	UNITS	TEST CONDITIONS
D.C.	ICCSB	Standby Supply Current		1.0		0.1	1.0	mA	IO = 0 VI = VCC or GND
	ICCOP	Operating Current ②		8		6	7	mA	f = 1MHz, IO = 0 VI = VCC or GND
	II	Input Leakage Current	-10	+10		±0.5	+7	μA	GND ≤ VI ≤ VCC
	IOZ	Output Leakage Current	-10	+10	-7	±0.5	+7	μA	GND ≤ VO ≤ VCC
	VIL	Input Low Voltage	-0.3	0.8	-0.3	2.0	1.5	V	
	VIH	Input High Voltage	VCC -2.0	VCC +3.0	2.5	2.0	5.3	V	
	VOL	Output Low Voltage		0.4		0.2	0.35	V	IOL = 2.0mA
	VOH	Output High Voltage	2.4		3.0	4.5		V	IOH = -2.0mA
	CI	Input Capacitance ③		6		4	6	pF	VI = VCC or GND f = 1MHz
	CO	Output Capacitance ③		10		6	10	pF	VO = VCC or GND f = 1MHz
A.C.	TELQV	Chip Enable Access Time		450		350	400	ns	④
	TSLQX	Chip Select Output Enable Time		300		130	180	ns	④
	TSHQZ	Chip Select Output Disable Time		300		130	180	ns	④
	TGLQX	Output Enable Time		250		130	180	ns	④
	TGHQZ	Output Disable Time		250		130	180	ns	④
	TELEL	Read or Write Cycle Time	700		560	650		ns	④
	TEHEL	Chip Enable Positive Pulse Width	250		210	250		ns	④
	TELEH	Chip Enable Negative Pulse Width	450		350	400		ns	④
	TAVEL	Address Setup Time	50		30	50		ns	④
	TELAX	Address Hold Time	100		75	100		ns	④
	TWLWH	Write Enable Pulse Width	300		175	200		ns	④
	TWLEH	Write Enable Pulse Setup Time	300		175	200		ns	④
	TELWH	Chip Enable Write Pulse Hold Time	300		175	200		ns	④
	TWLSH	Chip Select Write Pulse Setup Time	300		175	200		ns	④
	TSLWH	Chip Select Write Pulse Hold Time	300		175	200		ns	④
	TDVWH	Data Setup Time	200		120	150		ns	④
	TWHDX	Data Hold Time	75		25	50		ns	④
	TDVSH	Data To Chip Select Setup Time	220		120	150		ns	④
	TSHDX	Data to Chip Select Hold Time	75		25	50		ns	④
	TSLSH	Chip Select Write Setup Time	300		175	200		ns	④

NOTES:
1. All devices tested at worst case limits. Room temp., 5 volt data provided — not guaranteed.
2. Operating Supply Current (ICCOP) is proportional to Operating Frequency. Example Typical ICCOP = 6mA/MHz.
3. Capacitance sampled and guaranteed — not 100% tested.
4. A.C. Test Conditions: Inputs — TRISE = TFALL = 20ns; Outputs — 1TTL load and 50pF.

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HARRIS
SEMICONDUCTOR
PRODUCTS DIVISION
A DIVISION OF HARRIS CORPORATION

HM-6551

256 x 4 CMOS RAM

Features

- LOW STANDBY POWER . . . . . 55μW MAX
- LOW OPERATING POWER. . . . . 22mW/MHz MAX
- FAST ACCESS TIME . . . . . 220nsec MAX
- DATA RETENTION VOLTAGE . . . . . 2.0 VOLTS MIN
- TTL COMPATIBLE IN/OUT
- HIGH OUTPUT DRVIE – 2 TTL LOADS
- INTERNAL LATCHED CHIP SELECT
- HIGH NOISE IMMUNITY
- ON CHIP ADDRESS REGISTERS
- LATCHED OUTPUTS
- THREE STATE OUTPUTS
- MILITARY AND INDUSTRIAL TEMPERATURE RANGES

Description

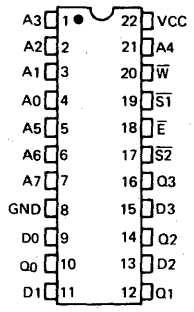
The HM-6551 is a 256 by 4 static CMOS RAM fabricated using self-aligned silicon gate technology. Synchronous circuit design techniques are employed to achieve high performance and low power operation.

On chip latches are provided for addresses and data outputs allowing efficient interfacing with microprocessor systems. The data output buffers can be forced to a high impedance state for use in expanded memory arrays.

The HM-6551 is a fully static RAM and may be maintained in any state for an indefinite period of time. Data retention supply voltage and supply current are guaranteed over temperature.

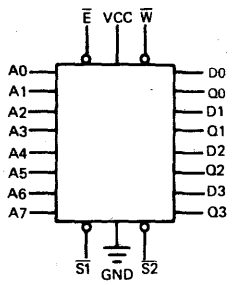
Pinout

TOP VIEW

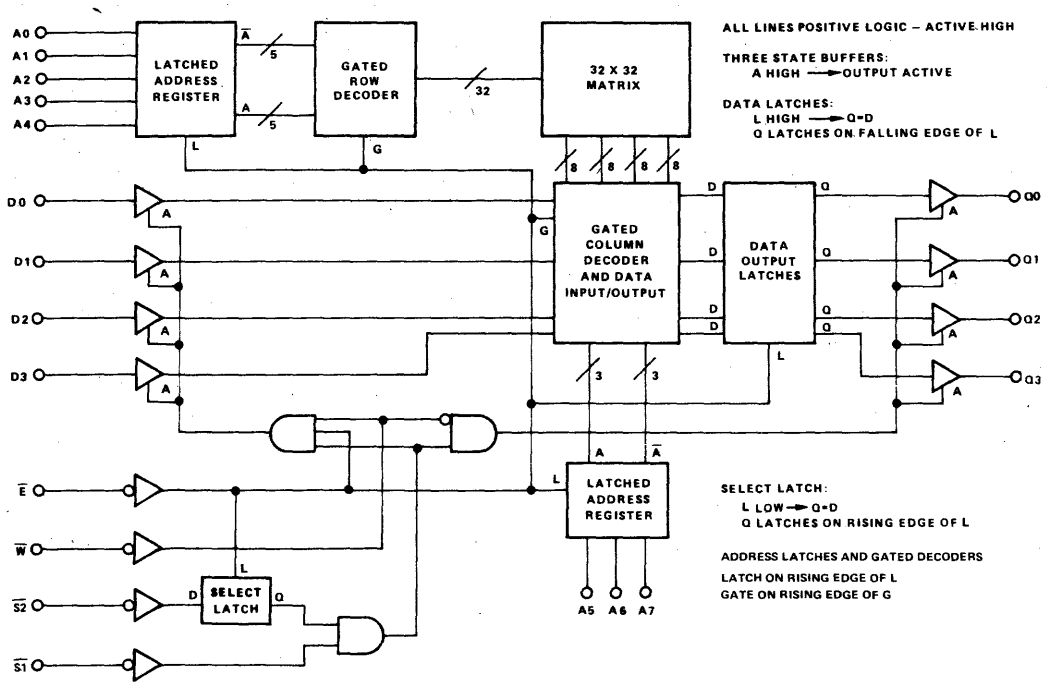


A – Address Input
Ē – Chip Enable
S̄ – Chip Select
W̄ – Write Enable
D – Data Input
Q – Data Output

Logic Symbol



Functional Diagram



"SEE PAGES 1409-1415 FOR PACKAGE SELECTION GUIDE"

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ABSOLUTE MAXIMUM RATINGS

Supply Voltage -VCC	+8.0V
Applied Input or Output Voltage	GND -0.3V VCC +0.3V
Storage Temperature	-65°C to +150°C

OPERATING RANGE

Operating Supply Voltage -VCC	
Military (-2)	4.5V to 5.5V
Industrial (-9)	4.5V to 5.5V
Operating Temperature	
Military (-2)	-55°C to +125°C
Industrial (-9)	-40°C to +85°C

ELECTRICAL CHARACTERISTICS

	SYMBOL	PARAMETER	TEMP. & VCC = OPERATING RANGE MIN	TEMP. & VCC = OPERATING RANGE MAX	TEMP. = 25°C ① VCC = 5.0V MIN	TEMP. = 25°C ① VCC = 5.0V TYP	TEMP. = 25°C ① VCC = 5.0V MAX	UNITS	TEST CONDITIONS
D.C.	ICCSB	Standby Supply Current		10 1(+25°C)		0.1	1	µA	IO = 0 VI = VCC or GND
	ICCOP	Operating Supply Current ②		4		1.5	25	mA	f = 1MHz, IO = 0 VI = VCC or GND
	ICCDR	Data Retention Supply Current		10		0.01	1	µA	VCC = 3.0, IO = 0 VI = VCC or GND
	VCCDR	Data Retention Supply Voltage	2.0		2.0	1.4		V	
	II	Input Leakage Current	-1.0	+1.0	-0.5	0.0	+0.5	µA	GND ≤ VI ≤ VCC
	IOZ	Output Leakage Current	-1.0	+1.0	-0.5	0.0	+0.5	µA	GND ≤ VO ≤ VCC
	VIL	Input Low Voltage	-0.3	0.8	-0.3	2.0	1.5	V	
	VIH	Input High Voltage	VCC -2.0	VCC +0.3	2.5	2.0	5.3	V	
	VOL	Output Low Voltage		0.4		0.2	0.35	V	IOL = 3.2mA
	VOH	Output High Voltage	2.4		3.0	4.5		V	IOH = -0.4mA
	CI	Input Capacitance ③		6		4	6	pF	VI = VCC or GND f = 1MHz
	CO	Output Capacitance ③		10		6	10	pF	VO= VCC or GND f = 1MHz
A.C.	TELQV	Chip Enable Access Time		220		120	170	ns	④
	TAVQV	Address Access Time		220		110	170	ns	④
	TS1LQX	Chip Select 1 Output Enable Time		130		50	90	ns	④
	TWLQZ	Write Enable Output Disable Time		130		50	90	ns	④
	TS1HQZ	Chip Select 1 Output Disable Time		130		50	90	ns	④
	TELEH	Chip Enable Pulse Negative Width	220		170	120		ns	④
	TEHEL	Chip Enable Pulse Positive Width	100		70	50		ns	④
	TAVEL	Address Setup Time	0		0	-10		ns	④
	TS2LEL	Chip Select 2 Setup Time	0		0	-10		ns	④
	TELAX	Address Hold Time	40		40	20		ns	④
	TELS2X	Chip Select 2 Hold Time	40		40	20		ns	④
	TDVWH	Data Setup Time	100		80	50		ns	④
	TWHDX	Data Hold Time	0		0	0		ns	④
	TWLS1H	Chip Select 1 Write Pulse Setup Time	120		100	60		ns	④
	TWLEH	Chip Enable Write Pulse Setup Time	120		100	60		ns	④
	TS1LWH	Chip Select 1 Write Pulse Hold Time	120		100	60		ns	④
	TELWH	Chip Enable Write Pulse Hold Time	120		100	60		ns	④
	TWLWH	Write Enable Pulse Width	120		100	60		ns	④
	TELEL	Read or Write Cycle Time	320		240	170		ns	④

NOTES:
1. All devices tested at worst case limits. Room temp., 5 volt data provided for information — not guaranteed.
2. Operating Supply Current (ICCOP) is proportional to Operating Frequency. Example: Typical ICCOP = 1.5mA/MHz.
3. Capacitance sampled and guaranteed — not 100% tested.
4. AC Test Conditions: Inputs — TRISE = TFALL = 20nsec; Outputs — 1 TTL load and 50pF. All timing measurements at 1/2 VCC.

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ABSOLUTE MAXIMUM RATINGS		OPERATING RANGE	
Supply Voltage -VCC	+8.0V	Operating Supply Voltage -VCC	
		Military (-2)	4.5V to 5.5V
Applied Input or Output Voltage	GND -0.3V VCC +0.3V	Industrial (-9)	4.5V to 5.5V
		Operating Temperature	
Storage Temperature	-65°C to +150°C	Military (-2)	-55°C to +125°C
		Industrial (-9)	-40°C to +85°C

ELECTRICAL CHARACTERISTICS

	SYMBOL	PARAMETER	TEMP. & VCC = OPERATING RANGE MIN	TEMP. & VCC = OPERATING RANGE MAX	TEMP. = 25°C ① VCC = 5.0V MIN	TEMP. = 25°C ① VCC = 5.0V TYP	TEMP. = 25°C ① VCC = 5.0V MAX	UNITS	TEST CONDITIONS
D.C.	ICCSB	Standby Supply Current		10 1(+25°C)		1.0	1	μA	IO = 0 VI = VCC or GND
	ICCOP	Operating Supply Current ②		4		1.5	2.5	mA	f = 1MHz, IO = 0 VI = VCC or GND
	ICCDR	Data Retention Supply Current		10		0.1	1	μA	VCC = 3.0, IO = 0 VI = VCC or GND
	VCCDR	Data Retention Supply Voltage	2.0		2.0	1.4		V	
	II	Input Leakage Current	-1.0	+1.0	-0.5	0.0	+0.5	μA	GND ≤ VI ≤ VCC
	IOZ	Output Leakage Current	-1.0	+1.0	-0.5	0.0	+0.5	μA	GND ≤ VO ≤ VCC
	VIL	Input Low Voltage	-0.3	0.8	-0.3	2.0	1.5	V	
	VIH	Input High Voltage	VCC -2.0	VCC +0.3	2.5	2.0	5.3	V	
	VOL	Output Low Voltage		0.4		0.2	0.35	V	IOL = 3.2mA
	VOH	Output High Voltage	2.4		3.0	4.5		V	IOH = -0.4mA
	CI	Input Capacitance ③		6		4	6	pF	VI = VCC or GND f = 1MHz
	CO	Output Capacitance ③		10		6	10	pF	VO= VCC or GND f = 1MHz
A.C.	TELQV	Chip Enable Access Time		300		160	240	ns	④
	TAVQV	Address Access Time		300		150	240	ns	④
	TS1LQX	Chip Select 1 Output Enable Time		150		60	120	ns	④
	TWLQZ	Write Enable Output Disable Time		150		60	120	ns	④
	TS1HQZ	Chip Select 1 Output Disable Time		150		60	120	ns	④
	TELEH	Chip Enable Pulse Negative Width	300		240	160		ns	④
	TEHEL	Chip Enable Pulse Positive Width	100		70	50		ns	④
	TAVEL	Address Setup Time	0		0	-10		ns	④
	TS2LEL	Chip Select 2 Setup Time	0		0	-10		ns	④
	TELAX	Address Hold Time	50		40	30		ns	④
	TELS2X	Chip Select 2 Hold Time	50		40	30		ns	④
	TDVWH	Data Setup Time	150		120	100		ns	④
	TWHDX	Data Hold Time	0		0	0		ns	④
	TWLS1H	Chip Select 1 Write Pulse Setup Time	180		150	120		ns	④
	TWLEH	Chip Enable Write Pulse Setup Time	180		150	120		ns	④
	TS1LWH	Chip Select 1 Write Pulse Hold Time	180		150	120		ns	④
	TELWH	Chip Enable Write Pulse Hold Time	180		150	120		ns	④
	TWLWH	Write Enable Pulse Width	180		150	120		ns	④
	TELEL	Read or Write Cycle Time	400		270	170		ns	④

NOTES:
1. All devices tested at worst case limits. Room temp., 5 volt data provided for information – not guaranteed.
2. Operating Supply Current (ICCOP) is proportional to Operating Frequency. Example: Typical ICCOP = 1.5mA/MHz.
3. Capacitance sampled and guaranteed – not 100% tested.
4. AC Test Conditions: Inputs – TRISE = TFALL = 20nsec; Outputs – 1 TTL load and 50pF. All timing measurements at 1/2 VCC.

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ABSOLUTE MAXIMUM RATINGS		OPERATING RANGE	
Supply Voltage -VCC	+8.0V	Operating Supply Voltage -VCC Commercial	4.75V to 5.25V
Applied Input or Output Voltage	GND -0.3V VCC +0.3V	Operating Temperature Commercial	0°C to 75°C
Storage Temperature	-65°C to +150°C		

ELECTRICAL CHARACTERISTICS

	SYMBOL	PARAMETER	TEMP. & VCC = OPERATING RANGE MIN	TEMP. & VCC = OPERATING RANGE MAX	TEMP. = 25°C ① VCC = 5.0V MIN	TEMP. = 25°C ① VCC = 5.0V TYP	TEMP. = 25°C ① VCC = 5.0V MAX	UNITS	TEST CONDITIONS
D.C.	ICCSB	Standby Supply Current		100		10	100	μA	IO = 0 VI = VCC or GND
	ICCOP	Operating Supply Current ②		4		1.5	2.5	mA	f = 1MHz, IO = 0 VI = VCC or GND
	VCCDR	Data Retention Supply Voltage	2.0		2.0			V	
	II	Input Leakage Current	-1.0	+1.0	-0.5	0.0	+0.5	μA	GND ≤ VI ≤ VCC
	IOZ	Output Leakage Current	-1.0	+1.0	-0.5	0.0	+0.5	μA	GND ≤ VO ≤ VCC
	VIL	Input Low Voltage	-0.3	0.8	-0.3	2.0	1.5	V	
	VIH	Input High Voltage	VCC -2.0	VCC +0.3	2.5	2.0	5.3	V	
	VOL	Output Low Voltage		0.4		0.2	0.35	V	IOL = 1.6mA
	VOH	Output High Voltage	2.4		3.0	4.5		V	IOH = -0.2mA
	CI	Input Capacitance ③		6		4	6	pF	VI = VCC or GND f = 1MHz
	CO	Output Capacitance ③		10		6	10	pF	VO= VCC or GND f = 1MHz
A.C.	TELQV	Chip Enable Access Time		350		200	300	ns	④
	TAVQV	Address Access Time		360		200	310	ns	④
	TS1LQX	Chip Select 1 Output Enable Time		180		80	160	ns	④
	TWLQZ	Write Enable Output Disable Time		180		80	160	ns	④
	TS1HQZ	Chip Select 1 Output Disable Time		180		80	160	ns	④
	TELEH	Chip Enable Pulse Negative Width	350		300	200		ns	④
	TEHEL	Chip Enable Pulse Positive Width	150		130	90		ns	④
	TAVEL	Address Setup Time	10		10	0		ns	④
	TS2LEL	Chip Select 2 Setup Time	10		10	0		ns	④
	TELAX	Address Hold Time	70		50	40		ns	④
	TELS2X	Chip Select 2 Hold Time	70		50	40		ns	④
	TDVWH	Data Setup Time	170		140	120		ns	④
	TWHDX	Data Hold Time	0		0	0		ns	④
	TWLS1H	Chip Select 1 Write Pulse Setup Time	210		170	150		ns	④
	TWLEH	Chip Enable Write Pulse Setup Time	210		170	150		ns	④
	TS1LWH	Chip Select 1 Write Pulse Hold Time	210		170	150		ns	④
	TELWH	Chip Enable Write Pulse Hold Time	210		170	150		ns	④
	TWLWH	Write Enable Pulse Width	210		170	150		ns	④
	TELEL	Read or Write Cycle Time	500		330	290		ns	④

NOTES:
1. All devices tested at worst case limits. Room temp., 5 volt data provided for information — not guaranteed.
2. Operating Supply Current (ICCOP) is proportional to Operating Frequency. Example: Typical ICCOP = 1.5mA/MHz.
3. Capacitance sampled and guaranteed — not 100% tested.
4. AC Test Conditions: Inputs — TRISE = TFALL = 20nsec; Outputs — 1 TTL load and 50pF. All timing measurements at 1/2 VCC.

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HM-6561

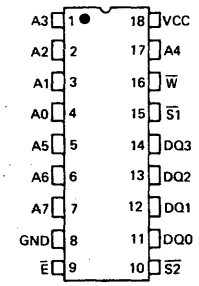
256 x 4 CMOS RAM

Features

- LOW STANDBY POWER . . . . . 55μW MAX
- LOW OPERATING POWER. . . . . 22mW/MHz MAX
- FAST ACCESS TIME . . . . . 220nsec MAX
- DATA RETENTION VOLTAGE . . . . . 2.0 VOLTS MIN
- TTL COMPATIBLE IN/OUT
- HIGH OUTPUT DRIVE – 2 TTL LOADS
- ON CHIP ADDRESS REGISTERS
- COMMON DATA IN/OUT
- THREE STATE OUTPUTS
- EASY MICROPROCESSOR INTERFACING
- MILITARY TEMPERATURE RANGE
- INDUSTRIAL TEMPERATURE RANGE

Pinout

TOP VIEW



A – Address Input
E – Chip Enable
S – Chip Select
W – Write Enable
DQ – Data In/Out

Description

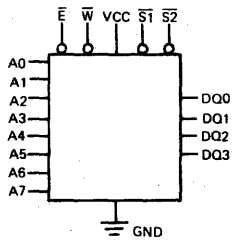
The HM-6561 is a 256 by 4 static CMOS RAM fabricated using self-aligned silicon gate technology. Synchronous circuit design techniques are employed to achieve high performance and low power operation.

On chip latches are provided for address and data outputs allowing efficient interfacing with microprocessor systems. The data output buffers can be forced to a high impedance state for use in expanded memory arrays. The data inputs and outputs are multiplexed internally for common I/O bus compatibility.

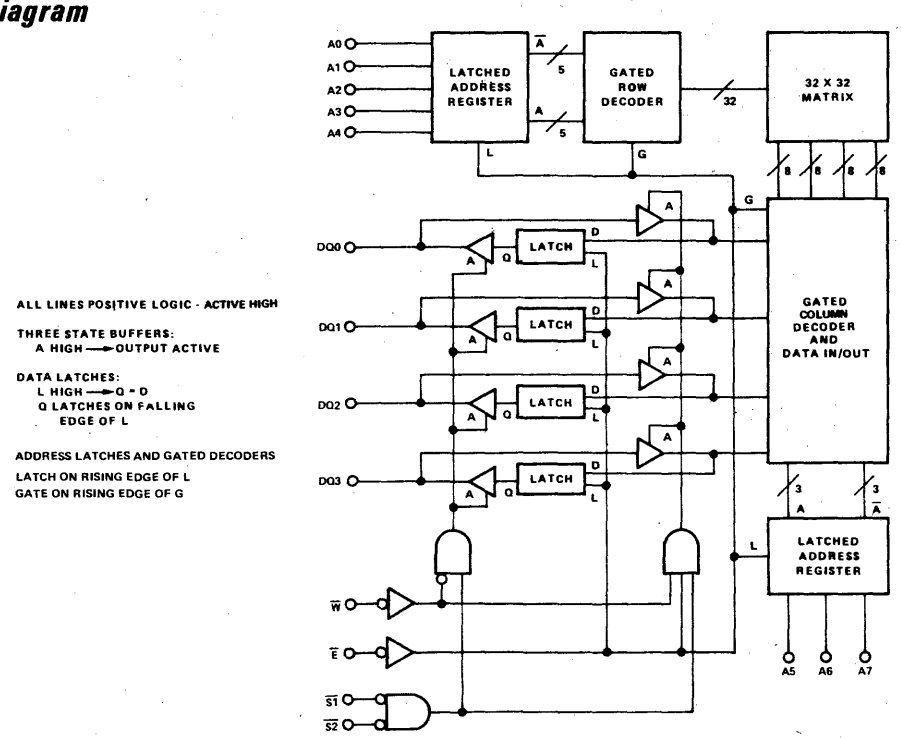
The HM-6561 is a fully static RAM and may be maintained in any state for an indefinite period of time. Data retention supply voltage and supply current are guaranteed over temperature.

The HM-6561 is pin for pin replaceable with the HM-6661, a 256 x 4 CMOS PROM. This allows a single memory board design with any organization of RAM and PROMs.

Logic Symbol



Functional Diagram



"SEE PAGES 1409-1415 FOR PACKAGE SELECTION GUIDE"

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ABSOLUTE MAXIMUM RATINGS

Supply Voltage -VCC	+8.0V
Input or Output Voltage Applied	GND -0.3V to VCC +0.3V
Storage Temperature	-65°C to +150°C

OPERATING RANGE

Operating Supply Voltage -VCC	
Military (-2)	4.5V to 5.5V
Industrial (-9)	4.5V to 5.5V
Operating Temperature	
Military (-2)	-55°C to +125°C
Industrial (-9)	-40°C to +85°C

ELECTRICAL CHARACTERISTICS

	SYMBOL	PARAMETER	TEMP. & VCC = OPERATING RANGE MIN	TEMP. & VCC = OPERATING RANGE MAX	TEMP. = 25°C ① VCC = 5.0V MIN	TEMP. = 25°C ① VCC = 5.0V TYP	TEMP. = 25°C ① VCC = 5.0V MAX	UNITS	TEST CONDITIONS
D.C.	ICCSB	Standby Supply Current		10 1(+25°C)		0.1	1	μA	IO = 0 VI = VCC or GND
	ICCOP	Operating Supply Current ②		4		1.5	2.5	mA	f = 1MHz, IO = 0 VI = VCC or GND
	ICCDR	Data Retention Supply Current		10		0.01	1	μA	VCC = 3.0, IO = 0 VI = VCC or GND
	VCCDR	Data Retention Supply Voltage	2.0		2.0	1.4		V	
	II	Input Leakage Current	-1.0	+1.0	-0.5	0.0	+0.5	μA	GND ≤ VI ≤ VCC
	IIOZ	Input/Output Leakage Current	-1.0	+1.0	-0.5	0.0	+0.5	μA	GND ≤ VO ≤ VCC
	VIL	Input Low Voltage	-0.3	0.8	-0.3	2.0	1.5	V	
	VIH	Input High Voltage	VCC -2.0	VCC +0.3	2.5	2.0	5.3	V	
	VOL	Output Low Voltage		0.4		0.2	0.35	V	IOL = 3.2mA
	VOH	Output High Voltage	2.4		3.0	4.5		V	IOH = -0.4mA
	CI	Input Capacitance ③		6		4	6	pF	VI = VCC or GND f = 1MHz
	CIO	Input/Output Capacitance ③		10		6	10	pF	VO = VCC or GND f = 1MHz
A.C.	TELQV	Chip Enable Access Time		220		120	170	ns	④
	TAVQV	Address Access Time		220		110	170	ns	④
	TSLQX	Chip Select Output Enable Time		120		50	90	ns	④
	TWLQZ	Write Enable Output Disable Time		120		50	90	ns	④
	TSHQZ	Chip Select Output Disable Time		120		50	90	ns	④
	TELEH	Chip Enable Pulse Negative Width	220		170	120		ns	④
	TEHEL	Chip Enable Pulse Positive Width	100		70	50		ns	④
	TAVEL	Address Setup Time	0		0	-10		ns	④
	TELAX	Address Hold Time	40		30	20		ns	④
	TDVWH	Data Setup Time	100		80	50		ns	④
	TWHDX	Data Hold Time	0		0	0		ns	④
	TWLDV	Write Data Delay Time	120		90	50		ns	④
	TWLSH	Chip Select Write Pulse Setup Time	220		170	100		ns	④
	TWLEH	Chip Enable Write Pulse Setup Time	220		170	100		ns	④
	TSLWH	Chip Select Write Pulse Hold Time	220		170	100		ns	④
	TELWH	Chip Enable Write Pulse Hold Time	220		170	100		ns	④
	TWLWH	Write Enable Pulse Width	220		170	100		ns	④
	TWLSL	Early Output High Z Time	0		0	-10		ns	④
	TSHWH	Late Output High Z Time	0		0	-10		ns	④
	TELEL	Read or Write Cycle Time	320		230	170		ns	④

NOTES:
1. All devices tested at worst case limits. Room temp., 5 volt data provided for information — not guaranteed.
2. Operating Supply Current (ICCOP) is proportional to Operating Frequency. Example: Typical ICCOP = 1.5mA/MHz.
3. Capacitance sampled and guaranteed — not 100% tested.
4. AC Test Conditions: Inputs — TRISE = TFALL = 20nsec; Outputs — 1 TTL load and 50pF. All timing measurements at 1/2 VCC.

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ABSOLUTE MAXIMUM RATINGS

Supply Voltage -VCC	+8.0V
Input or Output Voltage Applied	GND -0.3V to VCC +0.3V
Storage Temperature	-65°C to +150°C

OPERATING RANGE

Operating Supply Voltage -VCC	
Military (-2)	4.5V to 5.5V
Industrial (-9)	4.5V to 5.5V
Operating Temperature	
Military (-2)	-55°C to +125°C
Industrial (-9)	-40°C to +85°C

ELECTRICAL CHARACTERISTICS

	SYMBOL	PARAMETER	TEMP. & VCC = OPERATING RANGE MIN	TEMP. & VCC = OPERATING RANGE MAX	TEMP. = 25°C ① VCC = 5.0V MIN	TEMP. = 25°C ① VCC = 5.0V TYP	TEMP. = 25°C ① VCC = 5.0V MAX	UNITS	TEST CONDITIONS
D.C.	ICCSB	Standby Supply Current		10 1(+25°C)		1.0	1	µA	IO = 0 VI = VCC or GND
	ICCOP	Operating Supply Current ②		4		1.5	2.5	mA	f = 1MHz, IO = 0 VI = VCC or GND
	ICCDR	Data Retention Supply Current		10		0.1	1	µA	VCC = 3.0, IO = 0 VI = VCC or GND
	VCCDR	Data Retention Supply Voltage	2.0		2.0	1.4		V	
	II	Input Leakage Current	-1.0	+1.0	-0.5	0.0	+0.5	µA	GND ≤ VI ≤ VCC
	IIOZ	Input/Output Leakage Current	-1.0	+1.0	-0.5	0.0	+0.5	µA	GND ≤ VO ≤ VCC
	VIL	Input Low Voltage	-0.3	0.8	-0.3	2.0	1.5	V	
	VIH	Input High Voltage	VCC -2.0	VCC +0.3	2.5	2.0	5.3	V	
	VOL	Output Low Voltage		0.4		0.2	0.35	V	IOL = 3.2mA
	VOH	Output High Voltage	2.4		3.0	4.5		V	IOH = -0.4mA
	CI	Input Capacitance ③		6		4	6	pF	VI = VCC or GND f = 1MHz
	CIO	Input/Output Capacitance ③		10		6	10	pF	VO= VCC or GND f = 1MHz
A.C.	TELQV	Chip Enable Access Time		300		160	240	ns	④
	TAVQV	Address Access Time		300		150	240	ns	④
	TSLQX	Chip Select Output Enable Time		150		60	120	ns	④
	TWLQZ	Write Enable Output Disable Time		150		60	120	ns	④
	TSHQZ	Chip Select Output Disable Time		150		60	120	ns	④
	TELEH	Chip Enable Pulse Negative Width	300		240	160		ns	④
	TEHEL	Chip Enable Pulse Positive Width	100		70	50		ns	④
	TAVEL	Address Setup Time	0		0	-10		ns	④
	TELAX	Address Hold Time	50		40	30		ns	④
	TDVWH	Data Setup Time	150		120	100		ns	④
	TWHDX	Data Hold Time	0		0	0		ns	④
	TWLDV	Write Data Delay Time	150		120	60		ns	④
	TWLSH	Chip Select Write Pulse Setup Time	300		240	160		ns	④
	TWLEH	Chip Enable Write Pulse Setup Time	300		240	160		ns	④
	TSLWH	Chip Select Write Pulse Hold Time	300		240	160		ns	④
	TELWH	Chip Enable Write Pulse Hold Time	300		240	160		ns	④
	TWLWH	Write Enable Pulse Width	300		240	160		ns	④
	TWLSL	Early Output High Z Time	0		0	-10		ns	④
	TSHWH	Late Output High Z Time	0		0	-10		ns	④
	TELEL	Read or Write Cycle Time	400		310	210		ns	④

NOTES:
1. All devices tested at worst case limits. Room temp., 5 volt data provided for information — not guaranteed.
2. Operating Supply Current (ICCOP) is proportional to Operating Frequency. Example: Typical ICCOP = 1.5mA/MHz.
3. Capacitance sampled and guaranteed — not 100% tested.
4. AC Test Conditions: Inputs — TRISE = TFALL = 20nsec; Outputs — 1 TTL load and 50pF. All timing measurements at 1/2 VCC.

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ABSOLUTE MAXIMUM RATINGS		OPERATING RANGE	
Supply Voltage -VCC	+8.0V	Operating Supply Voltage -VCC Commercial	4.75V to 5.25V
Applied Input or Output Voltage	GND -0.3V VCC +0.3V	Operating Temperature Commercial	0°C to 75°C
Storage Temperature	-65°C to +150°C		

ELECTRICAL CHARACTERISTICS

	SYMBOL	PARAMETER	TEMP. & VCC = OPERATING RANGE MIN	TEMP. & VCC = OPERATING RANGE MAX	TEMP. = 25°C (1) VCC = 5.0V MIN	TEMP. = 25°C (1) VCC = 5.0V TYP	TEMP. = 25°C (1) VCC = 5.0V MAX	UNITS	TEST CONDITIONS
D.C.	ICCSB	Standby Supply Current		100		10	100	μA	IO = 0 VI = VCC or GND
	ICCOP	Operating Supply Current (2)		4		1.5	2.5	mA	f = 1MHz, IO = 0 VI = VCC or GND
	VCCDR	Data Retention Supply Voltage	2.0		2.0			V	
	II	Input Leakage Current	-1.0	+1.0	-0.5	0.0	+0.5	μA	GND ≤ VI ≤ VCC
	IIOZ	Input/Output Leakage Current	-1.0	+1.0	-0.5	0.0	+0.5	μA	GND ≤ VO ≤ VCC
	VIL	Input Low Voltage	-0.3	0.8	-0.3	2.0	1.5	V	
	VIH	Input High Voltage	VCC -2.0	VCC +0.3	2.5	2.0	5.3	V	
	VOL	Output Low Voltage		0.4		0.2	0.35	V	IOL = 1.6mA
	VOH	Output High Voltage	2.4		3.0	4.5		V	IOH = -0.2mA
	CI	Input Capacitance (3)		6		4	6	pF	VI = VCC or GND f = 1MHz
	CIO	Input/Output Capacitance (3)		10		6	10	pF	VO= VCC or GND f = 1MHz
A.C.	TELQV	Chip Enable Access Time		350		200	300	ns	(4)
	TAVQV	Address Access Time		360		200	310	ns	(4)
	TSLQX	Chip Select Output Enable Time		180		80	160	ns	(4)
	TWLQZ	Write Enable Output Disable Time		180		80	160	ns	(4)
	TSHQZ	Chip Select Output Disable Time		180		80	160	ns	(4)
	TELEH	Chip Enable Pulse Negative Width	350		300	200		ns	(4)
	TEHEL	Chip Enable Pulse Positive Width	150		130	90		ns	(4)
	TAVEL	Address Setup Time	10		10	0		ns	(4)
	TELAX	Address Hold Time	70		50	40		ns	(4)
	TDVWH	Data Setup Time	170		140	120		ns	(4)
	TWHDX	Data Hold Time	0		0	0		ns	(4)
	TWLDV	Write Data Delay Time	200		170	60		ns	(4)
	TWLSH	Chip Select Write Pulse Setup Time	350		300	200		ns	(4)
	TWLEH	Chip Enable Write Pulse Setup Time	350		300	200		ns	(4)
	TSLWH	Chip Select Write Pulse Hold Time	350		300	200		ns	(4)
	TELWH	Chip Enable Write Pulse Hold Time	350		300	200		ns	(4)
	TWLWH	Write Enable Pulse Width	350		300	200		ns	(4)
	TWLSL	Early Output High Z Time	0		0	-10		ns	(4)
	TSHWH	Late Output High Z Time	0		0	-10		ns	(4)
	TELEL	Read or Write Cycle Time	500		430	290		ns	(4)

NOTES:
1. All devices tested at worst case limits. Room temp., 5 volt data provided for information — not guaranteed.
2. Operating Supply Current (ICCOP) is proportional to Operating Frequency. Example: Typical ICCOP = 1.5mA/MHz.
3. Capacitance sampled and guaranteed — not 100% tested.
4. AC Test Conditions: Inputs — TRISE = TFALL = 20nsec; Outputs — 1 TTL load and 50pF. All timing measurements at 1/2 VCC.

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HARRIS
SEMICONDUCTOR
PRODUCTS DIVISION
A DIVISION OF HARRIS CORPORATION

HM-6562

256 x 4 CMOS RAM

Features

- LOW POWER STANDBY . . . . . 55μW MAX
- LOW POWER OPERATION. . . . . 22mW/MHz MAX
- FAST ACCESS TIME . . . . . 220nsec MAX
- DATA RETENTION VOLTAGE . . . . . 2.0 VOLTS MIN
- TTL COMPATIBLE IN/OUT
- HIGH OUTPUT DRIVE – 2 TTL LOADS
- HIGH NOISE IMMUNITY
- ON CHIP ADDRESS REGISTER
- 16 PIN PACKAGE FOR HIGH DENSITY
- THREE-STATE OUTPUTS
- MILITARY TEMPERATURE RANGE
- INDUSTRIAL TEMPERATURE RANGE

Description

The HM-6562 is a 256 by 4 static CMOS RAM fabricated using self-aligned silicon gate technology. Synchronous circuit design techniques are employed to achieve high performance and low power operation.

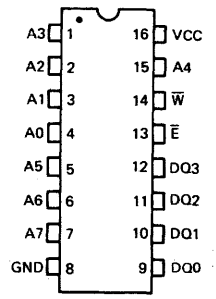
On chip latches are provided for address allowing for efficient interfacing with microprocessor systems. The data output buffers can be forced to a high impedance state for use in expanded memory arrays. The data inputs and outputs are multiplexed internally for common I/O bus compatibility.

The HM-6562 is a fully static RAM and may be maintained in any state for an indefinite period of time. Data retention supply voltage and supply current are guaranteed over temperature.

The HM-6611, 256 x 4 CMOS PROM, is pin for pin replaceable with the HM-6562. This allows a single memory board design with any organization of RAM and PROMs.

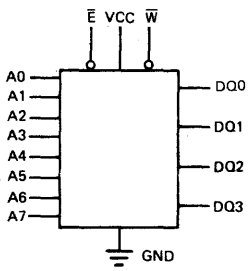
Pinout

TOP VIEW

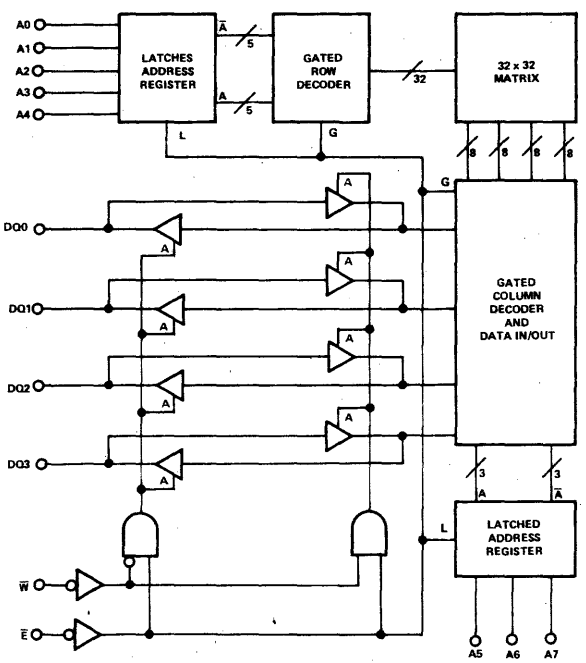


A – Address Input
$\overline{E}$ – Chip Enable
$\overline{W}$ – Write Enable
DQ – Data In/Out

Logic Symbol



Functional Diagram



ALL LINES POSITIVE LOGIC - ACTIVE HIGH

THREE STATE BUFFERS:
A HIGH ⟶ OUTPUT ACTIVE

ADDRESS LATCHES AND GATED DECODES
LATCH ON RISING EDGE OF L
GATE ON RISING EDGE OF G

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ABSOLUTE MAXIMUM RATINGS

Supply Voltage -VCC	+8.0V
Input or Output Voltage Applied	GND -0.3V to VCC +0.3V
Storage Temperature	-65°C to +150°C

OPERATING RANGE

Operating Supply Voltage -VCC	
Military (-2)	4.5V to 5.5V
Industrial (-9)	4.5V to 5.5V
Operating Temperature	
Military (-2)	-55°C to +125°C
Industrial (-9)	-40°C to +85°C

ELECTRICAL CHARACTERISTICS

	SYMBOL	PARAMETER	TEMP. & VCC = OPERATING RANGE MIN	TEMP. & VCC = OPERATING RANGE MAX	TEMP. = 25°C ① VCC = 5.0V MIN	TEMP. = 25°C ① VCC = 5.0V TYP	TEMP. = 25°C ① VCC = 5.0V MAX	UNITS	TEST CONDITIONS
D.C.	ICCSB	Standby Supply Current		10 1(+25°C)		0.1	1	μA	IO = 0 VI = VCC or GND
	ICCOP	Operating Supply Current ②		4		1.5	2.5	mA	f = 1MHz, IO = 0 VI = VCC or GND
	ICCDR	Data Retention Supply Current		10		0.01	1	μA	VCC = 3.0, IO = 0 VI = VCC or GND
	VCCDR	Data Retention Supply Voltage	2.0		2.0	1.4		V	
	II	Input Leakage Current	-1.0	+1.0	-0.5	0.0	+0.5	μA	GND ⩽ VI ⩽ VCC
	IIOZ	Input Output Leakage Current	-1.0	+1.0	-0.5	0.0	+0.5	μA	GND ⩽ VO ⩽ VCC
	VIL	Input Low Voltage	-0.3	0.8	-0.3	2.0	1.5	V	
	VIH	Input High Voltage	VCC -2.0	VCC +3.0	2.5	2.0	5.3	V	
	VOL	Output Low Voltage		0.4		0.2	0.35	V	IOL = 3.2mA
	VOH	Output High Voltage	2.4		3.0	4.5		V	IOH = -0.4mA
	CI	Input Capacitance ③		6		4	6	pF	VI = VCC or GND f = 1MHz
	CIO	Input Output Capacitance ③		10		6	10	pF	VO= VCC or GND f = 1MHz
A.C.	TELQV	Chip Enable Access Time		220		120	170	ns	④
	TAVQV	Address Access Time		220		110	170	ns	④
	TELQX	Chip Enable Output Enable Time		120		50	90	ns	④
	TWLQZ	Write Enable Output Disable Time		120		50	90	ns	④
	TEHQZ	Chip Enable Output Disable Time		120		50	90	ns	④
	TELEH	Chip Enable Pulse Negative Width	220		170	120		ns	④
	TEHEL	Chip Enable Pulse Positive Width	100		70	50		ns	④
	TAVEL	Address Setup Time	0		0	-10		ns	④
	TELAX	Address Hold Time	40		30	20		ns	④
	TDVWH	Data Setup Time	100		80	50		ns	④
	TWHDX	Data Hold Time	0		0	0		ns	④
	TWLDV	Write Data Delay Time	120		90	50		ns	④
	TWLEH	Chip Enable Write Pulse Setup Time	220		170	100		ns	④
	TELWH	Chip Enable Write Pulse Hold Time	220		170	100		ns	④
	TWLWH	Write Enable Pulse Width	220		170	100		ns	④
	TWLEL	Early Output High Z Time	0		0	-10		ns	④
	TEHWH	Late Output High Z Time	0		0	-10		ns	④
	TELEL	Read or Write Cycle Time	320		240	170		ns	④

NOTES:
1. All devices tested at worst case limits. Room temp., 5 volt data provided for information — not guaranteed.
2. Operating Supply Current (ICCOP) is proportional to Operating Frequency. Example: Typical ICCOP = 1.5mA/MHz.
3. Capacitance sampled and guaranteed — not 100% tested.
4. AC Test Conditions: Inputs — TRISE = TFALL = 20nsec; Outputs — 1 TTL load and 50pF. All timing measurements at 1/2 VCC.

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ABSOLUTE MAXIMUM RATINGS

Supply Voltage -VCC	+8.0V
Input or Output Voltage Applied	GND -0.3V to VCC +0.3V
Storage Temperature	-65°C to +150°C

OPERATING RANGE

Operating Supply Voltage -VCC	
Military (-2)	4.5V to 5.5V
Industrial (-9)	4.5V to 5.5V
Operating Temperature	
Military (-2)	-55°C to +125°C
Industrial (-9)	-40°C to +85°C

ELECTRICAL CHARACTERISTICS

	SYMBOL	PARAMETER	TEMP. & VCC = OPERATING RANGE MIN	TEMP. & VCC = OPERATING RANGE MAX	TEMP. = 25°C ① VCC = 5.0V MIN	TEMP. = 25°C ① VCC = 5.0V TYP	TEMP. = 25°C ① VCC = 5.0V MAX	UNITS	TEST CONDITIONS
D.C.	ICCSB	Standby Supply Current		10 1(+25°C)		1.0	1	μA	IO = 0 VI = VCC or GND
	ICCOP	Operating Supply Current ②		4		1.5	2.5	mA	f = 1MHz, IO = 0 VI = VCC or GND
	ICCDR	Data Retention Supply Current		10		0.1	1	μA	VCC = 3.0, IO = 0 VI = VCC or GND
	VCCDR	Data Retention Supply Voltage	2.0		2.0	1.4		V	
	II	Input Leakage Current	-1.0	+1.0	-0.5	0.0	+0.5	μA	GND ≤ VI ≤ VCC
	IIOZ	Input Output Leakage Current	-1.0	+1.0	-0.5	0.0	+0.5	μA	GND ≤ VO ≤ VCC
	VIL	Input Low Voltage	-0.3	0.8	-0.3	2.0	1.5	V	
	VIH	Input High Voltage	VCC -2.0	VCC +3.0	2.5	2.0	5.3	V	
	VOL	Output Low Voltage		0.4		0.2	0.35	V	IOL = 3.2mA
	VOH	Output High Voltage	2.4		3.0	4.5		V	IOH = -0.4mA
	CI	Input Capacitance ③		6		4	6	pF	VI = VCC or GND f = 1MHz
	CIO	Input Output Capacitance ③		10		6	10	pF	VO= VCC or GND f = 1MHz
A.C.	TELQV	Chip Enable Access Time		300		160	240	ns	④
	TAVQV	Address Access Time		300		150	240	ns	④
	TELQX	Chip Enable Output Enable Time		150		60	120	ns	④
	TWLQZ	Write Enable Output Disable Time		150		60	120	ns	④
	TEHQZ	Chip Enable Output Disable Time		150		60	120	ns	④
	TELEH	Chip Enable Pulse Negative Width	300		240	160		ns	④
	TEHEL	Chip Enable Pulse Positive Width	100		70	50		ns	④
	TAVEL	Address Setup Time	0		0	-10		ns	④
	TELAX	Address Hold Time	50		40	30		ns	④
	TDVWH	Data Setup Time	150		120	100		ns	④
	TWHDX	Data Hold Time	0		0	0		ns	④
	TWLDV	Write Data Delay Time	150		120	60		ns	④
	TWLEH	Chip Enable Write Pulse Setup Time	300		240	160		ns	④
	TELWH	Chip Enable Write Pulse Hold Time	300		240	160		ns	④
	TWLWH	Write Enable Pulse Width	300		240	160		ns	④
	TWLEL	Early Output High Z Time	0		0	-10		ns	④
	TEHWH	Late Output High Z Time	0		0	-10		ns	④
	TELEL	Read or Write Cycle Time	400		310	210		ns	④

NOTES:
1. All devices tested at worst case limits. Room temp., 5 volt data provided for information — not guaranteed.
2. Operating Supply Current (ICCOP) is proportional to Operating Frequency. Example: Typical ICCOP = 1.5mA/MHz.
3. Capacitance sampled and guaranteed — not 100% tested.
4. AC Test Conditions: Inputs — TRISE = TFALL = 20nsec; Outputs — 1 TTL load and 50pF. All timing measurements at 1/2 VCC.

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ABSOLUTE MAXIMUM RATINGS		OPERATING RANGE	
Supply Voltage -VCC	+8.0V	Operating Supply Voltage -VCC Commercial	4.75V to 5.25V
Applied Input or Output Voltage	GND -0.3V VCC +0.3V		
Storage Temperature	-65°C to +150°C	Operating Temperature Commercial	0°C to 75°C

ELECTRICAL CHARACTERISTICS

	SYMBOL	PARAMETER	TEMP. & VCC = OPERATING RANGE MIN	TEMP. & VCC = OPERATING RANGE MAX	TEMP. = 25°C ① VCC = 5.0V MIN	TYP	MAX	UNITS	TEST CONDITIONS
	ICCSB	Standby Supply Current		100		10	100	μA	IO = 0 VI = VCC or GND
	ICCOP	Operating Supply Current ②		4		1.5	2.5	mA	f = 1MHz, IO = 0 VI = VCC or GND
	VCCDR	Data Retention Supply Voltage	2.0		2.0			V	
D.C.	II	Input Leakage Current	-1.0	+1.0	-0.5	0.0	+0.5	μA	GND ≤ VI ≤ VCC
	IIOZ	Input Output Leakage Current	-1.0	+1.0	-0.5	0.0	+0.5	μA	GND ≤ VO ≤ VCC
	VIL	Input Low Voltage	-0.3	0.8	-0.3	2.0	1.5	V	
	VIH	Input High Voltage	VCC -2.0	VCC +3.0	2.5	2.0	5.3	V	
	VOL	Output Low Voltage		0.4		0.2	0.35	V	IOL = 1.6mA
	VOH	Output High Voltage	2.4		3.0	4.5		V	IOH = -0.2mA
	CI	Input Capacitance ③		6		4	6	pF	VI = VCC or GND f = 1MHz
	CIO	Input Output Capacitance ③		10		6	10	pF	VO = VCC or GND f = 1MHz
	TELQV	Chip Enable Access Time		350		200	300	ns	④
	TAVQV	Address Access Time		360		200	310	ns	④
	TELQX	Chip Enable Output Enable Time		180		80	160	ns	④
	TWLQZ	Write Enable Output Disable Time		180		80	160	ns	④
	TEHQZ	Chip Enable Output Disable Time		180		80	160	ns	④
	TELEH	Chip Enable Pulse Negative Width	350		300	200		ns	④
	TEHEL	Chip Enable Pulse Positive Width	150		130	90		ns	④
A.C.	TAVEL	Address Setup Time	10		10	0		ns	④
	TELAX	Address Hold Time	70		50	40		ns	④
	TDVWH	Data Setup Time	170		140	120		ns	④
	TWHDX	Data Hold Time	0		0	0		ns	④
	TWLDV	Write Data Delay Time	180		160	80		ns	④
	TWLEH	Chip Enable Write Pulse Setup Time	350		300	200		ns	④
	TELWH	Chip Enable Write Pulse Hold Time	350		300	200		ns	④
	TWLWH	Write Enable Pulse Width	350		300	200		ns	④
	TWLEL	Early Output High Z Time	0		0	-10		ns	④
	TEHWH	Late Output High Z Time	0		0	-10		ns	④
	TELEL	Read or Write Cycle Time	500		330	290		ns	④

NOTES:
1. All devices tested at worst case limits. Room temp., 5 volt data provided for information — not guaranteed.
2. Operating Supply Current (ICCOP) is proportional to Operating Frequency. Example: Typical ICCOP = 1.5mA/MHz.
3. Capacitance sampled and guaranteed — not 100% tested.
4. AC Test Conditions: Inputs — TRISE = TFALL = 20nsec; Outputs — 1 TTL load and 50pF. All timing measurements at 1/2 VCC.

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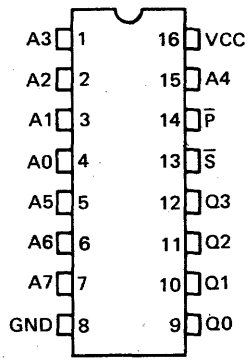
HM-6611
1024-BIT FIELD-PROGRAMMABLE CMOS PROM

Features

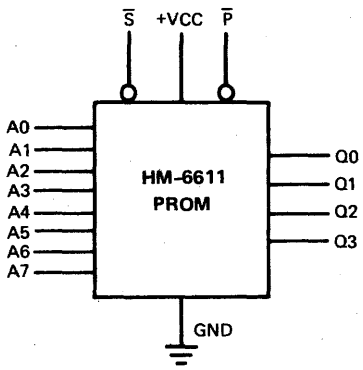
- FUSED LINK PROM
- FIELD-PROGRAMMABLE
- ORGANIZED 256 x 4
- LOW POWER STANDBY 0.1mW
- LOW POWER ENABLED 10mW
- CMOS RAM PINOUT EXCEPT FOR $\overline{P}$
- TTL COMPATIBLE IN/OUT
- THREE STATE OUTPUTS
- FULLY STATIC OPERATION
- FAST ACCESS TIME . . . . . 450nsec MAX
- HIGH NOISE IMMUNITY
- HIGH RELIABILITY
- MILITARY TEMPERATURE RANGE
- INDUSTRIAL TEMPERATURE RANGE
- 10 VOLT VERSION AVAILABLE

Pinout

TOP VIEW



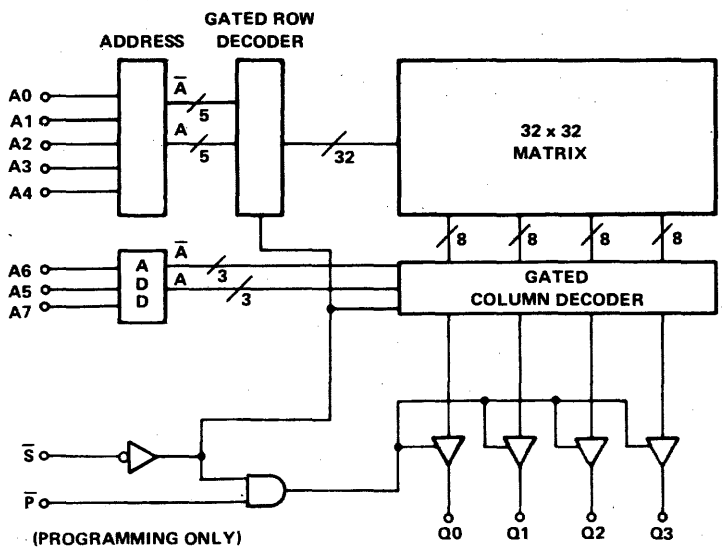
Logic Symbol



Description

The HM-6611 is a part of a family of fusible link CMOS PROMs featuring three state outputs. This device is static, TTL compatible, and has a 100 μA maximum standby current over temperature at a VCC of 5 volts. 10V and full military temperature devices are available. Chip Select ($\overline{S}$) is used to place the device in the standby state and also forces the outputs into the high impedance state when it is high. Program Enable ($\overline{P}$) is used only during programming, and must be connected to VCC in the system. Pinout is similar to Bipolar PROMs and is pin for pin replaceable with the HM-6562, a 256 x 4 CMOS RAM, if $\overline{P}$ is tied to VCC. This allows a single memory board design with any organization of RAM and PROM.

Functional Diagram



"SEE PAGES 1409-1415 FOR PACKAGE SELECTION GUIDE"

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ABSOLUTE MAXIMUM RATINGS		OPERATING RANGE	
Supply Voltage - VCC	+12.0V	Operating Supply Voltage -VCC ⑥	
Input or Output Voltage Applied	GND -0.3V to VCC +0.3V	Military (-2)	9V to 11V
Storage Temperature	-65°C to +150°C	Industrial (-9)	9.5V to 10.5V
		Operating Temperature	
		Military (-2)	-55°C to +125°C
		Industrial (-9)	-40°C to +85°C

ELECTRICAL CHARACTERISTICS

	SYMBOL	PARAMETER	TEMP. & VCC = OPERATING RANGE MIN	TEMP. & VCC = OPERATING RANGE MAX	TEMP. = 25°C ① VCC = 10.0V MIN	TEMP. = 25°C ① VCC = 10.0V TYP	TEMP. = 25°C ① VCC = 10.0V MAX	UNITS	TEST CONDITIONS
D.C.	ICCSB	Standby Supply Current		500		50	200	μA	VI = VCC or GND $\overline{S}$ = VCC
	ICCEN	Enabled Supply Current ②		25		5	15	mA	VI = VCC or GND $\overline{S}$ = GND, IO = 0
	II	Input Leakage Current ③	-1.0	+1.0	-0.5	0.0	+0.5	μA	GND≤VI≤VCC
	IOZ	Output Leakage Current	-10.0	+10.0	-5.0	±0.5	+5.0	μA	GND≤VO≤VCC
	VIL	Input Low Voltage	-0.3	1.8	-0.3	3.5	2.5	V	
	VIH	Input High Voltage	7.7	VCC + 0.3	5.5	3.5	10.3	V	
	VOL	Output Low Voltage		1.0		0.2	0.5	V	IO = 2.0mA
	VOH	Output High Voltage	8.0		8.5	9.5		V	IO = -2.0mA
	CI	Input Capacitance ③ ④		8.0		5.0	8.0	pF	VI = VCC or GND f = 1MHz
	CO	Output Capacitance ③ ④		10.0		8.0	10.0	pF	VO = VCC or GND f = 1MHz
A.C.	TAVQV	Address Access Time		350		200	250	ns	⑤
	TSLQV	Chip Select Access Time		400		250	300	ns	⑤
	TSLQX	Chip Select Output Enable Time		70		20	50	ns	⑤
	TSHQZ	Chip Select Output Disable Time		70		20	50	ns	⑤

NOTES:

1. All devices tested at worst case limits. Room temperature 10 volt data provided for information - not guaranteed.
2. ICCEN is proportional to the number of unblown fuses per word addressed. If all four fuses in the word addressed are blown ICCEN ≈ ICCSB.
3. Except $\overline{P}$. Program Enable is used only during programming and it's characteristics are accounted for in the programming specifications.
4. Capacitance is sampled and guaranteed, but not 100% tested.
5. AC test conditions: Inputs - TRISE = TFALL = 20nsec; Outputs - 100KΩ and 50pF to ground; Timing measured at ½VCC.
6. The HM-6611A will also meet the HM-6611 specifications when operated within the HM-6611 operating range.

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ABSOLUTE MAXIMUM RATINGS		OPERATING RANGE	
Supply Voltage - VCC	+12.0V	Operating Supply Voltage -VCC	
Input or Output Voltage Applied	GND -0.3V to VCC +0.3V	Military (-2)	4.5V to 5.5V
Storage Temperature	-65°C to +150°C	Industrial (-9)	4.5V to 5.5V
		Operating Temperature	
		Military (-2)	-55°C to +125°C
		Industrial (-9)	-40°C to +85°C

ELECTRICAL CHARACTERISTICS

	SYMBOL	PARAMETER	TEMP. & VCC = OPERATING RANGE MIN	TEMP. & VCC = OPERATING RANGE MAX	TEMP. = 25°C ① VCC = 5.0V MIN	TEMP. = 25°C ① VCC = 5.0V TYP	TEMP. = 25°C ① VCC = 5.0V MAX	UNITS	TEST CONDITIONS
D.C.	ICCSB	Standby Supply Current		100		5	20	μA	$\overline{S}$ = VCC
	ICCEN	Enabled Supply Current ②		10		2	5	mA	$\overline{S}$ = GND, IO = 0
	II	Input Leakage Current ③	-1.0	+1.0	-0.5	0.0	+0.5	μA	GND≤VI≤VCC
	IOZ	Output Leakage Current	-1.0	+1.0	-0.5	0.0	+0.5	μA	GND≤VO≤VCC
	VIL	Input Low Voltage	-0.3	0.8	-0.3	2.0	1.5	V	
	VIH	Input High Voltage	VCC - 2.0	VCC + 0.3	2.5	2.0	5.3	V	
	VOL	Output Low Voltage		0.4		0.3	0.35	V	IO = 2.0mA
	VOH	Output High Voltage	2.4		3.5	4.0		V	IO = -1.0mA
	CI	Input Capacitance ③ ④		8.0		5.0	8.0	pF	VI = VCC or GND f = 1MHz
	CO	Output Capacitance ③ ④		10.0		6.0	10.0	pF	VO = VCC or GND f = 1MHz
A.C.	TAVQV	Address Access Time		450		300	350	ns	⑤
	TSLQV	Chip Select Access Time		500		350	400	ns	⑤
	TSLQX	Chip Select Output Enable Time		150		70	120	ns	⑤
	TSHQZ	Chip Select Output Disable Time		150		70	120	ns	⑤

NOTES:

1. All devices tested at worst case limits. Room temperature 10 volt data provided for information - not guaranteed.
2. ICCEN is proportional to the number of unblown fuses per word addressed. If all four fuses in the word addressed are blown ICCEN ≈ ICCSB.
3. Except $\overline{P}$. Program Enable is used only during programming and it's characteristics are accounted for in the programming specifications.
4. Capacitance is sampled and guaranteed, but not 100% tested.
5. AC test conditions: Inputs - TRISE = TFALL = 20nsec; Outputs - 50pF and 1TTL load; Timing measured at ½VCC.

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ABSOLUTE MAXIMUM RATINGS		OPERATING RANGE	
Supply Voltage - VCC	+12.0V	Operating Supply Voltage -VCC Commercial	4.75V to 5.25V
Input or Output Voltage Applied	GND -0.3V to VCC +0.3V	Operating Temperature Commercial	0°C to 75°C
Storage Temperature	-65°C to +150°C		

ELECTRICAL CHARACTERISTICS

	SYMBOL	PARAMETER	TEMP. & VCC = OPERATING RANGE MIN	TEMP. & VCC = OPERATING RANGE MAX	TEMP. = 25°C ① VCC = 5.0V MIN	TEMP. = 25°C ① VCC = 5.0V TYP	TEMP. = 25°C ① VCC = 5.0V MAX	UNITS	TEST CONDITIONS
D.C.	ICCSB	Standby Supply Current		1.0		0.2	1.0	mA	$\overline{S}$ = VCC
	ICCEN	Enabled Supply Current ②		25		5	25	mA	$\overline{S}$ = GND, IO = 0
	II	Input Leakage Current ③	-10.0	+10.0	-7.0	±0.5	+7.0	μA	GND≤VI≤VCC
	IOZ	Output Leakage Current	-10.0	+10.0	-7.0	±0.5	+7.0	μA	GND≤VO≤VCC
	VIL	Input Low Voltage	-0.3	0.8	-0.3	2.0	1.5	V	
	VIH	Input High Voltage	VCC - 2.0	VCC + 0.3	2.5	2.0	5.3	V	
	VOL	Output Low Voltage		0.4		0.3	0.35	V	IO = 1.0mA
	VOH	Output High Voltage	2.4		3.5	4.0		V	IO = -0.5mA
	CI	Input Capacitance ③ ④		8.0		5.0	8.0	pF	VI = VCC or GND f = 1MHz
	CO	Output Capacitance ③ ④		10.0		6.0	10.0	pF	VO = VCC or GND f = 1MHz
A.C.	TAVQV	Address Access Time		650		400	550	ns	⑤
	TSLQV	Chip Select Access Time		800		500	650	ns	⑤
	TSLQX	Chip Select Output Enable Time		250		100	200	ns	⑤
	TSHQZ	Chip Select Output Disable Time		250		100	200	ns	⑤

NOTES:

1. All devices tested at worst case limits. Room temperature 10 volt data provided for information - not guaranteed.
2. ICCEN is proportional to the number of unblown fuses per word addressed. If all four fuses in the word addressed are blown ICCEN ≈ ICCSB.
3. Except $\overline{P}$. Program Enable is used only during programming and it's characteristics are accounted for in the programming specifications.
4. Capacitance is sampled and guaranteed, but not 100% tested.
5. AC test conditions: Inputs - TRISE = TFALL = 20nsec; Outputs - 50pF and 1TTL load; Timing measured at ½VCC.

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HM-6661

1024-BIT FIELD PROGRAMMABLE CMOS PROM

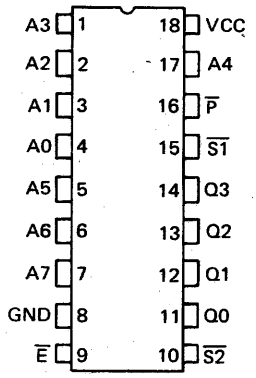
Advance Information

Features

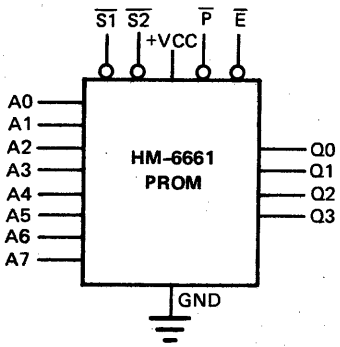
- FUSED LINK PROM
- FIELD-PROGRAMMABLE
- ORGANIZED 256 x 4
- LOW POWER STANDBY 0.1mW
- CMOS RAM PINOUT EXCEPT FOR $\overline{P}$
- TTL COMPATIBLE IN/OUT
- THREE STATE OUTPUTS
- SYNCHRONOUS OPERATION
- FAST ACCESS TIME . . . . . 450 nsec MAX
- HIGH NOISE IMMUNITY
- HIGH RELIABILITY
- MILITARY TEMPERATURE RANGE
- INDUSTRIAL TEMPERATURE RANGE
- 10 VOLT VERSION AVAILABLE

Pinout

TOP VIEW



Logic Symbol



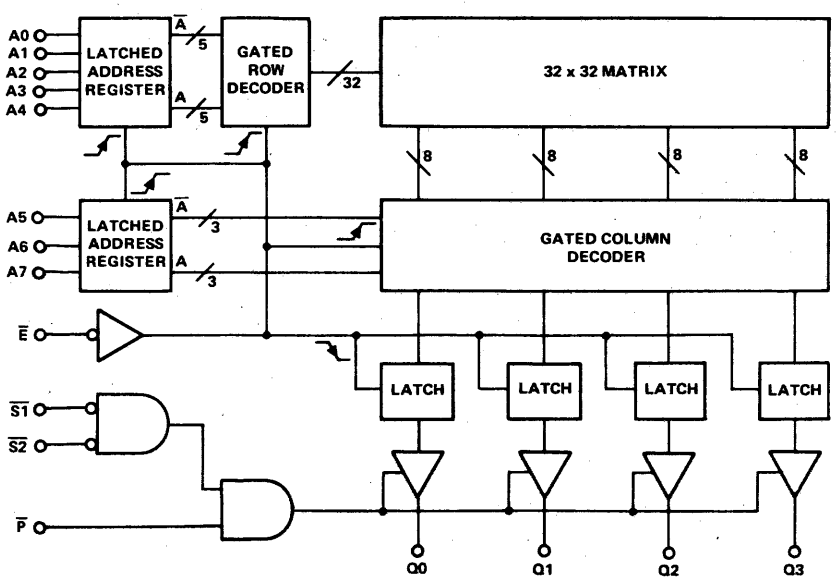
Description

The HM-6661 is a 256 x 4 static CMOS PROM fabricated using self-aligned silicon gate technology. Synchronous circuit techniques are employed to achieve high performance and low power operation.

On chip latches are provided for address and data outputs allowing efficient interfacing with microprocessor systems. The data output buffers can be forced to a high impedance state for use in expanded memory arrays.

The HM-6661 employs polysilicon fuses as static memory elements. It is also pin for pin replaceable with the HM-6561, a 256 x 4 CMOS RAM, if P is tied to VCC. This allows a single memory board design with any organization of RAM and PROM.

Functional Diagram



"SEE PAGES 1409-1415 FOR PACKAGE SELECTION GUIDE"

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MONOLITHIC DIODE MATRICES

Features

- FIELD PROGRAMMABLE
- CMOS COMPATIBLE
- ZERO POWER DISSIPATION
- FAST SWITCHING
- FIVE POPULAR ORGANIZATIONS

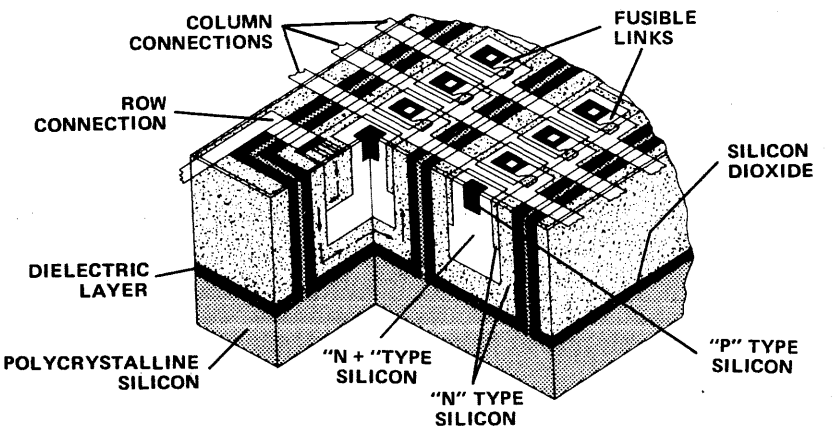
Description

Designed with the CMOS circuit engineer in mind, these versatile diode matrices allow the application of logically powerful programmable solutions to low power CMOS system applications.

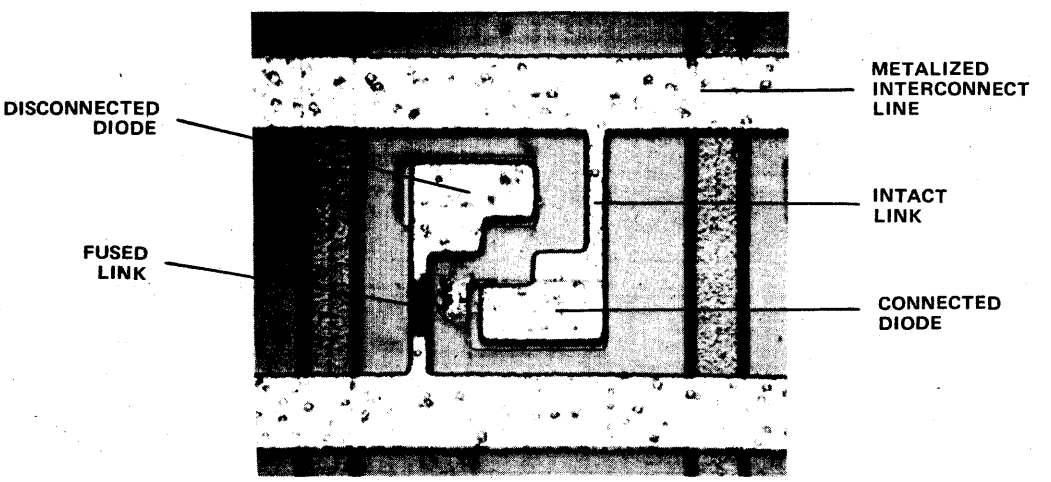
These devices incorporate an advanced dielectric isolation process to eliminate the need for power supply pins and allow parasitic free operation.

Programming is accomplished by cleanly vaporizing a fusible link by application of a brief high voltage pulse to a selected array element. This operation open circuits a row to column orring diode eliminating their former interaction.

Monolithic Structure



Fusible Link System



"SEE PAGES 1409-1415 FOR PACKAGE SELECTION GUIDE"

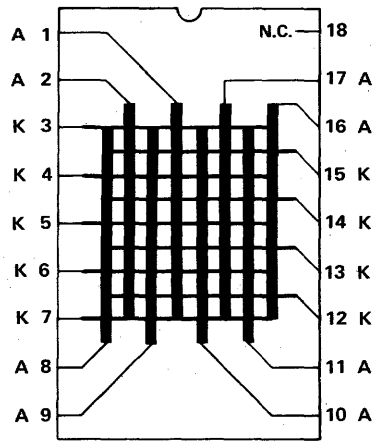
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Monolithic Diode Matrices

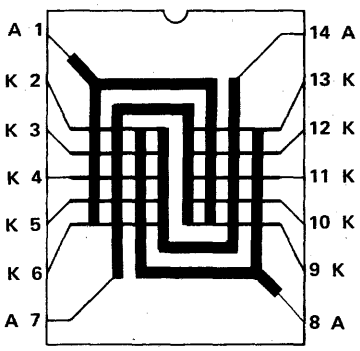
HM-0168 6 x 8 DIODE MATRICES
HM-0186 8 x 6 DIODE MATRICES
HM-0410 4 x 10 DIODE MATRICES
HM-0104 10 x 4 DIODE MATRICES
HM-0198 9 x 8 DIODE MATRICES

NOTE: Anodes are bold lines.

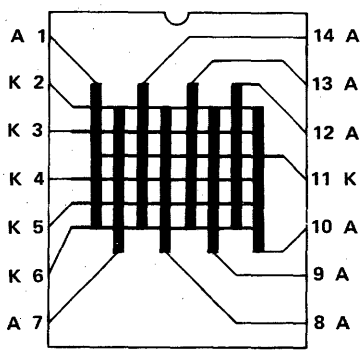
HM-0198



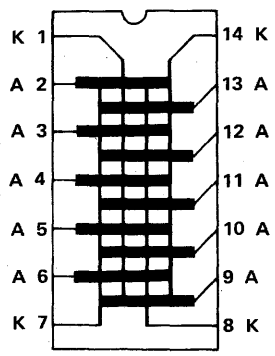
HM-0104



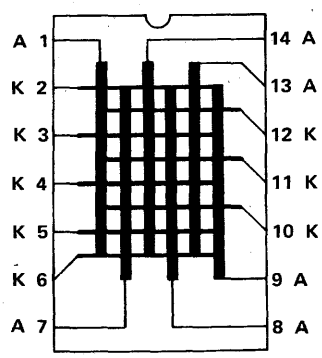
HM-0168



HM-0410



HM-0186



CUSTOM PATTERNS

When ordering a matrix with a custom pattern: Send a paper tape, or copy a matrix pattern and circle out those diodes to be removed from the matrix. Another method to clearly identify a pattern is to call out respective anode and cathode for each diode to be removed, by package pin number.

ABSOLUTE MAXIMUM RATINGS

Forward Current	100mA
Surge Current (100 μs Max.)	200mA
Total Ckt. Dissipation (Still Air)	450mW
Storage Temperature (Ambient)	-65°C to +150°C

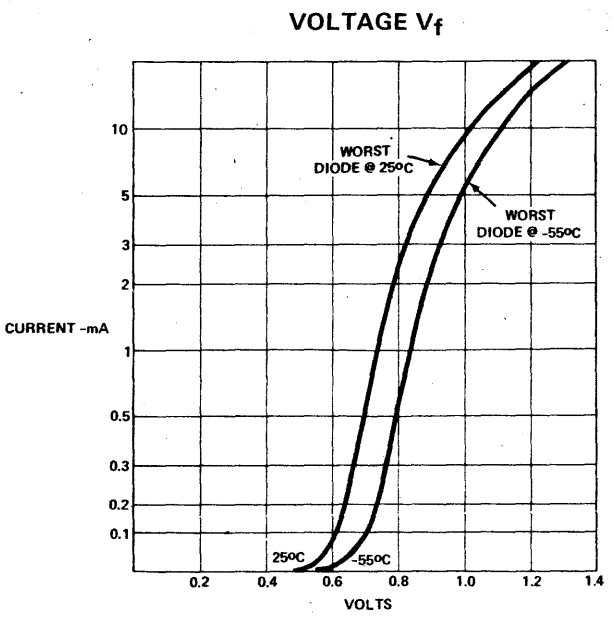
Maximum Ratings are limiting values above which permanent damage may occur.

ELECTRICAL CHARACTERISTICS

		HM-0XXX-5		HM-0XXX-2 HM-0XXX-8			
	T_A	0°C to +75°C		-55°C to +125°C			
SYMBOL	PARAMETER	MIN	MAX	MIN	MAX	UNITS	CONDITIONS
V_F	Forward Voltage		1.5 0.9		1.5 .9	V V	I_F = 20mA I_F = 1mA
BV_R	Reverse Breakdown Voltage	20		30		V	I_{BV} = 100μA
		25°C		25°C			
t_{rr}	Reverse Recovery Time		100		50	ns	I_F = 10mA to I_R = 10mA Recovery to 1mA
C_C	Crosspoint Capacitance				8	pF	V_R = 5V; f = 1MHz (1)

(1) $C_C \propto \frac{1}{V_{BIAS}}$

TYPICAL PERFORMANCE CURVES



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Selection Guide

PRODUCT	1* CERDIP	3* EPOXY	9* CERPACK
HM-0104	4U		9H
HM-0168	4U		9H
HM-0186	4U		9H
HM-0198			8C
HM-0410	4U		9H
HM-6312	4G	3D	8C
HM-6388 (Preliminary)			
HM-6389 (Preliminary)			
HD-6431	4Z	3G	8B
HD-6432	4N	3D	8C
HD-6433	4Z	3G	8B
HD-6440	4N	3D	8C
HD-6495	4Z	3G	8B
HD-6600	4D		
HM-6501	4M	3E	8E
HM-6503	5B	3D	8H
HM-6504 †	5B	3D	8H
HM-6508	4P	3G	8B
HM-6512	4N	3D	8C
HM-6513	5B	3D	8C
HM-6514 †	5B	3D	8C
HM-6518 †	4N	3D	8C
HM-6533	4M	3E	8K
HM-6543	4M	3E	8K
HM-6551	4M	3E	8E
HM-6561 †	4N	3D	8C
HM-6562	4P	3G	8B
HM-6611	5C		8B
HM-6661	4N		8C
JAN-0512	4K		
HM-7602	4Z	3G	8B
HM-7603	4Z	3G	8B
HM-76LS03	4Z	3G	8B
HM-7608	4K	3F	8F
HM-7610	4Z	3G	8B
HM-7610A	4Z	3G	8B
HM-7611	4Z	3G	8B
HM-7611A	4Z	3G	8B
HM-7616	5A		8L
HM-7620	4Z	3G	8B
HM-7620A	4Z	3G	8B
HM-7621	4Z	3G	8B
HM-7621A	4Z	3G	8B
HM-7625R	4K	3F	8F
HM-7629	4K	3F	8F
HM-7640	4K	3F	8F
HM-7640A	4K	3F	8F
HM-7640AR	4K	3F	8F

* These package numbers to be used in product ordering. Other numbers shown in Selection Guide and drawings are internal package numbers.

† Available in Leadless Carriers. See page 6-19.

(Continued)

PRODUCT	1* CERDIP	3* EPOXY	9* CERPACK
HM-7641	4K	3F	8F
HM-7641AR	4K	3F	8F
HM-7642	4N	3D	8C
HM-7642A	4N	3D	8C
HM-7642P	4N	3D	8C
HM-7643	4N	3D	8C
HM-7643A	4N	3D	8C
HM-7643P	4N	3D	8C
HM-7644	4P	3K	8C
HM-7644A	4P	3K	8C
HM-7647R	4K	3F	8F
HM-7648	4L	3N	8D
HM-7649	4L	3N	8D
HM-7680	4K	3F	8F
HM-7680R	4K	3F	8F
HM-7680P	4K	3F	8F
HM-7680RP	4K	3F	8F
HM-7681	4K	3F	8F
HM-7681R	4K	3F	8F
HM-7681P	4K	3F	8F
HM-7681RP	4K	3F	8F
HM-7683	4L		8J
HM-7684	5E		8H
HM-7684P	5E		8H
HM-7685	5E		8H
HM-7685P	5E		8H
HM-7686	4L		8J
HM-7686R	4L		8J
HM-7686P	4L		8J
HM-7686RP	4L		8J
HM-7687	4L		8J
HM-7687R	4L		8J
HM-7687P	4L		8J
HM-7687RP	4L		8J
HM-76160	5A		8L
HM-76161	5A		8L

† Available in Leadless Carriers. See page 6-19.

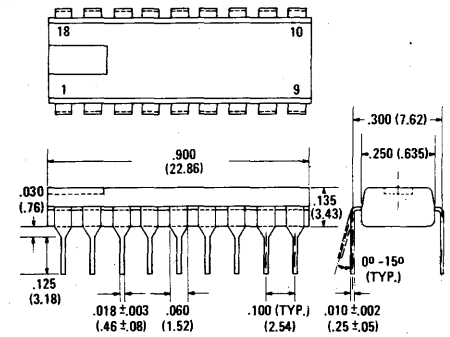
NOTE FOR PACKAGE DRAWINGS ON FOLLOWING PAGES:

1. All dimensions in inches; millimeters are shown in parentheses.
2. All dimensions ± .010 (± 0.25mm) unless otherwise shown.
3. Internal package codes are shown in black squares.

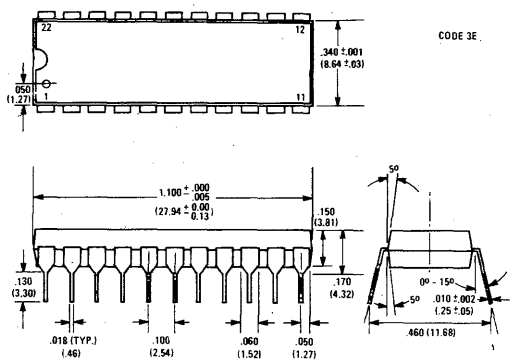
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Package Dimensions

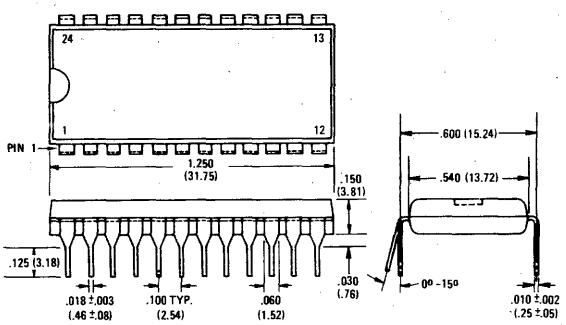
3D — 18 LEAD EPOXY



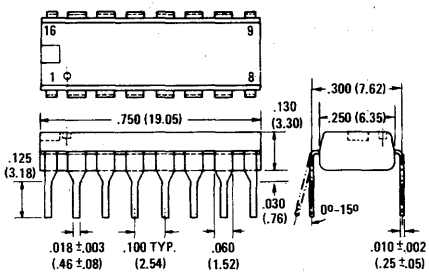
3E — 22 LEAD EPOXY



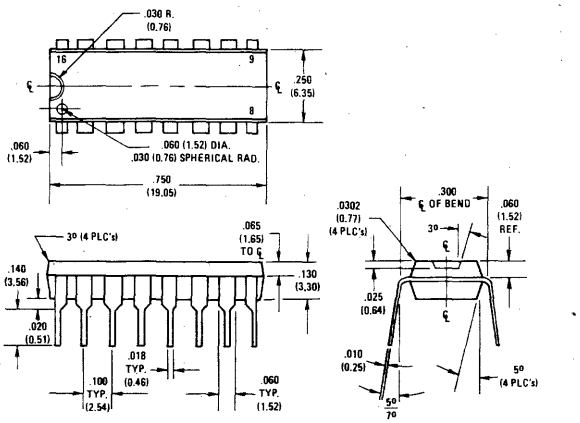
3F — 24 LEAD EPOXY



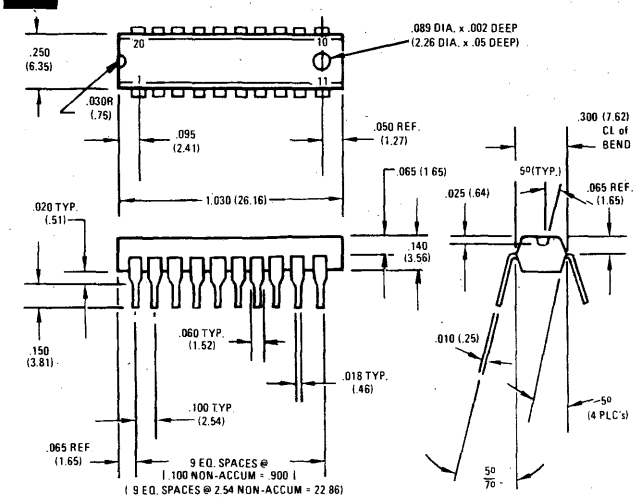
3G — 16 LEAD EPOXY



3K — 16 LEAD EPOXY

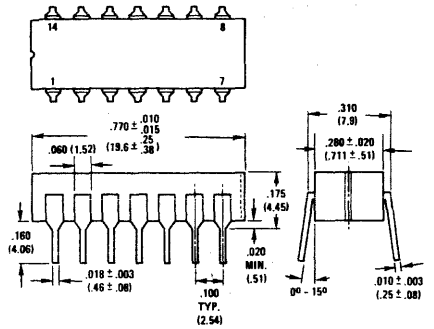


3N — 20 LEAD EPOXY

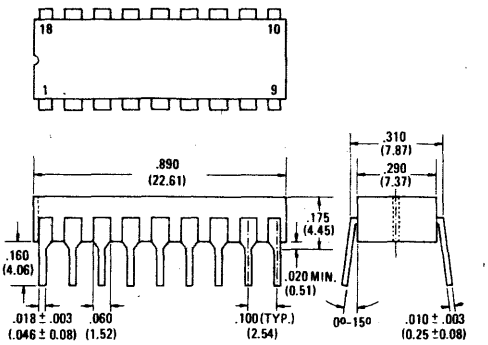


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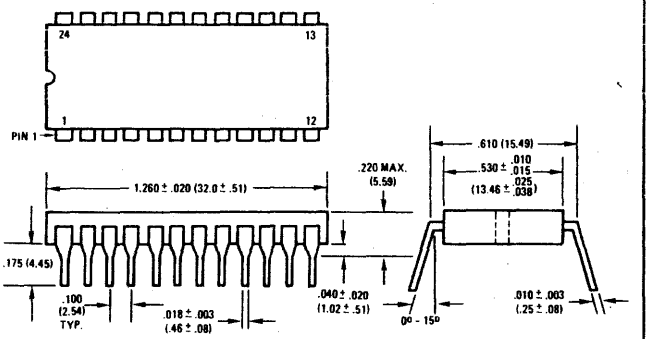
4D 5D — 14 LEAD CERDIP



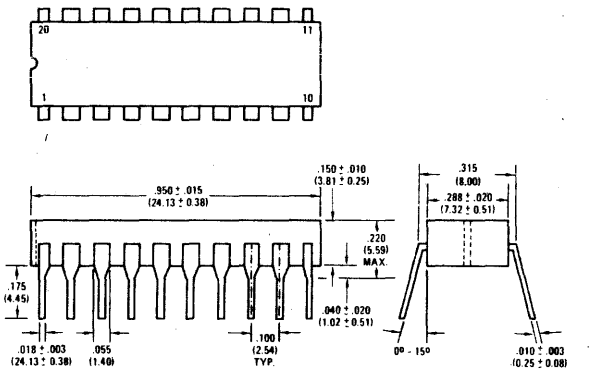
4G 4N 5B 5E — 18 LEAD CERDIP



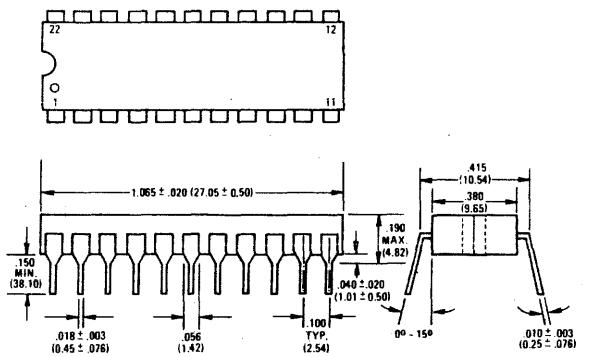
4K 5A — 24 LEAD CERDIP



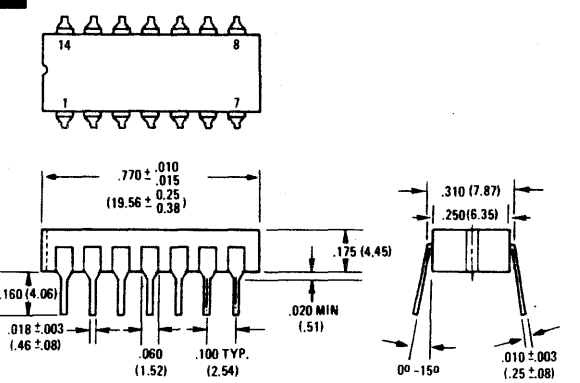
4L — 20 LEAD CERDIP



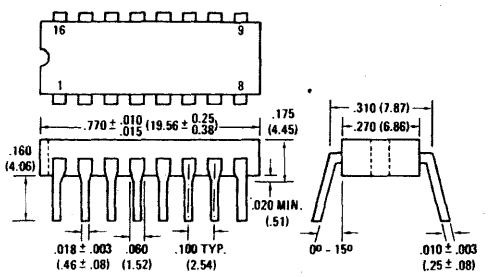
4M — 22 LEAD CERDIP



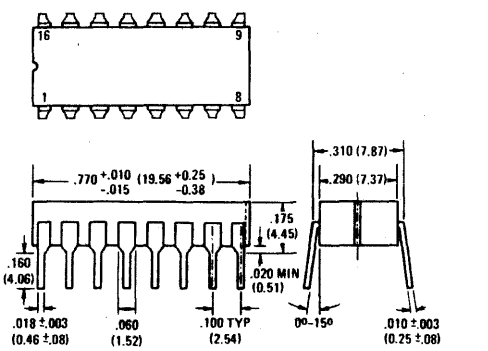
4U — 14 LEAD CERDIP



4Z — 16 LEAD CERDIP

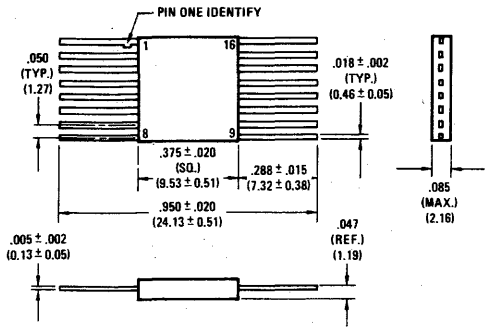


5C — 16 LEAD CERDIP

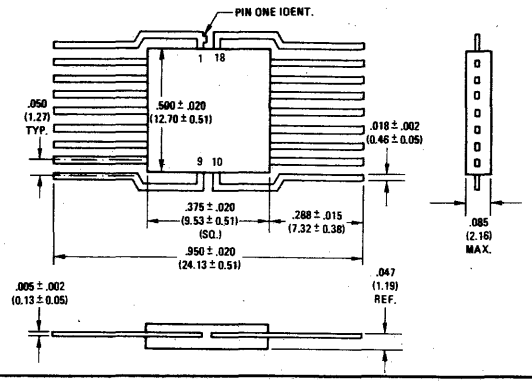


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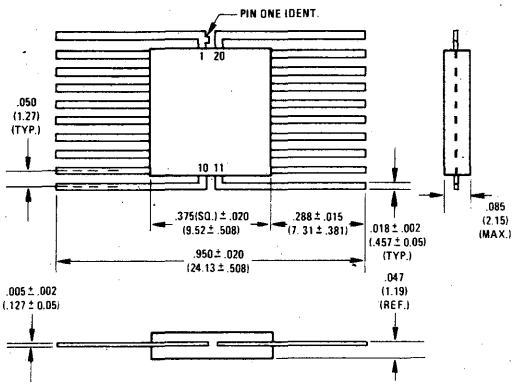
8B 16 LEAD CERPACK



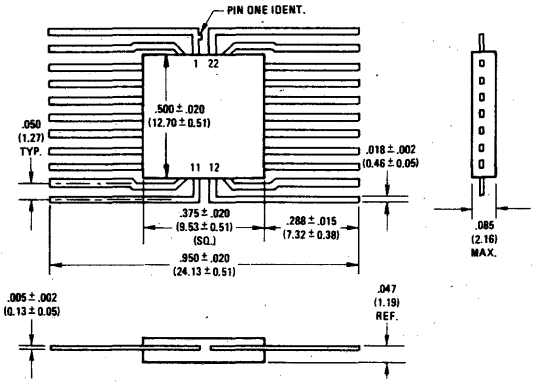
8C 18 LEAD CERPACK



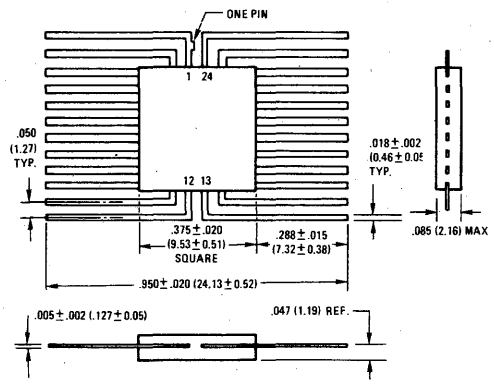
8D 20 LEAD CERPACK



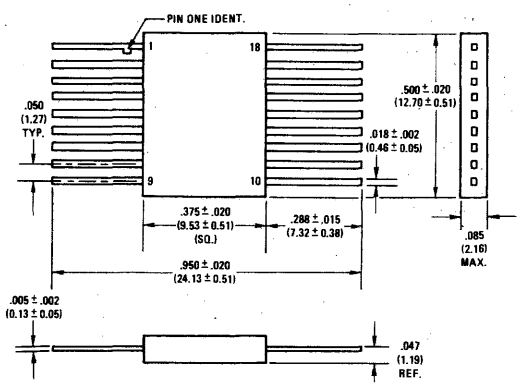
8E 22 LEAD CERPACK



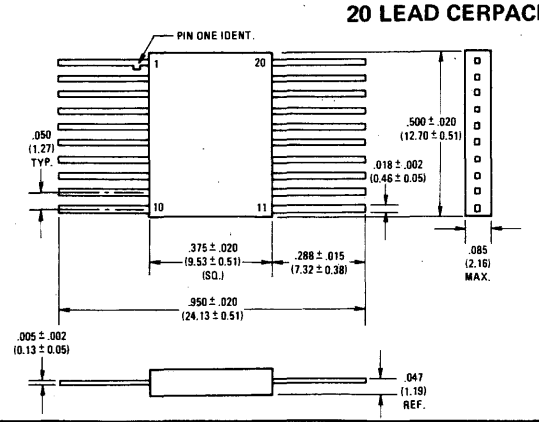
8F 24 LEAD CERPACK



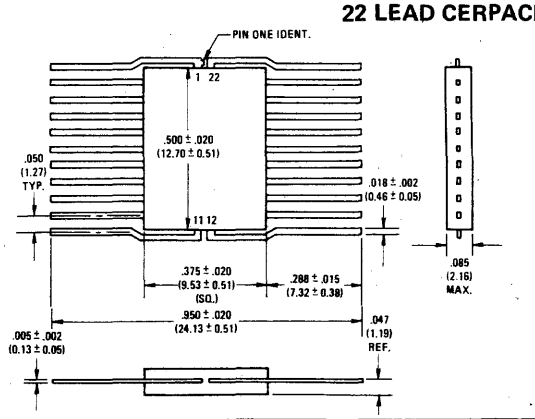
8H 18 LEAD CERPACK



8J 20 LEAD CERPACK

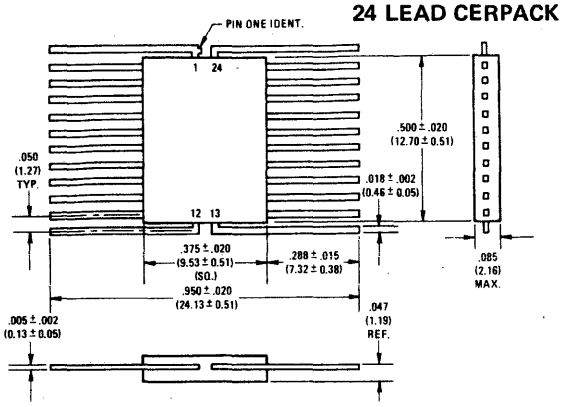


8K 22 LEAD CERPACK

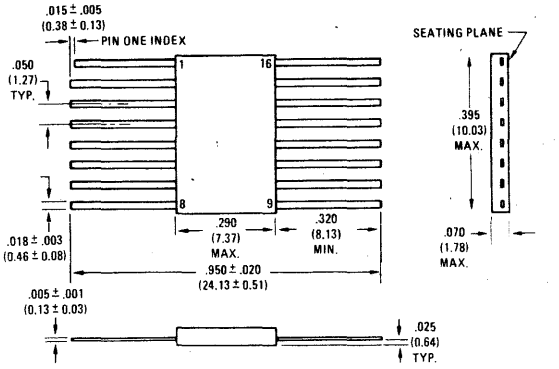


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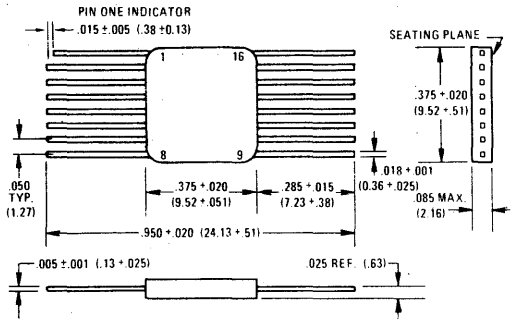
8L — 24 LEAD CERPACK



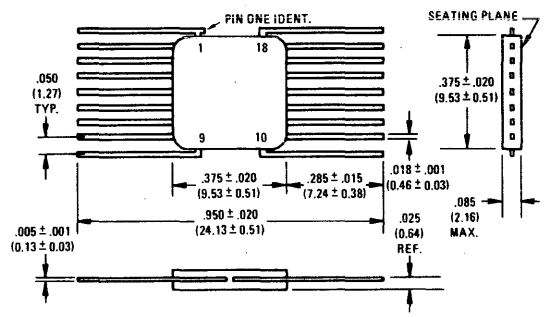
9B — 16 LEAD FLATPACK



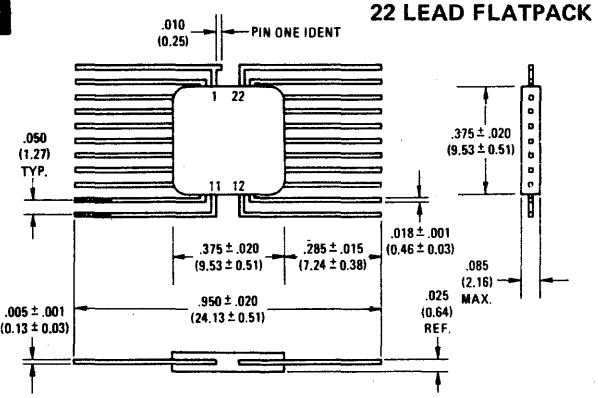
9C — 16 LEAD FLATPACK



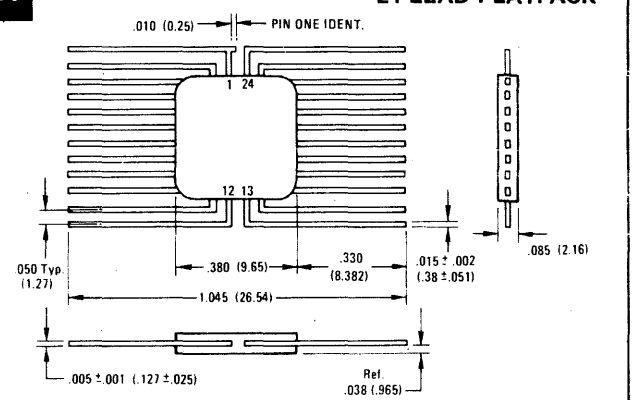
9D — 18 LEAD FLATPACK



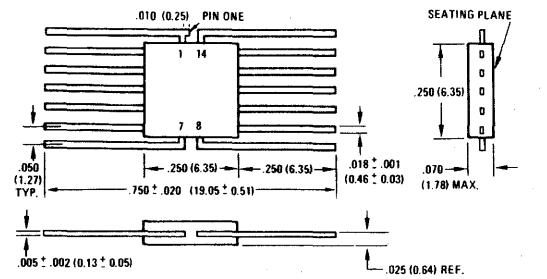
9E — 22 LEAD FLATPACK



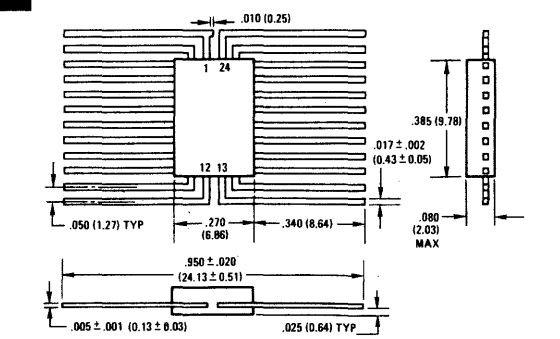
9F — 24 LEAD FLATPACK



9H — 14 LEAD FLATPACK



9M — 24 LEAD FLATPACK



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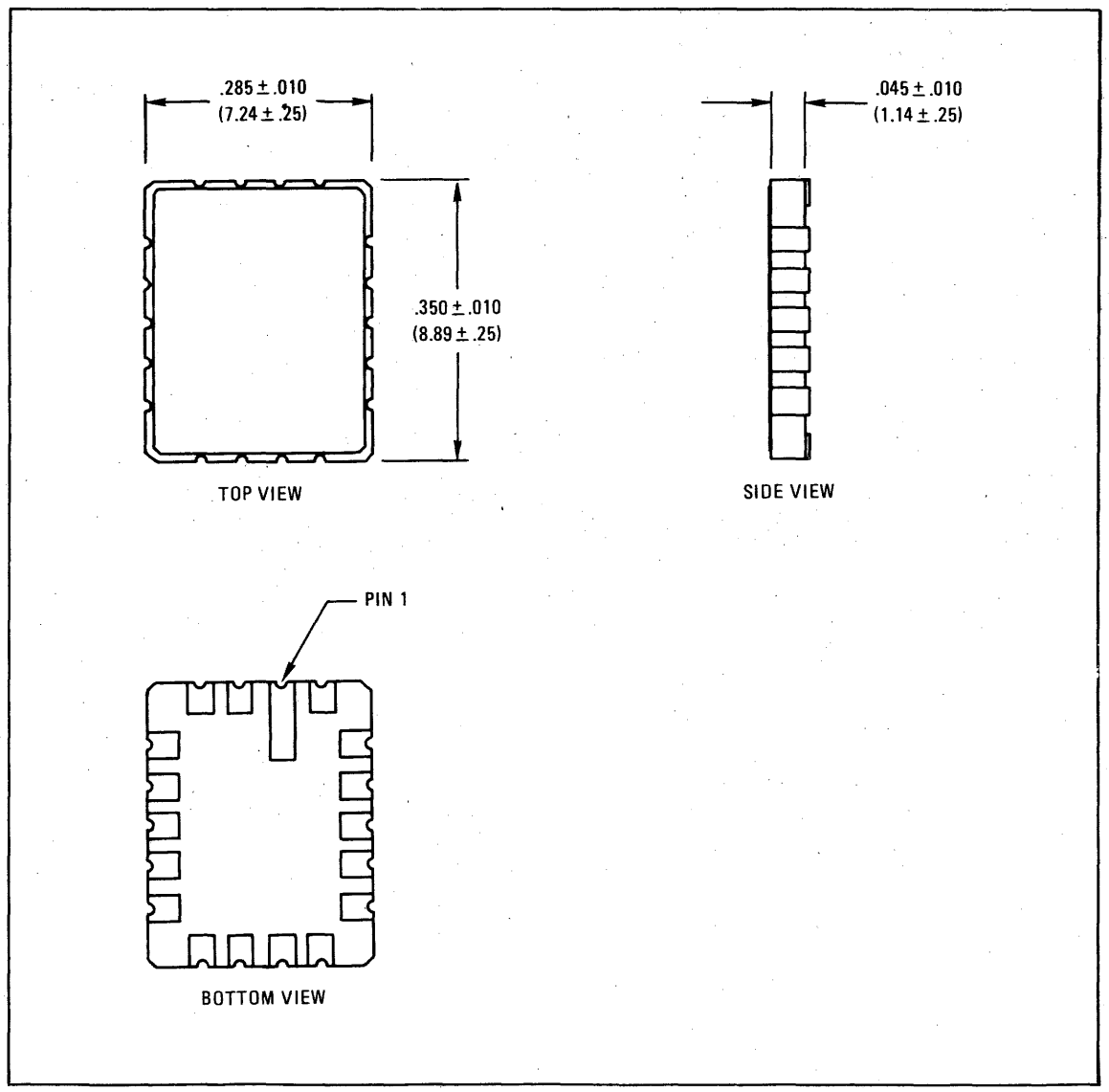
Leadless Carriers

Harris Semiconductor is offering four CMOS RAMs in 18 pin leadless carriers. Electrical specifications for these parts are identical to the equivalent product in the standard DIP package. Mechanical specifications for the 18 pin leadless carriers are shown below. For availability and additional information contact your nearest Harris Representative or Harris Sales Office.

All electrical grades of the following product types are available as stock items:

HM4-5618	1024 x 1	CMOS RAM	18 Pin
HM4-6561	256 x 4	CMOS RAM	18 Pin
HM4-6504	4096 x 1	CMOS RAM	18 Pin
HM4-6514	1024 x 4	CMOS RAM	18 Pin

The Package Code for Leadless Carriers is 4.



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2115A, 2125A FAMILY
HIGH SPEED 1K X 1 BIT STATIC RAM

	2115AL 2125AL	2115A 2125A	2115AL-2 2125AL-2	2115A-2 2125A-2	M2115AL M2125AL	M2115A M2125A
Max. T_{AA} (ns)	45	45	70	70	75	55
Max. I_{CC} (mA)	75	125	75	125	75	125
Operating Temperature Range (°C)	0-70				−55 to +125	

- **Pin Compatible to 93415A And 93425A**
- **Fan-Out Of 10 TTL (2115A Family) -- 16mA Output Sink Current**
- **HMOS Technology - High Reliability**
- **Low Operating Power Dissipation --Max. 0.39mW/Bit (2115AL, 2125AL) -- Max. 0.41mW/Bit (M2115AL, M2125AL)**
- **TTL Inputs And Outputs**
- **Single + 5V Supply**
- **Uncommitted Collector And Three-State Output**
- **Standard 16-Pin Dual in-Line Package**

The Intel® 2115A and 2125A families are high-speed, 1024 words by 1 bit random access memories. Both open collector (2115A) and three-state output (2125A) are available. The 2115A and 2125A use fully DC stable (static) circuitry throughout — in both the array and the decoding and, therefore, require no clocks or refreshing to operate. The data is read out non-destructively and has the same polarity as the input data.

The 2115AL/2125AL at 45 ns maximum access time and the 2115AL-2/2125AL-2 at 70 ns maximum access time are fully compatible with the industry-produced 1K bipolar RAMs, yet offer a significant reduction in power of their bipolar equivalents. The power dissipation of the 2115AL/2125AL and 2115AL-2/2125AL-2 is 394 mW maximum. For systems already designed for 1K bipolar RAMs, the 2115A/2125A and the 2115A-2/2125A-2 at 45 ns and 70 ns maximum access times, respectively, offer complete compatibility with substantial reduction in maximum power dissipation.

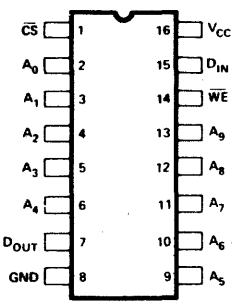
The M2115AL and M2125AL are ideal for high-performance systems where speed and power dissipation are significant design considerations. They have a maximum access time of 75 ns, while power dissipation is only 413 mW maximum. The M2115A/M2125A at 55 ns maximum should be considered for applications in which speed is a primary design objective.

The devices are directly TTL compatible in all respects: inputs, outputs, and a single + 5V supply. A separate select ($\overline{CS}$) lead allows easy selection of an individual package when outputs are OR-tied.

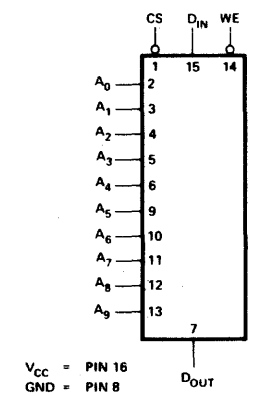
Intel

MEMORY

PIN CONFIGURATION

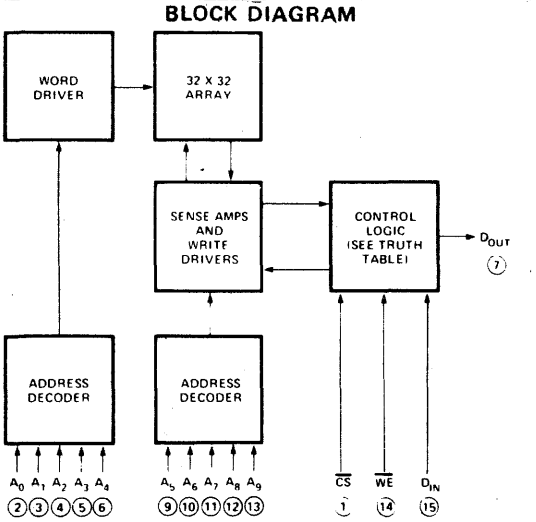


LOGIC SYMBOL



V_{CC} = PIN 16
GND = PIN 8

BLOCK DIAGRAM



PIN NAMES

$\overline{CS}$	CHIP SELECT
A_0 TO A_9	ADDRESS INPUTS
$\overline{WE}$	WRITE ENABLE
D_{IN}	DATA INPUT
D_{OUT}	DATA OUTPUT

TRUTH TABLE

INPUTS			OUTPUT 2115A FAMILY	OUTPUT 2125A FAMILY	MODE
$\overline{CS}$	$\overline{WE}$	D_{IN}	D_{OUT}	D_{OUT}	
H	X	X	H	HIGH Z	NOT SELECTED
L	L	L	H	HIGH Z	WRITE "0"
L	L	H	H	HIGH Z	WRITE "1"
L	H	X	D_{OUT}	D_{OUT}	READ

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intel®

PRELIMINARY
Notice: This is not a final specification. Some parametric limits are subject to change.

2118 FAMILY
16,384 x 1 BIT DYNAMIC RAM

	2118-2	2118-3	2118-4	2118-7
Maximum Access Time (ns)	80	100	120	150
Read, Write Cycle (ns)	210	210	225	260
Read-Modify-Write Cycle (ns)	250	250	285	315

- **Single +5V Supply, ±10% Tolerance**
- **HMOS Technology**
- **Low Power: 132mW Max. Operating 16mW Max. Standby**
- **Low V_{DD} Current Transients**
- **All Inputs, Including Clocks, TTL Compatible**
- **Non-Latched Output is Three-State, TTL Compatible**
- **$\overline{RAS}$ Only Refresh**
- **128 Refresh Cycles Required Every 2ms**
- **Page Mode Capability**
- **$\overline{CAS}$ Controlled Output Allows Hidden Refresh**

The Intel® 2118 is a 16,384 word by 1-bit Dynamic MOS RAM designed to operate from a single +5V power supply. The 2118 is fabricated using HMOS — a production proven process for high performance, high reliability, and high storage density.

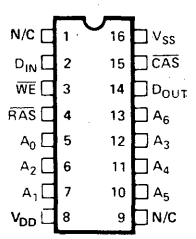
The 2118 uses a single transistor dynamic storage cell and advanced dynamic circuitry to achieve high speed with low power dissipation. The circuit design minimizes the current transients typical of dynamic RAM operation. These low current transients contribute to the high noise immunity of the 2118 in a system environment.

Multiplexing the 14 address bits into the 7 address input pins allows the 2118 to be packaged in the industry standard 16-pin DIP. The two 7-bit address words are latched into the 2118 by the two TTL clocks, Row Address Strobe ($\overline{RAS}$) and Column Address Strobe ($\overline{CAS}$). Non-critical timing requirements for $\overline{RAS}$ and $\overline{CAS}$ allow use of the address multiplexing technique while maintaining high performance.

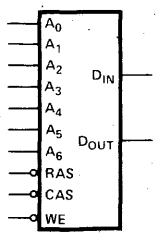
The 2118 three-state output is controlled by $\overline{CAS}$, independent of $\overline{RAS}$. After a valid read or read-modify-write cycle, data is latched on the output by holding $\overline{CAS}$ low. The data out pin is returned to the high impedance state by returning $\overline{CAS}$ to a high state. The 2118 hidden refresh feature allows $\overline{CAS}$ to be held low to maintain latched data while $\overline{RAS}$ is used to execute $\overline{RAS}$-only refresh cycles.

The single transistor storage cell requires refreshing for data retention. Refreshing is accomplished by performing $\overline{RAS}$-only refresh cycles, hidden refresh cycles, or normal read or write cycles on the 128 address combinations of A_0 through A_6 during a 2ms period. A write cycle will refresh stored data on all bits of the selected row except the bit which is addressed.

PIN CONFIGURATION

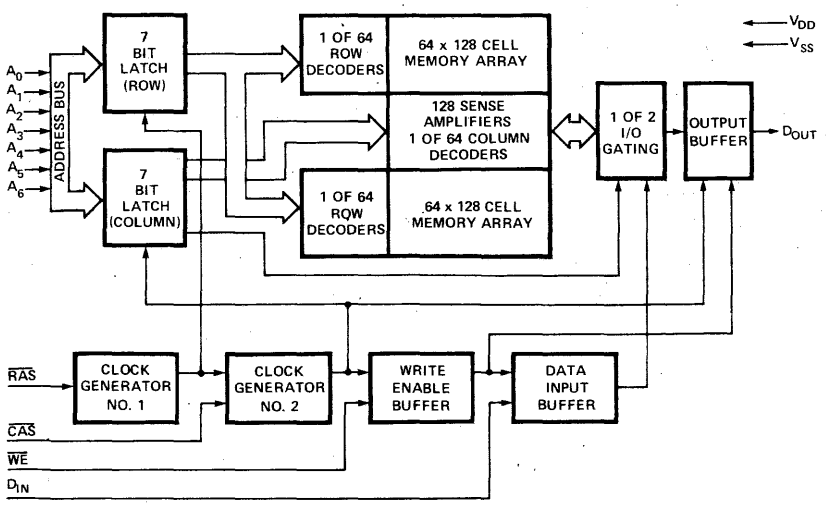


LOGIC SYMBOL



A_0-A_6	ADDRESS INPUTS
$\overline{CAS}$	COLUMN ADDRESS STROBE
D_{IN}	DATA IN
D_{OUT}	DATA OUT
$\overline{WE}$	WRITE ENABLE
$\overline{RAS}$	ROW ADDRESS STROBE
V_{DD}	POWER (+5V)
V_{SS}	GROUND

BLOCK DIAGRAM



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2141
4096 X 1 BIT STATIC RAM

	2141-2	2141-3	2141-4	2141-5	2141L-3	2141L-4	2141L-5
Max. Access Time (ns)	120	150	200	250	150	200	250
Max. Active Current (mA)	70	70	55	55	40	40	40
Max. Standby Current (mA)	20	20	12	12	5	5	5

- **HMOS Technology**
- **Industry Standard 2147 Pinout**
- **Completely Static Memory — No Clock or Timing Strobe Required**
- **Equal Access and Cycle Times**
- **Single +5V Supply**
- **Automatic Power-Down**
- **Directly TTL Compatible — All Inputs and Output**
- **Separate Data Input and Output**
- **Three-State Output**
- **High Density 18-Pin Package**

The Intel® 2141 is a 4096-bit static Random Access Memory organized as 4096 words by 1-bit using HMOS, a high-performance MOS technology. It uses a uniquely innovative design approach which provides the ease-of-use features associated with non-clocked static memories and the reduced standby power dissipation associated with clocked static memories. To the user this means low standby power dissipation without the need for clocks, address setup and hold times, nor reduced data rates due to cycle times that are longer than access times.

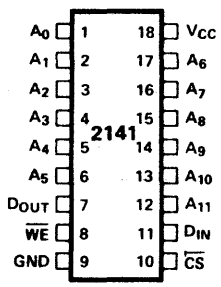
$\overline{CS}$ controls the power-down feature. In less than a cycle time after $\overline{CS}$ goes high — deselecting the 2141 — the part automatically reduces its power requirements and remains in this low power standby mode as long as $\overline{CS}$ remains high. This device feature results in system power savings as great as 85% in larger systems, where the majority of devices are de-selected.

The 2141 is placed in an 18-pin package configured with the industry standard pinout, the same as the 2147. It is directly TTL compatible in all respects: inputs, output, and a single +5V supply. The data is read out nondestructively and has the same polarity as the input data. A data input and a separate three-state output are used.

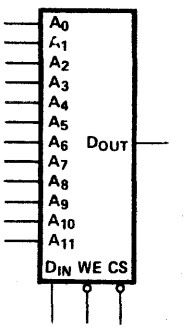
Intel

MEMORY

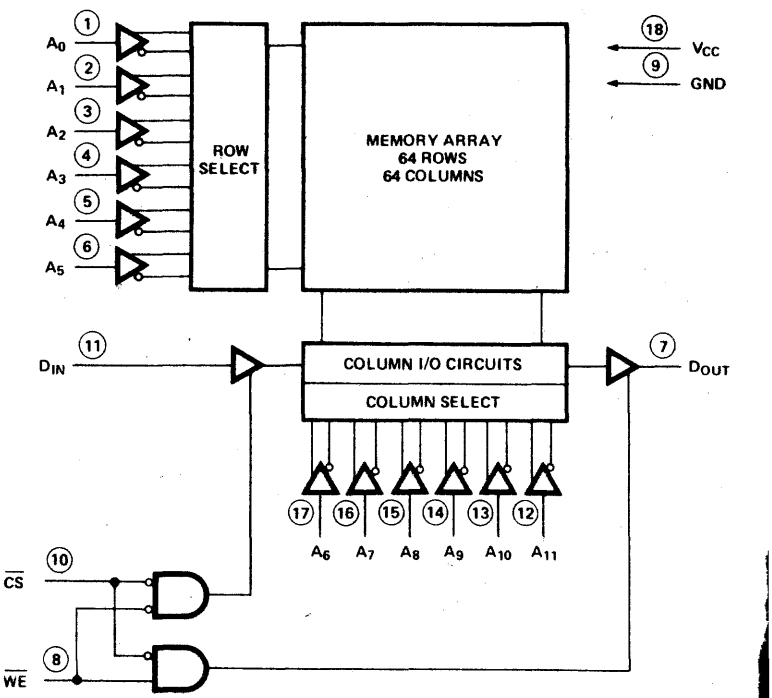
PIN CONFIGURATION



LOGIC SYMBOL



BLOCK DIAGRAM



PIN NAMES

A_0–A_{11}	ADDRESS INPUTS	V_{CC}	POWER (+5V)
$\overline{WE}$	WRITE ENABLE	GND	GROUND
$\overline{CS}$	CHIP SELECT		
D_{IN}	DATA INPUT		
D_{OUT}	DATA OUTPUT		

TRUTH TABLE

$\overline{CS}$	$\overline{WE}$	MODE	OUTPUT	POWER
H	X	NOT SELECTED	HIGH Z	STANDBY
L	L	WRITE	HIGH Z	ACTIVE
L	H	READ	D_{OUT}	ACTIVE

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M2147
4096 X 1 BIT STATIC RAM

	M2147
Max. Access Time (ns)	85
Max. Active Current (mA)	180
Max. Standby Current (mA)	30

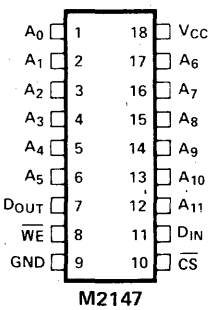
- HMOS Technology
- Completely Static Memory — No Clock or Timing Strobe Required
- Equal Access and Cycle Times
- Single +5V Supply
- ±10% Power Supply Tolerance
- Automatic Power-Down
- High Density 18-Pin Package
- Directly TTL Compatible — All Inputs and Outputs
- Separate Data Input and Output
- Three-State Output
- Full Military Temperature Range

The Intel® M2147 is a 4096-bit static Random Access Memory organized as 4096 words by 1-bit using HMOS, a high-performance MOS technology. It uses a uniquely innovative design approach which provides the ease-of-use features associated with non-clocked static memories and the reduced standby power dissipation associated with clocked static memories. To the military user this means low standby power dissipation without the need for clocks, address setup and hold times, nor reduced data rates due to cycle times that are longer than access times.

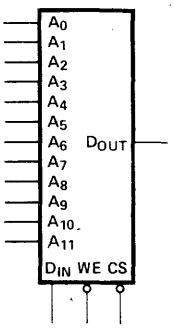
$\overline{CS}$ controls the power-down feature. In less than a cycle time after $\overline{CS}$ goes high — deselecting the M2147— the part automatically reduces its power requirements and remains in this low power standby mode as long as $\overline{CS}$ remains high. This device feature results in system power savings as great as 85% in larger systems, where the majority of devices are de-selected.

The M2147 is placed in an 18-pin package configured with the industry standard pinout. It is directly TTL compatible in all respects: inputs, outputs, and a single +5V supply. The data is read out nondestructively and has the same polarity as the input data. A data input and a separate three-state output are used.

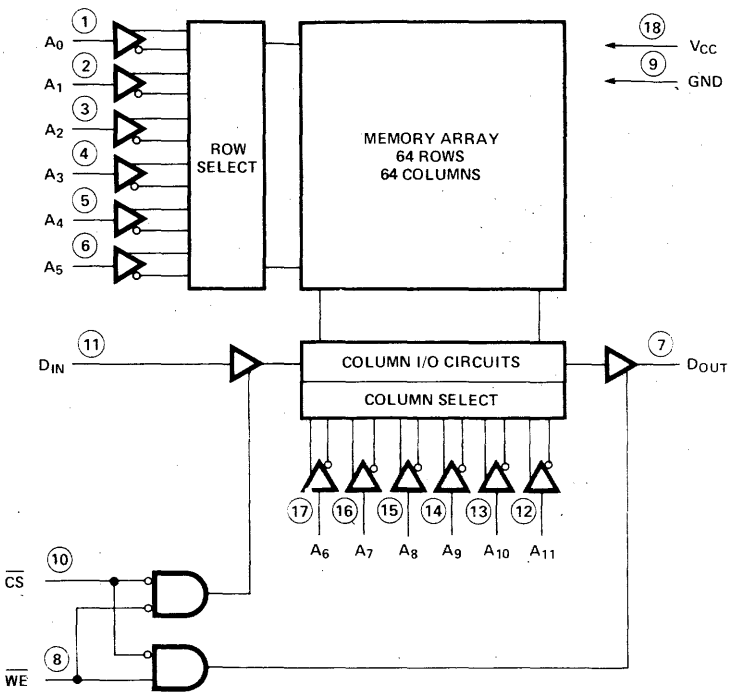
PIN CONFIGURATION



LOGIC SYMBOL



BLOCK DIAGRAM



PIN NAMES

A_0–A_{11}	ADDRESS INPUTS	V_{CC}	POWER (+5V)
$\overline{WE}$	WRITE ENABLE	GND	GROUND
$\overline{CS}$	CHIP SELECT		
D_{IN}	DATA INPUT		
D_{OUT}	DATA OUTPUT		

TRUTH TABLE

$\overline{CS}$	$\overline{WE}$	MODE	OUTPUT	POWER
H	X	NOT SELECTED	HIGH Z	STANDBY
L	L	WRITE	HIGH Z	ACTIVE
L	H	READ	D_{OUT}	ACTIVE

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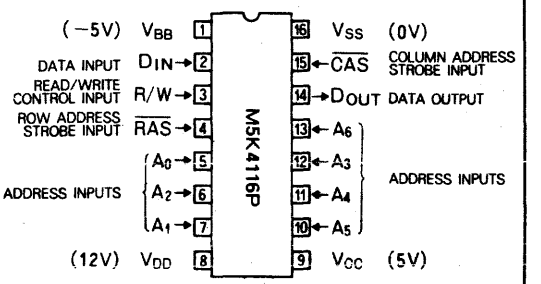
M5K 4116P, S-2, M5K 4116P, S-3, M5K 4116P, S-4

16384-BIT (16384-WORD BY 1-BIT) DYNAMIC RANDOM-ACCESS MEMORY

DESCRIPTION

The M5K 4116P and S are 16384-word by 1-bit dynamic RAMs, fabricated with the N-channel silicon-gate MOS process, and ideal for large-capacity memory systems where high speed, low power dissipation, and low costs are essential. The use of double-layer poly-silicon process technology and a single-transistor dynamic storage cell provide high circuit density at reduced costs, and the use of dynamic circuitry including sense amplifiers assures low power dissipation. Multiplexed address inputs permit both a reduction in pins to the standard 16-pin package configuration and an increase in system densities.

PIN CONFIGURATION (TOP VIEW)



Outline 16P1 (M5K4116P)
16S1 (M5K4116S)

FEATURES

Type name	Access time (max) (ns)	Cycle time (min) (ns)	Power dissipation (typ) (mW)
M5K4116P, S-2	150	375	280
M5K4116P, S-3	200	375	280
M5K4116P, S-4	250	410	260

- Standard 16-pin package
- Voltage range on all power supplies (V_{DD}, V_{CC}, V_{BB}): ±10%
- Low standby power dissipation: 19.8mW (max)
- Low operating power dissipation: 462mW (max)
- Unlatched output enables two-dimensional chip selection and extended page boundary.
- Early-write operation gives common I/O capability.
- Read-modify-write, $\overline{RAS}$-only refresh, and page-mode capabilities
- All input terminals have low input capacitance and are directly TTL-compatible.
- Output is three-state and directly TTL-compatible
- 128 refresh cycles
- Interchangeable with Mostek's MK4116 in both electrical characteristics and pin configuration.

APPLICATION

- Main memory unit for computers

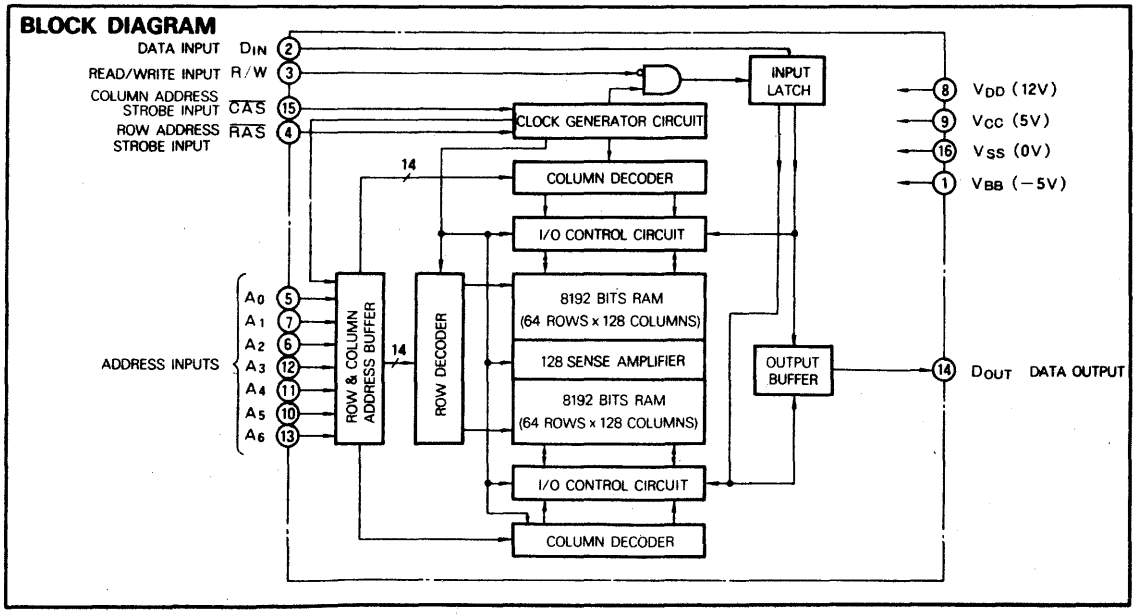
FUNCTION

The M5K 4116P and S provide, in addition to normal read, write, and read-modify-write operations, a number of other functions, e.g., page mode, $\overline{RAS}$-only refresh, and delayed-write. The input conditions for each are shown below.

Operation	Inputs						Output	Refresh	Remarks
	$\overline{RAS}$	$\overline{CAS}$	R/W	D_{IN}	Row address	Column address	D_{OUT}		
Read	ACT	ACT	NAC	DNC	APD	APD	VLD	YES	Page mode is identical except refresh is NO.
Write	ACT	ACT	ACT	VLD	APD	APD	OPN	YES	
Read-modify-write	ACT	ACT	ACT	VLD	APD	APD	VLD	YES	
$\overline{RAS}$-only refresh	ACT	NAC	DNC	DNC	APD	DNC	OPN	YES	
Standby	NAC	DNC	DNC	DNC	DNC	DNC	OPN	NO	

Note : ACT : active; NAC : nonactive; DNC : don't care; VLD : valid; APD : applied; OPN : open

BLOCK DIAGRAM



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M5K 4116P, S-2, M5K 4116P, S-3, M5K 4116P, S-4

16384-BIT (16384-WORD BY 1-BIT) DYNAMIC RANDOM-ACCESS MEMORY

SUMMARY OF OPERATIONS

Addressing

To select one of the 16384 memory cells in the M5K 4116P and S, the 14-bit address signal must be multiplexed into 7 address signals, which are then latched into the on-chip latch by two externally-applied clock pulses. First, the negative-going edge of the row-address-strobe pulse ($\overline{RAS}$) latches the 7 row-address bits; next, the negative-going edge of the column-address-strobe pulse ($\overline{CAS}$) latches the 7 column-address bits. Timing of the $\overline{RAS}$ and $\overline{CAS}$ clocks can be selected by either of the following two methods:

1. The delay time from $\overline{RAS}$ to $\overline{CAS}$ $t_{d(\overline{RAS}\text{-}\overline{CAS})}$ is set between the minimum and maximum values of the limits. In this case, the internal $\overline{CAS}$ control signals are inhibited almost until $t_{d(\overline{RAS}\text{-}\overline{CAS})max}$ ('gated $\overline{CAS}$' operation). The external $\overline{CAS}$ signal can be applied with a margin not affecting the on-chip circuit operations e.g. access time, and the address inputs can be easily changed from row address to column address.
2. The delay time $t_{d(\overline{RAS}\text{-}\overline{CAS})}$ is set larger than the maximum value of the limits. In this case the internal inhibition of $\overline{CAS}$ has already been released, so that the internal $\overline{CAS}$ control signals are controlled by the externally applied $\overline{CAS}$ which also controls the access time.

Data Input

Data to be written into a selected cell is strobed by the later of the two negative transitions of R/W input and $\overline{CAS}$ input. Thus when the R/W input makes its negative transition prior to $\overline{CAS}$ input (early write), the data input is strobed by $\overline{CAS}$, and the negative transition of $\overline{CAS}$ is set as the reference point for set-up and hold times. In the read-write or read-modify-write cycles, however, when the R/W input makes its negative transition after $\overline{CAS}$, the R/W negative transition is set as the reference point for set-up and hold times.

Data Output Control

The output of the M5K 4116P and S is in the high-impedance state when $\overline{CAS}$ is high. When the memory cycle in progress is a read, read-modify-write, or a delayed-write cycle, the data output will go from the high-impedance state to the active condition, and the data in the selected cell will be read. This data output will have the same polarity as the input data. Once the output has entered the active condition, this condition will be maintained until $\overline{CAS}$ goes high, irrespective of the condition of $\overline{RAS}$ (for a maximum of 10μs).

The output will remain in the high-impedance state throughout the entire cycle in an early-write cycle.

These output conditions, of the M5K 4116P and S, which can readily be changed by controlling the timing of the write pulse in a write cycle, and the width of the $\overline{CAS}$ pulse in a read cycle, offer capabilities for a number of applications, as follows.

1. Common I/O Operation

If all write operations are performed in the early-write mode, input and output can be connected directly to give a common I/O data bus.

2. Data Output Hold

The data output can be held between read cycles, without lengthening the cycle time, until the next cycle commences. This enables extremely flexible clock-timing settings for $\overline{RAS}$ and $\overline{CAS}$.

3. Two Methods of Chip Selection

Since the output is not latched, $\overline{CAS}$ is not required to keep the outputs of selected chips in the matrix in a high-impedance state. This means that $\overline{CAS}$ and/or $\overline{RAS}$ can both be decoded for chip selection.

4. Extended-Page Boundary

By decoding $\overline{CAS}$, the page boundary can be extended beyond the 128 column locations in a single chip. In this case, $\overline{RAS}$ must be applied to all devices.

Page-Mode Operation

This operation allows for multiple-column addressing at the same row address, and eliminates the power dissipation associated with the negative-going edge of $\overline{RAS}$, because once the row address has been strobed, $\overline{RAS}$ is maintained. Also, the time required to strobe in the row address for the second and subsequent cycles is eliminated, thereby decreasing the access and cycle times.

Refresh

The refreshing of the dynamic cell matrix is accomplished by performing a memory operation at each of the 128 row-address locations within a 2ms time interval. Any normal memory cycle will perform the refreshing, and $\overline{RAS}$-only refresh offers a significant reduction in operating power.

Power Dissipation

Most of the circuitry in the M5K 4116P and S is dynamic, and most of the power is dissipated when addresses are strobed. Both $\overline{RAS}$ and $\overline{CAS}$ are decoded and applied to the M5K 4116P and S as chip-select in the memory system, but if RAS is decoded, all unselected devices go into stand-by independent of the $\overline{CAS}$ condition, minimizing system power dissipation.

Power Supplies

Although the M5K 4116P and S require no particular power-supply sequencing so long as the devices are used within the limits of the absolute maximum ratings, it is recommended that the V_{BB} supply be applied first and removed last. V_{BB} should never be more positive than V_{SS} when power supply is applied to V_{DD}.

Some eight dummy cycles are necessary after power is applied to the device before memory operation is achieved.

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M5K4116P,S-2, M5K4116P,S-3, M5K4116P,S-4

16384-BIT (16384-WORD BY 1-BIT) DYNAMIC RANDOM-ACCESS MEMORY

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter		Conditions	Limits	Unit
V_{DD}	Supply voltage		With respect to V_{BB}	−0.5 ~ 20	V
V_{CC}	Supply voltage			−0.5 ~ 20	V
V_{SS}	Supply voltage			−0.5 ~ 20	V
V_I	Input voltage			−0.5 ~ 20	V
V_O	Output voltage			−0.5 ~ 20	V
V_{DD}	Supply voltage		With respect to V_{SS}	−1 ~ 15	V
V_{CC}	Supply voltage			−1 ~ 15	V
$V_{BB}-V_{SS}$	Supply voltage		$V_{DD}-V_{SS}>0$	0	V
I_O	Output current			50	mA
P_d	Power dissipation	M5K4116S	Ta = 25℃	1000	mW
		M5K4116P	Ta = 25℃	700	mW
Topr	Operating free-air temperature range			0 ~ 70	℃
Tstg	Storage temperature range	M5K4116S		−65 ~ 150	℃
		M5K4116P		−40 ~ 125	℃

3

RECOMMENDED OPERATING CONDITIONS (Ta = 0 ~ 70 ℃, unless otherwise noted. Note 1)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
V_{DD}	Supply voltage	10.8	12	13.2	V
V_{CC}	Supply voltage (Note 2)	4.5	5	5.5	V
V_{SS}	Supply voltage	0	0	0	V
V_{BB}	Supply voltage	−4.5	−5	−5.7	V
V_{IH1}	High-level input voltage, $\overline{RAS}$, $\overline{CAS}$, R/W	2.7		7	V
V_{IH2}	High-level input voltage, $A_0 \sim A_6$, D_{IN}	2.4		7	V
V_{IL}	Low-level input voltage, all inputs	−1		0.8	V

Note 1 : All voltages with respect to V_{SS}. Apply V_{BB} power supply first, prior to other power supplies, and remove last.

2 : The output voltage will swing from V_{SS} to V_{CC} when output loading current is zero. In standby mode V_{CC} may be reduced to V_{SS} without affecting refresh operations or data retention, but the V_{OH} min specification is not guaranteed in this mode.

ELECTRICAL CHARACTERISTICS

(Ta = 0 ~ 70 ℃, V_{DD} = 12V ± 10%, V_{CC} = 5V ± 10%, V_{SS} = 0V, −5.7V ≤ V_{BB} ≤ −4.5V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V_{OH}	High-level output voltage (Note 2)	I_{OH} = −5 mA	2.4		V_{CC}	V
V_{OL}	Low-level output voltage (Note 2)	I_{OL} = 4.2 mA	0		0.4	V
I_{OZ}	Off-state output current	D_{OUT} floating 0V ≤ V_{OUT} ≤ 5.5V	−10		10	μA
I_I	Input current	V_{BB} = −5V, 0V ≤ V_{IN} ≤ 7V All other pins = 0V	−10		10	μA
$I_{DD1(AV)}$	Average supply current from V_{DD}, operating	$\overline{RAS}$, $\overline{CAS}$ cycling $t_{C(RD)} = t_{C(WR)}$ = 375ns			35	mA
$I_{CC1(AV)}$	Average supply current from V_{CC}, operating					—
$I_{BB1(AV)}$	Average supply current from V_{BB}, operating (Note 4)				200	μA
I_{DD2}	Supply current from V_{DD}, standby	$\overline{RAS}$ = V_{IH} D_{OUT} = floating			1.5	mA
I_{CC2}	Supply current from V_{CC}, standby		−10		10	μA
I_{BB2}	Supply current from V_{BB}, standby				100	μA
$I_{DD3(AV)}$	Average supply current from V_{DD}, refreshing	$\overline{RAS}$ cycling $\overline{CAS}$ = V_{IH} $t_{C(REF)}$ = 375ns			27	mA
$I_{CC3(AV)}$	Average supply current from V_{CC}, refreshing		−10		10	μA
$I_{BB3(AV)}$	Average supply current from V_{BB}, refreshing				200	μA
$I_{DD4(AV)}$	Average supply current from V_{DD}, page mode	$\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling $t_{C(PG)}$ = 225ns			27	mA
$I_{CC4(AV)}$	Average supply current from V_{CC}, page mode (Note 4)					—
$I_{BB4(AV)}$	Average supply current from V_{BB}, page mode				200	μA
$C_{i(AD)}$	Input capacitance, address inputs	V_I = V_{SS} f = 1MHz V_I = 25mVrms			5	pF
$C_{i(DA)}$	Input capacitance, data input				5	pF
$C_{i(R/W)}$	Input capacitance, read/write control input				7	pF
$C_{i(\overline{RAS})}$	Input capacitance, $\overline{RAS}$ input				10	pF
$C_{i(\overline{CAS})}$	Input capacitance, $\overline{CAS}$ input				10	pF
C_O	Output capacitance	V_O = V_{SS}, f = 1MHz, V_I = 25mVrms			7	pF

Note 3 : Current flowing into an IC is positive; out is negative.

4 : V_{CC} is connected only to the output buffer, so that I_{CC1} and I_{CC4} depend upon output loading.

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M5K 4116P, S-2, M5K 4116P, S-3, M5K 4116P, S-4

16384-BIT (16384-WORD BY 1-BIT) DYNAMIC RANDOM-ACCESS MEMORY

TIMING REQUIREMENTS (For Read, Write, Read-Modify-Write, Refresh, and Page-Mode Cycle)

($Ta = 0 \sim 70℃$, $V_{DD} = 12V \pm 10\%$, $V_{CC} = 5V \pm 10\%$, $V_{SS} = 0V$, $-5.7V \leq V_{BB} \leq -4.5V$, unless otherwise noted. See notes 5, 6, and 7.)

Symbol	Parameter	Alternative Symbol	M5K4116-2 Limits		M5K4116-3 Limits		M5K4116-4 Limits		Unit
			Min	Max	Min	Max	Min	Max	
$t_{c(REF)}$	Refresh cycle time	t_{REF}		2		2		2	ms
$t_{w(\overline{RAS}H)}$	$\overline{RAS}$ high pulse width	t_{RP}	100		120		150		ns
$t_{w(\overline{RAS}L)}$	$\overline{RAS}$ low pulse width	t_{RAS}	150	10000	200	10000	250	10000	ns
$t_{w(\overline{CAS}L)}$	$\overline{CAS}$ low pulse width (Note 8)	t_{CAS}	100		135		165		ns
$t_{h(\overline{RAS}\text{-}\overline{CAS})}$	$\overline{CAS}$ hold time with respect to $\overline{RAS}$	t_{CSH}	150		200		250		ns
$t_{h(\overline{CAS}\text{-}\overline{RAS})}$	$\overline{RAS}$ hold time with respect to $\overline{CAS}$	t_{RSH}	100		135		165		ns
$t_{d(\overline{RAS}\text{-}\overline{CAS})}$	Delay time, $\overline{RAS}$ to $\overline{CAS}$ (Note 9)	t_{RCD}	20	50	25	65	35	85	ns
$t_{d(\overline{CAS}\text{-}\overline{RAS})}$	Delay time, $\overline{CAS}$ to $\overline{RAS}$	t_{CRP}	−20		−20		−20		ns
$t_{su(RA\text{-}\overline{RAS})}$	Row address setup time with respect to $\overline{RAS}$	t_{ASR}	0		0		0		ns
$t_{su(CA\text{-}\overline{CAS})}$	Column address setup time with respect to $\overline{CAS}$	t_{ASC}	−10		−10		−10		ns
$t_{h(\overline{RAS}\text{-}RA)}$	Row address hold time with respect to $\overline{RAS}$	t_{RAH}	20		25		35		ns
$t_{h(\overline{CAS}\text{-}CA)}$	Column address hold time with respect to $\overline{CAS}$	t_{CAH}	45		55		75		ns
$t_{h(\overline{RAS}\text{-}CA)}$	Column address hold time with respect to $\overline{RAS}$	t_{AR}	95		120		160		ns
t_{THL} t_{TLH}	Transition time	t_T	3	35	3	50	3	50	ns

Note 5 : After power supply is applied, some eight dummy cycles are required before memory operation is achieved.

6 : The switching characteristics are defined as $t_{THL} = t_{TLH} = 5ns$.

7 : Reference levels of input signals are V_{IH1} min, V_{IH2} min and V_{IL} max. Reference levels for transition time are also between V_{IH1} or V_{IH2} and V_{IL}.

8 : Assumes that $t_{d(\overline{RAS}\text{-}\overline{CAS})} \geq t_{d(\overline{RAS}\text{-}\overline{CAS})}$ max. If $t_{d(\overline{RAS}\text{-}\overline{CAS})} < t_{d(\overline{RAS}\text{-}\overline{CAS})}$ max, $t_{w(\overline{CAS}L)}$ will be increased by the amount that $t_{d(\overline{RAS}\text{-}\overline{CAS})}$ has decreased.

9 : The maximum value of $t_{d(\overline{RAS}\text{-}\overline{CAS})}$ does not define the limit of operation, but is specified as a reference point only; if $t_{d(\overline{RAS}\text{-}\overline{CAS})}$ is greater than the specified $t_{d(\overline{RAS}\text{-}\overline{CAS})}$ max limit, then access time is controlled exclusively by $t_{a(\overline{CAS})}$.

SWITCHING CHARACTERISTICS ($Ta = 0 \sim 70℃$, $V_{DD} = 12V \pm 10\%$, $V_{CC} = 5V \pm 10\%$, $V_{SS} = 0V$, $-5.7V \leq V_{BB} \leq -4.5V$, unless otherwi

Read Cycle

Symbol	Parameter	Alternative Symbol	M5K4116-2 Limits		M5K4116-3 Limits		M5K4116-4 Limits		Unit
			Min	Max	Min	Max	Min	Max	
$t_{c(RD)}$	Read cycle time	t_{RC}	320		375		410		ns
$t_{su(RD\text{-}\overline{CAS})}$	Read set-up time with respect to $\overline{CAS}$	t_{RCS}	0		0		0		ns
$t_{h(\overline{CAS}\text{-}RD)}$	Read hold time with respect to $\overline{CAS}$	t_{RCH}	0		0		0		ns
$t_{h(\overline{CAS}\text{-}OUT)}$	Data-out hold time	t_{OFF}	0	40	0	50	0	60	ns
$t_{a(\overline{CAS})}$	$\overline{CAS}$ access time (Note 10)	t_{CAC}		100		135		165	ns
$t_{a(\overline{RAS})}$	$\overline{RAS}$ access time (Note 11)	t_{RAC}		150		200		250	ns

Note 10 : This is the value when $t_{d(\overline{RAS}\text{-}\overline{CAS})} \geq t_{d(\overline{RAS}\text{-}\overline{CAS})}$max. Test conditions : Load = 2TTL, $C_L = 100pF$

11 : This is the value when $t_{d(\overline{RAS}\text{-}\overline{CAS})} < t_{d(\overline{RAS}\text{-}\overline{CAS})}$max. When $t_{d(\overline{RAS}\text{-}\overline{CAS})} \geq t_{d(\overline{RAS}\text{-}\overline{CAS})}$max. $t_{a(\overline{RAS})}$ increases by the amount of increase of $t_{d(\overline{RAS}\text{-}\overline{CAS})}$. Test conditions : Load = 2TTL, $C_L = 100pF$

Write Cycle

Symbol	Parameter	Alternative Symbol	M5K4116-2 Limits		M5K4116-3 Limits		M5K4116-4 Limits		Unit
			Min	Max	Min	Max	Min	Max	
$t_{c(WR)}$	Write cycle time	t_{RC}	320		375		410		ns
$t_{su(WR\text{-}\overline{CAS})}$	Write set-up time with respect to $\overline{CAS}$ (Note 12)	t_{WCS}	−20		−20		−20		ns
$t_{h(\overline{CAS}\text{-}WR)}$	Write hold time with respect to $\overline{CAS}$	t_{WCH}	45		55		75		ns
$t_{h(\overline{RAS}\text{-}WR)}$	Write hold time with respect to $\overline{RAS}$	t_{WCR}	95		120		160		ns
$t_{h(WR\text{-}\overline{RAS})}$	$\overline{RAS}$ hold time with respect to write	t_{RWL}	50		70		85		ns
$t_{h(WR\text{-}\overline{CAS})}$	$\overline{CAS}$ hold time with respect to write	t_{CWL}	50		70		85		ns
$t_{w(WR)}$	Write pulse width	t_{WP}	45		55		75		ns
$t_{su(DA\text{-}\overline{CAS})}$	Data-in setup time with respect to $\overline{CAS}$	t_{DS}	0		0		0		ns
$t_{h(\overline{CAS}\text{-}DA)}$	Data-in hold time with respect to	t_{DH}	45		55		75		ns
$t_{h(\overline{RAS}\text{-}DA)}$	Data-in hold time with respect to $\overline{RAS}$	t_{DHR}	95		120		160		ns

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Read-Write, Read-Modify-Write Cycle

Symbol	Parameter	Alternative symbol	M5K4116-2		M5K4116-3		M5K4116-4		Unit
			Limits		Limits		Limits		
			Min	Max	Min	Max	Min	Max	
$t_{c(RMW)}$	Read-modify-write cycle time	t_{RWC}	320		405		500		ns
$t_{h(WR-\overline{RAS})}$	$\overline{RAS}$ hold time with respect to write	t_{RWL}	50		70		85		ns
$t_{h(WR-\overline{CAS})}$	$\overline{CAS}$ hold time with respect to write	t_{CWL}	50		70		85		ns
$t_{w(WR)}$	Write pulse width	t_{WP}	45		55		75		ns
$t_{su(RD-\overline{CAS})}$	Read setup time with respect to $\overline{CAS}$	t_{RCS}	0		0		0		ns
$t_{d(\overline{RAS}-WR)}$	Delay time, $\overline{RAS}$ to write (Note 12)	t_{RWD}	110		145		175		ns
$t_{d(\overline{CAS}-WR)}$	Delay time, $\overline{CAS}$ to write (Note 12)	t_{CWD}	60		80		90		ns
$t_{su(DA-WR)}$	Data-in set-up time with respect to write	t_{DS}	0		0		0		ns
$t_{h(WR-DA)}$	Data-in hold time with respect to write	t_{DH}	45		55		75		ns
$t_{h(\overline{CAS}-OUT)}$	Data-out hold time	t_{OFF}	0	40	0	50	0	60	ns
$t_{a(\overline{CAS})}$	$\overline{CAS}$ access time (Note 10)	t_{CAC}		100		135		165	ns
$t_{a(\overline{RAS})}$	$\overline{RAS}$ access time (Note 11)	t_{RAC}		150		200		250	ns

Note 12 : $t_{su(WR-\overline{CAS})}$, $t_{d(\overline{RAS}-WR)}$, and $t_{d(\overline{CAS}-WR)}$ do not define the limits of operation, but are included as electrical characteristics only.
When $t_{su(WR-\overline{CAS})} \geqq t_{su(WR-\overline{CAS})min}$, an early-write cycle is performed, and the data output keeps the high-impedance state.
When $t_{d(\overline{RAS}-WR)} \geqq t_{d(\overline{RAS}-WR)min}$ and $t_{d(\overline{CAS}-WR)} \geqq t_{d(\overline{CAS}-WR)min}$, a read-modify-write cycle is performed, and the data of the selected address will be read out on the data outputs.
For all conditions other than those described above the condition of data output is not defined.

Page-Mode Cycle

Symbol	Parameter	Alternative symbol	M5K4116-2		M5K4116-3		M5K4116-4		Unit
			Limits		Limits		Limits		
			Min	Max	Min	Max	Min	Max	
$t_{c(PG)}$	Page-mode cycle time	t_{PC}	170		225		275		ns
$t_{w(\overline{CASH})}$	$\overline{CAS}$ high pulse width	t_{CP}	60		80		100		ns

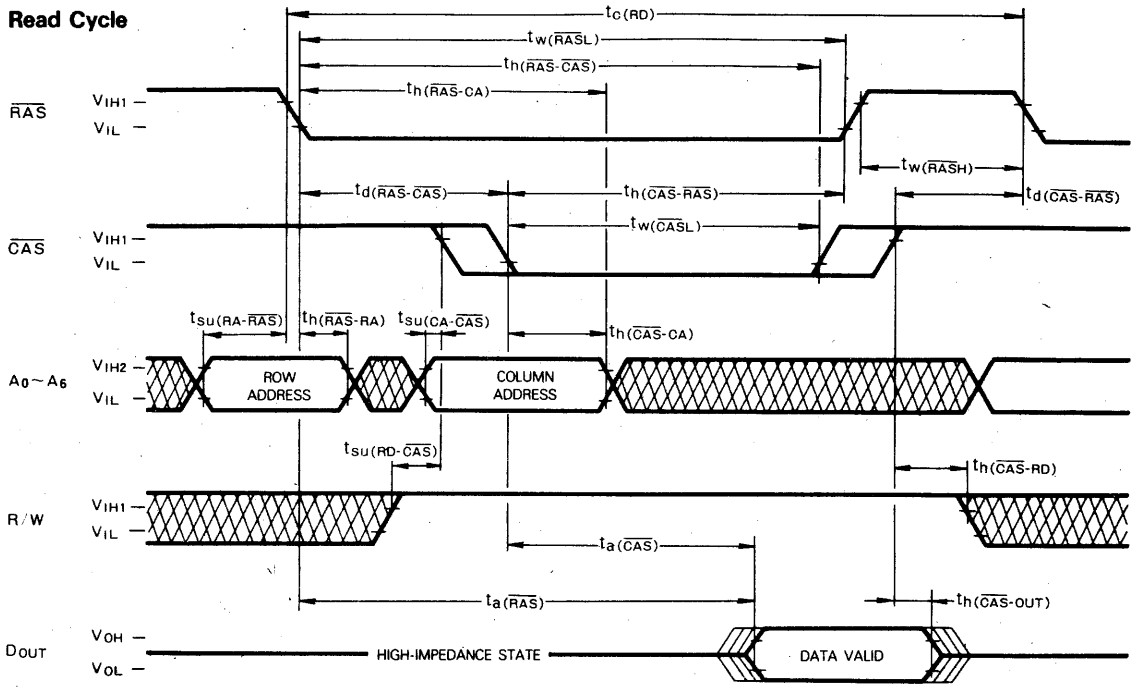
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M5K 4116P, S-2, M5K 4116P, S-3, M5K 4116P, S-4

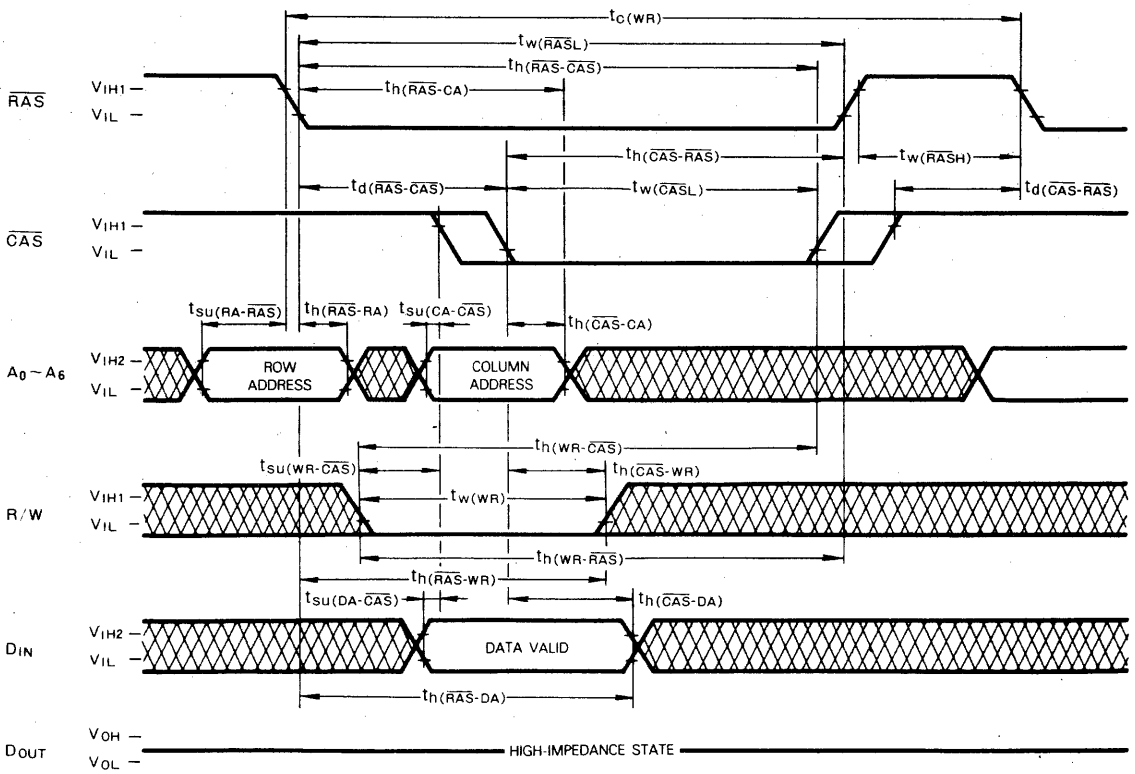
16384-BIT (16384-WORD BY 1-BIT) DYNAMIC RANDOM-ACCESS MEMORY

TIMING DIAGRAM

Read Cycle

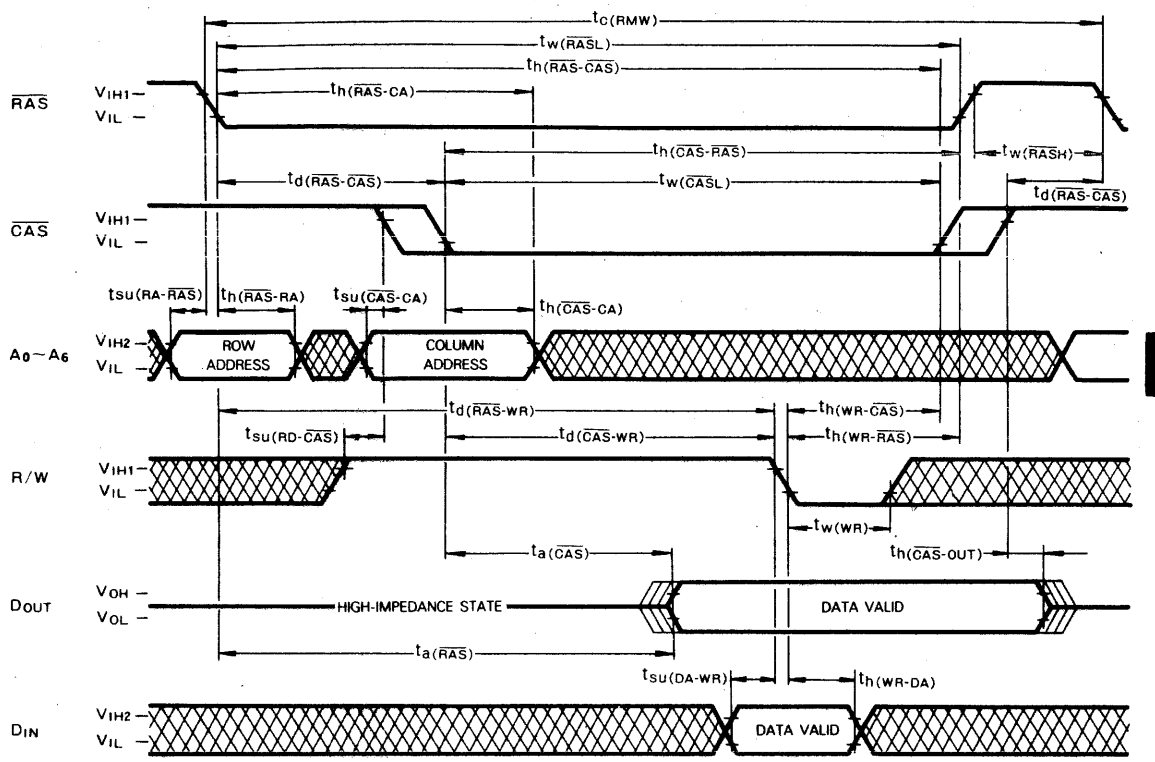


Write Cycle (Early Write)

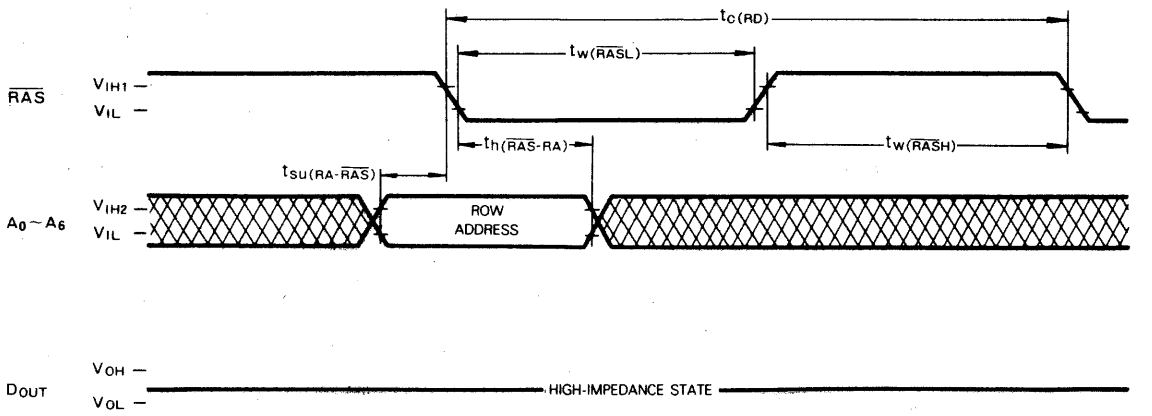


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Read-Write, Read-Modify-Write Cycle



RAS-Only Refresh Cycle

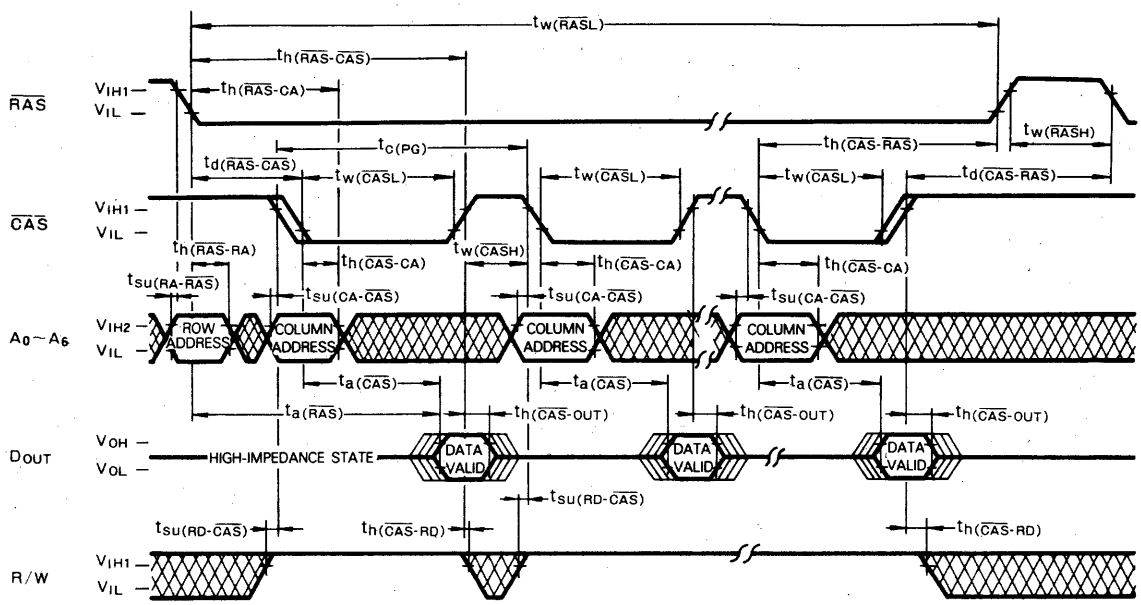


Note 13 : $\overline{CAS} = V_{IH1}$, R/W = don't care.

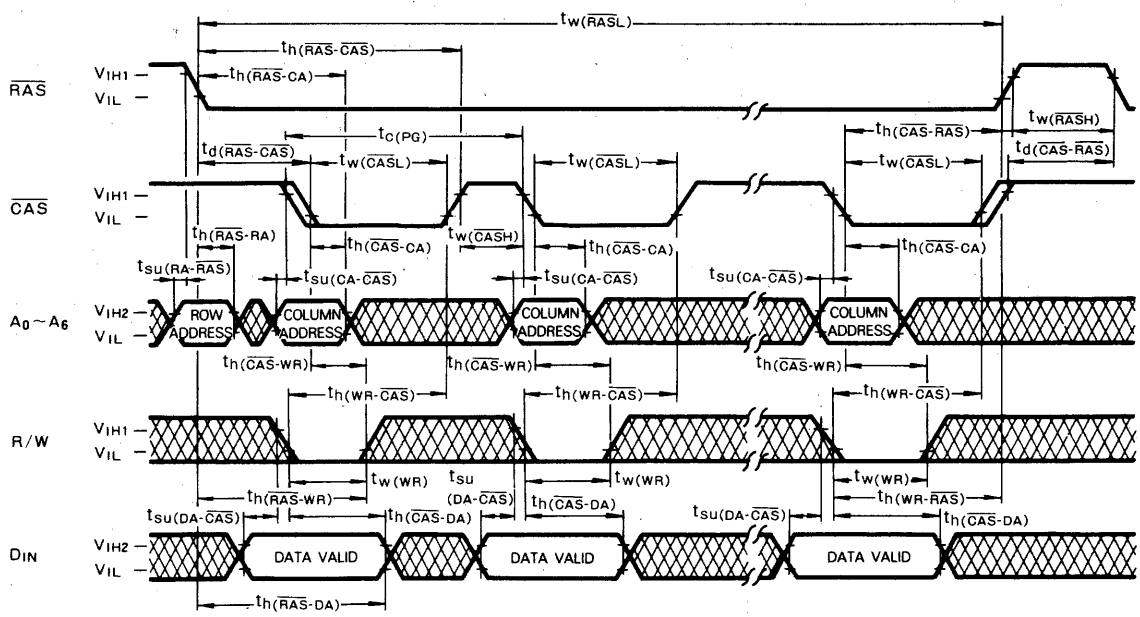
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16384-BIT (16384-WORD BY 1-BIT) DYNAMIC RANDOM-ACCESS MEMORY

Page-Mode Read Cycle



Page-Mode Write Cycle



Note 14 :

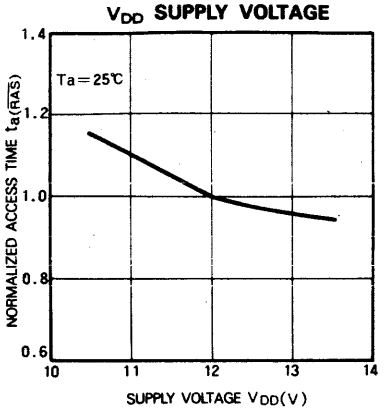
Indicates the don't care input.

The center-line indicates the high-impedance state.

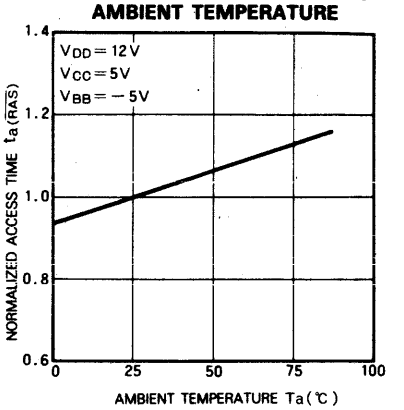
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TYPICAL CHARACTERISTICS

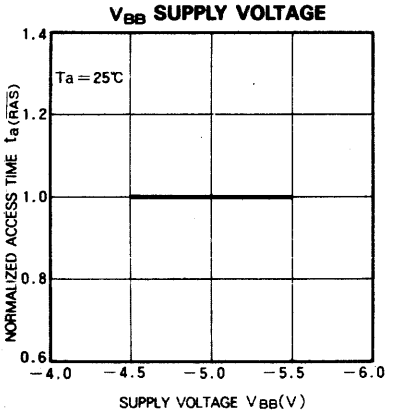
NORMALIZED ACCESS TIME VS. V_{DD} SUPPLY VOLTAGE



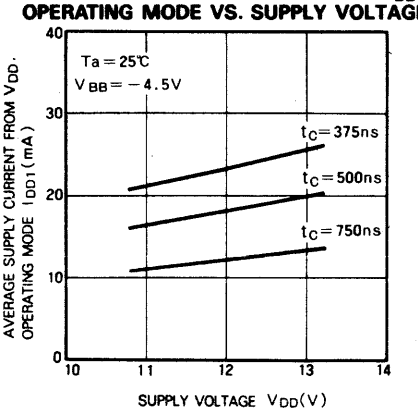
NORMALIZED ACCESS TIME VS. AMBIENT TEMPERATURE



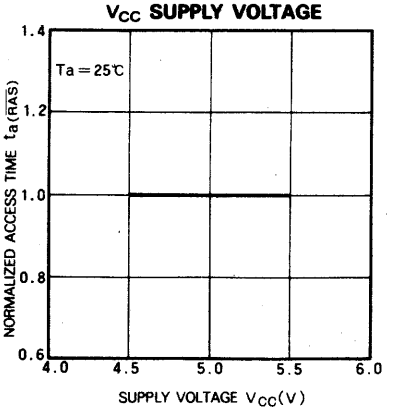
NORMALIZED ACCESS TIME VS. V_{BB} SUPPLY VOLTAGE



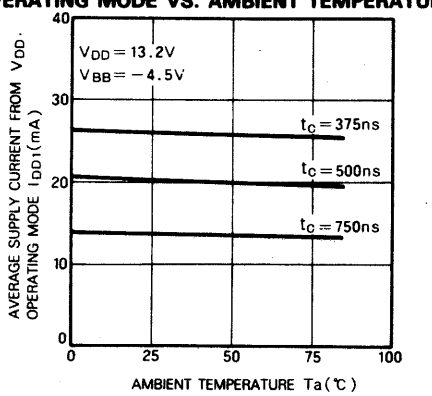
AVERAGE SUPPLY CURRENT FROM V_{DD}, OPERATING MODE VS. SUPPLY VOLTAGE



NORMALIZED ACCESS TIME VS. V_{CC} SUPPLY VOLTAGE



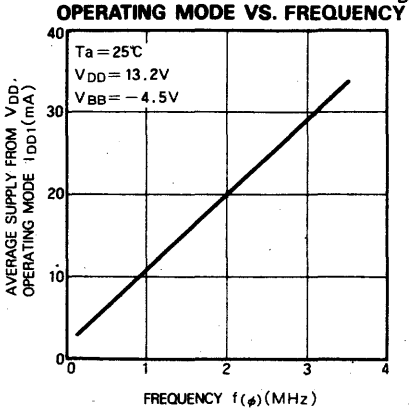
AVERAGE SUPPLY CURRENT FROM V_{DD}, OPERATING MODE VS. AMBIENT TEMPERATURE



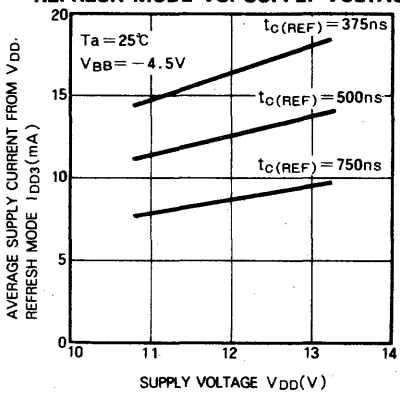
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16384-BIT (16384-WORD BY 1-BIT) DYNAMIC RANDOM-ACCESS MEMORY

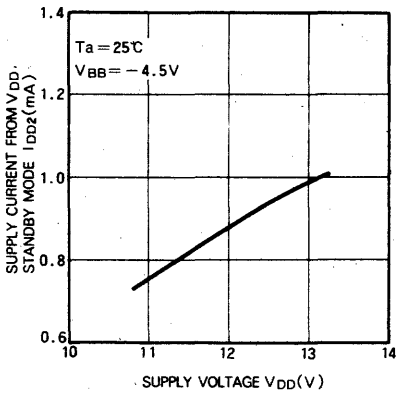
AVERAGE SUPPLY CURRENT FROM V_{DD}, OPERATING MODE VS. FREQUENCY



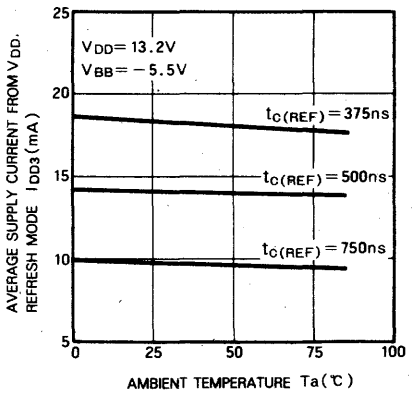
AVERAGE SUPPLY CURRENT FROM V_{DD}, REFRESH MODE VS. SUPPLY VOLTAGE



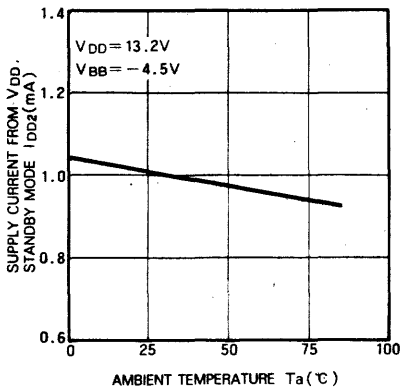
SUPPLY CURRENT FROM V_{DD}, STANDBY MODE VS. SUPPLY VOLTAGE



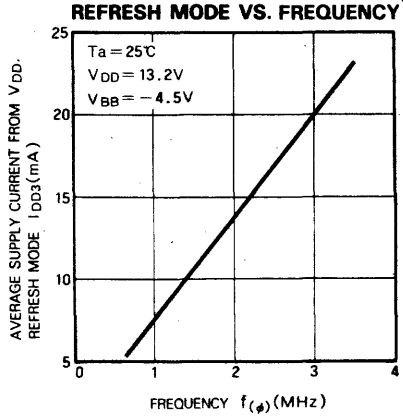
AVERAGE SUPPLY CURRENT FROM V_{DD}, REFRESH MODE VS. AMBIENT TEMPERATURE



SUPPLY CURRENT FROM V_{DD}, STANDBY MODE VS. AMBIENT TEMPERATURE

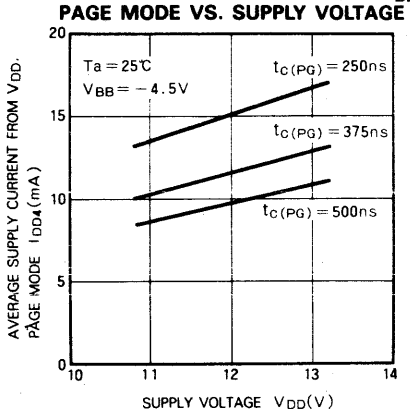


AVERAGE SUPPLY CURRENT FROM V_{DD}, REFRESH MODE VS. FREQUENCY

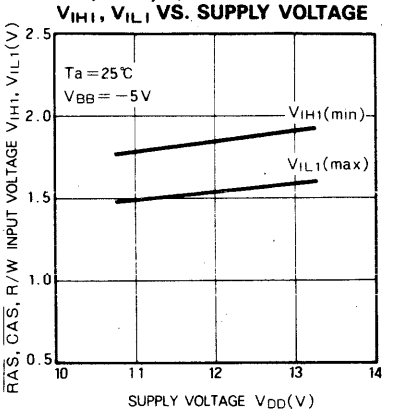


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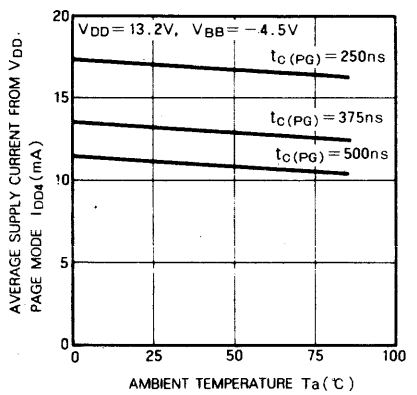
AVERAGE SUPPLY CURRENT FROM V_{DD}, PAGE MODE VS. SUPPLY VOLTAGE



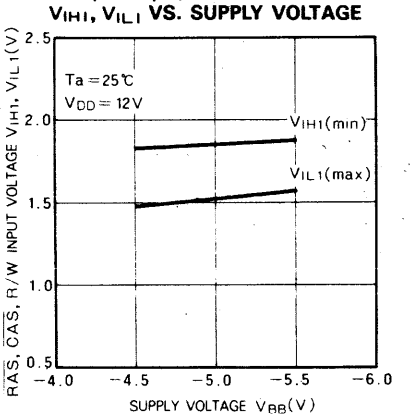
$\overline{RAS}$, $\overline{CAS}$, R/W INPUT VOLTAGE V_{IH1}, V_{IL1} VS. SUPPLY VOLTAGE



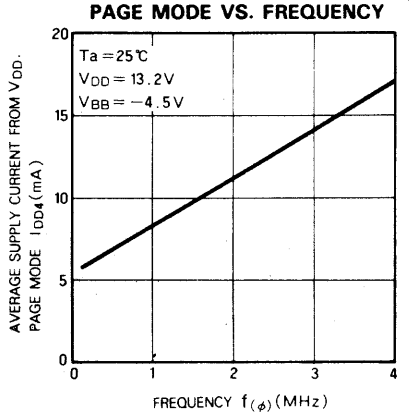
AVERAGE SUPPLY CURRENT FROM V_{DD}, PAGE MODE VS. AMBIENT TEMPERATURE



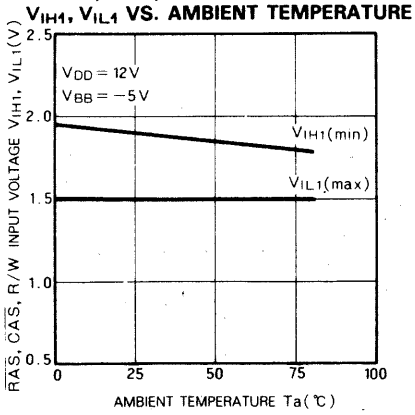
$\overline{RAS}$, $\overline{CAS}$, R/W INPUT VOLTAGE V_{IH1}, V_{IL1} VS. SUPPLY VOLTAGE



AVERAGE SUPPLY CURRENT FROM V_{DD}, PAGE MODE VS. FREQUENCY



$\overline{RAS}$, $\overline{CAS}$, R/W INPUT VOLTAGE V_{IH1}, V_{IL1} VS. AMBIENT TEMPERATURE

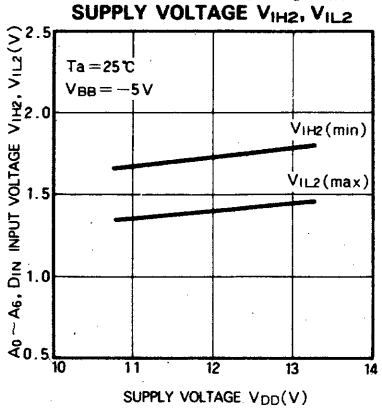


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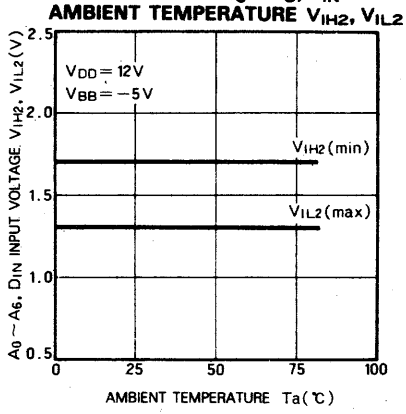
M5K 4116P,S-2, M5K 4116P,S-3, M5K 4116P,S-4

16384-BIT (16384-WORD BY 1-BIT) DYNAMIC RANDOM-ACCESS MEMORY

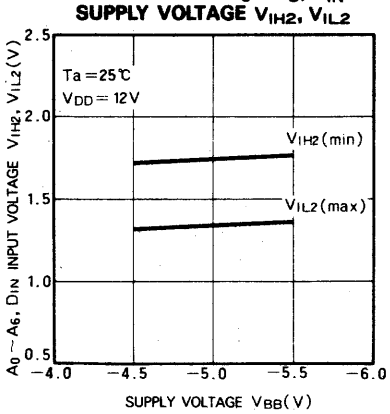
INPUT VOLTAGE $A_0 \sim A_6$, D_{IN} VS. SUPPLY VOLTAGE V_{IH2}, V_{IL2}



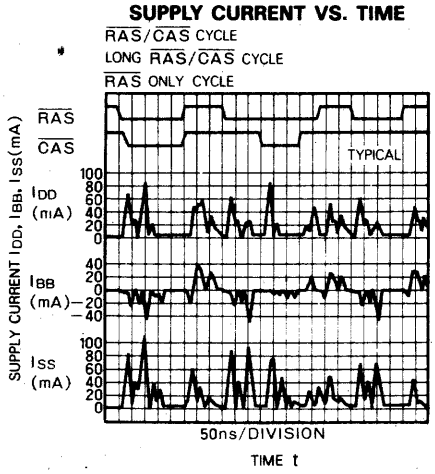
INPUT VOLTAGE $A_0 \sim A_6$, D_{IN} VS. AMBIENT TEMPERATURE V_{IH2}, V_{IL2}



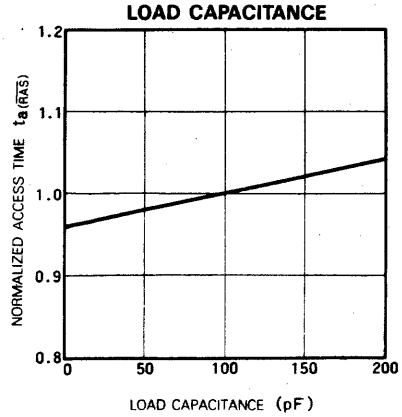
INPUT VOLTAGE $A_0 \sim A_6$, D_{IN} VS. SUPPLY VOLTAGE V_{IH2}, V_{IL2}



SUPPLY CURRENT VS. TIME



NORMALIZED ACCESS TIME VS. LOAD CAPACITANCE



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M5T4044P-20, M5T4044P-30, M5T4044P-45

4096-BIT(4096-WORD BY 1-BIT) STATIC RANDOM-ACCESS MEMORY

DESCRIPTION

The M5T 4044P series are 4096-word by 1-bit static RAMs, fabricated with the N-channel silicon-gate MOS process and designed for simple interfacing. They operate with a single 5V supply, as does TTL, and are directly TTL-compatible.

The members of the M5T 4044P series have three access time ranges; M5T 4044P-20, M5T 4044P-30, M5T 4044P-45.

FEATURES

Parameter	M5T4044P-20	M5T4044P-30	M5T4044P-45
Access time (max)	200ns	300ns	450ns
Cycle time (min)	200ns	300ns	450ns

- Low power dissipation: 50μw/bit (typ)
- Single 5V supply
- Requires no clocks or refreshing
- All inputs and outputs are directly TTL-compatible
- All outputs are three-state and have OR-tie capability
- Simple memory expansion by chip-select ($\overline{CS}$) input
- Interchangeable with TI's TMS4044 in pin configuration and electrical characteristics

APPLICATION

- Small-capacity memory units

FUNCTION

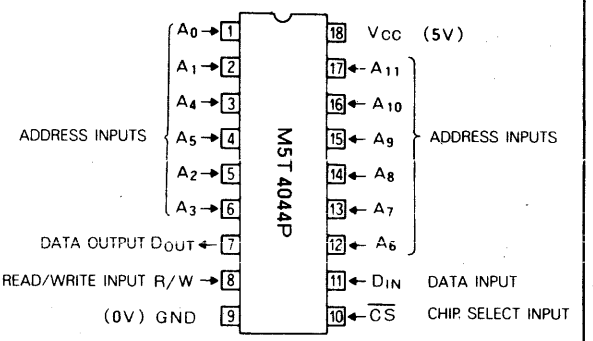
The M5T 4044P series are very convenient to use, as they feature static circuits which require neither external clocks nor refreshing, and all inputs and outputs are directly compatible with TTL.

During a write cycle, when a location is designated by address signals $A_0 \sim A_{11}$ and the R/W signal goes low, the D_{IN} signal data at that time are written.

During a read cycle, when the R/W signal goes high and a location is designated by address signals $A_0 \sim A_{11}$, the data of the designated address appear at the D_{OUT} terminals.

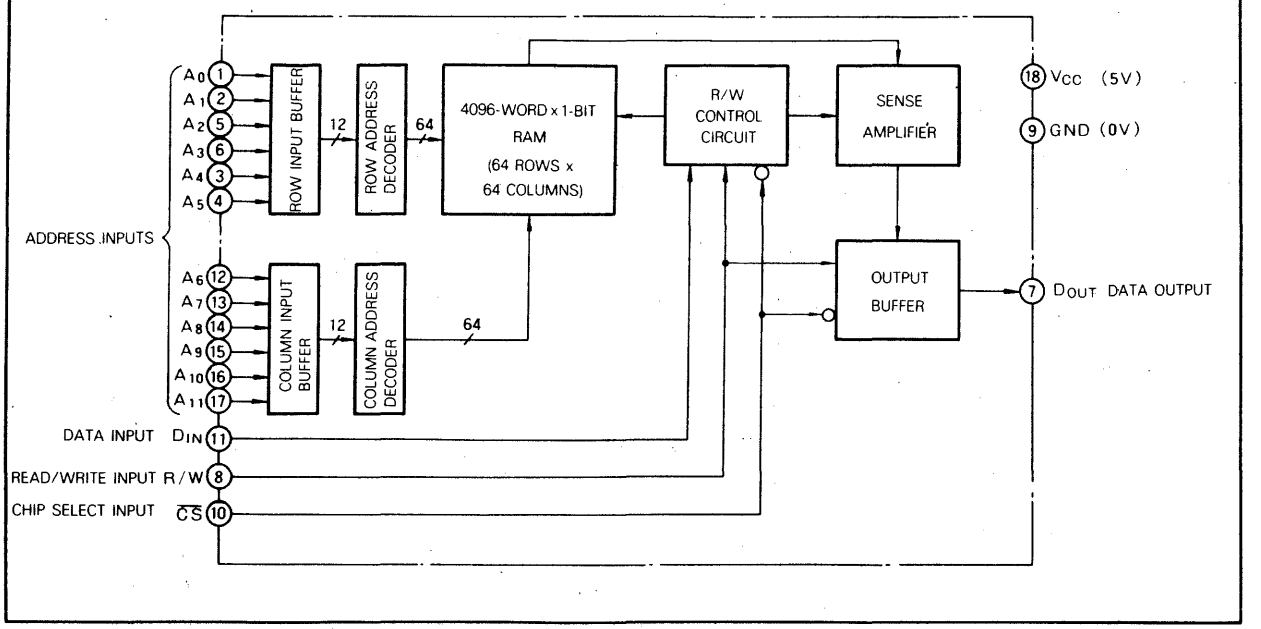
When signal $\overline{CS}$ is high, the chip is in the non-selectable state, disabling both reading and writing. In this case the output is in the floating (high-impedance) state, useful for OR-ties with other output terminals.

PIN CONFIGURATION (TOP VIEW)



Outline 18P1

BLOCK DIAGRAM



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M5T4044P-20, M5T4044P-30, M5T4044P-45

4096-BIT(4096-WORD BY 1-BIT) STATIC RANDOM-ACCESS MEMORY

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage	With respect to GND	−0.5～7	V
V_I	Input voltage		−0.5～7	V
V_O	Output voltage		−0.5～7	V
Pd	Maximum power dissipation	Ta = 25℃	700	mW
Topr	Operating free-air ambient temperature		0～70	℃
Tstg	Storage temperature		−40～−125	℃

RECOMMENDED OPERATING CONDITIONS (Ta = 0～70℃, unless otherwise noted)

Symbol	Parameter	Limits			Units
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IL}	Low-level input voltage	−0.5		0.8	V
V_{IH}	High-level input voltage	2		V_{CC}	V

ELECTRICAL CHARACTERISTICS (Ta = 0～70℃, V_{CC} = 5V ± 10%, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V_{IH}	High-level input voltage		2		V_{CC}	V
V_{IL}	Low-level input voltage		−0.5		0.8	V
V_{OH}	High-level output voltage	I_{OH} = −200μA, V_{CC} = 4.5V	2.4			V
V_{OH}	High-level output voltage	I_{OH} = −1.0mA, V_{CC} = 4.75V	2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 2.1mA			0.4	V
I_I	Input current	V_I = 0～5.5V			10	μA
I_{OZH}	Off-state high-level output current	$V_{I(\overline{CS})}$ = 2V, V_O = 2.4V～V_{CC}			10	μA
I_{OZL}	Off-state low-level output current	$V_{I(\overline{CS})}$ = 2V, V_O = 0.4V			−10	μA
I_{CC}	Supply current from V_{CC}	V_I = 5.5V, (all inputs), output open, Ta = 25℃		40	65	mA
C_I	Input capacitance, all inputs	V_I = GND, V_I = 25mVrms, f = 1MHz		3	5	pF
C_O	Output capacitance	V_O = GND, V_O = 25mVrms, f = 1MHz		5	8	pF

Note : Current flowing into an IC is positive, out is negative.

TIMING REQUIREMENTS (For Write Cycle) (Ta = 0～70℃, V_{CC} = 5V ± 10%, unless otherwise noted) (Note 2)

Symbol	Parameter	M5T4044P-20			M5T4044P-30			M5T4044P-45			Unit
		Limits			Limits			Limits			
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$t_{C(WR)}$	Write cycle time	200			300			450			ns
$t_{su(AD)}$	Address setup time with respect to write pulse	0			0			0			ns
$t_{w(WR)}$	Write pulse width	120			150			200			ns
t_{wr}	Write recovery time	0			0			0			ns
$t_{su(DA)}$	Data setup time	120			150			200			ns
$t_{h(DA)}$	Data hold time	0			0			0			ns
$t_{su(\overline{CS})}$	Chip select setup time	120			150			200			ns
$t_{PXZ(WR)}$	Output disable time with respect to write pulse			40			80			100	ns

SWITCHING CHARACTERISTICS (For Read Cycle) (Ta = 0～70℃, V_{CC} = 5V ± 10%, unless otherwise noted) (Note 2)

Symbol	Parameter	M5T4044P-20			M5T4044P-30			M5T4044P-45			Unit
		Limits			Limits			Limits			
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$t_{C(RD)}$	Read cycle time	200			300			450			ns
$t_{a(AD)}$	Address access time			200			300			450	ns
$t_{a(\overline{CS})}$	Chip select access time			70			100			100	ns
$t_{PXZ(\overline{CS})}$	Output disable time with respect to chip select			40			80			100	ns
$t_{dv(AD)}$	Data valid time with respect to address	50			50			50			ns

Note : 2 Test conditions

Input pulse level 0.8～2V

Input pulse rise time 20ns

Input pulse fall time 20ns

Reference level

Input 1.5V

Output 1.5V

Load = 1TTL, C_L = 100pF

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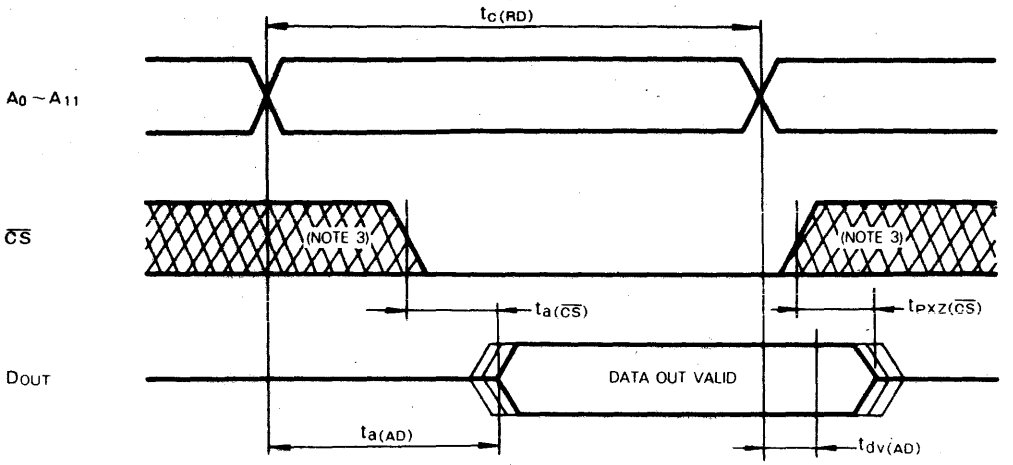
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M5T4044P-20, M5T4044P-30, M5T4044P-45

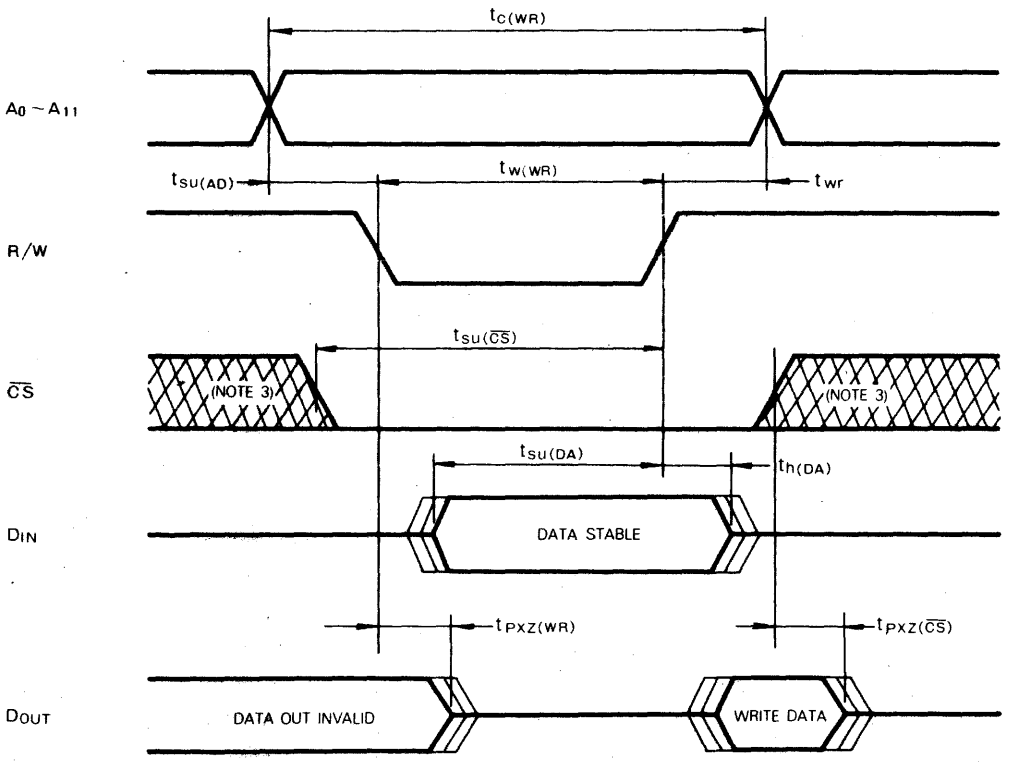
4096-BIT(4096-WORD BY 1-BIT) STATIC RANDOM-ACCESS MEMORY

TIMING DIAGRAMS

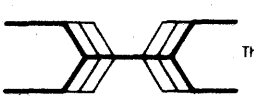
Read Cycle



Write Cycle



Note 3 : Hatching indicates the state is don't care.



The center line indicates a floating (high-impedance) state.

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M58981S-30,M58981S-45

4096-BIT (1024-WORD BY 4-BIT) CMOS STATIC RANDOM-ACCESS MEMORY

DESCRIPTION

The M58981S series consists of two 1024-word by 4-bit static RAMs fabricated with the silicon-gate CMOS process and designed for low power dissipation and easy application of battery back-up.

Each member of the series, while maintained in the chip non-select state by the chip-select signal $\overline{CS}$, consumes power only at the low value of 15μA (max) standby current and accordingly is especially suitable as a memory system for battery-operated applications and for battery back-up.

Each member operates on a single 5V supply, as does TTL, and inputs and outputs are directly TTL-compatible and are provided with common I/O terminals.

FEATURES

- Access time M58981S-30: 300ns (max)
  M58981S-45: 450ns (max)
- Low power dissipation in the standby mode: 15μA (max)
- Single 5V power supply
- Data holding at 2V supply voltage
- No external clock or refreshing operation required
- Both inputs and outputs are directly TTL-compatible
- Outputs are three-state, with OR-tie capability
- Simple memory expansion by chip-select signals
- Data terminals are common for both inputs and outputs
- Pin configuration is identical with those of Mitsubishi's M58724S (N-channel 4K static RAM), Intel's 2114, and TI's TMS4045.

APPLICATION

- Battery-driven or battery back-up small-capacity memory units

FUNCTIONS

Each member of the M58981S series has a 1024-word by 4-bit organization and provides common data input and output terminals.

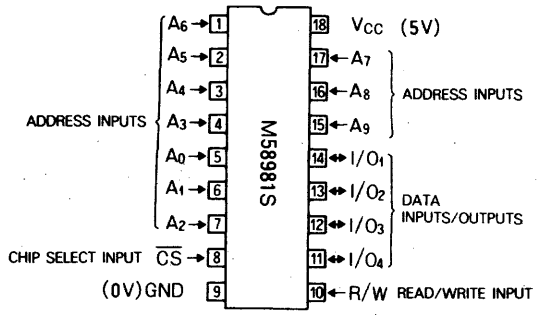
During a write cycle, when a location is designated by adress signals A_0~A_9 and signal R/W goes low, the data of the I/O at that time is written.

During a read cycle, when a location is designated by address signals A_0~A_9, and signal R/W goes high, the data of the designated address appears at the I/O terminals.

When signal $\overline{CS}$ is high, the chip is in the non-selectable state, disabling both reading and writing. In this case, the output is in the floating (high-impedance state) useful for OR-ties with the output terminals of other chips.

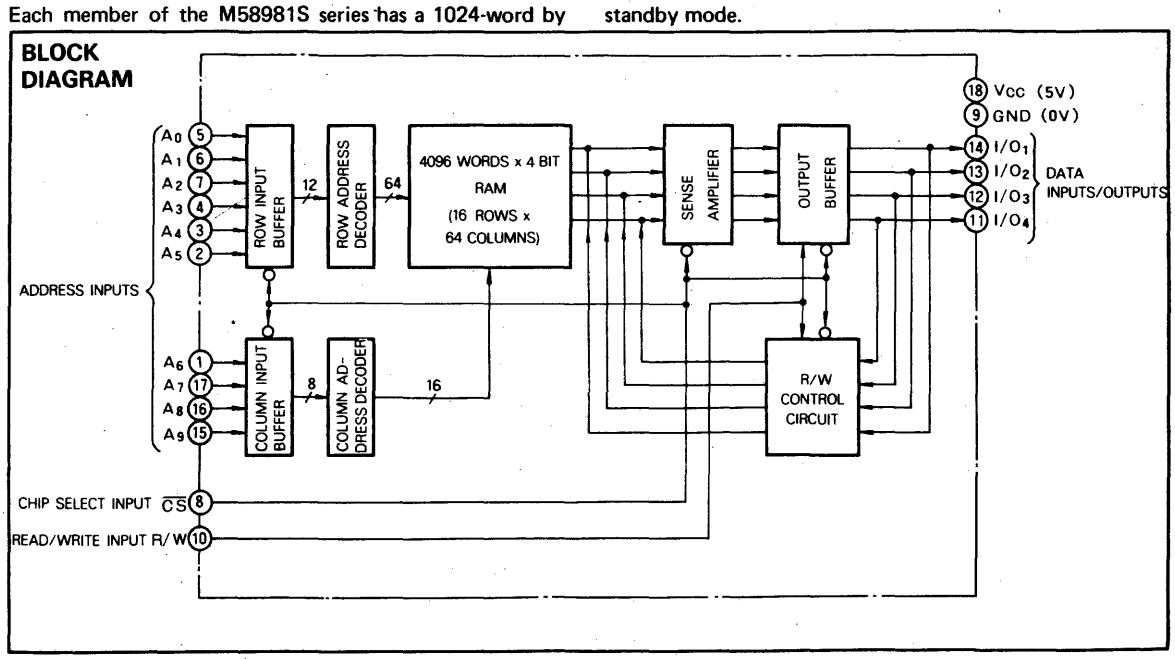
Also in the chip non-select state, the system operates with a low power dissipation, having a standby current of 15μA (max), so that the memory data can be held at a supply voltage of 2V, enabling battery back-up operation during power failure and power-down operation in the standby mode.

PIN CONFIGURATION (TOP VIEW)



Outline 18S1

BLOCK DIAGRAM



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M58981S-30,M58981S-45

4096-BIT (1024-WORD BY 4-BIT) CMOS STATIC RANDOM-ACCESS MEMORY

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage	With respect to GND	−0.3 ~ 7	V
V_I	Input voltage	With respect to GND	−0.3 ~ V_{CC} + 0.3	V
V_O	Output voltage	With respect to GND	0 ~ V_{CC}	V
P_d	Maximum power dissipation	T_a = 25℃	1000	mW
T_{opr}	Operating free-air ambient temperature		0 ~ 70	℃
T_{stg}	Storage temperature		−65 ~ 150	℃

RECOMMENDED OPERATING CONDITIONS (T_a = 0 ~ 70℃, unless otherwise noted)

Symbol	Parameter	Limits			Units
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IL}	Low-level input voltage	−0.3		0.65	V
V_{IH}	High-level input voltage	2.2		V_{CC}	V

ELECTRICAL CHARACTERISTICS (T_a = 0 ~ 70℃, V_{CC} = 5V ± 10%, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V_{IH}	High-level input voltage		2.2		V_{CC}	V
V_{IL}	Low-level input voltage		−0.3		0.65	V
V_{OH}	High-level output voltage	I_{OH} = −1mA	2.4			V
V_{OL}	Low-level output voltage	I_{OL} = 2mA			0.4	V
I_I	Input current	V_I = 0 ~ 5.5V			±1	μA
I_{OZH}	Off-state high-level output current	$V_I(\overline{CS})$ = 2.2V, V_O = 2.4V ~ V_{CC}			1	μA
I_{OZL}	Off-state low-level output current	$V_I(\overline{CS})$ = 2.2V, V_O = 0.4V			−1	μA
I_{CC1}	Supply current from V_{CC}	$\overline{CS}$ ≦ 0.01V, other inputs = V_{CC}, Output open		9		mA
I_{CC2}	Supply current from V_{CC}	$\overline{CS}$ ≦ 0.01V, other inputs = 2.2V, Output open		13		mA
I_{CC3}	Supply current from V_{CC}	$V_I(\overline{CS})$ ≧ 2.2V			15	μA
C_i	Input capacitance, all inputs	V_I = GND, V_i = 25mVrms, f = 1MHz		4	8	pF
C_o	Output capacitance	V_O = GND, V_o = 25mVrms, f = 1MHz		8	12	pF

Note : Current flowing into an IC is positive; out is negative.

TIMING REQUIREMENTS (For Write Cycle) (T_a = 0 ~ 70℃, V_{CC} = 5V ± 10%, unless otherwise noted)

Symbol	Parameter	Test conditions	M58981S-30 Limits			M58981S-45 Limits			Unit
			Min	Typ	Max	Min	Typ	Max	
$t_{c(WR)}$	Write cycle time	Input pulse V_{IH} = 2.2V, V_{OH} = 0.65V, $t_r = t_f$ = 20ns, Reference level = 1.5V, Load = 1TTL, C_L = 100pF	300			450			ns
$t_{su(AD)}$	Address setup time with respect to write pulse		100			130			ns
$t_{w(WR)}$	Write pulse width		150			250			ns
t_{wr}	Write recovery time		50			50			ns
$t_{su(DA)}$	Data setup time		200			250			ns
$t_{h(DA)}$	Data hold time		50			50			ns
$t_{su(\overline{CS})}$	Chip select setup time		250			350			ns
$t_{h(\overline{CS})}$	Chip select hold time		50			50			ns

SWITCHING CHARACTERISTICS (For Read Cycle) (T_a = 0 ~ 70℃, V_{CC} = 5V ± 10%, unless without noted)

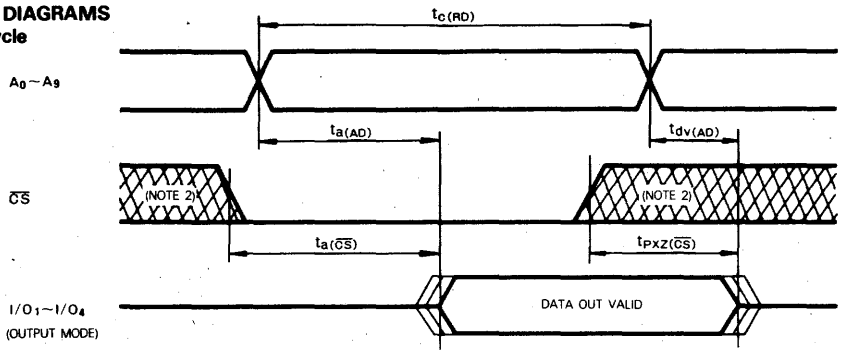
Symbol	Parameter	Test conditions	M58981S-30 Limits			M58981S-45 Limits			Unit
			Min	Typ	Max	Min	Typ	Max	
$t_{c(RD)}$	Read cycle time	Input pulse V_{IH} = 2.2V, V_{OH} = 0.6V, $t_r = t_f$ = 20ns, Reference level = 1.5V, Load = 1TTL, C_L = 100pF	300			450			ns
$t_{a(AD)}$	Address access time				300			450	ns
$t_{a(\overline{CS})}$	Chip select access time				350			500	ns
$t_{PXZ(\overline{CS})}$	Output disable time with respect to chip select				100			130	ns
$t_{dv(AD)}$	Data valid time with respect to address		0			0			ns

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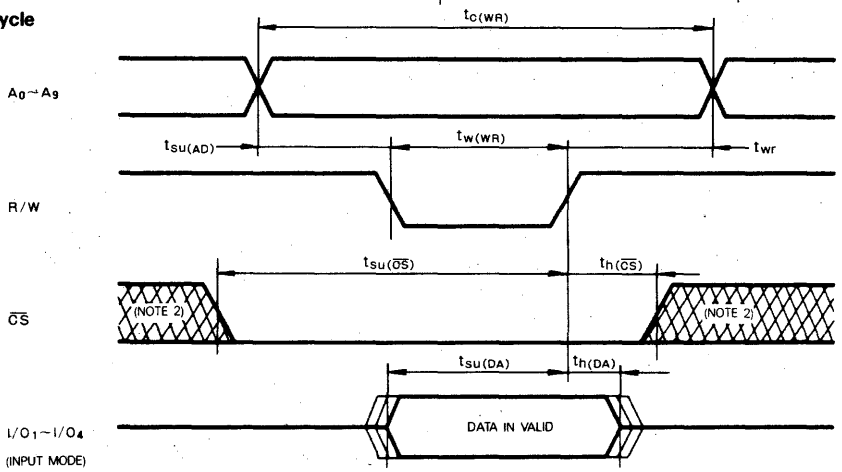
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TIMING DIAGRAMS

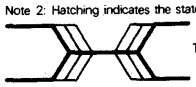
Read Cycle



Write Cycle



Note 2: Hatching indicates the state is unknown.



The center line indicates a floating (high-impedance) state.

POWER-DOWN OPERATION

Electrical Characteristics (T_a = 0 ~ 70°C, unless otherwise noted)

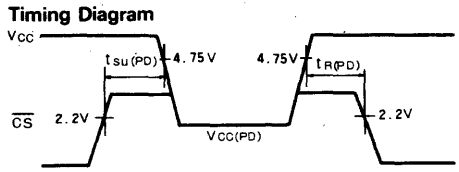
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$V_{CC(PD)}$	Power-down supply voltage		2.0			V
$V_{I(\overline{CS})}$	Power-down chip select input voltage	$2.2V \leqq V_{CC(PD)} \leqq V_{CC}$	2.2			V
		$2.0V \leqq V_{CC(PD)} \leqq 2.2V$	$V_{CC(PD)}$			V
$I_{CC(PD)}$	Power-down supply current from V_{CC}	V_{CC}=2.0V, all inputs = 2.0V			15	μA

Note : Current flowing into an IC is positive; out is negative.

Timing Requirements (T_a = 0 ~ 70°C, V_{CC} = 5V ± 10%, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Typ	Max	
$t_{su(PD)}$	Power-down setup time	0			ns
$t_{R(PD)}$	Power-down recovery time	$t_{c(RD)}$			ns

Timing Diagram



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M5L 2114LP, M5L 2114LP-2, M5L 2114LP-3

4096-BIT(1024-WORD BY 4-BIT) STATIC RANDOM-ACCESS MEMORY

DESCRIPTION

The M5L 2114LP series are 4096-bit static random-access memories organized as 1024 words of 4 bits and designed for simple interfacing. They are fabricated using N-channel silicon-gate MOS technology. They operate with a single 5V supply, as does TTL, and the inputs and outputs are directly TTL compatible. I/O terminals are common. The M5L 2114LP series has three access time ranges; M5L 2114LP, M5L 2114LP-2 and M5L 2114LP-3.

FEATURES

Parameter	M5L 2114LP-2	M5L 2114LP-3	M5L 2114LP
Access time (max)	200ns	300ns	450ns
Cycle time (min)	200ns	300ns	450ns

- Low power dissipation: 50μw/bit (typ)
- Single 5V supply voltage
- Requires neither external clock nor refreshing
- All inputs and outputs are directly TTL compatible
- All outputs are three-state, with OR-tie capability
- Easy memory expansion by chip-select ($\overline{CS}$) input
- Common data I/O terminals
- Interchangeable with Intel's 2114L and TI's TMS4045 in pin configuration and electrical characteristics.

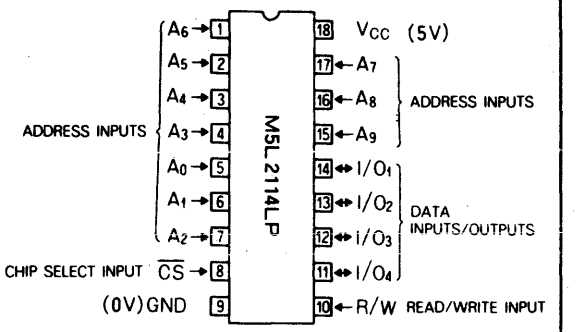
APPLICATION

- Small-capacity memory units

FUNCTION

The M5L 2114LP series operate with a single 5V power supply, and the inputs and outputs are directly compatible with TTL. All circuits are completely static, rendering external clock and refresh operations unnecessary, and making the members of the series extremely easy to use. Common data input and output terminals are provided.

PIN CONFIGURATION (TOP VIEW)



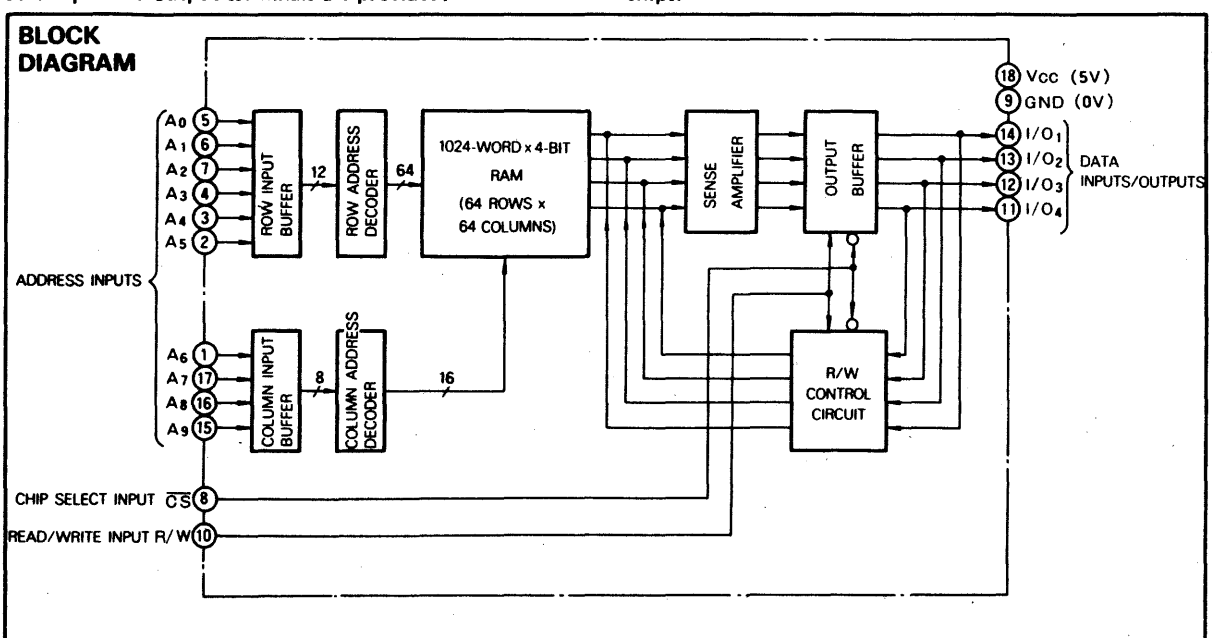
Outline 18P1

During a write cycle, when a location is designated by address signals $A_0 \sim A_9$ and the R/W signal goes low, the data at the I/O terminals are written.

During a read cycle, when the R/W signal goes high and a location is designated by address signals $A_0 \sim A_9$, the data of the designated address appear at the I/O terminals.

When signal $\overline{CS}$ is high, the chip is in the non-selectable state, disabling both reading and writing. In this case the data outputs are in the floating (high-impedance) state, useful for OR-ties with the output terminals of other chips.

BLOCK DIAGRAM



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M5L 2114LP, M5L 2114LP-2, M5L 2114LP-3

4096-BIT(1024-WORD BY 4-BIT) STATIC RANDOM-ACCESS MEMORY

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Limits	Unit
V_{CC}	Supply voltage	With respect to GND	−0.5～7	V
V_I	Input voltage		−0.5～7	V
V_O	Output voltage		−0.5～7	V
Pd	Maximum power dissipation	Ta＝25℃	700	mW
Topr	Operating free-air ambient temperature		0～70	℃
Tstg	Storage temperature		−40～125	℃

RECOMMENDED OPERATING CONDITIONS (Ta＝0～70℃, unless otherwise noted)

Symbol	Parameter	Limits			Units
		Min	Nom	Max	
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IL}	Low-level input voltage	−0.5		0.8	V
V_{IH}	High-level input voltage	2		V_{CC}	V

ELECTRICAL CHARACTERISTICS (Ta＝0～70℃, V_{CC}＝5V ± 10%, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
V_{IH}	High-level input voltage		2		V_{CC}	V
V_{IL}	Low-level input voltage		−0.5		0.8	V
V_{OH}	High-level output voltage	I_{OH}＝−200μA, V_{CC}＝4.5V	2.4			V
V_{OH}	High-level output voltage	I_{OH}＝−1mA, V_{CC}＝4.75V	2.4			V
V_{OL}	Low-level output voltage	I_{OL}＝2.1mA			0.4	V
I_I	Input current	V_I＝0～5.5V			10	μA
I_{OZH}	Off-state high-level output current	$V_{I(\overline{CS})}$＝2V, V_O＝2.4V～V_{CC}			10	μA
I_{OZL}	Off-state low-level output current	$V_{I(\overline{CS})}$＝2V, V_O＝0.4V			−10	μA
I_{CC}	Supply current from V_{CC}	V_I＝5.5V, (all inputs) output open, Ta＝25℃		40	65	mA
C_I	Input capacitance, all inputs	V_I＝GND, V_i＝25mVrms, f＝1MHz		3	5	pF
C_O	Output capacitance	V_O＝GND, V_o＝25mVrms, f＝1MHz		5	8	pF

Note : Current flowing into an IC is positive; out is negative.

TIMING REQUIREMENTS (For Write Cycle) (Ta＝0～70℃, V_{CC}＝5V ± 10%, unless otherwise noted) (Note 2)

Symbol	Parameter	Alt. symbol	M5L2114LP-2			M5L2114LP-3			M5L2114LP			Unit
			Limits			Limits			Limits			
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$t_{C(WR)}$	Write cycle time	t_{WC}	200			300			450			ns
$t_{su(AD)}$	Address setup time with respect to write pulse		0			0			0			ns
$t_{w(WR)}$	Write pulse width	t_W	120			150			200			ns
t_{wr}	Write recovery time	t_{WR}	0			0			0			ns
$t_{su(DA)}$	Data setup time	t_{DW}	120			150			200			ns
$t_{h(DA)}$	Data hold time	t_{DH}	0			0			0			ns
$t_{su(\overline{CS})}$	Chip select setup time		120			150			200			ns
$t_{PXZ(WR)}$	Output disable time with respect to write pulse	t_{OTW}			40			80			100	ns

SWITCHING CHARACTERISTICS (For Read Cycle) (Ta＝0～70℃, V_{CC}＝5V ± 10%, unless otherwise noted) (Note 2)

Symbol	Parameter	Alt. symbol	M5L2114LP-2			M5L2114LP-3			M5L2114LP			Unit
			Limits			Limits			Limits			
			Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$t_{C(RD)}$	Read cycle time	t_{RC}	200			300			450			ns
$t_{a(AD)}$	Address access time	t_A			200			300			450	ns
$t_{a(\overline{CS})}$	Chip select access time	t_{CO}			80			100			120	ns
$t_{PXZ(\overline{CS})}$	Output disable time with respect to chip select	t_{OTD}			40			80			100	ns
$t_{dv(AD)}$	Data valid time with respect to address	t_{OHA}	50			50			50			ns
$t_{PZX(\overline{CS})}$	Chip select to output active	t_{CX}	20			20			20			ns

Note : 2 Test conditions

Input pulse level 0.8～2V

Input pulse rise time 20ns

Input pulse fall time 20ns

Reference level

Input 1.5V

Output 1.5V

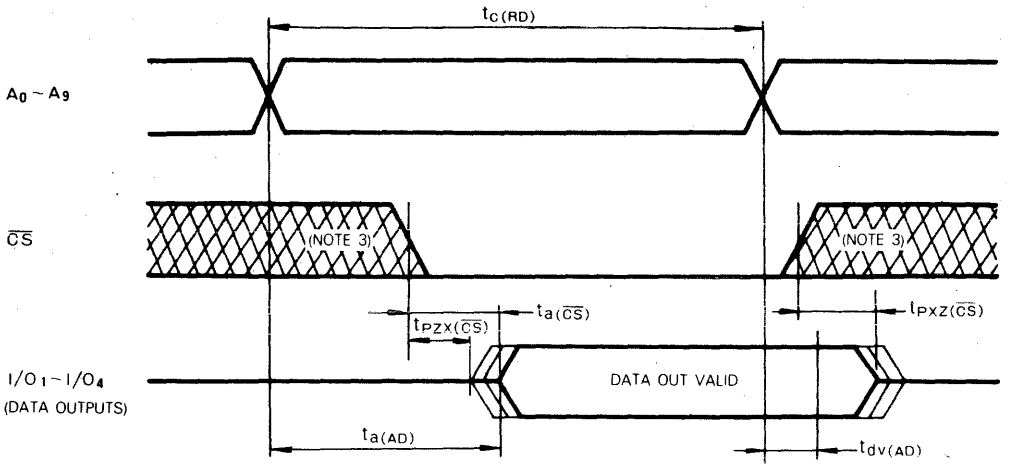
Load＝1TTL, C_L＝100pF

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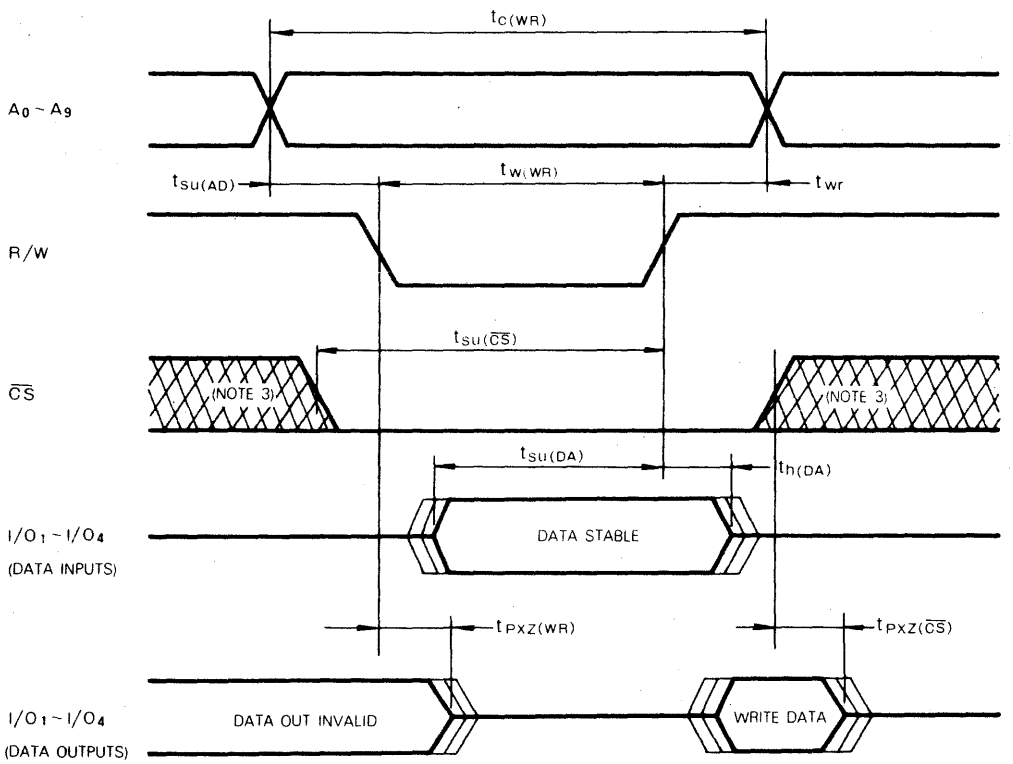
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TIMING DIAGRAMS

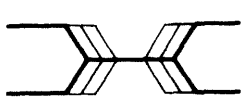
Read Cycle



Write Cycle



Note 3. Hatching indicates the state is don't care.



The center line indicates a floating (high-impedance) state.

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New publication, effective Sep. 1978.
Specifications subject to change without notice.

MITSUBISHI ELECTRIC

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M5L 2708S, M5L 2708S-65

8192-BIT (1024-WORD BY 8-BIT) ERASABLE AND ELECTRICALLY REPROGRAMMABLE ROM

DESCRIPTION

The M5L 2708S and M5L 2708S-65 are FAMOS (floating-gate avalanche-injection MOS) ultraviolet-light erasable and electrically reprogrammable 8192-bit (1024-word by 8-bit) EPROMs. They incorporate N-channel silicon-gate MOS technology, are designed for microcomputer system applications, and have direct TTL-compatibility for all inputs and outputs, without extra interface circuits.

FEATURES

- Fast programming: 100s/8192 bits (typ)
- Access time:
  - M5L 2708S: 450ns (max)
  - M5L 2708S-65: 650ns (max)
- Low power dissipation during programming
- No clocks required; the circuitry is entirely static
- Data inputs and outputs TTL-compatible during read and program modes
- Easy memory expansion by chip-select/write-enable ($\overline{CS}$/WE) input
- Typical power supply voltages: 12V, 5V, −5V
- For large volume production; pin compatible with the Mitsubishi M58730-XXXS mask ROM
- Interchangeable with Intel's 2708 in pin configuration and electrical characteristics

APPLICATION

- Computers and peripheral equipment

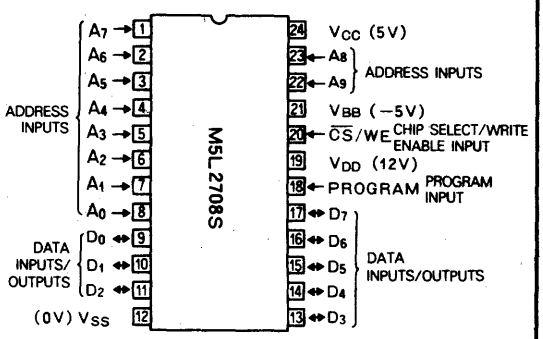
FUNCTION

Read—Set the $\overline{CS}$/WE terminal to the read mode (0~5V). Low-level input to $\overline{CS}$/WE and address signals to the address input ($A_0 \sim A_9$), make the data contents of the designated address location available at the data inputs/outputs ($D_0 \sim D_7$). When the $\overline{CS}$/WE signal is high, data inputs/outputs ($D_0 \sim D_7$) are in a floating state.

Write—Set the $\overline{CS}$/WE terminal to the write mode (12V). A program pulse will effect the write operation for the data at each address loaded via data inputs/outputs ($D_0 \sim D_7$). For details refer to the description of the programming mode.

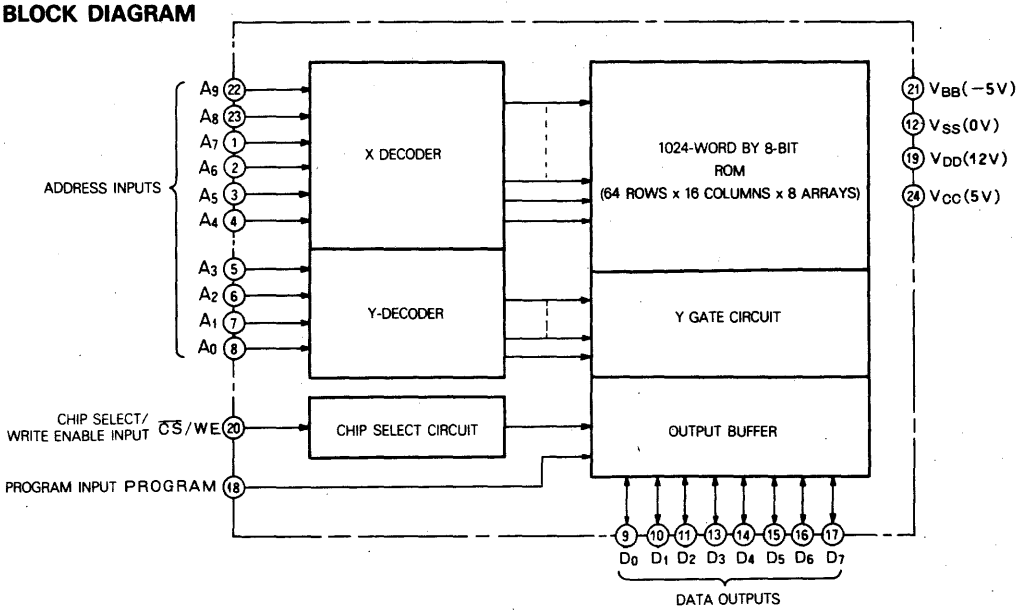
Erase—Erase is effected by exposure to ultraviolet light through the transparent window.

PIN CONFIGURATION (TOP VIEW)



Outline 24S10

BLOCK DIAGRAM



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M5L 2708S, M5L 2708S-65

8192-BIT (1024-WORD BY 8-BIT) ERASABLE AND ELECTRICALLY REPROGRAMMABLE ROM

FUNCTIONAL OPERATIONS

Programming Procedure

The M5L 2708S, S-65 are in the '1' state (with high-level output) after erase, and go into the '0' state (with low-level output) after programming. All bits of the M5L 2708S, S-65 are initially in the '1' state, and must be programmed according to the following procedures.

The chip enters the program mode when 12V is supplied to the $\overline{CS}$/WE input (pin 20). Data to be programmed are presented, 8 bits in parallel, to the data inputs/outputs ($D_0 \sim D_7$) and the addresses are set up by the address inputs. After address and data set-up, one program pulse is applied to the program input (pin 18) for each address from 0 to 1023. This pass through all addresses, known as a program loop, must be repeated a number of times, N, which depends upon the width of the program pulse and must satisfy the condition $N \cdot t_{W(P)} \geqq 100ms$.

Erase Procedure

The M5L 2708S, S-65 can be erased by exposure to high-intensity short-wave ultraviolet light at a wavelength of 2537Å through the transparent lid provided. The required exposure is approximately $15Ws/cm^2$. If the energy of the lamp used is unknown, find the total time (t_E) required to erase all bits and use a short-wave ultraviolet-light exposure time of 3 to 5 times this value.

HANDLING PRECAUTIONS FOR FAMOS DEVICES

In addition to general handling precautions for MOS devices, the following points apply to FAMOS devices.

1. High voltages are used when programming, and the conditions under which it is performed must be carefully controlled to prevent the application of excessively high voltages.
2. Before erasing, clean the surface of the transparent lid to remove completely oily impurities, which may impede irradiation and affect the erasing characteristics.
3 This ultraviolet-light erasable PROM is erasable by ultraviolet-light with wavelengths under 4,000Å. For use involving long exposure to direct sunlight or to lamps radiating at these wavelengths, the transparent window should be covered with opaque tape.

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8192-BIT (1024-WORD BY 8-BIT) ERASABLE AND ELECTRICALLY REPROGRAMMABLE ROM

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Limits	Unit
V_{I1}	Input voltage, V_{DD} and $\overline{CS}/WE$ write mode	With respect to V_{BB}	−0.3～20	V
V_{I2}	Input voltage, V_{CC}, V_{SS}, address and data signal		−0.3～15	V
V_{I3}	Input voltage, program mode		−0.3～35	V
Topr	Operating free-air temperature		0～70	℃
Tstg	Storage temperature		−65～125	℃

READ OPERATION

Recommended Operating Conditions (T_a=0～70℃, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
V_{CC}	Supply voltage	4.75	5	5.25	V
V_{DD}	Supply voltage	11.4	12	12.6	V
V_{BB}	Supply voltage	−4.75	−5	−5.25	V
V_{SS}	Supply voltage (GND)		0		V
V_{IL}	Low-level input voltage	V_{SS}		0.65	V
V_{IH}	High-level input voltage	3		V_{CC}+1	V

ELECTRICAL CHARACTERISTICS

(T_a=0～70℃, V_{CC}=5V±5%, V_{DD}=12V±5%, V_{BB}=−5V±5%, V_{SS}=0V, unless otherwise noted. Note 1)

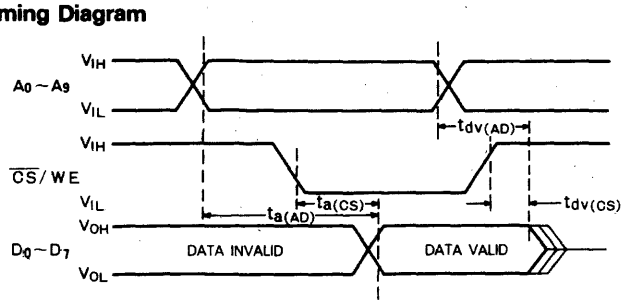
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
I_{IL}	Low-level input current, address, chip select input	V_I=5.25V			10	μA
I_{OZ}	Off-state (high-impedance-state) output current	V_O=5.25V, $V_{O(\overline{CS}/WE)}$=5V			10	μA
I_{DD}	Supply current from V_{DD}	Worst case,		50	65	mA
I_{CC}	Supply current from V_{CC}	all inputs high.		6	10	mA
I_{BB}	Supply current from V_{BB}	$V_{O(\overline{CS}/WE)}$=5V, T_a=0℃		30	45	mA
V_{OL}	Low-level output voltage	I_{OL}=1.6mA			0.45	V
V_{OH1}	High-level output voltage	I_{OH}=−100μA	3.7			V
V_{OH2}	High-level output voltage	I_{OH}=−1mA	2.4			V
Pd	Power dissipation	T_a=70℃			800	mW
C_i	Input capacitance	V_I=0V, f=1MHz		4	6	pF
C_o	Output capacitance			8	12	pF

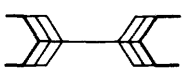
Note 1 : Typical values are at T_a=25℃ and nominal supply voltage.

SWITCHING CHARACTERISTICS (T_a=0～70℃, V_{CC}=5V±5%, V_{DD}=12V±5%, V_{BB}=−5V±5%, V_{SS}=0V, unless otherwise noted)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
$t_{a(AD)}$	Address access time	M5L 2708S			280	450	ns
		M5L 2708S-65				650	ns
$t_{a(CS)}$	Chip select access time				60	120	ns
$t_{dv(CSLH)}$	Data valid time with respect to chip select low-to-high			0		120	ns
$t_{dv(AD)}$	Data valid time with respect to address			0			ns

Timing Diagram





The center line indicates a floating (high-impedance) state.

Test Conditions for Switching Characteristics

Input voltage : V_{IL}=0.65V, V_{IH}=3V
Reference voltage at timing measurement : Input 0.8～2.8V
output 0.8～2.4V

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M5L 2708S, M5L 2708S-65

8192-BIT (1024-WORD BY 8-BIT) ERASABLE AND ELECTRICALLY REPROGRAMMABLE ROM

PROGRAM OPERATION

Recommended Operating Conditions (T_a=25℃, V_{CC}=5V±5%, V_{DD}=12V±5%, V_{BB}=−5V±5%, V_{SS}=0V, unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min	Nom	Max	
$V_{IL1(P)}$	Low-level input voltage, except program input	V_{SS}		0.65	V
$V_{IH1(P)}$	High-level input voltage, address, data input	3		V_{CC}+1	V
$V_{IH2(P)}$	High-level input voltage, $\overline{CS}$/WE	11.4		12.6	V
$V_{IH3(P)}$	High-level input voltage, program mode[1]	25		27	V
$V_{IL2(P)}$	Low-level input voltage, program mode[2]	V_{SS}		1	V

Note 1 : With respect to V_{SS}
2 : Where $V_{IH3(P)} - V_{IL2(P)}$ = 25V (min)

Electrical Characteristics (T_a=25℃, V_{CC}=5V±5%, V_{DD}=12V±5%, V_{BB}=−5V±5%, V_{SS}=0V, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$I_{IL1(P)}$	Low-level input current, address, chip select input	V_I = 5.25V			10	μA
$I_{IL2(P)}$	Low-level input current, program input				3	mA
$I_{IH1(P)}$	High-level current, program input				20	mA
I_{DD}	V_{DD} supply current	Worst case,		50	65	mA
I_{CC}	V_{CC} supply current	all inputs high[3]		6	10	mA
I_{BB}	V_{BB} supply current	$\overline{CS}$/WE = 5V, T_a = 0℃		30	45	mA

Note 3 : Typical values are at T_a = 25℃ and nominal supply voltage.

Timing Requirements (T_a=25℃, V_{CC}=5V±5%, V_{DD}=12V±5%, V_{BB}=−5V±5%, V_{SS}=0V unless otherwise noted)

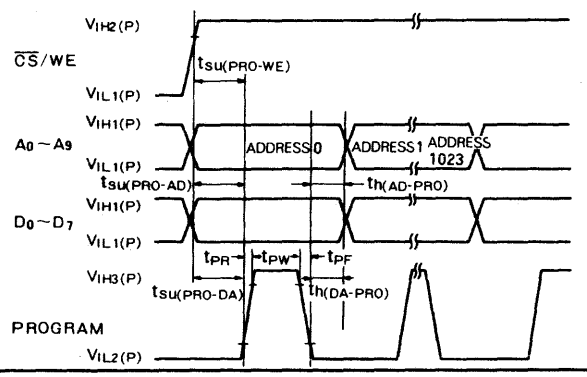
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{su(PRO-AD)}$	Program setup time with respect to address		10			μs
$t_{su(PRO-WE)}$	Program setup time with respect to WE low-to-high		10			μs
$t_{su(PRO-DA)}$	Program setup time with respect to data		10			μs
$t_{h(AD-PRO)}$	Address hold time with respect to program		1			μs
$t_{h(WE-PRO)}$	WE hold time with respect to program		0.5			μs
$t_{h(DA-PRO)}$	Data hold time with respect to program		1			μs
$t_{w(P)}$	Program pulse width		0.1		1	ms
$t_{r(P)}$	Program rise time		0.5		2	μs
$t_{f(P)}$	Program fall time		0.5		2	μs

Switching Characteristics (T_a=25℃, V_{CC}=5V±5%, V_{DD}=12V±5%, V_{BB}=−5V±5%, V_{SS}=0V, unless otherwise noted)

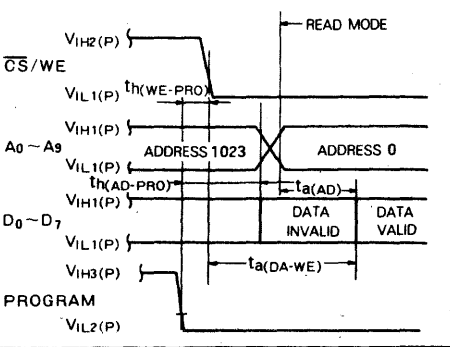
Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
$t_{a(DA-WE)}$	Access time with respect to WE high-to-low				10	μs
$t_{dv(DA-\overline{CS})}$	Data valid time with respect to $\overline{CS}$ low-to-high		0		120	ns

Timing Diagram

Program mode



From program mode to read mode



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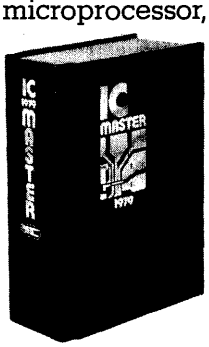
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MEMORY DESCRIPTION					MMI	AMD	FAIR-CHILD	HARRIS	INTEL	INTERSIL	MOTOROLA	NATIONAL	RAYTHEON	SIGNETICS	TI
SIZE	ORGANIZATION	PINS	OUTPUT	TYPE											
256	32x8	16	OC	STD	**6330-1**	27S08/29750		HM-7602-5		5600		—		N82S23	SN74S188
				S	**63S080***	27S18/		—		—		DM74S188		—	—
				LS	**63LS080***	27LS08		—		—		—		—	—
			TS	STD	**6331-1**	27S09/29751		HM-7603-5		5610		—		N82S123	SN74S288
				S	**63S081***	27S19/		—		—		DM74S288		—	—
				LS	**63LS081***	27LS09		—		—		—		—	—
1024	256x4	16	OC	STD	**6300-1**	29S10/29760	—	HM-7610-5	3601	5603		—	29660	N82S27/82S126	SN74S387
				S	**63S140**	27S20	93417	HM-7610A-5	—	—		DM74S387	—	—	—
				LS	**63LS140**	—	—	—	—	—		—	—	—	—
				PS	**63PS140***	—	—	—	—	—		—	29662	—	—
			TS	STD	**6301-1**	27S11/29761	—	HM-7611-5	3621	5623		—	29661	N82S129	SN74S287
				S	**63S141**	27S21	93427	HM-7611A-5	—	—		DM74S287	—	—	—
				LS	**63LS141**	—	—	—	—	—		—	—	—	—
				PS	**63PS141***	—	—	—	—	—		—	29663	—	—
2048	256x8	20	OC	STD	**6308-1**							DM74S470	29600		SN74S470
				S	**63S280***							—	—		—
				LS	**63LS280***							—	—		—
				PS	**63PS280***							—	—		—
			TS	STD	**6309-1**							DM74S471	29601		SN74S471
				S	**63S281***							—	—		—
				LS	**63LS281***							—	—		—
				PS	**63PS281***							—	—		—
		24	OC	STD	**6335-1**										
			TS	STD	**6336-1**										
		24S	TS	RA	**63RA283***										
2048	512x4	16	OC	STD	**6305-1**	27S12/29770	—	HM-7620-5	3602A	5604	MCM 7620	DM74S570	29610	N82S130	
				S	**63S240**	27S20	93436	HM-7620A-5	—	—	—	—	—	—	
				LS	**63LS240**	—	—	—	—	—	—	—	—	—	
				PS	**63PS240***	—	—	—	—	—	—	—	29612	—	
			TS	STD	**6306-1**	27S13/29771	—	HM-7621-5	3602A	5624	MCM 7621	DM74S571	29611	N82S131	
				S	**63S241**	27S21	93446	HM-7621A-5	—	—	—	—	—	—	
				LS	**63LS241**	—	—	—	—	—	—	—	—	—	
				PS	**63PS241***	—	—	—	—	—	—	—	29613	—	
4096	512x8	20	OC	STD	**6348-1**	—		HM-7648-5				DM74S473	29620	—	SN74S473
				S	**63S480***	27S28/29772		—				—	—	N82S146	—
				LS	**63LS480***	—		—				—	—	—	—
				PS	**63PS480***	—		—				—	29622	—	—
			TS	STD	**6349-1**	—		HM-7649-5				DM74S472	29621	—	SN74S472
				S	**63S481***	27S29/29773		—				—	—	N82S147	—
				LS	**63LS481***	—		—				—	—	—	—
				PS	**63PS481***	—		—				—	29622	—	—

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4096	512x8	24	OC	STD	**6340-1**	—	—	HM-7640-5	3604A	5605	MCM 7640	DM87S295	29624	N82S140	SN74S475
				S	**63S482***	27S30	93438	HM-7640A-5	—	—	—	—	—	—	—
				LS	**63LS482***	—	—	—	—	—	—	—	—	—	—
				PS	**63PS482***	—	—	—	—	—	—	—	29626	—	—
			TS	STD	**6341-1**	—	—	HM-7641-5	3624A	5625	MCM 7641	DM87S296	29625	N82S141	SN74S474
				S	**63S483***	27S31	93448	HM-7641-5	—	—	—	—	—	—	—
				LS	**63LS483***	—	—	—	—	—	—	—	—	—	—
				PS	**63PS483***	—	—	—	—	—	—	—	29627	—	—
		24S	TS	RA	**63RA483***										
4096	1024x4	18	OC	STD	**6352-1**	—	93452	HM-7642-5	3605	5606	MCM 7642	DM74S572		N82S136	—
				S	**63S440**	27S32	—	—	—	—	—	—		—	SN74S477
				LS	**63LS440**	—	—	—	—	—	—	—		—	—
				PS	**63PS440***	—	—	—	—	—	—	—		—	—
			TS	STD	**6353-1**	—	93453	HM-7643-5	3625	5626	MCM 7643	DM74S573		N82S137	—
				S	**63S441**	27S33	—	—	—	—	—	—		—	SN74S476
				LS	**63LS441**	—	—	—	—	—	—	—		—	—
				PS	**63PS441***	—	—	—	—	—	—	—		—	—
				RA	**63RA441**	—	—	—	—	—	—	—		—	—
				RS	**63RS441**	—	—	—	—	—	—	—		—	—
8192	1024x8	24	OC	STD	**6380-1**		93450	HM-7680-5	3608	5608	MCM 7680	DM87S229	29630	N82S180	SN74S479
				S	**63S880***		—	—	—	—	—	—	—	—	—
				LS	**63LS880***		—	—	—	—	—	—	—	—	—
				PS	**63PS880***		—	HM-7680P-5	—	—	—	—	29632	—	—
			TS	STD	**6381-1**		93451	HM-7681-5	3628	5618	MCM 7681	DM87S228	29631	N82S181	SN74S478
				S	**63S881***		—	—	—	—	—	—	—	—	—
				LS	**63LS881***		—	—	—	—	—	—	—	—	—
				PS	**63PS881***		—	HM-7681P-5	—	—	—	—	29633	—	—
		24S	TS	RA	**63RA883***									—	
8192	2048x4	18	OC	S	**63S840***			HM-7684-5					29650	N82S184	
				LS	**63LS840***			—					—	—	
				PS	**63PS840***			HM-7684P-5					29652	—	
			TS	S	**63S841***			HM-7685-5					29651	N82S185	
				LS	**63LS841***			—					—	—	
				PS	**63PS841***			HM-7685P-5					29653	—	
		20	TS	RA	**63RA841***										
				RS	**63RS841***										
16384	2048x8	24	OC	S	**63S1680***			HM-76160-5	3616					N82S190	
				LS	**63LS1680***			—	—					—	
				PS	**63PS1680***			—	—					—	
			TS	S	**63S1681***			HM-76161-5	3636					N82S191	
				LS	**63LS1681***			—	—					—	
				PS	**63PS1681***			—	—					—	
		24S	TS	RA	**63RA1683***										
16384	4096x4	20	OC	S	**63S1640***										
				LS	**63LS1640***										
				PS	**63PS1640***										
			TS	S	**63S1641***										
				LS	**63LS1641***										
				PS	**63PS1641***										
				RA	**63RA1641***										
				RS	**63RS1641***										

Note: Only Commercial Specification Part Numbers Are Listed.
*Preliminary Data; Check With Factory.

STD = Standard
S = High Speed Schottky
LS = Low Power
PS = Power Switched
RA = Registered Asynchronous
RS = Registered Synchronous

AMD	MMI
27LS08	**63LS080**
27LS09	**63LS081**
27S08/29750	**6330-1**
27S09/29751	**6331-1**
27S10/29760	**6300-1**
27S11/29761	**6301-1**
27S12/29770	**6305-1**
27S13/29771	**6306-1**
27S18	**63S080**
27S19	**63S081**
27S20	**63S140**
27S20	**63S240**
27S21	**63S141**
27S21	**63S241**
27S28/29772	**63S480**
27S29/29773	**63S481**
27S30	**63S482**
27S31	**63S483**
27S32	**63S440**
27S33	**63S441**

FAIRCHILD	MMI
93417	**63S140**
93427	**63S141**
93436	**63S240**
93438	**63S482**
93446	**63S241**
39448	**63S483**
93450	**6380-1**
93451	**6381-1**
93452	**6352-1**
93453	**6353-1**

HARRIS	MMI
HM-7602-5	**6331-1**
HM-7603-5	**6331-1**
HM-7610-5	**6300-1**
HM-7610A-5	**63S140**
HM-7611-5	**6301-1**
HM-7611A-5	**63S141**
HM-7620-5	**6305-1**
HM-7620A-5	**63S240**
HM-7621-5	**6306-1**
HM-7621A-5	**63S241**
HM-7648-5	**6348-1**
HM-7649-5	**6349-1**
HM-7640-5	**6340-1**
HM-7640A-5	**63S482**
HM-7641-5	**6341-1**
HM-7641-5	**63S483**
HM-7642-5	**6352-1**
HM-7643-5	**6353-1**
HM-7680-5	**6380-1**
HM-7680P-5	**63PS880**
HM-7681-5	**6381-1**
HM-7681P-5	**63PS881**
HM-7684-5	**63S840**
HM-7684P-5	**63PS840**
HM-7685-5	**63S841**
HM-7685P-5	**63PS841**
HM-7610-5	**63S1680**
HM-76161-5	**63S1681**

INTEL	MMI
3601	**6300-1**
3602A	**6305-1**
3602A	**6306-1**
3604A	**6340-1**
3605	**6352-1**
3608	**6380-1**
3616	**63S1680**
3621	**6301-1**
3624A	**6341-1**
3625	**6353-1**
3628	**6381-1**
3636	**63S1681**

INTERSIL	MMI
5600	**6330-1**
5603	**6300-1**
5604	**6305-1**
5605	**6340-1**
5606	**6352-1**
5608	**6380-1**
5610	**6331-1**
5618	**6381-1**
5623	**6301-1**
5624	**6306-1**
5625	**6341-1**
5626	**6353-1**

MOTOROLA	MMI
MCM 7620	**6305-1**
MCM 7621	**6306-1**
MCM 7640	**6340-1**
MCM 7641	**6341-1**
MCM 7642	**6352-1**
MCM 7643	**6353-1**
MCM 7680	**6380-1**
MCM 7681	**6381-1**

NATIONAL	MMI
DM74S188	**63S080**
DM74S287	**63S141**
DM74S288	**63S081**
DM74S387	**63S140**
DM74S470	**6308-1**
DM74S471	**6309-1**
DM74S472	**6349-1**
DM74S473	**6348-1**
DM74S570	**6305-1**
DM74S571	**6306-1**
DM74S572	**6352-1**
DM74S573	**6353-1**
DM87S228	**6381-1**
DM87S229	**6380-1**
DM87S295	**6340-1**
DM87S296	**6341-1**

RAYTHEON	MMI
29600	**6308-1**
29601	**6309-1**
29610	**6305-1**
29611	**6306-1**
29612	**63PS240**
29613	**63PS241**
29620	**6348-1**
29621	**6349-1**
29622	**63PS480**
29623	**63PS481**
29624	**6340-1**
29625	**6341-1**
29626	**63PS482**
29627	**63PS483**
29630	**6380-1**
29631	**6381-1**
29632	**63PS880**
29633	**63PS881**
29650	**63S840**
29651	**63S841**
29652	**63PS840**
29653	**63PS841**
29660	**6300-1**
29661	**6301-1**
29662	**63PS140**
29663	**63PS141**

SIGNETICS	MMI
N82S23	**6330-1**
N82S27/82S127	**6300-1**
N82S123	**6331-1**
N82S129	**6301-1**
N82S130	**6305-1**
N82S131	**6306-1**
N82S136	**6352-1**
N82S137	**6353-1**
N82S140	**6340-1**
N82S141	**6341-1**
N82S146	**63S480**
N82S147	**63S481**
N82S180	**6380-1**
N82S181	**6381-1**
N82S184	**63S840**
N82S185	**63S841**
N82S190	**63S1680**
N82S191	**63S1681**

TI	MMI
SN74S188	**6330-1**
SN74S287	**6301-1**
SN74S288	**6331-1**
SN74S387	**6300-1**
SN74S470	**6308-1**
SN74S471	**6309-1**
SN74S472	**6349-1**
SN74S473	**6348-1**
SN74S474	**6341-1**
SN74S475	**6340-1**
SN74S476	**63S441**
SN74S477	**63S440**
SN74S478	**6381-1**
SN74S479	**6380-1**

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Standard Performance Schottky Generic PROM Family 53/63XX-1

Features/Benefits

- Standard Schottky processing
- Reliability proven nichrome fusible links (qualified for MIL-M-38510)
- Drop in compatible ROMs
- PNP inputs for low input current
- Compatible pin configurations for upward expansion
- 4-bit-wide and 8-bit-wide for byte oriented applications

Application

- Microprogram instruction
- Microprocessor program store
- Look up table
- Character generator
- Random logic
- Code converter

Description

The 53/63XX-1-series generic PROM family offers the widest selection of sizes and organizations available in the industry. The 4-bit-wide PROMs range from 256x4 to 1024x4 and feature upward/downward pin out compatibility in the space saving 16 and 18 pin packages. The 8-bit-wide PROMs range from 32x8 to 1024x8 in a wide selection of package sizes. All PROMs have the same programming specifications allowing a single generic programmer.

The family features low input current PNP inputs, full Schottky clamping and three-state and open collector outputs. The nichrome fuses store a logical high and are programmed to the low state. Special on chip circuitry and extra fuses provide preprogramming tests which assure high programming yields and high reliability.

The 63 series is specified for operation over the commercial temperature and voltage range. The 53 series is specified for the military ranges.

Generic PROM Selection Guide

MEMORY			PACKAGE		DEVICE TYPE		INTERCHANGEABLE ROM	
SIZE	ORGANIZATION		PINS	TYPE*	0°C to +75°C	−55°C to +125°C	0°C to +75°C	−55°C to +125°C
1K	256x4	OC	16	J, N, F	6300-1	5300-1	6200-1	5200-1
		TS			6301-1	5301-1	6201-1	5201-1
2K	512x4	OC	16	J, N, F	6305-1	5305-1	6205-1	5205-1
		TS			6306-1	5306-1	6206-1	5206-1
4K	1024x4	OC	18	J, N, F	6350-1	5350-1	6250-1	5250-1
		TS			6351-1	5351-1	6251-1	5251-1
		OC			6352-1	5352-1	6252-1	5252-1
		TS			6353-1	5353-1	6253-1	5253-1
¼K	32x8	OC	16	J, N, F	6330-1	5330-1	6230-1	5230-1
		TS			6331-1	5331-1	6231-1	5231-1
2K	256x8	OC	20	J, N	6308-1	5308-1	6208-1	5208-1
		TS			6309-1	5309-1	6209-1	5209-1
		OC	24	J, N, F	6335-1	5335-1	6235-1	5235-1
		TS			6336-1	5336-1	6236-1	5236-1
4K	512x8	OC	24	J, N, F	6340-1	5340-1	6240-1	5240-1
		TS			6341-1	5341-1	6241-1	5241-1
		OC	20	J, N	6348-1	5348-1	6248-1	5248-1
		TS			6349-1	5349-1	6249-1	5249-1
8K	1024x8	OC	24	J, N, F	6380-1	5380-1	6280-1	5280-1
		TS			6381-1	5381-1	6281-1	5281-1
		OC				5384-1*	6284-1	5284-1
		TS				5385-1*	6285-1	5285-1

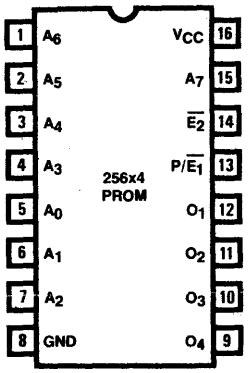
* Package Types: N is Plastic DIP, J is Ceramic DIP and F is Flat Pak

1165 East Arques Avenue, Sunnyvale, CA 94086 Tel: (408) 739-3535 TWX: 910-339-9229 Monolithic Memories

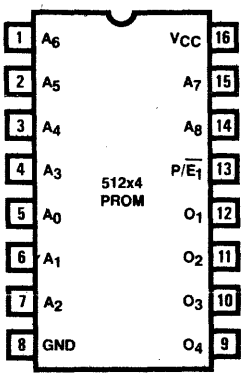
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Pin Configurations

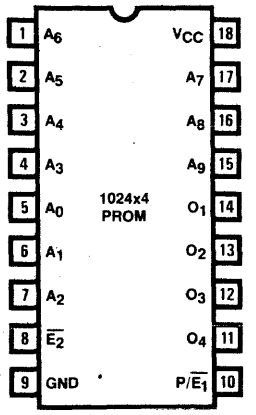
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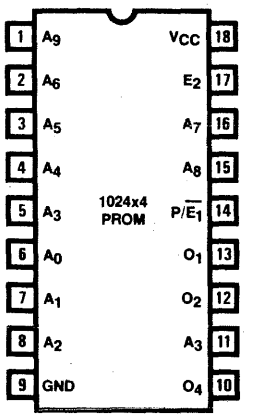
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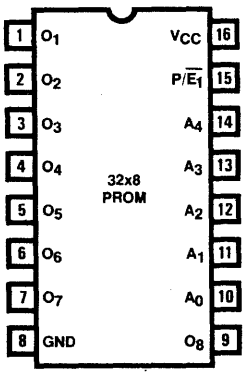
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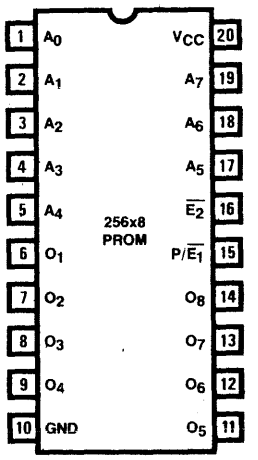
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53/6351-1



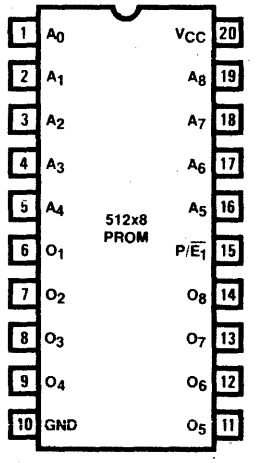
53/6330-1
53/6331-1



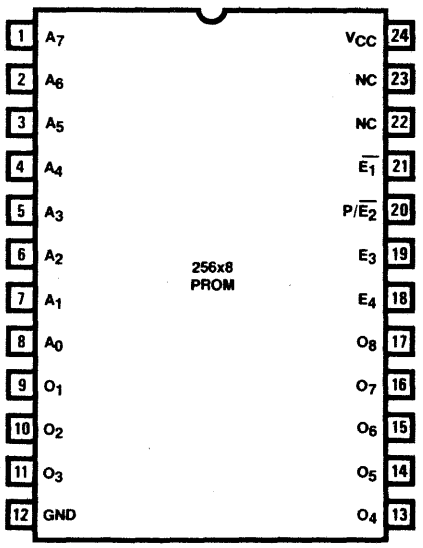
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53/6309-1



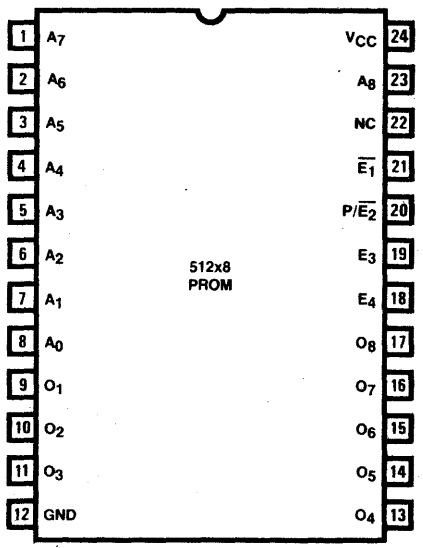
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53/6349-1



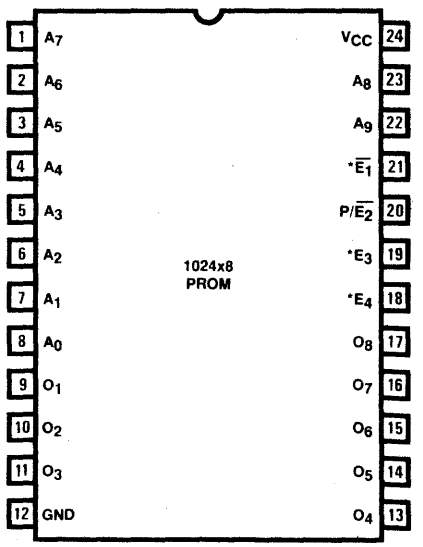
53/6335-1
53/6336-1



53/6340-1
53/6341-1



53/6380-1, *5384-1
53/6381-1, *5385-1



*NO CONNECTION Replacement for 2708 EPROM.

NOTE: Pin assignments for ceramic (J package), plastic (N package) and flat pack (F package) are the same.

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Absolute Maximum Ratings

Supply Voltage, V_{CC} ..... −0.5V to +7.0V
Input Voltage ..... −1.5V to +5.5V
Input Current ..... −20 mA to +5 mA
Output Current ..... −100 mA to +100 mA
Storage Temperature Range ..... −65°C to +150°C

Recommended Operating Conditions

SYMBOL	PARAMETER		Military MIN	Military NOM	Military MAX	Commercial MIN	Commercial NOM	Commercial MAX	UNIT
V_{CC}	Supply Voltage		4.5	5.0	5.5	4.75	5.00	5.25	V
I_{OH}	High-Level Output Current				−2.0			−3.2	mA
I_{OL}	Low-Level Output Current	'00, '01, '05, '06, '08, '09, '35, '36, '40, '41, '48, '49, '50, '51, '52, '53			12			16	mA
		'30, '31, '80, '81, '84, '85			8			12	mA
T_A	Operating Free Air Temperature		−55		125	0		75	°C

Electrical Characteristics

Over Recommended Operating Free Air Temperature Range (Unless Otherwise Noted)

SYMBOL	PARAMETER		CONDITIONS		MIN	TYP	MAX	UNIT
V_{IH}	High-Level Input Voltage				2.0			V
V_{IL}	Low-Level Input Voltage						0.8	V
V_{IC}	Input Clamp Voltage		V_{CC} = MIN, I_I = −18mA				−1.5	V
V_{OL}	Low-Level Output Voltage		V_{CC} = MIN, I_{OL} = Max				0.50	V
I_I	Maximum Input Current		V_{CC} = MAX, V_I = 4.5V (Program Pin) V_I = 5.5V (Other Inputs)				1.0	mA
I_{IH}	High-Level Input Current		V_{CC} = MAX, V_I = 2.4V				40	μA
I_{IL}	Low-Level Input Current		V_{CC} = MAX, V_I = 0.45V				−250	μA
C_I	Input Capacitance		V_{CC} = 5.0V T_A = 25°C f = 1 MHz	V_I = 2.0V		7		pF
C_O	Output Capacitance			V_O = 2.0V		8		pF
I_{CC}	Supply Current	'30, '31	V_{CC} = MAX All inputs grounded All outputs open			90	125	mA
		'00, '01, '05, '06				95	130	
		'08, '09, '48, '49				115	155	
		'35, '36, '40, '41				125	170	
		'50, '51, '52, '53				130	175	
		'80, '81, '84, '85				135	180	

OPEN COLLECTOR OUTPUT CURRENT

I_{CEX}	Output Leakage Current	V_{CC} = MAX, V_O = 2.4V		100	μA

THREE STATE OUTPUT ONLY

V_{OH}	High-Level Output Voltage	V_{CC} = MIN, I_{OH} = Max	2.4		V
I_{HZ}	High-Level OFF State Output Current	V_{CC} = MAX, V_O = 2.4V		100	μA
I_{LZ}	Low-Level OFF State Output Current	V_{CC} = MAX, V_O = 0.5V		−100	μA
I_{OS}	Output Short Circuit Current	V_{CC} = 5.0V, V_O = 0V	−20	−90	mA

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Switching Characteristics

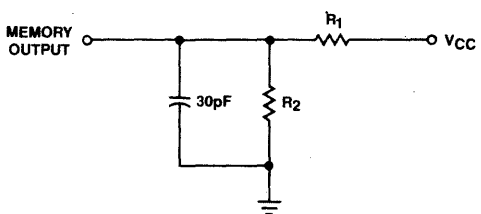
Over Recommended Ranges of T_A and V_{CC} (Unless Otherwise Noted)

DEVICE TYPE	CONDITIONS (See standard test load)		t_{AA} (ns) ADDRESS ACCESS TIME	t_{EA} & t_{ER} (ns) ENABLE ACCESS & RECOVERY TIME
	R_1 (Ω)	R_2 (Ω)	MAX	MAX
6300-1, 6301-1	300	600	55	30
5300-1, 5301-1	375	750	75	40
6305-1, 6306-1	300	600	60	30
5305-1, 5306-1	375	750	75	40
6308-1, 6309-1	300	600	70	30
5308-1, 5309-1	375	750	80	40
6330-1, 6331-1	375	750	50	30
5330-1, 5331-1	560	1120	60	40
6335-1, 6336-1	300	600	70	30
5335-1, 5336-1	375	750	80	40
6340-1, 6341-1	300	600	70	30
5340-1, 5341-1	375	750	80	40
6348-1, 6349-1	300	600	70	30
5348-1, 5349-1	375	750	80	40
6350-1, 6351-1	300	600	60	30
5350-1, 5351-1	375	750	75	40
6352-1, 6353-1	300	600	60	30
5352-1, 5353-1	375	750	75	40
6380-1, 6381-1	375	750	90	40
5380-1, 5381-1	560	1120	125	40
5384-1, 5385-1	560	1120	125	40

MMI

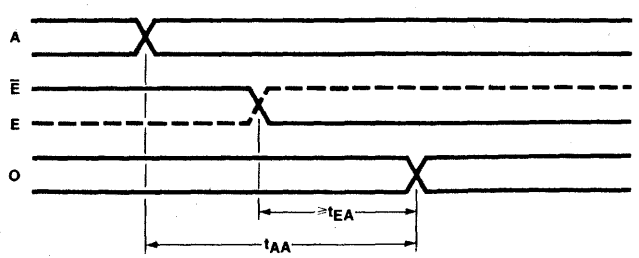
MEMORY

Standard Test Load

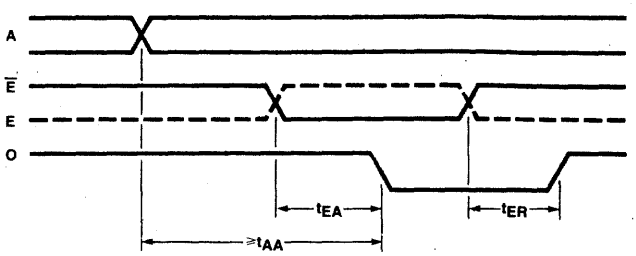


Input Pulse Amplitude 3.0V
Input Rise and Fall Times 5ns from 1.0V to 2.0V
Measurements Made at 1.5V

Definition of Waveforms



ADDRESS ACCESS TIME



ENABLE ACCESS TIME AND RECOVERY TIME

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High Performance Schottky Generic PROM Family 53/63SXXX

Features/Benefits

- **Highest speed Schottky PROM family available**
- **Advanced Schottky processing**
- **Pin compatible with standard Schottky PROMs and ROMs, 53/63XX-1, 52/62XX-1**
- **PNP inputs for low input current**
- **Compatible pin configurations for upward expansion**
- **4-bit-wide and 8-bit-wide for byte oriented applications**

Applications

- **Microprogram control store**
- **Microprocessor program store**
- **Look up table**
- **Character generator**
- **Random logic**
- **Code converter**

Description

The 53/63SXXX series generic PROM family offers the fastest and widest selection of sizes and organizations available in the industry. The 4-bit-wide PROMs range from 256x4 to 4096x4 and feature upward/downward pin out compatibility in the space saving 16, 18 and 20 pin packages. The 8-bit-wide PROMs range from 32x8 to 2048x8 in a wide selection of package sizes. All PROMs have the same programming specifications allowing a single generic programmer.

The family features low input current PNP inputs, full Schottky clamping and three-state and open collector outputs. The titanium-tungsten fuses store a logical low and are programmed to the high state. Special on chip circuitry and extra fuses provide pre-programming testing which assure high programming yields and high reliability.

The 63 series is specified for operation over the commercial temperature and voltage range. The 53 series is specified for the military ranges.

High Performance Generic PROM Selection Guide

MEMORY			PACKAGE		DEVICE TYPE	
SIZE	ORGANIZATION		PINS	TYPE	0°C to +75°C	−55°C to +125°C
¼K	32x8	OC	16	J,N,F	63S080*	53S080*
		TS			63S081*	53S081*
1K	256x4	OC	16	J,N,F	63S140	53S140
		TS			63S141	53S141
2K	512x4	OC	16	J,N,F	63S240	53S240
		TS			63S241	53S241
2K	256x8	OC	20	J,N	63S280*	53S280*
		TS			63S281*	53S281*
4K	1024x4	OC	18	J,N,F	63S440	53S440
		TS			63S441	53S441
4K	512x8	OC	20	J,N	63S480*	53S480*
		TS			63S481*	53S481*
4K	512x8	OC	24	J,N,F	63S482*	53S482*
		TS			63S483*	53S483*
8K	2048x4	OC	18	J,N,F	63S840*	53S840*
		TS			63S841*	53S841*
8K	1024x8	OC	24	J,N,F	63S880*	53S880*
		TS			63S881*	53S881*
16K	4096x4	OC	20	J,N	63S1640*	53S1640*
		TS			63S1641*	53S1641*
16K	2048x8	OC	24	J,N,F	63S1680*	53S1680*
		TS			63S1681*	53S1681

*Preliminary Data

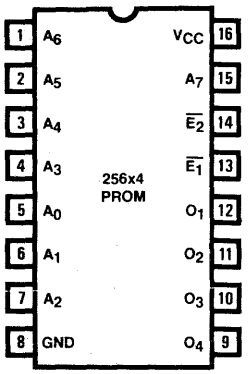
Note: This is not a final specification. Some limits of characteristics are subject to change.

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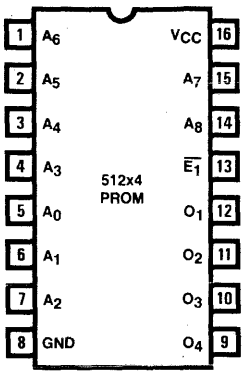
Pin Configurations

53/63S140
53/63S141



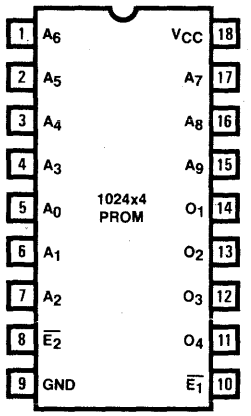
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53/63S240
53/63S241



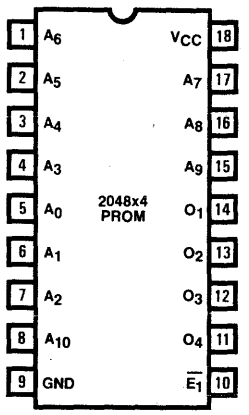
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53/63S440
53/63S441



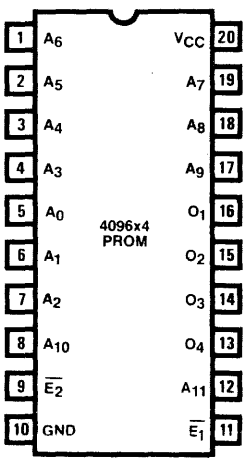
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53/63S840
53/63S841



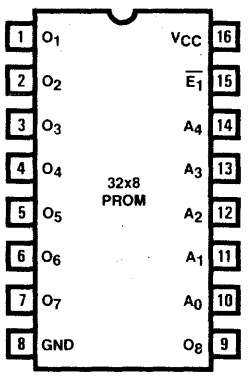
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53/63S1640
53/63S1641



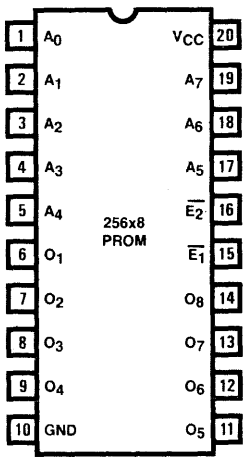
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53/63S080
53/63S080



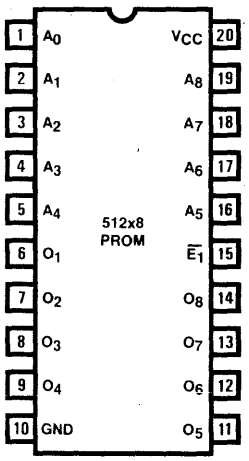
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53/63S280
53/63S281



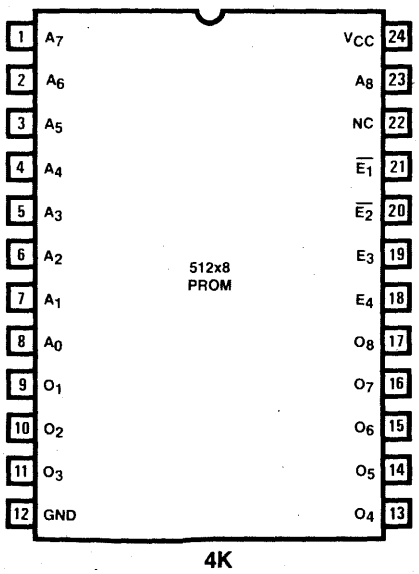
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53/63S480
53/63S481



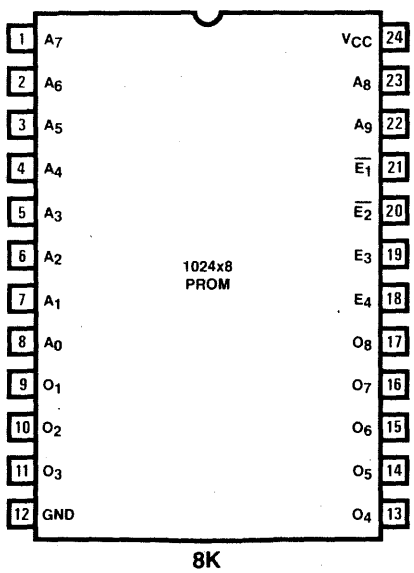
4K

53/63S482
53/63S483



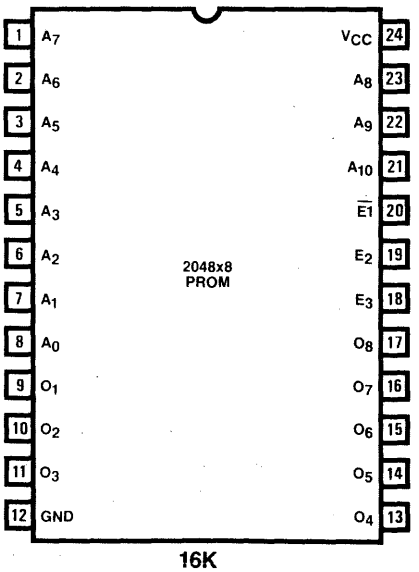
4K

53/63S880
53/63S881



8K

53/63S1680
53/63S1681



16K

NOTE: Pin assignments for ceramic (J package), plastic (N package) and flat pack (F package) are the same.

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Absolute Maximum Ratings

	Operating	Program
Supply voltage V_{CC}	−0.5V to 7V	12V
Input voltage	−1.5V to 5.5V	12V
Off-state output voltage	−1.5V to 5.5V	12V
Storage temperature range	−65°C to 150°C	

Recommended Operating Conditions

SYMBOL	PARAMETER	MILITARY MIN	MILITARY NOM	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL NOM	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage	4.5	5.0	5.5	4.75	5.00	5.25	V
I_{OH}	High level output current			−2.0			−6.5	mA
I_{OL}	Low level output current			16			16	mA
T_A	Operating free air temperature	−55		125	0		75	°C

Electrical Characteristics

Over Recommended Operating Free Air Temperature Range

SYMBOL	PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IH}	High-level input voltage				2		V_{CC}	V
V_{IL}	Low-level input voltage				0		0.8	V
V_{IC}	Input clamp voltage		V_{CC} = MIN, I_I = −18mA				−1.2	V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2V, V_{IL} = 0.8V, I_{OL} = MAX	53S			0.5	V
				63S			0.45	
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 5.5V				1.0	mA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.4V				25	μA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.4V				−250	μA
C_I	Input capacitance		V_{CC} = 5.0V, f = 1 MHz	V_I = 2.0V		4		pF
C_O	Output capacitance		T_A = 25°C	V_O = 2.0V		6		pF
I_{CC}	Supply current	080,081	V_{CC} = MAX, All inputs grounded, All outputs open			65		mA
		140,141				78	120	
		240,241				85	130	
		280,281,480,481				105		
		440,441,840,841				110	170	
		880,881,1640,1641				117		
		1680,1681				124		

OPEN COLLECTOR OUTPUT CURRENT

I_{CEX}	Output leakage current	V_{CC} = MAX, V_O = 2.4V		50	μA
		V_{CC} = MAX, V_O = 5.5V		100	μA

THREE STATE OUTPUT ONLY

V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2V, V_{IL} = 0.8V, I_{OH} = MAX	2.4		V
I_{OZH}	Off-state output current high-level voltage applied	V_{CC} = MAX, V_{IH} = 2V, V_O = 2.4V		100	μA
I_{OZL}	Off-state output current low-level voltage applied	V_{CC} = MAX, V_{IH} = 2V, V_O = 0.4V		−100	μA
I_{OS}	Short-circuit output current	V_{CC} = MAX, V_O = 0V	−30	−100	mA

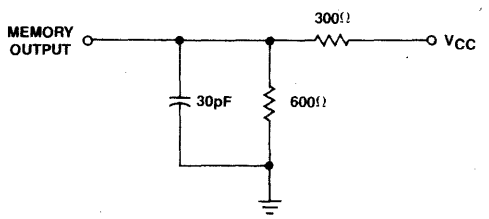
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Switching Characteristics

MAX = Over Recommended Ranges of T_A and V_{CC}
TYP = @ 5.0V V_{CC}, 25°C T_A

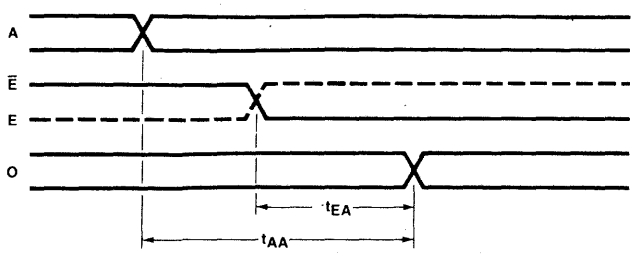
DEVICE TYPE	t_{AA}(ns) ADDRESS ACCESS TIME		t_{EA}(ns) ENABLE ACCESS TIME		t_{ER}(ns) ENABLE RECOVERY TIME	
	TYP	MAX	TYP	MAX	TYP	MAX
63S080,081	13		13		16	
53S080,081	13		13		16	
63S140,141	28	45	13	25	16	25
53S140,141	28	55	13	30	16	30
63S240,241	30	45	13	25	16	25
53S240,241	30	55	13	30	16	30
63S280,281	30		13		16	
53S280,281	30		13		16	
63S440,441	32	50	13	25	16	25
53S440,441	32	60	13	30	16	30
63S480,1,2,3	30		13		16	
53S480,1,2,3	30		13		16	
63S840,841	38		13		16	
53S840,841	38		13		16	
63S880,881	34		13		16	
53S880,881	34		13		16	
63S1640,1641	46		13		16	
53S1640,1641	46		13		16	
63S1680,1681	46		13		16	
63S1680,1681	46		13		16	

Standard Test Load

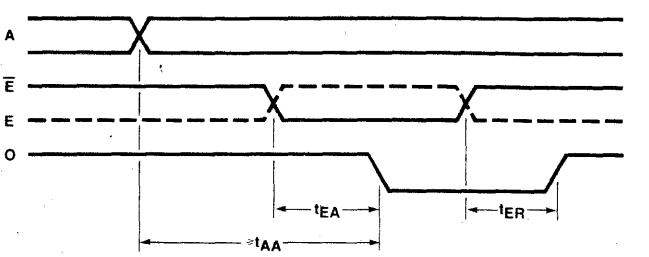


Input Pulse Amplitude 3.0V
Input Rise and Fall Times 5ns from 1.0V to 2.0V
Measurements Made at 1.5V

Definition of Waveforms

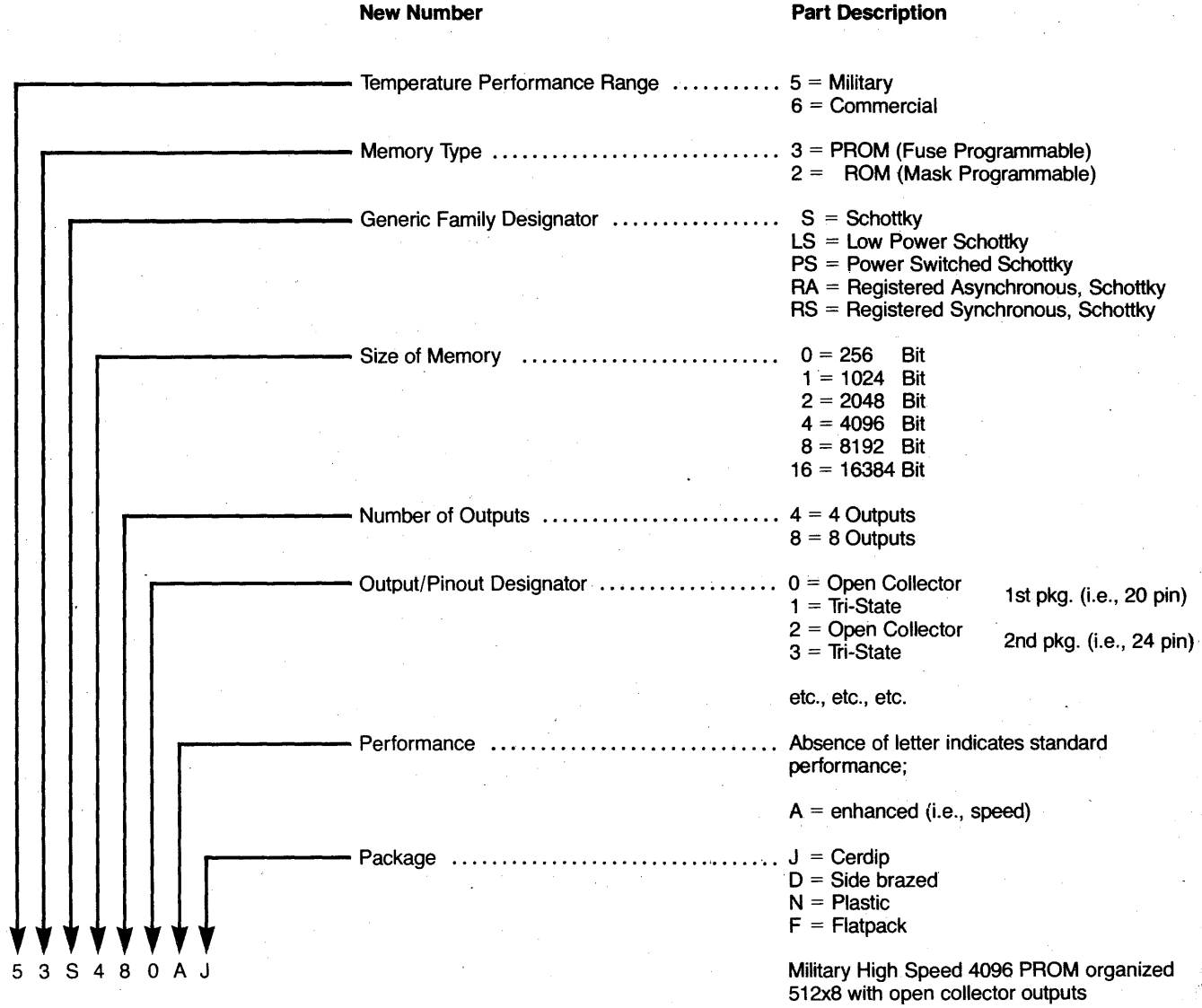


ADDRESS ACCESS TIME



ENABLE ACCESS TIME AND RECOVERY TIME

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MMI Part Numbering System

The new system approaches part numbering using the method of keying important attributes of the device. The military/commercial and PROM/ROM numbering system is preserved i.e., 5/6 - 3/2. These two digits are separated from the actual device number by a technology/configuration designator using letters.

"S" = Schottky
"LS" = Low Power Schottky
"PS" = Power Switched
"RA" = Registered Asynchronous
"RS" = Registered Synchronous

The number following this code describes....

1. The size of the memory (bits)
2. The memory organization by specifying the number of outputs
3. Output configuration and pin out/package options

If a higher performance part co-exists i.e., faster speed, then a suffix letter (A) is added to distinguish between the two devices. The normal package letter designator follows last as is custom.

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High Performance Low Power Schottky Generic PROM Family 53/63LSXXX

Features/Benefits

- **Largest generic low power Schottky PROM family available**
- **Advanced Schottky processing using ion implanted for low power and high speed**
- **Pin compatible with standard Schottky PROMs and ROMs, 53/63XX-1, 52/62XX-1**
- **PNP inputs for low input current**
- **Compatible pin configurations for upward expansion**
- **4-bit-wide and 8-bit-wide for byte oriented applications**

Applications

- **Microprogram control store**
- **Microprocessor program store**
- **Look up table**
- **Character generator**
- **Random logic**
- **Code converter**

Description

The 53/63LSXXX series generic PROM family offers the lowest power and fastest speeds available in the industry. The 4-bit-wide PROMs range from 256x4 to 2048x4 and feature upward/downward pin out compatibility in the space saving 16 and 18 pin packages. The 32x8 PROM is also included in our low power Schottky family and a typical access time of 24 ns makes it a natural programmable logic element choice. Other 8-bit- wide PROMs are available up to 2048x8. All PROMs have the same programming specifications allowing a single generic programmer.

The family features low input current PNP inputs, full Schottky clamping and three-state and open collector outputs. The titanium-tungsten fuses store a logical low and are programmed to the high state. Special on chip circuitry and extra fuses provide pre-programming testing which assure programming yields and high reliability.

The 63 series is specified for operation over the commercial temperature and voltage range. The 53 series is specified for the military range.

High Performance Low Power Schottky Generic PROM Selection Guide

MEMORY			PACKAGE		DEVICE TYPE	
SIZE	ORGANIZATION		PINS	TYPE	0°C to +75°C	−55°C to +125°C
¼K	32x8	OC	16	J,N,F	63LS080*	53LS080*
		TS			63LS081*	53LS081*
1K	256x4	OC	16	J,N,F	63LS140	53LS140
		TS			63LS141	53LS141
2K	512x4	OC	16	J,N,F	63LS240	53LS240
		TS			63LS241	53LS241
2K	256x8	OC	20	J,N	63LS280*	53LS280*
		TS			63LS281*	53LS281*
4K	1024x4	OC	18	J,N,F	63LS440	53LS440
		TS			63LS441	53LS441
4K	512x8	OC	20	J,N	63LS480*	53LS480*
		TS			63LS481*	53LS481*
4K	512x8	OC	24	J,N,F	63LS482*	53LS482*
		TS			63LS483*	53LS483*
8K	2048x4	OC	18	J,N,F	63LS840*	53LS840*
		TS			63LS841*	53LS841*
8K	1024x8	OC	24	J,N,F	63LS880*	53LS880*
		TS			63LS881*	53LS881*
16K	4096x4	OC	20	J,N	63LS1640*	53LS1640*
		TS			63LS1641*	53LS1641*
16K	2048x8	OC	24	J,N,F	63LS1680*	53LS1680*
		TS			63LS1681*	53LS1681*

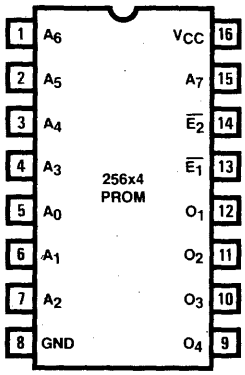
*Preliminary Data Note: This is not a final specification. Some limits of characteristics are subject to change.

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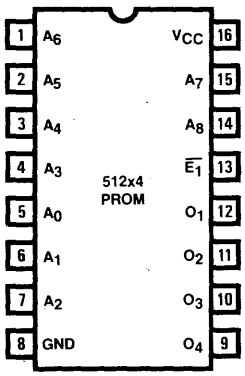
Pin Configurations

53/63LS140
53/63LS141



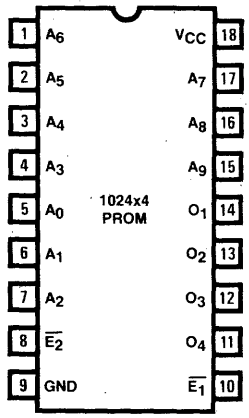
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53/63LS240
53/63LS241



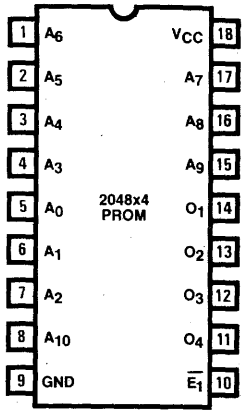
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53/63LS440
53/63LS441



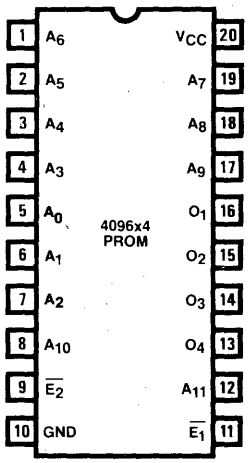
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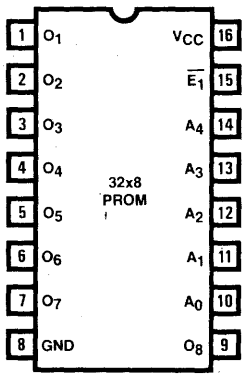
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53/63LS1641



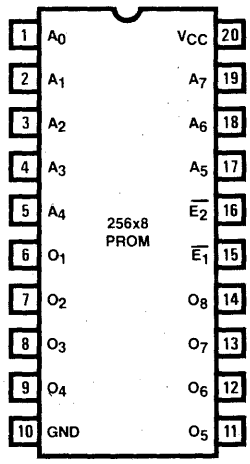
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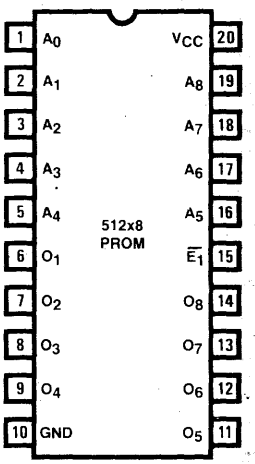
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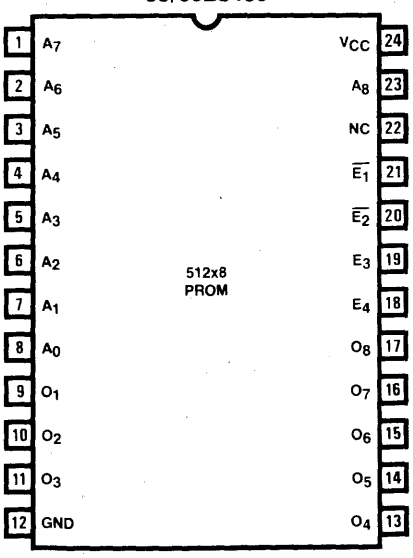
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53/63LS481



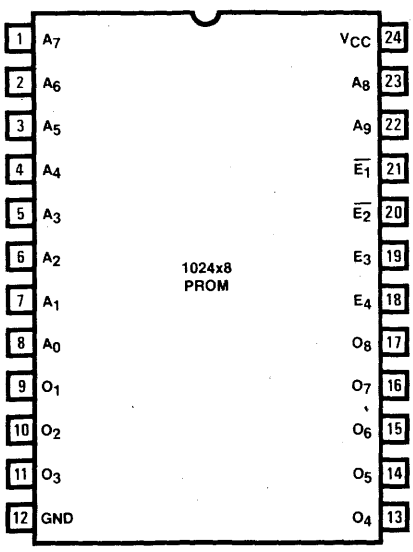
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53/63LS482
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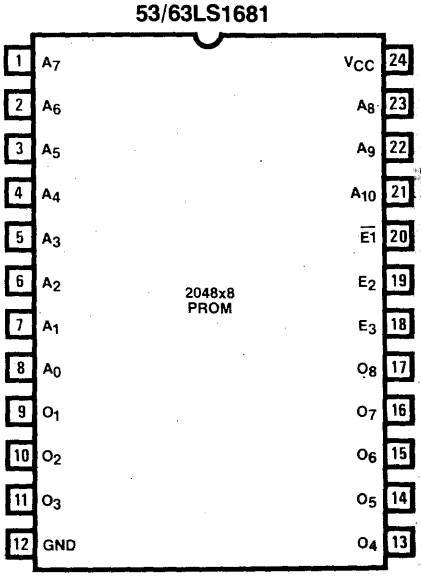
4K

53/63LS880
53/63LS881



8K

53/63LS1680
53/63LS1681



16K

NOTE: Pin assignments for ceramic (J package), plastic (N package) and flat pack (F package) are the same

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Absolute Maximum Ratings

	Operating	Program
Supply voltage V_{CC}	−.5V to 7V	12V
Input voltage	−1.5V to 5.5V	12V
Off-state output voltage	−1.5V to 5.5V	12V
Storage temperature range	−65°C to 150°C	

Recommended Operating Conditions

SYMBOL	PARAMETER	MILITARY MIN	MILITARY NOM	MILITARY MAX	COMMERCIAL MIN	COMMERCIAL NOM	COMMERCIAL MAX	UNIT
V_{CC}	Supply voltage	4.5	5.0	5.5	4.75	5.00	5.25	V
I_{OH}	High-level output current			−2.0			−6.5	mA
I_{OL}	Low-level output current			12			16	mA
T_A	Operating free air temperature	−55		125	0		75	°C

Electrical Characteristics

Over Recommended Operating Free Air Temperature Range

SYMBOL	PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IH}	High-level input voltage				2		V_{CC}	V
V_{IL}	Low-level input voltage				0		0.8	V
V_{IC}	Input clamp voltage		V_{CC} = MIN, I_I = −18mA				−1.2	V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2V, V_{IL} = 0.8V, I_{OL} = MAX	53LS			0.5	V
				63LS			0.45	
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 5.5V				1.0	mA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.4V				25	μA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.4V				−250	μA
C_I	Input capacitance		V_{CC} = 5.0V, f = 1 MHz, T_A = 25°C	V_I = 2.0V		4		pF
C_O	Output capacitance			V_O = 2.0V		6		pF
I_{CC}	Supply current	080,081	V_{CC} = MAX, All inputs grounded, All outputs open			35		mA
		140,141				46	65	
		240,241				49	70	
		280,281,480,481				55		
		440,441,840,841				60	85	
		880,881,1640,1641				63		
		1680,1681				67		

OPEN COLLECTOR OUTPUT CURRENT

I_{CEX}	Output leakage current	V_{CC} = MAX, V_O = 2.4V		50	μA
		V_{CC} = MAX, V_O = 5.5V		100	μA

THREE STATE OUTPUT ONLY

V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2V, V_{IL} = 0.8V, I_{OH} = MAX	2.4		V
I_{OZH}	Off-state output current high-level voltage applied	V_{CC} = MAX, V_{IH} = 2V, V_O = 2.4V		100	μA
I_{OZL}	Off-state output current low-level voltage applied	V_{CC} = MAX, V_{IH} = 2V, V_O = 0.4V		−100	μA
I_{OS}	Short-circuit output current	V_{CC} = MAX, V_O = 0V	−30	−100	mA

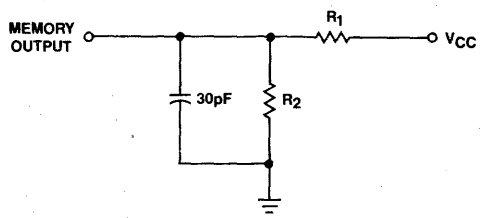
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Switching Characteristics

MAX = Over Recommended Ranges of T_A and V_{CC}
TYP = 5.0V V_{CC}, 25°C T_A

DEVICE TYPE	t_{AA}(ns) ADDRESS ACCESS TIME		t_{EA}(ns) ENABLE ACCESS TIME		t_{ER}(ns) ENABLE RECOVERY TIME	
	TYP	MAX	TYP	MAX	TYP	MAX
63LS080,081	24		15		21	
53LS080,081	24		15		21	
63LS140,141	40	55	15	30	21	30
53LS140,141	40	65	15	35	21	35
63LS240,241	42	60	15	30	21	30
53LS240,241	42	70	15	35	21	35
63LS280,281	51		15		21	
53LS280,281	51		15		21	
63LS440,441	53	65	15	30	21	30
53LS440,441	53	75	15	35	21	35
63LS480,1,2,3	51		15		21	
53LS480,1,2,3	51		15		21	
63LS840,841	62		15		21	
53LS840,841	62		15		21	
63LS880,881	55		15		21	
53LS880,881	55		15		21	
63LS1640,1641	66		15		21	
53LS1640,1641	66		15		21	
63LS1680,1681	66		15		21	
53LS1680,1681	66		15		21	

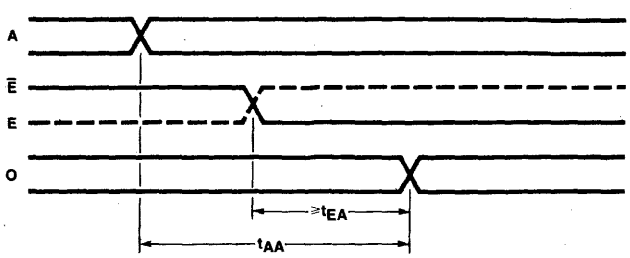
Standard Test Load



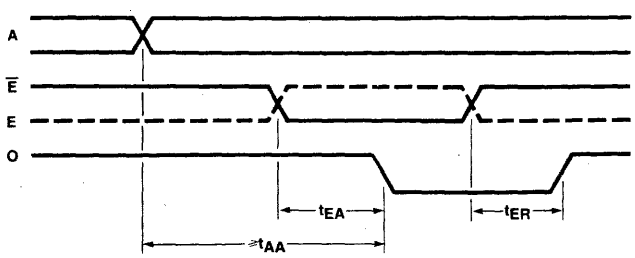
Input Pulse Amplitude 3.0V
Input Rise and Fall Times 5ns from 1.0V to 2.0V
Measurements Made at 1.5V

R_1 = 300Ω for 63LSXXX
R_2 = 600Ω for 63LSXXX
R_1 = 375Ω for 53LSXXX
R_2 = 750Ω for 53LSXXX

Definition of Waveforms



ADDRESS ACCESS TIME



ENABLE ACCESS TIME AND RECOVERY TIME

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High Performance Registered Schottky—4-Bit-Wide Generic PROM Family
53/63RAXXX, 53/63RSXXX

Features/Benefits
- **Largest generic PROM family available incorporating edge triggered "D" registers.**
- **Advanced Schottky processing.**
- **4-bit-wide in 18 and 20 pin Skinny DIPs™ for high board density.**
- **Synchronous enable allow easy busing of outputs for word expansion.**
- **Lower system package counts.**
- **Lower system power.**
- **Faster cycle times.**
- **25ns clock to output and 40ns address set-up times guaranteed over commercial specification.**
- **24mA I_{OL} output drive capability.**

Applications
- **Pipelined microprogramming**
- **State sequencers**
- **Next address generation**
- **Mapping PROM**

Description
A family of registered PROMs offers new savings for designers of pipelined microprogrammable systems. The wide instruction register, which holds the microinstruction during execution, is now incorporated into the PROM chip.

Edge Triggered Register
The PROM output is loaded into a 4-bit register on the rising edge of the clock. The use of the term "register" is to be distinguished from the term "latch," in that a register contains master slave flip-flops and the latch contains gated flip-flops. The advantages of using a register are that system timing is simplified, and faster micro cycle times can be obtained.

The output of the register is buffered by three-state drivers which are compatible with the new low-power Schottky three-state bus standard, i.e., I_{OL} is 24mA at V_{OL} of 0.5V.

The 4-bit-wide family in 18-pin and 20-pin packages feature either synchronous or asynchronous enables the synchronous enables and upwards pin compatibility. The synchronous enable powers up in the high impedance state and is used when more than one registered PROM is bused together to increase word length. All devices are specified over both commercial and military temperature ranges.

High Performance Generic PROM Selection Guide

MEMORY			PACKAGE		DEVICE TYPE	
SIZE	ORGANIZATION		PINS	TYPE	0°C to 75°C	−55°C to 125°C
4K	1024x4	ASYN	18	J,N,F	63RA441	53RA441
		SYN			63RS441	53RS441
8K	2048x4	ASYN	20	J,N	63RA841*	53RA841*
		SYN			63RS841*	53RS841*
16K	4096x4	ASYN	20	J,N	63RA1641*	53RA1641*
		SYN			63RS1641*	53RS1641*

*Preliminary Data
Note: This is not a final specification. Some limits of characteristics are subject to change.

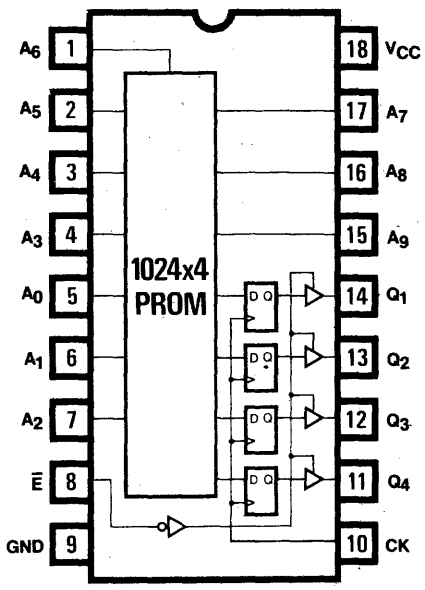
™ Skinny DIP is a trademark of Monolithic Memories

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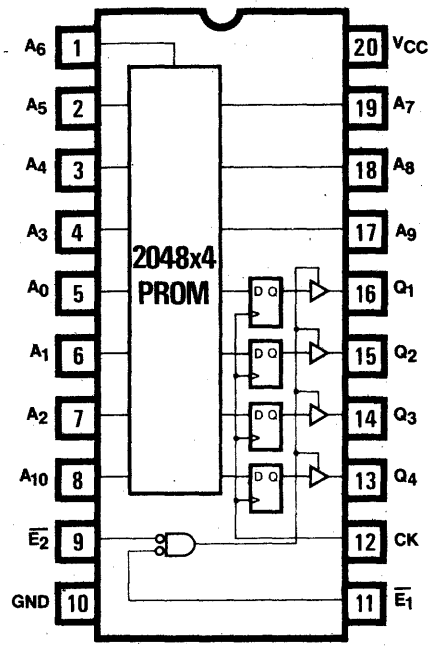
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Pin Configurations

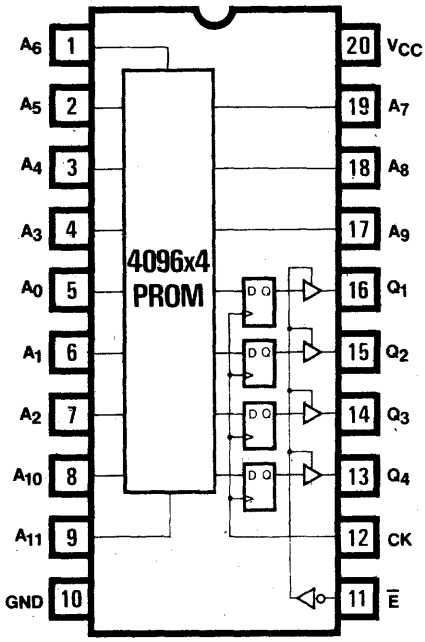
53/63RA441



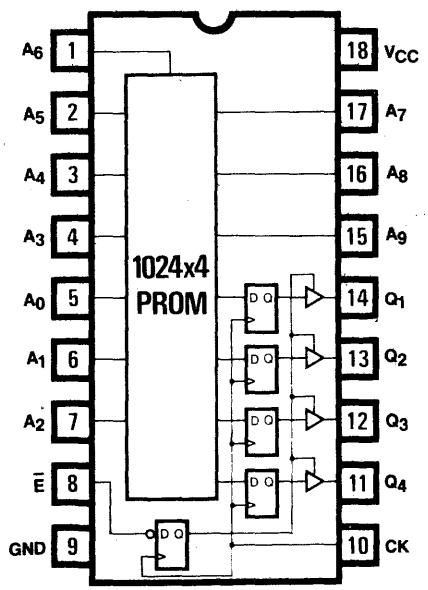
53/63RA841



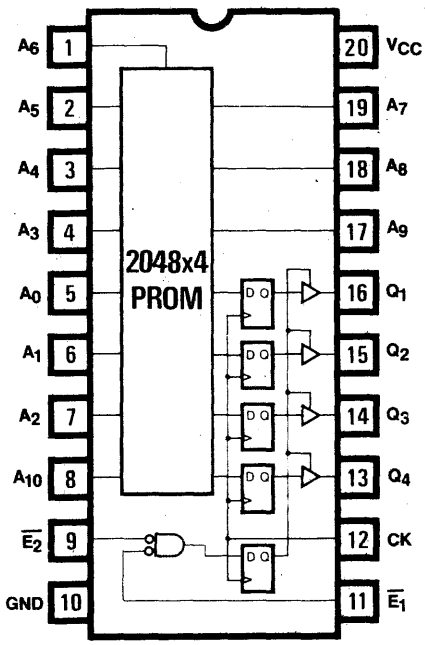
53/63RA1641



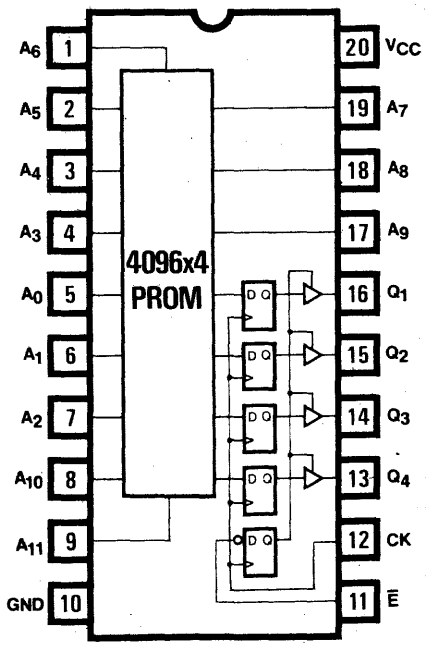
53/63 RS441



53/63RS841



53/63RS1641



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Absolute Maximum Ratings

	Operating	Program
Supply voltage V_{CC}	−.5V to 7V	12V
Input voltage	−1.5V to 5.5V	12V
Off-state output voltage	−1.5V to 5.5V	12V
Storage temperature	−65°C to 150°C	

Recommended Operating Conditions

SYMBOL	PARAMETER	MILITARY			COMMERCIAL			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5.0	5.5	4.75	5.00	5.25	V
I_{OH}	High-level output current			−2.0	2.4		−6.5	mA
I_{OL}	Low-level output current			16			24	mA
T_A	Operating free air temperature	−55		125	0		75	°C

Electrical Characteristics

Over Recommended Operating Free Air Tempeature Range

SYMBOL	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IH}	High-level input voltage			2.0		V_{CC}	V
V_{IL}	Low-level input voltage			0		0.8	V
V_{IC}	Input clamp voltage	V_{CC} = MIN, I_I = −18mA				−1.2	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2V, V_{IL} = 0.8V, I_{OH} = MAX		2.4			V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2V, V_{IL} = 0.8V, I_{OL} = MAX				0.5	V
I_{OZH}	Off-state output current high-level voltage applied	V_{CC} = MAX, V_{IH} = 2V, V_O = 2.4V				100	μA
I_{OZL}	Off-state output current low-level voltage applied	V_{CC} = MAX, V_{IH} = 2V, V_O = 0.4V				−100	μA
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5V				1.0	mA
I_{IH}	High-level input current	V_{CC} = MAX. V_I = 2.4V				25	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.4V				−250	μA
I_{OS}	Short-circuit output current	V_{CC} = MAX		−30		−100	mA
C_I	Input capacitance	V_{CC} = 5.0V, f = 1 MHz	V_I = 2.0V		4	10	pF
C_O	Output capacitance	T_A = 25°C	V_O = 2.0V		6	12	pF
I_{CC}	Supply current 441,	V_{CC} = MAX	All inputs GND All outputs open		125	180	mA
	Supply current 841, 1641	V_{CC} = MAX	All inputs GND All outputs open		130		mA

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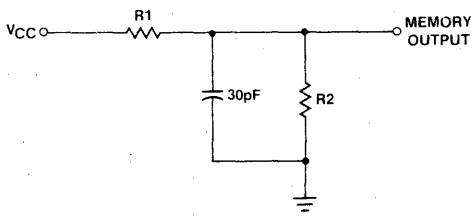
Switching Characteristics

Min/Max = Over Recommended Ranges of T_A and V_{CC}
Typ = 5.0V V_{CC}, 25°C T_A

SYMBOL	PARAMETER	DEVICE TYPE	MILITARY			COMMERCIAL		
			MIN	TYP	MAX	MIN	TYP	MAX
t_{pd}	Clock to output	(All)		18	30		18	25
t_{su}	Address set-up	RA441	45	30		40	30	
		RA841		35			35	
		RA1641		45			45	
		RS441	45	30		40	30	
		RS841		35			35	
		RS1641		45			45	
t_h	Address hold	(All)	0	−5		0	−5	
t_{pzx}	$\overline{E}$ to output enable	(All "RA")		15	30		15	25
t_{pxz}	$\overline{E}$ to output disable	(All "RA")		15	30		15	25
t_{pzx}	CK to output enable	(All "RS")		25	40		25	35
t_{pxz}	CK to output disable	(All "RS")		25	40		25	35
t_{su}	Enable set-up	(All "RS")	20	10		15	10	
t_h	Enable hold	(All "RS")	0	−5		0	−5	
t_w	Pulse width	(All)	20	12		20	12	
MAX	Maximum Clock frequency	RS/RA 441	20	24		25	33	
		RS/RA 841		29			33	
		RS/RA1641		25			25	

(See "Definition of Terms and Waveforms")

Standard Test Load



Input Pulse Amplitude 3.0V
Input Rise and Fall Times 5ns from 1.0V to 2.0V
Measurements Made at 1.5V
Commercial R1 = 200Ω, R2 = 390Ω
Military R1 = 300Ω, R2 = 600Ω

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Standard Performance Schottky Generic ROM Family

52/62XX-1, 52/62XX-2

Features/Benefits

- Largest generic ROM family available
- PNP inputs for low input current
- Compatible pin configurations for upward expansions
- 4-bit-wide and 8-bit-wide for byte oriented applications
- Bit density from 256 to 16384
- Interchangeable PROM compatibility
- High speed Schottky technology

Applications

- High speed for microprogrammed applications
- Microprocessor program store
- Look up table
- Character generator
- Random logic
- Code converter

Description

The 52/6200-series generic ROM family offers the widest selection of sizes and organizations available in the industry. The 4-bit-wide ROMs range from 256x4 to 1024x4 and feature upward/downward pinout compatibility in the space saving 16 and 18 pin packages. The 8-bit-wide ROMs range from 32x8 to 2048x8 in a wide selection of package sizes. Additional 5-bit, 9-bit and 10-bit-wide output configurations are available for your custom logic or character generator applications.

The family features low input current PNP inputs, full Schottky clamping and three-state and open collector outputs.

The 62 series is specified for operation over the commercial temperature and voltage range. The 52 series is specified for the military ranges. 52XX-2 and 62XX-2 devices offer enhanced speed specifications.

Generic ROM Selection Guide

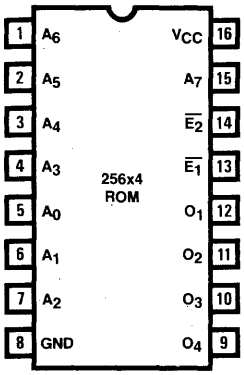
MEMORY			PACKAGE		DEVICE TYPE		INTERCHANGEABLE PROM	
SIZE	ORGANIZATION		PINS	TYPE	0°C to +75°C	−55°C to +125°C	0°C to +75°C	−55°C to +125°C
1024	256x4	OC	16	J, N, F	6200-1	5200-1	6300-1	5300-1
		TS			6201-1	5201-1	6301-1	5301-1
2048	512x4	OC	16	J, N, F	6205-1	5205-1	6305-1	5305-1
		TS			6206-1	5206-1	6306-1	5306-1
4096	1024x4	OC	18	J, N, F	6250-1	5250-1	6350-1	5350-1
		TS			6251-1	5251-1	6351-1	5351-1
		OC			6252-1	5252-1	6352-1	5352-1
		TS			6253-1	5253-1	6353-1	5353-1
1280	256x5	OC	16	J, N, F	6210-1	5210-1	—	—
2560	512x5	OC	18	J, N	6225-1	5225-1	—	—
256	32x8	OC	16	J, N, F	6230-1	5230-1	6330-1	5330-1
		TS			6231-1	5231-1	6331-1	5331-1
2048	256x8	OC	20	J, N	6208-1	5208-1	6308-1	5308-1
		TS			6209-1	5209-1	6309-1	5309-1
2048	256x8	OC	24	J, N, F	6235-1	5235-1	6335-1	5335-1
		TS			6236-1	5236-1	6336-1	5336-1
4096	512x8	OC	20	J, N	6248-1	5248-1	6348-1	5348-1
		TS			6249-1	5249-1	6349-1	5349-1
4096	512x8	OC	24	J, N, F	6240-1	5240-1	6340-1	5340-1
		TS			6241-1	5241-1	6341-1	5341-1

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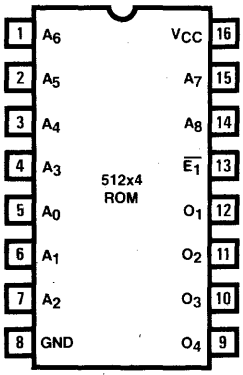
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Pin Configurations

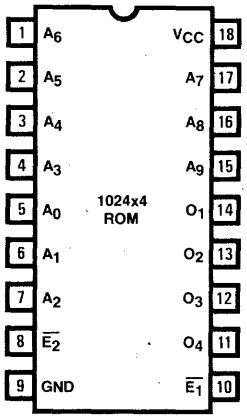
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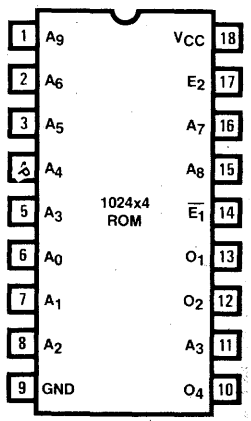
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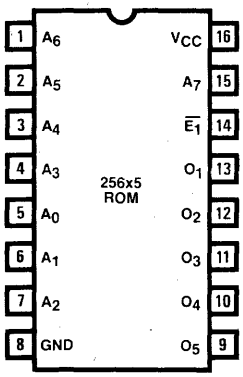
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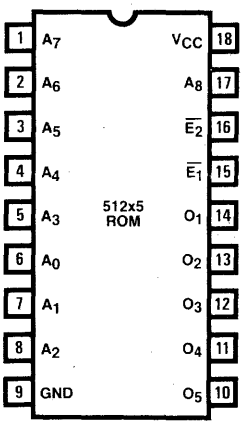
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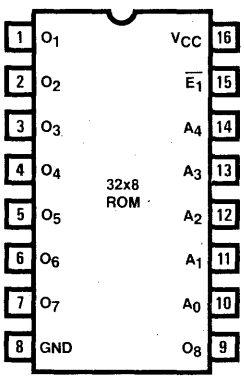
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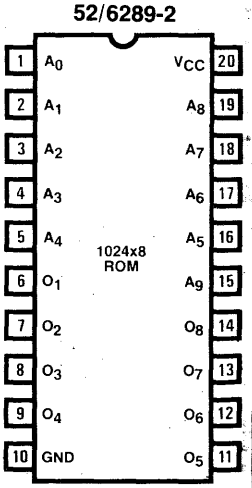
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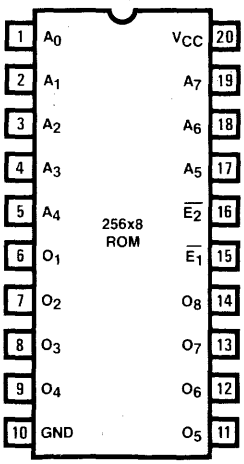
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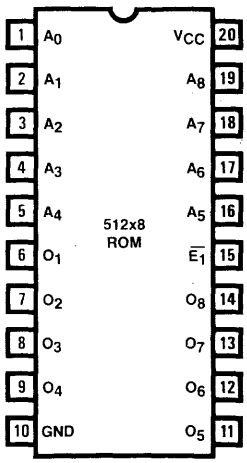
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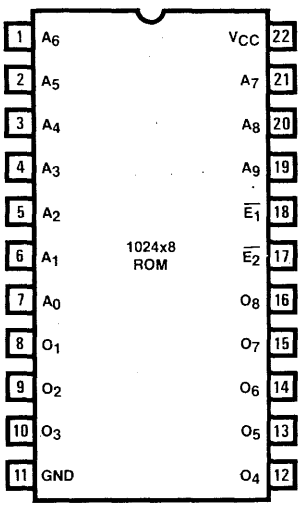
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52/6248-1
52/6249-1



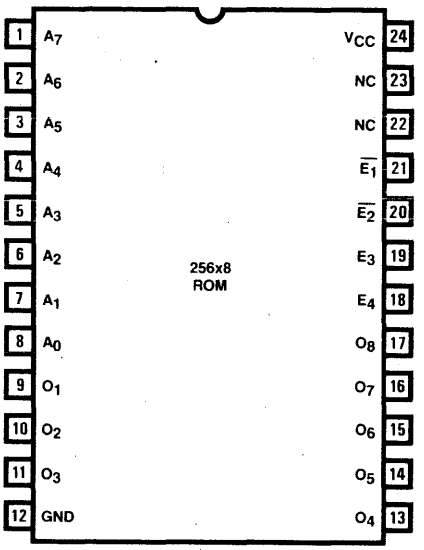
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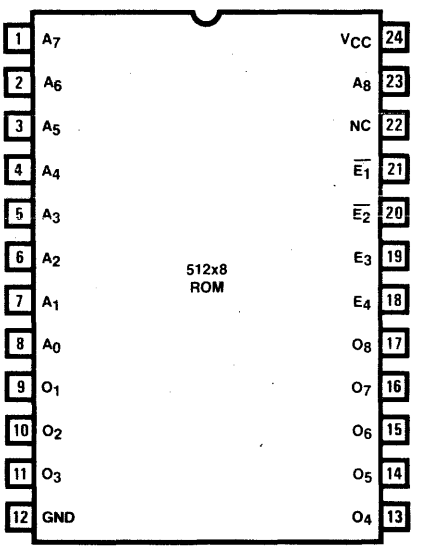
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Pin Configurations

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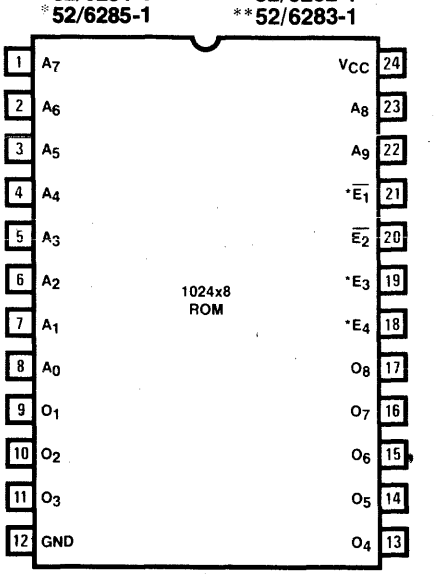


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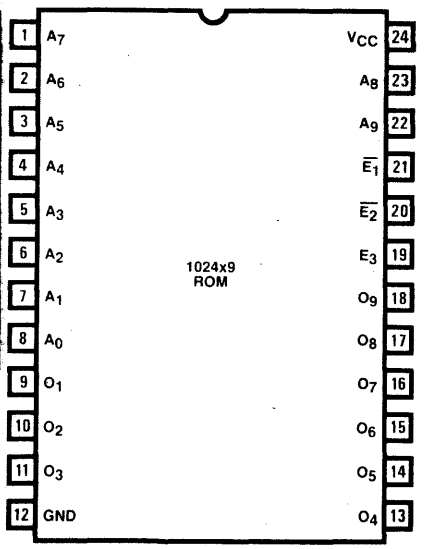
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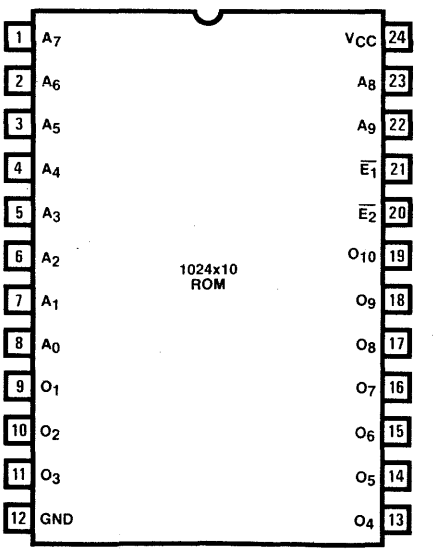


*NO CONNECTION
**"OR" ENABLE

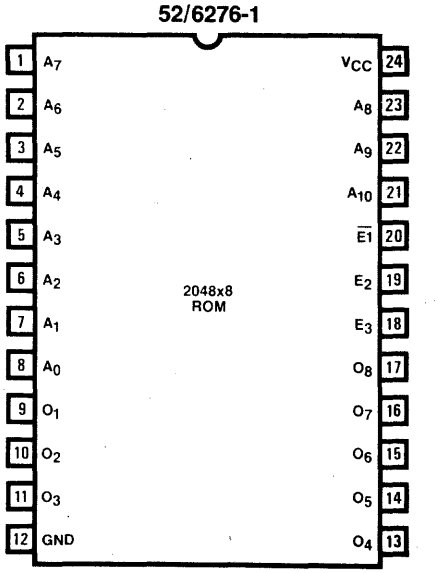
52/6260-1
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52/6255-1
52/6256-1



52/6275-1
52/6276-1



NOTE:
Pin assignments for ceramic (J package), plastic (N package) and flat pack (F package) are the same.

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Generic ROM Selection Guide

MEMORY			PACKAGE		DEVICE TYPE		INTERCHANGEABLE PROM	
SIZE	ORGANIZATION		PINS	TYPE	0°C to +75°C	−55°C to +125°C	0°C to +75°C	−55°C to +125°C
8192	1024x8	OC	24	J, N, F	6280-1	5280-1	6380-1	5380-1
		TS			6281-1	5281-1	6381-1	5381-1
		OC			6280-2	5280-2	—	—
		TS			6281-2	5281-2	—	—
		OC			6282-1	5282-1	—	—
		TS			6283-1	5283-1	—	—
		OC			6284-1	5284-1	—	5384-1
		TS			6285-1	5285-1	—	5385-1
		OC	22	J, N	6286-1	5286-1	—	—
		TS			6287-1	5287-1	—	—
		OC			6286-2	5286-2	—	—
		TS			6287-2	5287-2	—	—
		Active Pullup	20	J, N	6289-1	5289-1	—	—
					6289-2	5289-2	—	—
16384	2048x8	OC	24	J, N, F	6275-1	5275-1	635-1680	535-1680
		TS			6276-1	5276-1	635-1681	535-1681
9216	1024x9	OC	24	J, N, F	6260-1	5260-1	—	—
		TS			6261-1	5261-1	—	—
10240	1024x10	OC	24	J, N, F	6255-1	5255-1	—	—
		TS			6256-1	5256-1	—	—

Absolute Maximum Ratings

Supply voltage V_{CC} ..... −0.5V to +7.0V
Input voltage ..... −1.5V to +5.5V
Input current ..... −20 mA to +5 mA
Output current ..... −100 mA to +100 mA
Storage temperature range ..... −65°C to +150°C

Recommended Operating Conditions

SYMBOL	PARAMETER		Military MIN	Military NOM	Military MAX	Commercial MIN	Commercial NOM	Commercial MAX	UNIT
V_{CC}	Supply voltage		4.5	5.0	5.5	4.75	5.00	5.25	V
I_{OH}	High-level output current				−1.0			−2.0	mA
I_{OL}	Low-level operating current	'05, '06, '08, '09, '48, '49, '50, '51, '52, '53			12			16	mA
		'00, '01, '10, '25			10			15	
		'30, '31			8			12	
		'35, '36, '40, '41, '80, '81, '82, '83, '84, '85, '86, '87, '89, '75, '76			8			10	
		'55, '56, '60, '61			6			6	
T_A	Operating free air temperature		−55	25	125	0	25	75	°C

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Electrical Characteristics Over Recommended Operating Free Air Temperature Range

SYMBOL	PARAMETER		CONDITIONS		MIN	TYP	MAX	UNIT
V_{IH}	High level input voltage				2.0		V_{CC}	V
V_{IL}	Low level input voltage				0		0.8	V
V_{IC}	Input clamp voltage		V_{CC} = MIN, I_I = −18mA			−1.0	−1.5	V
V_{OL}	Low level output voltage		V_{CC} = MIN, I_{OL} = MAX				0.50	V
I_I	Maximum input current		V_{CC} = MAX, V_I = 5.5 V				1.0	mA
I_{IH}	High level input current		V_{CC} = MAX, V_I = 2.4V				40	μA
I_{IL}	Low level input current		V_{CC} = MAX, V_I = 0.45V				−250	μA
C_I	Input capacitance		V_{CC} = 5.0V, T_A = 25°C, f = 1 MHz	V_I = 2.0V		7		pF
C_O	Output capacitance		V_{CC} = 5.0V, T_A = 25°C, f = 1 MHz	V_O = 2.0V		8		pF
I_{CC}	Supply current	'00, '01, '30, '31	V_{CC} = MAX, All inputs grounded, All outputs open			92	125	mA
		'05, '06				96	130	
		'08, '09, '48, '49				115	155	
		'55, '60				122	165	
		'10, '25, '35, '40, '41, '80, '82, '84, '86, '89				126	170	
		'36, '50, '51, '52, '53, '56, '61				130	175	
		'81, '83, '85, '87				133	180	
		'75, '76				141	190	

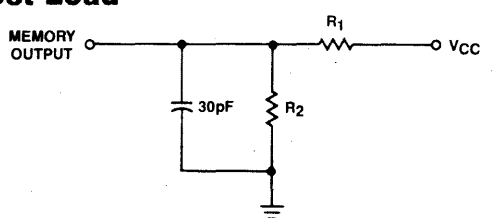
OPEN COLLECTOR OUTPUT CURRENT

I_{CEX}	Output leakage current	V_{CC} = MAX, V_O = 2.4V		100	μA

THREE STATE OUTPUT ONLY

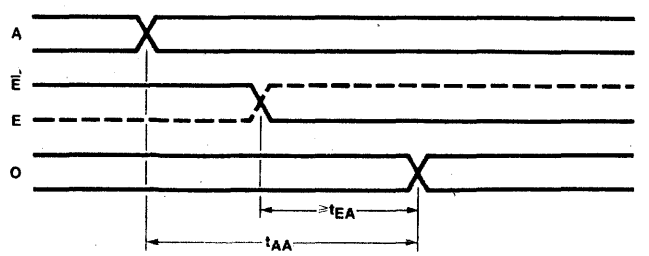
V_{OH}	High level output voltage		V_{CC} = MIN, I_{OH} = MAX	2.4		V
I_{HZ}	High level off State output current	8k, 9k, 10k	V_{CC} = MAX, V_O = 2.4V		50	μA
		All others			100	
I_{LZ}	Low level off State output current	8k, 9k, 10k	V_{CC} = MAX, V_O = 0.5V		−50	μA
		All others			−100	
I_{OS}	Output short circuit current		V_{CC} = 5.0V, V_O = 0V	−20	−90	mA

Standard Test Load

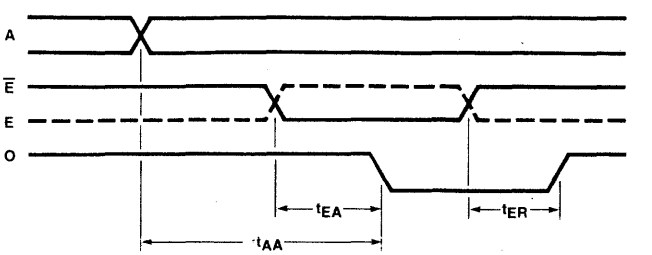


Input Pulse Amplitude 3.0V
Input Rise and Fall Times 5ns from 1.0V to 2.0V
Measurements Made at 1.5V

Definition of Waveforms



ADDRESS ACCESS TIME



ENABLE ACCESS TIME AND RECOVERY TIME

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Switching Characteristics

Over Recommended Ranges of T_A and V_{CC} (Unless Otherwise Noted)

DEVICE TYPE	CONDITIONS (See standard test load)		t_{AA}(ns) ADDRESS ACCESS TIME	t_{EA}(ns) ENABLE ACCESS TIME	t_{ER}(ns) ENABLE RECOVERY TIME
	$R_1\Omega$	$R_2\Omega$	MAX	MAX	MAX
6200-1, 6201-1	300	600	45	35	35
5200-1, 5201-1	450	900	60	35	35
6205-1, 6206-1	280	560	60	30	30
5205-1, 5206-1	375	750	75	40	40
6210-1	300	600	100	70	45
5210-1	450	900	175	90	50
6225-1	300	600	100	70	45
5225-1	450	900	175	90	50
6230-1, 6231-1	375	750	50	30	25
5230-1, 5231-1	560	1120	60	30	25
6208-1, 6209-1	280	560	70	30	30
5208-1, 5209-1	375	750	80	40	40
6235-1, 6236-1	450	900	100	70	45
5235-1, 5236-1	560	1120	175	90	50
6248-1, 6249-1	280	560	70	30	30
5248-1, 5249-1	375	750	80	40	40
6240-1, 6241-1	450	900	100	70	45
5240-1, 5241-1	560	1120	175	90	50
6250-1, 6251-1	280	560	60	30	30
5250-1, 5251-1	375	750	75	40	40
6252-1, 6253-1	280	560	60	30	30
5252-1, 5253-1	375	750	75	40	40
6255-1, 6256-1	750	1500	100	70	40
5255-1, 5256-1	750	1500	150	80	45
6260-1, 6261-1	750	1500	100	70	40
5260-1, 5261-1	750	1500	150	80	45
6275-1, 6276-1	450	900	110	40	40
5275-1, 5276-1	560	1120	120	50	50
6280-1, 6281-1	450	900	100	70	45
5280-1, 5281-1	560	1120	175	90	50
6280-2, 6281-2	450	900	55	30	30
5280-2, 5281-2	560	1120	75	35	35
6282-1, 6283-1	450	900	100	70	45
5282-1, 5283-1	560	1120	175	90	50
6284-1, 6285-1	450	900	100	70	45
5284-1, 5285-1	560	1120	175	90	50
6286-1, 6287-1	450	900	100	70	45
5286-1, 5287-1	560	1120	175	90	50
6286-2, 6287-2	450	900	55	30	30
5286-2, 5287-2	560	1120	75	35	35
6289-1	750	1500	100	70	45
5289-1	750	1500	175	90	50
6289-2	750	1500	55	30	30
5289-2	750	1500	75	35	35

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First-In First-Out (FIFO) 64x4 Serial Memory

57401/67401

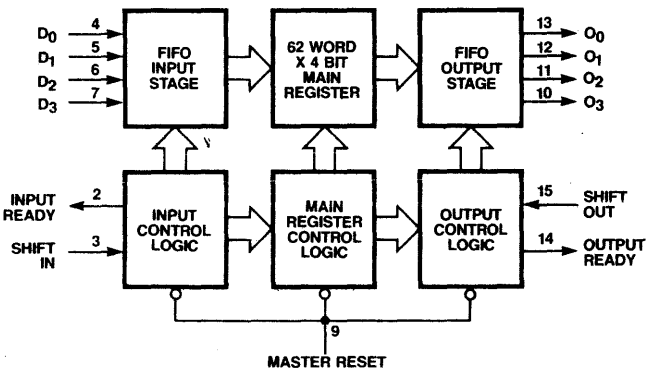
Features/Benefits

- 12 MHz shift in, shift out typical rates
- Advanced Schottky bipolar processing
- TTL inputs and outputs
- Readily expandable in word and bit dimensions
- Asynchronous or synchronous operation
- Pin compatible with Fairchild's F3341 MOS FIFO and ten times as fast

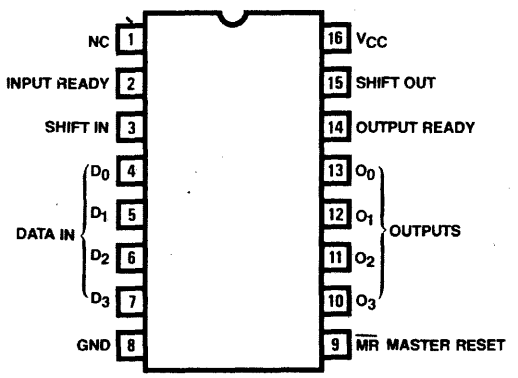
Description

The 57401 is an expandable "fall-through" high speed First-In First-Out (FIFO) memory organized 64 words by 4-bit. A 12 MHz data rate allows usage in high speed tape or disc controllers and communication buffer applications. The 67401 is specified over the commercial operating range 0 –75°C and the 57401 is specified over the military operating of –55°C to +125°C.

Block Diagram



Pin Configuration

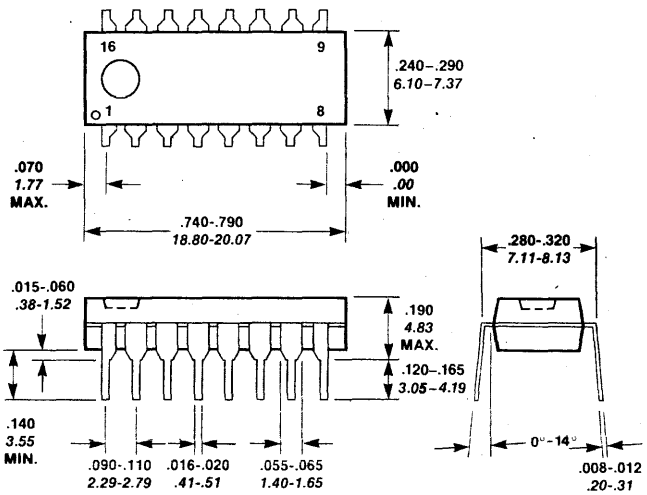


Selection Guide

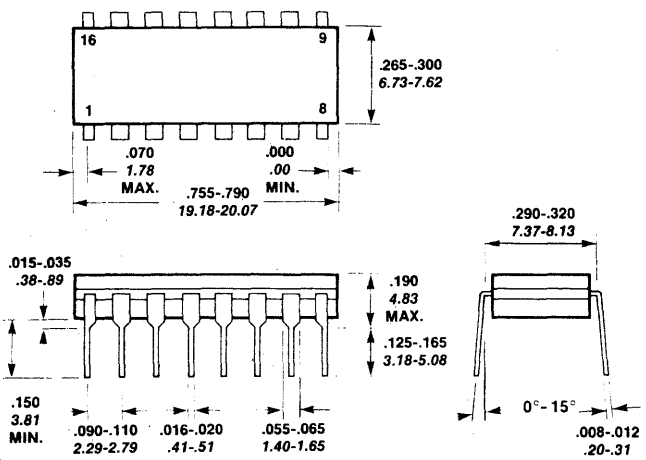
PART NUMBER	PACKAGE	TEMPERATURE RANGE
57401	J16	Military
67401	J/N16	Commercial

Package Drawing

N16 Plastic DIP



J16 Ceramic DIP



UNLESS OTHERWISE SPECIFIED:
ALL DIMENSIONS MIN.-MAX. IN INCHES.
ALL DIMENSIONS MIN.-MAX IN MILLIMETERS.

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Absolute Maximum Ratings

	Operating
Supply voltage V_{CC}	7V/12V
Input voltage	5.5V/12V
Off-state output voltage	5.5V/12V
Storage temperature range	−65°C to 150°C

Recommended Operating Conditions

SYMBOL	PARAMETER	MILITARY			COMMERCIAL			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5.0	5.5	4.75	5.00	5.25	V
I_{OH}	High-level output current			0.9			0.9	mA
I_{OL}	Low-level output current			8			8	mA
T_A	Operating free air temperature	−55		125	0		75	°C

Electrical Characteristics

Over Recommended Operating Free Air Temperature

SYMBOL	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_{IC}	Input clamp voltage	V_{CC} = MIN, I_I = −18mA				−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2V V_{IL} = 0.8V, I_{OH} = MAX		2.4			V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2V V_{IL} = 0.8V, I_{OL} = MAX				0.5	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5V				1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.4V				50	μA
I_{IL1}	Low-level input current inputs D_0-D_3, MR	V_{CC} = MAX, V_F = 0.45V				−0.8	mA
I_{IL2}	Low-level input current inputs S1, S0	V_{CC} = MAX, V_F = 0.45V				−1.6	mA
I_{OS}	Short-circuit output current	V_{CC} = 6V, V_O = .5V		−20		−90	mA
C_I	Input capacitance	V_{CC} = 5.0V	V_I = 2.0V		7		pF
C_O	Output capacitance	f = 1 MHz, T_A = 25°C	V_O = 2.0V		8		
I_{CC}	Supply current	V_{CC} = MAX[1]			111	150	mA

NOTE: 1. I_{CC} measured with worst case sequence; FIFO reset, one shift-in cycle with data inputs held low, measure I_{CC} with all inputs held low.

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Switching Characteristics

See Figure 1

SYMBOL	PARAMETER	FIGURE	57401—MILITARY 5 ±10%, −55°C to +125°C			67401—COMMERCIAL 5 ±5%, 0°C to 70°C		
			MIN	MAX	UNIT	MIN	MAX	UNIT
f_{IN}	Shift in Clock Rate	1	7		MHz	10		MHz
t_{SIH}	Shift in High Time	1	45		ns	35		ns
t_{SIL}	Shift in Low Time	1	45		ns	35		ns
t_{IRL}	Input Ready ON Delay	1		60	ns		45	ns
t_{IRH}	Input Ready OFF Delay	1		60	ns		45	ns
t_{IDS}	Input Data Set Up	1	10		ns	5		ns
t_{IDH}	Input Data Hold Time	1	55		ns	45		ns
f_{OUT}	Shift Out Clock Rate	2	7		MHz	10		MHz
t_{SOH}	Shift Out High Time	2	45		ns	35		ns
t_{SOL}	Shift Out Low Time	2	45		ns	35		ns
t_{ORL}	Output Ready ON Delay	2		65	ns		55	ns
t_{ORH}	Output Ready OFF Delay	2		65	ns		55	ns
t_{ODH}	Output Data Hold Time	2	10		ns	10		ns
t_{ODS}	Output Data Delay	2		65	ns		55	ns
t_{PT}	Data Throughput Time	Note 1		4.0	μs		3.0	μs
t_{MRW}	Master Reset Pulse	Note 2	30		ns	25		ns
t_{MRORL}	Master Reset to OR Low	5		65	ns		55	ns
t_{MRIRH}	Master Reset to IR High	5		45	ns		35	ns
t_{MRS}	Master Reset to SI	5	45		ns	35		ns
t_{IPH}	Input Ready Pulse High	4	45		ns	35		ns
t_{IPL}	Input Ready Pulse Low	6	45		ns	35		ns
t_{OPH}	Output Ready Pulse High	3	45		ns	35		ns
t_{OPL}	Output Ready Pulse Low	7	45		ns	35		ns

NOTES: 1. This parameter defines total time from the time data is present at D_0-D_3 to the time it is available at O_0-O_3 with FIFO initially empty and total time from the time data is extracted from O_0-O_3 to IR High with FIFO initially full.
2. Master Reset clears the 57401/67401 to the all cells empty state.

MMI

MEMORY

Functional Description

Data Input

Data is entered into the FIFO on D_0-D_3 inputs. To enter data the Input Ready (IR) output should be HIGH, indicating that the first location is ready to accept data. Data then present at the four data inputs is entered into the first location when the Shift In (SI) is brought HIGH. A SI HIGH signal causes the RI to go LOW. Data remains at the first location until SI is brought LOW. When SI is brought LOW and the FIFO is not full, IR will go HIGH, indicating that more room is available. Simultaneously, data will propagate to the second location and continue shifting until it reaches the output stage or a full location. If the memory is full, IR will remain LOW.

Data Transfer

Once data is entered into the second cell, the transfer of any full cell to the adjacent (downstream) empty cell is automatic, activated by an on-chip control. Thus data will stack up at the end of the device while empty locations will "bubble" to the front. t_{PT} defines the time required for the first data to travel from input to the output of a previously empty device.

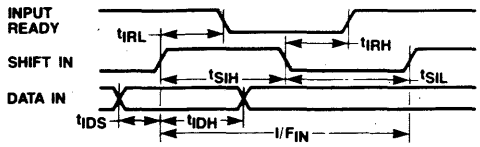
Data Output

Data is read from the O_0-O_3 outputs. When data is shifted to the output stage, Output Ready (OR) goes HIGH, indicating the presence of valid data. When the OR is HIGH, data may be shifted out by bringing the Shift Out (SO) HIGH. A HIGH signal at SO causes the OR to go LOW. Valid data is maintained while the SO is HIGH. When SO is brought LOW the upstream data, provided that stage has valid data, is shifted to the output stage. When new valid data is shifted to the output stage, OR goes HIGH. If the memory is emptied, OR stays LOW.

Input Ready and Output Ready may also be used as status signals indicating that the FIFO is completely full (Input Ready stays LOW for at least t_{PT}) or completely empty (Output Ready stays LOW for at least t_{PT}).

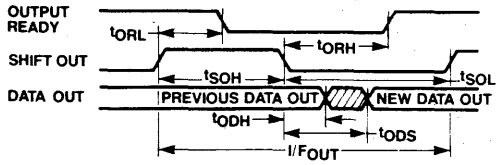
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Timing Diagrams



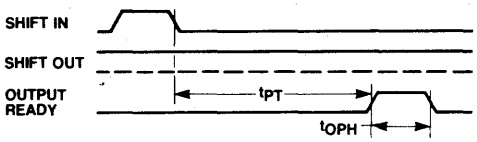
1. Input data must remain stable during t_{IDS} and t_{IDH}.
2. Input Ready HIGH indicates that space is available and a Shift In pulse may be applied. Input Ready LOW indicates that the FIFO is full or that a previous Shift In operation is not complete. Shift In pulses applied while Input Ready is LOW will be ignored.
3. The rise of Input Ready indicates that the data at the D0-D3 inputs has been accepted and that the input stage is empty.

Figure 1. FIFO Input Timing



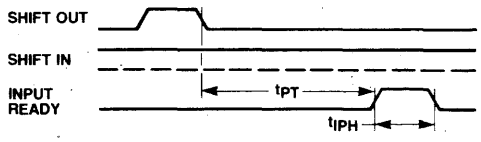
1. Output data will be stable at the rise of Output Ready.
2. Output Ready HIGH indicates that data is available and a Shift Out pulse may be applied. Output Ready LOW indicates that the FIFO is empty or that a previous Shift Out operation is still in progress. Shift Out pulses applied while Shift Out Ready is LOW will be ignored.
3. The rise of Output Ready indicates that new data has been loaded into the output stage.

Figure 2. FIFO Output Timing



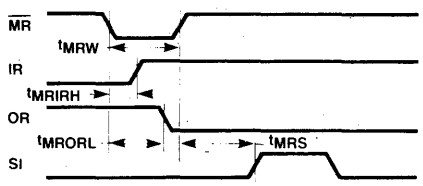
1. FIFO initially empty.
2. Shift Out held high (as shown).

Figure 3. t_{OPH} Specification



1. FIFO initially full.
2. Shift In held high (as shown).

Figure 4. t_{IPH} Specification



1. FIFO initially full

Figure 5. FIFO Master Reset Timing

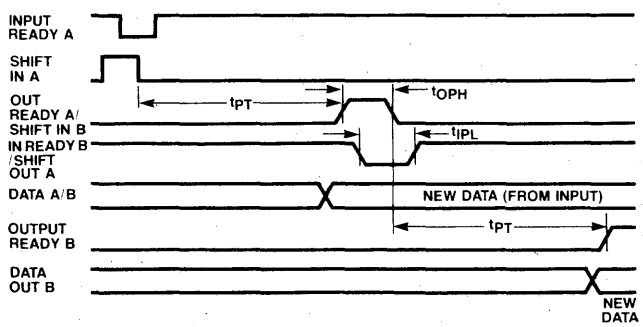
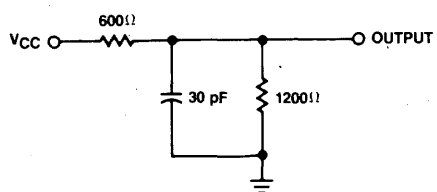


Figure 6. FIFO/FIFO Communication: Empty/Input Timing

Standard Test Circuit



Input Pulse Amplitude = 3.0V
Input Rise and Fall Time = 5.0 ns from 1.0V to 2.0V
Measurements made at 1.50V

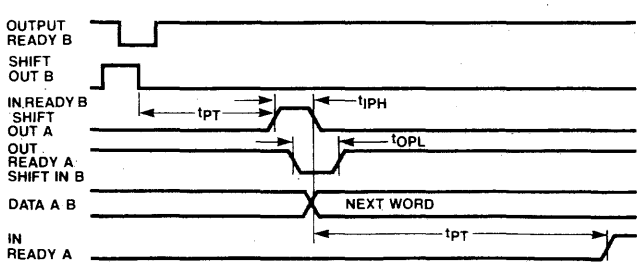


Figure 7. FIFO/FIFO Communication: Full/Output Timing

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First-In First-Out (FIFOs) 64x4, 64x5 Serial Memories

57401A/67401A, 57402A/67402A

Features/Benefits

- 15 MHz shift in, shift out typical rates
- Advanced Schottky bipolar processing
- TTL inputs and outputs
- Readily expandable in word and bit dimensions
- Asynchronous or synchronous operation
- 64x4 FIFO pin compatible with Fairchild's F3341 MOS FIFO and ten times as fast
- 4 & 5-bit organizations for 9 bit expansion
- Master reset clears outputs to zero state

Description

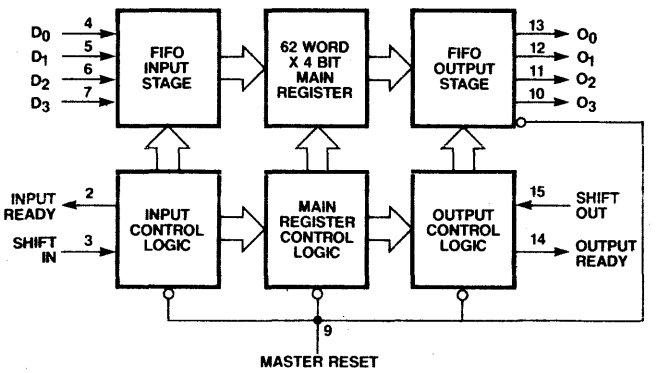
The 57401A/402A are expandable "fall-through" high speed First-In First-Out (FIFO) memories. The 57401A is organized 64 words by 4-bits. The 57402A is organized 64 words by 5-bits. A 15 MHz data rate allows usage in high speed tape or disc controllers and communication buffer applications. The 67401A/67402A is specified over the commercial operating range 0−75°C and the 57401A/57402A is specified over the military operating range of −55°C to +125°C.

Selection Guide

PART NUMBER	PACKAGE	TEMPERATURE RANGE
57401A	J16	Military
67401A	J/N16	Commercial
57402A	J18	Military
67402A	J/N18	Commercial

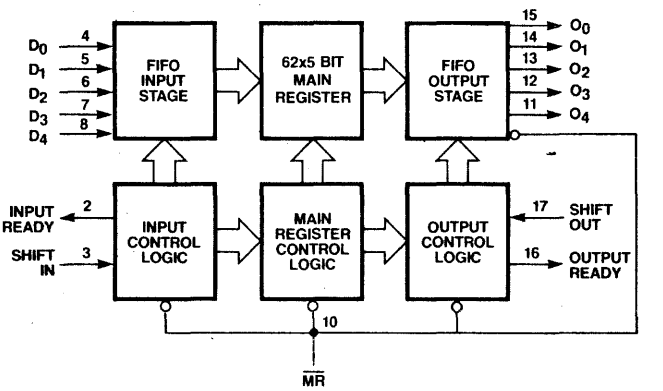
Block Diagram

57401A/67401A 64x4



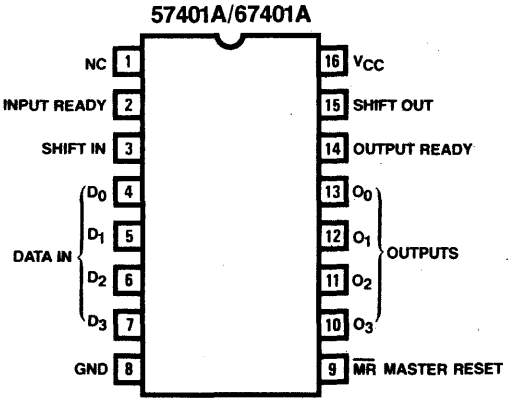
Block Diagram

57402A/67402A 64x5

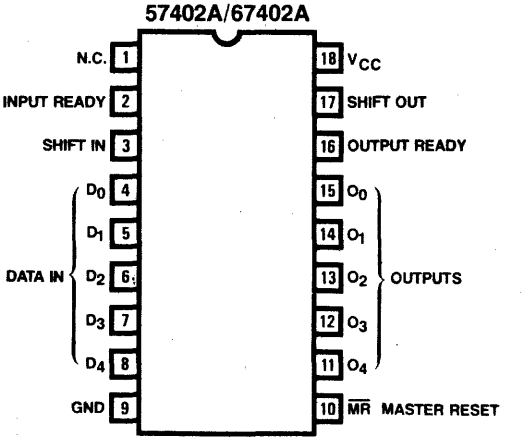


Pin Configuration

57401A/67401A



57402A/67402A



MMI

MEMORY

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Absolute Maximum Ratings

	Operating
Supply voltage V_{CC}	7V
Input voltage	5.5V
Off-state output voltage	5.5V
Storage temperature range	−65°C to 150°C

Recommended Operating Conditions

SYMBOL	PARAMETER	MILITARY			COMMERCIAL			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5.0	5.5	4.75	5.00	5.25	V
I_{OH}	High-level output current			0.9			0.9	mA
I_{OL}	Low-level output current			8			8	mA
T_A	Operating free air temperature	−55		125	0		75	°C

Electrical Characteristics

Over Recommended Operating Free Air Temperature

SYMBOL	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_{IC}	Input clamp voltage	V_{CC} = MIN, I_I = −18mA				−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2V V_{IL} = 0.8V, I_{OH} = MAX		2.4			V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2V V_{IL} = 0.8V, I_{OL} = MAX				0.5	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5V				1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.4V				50	μA
I_{IL1}	Low-level input current inputs $D_0 - D_3$, MR	V_{CC} = MAX, V_F = 0.45V				−0.8	mA
I_{IL2}	Low-level input current inputs S1, S0	V_{CC} = MAX, V_F = 0.45V				−1.6	mA
I_{OS}	Short-circuit output current	V_{CC} = MAX, V_O = .5V		−20		−90	mA
C_I	Input capacitance	V_{CC} = 5.0V f = 1 MHz, T_A = 25°C	V_I = 2.0V		7		pF
C_O	Output capacitance		V_O = 2.0V		8		pF
I_{CC}	Supply current 57401A/67401A	V_{CC} = MAX[1]			111	150	mA
I_{CC}	Supply current 57402A/67402A	V_{CC} = MAX[1]			119	160	mA

NOTE: 1. I_{CC} measured with worst case sequence; FIFO reset, one shift-in cycle with data inputs held low, measure I_{CC} with all inputs held low.

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Switching Characteristics

See Figure 1

SYMBOL	PARAMETER	FIGURE	57401A/57402A—MILITARY 5 ±10%, −55°C to +125°C MIN	TYP[3]	MAX	UNIT	67401A/67402A—COMM 5 ±5%, 0°C to 70°C MIN	TYP[3]	MAX	UNIT
f_{IN}	Shift in Clock Rate	1		15		MHz		15		MHz
t_{SIH}	Shift in High Time	1		18		ns		18		ns
t_{SIL}	Shift in Low Time	1		18		ns		18		ns
t_{IRL}	Input Ready ON Delay	1		30		ns		30		ns
t_{IRH}	Input Ready OFF Delay	1		30		ns		30		ns
t_{IDS}	Input Data Set Up	1		5		ns		5		ns
t_{IDH}	Input Data Hold Time	1		12		ns		12		ns
f_{OUT}	Shift Out Clock Rate	2		15		MHz		15		MHz
t_{SOH}	Shift Out High Time	2		18		ns		18		ns
t_{SOL}	Shift Out Low Time	2		18		ns		18		ns
t_{ORL}	Output Ready ON Delay	2		24		ns		24		ns
t_{ORH}	Output Ready OFF Delay	2		24		ns		24		ns
t_{ODH}	Output Data Hold Time	2		25		ns		25		ns
t_{ODS}	Output Data Delay	2		35		ns		35		ns
t_{PT}	Data Throughput Time	Note 1		2.0		μs		2.0		μs
t_{MRW}	Master Reset Pulse	Note 2		15		ns		15		ns
t_{MRORL}	Master Reset to OR Low	5		30		ns		30		ns
t_{MRIRH}	Master Reset to IR High	5		30		ns		30		ns
t_{MRS}	Master Reset to SI	5		20		ns		20		ns
t_{IPH}	Input Ready Pulse High	4		35		ns		35		ns
t_{IPL}	Input Ready Pulse Low	6		35		ns		35		ns
t_{OPH}	Output Ready Pulse High	3		35		ns		35		ns
t_{OPL}	Output Ready Pulse Low	7		35		ns		35		ns

NOTES: 1. This parameter defines total time from the time data is present at Dn to the time it is available at On with FIFO initially empty and total time from the time data is extracted from Dn to IR High with FIFO initially full.
2. Master Reset clears the FIFO to the all cells empty state and resets outputs On to zero state.
3. Typical values @ 5.0V V_{CC} and 25°C.

Functional Description

Data Input

Data is entered into the FIFO on Dn inputs. To enter data the Input Ready (IR) output should be HIGH, indicating that the first location is ready to accept data. Data then present at the data inputs is entered into the first location when the Shift In (SI) is brought HIGH. A SI HIGH signal causes the RI to go LOW. Data remains at the first location until SI is brought LOW. When SI is brought LOW and the FIFO is not full, IR will go HIGH, indicating that more room is available. Simultaneously, data will propagate to the second location and continue shifting until it reaches the output stage or a full location. If the memory is full, it will remain LOW.

Data Transfer

Once data is entered into the second cell, the transfer of any full cell to the adjacent (downstream) empty cell is automatic, activated by an on-chip control. Thus data will stack up at the end of the device while empty locations will "bubble" to the front. t_{PT} defines the time required for the first data to travel from input to the output of a previously empty device.

Data Output

Data is read from the On outputs. When data is shifted to the output stage, Output Ready (OR) goes HIGH, indicating the presence of valid data. When the OR is HIGH, data may be shifted out by bringing the Shift Out (SO) HIGH. A HIGH signal at SO causes the OR to go LOW. Valid data is maintained while the SO is HIGH. When SO is brought LOW the upstream data, provided that stage has valid data, is shifted to the output stage. When new valid data is shifted to the output stage, OR goes HIGH. If the memory is emptied, OR stays LOW.

Input Ready and Output Ready may also be used as status signals indicating that the FIFO is completely full (Input Ready stays LOW for at least t_{PT}) or completely empty (Output Ready stays LOW for at least t_{PT}).

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Programmable Array Logic Family

PAL™ Series 20 Data Sheet

Patent Allowed

Features/Benefits

- **Programmable replacement for conventional TTL logic.**
- **Reduces IC inventories substantially and simplifies their control.**
- **Reduces chip count by 4 to 1.**
- **Expedites and simplifies prototyping and board layout.**
- **Saves space with 20-pin Skinny DIP packages.**
- **High speed: 25ns typical propagation delay.**
- **Programmed on standard PROM programmers.**
- **Programmable three-state outputs.**
- **Special feature reduces possibility of copying by competitors.**

Description

The PAL family utilizes an advanced Schottky TTL process and the Bipolar PROM fusible link technology to provide user programmable logic for replacing conventional SSI/MSI gates and flip-flops at reduced chip count.

The family lets the systems engineer "design his own chip" by blowing fusible links to configure AND and OR gates to perform his desired logic function. Complex interconnections which previously required time-consuming layout are thus "lifted" from PC board etch and placed on silicon where they can be easily modified during prototype check-out or production.

The PAL transfer function is the familiar sum of products. Like the PROM, the PAL has a single array of fusible links. Unlike the PROM, the PAL is a programmable AND array driving a fixed OR array (the PROM is a fixed AND array driving a programmable OR array). In addition the PAL provides these options:

- Variable input/output pin ratio
- Programmable three-state outputs
- Registers with feedback
- Arithmetic capability

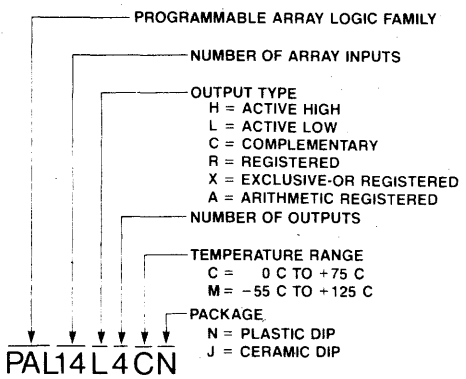
TM PAL is a Trade Mark of Monolithic Memories

Unused inputs are tied directly to V_{CC} or GND. Product terms with all fuses blown assume the logical high state, and product terms connected to both true and complement of any single input assume the logical low state. Registers consist of D type flip-flops which are loaded on the low to high transition of the clock. All registers are designed to power up to logical high state at the output pin. PAL Logic Diagrams are shown with all fuses blown, enabling the designer use of the diagrams as coding sheets. 8½ x 11 Logic Diagrams are available on request.

The entire PAL family is programmed on inexpensive conventional PROM programmers with appropriate personality and socket adapter cards. Once the PAL is programmed and verified, two additional fuses may be blown to defeat verification. This feature gives the user a proprietary circuit which is very difficult to copy.

PART NUMBER	DESCRIPTION
PAL10H8	OCTAL 10 INPUT AND-OR GATE ARRAY
PAL12H6	HEX 12 INPUT AND-OR GATE ARRAY
PAL14H4	QUAD 14 INPUT AND-OR GATE ARRAY
PAL16H2	DUAL 16 INPUT AND-OR GATE ARRAY
PAL16C1	16 INPUT AND-OR/AND-OR-INVERT GATE ARRAY
PAL10L8	OCTAL 10 INPUT AND-OR-INVERT GATE ARRAY
PAL12L6	HEX 12 INPUT AND-OR-INVERT GATE ARRAY
PAL14L4	QUAD 14 INPUT AND-OR-INVERT GATE ARRAY
PAL16L2	DUAL 16 INPUT AND-OR-INVERT GATE ARRAY
PAL16L8	OCTAL 16 INPUT AND-OR-INVERT GATE ARRAY
PAL16R8	OCTAL 16 INPUT REGISTERED AND-OR GATE ARRAY
PAL16R6	HEX 16 INPUT REGISTERED AND-OR GATE ARRAY
PAL16R4	QUAD 16 INPUT REGISTERED AND-OR GATE ARRAY
PAL16X4	QUAD 16 INPUT REGISTERED AND-OR-XOR GATE ARRAY
PAL16A4	QUAD 16 INPUT REGISTERED AND-CARRY-OR-XOR GATE ARRAY

Ordering Information

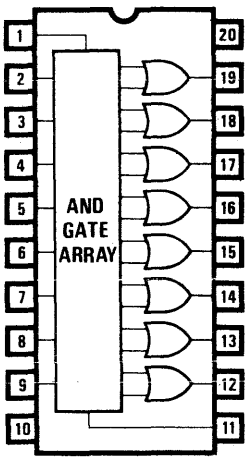


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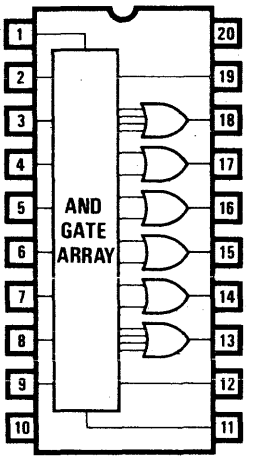
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PAL Logic Symbols

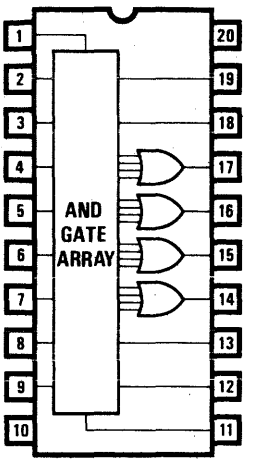
PAL10H8



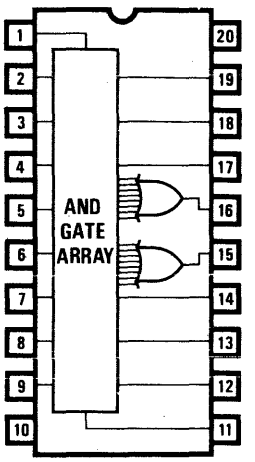
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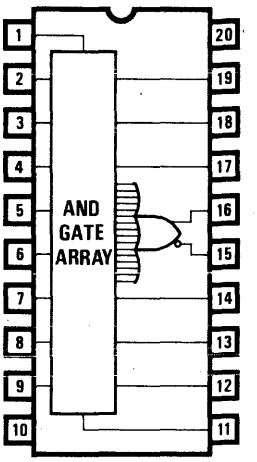
PAL14H4



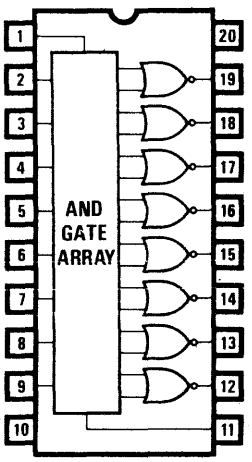
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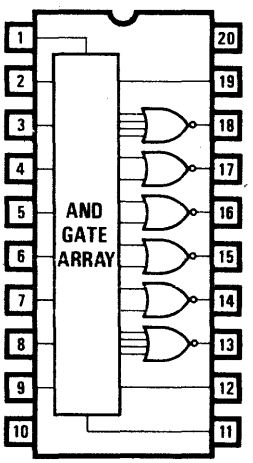
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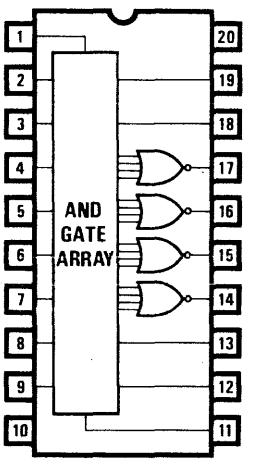
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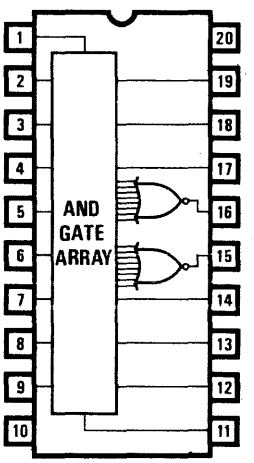
PAL12L6



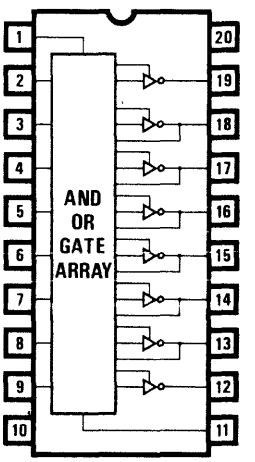
PAL14L4



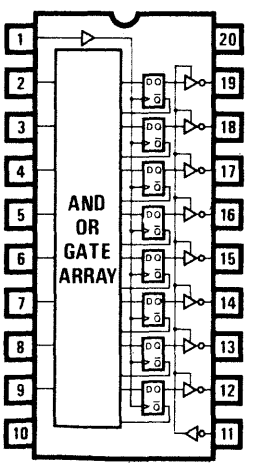
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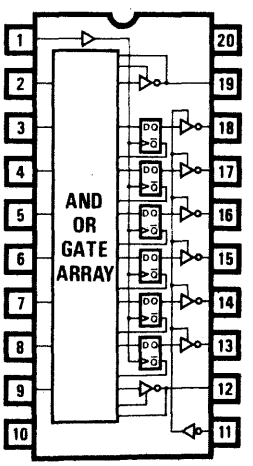
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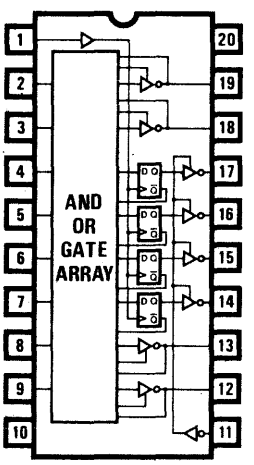
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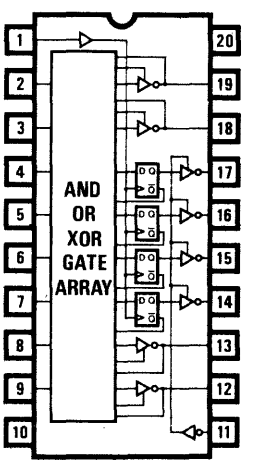
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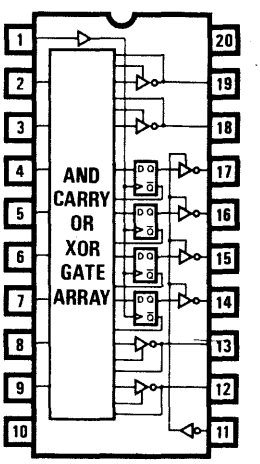
PAL16R4



PAL16X4



PAL16A4



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PRELIMINARY DATA

Absolute Maximum Ratings

	Operating	Programming
Supply voltage V_{CC}	7V	12V
Input voltage	5.5V	12V
Off-state output voltage	5.5V	12V
Storage temperature range	−65°C to 150°C	

10H8, 12H6, 14H4, 16H2, 16C1, 10L8, 12L6, 14L4, 16L2

Recommended Operating Conditions

SYMBOL	PARAMETER	MILITARY			COMMERCIAL			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5.0	5.5	4.75	5.00	5.25	V
I_{OH}	High-level output current			−2.0			−3.2	mA
I_{OL}	Low-level output current			8			8	mA
T_A	Operating free air temperature	−55		125	0		75	°C

Electrical Characteristics

Over Recommended Operating Temperature Range

SYMBOL	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
V_{IC}	Input clamp voltage	V_{CC} MIN, I_I 18 mA			−1.5	V
V_{OH}	High-level output voltage	V_{CC} MIN, V_{IH} 2V, V_{IL} 0.8V, I_{OH} MAX	2.4			V
V_{OL}	Low-level output voltage	V_{CC} MIN, V_{IH} 2V, V_{IL} 0.8V, I_{OL} = MAX			0.5	V
I_I	Input current at maximum input voltage	V_{CC} MAX, V_I 5.5V			1.0	mA
I_{IH}	High-level input current	V_{CC} MAX, V_I 2.4V			25	μA
I_{IL}	Low-level input current	V_{CC} MAX, V_I 0.4V			−250	μA
I_{OS}	Short-circuit output current	V_{CC} MAX	−30		−130	mA
I_{CC}	Supply current	V_{CC} MAX		55	90	mA

Switching Characteristics

Over Recommended Ranges of Temperature and V_{CC}

SYMBOL	PARAMETER	TEST CONDITIONS†† R_L = 2.0 KΩ	MILITARY T_A = −55° to +125°C V_{CC} = 5.0V ± 10%			COMMERCIAL T_A = 0° to 75°C V_{CC} = 5.0V ± 5%			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
t_{PD}	From any input to any output	C_L = 15pF		45			40		ns

†† See Standard Test Load and Definition of Waveforms, page 10-4

MMI

MEMORY

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16L8, 16R8, 16R6, 16R4, 16X4▼, 16A4▼

Recommended Operating Conditions

SYMBOL	PARAMETER	MILITARY			COMMERCIAL			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5.0	5.5	4.75	5.00	5.25	V
I_{OH}	High-level output current			−2.0			−3.2	mA
I_{OL}	Low-level output current			12			24	mA
T_A	Operating free air temperature	−55		125*	0		75	°C

Electrical Characteristics

Over Recommended Operating Temperature Range

SYMBOL	PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_{IC}	Input clamp voltage		V_{CC} = MIN, I_I = −18mA			−1.5	V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IH} = 2V, V_{IL} = 0.8V, I_{OH} = MAX	2.4			V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH}=2V, V_{IL} = 0.8V, I_{OL}=MAX			0.5	V
I_{OZH}	Off-state output current high-level voltage applied		V_{CC} = MAX, V_{IH} = 2V, V_O = 2.4V, VIL = 0.8V			100	μA
I_{OZL}	Off-state output current low-level voltage applied		V_{CC} = MAX, V_{IH} = 2V, V_O = 0.4V, VIL = 0.8V			−100	μA
I_I	Input current at maximum input voltage		V_{CC} = MAX, V_I = 5.5V			1.0	mA
I_{IH}	High-level input current		V_{CC} = MAX, V_I = 2.4V			25	μA
I_{IL}	Low-level input current		V_{CC} = MAX, V_I = 0.4V			−250	μA
I_{OS}	Short-circuit output current		V_{CC} = MAX,	−30		−130	mA
I_{CC}	Supply Current	16L8	V_{CC} = MAX		140	210†	mA
		16R4,16R6,16R8			150	225†	
		16X4,16A4			160		

Switching Characteristics

Over Recommended Ranges of Temperature and V_{CC}

SYMBOL	PARAMETER		TEST CONDITIONS†† R_L = 667 Ω	MILITARY* T_A = −55° to +125°C, V_{CC} = 5.0V ± 10%			COMMERCIAL T_A = −0° to +75°C, V_{CC} = 5.0V ± 5%			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
t_{PD}	Input to output		C_L = 45pF		25	45		25	40	ns
t_{PD}	Clock to output				15	25		15	25	ns
t_{PZX}	Pin 11 to output enable				15	25		15	25	ns
t_{PXZ}	Pin 11 to output disable		C_L = 5pF		15	25		15	25	ns
t_{PZX}	Input to output enable		C_L = 45pF		25	45		25	40	ns
t_{PXZ}	Input to output disable		C_L = 5pF		25	45		25	40	ns
t_w	Width of clock	High		25			25			ns
		Low		25			25			
t_{su}	Setup time	16R8,16R6,16R4		45			40			ns
		16X4, 16A4								
t_h	Hold time			0	−15		0	−15		ns

*Operating Case Temperature only, T_C = 125°C

†I_{CC} = MAX at minimum temperature

†† See Standard Test Load and Definition of Waveforms, page 10-4

▼PRELIMINARY

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Programming

PAL fuses are programmed using a low-voltage linear-select procedure which is common to all 15 PAL types. The array is divided into two groups, products 0 thru 31 and products 32 thru 63, for which pin identifications are shown in Figure 1. To program a particular fuse, both an input line and a product line are selected according to the following procedure:

Step 1 Raise Output Disable, OD, to V_{IHH}

Step 2 Select an input line by specifying I_0, I_1, I_2, I_3, I_4, I_5, I_6, I_7 and L/R as shown in Table 1

Step 3 Select a product line by specifying A_0, A_1 and A_2 one-of-eight select as shown in Table 2

Step 4 Raise V_{CC} (pin 20) to V_{IHH}

Step 5 Program the fuse by pulsing the output pins, O, of the selected product group to V_{IHH} as shown in Table 2.

Step 6 Lower V_{CC} (pin 20) to 6.0 V

Step 7 Pulse the CLOCK pin and verify the output pin, O, to be Low for active Low PAL types or High for active High PAL types.

Step 8 Lower V_{CC} (pin 20) to 4.2 V and repeat step 7

Step 9 Should the output not verify, repeat steps 1 thru 8 up to five (5) times.

This procedure is repeated for all fuses to be blown (see programming waveforms).

To prevent further verification, two last fuses may be blown by raising pin 1 and pin 11 to VP. VCC is not required during this operation.

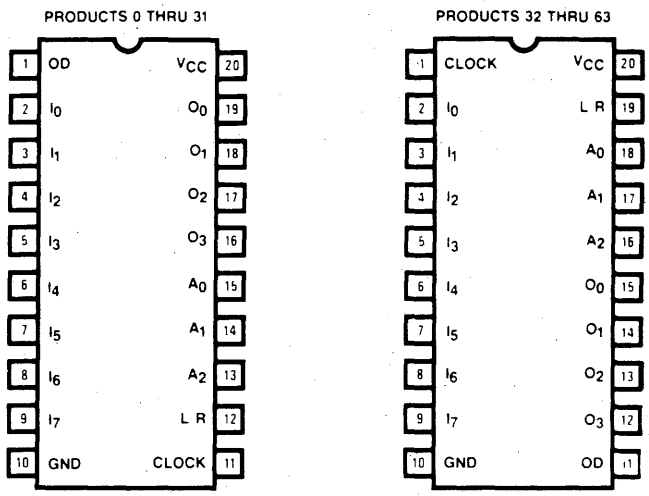
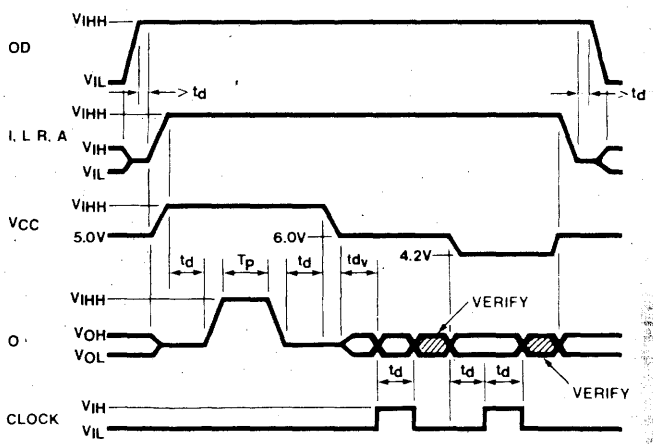


Figure 1 Pin Identification

Programming Waveforms



Programming Parameters

T_A = 25°C

SYMBOL	PARAMETER		LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT
V_{IHH}	Program-level input voltage		10.5	11	11.5	V
I_{IHH}	Program-level input current	Output Program Pulse			50	mA
		OD, L/R			25	
		All Other Inputs			5	
I_{CCH}	Program Supply Current				400	mA
T_P	Program Pulse Width		10		50	µs
t_d	Delay time		100			ns
	Program Pulse duty cycle				25	%
V_P	Program/Verify-Protect-input voltage			20		V
I_P	Program/Verify-Protect-input current				400	mA
t_{dv}	Delay Time to Verify		100			µs

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Voltage Legend

L = Low-level input voltage, V_{IL}
H = High-level input voltage, V_{IH}
HH = High-level program voltage, V_{IHH}
Z = High impedance (e.g. 10 KΩ to +5.0 V)

INPUT LINE NUMBER	PIN IDENTIFICATION								
	I_7	I_6	I_5	I_4	I_3	I_2	I_1	I_0	L/R
0	HH	HH	HH	HH	HH	HH	HH	L	L
1	HH	HH	HH	HH	HH	HH	HH	H	L
2	HH	HH	HH	HH	HH	HH	HH	L	HH
3	HH	HH	HH	HH	HH	HH	HH	H	HH
4	HH	HH	HH	HH	HH	HH	L	HH	L
5	HH	HH	HH	HH	HH	HH	H	HH	L
6	HH	HH	HH	HH	HH	HH	L	HH	HH
7	HH	HH	HH	HH	HH	HH	H	HH	HH
8	HH	HH	HH	HH	HH	L	HH	HH	L
9	HH	HH	HH	HH	HH	H	HH	HH	L
10	HH	HH	HH	HH	HH	L	HH	HH	HH
11	HH	HH	HH	HH	HH	H	HH	HH	HH
12	HH	HH	HH	HH	L	HH	HH	HH	L
13	HH	HH	HH	HH	H	HH	HH	HH	L
14	HH	HH	HH	HH	L	HH	HH	HH	HH
15	HH	HH	HH	HH	H	HH	HH	HH	HH
16	HH	HH	HH	L	HH	HH	HH	HH	L
17	HH	HH	HH	H	HH	HH	HH	HH	L
18	HH	HH	HH	L	HH	HH	HH	HH	HH
19	HH	HH	HH	H	HH	HH	HH	HH	HH
20	HH	HH	L	HH	HH	HH	HH	HH	L
21	HH	HH	H	HH	HH	HH	HH	HH	L
22	HH	HH	L	HH	HH	HH	HH	HH	HH
23	HH	HH	H	HH	HH	HH	HH	HH	HH
24	HH	L	HH	HH	HH	HH	HH	HH	L
25	HH	H	HH	HH	HH	HH	HH	HH	L
26	HH	L	HH	HH	HH	HH	HH	HH	HH
27	HH	H	HH	HH	HH	HH	HH	HH	HH
28	L	HH	HH	HH	HH	HH	HH	HH	L
29	H	HH	HH	HH	HH	HH	HH	HH	L
30	L	HH	HH	HH	HH	HH	HH	HH	HH
31	H	HH	HH	HH	HH	HH	HH	HH	HH

Table 1 Input Line Select

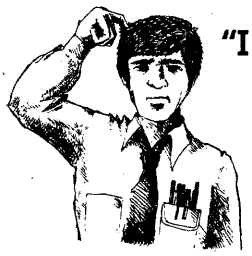
PRODUCT LINE NUMBER	PIN IDENTIFICATION						
	O_3	O_2	O_1	O_0	A_2	A_1	A_0
0, 32	Z	Z	Z	HH	Z	Z	Z
1, 33	Z	Z	Z	HH	Z	Z	HH
2, 34	Z	Z	Z	HH	Z	HH	Z
3, 35	Z	Z	Z	HH	Z	HH	HH
4, 36	Z	Z	Z	HH	HH	Z	Z
5, 37	Z	Z	Z	HH	HH	Z	HH
6, 38	Z	Z	Z	HH	HH	HH	Z
7, 39	Z	Z	Z	HH	HH	HH	HH
8, 40	Z	Z	HH	Z	Z	Z	Z
9, 41	Z	Z	HH	Z	Z	Z	HH
10, 42	Z	Z	HH	Z	Z	HH	Z
11, 43	Z	Z	HH	Z	Z	HH	HH
12, 44	Z	Z	HH	Z	HH	Z	Z
13, 45	Z	Z	HH	Z	HH	Z	HH
14, 46	Z	Z	HH	Z	HH	HH	Z
15, 47	Z	Z	HH	Z	HH	HH	HH
16, 48	Z	HH	Z	Z	Z	Z	Z
17, 49	Z	HH	Z	Z	Z	Z	HH
18, 50	Z	HH	Z	Z	Z	HH	Z
19, 51	Z	HH	Z	Z	Z	HH	HH
20, 52	Z	HH	Z	Z	HH	Z	Z
21, 53	Z	HH	Z	Z	HH	Z	HH
22, 54	Z	HH	Z	Z	HH	HH	Z
23, 55	Z	HH	Z	Z	HH	HH	HH
24, 56	HH	Z	Z	Z	Z	Z	Z
25, 57	HH	Z	Z	Z	Z	Z	HH
26, 58	HH	Z	Z	Z	Z	HH	Z
27, 59	HH	Z	Z	Z	Z	HH	HH
28, 60	HH	Z	Z	Z	HH	Z	Z
29, 61	HH	Z	Z	Z	HH	Z	HH
30, 62	HH	Z	Z	Z	HH	HH	Z
31, 63	HH	Z	Z	Z	HH	HH	HH

Table 2 Product Line Select

Approved Programmers:

- Data I/O models 5 or 9
- Programming card set: 909-1427
- Socket adapters: VOH-PAL: 715-1428-1
- Socket adapters: VOL-PAL: 715-1428-2
- Socket adapters: COHPL-PAL: 715-1428-3

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- Memory IC
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- Static
- 1024x1
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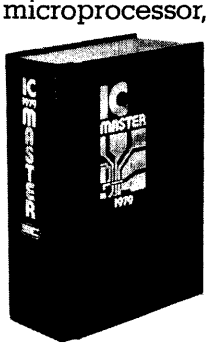
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UTP

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TMS2716L
TMS27A16L

MOS

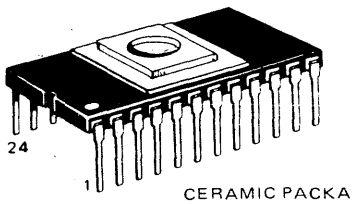
(N-CHANNEL, SILICON-GATE)

2048 × 8-BIT
UV ERASABLE PROM

2048 × 8 ERASABLE PROM

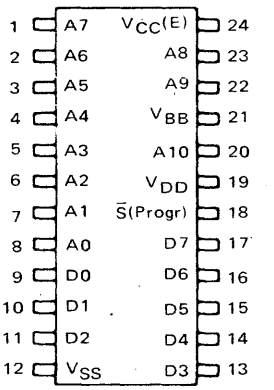
The TMS2716L and TMS27A16L are 16,384-bit Erasable and Electrically Reprogrammable PROMs designed for system debug usage and similar applications requiring nonvolatile memory that could be reprogrammed periodically. The transparent lid on the package allows the memory content to be erased with ultraviolet light. The TMS2716 is pin compatible with 2708 EPROMs, allowing easy memory size doubling.

- Organized as 2048 Bytes of 8 Bits
- Fully Static Operation (No Clocks, No Refresh)
- Standard Power Supplies of +12 V, +5 V, and −5 V
- Maximum Access Time = 300 ns — TMS27A16L
  450 ns — TMS2716L
- Chip-Select Input for Memory Expansion
- TTL Compatible — No Pull-up Resistors Required
- Three-State Outputs for OR-Tie Capability
- The TMS2716L is Pin Compatible to MCM2708L, MCM2708P, MCM2708C, and MCM68708L EPROMs

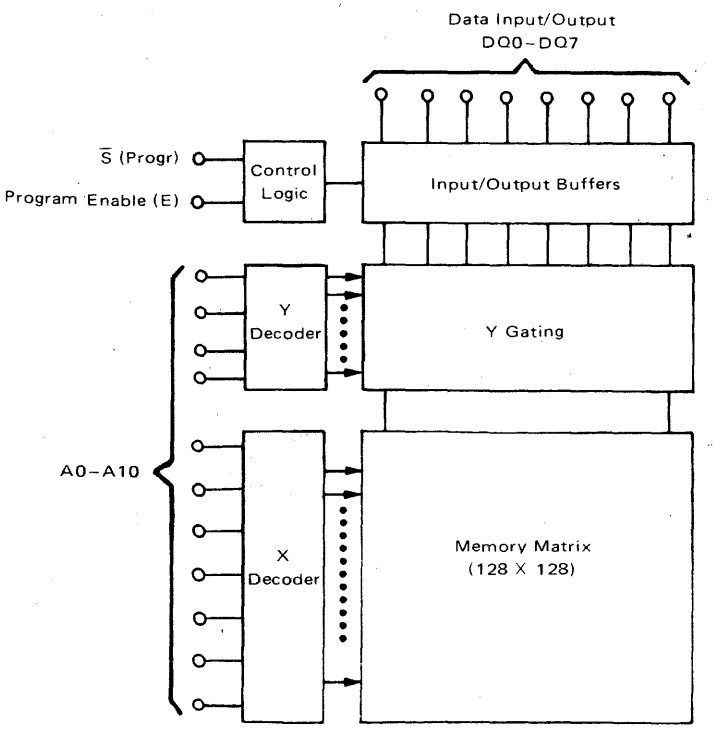


CERAMIC PACKAGE
CASE 716-03

PIN ASSIGNMENT



BLOCK DIAGRAM



PIN NAMES

A0–A10 . . . . Address Inputs
DQ0–DQ7 . . . Data Input (Program) or Output (Read)
(E) . . . . Program Enable
S . . . . Chip Select
(Progr) . . . . Program Pulse
V_{BB} . . . . −5 V Power Supply
V_{CC} . . . . +5 V Power Supply
V_{DD} . . . . +12 V Power Supply
V_{SS} . . . . Ground

This is advance information and specifications are subject to change without notice.

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DS 9518

Motorola

MEMORY

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DC READ OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature range unless otherwise noted)

RECOMMENDED DC READ OPERATING CONDITIONS

Parameter		Symbol	Min	Nom	Max	Unit
Supply Voltage	TMS2716L	V_{CC}	4.75	5.0	5.25	Vdc
		V_{DD}	11.4	12	12.6	Vdc
		V_{BB}	−5.25	−5.0	−4.75	Vdc
	TMS27A16L	V_{CC}	4.5	5.0	5.5	Vdc
		V_{DD}	10.8	12	13.2	Vdc
		V_{BB}	−5.5	−5.0	−4.5	Vdc
Input High Voltage		V_{IH}	2.2	–	V_{CC} + 1.0	Vdc
Input Low Voltage		V_{IL}	V_{SS}	–	0.65	Vdc

READ OPERATING DC CHARACTERISTICS

Characteristic	Condition	Symbol	Min	Typ	Max	Unit
Address Input Sink Current	$V_{in} = V_{CC}$max or $V_{in} = V_{IL}$	I_{in}	–	1	10	μA
Output Leakage Current	$V_{out} = V_{CC}$max and $\overline{S} = 5$ V	I_{LO}	–	1	10	μA
V_{DD} Supply Current	Worst-Case Supply Currents All Inputs High (E) = 5.0 V, $T_A = 0^oC$	I_{DD}	–	–	65	mA
V_{CC} Supply Current		I_{CC}	–	–	12	mA
V_{BB} Supply Current		I_{BB}	–	–	45	mA
Output Low Voltage	$I_{OL} = 1.6$ mA	V_{OL}	–	–	0.45	V
Output High Voltage	$I_{OH} = -100$ μA	V_{OH1}	3.7	–	–	V
Output High Voltage	$I_{OH} = -1.0$ mA	V_{OH2}	2.4	–	–	V

V_{BB} must be applied prior to V_{CC} and V_{DD}. V_{BB} must also be the last power supply switched off.

CAPACITANCE (periodically sampled rather than 100% tested)

Characteristic	Condition	Symbol	Typ	Max	Unit
Input Capacitance (f = 1.0 MHz)	$V_{in} = 0$ V, $T_A = 25^oC$	C_{in}	4.0	6.0	pF
Output Capacitance (f = 1.0 MHz)	$V_{out} = 0$ V, $T_A = 25^oC$	C_{out}	8.0	12	pF

AC READ OPERATING CONDITIONS AND CHARACTERISTICS

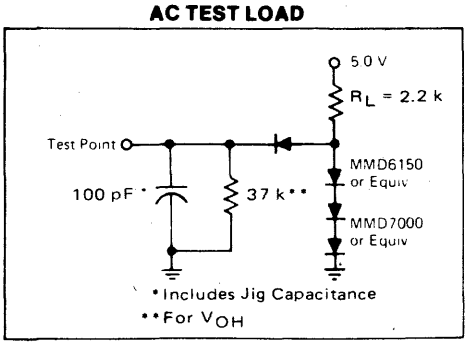
(Full operating voltage and temperature range unless otherwise noted)

(All timing with $t_r = t_f = 20$ ns, Load per Note 2)

Characteristic	Symbol	TMS2716L		TMS27A16L		Unit
		Min	Max	Min	Max	
Address to Output Delay	t_{AVQV}	–	450	–	300	ns
Chip Select to Output Delay	t_{SLQV}	–	120	–	120	ns
Data Hold from Address	t_{AXQZ}	10	–	10	–	ns
Data Hold from Deselection	t_{SHQZ}	10	120	10	120	ns

NOTE 2: Output Load = 1 TTL Gate and C_L = 100 pF (Includes Jig Capacitance)
Timing Measurement Reference Levels – Inputs: 0.8 V and 2.8 V
Outputs: 0.8 V and 2.4 V

AC TEST LOAD

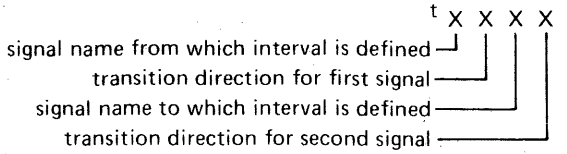


PIN CONNECTION DURING READ OR PROGRAM

Mode	Pin Number		
	9–11, 13–17	18	24
Read	D_{out}	V_{IL} or V_{IH}	V_{CC}
Program	D_{in}	Pulsed V_{IHP}	V_{IHW}

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TIMING PARAMETER ABBREVIATIONS



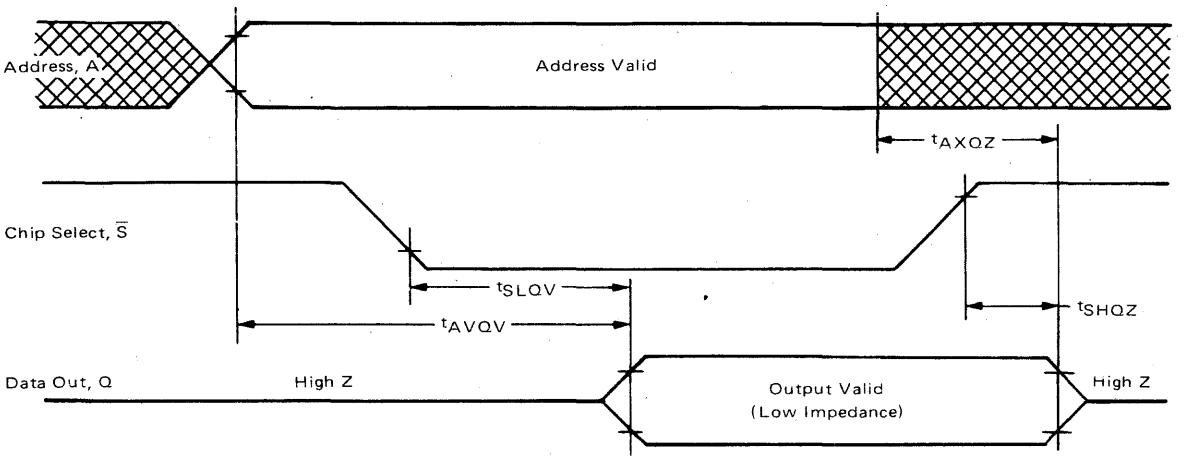
The transition definitions used in this data sheet are:

H = transition to high
L = transition to low
V = transition to valid
X = transition to invalid or don't care
Z = transition to off (high impedance)

TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

READ OPERATION TIMING DIAGRAM



DC PROGRAMMING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature range unless otherwise noted)

RECOMMENDED PROGRAMMING OPERATING CONDITIONS

Parameter	Symbol	Min	Nom	Max	Unit
Supply Voltage – TMS2716L and TMS27A16L	V_{CC} V_{DD} V_{BB}	4.75 11.4 -5.25	5.0 12 -5.0	5.25 12.6 -4.75	Vdc Vdc Vdc
Input High Voltage for Data	V_{IHD}	3.8	–	V_{CC} + 1	Vdc
Input Low Voltage for Data	V_{ILD}	V_{SS}	–	0.65	Vdc
Input High Voltage for Addresses	V_{IHA}	3.8	–	V_{CC} + 1	Vdc
Input Low Voltage for Addresses	V_{ILA}	V_{SS}	–	0.4	Vdc
Program Enable (E) Input High Voltage (Note 3)	V_{IHW}	11.4	12	12.6	Vdc
Program Enable (E) Input Low Voltage (Note 3)	$V_{ILW}=V_{CC}$	4.75	5.0	5.25	Vdc
Program Pulse Input High Voltage (Note 3)	V_{IHP}	25	–	27	Vdc
Program Pulse Input Low Voltage (Note 4)	V_{ILP}	V_{SS}	–	1.0	Vdc

NOTE 3: Referenced to V_{SS}.
NOTE 4: $V_{IHP} - V_{ILP} = 25$ V min.

PROGRAMMING OPERATION DC CHARACTERISTICS

Characteristic	Condition	Symbol	Min	Typ	Max	Unit
Address Input Sink Current	$V_{in} = 5.25$ V	I_{LI}	–	–	10	μAdc
Program Pulse Source Current		I_{IPL}	–	–	3.0	mAdc
Program Pulse Sink Current		I_{IPH}	–	–	20	mAdc
V_{DD} Supply Current	Worst-Case Supply Currents All Inputs High (E) = 5 V, $T_A = 0^oC$	I_{DD}	–	–	65	mAdc
V_{CC} Supply Current		I_{CC}	–	–	15	mAdc
V_{BB} Supply current		I_{BB}	–	–	45	mAdc

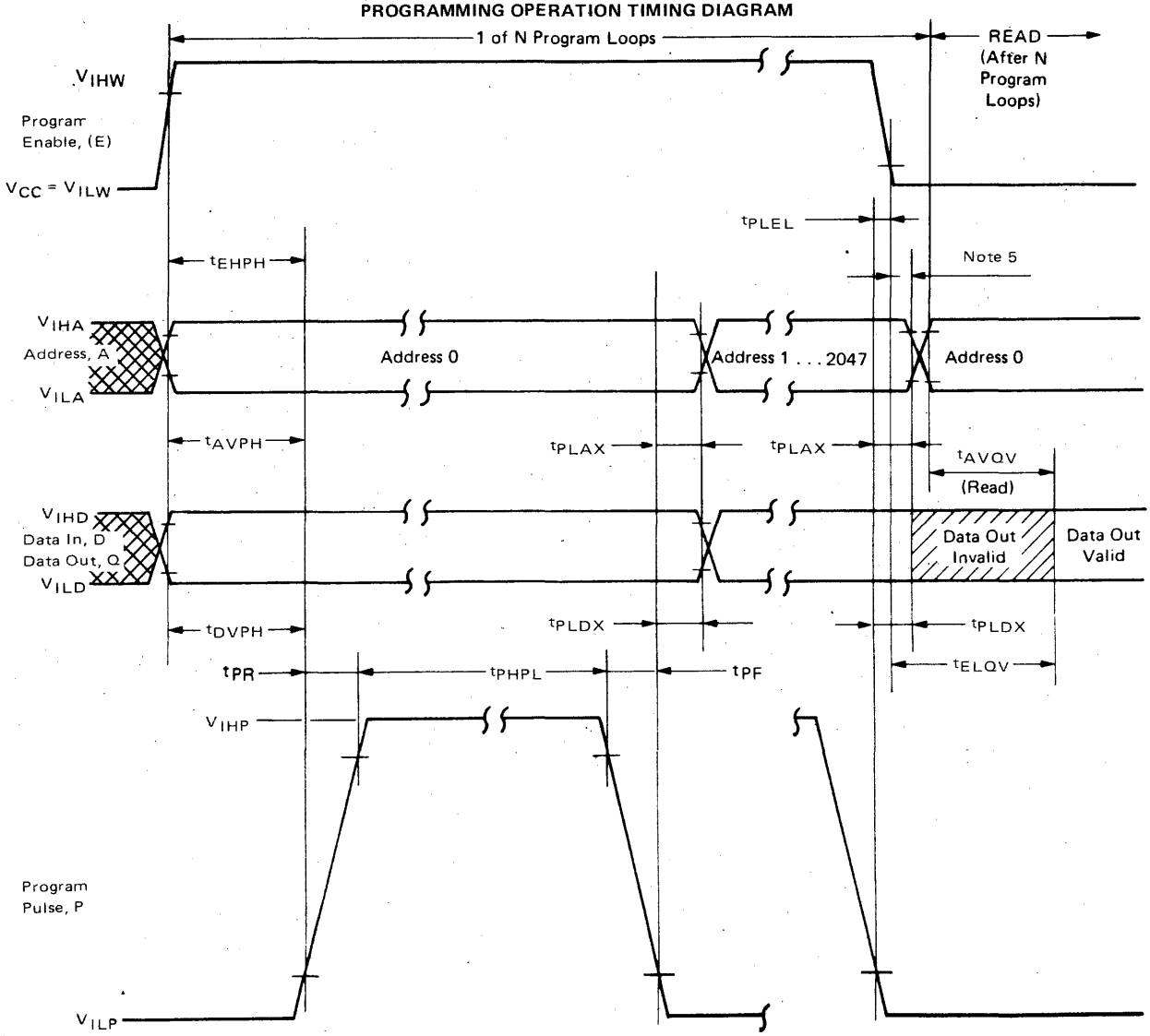
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AC PROGRAMMING OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature unless otherwise noted)

Characteristic	Symbol	Min	Max	Unit
Address Setup Time	t_{AVPH}	10	–	μs
(E) Setup Time	t_{EHPH}	10	–	μs
Data Setup Time	t_{DVPH}	10	–	μs
Address Hold Time	t_{PLAX}	1.0	–	μs
(E) Hold Time	t_{PLEL}	0.5	–	μs
Data Hold Time	t_{PLDX}	1.0	–	μs
Program to Read Delay	t_{ELQV}	–	10	μs
Program Pulse Width	t_{PHPL}	0.1	1.0	ms
Program Pulse Rise Time	t_{PR}	0.5	2.0	μs
Program Pulse Fall Time	t_{PF}	0.5	2.0	μs

PROGRAMMING OPERATION TIMING DIAGRAM



NOTE 5: This Program Enable tranistion must occur after the Program Pulse transition and before the Address Transition.

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3501 ED BLUESTEIN BLVD., AUSTIN, TEXAS 78721

MCM6670
MCM6674

MOS

(N-CHANNEL, SILICON GATE)

128c x 7 x 5
HORIZONTAL-SCAN
CHARACTER GENERATOR

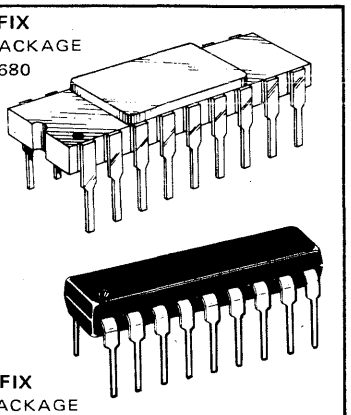
128c X 7 X 5 CHARACTER GENERATOR

The MCM6670 is a mask-programmable horizontal-scan (row select) character generator containing 128 characters in a 5 X 7 matrix. A 7-bit address code is used to select one of the 128 available characters, and a 3-bit row select code chooses the appropriate row to appear at the outputs. The rows are sequentially displayed, providing a 7-word sequence of 5 parallel bits per word for each character selected by the address inputs.

The MCM6674 is a preprogrammed version of the MCM6670. The complete pattern of this device is contained in this data sheet.

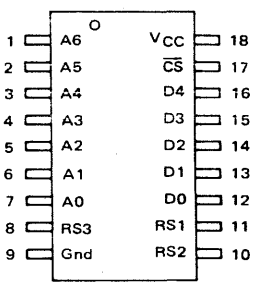
- Fully Static Operation
- TTL Compatibility
- Single ±10% +5 Volt Power Supply
- 18-Pin Package
- Diagonal Corner Power Supply Pins
- Fast Access Time, 350 ns (max)

L SUFFIX
CERAMIC PACKAGE
CASE 680



P SUFFIX
PLASTIC PACKAGE
CASE 707

PIN ASSIGNMENT



CAPACITANCE (T_A = 25°C, f = 1.0 MHz)

Characteristic	Symbol	Typ	Unit
Input Capacitance	C_{in}	5.0	pF
Output Capacitance	C_{out}	5.0	pF

DC OPERATING CONDITIONS AND CHARACTERISITCS

(Full operating voltage and temperature range unless otherwise noted.)

RECOMMENDED DC OPERATING CONDITIONS

Parameter	Symbol	Min	Nom	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	Vdc
Input High Voltage	V_{IH}	2.0	–	5.25	Vdc
Input Low Voltage	V_{IL}	-0.3	–	0.8	Vdc

DC CHARACTERISTICS

Characteristic	Symbol	Min	Typ	Max	Unit
Input Current (V_{in} = 0 to 5.25 V)	I_{in}	–	–	2.5	μAdc
Output High Voltage (I_{OH} = -205 μA)	V_{OH}	2.4	–	V_{CC}	Vdc
Output Low Voltage (I_{OL} = 1.6 mA)	V_{OL}	–	–	0.4	Vdc
Output Leakage Current (Three-State) (CS = 2.0 V or $\overline{CS}$ = 0.8 V, V_{out} = 0.4 V to 2.4 V)	I_{LO}	–	–	10	μAdc
Supply Current (V_{CC} = 5.25 V, T_A = 0°C)	I_{CC}	–	–	130	mAdc

This is advance information and specifications are subject to change without notice.
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DS 9459
Formerly ADI-353

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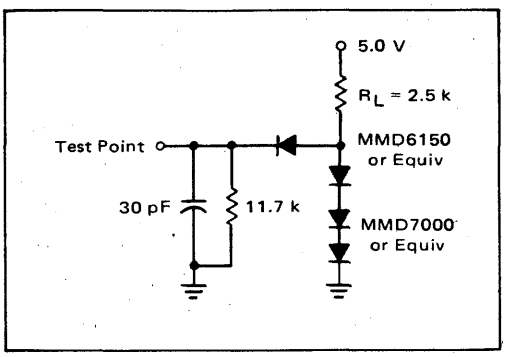
AC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature range unless otherwise noted.)

AC TEST CONDITIONS

Condition	Value
Input Pulse Levels	0.8 V to 2.0 V
Input Rise and Fall Times	20 ns
Output Load	1 TTL Gate and C_L = 30 pF

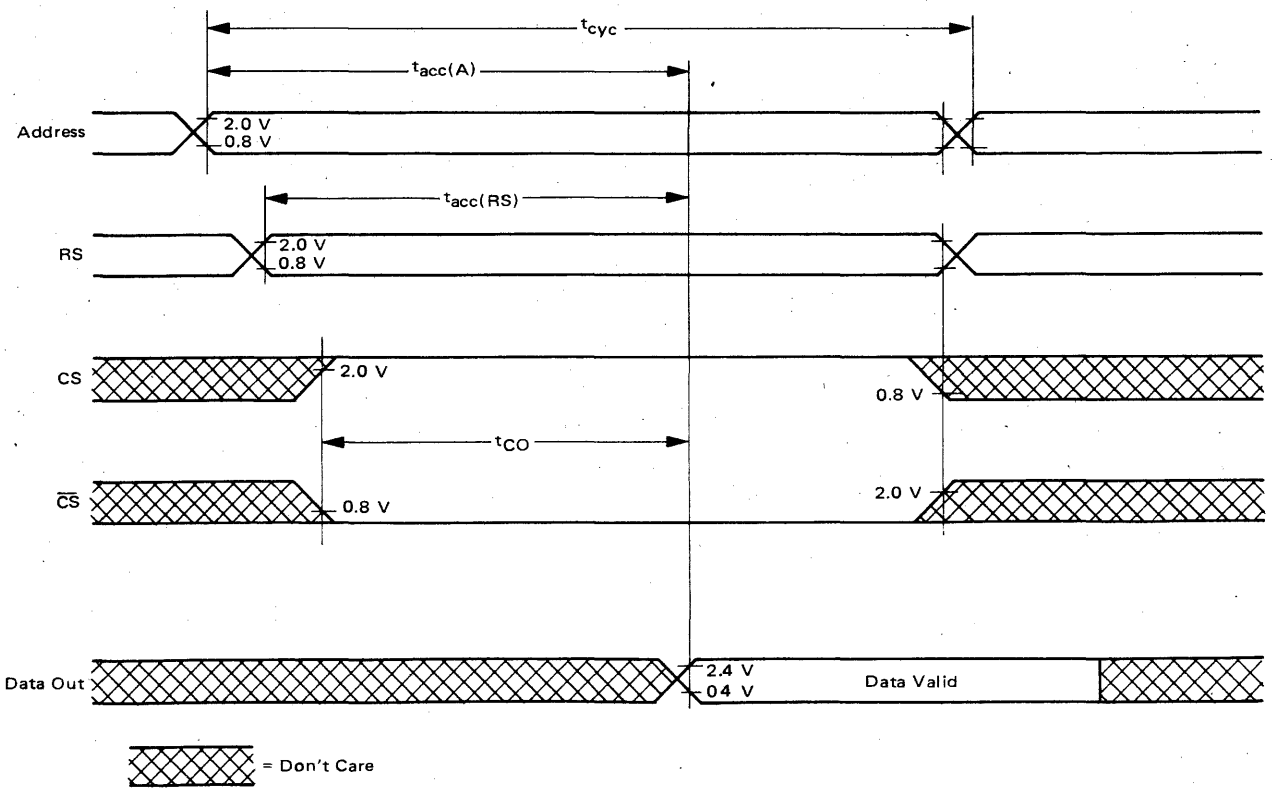
AC TEST LOAD



AC CHARACTERISTICS

Characteristic	Symbol	Min	Max	Unit
Cycle Time	t_{cyc}	350	–	ns
Address Access Time	$t_{acc(A)}$	–	350	ns
Row Select Access Time	$t_{acc(RS)}$	–	350	ns
Chip Select to Output Delay	t_{CO}	–	150	ns

TIMING DIAGRAM



©IC MASTER 1979

CUSTOM PROGRAMMING FOR MCM6670

By the programming of a single photomask, the customer may specify the content of the MCM6670/MCM66700 Encoding of the photomask is done with the aid of a computer to provide quick, efficient implementation of the custom bit pattern while reducing the cost of implementation.

Information for the custom memory content may be sent to Motorola in the following forms, in order of preference:

1. Hexadecimal coding using IBM Punch Cards
2. Hexadecimal coding using ASCII Paper Tape Punch

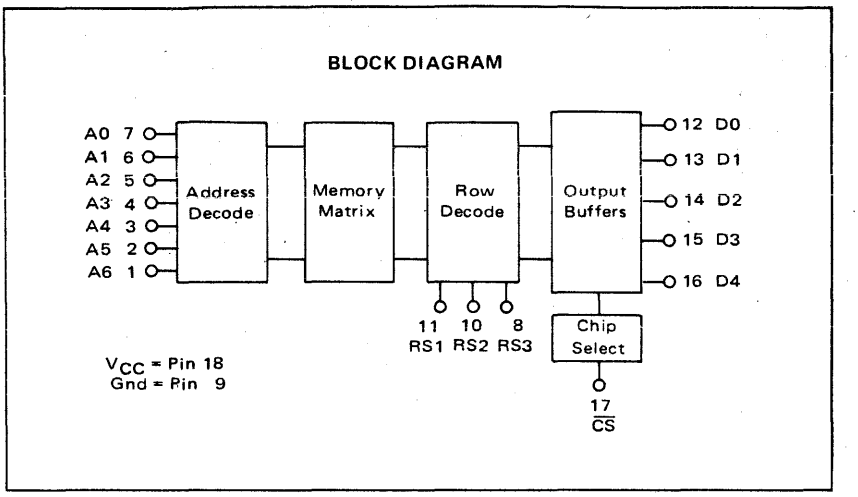
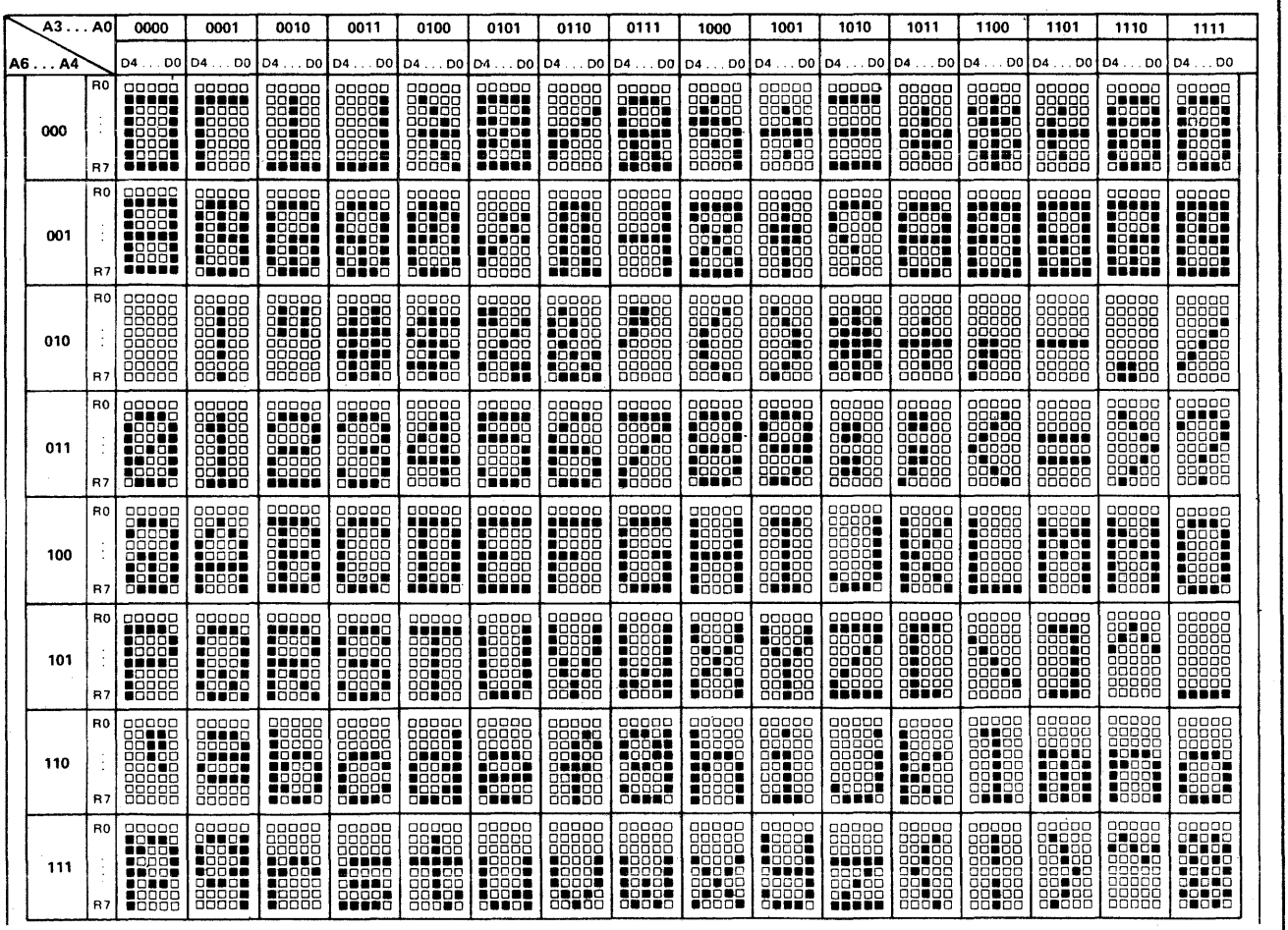


FIGURE 6 – MCM6674 PATTERN



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MOTOROLA
Semiconductors
3501 ED BLUESTEIN BLVD., AUSTIN, TEXAS 78721

MCM2716
MCM27A16

Product Preview

2048 X 8-BIT UV ERASABLE PROM

The MCM2716/27A16 is a 16,384-bit Erasable and Electrically Reprogrammable PROM designed for system debug usage and similar applications requiring nonvolatile memory that could be reprogrammed periodically. The transparent lid on the package allows the memory content to be erased with ultraviolet light.

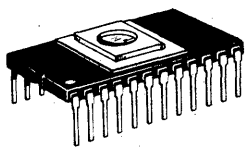
For ease of use, the device operates from a single power supply and has a static power-down mode. Pin-for-pin mask programmable ROMS are available for large volume production runs of systems initially using the MCM2716/27A16.

- Single ±10% 5 V Power Supply
- Automatic Power-down Mode (Standby)
- Organized as 2048 Bytes of 8 Bits
- Low Power Dissipation
- TTL Compatible During Read and Program
- Maximum Access Time = 450 ns MCM2716
  350 ns MCM27A16
- Pin Equivalent to Intel's 2716
- Pin Compatible to MCM68A316E Mask Programmable ROMs

MOS

(N-CHANNEL, SILICON-GATE)

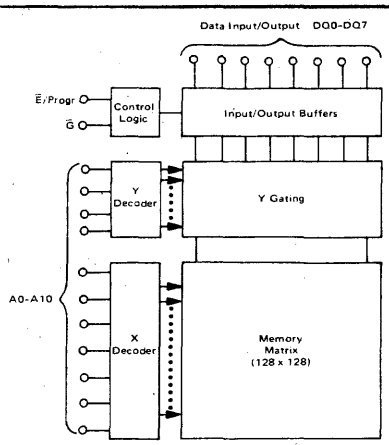
2048 X 8-BIT
UV ERASABLE PROM



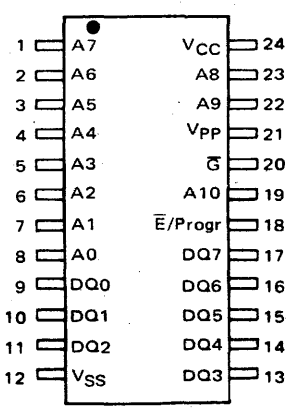
CERAMIC PACKAGE
CASE 716-03

Mode	PIN NUMBER					
	9–11, 13–17	12	18	20	21	24
	DQ	V_{SS}	$\overline{E}$/Progr	$\overline{G}$	V_{PP}	V_{CC}
Read	Data out	V_{SS}	V_{IL}	V_{IL}	V_{CC}	V_{CC}
Output Disable	Hi Z	V_{SS}	Don't Care	V_{IH}	V_{CC}	V_{CC}
Standby	Hi Z	V_{SS}	V_{IH}	Don't Care	V_{CC}	V_{CC}
Program	Data in	V_{SS}	Pulsed V_{IL} to V_{IH}	V_{IH}	V_{IHP}	V_{CC}
Program Verify	Data out	V_{SS}	V_{IL}	V_{IL}	V_{IHP}	V_{CC}
Program Inhibit	Hi Z	V_{SS}	V_{IL}	V_{IH}	V_{IHP}	V_{CC}

BLOCK DIAGRAM



PIN ASSIGNMENT



*PIN NAMES
A . . . . Address
DQ . . . . Data Input/Output
$\overline{E}$/Progr . . . . Chip Enable/Program
$\overline{G}$ . . . . Output Enable

*New industry standard nomenclature

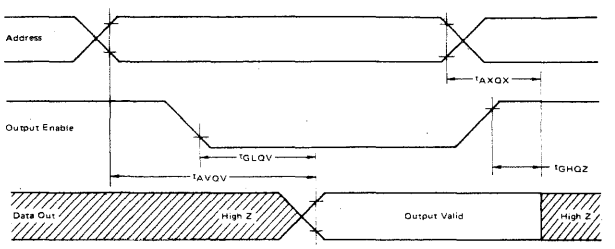
This is advance information and specifications are subject to change without notice.

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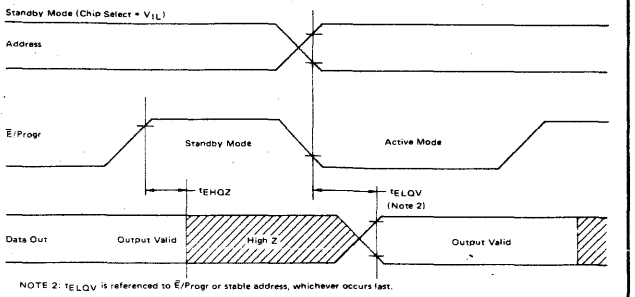
ADI-491

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READ MODE TIMING DIAGRAMS
(Chip Enable = V_{IL})



STANDBY MODE
(Output Enable = V_{IL})



NOTE 2: t_{ELQV} is referenced to $\overline{E}$/Progr or stable address, whichever occurs last.

DC OPERATING CONDITIONS AND CHARACTERISTICS
(Full operating voltage and temperature range unless otherwise noted)

RECOMMENDED DC READ OPERATING CONDITIONS (T_A = 0° to +70°C)

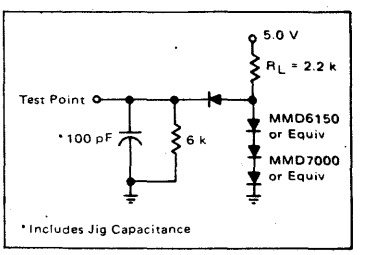
Parameter		Symbol	Min	Nom	Max	Unit
Supply Voltage*	MCM2716	V_{CC}	4.75	5.0	5.25	Vdc
	MCM27A16		4.5	5.0	5.5	
		V_{PP}	V_{CC} – 0.6	5.0	V_{CC} + 0.6	
Input High Voltage		V_{IH}	2.0	–	V_{CC} + 1.0	Vdc
Input Low Voltage		V_{IL}	-0.1	–	0.8	Vdc

READ OPERATION DC CHARACTERISTICS

Characteristic	Condition	Symbol	Min	Typ	Max	Unit
Address, $\overline{G}$ and $\overline{E}$/Progr Input Sink Current	V_{in} = 5.25 V	I_{in}	–	–	10	μA
Output Leakage Current	V_{out} = 5.25 V, $\overline{G}$ = 5.0 V	I_{LO}	–	–	10	μA
V_{CC} Supply Current* (Standby)	$\overline{E}$/Progr = V_{IH}, $\overline{G}$ = V_{IL}	I_{CC1}	–	10	25	mA
V_{CC} Supply Current* (Active)	$\overline{G}$ = $\overline{E}$/Progr = V_{IL}	I_{CC2}	–	57	100	mA
V_{PP} Supply Current*	V_{PP} = 5.85 V	I_{PP1}	–	–	5.0	mA
Output Low Voltage	I_{OL} = 2.1 mA	V_{OL}	–	–	0.45	V
Output High Voltage	I_{OH} = -400 μA	V_{OH}	2.4	–	–	V

*V_{CC} must be applied simultaneously or prior to V_{PP}. V_{CC} must also be switched off simultaneously with or after V_{PP}. With V_{PP} connected directly to V_{CC} during the read operation, the supply current would be the sum of I_{PP1} and I_{CC}. The additional 0.6 V tolerance on V_{PP} makes it possible to use a driver circuit for switching the V_{PP} supply pin from V_{CC} in Read mode to +25 V for programming. Typical values are for T_A = 25°C and nominal supply voltages.

FIGURE 1 – AC TEST LOAD



CAPACITANCE
(f = 1.0 MHz, T_A = 25°C, periodically sampled rather than 100% tested.)

Characteristic	Symbol	Typ	Max	Unit
Input Capacitance (V_{in} = 0 V)	C_{in}	4.0	6.0	pF
Output Capacitance (V_{out} = 0 V)	C_{out}	8.0	12	pF

Capacitance measured with a Boonton Meter or effective capacitance calculated from the equation: $C = \frac{I\Delta_t}{\Delta V}$.

AC OPERATING CONDITIONS AND CHARACTERISTICS
(T_A = 0 to +70°C, V_{CC} = 5.0 V ± 10% unless otherwise noted.)

Input Pulse Levels . . . . . 0.8 Volt to 2.2 Volts
Input Rise and Fall Times . . . . . 20 ns
Input and Output Timing Levels . . . . . 2.0 Volts
Output Load . . . . . See Figure 1

Characteristic	Condition	Symbol	MCM27A16 Min	MCM27A16 Max	MCM2716 Min	MCM2716 Max	Units
Address Valid to Output Valid	$\overline{E}$/Progr = G = V_{IL}	t_{AVQV}	–	350	–	450	ns
$\overline{E}$/Progr to Output Valid	(Note 2)	t_{ELQV}	–	350	–	450	
Output Enable to Output Valid	$\overline{E}$/Progr = V_{IL}	t_{GLQV}	–	120	–	120	
$\overline{E}$/Progr to Hi Z Output		t_{EHQZ}	0	100	0	100	
Output Disable to Hi Z Output	$\overline{E}$/Progr = V_{IL}	t_{GHQZ}	0	100	0	100	
Data Hold from Address	$\overline{E}$/Progr = G = V_{IL}	t_{AXDX}	0	–	0	–	

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MCM66700 MCM66710 MCM66714 MCM66720 MCM66730 MCM66734 MCM66740 MCM66750 MCM66751 MCM66760 MCM66770 MCM66780 MCM66790

8192-BIT READ ONLY MEMORIES
ROW SELECT CHARACTER GENERATORS

The MCM66700 is a mask-programmable 8192-bit horizontal-scan (row select) character generator. It contains 128 characters in a 7 X 9 matrix, and has the capability of shifting certain characters that normally extend below the baseline such as j, y, g, p, and q. Circuitry is supplied internally to effectively lower the whole matrix for this type of character—a feature previously requiring external circuitry.

A seven-bit address code is used to select one of the 128 available characters. Each character is defined as a specific combination of logic 1s and 0s stored in a 7 X 9 matrix. When a specific four-bit binary row select code is applied, a word of seven parallel bits appears at the output. The rows can be sequentially selected, providing a nine-word sequence of seven parallel bits per word for each character selected by the address inputs. As the row select inputs are sequentially addressed, the devices will automatically place the 7 X 9 character in one of two preprogrammed positions on the 16-row matrix, with the positions defined by the four row select inputs. Rows that are not part of the character are automatically blanked.

The devices listed are preprogrammed versions of the MCM66700. They contain various sets of characters to meet the requirements of diverse applications. The complete patterns of these devices are contained in this data sheet.

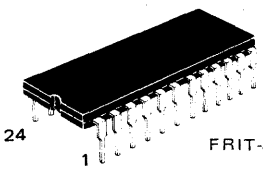
- Fully Static Operation
- Fully TTL Compatible with Three-State Outputs
- CMOS and MPU Compatible, Single ±10% 5 Volt Supply
- Shifted Character Capability
  (Except MCM66720, MCM66730, and MCM66734)
- Maximum Access Time = 350 ns
- 4 Programmable Chip Selects (0, 1, or X)
- Pin-for-Pin Replacement for the MCM6570, Including All Standard Patterns

MOS

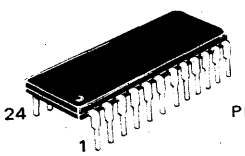
(N-CHANNEL, SILICON-GATE)

8K READ ONLY MEMORIES

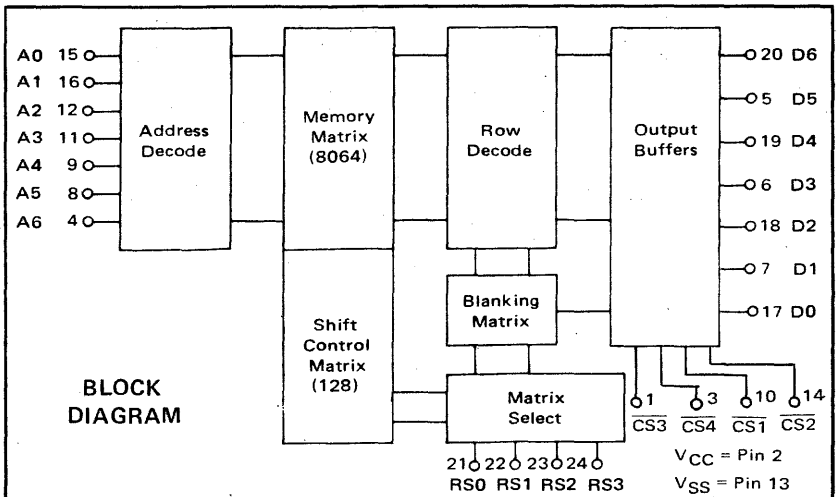
HORIZONTAL-SCAN
CHARACTER GENERATORS
WITH SHIFTED CHARACTERS



C SUFFIX
FRIT-SEAL PACKAGE
CASE 623



P SUFFIX
PLASTIC PACKAGE
CASE 709



BLOCK DIAGRAM

PIN ASSIGNMENT

1	CS3	RS3	24
2	V_{CC}	RS2	23
3	CS4	RS1	22
4	A6	RS0	21
5	D5	D6	20
6	D3	D4	19
7	D1	D2	18
8	A5	D0	17
9	A4	A1	16
10	CS1	A0	15
11	A3	CS2	14
12	A2	V_{SS}	13

This is advance information and specifications are subject to change without notice.

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DS9516
Replaces ADI-464

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DC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature range unless otherwise noted)

RECOMMENDED DC OPERATING CONDITIONS (Referenced to V_{SS})

Parameter	Symbol	Min	Nom	Max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	Vdc
Input Logic "1" Voltage	V_{IH}	2.0	–	V_{CC}	Vdc
Input Logic "0" Voltage	V_{IL}	-0.3	–	0.8	Vdc

DC CHARACTERISTICS

Characteristic	Symbol	Min	Typ	Max	Unit
Input Leakage Current (V_{IH} = 5.5 Vdc, V_{CC} = 4.5 Vdc)	I_{IH}	–	–	2.5	μAdc
Output Low Voltage (Blank) (I_{OL} = 1.6 mAdc)	V_{OL}	0	–	0.4	Vdc
Output High Voltage (Dot) (I_{OH} = -205 μAdc)	V_{OH}	2.4	–	–	Vdc
Power Supply Current	I_{CC}	–	–	80	mAdc
Power Dissipation	P_D	–	200	440	mW

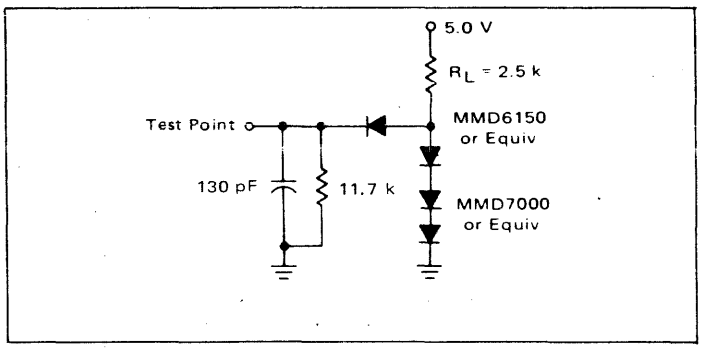
CAPACITANCE (Periodically sampled rather than 100% tested)

Input Capacitance (f = 1.0 MHz)	C_{in}	–	4.0	7.0	pF
Output Capacitance (f = 1.0 MHz)	C_{out}	–	4.0	7.0	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature range unless otherwise noted)

AC TEST LOAD



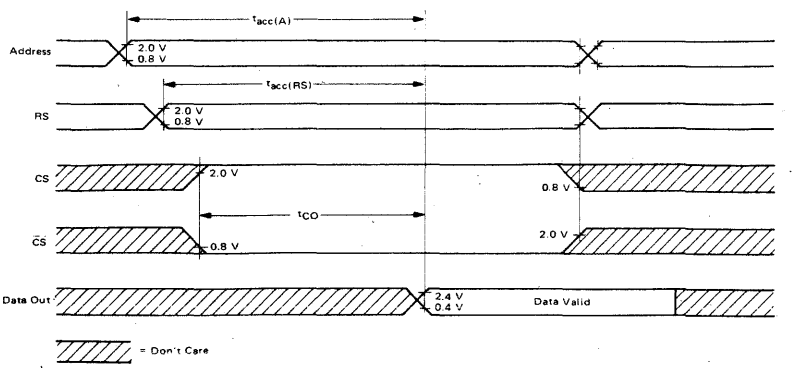
AC TEST CONDITIONS

Condition	Value
Input Pulse Levels	0.8 V to 2.0 V
Input Rise and Fall Times	20 ns
Output Load	1 TTL Gate and C_L = 130 pF

AC CHARACTERISTICS

Characteristic	Symbol	Typ	Max	Unit
Address Access Time	$t_{acc(A)}$	250	350	ns
Row Select Access Time	$t_{acc(RS)}$	250	350	ns
Chip Select to Output Delay	t_{CO}	100	150	ns

TIMING DIAGRAM



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MEMORY OPERATION (Using Positive Logic)

Most positive level = 1, most negative level = 0.

Address

To select one of the 128 characters, apply the appropriate binary code to the Address inputs (A0 through A6).

Row Select

To select one of the rows of the addressed character to appear at the seven output lines, apply the appropriate binary code to the Row Select inputs (RS0 through RS3).

Shifted Characters

These devices have the capability of displaying characters that descend below the bottom line (such as lowercase letters j, y, g, p, and q). Internal circuitry effectively drops the whole matrix for this type of character. Any character can be programmed to occupy either of the two positions in a 7 X 16 matrix. (Shifted characters are not available on MCM66720, MCM66730, or MCM66734.)

Output

For these devices, an output dot is defined as a logic 1 level, and an output blank is defined as a logic 0 level.

Programmable Chip Select

The MCM66700 has four Chip Select inputs that can be programmed with a 1, 0, or don't care (not connected). A don't care must always be the highest chip select pin or pins. All standard patterns have Don't Care Chip Select—except MCM66751.

DISPLAY FORMAT

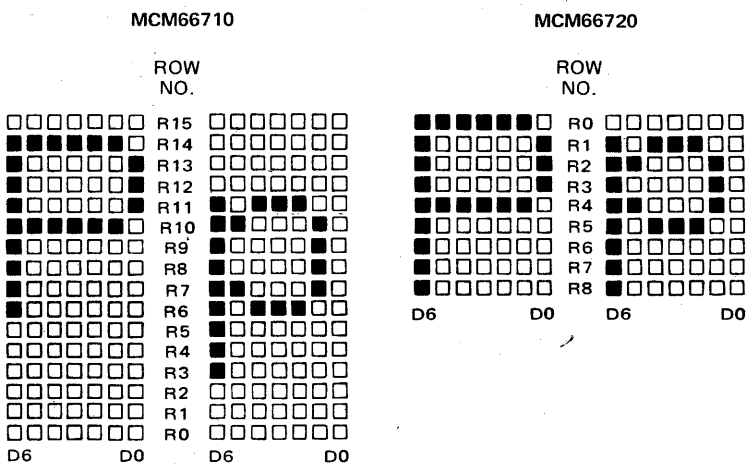
Figure 1 shows the relationship between the logic levels at the row select inputs and the character row at the outputs. The MCM66700 allows the user to locate the basic 7 X 9 font anywhere in the 7 X 16 array. In addition, a shifted font can be placed anywhere in the same 7 X 16 array. For example, the basic MCM66710 font is established in rows R14 through R6. All other rows are automatically blanked. The shifted font is established in rows R11 through R3, with all other rows blanked. Thus, while any one character is contained in a 7 X 9 array, the MCM66710 requires a 7 X 12 array on the CRT screen to contain both normal and descending characters. Other uses of the shift option may require as much as the full 7 X 16 array, or as little as the basic 7 X 9 array (when no shifting occurs, as in the MCM66720).

The MCM66700 can be programmed to be scanned either from bottom to top or from top to bottom. This is achieved through the option of assigning row numbers in ascending or descending count, as long as both the basic font and the shifted font are the same. For example, an up counter will scan the MCM66710 from bottom to top, whereas an up counter will scan the MCM66714 from top to bottom (see Figures 7 and 8 for row designation).

FIGURE 1 – ROW SELECT INPUT CODE AND SAMPLE CHARACTERS FOR MCM66710 AND MCM66720

ROW SELECT TRUTH TABLE

RS3	RS2	RS1	RS0	OUTPUT
0	0	0	0	R0
0	0	0	1	R1
0	0	1	0	R2
0	0	1	1	R3
0	1	0	0	R4
0	1	0	1	R5
0	1	1	0	R6
0	1	1	1	R7
1	0	0	0	R8
1	0	0	1	R9
1	0	1	0	R10
1	0	1	1	R11
1	1	0	0	R12
1	1	0	1	R13
1	1	1	0	R14
1	1	1	1	R15



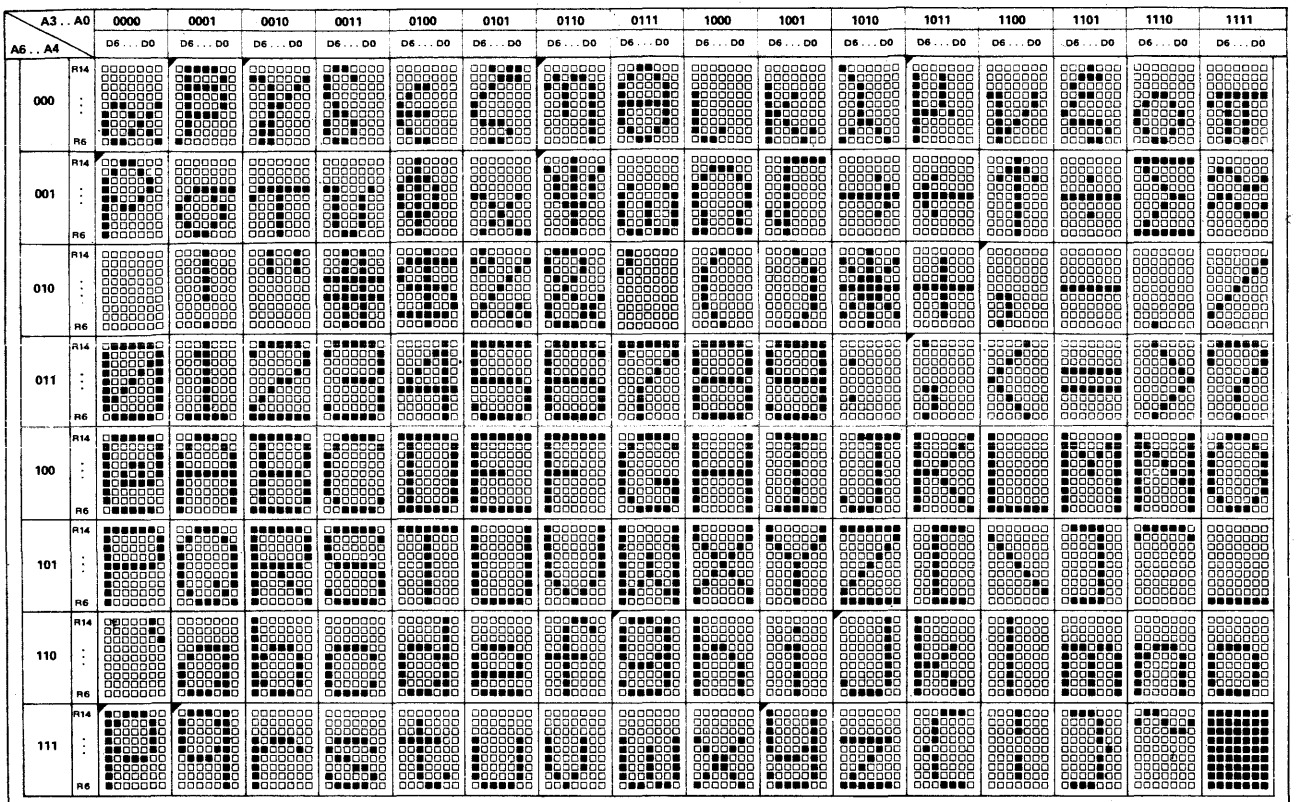
CUSTOM PROGRAMMING FOR MCM66700

By the programming of a single photomask, the customer may specify the content of the MCM66700. Encoding of the photomask is done with the aid of a computer to provide quick, efficient implementation of the custom bit pattern while reducing the cost of implementation.

Information for the custom memory content may be sent to Motorola in the forms specified on the Motorola data sheet.

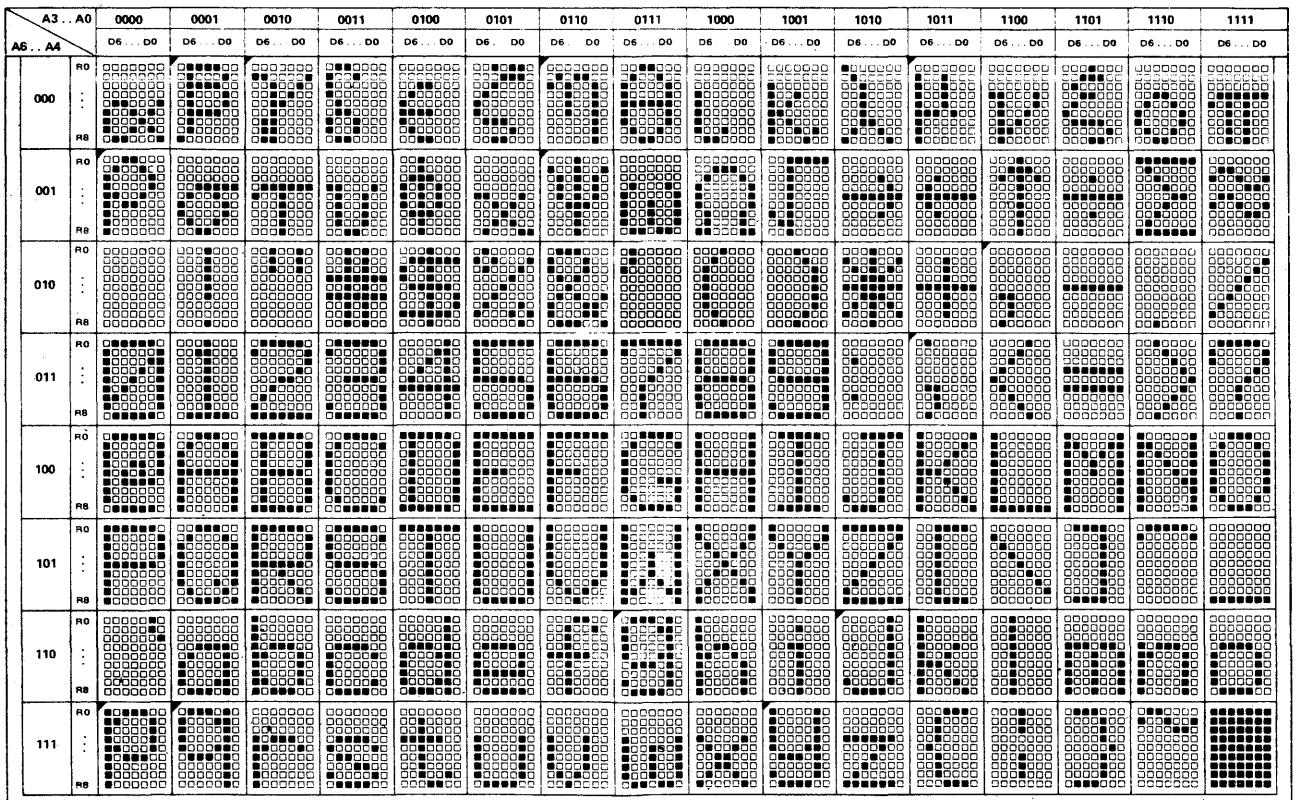
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FIGURE 7 – MCM66710 PATTERN



◤ = Shifted character. The character is shifted three rows to R11 at the top of the font and R3 at the bottom.

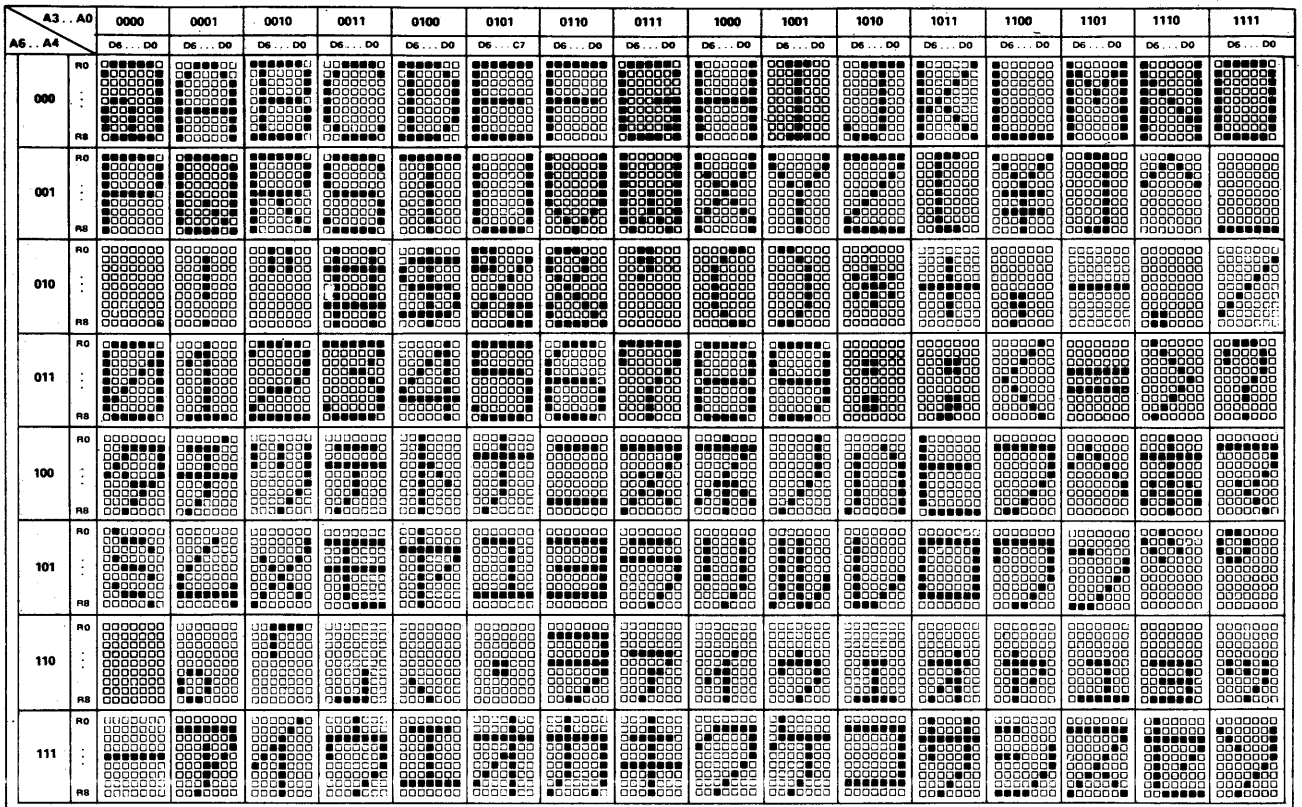
FIGURE 8 – MCM66714 PATTERN



◤ = Shifted character. The character is shifted three rows to R3 at the top of the font and R11 at the bottom.

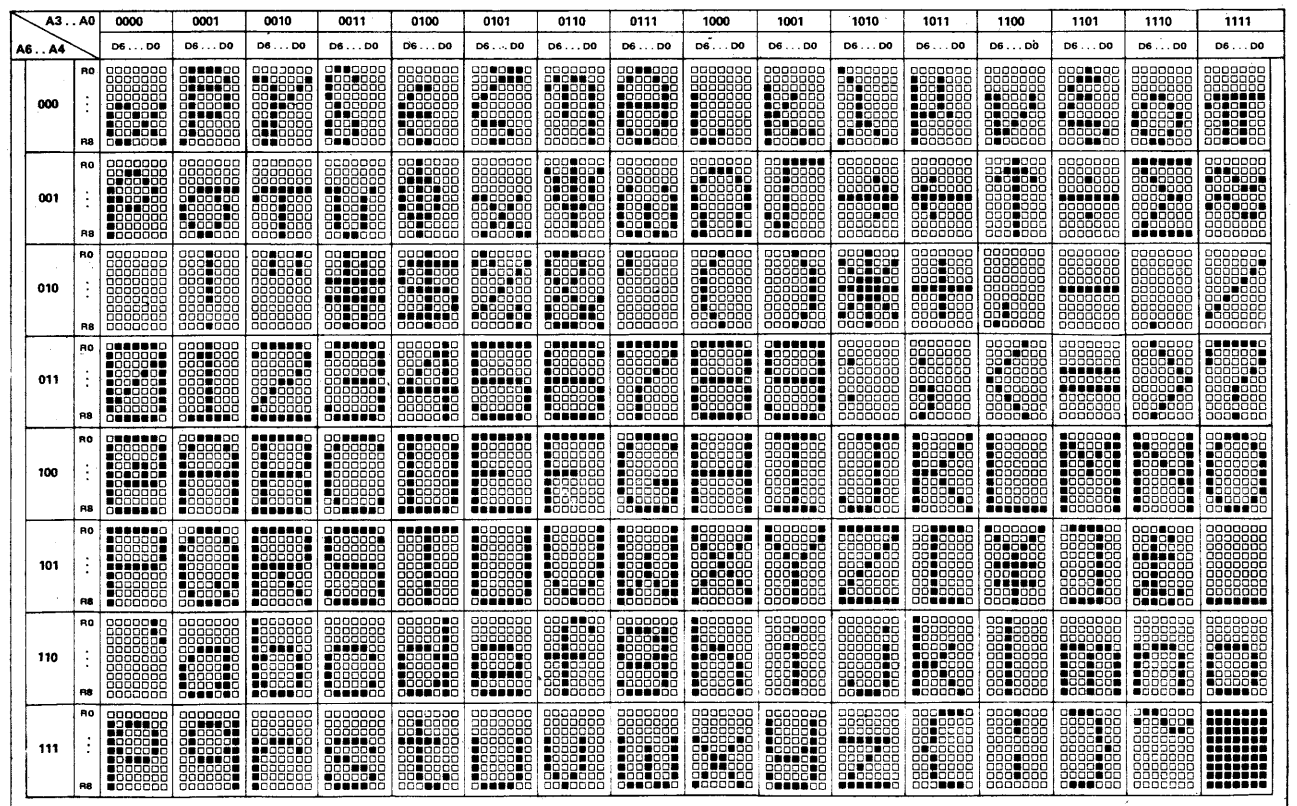
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FIGURE 9 — MCM66734 PATTERN*



*Shifted characters are not used; therefore, SCC = "0" for all characters.

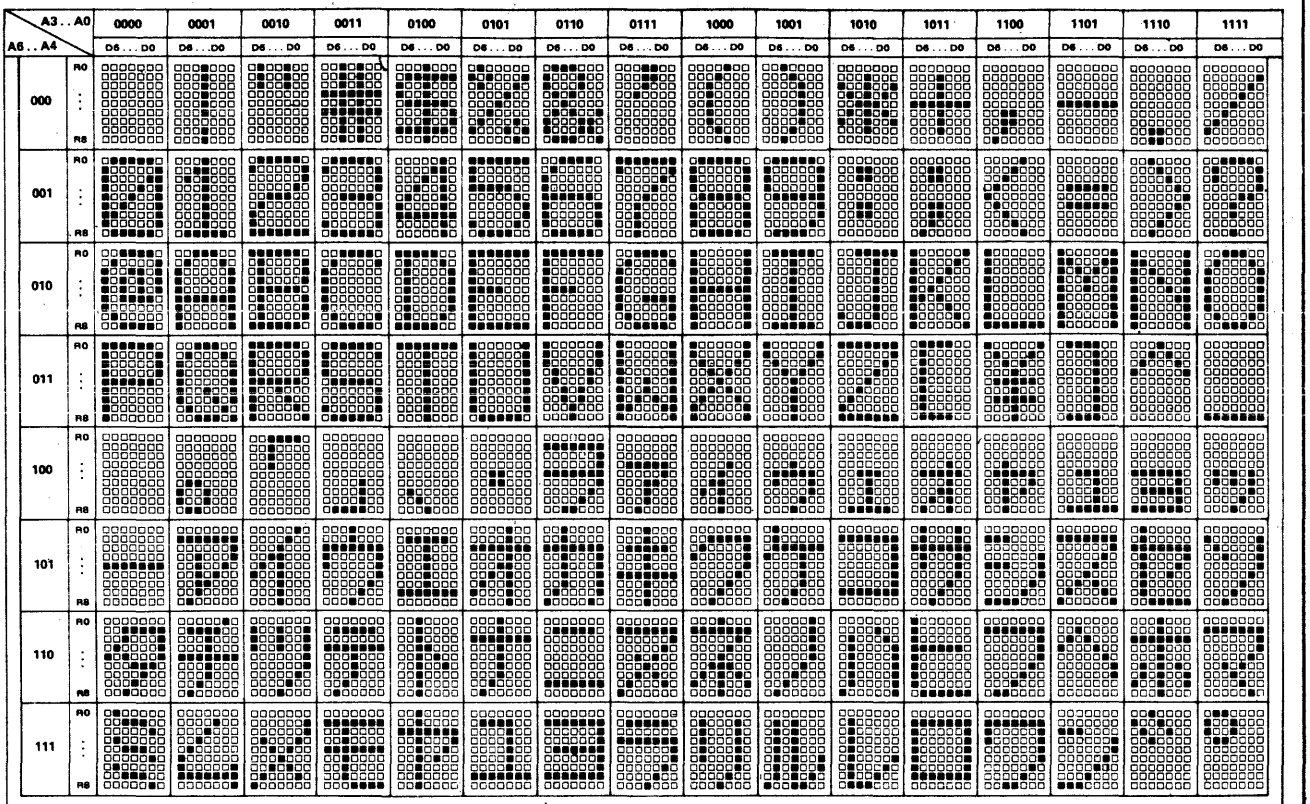
FIGURE 10 — MCM66720 PATTERN**



** Shifted characters are not used.

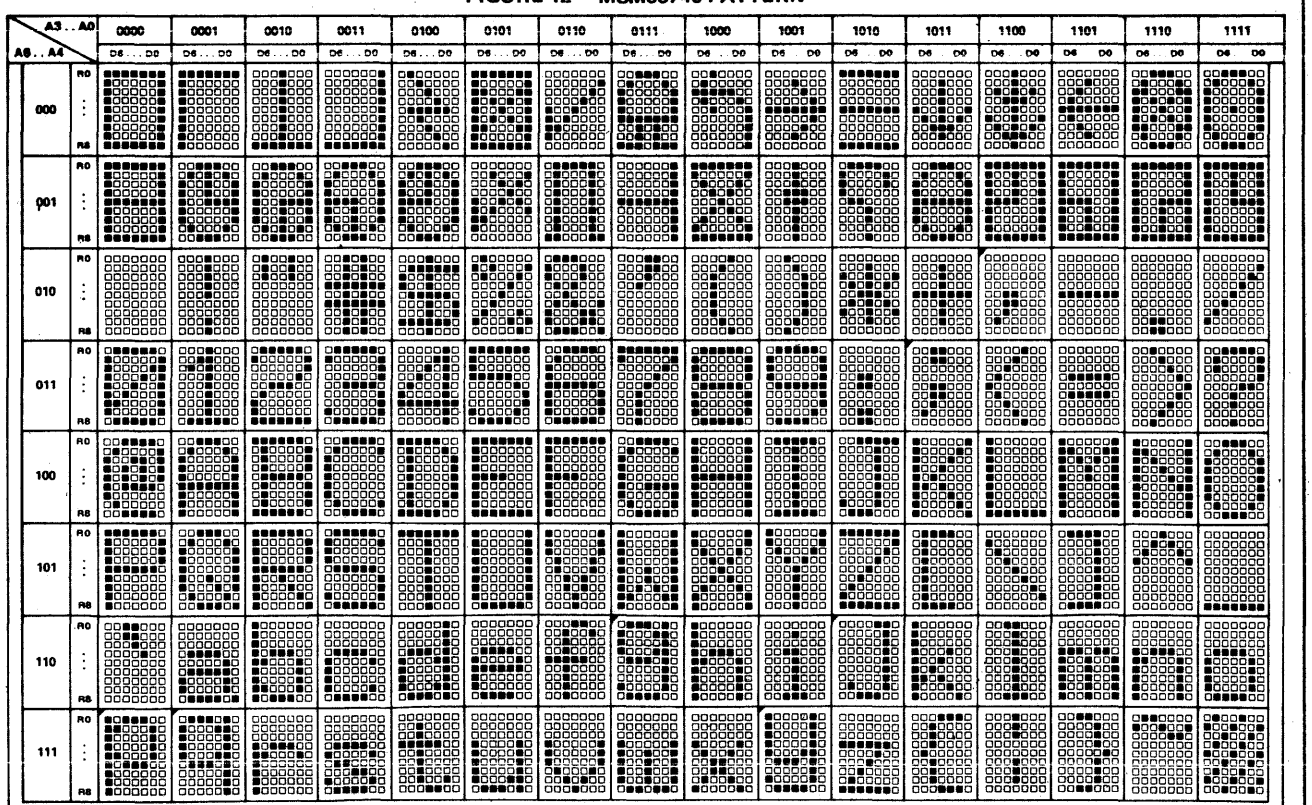
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FIGURE 11 – MCM66730 PATTERN**



** Shifted characters are not used.

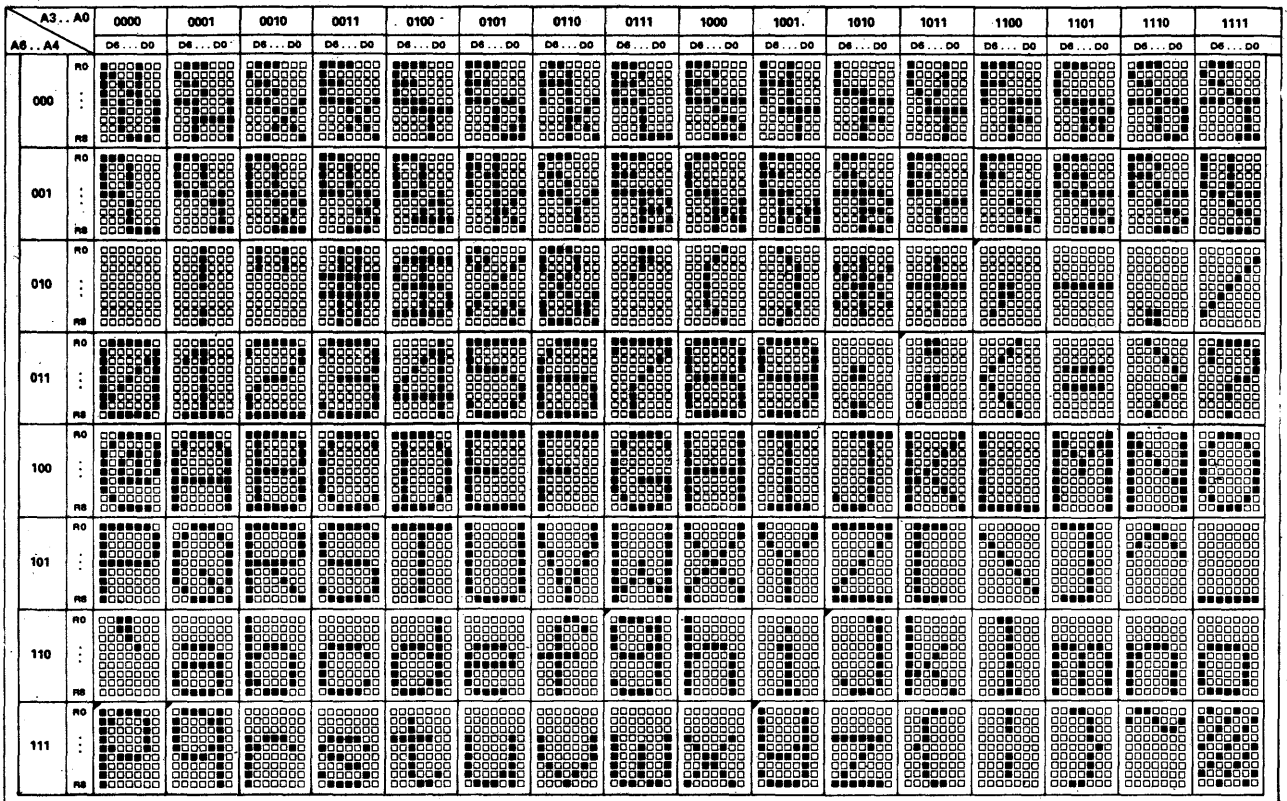
FIGURE 12 – MCM66740 PATTERN



◤ = Shifted character. The character is shifted three rows to R3 at the top of the font and R11 at the bottom.

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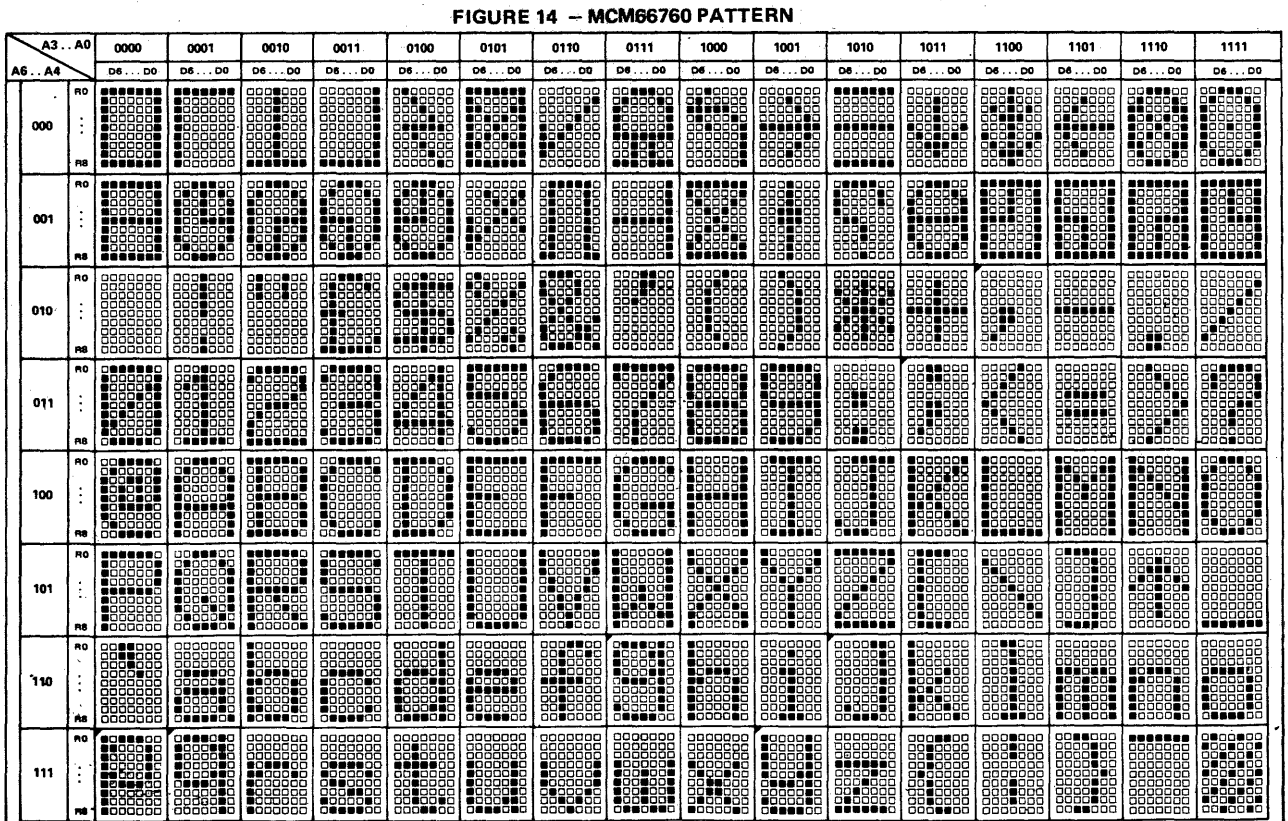
FIGURE 13 – MCM66750 PATTERN



▛ = Shifted character. The character is shifted three rows to R3 at the top of the font and R11 at the bottom.

MCM66751 – Same as MCM66750 except CS1 = 0, CS2 = 0, CS3 = X, and CS4 = X.

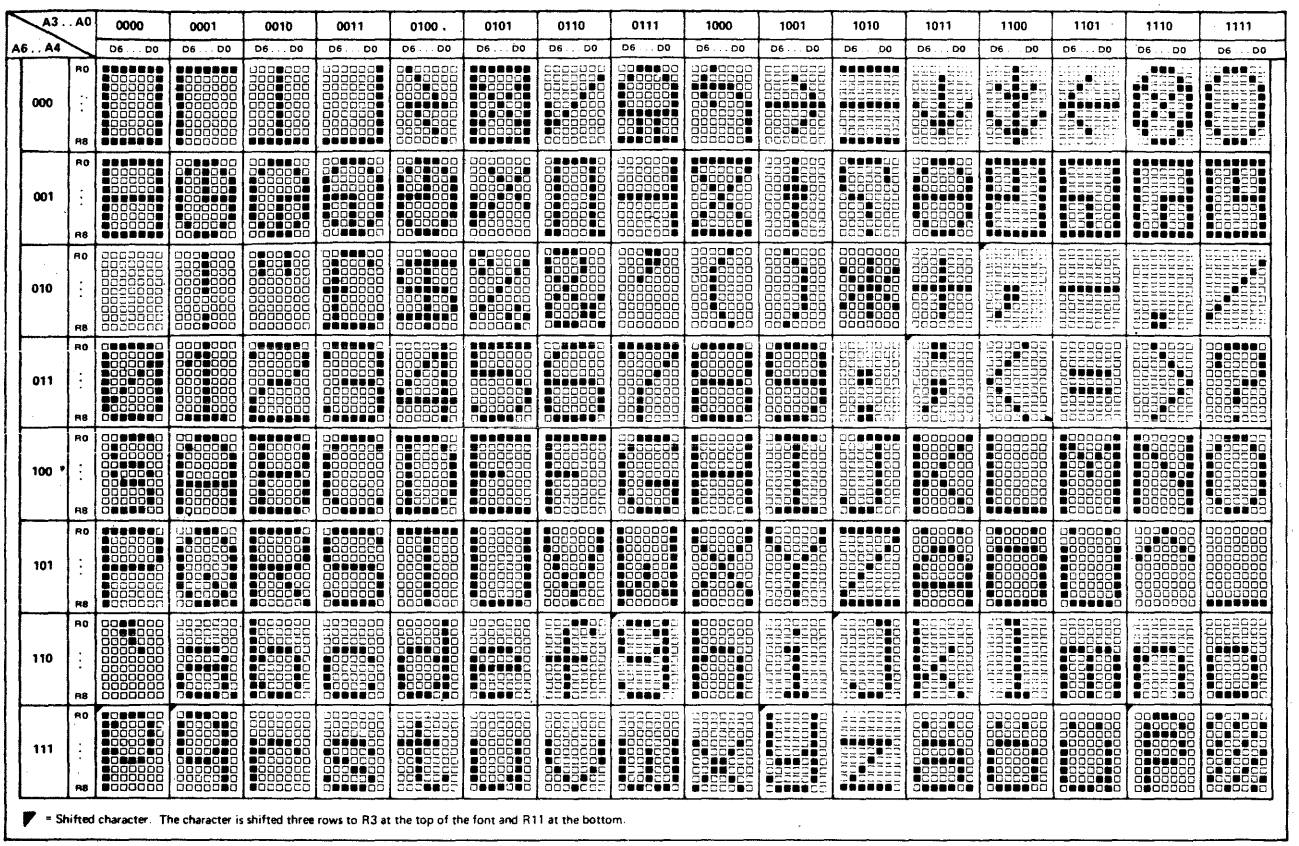
FIGURE 14 – MCM66760 PATTERN



▛ = Shifted character. The character is shifted three rows to R3 at the top of the font and R11 at the bottom.

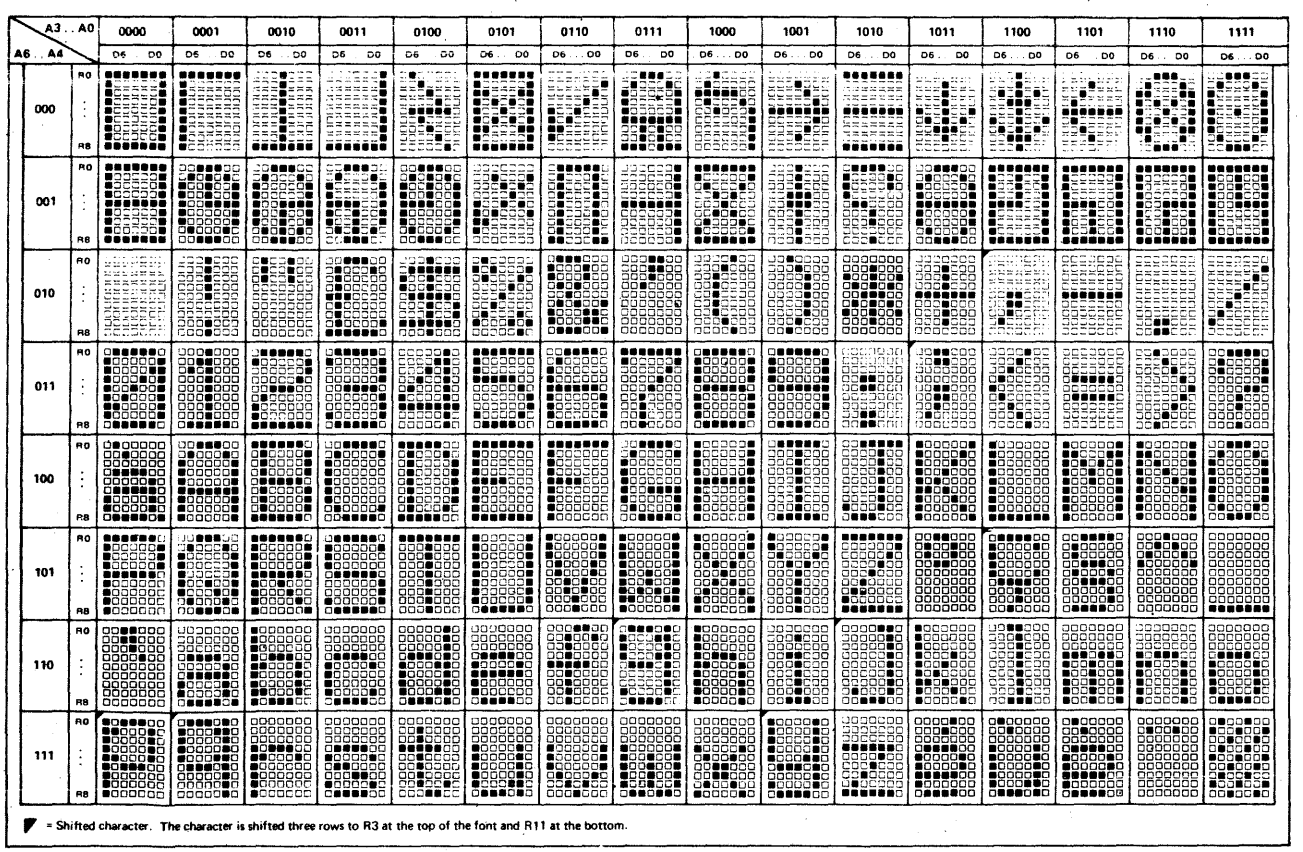
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FIGURE 15 – MCM66770 PATTERN



◤ = Shifted character. The character is shifted three rows to R3 at the top of the font and R11 at the bottom.

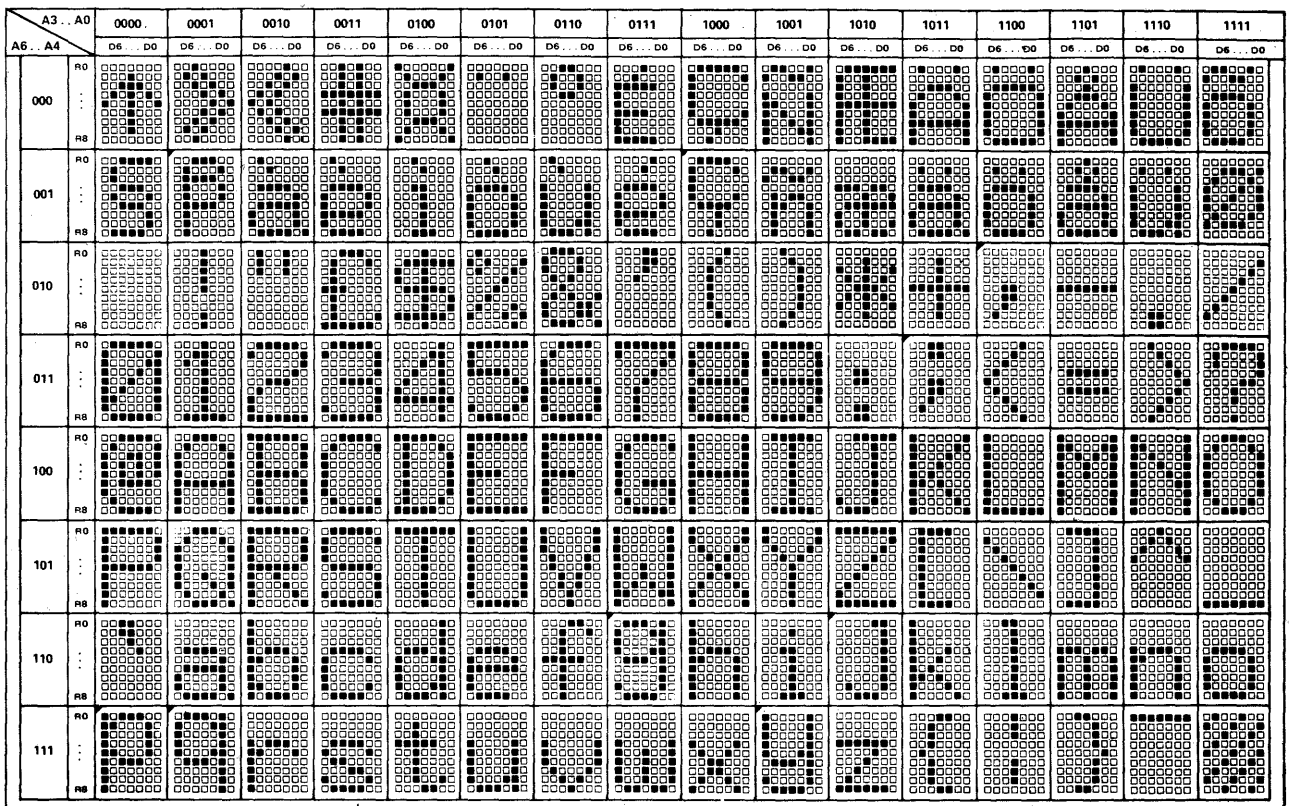
FIGURE 16 – MCM66780 PATTERN



◤ = Shifted character. The character is shifted three rows to R3 at the top of the font and R11 at the bottom.

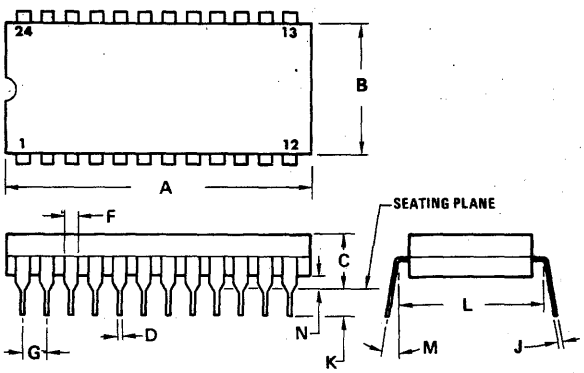
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FIGURE 17 – MCM66790 PATTERN



▛ = Shifted character. The character is shifted three rows to R3 at the top of the font and R11 at the bottom.

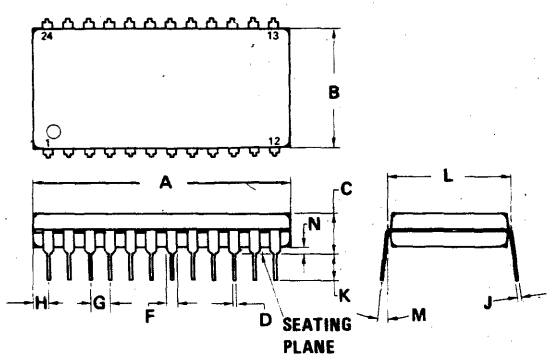
CASE 623-03



DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	31.24	32.26	1.230	1.270
B	12.70	13.72	0.500	0.540
C	4.06	5.59	0.160	0.220
D	0.41	0.51	0.016	0.020
F	1.27	1.52	0.050	0.060
G	2.54 BSC		0.100 BSC	
J	0.20	0.30	0.008	0.012
K	2.29	4.06	0.090	0.160
L	15.24 BSC		0.600 BSC	
M	0°	15°	0°	15°
N	0.51	1.27	0.020	0.050

NOTES:
1. DIM "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
2. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION. (WHEN FORMED PARALLEL)

CASE 709-02



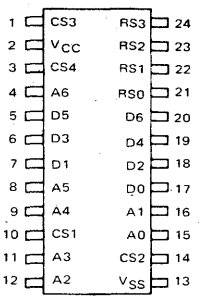
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	31.37	32.13	1.235	1.265
B	13.72	14.22	0.540	0.560
C	3.94	5.08	0.155	0.200
D	0.36	0.56	0.014	0.022
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.78	2.03	0.070	0.080
J	0.20	0.38	0.008	0.015
K	2.92	3.43	0.115	0.135
L	15.24 BSC		0.600 BSC	
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040

NOTES:
1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25 mm (0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

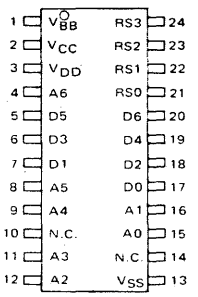
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MCM6570 Series	MCM66700 Equivalent	Description
MCM6571	MCM66710	ASCII, shifted
MCM6571A	MCM66714	ASCII, shifted
MCM6572	MCM66720	ASCII
MCM6573	MCM66730	Japanese
MCM6573A	MCM66734	Japanese
MCM6574	MCM66740	Math Symbols
MCM6575	MCM66750	Alphanumeric Control
MCM6576	MCM66760	British, shifted
MCM6577	MCM66770	German, shifted
MCM6578	MCM66780	French, shifted
MCM6579	MCM66790	European, shifted

MCM66700 Series Pin Assignment



MCM6570 Series Pin Assignment

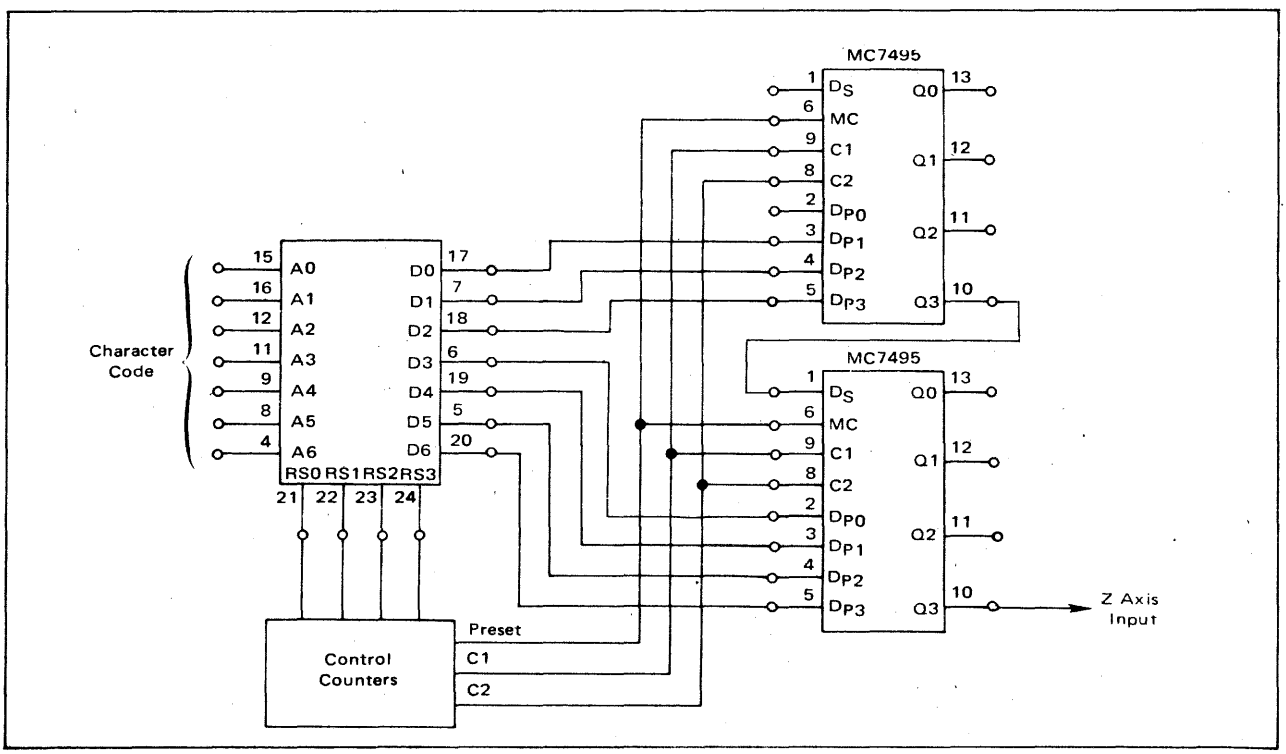


APPLICATIONS INFORMATION

One important application for the MCM66700 series is in CRT display systems (Figure 18). A set of buffer shift registers or random access memories applies a 7-bit character code to the input of the character generator, which then supplies one row of the character according to the count at the four row select inputs. As each row is available, it is put into the TTL MC7495 shift registers. The parallel information in these shift registers is clocked serially out to the Z-axis where it modulates the raster to form the character.

The MCM66700 series require one power supply of +5.0 volts. When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit spikes or glitches on their outputs when the ac power is switched on and off.

FIGURE 18 – CRT DISPLAY APPLICATION USING MCM66710



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MOTOROLA Semiconductors
3501 ED BLUESTEIN BLVD., AUSTIN, TEXAS 78721

MCM4116

16,384-BIT DYNAMIC RANDOM ACCESS MEMORY

MOS

(N-CHANNEL)

16,384-BIT DYNAMIC RANDOM ACCESS MEMORY

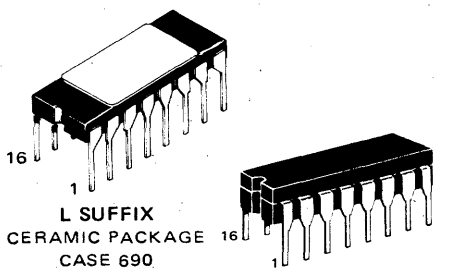
The MCM4116 is a 16,384-bit, high-speed dynamic Random Access Memory designed for high-performance, low-cost applications in mainframe and buffer memories and peripheral storage. Organized as 16,384 one-bit words and fabricated using Motorola's highly reliable N-channel double-polysilicon technology, this device optimizes speed, power, and density tradeoffs.

By multiplexing row and column address inputs, the MCM4116 requires only seven address lines and permits packaging in Motorola's standard 16-pin dual in-line packages. This packaging technique allows high system density and is compatible with widely available automated test and insertion equipment. Complete address decoding is done on chip with address latches incorporated.

All inputs are TTL compatible, and the output is 3-state TTL compatible. The data output of the MCM4116 is controlled by the column address strobe and remains valid from access time until the column address strobe returns to the high state. This output scheme allows higher degrees of system design flexibility such as common input/output operation and two dimensional memory selection by decoding both row address and column address strobes.

The MCM4116 incorporates a one-transistor cell design and dynamic storage techniques, with each of the 128 row addresses requiring a refresh cycle every 2 milliseconds.

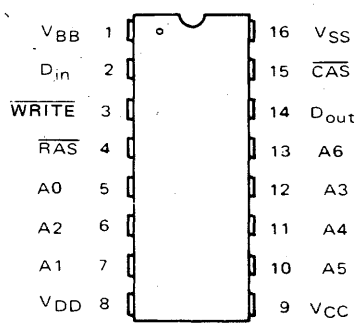
- Flexible Timing with Read-Modify-Write, RAS-Only Refresh, and Page-Mode Capability
- Industry Standard 16-Pin Package
- 16,384 X 1 Organization
- ±10% Tolerance on All Power Supplies
- All Inputs are Fully TTL Compatible
- Three-State Fully TTL-Compatible Output
- Common I/O Capability When Using "Early Write" Mode
- On-Chip Latches for Addresses and Data In
- Low Power Dissipation – 462 mW Active, 20 mW Standby (Max)
- Fast Access Time Options: 150 ns – MCM4116L-15, C-15
  200 ns – MCM4116L-20, C-20
  250 ns – MCM4116L-25, C-25
  300 ns – MCM4116L-30, C-30
- Easy Upgrade from 16-Pin 4K RAMs
- Pin Compatible with 2117, 2116, 6616, μPD416, and 4116



L SUFFIX
CERAMIC PACKAGE
CASE 690

C SUFFIX
FRIT-SEAL PACKAGE
CASE 620

PIN ASSIGNMENT



PIN NAMES

A0–A6	Address Inputs
$\overline{CAS}$	Column Address Strobe
D_{in}	Data In
D_{out}	Data Out
$\overline{RAS}$	Row Address Strobe
$\overline{WRITE}$	Read/Write Input
V_{BB}	Power (-5 V)
V_{CC}	Power (+5 V)
V_{DD}	Power (+12 V)
V_{SS}	Ground

ABSOLUTE MAXIMUM RATINGS (See Note 1)

Rating	Symbol	Value	Unit
Voltage on Any Pin Relative to V_{BB}	V_{in},V_{out}	-0.5 to +20	Vdc
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	–65 to +150	°C
Power Dissipation	P_D	1.0	W
Data Out Current	I_{out}	50	mA

NOTE 1: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit.

This is advance information and specifications are subject to change without notice.

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DS 9513
Second Printing

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DC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature range unless otherwise noted.)

RECOMMENDED OPERATING CONDITIONS

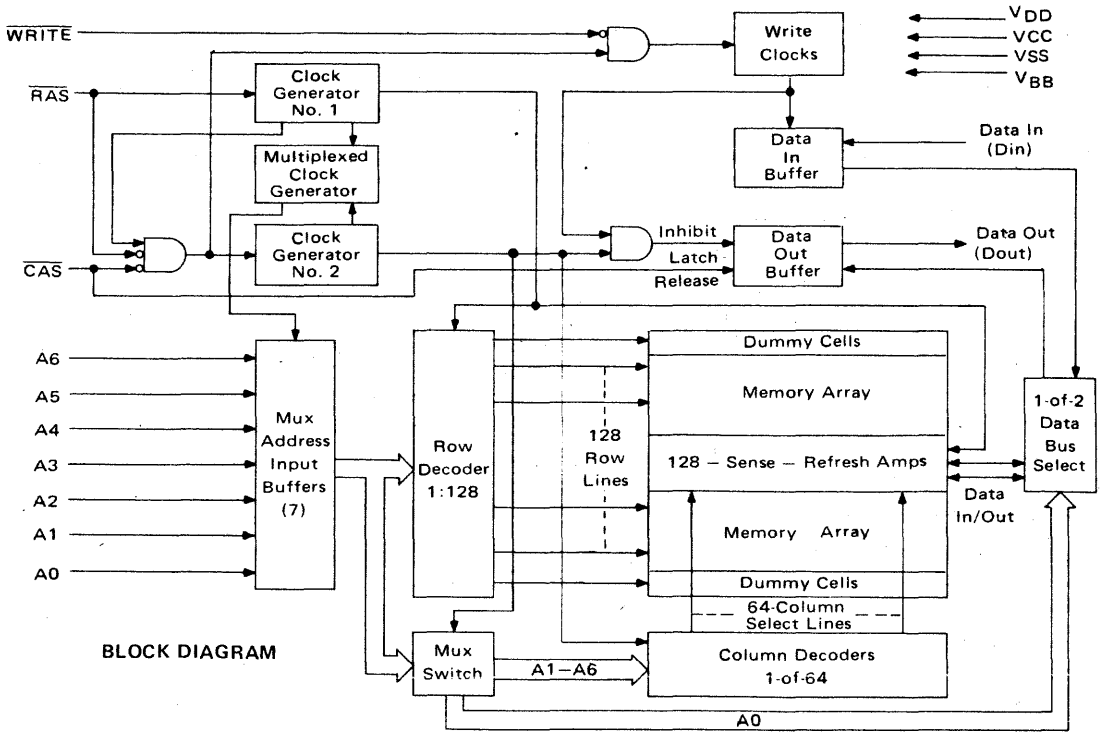
Parameter	Symbol	Min	Typ	Max	Unit	Notes
Supply Voltage	V_{DD}	10.8	12.0	13.2	Vdc	1
	V_{CC}	4.5	5.0	5.5	Vdc	1, 2
	V_{SS}	0	0	0	Vdc	1
	V_{BB}	-4.5	-5.0	-5.5	Vdc	1
Logic 1 Voltage, $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$	V_{IHC}	2.7	–	7.0	Vdc	1
Logic 1 Voltage, all inputs except $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$	V_{IH}	2.4	–	7.0	Vdc	1
Logic 0 Voltage, all inputs	V_{IL}	-1.0	–	0.8	Vdc	1

DC CHARACTERISTICS (V_{DD} = 12 V ± 10%, V_{CC} = 5.0 V ± 10%, V_{BB} = -5.0 V ± 10%, V_{SS} = 0 V, T_A = 0 to 70°C.)

Characteristic	Symbol	Min	Max	Units	Notes
Average V_{DD} Power Supply Current	I_{DD1}	–	35	mA	4
V_{CC} Power Supply Current	I_{CC}	–	–	mA	5
Average V_{BB} Power Supply Current	$I_{BB1,3}$	–	200	μA	
Standby V_{BB} Power Supply Current	I_{BB2}	–	100	μA	
Standby V_{DD} Power Supply Current	I_{DD2}	–	1.5	mA	6
Average V_{DD} Power Supply Current during "$\overline{RAS}$ only" cycles	I_{DD3}	–	27	mA	4
Input Leakage Current (any input)	$I_{I(L)}$	–	10	μA	
Output Leakage Current	$I_{O(L)}$	–	10	μA	6, 7
Output Logic 1 Voltage @ I_{out} = -5 mA	V_{OH}	2.4	–	Vdc	2
Output Logic 0 Voltage @ I_{out} = 4.2 mA	V_{OL}	–	0.4	Vdc	

NOTES:

1. All voltages referenced to V_{SS}. V_{BB} must be applied before and removed after other supply voltages.
2. Output voltage will swing from V_{SS} to V_{CC} under open circuit conditions. For purposes of maintaining data in power-down mode, V_{CC} may be reduced to V_{SS} without affecting refresh operations. V_{OH}(min) specification is not guaranteed in this mode.
3. Several cycles are required after power-up before proper device operation is achieved. Any 8 cycles which perform refresh are adequate.
4. Current is proportional to cycle rate; maximum current is measured at the fastest cycle rate.
5. I_{CC} depends upon output loading. The V_{CC} supply is connected to the output buffer only.
6. Output is disabled (open-circuit) and $\overline{RAS}$ and $\overline{CAS}$ are both at a logic 1.
7. $0 V \leq V_{out} \leq +5.5 V$.
8. Capacitance measured with a Boonton Meter or effective capacitance calculated from the equation: $C = \frac{I\Delta_t}{\Delta V}$



BLOCK DIAGRAM

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AC OPERATING CONDITIONS AND CHARACTERISTICS (See Notes 3, 9, 14)
(Read, Write, and Read-Modify-Write Cycles)

RECOMMENDED AC OPERATING CONDITIONS

(V_{DD} = 12 V ±10%, V_{CC} = 5.0 V ±10%, V_{BB} = −5.0 V ±10%, V_{SS} = 0 V, T_A = 0 to 70°C.)

Parameter	Symbol	MCM4116-15		MCM4116-20		MCM4116-25		MCM4116-30		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RC}	375	–	375	–	410	–	480	–	ns	
Read Write Cycle Time	t_{RWC}	375	–	375	–	515	–	660	–	ns	
Access Time from Row Address Strobe	t_{RAC}	–	150	–	200	–	250	–	300	ns	10, 12
Access Time from Column Address Strobe	t_{CAC}	–	90	–	135	–	165	–	200	ns	11, 12
Output Buffer and Turn-off Delay	t_{OFF}	0	40	0	50	0	60	0	60	ns	
Row Address Strobe Precharge Time	t_{RP}	100	–	120	–	150	–	180	–	ns	
Row Address Strobe Pulse Width	t_{RAS}	150	10,000	200	10,000	250	10,000	300	10,000	ns	
Column Address Strobe Pulse Width	t_{CAS}	90	10,000	135	10,000	165	10,000	200	10,000	ns	
Row to Column Strobe Lead Time	t_{RCD}	20	60	25	65	35	85	60	100	ns	13
Row Address Setup Time	t_{ASR}	0	–	0	–	0	–	0	–	ns	
Row Address Hold Time	t_{RAH}	20	–	25	–	35	–	60	–	ns	
Column Address Setup Time	t_{ASC}	−10	–	−10	–	−10	–	−10	–	ns	
Column Address Hold Time	t_{CAH}	45	–	55	–	75	–	100	–	ns	
Column Address Hold Time Referenced to $\overline{RAS}$	t_{AR}	105	–	120	–	160	–	200	–	ns	
Transition Time (Rise and Fall)	t_T	3.0	35	3.0	50	3.0	50	3.0	50	ns	14
Read Command Setup Time	t_{RCS}	0	–	0	–	0	–	0	–	ns	
Read Command Hold Time	t_{RCH}	0	–	0	–	0	–	0	–	ns	
Write Command Hold Time	t_{WCH}	45	–	55	–	75	–	100	–	ns	
Write Command Hold Time Referenced to $\overline{RAS}$	t_{WCR}	105	–	120	–	160	–	200	–	ns	
Write Command Pulse Width	t_{WP}	45	–	55	–	75	–	100	–	ns	
Write Command to Row Strobe Lead Time	t_{RWL}	60	–	80	–	100	–	180	–	ns	
Write Command to Column Strobe Lead Time	t_{CWL}	60	–	80	–	100	–	180	–	ns	
Data in Setup Time	t_{DS}	0	–	0	–	0	–	0	–	ns	15
Data in Hold Time	t_{DH}	45	–	55	–	75	–	100	–	ns	15
Data in Hold Time Referenced to $\overline{RAS}$	t_{DHR}	105	–	120	–	160	–	200	–	ns	
Column to Row Strobe Precharge Time	t_{CRP}	−20	–	−20	–	−20	–	−20	–	ns	
$\overline{RAS}$ Hold Time	t_{RSH}	100	–	135	–	165	–	200	–	ns	
Refresh Period	t_{RFSH}	–	2.0	–	2.0	–	2.0	–	2.0	ms	
$\overline{WRITE}$ Command Setup Time	t_{WCS}	−20	–	−20	–	−20	–	−20	–	ns	
$\overline{CAS}$ to $\overline{WRITE}$ Delay	t_{CWD}	70	–	95	–	125	–	180	–	ns	16
$\overline{RAS}$ to $\overline{WRITE}$ Delay	t_{RWD}	120	–	160	–	210	–	280	–	ns	16
$\overline{CAS}$ Precharge Time (Page mode cycle only)	t_{CP}	60	–	80	–	100	–	100	–	ns	
Page Mode Cycle Time	t_{PC}	170	–	225	–	275	–	325	–	ns	
$\overline{CAS}$ Hold Time	t_{CSH}	150	–	200	–	250	–	300	–	ns	

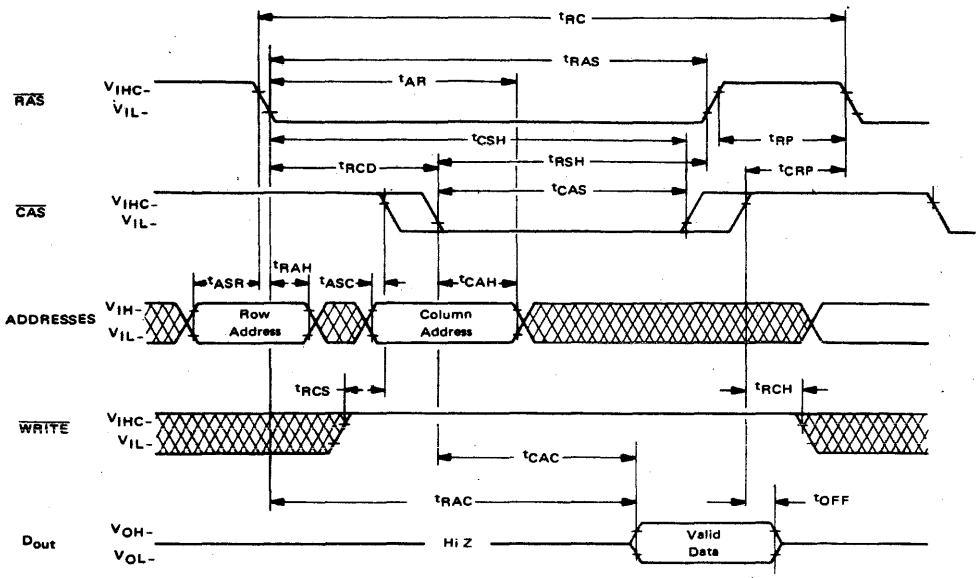
Parameter	Symbol	Typ	Max	Units	Notes
Input Capacitance (A0-A5), D_{in}	C_{I1}	4.0	5.0	pF	9
Input Capacitance $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$	C_{I2}	8.0	10	pF	9
Output Capacitance (D_{out})	C_o	5.0	7.0	pF	7, 9

NOTES: (continued)

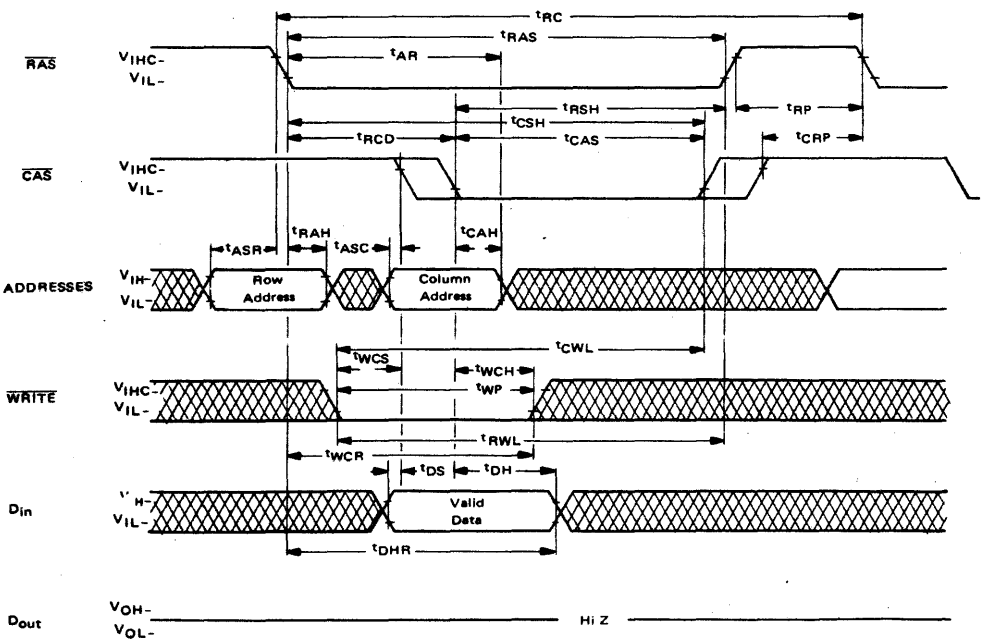
9. AC measurements assume t_T = 5.0 ns.
10. Assumes that $t_{RCD} + t_T \leq t_{RCD}$ (max).
11. Assumes that $t_{RCD} + t_T \geq t_{RCD}$ (max).
12. Measured with a load circuit equivalent to 2 TTL loads and 100 pF.
13. Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met. t_{RCD} (max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
14. V_{IHC} (min) or V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transistion times are measured between V_{IHC} or V_{IH} and V_{IL}.
15. These parameters are referenced to $\overline{CAS}$ leading edge in random write cycles and to $\overline{WRITE}$ leading edge in delayed write or read-modify-write cycles.
16. t_{WCS}, t_{CWD} and t_{RWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only: If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; If $t_{CWD} \geq t_{CWD}$ (min) and $t_{RWD} \geq t_{RWD}$ (min), the cycle is a read-write cycle and the data out will contain data read from the selected cell; If neither of the above sets of conditions is satisfied the condition of the data out (at access time) is indeterminate.

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READ CYCLE TIMING

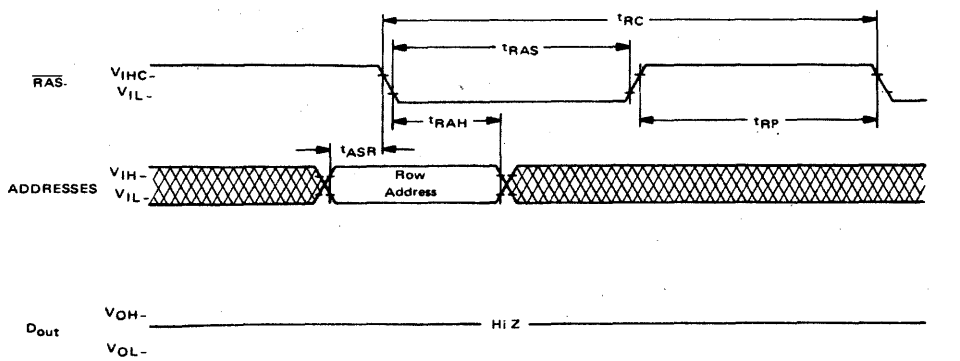


WRITE CYCLE TIMING



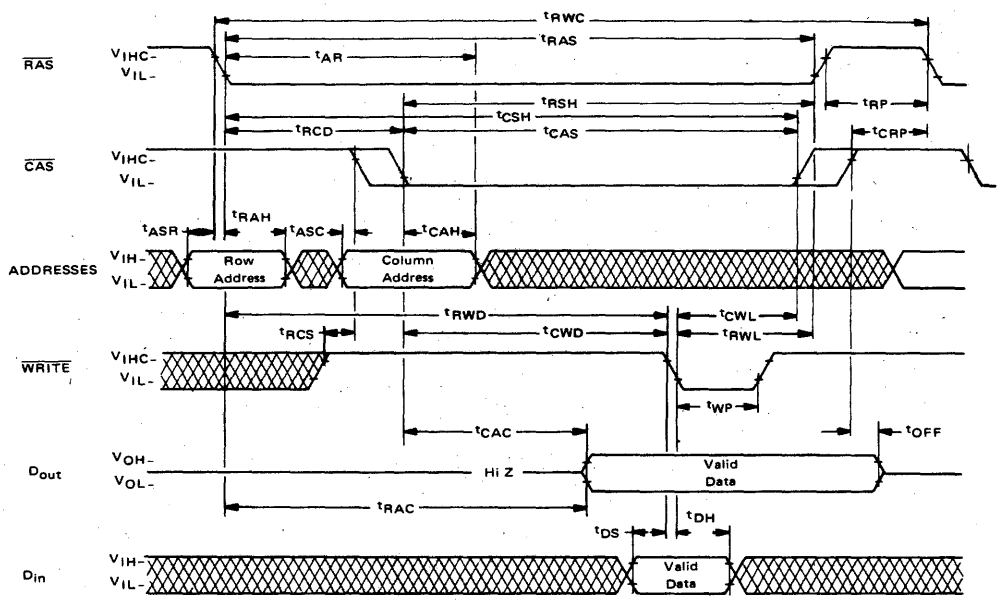
RAS ONLY REFRESH TIMING

Note: $\overline{CAS}$ = V_{IHC}, $\overline{WRITE}$ = Don't Care

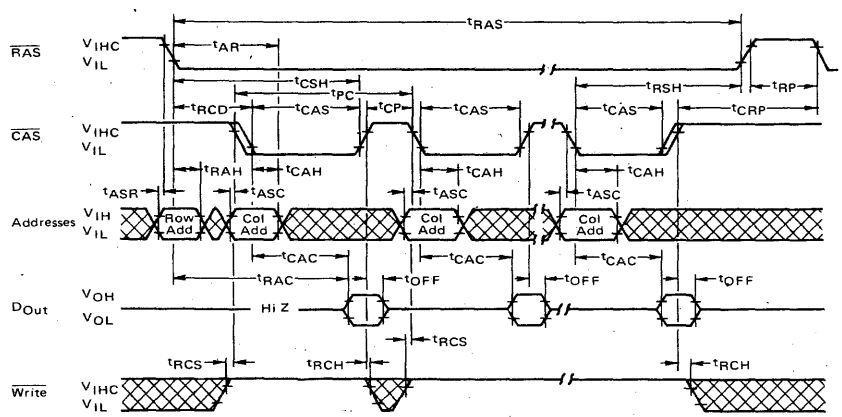


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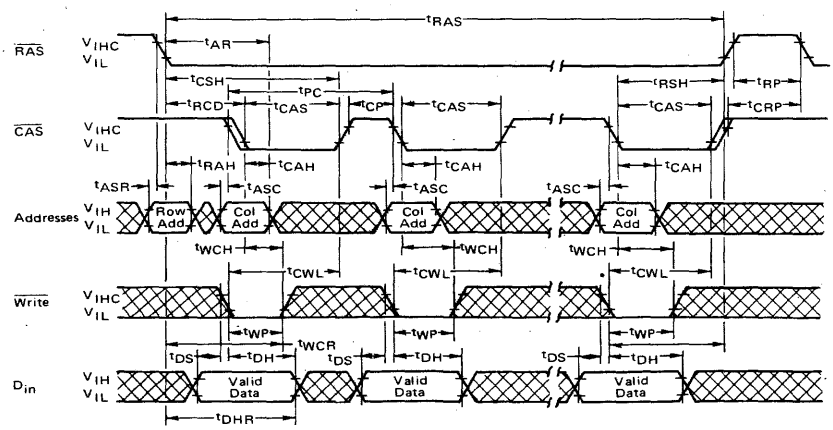
READ-WRITE/READ-MODIFY-WRITE CYCLE



PAGE MODE READ CYCLE



PAGE MODE WRITE CYCLE



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MOTOROLA
Semiconductors
3501 ED BLUESTEIN BLVD., AUSTIN, TEXAS 78721

MCM2147

Advance Information

MOS

(N-CHANNEL, SILICON-GATE)

4096-BIT STATIC RANDOM ACCESS MEMORY

4096-BIT STATIC RANDOM ACCESS MEMORY

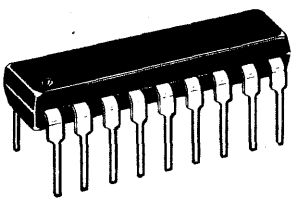
The MCM2147 is a 4096-bit static random access memory organized as 4096 words by 1-bit using Motorola's N-channel silicon-gate MOS technology. It uses a design approach which provides the simple timing features associated with fully static memories and the reduced standby power associated with semi-static and dynamic memories. This means low standby power without the need for clocks, nor reduced data rates due to cycle times that exceed access times.

$\overline{E}$ controls the power-down feature. It is not a clock but rather a chip select that affects power consumption. In less than a cycle time after $\overline{E}$ goes high, deselect mode, the part automatically reduces its power requirements and remains in this low-power standby mode as long as $\overline{E}$ remains high. This feature results in system power savings as great as 85% in larger systems, where most devices are deselected. The automatic power-down feature causes no performance degradation.

The MCM2147 is in an 18 pin dual in-line package with the industry standard pinout. It is TTL compatible in all respects. The data out has the same polarity as the input data. A data input and a separate three-state output provide flexibility and allow easy OR-ties.

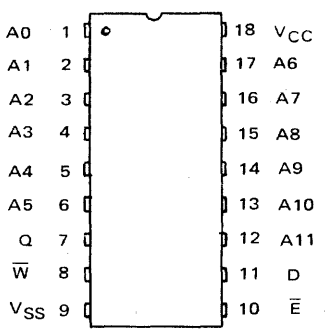
- Fully Static Memory — No Clock or Timing Strobe Required
- Single ±10% +5 V Supply
- High Density 18 Pin Package
- Automatic Power-Down
- Directly TTL Compatible—All Inputs and Outputs
- Separate Data Input and Output
- Three-State Output
- Access Time — MCM2147-55 = 55 ns max
  MCM2147-70 = 70 ns max
- Cycle Time — MCM2147-55 = 55 ns min
  MCM2147-70 = 70 ns min

C SUFFIX
FRIT-SEAL
CERAMIC PACKAGE
also available

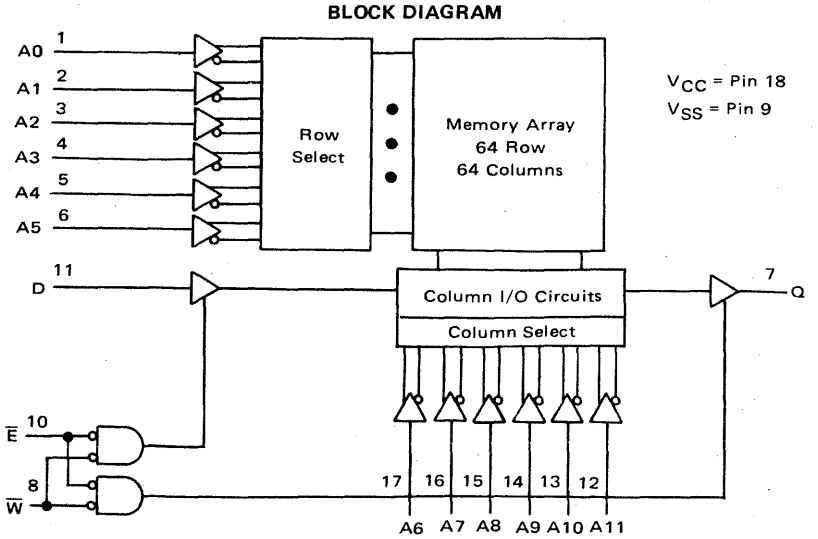


P SUFFIX
PLASTIC PACKAGE
CASE 707

PIN ASSIGNMENT



BLOCK DIAGRAM



PIN NAMES

A0-A11	Address Input
$\overline{W}$	Write Enable
$\overline{E}$	Chip Enable
D	Data Input
Q	Data Output
V_{CC}	Power (+5 V)
V_{SS}	Ground

TRUTH TABLE

$\overline{E}$	$\overline{W}$	Mode	Output	Power
H	X	Not Selected	High Z	Standby
L	L	Write	High Z	Active
L	H	Read	Data Out	Active

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DC OPERATING CONDITIONS AND CHARACTERISTICS

(T_A = 0 to +70°C, V_{CC} = 5.0 V ±10% unless otherwise noted.)

RECOMMENDED DC OPERATING CONDITIONS

Parameter	Symbol	MCM2147-55			MCM2147-70			Unit
		Min	Typ	Max	Min	Typ	Max	
Input Load Current (All Input Pins, V_{in} = 0 to 5.5 V)	I_{IL}	–	0.01	10	–	0.01	10	μA
Output Leakage Current ($\overline{E}$ = 2.0 V, V_{out} = 0 V to 5.5 V)	$\|I_{OL}\|$	–	0.1	50	–	0.1	50	μA
Power Supply Current ($\overline{E}$ = V_{IL}, Outputs Open, T_A = 25°C)	I_{CC1}	–	120	170	–	100	150	mA
Power Supply Current ($\overline{E}$ = V_{IL}, Outputs Open, T_A = 0°C)	I_{CC2}	–	–	180	–	–	160	mA
Standby Current ($\overline{E}$ = V_{IH})	I_{SB}	–	15	30	–	10	20	mA
Input Low Voltage	V_{IL}	-0.3	–	0.8	-0.3	–	0.8	V
Input High Voltage	V_{IH}	2.0	–	6.0	2.0	–	6.0	V
Output Low Voltage I_{OL} = 12 mA	V_{OL}	–	–	0.4	–	–	0.4	V
Output High Voltage I_{OH} = -4.0 mA	V_{OH}	2.4	–	–	2.4	–	–	V

Typical values are for T_A = 25°C and V_{CC} = +5 V

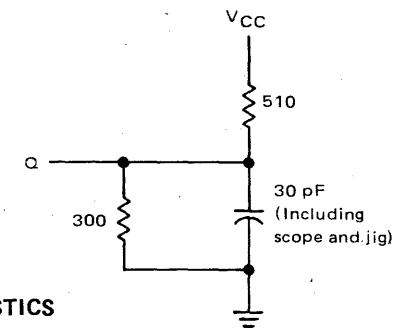
CAPACITANCE

(f = 1.0 MHz, T_A = 25°C, periodically sampled rather than 100% tested.)

Characteristic	Symbol	Max	Unit
Input Capacitance (V_{in} = 0 V)	C_{in}	5.0	pF
Output Capacitance (V_{out} = 0 V)	C_{out}	10	pF

Capacitance measured with a Boonton Meter or effective capacitance calculated from the equation: $C = \frac{I\Delta_t}{\Delta V}$.

FIGURE 1 – OUTPUT LOAD



AC OPERATING CONDITIONS AND CHARACTERISTICS

Read, Write Cycles

RECOMMENDED AC OPERATING CONDITIONS (T_A = 0 to 70°C, V_{CC} = 5.0 V ±10%)

Parameter	Symbol	MCM2147-55		MCM2147-70		Units
		Min	Max	Min	Max	
Address Valid to Address Don't Care (Cycle Time when Chip Enable is held Active)	T_{AVAX}	55	–	70	–	ns
Chip Enable Low to Chip Enable High	t_{ELEH}	55	–	70	–	
Address Valid to Output Valid (Access)	t_{AVQV}	–	55	–	70	
Chip Enable Low to Output Valid (Access)	t_{ELQV}	–	55	–	70	
Address Valid to Output Invalid	t_{AVQX}	10	–	10	–	
Chip Enable Low to Output Invalid	t_{ELQX}	10	–	10	–	
Chip Enable High to Output High Z	t_{EHQZ}	0	30	0	30	
Chip Selection to Power Up Time	t_{PU}	0	–	0	–	
Chip Deselection to Power Down Time	t_{PD}	0	40	0	50	
Address Valid to Chip Enable Low (Address Setup)	t_{AVEL}	0	–	0	–	
Chip Enable Low to Write High	t_{ELWH}	45	–	55	–	
Address Valid to Write High	t_{AVWH}	45	–	55	–	
Address Valid to Write Low (Address Setup)	t_{AVWL}	5.0	–	5.0	–	
Write Low to Write High (Write Pulse Width)	t_{WLWH}	35	–	40	–	
Write High to Address Don't Care	t_{WHAX}	10	–	15	–	
Data Valid to Write High	t_{DVWH}	25	–	30	–	
Write High to Data Don't Care (Data Hold)	t_{WHDX}	10	–	10	–	
Write Low to Output High Z	t_{WLQZ}	0	25	0	30	
Write High to Output Valid	t_{WHQV}	0	25	0	30	

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TIMING PARAMETER ABBREVIATIONS

t X X X X

- signal name from which interval is defined
- transition direction for first signal
- signal name to which interval is defined
- transition direction for second signal

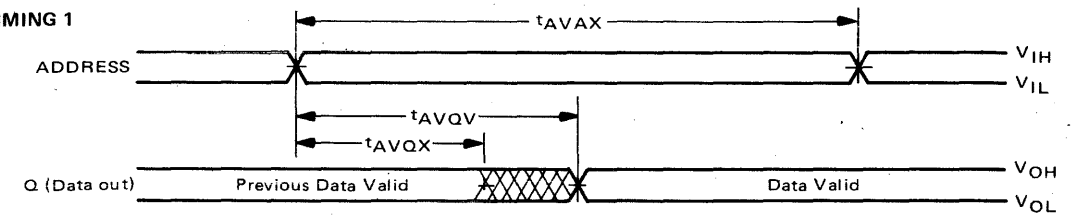
The transition definitions used in this data sheet are:

- H = transition to high
- L = transition to low
- V = transition to valid
- X = transition to invalid or don't care
- Z = transition to off (high impedance)

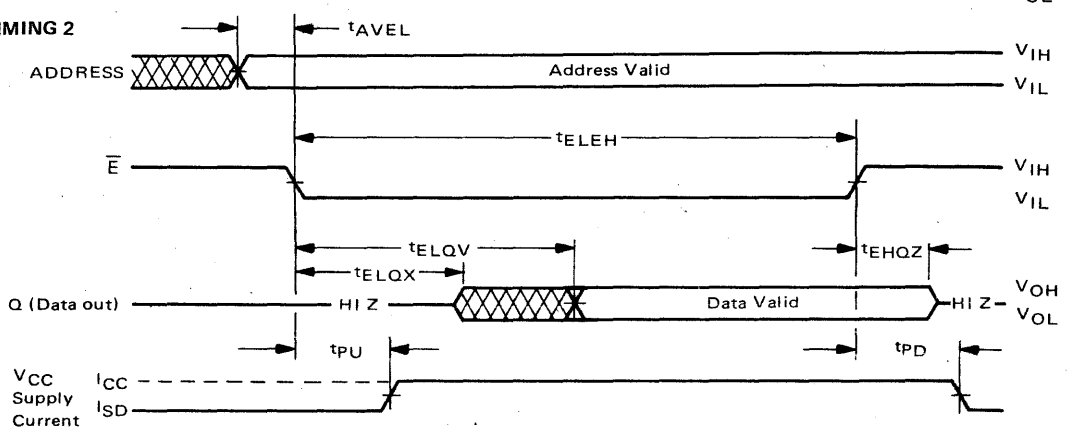
TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

READ CYCLE TIMING 1
($\overline{E}$ Held Low)

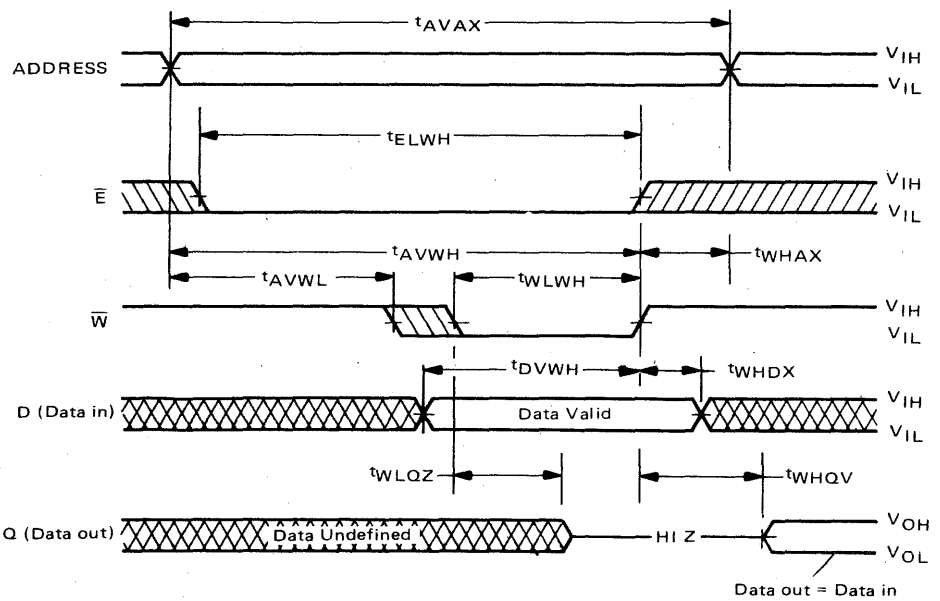


READ CYCLE TIMING 2



NOTE: $\overline{W}$ is high for Read Cycles.

WRITE CYCLE TIMING



WAVEFORMS

Waveform Symbol	Input	Output
———	MUST BE VALID	WILL BE VALID
▨	CHANGE FROM H TO L	WILL CHANGE FROM H TO L
▨	CHANGE FROM L TO H	WILL CHANGE FROM L TO H
▨	DON'T CARE: ANY CHANGE PERMITTED	CHANGING: STATE UNKNOWN
—	—	HIGH IMPEDANCE

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DEVICE DESCRIPTION

The MCM2147 is produced with a high-performance MOS technology which combines on-chip substrate bias generation with device scaling to achieve high speed. The speed-power product of this process is about four times better than earlier MOS processes.

This gives the MCM2147 its high speed, low power and ease-of-use. The low-power standby feature is controlled with the $\overline{E}$ input. *$\overline{E}$ is not a clock and does not have to be cycled.* This allows the user to tie $\overline{E}$ directly to system addresses and use the line as part of the normal decoding logic. Whenever the MCM2147 is deselected, it automatically reduces its power requirements.

SYSTEM POWER SAVINGS

The automatic power-down feature adds up to significant system power savings. Unselected devices draw low standby power and only the active devices draw active power. Thus the average power consumed by a device declines as the system size increases, asymptotically approaching the standby power level as shown in Figure 2.

The automatic power-down feature is obtained without any performance degradation, since access time from chip enable is ⩽ access time from address valid. Also the fully static design gives access time equal cycle time so multiple read or write operations are possible during a single select period. The resultant data rates are 14.3 MHz and 18 MHz for the MCM2147-70 and MCM2147-55 respectively.

DECOUPLING AND BOARD LAYOUT CONSIDERATIONS

The power switching characteristic of the MCM2147 requires careful decoupling. It is recommended that a 0.1 μF to 0.3 μF ceramic capacitor be used on every other device, with a 22 μF to 47 μF bulk electrolytic decoupler every 16 devices. The actual values to be used will depend on board layout, trace widths and duty cycle.

Power supply gridding is recommended for PC board layout. A very satisfactory grid can be developed on a two-layer board with vertical traces on one side and horizontal traces on the other, as shown in Figure 3. If fast drivers are used, terminations are recommended on input signal lines to the MCM2147 because significant reflections are possible when driving their high impedance inputs. Terminations may be required to match the impedance of the line to the driver.

FIGURE 2 – AVERAGE DEVICE DISSIPATION versus MEMORY SIZE

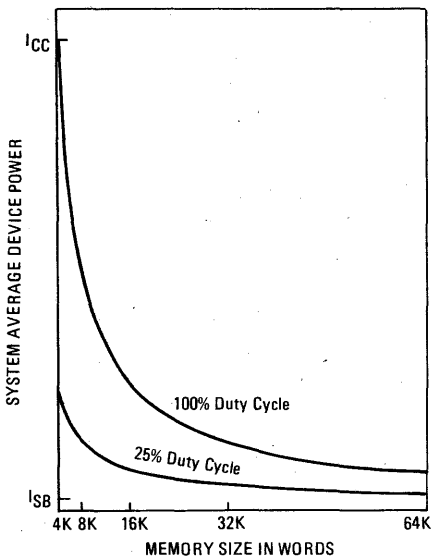
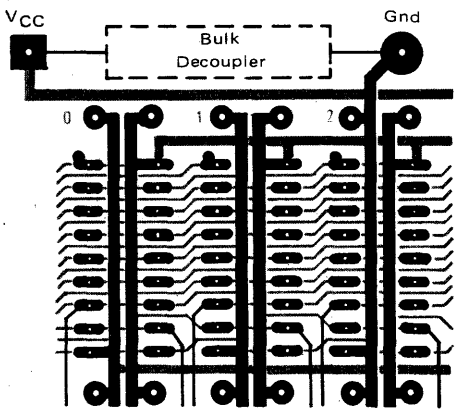


FIGURE 3 – PC LAYOUT



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MCM0464

Advance Information

MOS
(N-CHANNEL, SILICON-GATE)

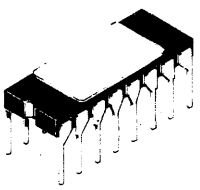
65,536 X 1-BIT DYNAMIC SERIAL MEMORY

65,536 X 1-BIT DYNAMIC SERIAL MEMORY

The MCM0464 device is a 65,536-bit dynamic serial memory configured as 16 randomly accessible shift registers, each 4096 bits long. Each of these shift registers is designed utilizing Charge Coupled Device (CCD) techniques along with the interleaved Serial-Parallel-Serial (SPS) register structure which features both low power and high density characteristics. The high density of the MCM0464 is further enhanced through the use of an electrode-per-bit memory cell approach. The high density permits packaging the memory in a standard 16-pin dual in-line package which allows the construction of highly dense memory systems using widely available automated testing and insertion equipment.

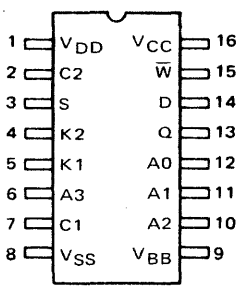
Furthermore, this buried-channel CCD memory is fabricated using our double-poly N-channel silicon-gate process. This process allows the MCM0464 to be a high performance, state-of-the-art memory circuit which is manufacturable in volume quantities.

- Industry Standard 16 Pin Dual In-Line Package
- Operating Frequency Range: 1 MHz to 5 MHz
- Low Capacitance TTL-Compatible Inputs (Except Clocks)
- 3-State, TTL-Compatible, Latched Data Output
- Output Drive Capability: 3.5 mA into 100 pF Load
- Low Capacitance 12 V Clocks:
  C1 and C2: 100 pF (typ)
  K1 and K2: 30 pF (typ)
- Low Power
  Normal Operation: < 400 mW (max) @ f_{max}
  Standby: < 70 mW (max) @ f_{min}
- Standard Power Supplies (+12 V, +5 V, and −5 V)

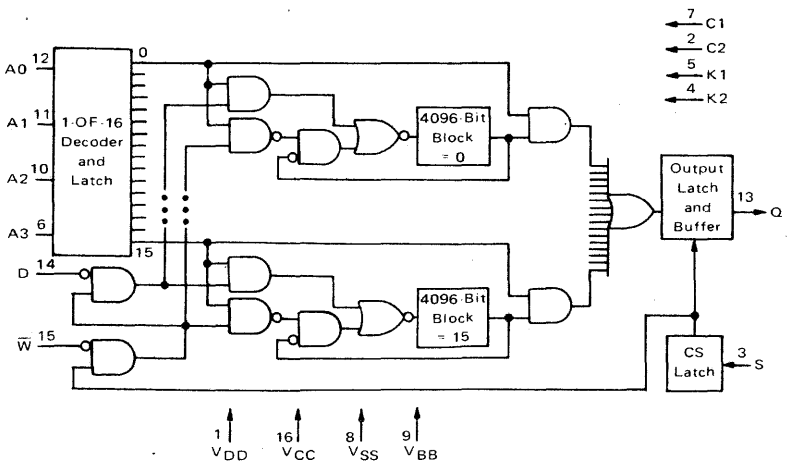


L SUFFIX
CERAMIC PACKAGE
CASE 690

PIN ASSIGNMENT



BLOCK DIAGRAM



PIN NAMES

C1, C2	Serial Shift Clocks
K1, K2	Transfer Clocks
A0-A3	Address Inputs
S	Chip Select Input
D	Data In
Q	Data Out
$\overline{W}$	Write Enable Input (Active Low)
V_{BB}	Power (−5 V)
V_{CC}	Power (+5 V)
V_{DD}	Power (+12 V)
V_{SS}	Power (0 V)

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FUNCTIONAL DESCRIPTION

Organization – The MCM0464 is a 65,536 X 1 bit dynamic serial memory organized internally as 16 dynamic shift registers (or blocks) of 4096 bits each in length. These 16 shift register blocks are randomly accessible through four internally decoded Address inputs (A0-A3). When a given register is selected, its input and output are internally connected (as needed) to the D and Q pins, respectively, thus permitting simultaneous read and write operations.

Architecture – Each of the sixteen shift register blocks is implemented using a Serial-Parallel-Serial (SPS) register architecture. In this approach N data bits are sequentially shifted into a "serial" input register. When full, the entire N-bit word is shifted in parallel into N "parallel" registers of M bits in length, as illustrated in Figure 1. At the other end of this parallel register structure, bits are loaded in parallel into an N-bit serial output register. Bits in this register are then shifted out toward the output latch and then are automatically recirculated back to the input serial register unless a Write operation is specified.

The primary advantages of this type of architecture include very high density, low power, and low clock capacitance. These features all result from the fact that in the SPS architecture the parallel registers which encompass most of the total storage capacity within each block are shifted at a considerably slower rate (f_{in}/N) than clock rate of the input or output serial registers, f_{in}.

In actuality, each 4096-bit block of the MCM0464 is implemented using an "interleaved" SPS structure in which each bit of the serial input register services two parallel registers rather than just one. The same is true for the output serial register. In addition, "electrode-per-bit" design techniques are used to reduce the effective cell size by minimizing the number of electrodes used to store each bit of information. These techniques obviously enhance the memory density considerably. The dimensions of the MCM0464 interleaved SPS structure are 32-bit input and output serial registers and 64 parallel registers, each 63 bits in length. See Figure 2. These dimensions were chosen in order to optimize the power/density/latency tradeofffs inherent in the CCD memory approach.

Clocks – The MCM0464 requires four MOS level clocks: Two high frequency (1 to 5 MHz) serial clocks and two low frequency transfer clocks. The serial clocks, C1 and C2, control the movement of data within the input and output serial registers of each 4096-bit block and have a frequency equal to the data rate. The transfer clock K1 is used to transfer data from the input serial register to the parallel registers while the transfer clock K2 is used to transfer data from the parallel registers to the output serial register of each block. The data present in the parallel registers is shifted by internally generated ripple clocks. This ripple clock technique allows a high bit-packing density approaching one electrode per bit.

To achieve proper transfer phasing, the two transfer clocks are asymmetrical about a 32-cycle interval (31.5 and 32.5 cycles) but symmetrical about a 64-cycle interval. The phasing between these transfer clocks alternates in order to achieve correct bit storage in each block. When K1 occurs during C1 time, K2 occurs during C2 time 1.5 cycles prior to K1. When K1 occurs during C2 time, K2 occurs during C1 time 2.5 cycles prior to K1. Figure 3 illustrates the clock phase relationships.

FIGURE 1 – SIMPLIFIED SPS EXAMPLE WITH N = 4

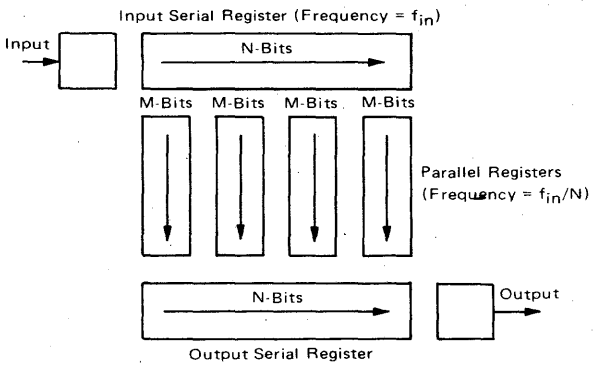
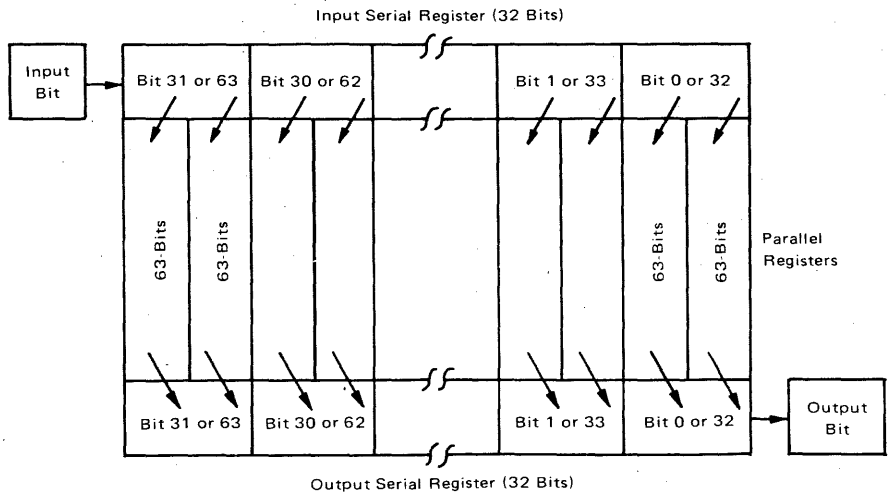
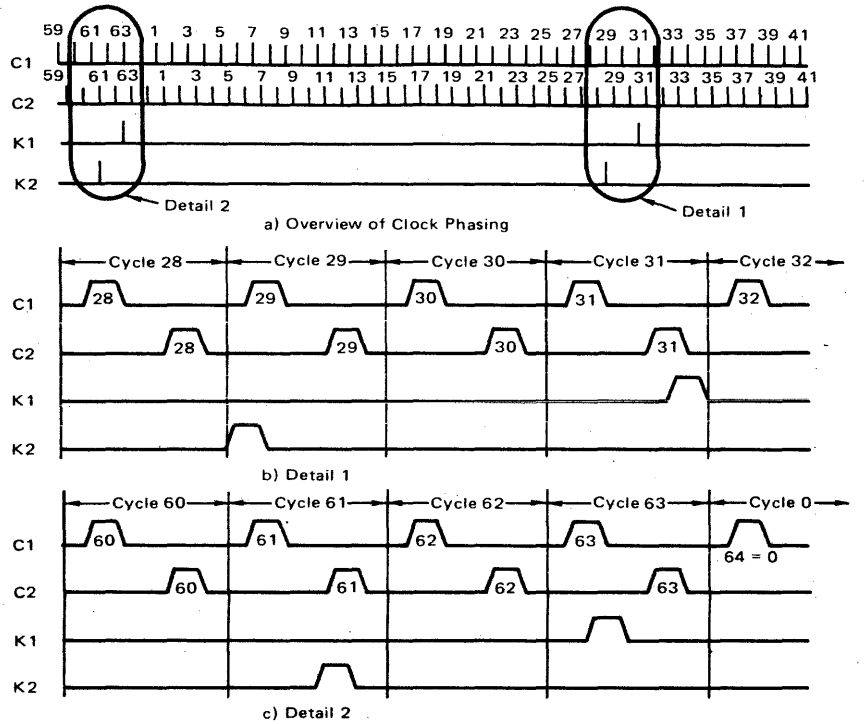


FIGURE 2 – INTERLEAVED SPS ARCHITECTURE



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FIGURE 3 – MCM0464 CLOCKS



CONTROLS

In addition to the four Address inputs (A0 through A3), other TTL level control signals available on the MCM0464 include Write Enable ($\overline{W}$) and Chip Select (S). The S input, along with the address information, is presented during C1 high time and dynamically latched with the trailing edge of C1 while simultaneously disabling both the address and S buffers. This action prevents changes that occur on the external pins from entering the internal circuitry when C1 is low. The $\overline{W}$ control signal determines whether new data from the D input pin, or recirculated output data, is presented to the input of the addressed block.

MODES OF OPERATION

Standby (Recirculate-only cycle) – In Standby mode (S low), the contents of all 16 blocks are recirculated automatically, and the device disregards the $\overline{W}$, Address, and D inputs. The output latch goes into the high impedance state after the trailing edge of the C1 clock. Minimum device power results when operating the device in the recirculate mode with minimum C1 and C2 pulse widths at the lowest allowed frequency.

Read-Recirculate Mode – In this mode of operation ($\overline{W}$ high and S high) the data from the selected block is presented to the output buffer immediately following the leading edge of C2 and appears at the output, Q, after a delay equal to the access time t_{Acc}. Thus, the access time is referenced from the leading edge of the C2 pulse and is independent of the duration of C2. The output data is latched and remains valid at the Q output pin until the end of the C1 clock pulse in the next cycle. The data present in all 16 blocks automatically recirculates from the output back to the input regardless of the address inputs, provided that $\overline{W}$ remains inactive throughout the cycle.

Read and Write Mode – In the Read and Write mode ($\overline{W}$ low and S high), the output data from the selected block is available at the output pin as in the read-recirculate mode; however, the recirculate path of that particular block is disabled. Input data present at the D input pin during C2 is written into the selected block by the falling edge of C2, while the other 15 blocks automatically recirculate their contents. This form of an "early-write" cycle ($\overline{W}$ low prior to the falling edge of C1) requires that both $\overline{W}$ and D have set-up times with respect to the trailing edge of C1. In fact, for successive write operations handled in this mode, $\overline{W}$ may be held low continuously without returning it to the high state between cycles. A "delayed-write" cycle ($\overline{W}$ goes low after the trailing edge of the C1 clock pulse) is also possible and is discussed in the next paragraph as a subset of the RMW operating mode.

Read-Modify-Write Mode – The Read-Modify-Write Mode (S high, $\overline{W}$ high goes low) is simplified by the fact that the MCM0464 is always in the read mode whenever it is selected (S high). Since the access time is referenced to the leading edge of C2 and the setup times of $\overline{W}$ and D are referenced to the trailing edge of C2, this mode of operation requires an extended C2 high time in order to provide the required modify time. This "stretched" C2 high time may be determined by the following relationship:

$$t_{C2HC2L} = t_{CHQV} + t_{Modify} + t_{DVCL} + t_{WLCL} + t_T$$

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The modify time, t_{Modify}, is determined by the memory designer and is dependent on the delays of the external logic used to modify the output data. The Read-Modify-Write (RMW) cycle time then, is given by:

$$\text{Cycle Time} = t_{C1HC1L} + t_{C1LC2H} + t_{C2HC2L} + t_{C2LC1H} + 4t_T$$

where tC2HC2L is the new "stretched" version of the C2 clock pulse.

If no modification of output data is required, then this operating mode reduces to a "delayed-write" mode in which D and W may occur after the C1 clock pulse.

MEMORY START-UP

When the MCM0464 is initially powered up, the V_{BB} supply (i.e., the -5 volt supply) should be applied to the memory before the other supplies. This action results in greater protection against accidental violation of the voltage limits specified in the Absolute Maximum Ratings section and, in general, enhances the long term reliability of the memory.

In order to clear the memory of extraneous charge following power-up, the MCM0464 must be clocked through a minimum of 32,000 cycles of any type before a valid memory cycle should be attempted.

ABSOLUTE MAXIMUM RATINGS (See Note)

Rating	Symbol	Value	Unit
Voltage on Any Pin Relative to V_{BB} ($V_{SS} - V_{BB} \geq 4.5$ V)	V_{in}, V_{out}	-0.5 to +20	Vdc
Operating Temperature Range	T_A	0 to +70	°C
Storage Temperature Range	T_{stg}	-55 to +150	°C
Power Dissipation	P_D	1.0	W

NOTE: Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature range unless otherwise noted.)

RECOMMENDED OPERATING CONDITIONS (Referenced to V_{SS})

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Supply Voltage	V_{DD} V_{CC} V_{SS} V_{BB}	11.4 4.75 0 -5.5	12 5.0 0 -5.0	12.6 5.25 0 -4.5	Vdc Vdc Vdc Vdc	1
Input High Clock Voltage	V_{IHC}	$V_{DD}-1$	–	$V_{DD}+1$	Vdc	
Input Low Clock Voltage	V_{ILC}	-0.5	–	0.8	Vdc	2
Voltage Differential Between Any Two Clock Lows	$\lvert\Delta V_{ILC}\rvert$	0	–	0.8	Vdc	2
Input High Voltage, all inputs except clocks	V_{IH}	2.4	–	V_{CC}	Vdc	1
Input Low Voltage, all inputs except clocks	V_{IL}	-0.5	–	0.8	Vdc	2

DC CHARACTERISTICS (Referenced to V_{SS})

Characteristic			Symbol	Min	Typ	Max	Units	Notes
Average V_{DD} Power Supply Current	Active	f_{min}	I_{DD}	–	5.0	8.0	mA	3, 10
		f_{max}		–	15	25	mA	
	Standby	f_{min}		–	3.0	5.0	mA	
		f_{max}		–	12	19	mA	
Average V_{CC} Power Supply Current	Active	f_{min}	I_{CC}	–	1.5	2.5	mA	3, 10
		f_{max}		–	2.5	4.0	mA	
	Standby	f_{min}		–	0.3	0.5	mA	
		f_{max}		–	1.2	2.0	mA	
Average V_{BB} Current			I_{BB}	–	–	100	μA	4
Output High Voltage			V_{OH}	2.8	–	–	V	5
Output Low Voltage			V_{OL}	–	–	0.4	V	6
Input Leakage Current (any input)			I_{in}	-10	–	10	μA	7
Output Leakage Current			I_{out}	-10	–	10	μA	8
Input Capacitance, C1 and C2			C_{in1}	–	100	–	pF	9
Input Capacitance, K1 and K2			C_{in2}	–	30	–	pF	9
Input Capacitance, A0-A3, S, W, and D_{in}			C_{in3}	–	5.0	–	pF	9
Output Capacitance, Q			C_{out}	–	7.0	–	pF	9

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RECOMMENDED CLOCKING CONDITIONS (Over Full Range of Voltage and Temperature)

Symbol	Parameter	MCM0464-50		MCM0464-60		MCM0464-70		Units	Notes
		Min	Max	Min	Max	Min	Max		
t_{C1HC1L}	C1 High Time	50	200	60	200	100	200	ns	10
t_{C2HC2L}	C2 High Time	50	300	60	300	100	300	ns	10
t_{C1LC2H}	C1 Low to C2 High	30	–	45	–	100	–	ns	
t_{C2LC1H}	C2 Low to C1 High	30	–	45	–	100	–	ns	
t_{K1HCL}	K1 High to (C1 or C2) Low	30	–	30	–	50	–	ns	
t_{K2HCL}	K2 High to (C1 or C2) Low	20	–	30	–	50	–	ns	
t_{CHK1H}	(C1 or C2) High to K1 High	0	–	0	–	0	–	ns	
t_{K1LCH}	K1 Low to (C1 or C2) High	0	–	0	–	0	–	ns	
t_{CLK2H}	(C1 or C2) Low to K2 High	0	–	0	–	0	–	ns	
t_{K2LCL}	K2 Low to (C1 or C2) Low	5	–	5	–	5	–	ns	
t_{CLK1L}	(C1 or C2) Low to K1 Low	20	–	30	–	50	–	ns	
t_T	Clock Transition Time	10	50	10	50	10	50	ns	11, 12
f	Operating Frequency	1.0	5.0	1.0	4.0	1.0	2.0	MHz	12

RECOMMENDED AC OPERATING CONDITIONS (Over Full Range of Voltage and Temperature)

Symbol	Parameter	MCM0464-50		MCM0464-60		MCM0464-70		Units	Notes
		Min	Max	Min	Max	Min	Max		
t_{AVCH}	Address Setup Time	5	–	5	–	5	–	ns	
t_{CLAX}	Address Hold Time	5	–	5	–	5	–	ns	
t_{SVCH}	Chip Select Setup Time	5	–	5	–	5	–	ns	
t_{CLSX}	Chip Select Hold Time	5	–	5	–	5	–	ns	
t_{WHCL}	Write Enable Setup Time (Read-Recirculate only)	5	–	5	–	5	–	ns	13
t_{WLCL}	Write Enable Setup Time	0	–	0	–	0	–	ns	
t_{CLWX}	Write Enable Hold Time	25	–	25	–	25	–	ns	
t_{WLC2L}	Write Enable Low to C2 Low (RMW only)	60	–	60	–	60	–	ns	
t_{DVCL}	Data Setup Time	0	–	0	–	0	–	ns	14
t_{DVWL}	Data Setup Time (RMW only)	25	–	25	–	25	–	ns	13
t_{CLDX}	Data Hold Time	25	–	25	–	25	–	ns	
t_{CLQZ}	Output Buffer Turn-off Delay	0	50	0	50	0	50	ns	15
t_{CHQV}	Access Time	–	50	–	60	–	70	ns	16
t_{CHCH}	Read/Write Cycle Time	200	–	250	–	500	–	ns	–

NOTES:

1. All voltages are measured with respect to V_{SS}.
2. The differential voltage between a low for any clock input and a low for any other clock input should not exceed 0.8 V.
3. Current levels at both minimum and maximum frequencies are specified for minimum C1 and C2 clock pulse widths. See Figure 4.
4. Measured at maximum frequency and V_{BB} = -5.5 V.
5. Measured with I_{out} = -2.5 mA.
6. Measured with I_{out} = 3.5 mA.
7. Input leakage current is measured with $V_{in} = V_{DD}$ for clock inputs and $V_{in} = V_{CC}$ for all other inputs.
8. Leakage current at the Q output pin is measured for both V_{out} equal to V_{CC} and V_{SS} when the output buffer is in the high impedance state.
9. Effective capacitance is calculated from the equation

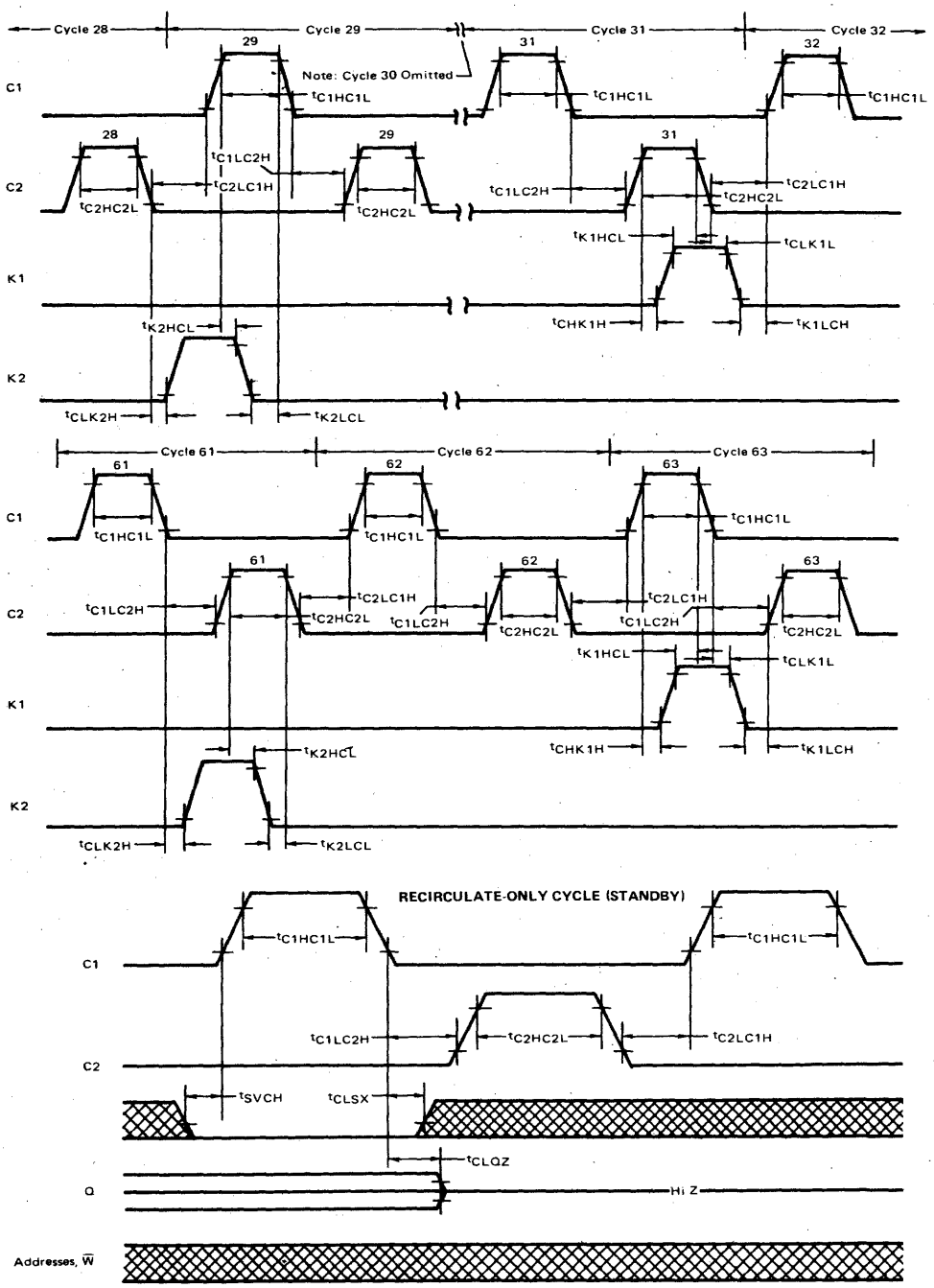
$$C = I\frac{\Delta t}{\Delta V}$$

with ΔV = 12 V for clock inputs and with ΔV = 3 V for TTL pins while the device is active.

10. Maximum clock pulse widths are specified in order to limit power dissipation. See Figure 4 showing the relationship between power and clock pulse width.
11. Reference levels used for timing measurements are V_{IHC} (min) and V_{ILC} (max) for clock inputs and V_{IH} (min) and V_{IL} (max) for all other inputs. Transition times for both rise and fall are measured between these reference points.
12. Minimum and maximum frequency values assume clock transition times of 10 ns.
13. The Read-Recirculate command is performed by keeping $\overline{W}$ in the inactive state (i.e., high) for the prescribed set-up and hold times.
14. t_{DVCL} references D to the trailing edge of C1 in a Read-(early) Write cycle. However, in a Read-Modify-Write (i.e., delayed write) cycle, t_{DVCL} references D to the negative-going edge of $\overline{W}$.
15. t_{CLQZ} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
16. Measured with a load equivalent to two TTL loads and 100 pF.

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SERIAL AND TRANSFER CLOCKS



RECIRCULATE-ONLY CYCLE (STANDBY)

TIMING PARAMETER ABBREVIATIONS

t X X X X

- signal name from which interval is defined
- transition direction for first signal
- signal name to which interval is defined
- transition direction for second signal

The transition definitions used in this data sheet are:

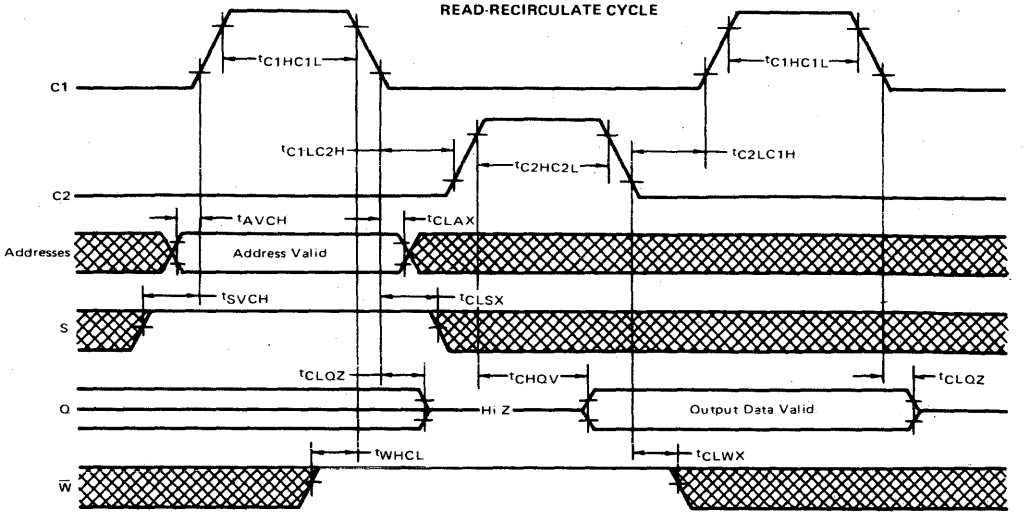
- H = transition to high
- L = transition to low
- V = transition to valid
- X = transition to invalid or don't care
- Z = transition to off (high impedance)

TIMING LIMITS

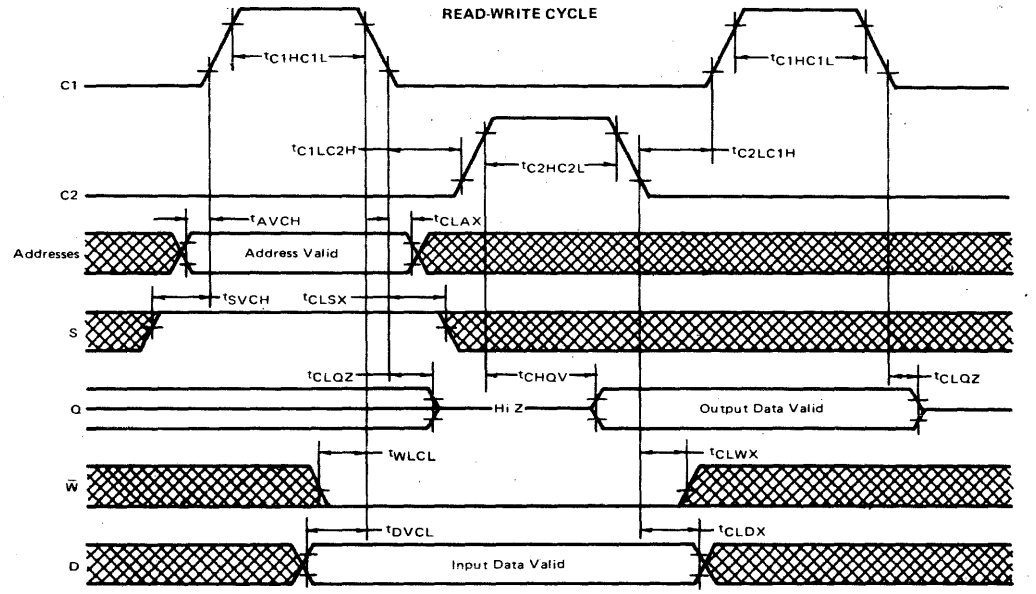
The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

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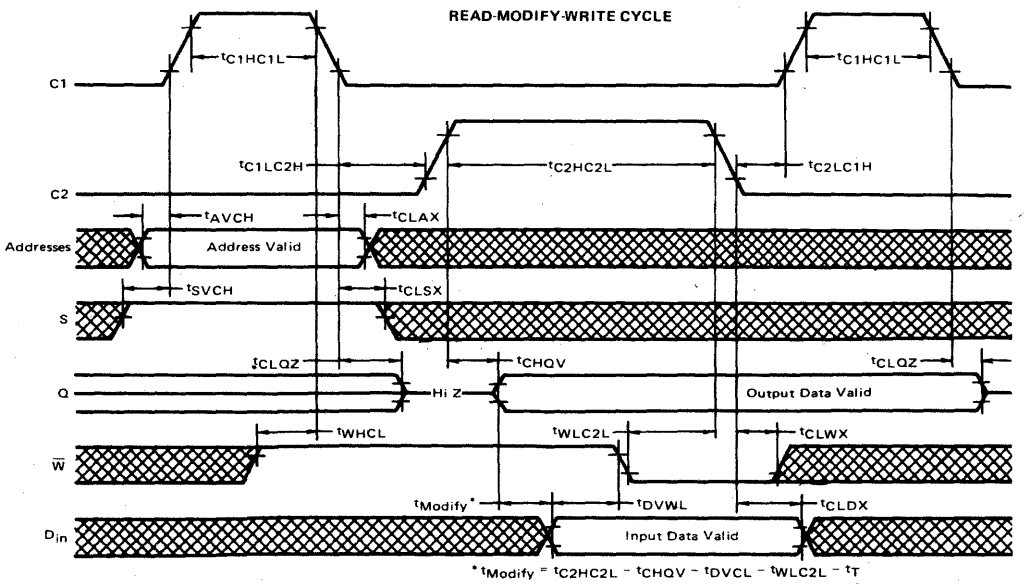
READ-RECIRCULATE CYCLE



READ-WRITE CYCLE



READ-MODIFY-WRITE CYCLE



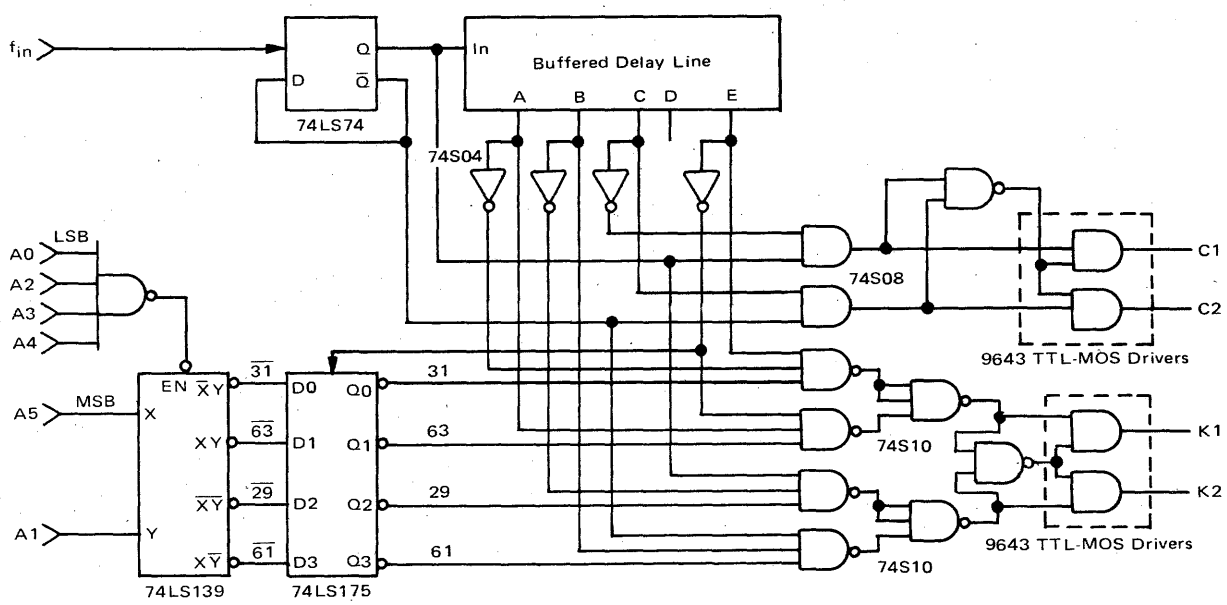
* $t_{Modify} = t_{C2HC2L} - t_{CHQV} - t_{DVCL} - t_{WLC2L} - t_T$

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CLOCK GENERATION CIRCUIT

The circuit shown below may be used to generate the four clocks required for operation of the MCM0464 with proper phase relationships from a single master clock. This master input frequency f_{in}, must be twice the desired data rate at the MCM0464 output pin. Since the input clock frequency is "squared-up" with a divide-by-two flipflop, the duty cycle of this clock is non-critical. A pulse edge at the input of the buffered delay line produces a sequence of delayed pulse edges from the A, B, C and D output taps. These delayed pulse edges are ANDed together to produce the required C1 and C2 clocks as well as the K1 and K2 transfer clocks. Since the transfer clocks are generated (but not necessarily used) every cycle, the outputs of the 6-bit, module 64 counter are decoded to enable selected transfer clock gates at counts of 29, 31, 61, and 63. Thus, K1 is passed along to the clock drivers only during cycles 31 and 63, while K2 is passed through only during cycles 29 and 61. These four counts are easily decoded with only 2 bits of the 6-bit, module 64 counter. These 6 bits are the lower order bits of the 12-bit, module 4096 loop counter required to define address locations within each 4K block and which will, in most cases be already present in the system.

SERIAL AND TRANSFER CLOCK GENERATION CIRCUIT



NOTE: All clock pulses are strictly a function of the edges of the input clock, i.e., pulse widths are *not* a function of frequency.

FIGURE 4 – TYPICAL POWER DEPENDENCE ON CLOCK PULSE WIDTH

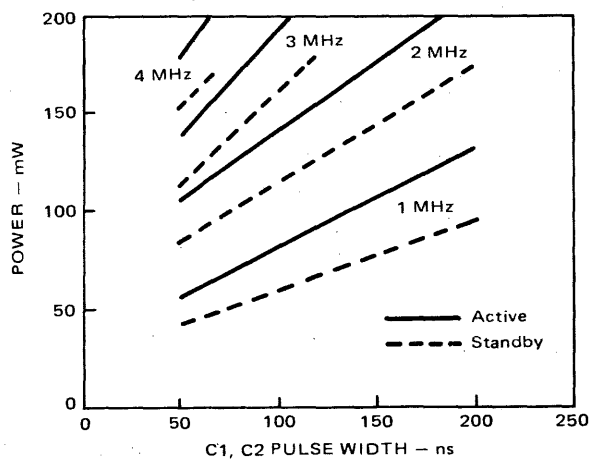
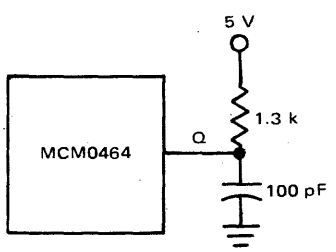


FIGURE 5 – TEST LOAD



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MOTOROLA Semiconductors
3501 ED BLUESTEIN BLVD., AUSTIN, TEXAS 78721

MCM4027

4096-BIT DYNAMIC RANDOM ACCESS MEMORY

The MCM4027 is a 4096-bit high-speed dynamic Random Access Memory designed for high-performance, low-cost applications in mainframe and buffer memories and peripheral storage. Organized as 4096 one-bit words and fabricated using Motorola's highly reliable N-channel silicon gate technology, this device optimizes speed, power, and density tradeoffs.

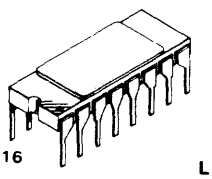
By multiplexing row and column address inputs, the MCM4027 requires only six address lines and permits packaging in Motorola's standard 16-pin dual in-line packages. Complete address decoding is done on chip with address latches incorporated.

All inputs are TTL compatible, and the output is 3-state TTL compatible. The MCM4027 incorporates a one-transistor cell design and dynamic storage techniques, with each of the 64 row addresses requiring a refresh cycle every 2.0 milliseconds.

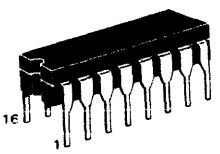
- Maximum Access Time = 150 ns – MCM4027L2, C2
  200 ns – MCM4027L3, C3
  250 ns – MCM4027L4, C4
- Maximum Read and Write Cycle Time =
  320 ns – MCM4027L2, C2
  375 ns – MCM4027L3, C3, L4, C4
- Low Power Dissipation –
  470 mW Max (Active) 27 mW Max (Standby)
- 3-State Output for OR-Ties
- On-Chip Latches for Address, Chip Select, and Data In
- Power Supply Pins on Package Corners for Optimum Layout
- Industry Standard 16-Pin Package
- Page-Mode Capability
- Compatible with the Popular 2104/MK4096/MCM6604
- Second Source for MK4027
- Also Available: MCM4027L4BECS – Mil-883 Level B Processing
  MCM4027L4CECS – Mil-883 Level C Processing

MOS
(N-CHANNEL, SILICON-GATE)

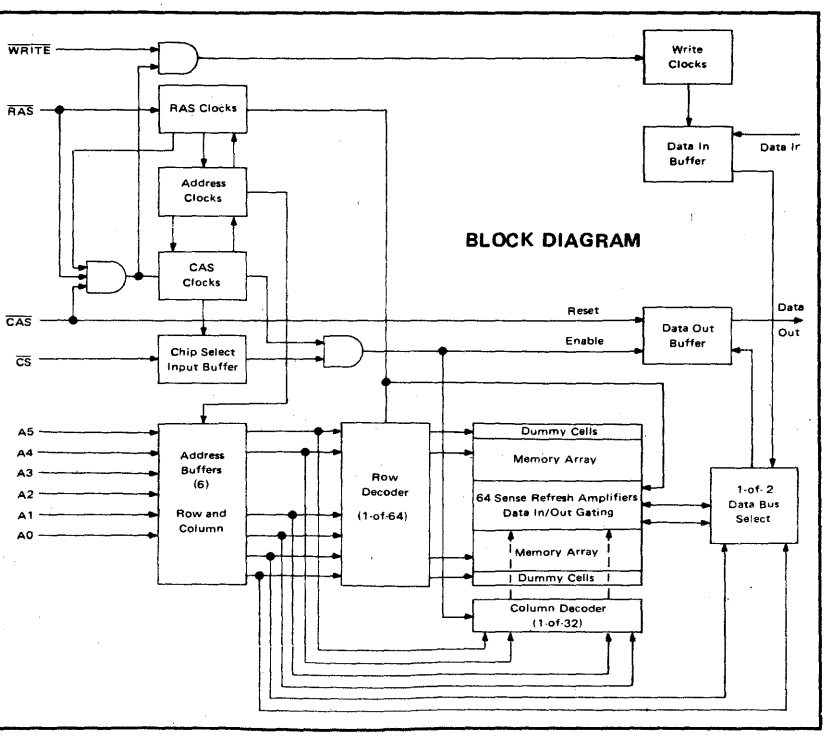
4096-BIT DYNAMIC RANDOM ACCESS MEMORY



L SUFFIX
CERAMIC PACKAGE
CASE 690

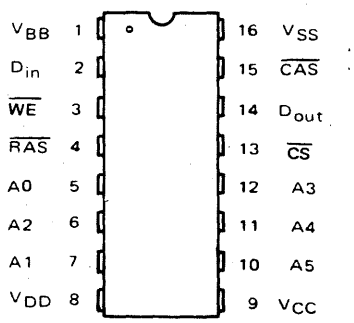


C SUFFIX
FRIT-SEAL PACKAGE
CASE 620



BLOCK DIAGRAM

PIN ASSIGNMENT



This is advance information and specifications are subject to change without notice.

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DS 9464
Formerly ADI-421

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OPERATING CHARACTERISTICS

ADDRESSING

The MCM4027 has six address inputs (A0–A5) and two clock signals designated Row Address Strobe ($\overline{RAS}$) and Column Address Strobe ($\overline{CAS}$). At the beginning of a memory cycle, the six low order address bits A0 through A5 are strobed into the chip with $\overline{RAS}$ to select one of the 64 rows. The row address strobe also initiates the timing that will enable the 64 column sense amplifiers. After a specified hold time, the row address is removed and the six high order address bits (A6–A11) are placed on the address pins. This address is then strobed into the chip with $\overline{CAS}$. Two of the 64 column sense amplifiers are selected by A1 through A5. A one of two data bus select is accomplished by A0 to complete the data selection. The Chip Select ($\overline{CS}$) is latched into the port along with the column addresses.

DATA OUTPUT

In order to simplify the memory system designed and reduce the total package count, the MCM4027 contains an input data latch and a buffered output data latch. The state of the output latch and buffer at the end of a memory cycle will depend on the type of memory cycle performed and whether the chip is selected or unselected for that memory cycle.

A chip will be unselected during a memory cycle if:

(1) The chip receives both $\overline{RAS}$ and $\overline{CAS}$ signals, but no $\overline{Chip\ Select}$ signal.

(2) The chip receives a $\overline{CAS}$ signal but no $\overline{RAS}$ signal. With this condition, the chip will be unselected regardless of the state of $\overline{Chip\ Select}$ input.

If, during a read, write, or read-modify-write cycle, the chip is unselected, the output buffer will be in the high impedance state at the end of the memory cycle. The output buffer will remain in the high impedance state until the chip is selected for a memory cycle.

For a chip to be selected during a memory cycle, it must receive the following signals: $\overline{RAS}$, $\overline{CAS}$, and $\overline{Chip\ Select}$. The state of the output latch and buffer of a selected chip during the following type of memory cycles would be:

(1) Read Cycle – On the negative edge of $\overline{CAS}$, the output buffer will unconditionally go to a high impedance state. It will remain in this state until access time. At this time, the output latch and buffer will assume the logic state of the data read from the selected cell. This output state will be maintained until the chip receives the next $\overline{CAS}$ signal.

(2) Write Cycle – If the $\overline{WE}$ input is switched to a logic 0 before the $\overline{CAS}$ transition, the output latch and buffer will be switched to the state of the data input at the end of the access time. This logic state will be maintained until the chip receives the next $\overline{CAS}$ signal.

(3) Read-Modify-Write – Same as read cycle.

DATA INPUT

Data to be written into a selected storage cell of the memory chip is first stored in the on-chip data latch. The gating of this latch is performed with a combination of the $\overline{WE}$ and $\overline{CAS}$ signals. The last of these signals to make a negative transition will strobe the data into the latch. If the $\overline{WE}$ input is switching to a logic 0 in the beginning of a write cycle, the falling edge of $\overline{CAS}$ strobes the data into the latch. The data setup and hold times are then referenced to the negative edge of $\overline{CAS}$.

If a read-modify-write cycle is being performed, the $\overline{WE}$ input would not make its negative transistion until after the $\overline{CAS}$ signal was enabled. Thus, the data would not be strobed into the latch until the negative transistion of $\overline{WE}$. The data setup and hold times would now be referenced to the negative edge of the $\overline{WE}$ signal. The only other timing constraints for a write-type-cycle is that both the $\overline{CAS}$ and $\overline{WE}$ signals remain in the logic 0 state for a sufficient time to accomplish the permanent storage of the data into the selected cell.

INPUT/OUTPUT LEVELS

All of the inputs to the MCM4027 are TTL-compatible, featuring high impedance and low capacitance (5 to 7 pF). The three-state data output buffer is TTL-compatible and has sufficient current sink capability (3.2 mA) to drive two TTL loads. The output buffer also has a separate V_{CC} pin so that it can be powered from the same supply as the logic being employed.

REFRESH

In order to maintain valid data, each of the 64 internal rows of the MCM4027 must be refreshed once every 2 ms. Any cycle in which a $\overline{RAS}$ signal occurs accomplishes a refresh operation. Any read, write, or read-modify-write cycle will refresh an entire internally selected row. However, if a write or read-modify-write cycle is used to perform a refresh cycle the chip must be deselected to prevent writing data into the selected cell. The memory can also be refreshed by employing only the $\overline{RAS}$ cycle. This refresh mode will not shorten the refresh cycle time, however the system standby power can be reduced by approximately 30%.

If the $\overline{RAS}$ only refresh cycles are employed for an extended length of time, the output buffer may eventually lose data and assume the high impedance state. Applying $\overline{CAS}$ to the chip will restore activity of the output buffer.

POWER DISSIPATION

Since the MCM4027 is a dynamic RAM, its power drain will be extremely small during the time the chip is unselected.

The power increases when the chip is selected and most of this increase is encountered on the address strobe edge. The circuitry of the MCM4027 is largely dynamic so power is not drawn during the whole time the strobe is active. Thus the dynamic power is a function of the operating frequency rather than the active duty cycle.

In a memory system, the $\overline{CAS}$ signal must be supplied to all the memory chips to ensure that the outputs of the unselected chips are switched to the high impedance state. Those chips that do not receive a $\overline{RAS}$ signal will not dissipate any power on the $\overline{CAS}$ edge except for that required to turn off the chip outputs. Thus, in order to ensure minimum system power, the $\overline{RAS}$ signal should be decoded so that only the chips to be selected receive a $\overline{RAS}$ signal. If the $\overline{RAS}$ signal is decoded, then the chip select input of all the chips can be set to a logic 0 state.

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DC OPERATING CONDITIONS AND CHARACTERISTICS
(Full operating voltage and temperature range unless otherwise noted.)

RECOMMENDED OPERATING CONDITIONS (Referenced to V_{SS} = Ground.)

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Supply Voltage	V_{DD}	10.8	12.0	13.2	Vdc	2
	V_{CC}	V_{SS}	5.0	V_{DD}	Vdc	3
	V_{SS}	0	0	0	Vdc	2
	V_{BB}	-4.5	-5.0	-5.5	Vdc	2
Logic 1 Voltage, $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$	V_{IHC}	2.4	5.0	7.0	Vdc	2, 4
Logic 1 Voltage, all inputs except $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$	V_{IH}	2.2	5.0	7.0	Vdc	2, 4
Logic 0 Voltage, all inputs	V_{IL}	-1.0	0	0.8	Vdc	2, 4

DC CHARACTERISTICS (V_{DD} = 12 V ±10%, V_{CC} = 5.0 V ±10%, V_{BB} = -5.0 V ±10%, V_{SS} = 0 V, T_A = 0 to 70°C.) Notes 1, 5

Characteristic	Symbol	Min	Typ	Max	Units	Notes
Average V_{DD} Power Supply Current	I_{DD1}			35	mA	6
V_{CC} Power Supply Current	I_{CC}				mA	7
Average V_{BB} Power Supply Current	I_{BB}			150	μA	
Standby V_{DD} Power Supply Current	I_{DD2}			2	mA	9
Average V_{DD} Power Supply Current during "$\overline{RAS}$ only" cycles	I_{DD3}			25	mA	6
Input Leakage Current (any input)	$I_{I(L)}$			10	μA	8
Output Leakage Current	$I_{O(L)}$			10	μA	9, 10
Output Logic 1 Voltage @ I_{out} = -5 mA	V_{OH}	2.4			Vdc	
Output Logic 0 Voltage @ I_{out} = 3.2 mA	V_{OL}			0.4	Vdc	

NOTES 1 through 11:

1. T_A is specified for operation at frequencies to $t_{RC} \geq t_{RC}(min)$. Operation at higher cycle rates with reduced ambient temperatures and higher power dissipation is permissible provided that all ac parameters are met.
2. All voltages referenced to V_{SS}.
3. Output voltage will swing from V_{SS} to V_{CC} when enabled, with no output load. For purposes of maintaining data in standby mode, V_{CC} may be reduced to V_{SS} without affecting refresh operations or data retention. However, the $V_{OH}(min)$ specification is not guaranteed in this mode.
4. Device speed is not guaranteed at input voltages greater than TTL levels (0 to 5 v).
5. Several cycles are required after power-up before proper device operation is achieved. Any 8 cycles which perform refresh are adequate for this purpose.
6. Current is proportional to cycle rate. $I_{DD1}(max)$ is measured at the cycle rate specified by $t_{RC}(min)$.
7. I_{CC} depends on output loading. During readout of high level data V_{CC} is connected through a low impedance (135 Ω typ) to Data Out. At all other times I_{CC} consists of leakage currents only.
8. All device pins at 0 volts except V_{BB} which is at -5 volts and the pin under test which is at +10 volts.
9. Output is disabled (high-impedance) and $\overline{RAS}$ and $\overline{CAS}$ are both at a logic 1. Transient stabilization is required prior to measurement of this parameter.
10. $0 V \leq V_{Out} \leq +10 V$.
11. Effective capacitance is calculated from the equation:

$$C = \frac{\Delta Q}{\Delta V} \text{ with } \Delta V = 3 \text{ volts.}$$

EFFECTIVE CAPACITANCE (Full operating voltage and temperature range, periodically sampled rather than 100% tested) Note 11

Characteristic		Symbol	Max	Unit
Input Capacitance	(A0-A5), D_{in}, $\overline{CS}$	$C_{in(EFF)}$	5.0	pF
	$\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$		7.0	
Output Capacitance		$C_{out(EFF)}$	7.0	pF

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AC OPERATING CONDITIONS AND CHARACTERISTICS
(Read, Write, and Read-Modify-Write Cycles)

RECOMMENDED AC OPERATING CONDITIONS (V_{DD} = 12 V ±10%, V_{CC} = 5.0 V ±10%, V_{BB} = -5.0 V ±10%, V_{SS} = 0 V, T_A = 0 to 70°C.) Notes 1, 5, 12, 18

Parameter	Symbol	MCM4027L2/C2		MCM4027L3/C3		MCM4027L4/C4		Units	Notes
		Min	Max	Min	Max	Min	Max		
Random Read or Write Cycle Time	t_{RC}	320		375		375		ns	13
Read Write Cycle Time	t_{RWC}	330		420		480		ns	13
Access Time from Row Address Strobe	t_{RAC}		150		200		250	ns	14, 16
Access Time from Column Address Strobe	t_{CAC}		100		135		165	ns	15, 16
Output Buffer and Turn-Off Delay	t_{OFF}		40		50		60	ns	
Row Address Strobe Precharge Time	t_{RP}	100		120		120		ns	
Row Address Strobe Pulse Width	t_{RAS}	150	10,000	200	10,000	250	10,000	ns	
Column Address Strobe Pulse Width	t_{CAS}	100		135		165		ns	
Row to Column Strobe Lead Time	t_{RCL}	20	50	25	65	35	85	ns	17
Row Address Setup Time	t_{ASR}	0		0		0		ns	
Row Address Hold Time	t_{RAH}	20		25		35		ns	
Column Address Setup Time	t_{ASC}	-10		-10		-10		ns	
Column Address Hold Time	t_{CAH}	45		55		75		ns	
Column Address Hold Time Referenced to $\overline{RAS}$	t_{AR}	95		120		160		ns	
Chip Select Setup Time	t_{CSC}	-10		-10		-10		ns	
Chip Select Hold Time	t_{CH}	45		55		75		ns	
Chip Select Hold Time Referenced to $\overline{RAS}$	t_{CHR}	95		120		160		ns	
Transition Time (Rise and Fall)	t_T	5.0	35	5.0	50	5.0	50	ns	18
Read Command Setup Time	t_{RCS}	0		0		0		ns	
Read Command Hold Time	t_{RCH}	0		0		0		ns	
Write Command Hold Time	t_{WCH}	45		55		75		ns	
Write Command Hold Time Referenced to $\overline{RAS}$	t_{WCR}	95		120		160		ns	
Write Command Pulse Width	t_{WP}	45		55		75		ns	
Write Command to Row Strobe Lead Time	t_{RWL}	50		70		85		ns	
Write Command to Column Strobe Lead Time	t_{CWL}	50		70		85		ns	
Data in Setup Time	t_{DS}	0		0		0		ns	19
Data in Hold Time	t_{DH}	45		55		75		ns	19
Data in Hold Time Referenced to $\overline{RAS}$	t_{DHR}	95		120		160		ns	
Column to Row Strobe Precharge Time	t_{CRP}	0		0		0		ns	
Column Precharge Time	t_{CP}	60		80		110		ns	
Refresh Period	t_{RFSH}		2.0		2.0		2.0	ms	
$\overline{CAS}$ to $\overline{WRITE}$ Delay	t_{CWD}	60		80		90		ns	20
$\overline{RAS}$ to $\overline{WRITE}$ Delay	t_{RWD}	110		145		175		ns	20

NOTES 12 through 20:

12. AC measurements assume t_T = 5 ns.

13. The specifications for t_{RC}(min) and t_{RWC}(min) are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_A ≤ 70°C) is assured.

14. Assumes that $t_{RCD} \leq t_{RCD}$(max).

15. Assumes that $t_{RCD} \geq t_{RCD}$ (max).

16. Measured with a load circuit equivalent to 2 TTL loads and 100 pF.

17. Operation within the t_{RCD}(max) limit insures that t_{RAC}(max) can be met. t_{RCD}(max) is specified as a reference point only; if t_{RCD} is greater than the specified t_{RCD}(max) limit, then access time is controlled exclusively by t_{CAC}.

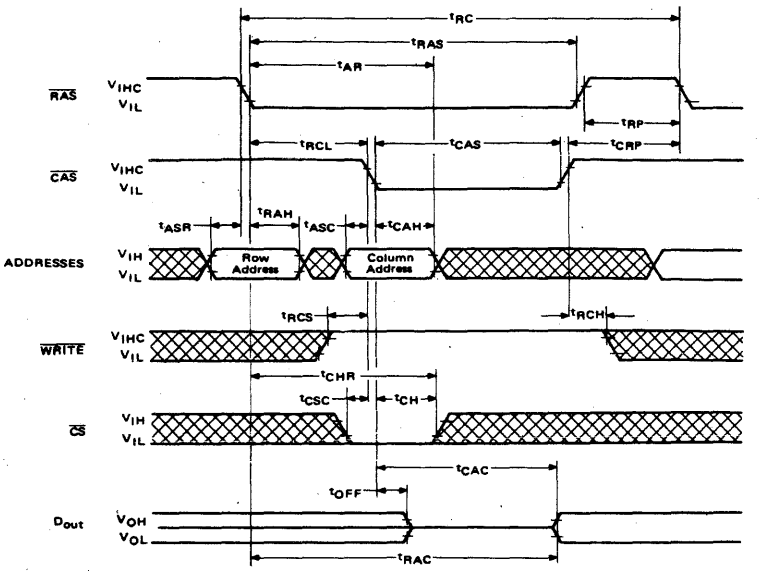
18. V_{IHC}(min) or V_{IH}(min) and V_{IL}(max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IHC} or V_{IH} and V_{IL}.

19. These parameters are referenced to $\overline{CAS}$ leading edge in random write cycles and to $\overline{WRITE}$ leading edge in delayed write or read-modify write cycles.

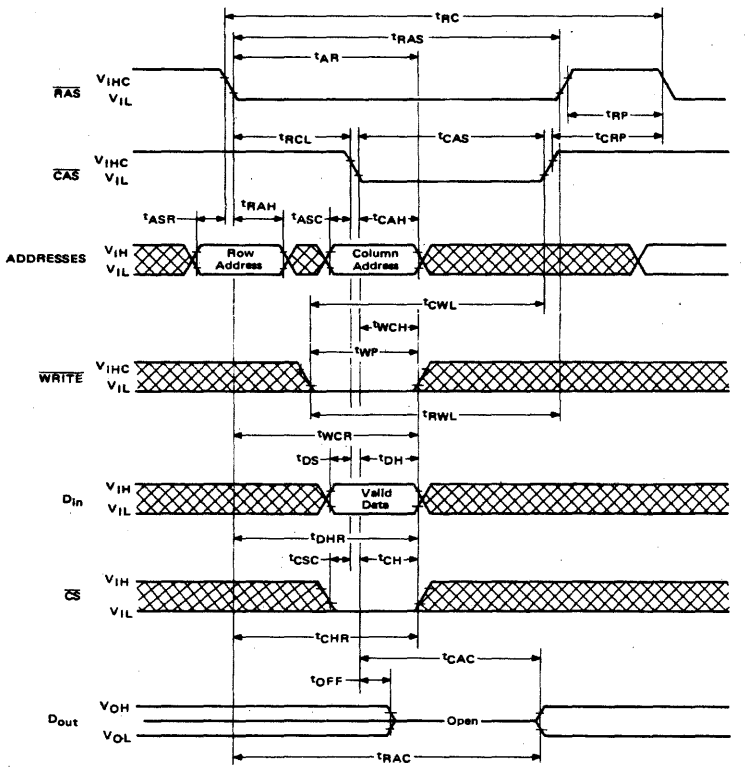
20. t_{WCS}, t_{CWD}, and t_{RWD} are not restrictive operating parameters. They are included in the data sheet as electrical characterisitcs only: If $t_{WCS} \geq t_{WCS}$(min), the cycle is an early write cycle and Data Out will contain the data written into the selected cell. If $t_{CWD} \geq t_{CWD}$(min) and $t_{RWD} \geq t_{RWD}$(min), the cycle is a read-write cycle and Data Out will contain data read from the selected cell. If neither of the above sets of conditions is satisfied, the condition of Data Out (at access time) is indeterminate.

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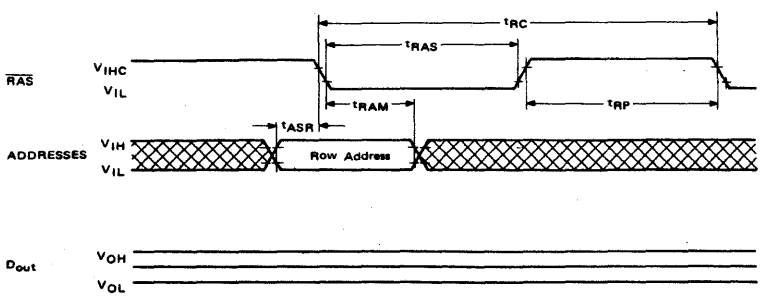
READ CYCLE TIMING



WRITE CYCLE TIMING

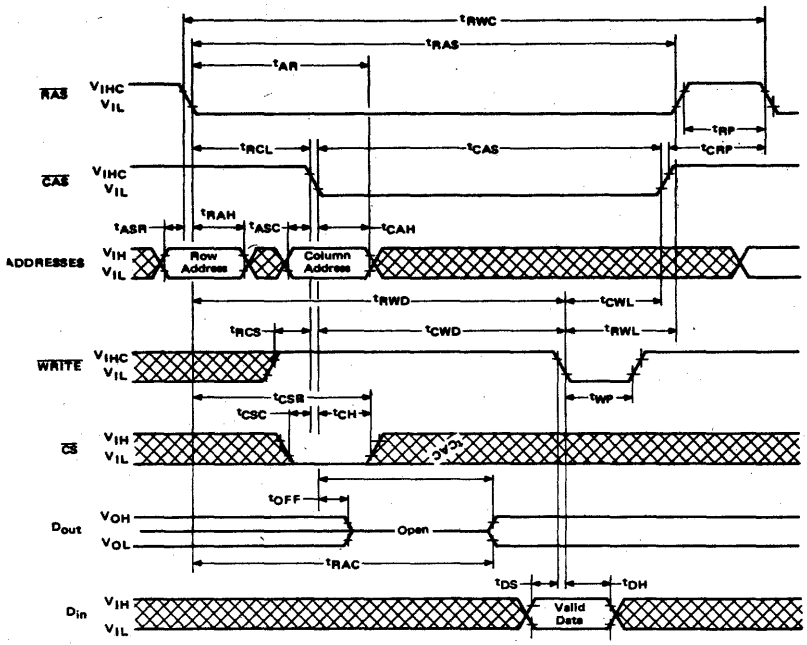


RAS ONLY REFRESH TIMING

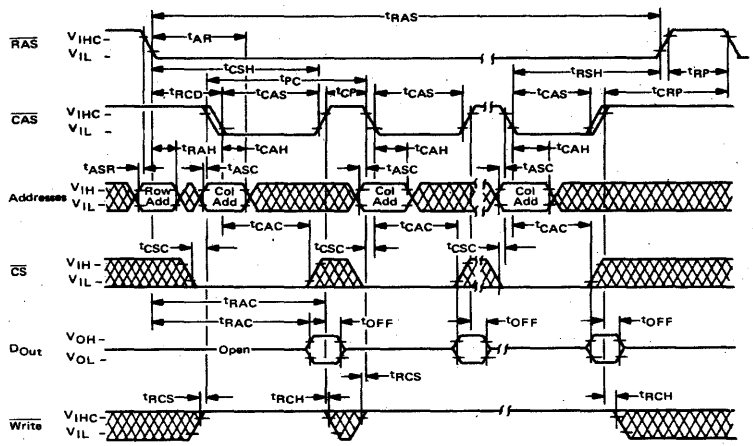


©IC MASTER 1979

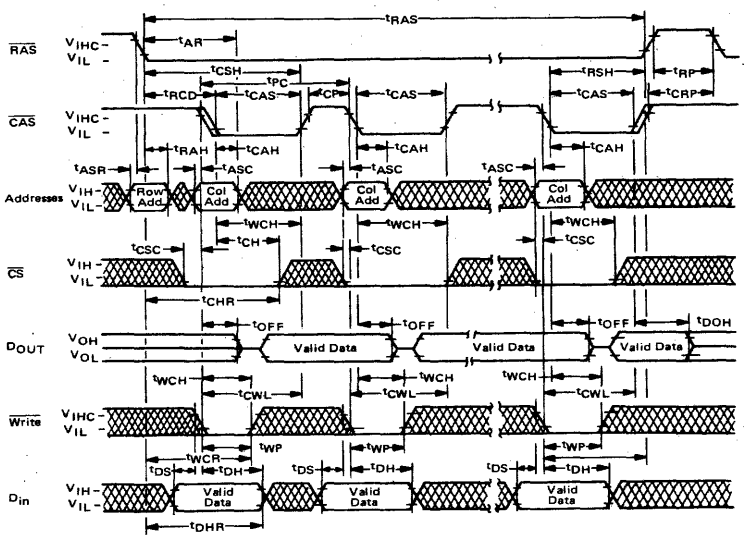
READ-MODIFY-WRITE TIMING



PAGE MODE READ CYCLE



PAGE MODE WRITE CYCLE



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3501 ED BLUESTEIN BLVD., AUSTIN, TEXAS 78721

MCM2114
MCM21L14

Advance Information

4096-BIT STATIC RANDOM ACCESS MEMORY

The MCM2114 is a 4096-bit random access memory fabricated with high density, high reliability N-channel silicon-gate technology. For ease of use, the device operates from a single power supply, is directly compatible with TTL and DTL, and requires no clocks or refreshing because of fully static operation. Data access is particularly simple, since address setup times are not required. The data out has the same polarity as the input data.

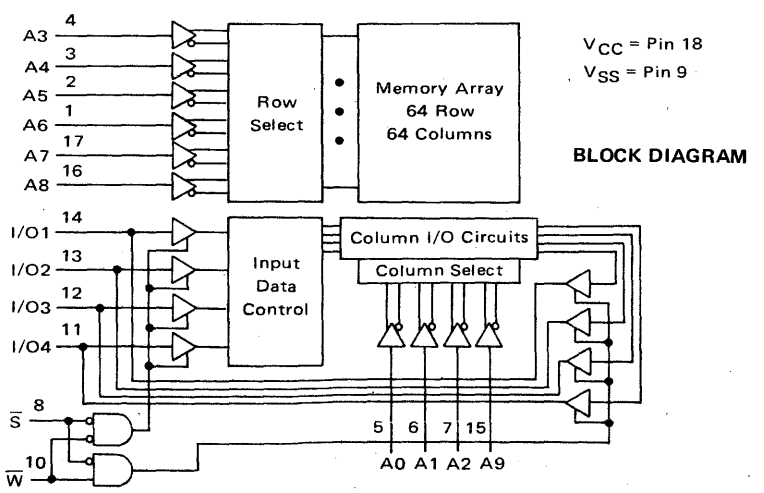
The MCM2114 is designed for memory applications where simple interfacing is the design objective. The MCM2114 is assembled in 18-pin dual in-line packages with the industry standard pin-out. A separate chip select ($\overline{S}$) lead allows easy selection of an individual package when the three-state outputs are OR-tied.

The MCM2114 series has a maximum power dissipation of 525 mW. Low power versions (i.e., MCM21L14 series) are available with a maximum power dissipation of only 370 mW.

- 1024 Words by 4-Bit Organization
- Industry Standard 18-Pin Configuration
- Single +5 Volt Supply ±10% Tolerance
- No Clock or Timing Strobe Required
- Fully Static: Cycle Time = Access Time
- Fully TTL/DTL Compatible
- Common Data Input and Output
- Three-State Outputs for OR-Ties
- Low Power Version Available — 370 mW (Max)

MAXIMUM ACCESS TIME/MINIMUM CYCLE TIME

MCM2114-20 MCM21L14-20	200 ns	MCM2114-30 MCM21L14-30	300 ns
MCM2114-25 MCM21L14-25	250 ns	MCM2114-45 MCM21L14-45	450 ns

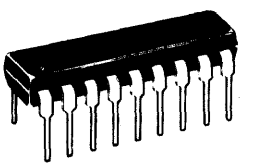


BLOCK DIAGRAM

MOS
(N-CHANNEL, SILICON-GATE)

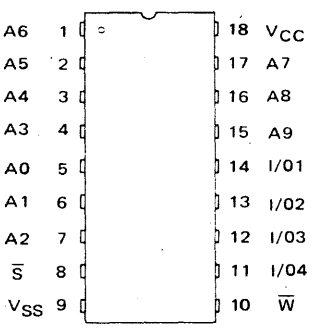
4096-BIT STATIC RANDOM ACCESS MEMORY

P SUFFIX
PLASTIC PACKAGE
CASE 707-01



C SUFFIX
FRIT-SEAL
CERAMIC PACKAGE
ALSO AVAILABLE

PIN ASSIGNMENT



PIN NAMES

A0-A9	Address Input
$\overline{W}$	Write Enable
$\overline{S}$	Chip Select
I/O1-I/O4	Data Input/Output
V_{CC}	Power (+5 V)
V_{SS}	Ground

This is advance information and specifications are subject to change without notice.

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ADI-470
Formerly NP-79

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DC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature range unless otherwise noted.)

RECOMMENDED DC OPERATING CONDITIONS

Parameter	Symbol	MCM2114			MCM21L14			Unit
		Min	Nom	Max	Min	Nom	Max	
Input Load Current (All Input Pins, V_{in} = 0 to 5.5 V)	I_{LI}	–	–	10	–	–	10	μA
I/O Leakage Current ($\overline{S}$ = 2.4 V, $V_{I/O}$ = 0.4 V to V_{CC})	$\|I_{LO}\|$	–	–	10	–	–	10	μA
Power Supply Current (V_{in} = 5.5, $I_{I/O}$ = 0 mA, T_A = 25°C)	I_{CC1}	–	80	95	–	–	65	mA
Power Supply Current (V_{in} = 5.5 V, $I_{I/O}$ = 0 mA, T_A = 0°C)	I_{CC2}	–	–	100	–	–	70	mA
Input Low Voltage	V_{IL}	-0.5	–	0.8	-0.5	–	0.8	V
Input High Voltage	V_{IH}	2.0	–	6.0	2.0	–	6.0	V
Output Low Current V_{OL} = 0.4 V	I_{OL}	2.1	6.0	–	2.1	6.0	–	mA
Output High Current V_{OH} = 2.4 V	I_{OH}	–	-1.4	-1.0	–	-1.4	-1.0	mA
Output Short Circuit Current	I_{OS} (2)	–	–	40	–	–	40	mA

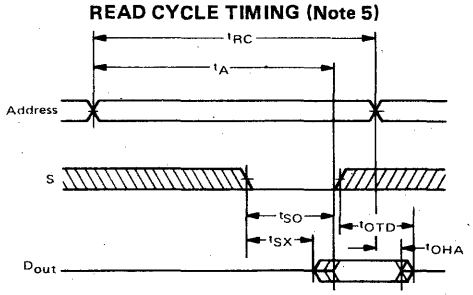
Note: 2. Duration not to exceed 30 seconds.

CAPACITANCE

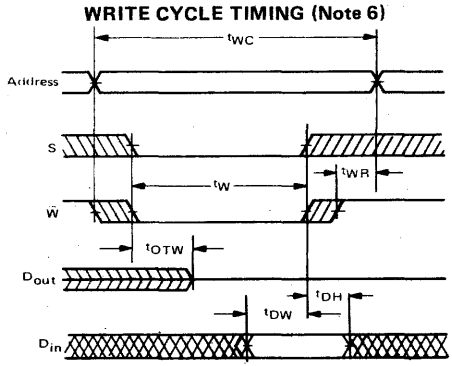
(f = 1.0 MHz, T_A = 25°C, periodically sampled rather than 100% tested.)

Characteristic	Symbol	Max	Unit
Input Capacitance (V_{in} = 0 V)	C_{in}	5.0	pF
Input/Output Capacitance ($V_{I/O}$ = 0 V)	$C_{I/O}$	5.0	pF

READ CYCLE TIMING (Note 5)



WRITE CYCLE TIMING (Note 6)



Notes: 5. $\overline{W}$ is high for a Read cycle.
6. If the $\overline{S}$ low transition occurs simultaneously with the $\overline{W}$ low transition, the output buffers remain in a high impedance rate.

AC OPERATING CONDITIONS AND CHARACTERISTICS

Read (Note 3), Write (Note 4) Cycles

RECOMMENDED AC OPERATING CONDITIONS (T_A = 0 to 70°C, V_{CC} = 5.0 V ± 10%)

Parameter	Symbol	MCM2114-20 MCM21L14-20		MCM2114-25 MCM21L14-25		MCM2114-30 MCM21L14-30		MCM2114-45 MCM21L14-45		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
Read Cycle Time	t_{RC}	200	–	250	–	300	–	450	–	ns
Access Time	t_A	–	200	–	250	–	300	–	450	ns
Chip Selection to Output Valid	t_{SO}	–	70	–	85	–	100	–	120	ns
Chip Selection to Output Active	t_{SX}	20	–	20	–	20	–	20	–	ns
Output 3-State From Deselection	t_{OTD}	–	60	–	70	–	80	–	100	ns
Output Hold From Address Change	t_{OHA}	50	–	50	–	50	–	50	–	ns
Write Cycle Time	t_{WC}	200	–	250	–	300	–	450	–	ns
Write Time	t_W	120	–	135	–	150	–	200	–	ns
Write Release Time	t_{WR}	0	–	0	–	0	–	0	–	ns
Output 3-State From Write	t_{OTW}	–	60	–	70	–	80	–	100	ns
Data to Write Time Overlap	t_{DW}	120	–	135	–	150	–	200	–	ns
Data Hold From Write Time	t_{DH}	0	–	0	–	0	–	0	–	ns

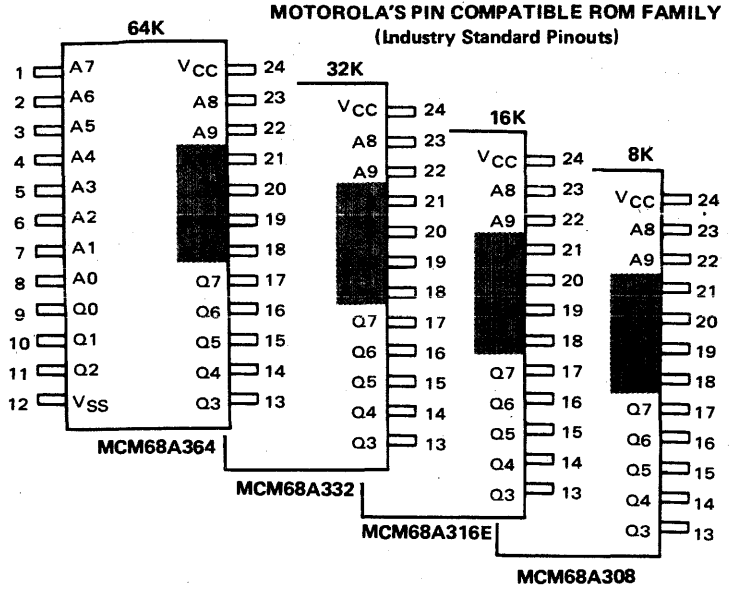
Notes: 3. A Read occurs during the overlap of a low $\overline{S}$ and a high $\overline{W}$.
4. A Write occurs during the overlap of a low $\overline{S}$ and a low $\overline{W}$.

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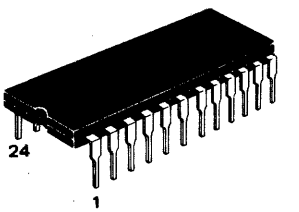
MOTOROLA
Semiconductors
3501 ED BLUESTEIN BLVD., AUSTIN, TEXAS 78721

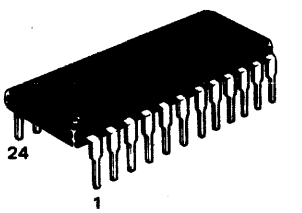
MCM68A364
MCM68B364
MCM68A308
MCM68B308
MCM68A316A
MCM68A30A
MCM68B30A

MOTOROLA'S PIN COMPATIBLE ROM FAMILY
(Industry Standard Pinouts)



C SUFFIX
FRIT-SEAL PACKAGE
CASE 623





P SUFFIX
PLASTIC PACKAGE
CASE 709

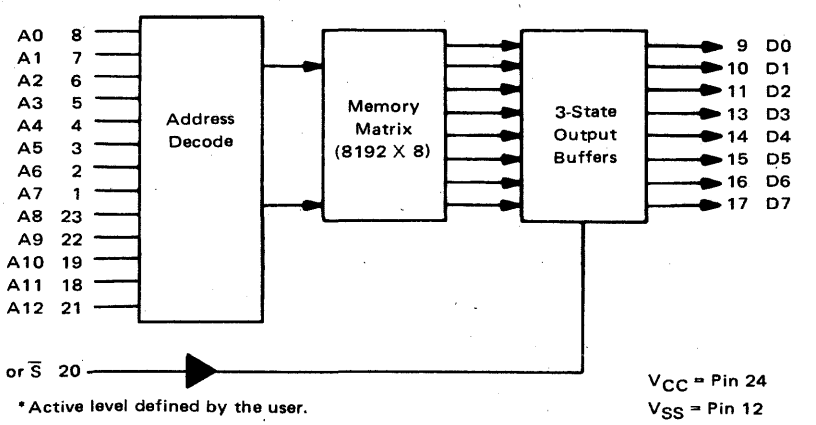
ROM FAMILY

The MCM68A/MCM68B is a mask-programmable byte-organized memory family designed for use in bus-organized systems. They are fabricated with N-channel silicon-gate technology. For ease of use, the devices operate from a single power supply, have compatibility with TTL and DTL, and need no clocks or refreshing because of static operation.

The memories are compatible with the M6800 Microcomputer Family, providing read only storage in byte increments.

- Fully Static Operation
- Single ± 10% 5-Volt Power Supply
- Three-State Data Output for OR-Ties
- Mask Programmable Chip Enable
- Full TTL Compatibility
- Maximum Access Time — 250 ns — MCM68B
  350 ns — MCM68A
- EPROM Pin Compatible

BLOCK DIAGRAM



*Active level defined by the user.

V_{CC} = Pin 24
V_{SS} = Pin 12

This is advance information and specifications are subject to change without notice.
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ADI-494

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DC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature range unless otherwise noted.)

RECOMMENDED DC OPERATING CONDITIONS

Parameter	Symbol	Min	Nom	Max	Unit
Supply Voltage (V_{CC} must be applied at least 100 μs before proper device operation is achieved)	V_{CC}	4.5	5.0	5.5	Vdc
Input High Voltage	V_{IH}	2.0	–	5.5	Vdc
Input Low Voltage	V_{IL}	-0.3	–	0.8	Vdc

DC CHARACTERISTICS

Characteristic	Symbol	Min	Typ	Max	Unit
Input Current (V_{in} = 0 to 5.5 V)	I_{in}	–	–	2.5	μAdc
Output High Voltage (I_{OH} = -205 μA)	V_{OH}	2.4	–	–	Vdc
Output Low Voltage (I_{OL} = 1.6mA or 3.2 mA for 64K)	V_{OL}	–	–	0.4	Vdc
Output Leakage Current (Three-State) (V_{out} = 0.4 V to 2.4 V)	I_{LO}	–	–	10	μAdc
Supply Current — Active (V_{CC} = 5.5 V, T_A = 0°C)	I_{CC}	–	45	80*	mAdc
Supply Current — Standby (V_{CC} = 5.5 V, T_A = 0°C, $\overline{E}$ = V_{IH})	I_{SB}	–	6.0	10	mAdc

*130 mAdc for MCM6830A and MCM68A316A,

CAPACITANCE

(f = 1.0 MHz, T_A = 25°C, periodically sampled rather than 100% tested.)

Characteristic	Symbol	Max	Unit
Input Capacitance	C_{in}	7.5	pF
Output Capacitance	C_{out}	12.5	pF

AC OPERATING CONDITIONS AND CHARACTERISTICS

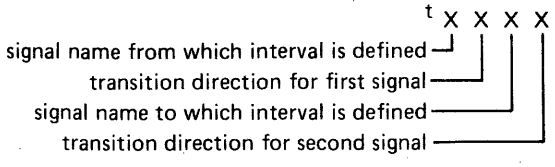
Read Cycle (64K only)

RECOMMENDED AC OPERATING CONDITIONS

(T_A = 0 to 70°C, V_{CC} = 5.0 V ± 10%. All timing with t_r = t_f = 20 ns, load of Figure 1.)

Parameter	Symbol	MCM68B364		MCM68A364		Unit
		Min	Max	Min	Max	
Address Valid to Address Don't Care (Cycle Time when Chip Enable is held Active)	t_{AVAX}	250	–	350	–	ns
Chip Enable Low to Chip Enable High	t_{ELEH}	250	–	350	–	
Address Valid to Output Valid (Access)	t_{AVQV}	–	250	–	350	
Chip Enable Low to Output Valid (Access)	t_{ELQV}	–	250	–	350	
Address Valid to Output Invalid	t_{AVQX}	10	–	10	–	
Chip Enable Low to Output Invalid	t_{ELQX}	10	–	10	–	
Chip Enable High to Output High Z	t_{EHQZ}	0	70	0	80	
Chip Selection to Power Up Time	t_{PU}	0	–	0	–	
Chip Deselection to Power Down Time	t_{PD}	–	100	–	120	
Address Valid to Chip Enable Low (Address Setup)	t_{AVEL}	0	–	0	–	

TIMING PARAMETER ABBREVIATIONS



The transition definitions used in this data sheet are:

- H = transition to high
- L = transition to low
- V = transition to valid
- X = transition to invalid or don't care
- Z = transition to off (high impedance)

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AC OPERATING CONDITIONS AND CHARACTERISTICS

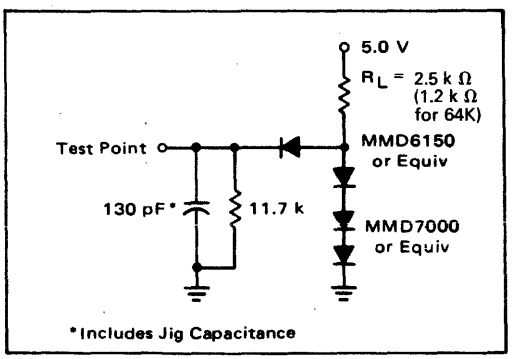
(Full operating voltage and temperature unless otherwise noted.
All timing with $t_r = t_f = 20$ ns, Load of Figure 1)

Characteristic	Symbol	MCM68A308		MCM68B308		Unit
		Min	Max	Min	Max	
Cycle Time	t_{cyc}	350	–	250	–	ns
Access Time	t_{acc}	–	350	–	250	ns
Chip Select to Output Delay	t_{SO}	–	150	–	150	ns
Data Hold from Address	t_{DHA}	10	–	10	–	ns
Data Hold from Deselection	t_{DHD}	10	150	10	150	ns

TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

FIGURE 1 – AC TEST LOAD



WAVEFORMS

Waveform Symbol	Input	Output
———	MUST BE VALID	WILL BE VALID
———		
⟋⟋⟋	CHANGE FROM H TO L	WILL CHANGE FROM H TO L
⟋⟋⟋	CHANGE FROM L TO H	WILL CHANGE FROM L TO H
⟋⟋⟋	DON'T CARE: ANY CHANGE PERMITTED	CHANGING: STATE UNKNOWN
⟋⟋⟋	–	HIGH IMPEDANCE

CUSTOM PROGRAMMING

By the programming of a single photomask for the MCM68/MCM68 family, the customer may specify the content of the memory and the method of enabling the outputs.

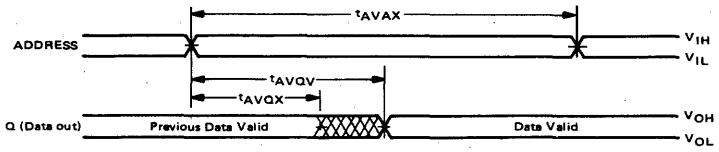
Information on the general options of the MCM68/MCM68 family should be submitted on an Organizational Data form such as that shown in Figure 3.

Information for custom memory content may be sent to Motorola in one of two forms (shown in order of preference):

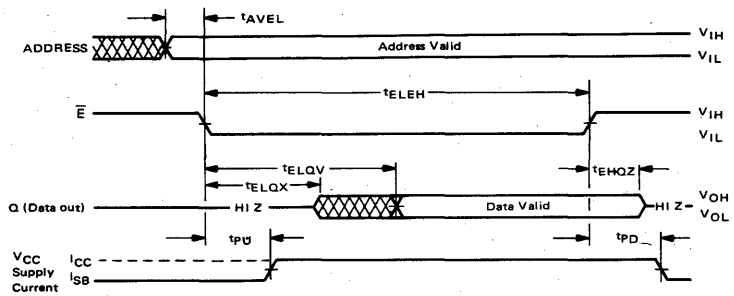
1. IBM Punch Cards
   A. Hexadecimal Format
   B. INTEL Hexadecimal Format
   C. Binary Negative-Positive Format
2. EPROMs – four 16K (MCM2716, or TMS2716, or eight 8K (MCM2708).

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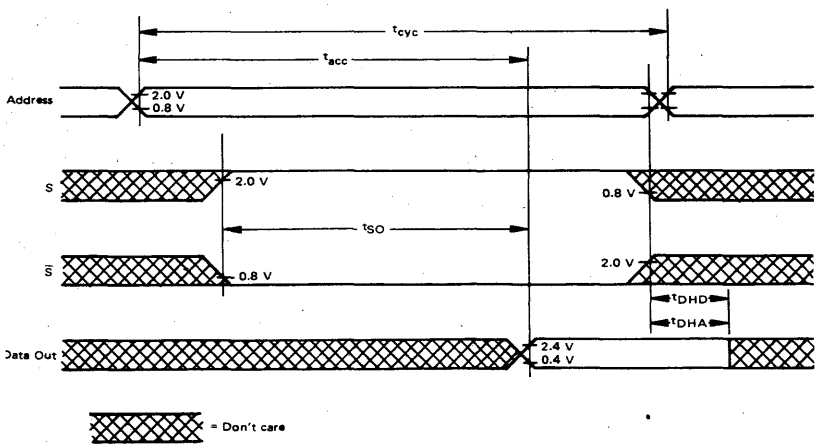
READ CYCLE TIMING 1/64K only
(E Held Low)



READ CYCLE TIMING 2/64K only



8K, 16K, and 32K READCYCLE TIMING DIAGRAM

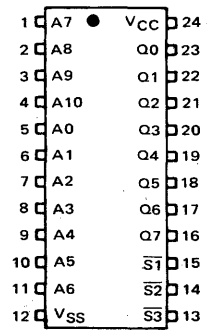


In addition to Motorola's upward compatible ROM family to other MPV, compatible ROMS are offered. All ROMs have compatible specifications (any execptions are noted). The 1Kx8 MCM6830A and 2Kx8 MCM68A316A pin assignments are shown below.

MCM68A316A

2048 X 8-BIT
READ ONLY MEMORY

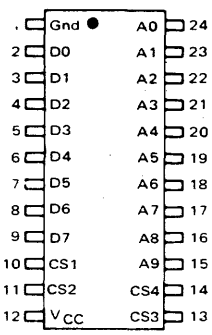
PIN ASSIGNMENT



MCM68A30A
MCM68B30A

1024 X 8-BIT
READ ONLY MEMORY

PIN ASSIGNMENT



PIN NAMES	
A0–A12	Address
$\overline{E}$	Chip Enable
Q0–Q7	Data Output
S	Chip Selects
V_{CC}	+5 V Power Supply
V_{SS}	Ground

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3501 ED BLUESTEIN BLVD., AUSTIN, TEXAS 78721

MCM146508
MCM146518

Advance Information

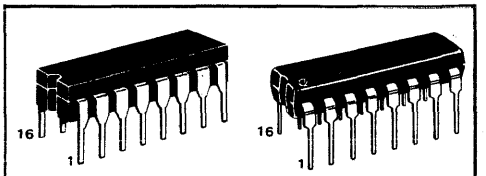
CMOS LSI
(LOW-POWER COMPLEMENTARY MOS)

1024 X 1 BIT STATIC RANDOM ACCESS MEMORY

1024 X 1 BIT STATIC RANDOM ADDRESS MEMORY

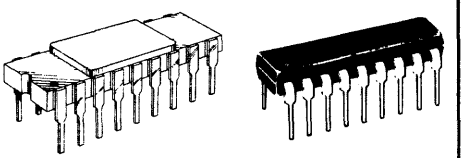
The MCM146508 and MCM146518 are fully static 1024 X 1 RAMS fabricated using high performance silicon gate CMOS technology. They offer low-power operation from a single 5.0 V supply with data retention to 2.0 V. The MCM146508 has the two select lines and the enable line brought out as a single enable line.

- Low Standby and Operating Power
- Single 5.0 V Supply
- Data Retention to 2.0 V
- Fast Access Time
- Address Latches
- Three-State Outputs
- Fully TTL Compatible Inputs/Outputs
- Fully Static Operation
- Direct Replacement for
  Harris HM6508/HM6518
  Intersil IM6508/IM6518



L SUFFIX
CASE 620

P SUFFIX
CASE 648



L SUFFIX
CASE 680

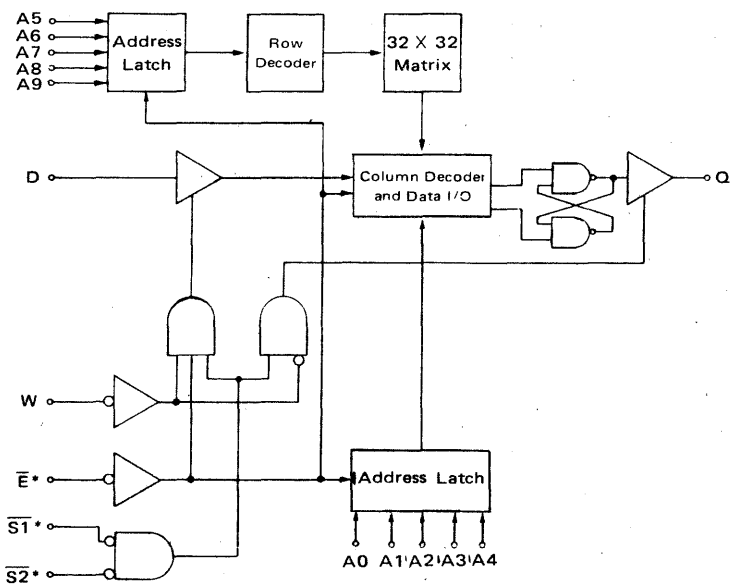
P SUFFIX
CASE 707

MCM14XXXX — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- See Table 1

TABLE 1

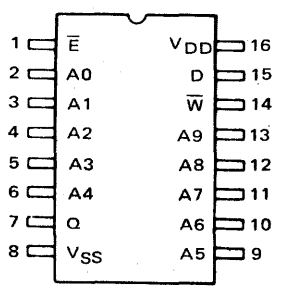
Type Number	Package Suffixes	Typical Current 2 Vdc	Typical Current 5 Vdc	Maximum Access Time	Operating Temperature Range
MCM146508/MCM146518	L/P	0.1 μA	5.0 μA	460 ns	-40 to +85°C
MCM146508-1/MCM146518-1	L/P	0.01 μA	1.0 μA	300 ns	-40 to +85°C
MCM146508-2/MCM146518-2	L	0.01 μA	1.0 μA	300 ns	-55 to +125°C

BLOCK DIAGRAM

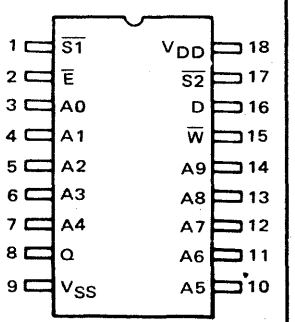


*For MCM146508 S1, S2 are connected to the $\overline{E}$ input.

PIN ASSIGNMENT



MCM146508



MCM146518

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MAXIMUM RATINGS (Voltages Referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	−0.5 to +7.0	Vdc
Input Voltage, All Inputs	V_{in}	−0.3 to V_{DD} + 0.3	Vdc
Operating Temperature Range MCM146508/MCM146518 MCM146508-1/MCM146518-1 MCM146508-2/MCM146518-2	T_A	 −40 to +85 −40 to +85 −55 to +125	°C
Storage Temperature Range	T_{stg}	−65 to +150	°C

CAPACITANCE

Characteristic	Symbol	Typ	Max	Unit
Input Capacitance (V_{in} = 0 V)	C_{in}	4.0	8.0	pF
Output Capacitance (V_{out} = 0 V)	C_{out}	8.0	12	pF

AC OPERATING CONDITIONS

Condition	Value
Input Pulse Levels	+0.8 V to V_{DD} − 2.0 V
Input Rise and Fall Times	20 ns
Output Load	1 TTL Gate and C_L = 50 pF
Timing Measurement Reference Level	1.5 V
Supply Voltage	5.0 V ± 10%
Temperature Range MCM146508/MCM146518 MCM146508-1/MCM146518-1 MCM146508-2/MCM146518-2	 −40°C to +85°C −40°C to +85°C −55°C to +125°C

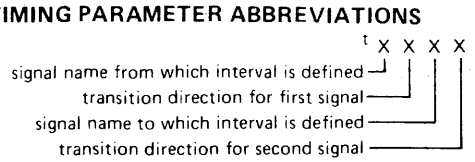
DC CHARACTERISTICS (V_{DD} = 5.0 V ±10%, T_A = 25°C)

Characteristic	Symbol	MCM146508-1 MCM146518-1			MCM146508 MCM146518			MCM146508-2 MCM146518-2			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Current	I_{in}	–	5.0	–	–	5.0	–	–	5.0	–	nAdc
Input High Voltage	V_{IH}	V_{DD} − 2.0	–	V_{DD}	V_{DD} − 2.0	–	V_{DD}	–	–	V_{DD}	Vdc
Input Low Voltage	V_{IL}	−0.3	–	0.8	−0.3	–	0.8	−0.3	–	0.8	Vdc
Output High Voltage (I_{OH} = −1.0 mA)	V_{OH}	2.4	–	–	2.4	–	–	2.4	–	–	Vdc
Output Low Voltage (I_{OL} = 2.0 mA)	V_{OL}	–	–	0.4	–	–	0.4	–	–	0.4	Vdc
Output Leakage Current (V_{OL} = 0 V to V_{DD})	I_{OL}	–	–	±1.0	–	–	±1.0	–	–	±1.0	μAdc
Standby Current (V_{IH} = $\overline{E}$ = $\overline{S1}$ = $\overline{S2}$ = V_{DD})	I_{DDSB}	–	0.1	10	–	1.0	100	–	1.0	100	nAdc
Data Retention Current (V_{DD} = 2.2 V = V_{IH} = $\overline{E}$ = $\overline{S1}$ = $\overline{S2}$)	I_{DDDR}	–	0.1	1.0	–	0.1	10	–	0.1	10	μAdc
Operating Current (t_{ELEH} = 1.0 μs)	I_{DDOP}	–	–	–	–	–	–	–	–	–	mAdc

AC CHARACTERISTICS

Parameter	Symbol	MCM146508-1 MCM146518-1		MCM146508-2 MCM146518-2		MCM146508 MCM146518		Unit
		Min	Max	Min	Max	Min	Max	
Read or Write Cycle Time	t_{ELEL}	500	–	500	–	760	–	ns
Enable Pulse Width, Low	t_{ELEH}	300	–	300	–	460	–	ns
Enable Pulse Width, High	t_{EHEL}	200	–	200	–	300	–	ns
Enable Access Time	t_{ELQV}	–	300	–	300	–	460	ns
Address Setup	t_{AVEL}	7.0	–	7.0	–	15	–	ns
Address Hold	t_{ELAX}	90	–	90	–	150	–	ns
Data Setup	t_{DVWH}	200	–	200	–	300	–	ns
Data Hold	t_{WHDX}	0	–	0	–	0	–	ns
Write Pulse Width	t_{WLWH}	200	–	200	–	300	–	ns
Write Enable to Output Disable	t_{WLQZ}	–	180	–	180	–	285	ns
Output Disable (MC146508 Only)	t_{EHQZ}	–	180	–	180	–	285	ns
Output Disable (MC146518 Only)	t_{SHQZ}	–	180	–	180	–	285	ns
Write Disable to Output Enable	t_{WHQX}	–	180	–	180	–	285	ns
Output Enable (MC146508 Only)	t_{ELQX}	–	180	–	180	–	285	ns
Output Enable (MC146518 Only)	t_{SLQX}	–	180	–	180	–	285	ns
Select to Write Pulse Setup	t_{WLSH}	200	–	200	–	300	–	ns
Select to Write Pulse Hold	t_{SLWH}	200	–	200	–	300	–	ns
Enable to Write Pulse Setup	t_{WLEH}	200	–	200	–	300	–	ns
Enable to Write Pulse Hold	t_{ELWH}	200	–	200	–	300	–	ns

TIMING PARAMETER ABBREVIATIONS



The transition definitions used in this data sheet are:

- H = transition to high
- L = transition to low
- V = transition to valid
- X = transition to invalid or don't care
- Z = transition to off (high impedance)

TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

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MOTOROLA
Semiconductors
3501 ED BLUESTEIN BLVD., AUSTIN, TEXAS 78721

MCM145101

256 X 4 BIT STATIC RAM

The MCM145101 family of CMOS RAMs offers ultra low power and fully static operation with a single 5 volt supply. The CMOS 1024-bit devices are organized in 256 words by 4 bits. Separate data inputs and data outputs permit maximum flexibility in bus-oriented systems. Data retention at a power supply as low as 2.0 volts over temperature readily allows design into applications using battery backup for nonvolatility. The MCM145101 is fully static and does not require clocking in standby mode.

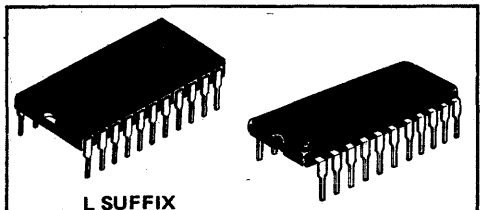
The MCM145101 is fabricated using the Motorola advanced ion-implanted, silicon-gate technology for high performance and high reliability.

- Low Standby Power
- Fast Access Time
- Single + 5.0 Volt Supply
- Fully TTL Compatible—All Inputs and Outputs
- Three-State Output
- Fully Static Operation
- Data Retention to 2.0 Volts
- Direct Replacement for:
  - Intel 5101 Series
  - AMI S5101 Series
  - Hitachi MH435101 Series
- Pin Replacement for Harris HM6501 Series

CMOS LSI

(LOW-POWER COMPLEMENTARY MOS)

1024-BIT STATIC RANDOM ACCESS MEMORY



L SUFFIX
CERAMIC PACKAGE
CASE 736

P SUFFIX
PLASTIC PACKAGE
CASE 708

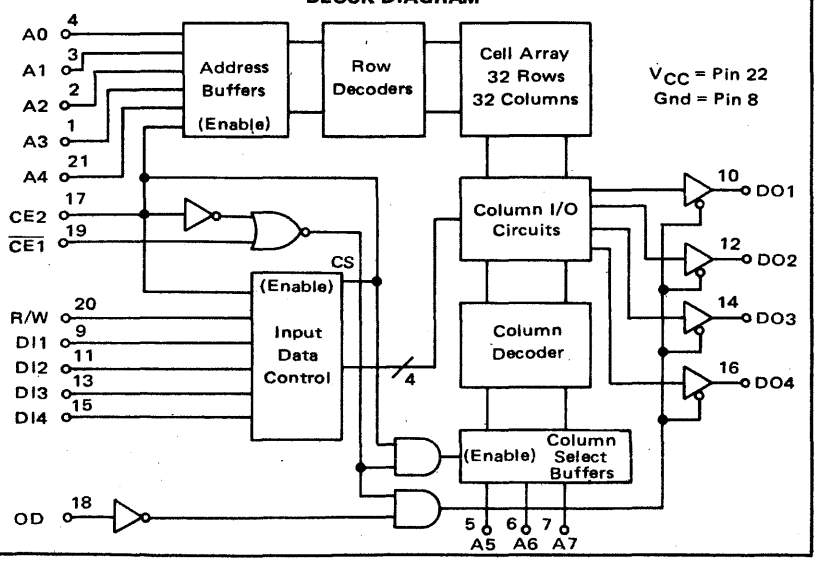
ORDERING INFORMATION

MCM14XXXX — Suffix Denotes
- L
- P
- -1
- -3
- -8
- (Not Used)

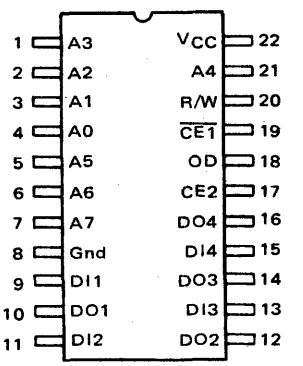
Selections for speed and power (see table)

Type Number	Typical Current @ 2 Vdc (μA)	Typical Current @ 5 Vdc (μA)	Max Access (ns)
MCM145101L, MCM145101P	0.14	0.2	650
MCM145101-1L, MCM145101-1P	0.14	0.2	450
MCM145101-3L, MCM145101-3P	0.70	1.0	650
MCM145101-8L, MCM145101-8P	–	10	800

BLOCK DIAGRAM



PIN ASSIGNMENT



TRUTH TABLE

$\overline{CE1}$	CE2	OD	R/W	D_{In}	Output	Mode
H	X	X	X	X	High Z	Not Selected
X	L	X	X	X	High Z	Not Selected
X	X	H	H	X	High Z	Output Disabled
L	H	H	L	X	High Z	Write
L	H	L	L	X	D_{In}	Write
L	H	L	H	X	D_{Out}	Read

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DS 9455 R1

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DC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature range unless otherwise noted)

DC CHARACTERISTICS (T_A = 0 to 70°C, V_{CC} = 5 V ±5%)

Characteristic	Symbol	MCM145101,-1			MCM145101-3			MCM145101-8			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Input Current	I_{in}(2)	–	5.0	–	–	5.0	–	–	5.0	–	nAdc
Input High Voltage	V_{IH}	2.2	–	V_{CC}	2.2	–	V_{CC}	2.2	–	V_{CC}	Vdc
Input Low Voltage	V_{IL}	-0.3	–	0.65	-0.3	–	0.65	-0.3	–	0.65	Vdc
Output High Voltage (I_{OH} = -1.0 mA)	V_{OH}	2.4	–	–	2.4	–	–	2.4	–	–	Vdc
Output Low Voltage (I_{OL} = 2.0 mA)	V_{OL}	–	–	0.4	–	–	0.4	–	–	0.4	Vdc
Output Leakage Current ($\overline{CE1}$ = 2.2 V, V_{OL} = 0 V to V_{CC})	I_{LO}(2)	–	–	±1.0	–	–	±1.0	–	–	±2.0	μAdc
Operating Current (V_{in} = V_{CC}, except $\overline{CE1}$ ≤ 0.65 V, outputs open)	I_{CC1}	–	9.0	22	–	9.0	22	–	11	25	mAdc
Operating Current (V_{in} = 2.2 V, except $\overline{CE1}$ ≤ 0.65 V, outputs open)	I_{CC2}	–	13	27	–	13	27	–	15	30	mAdc
Standby Current (CE2 ≤ 0.2 V)	I_{CCL}(2),(4)	–	–	10	–	–	200	–	–	500	μAdc

CAPACITANCE

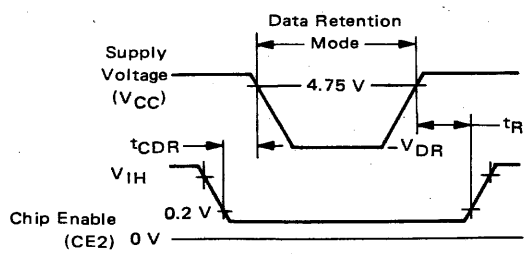
Characteristic	Symbol	Typ	Max	Unit
Input Capacitance (V_{in} = 0 V)	C_{in}	4.0	8.0	pF
Output Capacitance (V_{out} = 0 V)	C_{out}	8.0	12.0	pF

LOW V_{CC} DATA RETENTION CHARACTERISTICS (Excluding MCM145101-8) T_A = 0°C to 70°C

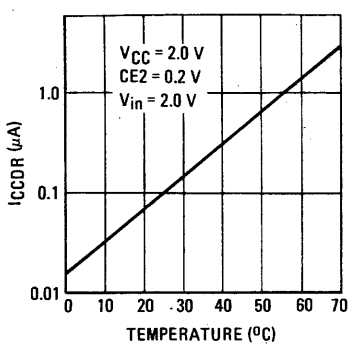
Parameter	Test Conditions		Symbol	Min	Typ.(1)	Max	Units
V_{CC} for Data Retention	CE2 ≤ 0.2 V		V_{DR}	2.0	–	–	Vdc
MCM145101 or MCM145101-1 Data Retention Current		V_{DR} = 2.0 V,	I_{CCDR1}	–	0.14	10	μAdc
MCM145101-3 Data Retention Current		V_{DR} = 2.0 V,	I_{CCDR2}	–	0.70	200	μAdc
Chip Deselect to Data Retention Time			t_{CDR}	0	–	–	ns
Operation Recovery Time			t_R	t_{RC}(3)	–	–	ns

NOTES: 1. Typical values are T_A = 25°C and nominal supply voltage.
2. Current through all inputs and outputs included in I_{CCL} measurement.
3. t_{RC} = Read Cycle Time.
4. Low current state is for CE2 = 0 only.

LOW V_{CC} DATA RETENTION WAVEFORM



TYPICAL I_{CCDR} versus TEMPERATURE



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AC OPERATING CONDITIONS AND CHARACTERISTICS

(Full operating voltage and temperature unless otherwise noted)

AC TEST CONDITIONS

Condition	Value
Input Pulse Levels	+0.65 V to 2.2 V
Input Rise and Fall Times	20 ns
Output Load —	1 TTL Gate and C_L = 100 pF
Timing Measurement Reference Level	1.5 Volt

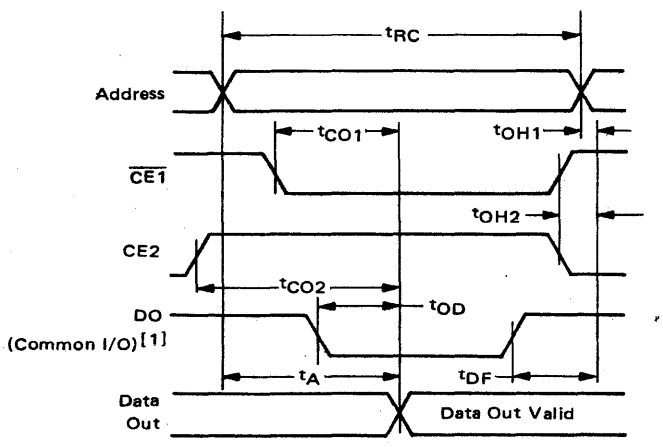
READ CYCLE

Parameter	Symbol	MCM145101-1		MCM145101,-3		MCM145101-8	
		Min	Max	Min	Max	Min	Max
Read Cycle	t_{RC}	450	–	650	–	800	–
Access Time	t_A	–	450	–	650	–	800
Chip Enable ($\overline{CE1}$) to Output	t_{CO1}	–	400	–	600	–	800
Chip Enable (CE2) to Output	t_{CO2}	–	500	–	700	–	850
Output Disable to Output	t_{OD}	–	250	–	350	–	450
Data Output to High Z State	t_{DF}	0	130	0	150	0	200
Previous Read Data Valid with Respect to Address Change	t_{OH1}	0	–	0	–	0	0
Previous Read Data Valid with Respect to Chip Enable	t_{OH2}	0	–	0	–	0	0

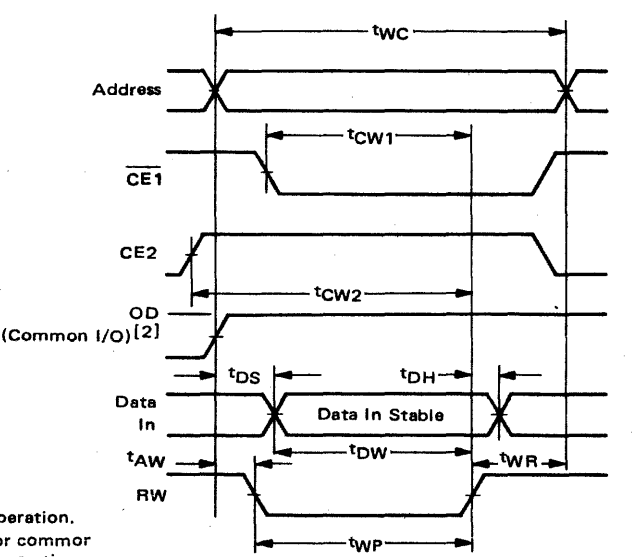
WRITE CYCLE

Write Cycle	t_{WC}	450	–	650	–	800	–
Write Delay	t_{AW}	130	–	150	–	200	–
Chip Enable ($\overline{CE1}$) to Write	t_{CW1}	350	–	550	–	650	–
Chip Enable (CE2) to Write	t_{CW2}	350	–	550	–	650	–
Data Setup	t_{DW}	250	–	400	–	450	–
Data Hold	t_{DH}	50	–	100	–	100	–
Write Pulse	t_{WP}	250	–	400	–	450	–
Write Recovery	t_{WR}	50	–	50	–	100	–
Output Disable Setup	t_{DS}	130	–	150	–	200	–

READ CYCLE TIMING



WRITE CYCLE TIMING



NOTES: 1. OD may be tied low for separate I/O operation.
2. During the write cycle, OD is "high" for common I/O and "don't care" for separate I/O operation.

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Future Memory Technology Development

National Semiconductor
Thomas Klein*
January 1978

ABSTRACT: Semiconductor integrated circuit based memory devices became the dominant Random Access Memory technology in less than 8 years. They were able to achieve this because their batch manufacturing process allowed a very rapid reduction of cost per bit of storage through technological changes to increase batch density. Continued progress in density improvement at essentially unchanged rates is still feasible. It will, however, require major changes in manufacturing, device and material technology.

Since the beginning of the 70's, semiconductor integrated circuits used as digital storage elements have become a very significant factor in the total spectrum of information storage technology. They became the dominant technology for random access memories and are beginning to make inroads into the slower serial access memory market, presently dominated by magnetic discs and drums.

The ability of integrated circuit technology to continue to offer digital data storage at very rapidly decreasing cost per bit of storage is a consequence of the batch manufacturing process. It allows introductions of new products which are cost effective even at very low manufacturing efficiency level, obtain very steep cost reduction during product life by rapid increase of manufacturing efficiency and continue to stay on the steep cost reduction curve by going to a higher level of integration when cost improvements through improved manufacturing efficiencies are starting to flatten out.

However, to go to a higher level of integration, which in case of Random Access Memory circuits, usually means a four-fold increase in number of bits on the chip, a significant improvement in batch density is required, otherwise no benefit is derived *(Figure 1)*.

This batch density (i.e., number of potentially good storage elements processed together as a single unit (i.e., a silicon wafer) has shown an even higher rate of growth than the much more visible increase in the number storage bits/memory circuit.

During the past eight years the number of potentially good storage elements contained on a single silicon wafer has risen from about 50,000 to over 6 million, with the cost of processing a wafer rising only very slowly and manufacturing efficiency expressed as the percentage of good units staying level or improving slightly.

Future progress in memory technology can be examined in terms of this single variable common to all present and future solid state memory technologies.

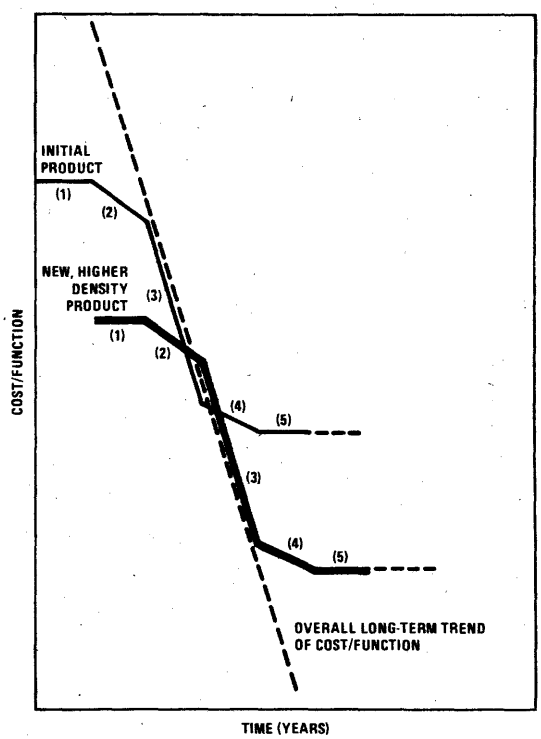
There are several technological trends that are unfolding right now which are likely to impact future memory technology developments.

These trends can be classified under the following categories:

a. Continued evolutionary process of memory cost reduction through more advanced circuit and device design techniques and improved process and manufacturing efficiencies.

b. A significant change in device and circuit sizes through major changes in pattern definition technology and an electrical scaling of devices to take advantage of the size reduction.

c. Charge Coupled Device and Magnetic Bubble Domain device based memory technologies.



NOTES:
(1) Product is introduced, very little or no competition.
(2) Product is multiple sourced but prices still hold up as production is limited.
(3) Production expands dramatically as yields improve, competition is fierce, prices tumble, marginal suppliers are beginning to drop out.
(4) Significant yield improvements are no longer available, new product is beginning to compete for the same market, competition is still intense, suppliers still drop out.
(5) Major market share is taken by new generation of product, market shrinks but prices hold up as competition is minimal.

FIGURE 1. Typical Decrease of Memory Products' Prices/Costs During Product Life

*Refer to Introduction. This paper presented at COMPCON 1977

"TURN TO PAGES 270-285 FOR FULL APPLICATION NOTE"

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a. EVOLUTIONARY PROCESS

This approach has so far been the most successful and continued improvements may still be expected. In fact, as long as this is a viable path for future development, it is likely to be the most vigorously pursued approach.

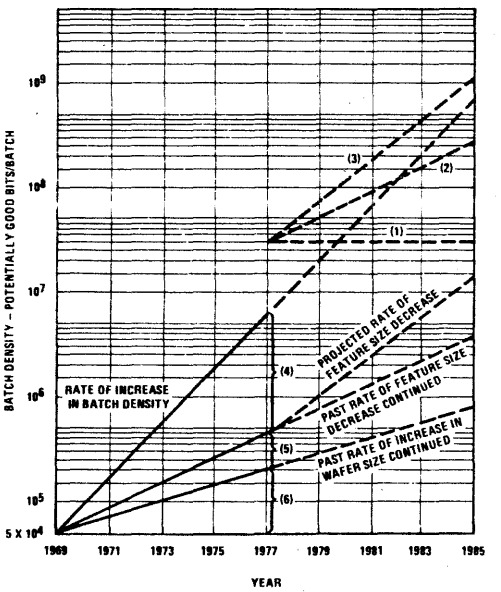
In terms of its future potential, we might examine past contributions to batch density improvements.

The total batch density improvement of 120-fold in eight years was contributed by:

1. Higher bit density through design and process innovation: 13.5x
2. Larger wafer area: 4x
3. Smaller feature sizes and tighter alignment tolerances: 2.2x

Continued improvement based on comparable contributions from the same sources is no longer feasible for the following reasons:

Design and process improvements, the most profitable source of past batch density improvement, is getting sufficiently close to its theoretical limits so that progress in it is likely to slow down *(Figure 2)*. It is clear that regardless of whatever technique we use to design or build a memory cell, it must have at least 2 features in both x and y directions, one to store the information and one to separate it from the adjacent cell. This defines a theoretical minimum cell size of 4 f^2 where f is the minimum feature size determined by the limits of pattern definition technology.



NOTES:
(1) Theoretical limit, current wafer and feature sizes.
(2) Theoretical limit, assuming continued improvements in wafer size increase and feature size reduction.
(3) Theoretical limit, assuming constant rate of wafer size increase and an *increasing* rate of feature size reduction.
(4) Increase due to design and process innovations.
(5) Increase due to feature size improvement.
(6) Increase due to wafer size.

FIGURE 2. Past and Projected Contributions to Batch Density Improvements

Cell size eight years ago was a rich 200 f^2 leaving plenty of room for improvement. Today's cell size of 20 f^2 or less is sufficiently close to the theoretical limit of 4 f^2 that we can no longer project a rate of improvement comparable to past norms. We will do extremely well if we can extract a further 3-fold improvement.

Wafer size improvement will continue at an essentially constant rate. Wafer size increases are important not only for increased productivity, but wafer size is strongly correlated to maximum economically manufacturable die size *(Figure 3)*. Wafer diameter has been increasing at a rate of about 1.4 times every four years. This rate of increase is tied not only to the rate at which equipment manufacturers can develop new tooling to handle the larger wafer size, but also to the rate at which capital is invested in the semiconductor industry.

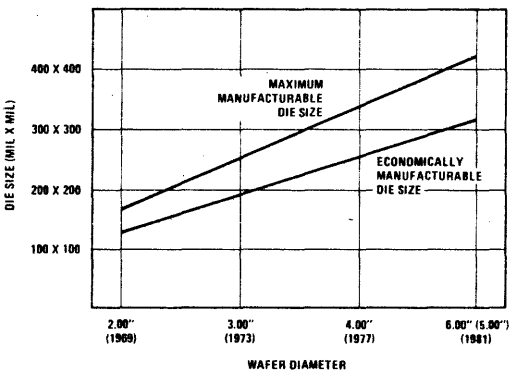


FIGURE 3. Maximum and Economic Die Size as a Function of Wafer Diameter (Time)

Feature size reduction. While we expect significant progress in this area, little of it can be considered evolutionary. In the past, progress in this area was completely evolutionary; contributing relatively little to density improvement. In the next 5 to 10 years we expect major changes in the technology and we will discuss those changes in detail later.

We also expect that manufacturing yields will increase in the next 5 to 10 years. This will be a factor in cost reduction but not in density.

The reason for yield improvement is the expected reduction in the rate of density improvement due to design and process improvements. Present manufacturing yields which include losses in wafer manufacturing, die sort, assembly and final test vary from under 5% for a leading edge product to about 25% for a mature product.

In the past, as long as significant density improvements were available from design and process innovations, engineering effort and talent was better utilized in trying to improve a new high density product's yield from 5% to 25%. Trying to extract the yield improvement available between 25% and 50%–60% which is

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probably the practical upper limit for any semiconductor product, was both harder and less rewarding. With less potential improvement available from design and process innovations, we can probably expect higher overall yields for mature products.

In summary, the evolutionary trend, while it will still contribute significantly to future cost reductions, its contribution will be proportionately less than it has been in the past.

b. FEATURE SIZE IMPROVEMENT

Minimum feature size has been remarkably stable over the past 20 years of integrated circuit technology development. This was probably due to the fact that there was very little change in pattern definition technology. Up to 1975 the pattern definition technology, at least at wafer level, was basically unchanged from what it was in the late 50's and progress was obtained by better engineering, controlling and understanding the process and using improved photochemical materials.

Maskmaking technology made much more consistent progress, converting from an essentially manual drafting to a completely computerized pattern definition process.

Since the mid-70's, very significant changes are beginning to occur at wafer level too. Availability and acceptance of *projection aligners* is the first and probably the most significant of these changes.

Their introduction did not lead to an immediate reduction in feature size, but the control, reproducibility and accuracy of mask dimensions that they allow, makes feature size reduction a much more realistic task.

Improved high resolution photoresists are also becoming available.

Dry etching techniques are important technological achievements and will also be contributing to feature size reduction.

Electron beam and X-ray lithography are the most frequently mentioned technologies to achieve significant reductions in feature size.

There is undoubtedly significant progress being made in these areas and some of the results are impressive. However, they have to overcome some very significant technical and economic hurdles before they can make an impact on memory technology *(Figure 4)*.

Electron beam writing techniques are already available for maskmaking purposes where they offer some very real advantages. For direct writing on wafers, however, they still have to improve significantly and come down in price before they can make an impact on memory technology. Presently, projected machine costs and throughput times are such that processing wafers with electron beam writing instead of conventional masking—assuming no other technical problems—would raise wafer processing cost by a factor of 5. This cost increase would take care of all cost reduction achieved by the smaller feature size at *equal yield*. Since the smaller feature size means more densely built circuits sensitive to much smaller defect sizes the most immediate consequence of feature size reduction is yield reduction.

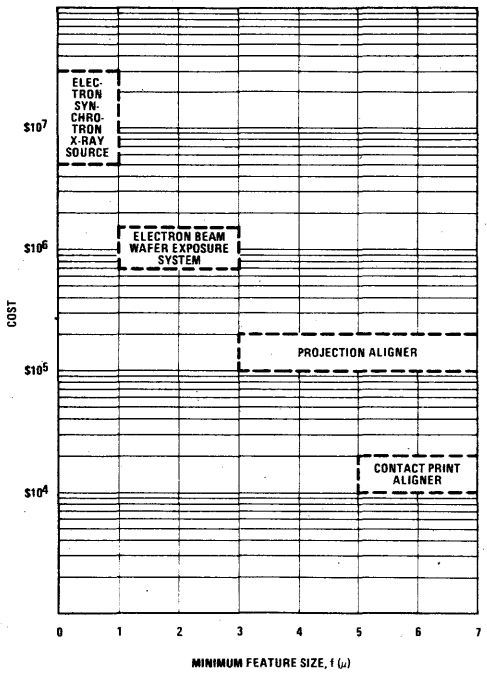


FIGURE 4. Cost of Key Equipment for Various Pattern Definition Technologies and Minimum Feature Sizes

X-ray lithography techniques have still to resolve three basic problems.

a. Maskmaking technology

b. Sufficiently intensive X-ray sources

c. Pattern registration

If they can solve these problems, they can be potentially very powerful as they can use a fixed mask and do not have to regenerate the entire pattern at every exposure.

Summarizing present status of pattern definition technologies, we can project improvements in optical pattern definition technology to yield a 5 to 8-fold increase in batch density over the next 5 to 8 years. This will represent a 2.5 to 4-fold increase in the rate of progress compared to past experience. Even higher rates of progress are possible if electron beam and/or X-ray lithography matures sufficiently to become cost effective, over the next 5 to 8 years.

Electrical Scaling of Devices

In the previous discussion, we have made the implicit assumption that feature size reduction is equivalent to circuit area reduction.

This is most certainly not the case. Feature size reduction will merely define limits to circuit size reduction. The actual reduction available will be determined by how closely the electrical device and circuit characteristics allow us to approach the limits imposed by pattern definition technology.

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All three presently used major memory technologies (i.e., MOS dynamic, MOS static and bipolar static) are more limited by device and circuit design considerations, rather than optical pattern resolution.

In case of MOS devices, their performance is a function of the operating voltages and their ability to handle high operating voltages decreases very rapidly with reduced device sizes. Consequently, if denser memory circuits were to be built by taking advantage of feature size reduction, the operating voltages will have to be reduced. The resulting device and circuit performance reduction can be regained by re-engineering the entire device, reducing oxide thickness, junction depth and increasing substrate doping to make the device deliver an equivalent performance at lower operating voltages.

This total re-engineering of device structure, processing and manufacturing technology is called "scaling" and it is obviously a major engineering and manufacturing task, involving all aspects of wafer technology.

Bipolar memory circuits do not appear to suffer from this limitation; their's is, however, a different one. Device sizes can be reduced but their density cannot be significantly increased, because current drain of a bipolar device does not scale with size. Consequently, any attempt to take advantage of reduced device size by increasing number of bits/chip will run into severe power dissipation limits. Again the problem is technically solvable at an expense of major circuit design/process re-engineering efforts to "current scale" bipolar device/process technology.

I^2L technology appears technically attractive from this point of view (i.e., it would be able to take advantage of feature size reduction with the least amount of device and/or process engineering changes). Its problem is that it has so far not been able to establish a sufficiently attractive price/performance combination to gain a significant position in the memory market.

Feature size reduction and the required electrical scaling of devices will have some very important consequences in terms of relative impact on various memory technologies. When we scale devices, we adjust some basic device parameters and operating voltages so as to obtain as nearly identical device and circuit characteristics as possible. This can be achieved quite successfully for the type of circuits whose design is by and large based on the device characteristics that we have scaled (i.e., MOS static devices). For these devices, reduction of supply voltage also brings about a reduction in power dissipation, so one limitation to higher density, characteristic of static devices has also been removed.

MOS dynamic circuits which have traditionally enjoyed a 4:1 density advantage over static devices, rely more on second order effects like leakage currents, subthreshold conduction and signal to noise ratio in their sense amplifier designs, do not benefit quite as readily from scaling.

Leakage current, whose relation to stored charge is vitally important to the successful operation of MOS dynamic random access memory circuits, does not scale proportionately with voltage, due the point defect nature of the leakage current. Typically any junction's leakage current represents a spatial averaging over a relatively large number of defects. Reducing junction area will increase fluctuation in number of defect sites from one storage area to the next. Since dynamic RAM design imposes requirement that *all* storage areas have less than certain pre-determined amount of leakage current, scaling will typically reduce ratio of stored charge to leakage current. Since the signal available is already reduced by both scaling and the resulting increase in density, designers of future generation of dynamic RAM's face some formidable challenges. It is possible that the only way they will be able to overcome these challenges is to impose very strict environmental limitations on the finished product, namely cooling or even refrigeration of memory systems.

Feature size reduction and electrical scaling will impose some very stringent demands on process engineering in terms of both control and the degree of perfection required for good yields from the scaled structures. We are assuming that these problems are solvable by evolutionary improvements in processing techniques. We should not be surprised, however, if progress in those areas from time to time fails to keep up with the more visible improvements available from pattern definition technology.

c. NEW TECHNOLOGIES

Success in semiconductor integrated circuit based random access memory technology prompted considerable interest in solid state replacements for serial memories. The two most often considered candidates are Charge Coupled Devices and Bubble Domain Memory devices.

Charge Coupled Devices represent the densest silicon based technology we know. However, their speed and ease of use is considerably inferior to random access memories and as long as random access memories can be made with comparable circuit density, C.C.D. is hard pressed to carve out a market position. Typically, for a C.C.D. circuit to be competitive with RAMs, it has to offer a 4:1 density advantage over a comparably sized RAM circuit. So far it has not been able to do it, partly because RAM technology very quickly adopted all process improvements made for C.C.D. circuits and used them to make competitively sized RAMs.

However, C.C.D. technology is expected to establish a 4:1 density advantage over RAMs in the reasonably near future because its technology and organization permits:

a. Approaching the theoretical minimum storage area of 4 f^2 both more easily and more closely than RAMs.

b. Meeting the challenges of feature size reduction and device scaling more easily than dynamic RAM's.

Several features of C.C.D. technology contribute to these advantages. Absence of P-N junctions allows storage and transfer functions to be very similar structurally and either very closely spaced, or used interchangeably for both functions.

Although charge is stored dynamically, it is not held at any location for longer than a clock cycle so effect of

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defect density fluctuation is averaged out over a large area. Signal strength is comparable to RAM's but there is more flexibility in sense amplifier design. Absence of contacts and P-N junctions allows more efficient layout and easier scaling of devices.

Bubble Memory Technology

Although both its device and material technology is significantly different from silicon integrated circuits, it is also based on a batch manufacturing process with the cost of a function very strongly dependent of the functional density per batch and manufacturing yields.

Examined from this point of view, it has some very major disadvantages coupled with some even greater potential long-term benefits.

First of all, as a device it is very well suited to serial storage of data. Although it is slower than any silicon I.C. based storage circuit, it is non-volatile—or at least it can be designed to be—and it can also be used to perform very simple logic functions which allow data to be stored and retrieved efficiently. Also, it can be used to pre-amplify the otherwise very small signal magnetically so it can be used to design a reasonably self-contained memory chip.

Its known major disadvantages are:

1. Very high material cost, caused by both very high initial substrate cost and a very costly, difficult and low productivity liquid phase epitaxy deposition process. Material cost is 30—50 times higher than silicon.
2. Very high packaging cost. Every circuit has to have an individually adjusted bias field and a rotating magnetic field built into the package.
3. A batch density which is presently not significantly higher than what is achievable with silicon.

Set against these disadvantages we can consider the potential long-term benefits which motivate the ever increasing activity in the field:

1. Processing typically requires only 3 masking steps, only one of which is critical, compared to 6+ for silicon.
2. Although present bit density is not impressive, it is based on a relatively simple design with bit area being in the 200 f^2 region for a T bar configuration, indicating very much room for improvement, some of which has already been implemented experimentally.
3. Because it has only one critical masking step and no critical alignment requirements, it is the technology best positioned to take advantage of improvements in pattern definition techniques.

It is difficult today to determine the point both in time and in level of complexity at which Bubble Memory Devices will be able to enter the market and compete successfully. But once they do, they will enjoy a very rapid growth comparable to silicon integrated circuit based memory circuits for exactly the same reasons.

Summarizing these trends, there is sufficient visibility for the continued technical progress of memory technology at essentially unchanged rates for the next 5 to 8 years.

One word of caution, however, is worth mentioning here. The key to past success and the continued objective of memory technology development is *cost reduction*.

Technical developments to continue to increase density of memory circuits are worthwhile only if they can make a significant contribution to this overall objective. They cannot do it if the cost of improvement is so high that it swallows up all future cost benefits.

Even if their cost is less than potential cost reduction benefit, they still represent a very significant investment in design, process development, production and testing facilities and product start-up costs for the component manufacturer.

Such an investment will only be economically attractive if the market for memory products continues to expand at a fast rate.

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National Semiconductor

MOS RAMs

MM5290 16,384-Bit (16,384 × 1) Dynamic RAM

General Description

The MM5290 is a 16,384 x 1 bit dynamic RAM. It features a multiplexed address input with separate row and column strobes. This added flexibility allows the MM5290 to be used in page mode operation.

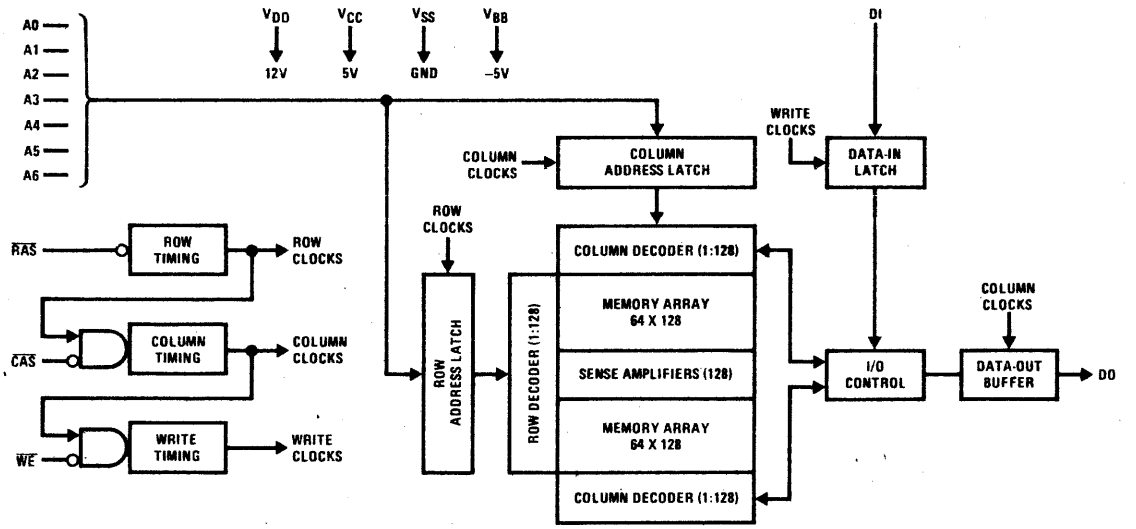
The MM5290 must be refreshed every 2 ms. This can be accomplished by performing any cycle which brings the Row Address Strobe active including a $\overline{RAS}$-only cycle at each of the 128 row addresses.

N-channel double-poly silicon gate technology, developed by National, is used in the manufacture of the MM5290. This process combines high density and performance with reliability. Greater system densities are achievable by the use of a 16-pin dual-in-line package for the MM5290.

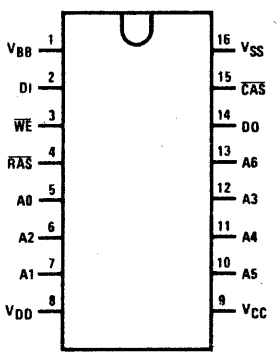
Features

- Access times: 150 ns, 200 ns, 250 ns
- Low power: 528 mW max
- TTL compatible: all inputs and output
- Gated $\overline{CAS}$—noncritical timing
- Read, Write, Read-Modify-Write and $\overline{RAS}$-only Refresh cycles
- Page mode operation
- Industry standard 16-pin configuration

Block and Connection Diagrams



Dual-In-Line Package



TOP VIEW

Order Number MM5290J
See NS Package J16A

Pin Names

$\overline{RAS}$	Row Address Strobe
$\overline{CAS}$	Column Address Strobe
$\overline{WE}$	Write Enable
A0—A6	Address Inputs
DI	Data Input
DO	Data Output
V_{DD}	Power (12V)
V_{CC}	Power (5V)
V_{SS}	Ground
V_{BB}	Power (−5V)

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Absolute Maximum Ratings (Note 1)

Operating Temperature Range	0°C to +70°C	Voltage on Any Pin Relative to V_{BB}	−0.3V to +20V
Storage Temperature	−65°C to +150°C	($V_{SS} - V_{BB} \geq 4.5V$)	
Power Dissipation	1W	Lead Temperature (Soldering, 10 seconds)	300°C

Recommended DC Operating Conditions

SYMBOL	PARAMETER	MIN	MAX	UNITS	NOTES
T_A	Ambient Temperature	0	70	°C	
V_{DD}	Supply Voltages	10.8	13.2	V	2, 3
V_{CC}		4.5	5.5	V	2, 3
V_{SS}		0	0	V	2, 3
V_{BB}		−4.5	−5.5	V	2, 3
V_{IHC}	Input High Voltage, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$	2.7	7.0	V	2
V_{IH}	Input High Voltage, A0–A6, DI	2.4	7.0	V	2
V_{IL}	Input Low Voltage, All Inputs	−1.0	0.8	V	2

DC Electrical Characteristics

Over the range of Recommended DC Operating Conditions unless otherwise noted

SYMBOL	PARAMETER	MIN	MAX	UNITS	NOTES
I_{DD1}	**Operating Current**		40	mA	4
I_{CC1}	Average Power Supply Operating Current				5
I_{BB1}	($\overline{RAS}$, $\overline{CAS}$ Cycling; $t_{RC} = t_{RC}$ MIN)		200	μA	
I_{DD2}	**Standby Current**		1.5	mA	
I_{CC2}	Power Supply Standby Current ($\overline{RAS} = V_{IHC}$,	−10	10	μA	
I_{BB2}	DO = High Impedance)		100	μA	
I_{DD3}	**Refresh Current**		30	mA	4
I_{CC3}	Average Power Supply Current, Refresh Mode	−10	10	μA	
I_{BB3}	($\overline{RAS}$ Cycling, $\overline{CAS} = V_{IHC}$; $t_{RC} = t_{RC}$ MIN)		200	μA	
I_{DD4}	**Page Mode Current**		32	mA	4
I_{CC4}	Average Power Supply Current, Page Mode				5
I_{BB4}	($\overline{RAS} = V_{IL}$, $\overline{CAS}$ Cycling; $t_{PC} = 225$ ns)		200	μA	
$I_{I(L)}$	**Input Leakage**	−10	10	μA	
	Input Leakage Current, Any Input				
	($V_{BB} = -5V$, $0V \leq V_{IN} \leq 7V$, All Other				
	Pins not Under Test = 0V)				
$I_{O(L)}$	**Output Leakage**	−10	10	μA	
	Output Leakage Current (DO is Disabled,				
	$0V \leq V_{OUT} \leq 5.5V$)				
	Output Levels				
V_{OH}	Output High Voltage ($I_{OUT} = -5$ mA)	2.4		V	
V_{OL}	Output Low Voltage ($I_{OUT} = 4.2$ mA)		0.4	V	
CAPACITANCE					
C_I	Input Capacitance A0–A6, DI		5	pF	6
C_C	Input Capacitance $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$		10	pF	6
C_O	Output Capacitance, DO		7	pF	6

Note 1: "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. Except for "Operating Temperature Range" they are not meant to imply that the devices should be operated at these limits. The table of "Recommended DC Operating Conditions" provides conditions for actual device operation.

Note 2: All voltages referenced to V_{SS}. When applying voltages to the device, V_{DD}, V_{CC} or V_{SS} should never be 0.3V more negative than V_{BB}.

Note 3: Several cycles are required after power-up before proper device operation is achieved. Any 8 RAS cycles are adequate for this purpose.

Note 4: I_{DD1}, I_{DD3}, and I_{DD4} depend on cycle rate.

Note 5: I_{CC} depends on output load.

Note 6: Capacitance measured with Boonton Meter or effective capacitance calculated from the equation $C = I\Delta t/\Delta V$. Capacitance is guaranteed by periodic testing.

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AC Electrical Characteristics

Over the range of Recommended DC Operating Conditions unless otherwise noted

SYMBOL	PARAMETER	MM5290-2		MM5290-3		MM5290-4		UNITS	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX		
t_{RC}	Random Read or Write Cycle Time	375		375		410		ns	7, 8
t_{RWC}	Read-Write Cycle Time	375		375		515		ns	7, 8
t_{PC}	Page Mode Cycle Time	170		225		275		ns	
t_{RAC}	Access Time from $\overline{RAS}$		150		200		250	ns	9, 11
t_{CAC}	Access Time from $\overline{CAS}$		100		135		165	ns	10, 11
t_{OFF}	Output Buffer Turn-Off Delay	0	40	0	50	0	60	ns	12
t_T	Transition Time (Rise and Fall)	3	35	3	50	3	50	ns	
t_{RP}	$\overline{RAS}$ Precharge Time	100		120		150		ns	
t_{RAS}	$\overline{RAS}$ Pulse Width	150	10,000	200	10,000	250	10,000	ns	
t_{RSH}	$\overline{RAS}$ Hold Time	100		135		165		ns	
t_{CSH}	$\overline{CAS}$ Hold Time	150		200		250		ns	
t_{CAS}	$\overline{CAS}$ Pulse Width	100	10,000	135	10,000	165	10,000	ns	
t_{RCD}	$\overline{RAS}$ to $\overline{CAS}$ Delay Time	20	50	25	65	35	85	ns	9
t_{CRP}	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	−20		−20		−20		ns	
t_{ASR}	Row Address Set-Up Time	0		0		0		ns	
t_{RAH}	Row Address Hold Time	20		25		35		ns	
t_{ASC}	Column Address Set-Up Time	−10		−10		−10		ns	
t_{CAH}	Column Address Hold Time	45		55		75		ns	
t_{AR}	Column Address Hold Time Referenced to $\overline{RAS}$	95		120		160		ns	
t_{RCS}	Read Command Set-Up Time	0		0		0		ns	
t_{RCH}	Read Command Hold Time	0		0		0		ns	
t_{WCH}	Write Command Hold Time	45		55		75		ns	
t_{WCR}	Write Command Hold Time Referenced to $\overline{RAS}$	95		120		160		ns	
t_{WP}	Write Command Pulse Width	45		55		75		ns	
t_{RWL}	Write Command to $\overline{RAS}$ Lead Time	60		80		100		ns	
t_{CWL}	Write Command to $\overline{CAS}$ Lead Time	60		80		100		ns	
t_{DS}	Data-In Set-Up Time	0		0		0		ns	13, 14
t_{DH}	Data-In Hold Time	45		55		75		ns	13, 14
t_{DHR}	Data-In Hold Time Referenced to $\overline{RAS}$	95		120		160		ns	
t_{CP}	$\overline{CAS}$ Precharge Time (for Page Mode Cycle Only)	60		80		100		ns	
t_{REF}	Refresh Period		2		2		2	ms	
t_{WCS}	$\overline{WE}$ to $\overline{CAS}$ Set-Up Time	−20		−20		−20		ns	14
t_{CWD}	$\overline{CAS}$ to $\overline{WE}$ Delay	70		95		125		ns	15
t_{RWD}	$\overline{RAS}$ to $\overline{WE}$ Delay	120		160		200		ns	15

Note 7: The specifications for $t_{RC(MIN)}$ and $t_{RWC(MIN)}$ are used only to indicate cycle time at which proper operation over the full temperature range is guaranteed.

Note 8: Transition times are measured between V_{IHC} or V_{IH} and V_{IL}. Timing measurements are made between $V_{IHC(MIN)}$ or $V_{IH(MIN)}$ and $V_{IL(MAX)}$, and assume t_T = 5 ns.

Note 9: Assumes row-limited access, i.e., $t_{RCD} \leq t_{RCD(MAX)}$. If this condition is not satisfied, then note 10 applies.

Note 10: Assumes column-limited access, i.e., $t_{RCD} > t_{RCD(MAX)}$.

Note 11: Equivalent load is 2 standard TTL inputs plus 100 pF.

Note 12: $\overline{CAS}$ going high disables the Data Output. t_{OFF} is the delay to the high impedance state.

Note 13: These parameters are referenced to the negative edge of $\overline{CAS}$ in an early-write cycle and to the negative edge of $\overline{WE}$ in a Read-Modify-Write cycle. (See Note 12, below).

Note 14: If $t_{WCS} \geq t_{WCS(MIN)}$, the Data Output is guaranteed to remain in the high impedance state for the duration of the cycle. This is the "early-write" cycle.

Note 15: If $t_{CWD} \geq t_{CWD(MIN)}$ and $t_{RWD} \geq t_{RWD(MIN)}$, the Data Output will contain the original data in the selected cell. This is the Read-Modify-Write cycle. If either of these conditions is not satisfied, the output will be indeterminate unless the early-write condition of Note 12 is met.

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NEC

μPD411-E
μPD411
μPD411-1
μPD411-2
μPD411-3
μPD411-4

FULLY DECODED RANDOM ACCESS MEMORY

DESCRIPTION

The μPD411 Family consists of six 4096 words by 1 bit dynamic N-channel MOS RAMs. They are designed for memory applications where very low cost and large bit storage are important design objectives. The μPD411 Family is designed using dynamic circuitry which reduces the standby power dissipation.

Reading information from the memory is a non-destructive. Refreshing is easily accomplished by performing one read cycle on each of the 64 row addresses. Each row address must be refreshed every two milliseconds. The memory is refreshed whether Chip Select is a logic high or a logic low.

FEATURES

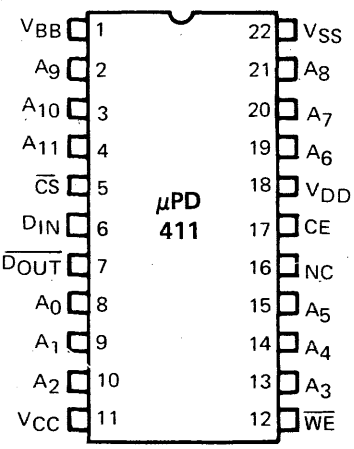
All of these products are guaranteed for operation over the 0 to 70°C temperature range.

Important features of the μPD411 family are:

- Low Standby Power
- 4096 words x 1 bit Organization
- A single low-capacitance high level clock input with solid ±1 volt margins.
- Inactive Power/0.3 mW (Typ.)
- Power Supply: +12, +5, -5V
- Easy System Interface
- TTL Compatible (Except CE)
- Address Registers on the Chip
- Simple Memory Expansion by Chip Select
- Three State Output and TTL Compatible
- 22 pin Ceramic Dual-in-Line Package
- Replacement for INTEL'S 2107B, TI'S 4060 and Equivalent Devices.
- 4 Performance Ranges:

	ACCESS TIME	R/W CYCLE	RMW CYCLE	REFRESH TIME
μPD411-E	350 ns	800 ns	960 ns	1 ms
μPD411	300 ns	470 ns	650 ns	2 ms
μPD411-1	250 ns	470 ns	640 ns	2 ms
μPD411-2	200 ns	400 ns	520 ns	2 ms
μPD411-3	150 ns	380 ns	470 ns	2 ms
μPD411-4	135 ns	320 ns	320 ns	2 ms

PIN CONFIGURATION



PIN NAMES

$A_0 - A_{11}$	Address Inputs
$A_0 - A_5$	Refresh Addresses
CE	Chip Enable
$\overline{CS}$	Chip Select
D_{IN}	Data Input
$\overline{D_{OUT}}$	Data Output
$\overline{WE}$	Write Enable
V_{DD}	Power (+12V)
V_{CC}	Power (+5V)
V_{SS}	Ground
V_{BB}	Power
NC	No Connection

Rev/2

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FUNCTIONAL DESCRIPTION

CE Chip Enable

A single external clock input is required. All read, write, refresh and read-modify-write operations take place when chip enable input is high. When the chip enable is low, the memory is in the low power standby mode. No read/write operations can take place because the chip is automatically precharging.

$\overline{CS}$ Chip Select

The chip select terminal affects the data in, data out and read/write inputs. The data input and data output terminals are enabled when chip select is low. The chip select input must be low on or before the rising edge of the chip enable and can be driven from standard TTL circuits. A register for the chip select input is provided on the chip to reduce overhead and simplify system design.

$\overline{WE}$ Write Enable

The read or write mode is selected through the write enable input. A logic high on the $\overline{WE}$ input selects the read mode and a logic low selects the write mode. The $\overline{WE}$ terminal can be driven from standard TTL circuits. The data input is disabled when the read mode is selected.

A_0–A_{11} Addresses

All addresses must be stable on or before the rising edge of the chip enable pulse. All address inputs can be driven from standard TTL circuits. Address registers are provided on the chip to reduce overhead and simplify system design.

D_{IN} Data Input

Data is written during a write or read-modify-write cycle while the chip enable is high. The data in terminal can be driven from standard TTL circuits. There is no register on the data in terminal.

$\overline{D_{OUT}}$ Data Output

The three state output buffer provides direct TTL compatibility with a fan-out of two TTL gates. The output is in the high-impedance (floating) state when the chip enable is low or when the Chip Select input is high. Data output is inverted from data in.

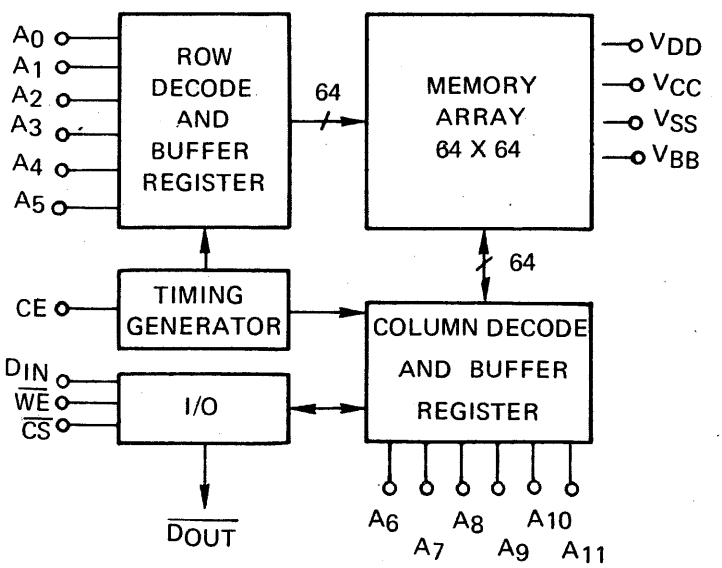
Refresh

Refresh must be performed every two milliseconds by cycling through the 64 addresses of the lower-order-address inputs A_0 through A_5 or by addressing every row within any 2*-millisecond period. Addressing any row refreshes all 64 bits in that row.

The chip does not need to be selected during the refresh. If the chip is refreshed during a write mode, the chip select must be high.

*μPD411-E = 1 millisecond refresh period.

BLOCK DIAGRAM



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ABSOLUTE MAXIMUM RATINGS*

	μPD411 FAMILY (EXCEPT 411-4)	μPD411-4
Operating Temperature	0°C to +70°C	+10°C to +55°C
Storage Temperature	−55°C to +150°C	−55°C to +150°C
All Output Voltages	−0.3 to +20 Volts	−0.3 to +25 Volts ①
All Input Voltages	−0.3 to +20 Volts	−0.3 to +25 Volts ①
Supply Voltage V_{DD}	−0.3 to +20 Volts	−0.3 to +25 Volts ①
Supply Voltage V_{CC}	−0.3 to +20 Volts	−0.3 to +25 Volts ①
Power Dissipation	1.0W	1.5W

Note: ① Relative to V_{BB}

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

DC CHARACTERISTICS

T_a = 0°C to 70°C, V_{DD} = +12V ±5%, V_{CC} = +5V ±5%, V_{BB} = −5V ±5%, V_{SS} = 0V,
Except V_{DD} = +15V ±5% for 411-4.

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP ①	LIMITS MAX	UNIT	TEST CONDITIONS
Input Load Current	I_{LI}		0.01	10	μA	V_{IN} = V_{IL} MIN to V_{IH} MAX
CE Input Load Current	I_{LC}		0.01	10	μA	V_{IN} = V_{ILC} MIN to V_{IHC} MAX
Output Leakage Current for High Impedance State	I_{LO}		0.01	±10	μA	CE = V_{ILC} or $\overline{CS}$ = V_{IH} V_O = 0V to 5.25V
V_{DD} Supply Current during CE off	I_{DD} OFF		20	200	μA	CE = −1.0V to 0.6V
V_{DD} Supply Current during CE on	I_{DD} ON		35④	60⑤	mA	CE = V_{IHC}, T_a = 25°C
Average V_{DD} Current						T_a = 25°C
μPD411-E	I_{DD} AV		29	60	mA	Cycle Time = 800 ns
μPD411	I_{DD} AV		37	60	mA	Cycle Time = 470 ns
μPD411-1	I_{DD} AV		37	60	mA	Cycle Time = 470 ns
μPD411-2	I_{DD} AV		37	60	mA	Cycle Time = 400 ns
μPD411-3	I_{DD} AV		41	65	mA	Cycle Time = 380 ns
μPD411-4	I_{DD} AV		55	80	mA	Cycle Time = 320 ns
V_{BB} Supply Current ②	I_{BB}		5	100	μA	
V_{CC} Supply Current during CE off ③	I_{CC} OFF		0.01	10	μA	CE = V_{ILC} or $\overline{CS}$ = V_{IH}
Input Low Voltage	V_{IL}	−1.0		0.6	V	
Input High Voltage	V_{IH}	2.4 ④		V_{CC}+1	V	
CE Input Low Voltage	V_{ILC}	−1.0		0.6	V	
CE Input High Voltage	V_{IHC}	V_{DD}−1	V_{DD}	V_{DD}+1	V	
Output Low Voltage	V_{OL}	0		0.40	V	I_{OL} = 3.2 mA
Output High Voltage	V_{OH}	2.4		V_{CC}	V	I_{OH} = −2.0 mA

Notes: ① Typical values are for T_a = 25°C and nominal power supply voltages.
② The I_{BB} current is the sum of all leakage currents.
③ During CE on V_{CC} supply current is dependent on output loading.
V_{CC} is connected to output buffer only.
④ 3.5V for μPD411-E
⑤ 65 mA for μPD411-3
80 mA for μPD411-4
⑥ 41 mA for μPD411-3
55 mA for μPD411-4

CAPACITANCE

T_a = 0° − 70°C

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Address Capacitance, $\overline{CS}$	C_{AD}		4	6	pF	V_{IN} = V_{SS}
CE Capacitance	C_{CE}		18	27	pF	V_{IN} = V_{SS}
Data Output Capacitance	C_{OUT}		5	7	pF	V_{OUT} = 0V
D_{IN} and $\overline{WE}$ Capacitance	C_{IN}		8	10	pF	V_{IN} = V_{SS}

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READ CYCLE

T_a = 0°C to 70°C, V_{DD} = 12V ± 5%, V_{CC} = 5V ± 5%, V_{BB} = −5V ± 5%, V_{SS} = 0V, unless otherwise noted,
Except V_{DD} = +15V ± 5% for 411-4

PARAMETER	SYMBOL	LIMITS												UNIT
		μPD411-E		μPD411		μPD411-1		μPD411-2		μPD411-3		μPD411-4		
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
Time Between Refresh	t_{REF}		1		2		2		2		2		2	ms
Address to CE Set Up Time	t_{AC}	0		0		0		0		0		0		ns
Address Hold Time	t_{AH}	150		150		150		150		150		100		ns
CE Off Time	t_{CC}	380		130		170		130		130		80		ns
CE Transition Time	t_T	0	40	0	40	0	40	0	40	0	40	0	40	ns
CE Off to Output High Impedance State	t_{CF}	0	130	0	130	0	130	0	130	0	130	0	130	ns
Cycle Time	t_{CY}	800		470		470		400		380		320		ns
CE on Time	t_{CE}	380	3000	300	3000	260	3000	230	3000	210	3000	200	3000	ns
CE Output Delay	t_{CO}		330		280		230		180		130		115	ns
Access Time	t_{ACC}		350		300		250		200		150		135	ns
CE to $\overline{WE}$	t_{WL}	40		40		40		40		40		40		ns
$\overline{WE}$ to CE on	t_{WC}	0		0		0		0		0		0		ns

WRITE CYCLE

T_a = 0°C to 70°C, V_{DD} = 12V ± 5%, V_{CC} = 5V ± 5%, V_{BB} = −5V ± 5%, V_{SS} = 0V, unless otherwise noted,
Except V_{DD} = +15V ± 5% for 411-4

PARAMETER	SYMBOL	LIMITS												UNIT
		μPD411-E		μPD411		μPD411-1		μPD411-2		μPD411-3		μPD411-4		
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
Cycle Time	t_{CY}	800		470		470		400		380		320		ns
Time Between Refresh	t_{REF}		1		2		2		2		2		2	ms
Address to CE Set Up Time	t_{AC}	0		0		0		0		0		0		ns
Address Hold Time	t_{AH}	150		150		150		150		150		100		ns
CE Off Time	t_{CC}	380		130		170		130		130		80		ns
CE Transition Time	t_T	0	40	0	40	0	40	0	40	0	40	0	40	ns
CE Off to Output High Impedance State	t_{CF}	0	130	0	130	0	130	0	130	0	130	0	130	ns
CE on Time	t_{CE}	380	3000	300	3000	260	3000	230	3000	210	3000	200	3000	ns
$\overline{WE}$ to CE off	t_W	200		180		180		150		150		65		ns
CE to $\overline{WE}$	t_{CW}	380		300		260		230		210		200		ns
D_{IN} to $\overline{WE}$ Set Up ①	t_{DW}	0		0		0		0		0		0		ns
D_{IN} Hold Time	t_{DH}	40		40		40		40		40		40		ns
$\overline{WE}$ Pulse Width	t_{WP}	200		180		180		150		100		65		ns

Note: ① If $\overline{WE}$ is low before CE goes high then D_{IN} must be valid when CE goes high.

READ-MODIFY-WRITE CYCLE

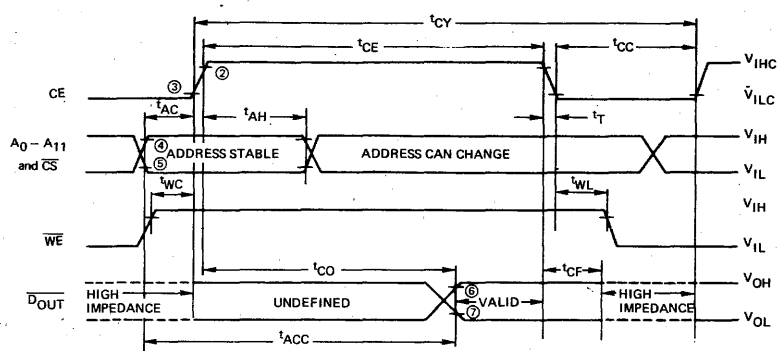
T_a = 0°C to 70°C, V_{DD} = 12V ± 5%, V_{CC} = 5V ± 5%, V_{BB} = −5V ± 5%, V_{SS} = 0V, unless otherwise noted,
Except V_{DD} = +15V ± 5% for 411-4

PARAMETER	SYMBOL	LIMITS												UNIT
		μPD411-E		μPD411		μPD411-1		μPD411-2		μPD411-3		μPD411-4		
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
Read–Modify–Write (RMW) Cycle Time	t_{RWC}	960		650		640		520		470		320		ns
Time Between Refresh	t_{REF}		1		2		2		2		2		2	ms
Address to CE Set Up Time	t_{AC}	0		0		0		0		0		0		ns
Address Hold Time	t_{AH}	150		150		150		150		150		100		ns
CE Off Time	t_{CC}	380		130		170		130		130		80		ns
CE Transition Time	t_T	0	40	0	40	0	40	0	40	0	40	0	40	ns
CE Off to Output High Impedance State	t_{CF}	0	130	0	130	0	130	0	130	0	130	0	130	ns
CE Width During RMW	t_{CRW}	540	3000	480	3000	430	3000	350	3000	300	3000	200	3000	ns
$\overline{WE}$ to CE on	t_{WC}	0		0		0		0		0		0		ns
$\overline{WE}$ to CE off	t_W	200		180		180		150		150		65		ns
$\overline{WE}$ Pulse Width	t_{WP}	200		180		180		150		100		65		ns
D_{IN} to $\overline{WE}$ Set Up	t_{DW}	0		0		0		0		0		0		ns
D_{IN} Hold Time	t_{DH}	40		40		40		40		40		40		ns
CE to Output Display	t_{CO}		330		280		230		180		130		115	ns
Access Time	t_{ACC}		350		300		250		200		150		135	ns

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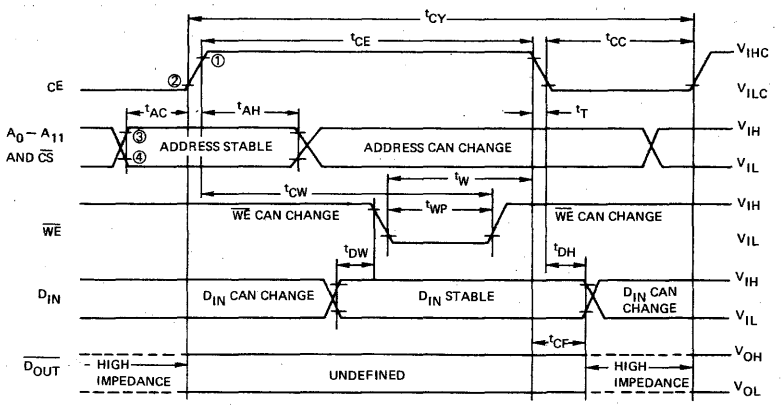
TIMING WAVEFORMS

READ CYCLE ①



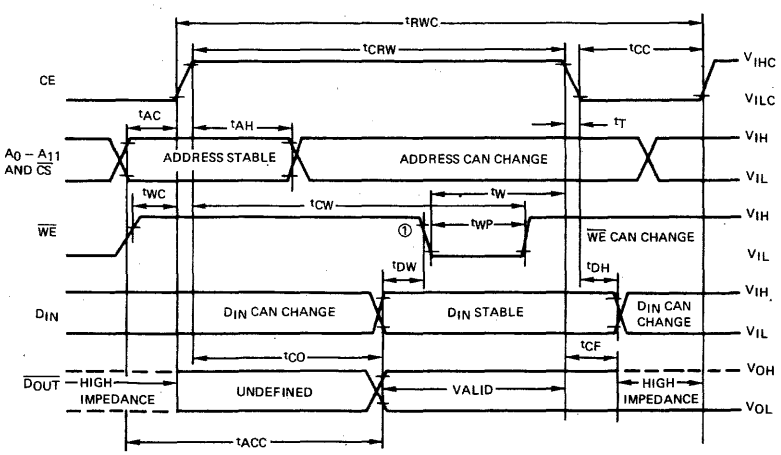
Notes: ① For refresh cycle row and column addresses must be stable t_{AC} and remain stable for entire t_{AH} period.
② V_{DD} –2V is the reference level for measuring timing of CE.
③ V_{SS} +2V is the reference level for measuring timing of CE.
④ V_{IHMIN} is the reference level for measuring timing of the addresses, $\overline{CS}$, $\overline{WE}$ and D_{IN}.
⑤ V_{ILMAX} is the reference level for measuring timing of the addresses, $\overline{CS}$, $\overline{WE}$ and D_{IN}.
⑥ V_{SS} +2.0V is the reference level for measuring timing of $\overline{D_{OUT}}$.
⑦ V_{SS} +0.8V is the reference level for measuring timing of $\overline{D_{OUT}}$.

WRITE CYCLE



Notes: ① V_{DD} –2V is the reference level for measuring timing of CE.
② V_{SS} +2V is the reference level for measuring timing of CE.
③ V_{IHMIN} is the reference level for measuring timing of the addresses, $\overline{CS}$, $\overline{WE}$ and D_{IN}.
④ V_{ILMAX} is the reference level for measuring timing of the addresses, $\overline{CS}$, $\overline{WE}$ and D_{IN}.

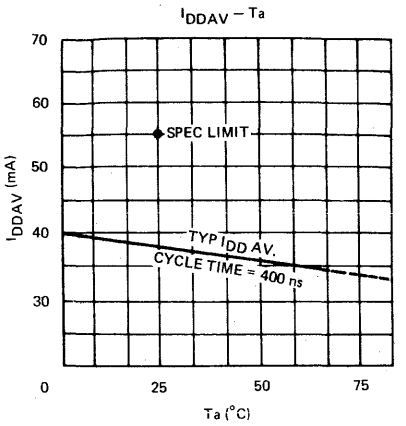
READ-MODIFY-WRITE CYCLE

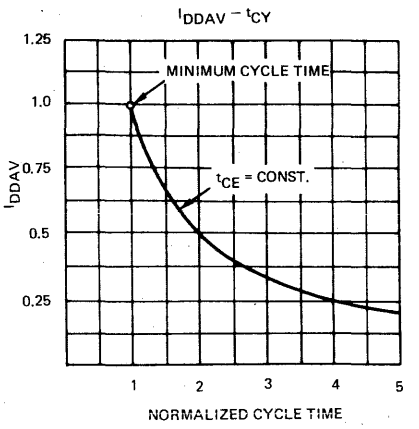


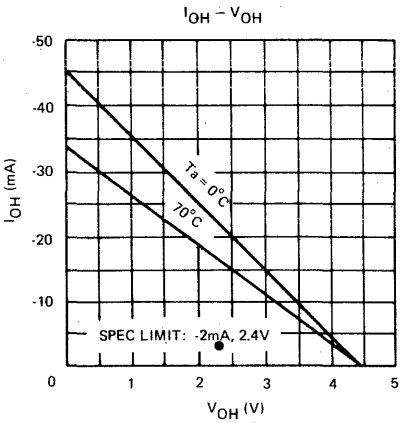
Note: ① $\overline{WE}$ must be at V_{IH} until end of t_{CO}.

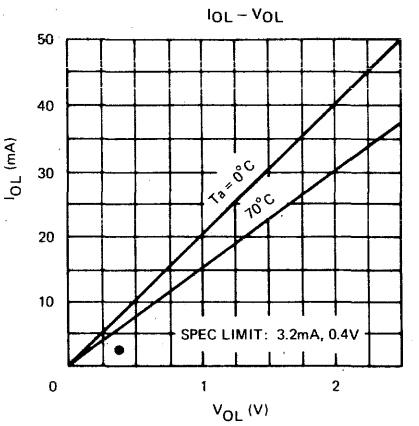
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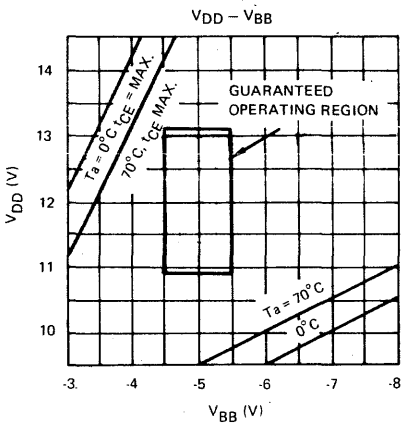
TYPICAL OPERATING CHARACTERISTICS (Except 411-4)

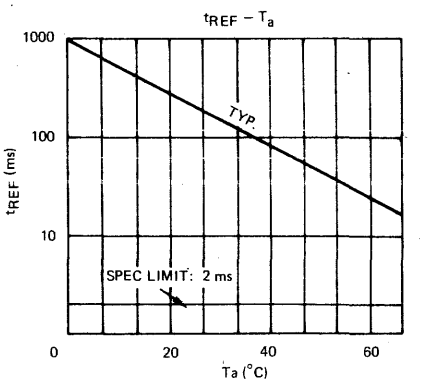












POWER CONSUMPTION

Power consumption = $V_{DD} \times I_{DDAV} + V_{BB} \times I_{BB}$.

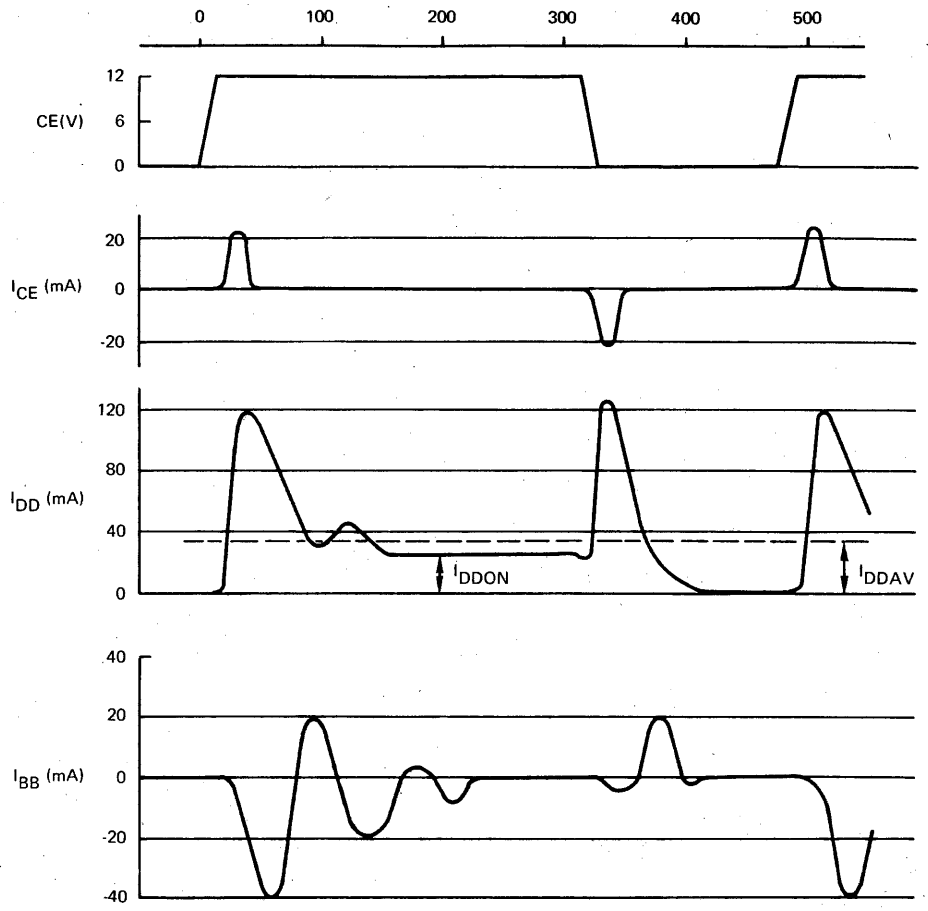
Typical power dissiption for each product is shown below.

	mW (TYP.)	CONDITIONS
μPD411-E	350	Ta = 25° C, t_{cy} = 800ns, t_{CE} = 380ns
μPD411	450	Ta = 25° C, t_{cy} = 470ns, t_{CE} = 300ns
μPD411-1	450	Ta = 25° C, t_{cy} = 470ns, t_{CE} = 260ns
μPD411-2	450	Ta = 25° C, t_{cy} = 400ns, t_{CE} = 230ns
μPD411-3	550	Ta = 25° C, t_{cy} = 380ns, t_{CE} = 210ns
μPD411-4	660	Ta = 25° C, t_{cy} = 320ns, t_{CE} = 200ns

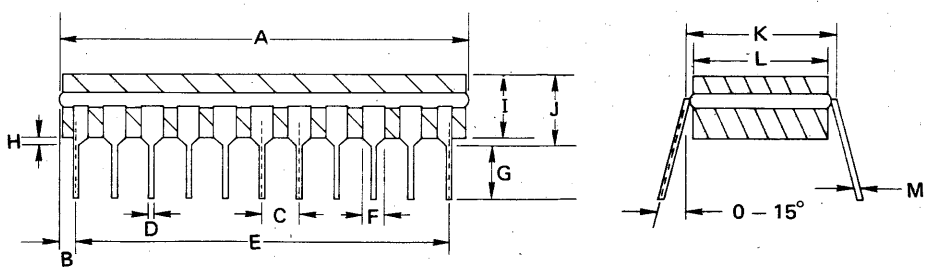
See above curves for power dissipation versus cycle time.

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CURRENT WAVEFORMS



PACKAGE OUTLINE μPD411D



ITEM	MILLIMETERS	INCHES
A	27.43 MAX	1.079 MAX
B	1.27 MAX	0.05 MAX
C	2.54 ± 0.1	0.10
D	0.42 ± 0.1	0.016
E	25.4 ± 0.3	1.0
F	1.5 ± 0.2	0.059
G	3.5 ± 0.3	0.138
H	3.7 ± 0.3	0.145
I	4.2 MAX	0.165 MAX
J	5.08 MAX	0.200 MAX
K	10.16 ± 0.15	0.400
L	9.1 ± 0.2	0.358
M	0.25 ± 0.05	0.009

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NEC

μPD411A-E
μPD411A
μPD411A-1
μPD411A-2

4096 BIT DYNAMIC RAMS

DESCRIPTION

The μPD411A Family consists of four 4096 words by 1 bit dynamic N-channel MOS RAMs. They are designed for memory applications where very low cost and large bit storage are important design objectives. The μPD411A Family is designed using dynamic circuitry which reduces the standby power dissipation.

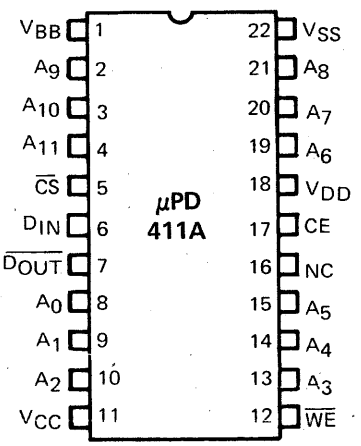
Reading information from the memory is non-destructive. Refreshing is easily accomplished by performing one read cycle on each of the 64 row addresses. Each row address must be refreshed every two milliseconds. The memory is refreshed whether Chip Select is a logic high or a logic low.

FEATURES

- Low Standby Power
- 4096 words x 1 bit Organization
- A single low-capacitance high level clock input with solid ±1 volt margins.
- Inactive Power 0.7 mW (Typ.)
- Power Supply +12, +5, −5V
- Easy System Interface
- TTL Compatible (Except CE)
- Address Registers on the Chip
- Simple Memory Expansion by Chip Select
- Three State Output and TTL Compatible
- 22 pin Plastic or Cerdip Dual-in-Line Package
- Replacement for INTEL's 2107B, TI's 4060 and Equivalent Devices.
- 4 Performance Ranges:

	ACCESS TIME	R/W CYCLE	RMW CYCLE	REFRESH TIME
μPD411A-E	350 ns	800 ns	960 ns	1 ms
μPD411A	300 ns	470 ns	650 ns	2 ms
μPD411A-1	250 ns	430 ns	600 ns	2 ms
μPD411A-2	200 ns	400 ns	520 ns	2 ms

PIN CONFIGURATION



PIN NAMES

A_0 - A_{11}	Address Inputs
A_0 - A_5	Refresh Addresses
CE	Chip Enable
$\overline{CS}$	Chip Select
D_{IN}	Data Input
$\overline{D_{OUT}}$	Data Output
$\overline{WE}$	Write Enable
V_{DD}	Power (+12V)
V_{CC}	Power (+5V)
V_{SS}	Ground
V_{BB}	(Powe. −5V)
NC	No Connection

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FUNCTIONAL DESCRIPTION

CE Chip Enable

A single external clock input is required. All read, write, refresh and read-modify-write operations take place when chip enable input is high. When the chip enable is low, the memory is in the low power standby mode. No read/write operations can take place because the chip is automatically precharging.

$\overline{CS}$ Chip Select

The chip select terminal affects the data in, data out and read/write inputs. The data input and data output terminals are enabled when chip select is low. The chip select input must be low on or before the rising edge of the chip enable and can be driven from standard TTL circuits. A register for the chip select input is provided on the chip to reduce overhead and simplify system design.

$\overline{WE}$ Write Enable

The read or write mode is selected through the write enable input. A logic high on the $\overline{WE}$ input selects the read mode and a logic low selects the write mode. The $\overline{WE}$ terminal can be driven from standard TTL circuits. The data input is disabled when the read mode is selected.

A_0–A_{11} Addresses

All addresses must be stable on or before the rising edge of the chip enable pulse. All address inputs can be driven from standard TTL circuits. Address registers are provided on the chip to reduce overhead and simplify system design.

D_{IN} Data Input

Data is written during a write or read-modify-write cycle while the chip enable is high. The data in terminal can be driven from standard TTL circuits. There is no register on the data in terminal.

$\overline{D_{OUT}}$ Data Output

The three state output buffer provides direct TTL compatibility with a fan-out of two TTL gates. The output is in the high-impedance (floating) state when the chip enable is low or when the Chip Select input is high. Data output is inverted from data in.

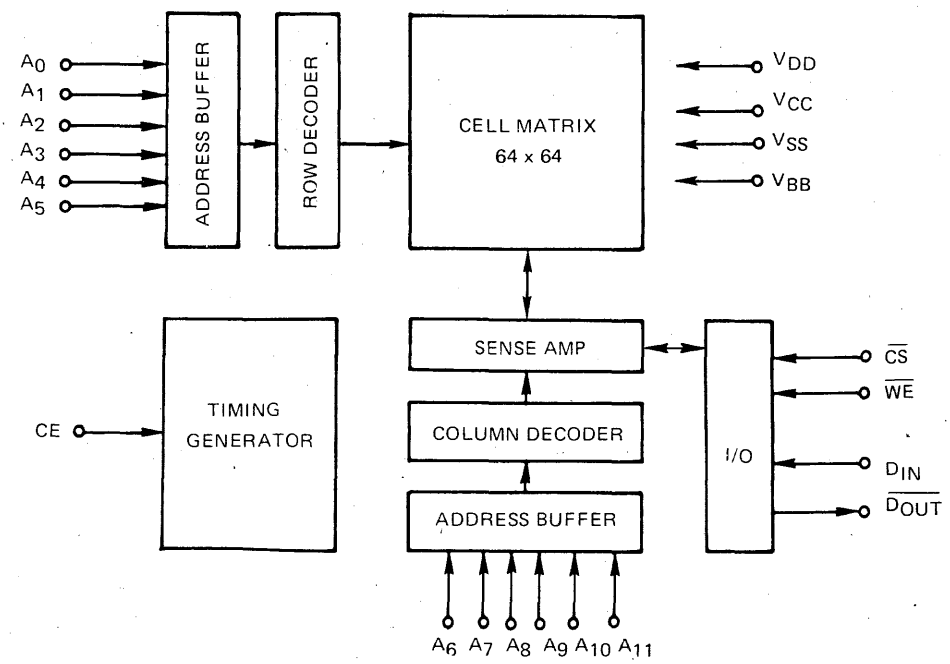
Refresh

Refresh must be performed every two milliseconds by cycling through the 64 addresses of the lower-order-address inputs A_0 through A_5 or by addressing every row within any 2*-millisecond period. Addressing any row refreshes all 64 bits in that row.

The chip does not need to be selected during the refresh. If the chip is refreshed during a write mode, the chip select must be high.

*μPD411A-E = 1 millisecond refresh period.

BLOCK DIAGRAM



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ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	0°C to +70°C
Storage Temperature	−55°C to +150°C
Output Voltage ①	+20 to −0.3 Volts
All Input Voltages ①	+20 to −0.3 Volts
Supply Voltage V_{DD} ①	+20 to −0.3 Volts
Supply Voltage V_{CC} ①	+20 to −0.3 Volts
Supply Voltage V_{SS} ①	+20 to −0.3 Volts
Power Dissipation	1.0W

Note: ① Relative to V_{BB}.

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

DC CHARACTERISTICS

T_a = 0°C to 70°C, V_{DD} = +12V ± 10%, V_{CC} = +5V ± 10%, V_{BB} = −5V ± 10%, V_{SS} = 0V

PARAMETER	SYMBOL	LIMITS MIN.	LIMITS TYP. ①	LIMITS MAX.	UNIT	TEST CONDITIONS
Input Load Current	I_{LI}		0.01	10	μA	V_{IN} = V_{IL} MIN to V_{IH} MAX
CE Input Load Current	I_{LC}		0.01	10	μA	V_{IN} = V_{ILC} MIN to V_{IHC} MAX
Output Leakage Current for High Impedance State	I_{LO}		0.01	±10	μA	CE = V_{ILC} or $\overline{CS}$ = V_{IH} V_O = 0V to 5.25V
V_{DD} Supply Current during CE off	I_{DD} OFF		50	200	μA	CE = −1.0V to 0.6V
V_{DD} Supply Current during CE on	I_{DD} ON		35	50	mA	CE = V_{IHC}, T_a = 25°C
Average V_{DD} Current						T_a = 25°C
μPD411A-E	I_{DD} AV		25	40	mA	Cycle Time = 800 ns
μPD411A	I_{DD} AV		38	55	mA	Cycle Time = 470 ns
μPD411A-1	I_{DD} AV		38	55	mA	Cycle Time = 430 ns
μPD411A-2	I_{DD} AV		38	55	mA	Cycle Time = 400 ns
V_{BB} Supply Current ②	I_{BB}		5	100	μA	
V_{CC} Supply Current during CE off ③	I_{CC} OFF		0.01	10	μA	CE = V_{ILC} or $\overline{CS}$ = V_{IH}
Input Low Voltage	V_{IL}	−1.0		0.6	V	
Input High Voltage	V_{IH}	2.4		V_{CC} + 1	V	
CE Input Low Voltage	V_{ILC}	−1.0		0.6	V	
CE Input High Voltage	V_{IHC}	V_{DD} − 1	V_{DD}	V_{DD} + 1	V	
Output Low Voltage	V_{OL}	0		0.40	V	I_{OL} = 3.2 mA
Output High Voltage	V_{OH}	2.4		V_{CC}	V	I_{OH} = −2.0 mA

Notes: ① Typical values are for T_a = 25°C and nominal power supply voltages.
② The I_{BB} current is the sum of all leakage currents.
③ During CE on V_{CC} supply current is dependent on output loading.

CAPACITANCE

T_a = 0°C to 70°C, V_{DD} = +12V ± 10%, V_{CC} = +5V ± 10%, V_{BB} = −5V ± 10%, V_{SS} = 0V

PARAMETER	SYMBOL	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNIT	TEST CONDITIONS
Address Capacitance	C_{AD}			6	pF	V_{IN} = V_{SS}
$\overline{CS}$ Capacitance	C_{CS}			6	pF	V_{IN} = V_{SS}
D_{IN} Capacitance	C_{IN}			6	pF	V_{IN} = V_{SS}
$\overline{D_{OUT}}$ Capacitance	C_{OUT}			7	pF	V_{OUT} = V_{SS}
$\overline{WE}$ Capacitance	C_{WE}			7	pF	V_{IN} = V_{SS}
CE Capacitance	C_{CE1}			27	pF	V_{IN} = V_{SS}
	C_{CE2}			22	pF	V_{IN} = V_{DD}

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READ CYCLE

T_a = 0°C to 70°C, V_{DD} = 12V ± 10%, V_{CC} = 5V ± 10%, V_{BB} = -5V ± 10%, V_{SS} = 0V, unless otherwise noted.

PARAMETER	SYMBOL	LIMITS μPD411A-E MIN	μPD411A-E MAX	μPD411A MIN	μPD411A MAX	μPD411A-1 MIN	μPD411A-1 MAX	μPD411A-2 MIN	μPD411A-2 MAX	UNIT	TEST CONDITIONS
Time Between Refresh	t_{REF}		1		2		2		2	ms	
Address to CE Set Up Time	t_{AC}	0		0		0		0		ns	
Address Hold Time	t_{AH}	150		150		150		150		ns	
CE Off Time	t_{CC}	380		130		130		130		ns	
CE Transition Time	t_T	0	40	0	40	0	40	0	40	ns	$t_T = t_r = t_f = 20$ ns
CE Off to Output High Impedance State	t_{CF}	0	130	0	130	0	130	0	130	ns	C_L = 50 pF
Cycle Time	t_{CY}	800		470		430		400		ns	Load = 1_{TTL} Gate
CE on Time	t_{CE}	380	3000	300	3000	260	3000	230	3000	ns	V_{ref} = 2.0 or 0.8 Volts
CE Output Delay	t_{CO}		330		280		230		180	ns	
Access Time	t_{ACC}		350		300		250		200	ns	
CE to $\overline{WE}$	t_{WL}	40		40		40		40		ns	
$\overline{WE}$ to CE on	t_{WC}	0		0		0		0		ns	

WRITE CYCLE

T_a = 0°C to 70°C, V_{DD} = 12V ±10%, V_{CC} = 5V ± 10%, V_{BB} = -5V ± 10%, V_{SS} = 0V, unless otherwise noted.

PARAMETER	SYMBOL	LIMITS μPD411A-E MIN	μPD411A-E MAX	μPD411A MIN	μPD411A MAX	μPD411A-1 MIN	μPD411A-1 MAX	μPD411A-2 MIN	μPD411A-2 MAX	UNIT	TEST CONDITIONS
Cycle Time	t_{CY}	800		470		430		400		ns	
Time Between Refresh	t_{REF}		1		2		2		2	ms	
Address to CE Set Up Time	t_{AC}	0		0		0		0		ns	
Address Hold Time	t_{AH}	150		150		150		150		ns	
CE Off Time	t_{CC}	380		130		130		130		ns	
CE Transition Time	t_T	0	40	0	40	0	40	0	40	ns	$t_T = t_r = t_f = 20$ ns
CE Off to Output High Impedance State	t_{CF}	0	130	0	130	0	130	0	130	ns	C_L = 50 pF
CE on Time	t_{CE}	380	3000	300	3000	260	3000	230	3000	ns	Load = ITTL Gate
$\overline{WE}$ to CE off	t_W	200		180		180		150		ns	V_{ref} = 2.0 or 0.8 Volts
CE to $\overline{WE}$	t_{CW}	380		300		260		230		ns	
D_{IN} to $\overline{WE}$ Set Up ①	t_{DW}	0		0		0		0		ns	
D_{IN} Hold Time	t_{DH}	40		40		40		40		ns	
$\overline{WE}$ Pulse Width	t_{WP}	200		180		180		150		ns	

Note: ① If $\overline{WE}$ is low before CE goes high then D_{IN} must be valid when CE goes high.

READ-MODIFY-WRITE CYCLE

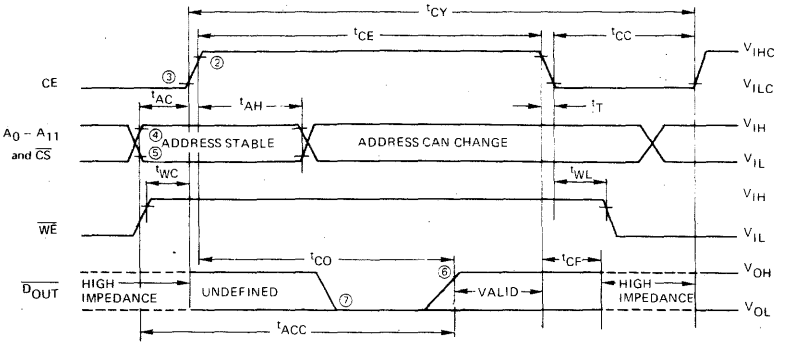
T_a = 0°C to 70°C, V_{DD} = 12V ± 10%, V_{CC} = 5V ± 10%, V_{BB} = -5V ± 10%, V_{SS} = 0V, unless otherwise noted.

PARAMETER	SYMBOL	LIMITS μPD411A-E MIN	μPD411A-E MAX	μPD411A MIN	μPD411A MAX	μPD411A-1 MIN	μPD411A-1 MAX	μPD411A-2 MIN	μPD411A-2 MAX	UNIT	TEST CONDITIONS
Read-Modify-Write (RMW) Cycle Time	t_{RWC}	960		650		600		520		ns	
Time Between Refresh	t_{REF}		1		2		2		2	ms	
Address to CE Set Up Time	t_{AC}	0		0		0		0		ns	
Address Hold Time	t_{AH}	150		150		150		150		ns	
CE Off Time	t_{CC}	380		130		130		130		ns	
CE Transition Time	t_T	0	40	0	40	0	40	0	40	ns	
CE Off to Output High Impedance State	t_{CF}	0	130	0	130	0	130	0	130	ns	$t_T = t_r = t_f = 20$ ns
CE Width During RMW	t_{CRW}	540	3000	480	3000	430	3000	350	3000	ns	C_L = 50 pF
$\overline{WE}$ to CE on	t_{WC}	0		0		0		0		ns	Load = 1_{TTL} Gate
$\overline{WE}$ to CE off	t_W	200		180		180		150		ns	V_{ref} = 2.0 or 0.8 Volts
$\overline{WE}$ Pulse Width	t_{WP}	200		180		180		150		ns	
D_{IN} to $\overline{WE}$ Set Up	t_{DW}	0		0		0		0		ns	
D_{IN} Hold Time	t_{DH}	40		40		40		40		ns	
CE to Output Delay	t_{CO}		330		280		230		180	ns	
Access Time	t_{ACC}		350		300		250		200	ns	

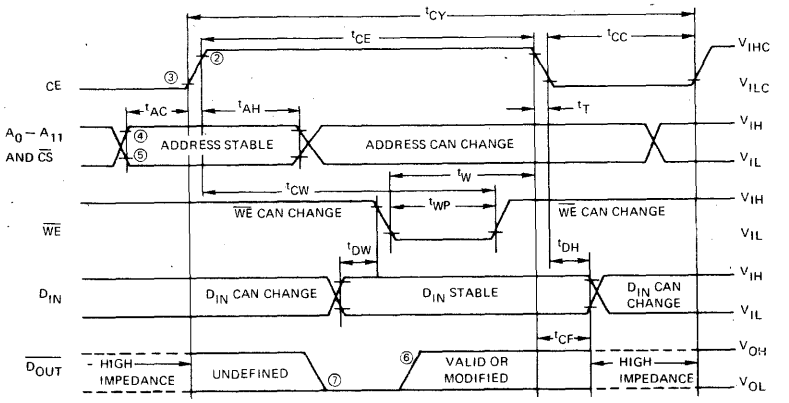
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TIMING WAVEFORMS

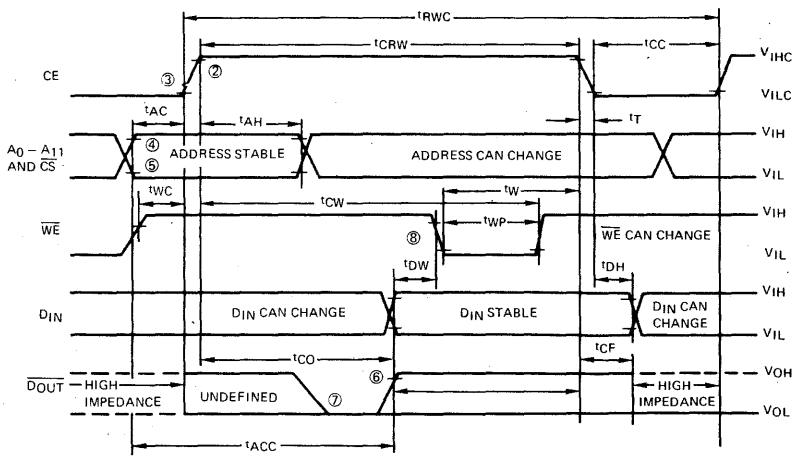
READ AND REFRESH CYCLE ①



WRITE CYCLE



READ-MODIFY-WRITE CYCLE



Notes:

① For refresh cycle, row and column addresses must be stable t_{AC} and remain stable for entire t_{AH} period.

② V_{DD} – 2V is the reference level for measuring timing of CE.

③ V_{SS} + 2V is the reference level for measuring timing of CE.

④ V_{IHMIN} is the reference level for measuring timing of the addresses, $\overline{CS}$, $\overline{WE}$ and D_{IN}.

⑤ V_{ILMAX} is the reference level for measuring timing of the addresses, $\overline{CS}$, $\overline{WE}$ and D_{IN}.

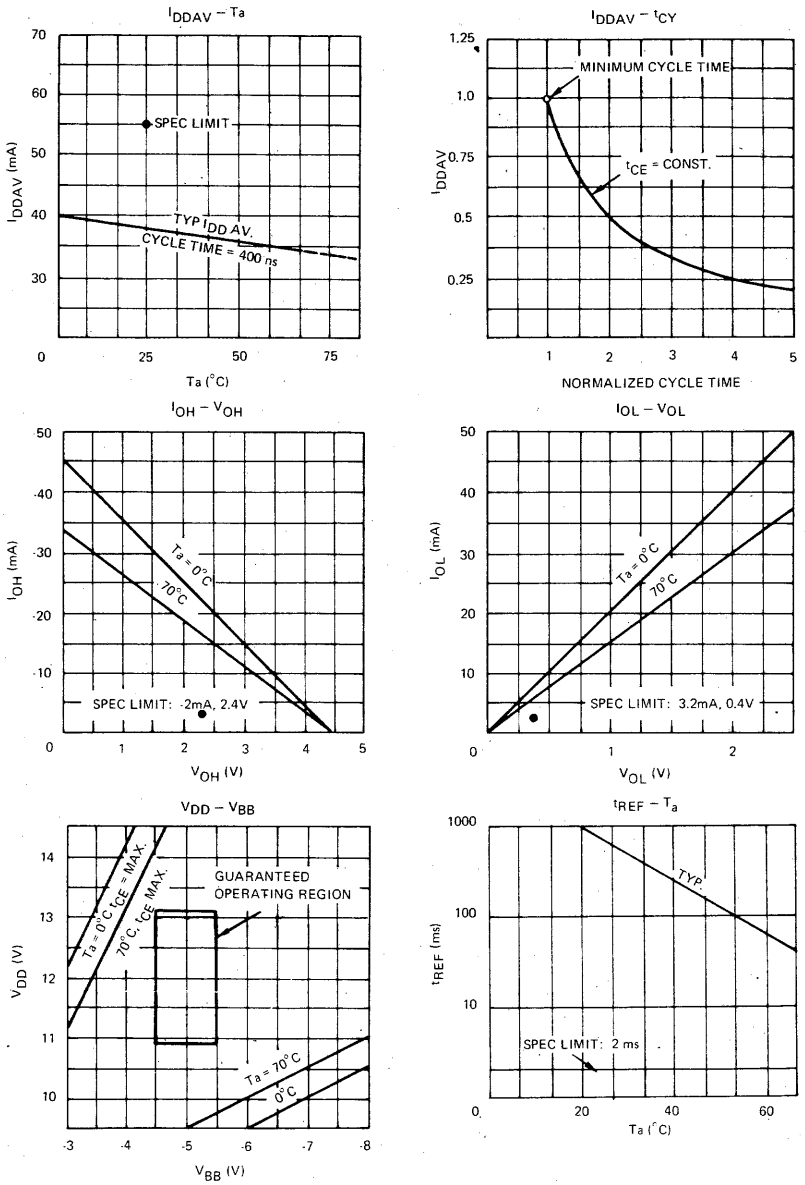
⑥ V_{SS} + 2.0V is the reference level for measuring timing of $\overline{D_{OUT}}$.

⑦ V_{SS} + 0.8V is the reference level for measuring timing of $\overline{D_{OUT}}$.

⑧ $\overline{WE}$ must be at V_{IH} until end of t_{CO}.

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TYPICAL OPERATING CHARACTERISTICS



POWER CONSUMPTION

Power consumption = $V_{DD} \times I_{DDAV} + V_{BB} \times I_{BB}$

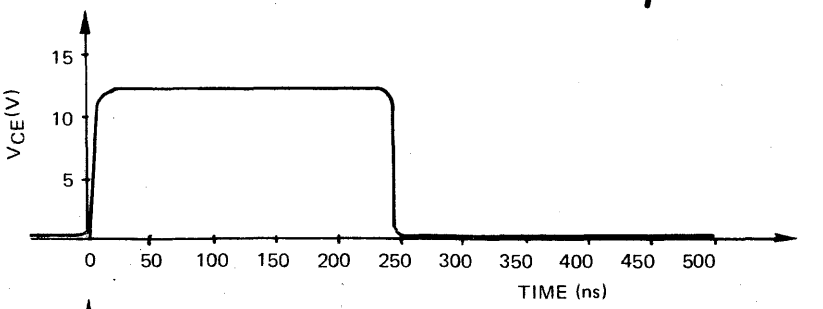
Typical power dissipation for each product is shown below.

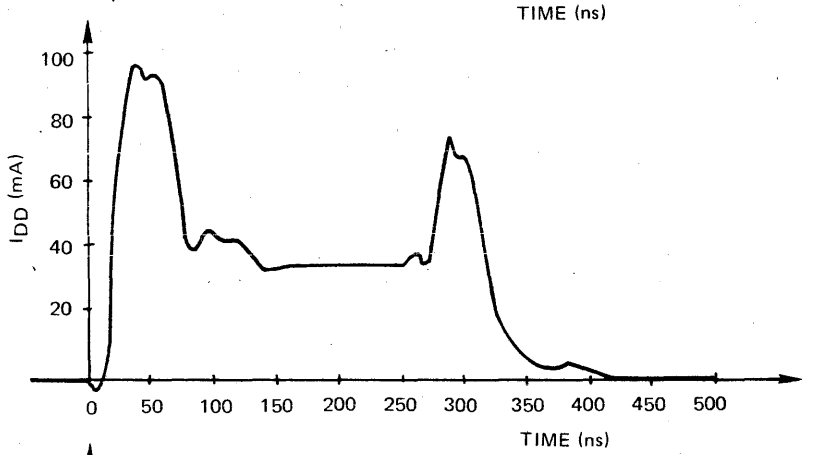
	mW (TYP.)	CONDITIONS
μPD411A-E	300 mW	$T_a = 25°C$, $t_{cy} = 800$ ns, $t_{CE} = 380$ ns
μPD411A	460 mW	$T_a = 25°C$, $t_{cy} = 470$ ns, $t_{CE} = 300$ ns
μPD411A-1	460 mW	$T_a = 25°C$, $t_{cy} = 430$ ns, $t_{CE} = 260$ ns
μPD411A-2	460 mW	$T_a = 25°C$, $t_{cy} = 400$ ns, $t_{CE} = 230$ ns

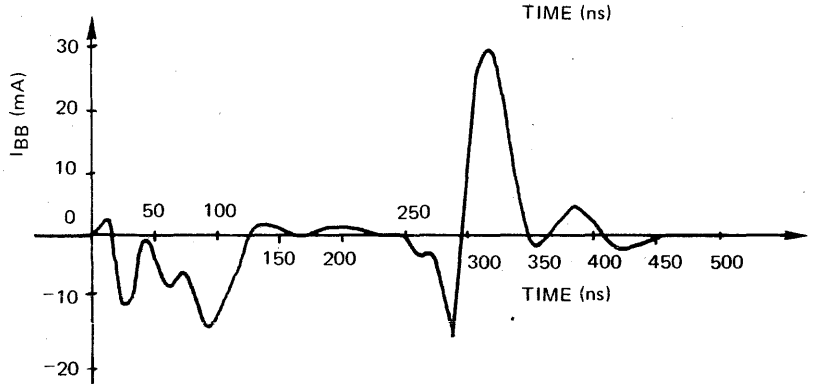
See curve above for power dissipation versus cycle time.

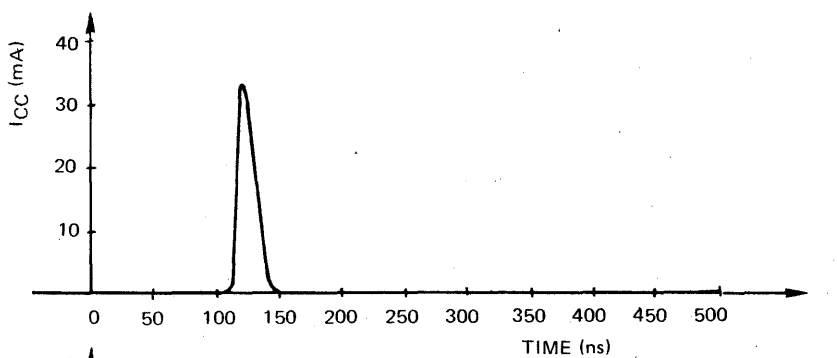
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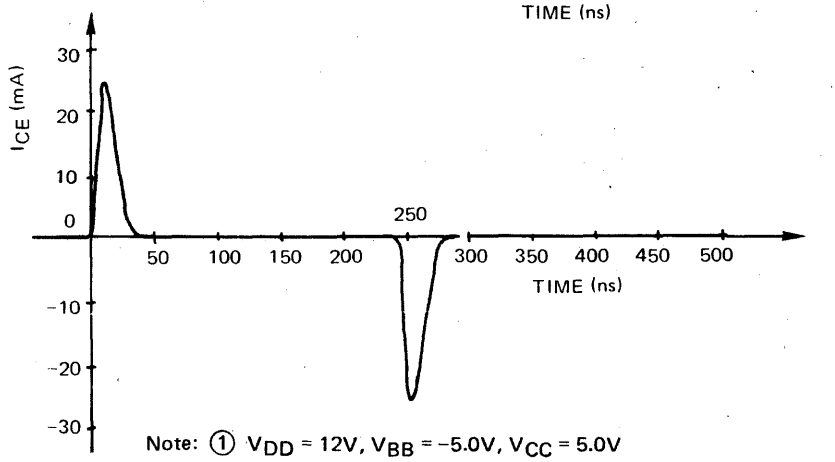
CURRENT WAVEFORMS ①







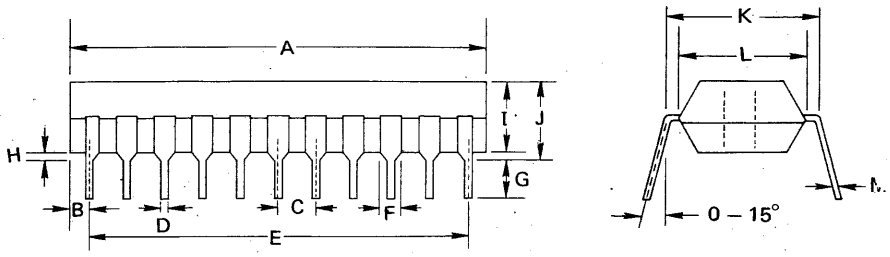




Note: ① V_{DD} = 12V, V_{BB} = −5.0V, V_{CC} = 5.0V

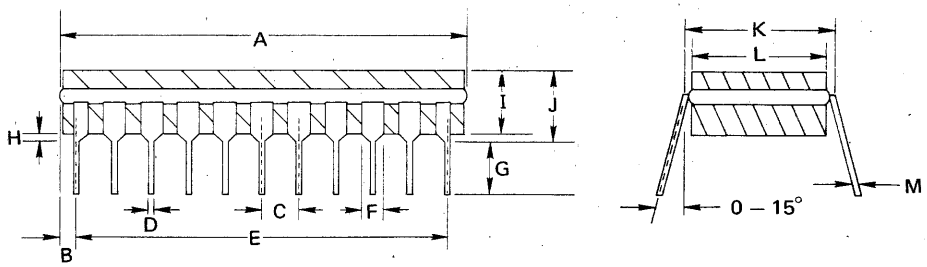
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PACKAGE OUTLINE
μPD411AC/D



μPD411AC (Plastic)

ITEM	MILLIMETERS	INCHES
A	28.0 Max.	1.10 Max.
B	1.4 Max.	0.025 Max.
C	2.54	0.10
D	0.50	0.02
E	25.4	1.00
F	1.40	0.055
G	2.54 Min.	0.10 Min.
H	0.5 Min.	0.02 Min.
I	4.7 Max.	0.18 Max.
J	5.2 Max.	0.20 Max.
K	10.16	0.40
L	8.5	0.33
M	$0.25^{+0.10}_{-0.05}$	$0.01^{+0.004}_{-0.002}$



μPD411AD (Cerdip)

ITEM	MILLIMETERS	INCHES
A	27.43 Max.	1.079 Max.
B	1.27 Max.	0.05 Max.
C	2.54 ± 0.1	0.10
D	0.42 ± 0.1	0.016
E	25.4 ± 0.3	1.0
F	1.5 ± 0.2	0.059
G	3.5 ± 0.3	0.138
H	3.7 ± 0.3	0.145
I	4.2 Max.	0.165 Max.
J	5.08 Max.	0.200 Max.
K	10.16 ± 0.15	0.400
L	9.1 ± 0.2	0.358
M	0.25 ± 0.05	0.009

SP411A-8-77-GY-CAT

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NEC
μPD416
μPD416-1
μPD416-2
μPD416-3
μPD416-5

16384 x 1 BIT DYNAMIC MOS RANDOM ACCESS MEMORY

DESCRIPTION

The NEC μPD416 is a 16384 words by 1 bit Dynamic MOS RAM. It is designed for memory applications where very low cost and large bit storage are important design objectives.

The μPD416 is fabricated using a double-poly-layer N channel silicon gate process which affords high storage cell density and high performance. The use of dynamic circuitry throughout, including the sense amplifiers, assures minimal power dissipation.

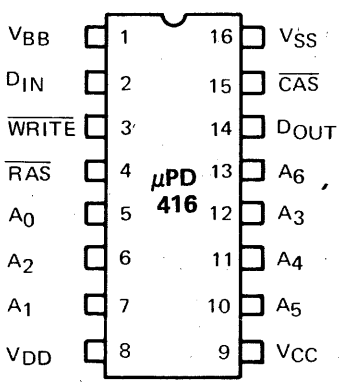
Multiplexed address inputs permit the μPD416 to be packaged in the standard 16 pin dual-in-line package. The 16 pin package provides the highest system bit densities and is available in either ceramic or plastic. Noncritical clock timing requirements allow use of the multiplexing technique while maintaining high performance.

FEATURES

- 16384 Words x 1 Bit Organization
- High Memory Density – 16 Pin Ceramic and Plastic Packages
- Multiplexed Address Inputs
- Standard Power Supplies +12V, -5V, +5V
- Low Power Dissipation; 462 mW Active (MAX), 40 mW Standby (MAX)
- Output Data Controlled by $\overline{CAS}$ and Unlatched at End of Cycle
- Read-Modify-Write, $\overline{RAS}$-only Refresh, and Page Mode Capability
- All Inputs TTL Compatible, and Low Capacitance
- 128 Refresh Cycles
- 5 Performance Ranges:

	ACCESS TIME	R/W CYCLE	RMW CYCLE
μPD416	300 ns	510 ns	575 ns
μPD416-1	250 ns	410 ns	465 ns
μPD416-2	200 ns	375 ns	375 ns
μPD416-3	150 ns	375 ns	375 ns
μPD416-5	120 ns	320 ns	320 ns

PIN CONFIGURATION

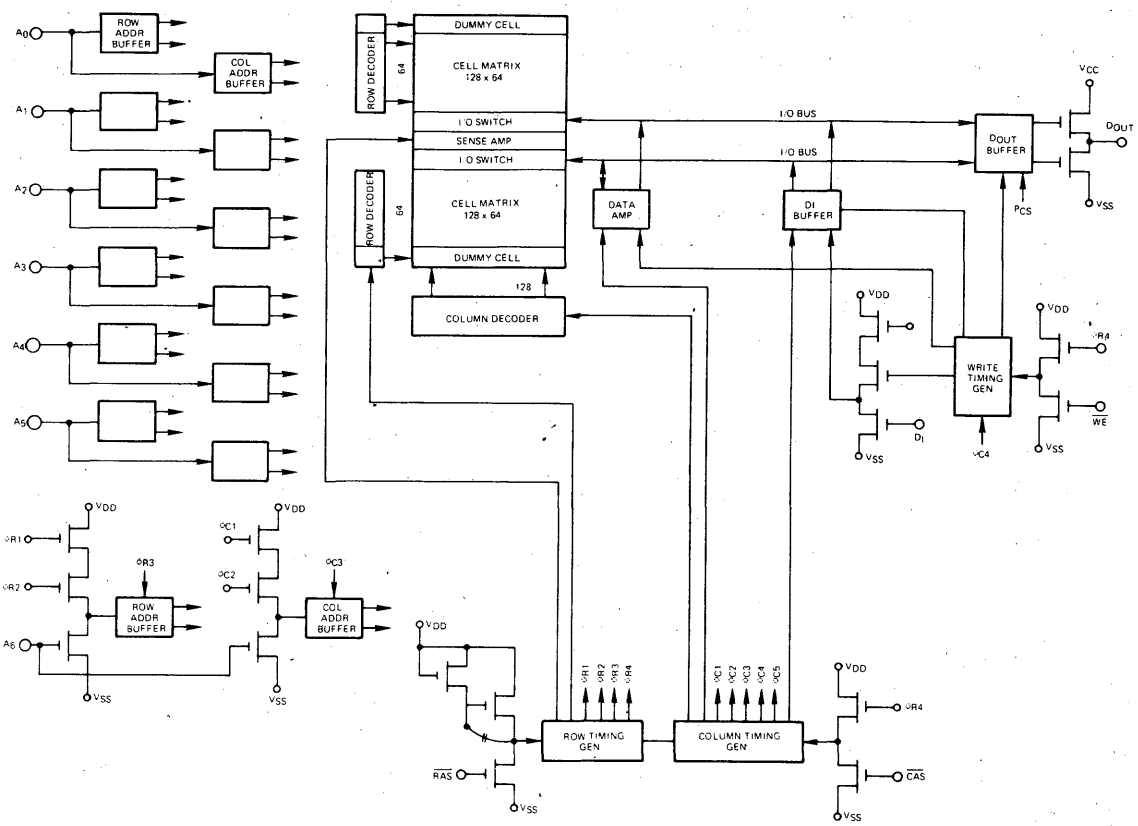


A_0-A_6	Address Inputs
$\overline{CAS}$	Column Address Strobe
D_{IN}	Data In
D_{OUT}	Data Out
$\overline{RAS}$	Row Address Strobe
$\overline{WRITE}$	Read/Write
V_{BB}	Power (-5V)
V_{CC}	Power (+5V)
V_{DD}	Power (+12V)
V_{SS}	Ground

Rev/1

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BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	0°C to +70°C
Storage Temperature	−55°C to +150°C
All Output Voltages ①	−0.5 to +20 Volts
All Input Voltages ①	−0.5 to +20 Volts
Supply Voltages V_{DD}, V_{CC}, V_{SS} ①	−0.5 to +20 Volts
Supply Voltages V_{DD}, V_{CC} ②	−1.0 to +15 Volts
Short Circuit Output Current	50 mA
Power Dissipation	1 Watt

Notes: ① Relative to V_{BB}
② Relative to V_{SS}

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

CAPACITANCE

T_a = 0°C to 70°C, V_{DD} = +12V ± 10%, V_{BB} = −5V ± 10%, V_{CC} = +5V ± 10%, V_{SS} = 0V

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN	TYP	MAX		
Input Capacitance (A_0-A_6), D_{IN}	C_{I1}		4	5	pF	
Input Capacitance $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$	C_{I2}		8	10	pF	
Output Capacitance (D_{OUT})	C_O		5	7	pF	

DC CHARACTERISTICS

T_a = 0°C to +70°C (1), V_{DD} = +12V ± 10%, V_{CC} = +5V ± 10%, V_{BB} = −5V ± 10%, V_{SS} = 0V

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Supply Voltage	V_{DD}	10.8	12.0	13.2	V	(2)
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	(2) (3)
Supply Voltage	V_{SS}	0	0	0	V	(2)
Supply Voltage	V_{BB}	− 4.5	−5.0	−5.5	V	(2)
Input High (Logic 1) Voltage, $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$	V_{IHC}	2.7		7.0	V	(2)
Input High (Logic 1) Voltage, all inputs except $\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$	V_{IH}	2.4		7.0	V	(2)
Input Low (Logic 0) Voltage, all inputs	V_{IL}	− 1.0		0.8	V	(2)
Operating V_{DD} Current	I_{DD1}			35	mA	$\overline{RAS}$, $\overline{CAS}$ cycling; t_{RC} = t_{RC} Min. (4)
Standby V_{DD} Current	I_{DD2}			1.5	mA	$\overline{RAS}$ = V_{IHC}, D_{OUT} = High Impedance
Refresh V_{DD} Current — All Speeds except μPD416-5	I_{DD3}			25	mA	$\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IHC}; t_{RC} = 375 ns (4)
Refresh V_{DD} Current — μPD416-5	I_{DD3}			27	mA	$\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IHC}; t_{RC} = 375 ns (4)
Page Mode V_{DD} Current	I_{DD4}			27	mA	$\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling; t_{PC} = 225 ns (4)
Operating V_{CC} Current	I_{CC1}				μA	$\overline{RAS}$, $\overline{CAS}$ cycling. t_{RC} = 375 ns (5)
Standby V_{CC} Current	I_{CC2}	-10		10	μA	$\overline{RAS}$ = V_{IHC}, D_{OUT} = High Impedance
Refresh V_{CC} Current	I_{CC3}	−10		10	μA	$\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IHC}, t_{RC} = 375 ns
Page Mode V_{CC} Current	I_{CC4}				μA	$\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling, t_{PC} = 225 ns (5)
Operating V_{BB} Current	I_{BB1}			200	μA	$\overline{RAS}$, $\overline{CAS}$ cycling t_{RC} = 375 ns
Standby V_{BB} Current	I_{BB2}			100	μA	$\overline{RAS}$ = V_{IHC}, D_{OUT} = High Impedance
Refresh V_{BB} Current	I_{BB3}			200	μA	$\overline{RAS}$ cycling, $\overline{CAS}$ = V_{IHC}, t_{RC} = 375 ns
Page Mode V_{BB} Current	I_{BB4}			200	μA	$\overline{RAS}$ = V_{IL}, $\overline{CAS}$ cycling; t_{PC} = 225 ns
Input Leakage (any input)	$I_{I(L)}$	−10		10	μA	V_{BB} = −5V, 0V ≤ V_{IN} ≤ +7V, all other pins not under test = 0V
Output Leakage	$I_{O(L)}$	−10		10	μA	D_{OUT} is disabled, 0V ≤ V_{OUT} ≤ +5.5V
Output High Voltage (Logic 1)	V_{OH}	2.4			V	I_{OUT} = −5 mA (3)
Output Low Voltage (Logic 0)	V_{OL}			0.4	V	I_{OUT} = 4.2 mA

Notes: (1) T_a is specified here for operation at frequencies to $t_{RC} \geq t_{RC}$ (min). Operation at higher cycle rates with reduced ambient temperatures and high power dissipation is permissible, however, provided AC operating parameters are met. See Figure 1 for derating curve.

(2) All voltages referenced to V_{SS}.

(3) Output voltage will swing from V_{SS} to V_{CC} when activated with no current loading. For purposes of maintaining data in standby mode, V_{CC} may be reduced to V_{SS} without affecting refresh operations or data retention. However, the V_{OH} (min) specification is not guaranteed in this mode.

(4) I_{DD1}, I_{DD3}, and I_{DD4} depend on cycle rate. See Figures 2, 3 and 4 for I_{DD} limits at other cycle rates.

(5) I_{CC1} and I_{CC4} depend upon output loading. During readout of high level data V_{CC} is connected through a low impedance (135Ω typ) to data out. At all other times I_{CC} consists of leakage currents only.

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DERATING CURVES

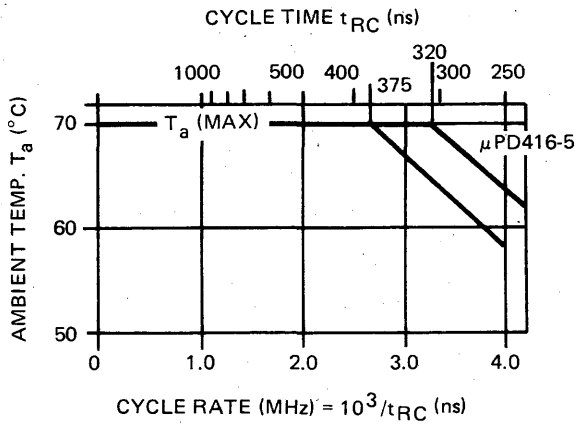


FIGURE 1

Maximum ambient temperature versus cycle rate for extended frequency operation. T_a (max) for operation at cycling rates greater than 2.66 MHz (t_{CYC} < 375 ns) is determined by T_a (max) [°C] = 70 – 9.0 x (cycle rate [MHz] –2.66). For μPD416-5, it is T_a (max) [°C] = 70 – 9.0 (cycle rate [MHz] – 3.125).

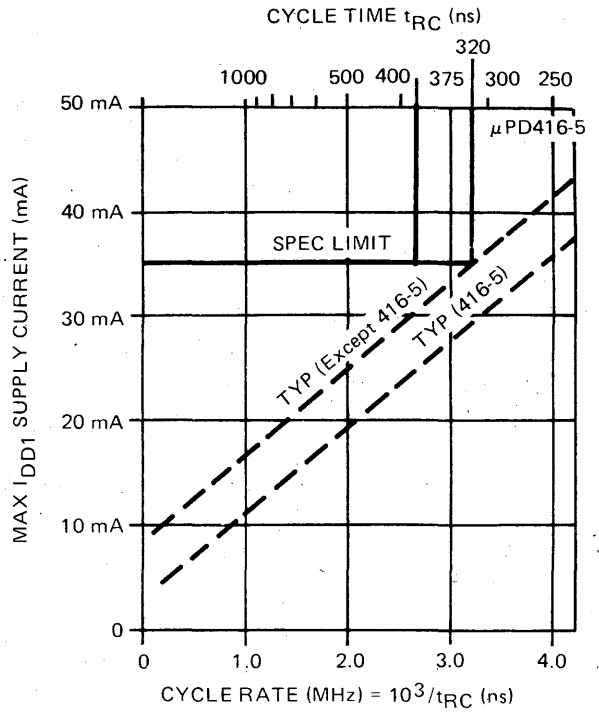


FIGURE 2

Maximum I_{DD1} versus cycle rate for device operation at extended frequencies.

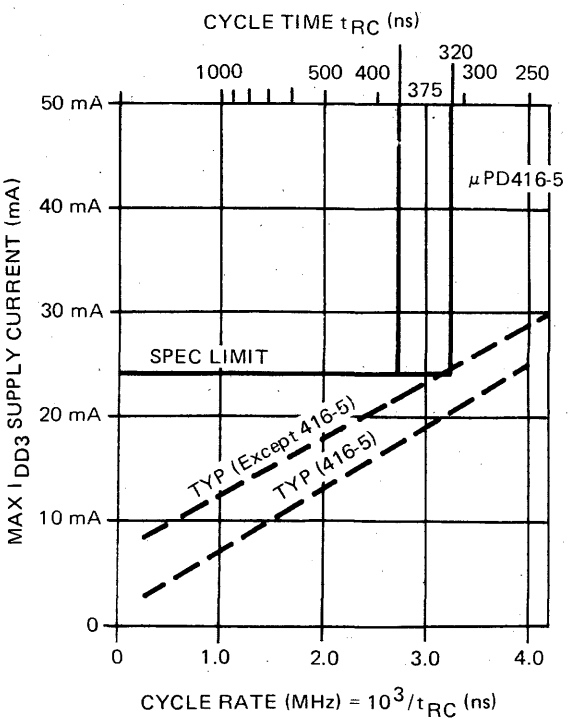


FIGURE 3

Maximum I_{DD3} versus cycle rate for device operation at extended frequencies.

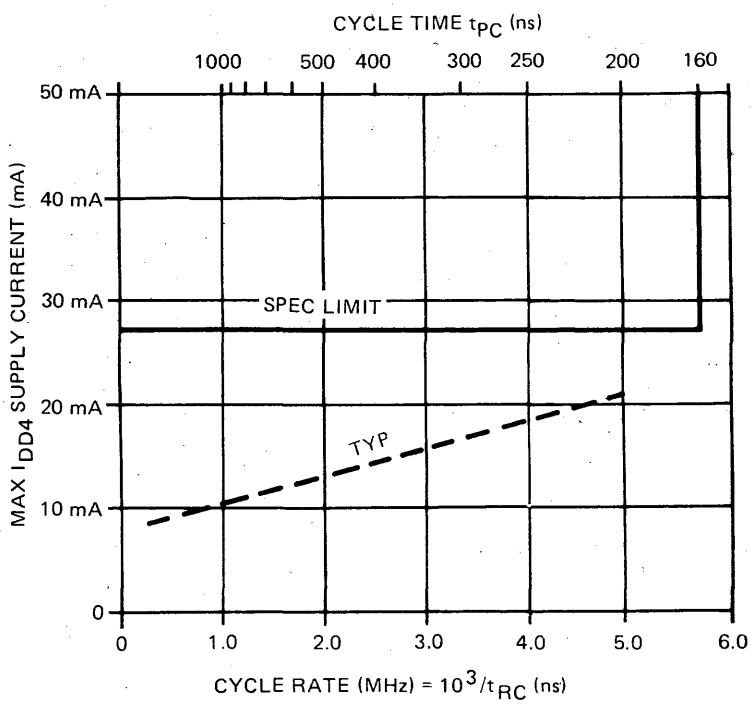


FIGURE 4

Maximum I_{DD4} versus cycle rate for device operation in page mode.

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AC CHARACTERISTICS

T_a = 0°C to +70°C, V_{DD} = +12V ± 10%, V_{CC} = +5V ± 10%, V_{BB} = −5V ± 10%, V_{SS} = 0V

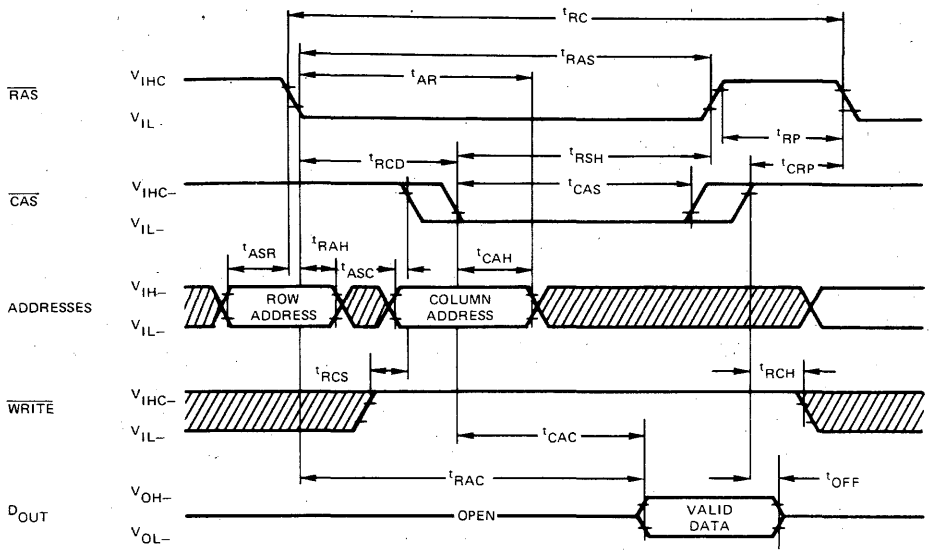
PARAMETER	SYMBOL	LIMITS μPD416 MIN	LIMITS μPD416 MAX	LIMITS μPD416-1 MIN	LIMITS μPD416-1 MAX	LIMITS μPD416-2 MIN	LIMITS μPD416-2 MAX	LIMITS μPD416-3 MIN	LIMITS μPD416-3 MAX	LIMITS μPD416-5 MIN	LIMITS μPD416-5 MAX	UNIT	TEST CONDITIONS
Random read or write cycle time	t_{RC}	510		410		375		375		320		ns	③
Read-write cycle time	t_{RWC}	575		465		375		375		320		ns	③
Page mode cycle time	t_{PC}	330		275		225		170		160		ns	
Access time from $\overline{RAS}$	t_{RAC}		300		250		200		150		120	ns	④ ⑥
Access time from $\overline{CAS}$	t_{CAC}		200		165		135		100		80	ns	⑤ ⑥
Output buffer turn-off delay	t_{OFF}	0	80	0	60	0	50	0	40	0	35	ns	⑦
Transition time (rise and fall)	t_T	3	50	3	50	3	50	3	35	3	35	ns	②
$\overline{RAS}$ precharge time	t_{RP}	200		150		120		100		100		ns	
$\overline{RAS}$ pulse width	t_{RAS}	300	10,000	250	10,000	200	32,000	150	32,000	120	10,000	ns	
$\overline{RAS}$ hold time	t_{RSH}	200		165		135		100		80		ns	
$\overline{CAS}$ pulse width	t_{CAS}	200	10,000	165	10,000	135	10,000	100	10,000	80	10,000	ns	
$\overline{RAS}$ to $\overline{CAS}$ delay time	t_{RCD}	40	100	35	85	25	65	20	50	15	40	ns	⑧
$\overline{CAS}$ to $\overline{RAS}$ precharge time	t_{CRP}	−20		−20		−20		−20		0		ns	
Row address set-up time	t_{ASR}	0		0		0		0		0		ns	
Row address hold time	t_{RAH}	40		35		25		20		15		ns	
Column address set-up time	t_{ASC}	−10		−10		−10		−10		−10		ns	
Column address hold time	t_{CAH}	90		75		55		45		40		ns	
Column address hold time referenced to $\overline{RAS}$	t_{AR}	190		160		120		95		80		ns	
Read command set-up time	t_{RCS}	0		0		0		0		0		ns	
Read command hold time	t_{RCH}	0		0		0		0		0		ns	
Write command hold time	t_{WCH}	90		75		55		45		40		ns	
Write command hold time referenced to $\overline{RAS}$	t_{WCR}	190		160		120		95		80		ns	
Write command pulse width	t_{WP}	90		75		55		45		40		ns	
Write command to $\overline{RAS}$ lead time	t_{RWL}	120		100		80		60		60		ns	
Write command to $\overline{CAS}$ lead time	t_{CWL}	120		100		80		60		60		ns	
Data-in set-up time	t_{DS}	0		0		0		0		0		ns	⑨
Data-in hold time	t_{DH}	90		75		55		45		40		ns	⑨
Data-in hold time referenced to $\overline{RAS}$	t_{DHR}	190		160		120		95		80		ns	
CAS precharge time (for page mode cycle only)	t_{CP}	120		100		80		60		60		ns	
Refresh period	t_{REF}		2		2		2		2		2	ms	
$\overline{WRITE}$ command set-up time	t_{WCS}	−20		−20		−20		−20		0		ns	⑩
$\overline{CAS}$ to $\overline{WRITE}$ delay	t_{CWD}	140		125		95		70		80		ns	⑩
$\overline{RAS}$ to $\overline{WRITE}$ delay	t_{RWD}	240		200		160		120		120		ns	⑩

Notes:
① AC measurements assume t_T = 5 ns.
② V_{IHC} (min) or V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IHC} or V_{IH} and V_{IL}.
③ The specifications for t_{RC} (min) and t_{RWC} (min) are used only to indicate cycle time at which proper operation over the full temperature range (0°C ≤ T_a ≤ 70°C) is assured.
④ Assumes that $t_{RCD} \leq t_{RCD}$ (max). If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} will increase by the amount that t_{RCD} exceeds the values shown.
⑤ Assumes that $t_{RCD} \geq t_{RCD}$ (max).
⑥ Measured with a load equivalent to 2 TTL loads and 100 pF.
⑦ t_{OFF} (max) defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
⑧ Operation within the t_{RCD} (max) limit ensures that t_{RAC} (max) can be met, t_{RCD} (max) is specified as a reference point only, if t_{RCD} is greater than the specified t_{RCD} (max) limit, then access time is controlled exclusively by t_{CAC}.
⑨ These parameters are referenced to $\overline{CAS}$ leading edge in early write cycles and to $\overline{WRITE}$ leading edge in delayed write or read-modify-write cycles.
⑩ t_{WCS}, t_{CWD} and t_{RWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only. If $t_{WCS} \geq t_{WCS}$ (min), the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) $\geq t_{RWD}$ (min), the cycle is a read-write cycle and the data out will contain data read from the selected cell; if neither of the above sets of conditions is satisfied the condition of the data out (at access time) is indeterminate.

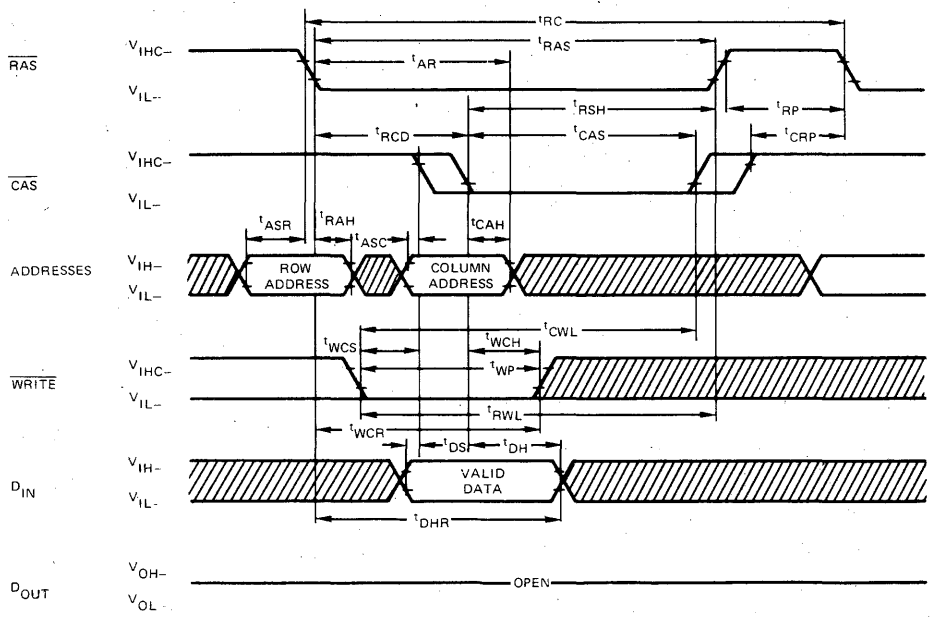
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TIMING WAVEFORMS

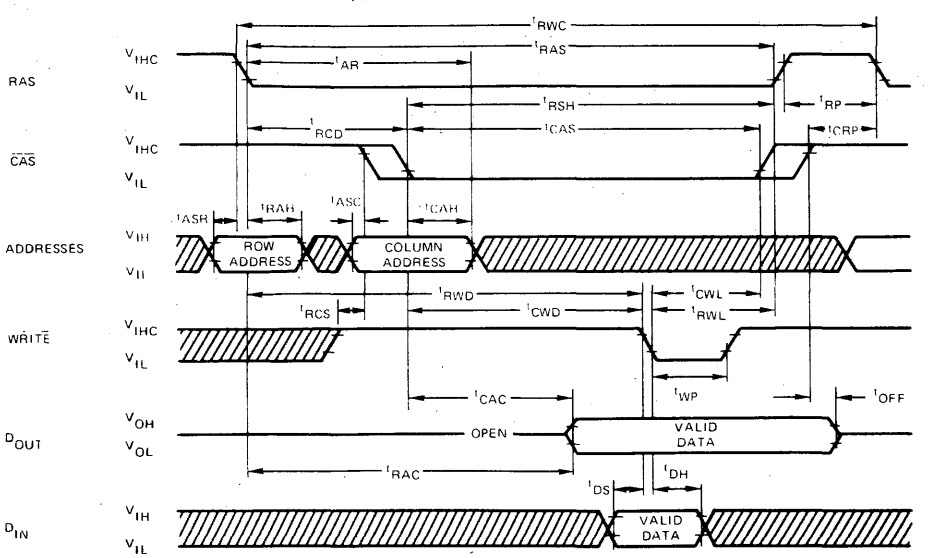
READ CYCLE



WRITE CYCLE



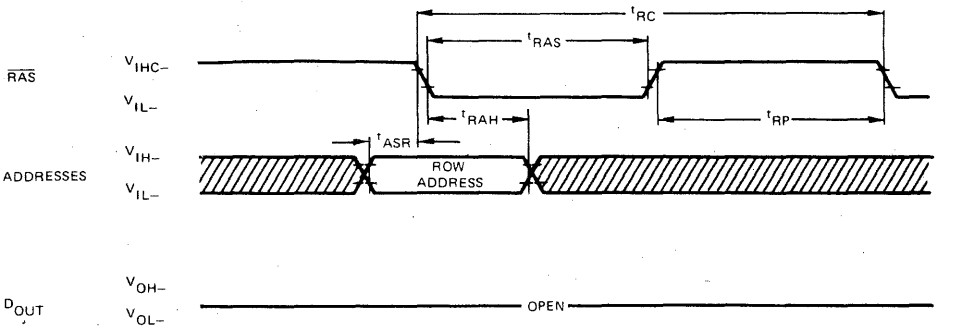
READ-WRITE/READ-MODIFY–WRITE CYCLE



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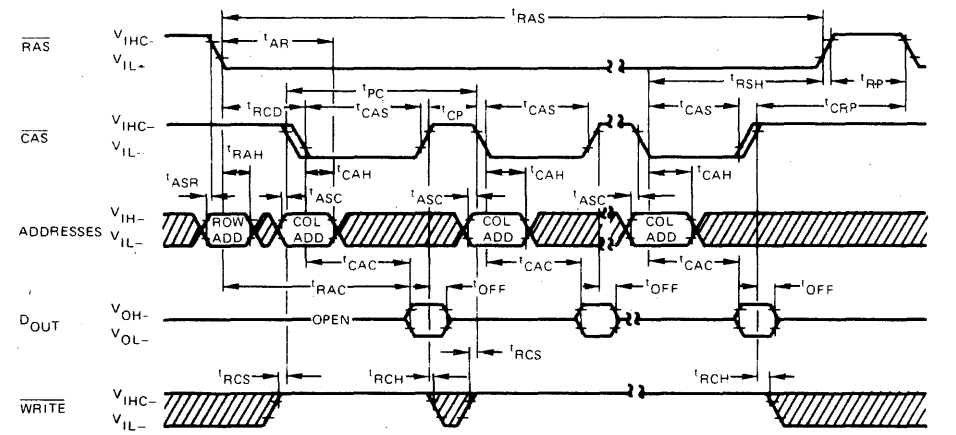
TIMING WAVEFORMS (CONT.)

"$\overline{RAS}$-ONLY" REFRESH CYCLE

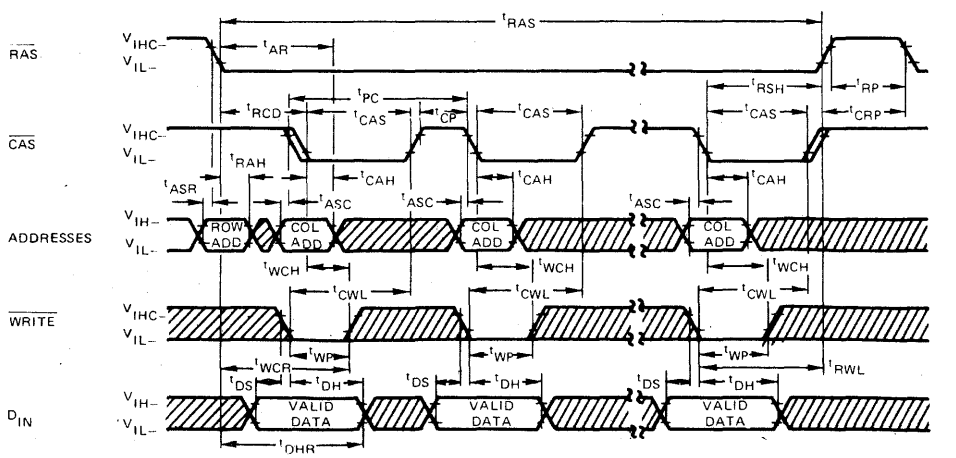


Note: $\overline{CAS}$ = V_{IHC}, $\overline{WRITE}$ = Don't Care

PAGE MODE READ CYCLE



PAGE MODE WRITE CYCLE



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ADDRESSING

The 14 address bits required to decode 1 of 16,384 bit locations are multiplexed onto the 7 address pins and then latched on the chip with the use of the Row Address Strobe ($\overline{RAS}$), and the Column Address Strobe ($\overline{CAS}$). The 7 bit row address is first applied and $\overline{RAS}$ is then brought low. After the $\overline{RAS}$ hold time has elapsed, the 7 bit column address is applied and $\overline{CAS}$ is brought low. Since the column address is not needed internally until a time of t_{CRD} MAX after the row address, this multiplexing operation imposes no penalty on access time as long as $\overline{CAS}$ is applied no later than t_{CRD} MAX. If this time is exceeded, access time will be defined from $\overline{CAS}$ instead of $\overline{RAS}$.

DATA I/O

For a write operation, the input data is latched on the chip by the negative going edge of $\overline{WRITE}$ or $\overline{CAS}$, whichever occurs later. If $\overline{WRITE}$ is active before $\overline{CAS}$, this is an "early WRITE" cycle and data out will remain in the high impedance state throughout the cycle. For a READ, WRITE, OR READ-MODIFY-WRITE cycle, the data output will contain the data in the selected cell after the access time. Data out will assume the high impedance state anytime that $\overline{CAS}$ goes high.

PAGE MODE

The page mode feature allows the μPD416 to be read or written at multiple column addresses for the same row address. This is accomplished by maintaining a low on $\overline{RAS}$ and strobing the new column addresses with $\overline{CAS}$. This eliminates the setup and hold times for the row address resulting in faster operation.

REFRESH

Refresh of the memory matrix is accomplished by performing a memory cycle at each of the 128 row addresses every 2 milliseconds or less. Because data out is not latched, "$\overline{RAS}$ only" cycles can be used for simple refreshing operation.

CHIP SELECTION

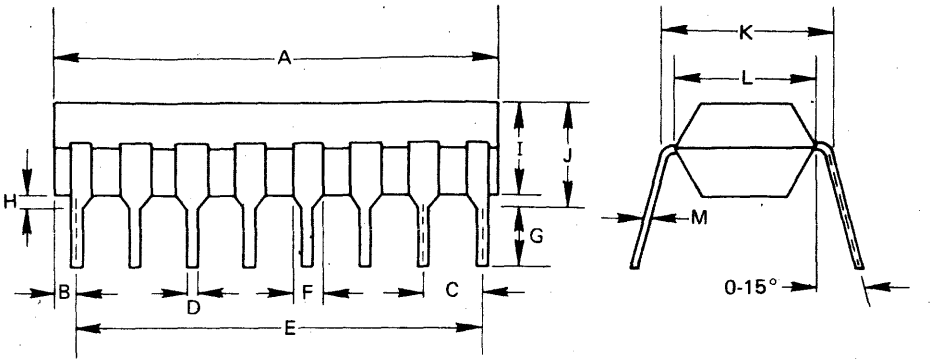
Either $\overline{RAS}$ and/or $\overline{CAS}$ can be decoded for chip select function. Unselected chip outputs will remain in the high impedance state.

POWER SEQUENCING

In order to assure long term reliability, V_{BB} should be applied first during power up and removed last during power down.

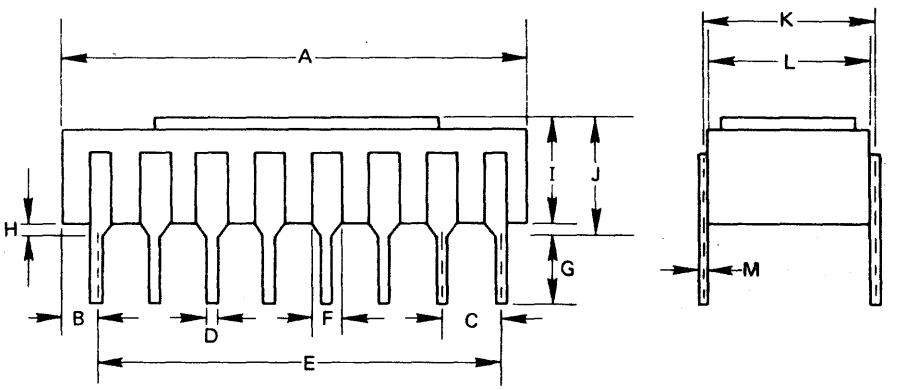
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PACKAGE OUTLINE
μPD416C/D



μPD416C
(Plastic)

ITEM	MILLIMETERS	INCHES
A	19.4 MAX.	0.76 MAX.
B	0.81	0.03
C	2.54	0.10
D	0.5	0.02
E	17.78	0.70
F	1.3	0.051
G	2.54 MIN.	0.10 MIN.
H	0.5 MIN.	0.02 MIN.
I	4.05 MAX.	0.16 MAX.
J	4.55 MAX.	0.18 MAX.
K	7.62	0.30
L	6.4	0.25
M	$0.25^{+0.10}_{-0.05}$	0.01



μPD416D
(Ceramic)

ITEM	MILLIMETERS	INCHES
A	20.5 MAX.	0.81 MAX.
B	1.36	0.05
C	2.54	0.10
D	0.5	0.02
E	17.78	0.70
F	1.3	0.051
G	3.5 MIN.	0.14 MIN.
H	0.5 MIN.	0.02 MIN.
I	4.6 MAX.	0.18 MAX.
J	5.1 MAX.	0.20 MAX.
K	7.6	0.30
L	7.3	0.29
M	0.27	0.01

SP416-8-78-GY-CAT

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NEC

μPD443/6508
μPD443/6508-1

PRELIMINARY

1024 BIT CMOS RANDOM ACCESS MEMORY

DESCRIPTION

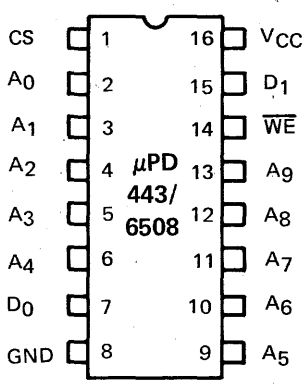
The μPD443/6508 is a high speed, low power, silicon gate CMOS 1024 bit static RAM organized as 1024 words by 1 bit. In all static states this RAM exhibits the microwatt power requirements typical of CMOS.

Inputs and three state output are TTL compatible. The basic part operates at 4 to 7 volts with a +5V, 25°C access time of 200 ns and supply current of 100 μA. Data retention is guaranteed to 3V on all parts.

FEATURES

- Low Power Operation
- Excellent Speed Operation
- TTL Compatible on Inputs and Outputs
- Static Operation
- On-Chip Address Register
- Replacement for IM 6508 and Equivalent Devices
- Available in Standard 16 Pin Ceramic Package

PIN CONFIGURATION

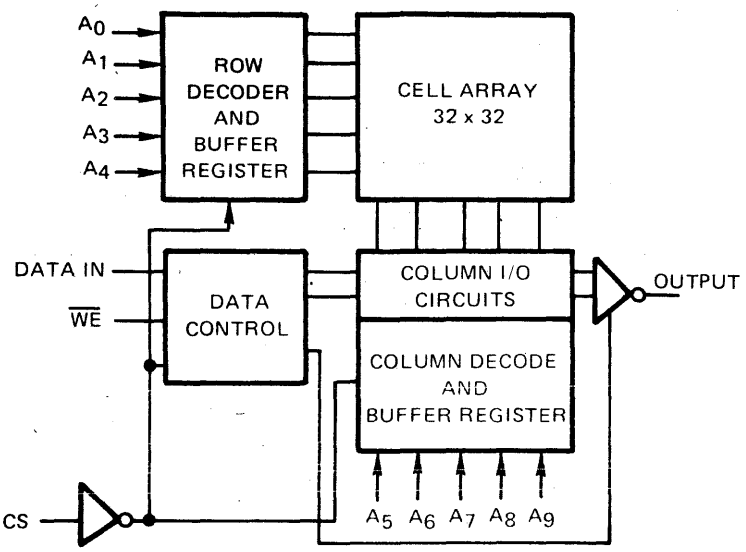


PIN NAMES

A_0-A_9	Address Input
CS	Chip Select
$\overline{WE}$	Write Enable
V_{CC}	Power (+5V)
D_I	Data Input
D_O	Data Output

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BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	0°C to +70°C
Storage Temperature	−65°C to +150°C
Input Voltages	−0.5 to V_{CC} +0.5 Volts
Output Voltages	−0.5 to V_{CC} +0.5 Volts
Supply Voltage	+8 Volts

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

DC CHARACTERISTICS

T_a = 0°C to +70°C; V_{CC} = +5V ± 5%

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Logical "1" Input Voltage	V_{IH}	V_{CC}−2.0			V	
Logical "0" Input Voltage	V_{IL}			0.8	V	
Input Leakage	I_{IL}	−1.0		1.0	μA	$0V \leq V_{IN} \leq V_{CC}$
Logical "1" Output Voltage	V_{OH2}	V_{CC}−0.01			V	I_{OUT} = 0
Logical "1" Output Voltage	V_{OH1}	2.4			V	I_{OH} = −0.2 mA
Logical "0" Output Voltage	V_{OL2}			GND+0.01	V	I_{OUT} = 0
Logical "0" Output Voltage	V_{OL1}			0.45	V	I_{OL} = 2.0 mA
Output Leakage	I_O	−1.0		1.0	μA	$0V \leq V_O \leq V_{CC}$
Supply Current	I_{CC}		1.0	100	μA	$V_{IN} = V_{CC}$

CAPACITANCE

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input Capacitance	C_{IN}		5.0	7.0	pF	
Output Capacitance	C_{OUT}		6.0	10.0	pF	

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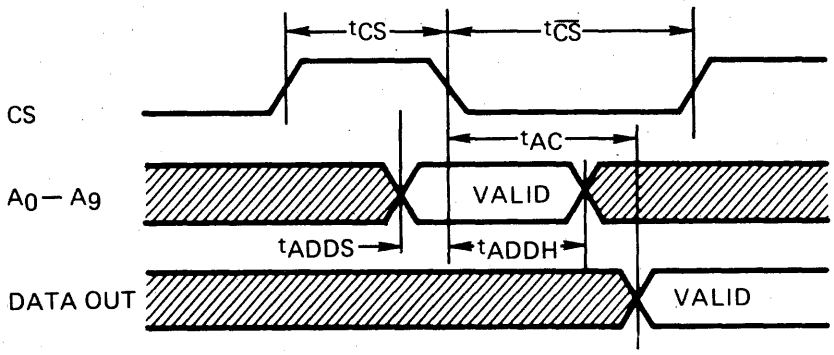
AC CHARACTERISTICS

T_a = 0°C to +70°C; V_{CC} = +5V ± 10%

PARAMETER	SYMBOL	LIMITS μPD443/6508-1 MIN	LIMITS μPD443/6508-1 MAX	LIMITS μPD443/6508 MIN	LIMITS μPD443/6508 MAX	UNIT	TEST CONDITIONS
Access Time From CS	t_{AC}		250		300	ns	$t_r = t_f$ = 20 ns V_{ref} = 50% Load = 1 TTL Gate C_L = 50 pF
Output Enable Time	t_{EN}		180		180	ns	
Output Disable Time	t_{DIS}		180		180	ns	
CS Pulse Width (Positive)	t_{CS}	150		165		ns	
CS Pulse Width (Negative)	$t_{\overline{CS}}$	250		300		ns	
Write Pulse Width (Negative)	t_{WP}	165		165		ns	
Address Set Up Time	t_{ADDS}	7		7		ns	
Address Hold Time	t_{ADDH}	90		90		ns	
Data Set Up Time	t_{DS}	165		165		ns	
Data Hold time	t_{DH}	0		0		ns	

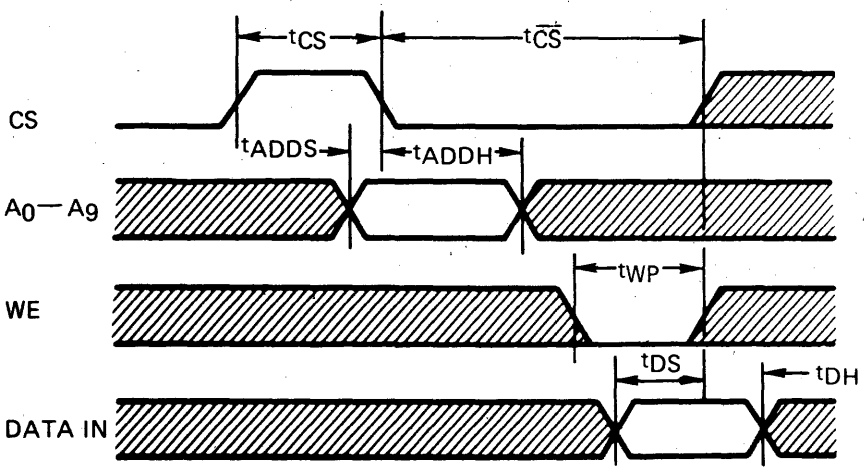
TIMING WAVEFORMS

READ CYCLE



Note: ① The μPD443/6508 output is active when CS is low.

WRITE CYCLE

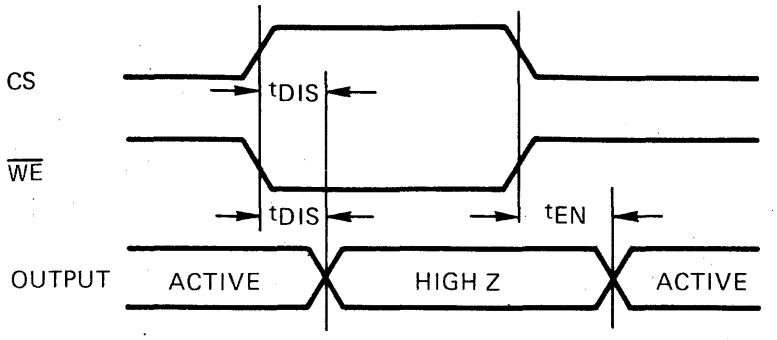


Notes: ① The μPD443/6508 performs a write operation when CS = WE = 0.
② The write operation is terminated on the positive edge from CS.

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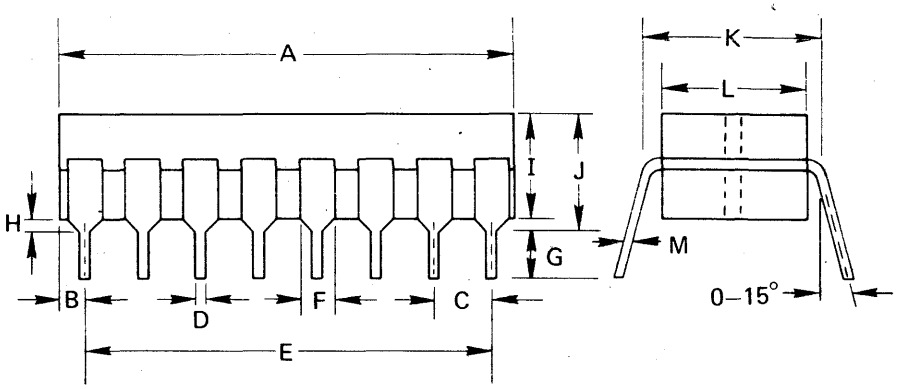
TIMING WAVEFORMS (CONT.)

OUTPUT ENABLE



Note: ① μPD443/6508 output is high impedance when CS = 1 or $\overline{WE}$ = 0.

PACKAGE OUTLINE μPD443/6508D



ITEM	MILLIMETERS	INCHES
A	19.9 MAX	0.784 MAX
B	1.06	0.042
C	2.54	0.10
D	0.46 ± 0.10	0.018 ± 0.004
E	17.78	0.70
F	1.5	0.059
G	2.54 MIN	0.10 MIN
H	0.5 MIN	0.019 MIN
I	4.58 MAX	0.181 MAX
J	5.08 MAX	0.20 MAX
K	7.62	0.30
L	6.4	0.25
M	$0.25^{+0.10}_{-0.05}$	$0.0098^{+0.0039}_{-0.0019}$

SP443/6508-9-78-GY-CAT

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1024 BIT (256x4) STATIC CMOS RAM

DESCRIPTION

The μPD5101L and μPD5101L-1 are very low power 1024 bit (256 words by 4 bits) static CMOS Random Access Memories. They meet the low power requirements of battery operated systems and can be used to ensure non-volatility of data in systems using battery backup power.

All inputs and outputs of the μPD5101L and μPD5101L-1 are TTL compatible. Two chip enables ($\overline{CE}_1$, CE_2) are provided, with the devices being selected when $\overline{CE}_1$ is low and CE_2 is high. The devices can be placed in standby mode, drawing 10 μA maximum, by driving $\overline{CE}_1$ high and inhibiting all address and control line transitions. The standby mode can also be selected unconditionally by driving CE_2 low.

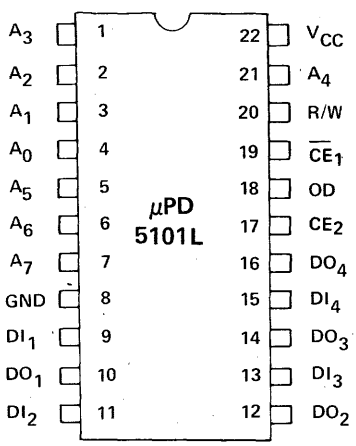
The μPD5101L and μPD5101L-1 have separate input and output lines. They can be used in common I/O bus systems through the use of the OD (Output Disable) pin and OR-tying the input/output pins. Output data is the same polarity as input data and is nondestructively read out. Read mode is selected by placing a high on the R/W pin. Either device is guaranteed to retain data with the power supply voltage as low as 2.0 volts. Normal operation requires a single +5 volt supply.

The μPD5101L and μPD5101L-1 are fabricated using NEC's silicon gate complementary MOS (CMOS) process.

FEATURES

- Directly TTL Compatible – All Inputs and Outputs
- Three-State Output
- Access Time – 650 ns (μPD5101L); 450 ns (μPD5101L-1)
- Single +5V Power Supply
- CE_2 Controls Unconditional Standby Mode
- Available in a 22-pin Dual-in-Line Package

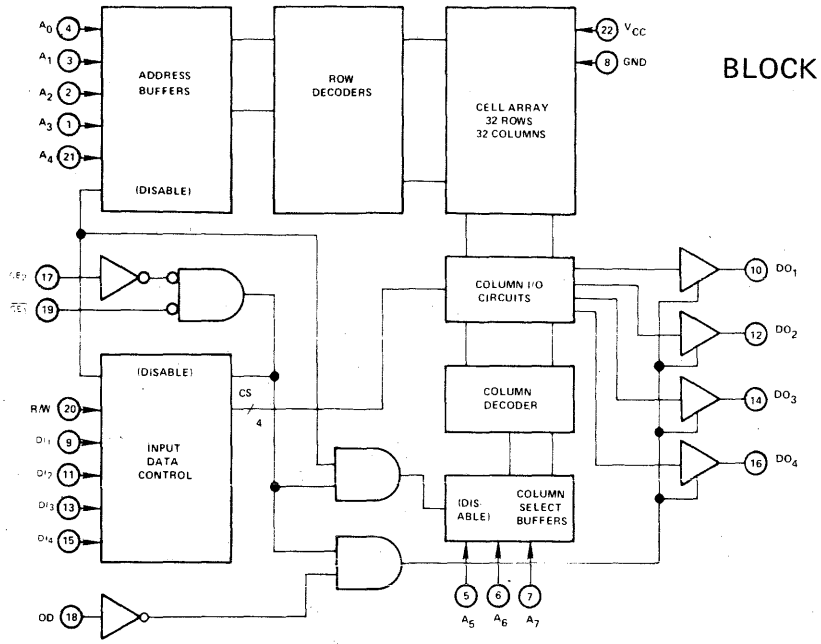
PIN CONFIGURATION



PIN NAMES

$DI_1 - DI_4$	Data Input
$A_0 - A_7$	Address Inputs
R/W	Read/Write Input
$\overline{CE}_1$, CE_2	Chip Enables
OD	Output Disable
$DO_1 - DO_4$	Data Output
V_{CC}	Power (+5V)

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BLOCK DIAGRAM

ABSOLUTE MAXIMUM RATINGS*

Operating Temperature . . . . . 0°C to +70°C
Storage Temperature . . . . . −40°C to +125°C
Voltage On Any Pin With Respect to Ground . . . . . −0.3 Volts to V_{CC} +0.3 Volts
Power Supply Voltage . . . . . −0.3 to +7.0 Volts

COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

DC CHARACTERISTICS

T_a = 0°C to 70°C; V_{CC} = +5V ± 5%, unless otherwise specified.

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP ①	LIMITS MAX	UNIT	TEST CONDITIONS
Input High Leakage	I_{LIH} ②			1	μA	$V_{IN} = V_{CC}$
Input Low Leakage	I_{LIL} ②			−1	μA	V_{IN} = 0V
Output High Leakage	I_{LOH} ②			1	μA	$\overline{CE}_1$ = 2.2V, $V_{OUT} = V_{CC}$
Output Low Leakage	I_{LOL} ②			−1	μA	$\overline{CE}_1$ = 2.2V, V_{OUT} = 0.0V
Operating Current	I_{CC1}			22	mA	$V_{IN} = V_{CC}$ Except $\overline{CE}_1$ ≤0.65V, Outputs Open
Operating Current	I_{CC2}			27	mA	V_{IN} = 2.2V Except $\overline{CE}_1$ ≤0.65V, Outputs Open
Standby Current	I_{CCL} ②			10	μA	V_{IN} = 0 to 5.25V $CE_2 \leq$ 0.2V
Input Low Voltage	V_{IL}	−0.3		0.65	V	
Input High Voltage	V_{IH}	2.2		V_{CC}	V	
Output Low Voltage	V_{OL}			0.4	V	I_{OL} = 2.0 mA
Output High Voltage	V_{OH1}	2.4			V	I_{OH} = −1.0 mA
Output High Voltage	V_{OH2}	3.5			V	I_{OH} = −100 μA

Notes: ① Typical values at T_a = 25°C and nominal supply voltage.
② Current through all inputs and outputs included in I_{CCL}.

CAPACITANCE

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input Capacitance (All Input Pins)	C_{IN}		4	8	pF	V_{IN} 0V
Output Capacitance	C_{OUT}		8	12	pF	V_{OUT} 0V

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AC CHARACTERISTICS

READ CYCLE

T_a = 0°C to 70°C; V_{CC} = 5V±5%, unless otherwise specified

PARAMETER	SYMBOL	LIMITS 5101L MIN	5101L TYP	5101L MAX	5101L-1 MIN	5101L-1 TYP	5101L-1 MAX	UNIT	TEST CONDITIONS
Read Cycle	t_{RC}	650			450			ns	Input pulse amplitude: 0.65 to 2.2 Volts
Access Time	t_A			650			450	ns	Input rise and fall times: 20 ns
Chip Enable ($\overline{CE}_1$) to Output	t_{CO1}			600			400	ns	Timing measurement reference level: 1.5 Volt
Chip Enable (CE_2) to Output	t_{CO2}			700			500	ns	Output load: I_{TTL}
Output Disable to Output	t_{OD}			350			250	ns	Gate and C_L = 100 pF
Data Output to High Z State	t_{DF}	0		150	0		130	ns	
Previous Read Data Valid with Respect to Address Change	t_{OH1}	0			0			ns	
Previous Read Data Valid with Respect to Chip Enable	t_{OH2}	0			0			ns	

WRITE CYCLE

T_a = 0°C to 70°C; V_{CC} = 5V±5%, unless otherwise specified

PARAMETER	SYMBOL	LIMITS 5101L MIN	5101L TYP	5101L MAX	5101L-1 MIN	5101L-1 TYP	5101L-1 MAX	UNIT	TEST CONDITIONS
Write Cycle	t_{WC}	650			450			ns	Input pulse amplitude: 0.65 to 2.2 Volts
Write Delay	t_{AW}	150			130			ns	Input rise and fall times: 20 ns
Chip Enable ($\overline{CE}_1$) to Write	t_{CW1}	550			350			ns	Timing measurement reference level: 1.5 Volt
Chip Enable (CE_2) to Write	t_{CW2}	550			350			ns	Output load: I_{TTL}
Data Setup	t_{DW}	400			250			ns	Gate and C_L = 100 pF
Data Hold	t_{DH}	100			50			ns	
Write Pulse	t_{WP}	400			250			ns	
Write Recovery	t_{WR}	50			50			ns	
Output Disable Setup	t_{DS}	150			130				

LOW V_{CC} DATA RETENTION CHARACTERISTICS

T_a = 0°C to 70°C

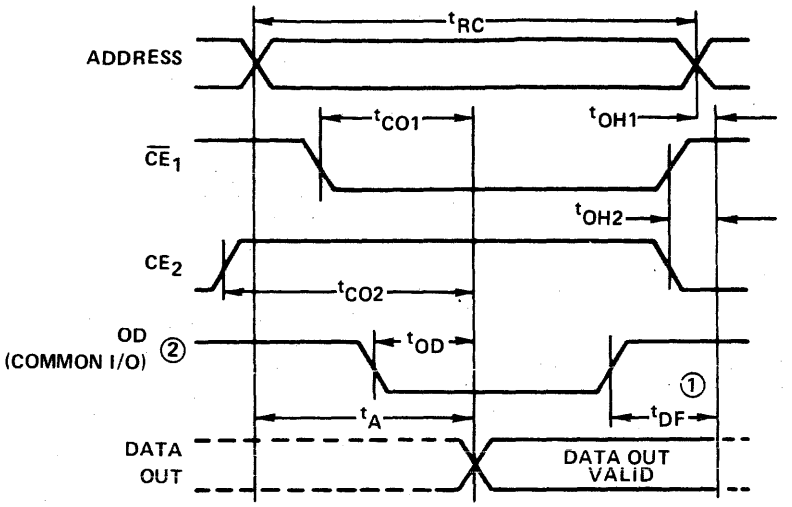
PARAMETER	SYMBOL	LIMITS MIN	TYP	MAX	UNIT	TEST CONDITIONS
V_{CC} for Data Retention	V_{CCDR}	+2.0			V	$CE_2 \geq +0.2V$
Data Retention Current	I_{CCDR}			+10	μA	V_{CCDR} = +2.0V $CE_2 \geq +0.2V$
Chip Deselect Setup Time	t_{CDR}	0			ns	
Chip Deselect Hold Time	t_R	t_{RC}①			ns	

Note: ① t_{RC} = Read Cycle Time

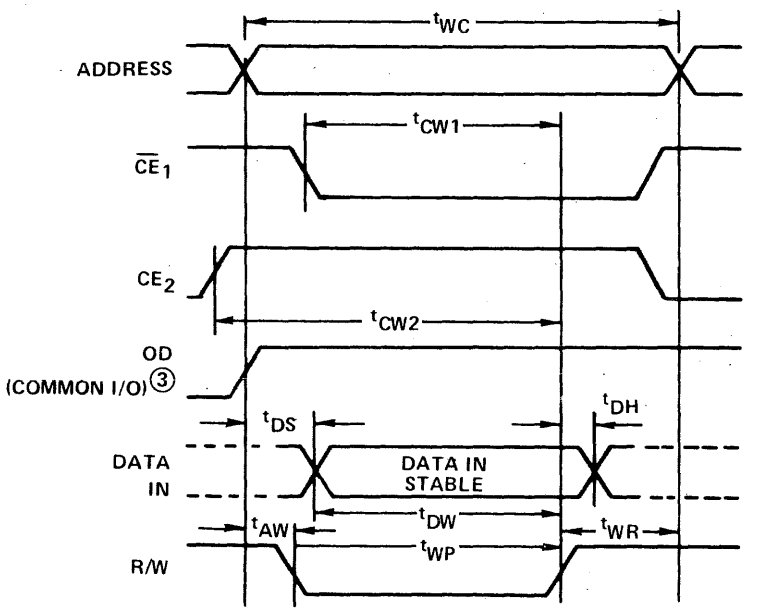
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TIMING WAVEFORMS

READ CYCLE

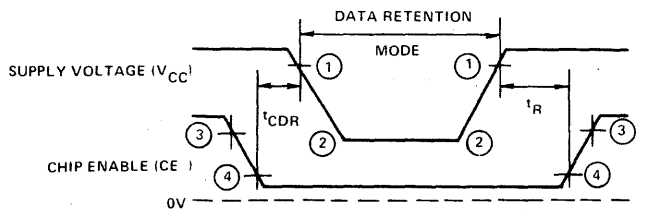


WRITE CYCLE



Notes: ① Typical values are for $T_a = 25°C$ and nominal supply voltage.
② OD may be tied low for separate I/O operation.
③ During the write cycle, OD is "high" for common I/O and "don't care" for separate I/O operation.

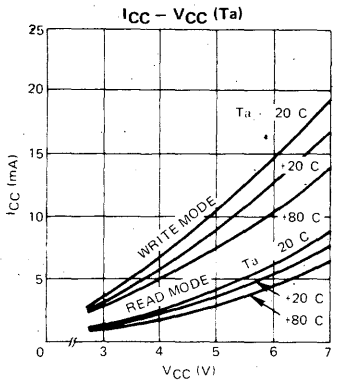
LOW V_{CC} DATA RETENTION

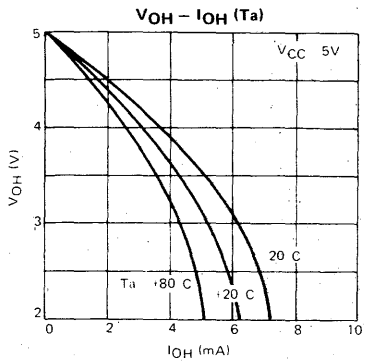


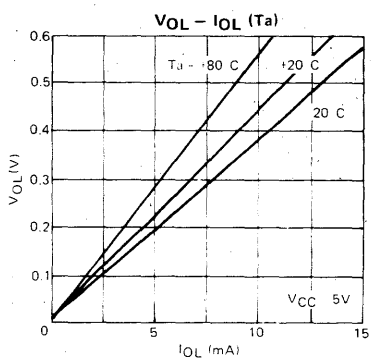
Notes: ① 4.75V
② V_{CCDR}
③ V_{IH}
④ 0.2V

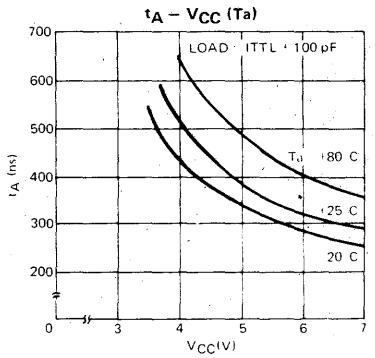
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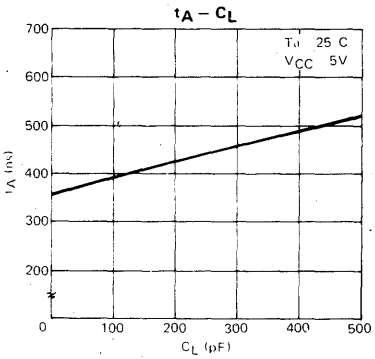
TYPICAL OPERATING CHARACTERISTICS

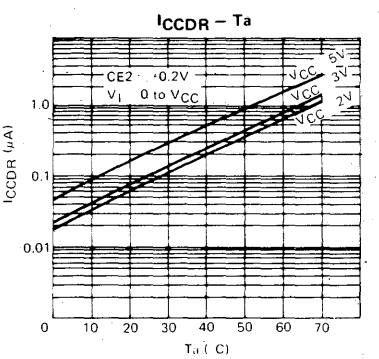




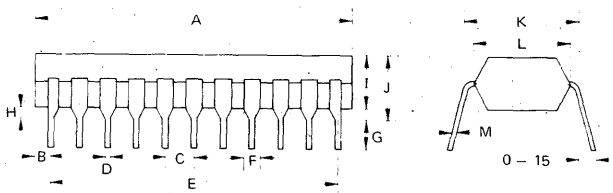








PACKAGE OUTLINE μPD5101LC



ITEM	MILLIMETERS	INCHES
A	28.0 Max.	1.10 Max.
B	1.4 Max.	0.025 Max.
C	2.54	0.10
D	0.50 ± 0.10	0.02 ± 0.004
E	25.4	1.0
F	1.40	0.055
G	2.54 Min.	0.10 Min.
H	0.5 Min.	0.02 Min.
I	4.7 Max.	0.18 Max.
J	5.2 Max.	0.20 Max.
K	10.16	0.40
L	8.5	0.33
M	$0.25^{+0.10}_{-0.05}$	$0.01^{+0.004}_{-0.002}$

SP5101L-8-77-GY-CAT

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4K STATIC CMOS RAM

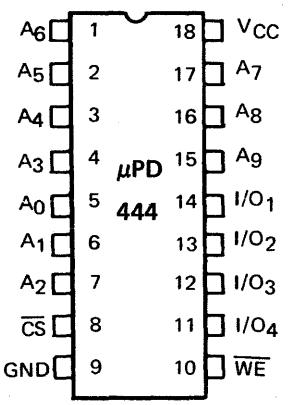
DESCRIPTION

The μPD444 is a 4K Static CMOS RAM, organized as 1K x 4. Its use of CMOS technology assures extremely low operating and standby power requirements.

FEATURES

- Compatible with 2114L
- Single +5V Supply
- Fully Static — No Clocks
- 300 ns Access Time

PIN CONFIGURATION



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FULLY DECODED 4096 STATIC CMOS RAM

DESCRIPTION

The μPD445L is a very low power 4,096 bit (1024 words by 4 bits) static RAM fabricated with NEC's complementary MOS (CMOS) process. It has two chip enable inputs ($\overline{CE}_1$, CE_2). Minimum standby current is drawn when $\overline{CE}_1$ is at a high level, while inhibiting all address and control line transitions or, unconditionally when CE_2 is at a low level. This device ideally meets the low power requirements of battery operated systems and battery back-up systems for non-volatility of data.

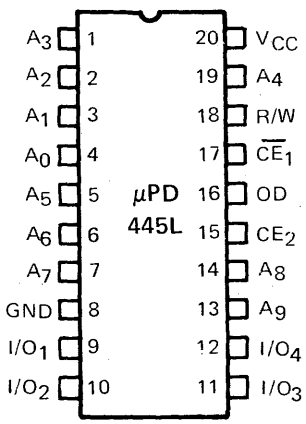
The μPD445L uses fully static circuitry requiring no clocking. Output data is read out non-destructively by placing a high on the R/W pin and has the same polarity as input data. All inputs and outputs are directly TTL compatible. The device has common input/output data busses and an OD (Output Disable) pin for use in common I/O bus systems.

The μPD445L is guaranteed to retain data with the power supply voltage as low as 2.0 volts.

FEATURES

- Single +5V Power Supply
- Ideal for Battery Operation
- Low Standby Power for Data Retention
- Simple Memory Expansion – Chip Enable Inputs
- Access Time – 650 ns Max. (μPD445L)
  450 ns Max. (μPD445L-1)
- Directly TTL Compatible – All Inputs and Outputs
- Common Data Input and Output
- Static CMOS – No Clocks Refreshing Required
- 20 Pin Dual-In-Line Plastic Package

PIN CONFIGURATION



PIN NAMES

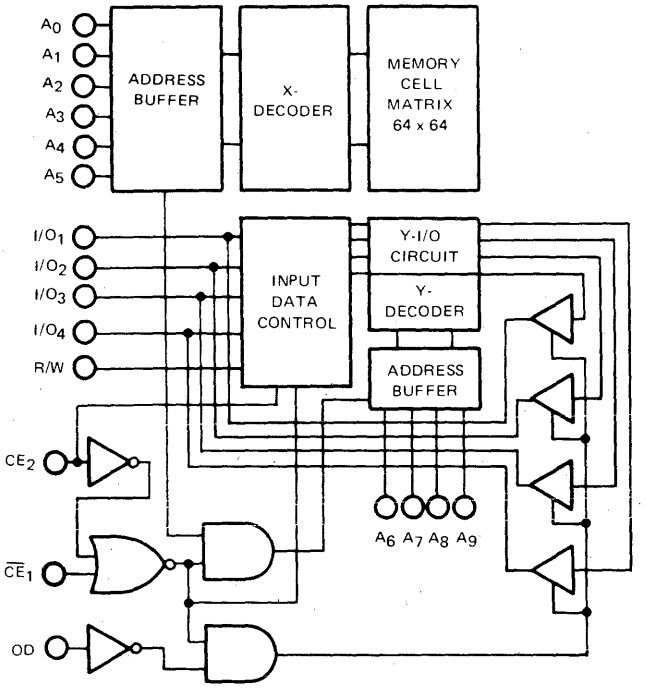
A_0-A_9	Address Input
OD	Output Disable
R/W	Read/Write
$\overline{CE}_1$	Chip Enable 1
CE_2	Chip Enable 2
I/O_1-I/O_4	Data Input/Output
V_{CC}	Power Supply
GND	Ground

OPERATION MODES

$\overline{CE}_1$	CE_2	OD	Chip	Output Mode
0	1	0	Selected	Data Out
0	1	1		High Impedance
Others			Non-Selected	

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BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature . . . . . −10°C to +70°C
Storage Temperature. . . . . −40°C to +125°C
All Output Voltages . . . . . −0.3 to V_{CC} +0.3 Volts
All Input Voltages . . . . . −0.3 to V_{CC} +0.3 Volts
Supply Voltage V_{CC} . . . . . −0.3 to +7 Volts

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

DC CHARACTERISTICS

T_a = −10 to +70°C; +5V ± 10%

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input High Voltage	V_{IH}	+2.2		V_{CC}	V	
Input Low Voltage	V_{IL}	−0.3		+ 0.65	V	
Output High Voltage	V_{OH1}	+2.4			V	I_{OH} = −1.0 mA
	V_{OH2}	+3.5			V	I_{OH} = −100 μA
Output Low Voltage	V_{OL}			+ 0.4	V	I_{OL} = +2.0 mA
Input Leakage Current High	I_{LIH}			+ 1.0	μA	$V_I = V_{CC}$
Input Leakage Current Low	I_{LIL}			− 1.0	μA	V_I = 0V
Output Leakage Current High	I_{LOH}			+ 1.0	μA	$V_O = V_{CC}$, $\overline{CE}_1$ = 2.2V
Output Leakage Current Low	I_{LOL}			− 1.0	μA	V_O = 0V, $\overline{CE}_1$ = 2.2V
Supply Current	I_{CC1}		12	25	mA	Outputs Open $V_I = V_{CC}$ except $\overline{CE}_1 \leq 0.65V$
Supply Current	I_{CC2}		16	30	mA	Outputs Open V_I = 2.2V except $\overline{CE}_1 \leq 0.65V$
Standby Current	I_{CCL}			40	μA	V_I = 0 to 5.25V Except $CE_2 \leq 0.2V$

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AC CHARACTERISTICS

READ CYCLE

$T_a = -10°C$ to $+70°C$; $V_{CC} = +5V \pm 10\%$

PARAMETER	SYMBOL	LIMITS 445L MIN	LIMITS 445L MAX	LIMITS 445L-1 MIN	LIMITS 445L-1 MAX	UNIT	TEST CONDITIONS
Read Cycle Time	t_{RC}	650		450		ns	
Access Time	t_A		650		450	ns	Input Voltage Levels V = +0.65 to +2.2V
Chip Enable ($\overline{CE_1}$) to Output	t_{CO1}		600		400	ns	
Chip Enable (CE_2) to Output	t_{CO2}		700		500	ns	Input Rise Time 20 ns
Output Enable to Output	t_{OD}		350		250	ns	Input Fall Time 20 ns
Output Disable (OD) to Floating	t_{DF}	0	150	0	130	ns	Timing Measurement Reference Level = +1.5V
Data Output Hold Time	t_{OH1}	0		0		ns	Output Load
Chip Disable to Floating	t_{OH2}	0		0		ns	1 TTL + 100 pF
Address Rise and Fall Time	t_r t_f		300		300	ns	For Address change during Chip Enabled

WRITE CYCLE

$T_a = 0°C$ to $+70°C$; $V_{CC} = +5V \pm 10\%$

PARAMETER	SYMBOL	LIMITS 445L MIN	LIMITS 445L MAX	LIMITS 445L-1 MIN	LIMITS 445L-1 MAX	UNIT	TEST CONDITIONS
Write Cycle Time	t_{WC}	650		450		ns	
Address Setup Time	t_{AW}	150		130		ns	Input Voltage Levels V_I = +0.65 to +2.2V
Chip Enable ($\overline{CE_1}$) to Write End	t_{CW1}	550		350		ns	Input Rise Time 20 ns
Chip Enable (CE_2) to Write End	t_{CW2}	550		350		ns	Input Fall Time 20 ns
Data Setup Time	t_{DW}	400		250		ns	
Data Hold Time	t_{DH}	100		50		ns	Timing Measurement
Write Pulse Width	t_{WP}	400		250		ns	Reference Level = +1.5V
Address Hold Time	t_{WR}	50		50		ns	
Output Disable Setup Time	t_{DS}	150		130		ns	
Address Rise and Fall Time	t_r t_f		300		300	ns	For Address change during Chip Enabled

LOW V_{CC} DATA RETENTION

$T_a = -10°C$ to $+70°C$

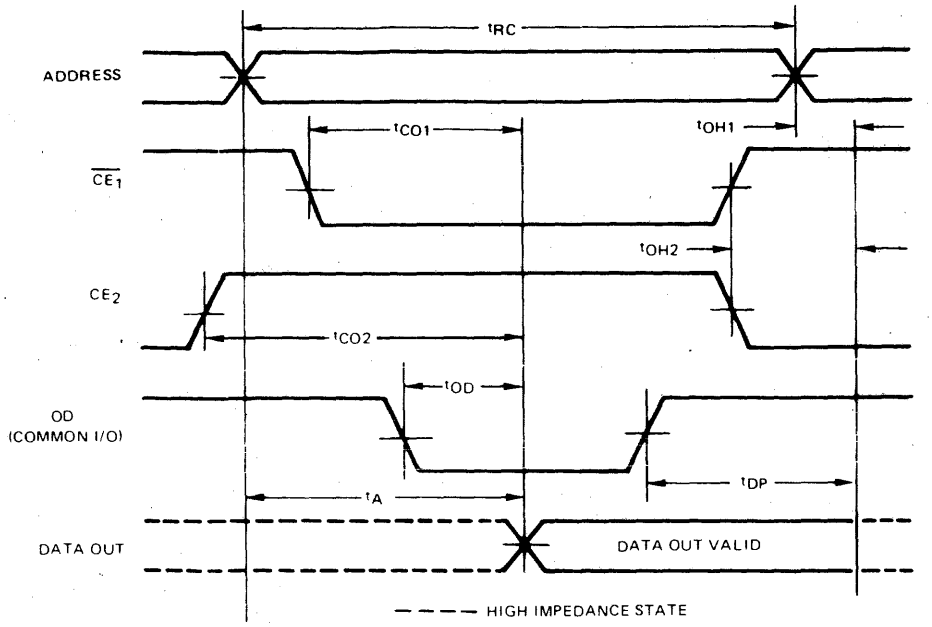
PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
V_{CC} for Data Retention	V_{CCDR}	+2.0			V	$CE_2 \leqslant +0.2V$
Data Retention Current	I_{CCDR}			40	μA	V_{CCDR} = +2.0V $CE_2 \leqslant +0.2V$
Chip Deselect Setup Time	t_{CDR}	0			ns	
Chip Deselect Hold Time	t_R	t_{RC} ①			ns	

Note: ① t_{RC} = Read Cycle Time

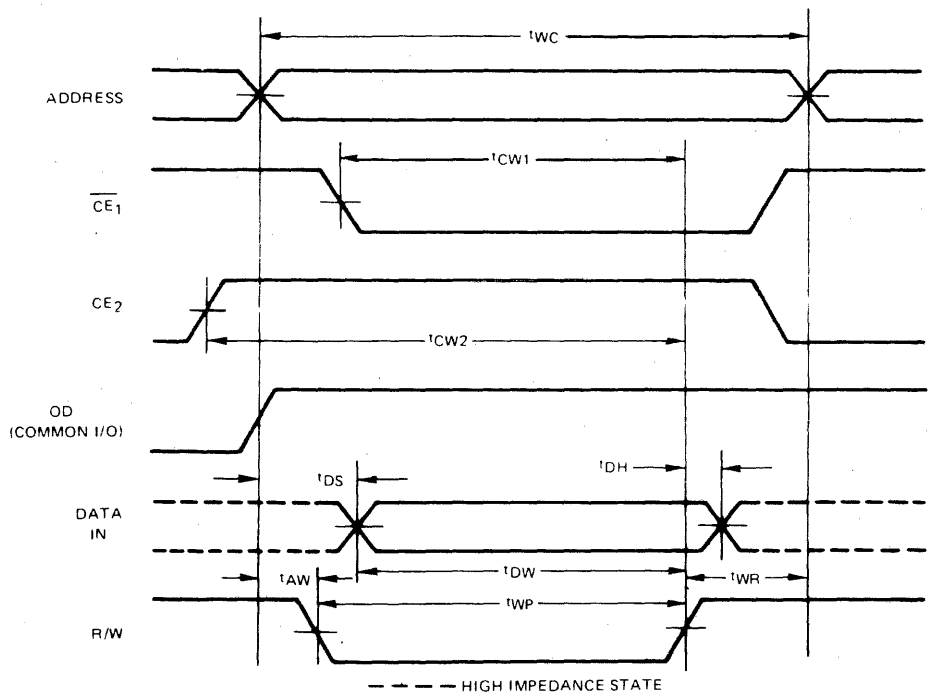
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TIMING WAVEFORMS

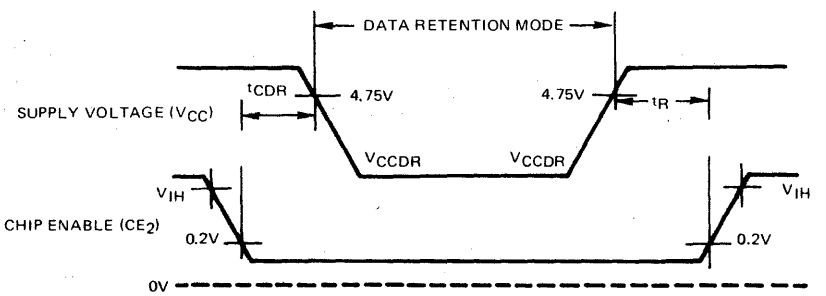
READ CYCLE



WRITE CYCLE



LOW V_{CC} DATA RETENTION ①



Note ① Apply less than V_{CCDR} to all inputs for data retention mode.

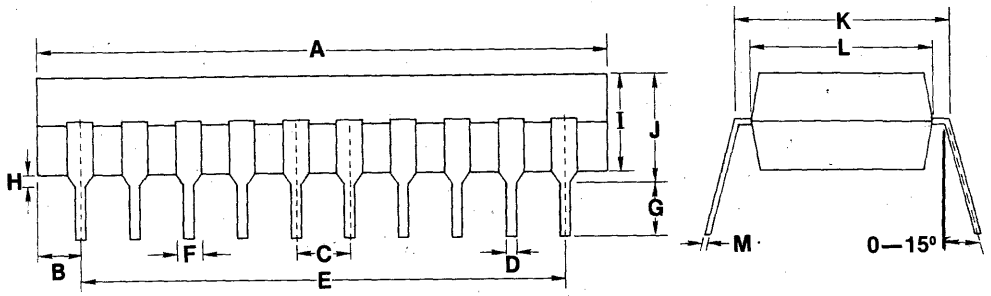
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CAPACITANCE

T_a = 25°C; f = 1 MHz

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input Capacitance	C_I		5	8	pF	V_I = 0V
Output Capacitance	C_O		8	12	pF	V_O = 0V

PACKAGE OUTLINE μPD445LC



ITEM	MILLIMETERS	INCHES
A	27.00	1.07
B	2.07	0.08
C	2.54	0.10
D	0.50	0.02
E	22.86	0.90
F	1.20	0.05
G	2.54 MIN	0.10 MIN
H	0.50 MIN	0.02 MIN
I	4.58 MAX	0.18
J	5.08 MAX	0.20
K	10.16	0.40
L	8.60	0.39
M	$0.25^{+0.10}_{-0.05}$	$0.01^{+0.004}_{-0.002}$

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NEC

μPD2101AL
μPD2101AL-2
μPD2010AL-4

1024 BIT (256 X 4) STATIC MOS RAM WITH SEPARATE I/O

DESCRIPTION

The μPD2101AL is a 256 word by 4 bit static random access memory requiring no clocks or refreshing. It features high speed, low cost, and simplicity of interfacing.

It is directly TTL compatible in all respects; inputs, outputs, and a single +5V supply. Two chip-enables allow easy selection of an individual package when outputs are OR-tied. An output disable is provided so that data inputs and outputs can be tied for common I/O systems. The output disable function eliminates the need for bidirectional logic in a common I/O system. Output data is the same polarity as input data, and readout is non-destructive.

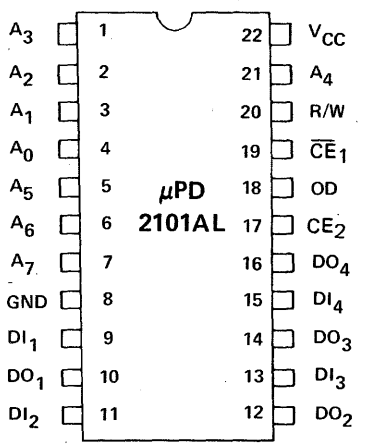
The μPD2101AL family of devices offers access times from 450 ns to 250 ns with a typical standby mode power dissipation of only 36 mW.

The use of NEC's N-channel silicon gate MOS process, with its excellent protection from contamination, permits the use of a low cost 22 pin plastic package in providing a high performance, high reliability MOS circuit at a most cost effective price level. The μPD2101AL is pin-compatible with the μPD5101 CMOS static RAM.

FEATURES

- 256 x 4 Organizations to Meet Needs for Small System Memories
- Access Time – 250 to 450 nsec max
- Directly TTL Compatible – All Inputs and Output
- Static MOS – No Clocks or Refreshing Required
- Simple Memory Expansion – Chip Enable Input
- Low Standby Power – 36 mW typ.
- Low Cost Packaging – 22 Pin Plastic Dual-In-Line Configuration
- Low Operating Power
- Three-State Output – OR-Tie Capability
- Output Disable Provided for Ease of Use in Common Data Bus Systems

PIN CONFIGURATION



PIN NAMES

DI_1–DI_4	DATA INPUT	CE_2	CHIP ENABLE 2
A_0–A_7	ADDRESS INPUTS	OD	OUTPUT DISABLE
R/W	READ/WRITE INPUT	DO_1–DO_4	DATA OUTPUT
$\overline{CE}_1$	CHIP ENABLE 1	V_{CC}	POWER (+5V)

OPERATION MODES

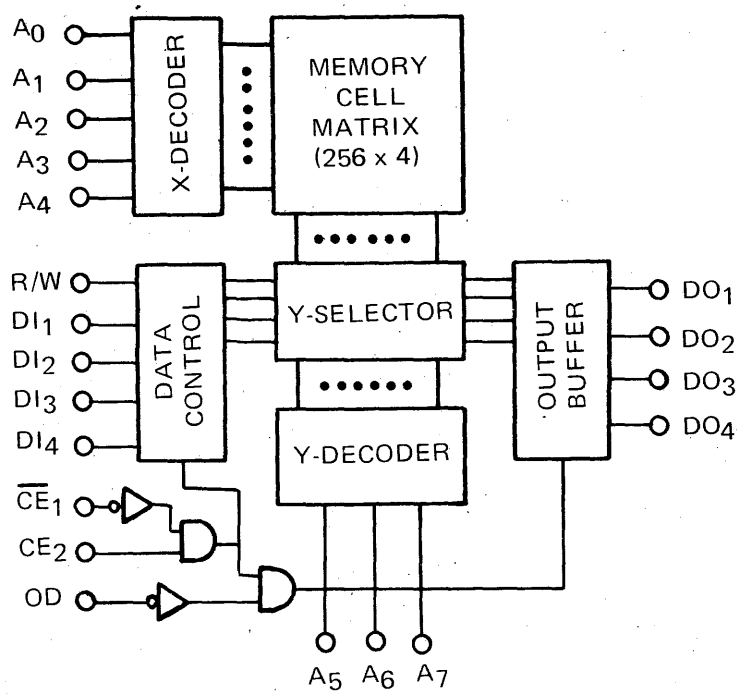
$\overline{CE}_1$	CE_2	OD	CHIP	OUTPUT MODE
0	1	0	Selected	Data Out
0	1	1		High Impedance
Others			No-Selected	

NEC Microcomputer

MEMORY

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BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	−10°C to +70°C
Storage Temperature	−65°C to +125°C
All Output Voltages	−0.5 to +7 Volts
All Input Voltages	−0.5 to +7 Volts
Supply Voltage V_{CC}	−0.5 to +7 Volts

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

DC CHARACTERISTICS

T_a = −10°C to +70°C, V_{CC} = +5V ± 5%

PARAMETER.	SYMBOL	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNIT	TEST CONDITIONS
Input High Voltage	V_{IH}	+2.0		V_{CC}	V	
Input Low Voltage	V_{IL}	−0.5		+0.8	V	
Output High Voltage	V_{OH}	+2.4			V	I_{OH} = −100 μA
Output Low Voltage	V_{OL}			+0.4	V	I_{OL} = +2.1 mA
Input Leakage Current High	I_{LIH}			+10	μA	$V_I = V_{CC}$
Input Leakage Current Low	I_{LIL}			−10	μA	V_I = 0V
Output Leakage Current High	I_{LOH}			+10	μA	V_O = +2.4V to V_{CC} $\overline{CE}_1$ = +2.0V
Output Leakage Current Low	I_{LOL}			−10	μA	V_O = +0.4V $\overline{CE}_1$ = +2.0V
Power Supply Current	I_{CC1}			+60	mA	V_I = +5.25V I_O = 0 mA T_a = +25°C
Power Supply Current	I_{CC2}			+70	mA	V_I = +5.25V I_O = 0 mA T_a = −10°C to +70°C

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AC CHARACTERISTICS

READ CYCLE

$T_a = -10°C$ to $+70°C$, $V_{CC} = +5V \pm 5\%$

PARAMETER	SYMBOL	LIMITS									UNIT
		2101AL-4			2101AL			2101AL-2			
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Read Cycle Time	t_{RC}	450			350			250			ns
Access Time	t_A			450			350			250	ns
Chip Enable to Output	t_{CO}			180			150			130	ns
Output Disable to Output	t_{OD}			150			130			120	ns
Data Output to High Z State	t_{DF}*	0		130	0		115	0		100	ns
Previous Read Data Valid After Change of Address	t_{OH}	40			40			40			ns

*t_{DF} is with respect to the trailing edge of $\overline{CE}_1$, CE_2, or OD, whichever occurs first.

WRITE CYCLE

$T_a = -10°C$ to $+70°C$, $V_{CC} = +5V \pm 5\%$

PARAMETER	SYMBOL	LIMITS									UNIT
		2101AL-4			2101AL			2101AL-2			
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Write Cycle Time	t_{WC}	450			350			250			ns
Write Delay	t_{AW}	20			20			20			ns
Chip Enable to Write	t_{CW}	180			150			130			ns
Data Setup Time	t_{DW}	180			150			130			ns
Data Hold Time	t_{DH}	0			0			0			ns
Write Pulse Width	t_{WP}	160			130			120			ns
Write Recovery	t_{WR}	0			0			0			ns
Output Disable Setup	t_{DS}	20			20			10			ns

Note: OD is a logical 1 for common I/O and "don't care" for separate I/O operation.

STANDBY CHARACTERISTICS

$T_a = -10°C$ to $+70°C$

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN.	TYP①	MAX.		
V_{CC} in Standby	V_{PD}	1.5			V	
$\overline{CE}_1$ Bias in Standby	V_{CES}	2.0			V	$2.0V \leqslant V_{PD} \leqslant 5.25V$
		V_{PD}			V	$1.5V \leqslant V_{PD} < 2.0V$
Standby Current Drain	I_{PD1}		24	36	mA	All Inputs = $V_{PD1} = 1.5V$
Standby Current Drain	I_{PD2}		30	45	mA	All Inputs = $V_{PD2} = 2.0V$
Chip Deselect to Standby Time	t_{CP}	0			ns	
Standby Recovery Time	t_R	t_{RC}②			ns	

Notes: ① Typical values are for $T_a = 25°C$ and nominal supply voltage.

② $t_R = t_{RC}$ (Read Cycle Time).

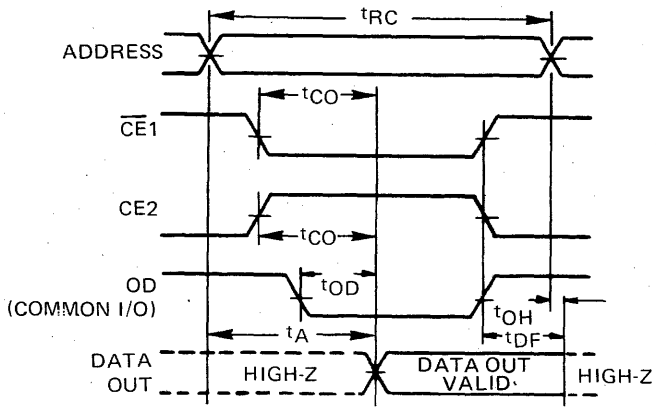
CAPACITANCE

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN.	TYP.	MAX.		
Input Capacitance	C_{IN}			8	pf	$V_I = 0V$
Output Capacitance	C_{OUT}			12	pf	$V_O = 0V$

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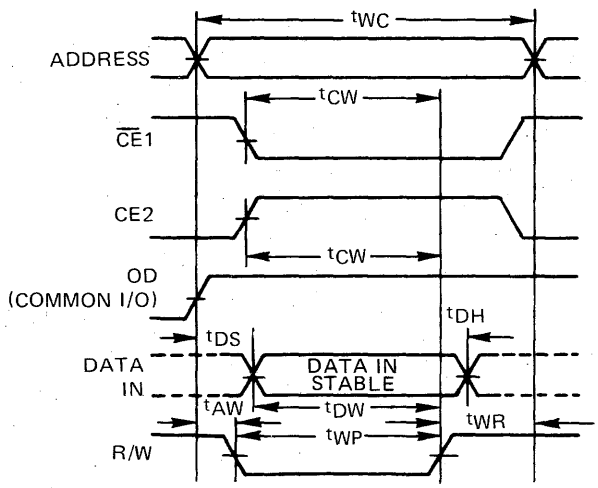
TIMING WAVEFORMS

READ CYCLE



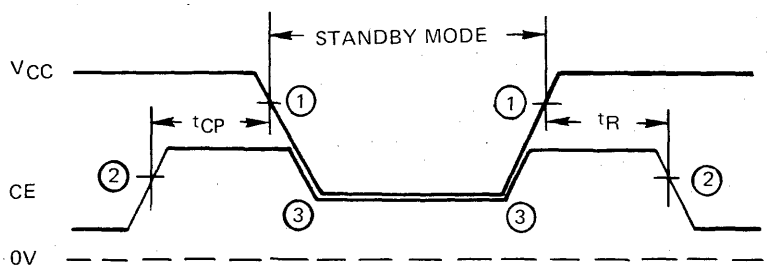
Notes: (1) OD should be tied low for separate I/O operation.
(2) R/W is high for read operation.

WRITE CYCLE



Note: OD is a logical 1 for common I/O and "don't care" for separate I/O operation.

STANDBY WAVEFORMS



Notes: (1) 4.75V
(2) 2.0V
(3) 1.5V

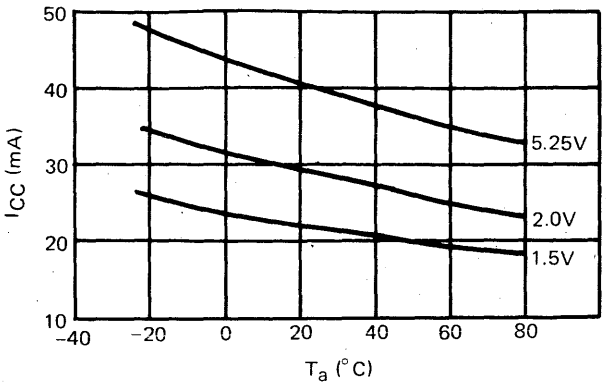
AC CONDITIONS OF TEST

Input Pulse Levels	+0.8V to +2.0V
Input Pulse Rise and Fall Times	20 ns
Timing Measurement Reference Level	1.5V
Output Load	1 TTL + 100 pF

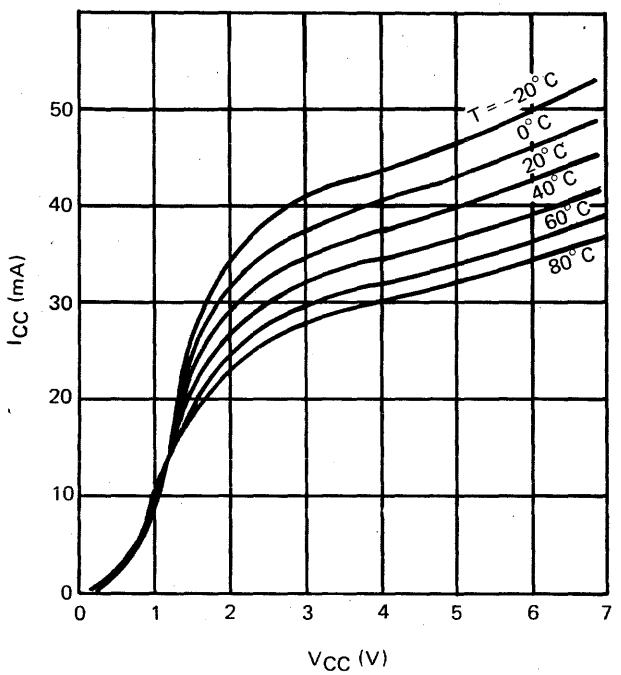
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TYPICAL OPERATING CHARACTERISTICS

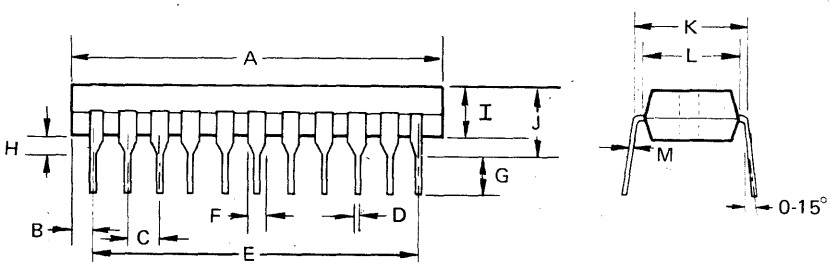
I_{CC} VS T_a



I_{CC} VS V_{CC}



PACKAGE OUTLINE μPD2101AL



ITEM	MILLIMETERS	INCHES
A	28.0 MAX.	1.10 MAX.
B	1.4 MAX.	0.025
C	2.54	0.10
D	0.50	0.02
E	25.4	1.00
F	1.40	0.055
G	2.54 MIN.	0.10 MIN.
H	0.5 MIN.	0.02 MIN.
I	4.7 MAX.	0.18 MAX.
J	5.2 MAX.	0.20 MAX.
K	10.16	0.40
L	8.5	0.33
M	$0.25^{+0.10}_{0.05}$	$0.01^{+0.004}_{0.002}$

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1024 BIT FULLY DECODED STATIC MOS RANDOM ACCESS MEMORY

DESCRIPTION

The μPD2102AL is a 1024 words by one bit static Random Access Memory requiring no clocks or refreshing. A family of devices with maximum access times ranging from 250 ns to 450 ns meet the requirements of microcomputer memory applications where speed, low cost and easy interfacing are prime design objectives.

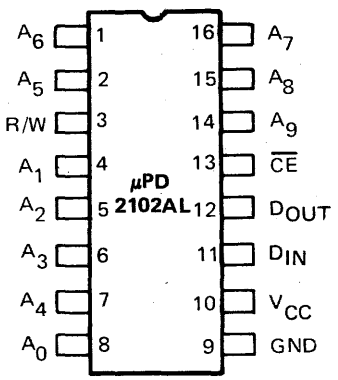
All μPD2102AL inputs and outputs are TTL compatible. A single chip-enable ($\overline{CE}$) pin is provided for selection of an individual device in systems with OR-tied outputs. Output data is the same polarity as input data and is nondestructively read out. Only a single +5 volt supply is required. In standby mode, with the supply lowered to 1.5 volts, power dissipation is reduced to 42 mW max.

The μPD2102AL family is fabricated using NEC's N-channel MOS silicon gate process, providing excellent contamination protection. This process permits the use of a low cost plastic package (16 pin) and enables high performance, highly reliable MOS circuits to be produced.

FEATURES

- Access Time – μPD2102AL-2 – 250 ns Max
  μPD2102AL – 350 ns Max
  μPD2102AL-4 – 450 ns Max
- Single +5 Volts Supply Voltage
- Directly TTL Compatible – All Inputs and Output
- Static MOS – No Clocks or Refreshing Required
- Low Power – Typically 150 mW
- Low Standby Power – 42 mW max
- Three-State Output – OR-TIE Capability
- Simple Memory Expansion – Chip Enable Input
- Fully Decoded – On Chip Address Decode
- Inputs Protected – All Inputs have Protection against Static Charge
- Low Cost Packaging – 16 Pin Plastic Dual-In-Line Configuration

PIN CONFIGURATION

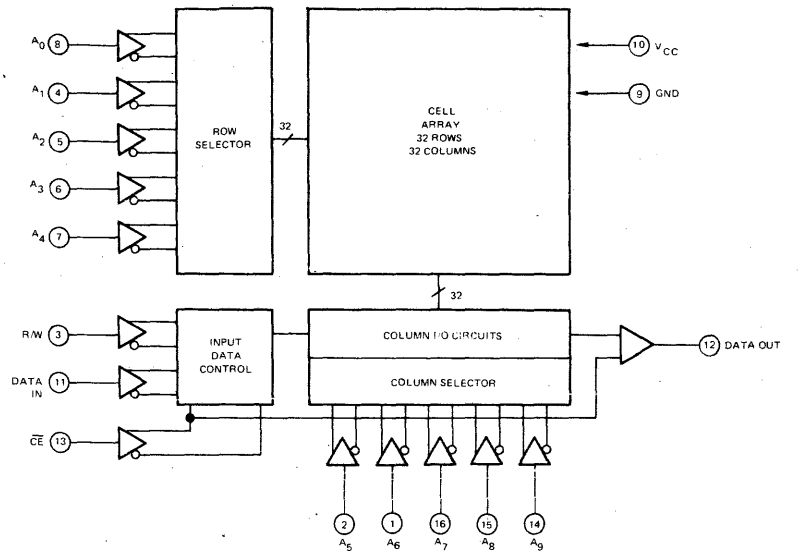


PIN NAMES

$A_0 - A_9$	Address Inputs
R/W	Read/Write
$\overline{CE}$	Chip Enable
V_{CC}	Power (+5V)

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BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature . . . . . -10°C to 70°C
Storage Temperature . . . . . -65°C to +125°C
Voltage On Any Pin . . . . . -0.5 to +7 Volts ①

Note: ① With Respect to Ground

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability

*T_a = 25°C

DC CHARACTERISTICS

T_a = −10°C to +70°C; V_{CC} = 5V ± 5% unless otherwise specified.

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP ①	LIMITS MAX	UNIT	TEST CONDITIONS
Input Leakage Current	I_{LI}			±10	μA	V_{IN} = 0 to 5.25V
I/O Leakage Current	I_{LOH}			+5	μA	$\overline{CE}$ = 2.0V, V_{OUT} = +2.4V to V_{CC}
I/O Leakage Current	I_{LOL}			−10	μA	$\overline{CE}$ = 2.0V, V_{OUT} = 0.4V
Power Supply Current	I_{CC1}		30	70	mA	All Inputs = 5.25V, Data Out Open
Input "Low" Voltage	V_{IL}	-0.5		+0.8	V	
Input "High" Voltage	V_{IH}	20		V_{CC}	V	
Output "Low" Voltage	V_{OL}			+0.4	V	I_{OL} = 2.1 mA
Output "High"	V_{OH}	2.4			V	I_{OH} = −100 μA

Note: ① Typical values are for T_a = 25°C and nominal supply voltage

CAPACITANCE

T_a = 25°C; f = 1 MHz

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input Capacitance	C_{IN}		3	5	pf	V_{IN} = 0V
Output Capacitance	C_{OUT}		7	10	pf	V_{OUT} = 0V

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AC CHARACTERISTICS

READ CYCLE

$T_a = -10°C$ to $+70°C$; $V_{CC} = +5V$ ±5% unless otherwise noted

PARAMETER	SYMBOL	LIMITS						UNIT	TEST CONDITIONS
		2102AL-4		2102AL		2102AL-2			
		MIN	MAX	MIN	MAX	MIN	MAX		
Read Cycle	t_{RC}	450		350		250		ns	$t_T = t_r = t_f = 100$ ns $C_L = 100$ pF Load = 1 TTL Gate $V_{ref} = 2.0$ or 0.8V
Access Time	t_A		450		350		250	ns	
Chip Enable to Output Time	t_{CO}		230		180		130	ns	
Previous Read Data Valid in Respect to Address	t_{OH1}	40		40		40		ns	
Previous Read Data Valid in Respect to Chip Enable	t_{OH2}	0		0		0		ns	

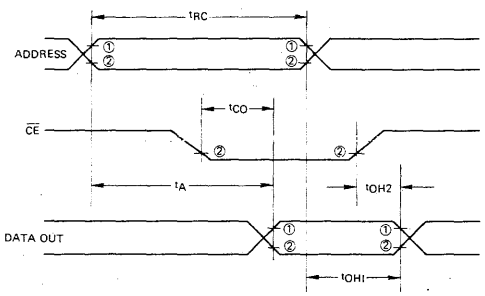
WRITE CYCLE

$T_a = -10°C$ to $+70°C$; $V_{CC} = +5V$ ± 5% unless otherwise noted

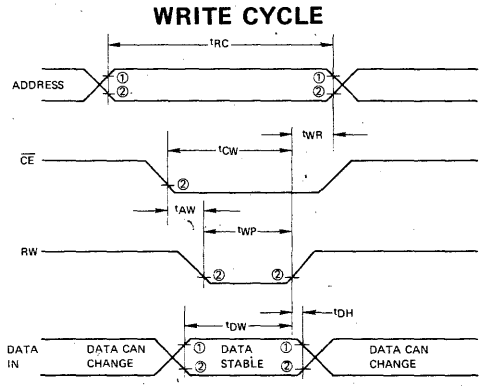
PARAMETER	SYMBOL	LIMITS						UNIT	TEST CONDITIONS
		2102AL-4		2102AL		2102AL-2			
		MIN	MAX	MIN	MAX	MIN	MAX		
Write Cycle	t_{WC}	450		350		250		ns	$t_T = t_r = t_f = 100$ ns $C_L = 100$ pF Load = 1 TTL Gate $V_{ref} = 2.0$ or 0.8V
Address to Write Setup Time	t_{AW}	20		20		20		ns	
Write Pulse Width	t_{WP}	300		250		180		ns	
Write Recovery Time	t_{WR}	0		0		0		ns	
Data Setup Time	t_{DW}	300		250		180		ns	
Data Hold Time	t_{DH}	0		0		0		ns	
Chip Enable to Write Setup Time	t_{CW}	300		250		180		ns	

TIMING WAVEFORMS

READ CYCLE



WRITE CYCLE



Notes: ① 2.0 Volts
② 0.8 Volts

STANDBY CHARACTERISTICS

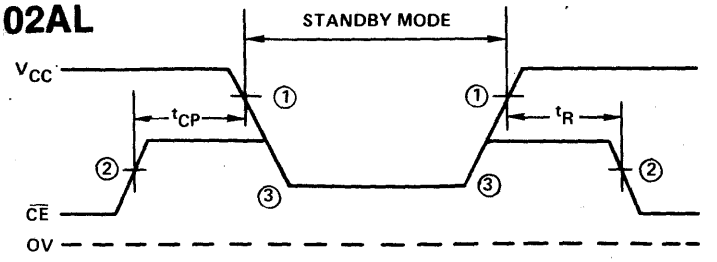
$T_a = 0$ to $+70°C$

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN	TYP	MAX		
V_{CC} in Standby	V_{PD}	1.5			V	
$\overline{CE}$ Bias in Standby	V_{CES}	2.0			V	$+2.0V \leq V_{PD} \leq +5.25V$
		V_{PD}			V	$+1.5V \leq V_{PD} < +2.0V$
Standby Current Drain	I_{PD1}		14	28	mA	All Inputs, $V_{PD1} = +1.5$
Standby Current Drain	I_{PD2}		18	38	mA	All Inputs, $V_{PD2} = +2.0V$
Chip Deselect to Standby Time	t_{CP}	0			ns	
Standby Recovery Time	t_R	t_{RC} ①			ns	

① t_{RC} = Read Cycle Time

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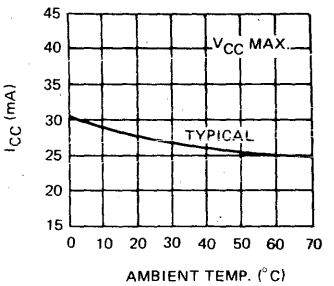
STANDBY MODE TIMING WAVEFORM



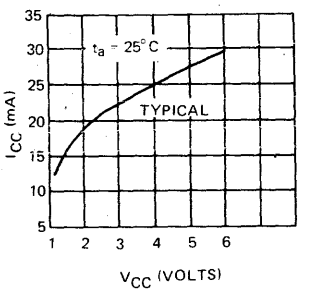
① 4.75V
② 2.0V
③ 1.5V

TYPICAL CHARACTERISTICS

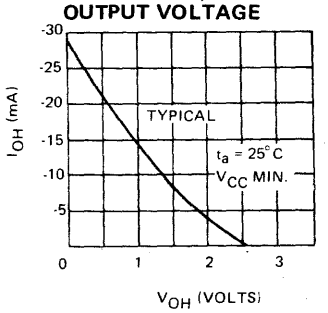
POWER SUPPLY CURRENT VS AMBIENT TEMPERATURE



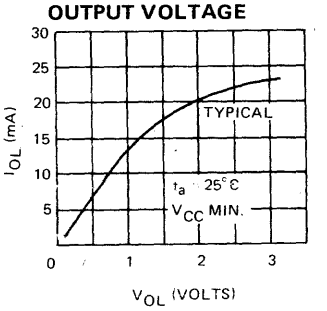
POWER SUPPLY CURRENT VS SUPPLY VOLTAGE



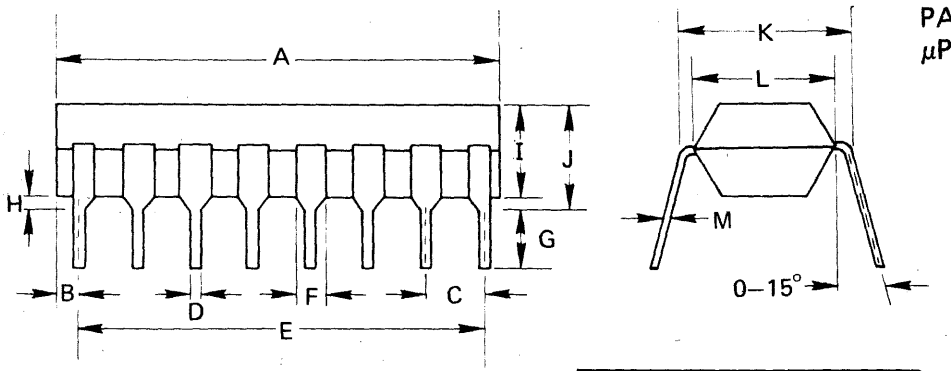
OUTPUT SOURCE CURRENT VS OUTPUT VOLTAGE



OUTPUT SINK CURRENT VS OUTPUT VOLTAGE



PACKAGE OUTLINE μPD2102ALC



ITEM	MILLIMETERS	INCHES
A	19.4 MAX.	0.76 MAX.
B	0.81	0.03
C	2.54	0.10
D	0.5	0.02
E	17.78	0.70
F	1.3	0.051
G	2.54 MIN.	0.10 MIN.
H	0.5 MIN.	0.02 MIN.
I	4.05 MAX.	0.16 MAX.
J	4.55 MAX.	0.18 MAX.
K	7.62	0.30
L	6.4	0.25
M	$0.25^{+0.10}_{-0.05}$	0.01

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NEC

μPD2111AL
μPD2111AL-2
μPD2111AL-4

1024 BIT (256 x 4) STATIC MOS RAM WITH COMMON I/O AND OUTPUT DISABLE

DESCRIPTION

The μPD2111AL is a 256 words by 4 bits static random access memory fabricated with N-channel MOS technology. It uses fully static circuitry and therefore requires no clocks or refreshing to operate. The data is read out nondestructively and has the same polarity as the input data. Common input/output pins are provided.

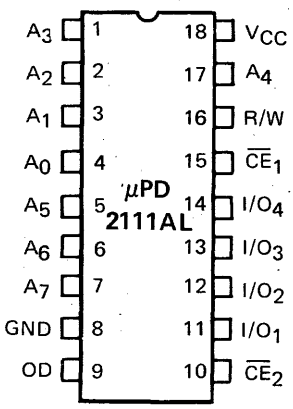
It is directly TTL compatible in all respects: inputs, outputs, and a single +5V supply. Separate chip enable ($\overline{CE}$) leads allow easy selection of an individual package when outputs are OR-tied.

All members in the μPD2111AL family feature a low standby power mode with the supply voltage being reduced to +1.5V.

FEATURES

- 256 Words x 4 Bits Organization
- Common Data Input and Output
- Single +5V Supply Voltage
- Directly TTL Compatible — All Inputs and Outputs
- Static MOS — No Clocks or Refreshing Required
- Access Time — 250 ns to 450 ns max.
- Simple Memory Expansion — Chip Enable Inputs
- Fully Decoded — On Chip Address Decode
- Inputs Protected — All Inputs have Protection Against Static Charge
- Low Cost Packaging — 18 Pin Plastic Dual-In-Line Configuration
- Three-State Output — OR-Tie Capability
- Low Standby Power

PIN CONFIGURATION



PIN NAMES

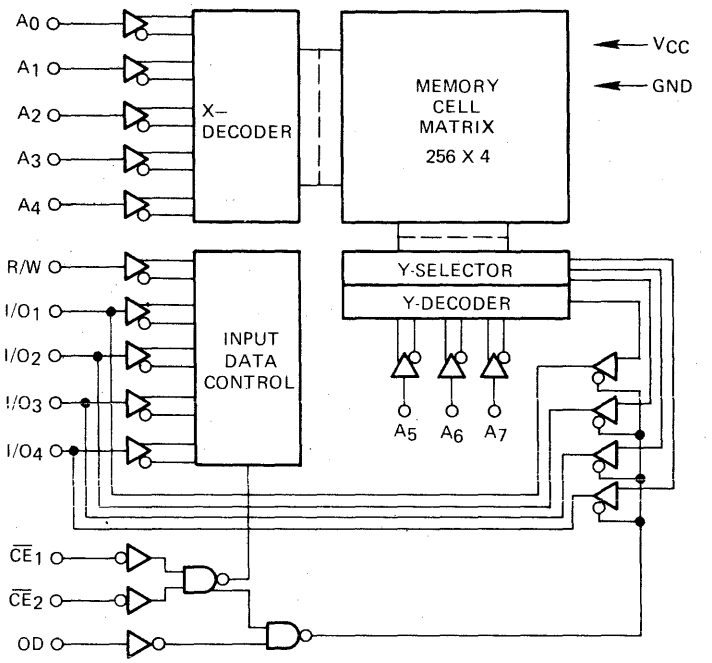
A_0 - A_7	Address Inputs
OD	Output Disable
R/W	Read/Write Input
$\overline{CE}_1$	Chip Enable 1
$\overline{CE}_2$	Chip Enable 2
I/O_1 - I/O_4	Data Input/Output

OPERATION MODES

CE_1	CE_2	OD	Chip Output Status	
0	1	0	Selected	Data Output
0	1	1		High Z
Others			Unselected	State

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BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	−10°C to +70°C
Storage Temperature	−65°C to +125°C
All Output Voltages	−0.5 to +7 Volts
All Input Voltages	−0.5 to +7 Volts
Supply Voltage V_{CC}	−0.5 to +7 Volts

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

DC CHARACTERISTICS

T_a = -10 to +70°C; V_{CC} = +5V ± 5%

PARAMETER		SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input High Voltage		V_{IH}	+2.0		V_{CC}	V	
Input Low Voltage		V_{IL}	−0.5		+0.8	V	
Output High Voltage	2111AL-4	V_{OH}	+2.4			V	I_{OH} = −150 μA
	2111AL 2111AL-2		+2.4			V	I_{OH} = −200 μA
Output Low Voltage		V_{OL}			+0.4	V	I_{OL} = +2.1 mA
Input Leakage Current High		I_{LIH}			+10	μA	$V_I = V_{CC}$
Input Leakage Current Low		I_{LIL}			−10	μA	V_I = 0V
Output Leakage Current High		I_{LOH}			+5	μA	V_O = +2.4V to V_{CC} $\overline{CE}$ = +2.0V
Output Leakage Current Low		I_{LOL}			−10	μA	V_O = +0.4V $\overline{CE}$ = +2.0V
Power Supply Current	2111AL-4	I_{CC1}			50	mA	V_I = +5.25V
	2111AL 2111AL-2				55	mA	I_O = 0 mA T_a = +25°C
Power Supply Current	2111AL-4	I_{CC2}			60	mA	V_I = +5.25V
	2111AL 2111AL-2				65	mA	I_O = 0 mA T_a = −10 to +70°C

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AC CHARACTERISTICS

READ CYCLE

$T_a = -10°C$ to $+70°C$, $V_{CC} = +5V \pm 5\%$

PARAMETER	SYMBOL	LIMITS									UNIT
		2111AL-4			2111AL			2111AL-2			
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Read Cycle Time	t_{RC}	450			350			250			ns
Access Time	t_A			450			350			250	ns
Chip Enable to Output	t_{CO}			310			240			180	ns
Output Disable to Output	t_{OD}			250			180			130	ns
Data Output to High Z State	t_{DF} ①	0		200	0		150	0		130	ns
Previous Read Data Valid After Change of Address	t_{OH}	40			40			40			ns

Note: ① t_{DF} is with respect to the trailing edge of $\overline{CE}_1$, $\overline{CE}_2$, or OD, whichever occurs first.

WRITE CYCLE

$T_a = -10°C$ to $+70°C$, $V_{CC} = +5V \pm 5\%$

PARAMETER	SYMBOL	LIMITS									UNIT
		2111AL-4			2111AL			2111AL-2			
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Write Cycle Time	t_{WC}	270			220			170			ns
Write Delay	t_{AW}	20			20			20			ns
Chip Enable to Write	t_{CW}	250			200			150			ns
Data Setup Time	t_{DW}	250			200			150			ns
Data Hold Time	t_{DH}	0			0			0			ns
Write Pulse Width	t_{WP}	250			200			150			ns
Write Recovery	t_{WR}	0			0			0			ns
Output Disable Setup	t_{DS}	20			20			20			ns

Note: OD is a logical 1 for common I/O and "don't care" for separate I/O operation.

AC CONDITIONS OF TEST

Input Pulse Levels ..... +0.8V to +2.0V
Input Pulse Rise and Fall Times ..... 20 ns
Timing Measurement Reference Level 1.5V
Output Load ..... 1 TTL + 100 pF

STANDBY CHARACTERISTICS

$T_a = -10°C$ to $+70°C$

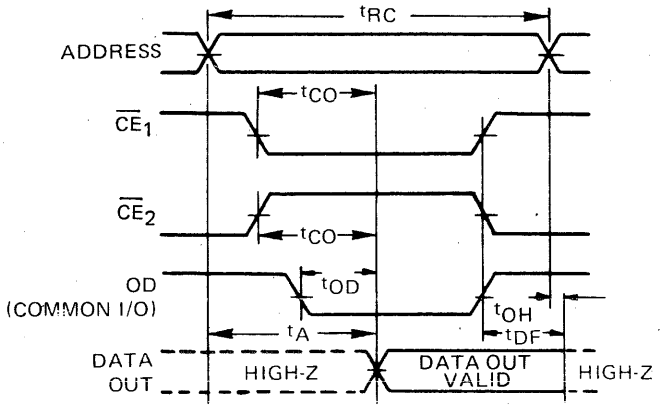
PARAMETER		SYMBOL	LIMITS			UNIT	TEST CONDITIONS
			MIN	TYP ①	MAX		
V_{CC} in Standby		V_{PD}	1.5			V	
$\overline{CE}_1$ Bias in Standby		V_{CES}	2.0			V	$2.0V \leq V_{PD} \leq 5.25V$
			V_{PD}			V	$1.5V \leq V_{PD} < 2.0V$
Standby Current Drain	2111AL-4	I_{PD_1}			36	mA	All Inputs = $V_{PD_1} = 1.5V$
	2111AL/AL-2				38		
Standby Current Drain	2111AL-4	I_{PD_2}			45	mA	All Inputs = $V_{PD_2} = 2.0V$
	2111AL/AL-2				48		
Chip Deselect to Standby Time		t_{CP}	0			ns	
Standby Recovery		t_R	t_{RC} ②			ns	

Notes: ① Typical values are for $T_a = 25°C$ and nominal supply voltage
② $t_R = t_{RC}$ (Read Cycle Time)

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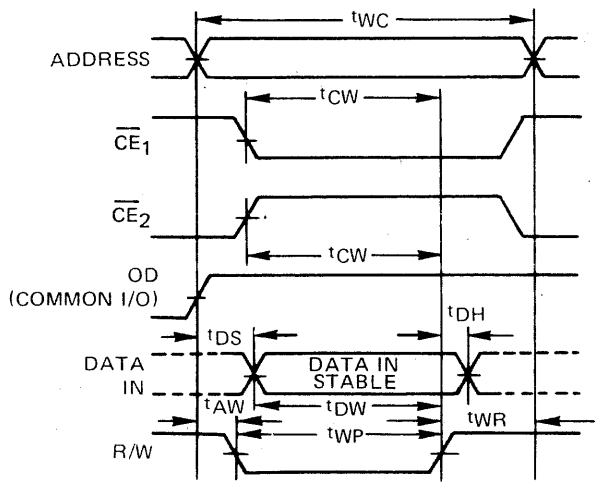
TIMING WAVEFORMS

READ CYCLE



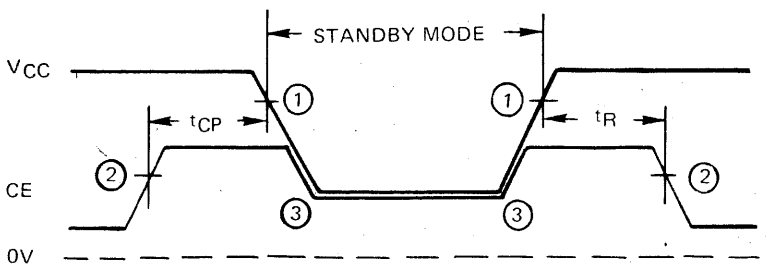
Notes: (1) OD should be tied low for separate I/O operation.
(2) R/W is high for read operation.

WRITE CYCLE



Note: OD is a logical 1 for common I/O and "don't care" for separate I/O operation.

STANDBY WAVEFORMS



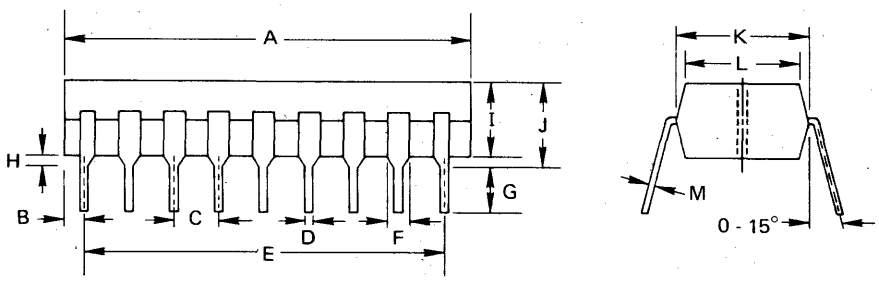
Notes: (1) 4.75V
(2) 2.0V
(3) 1.5V
(4) If the standby voltage (V_{PD}) is between 5.25V (V_{CC} Max) and 2.0V, then $\overline{CE}$ must be held at 2.0V Min (V_{IH}). If the standby voltage is less than 2.0V but greater than 1.5V (V_{PD} Min), then $\overline{CE}$ and standby voltage must be at least the same value or, if they are different, $\overline{CE}$ must be the more positive of the two. $\overline{CE}$ may be either of $\overline{CE_1}$ or $\overline{CE_2}$.

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CAPACITANCE $T_a = 25°C$; f = 1 MHz

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN	TYP	MAX		
Input Capacitance	C_{IN}			8	pf	V_I = 0V
Output Capacitance	C_{OUT}			12	pf	V_O = 0V

PACKAGE OUTLINE μPD2111ALC



ITEM	MILLIMETERS	INCHES
A	22.5 MAX.	0.89
B	1.09	0.04
C	2.54	0.10
D	0.50 ± 0.10	0.02
E	20.32	0.80
F	1.2 MIN.	0.05
G	2.54 MIN.	0.10 MIN.
H	0.5 MIN.	0.02 MIN.
I	4.05 MAX.	0.16 MAX.
J	4.55 MAX.	0.18 MAX.
K	7.62	0.30
L	6.4	0.25
M	$0.25^{+0.10}_{-0.05}$	0.01

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NEC

μPD410
μPD410-1
μPD410-2
μPD410-3
μPD410-5

4096 BIT HIGH SPEED STATIC MOS RANDOM ACCESS MEMORY

DESCRIPTION

The μPD410 is a very high speed 4K bit static random access memory. It is organized as 4096 words by 1 bit per word and fabricated using N channel silicon gate MOS technology.

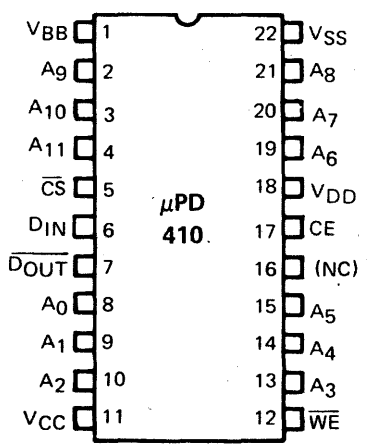
All signals to the device are TTL compatible except for Chip Enable which is standard +12 Volt MOS level.

Circuit operation starts with the rising edge of CE. Data is latched and valid until falling edge of CE. Address and Chip Select signals are latched on-chip to simplify system timing requirements.

FEATURES

- 4096 Words x 1 Bit Organization
- Fully Decoded
- TTL Compatible (except CE)
- High Speed-Access Time: 80 ns max.
- Cycle Time: 220 ns min.
- Static Operation — No Refresh Required
- Standby Power: 75 mW max.
- Active Power: 470 mW typ.
- Supply Voltages: V_{DD} = +12V, V_{CC} = +5V, V_{BB} = -5V
- Address Registers on the Chip
- Three State Output
- Standard 22 Pin Ceramic Dual-in-Line Package
- Pin Compatible with μPD411 and Other 4K Dynamic RAMs

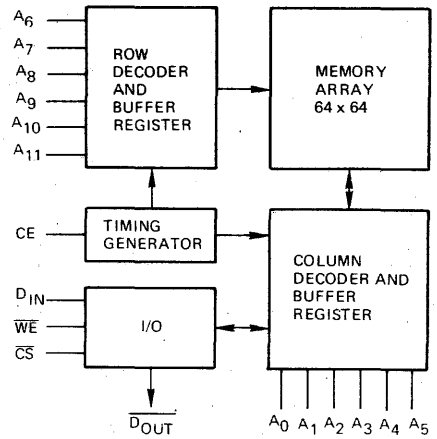
PIN CONFIGURATION



Rev/2

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BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	0°C to +70°C
Storage Temperature	-65°C to +150°C
All Output Voltages	-0.3 to +20 Volts①
All Input Voltages	-0.3 to +20 Volts①
Supply Voltage V_{DD}	-0.3 to +20 Volts①
Supply Voltage V_{CC}	-0.3 to +20 Volts①
Supply Voltage V_{SS}	-0.3 to +20 Volts①
Power Dissipation	1.0W

Note: ① Relative to V_{BB}

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

*T_a = 25°C
T_a = 0°C to 70°C; V_{DD} = 12V ± 5%; V_{CC} = 5V ± 5%; V_{BB} = -5V ± 5%; V_{SS} = 0V

PARAMETER	SYMBOL	LIMITS MIN	LIMITS MAX	UNIT	TEST CONDITIONS
Input Leakage Current	I_{LI}		10	μA	V_{IN} = V_{IL}MIN to V_{IH}MAX
CE Input Leakage Current	I_{LC}		10	μA	V_{IN} = V_{ILC}MIN to V_{IHC}MAX
Output Leakage Current	I_{LO}		10	μA	$\overline{CE}$ = V_{ILC} or $\overline{CS}$ = V_{IH} V_O = 0V to 5.25V
V_{DD} Supply Current during CE off	I_{DDOFF}		200	μA	CE = -1.0V to 0.6V
V_{DD} Supply Current during CE on	I_{DDON}		20	mA	CE = V_{IHC}
Average V_{DD} Current μPD410	I_{DDAV}		24	mA	Minimum Cycle Time
Average V_{DD} Current μPD410-1	I_{DDAV}		32	mA	Minimum Cycle Time
Average V_{DD} Current μPD410-2	I_{DDAV}		45	mA	Minimum Cycle Time
Average V_{DD} Current μPD410-3	I_{DDAV}		45	mA	Minimum Cycle Time
Average V_{DD} Current μPD410-5	I_{DDAV}		45	mA	Minimum Cycle Time
V_{BB} Supply Current	I_{BB}		100	μA	
V_{CC} Supply Current during CE off	I_{CCOFF}		15	mA	$\overline{CE}$ = V_{ILC} or $\overline{CS}$ = V_{IH}
Average V_{CC} Current	I_{CCAV}		21	mA	D_{OUT} = No load
Input Low Voltage	V_{IL}	-1.0	0.6	V	
Input High Voltage	V_{IH}	2.4	V_{CC}+1	V	
CE Input Low Voltage	V_{ILC}	-1.0	0.6	V	
CE Input High Voltage	V_{IHC}	V_{DD}-1	V_{DD}+1	V	
Output Low Voltage	V_{OL}	0	0.4	V	I_{OL} = 3.2 mA
Output High Voltage	V_{OH}	2.4	V_{CC}	V	I_{OH} = 2.0 mA

CAPACITANCE

T_a = 0°C to 70°C; V_{DD} = 12V ± 5%; V_{CC} = 5V ± 5%; V_{BB} = -5V ± 5%; V_{SS} = 0V

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Address Capacitance	C_{AD}		4	6	pF	V_{IN} = V_{SS}
$\overline{CS}$ Capacitance	C_{CS}		4	6	pF	V_{IN} = V_{SS}
D_{IN} Capacitance	C_{IN}		8	10	pF	V_{IN} = V_{SS}
$\overline{D_{OUT}}$ Capacitance	C_{OUT}		5	7	pF	V_{OUT} = V_{SS}
$\overline{WE}$ Capacitance	C_{WE}		8	10	pf	V_{IN} = V_{SS}
CE Capacitance	C_{CE}		18	27	pf	V_{IN} = V_{SS}

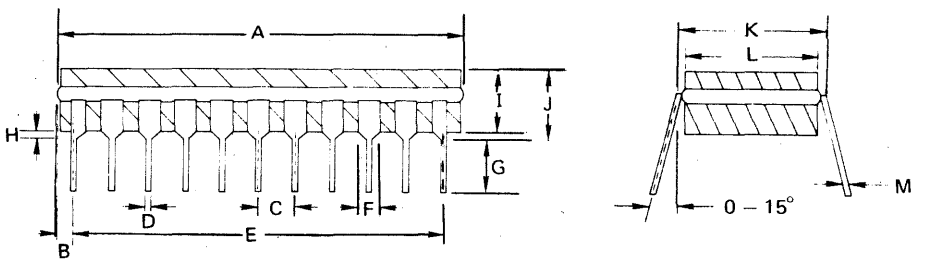
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AC CHARACTERISTICS

T_a = 0°C to 70°C; V_{DD} = 12V ± 5%; V_{CC} = 5V ± 5%; V_{BB} = −5V ± 5%; V_{SS} = 0V

PARAMETER	SYMBOL	LIMITS 410 MIN	410 MAX	410-1 MIN	410-1 MAX	410-2 MIN	410-2 MAX	410-3 MIN	410-3 MAX	410-5 MIN	410-5 MAX	UNIT	TEST CONDITIONS
READ, WRITE AND READ-MODIFY-WRITE													
Address to CE Set Up Time	t_{AC}	0		0		0		0		0		ns	
Address Hold Time	t_{AH}	90		70		50		50		50		ns	
CE Off Time	t_{CC}	190		140		90		90		90		ns	
CE Transition Time	t_T	0	40	0	40	0	40	0	40	0	40	ns	
CE off to Output High Impedance State	t_{CF}	0	90	0	90	0	90	0	90	0	90	ns	
READ													
Cycle Time	t_{CY}	440		330		220		220		220		ns	t_T = 10 ns
CE on Time	t_{CE}	230	2000	170	2000	110	2000	110	2000	110	2000	ns	
CE Output Delay	t_{CO}		190		140		90		80		70	ns	Load = 50 pF + 1TTL, Ref = 2.0 or 0.8V
Access Time	t_{ACC}		200		150		100		90		80	ns	$t_{ACC} = t_{AC} + t_{CO} + t_T$
CE to $\overline{WE}$	t_{WL}	20		20		20		20		20		ns	
$\overline{WE}$ to CE on	t_{WC}	0		0		0		0		0		ns	
WRITE													
Cycle Time	t_{CY}	440		330		220		220		220		ns	t_T = 10 ns
CE on Time	t_{CE}	230	2000	170	2000	110	2000	110	2000	110	2000	ns	
$\overline{WE}$ to CE off	t_W	130		100		70		70		70		ns	
CE to $\overline{WE}$	t_{CW}	130		100		70		70		70		ns	
D_{IN} to $\overline{WE}$ Set Up	t_{DW}	0		0		0		0		0		ns	
D_{IN} Hold Time	t_{DH}	60		40		20		20		20		ns	
$\overline{WE}$ Pulse Width	t_{WP}	130		100		70		70		70		ns	
READ-MODIFY-WRITE													
Read-Modify-Write (RMW) Cycle Time	t_{RWC}	560		420		280		280		280		ns	t_T = 10 ns
CE Width During RMW	t_{CRW}	350	2000	260	2000	170	2000	170	2000	170	2000	ns	
$\overline{WE}$ to CE on	t_{WC}	0		0		0		0		0		ns	
$\overline{WE}$ to CE off	t_W	130		100		70		70		70		ns	
$\overline{WE}$ Pulse Width	t_{WP}	130		100		70		70		70		ns	
D_{IN} to $\overline{WE}$ Set Up	t_{DW}	0		0		0		0		0		ns	
D_{IN} Hold Time	t_{DH}	60		40		20		20		20		ns	
CE to Output Delay	t_{CO}		190		140		90		80		70	ns	Load = 50 pF + 1TTL, Ref = 2.0 or 0.8V
Access Time	t_{ACC}		200		150		100		90		80		$t_{ACC} = t_{AC} + t_{CO} + t_T$

PACKAGE OUTLINE μPD410D

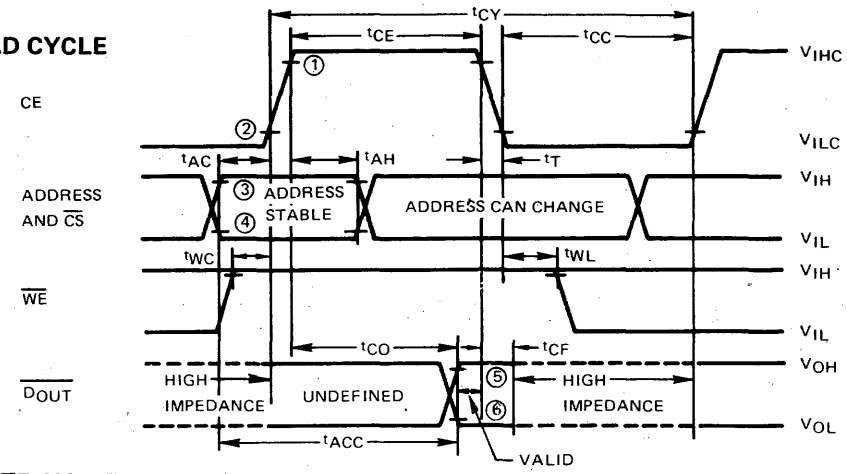


ITEM	MILLIMETERS	INCHES
A	27.43 Max.	1.079 Max.
B	1.27 Max.	0.05 Max.
C	2.54 ± 0.1	0.10
D	0.42 ± 0.1	0.016
E	25.4 ± 0.3	1.0
F	1.5 ± 0.2	0.059
G	3.5 ± 0.3	0.138
H	3.7 ± 0.3	0.145
I	4.2 Max.	0.165 Max.
J	5.08 Max.	0.200 Max.
K	10.16 ± 0.15	0.400
L	9.1 ± 0.2	0.358
M	0.25 ± 0.05	0.009

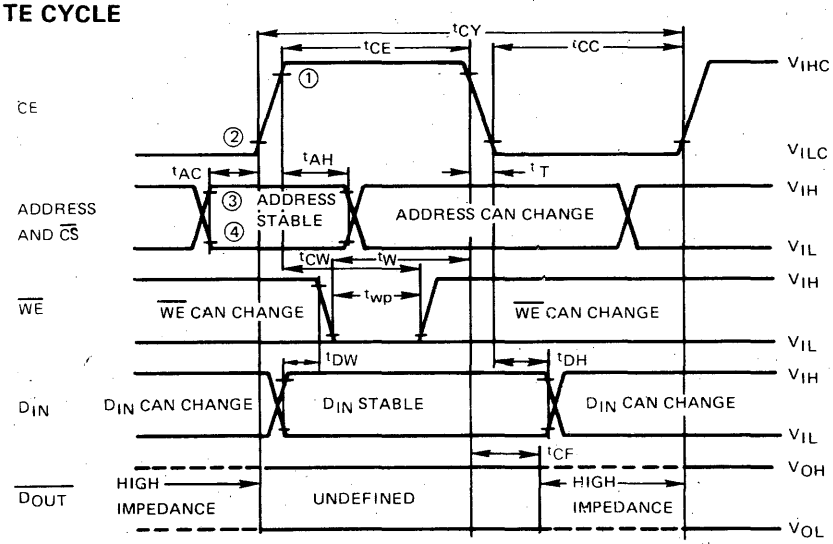
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TIMING WAVEFORMS

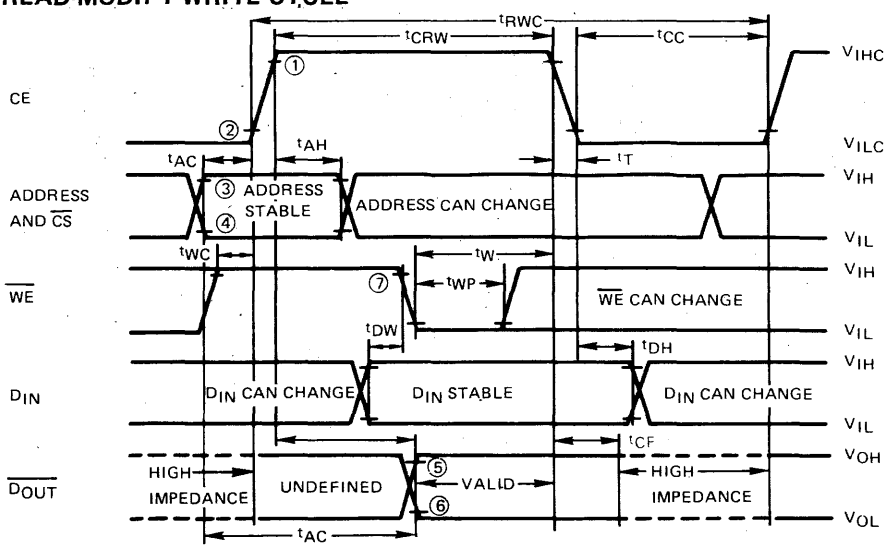
READ CYCLE



WRITE CYCLE



READ-MODIFY-WRITE CYCLE



Notes:
① V_{DD} − 2V is the reference level for measuring timing of CE.
② V_{SS} + 2V is the reference level for measuring timing of CE.
③ V_{IHMIN} is the reference level for measuring timing of the addresses, $\overline{CS}$, $\overline{WE}$ and D_{IN}.
④ V_{ILMAX} is the reference level for measuring timing of the addresses, $\overline{CS}$, $\overline{WE}$ and D_{IN}.
⑤ V_{SS} + 2.0V is the reference level for measuring timing of $\overline{D_{OUT}}$.
⑥ V_{SS} + 0.8V is the reference level for measuring timing of $\overline{D_{OUT}}$.
⑦ $\overline{WE}$ must be at V_{IH} until end of t_{CO}.

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NEC
μPD2114L
μPD2114L-1
μPD2114L-2

4096 BIT (1024 × 4 BITS) STATIC RAM

DESCRIPTION

The NEC μPD2114L is a 4096 bit static Random Access Memory organized as 1024 words by 4 bits using N-channel Silicon-gate MOS technology. It uses fully DC stable (static) circuitry throughout, in both the array and the decoding, and therefore requires no clocks or refreshing to operate and simplify system design. The data is read out nondestructively and has the same polarity as the input data. Common input/output pins are provided.

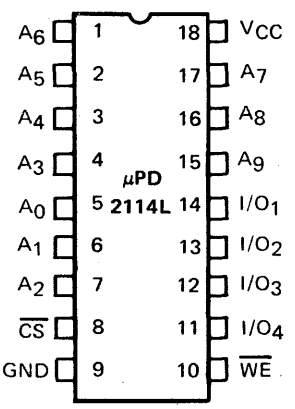
The μPD2114L is designed for memory applications where high performance, low cost, large bit storage, and simple interfacing are important design objectives. The μPD2114L is placed in an 18-pin package for the highest possible density.

It is directly TTL compatible in all respects: inputs, outputs, and a single +5V supply. A separate Chip Select ($\overline{CS}$) lead allows easy selection of an individual package when outputs are OR-Tied.

FEATURES

- Access Time: Selection from 250-450 ns
- Single +5 Volt Supply
- Directly TTL Compatible — All Inputs and Outputs
- Completely Static — No Clock or Timing Strobe Required
- Low Operating Power — Typically 0.06 mW/Bit
- Identical Cycle and Access Times
- Common Data Input and Output using Three-State Output
- High Density 18-pin Plastic and Ceramic Packages
- Replacement for 2114L and Equivalent Devices

PIN CONFIGURATION

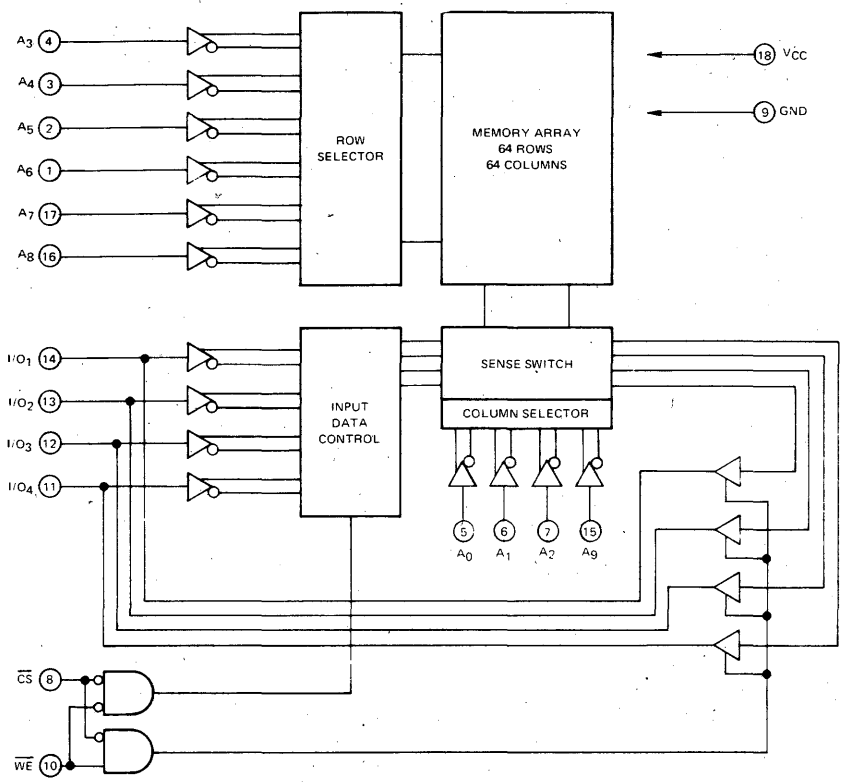


PIN NAMES

A_0-A_9	Address Inputs
$\overline{WE}$	Write Enable
$\overline{CS}$	Chip Select
I/O_1-I/O_4	Data Input/Output
V_{CC}	Power (+5V)
GND	Ground

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BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	-10°C to +80°C
Storage Temperature	-65°C to +150°C
Voltage on any Pin	-0.5 to +7 Volts ①
Power Dissipation	1 Watt

Note: ① With respect to ground.

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

CAPACITANCE

T_a = 25°C; f = 1.0 MHz

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input/Output Capacitance	$C_{I/O}$			12	pf	$V_{I/O}$ = 0V
Input Capacitance	C_{IN}			5	pf	V_{IN} = 0V

DC CHARACTERISTICS

T_a = 0°C to 70°C; V_{CC} = +5V ± 10% unless otherwise noted.

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input Load Current (All Input Pins)	I_{LI}			10	μA	V_{IN} = 0 to 5.5V
I/O Leakage Current	I_{LO}			10	μA	$\overline{CS}$ = 2V, $V_{I/O}$ = 0.4V to V_{CC}
Power Supply Current	I_{CC1}			65	mA	V_{IN} = 5.5V, $I_{I/O}$ = 0 mA, T_a = 25°C
Power Supply Current	I_{CC2}			70	mA	V_{IN} = 5.5V, $I_{I/O}$ = 0 mA, T_a = 0°C
Input Low Voltage	V_{IL}	-0.5		0.8	V	
Input High Voltage	V_{IH}	2.0		6.0	V	
Output Low Current	I_{OL}	3.2			mA	V_{OL} = 0.4V
Output High Current	I_{OH}			-1.0	mA	V_{OH} = 2.4V, V_{CC} = 4.75V
						V_{OH} = 2.2V, V_{CC} = 4.5V

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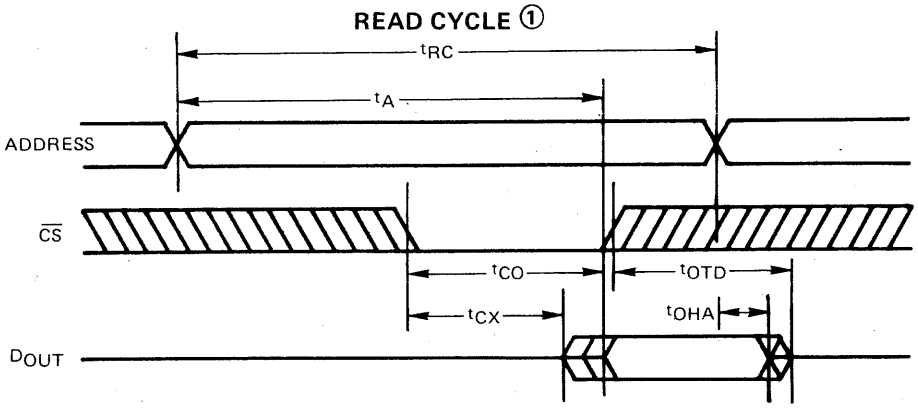
AC CHARACTERISTICS

T_a = 0°C to +70°C; V_{CC} = +5V ± 10%, unless otherwise noted.

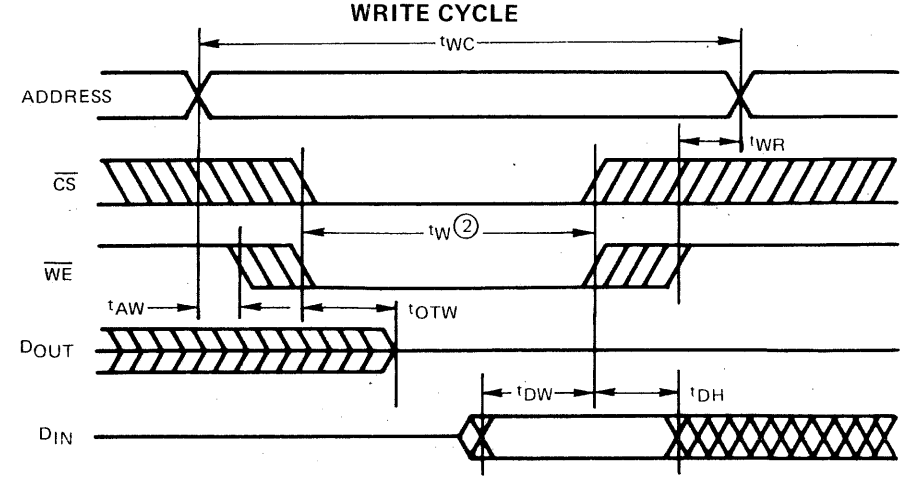
PARAMETER	SYMBOL	LIMITS 2114L MIN	LIMITS 2114L MAX	LIMITS 2114L MIN	LIMITS 2114L MAX	LIMITS 2114L MIN	LIMITS 2114L MAX	UNIT	TEST CONDITIONS
READ CYCLE									
Read Cycle Time	t_{RC}	250		300		450		ns	$t_T = t_r = t_f = 10$ ns
Access Time	t_A		250		300		450	ns	C_L = 100 pF
Chip Selection to Output Valid	t_{CO}		80		100		120	ns	Load = 1 TTL gate
Chip Selection to Output Active	t_{CX}	20		20		20		ns	Input Levels = 0.8 and 2.0V
Output 3-State from Deselection	t_{OTD}		70		80		100	ns	V_{ref} = 1.5V
Output Hold from Address Change	t_{OHA}	50		50		50		ns	
WRITE CYCLE									
Write Cycle Time	t_{WC}	250		300		450		ns	$t_T = t_r = t_f = 10$ ns
Write Time	t_W	120		150		200		ns	C_L = 100 pF
Write Release Time	t_{WR}	0		0		0		ns	Load = 1 TTL gate
Output 3-State from Write	t_{OTW}		70		80		100	ns	Input Levels = 0.8 and 2.0V
Data to Write Time Overlap	t_{DW}	120		150		200		ns	V_{ref} = 1.5V
Data Hold from Write Time	t_{DH}	0		0		0		ns	
Address to Write Setup Time	t_{AW}	0		0		0		ns	

TIMING WAVEFORMS

READ CYCLE ①



WRITE CYCLE



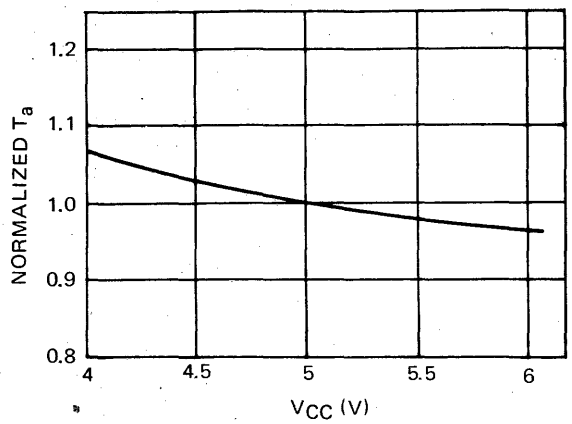
Notes: ① $\overline{WE}$ is high for Read Cycle

② t_W is measured from the latter of $\overline{CS}$ or $\overline{WE}$ going low to the earlier of $\overline{CS}$ or $\overline{WE}$ going high.

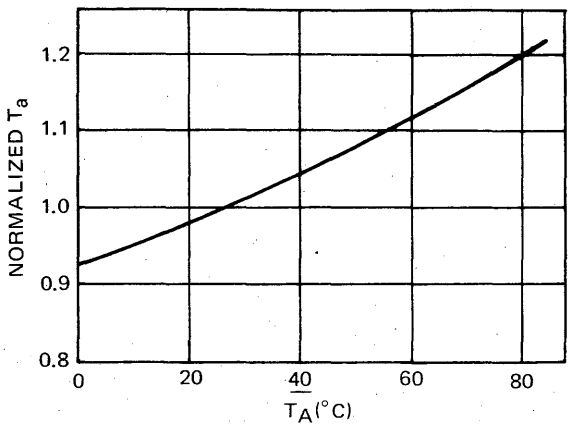
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TYPICAL OPERATING CHARACTERISTICS

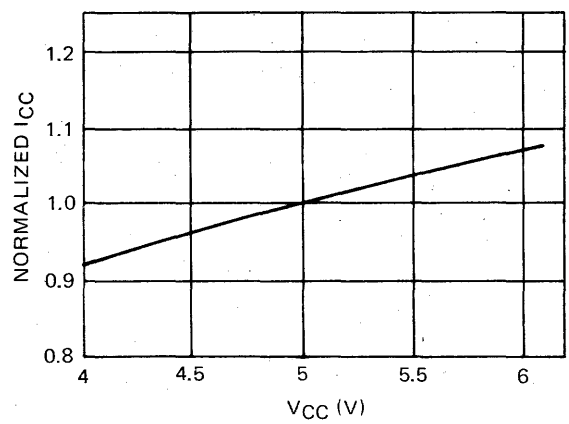
NORMALIZED ACCESS TIME VS. SUPPLY VOLTAGE



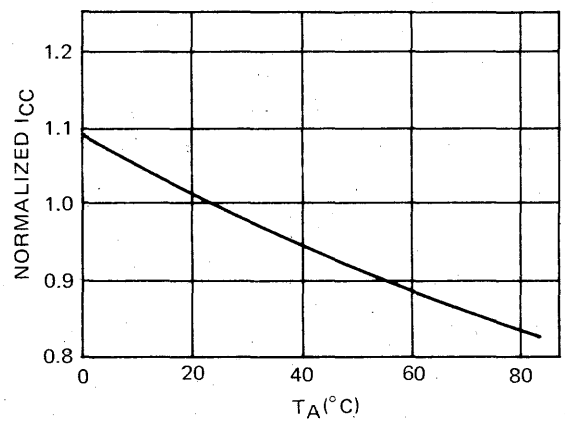
NORMALIZED ACCESS TIME VS. AMBIENT TEMPERATURE



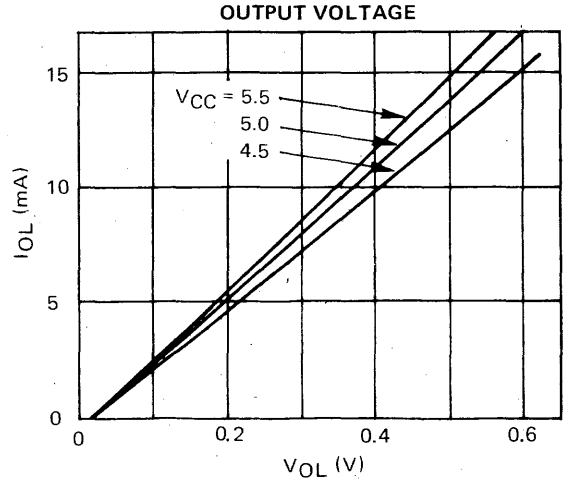
NORMALIZED POWER SUPPLY CURRENT VS. SUPPLY VOLTAGE



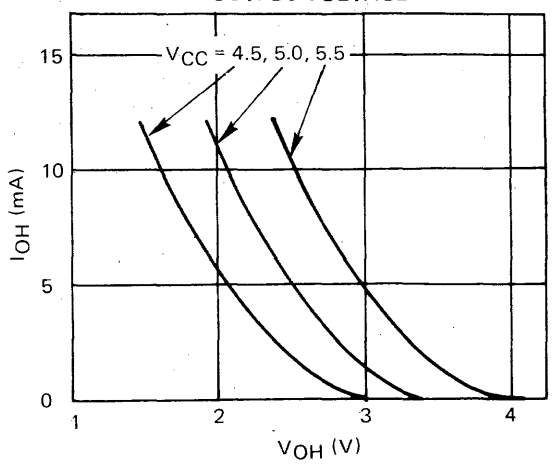
NORMALIZED POWER SUPPLY CURRENT VS. AMBIENT TEMPERATURE



OUTPUT SINK CURRENT VS. OUTPUT VOLTAGE

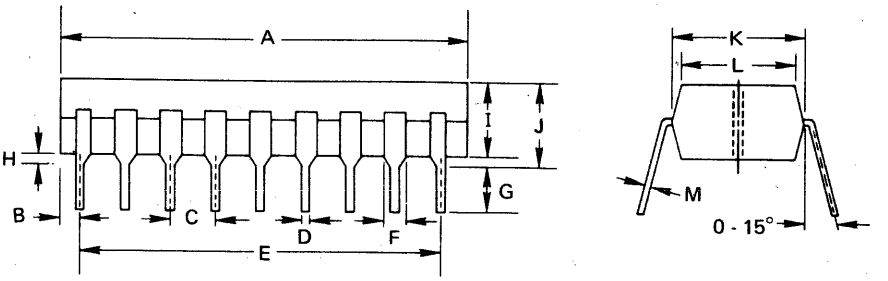


OUTPUT SOURCE CURRENT VS. OUTPUT VOLTAGE



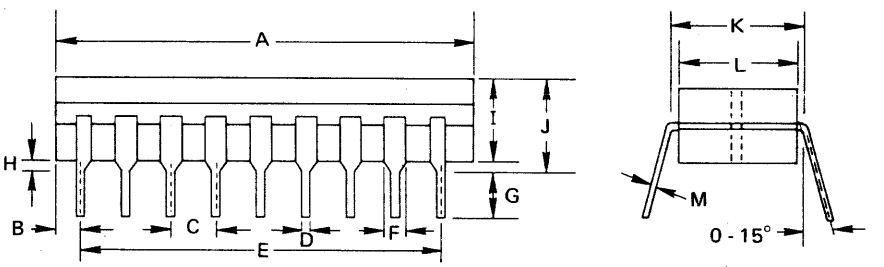
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PACKAGE OUTLINES
μPD2114LC/D



μPD2114LC (Plastic)

ITEM	MILLIMETERS	INCHES
A	23.2 MAX.	0.91 MAX.
B	1.44	0.055
C	2.54	0.1
D	0.45	0.02
E	20.32	0.8
F	1.2	0.06
G	2.5 MIN.	0.1 MIN.
H	0.5 MIN.	0.02 MIN.
I	4.6 MAX.	0.18 MAX.
J	5.1 MAX.	0.2 MAX.
K	7.62	0.3
L	6.7	0.26
M	0.25	0.01



μPD2114LD (Cerdip)

ITEM	MILLIMETERS	INCHES
A	23.2 MAX.	0.91 MAX.
B	1.44	0.055
C	2.54	0.1
D	0.45	0.02
E	20.32	0.8
F	1.2	0.06
G	2.5 MIN.	0.1 MIN.
H	0.5 MIN.	0.02 MIN.
I	4.6 MAX.	0.18 MAX.
J	5.1 MAX.	0.2 MAX.
K	7.62	0.3
L	6.7	0.26
M	0.25	0.01

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NEC
μPD2147
μPD2147-3
PRELIMINARY

4096 BIT HIGH SPEED STATIC RAM

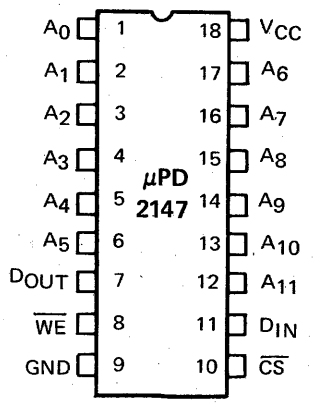
DESCRIPTION

The μPD2147 is a very high speed, fully static, NMOS RAM, organized as 4096 x 1. It is available in an 18 pin dual-in-line package.

FEATURES

- Extremely High Speed, −55 ns (μPD2147-3)
- Single +5V Supply
- Fully Static — No Clocking Required
- Automatic Power-Down
- Fully TTL Compatible

PIN CONFIGURATION



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NEC

μPD4104-30
μPD4104-32
μPD4104-33
μPD4104-35
μPD4104-36

PRELIMINARY

4096 x 1 STATIC NMOS RAM

DESCRIPTION

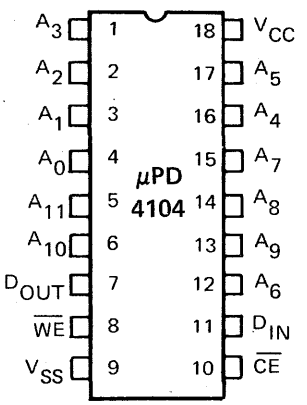
The μPD4104 is a high performance 4K static RAM. Organized as 4096 x 1, it uses a combination of static storage cells with dynamic input/output circuitry to achieve high speed and low power in the same device. Utilizing NMOS technology, the μPD4104 is fully TTL compatible and operates with a single +5V ± 10% supply.

FEATURES

- Fast Access Time – 85 ns (μPD4104-36)
- Very Low Stand-By Power – 25 mW Max.
- Low V_{CC} Data Retention Mode to +3 Volts
- Single +5V ± 10% Supply
- Fully TTL Compatible
- Available in 18 Pin Plastic and Ceramic Dual-in-Line Packages
- 5 Performance Ranges:

	ACCESS TIME	R/W CYCLE	SUPPLY CURRENT	
			ACTIVE	STANDBY
μPD4104-30	300 ns	460 ns	21 mA	5 mA
μPD4104-32	200 ns	310 ns	21 mA	5 mA
μPD4104-33	150 ns	260 ns	40 mA	5 mA
μPD4104-35	120 ns	230 ns	40 mA	5 mA
μPD4104-36	85 ns	180 ns	40 mA	5 mA

PIN CONFIGURATION

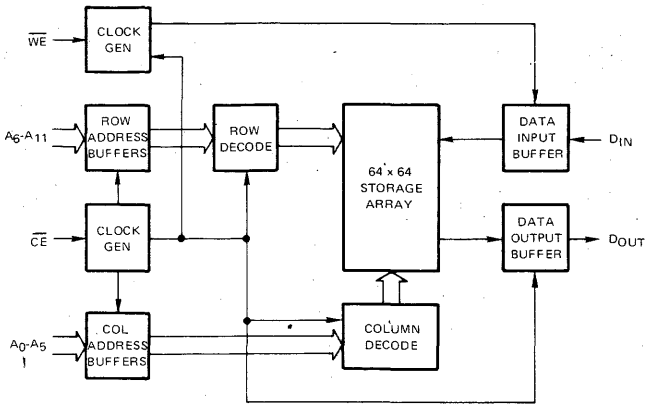


PIN NAMES

A_0-A_{11}	Address Inputs
$\overline{CE}$	Chip Enable
D_{IN}	Data Input
D_{OUT}	Data Output
V_{SS}	Ground
V_{CC}	Power (+5V)
$\overline{WE}$	Write Enable

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BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	0°C to +70°C
Storage Temperature (Plastic Package)	−55°C to +125°C
(Ceramic Package)	−65°C to +150°C
Voltage on Any Pin	−1 to +7 Volts ①
Power Dissipation	1 Watt
Short Circuit Output Current	50 mA

Note: ① Relative to V_{SS}

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

DC CHARACTERISTICS ① ⑥

T_a = 0°C to +70°C; V_{CC} = +5V ± 10%

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Supply Voltage	V_{CC}	4.5		5.5	V	All Voltages Referenced to V_{SS}
Supply Voltage	V_{SS}	0		0	V	
Logic "1" Voltage All Inputs	V_{IH}	2.2		7.0	V	
Logic "0" Voltage All Inputs	V_{IL}	−1.0		0.8	V	
Average V_{CC} Power 4104-30, 4104-32	I_{CC1}			21	mA	
Supply Current 4104-33, 4104-35, 4104-36	I_{CC1}			40	mA	②
Standby V_{CC} Power Supply Current	I_{CC2}			5	mA	③
Input Leakage Current (Any Input)	I_{IL}	−10		10	μA	④
Output Leakage Current	I_{OL}	−10		10	μA	③, ⑤
Output Logic "1" Voltage I_{OUT} = −500 μA	V_{OH}	2.4			V	
Output Logic "0" Voltage I_{OUT} = 5 mA	V_{OL}			0.4	V	

CAPACITANCE ①

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input Capacitance	C_{IN}		4	6	pF	⑦
Output Capacitance	C_{OUT}		6	7	pF	⑦

Notes: ① All voltages referenced to V_{SS}.

② I_{CC1} is related to precharge and cycle times. Guaranteed maximum values for I_{CC1} may be calculated by:

$$I_{CC1}\ [ma] = (5t_p + 13\ (t_C - t_p) + 3420) \div t_C$$

where t_p and t_C are expressed in nanoseconds. Equation is referenced to the −3 device, other devices derate to the same curve.

③ Output is disabled (open circuit), $\overline{CE}$ is at logic 1.

④ All device pins at 0 volts except pin under test at $0 \leq V_{IN} \leq 5.5$ volts.

⑤ $0V \leq V_{OUT} \leq +5.5V$.

⑥ During power up, $\overline{CE}$ and $\overline{WE}$ must be at V_{IH} for minimum of 2 ms after V_{CC} reaches 4.5V, before a valid memory cycle can be accomplished.

⑦ Effective capacitance calculated from the equation $C = I\frac{\Delta t}{\Delta V}$ with ΔV equal to 3V and V_{CC} nominal.

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AC CHARACTERISTICS ② ⑦

T_a = 0°C to +70°C; V_{CC} = +5V ± 10% ①

PARAMETER	SYMBOL	LIMITS 4104-30 MIN	4104-30 MAX	4104-32 MIN	4104-32 MAX	4104-33 MIN	4104-33 MAX	4104-35 MIN	4104-35 MAX	4104-36 MIN	4104-36 MAX	UNIT	TEST CONDITIONS
Read or Write Cycle Time	t_C	460		310		260		230		180		ns	⑧
Random Access	t_{AC}		300		200		150		120		85	ns	③
Chip Enable Pulse Width	t_{CE}	300	10,000	200	10,000	150	10,000	120	10,000	85	10,000	ns	
Chip Enable Precharge Time	t_P	150		100		100		100		85		ns	
Address Hold Time	t_{AH}	165		110		95		75		60		ns	
Address Set-Up Time	t_{AS}	0		0		0		0		0		ns	
Output Buffer Turn-Off Delay	t_{OFF}	0	75	0	50							ns	⑨
Read Command Set-Up Time	t_{RS}	0		0		0		0		0		ns	④
Write Enable Set-Up Time	t_{WS}	− 20		− 20		0		0		0		ns	④
Data Input Hold Time Referenced to $\overline{CE}$	t_{DHC}											ns	
Data Input Hold Time Referenced to $\overline{WE}$	t_{DIH}	25		25		20		20		20		ns	
Write Enabled Pulse Width	t_{WW}	90		60		55		50		45		ns	
Modify Time	t_{MOD}	0	10,000	0	10,000	0	10,000	0	10,000	0	10,000	ns	⑤
$\overline{WE}$ to $\overline{CE}$ Precharge Lead Time	t_{WPL}	105		70		65		60		55		ns	⑥
Data Input Set-Up Time	t_{DS}	0		0		0		0		0		ns	
Write Enable Hold Time	t_{WH}	225		150		115		90		65		ns	
Transition Time	t_T	5	50	5	50	5	50	5	50	5	50	ns	
Read-Modify-Write Cycle Time	t_{RMW}	565		380		325		290		235		ns	⑩

Notes: ① All voltages referenced to V_{SS}.

② During power up, $\overline{CE}$ and $\overline{WE}$ must be at V_{IH} for minimum of 2 ms after V_{CC} reaches 4.5V, before a valid memory cycle can be accomplished.

③ Measured with load circuit equivalent to 2 TTL loads and CL = 100 pF.

④ If $\overline{WE}$ follows $\overline{CE}$ by more than t_{WS} then data out may not remain open circuited.

⑤ Determined by user. Total cycle time cannot exceed t_{CE} max.

⑥ Data-in set-up time is referenced to the later of the two falling clock edges $\overline{CE}$ or $\overline{WE}$.

⑦ AC measurements assume t_T = 5 ns. Timing points are taken as V_{IL} = 0.8V and V_{IH} = 2.2V on the inputs and V_{OL} = 0.4V and V_{OH} = 2.4V on the output waveform.

⑧ $t_C = t_{CE} + t_P + 2\,t_T$.

⑨ The true level of the output in the open circuit condition will be determined totally by output load conditions. The output is guaranteed to be open circuit within t_{OFF}.

⑩ $t_{RMW} = t_{AC} + t_{WPL} + t_P + 3\,t_T + t_{MOD}$.

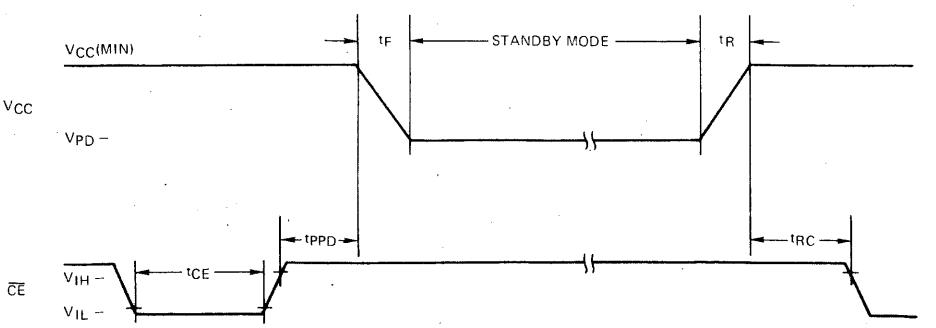
STANDBY CHARACTERISTICS

T_a = 0°C to +70°C

PARAMETER	SYMBOL	LIMITS 4104-E MIN	4104-E MAX	4104 MIN	4104 MAX	4104-1 MIN	4104-1 MAX	4104-2 MIN	4104-2 MAX	4104-3 MIN	4104-3 MAX	UNIT	TEST CONDITIONS
V_{CC} In Standby	V_{PD}	3.0		3.0								V	
Standby Current	I_{PD}		3.3		3.3							mA	
Power Supply Fall Time	T_F	100		100								μs	
Power Supply Rise Time	T_R	100		100								μs	
Chip Enable Pulse $\overline{CE}$ Width	T_{CE}	300		200								μs	
Chip Enable Precharge To Power Down Time	T_{PPD}	150		100								ns	
"1" Level $\overline{CE}$ Min Level	V_{IH}	2.2		2.2								V	
Standby Recovery Time	T_{RC}	500		500								μs	

TIMING WAVEFORMS

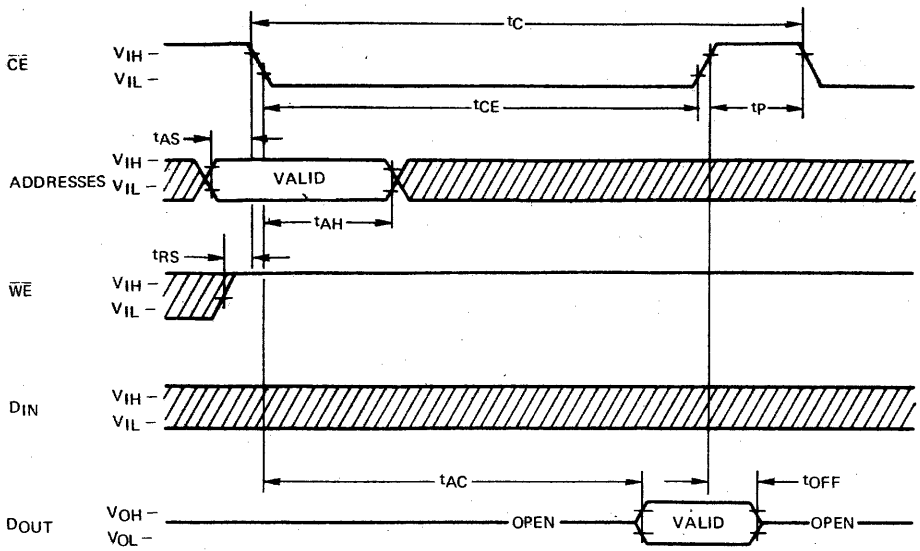
POWER DOWN



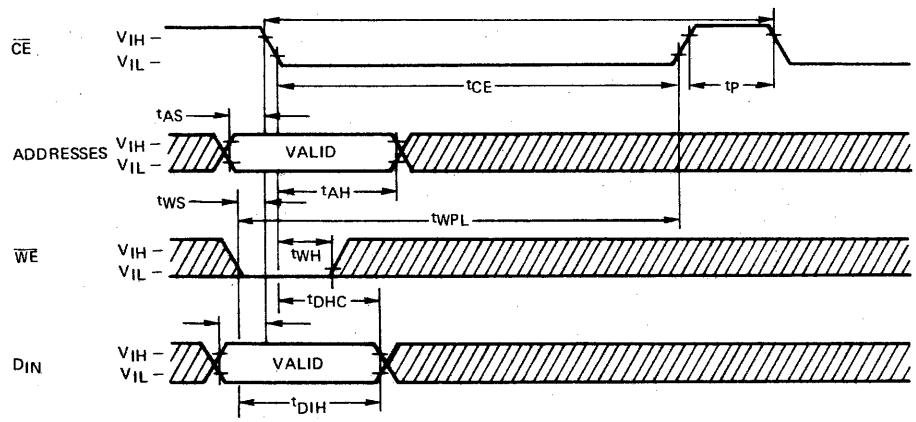
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TIMING WAVEFORMS (CONT.)

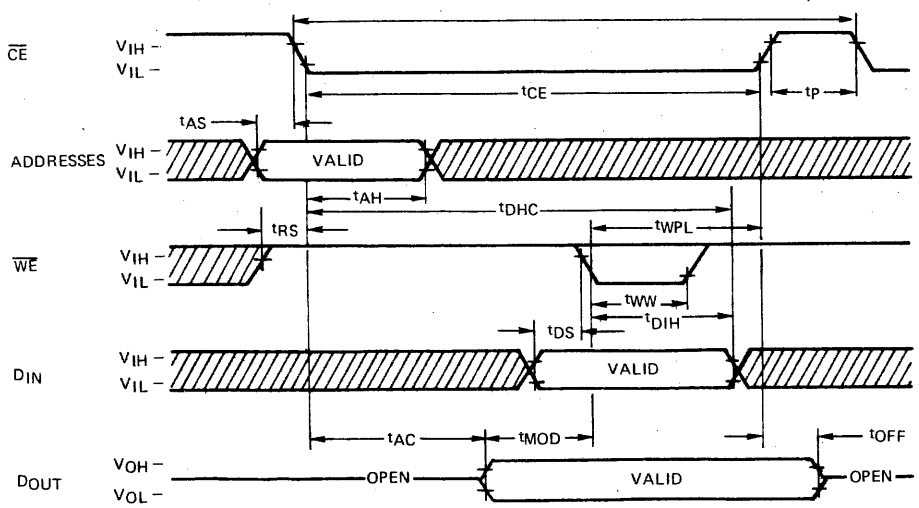
READ CYCLE



WRITE CYCLE



READ-MODIFY-WRITE CYCLE



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OPERATIONAL DESCRIPTION

READ CYCLE

The selection of one of the possible 4096 bits is made by virtue of the 12 address bits presented at the inputs. These are latched into the chip by the negative going edge of chip enable ($\overline{CE}$). If the write enable ($\overline{WE}$) input is held at a high level (V_{IH}) while the $\overline{CE}$ input is clocked to a low level (V_{IL}), a read operation will be performed. At the access time (t_{AC}), valid data will appear at the output. Since the output is unlatched by a positive transition of $\overline{CE}$, it will be in the high impedance state from the previous cycle until the access time. It will go to the high impedance state again at the end of the current cycle when $\overline{CE}$ goes high.

The address lines may be set up for the next cycle any time after the address hold time has been satisfied for the current cycle.

WRITE CYCLE

Data to be written into a selected cell is latched into the chip by the later negative transition of $\overline{CE}$ or WE. If $\overline{WE}$ is brought low before $\overline{CE}$, the cycle is an "Early Write" cycle, and data will be latched by $\overline{CE}$. If $\overline{CE}$ is brought low before $\overline{WE}$, as in a Read-Modify-Write cycle, then data will be latched by $\overline{WE}$. Two independent timing parameters must be satisfied for the data-in hold time; t_{DHI} and t_{DHC}. When the cycle is a R/W or R-M-W, t_{DHC} will be automatically satisfied. For a write cycle, both parameters must be paid attention to.

If the cycle is an "Early Write" cycle, the output will remain in the high impedance state. For a Read-Modify-Write cycle; the output will be active for the Modify and Write portions of the memory cycle until $\overline{CE}$ goes high. If $\overline{WE}$ is brought low after $\overline{CE}$ but before the access time, the state of the output will be undefined. The desired data will be written into the cell if data-in is valid on the leading edge of $\overline{WE}$, t_{DHI} and t_{DHC} are satisfied, and $\overline{WE}$ occurs prior to $\overline{CE}$ going high by at least the minimum lead time (t_{WPL}).

READ-MODIFY-WRITE

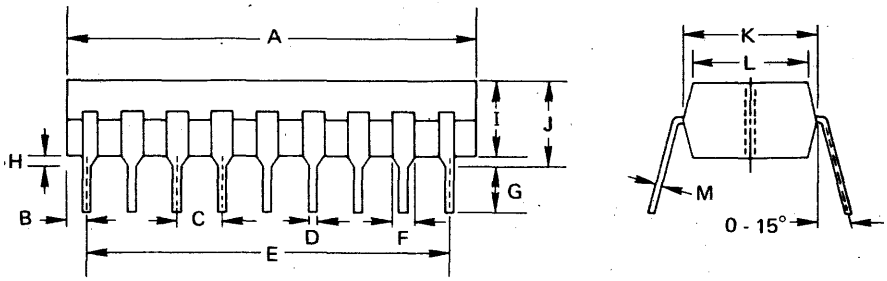
Read and Write cycles can be combined to allow reading of a selected location and then modifying that data within the same memory cycle. Data is read at the access time and modified during a period defined by the user. New data is written between $\overline{WE}$ low and the positive transition of $\overline{CE}$. Data out will remain valid until the rising edge of $\overline{CE}$. A minimum R-M-W cycle time can be calculated by $t_{RMW} = t_{AC} + t_{MOD} + t_{WPL} + t_P + 3\,t_T$; where t_{RMW} is the cycle time, t_{AC} is the access time, t_{MOD} is the user defined modify time, t_{WPL} is the $\overline{WE}$ to $\overline{CE}$ lead time, t_P is the $\overline{CE}$ high time, and t_T is one transition time.

POWER DOWN MODE

In power down, data may be retained indefinitely by maintaining V_{CC} at +3V. However, prior to V_{CC} going below V_{CC} minimum ($\leqslant$4.5V) $\overline{CE}$ must be taken high (V_{IH} = 2.2V) and held for a minimum time period t_{PPD} and maintained at V_{IH} for the entire standby period. After power is returned to V_{CC} min or above, $\overline{CE}$ must be held high for a minimum of t_{RC} in order that the device may operate properly. See power down waveforms herein. Any active cycle in progress prior to power down must be completed so that t_{CE} min is not violated.

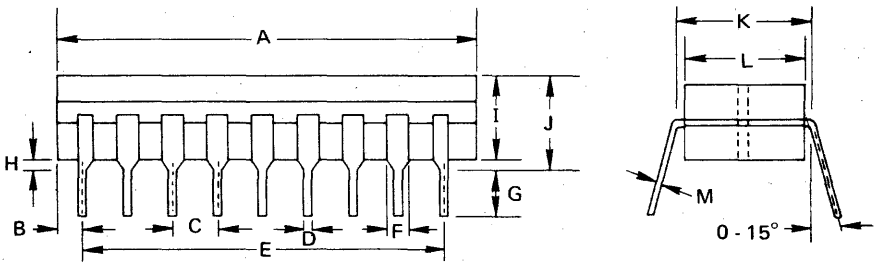
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PACKAGE OUTLINES
μPD4104C/D



Plastic

ITEM	MILLIMETERS	INCHES
A	23.2 MAX.	0.91 MAX.
B	1.44	0.055
C	2.54	0.1
D	0.45	0.02
E	20.32	0.8
F	1.2	0.06
G	2.5 MIN.	0.1 MIN.
H	0.5 MIN.	0.02 MIN.
I	4.6 MAX.	0.18 MAX.
J	5.1 MAX.	0.2 MAX.
K	7.62	0.3
L	6.7	0.26
M	0.25	0.01



Cerdip

ITEM	MILLIMETERS	INCHES
A	23.2 MAX.	0.91 MAX.
B	1.44	0.055
C	2.54	0.1
D	0.45	0.02
E	20.32	0.8
F	1.2	0.06
G	2.5 MIN.	0.1 MIN.
H	0.5 MIN.	0.02 MIN.
I	4.6 MAX.	0.18 MAX.
J	5.1 MAX.	0.2 MAX.
K	7.62	0.3
L	6.7	0.26
M	0.25	0.01

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NEC
μPD8108
PRELIMINARY

8K BIT STATIC RAM

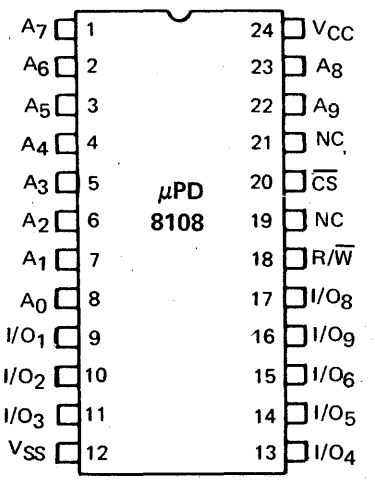
DESCRIPTION

The NEC μPD8108 is a very high speed 8192 bit static RAM. Organized as 1K x 8, it features a 22 pin dual-in-line package, full TTL compatibility, and a single +5V supply.

FEATURES

- 1024 x 8-Bit Organization
- Very Fast Access Time: 85/100/150/200 ns
- Single +5V Power Supply
- N-Channel Silicon Gate E/D Process
- 6-Device Static Cell
- Three State Common I/O
- Compatible with 8308 and Equivalent Devices
- Available in a 24 Pin Dual-in-Line Package

PIN CONFIGURATION



NC: No Connection

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NEC
μPD2716
PRELIMINARY

16K ULTRAVIOLET ERASABLE PROM

DESCRIPTION

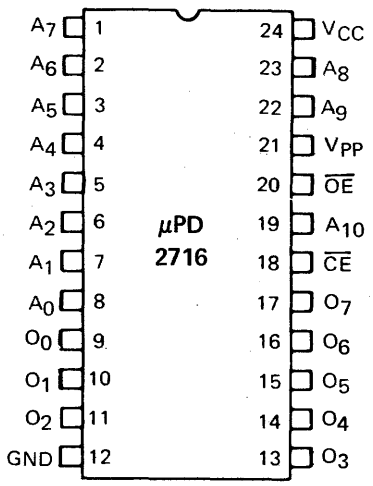
The μPD2716 is a 16,384-bit Ultraviolet Erasable and Electrically Programmable Read Only Memory. Organized as 2048 words x 8 bits, it operates from a single +5 volt power supply, making it ideal for microprocessor applications. It is pin-for-pin compatible with the μPD2316E, allowing economical changeover to a masked ROM for production quantities.

The μPD2716 features fast, simple, one pulse programming, controlled by TTL level signals. Total programming time for all 16,384 bits is only 100 seconds.

FEATURES

- Access Time — 450 ns Max
- 2048 Words x 8 Bits Organization
- Single +5V Supply
- Pin Compatible with μPD2316E Masked ROM
- Fast Programming
- TTL Level Controls for Reading and Programming
- Available in a 24 Pin Ceramic Package

PIN CONFIGURATION



PIN NAMES

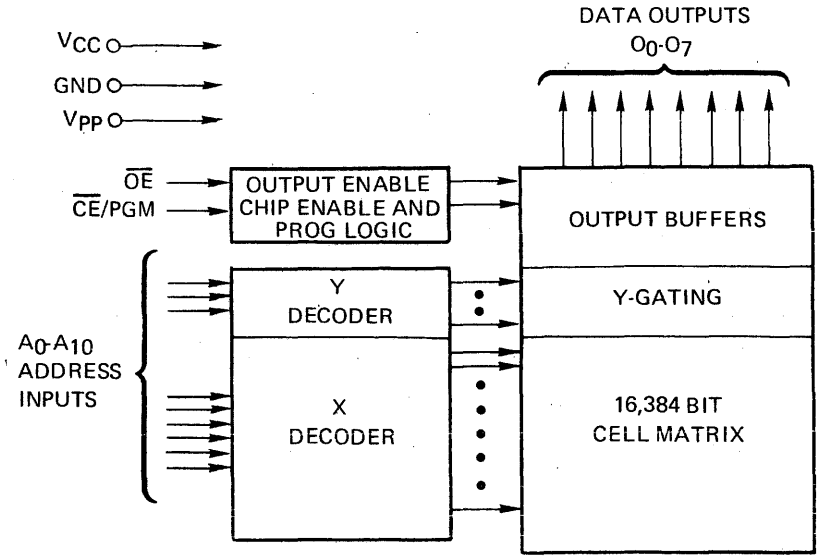
A_0-A_9	Addresses
$\overline{CE}$/PGM	Chip Enable/Program
$\overline{OE}$	Output Enable
O_0-O_7	Outputa

MODE SELECTION

MODE \ PINS	$\overline{CE}$/PGM	$\overline{OE}$	V_{PP}	V_{CC}	OUTPUTS
Read	V_{IL}	V_{IL}	+5	+5	D_{OUT}
Standby	V_{IH}	Don't Care	+5	+5	High Z
Program	Pulsed V_{IL} to V_{IH}	V_{IH}	+25	+5	D_{IN}
Program Verify	V_{IL}	V_{IL}	+25	+5	D_{OUT}
Program Inhibit	V_{IL}	V_{IH}	+25	+5	High Z

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BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	-10°C to +80°C
Storage Temperature	-65°C to +125°C
All Input Voltages	+6 to -0.3 Volts ①
All Output Voltages	+6 to -0.3 Volts ①
Supply Current V_{PP}	+26.5 to -0.3 Volts ②

Notes: ① With Respect to Ground.

② With Respect to Ground During Program.

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

CAPACITANCE ①

T_a = 25°C; f = 1 MHz

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input Capacitance	C_{IN}		4	6	pF	V_{IN} = 0V
Output Capacitance	C_{OUT}		8	12	pF	V_{OUT} = 0V

Note: ① This parameter is only sampled and is not 100% tested.

ERASURE OPERATION

The recommended erasure procedure is to illuminate the window with a ultraviolet lamp which has a wavelength of 2537 angstroms (Å). The distance should be one inch from the window to the lamp. Erasure time will be from 19 to 45 minutes depending on the type of ultraviolet lamp. The amount of time required can be expressed as the total amount of ultraviolet energy incident to the window, expressed in watt-seconds per square centimeter. The μPD2716 requires an integrated dosage (ultraviolet intensity x exposure time) of 15 watt-seconds/cm^2. This erase energy includes sufficient guard-band to ensure complete erasure of all bits.

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READ OPERATION

DC CHARACTERISTICS

$T_a = 0°C$ to $+70°C$; $V_{CC} = 5V \pm 5\%$; ① ② ; $V_{PP} = V_{CC} \pm 0.6V$ ③

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP ④	LIMITS MAX	UNIT	TEST CONDITIONS
Input Load Current	I_{LI}			10	μA	$V_{IN} = 5.25V$
Output Leakage Current	I_{LO}			10	μA	$V_{OUT} = 5.25V$
V_{PP} Current	I_{PP1} ②			12	mA	$V_{PP} = 5.85V$
V_{CC} Current (Standby)	I_{CC1} ②		10	25	mA	$\overline{CE} = V_{IH}$, $\overline{OE} = V_{IL}$
V_{CC} Current (Active)	I_{CC2} ②		57	100	mA	$\overline{CE} = \overline{CE} = V_{IL}$
Input Low Voltage	V_{IL}	-0.1		0.8	V	
Input High Voltage	V_{IH}	2.0		$V_{CC} + 1$	V	
Output Low Voltage	V_{OL}			0.45	V	$I_{OL} = 2.1$ mA
Output High Voltage	V_{OH}	2.2			V	$I_{OH} = -400\,\mu A$

AC CHARACTERISTICS

$T_a = 0°C$ to $+70°C$; $V_{CC} = 5V \pm 5\%$ ① ② ; $V_{PP} = V_{CC} \pm 0.6V$ ③

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP ④	LIMITS MAX	UNIT	TEST ⑥ CONDITIONS
Address to Output Delay	t_{ACC}			450	ns	$\overline{CE} = \overline{OE} = V_{IL}$
$\overline{CE}$ to Output Delay	t_{CE}			450	ns	$\overline{OE} = V_{IL}$
Output Enable to Output Delay	t_{OE}			140	ns	$\overline{CE} = V_{IL}$
Output Enable High to Output Float	t_{DF}	0		100	ns	$\overline{CE} = V_{IL}$
Address to Output Hold	t_{DH}	0			ns	$\overline{CE} = \overline{OE} = V_{IL}$

Notes: ① V_{CC} must be applied simultaneously or before V_{PP} and removed simultaneously or after V_{PP}.

② V_{PP} may be connected directly to V_{CC} except during programming. The supply current would then be the sum of I_{CC} and I_{PP1}.

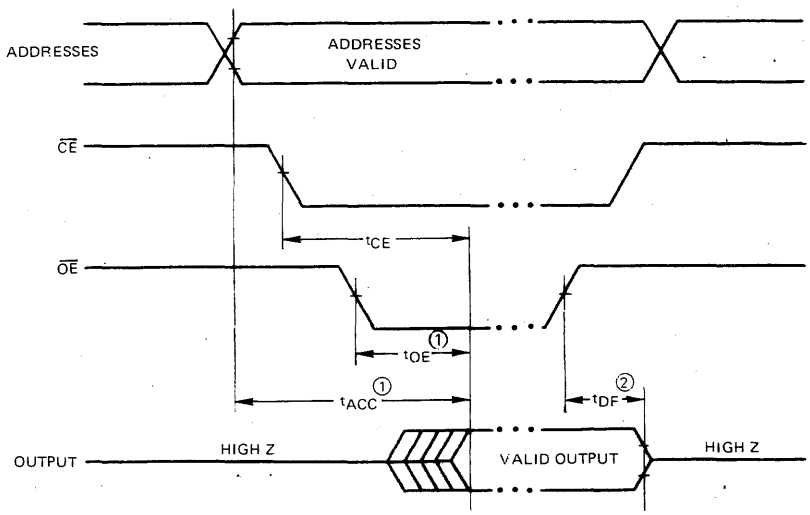
③ The tolerance of 0.6V allows the use of a driver circuit for switching the V_{PP} supply pin from V_{CC} in read to 25V for programming.

④ Typical values are for $T_a = 25°C$ and nominal supply voltages.

⑤ This parameter is only sampled and is not 100% tested.

⑥ AC Test Conditions: Output Load: 1 TTL gate and $C_L = 100$ pF
Input Rise and Fall Times: ≤20 ns
Input Pulse Levels: 0.8V to 2.2V
Timing Measurement Reference Level:
Inputs: 1V and 2V
Outputs: 0.8V and 2V

TIMING WAVEFORMS ①



Notes: ① $\overline{OE}$ may be delayed up to $t_{ACC} - t_{OE}$ after the falling edge of $\overline{CE}$ without impact on t_{ACC}.

② t_{DF} is specified from $\overline{OE}$ or $\overline{CE}$, whichever occurs first.

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PROGRAMMING OPERATION

Initially, and after each erasure, all bits of the μPD2716 are in the "1" state. Information is introduced by selectively programming "0" into the desired bit locations. A programmed "0" can only be changed to a "1" by UV erasure.

The μPD2716 is programmed by applying a 50 ms, TTL programming pulse to the $\overline{CE}$/PGM pin with the $\overline{CE}$ input high and the Vpp supply at 25V ± 1V. Any location may be programmed at any time – either individually, sequentially, or randomly. The programming time for a single bit is only 50 ms and for all bits is approximately 100 seconds for the μPD2716.

CAUTION: The V_{CC} and Vpp supplied must be sequenced on and off such that V_{CC} is applied simultaneously or before Vpp and removed simultaneously or after Vpp to prevent damage to the μPD2716. The maximum allowable voltage during programming which may be applied to the Vpp with respect to ground is +26V. Care must be taken when switching the Vpp supply to prevent overshoot exceeding the 26V maximum specification. For convenience in programming, the μPD2716 may be verified with the Vpp supply at 25V ± 1V. During normal read operation, however, Vpp must be at V_{CC}.

DC CHARACTERISTICS ①

T_a = 25°C ± 5°C; V_{CC} = 5V ± 5% ②; Vpp = 25V ± 1V ② ③

PARAMETER	SYMBOL	LIMITS MIN	TYP	MAX	UNIT	TEST CONDITIONS
Input Current (for Any Input)	I_{LI}			10	μA	V_{IN} = 5.25V/0.45
Vpp Supply Current	I_{PP1}			12	mA	$\overline{CE}$/PGM = V_{IL}
Vpp Supply Current During Programming Pulse	I_{PP2}			30	mA	$\overline{CE}$/PGM = V_{IH}
V_{CC} Supply Current	I_{CC}			100	mA	
Input Low Level	V_{IL}	-0.1		0.8	V	
Input High Level	V_{IH}	2.0		V_{CC} + 1	V	

AC CHARACTERISTICS ①

T_a = 25°C ± 5°C; V_{CC} = 5V ± 5% ②; Vpp = 25V ± 1V ② ③

PARAMETER	SYMBOL	LIMITS MIN	TYP	MAX	UNITS	TEST CONDITIONS ④
Address Setup Time	t_{AS}	2			μs	
$\overline{OE}$ Setup Time	t_{OES}	2			μs	
Data Setup Time	t_{DS}	2			μs	
Address Hold Time	t_{AH}	2			μs	
$\overline{OE}$ Hold Time	t_{OEH}	2			μs	
Data Hold Time	t_{DH}	2			μs	
Output Enable to Output Float Delay	t_{DF}	0		120	ns	$\overline{CE}$/PGM = V_{IL}
Output Enable to Output Delay	t_{OE}			120	ns	$\overline{CE}$/PGM = V_{IL}
Program Pulse Width	t_{PW}	45	50	55	ms	
Program Pulse Rise Time	t_{PRT}	5			ns	
Program Pulse Fall Time	t_{PFT}	5			ns	

Notes: ① NEC Microcomputer's standard product warranty applies only to devices programmed to specifications described herein.

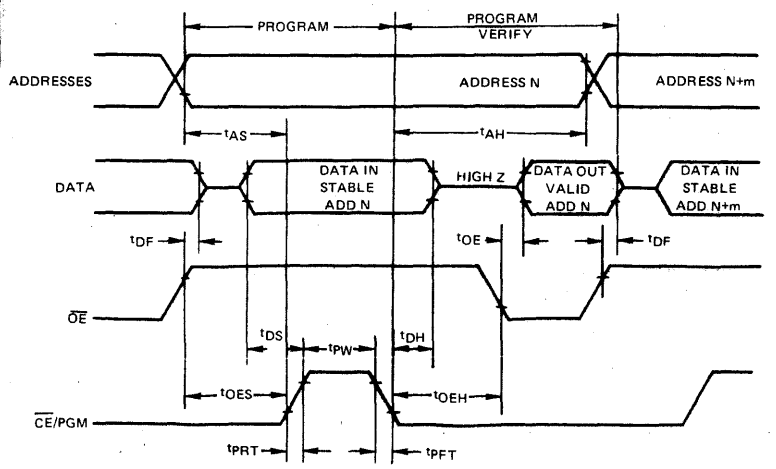
② V_{CC} must be applied simultaneously or before Vpp and removed simultaneously or after Vpp. The μPD2716 must not be inserted into or removed from a board with Vpp at 25 ± 1V to prevent damage to the device.

③ The maximum allowable voltage which may be applied to the Vpp pin during programming is +26V. Care must be taken when switching the Vpp supply to prevent overshoot exceeding this 26V maximum specification.

④ AC Test Conditions:

V_{CC}	5V ± 5%	Input Pulse Levels	0.8V to 2.2V
Vpp	25V ± 1V	Input Timing Reference Level	1V and 2V
Input Rise and Fall Times (10% to 90%)	20 ns	Output Timing Reference Level	0.8V and 2V

TIMING WAVEFORM



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4096-BIT BIPOLAR TTL PROGRAMMABLE READ ONLY MEMORY

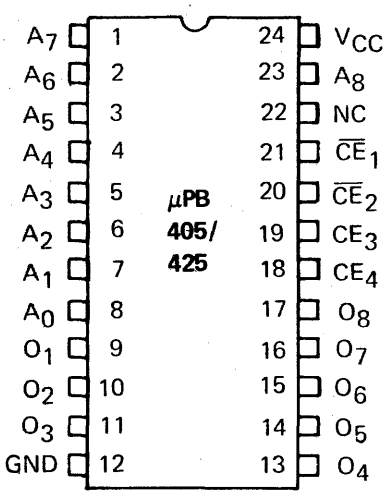
DESCRIPTION

The μPB405 and μPB425 are high speed, electrically programmable, fully decoded 4096-bit TTL read only memories. On-chip address decoding, four chip enable inputs and open-collector outputs allow easy expansion of memory capacity. The μPB405 and μPB425 are fabricated with logic level zero (low); logic level one (high) can be electrically programmed into the selected bit locations. The same address inputs are used for both programming and reading.

FEATURES

- 512 Words X 8 Bits Organization (Fully Decoded)
- TTL Interface
- Fast Read Access Time: 70 ns max. (μPB425)
- Medium Power Consumption: 600 mW TYP.
- Four Chip Enable Inputs for Memory Expansion
- Open-Collector Outputs (μPB405)/Three-State Outputs (μPB425)
- Ceramic 24-Lead Dual In-Line Package
- Fast Programming Time: 200 μs/bit TYP.
- Compatibility with: Intersil's IM5605/5625 (both in programming and as a ROM), Harris' HPROM HM-7640/7641 and Equivalent Devices (as a ROM).
- A.I.M. (Avalanche Induced Migration) Technology

PIN CONFIGURATION



NC: No Connection

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OPERATION

Chip Enable logic is defined by:

$\overline{CE}_1$	$\overline{CE}_2$	CE_3	CE_4	CE'
0	0	1	1	0
All other combinations				1

Where: CE' = 0 denotes chip selected
CE' = 1 denotes chip deselected

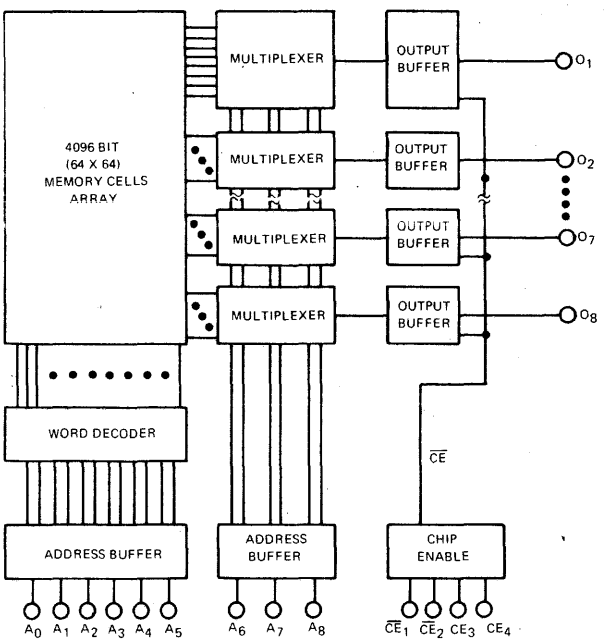
Programming

A logic one can be permanently programmed into a selected bit location in accordance with the programming procedures specified. First, the desired word is selected by the eight TTL address inputs. The four Chip Enable inputs must be set so that CE' is a logical one. Secondly, a train of high current programming pulses is applied to the desired output. After the sensed voltage indicates that the selected bit is in the logic one state, an additional pulse train is applied, and programming is complete.

Reading

To read the memory, the four Chip Enable inputs must be set so that CE' is a logical zero. The outputs then correspond to the data programmed in the selected words. When the four Chip Enable inputs are set so that CE' becomes a logical one, all the outputs will be high (floating).

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	−25°C to +75°C
Storage Temperature	−65°C to +150°C
All Output Voltages	−0.5 to +5.5 Volts
All Input Voltages	−0.5 to +5.5 Volts
Supply Voltage V_{CC}	−0.5 to +7.0 Volts
Output Currents	50 mA

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

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DC CHARACTERISTICS

T_a = 0°C to +65°C, V_{CC} = 4.75V to 5.25V

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN.	TYP.	MAX.		
Input High Voltage	V_{IH}	2.0			V	
Input Low Voltage	V_{IL}			0.8	V	
Input High Current	I_{IH}			40	μA	V_I = 2.7V
Input Low Current	$-I_{IL}$			0.5	mA	V_I = 0.4V
Output Low Voltage	V_{OL}			0.45	V	I_O = 16 mA
Output Leakage Current	I_{OFF1}			40	μA	V_O = 5.25V
Output Leakage Current	$-I_{OFF2}$	40			μA	V_O = 0.4V
Input Clamp Voltage	$-V_{IC}$			1.3	V	I_I = −12 mA
Power Supply Current	I_{CC}		120	160	mA	All Inputs Grounded
Output High Voltage①	V_{OH}	2.4			V	I_O = −2.4 mA
Output Short Circuit Current①	$-I_{SC}$	15		60	mA	V_O = 0V

NOTE: ① Applicable to μPB425D only.

AC CHARACTERISTICS

T_a = 25°C; V_{CC} = 5.0V

PARAMETER	SYMBOL	LIMITS						UNIT	TEST CONDITIONS
		μPB405-E/425-E			μPB425				
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.		
Address Access Time	t_{AA}			100		40	70	ns	
Chip Enable Access Time	t_{ACE}			70			35	ns	
Chip Enable Disable Time	t_{DCE}			70			35	ns	

Notes: ① Output Load: See Figure 1
② Input Waveform: 0.0V for low level and 3.0V for high level, less than 10 ns for both rise and fall times.
③ Measurement References: 1.5V for both inputs and outputs
④ C_L in Figure 1 includes jig and probe stray capacitances.

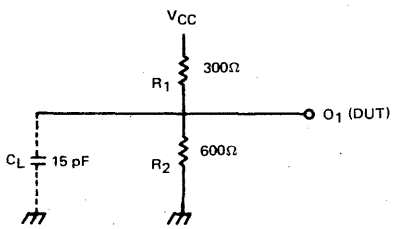
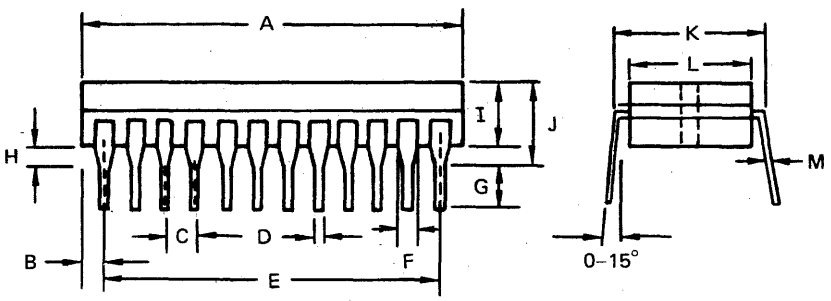


Figure 1

PACKAGE OUTLINE
μPB405D
μPB425D



ITEM	MILLIMETERS	INCHES
A	33.5 MAX.	1.32 MAX.
B	2.78	0.11
C	2.54	0.1
D	0.46	0.018
E	27.94	1.1
F	1.5	0.059
G	2.54 MIN.	0.1 MIN.
H	0.5 MIN.	0.019 MIN.
I	4.58 MAX.	0.181 MAX.
J	5.08 MAX.	0.2 MAX.
K	15.24	0.6
L	13.5	0.53
M	$0.25^{+0.10}_{-0.05}$	$0.01^{+0.004}_{-0.002}$

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PROGRAMMING SPECIFICATION

It is imperative that this specification be rigorously observed in order to correctly program the μPB405 and μPB425. NEC will not accept responsibility for any device found to be defective if it were not programmed according to this specification.

A typical programming operation is performed by first sensing, then programming, then sensing again to see if the word to be programmed has reached the desired state.

Sensing is accomplished by forcing a 20 mA current into the selected location via the output. The μPB405 and μPB425 are disabled in accordance with the truth table on page 2. The sense measurement is to ensure that the voltage required to force this 20 mA current is less than the reference voltage. If this condition is satisfied, then that bit location is in the logic "1" (high) state.

Programming is accomplished by forcing a 200 mA current into the selected bit via the output. This current pulse is applied for 7.5 μs and then the location is sensed before a second programming current pulse is applied. This process is continued until that location is altered to the "1" state. A bit is judged to be programmed when two successive sense readings 10 μs apart with no intervening programming pulse, pass the limit. When this condition has been met, four additional pulses are applied and the pulse train, then the sense current is terminated.

CHARACTERISTIC	LIMIT	UNIT	NOTES
Ambient Temperature	25 ± 5	°C	
Programming Pulse			
Amplitude	200 ± 5%	mA	
Clamp Voltage	28 + 0% − 2%	V	
Ramp Rate (both in Rise and in Fall)	70 MAX.	V/μs	
Pulse Width	7.5 ± 5%	μs	15V point/ 150Ω load.
Duty Cycle	70% MIN.		
Sense Current			
Amplitude	20 ± 0.5	mA	
Clamp Voltage	28 + 0% − 2%	V	
Ramp Rate	70 MAX.	V/μs	15V point/ 150Ω load.
Sense Current Interruption before and after address change	10 MIN.	μs	
Programming V_{CC}	5.0 + 5% − 0%	V	
Maximum Sensed Voltage for programmed "1"	7.0 ± 0.1	V	
Delay from trailing edge of programming pulse before sensing output voltage	0.7 MIN.	μs	

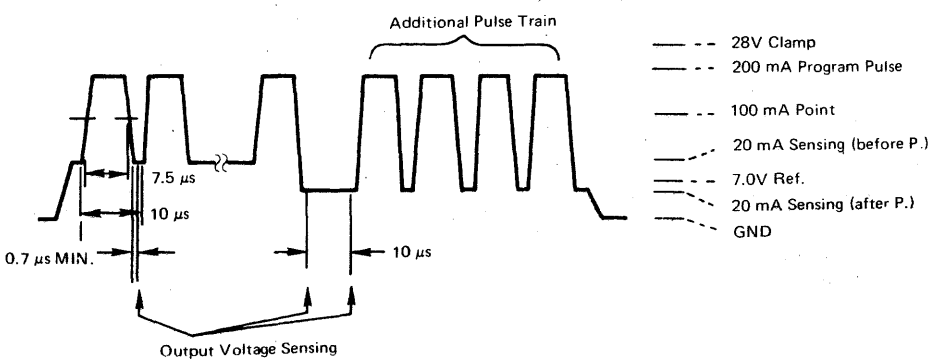


Figure 2. Typical Output Voltage Waveform

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NEC
μPB406
μPB406-E
μPB426
μPB426-E

4096-BIT BIPOLAR TTL PROGRAMMABLE READ ONLY MEMORY

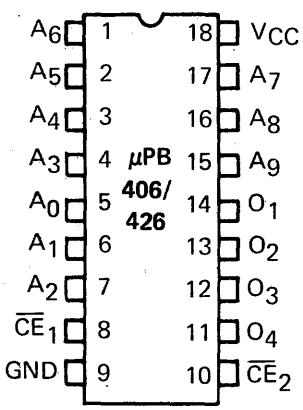
DESCRIPTION

The μPB406 and μPB426 are high speed electrically programmable fully decoded 4096-bit TTL read only memories. On-chip address decoding, two chip enable inputs and open-collector/three-state outputs allow easy expansion of memory capacity. The μPB406 and μPB426 are fabricated with logic level zero (low); logic level one (high) can be electrically programmed into the selected bit locations. The same address inputs are used for both programming and reading.

FEATURES

- 1024 Words X 4 Bits Organization (Fully Decoded)
- TTL Interface
- Fast Read Access Time: 70 ns MAX. (μPB406/426)
- Medium Power Consumption: 500 mW TYP.
- Two Chip Enable Inputs for Memory Expansion
- Open-Collector Output (μPB406/406-E)/Three-State Outputs (μPB426/426-E)
- Ceramic 18-Lead Dual In-Line Package
- Fast Programming Time: 200 μs/bit TYP.
- Compatibility with: Intersil's IM56S06/56S26 (both in programming and as a ROM), Harris' HPROM HM-7642/7643 and Equivalent Devices (as a ROM)
- A.I.M. (Avalanche Induced Migration) Technology

PIN CONFIGURATION



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OPERATION

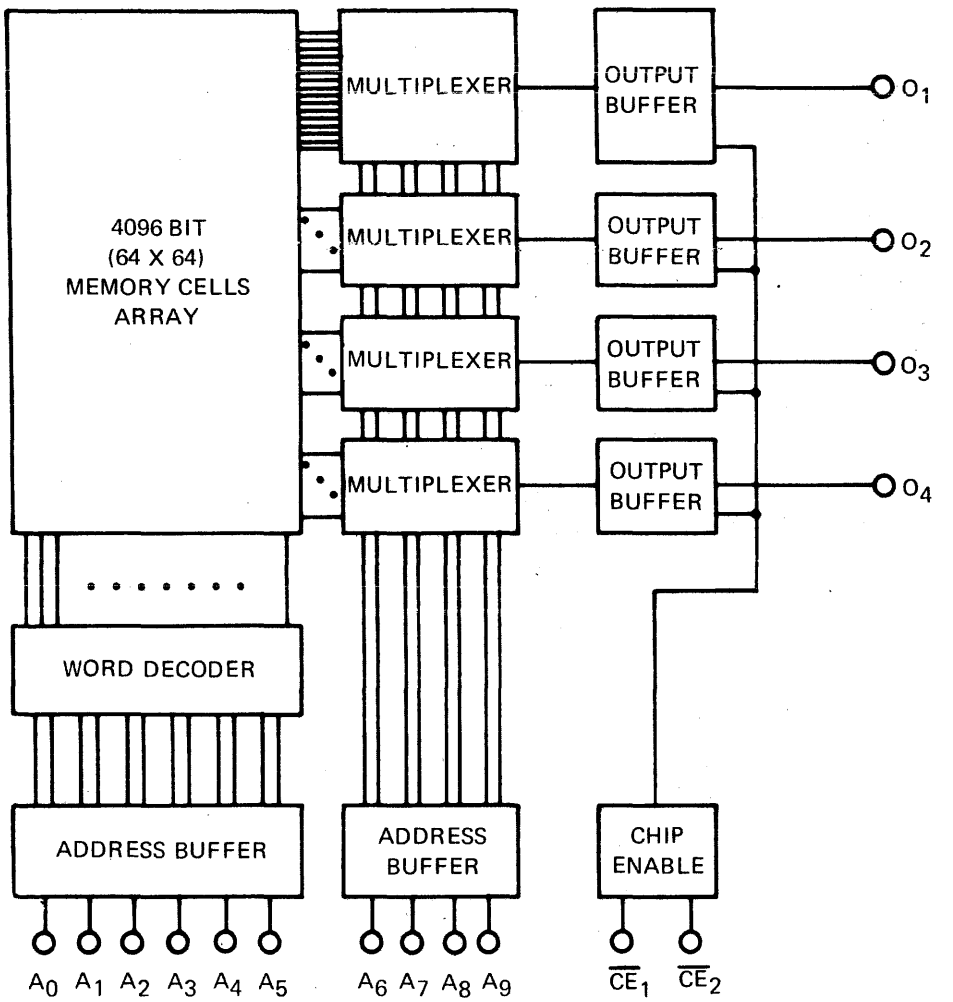
Programming

A logic one can be permanently programmed into a selected bit location by using special equipment (programmer). First, the desired word is selected by the ten address inputs in TTL levels. Either or both of the two chip enable inputs must be at a logic one (high). Secondly, a train of high current programming pulses is applied to the desired output. After the sensed voltage indicates that the selected bit is in the logic one state, an additional pulse train is applied, then is stopped.

Reading

To read the memory, both of the two chip enable inputs should be held at logic zero (low). The outputs then correspond to the data programmed in the selected words. When either or both of the two chip enable inputs are at logic one (high), all the outputs will be high (floating).

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	-25°C to +75°C
Storage Temperature	-65°C to +150°C
All Output Voltages	-0.5 to +5.5 Volts
All Input Voltages	-0.5 to +5.5 Volts
Supply Voltage V_{CC}	-0.5 to +7.0 Volts
Output Currents	50 mA

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

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DC CHARACTERISTICS

T_a = 0°C to +65°C, V_{CC} = 4.75V to 5.25V

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN.	TYP.	MAX.		
Input High Voltage	V_{IH}	2.0			V	
Input Low Voltage	V_{IL}			0.8	V	
Input High Current	I_{IL}			40	μA	V_I = 2.7V
Input Low Current	$-I_{IL}$			0.5	mA	V_I = 0.4V
Output Low Voltage	V_{OL}			0.45	V	I_O = 16 mA
Output Leakage Current	I_{OFF1}			40	μA	V_O = 5.25V
Output Leakage Current	$-I_{OFF2}$	40			μA	V_O = 0.4V
Input Clamp Voltage	$-V_{IC}$			1.3	V	I_I = −12 mA
Power Supply Current	I_{CC}		100	150	mA	All Inputs Grounded
Output High Voltage①	V_{OH}	2.4			V	I_O = −2.4 mA
Output Short Circuit Current①	$-I_{SC}$	15		60	mA	V_O = 0V

NOTE: ① Applicable to μPB426D only.

AC CHARACTERISTICS

T_a = 25°C, V_{CC} = 5.0V

PARAMETER	SYMBOL	LIMITS						UNIT	TEST CONDITIONS
		μPB406-E/426-E			μPB406/426				
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.		
Address Access Time	t_{AA}			100		40	70	ns	
Chip Enable Access Time	t_{ACE}			70			40	ns	
Chip Enable Disable Time	t_{DCE}			70			40	ns	

Notes: ① Output Load: See Figure 1.
② Input Waveform: 0.0V for low level and 3.0V for high level, less than 10 ns for both rise and fall times.
③ Measurement References: 1.5V for both inputs and outputs.
④ C_L in Figure 1 includes jig and probe stray capacitances.

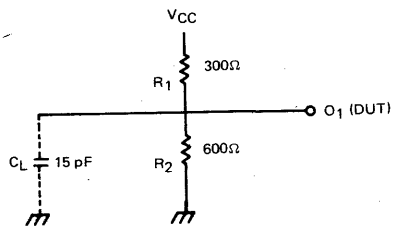
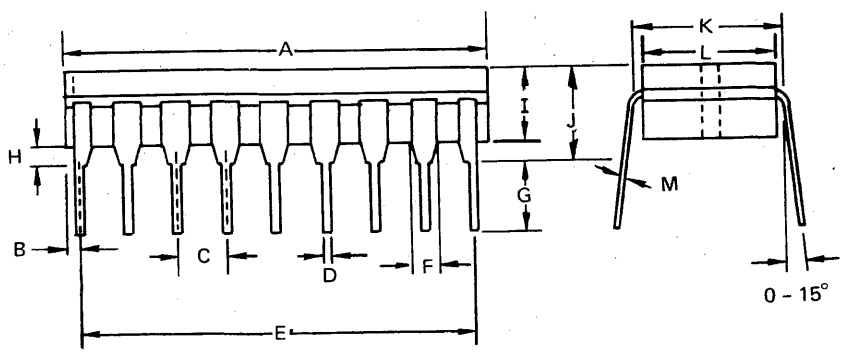


Figure 1

PACKAGE OUTLINE
μPB406D
μPB426D



ITEM	MILLIMETERS	INCHES
A	23.2 MAX.	0.91 MAX.
B	1.44	0.055
C	2.54	0.1
D	0.45	0.02
E	20.32	0.8
F	1.2	0.05
G	2.5 MIN.	0.1 MIN.
H	0.5 MIN.	0.02 MIN.
I	4.6 MAX.	0.18 MAX.
J	5.1 MAX.	0.2 MAX.
K	7.62	0.3
L	6.7	0.26
M	0.25	0.01

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PROGRAMMING SPECIFICATION

It is imperative that this specification be rigorously observed in order to correctly program the μPB406 and μPB426. NEC will not accept responsibility for any device found to be defective if it were not programmed according to this specification.

A typical programming operation is performed by first sensing, then programming, then sensing again to see if the word to be programmed has reached the desired state. Either or both of the two chip enable inputs must be at a logic one (high).

Sensing is accomplished by forcing a 20 mA current into the selected location via the output. The sense measurement is to ensure that the voltage required to force this 20 mA current is less than the reference voltage. If this condition is satisfied, then that bit location is in the logic "1" (high) state.

Programming is accomplished by forcing a 200 mA current into the selected bit via the output. This current pulse is applied for 7.5 μs and then the location is sensed before a second programming current pulse is applied. This process is continued until that location is altered to the "1" state. A bit is judged to be programmed when two successive sense readings 10 μs apart with no intervening programming pulse, pass the limit. When this condition has been met, four additional pulses are applied and the pulse train, then the sense current is terminated.

CHARACTERISTIC	LIMIT	UNIT	NOTES
Ambient Temperature	25 ± 5	°C	
Programming Pulse			
Amplitude	200 ± 5%	mA	
Clamp Voltage	28 + 0% − 2%	V	
Ramp Rate (both in Rise and in Fall)	70 MAX.	V/μs	
Pulse Width	7.5 ± 5%	μs	15V point/ 150Ω load.
Duty Cycle	70% MIN.		
Sense Current			
Amplitude	20 ± 0.5	mA	
Clamp Voltage	28 + 0% − 2%	V	
Ramp Rate	70 MAX.	V/μs	15V point/ 150Ω load.
Sense Current Interruption before and after address change	10 MIN.	μs	
Programming V_{CC}	5.0 + 5% − 0%	V	
Maximum Sensed Voltage for programmed "1"	7.0 ± 0.1	V	
Delay from trailing edge of programming pulse before sensing output voltage	0.7 MIN.	μs	

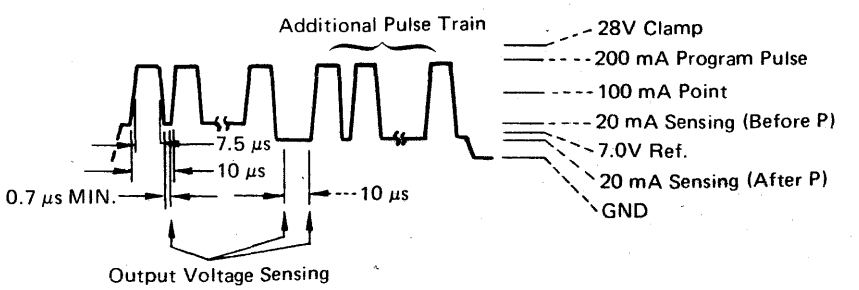


Figure 2 – Typical Output Voltage Waveform

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8192 BIT BIPOLAR TTL PROGRAMMABLE READ ONLY MEMORY

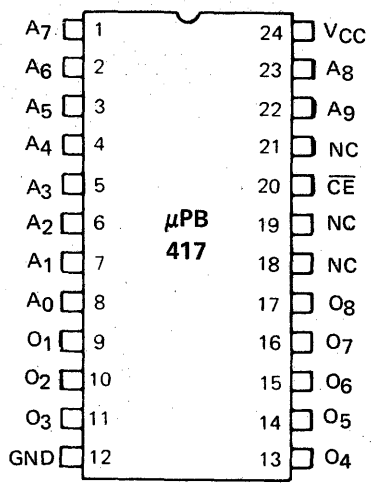
DESCRIPTION

The μPB417 is a high speed, electrically programmable, fully decoded 8192-bit TTL read only memory. On-chip address decoding, two chip enable input and three-state outputs allow easy expansion of memory capacity. The μPB417 is fabricated with logic level zero (low); logic level one (high) can be electrically programmed into the selected bit locations. The same address inputs are used for both programming and reading.

FEATURES

- 1024 Words x 8 Bits Organization (Fully Decoded)
- TTL Interface
- Fast Read Access Time: 200 ns Max.
- Power Dissipation: 500 mW Typ.
- Two Chip Enable Inputs for Memory Expansion
- Three-State Outputs
- Fast Programming Time: 200 μs/bit Typ.
- Direct Replacement for 2708 and Equivalent Devices (as a ROM)
- Available in Plastic and Ceramic 24 Pin Packages

PIN CONFIGURATION



NC: No Connection

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OPERATION

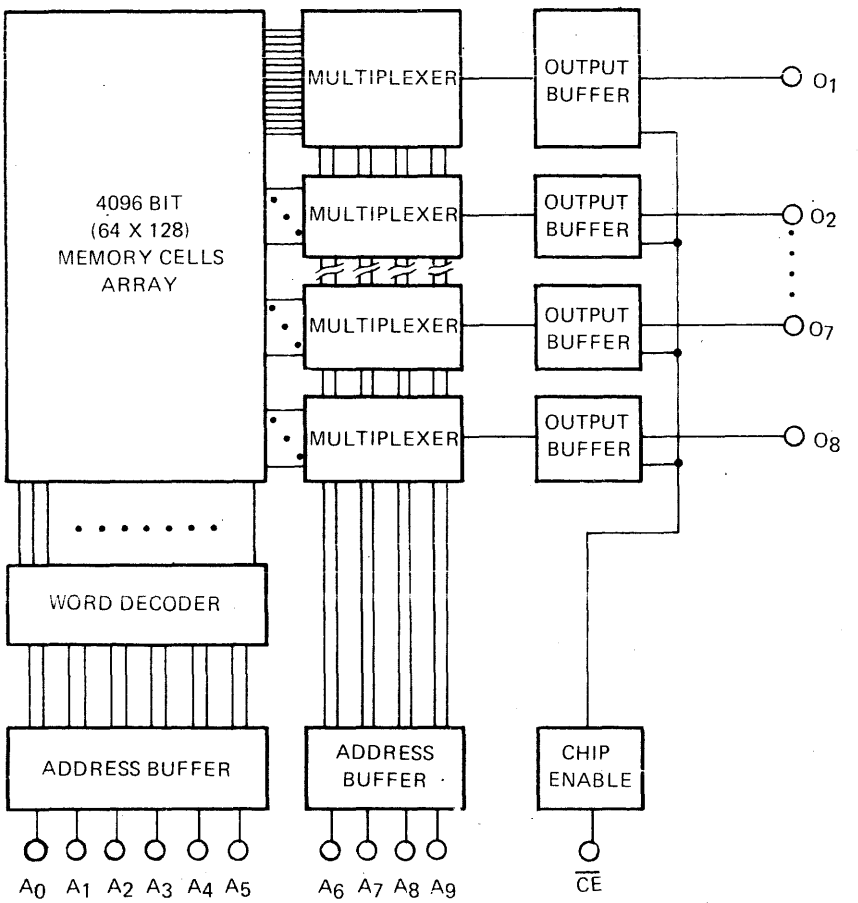
Programming

A logic one can be permanently programmed into a selected bit location by using special equipment (programmer). First the Chip Enable CE must be a logical one in order to disable the outputs. Second, the desired word is selected by the ten address inputs in TTL levels. Third, a train of high current programming pulses is applied to the desired output. After the sensed voltage indicates that the selected bit is in the logic one state, an additional pulse train is applied, then is stopped.

Reading

To read the memory, the Chip Enable input must be a logical zero. The outputs then correspond to the data programmed in the selected words. When the Chip Enable input is a logical one, all the outputs will be disabled (floating).

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	−25°C to +75°C
Storage Temperature	−65°C to +150°C
All Output Voltages	−0.5 to +5.5 Volts
All Input Voltages	−0.5 to +5.5 Volts
Supply Voltage V_{CC}	−0.5 to +7.0 Volts
Output Currents	50 mA

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

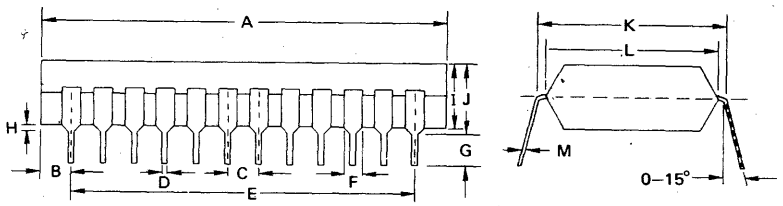
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DC CHARACTERISTICS

$T_a = 0°$ to $+65°C$; $V_{CC} = 4.75$ to $5.25V$

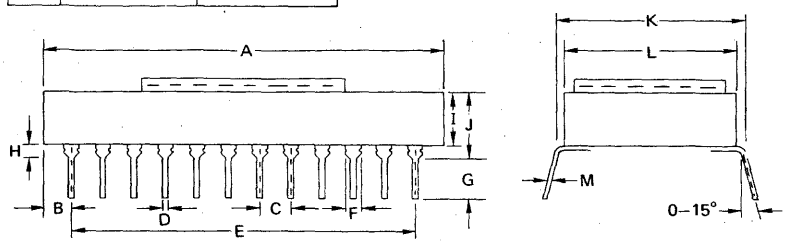
PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input High Voltage	V_{IH}	2.0			V	
Input Low Voltage	V_{IL}			0.8	V	
Input High Current	I_{IH}			40	μA	$V_I = 2.7V$
Input Low Current	$-I_{IL}$			0.3	mA	$V_I = 0.4V$
Output Low Voltage	V_{OL}			0.45	V	$I_O = 3.2$ mA
Output Leakage Current	I_{OFF1}			40	μA	$V_O = 5.25V$
Output Leakage Current	$-I_{OFF2}$	40			μA	$V_O = 0.4V$
Input Clamp Voltage	$-V_{IC}$			1.3	V	$I_I = -12$ mA
Active Power Supply Current	I_{CCA}		100	140	mA	All Inputs Grounded
Output High Voltage	V_{OH}	2.4			V	$I_O = -1.0$ mA

PACKAGE OUTLINES μPB417C/D



μPB417C (Plastic)

ITEM	MILLIMETERS	INCHES
A	33 MAX	1.3 MAX
B	2.53	0.1
C	2.54	0.1
D	0.5 ± 0.1	0.02 ± 0.004
E	27.94	1.1
F	1.5	0.059
G	2.54 MIN	0.1 MIN
H	0.5 MIN	0.02 MIN
I	5.22 MAX	0.205 MAX
J	5.72 MAX	0.225 MAX
K	15.24	0.6
L	13.2	0.52
M	$0.25^{+0.10}_{-0.05}$	$0.01^{+0.004}_{-0.0019}$



μPB417D (Ceramic)

ITEM	MILLIMETERS	INCHES
A	32.5 MAX	1.28 MAX
B	2.28	0.09
C	2.54	0.1
D	0.5 ± 0.1	0.02 ± 0.004
E	27.94	1.1
F	1.20 MIN	0.047 MIN
G	3.2 MIN	0.126 MIN
H	1.0 MIN	0.04 MIN
I	4.2 MAX	0.165 MAX
J	5.2 MAX	0.205 MAX
K	15.24	0.6
L	13.9	0.55
M	0.30 ± 0.1	0.012 ± 0.004

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AC CHARACTERISTICS

T_a = 25°C; V_{CC} = 5.0V

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Address Access Time	t_{AA}			200	ns	
Chip Enable Access Time	t_{ACE}			120	ns	
Chip Enable Disable Time	t_{DCE}			120	ns	

Notes: ① Output Load: See Figure 1.
② Input Waveform: 0.0V for low level and 3.0V for high level, less than 10 ns for both rise and fall times.
③ Measurement References: 1.5V for both inputs and outputs.
④ C_L in Figure 1 includes jig and probe stray capacitances.

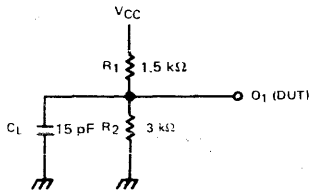


Figure 1

PROGRAMMING SPECIFICATION

It is imperative that this specification be rigorously observed in order to correctly program the μPB417. NEC will not accept responsibility for any device found to be defective if it were not programmed according to this specification.

CHARACTERISTIC	LIMIT	UNIT	NOTES
Ambient Temperature	25 ± 5	°C	
Programming Pulse			
Amplitude	200 ± 5%	mA	
Clamp Voltage	28 + 0% − 2%	V	
Ramp Rate (both in Rise and in Fall)	70 Max.	V/μs	
Pulse Width	7.5 ± 5%	μs	15V point/ 150Ω load.
Duty Cycle	70% Min.		
Sense Current			
Amplitude	20 ± 0.5	mA	
Clamp Voltage	28 + 0% − 2%	V	
Ramp Rate	70 Max.	V/μs	15V point/ 150Ω load.
Sense Current Interruption before and after address change	10 Min.	μs	
Programming V_{CC}	5.0 + 5% − 0%	V	
Maximum Sensed Voltage ① for programmed "1"	7.0 ± 0.1	V	
Delay from trailing edge of programming pulse before sensing output voltage	0.7 Min.	μs	

Note: ① A bit is judged to be programmed when two successive sense readings 10 μs apart with no intervening programming pulse, pass the limit. When this condition has been met, four additional pulses are applied and the pulse train, then the sense current is terminated.

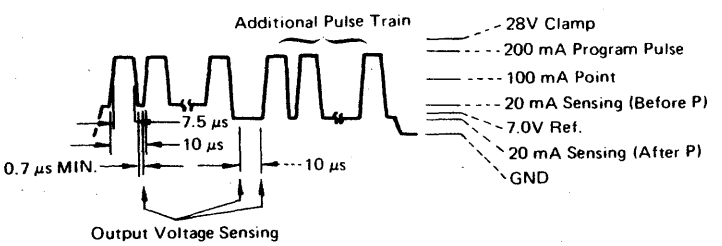


Figure 2 — Typical Output Voltage Waveform

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FULLY DECODED 16,384 BIT MASK PROGRAMMABLE READ ONLY MEMORY

DESCRIPTION

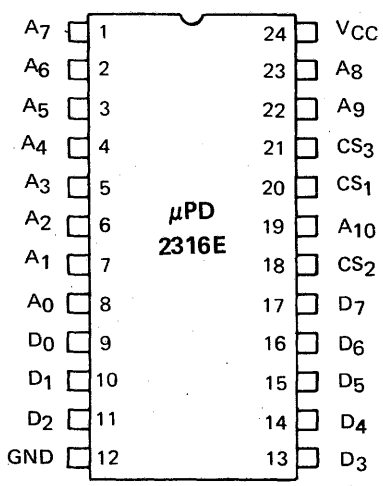
The NEC μPD2316E is a high speed 16,384 bit mask programmable Read Only Memory organized as 2048 words by 8 bits. The μPD2316E is fabricated with N-channel MOS technology.

The inputs and outputs are fully TTL compatible. The device operates with a single +5V power supply. The three chip select inputs are programmable. Any combination of active high or low level chip select inputs can be defined and desired chip select code is fixed during the masking process.

FEATURES

- Access Time 450 ns Max
- 2048 Words x 8 Bits Organization
- Single +5V ±10% Power Supply Voltage
- Directly TTL Compatible – All Inputs and Outputs
- Three Programmable Chip Select Inputs for Easy Memory Expansion
- Three-State Output – OR-Tie Capability
- On-Chip Address Fully Decoded
- All Inputs Protected Against Static Charge
- Direct Replacement for 2316E
- Available in 24-pin plastic or ceramic packages

PIN CONFIGURATION

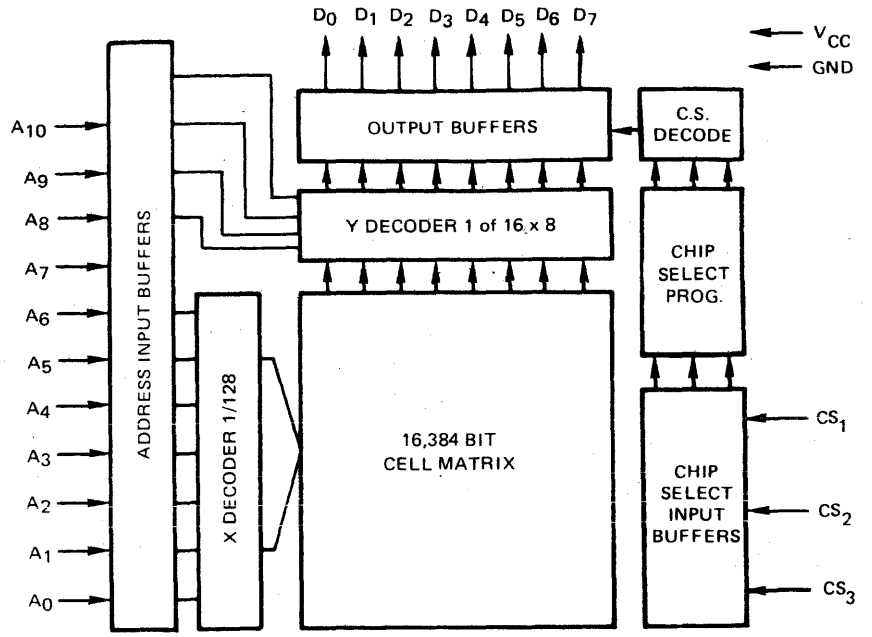


PIN NAMES

$A_0 - A_{10}$	Address Inputs
$D_1 - D_8$	Data Outputs
$CS_1 - CS_3$	Programmable Chip Select Inputs

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BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	−10°C to +70°C
Storage Temperature	−65°C to +125°C
Voltage on Any Pin	−0.5 to +7.0 Volts (1)

Note: (1) With Respect to Ground.

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

DC CHARACTERISTICS

T_a = −10°C to +70°C; V_{CC} = +5 ± 5% unless otherwise noted.

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP (1)	LIMITS MAX	UNIT	TEST CONDITIONS
Input Load Current (All Input Pins)	I_{LI}			+10	μA	$V_{IN} = V_{CC}$
				−10	μA	V_{IN} = 0V
Output Leakage Current	I_{LOH}			+10	μA	Chip Deselected, $V_O = V_{CC}$
Output Leakage Current	I_{LOL}			−20	μA	Chip Deselected, V_O = 0V
Power Supply Current	I_{CC}		70	120	mA	
Input "Low" Voltage	V_{IL}	−0.5		0.8	V	
Input "High" Voltage	V_{IH}	+2.4		V_{CC} + 1.0V	V	
Output "Low" Voltage	V_{OL}			0.4	V	I_{OL} = 2.1 mA
Output "High" Voltage	V_{OH}	+2.4			V	I_{OH} = −400 μA

Note: (1) Typical values for T_a = 25°C and nominal supply voltage.

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CAPACITANCE

$T_a = 25°C$; f = 1 MHz

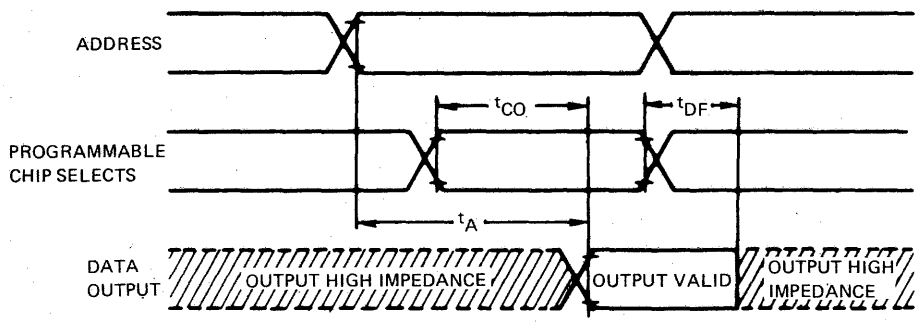
PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input Capacitance	C_{IN}		5	10	pf	All Pins Except Pin Under Test Tied to AC Ground
Output Capacitance	C_{OUT}		10	15	pf	All Pins Except Pin Under Test Tied to AC Ground

AC CHARACTERISTICS

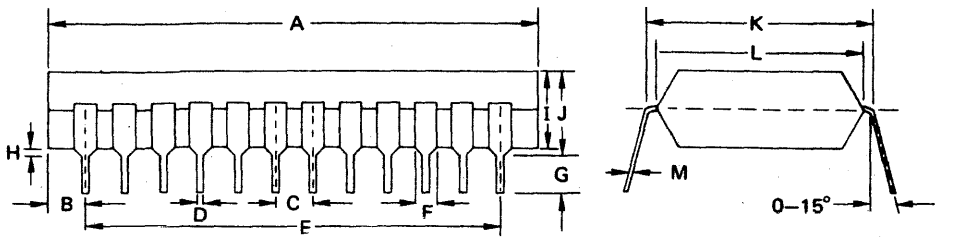
$T_a = -10°C$ to $+70°C$; $V_{CC} = +5V \pm 5\%$ unless otherwise specified.

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Address to Output Delay Time	t_A			450	ns	$t_T = t_r = t_f = 20$ ns $V_{ref\ in} = 1V, 2.2V$ $V_{ref\ out} = 0.8V, 2V$ Output LOAD = 1 TTL GATE $C_L = 100$ pf
Chip Select to Output Enable Delay Time	t_{CO}			120	ns	
Chip Deselect to Output Data Float Delay Time	t_{DF}	10		100	ns	

TIMING WAVEFORMS



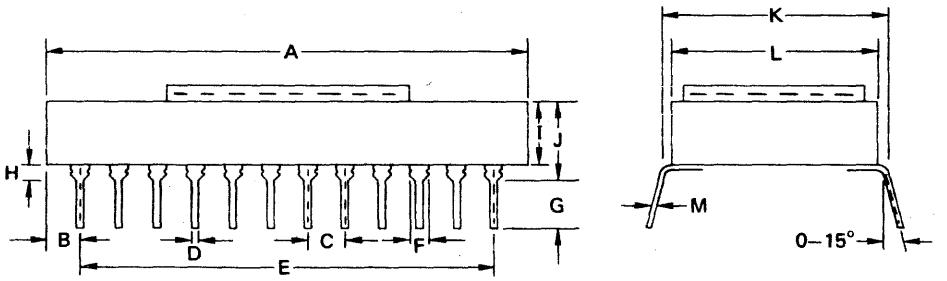
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PACKAGE OUTLINE
μPD2316EC/D

μPD2316EC (Plastic)

ITEM	MILLIMETERS	INCHES
A	33 MAX	1.3 MAX
B	2.53	0.1
C	2.54	0.1
D	0.5 ± 0.1	0.02 ± 0.004
E	27.94	1.1
F	1.5	0.059
G	2.54 MIN	0.1 MIN
H	0.5 MIN	0.02 MIN
I	5.22 MAX	0.205 MAX
J	5.72 MAX	0.225 MAX
K	15.24	0.6
L	13.2	0.52
M	$0.25^{+0.10}_{-0.05}$	$0.01^{+0.004}_{-0.0019}$



μPD2316ED (Ceramic)

ITEM	MILLIMETERS	INCHES
A	32.5 MAX	1.28 MAX
B	2.28	0.09
C	2.54	0.1
D	0.5 ± 0.1	0.02 ± 0.004
E	27.94	1.1
F	1.20 MIN	0.047 MIN
G	3.2 MIN	0.126 MIN
H	1.0 MIN	0.04 MIN
I	4.2 MAX	0.165 MAX
J	5.2 MAX	0.205 MAX
K	15.24	0.6
L	13.9	0.55
M	0.30 ± 0.1	0.012 ± 0.004

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FULLY DECODED 32,768 BIT MASK PROGRAMMABLE READ ONLY MEMORY

DESCRIPTION

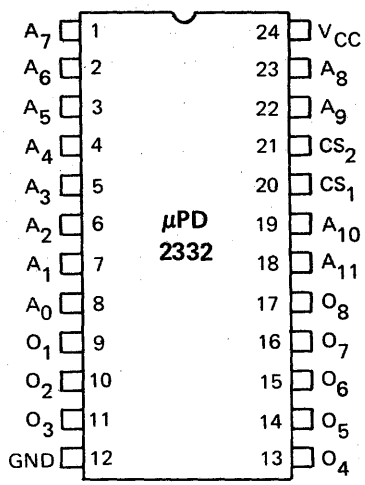
The NEC μPD2332 is a Fully Decoded 32,768 Bit Mask Programmable Read-Only Memory organized as 4,096 Words by 8 Bits. The μPD2332 has two chip select inputs and the combination of "High"/"Low" levels of these inputs is mask-programmable.

The μPD2332 is fabricated with sophisticated N-channel MOS technology and features high speed and TTL compatibility for simple interface with bipolar circuits.

FEATURES

- 4096 Words x 8 Bits Organization
- Directly TTL Compatible – All Inputs and Outputs
- Fully Static (No Clock or Refresh Required)
- Single +5V Power Supply
- High Speed – Access Time 450 ns Max.
- Three-State Output – OR-Tie Capability
- Two Programmable Chip Select Inputs for Easy Memory Expansion
- N-Channel MOS Technology
- Pin Compatible with TI TMS4732
- 24 Pin Plastic or Ceramic Dual-in-Line Package

PIN CONFIGURATION



PIN NAMES

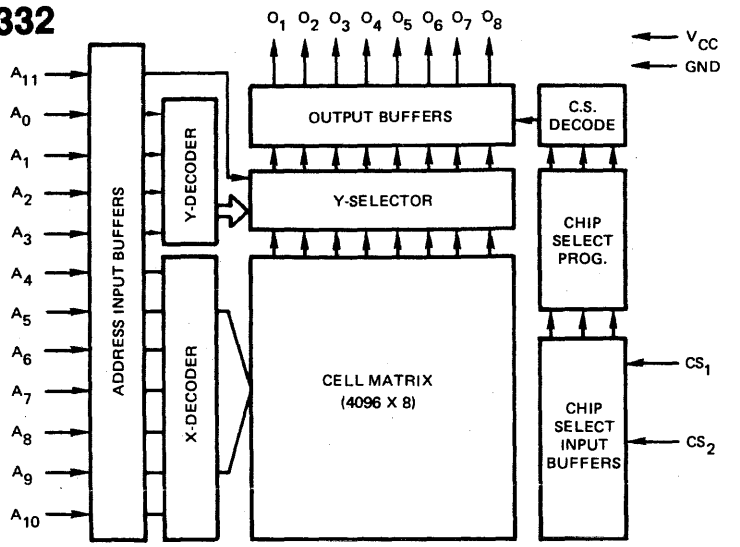
$A_0 - A_{11}$	Address Inputs
$O_1 - O_8$	Data Outputs
$CS_1 - CS_2$	Programmable Chip Select Inputs

When ordering the μPD2332, specify a chip select combination of CS_1 and CS_2 from the following.

CS_2	CS_1
0	0
0	1
1	0
1	1

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BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature . . . . . −10°C to +70°C
Storage Temperature . . . . . −65°C to +125°C
Supply Voltage On Any Pin . . . . . −0.5 to +7.0 Volts①

Note: ① With Respect to Ground

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

DC CHARACTERISTICS

T_a = −10°C to +70°C; V_{CC} = +5V ± 5% unless otherwise specified

PARAMETER	SYMBOL	LIMITS MIN.	LIMITS TYP.①	LIMITS MAX.	UNIT	TEST CONDITIONS
Input Load Current (All Input Pins)	I_{LI}			10	μA	
Output Leakage Current	I_{LOH}			+10	μA	CS = 2.2V (Deselected) V_{OUT} = V_{CC}
Output Leakage Current	I_{LOL}			−10	μA	CS = 2.2V (Deselected) V_{OUT} = 0V
Power Supply Current	I_{CC}		55	110	mA	All inputs 5.25V Data Out Open
Input "Low" Voltage	V_{IL}	−0.5		0.8	V	
Input "High" Voltage	V_{IH}	2.0		V_{CC} + 1.0V	V	
Output "Low" Voltage	V_{OL}			0.45	V	I_{OL} = 2.0 mA
Output "High" Voltage	V_{OH}	2.2			V	I_{OH} = −100 μA

Note: ① Typical Values for T_a = 25°C and nominal supply voltages.

CAPACITANCE

T_a = 25°C; f = 1 MHz

PARAMETER	SYMBOL	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNIT	TEST CONDITIONS
Input Capacitance	C_{IN}			10	pF	All Pins Except Pin Under Test Tied to AC Ground
Output Capacitance	C_{OUT}			15	pF	All Pins Except Pin Under Test Tied to AC Ground

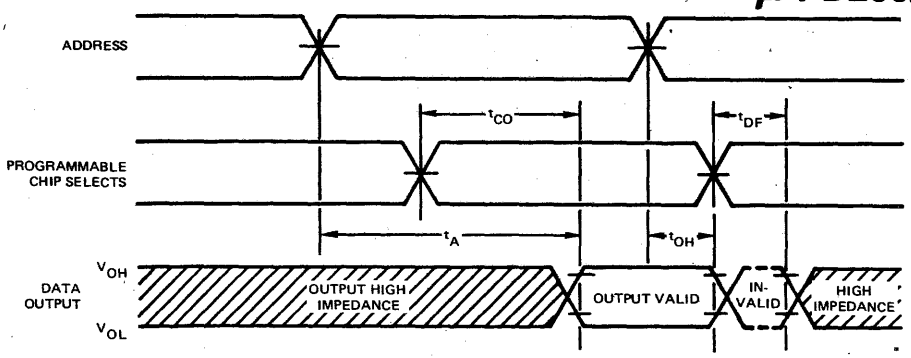
AC CHARACTERISTICS

T_a = −10°C to +70°C, V_{CC} = +5V ± 5% unless otherwise specified.

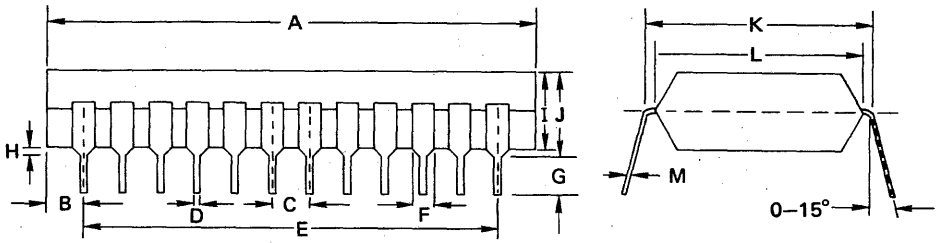
PARAMETER	SYMBOL	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNIT	TEST CONDITIONS
Address to Output Delay Time	t_A			450	ns	t_T = t_r = t_f = 20 ns
Chip Select to Output Enable Delay Time	t_{CO}			150	ns	C_L = 100 pF
Chip Deselect to Output Data Float Delay Time	t_{DF}	0		150	ns	Load = ITTL gate
Output Hold Time	t_{OH}	20			ns	V_{IN} = 0.8 to 2V V_{ref} Input = 1.5V V_{ref} Output = 0.45/2.2V

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TIMING WAVEFORMS

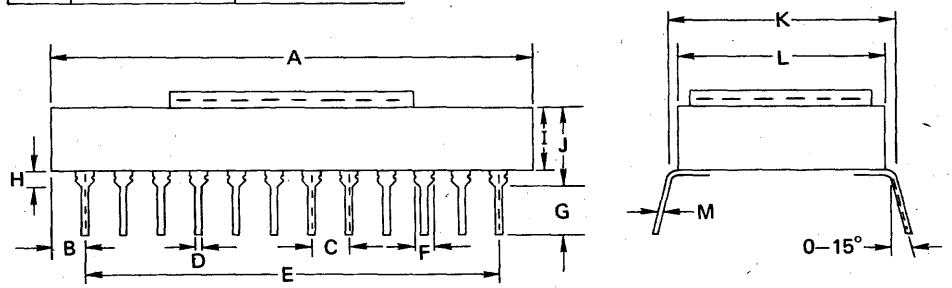


PACKAGE OUTLINE μPD2332C/D



μPD2332C (Plastic)

ITEM	MILLIMETERS	INCHES
A	33 MAX	1.3 MAX
B	2.53	0.1
C	2.54	0.1
D	0.5 ± 0.1	0.02 ± 0.004
E	27.94	1.1
F	1.5	0.059
G	2.54 MIN	0.1 MIN
H	0.5 MIN	0.02 MIN
I	5.22 MAX	0.205 MAX
J	5.72 MAX	0.225 MAX
K	15.24	0.6
L	13.2	0.52
M	$0.25^{+0.10}_{-0.05}$	$0.01^{+0.004}_{-0.0019}$



μPD2332D (Ceramic)

ITEM	MILLIMETERS	INCHES
A	32.5 MAX	1.28 MAX
B	2.28	0.09
C	2.54	0.1
D	0.5 ± 0.1	0.02 ± 0.004
E	27.94	1.1
F	1.20 MIN	0.047 MIN
G	3.2 MIN	0.126 MIN
H	1.0 MIN	0.04 MIN
I	4.2 MAX	0.165 MAX
J	5.2 MAX	0.205 MAX
K	15.24	0.6
L	13.9	0.55
M	0.30 ± 0.1	0.012 ± 0.004

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FULLY DECODED 65,536 BIT MASK PROGRAMMABLE READ ONLY MEMORY

DESCRIPTION

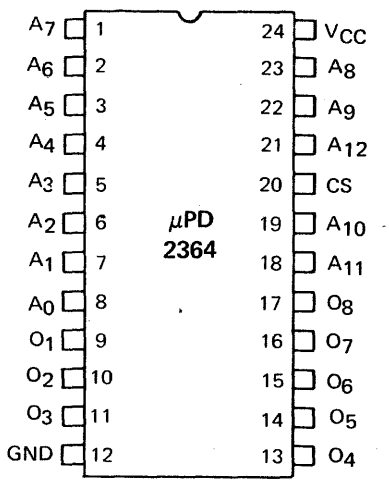
The NEC μPD2364 is a high speed 65,536 bit mask programmable Read Only Memory organized as 8,192 words by 8 bits. The μPD2364 is fabricated with N-channel MOS technology.

The inputs and outputs are fully TTL compatible. This device operates with a single +5V power supply. The chip select input is programmable. Any of active high or low level chip select input can be defined and desired chip select code is fixed during the masking process.

FEATURES

- 8,192 Words x 8 Bits Organization
- Directly TTL Compatible — All Inputs and Outputs
- Single +5V Power Supply
- High Speed — Access Time 450 ns Max.
- Three-State Output — OR-Tie Capability
- One Programmable Chip Select Input for Easy Memory Expansion
- On-Chip Address Fully Decoded
- All Inputs Protected Against Static Charge
- Pin Compatible with MK36000
- Available in 24 Pin Ceramic Dual-in-Line Package

PIN CONFIGURATION

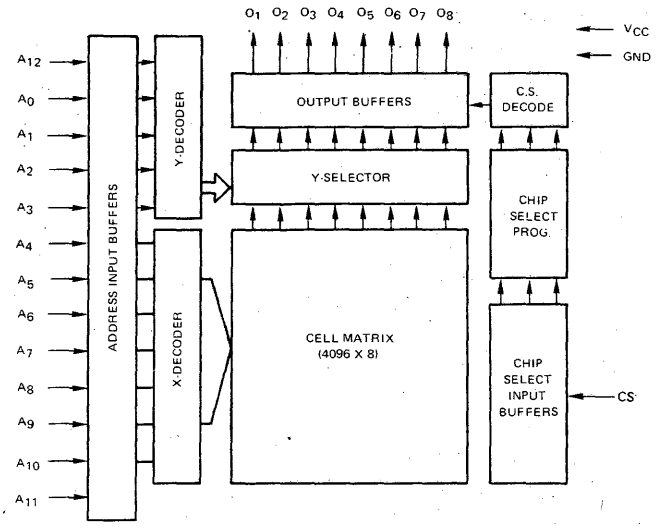


PIN NAMES

$A_0 - A_{12}$	Address Inputs
$O_1 - O_8$	Data Outputs
CS	Programmable Chip Select Input

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BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature . . . . . −10°C to +70°C
Storage Temperature . . . . . −65°C to +125°C
Supply Voltage On Any Pin . . . . . −0.5 to +7.0 Volts ①

Note: ① With Respect to Ground.

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

DC CHARACTERISTICS

T_a = −10°C to +70°C; V_{CC} = +5V ± 5% unless otherwise specified.

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP ①	LIMITS MAX	UNIT	TEST CONDITIONS
Input Load Current (All Input Pins)	I_{LI}			+10	μA	$V_{IN} = V_{CC}$
				−10	μA	V_{IN} = 0V
Output Leakage Current	I_{LOH}			+10	μA	Chip Deselected, $V_O = V_{CC}$
Output Leakage Current	I_{LOL}			−10	μA	Chip Deselected, V_O = 0V
Power Supply Current	I_{CC}			160	mA	
Input "Low" Voltage	V_{IL}	−0.5		0.8	V	
Input "High" Voltage	V_{IH}	2.0		V_{CC} + 1.0	V	
Output "Low" Voltage	V_{OL}			0.45	V	I_{OL} = 2.0 mA
Output "High" Voltage	V_{OH}	2.2			V	I_{OH} = −100 μA

Note: ① Typical Values for T_a = 25°C and nominal supply voltages.

CAPACITANCE

T_a = 25°C; f = 1 MHz

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input Capacitance	C_{IN}			10	pF	All Pins Except Pin Under Test Tied to AC Ground
Output Capacitance	C_{OUT}			15	pF	All Pins Except Pin Under Test Tied to AC Ground

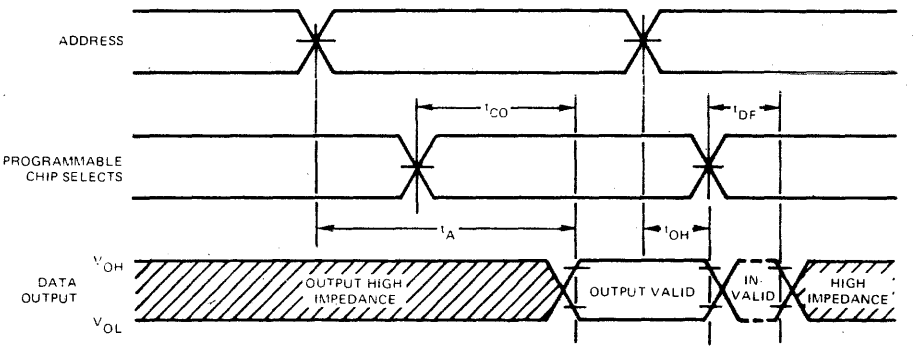
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AC CHARACTERISTICS

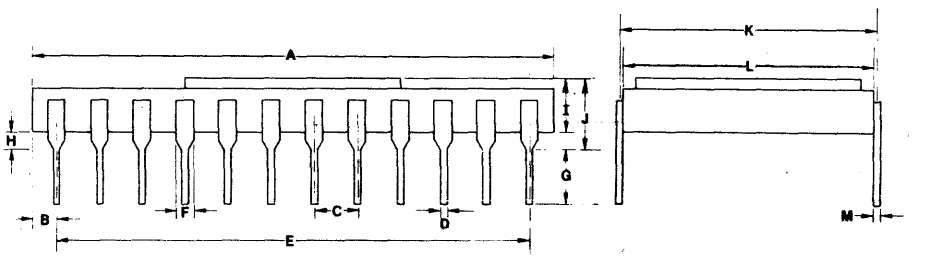
$T_a = -10°C$ to $+70°C$, $V_{CC} = +5V \pm 5\%$ unless otherwise specified.

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Address to Output Delay Time	t_A			450	ns	$t_T = t_r = t_f = 20$ ns
Chip Select to Output Enable Delay Time	t_{CO}			150	ns	$C_L = 100$ pF
Chip Deselect to Output Data Float Delay Time	t_{DF}	0		150	ns	Load = ITTL gate
Output Hold Time	t_{OH}	20			ns	$V_{IN} = 0.8$ to 2V V_{ref} Input = 1.5V V_{ref} Output = 0.8 to 2.0V

TIMING WAVEFORMS



PACKAGE OUTLINE μPD2364D



ITEM	MILLIMETERS	INCHES
A	30.78 Max	1.21 Max
B	1.42	0.06
C	2.54	0.10
D	0.46 ± 0.8	0.018 ± 0.03
E	27.94	1.10
F	1.02	0.04
G	3.2 Min	0.13 Min
H	1.02	0.04
I	3.23	0.13
J	4.25 Max	0.17 Max
K	15.24	0.60
L	14.93	0.59
M	0.25 ± 0.05	0.010 ± 0.002

SP2364-9-78-GY-CAT

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65,536 BIT CCD MEMORY

DESCRIPTION

The μPD3064 is a high speed, dynamic, 65,536 bit Charge Coupled Device (CCD) memory. It is organized as 65,536 x 1 in 16 addressable blocks of 4096 bits each. Operating clock frequency is from 1 MHz to 5 MHz.

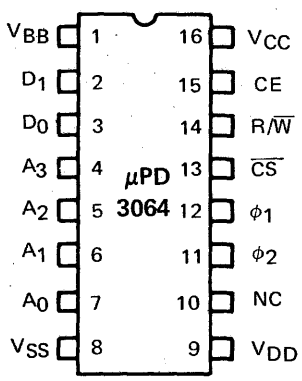
With the exception of the two clocks and chip enable, all inputs are TTL compatible. The use of only two clocks simplifies system design.

The μPD3064 is packaged in a standard, 16 pin dual-in-line with 400-mil centers.

FEATURES

- High Speed: Latency Time at 5 MHz (max) – 820 μs
  Read or Write Cycle (min) – 200 ns
  Read, Modify, Write Cycle (min) – 300 ns
- Fully TTL Compatible Except ϕ_1, ϕ_2, and CE
- Low Power Operation: 260 mW Operating (Typical at 5 MHz)
  25 mW Recirculating (Typical at 1 MHz)
  <1 mW Standby (Typical)
- Two-Phase CCD Clocks

PIN CONFIGURATION



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ABBREVIATIONS OF COMPANY NAMES

AD	Analog Devices
AMD	Advanced Micro Devices
AMI	American Microsystems, Inc.
Amperex	Amperex Electronics Corp.
Analogic	Analogic Corp.
Beckman	Beckman Instruments, Helipot Division
BEI	BEI Electronics
Burr-Brown	Burr-Brown Research
Cermetek	Cermetek
Cherry	Cherry Semiconductor
CMA	Consumer Microcircuits of America
Cybernetic	Cybernetic Micro Systems
Data General	Data General
Datel	Datel Systems
DDC	Data Devices Corp.
Delco	Delco Electronics
Dionics	Dionics Inc.
EA	Electronic Arrays
EMM/Semi	EMM Semi, Div. of Electronic Memories & Magnetics
Essex	Essex International
Exar	Exar Integrated Systems
Fairchild	Fairchild
Ferranti	Ferranti Electric
Fujitsu	Fujitsu
GI	General Instrument
Harris	Harris Semiconductor
Hitachi	Hitachi America Ltd.
Holt	Holt Inc.
Hughes	Hughes Aircraft Solid State Products
Hybrid Sys	Hybrid Systems
HyComp	HyComp
IMI	International Microcircuits, Inc.
Intech/FMI	Intech/Function Modules Inc.
Intel	Intel
Interdesign	Interdesign
Intersil	Intersil
IPI	Integrated Photomatrix, Inc.
Lambda	Lambda Electronics
LSI	LSI Computer Systems
Maruman	Maruman Integrated Circuits
Master Logic	Master Logic
Matrox	Matrox Electronics Systems
Micro Net	Micro Networks
Micropac	Micropac Industries
Micro Power	Micro Power Systems
Micro Tech	Microcircuits Technology
Mitel	Mitel Semiconductor
Mitsubishi	Mitsubishi Electric Co.
MMI	Monolithic Memories, Inc.
Monosil	Monosil
MOS	MOS Technology
Mostek	Mostek
Motorola	Motorola Semiconductor
National	National Semiconductor
NCR	NCR Corp., Microelectronics Division
NEC America	NEC America
NEC Micro	NEC Microcomputers
Nitron	Nitron
Nortec	Nortec Electronics
Novonics	Novonics
NPC	Nucleonic Products Co.
OEI	Optical Electronics, Inc.
OKI	OKI Semiconductor
Panasonic	Panasonic, Matsushita Electric Corp.
Photo Therm	Photo Therm
Plessey	Plessey Semiconductors
PMI	Precision Monolithics, Inc.
Raytheon	Raytheon Semiconductor
RCA	RCA Solid State Division
Reticon	Reticon
RIFA	RIFA
Rockwell	Rockwell Microelectronic Devices
RTC	Real Time Corp.
Sanken	Sanken Electric
Sanyo	Sanyo Electric
SGS	SGS-Ates Semiconductor
Siemens	Siemens
Signetics	Signetics (Philips)
Silicon G	Silicon General
Siliconix	Siliconix
Silicon Sys.	Silicon Systems, Inc.
Silitronics	Silitronics
SMC	Standard Microsystems
Solitron	Solitron Devices
Sprague	Sprague Electric Company
Supertex	Supertex, Inc.
SSM	Solid State Microtechnology for Music
SSS	Solid State Scientific
Synertek	Synertek
Telaris	Telaris
Teledyne C	Teledyne Crystalonics
Teledyne P	Teledyne Philbrick
Teledyne S	Teledyne Semiconductor
Telefunken	AEG-Telefunken
TI	Texas Instruments
TMX	TMX
Toshiba	Toshiba
Trans-Data	Trans-Data
TRW	TRW
Unitrode	Unitrode
Western	Western Digital
Zilog	Zilog

Field-Programmable Read-Only Memories

29000 Series

DESCRIPTION

Raytheon's 29000 Series of Field-Programmable Read-Only Memories includes most of the popular PROM configurations in both standard and power-switched versions. The power-switched devices (SPROMs) were originated by Raytheon to reduce overall power dissipation in large PROM arrays. This technique takes advantage of the non-volatile nature of PROMs by removing power when a particular device is not being used in the system. Unlike previous power-switching schemes, which employed external transistors and resistors, the SPROM includes all power-switching circuitry on the same chip as the memory. Moreover, the power-switch is activated by the same Chip Select (CS) input that is used to address a standard PROM; thus, in most cases, SPROMs can be directly substituted for standard devices without system redesign.

All Raytheon 29000 Series PROMs and SPROMs are manufactured with nichrome fuses and Low-Power Schottky technology. The devices are shipped with all bits in the HIGH (logical ONE) state. To achieve a LOW state in a given bit position, the nichrome link is fused open by passing a short, high-current pulse through the link. All 29000 Series devices are programmed using the same programming technique. (See page 3.)

FEATURES

- Low-Power Schottky technology
- Highly reliable nichrome fuses
- Three-state and open-collector versions
- PROM and SPROM versions of most configurations
- Typical SPROM "OFF" power is 25% of standard power
- SPROMs feature guaranteed access times and full V_{CC} tolerance under power-switched conditions
- All devices use same programming techniques (generic)
- All devices available in both commercial (0 to 75°C) and military (-55 to +125°C) versions
- All devices are industry standard pin-out

ORDERING INFORMATION

Configuration (Words x Bits)	Package (No. of Pins)	Output	Part Numbers			
			PROMs		SPROMs	
			0 to +75°C DIP	-55 to +125°C DIP	0 to +75°C DIP	-55 to +125°C DIP
256 x 4	16	OC	29660DC	29660DM	29662DC	29662DM
		TS	29661DC	29661DM	29663DC	29663DM
256 x 8	20	OC	29600DC	29600DM	29602DC	29602DM
		TS	29601DC	29601DM	29603DC	29603DM
512 x 4	16	OC	29610DC	29610DM	29612DC	29612DM
		TS	29611DC	29611DM	29613DC	29613DM
512 x 8	20	OC	29620DC	29620DM	29622DC	29622DM
		TS	29621DC	29621DM	29623DC	29623DM
	24	OC	29624DC	29624DM	29626DC	29626DM
		TS	29625DC	29625DM	29627DC	29627DM
1024 x 8	24	OC	29630DC	29630DM	29632DC	29632DM
		TS	29631DC	29631DM	29633DC	29633DM
	24	OC	29634DC	29634DM	29636DC	29636DM
		TS	29635DC	29635DM	29637DC	29637DM

Note: For 883B processing, add the letter "B" to the basic part number, e.g., 29660DMB.

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MAXIMUM RATINGS (Above which the useful life may be impaired)

Storage temperature . . . . . -65 to +150°C
Temperature (ambient) under bias . . . -55 to +125°C
Supply voltage to ground potential (continuous) . . . . . -0.5 to +7V
DC voltage applied to outputs (except during programming) . . -0.5V to +V_{CC} max
DC input voltage (address inputs) . . . -0.5 to +5.5V
DC voltage applied to outputs during programming 26V
Output current into outputs during programming . . . . . 125 mA
DC input voltage (chip select input - pin) . -0.5 to +33V
DC input current . . . . . -30 to +5 mA

OPERATING RANGE

29000XC	T_A = 0 to +75°C	V_{CC} = 5.0V ±5%	Commercial
29000XM	T_A = -55 to +125°C	V_{CC} = 5.0V ±10%	Military

COMMON ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE (unless otherwise noted)

Parameter	Description	Test Conditions		Min.	Typ.	Max.	Units
V_{OH} (tri-state only)	Output HIGH voltage	V_{CC} = MIN, I_{OH} = 2.0 mA V_{IN} = V_{IH} or V_{IL}		2.4			Volts
V_{OL}	Output LOW voltage	V_{CC} = MIN V_{IN} = V_{IH} or V_{IL}	I_{OL} = 8 mA			0.4	Volts
			I_{OL} = 16 mA			0.5	
V_{IH}	Input HIGH level	Guaranteed input logical HIGH voltage for all inputs		2.0			Volts
V_{IL}	Input LOW level	Guaranteed input logical LOW voltage for all inputs				0.8	Volts
I_{IL}	Input LOW current	V_{CC} = MAX, V_{IN} = 0.4V			-60	-250	μA
I_I	Input HIGH current	V_{CC} = MAX, V_{IN} = 2.7V				10	μA
I_I	Input HIGH current	V_{CC} = MAX, V_{IN} = 5.5V				1.0	mA
I_I (program pin only)	Input HIGH current	V_{CC} = MAX, V_{IN} = 4.5V				1.0	mA
I_{SC} (tri-state only)	Output short circuit current	V_{CC} = MAX, V_{OUT} = 0.0V		-12	-35	-85	mA
V_I	Input clamp voltage	V_{CC} = MIN, I_{IN} = 18 mA				-1.5	V
I_{CEX}	Output leakage current	V_{CC} = MAX V_{CS} = 2.4V	V_O = 4.5V			100	μA
			V_O = 2.4V			40	
			V_O = 0.4V			-40	

Note: 1. Typical limits are at V_{CC} = 5.0V and T_A = 25° C
2. Not more than one output should be shorted at a time. Duration of the short circuit should not be more than one second.

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AC TEST CONDITIONS

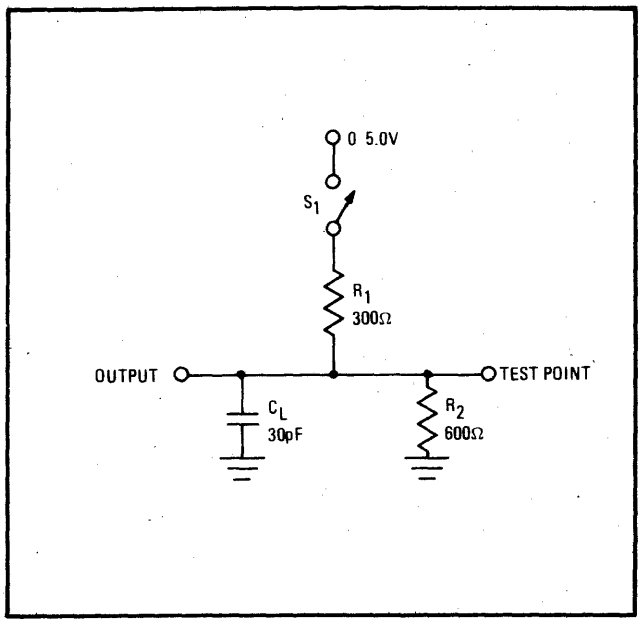


Figure 1. AC Test Circuit

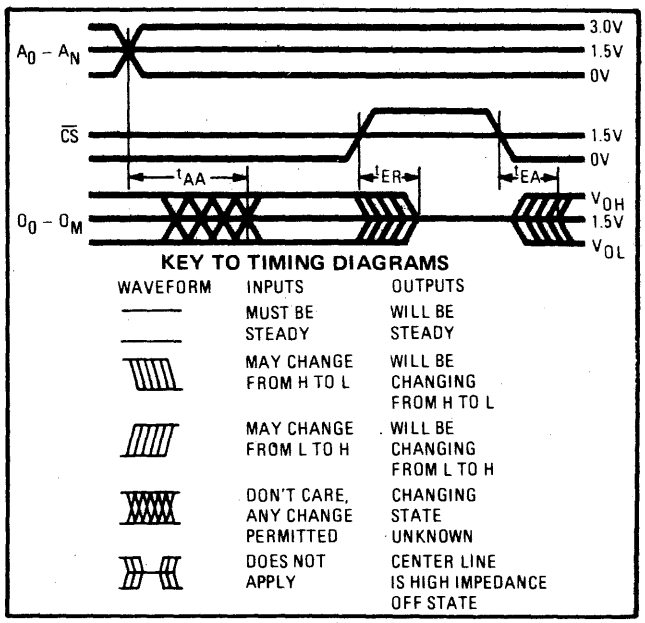


Figure 2. Switching Waveforms

PROGRAMMING INSTRUCTIONS

GENERAL

The device is manufactured with all outputs high in all storage locations. To make an output low at a particular word, a nichrome fusible link must be opened. This procedure is called programming.

PROGRAMMING DESCRIPTION

To select a particular link for programming, the word address is presented with TTL levels on A_0 through A_N, a V_{CC} of 5.50V is applied or left applied, and the program pin and the output to be programmed is taken to an elevated voltage to supply the required current to the fuse. The outputs must be programmed one at a time, since internal decoding circuitry is capable of sinking only one unit of programming current.

OTHER CHIP SELECT INPUTS

On some devices, additional Chip Select Inputs are present. These may be high, low or open during programming. When checking that an output is programmed (which is called verification) these inputs must be "on" to activate the device. Since they must be "on" during verification and the state is irrelevant during programming, the simplest procedure is to activate them during the entire procedure.

TIMING

The programming procedure involves the use of the program pin (a chip select) and the output pin. In order to guarantee that the output transistor is off before increasing the voltage on the output pin, the program pin's voltage pulse must come before the output pin's programming pulse and leave after the output pin's programming pulse. 100 ns delay is adequate. The programming pulse applied to the output pin and program pin must have a 50 to 70 microsecond rise time. See Figure 3.

It is recommended that only one programming pulse be applied for each bit to be programmed.

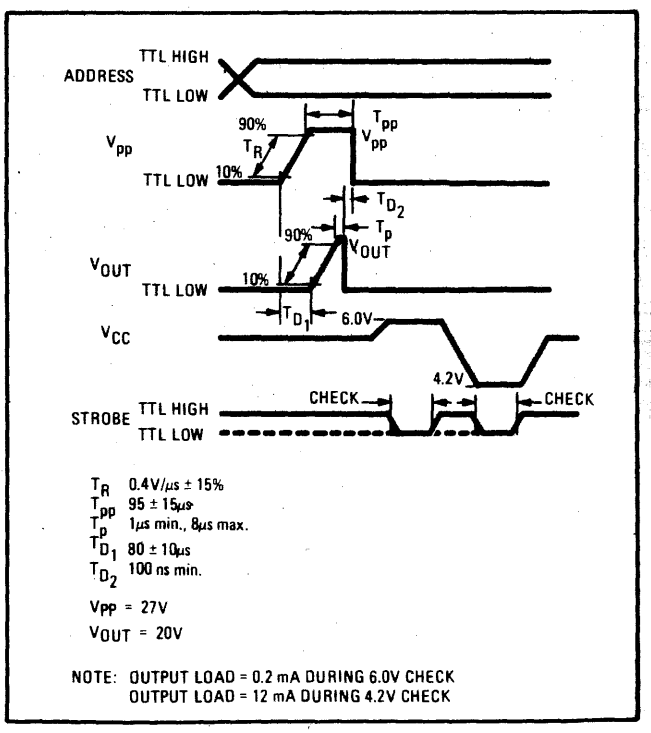


Figure 3. Programming Timing

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VERIFICATION

After programming a device, it can be checked for a low output by turning all chip selects on. To guarantee operation at minimum and maximum Vcc, current and temperature, the device must sink 12 mA at 4.20V Vcc and 20 mA at 6.0V Vcc at room temperature.

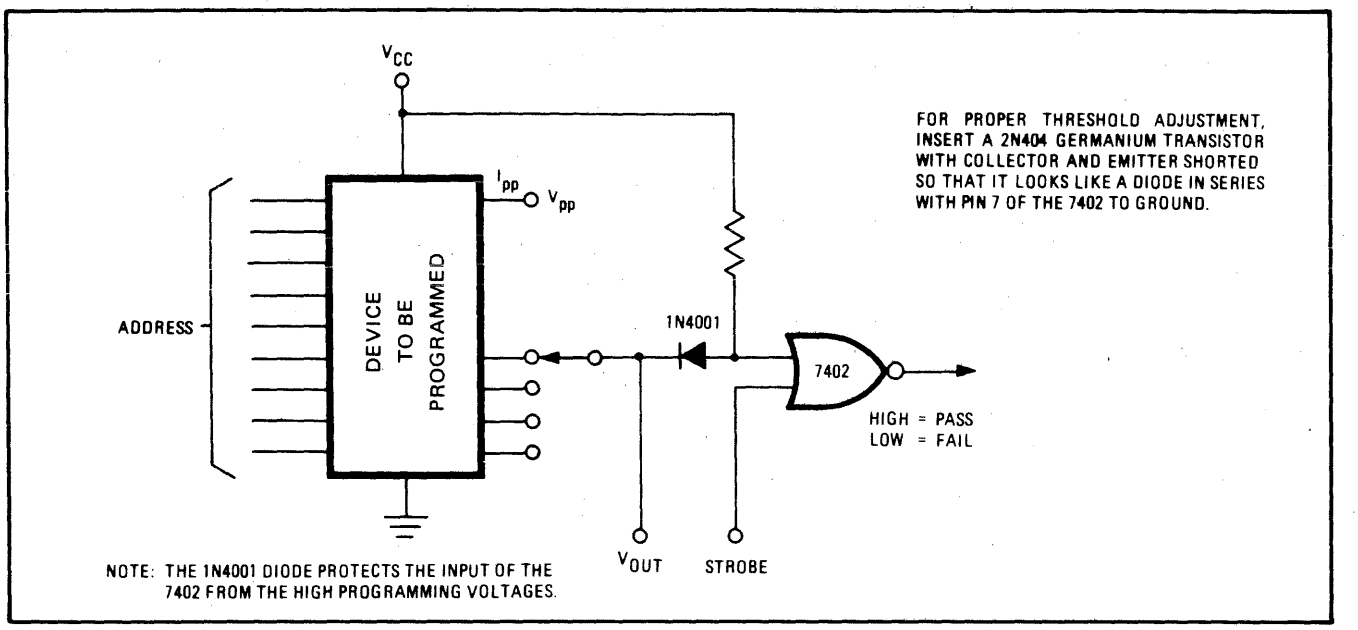


Figure 4. Suggested Implementation of the Verification Circuitry

BOARD PROGRAMMING

Units may be programmed at the board level by bringing the program pin of each package to the card connector. To program a particular package "A", the program pin of package A and one output of package A, which may or may not be "OR" tied to other packages, are taken to the required programming voltage. An alternate procedure is to tie the enable and outputs together as required by the system function and only apply V_{CC} to the device to be programmed. The number of units soldered on a board should be consistent with expected programming yields to avoid rework.

UNPROGRAMMABLE UNITS

Visual inspection at 200X prior to encapsulation, test fuses and decoding circuitry tests are used to guarantee a high programming yield of the device in the field. However, because of random defects, it is impossible to guarantee that a link will open without actually programming it. UNITS RETURNED TO RAYTHEON AS UNPROGRAMMABLE MUST BE ACCOMPANIED BY A COMPLETE DEVICE TRUTH TABLE WITH THE LOCATION WHICH COULD NOT BE PROGRAMMED, OR WHICH FALSELY PROGRAMMED, CLEARLY INDICATED.

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PROGRAMMING PARAMETERS — Do not test these limits or you may program the device

Parameter	Description	Test Conditions	Min.	Typ.	Max.	Units
I_{pp}	Current program pin during programming, before and after fuse has blown	V_{CC} = 5.50V V_{out} = 5.0V to 25V V_{pp} = 4.50V		0		mA
		V_{pp} = 27V		77		mA
I_{out}	Current into output during programming before the fuse has programmed	V_{pp} = 27V, V_{CC} = 5.50V V_{out} = 9.0V		0.1		mA
		V_{out} = 20V		16		mA
I_{out}	Current into output during programming after the fuse has programmed	V_{pp} = 27V V_{out} = 20V V_{CC} = 5.50V		0.1		mA
T_R	Rise time of program pulse applied to the data out or program pin		0.34	0.4	0.46	V/μs
V_{CCP}	V_{CC} required during programming		5.40	5.50	5.60	V
I_{OLV_1}	Output current required during verification	Both chip enables low T_A = 25°C, V_{CC} = 4.2V	11	12	13	mA
I_{OLV_2}	Output current required during verification	Both chip enables low	0.19	0.2	0.21	mA
MDC	Maximum duty cycle during automatic programming of program pin and output pin	$\frac{T_p}{T_C}$			25	%
V_{pp}	Required programming voltage on program pin		27	27	33	V
V_{out}	Required programming voltage on output pin		20	20	26	V
I_L	Required current limit of the power supply feeding the program pin and the output during programming	V_{pp} = 33V V_{out} = 26V V_{CC} = 5.50V	150			mA
T_{pp}	Required coincidence among the program pin, output, address and V_{CC} for programming		80	95	110	μs
T_{D_1}	Required time delay between disabling the memory output and application of the output programming pulse	Measure at 10% levels	70	80	90	μs
T_{D_2}	Required time delay between removal of programming pulse and enabling the memory output	Measure at 10% levels	100			ns

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TRUTH TABLES

Raytheon can program devices at our facility from Raytheon truth table forms (see page 8). For customers desiring to make their own forms, an example is shown below:

EXAMPLE FOR X8 DEVICES:

WORD NUMBER	PIN	OUTPUTS 14 O_8	13 O_7	12 O_6	11 O_5	9 O_4	8 O_3	7 O_2	6 O_1
0		H	H	H	L	H	L	L	L
1		L	H	L	H	H	H	H	L
.		.	.	.	.	.	.	.	.
.		.	.	.	.	.	.	.	.
Last		L	H	H	H	H	H	H	H

EXAMPLE FOR X4 DEVICES:

WORD NUMBER	PIN	OUTPUTS 9 O_4	10 O_3	11 O_2	12 O_1
0		H	H	H	L
1		L	H	L	H
.		.	.	.	.
.		.	.	.	.
Last		L	H	H	H

Note: A high voltage on the data out lines is signified by an "H". A low voltage on the data out lines is signified by an "L". The word number assumes positive logic on the address pins, so for example, word 511 = HHHHHHHHH.

PAPER TAPE FORMAT

Truth tables can also be sent to Raytheon in an ASCII tape format. Information can be sent to us by air mail or TWX 910-379-6481. The tape reading equipment at Raytheon only recognizes ASCII characters S, B, P, N, F, and E and interprets them as:

S	Start
B	Begin a word
P	High data
N	Low data
F	Finish a word
E	End of tape

All other characters such as carriage returns, line feeds, etc. are ignored so that comments and spaces may be sent in the data field to improve readability. Comments, however, should not use the characters S, B, P, N, F, and E. Word addresses must begin with zero and count sequentially to the highest address.

In order to assist the machine operator in determining where the heading information stops and the data field begins, 25 bell characters or rubout characters should precede the start of the truth table. Any type of 8 level tape (paper, mylar, fanfold, etc.) is acceptable. Channel 1 is the most significant bit and channel 8 (parity) is ignored. Sprocket holes are located between channels 3 and 4. Note that the order of the outputs between characters B and F is:

$$O_8, O_7, O_6, O_5, O_4, O_3, O_2, O_1$$

not

$$O_1, O_2, O_3, O_4, O_5, O_6, O_7, O_8$$

A typical list of characters and their machine interpretations are shown on page 7.

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PAPER TAPE FORMAT (Cont.)

The required heading information at the beginning of the tape is as follows:

Customer name and phone_____ Truth table number_____

Customer TWX number_____ Number of truth tables_____

Purchase order number_____ Total number of parts_____

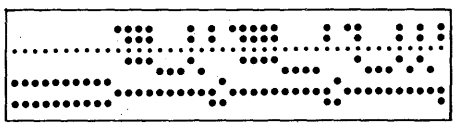
Raytheon part number_____ Number of parts of each truth table_____

Customer symbolized part number_____ 25 bell or rubout characters_____

EXAMPLE FOR X 4 DEVICES

BLARNEY ELECTRONICS 408-735-8140
TWX 911-338-9225
PO142
29662
0431
12
1
3
3

BNNNPF BNNNNF BNPNPF BNPPPF
BNNNNF BNPNPF BNNPPF BPPPNF



BEGIN DATA FIELD

DATA FIELD (H = HIGH VOLTAGE, L = LOW VOLTAGE)

FINISHED DATA FIELD

B P P N P F BPPPPF BPNNPF – etc – BPNNNF

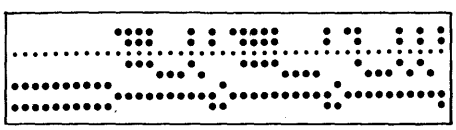
O_4 O_3 O_2 O_1

WORD 0 WORD 1 WORD 2 WORD N

EXAMPLE FOR X 8 DEVICES

BLARNEY ELECTRONICS 408-735-8140
TWX 911-338-9225
PO142
29601
etc.

BNNNPPPNPF BNNNNPPPPF BNPPPNPNF BNNNNNNNF
BNNNNNNNF BNNNPPPNPF BPPPPPPPPF BNPPNPNNNF



BEGIN DATA FIELD

DATA FIELD (H = HIGH VOLTAGE, L = LOW VOLTAGE)

FINISHED DATA FIELD

B P P P N P P N P F BPPPPPPPPF BPNPPPNNPF – etc – BPPNPPNNNF

O_8 O_7 O_6 O_5 O_4 O_3 O_2 O_1

WORD 0 WORD 1 WORD 2 WORD N

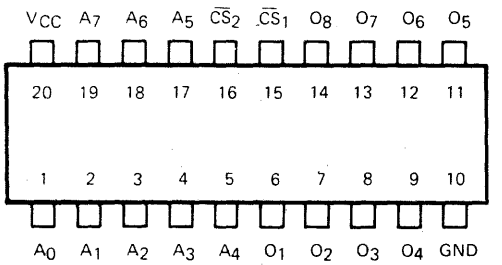
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POWER AND AC CHARACTERISTICS OVER OPERATING RANGE (Unless otherwise noted)

Parameter	Description	Test Conditions	Typical 5V 25°C	Maximum 25°C	Maximum Com'l	Maximum Mil	Units
I_{CC}	Power supply current		90	–	130	130	mA
t_{AA}	Address access time	CL = 30 pF RL = 300Ω to V_{CC} and 600Ω to GND (16 mA load) Note 1	50	70	75	90	ns
t_{EA}	Enable access time		20	35	40	50	ns
t_{ER}	Enable recovery time		20	35	40	50	ns

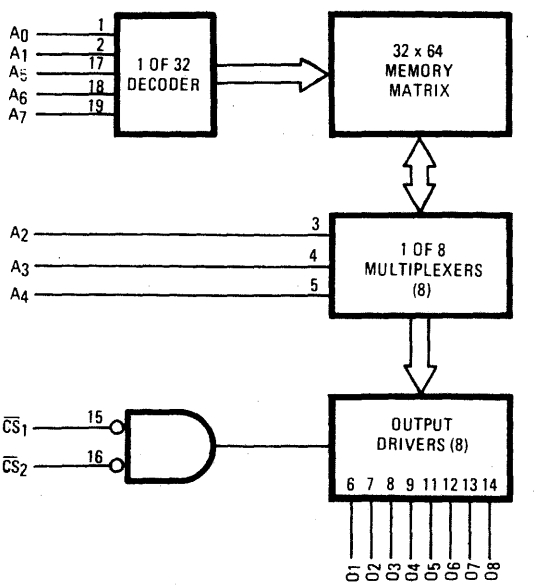
Note 1. 300Ω resistor opened for t_{EA} and t_{ER} measurements between HIGH and OFF states.

PIN OUT INFORMATION



Pin 15 is also the programming pin (pp).

BLOCK DIAGRAM



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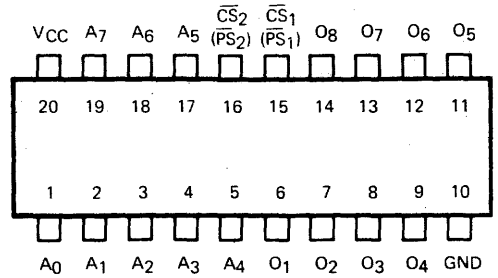
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POWER AND AC CHARACTERISTICS OVER OPERATING RANGE (Unless otherwise noted)

Parameter	Description	Test Conditions		Typical 5V 25°C	Maximum 25°C	Maximum Com'l	Maximum Mil	Units
I_{CC}	Power supply current	CS = 2.4V	29602	20		30	30	mA
			29603	30		45	45	mA
		CS = 0.4V		110		170	170	mA
t_{AA}	Address access time	CL = 30 pF RL = 300Ω to V_{CC} and 600Ω to GND (16 mA load) Note 1		40	55	60	75	ns
t_{EA}	Enable access time			40	55	60	75	ns
t_{ER}	Enable recovery time			15	25	30	40	ns

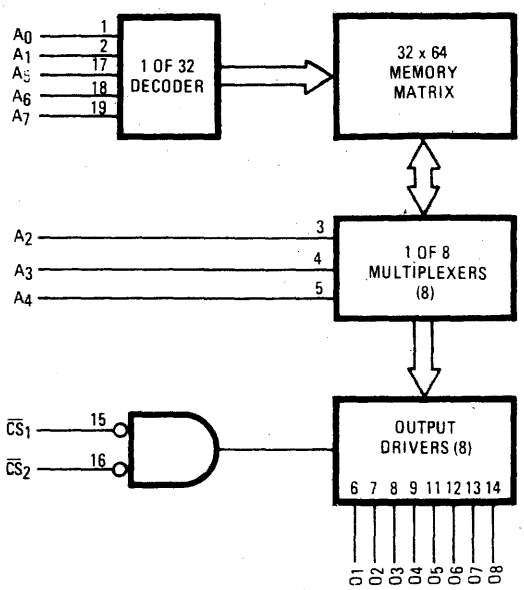
Note 1. 300Ω resistor opened for t_{EA} and t_{ER} measurements between HIGH and OFF states.

PIN OUT INFORMATION



Pin 15 is also the programming pin (pp).

BLOCK DIAGRAM



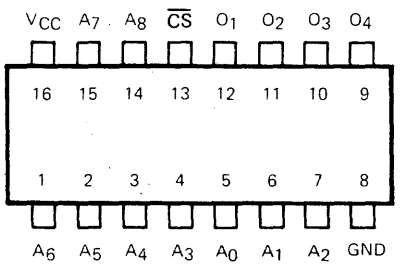
©IC MASTER 1979

POWER AND AC CHARACTERISTICS OVER OPERATING RANGE (Unless otherwise noted)

Parameter	Description	Test Conditions	Typical 5V 25°C	Maximum 25°C	Maximum Com'l	Maximum Mil	Units
I_{CC}	Power supply current		90	–	130	130	mA
t_{AA}	Address access time	CL = 30 pF RL = 300Ω to V_{CC} and 600Ω to GND (16 mA load) Note 1	30	50	55	70	ns
t_{EA}	Enable access time		15	25	30	40	ns
t_{ER}	Enable recovery time		15	25	30	40	ns

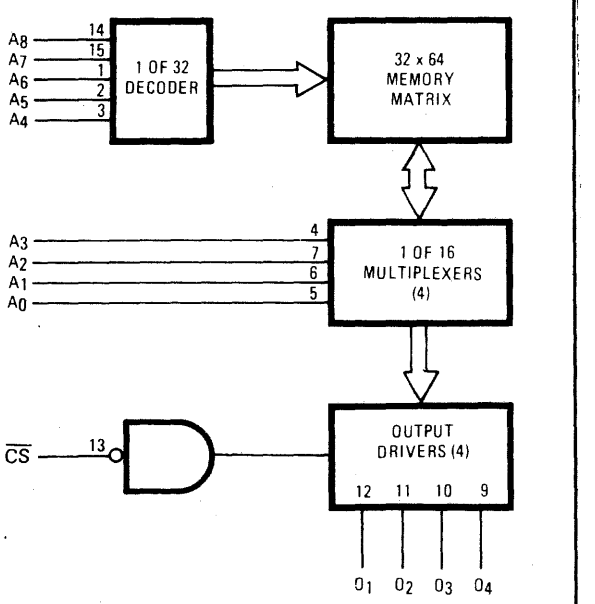
Note 1. 300Ω resistor opened for t_{EA} and t_{ER} measurements between HIGH and OFF states.

PIN OUT INFORMATION



Pin 13 is also the programming pin (pp).

BLOCK DIAGRAM



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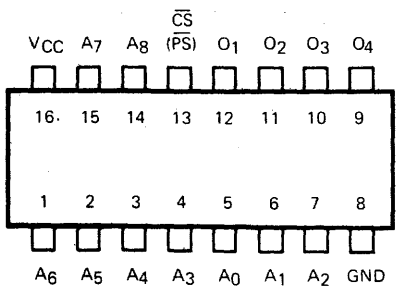
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POWER AND AC CHARACTERISTICS OVER OPERATING RANGE (Unless otherwise noted)

Parameter	Description	Test Conditions		Typical 5V 25°C	Maximum 25°C	Maximum Com'l	Maximum Mil	Units
I_{CC}	Power supply current	CS = 2.4V	29612	20		30	30	mA
			29613	30		45	45	mA
		CS = 0.4V		90		130	130	mA
t_{AA}	Address access time	CL = 30 pF RL = 300Ω to V_{CC} and 600Ω to GND (16 mA load) Note 1		35	55	60	75	ns
t_{EA}	Enable access time			40	55	60	75	ns
t_{ER}	Enable recovery time			15	25	30	40	ns

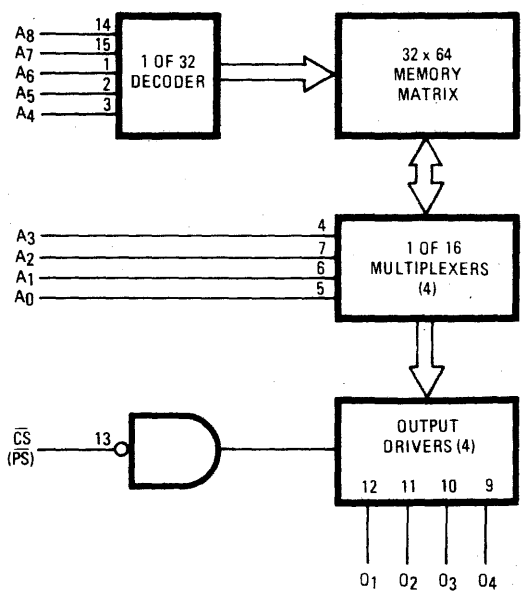
Note 1. 300Ω resistor opened for t_{EA} and t_{ER} measurements between HIGH and OFF states.

PIN OUT INFORMATION



Pin 13 is also the programming pin (pp).

BLOCK DIAGRAM



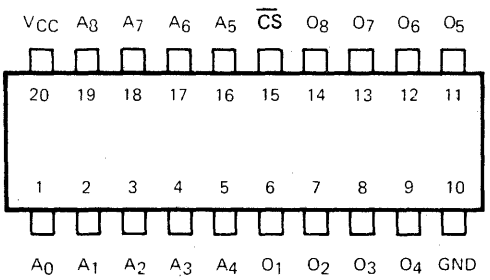
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POWER AND AC CHARACTERISTICS OVER OPERATING RANGE (Unless otherwise noted)

Parameter	Description	Test Conditions	Typical 5V 25°C	Maximum 25°C	Maximum Com'l	Maximum Mil	Units
I_{CC}	Power supply current		90	–	155	155	mA
t_{AA}	Address access time	CL = 30 pF RL = 300Ω to V_{CC} and 600Ω to GND (16 mA load) Note 1	50	60	65	80	ns
t_{EA}	Enable access time		20	25	30	40	ns
t_{ER}	Enable recovery time		20	25	30	40	ns

Note 1. 300Ω resistor opened for t_{EA} and t_{ER} measurements between HIGH and OFF states.

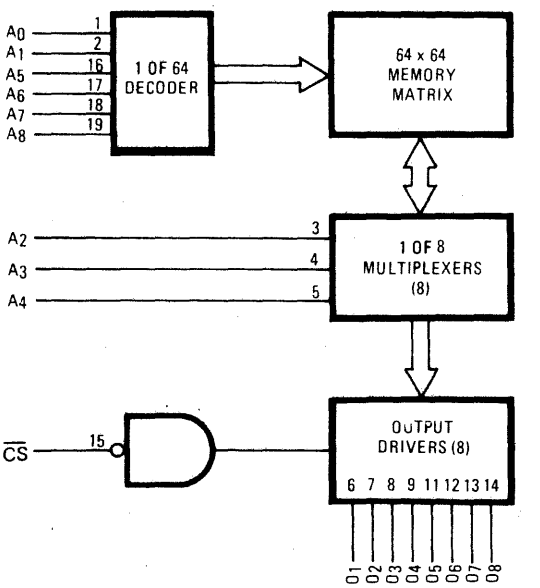
PIN OUT INFORMATION



Pin 15 is also the programming pin.

Pin 1 is marked for orientation.

BLOCK DIAGRAM



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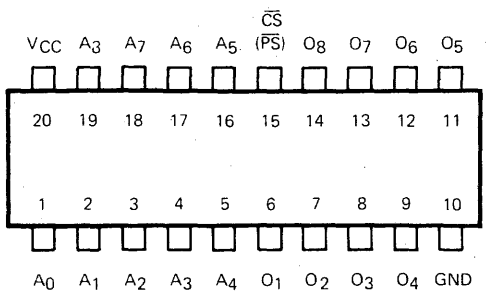
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POWER AND AC CHARACTERISTICS OVER OPERATING RANGE (Unless otherwise noted)

Parameter	Description	Test Conditions		Typical 5V 25°C	Maximum 25°C	Maximum Com'l	Maximum Mil	Units
I_{CC}	Power supply current	CS = 2.4V	29622	20	–	30	30	mA
			29623	30	–	45	45	mA
		CS = 0.4V		90	–	155	155	mA
t_{AA}	Address access time	CL = 30 pf RL = 300Ω to V_{CC} and 600Ω to GND (16 mA load) Note 1		55	65	70	85	ns
t_{EA}	Enable access time			55	65	70	85	ns
t_{ER}	Enable recovery time			20	25	30	40	ns

Note 1. 300Ω resistor opened for t_{EA} and t_{ER} measurements between HIGH and OFF states.

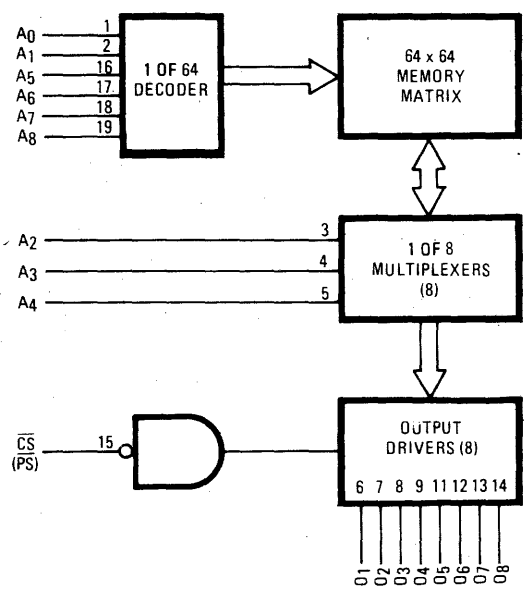
PIN OUT INFORMATION



Pin 15 is also the programming pin.

Pin 1 is marked or orientation.

BLOCK DIAGRAM



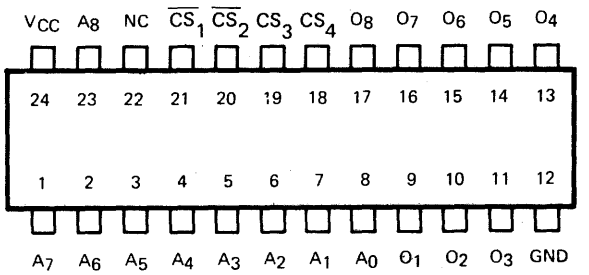
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POWER AND AC CHARACTERISTICS OVER OPERATING RANGE (Unless otherwise noted)

Parameter	Description	Test Conditions	Typical 5V 25°C	Maximum 25°C	Maximum Com'l	Maximum Mil	Units
I_{CC}	Power supply current		110	–	170	170	mA
t_{AA}	Address access time	CL = 30 pF RL = 300Ω to V_{CC} and 600Ω to GND (16 mA load) Note 1	35	55	60	75	ns
t_{EA}	Enable access time		20	25	30	40	ns
t_{ER}	Enable recovery time		15	20	25	35	ns

Note 1. 300Ω resistor opened for t_{EA} and t_{ER} measurements between HIGH and OFF states.

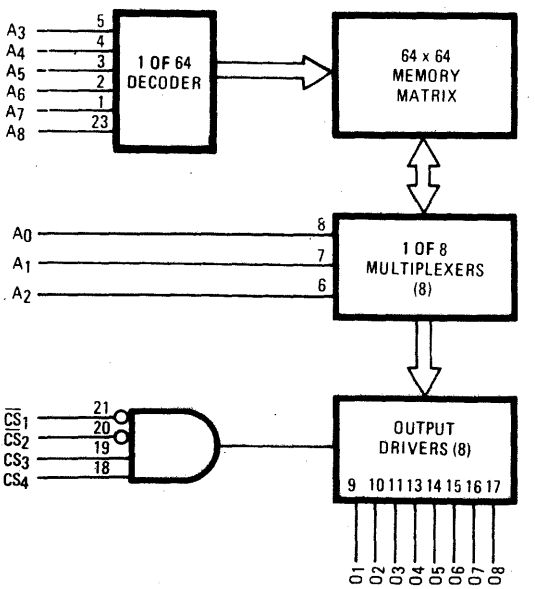
PIN OUT INFORMATION



Pin 20 is also the programming pin.

Pin 1 is marked for orientation.

BLOCK DIAGRAM



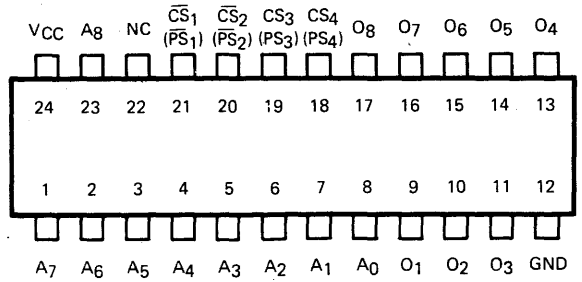
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POWER AND AC CHARACTERISTICS OVER OPERATING RANGE (Unless otherwise noted)

Parameter	Description	Test Conditions		Typical 5V 25°C	Maximum 25°C	Maximum Com'l	Maximum Mil	Units
I_{CC}	Power supply current	Disabled	29626	20	–	30	30	mA
			29627	30	–	45	45	mA
		Enabled		110	–	170	170	mA
t_{AA}	Address access time	CL = 30 pF RL = 300Ω to V_{CC} and 600Ω to GND (16 mA load) Note 1		40	60	65	80	ns
t_{EA}	Enable access time			40	60	65	80	ns
t_{ER}	Enable recovery time			15	20	25	35	ns

Note 1. 300Ω resistor opened for t_{EA} and t_{ER} measurements between HIGH and OFF states.

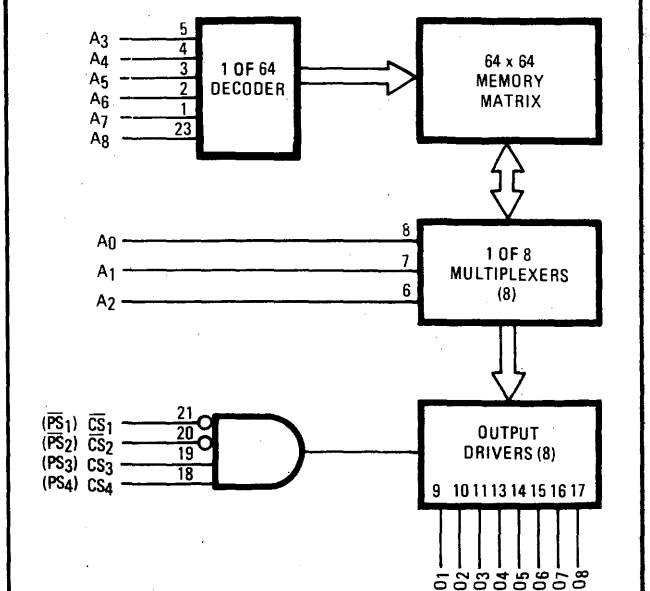
PIN OUT INFORMATION



Pin 20 is also the programming pin.

Pin 1 is marked for orientation.

BLOCK DIAGRAM



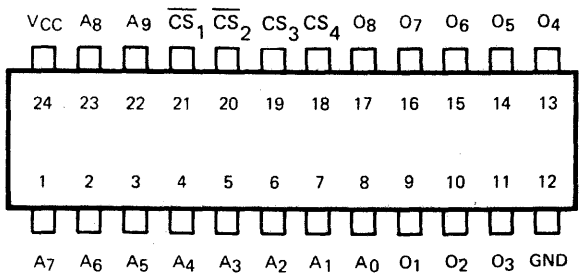
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POWER AND AC CHARACTERISTICS OVER OPERATING RANGE (Unless otherwise noted)

Parameter	Description	Test Conditions	Typical 5V 25°C	Maximum 25°C	Maximum Com'l	Maximum Mil	Units
I_{CC}	Power supply current		120	–	170	170	mA
t_{AA}	Address access time	C_L = 30 pF R_L = 300Ω to V_{CC} and 600Ω to GND (16 mA load) Note 1	45	65	70	90	ns
t_{EA}	Enable access time		20	30	35	45	ns
t_{ER}	Enable recovery time		15	25	30	40	ns

Note 1. 300Ω resistor opened for t_{EA} and t_{ER} measurements between HIGH and OFF states.

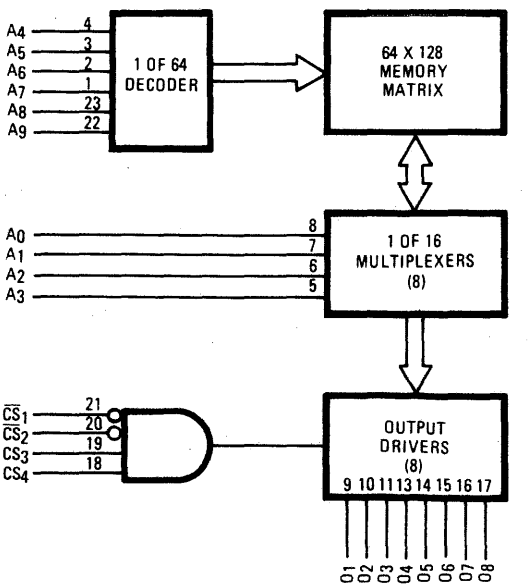
PIN OUT INFORMATION



Pin 20 is also the programming pin.

Pin 1 is marked for orientation.

BLOCK DIAGRAM



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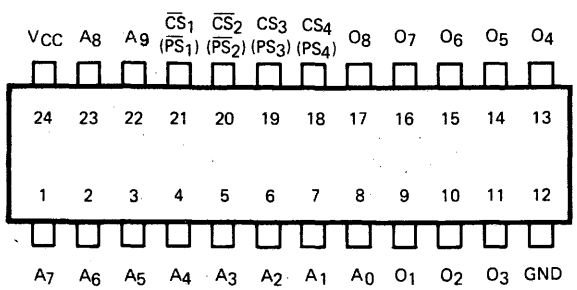
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POWER AND AC CHARACTERISTICS OVER OPERATING RANGE (Unless otherwise noted)

Parameter	Description	Test Conditions		Typical 5V 25°C	Maximum 25°C	Maximum Com'l	Maximum Mil	Units
I_{CC}	Power supply current	Disabled	29632	20	–	30	30	mA
			29633	30	–	45	45	mA
		Enabled		110	–	170	170	mA
t_{AA}	Address access time	CL = 30 pF RL = 300Ω to V_{CC} and 600Ω to GND (16 mA load) Note 1		50	70	75	95	ns
t_{EA}	Enable access time			50	70	75	95	ns
t_{ER}	Enable recovery time			15	25	30	40	ns

Note 1. 300Ω resistor opened for t_{EA} and t_{ER} measurements between HIGH and OFF states.

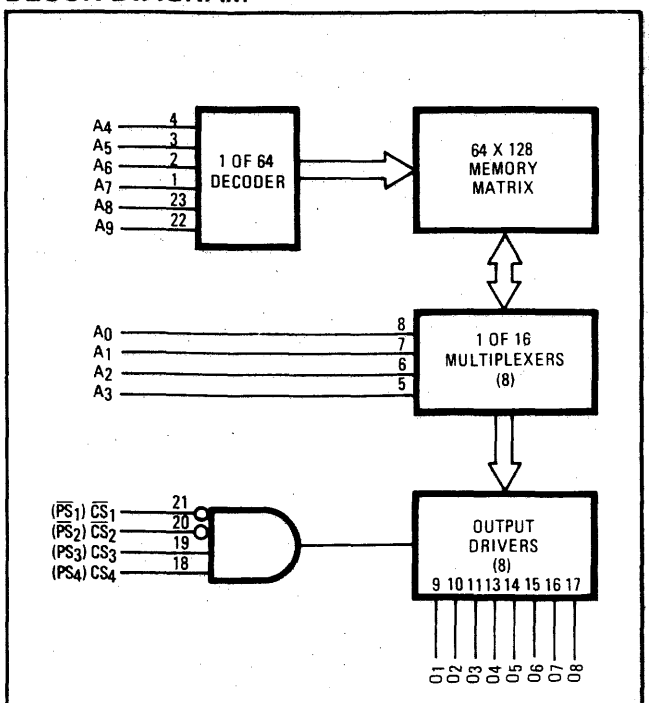
PIN OUT INFORMATION



Pin 20 is also the programming pin.

Pin 1 is marked for orientation.

BLOCK DIAGRAM



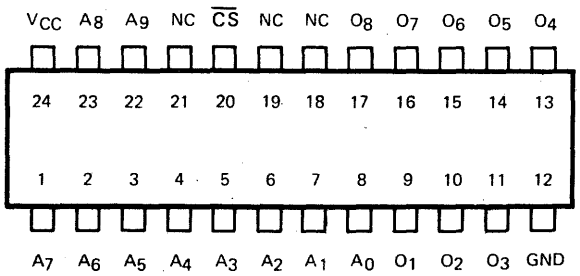
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POWER AND AC CHARACTERISTICS OVER OPERATING RANGE (Unless otherwise noted)

Parameter	Description	Test Conditions	Typical 5V 25°C	Maximum 25°C	Maximum Com'l	Maximum Mil	Units
I_{CC}	Power supply current		120	–	170	170	mA
t_{AA}	Address access time	CL = 30 pF RL = 300Ω to V_{CC} and 600Ω to GND (16 mA load) Note 1	45	65	70	90	ns
t_{EA}	Enable access time		20	30	35	45	ns
t_{ER}	Enable recovery time		15	25	30	40	ns

Note 1. 300Ω resistor opened for t_{EA} and t_{ER} measurements between HIGH and OFF states.

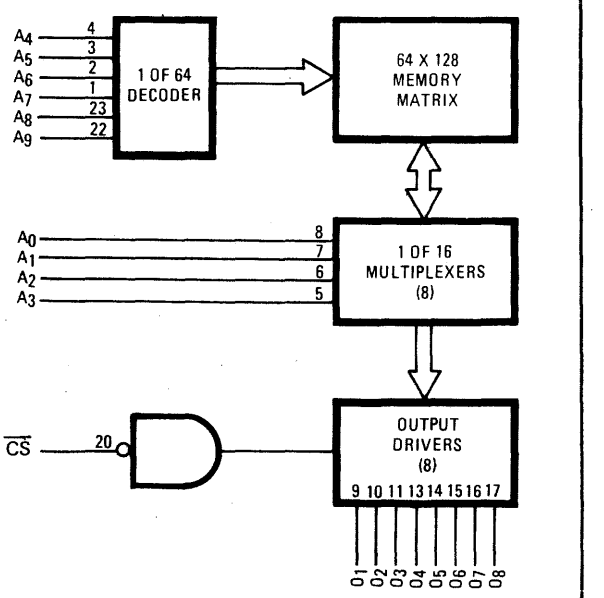
PIN OUT INFORMATION



Pin 20 is also the programming pin.

Pin 1 marked for orientation.

BLOCK DIAGRAM



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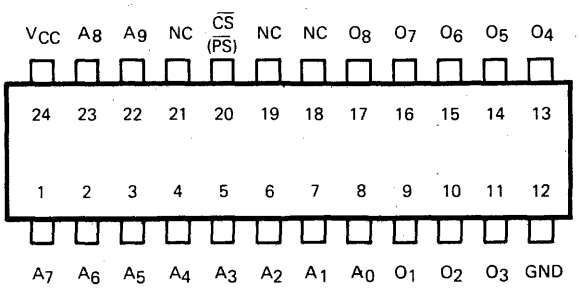
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POWER AND AC CHARACTERISTICS OVER OPERATING RANGE (Unless otherwise noted)

Parameter	Description	Test Conditions		Typical 5V 25°C	Maximum 25°C	Maximum Com'l	Maximum Mil	Units
I_{CC}	Power supply current	Disabled	29636	20	–	30	30	mA
			29637	30	–	45	45	mA
		Enabled		110	–	170	170	mA
t_{AA}	Address access time	CL = 30 pF RL = 300Ω to V_{CC} and 600Ω to GND (16 mA load) Note 1		50	70	75	95	ns
t_{EA}	Enable access time			50	70	75	95	ns
t_{ER}	Enable recovery time			15	25	30	40	ns

Note 1. 300Ω resistor opened for t_{EA} and t_{ER} measurements between HIGH and OFF states.

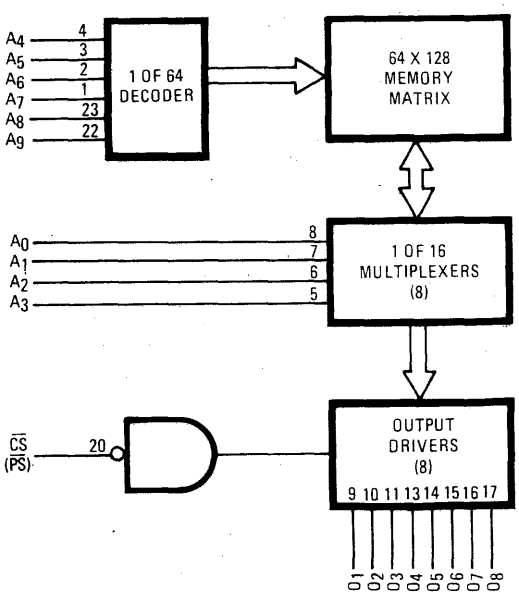
PIN OUT INFORMATION



Pin 20 is also the programming pin.

Pin 1 marked for orientation.

BLOCK DIAGRAM



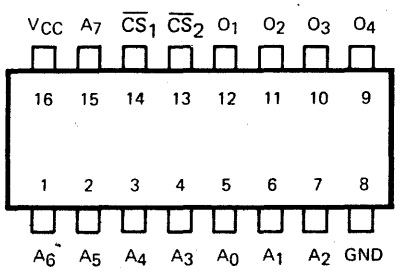
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POWER AND AC CHARACTERISTICS OVER OPERATING RANGE (Unless otherwise noted)

Parameter	Description	Test Conditions	Typical 5V 25°C	Maximum 25°C	Maximum Com'l	Maximum Mil	Units
I_{CC}	Power supply current		90	–	130	130	mA
t_{AA}	Address access time	CL = 30 pF RL = 300Ω to V_{CC} and 600Ω to GND (16 mA load) Note 1	45	60	70	80	ns
t_{EA}	Enable access time		20	30	35	40	ns
t_{ER}	Enable recovery time		20	30	35	40	ns

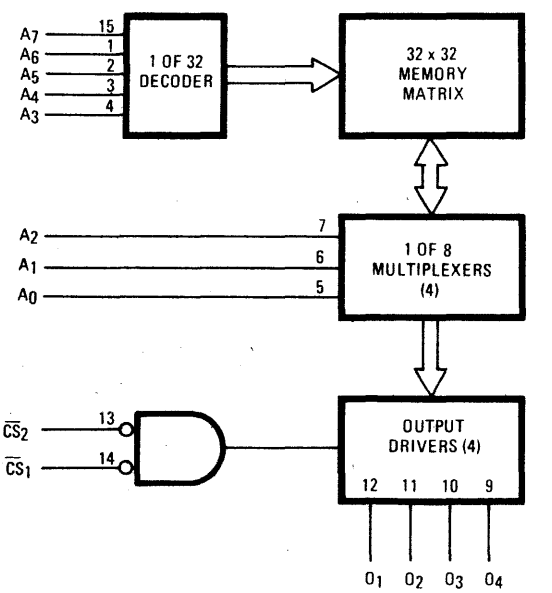
Note 1. 300Ω resistor opened for t_{EA} and t_{ER} measurements between HIGH and OFF states.

PIN OUT INFORMATION



Pin 13 is also the programming pin.
Pin 1 is marked for orientation.

BLOCK DIAGRAM



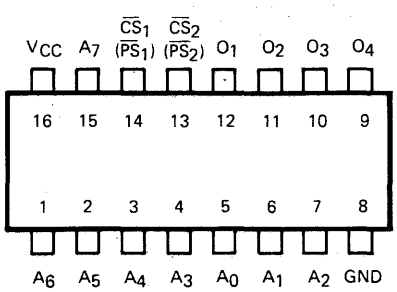
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POWER AND AC CHARACTERISTICS OVER OPERATING RANGE (Unless otherwise noted)

Parameter	Description	Test Conditions		Typical 5V 25°C	Maximum 25°C	Maximum Com'l	Maximum Mil	Units
I_{CC}	Power supply current	CS = 2.4V	29662	20	–	30	30	mA
			29663	30	–	45	45	mA
		CS = 0.4V		90	–	130	130	mA
t_{AA}	Address access time	CL = 30 pF RL = 300Ω to V_{CC} and 600Ω to GND (16 mA load) Note 1		35	55	60	75	ns
t_{EA}	Enable access time			40	55	60	75	ns
t_{ER}	Enable recovery time			15	25	30	40	ns

Note 1. 300Ω resistor opened for t_{EA} and t_{ER} measurements between HIGH and OFF states.

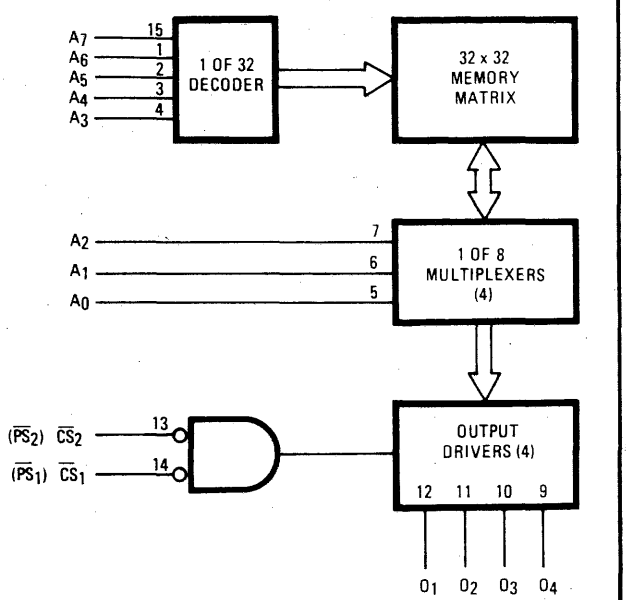
PIN OUT INFORMATION



Pin 13 is also the programming pin.

Pin 1 is marked for orientation.

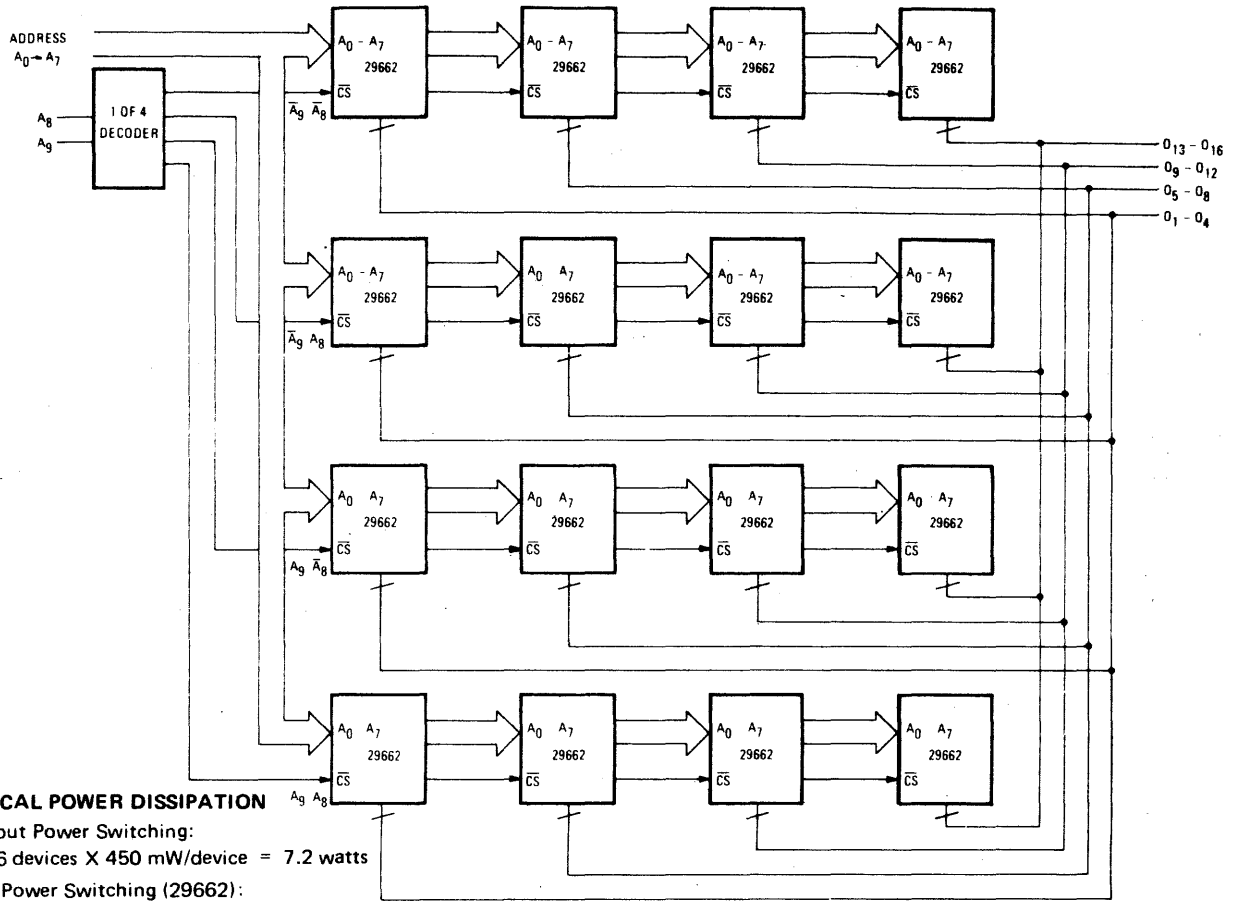
BLOCK DIAGRAM



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SPROM Applications

1024 x 16 BIT PROM ARRAY EXAMPLE USING 256 x 4 SPROMs



TYPICAL POWER DISSIPATION

Without Power Switching:

16 devices X 450 mW/device = 7.2 watts

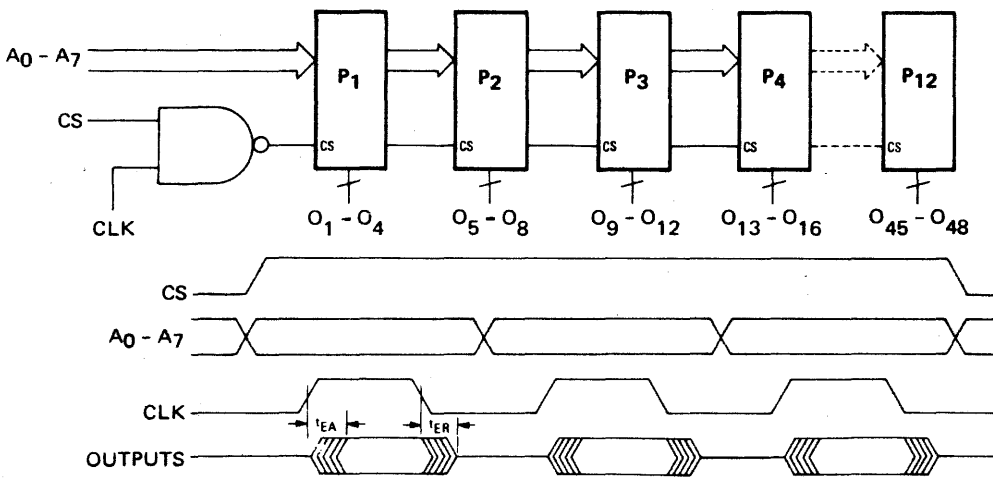
With Power Switching (29662):

4 devices X 450 mW/device = 1.8 watts

12 devices X 100 mW/device = 1.2 watts

Total Power = 3.0 watts

256 x 48 BIT CLOCKED PROM APPLICATIONS USING 256 x 4 SPROMs



TYPICAL POWER DISSIPATION

Without Power Switching:

12 devices X 450 mW/device = 5.4 watts

With Power Switching (29662 and 50% duty cycle clock):

(0.5 X 12 devices X 450 mW/device) + (0.5 X 12 devices X 100 mW/device) = 3.3 watts

With Power Switching (29662 and 20% duty cycle clock):

(0.2 X 12 devices X 450 mW/device) + (0.8 X 12 devices X 100 mW/device) = 2.04 watts

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"I need to know if this device exists, and if there are any alternate sources. Where do I start?"

- Memory IC
- RAM
- Static
- 1024x1
- CMOS
- 250 Nanoseconds
- 5 Volts

If you're spending hours to solve a problem similar to the one above, you're behind the times...



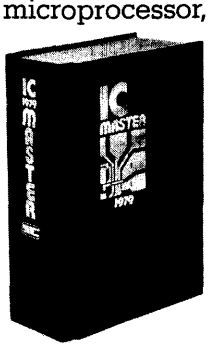
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You don't have to search through stacks of catalogs. Simply look up the specs and function you need. You don't need a part number to start with.

All you need is a problem to use The Master. Does the device exist? Who makes it? Is there an alternate source? What's the part number? Is there an applications note? Who is my closest distributor—etc.



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DESCRIPTION

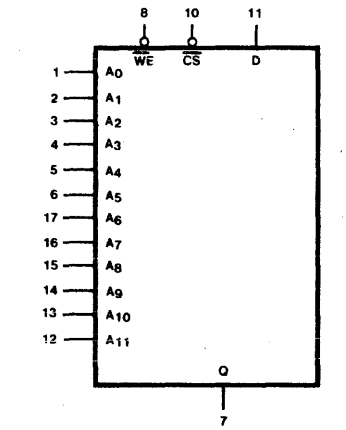
The Signetics 2613 is a high speed, 4096 bit static random access memory. Utilizing the Signetics n-channel, si-gate Mini-MOS technology to achieve high performance and high bit density, the 4096x1 organization offers a cost effective solution for designer needs.

The 2613 is fully static (access time=cycle time), all input and outputs are TTL compatible, and it has a single +5V supply. It is manufactured in the industry standard pinout 18 pin package.

FEATURES

- **Typical access time 80ns**
- **Power dissipation 0.1 mW/bit typical**
- **3-state TTL compatible output**
- **All inputs TTL compatible**
- **Fully static operation**
- **Identical access & cycle times**
- **High output impedance during write**
- **Single +5V power supply**
- **Standard 18-pin DIP**

LOGIC SYMBOL



V_{CC} = Pin 18
GND = Pin 9

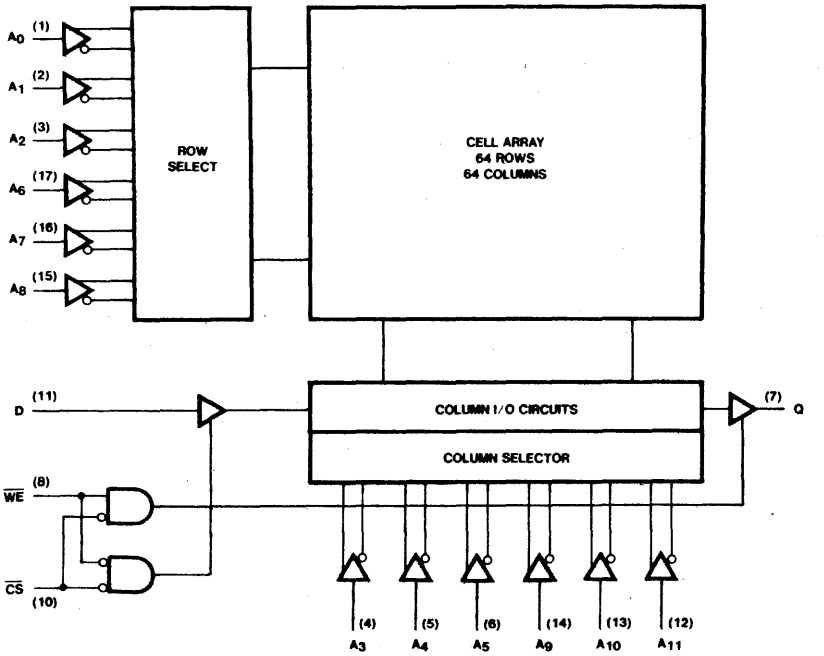
ORDERING CODE (See Package Section for further information)

PACKAGES	ACCESS TIME			
	150ns	200ns	250ns	450ns
Ceramic DIP	2613-15I	2613-20I	2613-25I	2613-45I
Cerdip	2613-15F	2613-20F	2613-25F	2613-45F
Plastic DIP	2613-15N	2613-20N	2613-25N	2613-45N

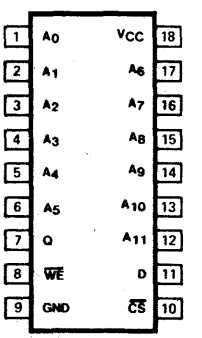
PIN DESIGNATION

SYMBOL	DESCRIPTION
A_0-A_{11}	Address inputs
$\overline{CS}$	Chip select (active LOW) input
$\overline{WE}$	Write enable (active LOW) input
D	Data input
Q	Data output (3-State)
GND	Ground (0V)
V_{CC}	Power supply (+5V)

BLOCK DIAGRAM



PIN CONFIGURATION



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DESCRIPTION

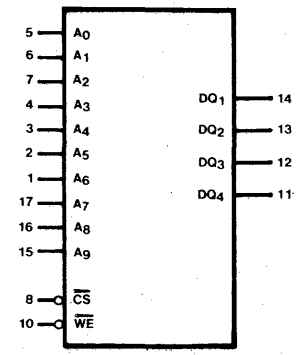
The Signetics 2614 is a high speed, 4096 bit static random access memory. Utilizing the Signetics n-channel, si-gate Mini-MOS technology to achieve high performance and high bit density, the 1024 x 4 organization offers a cost effective solution for designer needs.

The 2614 is fully static (access time = cycle time), all input and outputs are TTL compatible, and it has a single +5V supply. It is manufactured in the industry standard pinout 18 pin package.

FEATURES

- **Typical access time of 80ns**
- **Power dissipation of 0.1mW/bit typical**
- **3-state TTL compatible output**
- **All inputs TTL compatible**
- **Fully static operation**
- **Identical access & cycle time**
- **Single +5V power supply**
- **Standard 18-pin DIP**

LOGIC SYMBOL



V_{CC} = Pin 18
GND = Pin 9

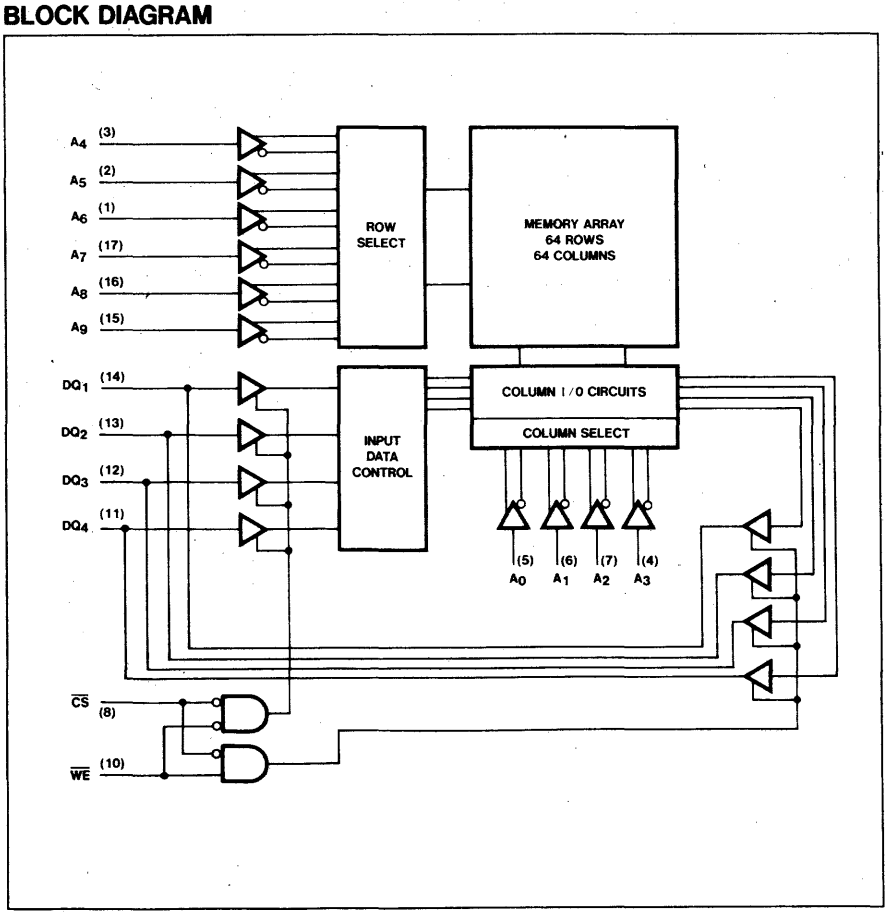
ORDERING CODE (See Packages Section for further information)

PACKAGES	ACCESS TIME			
	150ns	200ns	250ns	450ns
Ceramic DIP	2614-15I	2614-20I	2614-25I	2614-45I
Cerdip	2614-15F	2614-20F	2614-25F	2614-45F
Plastic	2614-15N	2614-20N	2614-25N	2614-45N

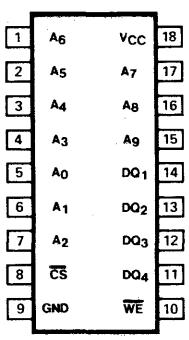
PIN DESIGNATION

SYMBOL	NAME & FUNCTION
A_0-A_9	Address inputs
$\overline{CS}$	Chip select (active LOW) input
$\overline{WE}$	Write enable (active LOW) input
DQ_1-DQ_4	Input/Output port (3-State)
GND	Ground (0V)
V	Power supply (+5V)

BLOCK DIAGRAM



PIN CONFIGURATION



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DESCRIPTION

The Signetics 2616 is a 16,384-bit static MOS read-only memory organized as 2048 words by 8 bits. This ROM is designed for memory applications where high performance, large bit storage, and simple interfacing are important design objectives.

The inputs and outputs are fully TTL compatible. This device operates with a single 5V power supply. The three chip select inputs are programmable. Any combination of active high or low level chip select inputs can be defined by the designer and the desired chip select logic level is fixed during the masking process. These three programmable chip select inputs, as well as OR-tie compatibility on the outputs, facilitates easy memory expansion.

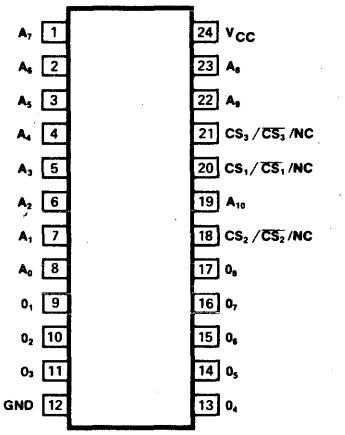
The 2616 read-only memory is fabricated with n-channel silicon gate technology. This technology provides the designer with high performance, easy-to-use MOS circuits. Only a single 5V power supply is needed and all devices are directly TTL compatible.

FEATURES

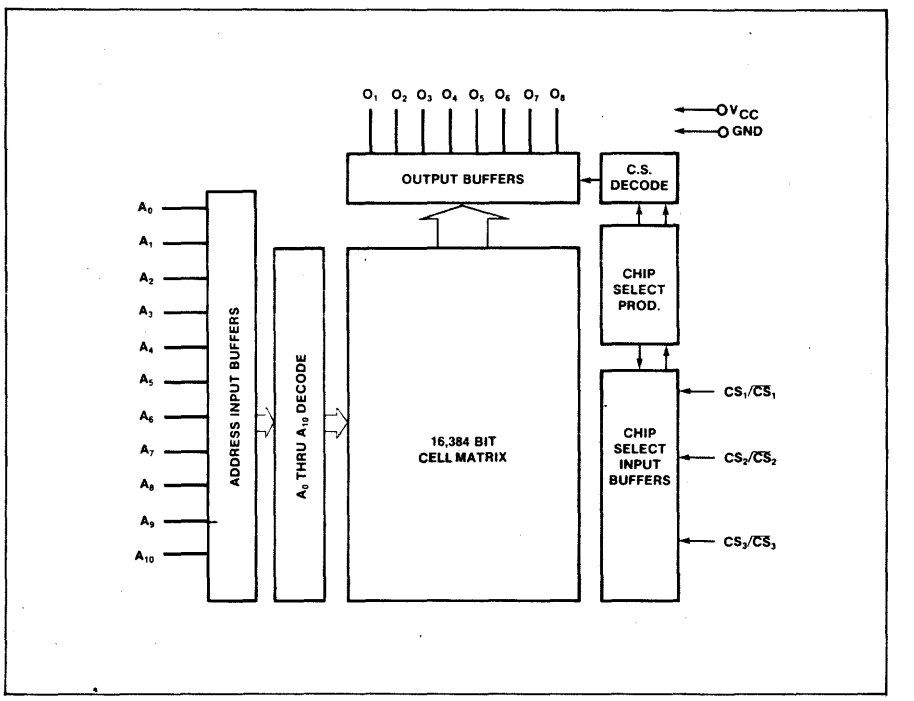
- **Single 5V power supply**
- **Guaranteed 350/450ns access time**
- **Directly TTL compatible—all inputs and outputs**
- **Three programmable chip select inputs for easy memory expansion or no connection option**
- **Three-state output—OR-tie capability**
- **Fully decoded—on chip address decode**
- **Inputs protected—all inputs have protection against static charge**

PIN CONFIGURATION

F,I,N PACKAGE



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS[1]

	PARAMETER	RATING	UNIT
	Temperature range		°C
T_A	Operating	0 to 70	
T_{STG}	Storage	-65 to 150	
	Supply voltage to ground potential	-0.5 to 7	V
	Applied voltage		V
	Input	-0.5 to 7	
	Output	-0.5 to 7	
P_D	Power dissipation	1	W

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DC ELECTRICAL CHARACTERISTICS

T_A = 0°C to 70°C, V_{CC} = 5.0V ± 5% unless otherwise specified

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
	Input voltage[2]					V
V_{IL}	Low		-0.5		0.8	
V_{IH}	High		2.2		V_{CC}	
	Output voltage	V_{CC} = 4.75V				V
V_{OL}	Low	I_{OL} = 1.6mA			0.4	
V_{OH}	High	I_{OH} = -100μA	2.4		V_{CC}	
I_{LI}	Input load current	V_{CC} = 5.25V, OV ≤ V_{IN} ≤ 5.25V			10	μA
I_{LO}	Output leakage current	Chip deselected, V_{OUT} = 0.4V to V_{CC}			10	μA
I_{CC}	Supply current	Output unloaded, T_A = 25°C, V_{CC} = 5.25V, V_{IN} = V_{CC}			115	mA
	Capacitance[3]	T_A = 25°C, f = 1.0MHz, all pins except pin under test tied to ac ground				pF
C_{IN}	Input				7	
C_O	Output				10	

AC ELECTRICAL CHARACTERISTICS

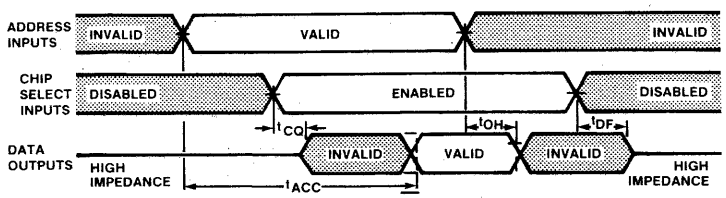
T_A = 0°C to 70°C, V_{CC} = 5.0V ± 5%, Output load = 1 TTL load and 100pF, Input transition time = 20ns, Timing reference levels: Input = 0.8V and 2.2V, Output = 0.4V and 2.4V unless otherwise specified.

PARAMETER		2616			2616-1			UNIT
		Min	Typ	Max	Min	Typ	Max	
t_{ACC}	Address access time			450			350	ns
t_{CO}	Chip select delay			200			150	ns
t_{DF}	Chip deselect delay			200			150	ns
t_{OH}	Previous data valid after address change delay	20			20			ns

NOTES

1. Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
2. Input levels that swing more negative than -0.5V will be clamped and may cause damage to the device.
3. This parameter is periodically sampled and is not 100% tested.

TIMING DIAGRAM



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OBJECTIVE SPECIFICATION 2632-F,I,N

DESCRIPTION

This ROM is designed for memory applications where high performance, large bit storage, and simple interfacing are important design objectives.

The two chip select inputs are programmable. Any combination of active high or low level chip select inputs can be defined by the designer and the desired chip select logic level is fixed during the masking process. These two programmable chip select inputs, as well as OR-tie compatibility on the outputs, facilitates easy memory expansion.

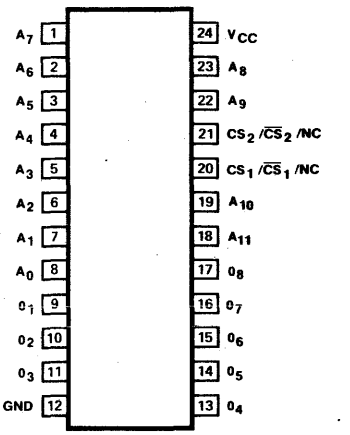
The 2632 Read Only Memory is fabricated with n-channel silicon gate technology. This technology provides the designer with high performance, easy-to-use MOS circuits.

FEATURES

- **Guaranteed 450ns address time**
- **Completely TTL compatible**
- **Single +5V power supply**
- **3-state output—OR-tie capability**
- **Fully decoded—on chip address decode**
- **Inputs protected—all inputs have protection against static charge**

PIN CONFIGURATION

F,I,N PACKAGE



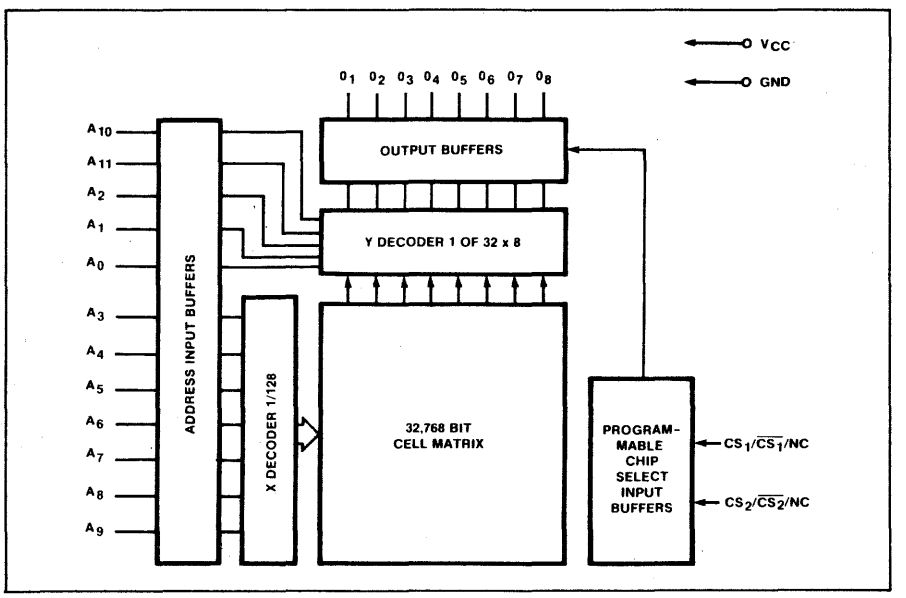
ABSOLUTE MAXIMUM RATINGS[1]

PARAMETER		RATING	UNIT
	Temperature range		°C
T_A	Operating	0° to +70	
T_{STG}	Storage	-65° to +150	
P_D	Power dissipation	1.2	W
	Applied voltage		V
	Input	-0.5 to +7	
	Output	-0.5 to +7	
	Supply voltage to ground potential	-0.5 to +7	V

NOTE

1. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

BLOCK DIAGRAM



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OBJECTIVE SPECIFICATION 2632-F,I,N

DC ELECTRICAL CHARACTERISTICS

T_A = 0°C to +70°C, V_{CC} = 5.0V ± 5%, unless otherwise specified.

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
	Input voltage					V
V_{IL}	Low[2]		-0.5		0.8	
V_{IH}	High		2.2		V_{CC}	
	Output voltage					V
V_{OL}	Low	I_{OL} = 1.6mA			0.4	
V_{OH}	High	I_{OH} = -100μA	2.4		V_{CC}	
I_{LI}	Input load current	0V ≤ V_{IN} ≤ 5.25V			10	μA
I_{LO}	Output leakage	Chip deselected V_{OUT} = +0.4V to V_{CC}			10	μA
I_{CC}	Supply current	Output unloaded T_A = 25°C, V_{IN} = V_{CC}			80	mA
	Capacitance[3]	T_A = 25°C, f = 1MHz, all pins except pin under test tied to ground				pF
C_{IN}	Input				7	
C_{OUT}	Output				10	

NOTES

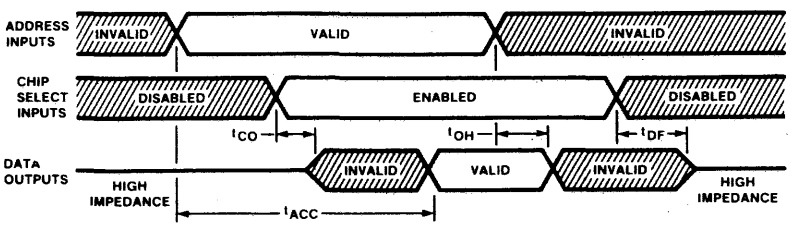
2. Input levels that swing more negative than -0.5 will be clamped and may cause damage to the device.
3. This parameter is periodically sampled and is not 100% tested.

AC ELECTRICAL CHARACTERISTICS

T_A = 0°C to +70°C, V_{CC} = 5V ± 5%, Output load = 1 TTL load and 100pF, Input transition time = 20ns, Timing reference levels: Input = 0.8V and 2.2V, Output = 0.4V and 2.4V unless otherwise specified.

PARAMETER		LIMITS			UNIT
		Min	Typ	Max	
t_{ACC}	Address access time			450	ns
t_{CO}	Chip select delay			200	ns
t_{DF}	Chip deselect delay			200	ns
t_{OH}	Previous data valid after address change delay	20			ns

TIMING DIAGRAM



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OBJECTIVE SPECIFICATION 2664-F,I,N

DESCRIPTION

This ROM is designed for memory applications where high performance, large bit storage, and simple interfacing are important design objectives.

The chip select input is programmable. Active high or active low level chip select input can be defined by the designer and the desired chip select logic level is fixed during the masking process. The programmable chip select input, as well as OR-tie compatibility on the outputs, facilitates easy memory expansion.

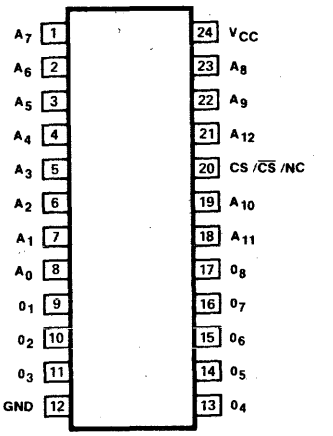
The 2664 Read Only Memory is fabricated with n-channel silicon gate technology. This technology provides the designer with high performance, easy-to-use MOS circuits.

FEATURES

- **Guaranteed 450ns access time**
- **Completely TTL compatible**
- **One +5V power supply**
- **3-state output—OR-tie capability**
- **Fully decoded—on chip address decode**
- **Inputs protected—all inputs have protection against static charge**

PIN CONFIGURATION

F,I,N PACKAGE



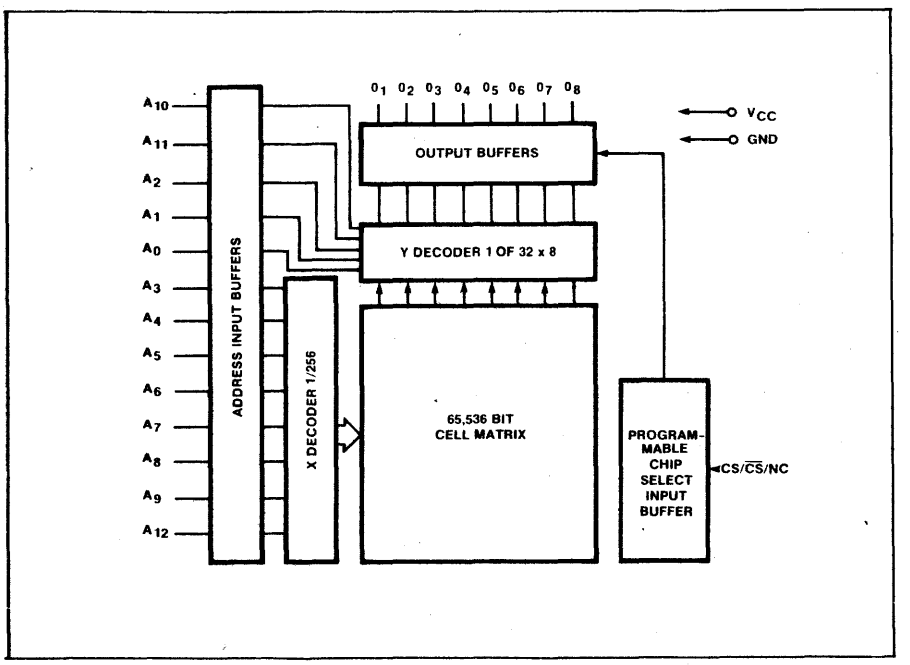
ABSOLUTE MAXIMUM RATINGS[1]

PARAMETER		RATING	UNIT
	Temperature range		°C
T_A	Operating	0° to +70	
T_{STG}	Storage	-65° to +150	
P_D	Power dissipation	1.5	W
	Applied voltage		V
	Input	-0.5 to +7	
	Output	-0.5 to +7	
	Supply voltage to ground potential	-0.5 to +7	V

NOTE

1. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied and exposure to absolute maximum rating conditions for extended periods may affect device reliability.

BLOCK DIAGRAM



Signetics

MEMORY

DC ELECTRICAL CHARACTERISTICS $T_A = 0°C$ to $+70°C$, $V_{CC} = 5.0V \pm 5\%$, unless otherwise specified.

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
	Input voltage					V
V_{IL}	Low[2]		-0.5		0.8	
V_{IH}	High		2.2		V_{CC}	
	Output voltage					V
V_{OL}	Low	$I_{OL} = 1.6mA$			0.4	
V_{OH}	High	$I_{OH} = -100\mu A$	2.4		V_{CC}	
I_{LI}	Input load current	$0V \le V_{IN} \le 5.25V$			10	μA
I_{LO}	Output Leakage	Chip deselected, $V_{OUT} = +0.4V$ to V_{CC}			10	μA
I_{CC}	Supply current	Output unloaded $T_A = 25°C$, $V_{IN} = V_{CC}$			150	mA
	Capacitance[3]	$T_A = 25°C$, f = 1MHz, all pins except pin under test tied to ground				pF
C_{IN}	Input				7	
C_{OUT}	Output				10	

NOTES

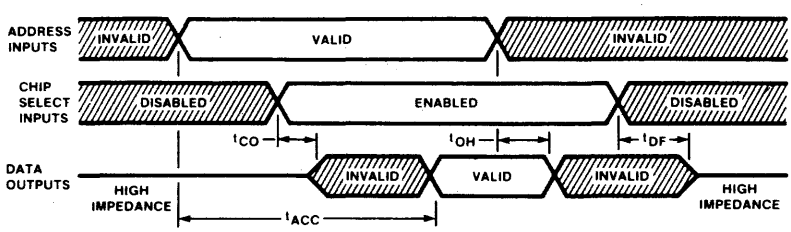
2. Input levels that swing more negative than -0.5V will be clamped and may cause damage to the device.
3. This parameter is periodically sampled and is not 100% tested.

AC ELECTRICAL CHARACTERISTICS

$T_A = 0°C$ to $+70°C$, $V_{CC} = 5.0V \pm 5\%$, Output load = 1 TTL load and 100pF, Input transition time = 20ns, Timing reference levels: Input = 0.8V and 2.2V, Output = 0.4V and 2.4V unless otherwise specified.

PARAMETER		LIMITS			UNIT
		Min	Typ	Max	
t_{ACC}	Address access time			450	ns
t_{CO}	Chip select delay			200	ns
t_{DF}	Chip deselect delay			200	ns
t_{OH}	Previous data valid after address change delay	20			ns

TIMING DIAGRAM



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OBJECTIVE SPECIFICATION

2690-2—F,I,N • 2690-3—F,I,N • 2690-4—F,I,N

DESCRIPTION

The 2690 is fabricated with double-poly n-channel silicon gate technology for high performance and high functional density. It uses a single transistor dynamic storage cell and dynamic circuitry to achieve high speed and low power dissipation.

The unique design of the 2690 allows it to be packaged in the industry standard 16-pin in-line package, which provides the highest system bit densities and is compatible with widely available automated handling equipment.

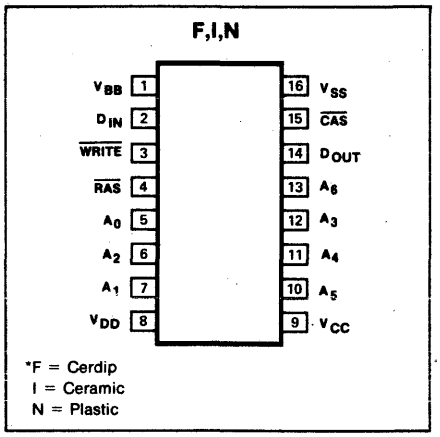
The use of the 16-pin package is made possible by multiplexing the 14 address bits (required to address one of 16,384 bits) into the 2690 on 7 address input pins. The two 7-bit address words are latched into the device by the 2 TTL clocks, Row Address Strobe ($\overline{RAS}$) and Column Address Strobe ($\overline{CAS}$). Non-critical clock timing requirements allow use of the multiplexing technique while maintaining high performance.

The memory cell requires refreshing for data retention. This is most easily accomplished by performing a $\overline{RAS}$ only cycle at each of 128 row addresses every 2ms.

FEATURES

- **Access time:**
  2690-2: 150ns
  2690-3: 200ns
  2690-4: 250ns
- **Read and write cycle time:**
  2690-2: 375ns
  2690-3: 375ns
  2690-4: 410ns
- **Low power:**
  Operating: 462mW (max)
  Standby: 20mW (max)
- **±10% power supply margins**
- **On-chip latches for address and data in**
- **Output data controlled by $\overline{CAS}$ and unlatched at end of cycle to allow 2-dimensional chip selection and extended page boundary**
- **Page mode addressing**
- **$\overline{RAS}$ only refresh**
- **Common I/O capability using "early write" operation**
- **All inputs TTL compatible**
- **3-state TTL compatible output**

PIN CONFIGURATION

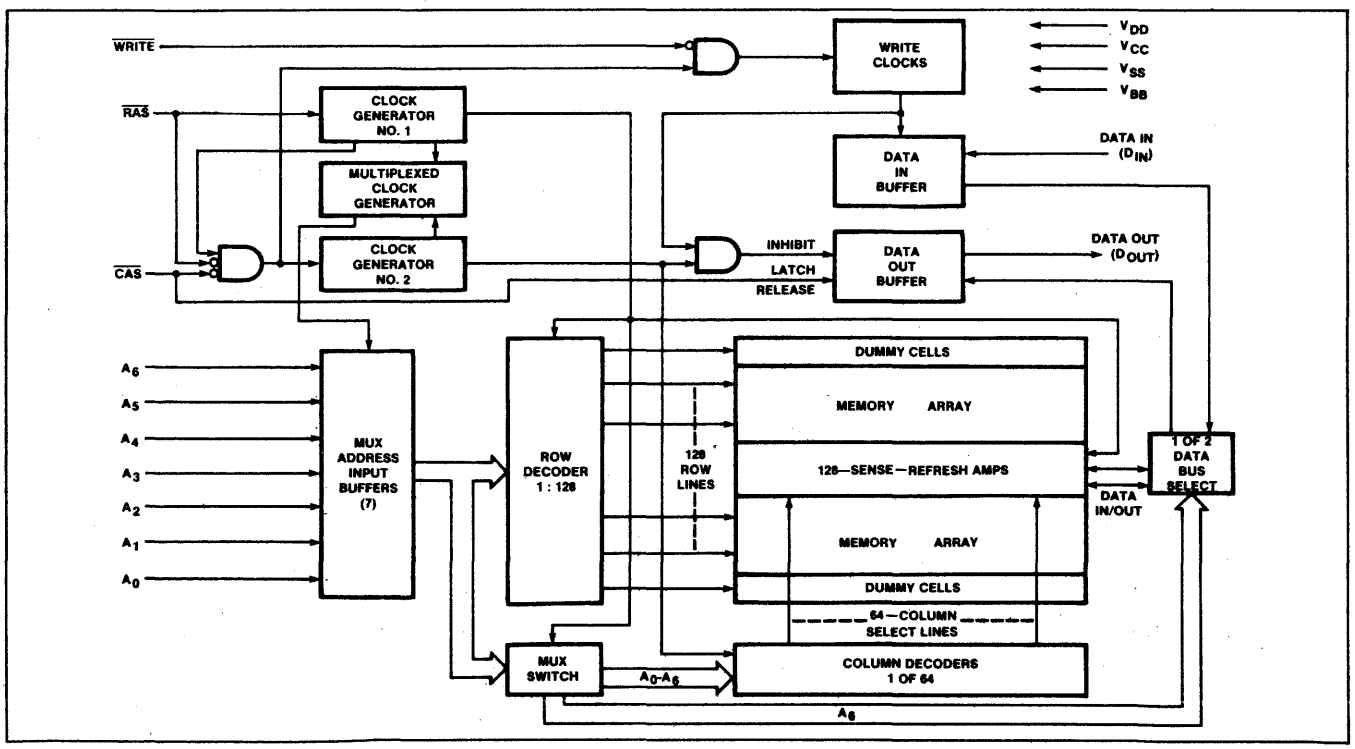


*F = Cerdip
I = Ceramic
N = Plastic

PIN DESIGNATION

PIN NO.	SYMBOL	NAME & FUNCTION
5-7, 10-13	A_0-A_6	Address inputs
15	$\overline{CAS}$	Column address strobe
2	D_{IN}	Data in
14	D_{OUT}	Data out
4	$\overline{RAS}$	Row address strobe
3	$\overline{WRITE}$	Read/write input
1	V_{BB}	Power (-5V)
9	V_{CC}	Power (+5V)
8	V_{DD}	Power (+12V)
16	V_{SS}	Ground

BLOCK DIAGRAM



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4027-2/4027-3/4027-4–F,I,N

DESCRIPTION

The 4027 is fabricated with n-channel silicon gate technology for high performance and high functional density, and uses a single transistor dynamic storage cell and dynamic circuitry to achieve high speed and low power dissipation.

The unique design of the 4027 allows it to be packaged in the industry standard 16-pin dual inline package, which provides the highest system bit densities and is compatible with widely available automated handling equipment.

The use of the 16-pin package is made possible by multiplexing the 12 address bits (required to address 1 of 4096 bits) into the 4027 on 6 address input pins. The two 6-bit address words are latched into the device by the 2TTL clocks, Row Address Strobe ($\overline{RAS}$), and Column Address Strobe ($\overline{CAS}$). Non-critical clock timing requirements allow use of the multiplexing technique while maintaining high performance.

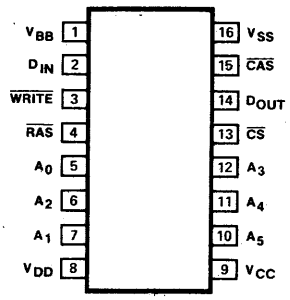
The single transistor dynamic storage cell provides high speed along with low power dissipation. The memory cell requires refreshing for data retention, and this is most easily accomplished by performing a read cycle at each of the 64 row addresses every 2ms, or by performing a $\overline{RAS}$ only cycle.

FEATURES

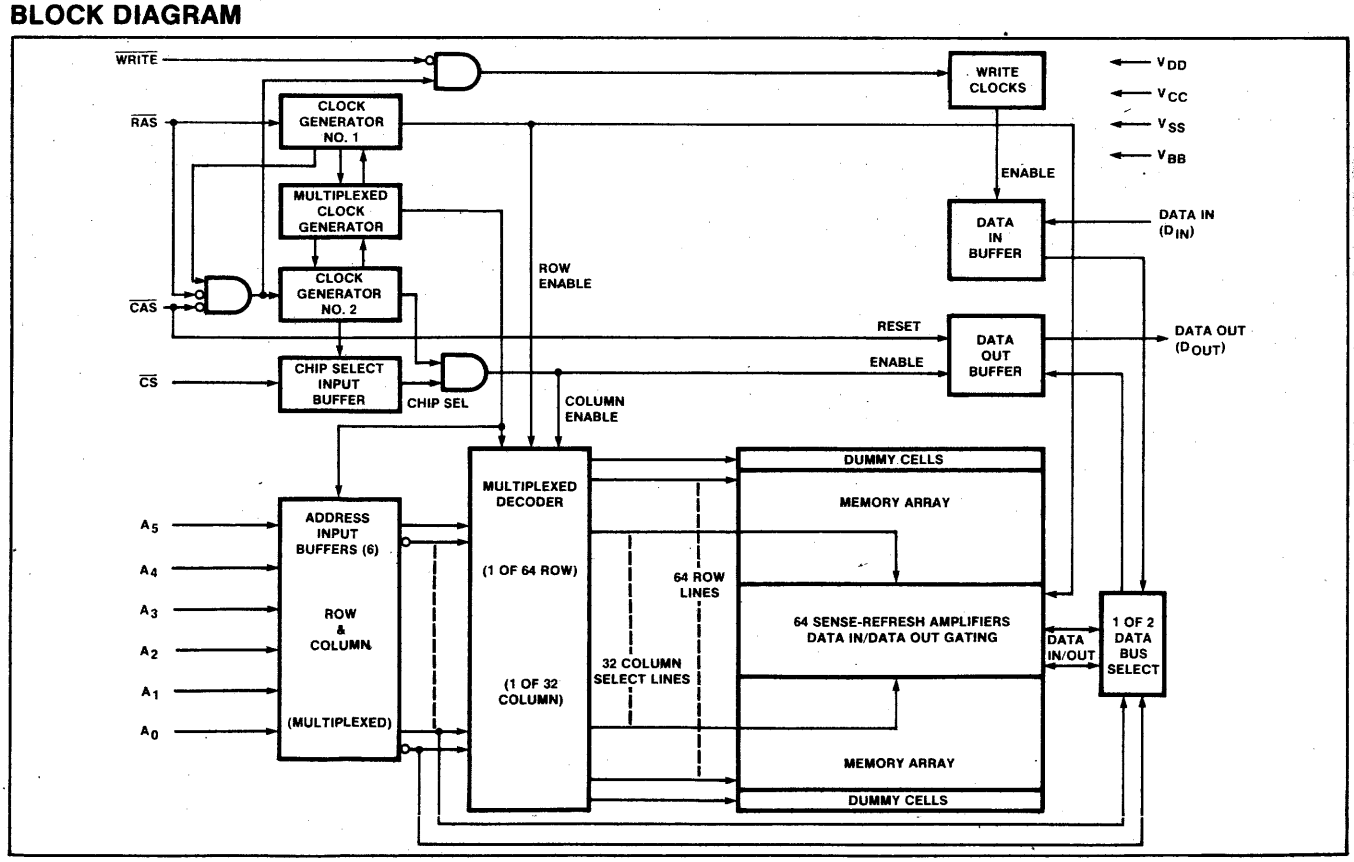
- **All inputs including clock TTL compatible**
- **On chip latches for address, chip select and data in**
- **3-state TTL compatible output**
- **Output data is latched and valid into next cycle**
- **Access time:**
  - **4027-2: 150ns**
  - **4027-3: 200ns**
  - **4027-4: 250ns**
- **Read and write cycle time:**
  - **4027-2: 320ns**
  - **4027-3: 375ns**
  - **4027-4: 375ns**
- **Low power:**
  - **Operating: 462mW**
  - **Standby: 27mW**
- **RAS only refresh (no dummy cycles required)**
- **Page mode addressing**
- **±10% power supply margins**

PIN CONFIGURATION

F,I,N PACKAGE



BLOCK DIAGRAM



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FEATURES

- **Full line of bipolar RAMs**
- **Military and commercial temperature ranges**
- **On-chip address latches**
- **2 port memories**
- **Read-while-write memory**
- **PNP inputs for low current**
- **Schottky clamped**
- **TTL compatible**

DESCRIPTION

The 82SXXX family of bipolar RAMs offers one of the widest selection of memories available in the industry. Along with all the standard RAMs, special features have been integrated on many devices enhancing their application effectiveness. Such features as address latches, output latches, 2 port memories and 8 and 9 bit outputs allow this family to answer almost every need.

Also, both commercial and military temperature ranges are available. For commercial range (0°C to +75°C) specify N82SXXX, and for military range (−55°C to +125°C) specify S82SXXX.

RAM QUICK SELECTION GUIDE

RAM		PACKAGE		TEMPERATURE RANGE		OUTPUT[11]		POWER/BIT	SPECIAL
ORGANIZATION	SIZE	PINS	TYPE[10]	0°C to +75°C	−55°C to +125°C	LOGIC	TYPE	(typ)	FEATURES
8 × 4	32	24	F, N	N82S12		T	OC	8500μW	2 PORT RAM
				N82S112		T	TS		
16 × 4	64	16	F, N	N82S25	S82S25	B	OC	6250μW	SCRATCH PAD RAM
				N74S89	S54S89	T	OC		
				N74S189	S54S189	B	TS		
				N3101A	S3101A	B	OC		
32 × 2	64	16	F, N	N82S21		T	OC	7800μW	READ WHILE WRITE RAM
256 × 1	256	16	F, N	N82S16	S82S16	T	TS	1500μW	FAST R/W CYCLE
				N82S17	S82S17	T	OC		
				N82S116		T	TS		
				N82S117		T	OC		
				N74S200	S54S200	B	TS		
				N74S201	S54S201	B	TS		
				N74S301	S54S301	B	OC		
64 × 9	576	28	I, N	N82S09	S82S09	T	OC	1302μW	9 BIT OUTPUT
1024 × 1	1024	16	F, N	N82S10	S82S10	B	OC	586μW	
				N82S11	S82S11	B	TS		
				N82S110		B	OC		T_{AA} = 30ns MAX
				N82S111		B	TS		
				N93415A		B	OC		FSC PIN OUTS
				N93425A		B	TS		
256 × 8	2048	22	F	N8X350	S8X350	C	I/O	329μW	ADDRESS LATCH
				N82S208		C	I/O		
256 × 9	2304	24	F, N	N82S210		C	I/O	292μW	
256 × 9	2304	24	F, N	N82S212		C	I/O	282μW	9 BIT OUTPUT
4096 × 1	4096	18	I	N82S400		B	OC	146μW	
				N82S401			TS		

NOTES
1. All voltage values are with respect to network ground terminal.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Test each input one at a time.
4. Measured with the logic low stored. Output sink current is supplied through a resistor to V_{CC}.
5. Measured with V_{IH} applied to $\overline{CE}$.
6. I_{CC} is measured with the write enable and memory enable input grounded, all other inputs at 4.5V, and the outputs open.
7. Minimum required to guarantee a Write into the slowest bit.
8. The operating ambient temperature ranges are guaranteed with transverse air flow exceeding 400 linear feet per minute and a 2-minute warm-up.
9. For more detailed specifications, see Signetics data sheet.
10. Package type: N = Plastic, F = Cerdip, I = Ceramic
11. Output definition: OC = Open-collector, TS = 3-state, T = transparent, B = Blanking, C = Common

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DC ELECTRICAL CHARACTERISTICS[8, 9]

N grade (COM) : $0°C \leq T_A \leq +70°C$, $4.75V \leq V_{CC} \leq 5.25V$
S grade (MIL) : $-55°C \leq T_A \leq +125°C$, $4.5V \leq V_{CC} \leq 5.5V$

PARAMETER[1]		TEST CONDITIONS	N grade (COM)			S grade (MIL)			UNIT
			Min	Typ[2]	Max	Min	Typ[2]	Max	
	Input voltage								V
V_{IL}	Low	V_{CC} = Min			0.85			0.8	
V_{IH}	High	V_{CC} = Max	2.0			2.0			
V_{IC}	Clamp[3]	V_{CC} = Min, I_{IN} = −18mA		−0.8	−1.2		−0.8	−1.2	
	Output voltage	V_{CC} = Min							V
V_{OL}	Low[4]	I_{OL} = 16mA		0.35	0.45		0.30	0.50	
V_{OH}	High	I_{OH} = 10.3mA	2.4						
V_{OH}	High	I_{OH} = −5.2mA				2.4			
	Input current[3]	V_{CC} = Max							
I_I	At V_{IN} Max	V_{IN} = 5.5V			1			1	mA
I_{IL}	Low	V_{IL} = 0.45 V		−10	−100		−10	−250	μA
I_{IH}	High	V_{IN} = 2.7V		1	25		1	25	μA
	Output current[5]								
I_{OLK}	Leakage	V_{IH} = 2V, V_O = 5.5V		1	40		1	50	μA
$I_{O(OFF)}$	Hi-Z state	V_{CC} = Max, V_O = 5.5V		1	40		1	100	μA
		V_{IH} = 2V, V_O = 0.4V		−1	−40		−1	−100	
I_{OS}	Short circuit	V_{CC} = Max, V_O = 0V	−30		−100	−30		−100	mA
	Capacitance	V_{CC} = 5.0V							pF
C_{IN}	Input	V_{IN} = 2.0V		5			5		
C_{OUT}	Output	V_{OUT} = 2.0V		8			8		

ADDITIONAL ELECTRICAL CHARACTERISTICS[8, 9]

N grade (COM) : $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$
S grade (MIL) : $-55°C \leq T_A \leq +125°C$, $4.5V \leq V_{CC} \leq 5.5V$

DEVICE	T_{AA}(Max)		T_{CE}(Max)		T_{WP}(Min)[7]		WRTcycle(Min)		I_{CC} (Max)[6]	
	N	S	N	S	N	S	N	S	N	S
82S12/112	40		30		45		65		160	
82S25	50	60	35	35	30	30	40	50	105	120
3101A	35	50	17	25	25	30	25	40	105	120
74S89	50	60	35	35	30	30	40	50	105	120
74S189	35	50	17	25	25	30	25	40	110	110
82S21	50		50		25		45		130	
82S16/17	50	70	40	40	30	40	55	70	115	120
82S116/117	40		25		25		25		115	
74S200/201 /301	50	70	35	45	40	50	50	60	130	130
82S09	45	80	30	50	35	50	45	70	190	200
82S10/11	45	70	30	45	35	50	45	75	155	170
82S110/111	35		25		25		40		155	
93415/425	45		30		35		45		155	
82S208/210	60		35		40		60		185	
8X350	75	95	35	40	40	50	45	55	185	185
82S212	45		35		40		60		185	
82S400/401	45		30		35		45		155	
UNITS	ns		ns		ns		ns		mA	

MEMORY TIMING DEFINITIONS

T_{AA} Delay between beginning of valid Address (with Chip Enable low) and when Data Output becomes valid.

T_{CE} Delay between beginning of Chip Enable low (with Address valid) and when Data Output becomes valid.

T_{WP} Width of Write Enable pulse.

WRT CYCLE Defines the minimum amount of time required to perform a write. This is the sum of T_{WP}(min) plus the minimum address set-up (T_{WSA}) and hold (T_{WHA}) time.

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SIGNETICS GENERIC BIPOLAR PROM FAMILY

FEATURES

- **Largest generic PROM family**
- **PNP inputs for low input current**
- **Compatible pin configurations for upward expansion**
- **On-chip output latches**
- **Schottky and Low-Power Schottky PROMs**
- **3-state and open-collector outputs**
- **Fully TTL compatible**
- **Reliability proven Ni-Cr fuses**

DESCRIPTION

The 82SXXX-series generic PROM family offers a wide selection of memory size and organization. The 4-bit wide PROMs range in capacity from 256 words to 2048 words and are packaged in a space saving 16 or 18-pin package. The 8-bit PROMs range in organization from 32 × 8 to 2048 × 8 and are available in a wide selection of package sizes. All PROMs have the same programming specifications allowing a single programmer to program the entire family.

The family also provides low current PNP inputs, both Schottky and low-power Schottky clamping, on-chip latches, and open-collector or 3-state outputs. All PROM fuse links store a low and are programmed to a high.

The entire family is available in both commercial and military temperature ranges. For commercial range (0°C to +75°C) specify N82SXXX, or for military range (−55°C to +125°C) specify S82XXX.

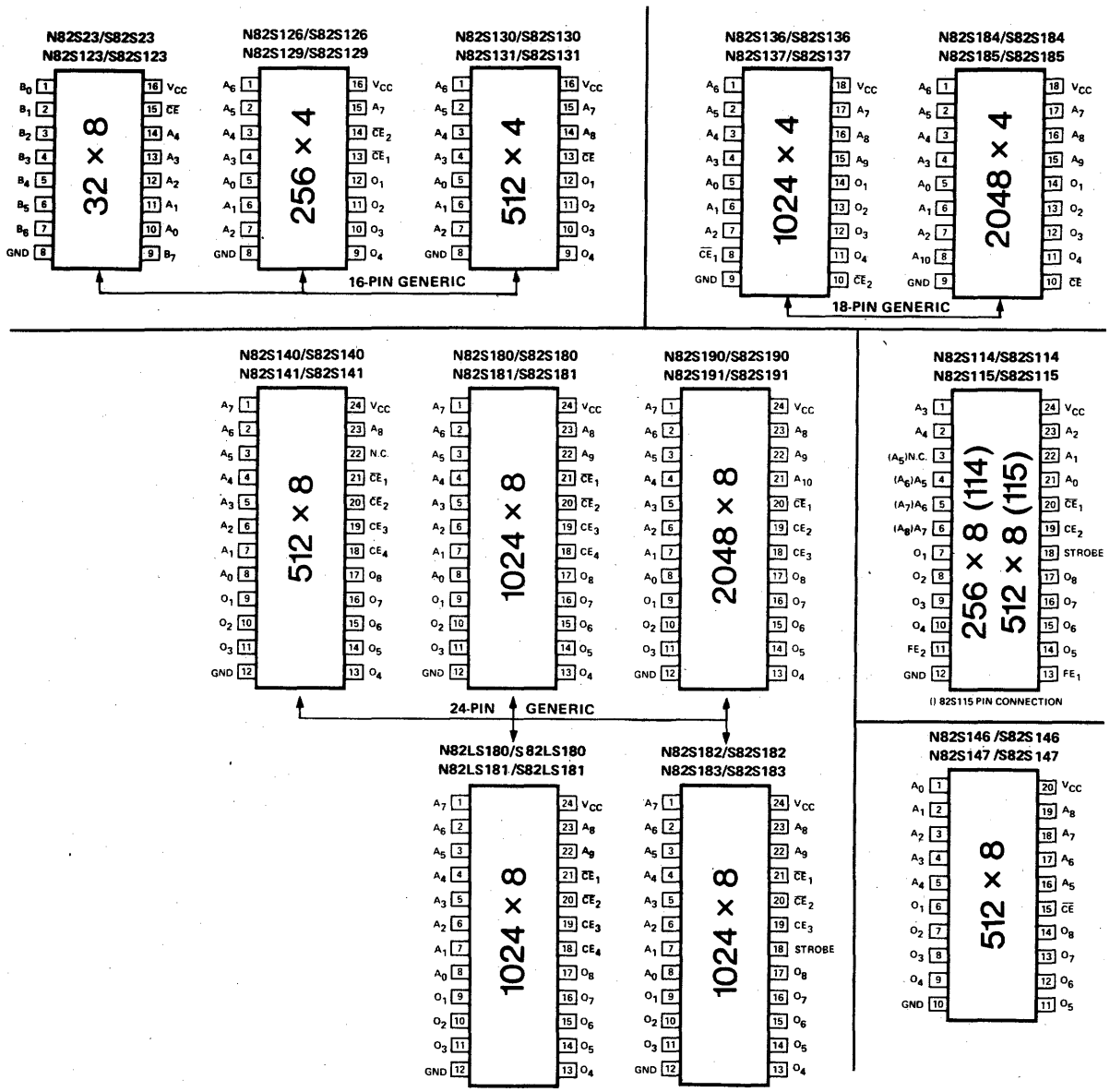
PROM QUICK SELECTION GUIDE

PROM		PACKAGE		TEMPERATURE RANGE		OUTPUT	OUTPUT	POWER/BIT
ORGANIZATION	SIZE	PINS	TYPE*	0°C to +75°C	−55°C to +125°C	TYPE	LATCH	(typical)
32 × 8	256	16	F, N	N82S23 N82S123	S82S23 S82S123	OC TS	NO NO	1300μW
256 × 4	1K	16	F, N	N82S126 N82S129	S82S126 S82S129	OC TS	NO NO	500μW
512 × 4	2K	16	F, N	N82S130 N82S131	S82S130 S82S131	OC TS	NO NO	300μW
1024 × 4	4K	18	F, N	N82S136 N82S137	S82S136 S82S137	OC TS	NO NO	130μW
2048 × 4	8K	18	I	N82S184 N82S185	S82S184 S82S185	OC TS	NO NO	50μW
256 × 8 512 × 8	2K 4K	24	F, N	N82S114 N82S115	S82S114 S82S115	TS TS	YES YES	330μW 165μW
512 × 8	4K	22	F	N82S146 N82S147	S82S146 S82S147	OC TS	NO NO	155μW
512 × 8	4K	24	F, N	N82S140 N82S141	S82S140 S82S141	OC TS	NO NO	170μW
1024 × 8	8K	24	F, N	N82S180 N82S181	S82S180 S82S181	OC TS	NO NO	85μW
1024 × 8	8K	24	F, N	N82S182 N82S183	S82S182 S82S183	OC TS	YES YES	85μW
1024 × 8	8K	24	F, N	N82LS180 N82LS181	S82LS180 S82LS181	OC TS	NO NO	37μW
2048 × 8	16K	24	I	N82S190 N82S191	S82S190 S82S191	OC TS	NO NO	40μW

* N = Plastic, F = Cerdip, I = Ceramic

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PIN CONFIGURATION



N.C. = No Connection

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DC ELECTRICAL CHARACTERISTICS[1]

N82SXXX : $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

S82SXXX : $-55°C \leq T_A \leq +125°C$, $4.5V \leq V_{CC} \leq 5.5V$

PARAMETER		TEST CONDITIONS	COMMERCIAL			MILITARY			UNIT
			Min	Typ[2]	Max	Min	Typ[2]	Max	
	Input voltage[3]								V
V_{IL}	Low				0.85			0.80	
V_{IH}	High		2.0			2.0			
V_{IC}	Clamp[5]	$I_{IN} = -18mA$		−0.8	−1.2		−0.8	−1.2	
	Output voltage[3]								V
V_{OL}	Low	$I_{OUT} = 9.6mA$			0.45			0.50	
V_{OH}	High (3-state)	$\overline{CE}_1$ = low, $I_{OUT} = -2mA$, $\overline{CE}_2$ = low, CE_2 = high, CE_4 = high, high stored	2.4			2.4			
	Input current								μA
I_{IL}	Low	$V_{IN} = 0.45V$			−100			−150	
I_{IH}	High	$V_{IN} = 5.5V$			40			50	
	Output current								
I_{OLK}	Leakage (open collector)	$\overline{CE}_1$ = high, $V_{OUT} = 5.5V$, $\overline{CE}_2$ = high, CE_3 = low, CE_4 = low			40			60	μA
$I_{O(OFF)}$	Hi-Z state (3-state)	$\overline{CE}_1$ = high, $V_{OUT} = 0.5V$, $\overline{CE}_2$ = high, CE_3 = low, CE_4 = low			−40			−60	μA
		$\overline{CE}_1$ = high, $V_{OUT} = 5.5V$, $\overline{CE}_2$ = high, CE_3 = low, CE_4 = low			40			60	μA
I_{OS}	Short circuit (3-state)[5, 6]	$V_{OUT} = 0V$	−20		−70	−15		−85	mA
I_{CC}	23/123			65	77		65	85	mA
	126/129			105	120		105	125	
	114/115/182/183/190/191			130	175		130	185	
	130/131			120	140		120	140	
	140/141/180/181			140	175		140	185	
	146/147			115	155			165	
	136/137			105	140		105	140	
	184/185			80	120		80	130	
	LS180/LS181			60	80		60	85	
	Capacitance	$V_{CC} = 5.0V$							pF
C_{IN}	Input	$V_{IN} = 2.0V$		5			5		
C_{OUT}	Output	$V_{OUT} = 2.0V$		8			8		

NOTES ON NEXT PAGE

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AC ELECTRICAL CHARACTERISTICS

$R_1 = 470\Omega$, $R_2 = 1k\Omega$, $C_L = 30pF$

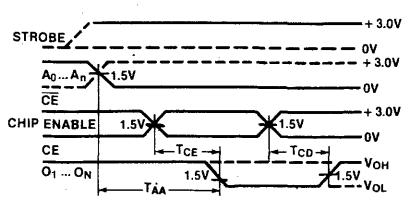
N82SXXX : $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$

S82SXXX : $-55°C \leq T_A \leq +125°C$, $4.5V \leq V_{CC} \leq 5.5V$

PARAMETER	PART TYPES	TO	FROM	COMMERCIAL Min	COMMERCIAL Typ[2]	COMMERCIAL Max	MILITARY Min	MILITARY Typ[2]	MILITARY Max	UNIT
T_{AA}	23/123	OUTPUT	ADDRESS		35	50		35	65	ns
	126/129				35	50		35	70	
	114/115/182/183				35	60		35	90	
	130/131				40	50		40	70	
	140/141				40	60		40	90	
	146/147				30	45		30	75	
	136/137				40	60		40	80	
	180/181				50	70		50	90	
	184/185				70	100		70	125	
	190/191				50	80		50	100	
	LS180/181				100	175		100	225	
T_{CE}	23/123	OUTPUT	CHIP ENABLE		25	35		25	40	ns
	126/129				15	25		15	35	
	114/115/140/141/180/181/182/183/190/191				20	40		20	50	
	130/131/146/147/136/137				20	30		20	40	
	184/185				30	40		30	60	
	LS180/181				35	60		35	80	
T_{CD}	23/123	OUTPUT	CHIP DISABLE		25	35		25	40	ns
	126/129				15	25		15	35	
	114/115/140/141/180/181/182/183/190/191				20	40		20	50	
	130/131/146/147/136/137				20	30		20	40	
	184/185				30	40		30	60	
	LS180/181				35	50		35	70	
	Setup and hold time[4]									ns
T_{CDS}	Setup time	OUTPUT	CHIP ENABLE	40			50			
T_{CDH}	Hold time			10	0		10	0		
T_{ADH}	Hold time[4]	OUTPUT	ADDRESS	0	−10		5	−10		
	Pulse width[4]									ns
T_{SW}	Strobe			30	20		40	20		
	Latch time[4]									ns
T_{SL}	Strobe			60	35		90	35		
	Delatch time[4]									ns
T_{DL}	Strobe					30			35	

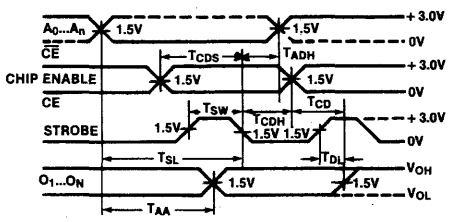
TIMING DIAGRAMS

TRANSPARENT READ



Output Latches Not Used

LATCHED READ[4]



Output Latches Used

NOTES
1. Positive current is defined as into the terminal referenced.
2. Typical values are at $V_{CC} = 5.0V$, $T_A = +25°C$.
3. All voltage values are with respect to network ground terminal.
4. Applies only to the 82S114/115/182/183.
5. Test one pin at a time.
6. Duration of short-circuit should not exceed 1 second.

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DESCRIPTION

The 82S100 (tri-state outputs) and the 82S101 (open collector outputs) are Bipolar Programmable Logic Arrays, containing 48 product terms (AND terms), and 8 sum terms (OR terms). Each OR term controls an output function which can be programmed either true active-high (Fp), or true active-low ($F\dot{p}$). The true state of each output function is activated by any logical combination of 16-input variables, or their complements, up to 48 terms. Both devices are field programmable, which means that custom patterns are immediately available by following the fusing procedure outlined in this data sheet.

The 82S100 and 82S101 are fully TTL compatible, and include chip-enable control for expansion of input variables, and output inhibit. They feature either open collector or tri-state outputs for ease of expansion of product terms and application in bus-organized systems.

Both devices are available in commercial and military temperature ranges. For the commercial temperature range (0°C to +75°C) specify N82S100/101,I or N, and for the military temperature range (-55°C to +125°C) specify S82S100/101,I.

FEATURES

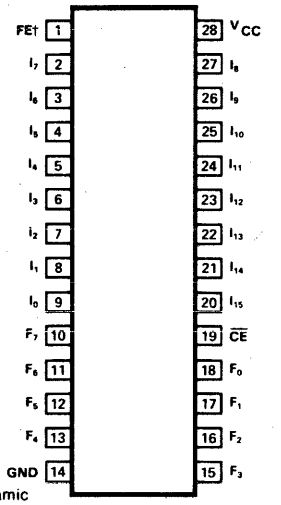
- **Field programmable (Ni-Cr link)**
- **Input variables: 16**
- **Output functions: 8**
- **Product terms: 48**
- **Address access time:**
  S82S100/101—80ns Max
  N82S100/101—50ns Max
- **Power dissipation: 600mW typ**
- **Input loading:**
  S82S100/101: -50μA Max
  N82S100/101: -100μA Max
- **Chip enable input**
- **Output option:**
  82S100: Tri-state
  82S101: Open collector
- **Output disable function:**
  Tri-state—Hi-Z
  Open collector—Hi

APPLICATIONS

- **CRT display systems**
- **Random logic**
- **Code conversion**
- **Peripheral controllers**
- **Function generators**
- **Look-up and decision tables**
- **Microprogramming**
- **Address mapping**
- **Character generators**
- **Sequential controllers**
- **Data security encoders**
- **Fault detectors**
- **Frequency synthesizers**

PIN CONFIGURATION

I,N PACKAGE*

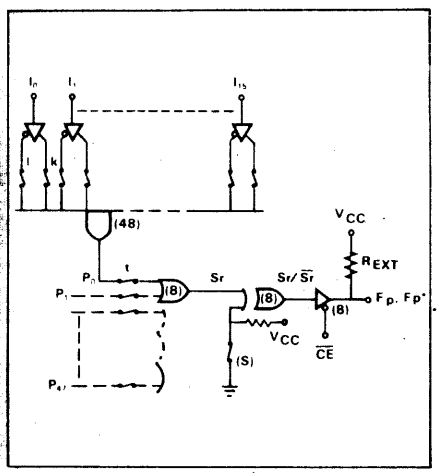


* I = Ceramic
N = Plastic
†Open during normal operation

TRUTH TABLE

MODE	Pn	$\overline{CE}$	Sr ? f(Pn)	Fp	$F\dot{p}$
Disabled (82S101)	X	1	X	1	1
Disabled (82S100)				Hi-Z	Hi-Z
Read	1	0	Yes	1	0
	0	0		0	1
	X	0	No	0	1

FPLA EQUIVALENT LOGIC PATH



LOGIC FUNCTION

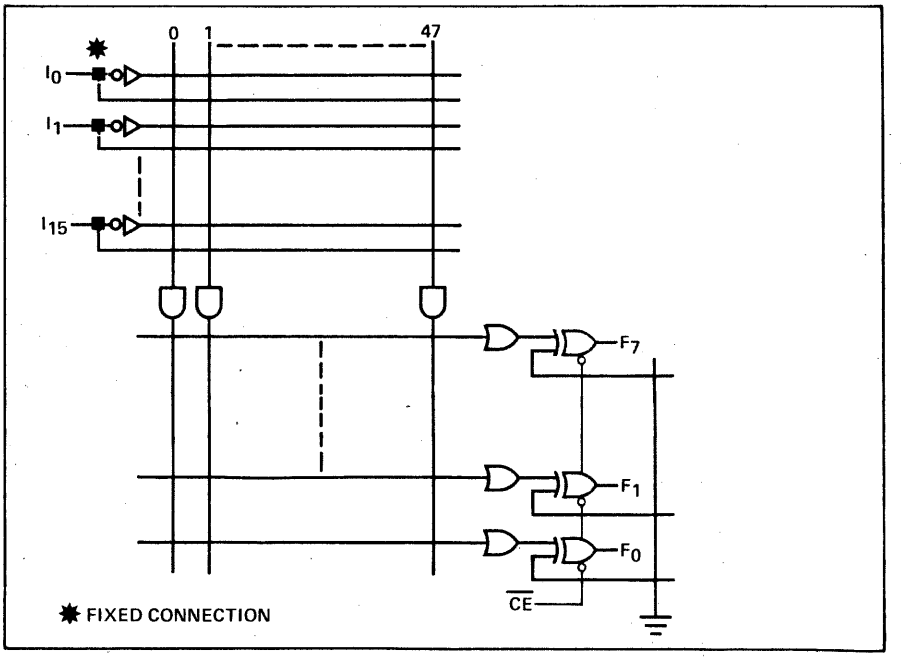
Typical Product Term:
$P_0 = I_0 \bullet I_1 \bullet \overline{I_2} \bullet I_5 \bullet \overline{I_{13}}$

Typical Output Functions:
$F_0 = (\overline{CE}) + (P_0 + P_1 + P_2)$ @ S = Closed
$F_0^* = (\overline{CE}) + (\overline{P_0} \bullet \overline{P_1} \bullet \overline{P_2})$ @ S = Open

NOTE

For each of the 8 outputs, either the function Fp (active-high) or $F\dot{p}$ (active low) is available, but not both. The required function polarity is programmed via link (S).

LOGIC DIAGRAM



✸ FIXED CONNECTION

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ABSOLUTE MAXIMUM RATINGS[1]

PARAMETER		RATING Min	RATING Max	UNIT
V_{CC}	Supply voltage		+7	Vdc
V_{IN}	Input voltage		+5.5	Vdc
V_{OUT}	Output voltage		+5.5	Vdc
I_{IN}	Input currents	-30	+30	mA
I_{OUT}	Output currents		+100	mA
	Temperature range			°C
T_A	Operating			
	N82S100/101	0	+75	
	S82S100/101	-55	+125	
T_{STG}	Storage	-65	+150	

THERMAL RATINGS

TEMPERATURE	MILITARY	COMMERCIAL
Maximum junction	175°C	150°C
Maximum ambient	125°C	75°C
Allowable thermal rise ambient to junction	50°C	75°C

DC ELECTRICAL CHARACTERISTICS

N82S100/101: $0° \le T_A \le +75°C$, $4.75V \le V_{CC} \le 5.25V$

S82S100/101: $-55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

PARAMETER		TEST CONDITIONS	N82S100/101 Min	N82S100/101 Typ[2]	N82S100/101 Max	S82S100/101 Min	S82S100/101 Typ[2]	S82S100/101 Max	UNIT
	Input voltage[3]								V
V_{IH}	High	V_{CC} = Max	2			2			
V_{IL}	Low	V_{CC} = Min			0.85			0.8	
V_{IC}	Clamp[3,4]	V_{CC} = Min, I_{IN} = -18mA		-0.8	-1.2		-0.8	-1.2	
	Output voltage	V_{CC} = Min							V
V_{OH}	High (82S100)[3,5]	I_{OH} = -2mA	2.4			2.4			
V_{OL}	Low[3,6]	I_{OL} = 9.6mA		0.35	0.45		0.35	0.50	
	Input current								μA
I_{IH}	High	V_{IN} = 5.5V		<1	25		<1	50	
I_{IL}	Low	V_{IN} = 0.45V		-10	-100		-10	-150	
	Output current	V_{CC} = Max							
I_{OLK}	Leakage[7]	V_{OUT} = 5.5V		1	40		1	60	μA
$I_{O(OFF)}$	Hi-Z state (82S100)[7]	V_{OUT} = 5.5V		1	40		1	60	μA
		V_{OUT} = 0.45V		-1	-40		-1	-60	
I_{OS}	Short circuit (82S100)[4,8]	V_{OUT} = 0V	-20		-70	-15		-85	mA
I_{CC}	V_{CC} supply current[9]	V_{CC} = Max		120	170		120	180	mA
	Capacitance[7]	V_{CC} = 5.0V							pF
C_{IN}	Input	V_{IN} = 2.0V		8			8		
C_{OUT}	Output	V_{OUT} = 2.0V		17			17		

AC ELECTRICAL CHARACTERISTICS

$R_1 = 470\Omega$, $R_2 = 1k\Omega$, $C_L = 30pF$

N82S100/101: $0°C \le T_A \le +75°C$, $4.75V \le V_{CC} \le 5.25V$

S82S100/101: $-55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

PARAMETER		TO	FROM	N82S100/101 Min	N82S100/101 Typ[2]	N82S100/101 Max	S82S100/101 Min	S82S100/101 Typ[2]	S82S100/101 Max	UNIT
	Access time									ns
T_{IA}	Input	Output	Input		35	50		35	80	
T_{CE}	Chip enable	Output	Chip enable		15	30		15	50	
	Disable time									ns
T_{CD}	Chip disable	Output	Chip enable		15	30		15	50	

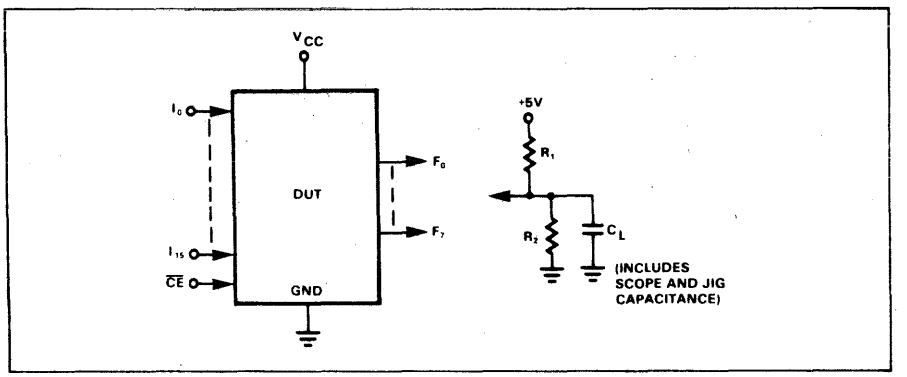
NOTES on following page.

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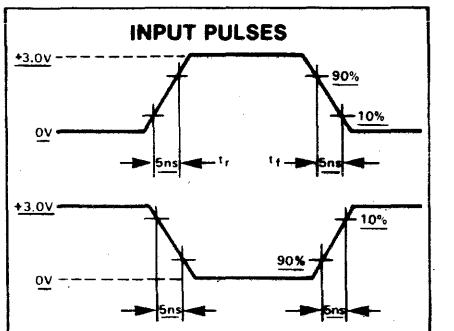
NOTES

1. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device of these or any other condition above those indicated in the operation of the device specifications is not implied.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. All voltage values are with respect to network ground terminal.
4. Test one at the time.
5. Measured with V_{IL} applied to $\overline{CE}$ and a logic high stored.
6. Measured with a programmed logic condition for which the output test is at a low logic level. Output sink current is applied thru a resistor to V_{CC}.
7. Measured with: V_{IH} applied to $\overline{CE}$.
8. Duration of short circuit should not exceed 1 second.
9. I_{CC} is measured with the chip enable input grounded, all other inputs at 4.5V and the outputs open.

TEST LOAD CIRCUIT

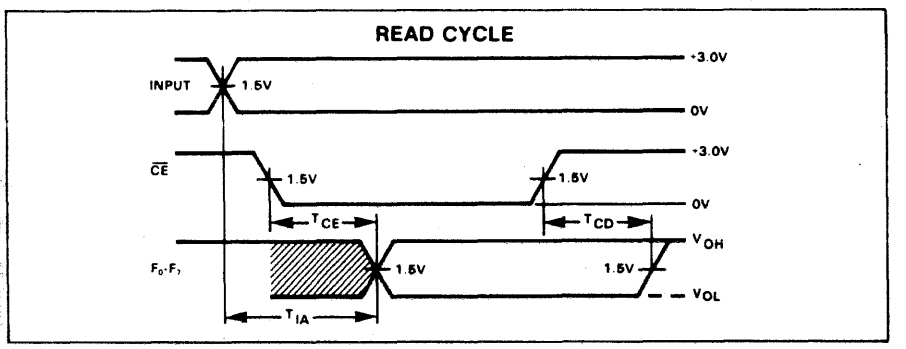


VOLTAGE WAVEFORM



Measurements: All circuit delays are measured at the +1.5V level of inputs and outputs.

TIMING DIAGRAM



TIMING DEFINITIONS

T_{CE} Delay between beginning of Chip Enable low (with Address valid), and when Data Output becomes valid.

T_{CD} Delay between when Chip Enable becomes high and Data Output is in off state (Hi-Z or high).

T_{IA} Delay between beginning of valid Input (with Chip Enable low) and when Data Output becomes valid.

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DESCRIPTION

The 82S102 and 82S103 are Bipolar programmable AND/NAND gate arrays, containing 9 gates sharing 16 common inputs. On-chip input buffers enable the user to individually program for each gate either the True (I_m), Complement ($\overline{I_m}$), or Don't Care (X) logic state of each input. In addition, the polarity of each gate output is individually programmable to implement either AND or NAND logic functions.

Alternately, if desired, OR/NOR logic functions can also be realized by programming for each gate the complement of its input variables, and output (DeMorgan theorem).

Both devices are field-programmable, which means that custom patterns are immediately available by following the fusing procedure outlined in this data sheet.

The 82S102 and 82S103 include chip-enable control for output strobing and inhibit. They feature either open collector or tri-state outputs for ease of expansion of input variables and application in bus-organized systems.

Both devices are available in the commercial and military temperature ranges. For the commercial range (0°C to +75°C) specify N82S102/103, I or N, and for the military range (-55°C to +125°C) specify S82S102/103, I.

FEATURES

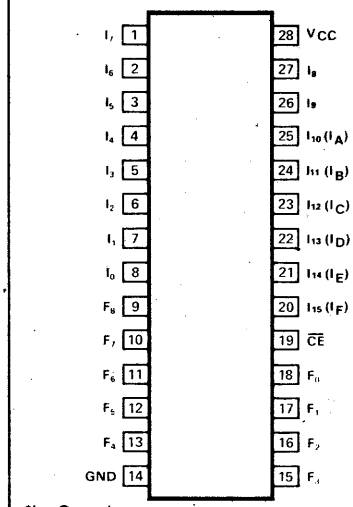
- **Field programmable (Ni-Cr link)**
- **16 input variables**
- **9 output functions**
- **Chip enable input**
- **I/O propagation delay:**
  N82S102/103: 35ns max
  S82S102/103: 50ns max
- **Power dissipation: 600mW typ**
- **Input loading:**
  N82S102/103: -100μA max
  S82S102/103: -150μA max
- **Output options:**
  82S102: Open collector
  82S103: Tri-state
- **Output disable function:**
  82S102: Hi
  82S103: Hi-Z
- **Fully TTL compatible**

APPLICATIONS

- **Random logic**
- **Address decoders**
- **Code detectors**
- **Peripheral selectors**
- **Fault monitors**
- **Machine state decoders**

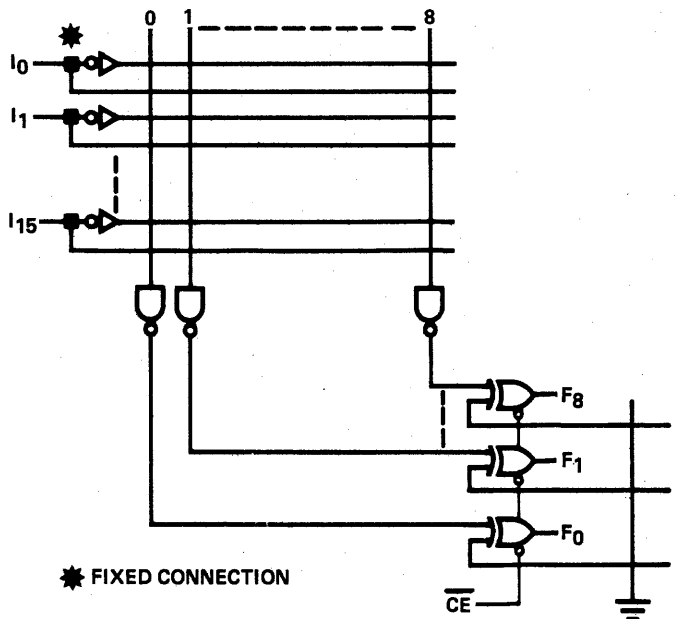
PIN CONFIGURATION

I,N PACKAGE*



*I = Ceramic
N = Plastic

LOGIC DIAGRAM



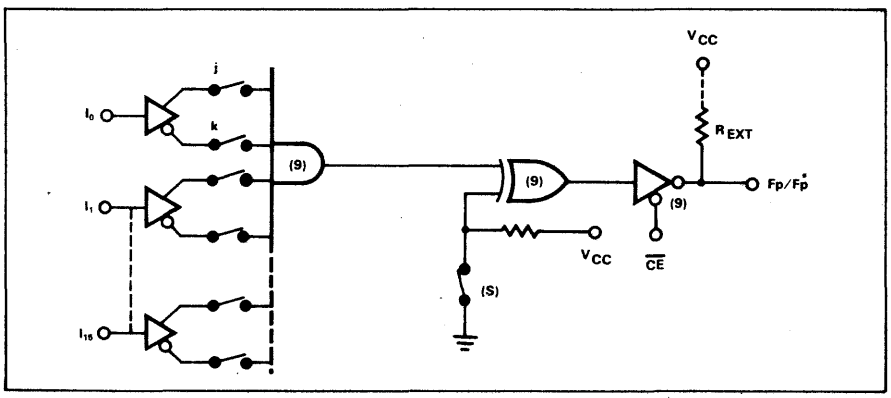
For each of the 9 outputs, either the function Fp (active high) or Fp (active low) is available, but not both. The required function polarity is user programmable via fuse (S).

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ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
V_{CC}	Supply voltage	+7	Vdc
V_{IN}	Input voltage	+5.5	Vdc
	Output voltage		Vdc
V_{OH}	High (82S102)	+5.5	
V_O	Off-state (82S103)	+5.5	
I_{IN}	Input current	±30	mA
I_{OUT}	Output current	+100	mA
	Temperature range		°C
T_A	Operating		
	N82S102/103	0 to +75	
	S82S102/103	-55 to +125	
T_{STG}	Storage	-65 to +150	

EQUIVALENT LOGIC PATH



The Field Programmable Gate Array consists of 9 gates with individually programmable inputs and outputs.

The inputs to each gate can be programmed either True (I_m), Complement ($\overline{I_m}$), or Don't Care via corresponding links (j) and (k). The outputs of each gate can be programmed active-high (F_p) or active-low (F_p^*) via corresponding links (S). Thus, each gate provides either of 2 output logic functions in terms of *external* input logic variables X_m as defined below (positive logic):

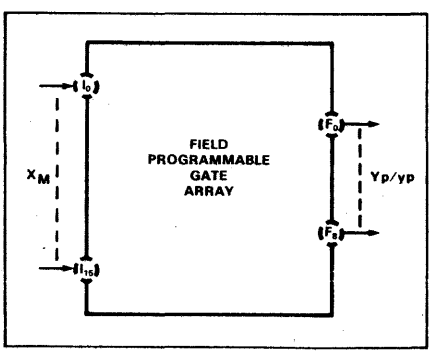
At S = Open:

$F_P = \overline{CE} + (X_0 \bullet X_1 \bullet X_2 \bullet \ldots . X_m) = Y_P$

At S = Closed:

$F_P^* = \overline{CE} + (\overline{X}_0 + \overline{X}_1 + \overline{X}_2 + \ldots . X_m) = y_P$

$m = 0, 1, 2, \ldots . 15$



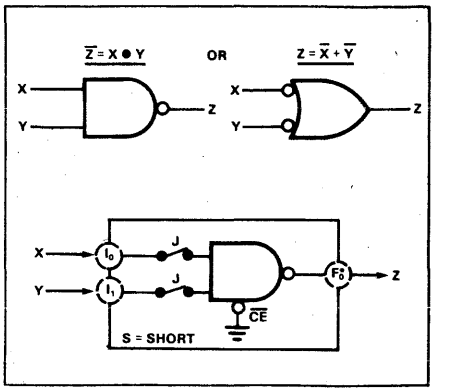
$p = 0, 1, 2, \ldots . 8$

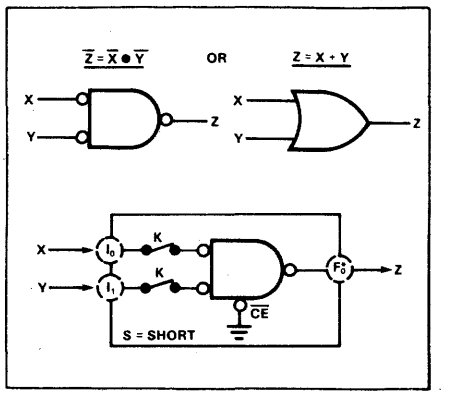
and where $X_m = I_m, \overline{I_m}$, Don't Care, as assigned by programming polarity of inputs I_0–I_{15}.

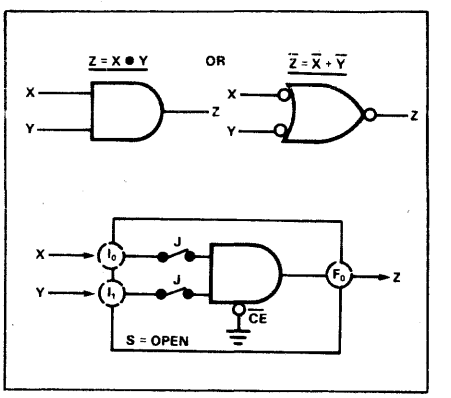
When $\overline{CE}$ = low, all gates are enabled, and $F_P^* = \overline{F}_P$ giving $y_P = \overline{Y}_P$.

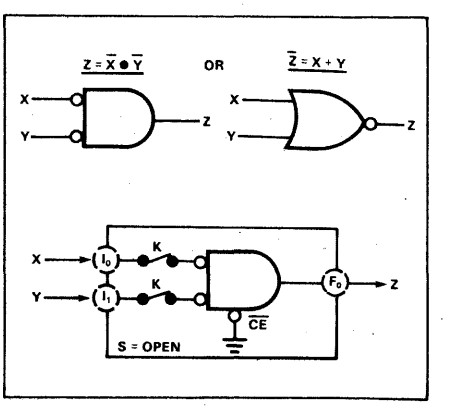
PROGRAMMABLE LOGIC FUNCTIONS

All internal links of virgin FPGAs are intact. Therefore, as shown in the Equivalent Logic Path, all symbolic switches are initially closed. Selective programming (opening) of links (J), (K), and (S) enables the user to assign input and output polarities to each gate for implementing NAND, NOR, AND, OR logic functions without changing the routing of input and output wires. This is shown in the following diagrams for a typical gate in terms of 2 input variables, which can be readily extended up to 16.









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DC ELECTRICAL CHARACTERISTICS

N82S102/103: $0°C \le T_A \le +75°C$, $4.75V \le V_{CC} \le 5.25V$
S82S102/103: $-55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

PARAMETER[1]		TEST CONDITIONS	N82S102/103			S82S102/103			UNIT
			Min	Typ[2]	Max	Min	Typ[2]	Max	
	Input voltage								V
V_{IL}	Low[1]	V_{CC} = Min			0.85			0.8	
V_{IH}	High[1]	V_{CC} = Max	2.0			2.0			
V_{IC}	Clamp[1,3]	V_{CC} = Min, I_{IN} = -18mA		-0.8	-1.2		-0.8	-1.2	
	Output voltage	V_{CC} = Min							V
V_{OL}	Low[1,4]	I_{OL} = 9.6mA		0.35	0.45		0.35	0.50	
V_{OH}	High (82S103)[1,5]	I_{OH} = -2mA	2.4			2.4			
	Input current								μA
I_{IL}	Low	V_{IN} = 0.45V		-10	-100		-10	-150	
I_{IH}	High	V_{IN} = 5.5V		<1	25		<1	50	
	Output current	V_{CC} = Max							
I_{OLK}	Leakage (82S102)[6]	V_{OUT} = 5.5V		1	40		1	60	μA
$I_{O(OFF)}$	Hi-Z state (82S103)[6]	V_{OUT} = 5.5V		1	40		1	60	μA
		V_{OUT} = 0.45V		-1	-40		-1	-60	
I_{OS}	Short circuit (82S103)[3,7]	V_{OUT} = 0V	-20		-70	-15		-85	mA
I_{CC}	V_{CC} supply current[8]	V_{CC} = Max		120	170		120	180	mA
	Capacitance	V_{CC} = 5.0V							pF
C_{IN}	Input	V_{IN} = 2.0V		8			8		
C_{OUT}	Output[6]	V_{OUT} = 2.0V		15			15		

AC ELECTRICAL CHARACTERISTICS

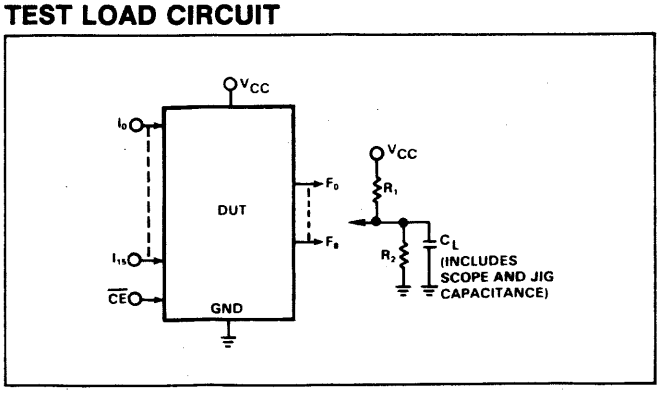
$R_1 = 470\Omega$, $R_2 = 1k\Omega$, $C_L = 30pF$
N82S102/103: $0°C \le T_A \le +75°C$, $4.75V \le V_{CC} \le 5.25V$
S82S102/103: $-55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

PARAMETER		TO	FROM	N82S102/103			S82S103/103			UNIT
				Min	Typ[2]	Max	Min	Typ[2]	Max	
	Access time									ns
T_{IA}	Input	Output	Input		20	35		20	55	
T_{CE}	Chip enable	Output	Chip enable		15	30		15	45	
	Disable time									ns
T_{CD}	Chip disable	Output	Chip enable		15	30		15	45	

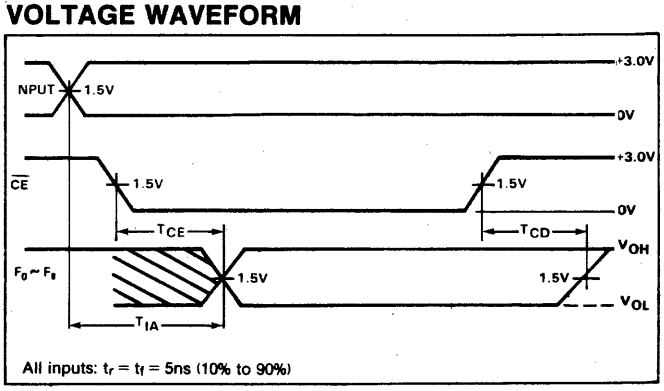
NOTES

1. All voltage values are with respect to network ground terminal.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. Test each output one at a time.
4. Measured with a programmed logic condition for which the output under test is at a low logic level. Output sink current is supplied through a resistor to V_{CC}.
5. Measured with V_{IL} applied to $\overline{CE}$ and a logic high at the output.
6. Measured with V_{IH} applied to $\overline{CE}$.
7. Duration of short circuit should not exceed 1 second.
8. I_{CC} is measured with the chip enable input grounded, all other inputs at 4.5V and the outputs open.

TEST LOAD CIRCUIT



VOLTAGE WAVEFORM



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DESCRIPTION

The 82S104 (open collector outputs) and the 82S105 (tri-state outputs) are bipolar, programmable state machines of the Mealy type. They contain logic AND-OR gate arrays with user programmable connections which control the inputs of on-chip State and Output registers. These consist respectively of 6 Q_S, and 8 Q_f edge triggered, clocked S/R flip-flops, with asynchronous Preset option. All flip-flops are unconditionally preset to "1" during power turn on.

The AND array combines 16 external inputs $I_{0\text{-}15}$ with 6 internal inputs $Q_{0\text{-}5}$ fed back from the State register to form up to 48 Transition terms (AND terms). All Transition terms can include True, False, or Don't Care states of the controlling variables, and are merged in the OR array to issue next-state and next-output commands to their respective registers on the Low to High transition of the Clock pulse. Both True and Complement Transition terms can be generated by optional use of the internal input variable (C) from the Complement array. Also, if desired, the Preset input can be converted to Output-Enable function, as an additional user programmable option.

Both devices are available in commercial and military temperature ranges. For the commercial temperature range (0°C to +75°C) specify N82S104/105, I or N, and for the military temperature range (−55°C to +125°C) specify S82S104/105, I.

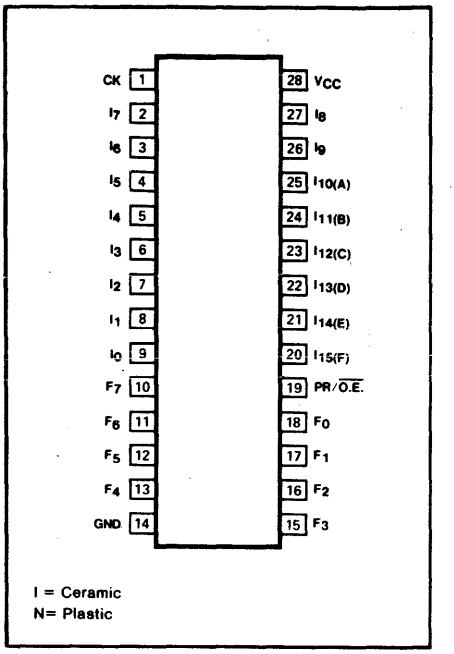
TRUTH TABLE (Output Control)

I_O	INPUT OPTION		F_N
	PR	$\overline{O.E.}$	
X	H		H
+10	L		Q_S
X		H	H/Hi-Z
X		L	Q_F
+10		L	Q_S

NOTES

1. Positive Logic:
   $S/R = T_O + T_1 + T_2 \ldots T_{47}$
   $T_n = C \bullet (I_O \bullet i_1 \bullet i_2 \ldots) \bullet (P_O \bullet P_1 \ldots P_5)$
   C, I_m, P_s = High, Low or Don't Care
2. Either Preset (active-High) or Output Enable (active-Low) are available, but not both. The desired function is a user programmable option.
3. ↑ denotes transition from Low to High level.
4. R = S = High is an illegal input condition.

PIN CONFIGURATION

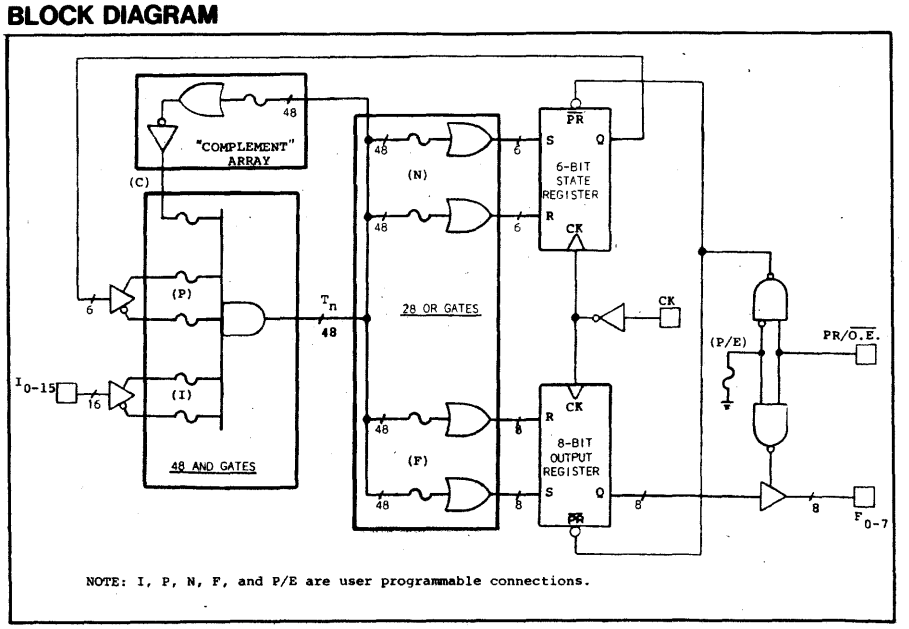


I = Ceramic
N= Plastic

TRUTH TABLE (All flip-flops)

V_{CC}	INPUT OPTION		CK	R	S	STATE REGISTER	OUTPUT REGISTER
	PR	$\overline{O.E.}$				Q_S	Q_F
+5V	H		X	X	X	H	H
	L	X	↑	L	L	Q_S	Q_F
	L	X	↑	L	H	L	L
	L	X	↑	H	L	H	H
	L	X	↑	H	H	INDET.	INDET.
↑	X	X	X	X	X	H	H

BLOCK DIAGRAM



NOTE: I, P, N, F, and P/E are user programmable connections.

FEATURES

- Field programmable (Ni-Cr link)
- 16 input variables
- 8 output functions
- 48 transition terms
- 6-BIT state register
- 8-BIT output register
- Transition complement array
- Positive edge trigger clock
- Programmable asynchronous preset or output enable
- Power-on preset to all "1" of internal Registers
- 90 Ns maximum I/O delay
- 650mW power dissipation (typical)
- TTL compatible
- SINGLE +5V supply

APPLICATIONS

- Interface protocols
- Sequence detectors
- Peripheral controllers
- Timing generators
- Sequential circuits
- Elevator controllers
- Security locking systems

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ABSOLUTE MAXIMUM RATINGS[1]

PARAMETER		RATING Min	RATING Max	UNIT
V_{CC}	Supply voltage		+7	Vdc
V_{IN}	Input voltage		+5.5	Vdc
V_{OUT}	Output voltage		+5.5	Vdc
I_{IN}	Input currents	−30	+30	mA
I_{OUT}	Output currents		+100	mA
	Temperature range			°C
T_A	Operating			
	N82S104/105	0	+75	
	S82S104/105	−55	+125	
T_{STG}	Storage	−65	+150	

THERMAL RATINGS

TEMPERATURE	MILI-TARY-	COM-MER-CIAL
Maximum junction	175°C	150°C
Maximum ambient	125°C	75°C
Allowable thermal rise ambient to junction	50°C	75°C

DC ELECTRICAL CHARACTERISTICS

N82S104/105: 0° ≤ T_A ≤ +75°C, 4.75V ≤ V_{CC} ≤ 5.25V

S82S104/105: −55°C ≤ T_A ≤ +125°C, 4.5V ≤ V_{CC} ≤ 5.5V

PARAMETER		TEST CONDITIONS	N82S104/105 Min	N82S104/105 Typ[2]	N82S104/105 Max	S82S104/105 Min	S82S104/105 Typ[2]	S82S104/105 Max	UNIT
	Input voltage[3]								V
V_{IH}	High	V_{CC} = Max	2			2			
V_{IL}	Low	V_{CC} = Min			0.85			0.8	
V_{IC}	Clamp[3,4]	V_{CC} = Min. I_{IN} = −18mA		−0.8	−1.2		−0.8	−1.2	
	Output voltage	V_{CC} = Min							V
V_{OH}	High (82S105)[3,5]	I_{OH} = 2mA	2.4			2.4			
V_{OL}	Low[3,6]	I_{OL} = 9.6mA		0.35	0.45		0.35	0.50	
	Input current								μA
I_{IH}	High	V_{IN} = 5.5V		<1	25		<1	50	
I_{IL}	Low	V_{IN} = 0.45V		−10	−100		−10	−150	
I_{IL}	Low (CK input)	V_{IN} = 0.45V		−50	−250		−50	−350	
	Output current	V_{CC} = Max							
I_{OLK}	Leakage[7]	V_{OUT} = 5.5V		1	40		1	60	μA
$I_{O(OFF)}$	Hi-Z state (82S105)[2]	V_{OUT} = 5.5V		1	40		1	60	μA
		V_{OUT} = 0.45V		−1	−40		−1	−60	
I_{OS}	Short circuit (82S105)[4,5]	V_{OUT} = 0V	−20		−70	−15		−85	mA
I_{CC}	V_{CC} supply current[9]	V_{CC} = Max		120	170		120	180	mA
	Capacitance[7]	V_{CC} = 5.0V							pF
C_{IN}	Input	V_{IN} = 2.0V		8			8		
C_{OUT}	Output	V_{OUT} = 2.0V		10			10		

NOTES

1. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device of these or any other condition above those indicated in the operation of the device specifications is not implied.
2. All typical values are at V_{CC} = 5V. T_A = 25°C.
3. All voltage values are with respect to network ground terminal.
4. Test one at a time.
5. Measured with V_{IL} applied to $\overline{O.E.}$ and a logic high stored, or with V_{IH} applied to PR.
6. Measured with a programmed logic condition for which the input is at a low logic level, and V_{IL} applied to PR/$\overline{O.E.}$ Output sink current is supplied thru a resistor to V_{CC}.
7. Measured with: V_{IH} applied to PR/$\overline{O.E.}$.
8. Duration of short circuit should not exceed 1 second.
9. I_{CC} is measured with the PR/$\overline{O.E.}$ input grounded, all other inputs at 4.5V and the outputs open.

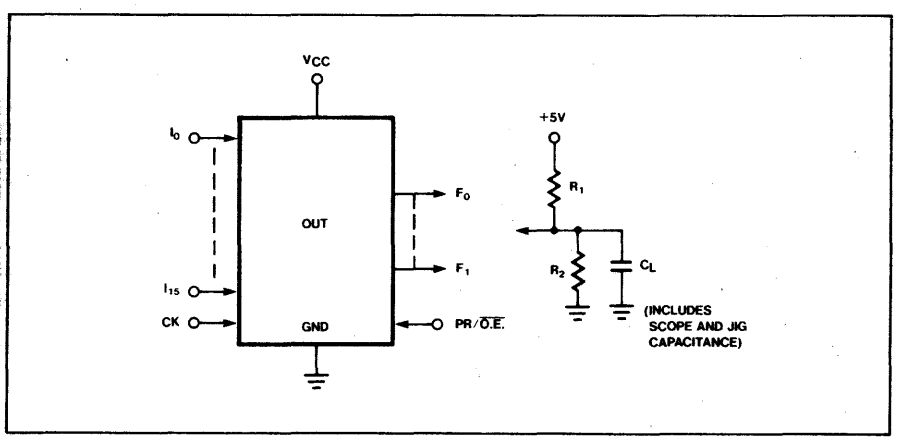
AC ELECTRIC CHARACTERISTICS

$R_1 = 470\Omega$, $R_2 = 1k\Omega$, $C_L = 30pF$
N82S104/105: $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$
S82S104/105: $-55°C \leq T_A \leq +125°C$, $4.5V \leq V_{CC} \leq 5.5V$

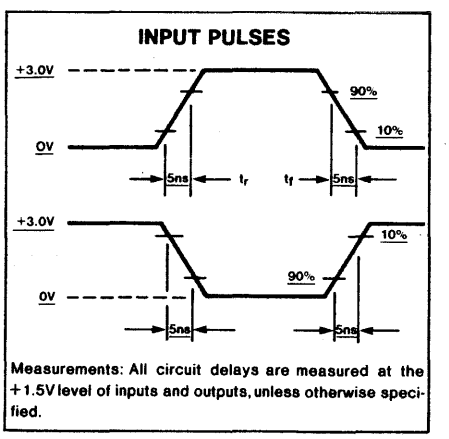
	PARAMETER	TO	FROM	N82S104/105			S82S104/105			UNIT
				Min	Typ[1]	Max	Min	Typ[1]	Max	
	Clock pulse									ns
T_{CKH}	Clock High	CK−	CK+		10			10		
T_{CKL}	Clock Low	CK+	CK−		10			10		
T_{CKP}	Period	CK+	CK+		65			65		
	Set up time									ns
T_{IS1}	Input	CK+	Input ±		40			40		
T_{IS2}	Input (through Complement array)	CK+	Input ±		70			70		
T_{VS}	Power-on preset	CK−	V_{CC}+		10			10		
T_{PRS}	Preset	CK−	PR−		−10			−10		
	Hold time									ns
T_{IH}	Input	Input ±	CK+		−15			−15		
	Propagation delay									ns
T_{CKO}	Clock	Output ±	CK+		25			25		
T_{OE}	Output enable	Output−	$\overline{O.E.}$−		25			25		
T_{OD}	Output disable	Output+	$\overline{O.E.}$+		25			25		
T_{SRE}	State register enable	Output ±	I_O+		50			50		
T_{SRD}	State register disable	Output ±	I_O−		50			50		
T_{PR}	Preset	Output+	PR+		50			50		
T_{PPR}	Power-on preset	Output+	V_{CC}+		70			70		

NOTE
1. All typical values are at $V_{CC} = 5V$, $T_A = 25°C$.

TEST LOAD CIRCUIT



VOLTAGE WAVEFORM

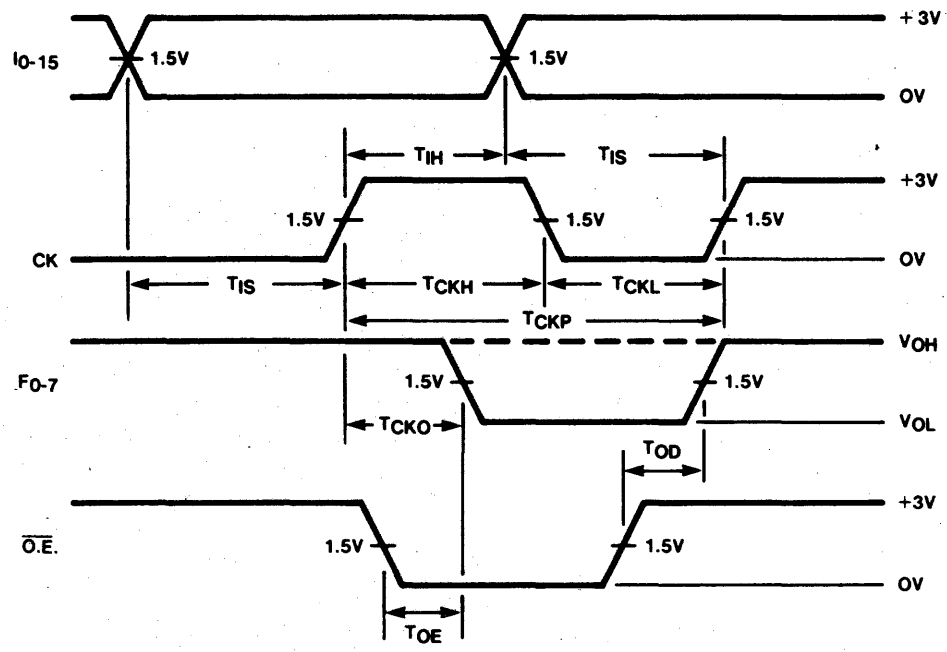


Measurements: All circuit delays are measured at the +1.5V level of inputs and outputs, unless otherwise specified.

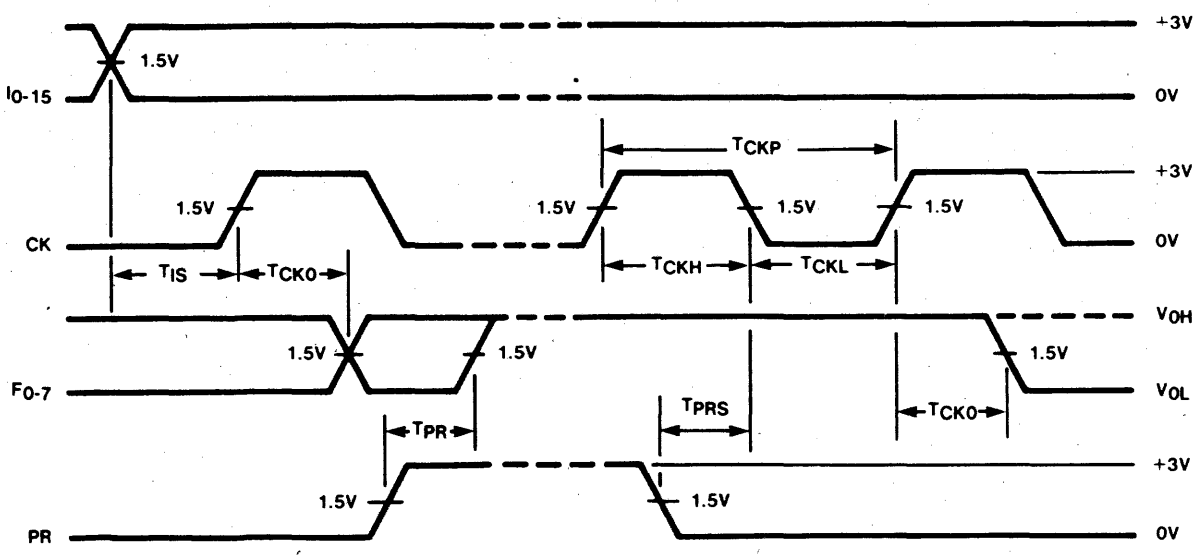
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TIMING DIAGRAMS

SEQUENTIAL MODE



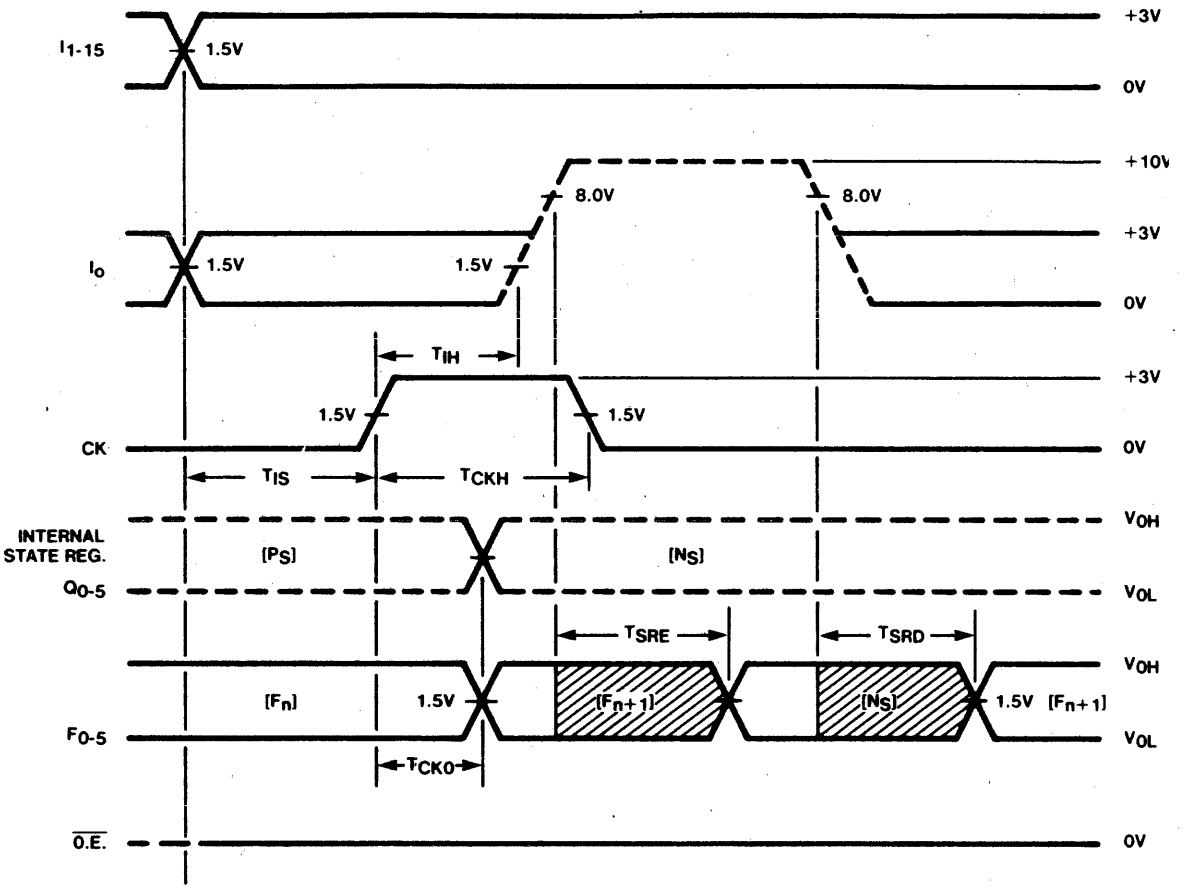
ASYNCHRONOUS PRESET



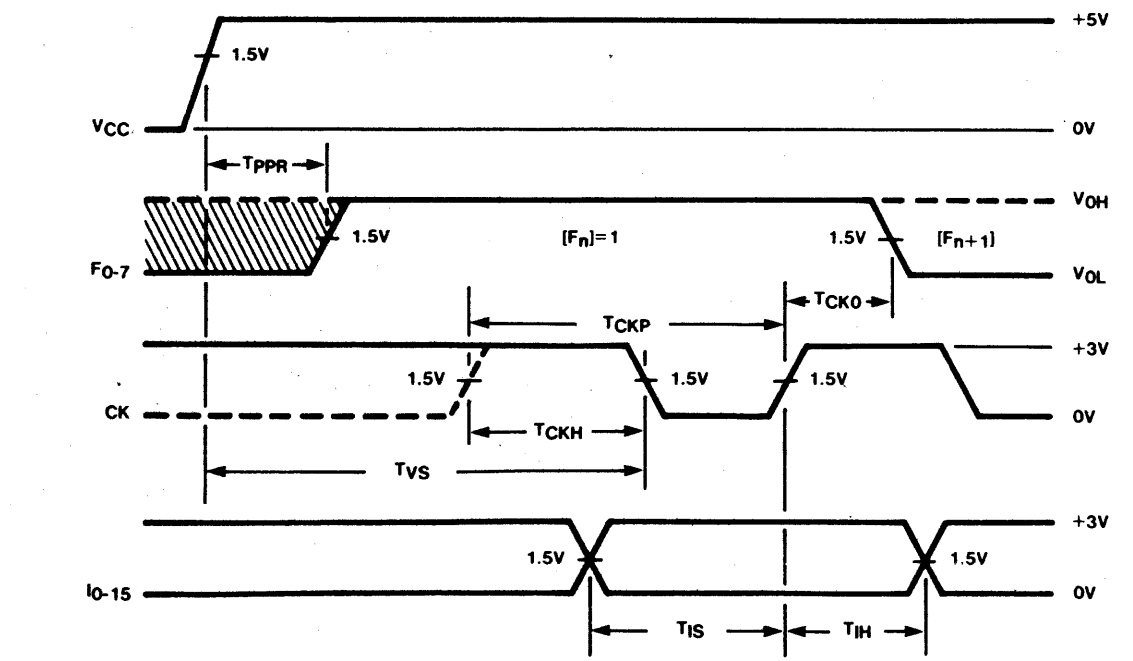
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TIMING DIAGRAMS (Cont'd)

DIAGNOSTIC MODE



POWER-ON PRESET



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MEMORY TIMING DEFINITIONS

T_{CKH} Width of input clock pulse.

T_{CKL} Interval between clock pulses.

T_{CKP} Clock period.

T_{IS1} Required delay between beginning of valid Input and positive transition of clock.

T_{IS2} Required delay between beginning of valid Input and positive transition of clock, when using optional Complement Array (two passes necessary through the AND array).

T_{VS} Required delay between V_{CC} (after power-on) and negative transition of clock preceding first reliable clock pulse.

T_{PRS} Required delay between negative transition of asynchronous Preset and negative transition of clock preceding first reliable clock pulse.

T_{IH} Required delay between positive transition of clock and end of valid Input data.

T_{CKO} Delay between positive transition of clock and when Outputs become valid (with PR/$\overline{O.E.}$ low).

T_{OE} Delay between beginning of Output Enable Low and when Outputs become valid.

T_{OD} Delay between beginning of Output Enable High and when Outputs are in the off state.

T_{SRE} Delay between input lo transition to Diagnostic mode and when the Outputs reflect the contents of the state Register.

T_{SRD} Delay between input lo transition to Logic mode and when the Outputs reflect the contents of the Output Register.

T_{PR} Delay between positive transition of Preset and when Outputs become valid at "1".

T_{PPR} Delay between V_{CC} (after power-on) and when Outputs become preset at "1".

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82S106-I,N • 82S107-I,N

DESCRIPTION

The 82S106 (Open collector outputs) and 82S107 (3-state outputs) are bipolar Programmable ROM Patches organized as 48 words by 8 bits, addressed via a 16 bit programmable address comparator. Each word can be assigned a unique address code, P_n, within a 64K (2^{16}) address range by programming the comparator inputs High, Low, or Don't care via True/Complement input buffers.

The contents of each word are also programmable, and are enabled to the active-High Patch outputs only when a programmed address is detected, which causes the $\overline{\text{Flag}}$ output to go Low. For all unprogrammed addresses, the device outputs remain High (82S106) or Hi-Z (82S107) while the $\overline{\text{Flag}}$ output remains High. The $\overline{\text{Flag}}$ is open collector to allow wire-ANDing for expansion to more than 48 patch words.

The 82S106 and 82S107 are fully TTL compatible and can be programmed in the field by following the fusing procedure outlined in this data sheet, or by means of commercially available equipment.

Both devices are available in commercial and military temperature ranges. For the commercial range (0°C to +75°C) specify N82S106/107, I or N, and for the military temperature range (-55°C to +125°C) specify S82S106/107, I.

FEATURES

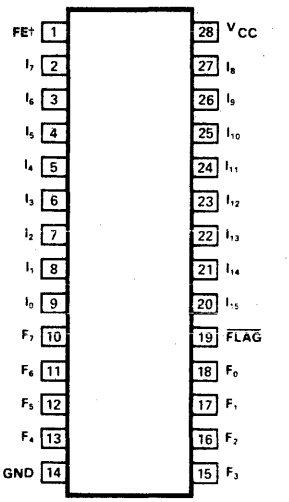
- **Field programmable (Ni-Cr link)**
- **Address Inputs: 16**
- **Data Outputs: 8**
- **Patch Words: 48**
- **Address access time:**
  S82S106/107—100ns Max
  N82S106/107—70ns Max
- **Power dissipation: 600mW typ**
- **Input loading:**
  S82S106/107: -150μA Max
  N82S106/107: -100μA Max
- **Open collector $\overline{\text{Flag}}$**
- **Output option:**
  82S106: Open collector
  82S107: 3-state
- **Output disabled state**
  3-state—Hi-Z
  Open collector—Hi

APPLICATIONS

- **ROM data modifications**
- **Memory address trap**
- **Digital filter**
- **Interrupt request/vector generator**
- **Data security encoder**

PIN CONFIGURATION

I,N PACKAGE*

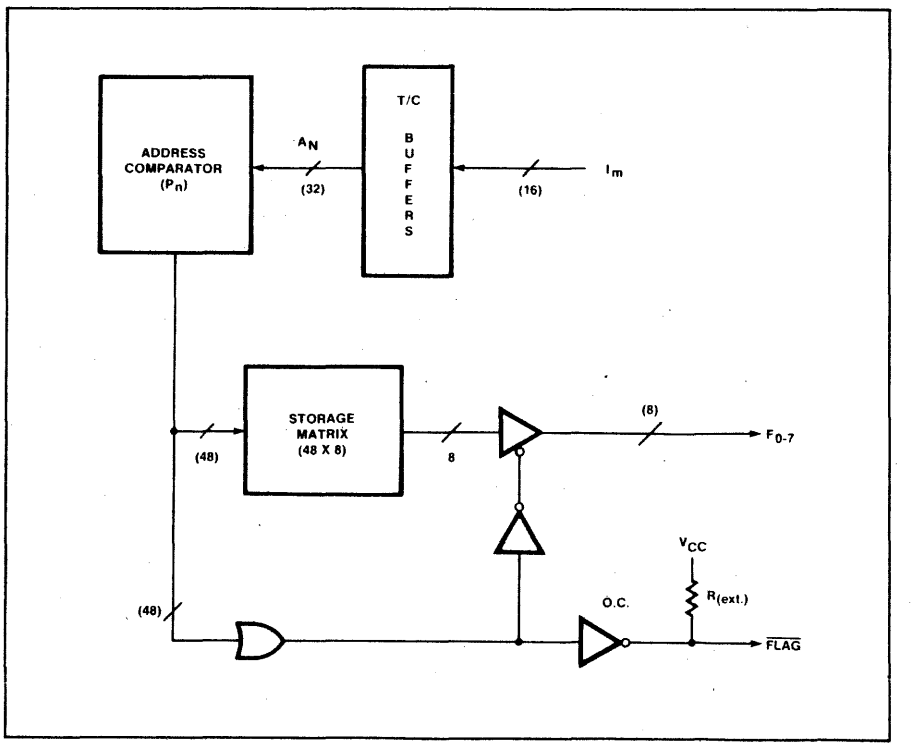


*I = Ceramic
N= Plastic
†Open during normal operation

TRUTH TABLE

? $A_N = P_N$	$\overline{\text{Flag}}$	F_{0-7}	
		82S106	82S107
NO	1	1	Hi-Z
YES	0	Stored Data	

LOGIC DIAGRAM



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ABSOLUTE MAXIMUM RATINGS[1]

PARAMETER		RATING Min	RATING Max	UNIT
V_{CC}	Supply voltage		+7	Vdc
V_{IN}	Input voltage		+5.5	Vdc
V_{OUT}	Output voltage		+5.5	Vdc
I_{IN}	Input currents	-30	+30	mA
I_{OUT}	Output currents		+100	mA
	Temperature range			°C
T_A	Operating			
	N82S106/107	0	+75	
	S82S106/107	-55	+125	
T_{STG}	Storage	-65	+150	

THERMAL RATINGS

TEMPERATURE	MILITARY	COMMERCIAL
Maximum junction	175°C	150°C
Maximum ambient	125°C	75°C
Allowable thermal rise ambient to junction	50°C	75°C

DC ELECTRICAL CHARACTERISTICS

N82S106/107: 0° ≤ T_A ≤ +75°C, 4.75V ≤ V_{CC} ≤ 5.25V

S82S106/107: -55°C ≤ T_A ≤ +125°C, 4.5V ≤ V_{CC} ≤ 5.5V

PARAMETER		TEST CONDITIONS	N82S106/107 Min	N82S106/107 Typ[2]	N82S106/107 Max	S82S106/107 Min	S82S106/107 Typ[2]	S82S106/107 Max	UNIT
	Input voltage[3]								V
V_{IH}	High	V_{CC} = Max	2			2			
V_{IL}	Low	V_{CC} = Min			0.85			0.8	
V_{IC}	Clamp[3,4]	V_{CC} = Min, I_{IN} = -18mA		-0.8	-1.2		-0.8	-1.2	
	Output voltage	V_{CC} = Min							V
V_{OH}	High (82S107)[3,5]	I_{OH} = -2mA	2.4			2.4			
V_{OL}	Low[3,6] (F_{0-7})	I_{OL} = 9.6mA		0.35	0.45		0.35	0.50	
V_{OL}	Low[3,6] ($\overline{Flag}$)	I_{OL} = 4.8mA		0.35	0.45		0.35	0.50	
	Input current								μA
I_{IH}	High	V_{IN} = 5.5V		<1	25		<1	50	
I_{IL}	Low	V_{IN} = 0.45V		-10	-100		-10	-150	
	Output current	V_{CC} = Max							
I_{OLK}	Leakage[7]	V_{OUT} = 5.5V		1	40		1	60	μA
$I_{O(OFF)}$	Hi-Z state (82S107)[7]	V_{OUT} = 5.5V		1	40		1	60	μA
		V_{OUT} = 0.45V		-1	-40		-1	-60	
I_{OS}	Short circuit (82S107)[4,8]	V_{OUT} = 0V	-20		-70	-15		-85	mA
I_{CC}	V_{CC} supply current[9]	V_{CC} = Max		120	170		120	180	mA
	Capacitance[7]	V_{CC} = 5.0V							pF
C_{IN}	Input	V_{IN} = 2.0V		8			8		
C_{OUT}	Output	V_{OUT} = 2.0V		17			17		

AC ELECTRICAL CHARACTERISTICS

R_1 = 470Ω, R_2 = 1kΩ, C_L = 30pF

N82S106/107: 0°C ≤ T_A ≤ +75°C, 4.75V ≤ V_{CC} ≤ 5.25V

S82S106/107: -55°C ≤ T_A ≤ +125°C, 4.5V ≤ V_{CC} ≤ 5.5V

PARAMETER		TO	FROM	N82S106/107 Min	N82S106/107 Typ[2]	N82S106/107 Max	S82S106/107 Min	S82S106/107 Typ[2]	S82S106/107 Max	UNIT
	Access time									ns
T_{IA}	Address	Output	Input		45	70		45	100	
T_{FL}	Enable	$\overline{Flag}$	Input		40	70		40	100	

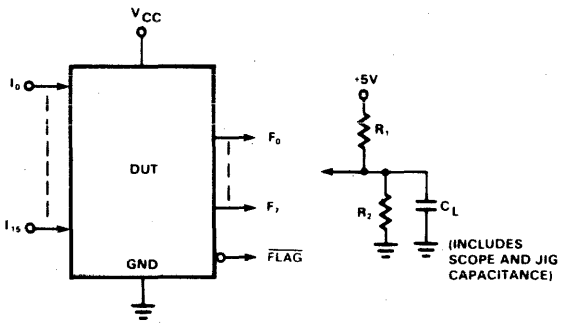
NOTES on following page.

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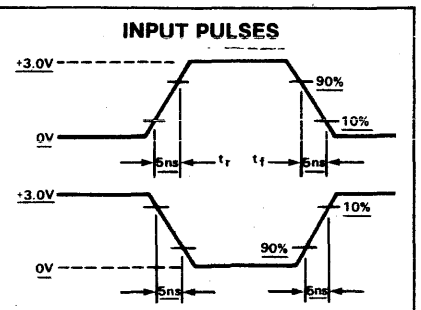
NOTES

1. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device of these or any other condition above those indicated in the operation of the device specification is not implied.
2. All typical values are at V_{CC} = 5V, T_A = 25°C.
3. All voltage values are with respect to network ground terminal.
4. Test one at the time.
5. Measured with the Patch enabled ($A_N = P_N$) and a logic high stored.
6. Measured with a programmed logic condition for which the output under test is at a low logic level when the Patch is enabled ($A_N = P_N$). Output sink current is applied thru a resistor to V_{CC}.
7. Measured with the Patch disabled ($A_N \neq P_N$).
8. Duration of short circuit should not exceed 1 second.
9. I_{CC} is measured with all inputs at 4.5V and the outputs open.

TEST LOAD CIRCUIT

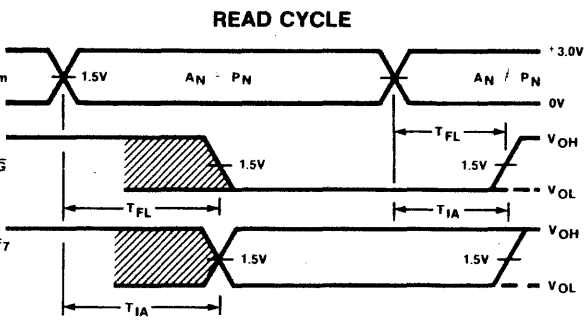


VOLTAGE WAVEFORM



Measurements: All circuit delays are measured at the +1.5V level of inputs and outputs.

TIMING DIAGRAM



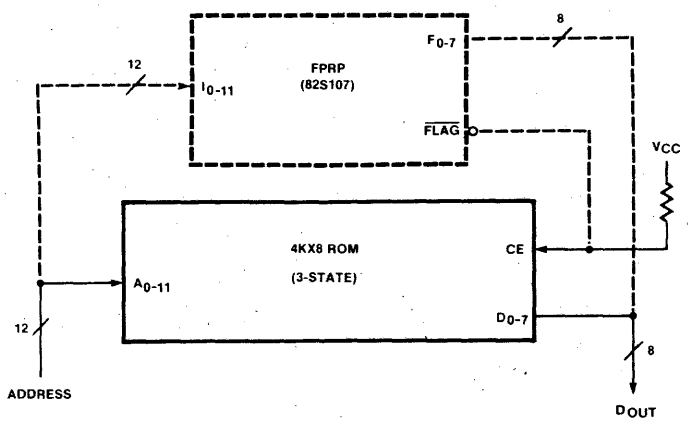
TIMING DEFINITIONS

T_{IA} Delay between latest Address variable change and when Data Output becomes stable.

T_{FL} Delay between latest Address variable change and when $\overline{Flag}$ output becomes stable.

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TYPICAL APPLICATION



PATCH SPECIFICATIONS

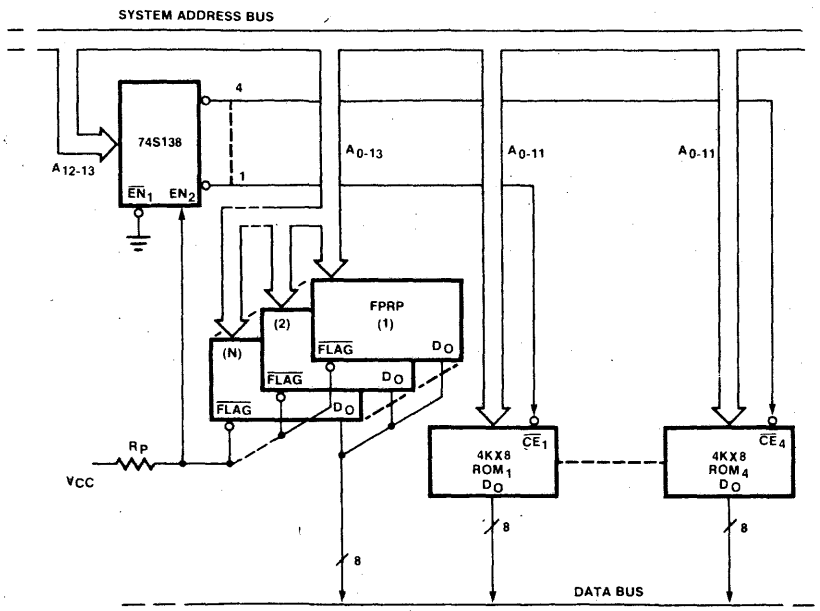
ADDRESS	NEW DATA
750	A9
5FE	7F
0A4	B4
0A5	
0A6	
0A7	

FPRP PROGRAM TABLE

INPUT ADDRESS	NO.	PRODUCT TERM: COMPARATOR INPUT 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	ACTIVE LEVEL: H H H H H H H H	OUTPUT FUNCTION 7	6	5	4	3	2	1	0	OUTPUT DATA
750	0	–	–	–	–	L	H	H	H	L	H	L	H	L	L	L	L		A	•	A	•	A	•	•	A	A9
5FE	1	–	–	–	–	L	H	L	H	H	H	H	H	H	H	H	L		•	A	A	A	A	A	A	A	7F
OA4-OA7	2	–	–	–	–	L	L	L	L	H	L	H	L	L	H	–	–		A	•	A	A	•	A	•	•	B4
I/O ASSIGNMENT		UNUSED				A_{11}											A_0		D_7							D_0	

Since Patch inputs I_{12-15} are unused, they are programmed Don't Care (–), and left open in the circuit. Note however that I_0 and I_1 are programmed as (–) in P-term 2 because they define an address block of 4 memory locations.

EXPANSION



When more than 48 memory locations need to be patched, several devices can be paralleled by wire-ANDing the $\overline{Flag}$ outputs.

82LS180-F,N • 82LS181-F,N

DESCRIPTION

The 82LS180 and 82LS181 are field programmable, which means that custom patterns are immediately available by following the fusing procedure given in this data sheet. The standard 82LS180 and 82LS181 are supplied with all outputs at logical low. Outputs are programmed to a logic high level at any specified address by fusing a Ni-Cr link matrix.

These devices include on-chip decoding and 4 chip enable inputs for ease of memory expansion. They feature either open collector or 3-state outputs for optimization of word expansion in bused organizations.

The 82LS180 and 82LS181 are available in both the commercial and military temperature ranges. For the commercial temperature range (0°C to +75°C) specify N82LS180/181, F or N, and for the military temperature range (−55°C to +125°C) specify S82LS180/181, F.

FEATURES

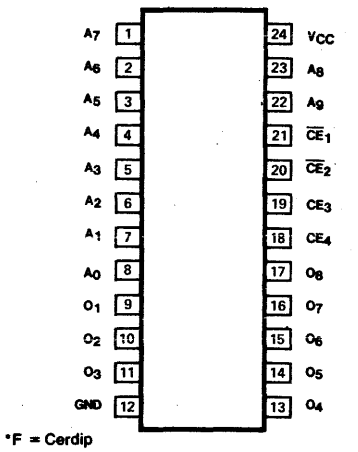
- **Address access time:**
  N82LS180/181: 175ns max
  S82LS180/181: 225ns max
- **Power dissipation: 37μW/bit typ**
- **Input loading:**
  N82LS180/181: −100μA max
  S82LS180/181: −150μA max
- **On-chip address decoding**
- **Output options:**
  82LS180: Open collector
  82LS181: 3-state
- **No separate fusing pins**
- **Unprogrammed outputs are low level**
- **Fully TTL compatible**

APPLICATIONS

- **Prototyping/volume production**
- **Sequential controllers**
- **Microprogramming**
- **Hardwired algorithms**
- **Control store**
- **Random logic**
- **Code conversion**

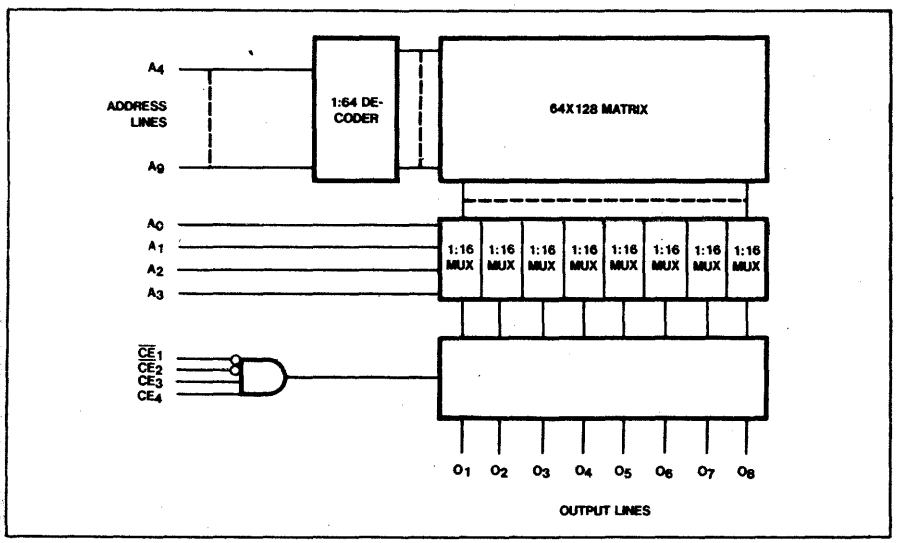
PIN CONFIGURATION

F,N PACKAGE*



*F = Cerdip
N = Plastic

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

	PARAMETER	RATING	UNIT
V_{CC}	Supply voltage	+7	Vdc
V_{IN}	Input voltage	+5.5	Vdc
	Output voltage		Vdc
V_{OH}	High (82LS180)	+5.5	
V_O	Off-state (82LS181)	+5.5	
	Temperature range		°C
T_A	Operating		
	N82LS180/181	0 to +75	
	S82LS180/181	−55 to +125	
T_{STG}	Storage	−65 to +150	

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DC ELECTRICAL CHARACTERISTICS

N82LS180/181: $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$
S82LS180/181: $-55°C \leq T_A \leq +125°C$, $4.5V \leq V_{CC} \leq 5.5V$

PARAMETER		TEST CONDITIONS		N82LS180/181			S82LS180/181			UNIT
				Min	Typ[2]	Max	Min	Typ[2]	Max	
	Input voltage									V
V_{IL}	Low					.85			.80	
V_{IH}	High			2.0			2.0			
V_{IC}	Clamp	$I_{IN} = -18mA$			−0.8	−1.2		−0.8	−1.2	
	Output voltage									V
V_{OL}	Low	$I_{OUT} = 4.8mA$				0.45			0.5	
V_{OH}	High (82LS181)	$\overline{CE}_1$ = low, $I_{OUT} = -1mA$, CE_2 = low, CE_2 = high, $\overline{CE}_4$ = high, high stored		2.4			2.4			
	Input current									μA
I_{IL}	Low	$V_{IN} = 0.45V$				−100			−150	
I_{IH}	High	$V_{IN} = 5.5V$				40			50	
	Output current									
I_{OLK}	Leakage (82LS180)	$\overline{CE}_1 = \overline{CE}_2$ = HIGH, $CE_3 = CE_4$ = LOW	$V_{OUT} = 5.5V$			40			60	μA
$I_{O(OFF)}$	Hi-Z state (82LS181)		$V_{OUT} = 0.5V$			−40			−60	μA
			$V_{OUT} = 5.5V$			40			60	μA
I_{OS}	Short circuit (82LS181)	$\overline{CE}_1 = \overline{CE}_2$ = LOW, $CE_2 = CE_3$ = HIGH	$V_{OUT} = 0V$	−10		−70	−10		−85	mA
I_{CC}	V_{CC} supply current				60	80		60	85	mA
	Capacitance	$V_{CC} = 5.0V$								pF
C_{IN}	Input	$V_{IN} = 2.0V$			5			5		
C_{OUT}	Output	$V_{OUT} = 2.0V$			8			8		

AC ELECTRICAL CHARACTERISTICS

$R_1 = 1k\Omega$, $R_2 = 2k\Omega$, $C_L = 30pF$
N82LS180/181: $0°C \leq T_A \leq +75°C$, $4.75V \leq V_{CC} \leq 5.25V$
S82LS180/181: $-55°C \leq T_A \leq +125°C$, $4.5V \leq V_{CC}$ 5.5V

PARAMETER		TO	FROM	N82LS180/181			S82LS180/181			UNIT
				Min	Typ[2]	Max	Min	Typ[2]	Max	
	Access time									ns
T_{AA}		Output	Address		100	175		100	225	
T_{CE}		Output	Chip enable		35	60		35	80	
	Disable time									ns
T_{CD}		Output	Chip disable		35	50		35	70	

NOTES

1. Positive current is defined as into the terminal referenced.
2. Typical values are at $V_{CC} = 5.0V$, $T_A = +25°C$.

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82S2708-F

DESCRIPTION

The 82S2708 is field programmable, which means that custom patterns are immediately available by following the fusing procedure given in this data sheet. The standard 82S2708 is supplied with all outputs at logical low. Outputs are programmed to a logic high level at any specified address by fusing a Ni-Cr link matrix.

This device includes on-chip decoding and 1 chip enable input for ease of memory expansion. It features tri-state outputs for optimization of word expansion in bused organizations.

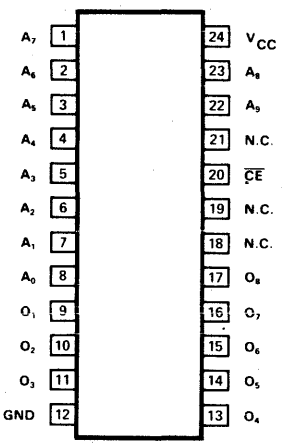
The 82S2708 is available only in the military temperature range. For the military temperature range (-55°C to +125°C) specify S82S2708.

FEATURES

- **Address access time:**
  S82S2708: 90ns max
- **Power dissipation: 85μW/bit typ**
- **Input loading:**
  S82S2708: -150μA max
- **Chip enable input**
- **On-chip address decoding**
- **No separate fusing pins**
- **Unprogrammed outputs are low level**
- **Pin for pin replacement for 2708 EROM**
- **Fully TTL compatible**

PIN CONFIGURATION

F PACKAGE*

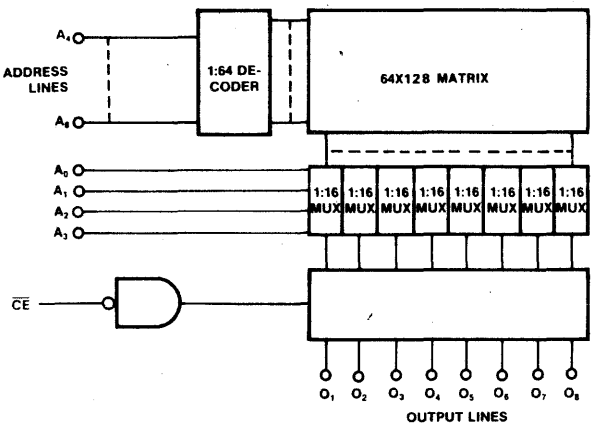


*F = Cerdip
NC = No connection

APPLICATIONS

- **Prototyping/volume production**
- **Sequential controllers**
- **Microprogramming**
- **Hardwired algorithms**
- **Control store**
- **Random logic**
- **Code conversion**

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

PARAMETER		RATING	UNIT
V_{CC}	Supply voltage	+7	Vdc
V_{IN}	Input voltage	+5.5	Vdc
	Output voltage		Vdc
V_{OH}	High	+5.5	
V_O	Off-state	+5.5	
	Temperature range		°C
T_A	Operating		
	S82S2708	-55 to +125	
T_{STG}	Storage	-65 to +150	

MEMORY

signetics

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DC ELECTRICAL CHARACTERISTICS

S82S2708: $-55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

PARAMETER		TEST CONDITIONS[1]	S82S2708 Min	S82S2708 Typ[2]	S82S2708 Max	UNIT
	Input voltage					V
V_{IL}	Low				.80	
V_{IH}	High		2.0			
V_{IC}	Clamp	I_{IN} = -18mA		-0.8	-1.2	
	Output voltage					V
V_{OL}	Low	I_{OUT} = 9.6mA			0.5	
V_{OH}	High	I_{OUT} = -2.0mA, $\overline{CE}$ = Low, High stored	2.4			
	Input current					μA
I_{IL}	Low	V_{IN} = 0.45V			-150	
I_{IH}	High	V_{IN} = 5.5V			50	
	Output current					
$I_{O(OFF)}$	Hi-Z state	$\overline{CE}$ = High, V_{OUT} = 0.5V			-60	μA
		$\overline{CE}$ = High, V_{OUT} = 5.5V			60	
I_{OS}	Short circuit	V_{OUT} = 0V	-15		-85	mA
I_{CC}	V_{CC} supply current			140	185	mA
	Capacitance	V_{CC} = 5.0V				pF
C_{IN}	Input	V_{IN} = 2.0V		5		
C_{OUT}	Output	V_{OUT} = 2.0V		8		

AC ELECTRICAL CHARACTERISTICS

$R_1 = 470\Omega$, $R_2 = 1k\Omega$, $C_L = 30pF$

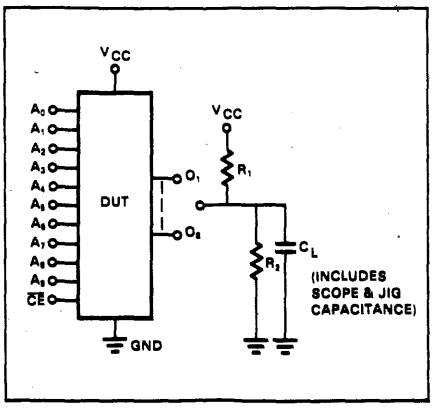
S82S2708: $-55°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$

PARAMETER		TO	FROM	S82S2708 Min	S82S2708 Typ[2]	S82S2708 Max	UNIT
	Access time						ns
T_{AA}		Output	Address		50	90	
T_{CE}		Output	Chip enable		20	50	
	Disable time						ns
T_{CD}		Output	Chip disable		20	50	

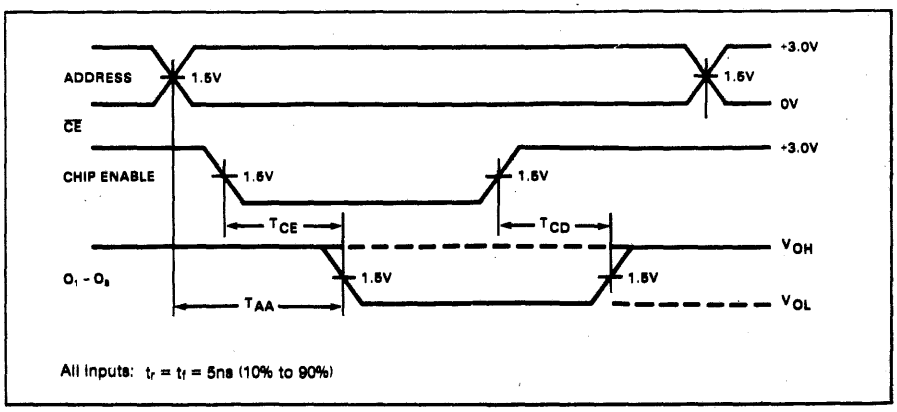
NOTES

1. Positive current is defined as into the terminal referenced.
2. Typical values are V_{CC} = 5.0V, T_A = +25°C.

TEST LOAD CIRCUIT



VOLTAGE WAVEFORM



Supertex inc.

SM74S188/288
MM74S188/288

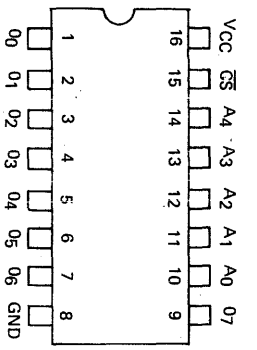
SUPER HIGH SPEED 256 BIT TTL PROGRAMMABLE READ ONLY MEMORY

Preliminary January 1979

FEATURES

- Electrically Programmable—Fuse Link
- High Speed—Schottky clamped
- Address Access—15 ns max.
- Enable Access—10 ns max.
- DTL/TTL Compatible
- Board Level Programming

Pin-Outs



DESCRIPTION

These are super high speed Schottky TTL programmable read-only Memories, organized in 32 word by 8 bit configuration. They are fully TTL input/output compatible and operate over commercial and military voltage and temperature ranges. The logic levels are "zero"s when low and "one"s when high. It can be electrically programmed in selected bit locations. All the address inputs can be used for programming and reading.

They are both available in open collector (SM 74S188 and MM 74S188) and tri-state (SM 74S288 and MM 74288) output versions.

APPLICATIONS

High Speed Logic Substitution and High Speed Programmable Logic Array

ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Min	Typ	Max	Units	Conditions
t_{AA}	Address Access Time		10	15	ns	Operating Ranges: SM74S188/288 0°C to 75°C 5V ± 5% MM74S188/288 −55°C to 125°C 5V ± 10%
t_{EA}, t_{ER}	Enable Access Time Enable Recovery Time		7	10	ns	
I_{CC}	Power Supply Current		90	130	mA	V_{CC} = Max, All inputs grounded, outputs open.

Supertex

MEMORY

1225 Bordeaux Drive • Sunnyvale, California 94086 • (408) 744-0100 • TWX910-3399388

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Supertex inc.

SM82S190/191
MM82S190/191

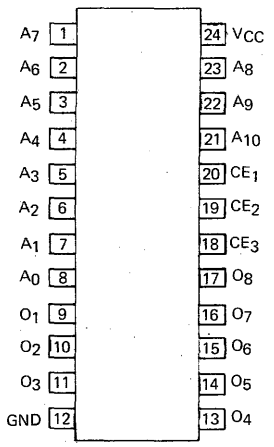
16,384 BIT TTL PROGRAMMABLE READ-ONLY MEMORY

Preliminary January 1979

FEATURES

- Fast Access Times: 40 nsec typical
- Temperature compensating for wide range of operation
- Low Voltage Programming
- Board Level Programming
- Highly reliable fuses for ultra-fast programming
- Pin for Pin replacement of Industry Standard
- Fully TTL compatible.

Pin-Outs



GENERAL DESCRIPTION

These are Memories organized in 2048 word by 8 bit configuration. The 82S190/191 are field programmable devices. This means that the desired patterns are available by following the programming procedure. These PROM's are shipped in unprogrammed forms. They have Low's in all locations. The Logical High is achieved by blowing open the fuses at the selected locations. After fusing, the state of the programming is irreversible.

These PROM's use a Supertex Proprietary Schottky Technology. This innovation makes it possible to produce a very small cell size. The design also incorporates advanced circuit and decoding techniques which contribute to the fast access times.

These devices are available with Open Collector 82S190 and Tri-State 82S191 outputs. Both of them are available in the commercial and military ranges.

OPERATING RANGES AND ACCESS TIMES

SM82S190/SM82S191	0°C to +75°C	V_{CC} = 5.0V ± 5%	t_{AA} (typ.) = 40 nsec
MM82S190/MM82S191	−55°C to +125°C	V_{CC} = 5.0V ± 10%	t_{AA} (typ.) = 50 nsec
			t_{EA} (typ.) = 20 nsec

APPLICATIONS

Microprogramming, Hardwired Algorithms, Control Store, Random Logic, Code Conversion, and Sequential Controllers.

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CM3200

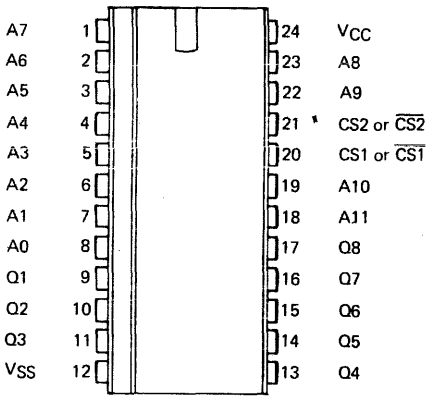
32,768 BIT STATIC CMOS READ-ONLY MEMORY

Preliminary December 1978

FEATURES

- 4096 x 8 Organization
- All Inputs and Outputs TTL Compatible
- Fully Static—No clocks or refresh
- Single 5V Power Supply
- Maximum Access Time . . . 450 ns
- Minimum Cycle Time . . . 450 ns
- Typical Operating Power Dissipation . . . 10mW/MHz
- 3-State Outputs for OR-ties
- Industry Standard Pin Configuration . . . Pin Compatible with Intel 2708, Intel 8316B, TMS 2708
- Two programmable Chip Select Inputs
- Low power CMOS Technology
- Typical Standby Power Dissipation . . . 50 uW total or 1.5 nW/bit

24-Pin Ceramic and Plastic Dual-in-Line Packages (Top View)



DESCRIPTION

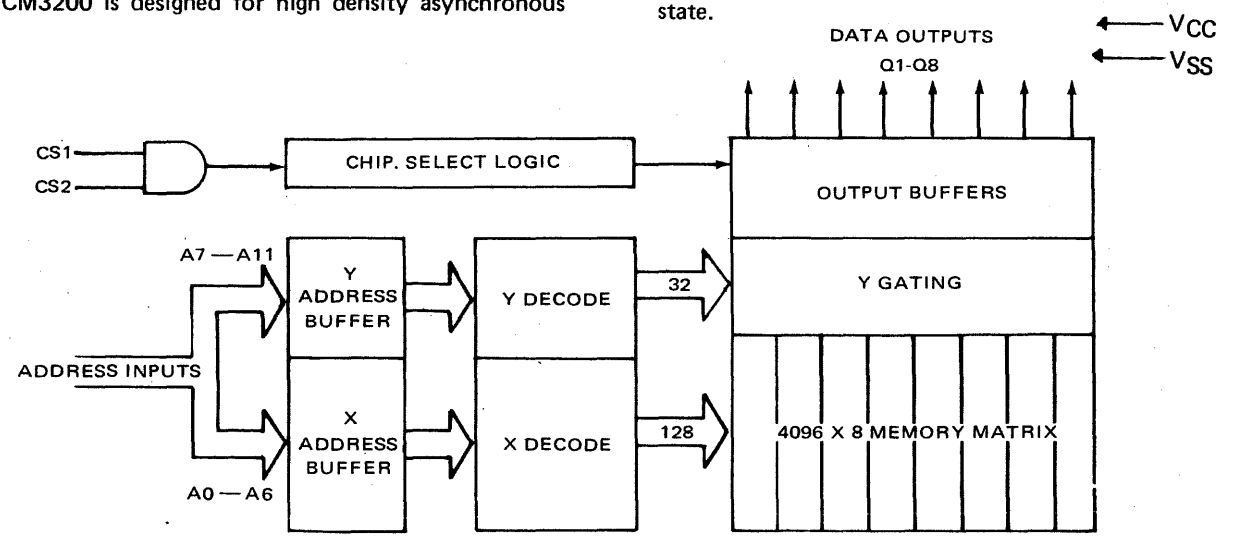
The CM3200 is a 32,768 bit read-only memory organized in 4096 word by 8 bit configuration. Low power, low cost CMOS technology and advanced circuit design makes the CM3200 ideal for microprocessor based or battery operated systems. The device operates at high speed and interface simply with TTL circuits, does not require any clock input, and yet consumes very little operating or standby power.

All inputs can be driven directly by Series 74 TTL circuits or 4000 series CMOS circuits without any external components. Each output can drive one standard TTL load. The data outputs are three-state and allows multiple devices or-tied on a common bus. Two TTL compatible chip select inputs allow easier memory expansion.

The CM3200 is designed for high density asynchronous fixed Memory applications such as look-up logic tables and microprogramming. Industry standard pin out configuration makes it very easy to replace four 8K EPROMS, two 16K ROMS or one 32K ROM for lower power dissipation and lower cost.

The CM3200 is available in 24-pin dual-in-line plastic or ceramic packages.

The 12 address inputs are decoded on-chip and selects one of 4096 word of 8 bit data. Each of the two chip select inputs are programmable to be either active high or active low level. When both chip select inputs are active, the eight outputs are enabled. When either chip select input is not active, all the eight outputs are in a high-impedance state.



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CM3200

32,768 BIT STATIC CMOS READ-ONLY MEMORY

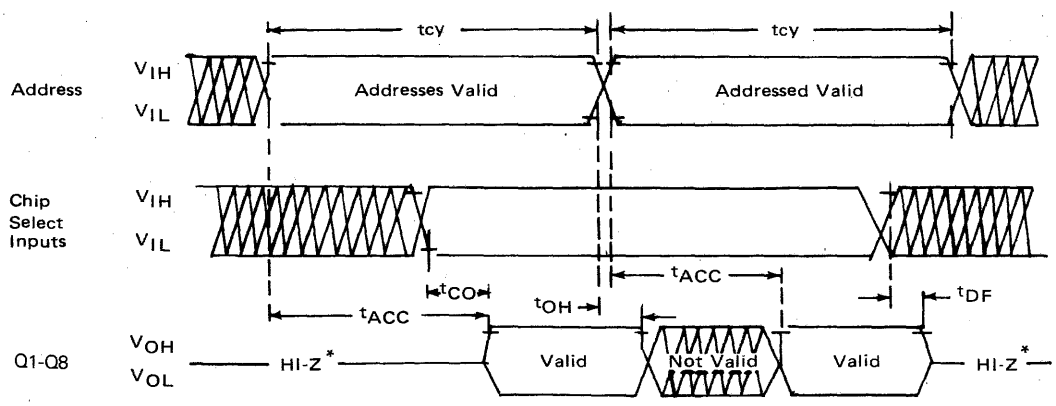
Electrical Characteristics, TA = 0°C to 70°C, V_{CC} = 5 V ± 5% (unless otherwise noted)

Parameter	Test Conditions	Min	Max	Unit
V_{OH} High Level output voltage	V_{CC}=4.75V I_{OH} =–200 uA	2.4	V_{CC}	V
V_{OL} Low-level output voltage	V_{CC} =4.75V I_{OL} = 2 mA		0.4	V
I_1 Input current	V_{CC} 5.25V V_{IN} = 5.25V		10	uA
I_{OL} Output leakage current	V_O=0.4V to V_{CC} Chip deselected		±10	uA
I_{CC} Supply current from V_{CC}	V_{CC} = 5.25V output not loaded		10	mA
C_i Input capacitance	V_O = 0 V T_A = 25°C f = 1 MHz		10	pF
C_o Output capacitance	V_O = 0 V T_A = 25°C f = 1 MHz		10	pF
V_{IH} High level input voltage		2.0	V_{CC}	V
V_{1L} Low level input voltage		V_{SS}	0.65	V

Switching characteristics, T_A = 0°C to 70°C, V_{CC} = 5V ± 5%, 1 series 74 TTL load, C_L=100 pF

Parameter		Min	Max	Units
t_{ACC}	Address Access Time		450	ns
t_{CO}	Chip Select Time		200	ns
t_{OH}	Previous Output Valid after address change	50		ns
t_{DF}	Chip Deselect Time		200	ns
t_{CY}	Cycle Time	450		ns

read cycle timing



*High Impedance

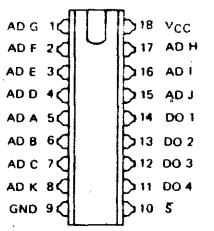
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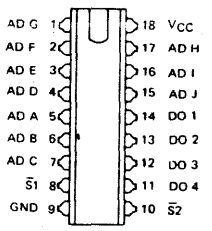
- Titanium-Tungsten (Ti-W) Fuse Links for Fast, Reliable Low-Voltage Programming
- Full Decoding and Chip Select Simplify System Design
- Fast Chip Select to Simplify System Decode
- Choice of Three-State or Open-Collector Outputs
- P-N-P Inputs for Reduced Loading on System Buffers/Drivers
- Applications Include:
  Microprogramming/Firmware Loaders
  Code Converters/Character Generators
  Translators/Emulators
  Address Mapping/Look-Up Tables

TYPE NUMBER (PACKAGES)		BIT SIZE (ORGANIZATION)	OUTPUT CONFIGURATION	TYPICAL PERFORMANCE		
				ACCESS TIMES		POWER
–55°C to 125°C	0°C to 70°C			ADDRESS	SELECT	DISSIPATION
SN54S452(J)*	SN74S452(J,N)*	16,384 bits	three-state	50 ns	20 ns	625 mW
SN54S453(J)*	SN74S453(J,N)*	2048 W x 8 B	open-collector			
SN54S454(J)	SN74S454(J,N)	8192 bits	three-state	45 ns	20 ns	625 mW
SN54S455(J)	SN74S455(J,N)	2048 W x 4 B	open-collector			
SN54S476(J)	SN74S476(J,N)	4096 bits	three-state	40 ns	20 ns	475 mW
SN54S477(J)	SN74S477(J,N)	1024 W x 4 B	open-collector			
SN54S478(J)	SN74S478(J,N)	8192 bits	three-state	45 ns	20 ns	625 mW
SN54S479(J)	SN74S479(J,N)	1024 W x 8 B	open-collector			
SN54LS478(J)*	SN74LS478(J,N)*	8192 bits	three-state	80 ns	35 ns	350 mW
SN54LS479(J)*	SN74LS479(J,N)*	1024 W x 8 B	open-collector			
SN54S2708(J)	SN74S2708(J,N)	8192 bits	three-state	45 ns	20 ns	625 mW
SN54S3708(J)	SN74S3708(J,N)	1024 W x 8 B	open-collector			

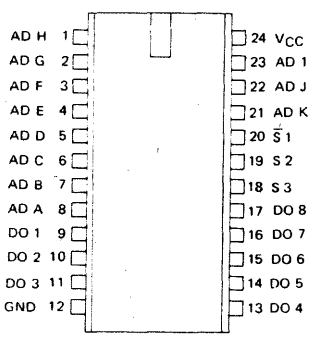
'S454, 'S455



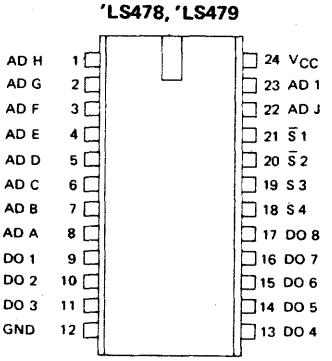
'S476, 'S477



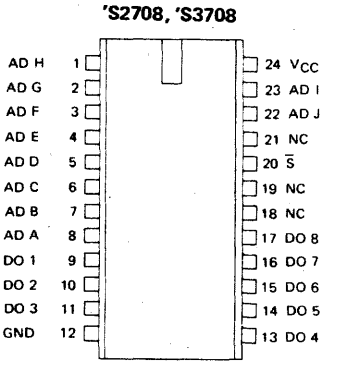
'S452, 'S453



'S478, 'S479
'LS478, 'LS479



'S2708, 'S3708



*Electrical parameters for the 'S452, 'S453, 'LS478, 'LS479 are design goals only.

DESIGN GOAL
This document provides tentative information on a product in the developmental stage. Texas Instruments reserves the right to change or discontinue this product without notice.

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†Integrated Schottky-Barrier diode-clamped transistor is patented by Texas Instruments. U. S. Patent Number 3,463,975.

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description (continued)

Data can be electronically programmed, as desired, at any bit location in accordance with the programming procedure specified. All PROM's, except the 'S287 and 'S387 are supplied with a low-logic-level output condition stored at each bit location. The programming procedure open-circuits Ti-W metal links, which reverses the stored logic level at selected locations. The procedure is irreversible; once altered, the output for that bit location is permanently programmed. Outputs never having been altered may later be programmed to supply the opposite output level. Operation of the unit within the recommended operating conditions will not alter the memory content.

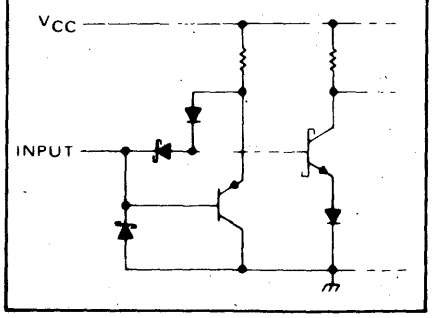
Active level(s) at the chip-select input(s) enables all of the outputs. An inactive level at any chip-select input causes all outputs to be off.

The three-state output offers the convenience of an open-collector output with the speed of a totem-pole output; it can be bus-connected to other similar outputs yet it retains the fast rise time characteristic of the TTL totem-pole output. The open-collector output offers the capability of direct interface with a data line having a passive pull-up.

schematics of inputs and outputs

'S188, 'S287, 'S288, 'S387, 'S470, 'S471, 'S472, 'S473, 'S474, 'S745

EQUIVALENT OF EACH INPUT



'S188, 'S387, 'S470 S743, 'S475

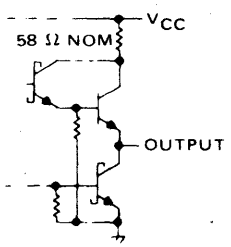
TYPICAL OF ALL OUTPUTS



Programming circuit not shown

'S287, 'S288, 'S471, 'S472, 'S474

TYPICAL OF ALL OUTPUTS



Programming circuit not shown

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage (see Note 1)		7 V
Input voltage		5.5 V
Off-state output voltage		5.5 V
Operating free-air temperature range:	SN54S' Circuits	−55°C to 125°C
	SN74S' Circuits	0°C to 70°C
Storage temperature range		−65°C to 150°C

recommended conditions for programming the 'S188, 'S287, 'S288, 'S387, 'S470 through 'S475

		SN54S', SN74S'			UNIT
		MIN	NOM	MAX	
Supply voltage, V_{CC} (see Note 1)	Steady state	4.75	5	5.25	V
	Program pulse	10	10.5	11†	
Input voltage	High level, V_{IH}	2.4		5	V
	Low level, V_{IL}	0		0.5	
Termination of all outputs except the one to be programmed		See load circuit (Figure 1)			
Voltage applied to output to be programmed, $V_{O(pr)}$ (see Note 2)		0	0.25	0.3	V
Duration of V_{CC} programming pulse Y (see Figure 2 and Note 3)		98	100	103	μs
Programming duty cycle			25	35	%
Free-air temperature		0		55	°C

†Absolute maximum ratings.

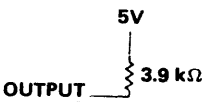
NOTES: 1. Voltage values are with respect to network ground terminal. The supply voltage rating does not apply during programming.
2. The 'S188, 'S288, 'S470, 'S471, 'S472, 'S473, 'S474, and 'S475 are supplied with all bit locations containing a low logic level, and programming a bit changes the output of the bit to high logic level. The 'S287 and 'S387 are supplied with all bit outputs at a high logic level, and programming a bit changes it to a low logic level.
3. Programming is guaranteed if the pulse applied is 98 μs in duration.

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step-by-step programming procedure for the 'S188, 'S287, 'S288, 'S387, 'S470 through 'S475

1. Apply steady-state supply voltage (V_{CC} = 5 V) and address the word to be programmed.
2. Verify that the bit location needs to be programmed. If not, proceed to the next bit.
3. If the bit requires programming, disable the outputs by applying a high-logic-level voltage to the chip-select input(s).
4. Only one bit location is programmed at a time. Connect each output not being programmed to 5 V through 3.9kΩ and apply the voltage specified in the table to the output to be programmed. Maximum current out of the programming output is 150 mA. This current flows from the programmer into the PROM output.
5. Step V_{CC} to 10.5 V nominal. Maximum supply current required during programming is 750 mA.
6. Apply a low-logic-level voltage to the chip-select input(s). This should occur between 1 μs and 1 ms after V_{CC} has reached its 10.5-V level. See programming sequence of Figure 2.
7. After the X pulse time is reached, a high logic level is applied to the chip-select inputs to disable the outputs.
8. Within 1 μs to 1 ms after the chip-select input(s) reach a high logic level, V_{CC} should be stepped down to 5 V at which level verification can be accomplished.
9. The chip-select input(s) may be taken to a low logic level (to permit program verification) 1 μs or more after V_{CC} reaches its steady-state value of 5 V.
10. At a Y pulse duty cycle of 35% or less, repeat steps 1 through 8 for each output where it is desired to program a bit.

NOTE: Only one programming attempt per bit is recommended.



LOAD CIRCUIT FOR EACH OUTPUT
NOT BEING PROGRAMMED OR FOR
PROGRAM VERIFICATION

FIGURE 1 – LOAD CIRCUIT

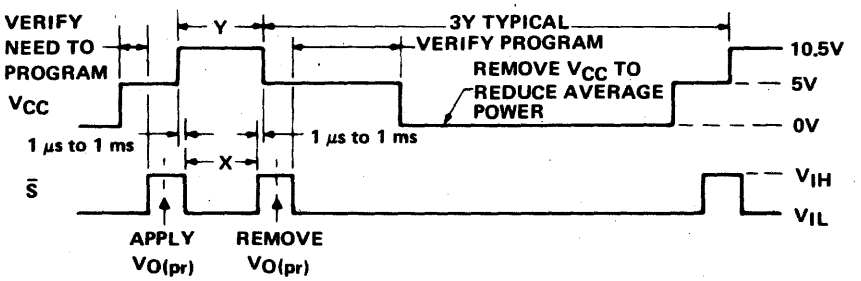


FIGURE 2 – VOLTAGE WAVEFORMS FOR PROGRAMMING

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recommended operating conditions

PARAMETER		'S287, 'S471			'S288			'S472, 'S474			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	Series 54S	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	V
	Series 74S	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	
High-level output current, I_{OH}	Series 54S			−2			−2			−2	mA
	Series 74S			−6.5			−6.5			−6.5	
Low-level output current, I_{OL}				16			20			12	mA
Operating free-air temperature, T_A	Series 54S	−55		125♦	−55		125	−55		125	°C
	Series 74S	0		70	0		70	0		70	

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		SN54S'			SN74S'			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			2			V
V_{IL}	Low-level input voltage					0.8			0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN,	I_I = −18 mA			−1.2			−1.2	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, I_{OH} = MAX	2.4	3.4		2.4	3.2		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, I_{OL} = MAX			0.5			0.5	V
I_{OZH}	Off-state output current, high-level voltage applied	V_{CC} = MAX, V_O = 2.4 V	V_{IH} = 2 V,			50			50	μA
I_{OZL}	Off-state output current, low-level voltage applied	V_{CC} = MAX, V_O = 0.5 V	V_{IH} = 2 V,			−50			−50	μA
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 5.5 V			1			1	mA
I_{IH}	High-level input current	V_{CC} = MAX,	V_I = 2.7 V			25			25	μA
I_{IL}	Low-level input current	V_{CC} = MAX,	V_I = 0.5 V			−250			−250	μA
I_{OS}	Short-circuit output current§	V_{CC} = MAX		−30		−100	−30		−100	mA
I_{CC}	Supply current	V_{CC} = MAX, Chip select(s) at 0 V, Outputs open, See Note 4	'S287		100	135		100	135	mA
			'S288		80	110		80	110	
			'S471		110	155		110	155	
			'S472, 'S474		120	155		120	155	

switching characteristics over recommended ranges of T_A and V_{CC} (unless otherwise noted)

TYPE	TEST CONDITIONS	$t_{a(ad)}$ (ns) Access time from address			$t_{a(\overline{S})}$ (ns) Access time from chip select (enable time)			t_{PXZ} (ns) Disable time from high or low level			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	
SN54S287	C_L = 30 pF for $t_{a(ad)}$ and $t_{a(\overline{S})}$ 5 pF for t_{PXZ}; R_L = 300 Ω; See Figure 2, Page 13		42	75		15	40		12	40	ns
SN74S287			42	65		15	35		12	35	ns
SN54S288			25	50		12	30		8	30	ns
SN74S288			25	40		12	25		8	20	ns
SN54S471			50	80		20	40		15	35	ns
SN74S471			50	70		20	35		15	30	ns
SN54S472, SN54S474			55	85		20	45		15	40	ns
SN74S472, SN74S474			55	75		20	40		15	35	ns

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.
♦An SN54S287 in the W package operating at free air temperatures above 108°C requires a heat sink that provides a thermal resistance from case to free air, $R_{\theta CA}$, of not more than 42°C/W.
NOTE 4: The typical values of I_{CC} shown are with all outputs low.

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recommended operating conditions

PARAMETER		'S188			'S387, 'S470			'S473, 'S475			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	Series 54S	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	V
	Series 74S	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	
High-level output voltage, V_{OH}				5.5			5.5			5.5	V
Low-level output current, I_{OL}				20			16			12	mA
Operating free-air temperature, T_A	Series 54S	−55		125	−55		125♦	−55		125	°C
	Series 74S	0		70	0		70	0		70	

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		MIN	TYP‡	MAX	UNIT
V_{IH}	High-level input voltage			2			V
V_{IL}	Low-level input voltage					0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN,	I_I = −18 mA			−1.2	V
I_{OH}	High-level output current	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V	V_{OH} = 2.4 V			50	μA
			V_{OH} = 5.5 V			100	
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IL} = 0.8 V,	V_{IH} = 2 V, I_{OL} = MAX			0.5	V
I_I	Input current at maximum input voltage	V_{CC} = MAX,	V_I = 5.5 V			1	mA
I_{IH}	High-level input current	V_{CC} = MAX,	V_I = 2.7 V			25	μA
I_{IL}	Low-level input current	V_{CC} = MAX,	V_I = 0.5 V			−250	μA
I_{CC}	Supply current	V_{CC} = MAX, Chip select(s) at 0 V, Outputs open, See Note 4	'S188		80	110	mA
			'S387		100	135	
			'S470		110	155	
			'S473; 'S475		120	155	

switching characteristics over recommended ranges of T_A and V_{CC} (unless otherwise noted)

TYPE	TEST CONDITIONS	$t_{a(ad)}$ Access time from address			$t_{a(\overline{S})}$ Access time from chip select (enable time)			t_{PLH} Propagation delay time, low-to-high-level output from chip select (disable time)			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	
SN54S188	C_L = 30 pF, R_{L1} = 300 Ω, R_{L2} = 600 Ω, See Figure 1, Page 13		25	50		12	30		12	30	ns
SN74S188			25	40		12	25		12	25	ns
SN54S387			42	75		15	40		15	40	ns
SN74S387			42	65		15	35		15	35	ns
SN54S470			50	80		20	40		15	35	ns
SN74S470			50	70		20	35		15	30	ns
SN54S473, SN54S475			55	85		20	45		15	40	ns
SN74S743, SN74S475			55	75		20	40		15	35	ns

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
♦A SN54S387 in the W package operating at free-air temperatures above 108°C requires a heat sink that provides a thermal resistance from case-to free-air, $R_{\theta CA}$, of not more than 42°C/W.
NOTE 4: The typical values of I_{CC} shown are with all outputs low.

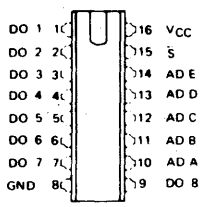
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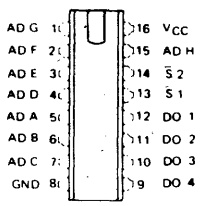
- Titanium-Tungsten (Ti-W) Fuse Links for Fast, Low-Voltage, Reliable Programming
- All Schottky-Clamped PROM's Offer:
  - Fast Chip Select to Simplify System Decode
  - Choice of Three-State or Open-Collector Outputs
  - P-N-P Inputs for Reduced Loading on System Buffers/Drivers
- Full Decoding and Chip Select Simplify System Design
- Applications Include:
  - Microprogramming/Firmware Loaders
  - Code Converters/Character Generators
  - Translators/Emulators
  - Address Mapping/Look-Up Tables

TYPE NUMBER (PACKAGES)		BIT SIZE (ORGANIZATION)	OUTPUT CONFIGURATION	TYPICAL PERFORMANCE	
–55°C to 125°C	0°C to 70°C			ADDRESS ACCESS TIME	POWER DISSIPATION
SN54S188(J, W)	SN74S188(J, N)	256 bits (32 W x 8 B)	open-collector	25 ns	400 mW
SN54S288(J, W)	SN74S288(J, N)		three-state		
SN54S287(J, W)	SN74S287(J, N)	1024 bits (256 W x 4 B)	three-state	42 ns	500 mW
SN54S387(J, W)	SN74S387(J, N)		open-collector		
SN54S470(J)	SN74S470(J, N)	2048 bits (256 W x 8 B)	open-collector	50 ns	550 mW
SN54S471(J)	SN74S471(J, N)		three-state		
SN54S472(J)	SN74S472(J, N)	4096 bits (512 W x 8 B)	three-state	55 ns	600 mW
SN54S473(J)	SN74S473(J, N)		open-collector		
SN54S474(J, W)	SN74S474(J, N)	4096 bits (512 W x 8 B)	three-state	55 ns	600 mW
SN54S475(J, W)	SN74S475(J, N)		open-collector		

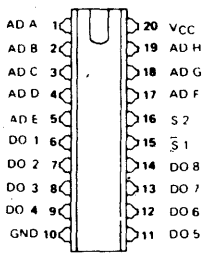
256 BITS (32 WORDS BY 8 BITS) 'S188, 'S288



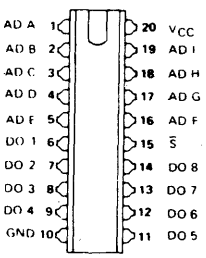
1024 BITS (256 WORDS BY 4 BITS) 'S287, 'S387



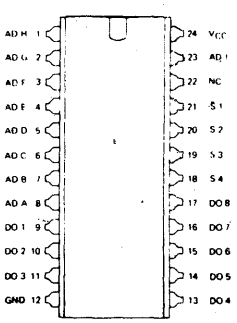
2048 BITS (256 WORDS BY 8 BITS) 'S470, 'S471



4096 BITS (512 WORDS BY 8 BITS) 'S472, 'S473



4096 BITS (512 WORDS BY 8 BITS) 'S474, 'S475



Pin assignments for all of these memories are the same for all packages.

description

These monolithic TTL programmable read-only memories (PROM's) feature titanium-tungsten (Ti-W) fuse links with each link designed to program with a 100 microsecond pulse. These PROM's offer considerable flexibility for upgrading existing designs or improving new designs as they feature full Schottky clamping for improved performance, low-current MOS-compatible p-n-p inputs, choice of bus-driving three state or open-collector outputs, and improved chip-select access times.

The high-complexity 2048- and 4096-bit 20-pin PROM's can be used to significantly improve system density for fixed memories as all are offered in dual-in-line packages having pin-row spacings of 0.300 inch.

PRELIMINARY DATA SHEET: Supplementary data may be published at a later date.

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†Integrated Schottky-Barrier diode-clamped transistor is patented by Texas Instruments. U. S. Patent Number 3,463,975.

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recommended operating conditions

PARAMETER		'S452* 'S478, 'S2708			'S454, 'S476			'LS478*			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	54 Family	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	V
	74 Family	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	
High-level output current, I_{OH}	54 Family			−2			−2			−2	mA
	74 Family			−3.2			−3.2			−1.6	
Low level output current, I_{OL}	54 Family			12			16			4	mA
	74 Family			12			16			8	
Operating free-air temperature range	54 Family	−55		125	−55		125	−55		125	°C
	74 Family	0		70	0		70	0		70	

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		'S452*, 'S454 'S478, 'S2708			'S476			'LS478*			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			2			2			V
V_{IL}	Low-level input voltage					0.8			0.8			0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = −18 mA				−1.2			−1.2			−1.2	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = MAX		2.4	3.1		2.4	3.1		2.4	3.1		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = MAX	54 Family			0.5			0.5			0.5	V
			74 Family			0.5			0.5			0.45	
I_{OZH}	Off-state output current, high-level voltage applied	V_{CC} = MAX, V_{IH} = 2 V, V_O = 2.4 V				50			50			50	μA
I_{OZL}	Off-state output current, low-level voltage applied	V_{CC} = MAX, V_{IH} = 2 V, V_O = 0.5 V				−50			−50			−50	μA
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V				1			1			1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7 V				25			25			25	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.5 V				−250			−250			−250	μA
I_{OS}	Short-circuit output current§	V_{CC} = MAX	54 Family	−15		−100	−15		−100	−10		−100	mA
			74 Family	−20		−100	−20		−100	−10		−100	
I_{CC}	Supply current	V_{CC} = MAX	54 Family		125	185		95	140		70		mA
			74 Family		125	175		95	140		70		

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡All typical values are at V_{CC} = 5 V, T_A = 25°C.
§Not more than one output should be shorted at a time, and duration of the short circuit should not exceed one second.

switching characteristics over recommended ranges of T_A and V_{CC} (unless otherwise noted)

TYPE		TEST CONDITIONS		$t_{a(ad)}$ Access time from address			$t_{a(s)}$ Access time from chip select (enable time)			t_{pxz} Disable time			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
'S452*		C_L = 30 pF for $t_{a(ad)}$ and $t_{a(s)}$, C_L = 5 pF for t_{pxz}, See Note 3	R_L = 300 Ω		50			20			20		ns
'S454					45			20			20		ns
'S476	54 Family				40	75		20	40		20	40	ns
	74 Family				40	60		20	30		20	30	
'S478, 'S2708	54 Family				45	90		20	50		20	50	ns
	74 Family				45	70		20	40		20	40	
'LS478*			R_L = 600 Ω		80			35			35		ns

NOTE 3: Load circuits are shown in Figure 2, page 13, section 4 of *The Bipolar Microcomputer Components Data Book*, December 1977.
•Electrical parameters for 'S452, 'S453, 'LS478, 'LS479 are design goals only.

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recommended operating conditions

PARAMETER		'S453* 'S479, 'S3708			'S455, 'S477			'LS479*			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	54 Family	4.5	5	5.5	4.5	5	5.5	4.5	5	5.5	V
	74 Family	4.75	5	5.25	4.75	5	5.25	4.75	5	5.25	
High-level output voltage, V_{OH}				5.5			5.5			5.5	V
Low level output current, I_{OL}	54 Family			12			16			4	mA
	74 Family			12			16			8	
Operating free-air temperature range	54 Family	−55		125	−55		125	−55		125	°C
	74 Family	0		70	0		70	0		70	

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		'S453*, 'S455 'S479, 'S3708			'S477			'LS479*			UNIT
				MIN	TYP‡	MAX	MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IH}	High-level input voltage			2			2			2			V
V_{IL}	Low-level input voltage					0.8			0.8			0.8	V
V_{IK}	Input clamp voltage	V_{CC} = MIN, I_I = −18 mA				−1.2			−1.2			−1.2	V
I_{OH}	High-level output current	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V	V_O = 2.4 V			50			50			50	μA
			V_O = 5.5 V			100			100			100	
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = 0.8 V, I_{OL} = MAX	54 Family			0.5			0.5			0.5	V
			74 Family			0.5			0.5			0.45	
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V				1			1			1	mA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.7 V				25			25			25	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.5 V				−250			−250			−250	μA
I_{CC}	Supply current	V_{CC} = MAX	54 Family		125	185		95	140		70		mA
			74 Family		125	175		95	140		70		

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

switching characteristics over recommended ranges of T_A and V_{CC} (unless otherwise noted)

TYPE		TEST CONDITIONS	$t_{a(ad)}$ Access time from address			$t_{a(s)}$ Access time from chip select (enable time)			t_{PLH} Propagation delay time, low-to-high-level output from chip select			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
'S453*		C_L = 30 pF, See Note 4		50			20			20		ns
'S455				45			20			20		ns
'S477	54 Family			40	75		20	40		20	40	ns
	74 Family			40	60		20	30		20	30	
'S479, 'S3708	54 Family			45	90		20	50		20	50	ns
	74 Family			45	70		20	40		20	40	
'LS479*				80			35			35		ns

NOTE 4: Load circuits are shown in Figure 1, page 13, section 4 of *The Bipolar Microcomputer Components Data Book*, December 1977. For 'LS479 R_{L1} = 600 Ω and R_{L2} = 1.2 kΩ. For all other devices R_{L1} = 300 Ω and R_{L2} = 600 Ω.

*Electrical parameters for 'S452, 'S453, 'LS478, 'LS479 are design goals only.

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recommended conditions for programming*

PARAMETER		MIN	TYP	MAX	UNIT
Steady-state supply voltage, V_{CC}		4.5	5	5.5	V
Address input voltage	V_{IH}	2.4		5	V
	V_{IL}	0		0.5	
S3 and S4 input voltage (where appropriate)	V_{IH}	2.4		5	V
Voltage at all outputs except the one to be programmed		0		0.5	V
Supply voltage programming pulse (see Figure 1)	Voltage, $V_{CC(pr)}$	5.75	6	6.25	V
	Pulse width, t_w	1000		2000	μs
	Duty cycle		25	35	%
$\overline{S}$, $\overline{S1}$ or $\overline{S2}$ programming pulse (see Figure 1)	Voltage, $V_{\overline{S}(pr)}$	9.75	10	11	V
	V_{IL}	0		0.5	
Output programming pulse (see Figure 1)	Voltage, $V_{O(pr)}$	16.75	17	17.25	V
	Rise time, t_r	10		50	μs
	Pulse width, t_w	98	100	1000	μs
	V_{IL}	0		0.5	
Free-air temperature, T_A		0		55	°C

step-by-step programming instructions (see Figure 1)

1. Address the word to be programmed, apply 5 V ± 10% to V_{CC} and active levels to all chip select (S and $\overline{S}$) inputs.
2. Verify the status of a bit location by checking the output level.
3. Increase V_{CC} to $V_{CC(pr)}$ with a minimum current capability of 200 milliamperes.
4. Apply $V_{\overline{S}(pr)}$ to all the $\overline{S}$ inputs. $I_I \leqslant 5$ mA.
5. Connect all outputs, except the one to be programmed, to a logic low level ($0 \leqslant V_{IL} \leqslant 0.5$ V). Only one bit is programmed at a time.
6. Apply the output programming pulse for at least 98 microseconds. Minimum current capability of the programming supply should be 200 milliamperes.
7. After terminating the output pulse, disconnect all outputs from V_{IL} conditions.
8. Reduce the voltage at $\overline{S}$ inputs to V_{IL}.
9. Reduce V_{CC} to steady-state voltage and verify output status.
10. Repeat Steps 3 thru 9 for each bit location that requires programming. Only one programming attempt per bit is recommended.
11. Verify accurate programming of every word after all words have been programmed using V_{CC} values of 4.5 and 5.5 volts.

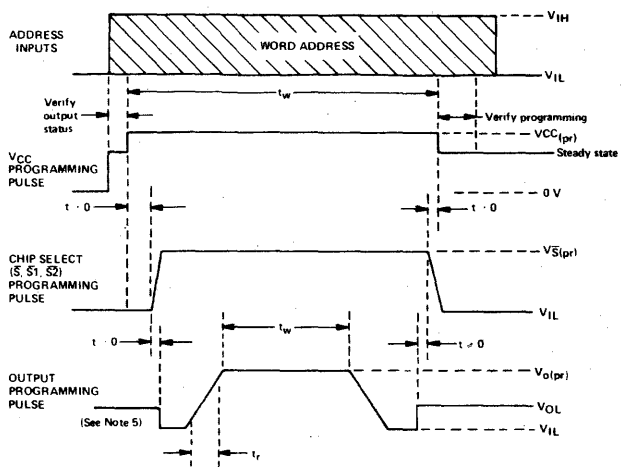


FIGURE 1–TIMING DIAGRAM AND VOLTAGE WAVEFORMS FOR PROGRAMMING SEQUENCE

NOTE 5: The output to be programmed may be forced to zero volts after the transition to $V_{O(pr)}$ at the $\overline{S}$ input has begun.

*Electrical parameters for the 'S452, 'S453, 'LS478, 'LS479 are design goals only.

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TYPES SN54LS668, SN54LS669, SN74LS668, SN74LS669
SYNCHRONOUS 4-BIT UP/DOWN COUNTERS

BULLETIN NO. DL-S 12517, APRIL 1977—REVISED NOVEMBER 1977

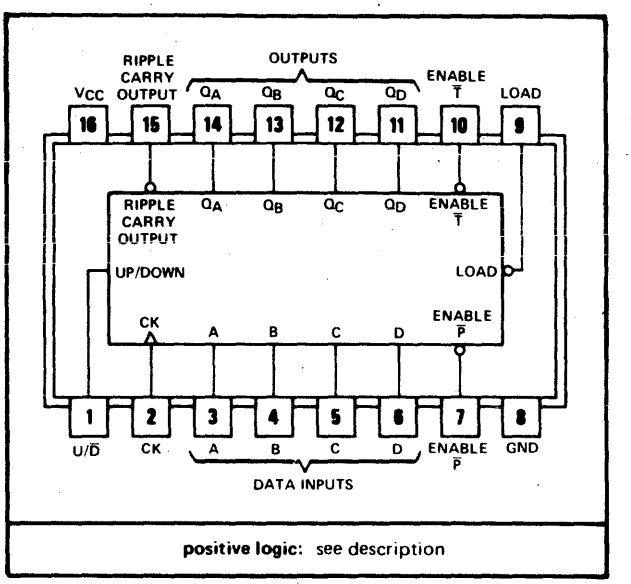
'LS668 . . . SYNCHRONOUS UP/DOWN DECADE COUNTERS
'LS669 . . . SYNCHRONOUS UP/DOWN BINARY COUNTERS

Programmable Look-Ahead Up/Down Binary/Decade Counters

- **Fully Synchronous Operation for Counting and Programming**
- **Internal Look-Ahead for Fast Counting**
- **Carry Output for n-Bit Cascading**
- **Fully Independent Clock Circuit**
- **Buffered Outputs**

TYPE	TYPICAL MAXIMUM CLOCK FREQUENCY		TYPICAL POWER DISSIPATION
	COUNTING UP	COUNTING DOWN	
'LS668, 'LS669	35 MHz	35 MHz	100 mW

SERIES SN54LS' . . . J OR W PACKAGE
SERIES SN74LS' . . . J OR N PACKAGE
(TOP VIEW)



positive logic: see description

description

These synchronous presettable counters feature an internal carry look-ahead for cascading in high-speed counting applications. The 'LS668 are decade counters and the 'LS669 are 4-bit binary counters. Synchronous operation is provided by having all flip-flops clocked simultaneously so that the outputs change coincident with each other when so instructed by the count-enable inputs and internal gating. This mode of operation helps eliminate the output counting spikes that are normally associated with asynchronous (ripple-clock) counters. A buffered clock input triggers the four master-slave flip-flops on the rising (positive-going) edge of the clock waveform.

These counters are fully programmable; that is, the outputs may each be preset to either level. The load input circuitry allows loading with the carry-enable output of cascaded counters. As loading is synchronous, setting up a low level at the load input disables the counter and causes the outputs to agree with the data inputs after the next clock pulse.

The carry look-ahead circuitry provides for cascading counters for n-bit synchronous applications without additional gating. Instrumental in accomplishing this function are two count-enable inputs and a carry output. Both count enable inputs ($\overline{P}$ and $\overline{T}$) must be low to count. The direction of the count is determined by the level of the up/down input. When the input is high, the counter counts up; when low, it counts down. Input $\overline{T}$ is fed forward to enable the carry output. The carry output thus enabled will produce a low-level output pulse with a duration approximately equal to the high portion of the Q_A output when counting up and approximately equal to the low portion of the Q_A output when counting down. This low-level overflow carry pulse can be used to enable successive cascaded stages. Transitions at the enable $\overline{P}$ or $\overline{T}$ inputs are allowed regardless of the level of the clock input. All inputs are diode-clamped to minimize transmission-line effects, thereby simplifying system design.

These counters feature a fully independent clock circuit. Changes at control inputs (enable $\overline{P}$, enable $\overline{T}$, load, up/down) that will modify the operating mode have no effect until clocking occurs. The function of the counter (whether enabled, disabled, loading, or counting) will be dictated solely by the conditions meeting the stable setup and hold times.

The 'LS668 and 'LS669 are completely new designs. Compared to the original 'LS168 and 'LS169, they feature 0-nanosecond minimum hold time, reduced input currents I_{IH} and I_{IL}, and all buffered outputs.

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recommended operating conditions

		SN54LS668 SN54LS669			SN74LS668 SN74LS669			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}		4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}				−400			−400	μA
Low-level output current, I_{OL}				4			8	mA
Clock frequency, f_{clock}		0		25	0		25	MHz
Width of clock pulse, $t_{w(clock)}$ (high or low)		25			25			ns
Setup time, t_{su}	Data inputs A, B, C, D	20			20			ns
	Enable $\overline{P}$ or $\overline{T}$	20			20			
	Load	25			25			
	Up/Down	30			30			
Hold time at any input with respect to clock, t_h		0			0			ns
Operating free-air temperature, T_A		−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS		SN54LS668 SN54LS669			SN74LS668 SN74LS669			UNIT
					MIN	TYP	MAX	MIN	TYP	MAX	
V_{IH}	High-level input voltage				2			2			V
V_{IL}	Low-level input voltage						0.7			0.8	V
V_{IK}	Input clamp voltage		V_{CC} = MIN,	I_I = −18 mA			−1.5			−1.5	V
V_{OH}	High-level output voltage		V_{CC} = MIN, V_{IL} = V_{IL} max,	V_{IH} = 2 V, I_{OH} = −400 μA	2.5	3.4		2.7	3.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, V_{IH} = 2 V, V_{IL} = V_{IL} max	I_{OL} = 4 mA		0.25	0.4		0.25	0.4	V
				I_{OL} = 8 mA					0.35	0.5	
I_I	Input current at maximum input voltage	A, B, C, D, $\overline{P}$, U/$\overline{D}$	V_{CC} = MAX,	V_I = 7 V			0.1			0.1	mA
		Clock, $\overline{T}$					0.1			0.1	
		Load					0.2			0.2	
I_{IH}	High-level input current	A, B, C, D, $\overline{P}$, U/$\overline{D}$	V_{CC} = MAX,	V_I = 2.7 V			20			20	μA
		Clock, $\overline{T}$					20			20	
		Load					40			40	
I_{IL}	Low-level input current	A, B, C, D, $\overline{P}$, U/$\overline{D}$	V_{CC} = MAX,	V_I = 0.4 V			−0.4			−0.4	mA
		Clock, $\overline{T}$					−0.4			−0.4	
		Load					−0.8			−0.8	
I_{OS}	Short-circuit output current		V_{CC} = MAX		−20		−100	−20		−100	mA
I_{CC}	Supply current		V_{CC} = MAX			20	34		20	34	mA

switching characteristics, V_{CC} = 5 V, T_A = 25°C

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{max}			C_L = 15 pF, R_L = 2 kΩ	25	32		MHz
t_{PLH}	Clock	Ripple carry			26	40	ns
t_{PHL}					40	60	
t_{PLH}	Clock	Any Q			18	27	ns
t_{PHL}					18	27	
t_{PLH}	Enable $\overline{T}$	Ripple carry			11	17	ns
t_{PHL}					29	45	
t_{PLH}	Up/Down	Ripple carry			22	35	ns
t_{PHL}					26	40	

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INTRODUCTION TO MICROPROCESSORS

This section describes microprocessors from 32 manufacturers. First, there is the "Master Selection Guide" for microprocessors. A complete survey, it covers all major areas of information needed to choose a microprocessor for a particular application. Next is the "System Components" section. Arranged alphanumerically by microprocessor, it shows all the available peripheral devices that work with a particular microprocessor. Finally, there is a "General Purpose" section describing devices that can be used in different microprocessor systems, not necessarily with one family.

Those manufacturers and page numbers listed below in **BOLD PRINT,** are providing detailed information on the latest and most significant products.

INDEX TO MICROPROCESSOR SECTION

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MICROPROCESSORS

Manufacturer Model For Detailed Data See:	AMD AM2901/AM2901A	AMD AM2903	AMD 9080A	AMI S2000/A (Page 1764)
General Structure	4-Bit Slice	4-Bit Slice	8-Bit CPU	4-Bit Microcomputer
Type	TTL	TTL	NMOS	NMOS
No. of Devices per CPU	Varies	Varies	1	1
CPU Size (Pins)	40	48	40	40
Supply Voltage	5	5	±5, 12	9
CPU Power Dissipation (mw)	925	1750	830	250
Architecture Data Word Size (bits)	Multiple of 4	Multiple of 4	8	4 (8-Bit I/O Bus)
Instruction Word Size (bits)	User defined	User defined	8, 16, 24	8
Directly Addressable Instruction Words (No.)	User defined	User defined	65K	8K
Clock Frequency (Hz/ext. phases required)	to 10 MHz/1 phase	to 10 MHz/1 phase	to 4 MHz/2 phase	85ϕ kHz/1 phase
Register to Register Add Time (μsec/data word)	0.125/0.145	0.145	2 (2 MHz clock)	5
No. of Registers Arithmetic	0	0	1	1
Index	0	0	0	2
General Purpose	17	17 (expandable)	6	1
Return Stack Size (No. x bits)	4x4, 5x5 (2909); 17x17 (2930)	4x4, 5x5 (2909); 17x17 (2930)	External RAM	3x10
Interrupts	Optional (2914)	Optional (2924)	Standard	None
Type	Vectored	Vectored	Vectored 8 Level	
Direct Memory Access	Optional (2940)	Optional (2940)	Standard	None
BCD Arithmetic (Hardware)	No	No	Yes	No
Microprogrammable	Yes	Yes	No	No
Extended Temp. Range Available	−55°C to 125°C	−55°C to 125°C	−55°C to 125°C	Yes
Devices See System Components:	2900	2900	8080	2000
Hardware Support Processor Cards (CPU system on a card)	Yes	Yes	No	Yes (Emulator)
Prototyping System (Hardware & software development system)	Yes	Yes	No	Yes
In-System Emulator (Tests system in place)	Yes	Yes	No	Yes
Software Support (from this manufacturer) Resident Assembler	Yes	Yes	No	No
Cross Assembler	AMDASM	No	No	Yes
Simulator	No	No	No	Yes
High Level Language	Yes	Yes	No	No
Programs Debug	Yes	Yes	No	Yes
Diagnostic	Yes	Yes	No	Yes
Edit	Yes	Yes	No	Yes
User Library (>25 programs from user)	No	Yes	No	Macro's
Delivery Start (Qtr.-Year)	3 Qtr. 75	4 Qtr. 77	3 Qtr. 75	2 Qtr. 78
Alternate Sources	Fairchild, Motorola, MMI, National, NEC, Raytheon, Signetics	Fairchild, Motorola National	Intel, Mitsubishi, National, NEC, Raytheon, Signetics	Future
Comments		Hardware multiple and divide; normalize; parity.	Priority interrupts with Intel 8214.	64x4 RAM, 1024x8 ROM, Timer, Touch Switch Input, Fluorescent Display Driver On-chip.

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MICROPROCESSORS (cont)

Manufacturer Model For Detailed Data See:	AMI S2150/A	AMI S2200/A	AMI S6800/S6802 (Pages 1781, 1786)	AMI S9900 (Page 1841)
General Structure	4-Bit Microcomputer	4-Bit Microcomputer	8-Bit CPU	16-Bit CPU
Type	NMOS	NMOS	NMOS	NMOS
No. of Devices per CPU	1	1	1	1
CPU Size (Pins)	40	40	40	64
Supply Voltage	9	9	5	±5, 12
CPU Power Dissipation (mw)	250	250	600	1000
Architecture Data Word Size (bits)	4 (8-Bit I/O Bus)	4 (8-Bit I/O Bus)	8	16
Instruction Word Size (bits)	8	8	8, 16, 24	16, 32, 48
Directly Addressable Instruction Words (No.)	8K	8K	65K	65K bytes, 32K words
Clock Frequency (Hz/ext. phases required)	850 kHz/1 phase	850 kHz/1 phase	1-2 MHz/2 phase	3 MHz/4 phase
Register to Register Add Time (μsec/data word)	5	5	1 (2 MHz clock)	4.67
No. of Registers Arithmetic	1	1	2	16
Index	2	2	1 (16-Bit)	15
General Purpose	1	2	0	16 (in memory)
Return Stack Size (No. x bits)	3x10	5x10	External RAM/128x8	None
Interrupts	None	3	Standard	Standard
Type		Maskable, 2 level priority	Vectored, Multilevel	Vectored, 16 Levels
Direct Memory Access			Optional	Standard
BCD Arithmetic (Hardware)	No	No	Yes	No
Microprogrammable	No	No	No	No
Extended Temp. Range Available	Yes	Yes	No	−25°C to 85°C
Devices See System Components:	2000	2000	6800	9900
Hardware Support Processor Cards (CPU system on a card)	Yes (Emulator)	Yes (Emulator)	Yes	No
Prototyping System (Hardware & software development system)	Yes	Yes	Yes	Yes
In-System Emulator (Tests system in place)	Yes	Yes	Yes	No
Software Support (from this manufacturer) Resident Assembler	No	No	Yes	Yes
Cross Assembler	Yes	Yes	Fortran IV	Yes
Simulator	Yes	Yes	Fortran IV	Timesharing
High Level Language	No	No	No	Fortran, Cobol
Programs Debug	Yes	Yes	Yes	Yes
Diagnostic	Yes	Yes	Yes	Yes
Edit	Yes	Yes	Yes	Yes
User Library (>25 programs from user)	Macro's	Macro's	No	No
Delivery Start (Qtr.-Year)	4 Qtr. 78	1 Qtr. 79	1 Qtr. 75	1 Qtr. 78
Alternate Sources	Future	Future	Fairchild, Fujitsu, Hitachi Motorola	TI
Comments	80x4 RAM, 1536x8 ROM, Timer, Touch Switch Fluorescent Display Driver on-chip	128x4 RAM, 2048x8 ROM, ADC-8-Bit, 8 Channel, Same additional features as 2150	DMA through HALT and three state control 6802 has 6800, 6820, and 6875 on chip	Software compatible with 990 minicomputer

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MICROPROCESSORS (cont)

Manufacturer Model For Detailed Data See:	AMI S9940 (Page 1850)	AMI S9980 (Page 1852)	Data General mN601	Essex SX2000
General Structure	16 Bit Microcomputer	8/16 Bit CPU	16-Bit CPU	4-Bit CPU
Type	NMOS	NMOS	NMOS	PMOS
No. of Devices per CPU	1	1	1	1
CPU Size (Pins)	40	40	40	28
Supply Voltage	5	±5, 12	±5, 15	15
CPU Power Dissipation (mw)	1000	1000	1000	150
Architecture Data Word Size (bits)	16	8	16	4
Instruction Word Size (bits)	16, 32, 48	16, 32, 48	16	8
Directly Addressable Instruction Words (No.)	1K	16K bytes	32K	1K
Clock Frequency (Hz/ext. phases required)	5 MHz/1 phase	2-3 MHz/0 phase	8.3 MHz/2 phase	to 500/0 phase
Register to Register Add Time (μsec/data word)		8.8 (2 MHz)	2.4	16
No. of Registers Arithmetic	16	16	4	1
Index	15	15	2	1
General Purpose	16	16 (in memory)	4	0
Return Stack Size (No. x bits)		None	External RAM	1x10
Interrupts	Standard	Standard	Standard	None
Type	Masked, Prioritized, Vectored	Vectored, 6 Levels	16 Levels	
Direct Memory Access		Standard	Standard	None
BCD Arithmetic (Hardware)	Yes	No	No	Yes
Microprogrammable	12 XOPs	No	No	No
Extended Temp. Range Available	No		No	−40°C to 100°C Std.
Devices See System Components:	9900	9900	Micro Nova	SX200
Hardware Support Processor Cards (CPU system on a card)	Yes	No	Yes	No
Prototyping System (Hardware & software development system)	Yes	Yes	Yes	Yes
In-System Emulator (Tests system in place)	Yes	No	No	Yes
Software Support (from this manufacturer) Resident Assembler	Yes	Yes	Yes	No
Cross Assembler	Yes	Timesharing	Yes	Fortran
Simulator	Timesharing	Timesharing	Yes	Yes
High Level Language	Fortran, Pascal	Fortran, Cobol	Basic, Fortran	No
Programs Debug	Yes	Yes	Yes	No
Diagnostic	Yes	Yes	Yes	No
Edit	Yes	Yes	Yes	No
User Library (>25 programs from user)	No		Yes	No
Delivery Start (Qtr.-Year)	2 Qtr. 79	1 Qtr. 78	3 Qtr. 76	2 Qtr. 76
Alternate Sources	Texas Instruments	TI	None	None
Comments	TMS9000 Compatible, 128 bytes RAM, 2K bytes ROM, 16-bit instruction	8-Bit data bus, 16-Bit internal operation. Software compatible with TMS9900.	Software compatible with Nova 3 minicomputer	

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MICROPROCESSORS (cont)

Manufacturer Model For Detailed Data See:	Fairchild F8	Fairchild F2901A/9409 (Page 1893)	Fairchild F2903	Fairchild 3870 (Page 1863)
General Structure	8-Bit CPU	4-Bit Slice	4-Bit Slice	8-Bit CPU
Type	NMOS	TTL	TTL	NMOS
No. of Devices per CPU	1	Varies	Varies	1
CPU Size (Pins)	40	40	48	40
Supply Voltage	5, 12	5	5	5
CPU Power Dissipation (mw)	300	925	1750	300
Architecture Data Word Size (bits)	8	Multiple of 4	Multiple of 4	8
Instruction Word Size (bits)	8, 16, 24	9	User defined	8, 16, 24
Directly Addressable Instruction Words (No.)	65K	User defined	User defined	2K
Clock Frequency (Hz/ext. phases required)	2 MHz/0 phase	to 10 MHz/1 phase	to 10 MHz/1 phase	4 MHz/0 phase
Register to Register Add Time (μsec/data word)	2	0.125	0.145	2
No. of Registers Arithmetic	1	0	0	1
Index	2	0	0	2
General Purpose	64	17	17 (expandable)	65
Return Stack Size (No. x bits)	33x16 or RAM	4x4 (2909)	4x4, 5x5 (2909); 17x17 (2930)	1x16 or RAM
Interrupts	Standard	Optional (2914)	Optional (2914)	Standard
Type	Vectored, 1 Level/PSU		Vectored	Vectored, 1 Level
Direct Memory Access	Optional (3854)	Optional (2940)	Optional 2940	None
BCD Arithmetic (Hardware)	Yes	No	No	Yes
Microprogrammable	No	Yes	Yes	No
Extended Temp. Range Available	−55°C to 125°C	−55°C to 125°C	Future	Future
Devices See System Components:	F8	2900	2900	F8
Hardware Support Processor Cards (CPU system on a card)	Yes	No	No	Yes
Prototyping System (Hardware & software development system)	Yes	No	No	Yes
In-System Emulator (Tests system in place)	Yes	No	No	Yes
Software Support (from this manufacturer) Resident Assembler	Yes	No	No	Yes
Cross Assembler	Fortran IV	No	No	Fortran IV
Simulator	Prototyping Sys, Fortran IV	No	No	No
High Level Language	No	No	No	No
Programs Debug	Yes	No	No	Yes
Diagnostic	Yes	No	No	Yes
Edit	Yes	No	No	Yes
User Library (>25 programs from user)	Yes	No	No	Yes
Delivery Start (Qtr.-Year)	1 Qtr. 75		1 Qtr. 79	1 Qtr. 78
Alternate Sources	Mostek, SGS	AMD, Motorola, National, NEC, Raytheon, Signetics, MMI	AMD, Motorola, National	Mostek, Motorola
Comments	64 bytes of RAM in CPU 1024 or 2048 bytes of ROM in PSU, Programmable Timer.		Hardware multiply and divide; normalize; parity.	One chip microcomputer. Programmable hardware, timer on-chip. Software compatible with F8.

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MICROPROCESSORS (cont)

Manufacturer Model For Detailed Data See:	Fairchild 3880	Fairchild F6800 (Page 1886)	Fairchild F6801(E) (Page 1887)	Fairchild F6809 (Page 1887)
General Structure	8-Bit	8-Bit CPU	8/16-Bit CPU	8/16-Bit CPU
Type	NMOS	NMOS	NMOS	NMOS
No. of Devices per CPU	1	1	1	1
CPU Size (Pins)	40	40	40	40
Supply Voltage	5	5	5	5
CPU Power Dissipation (mw)	350	600	1000	1000
Architecture Data Word Size (bits)	8	8	8	8/16
Instruction Word Size (bits)	8, 16, 24	8, 16, 24	8, 16, 24	8, 16, 24, 32
Directly Addressable Instruction Words (No.)	2K EPROM	65K	65K	65K
Clock Frequency (Hz/ext. phases required)	4 MHz/0 phase	1 MHz/2 phase	1 MHz/2 phase	1-2 MHz/2 phase
Register to Register Add Time (μsec/data word)	2	2	2 (1 MHz clock)	1 (2 MHz clock)
No. of Registers Arithmetic	1	2	2	2
Index	2	1 (16-Bit)	1 (16-Bit)	4 (16-Bit)
General Purpose	64	0	1	4
Return Stack Size (No. x bits)	2x16 or RAM	External RAM/128x8	External RAM	External RAM
Interrupts	Standard	Standard	Standard	Standard
Type	1 Level Vectored	Vectored, Multilevel	Vectored, Multilevel	Vectored, Multilevel
Direct Memory Access	None	Optional	Optional	Optional
BCD Arithmetic (Hardware)	Yes	Yes	Yes	Yes
Microprogrammable	No	No	No	No
Extended Temp. Range Available	Future	Future	Future	Future
Devices See System Components:	F8	6800	6800	6800
Hardware Support Processor Cards (CPU system on a card)	Yes	Yes	Yes	Future
Prototyping System (Hardware & software development system)	Yes	Yes	Yes	Future
In-System Emulator (Tests system in place)	Yes	Yes	Yes	Future
Software Support (from this manufacturer) Resident Assembler	Yes	Yes	Yes	Future
Cross Assembler	Yes	Fortran IV	No	Future
Simulator	No	Fortran IV	No	Future
High Level Language	No	MPL	Basic	Future
Programs Debug	Yes	Yes	Yes	Future
Diagnostic	Yes	Yes	Yes	Future
Edit	Yes	Yes	Yes	Future
User Library (>25 programs from user)	Yes	No	No	No
Delivery Start (Qtr.-Year)	4 Qtr. 78	1 Qtr. 77	2 Qtr. 79	2 Qtr. 79
Alternate Sources	None	AMI, Fujitsu, Hitachi, Motorola	Motorola	Motorola
Comments	EPROM program storage.	DMA through HALT and three state control. 6802 has 6800, 6810 and 6875 on-chip.	DMA through HALT. 128x8 RAM, 2048x8 ROM.	DMA through HALT, three-state Control, hardware multiply.

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MICROPROCESSORS (cont)

Manufacturer Model For Detailed Data See:	Fairchild 9440 (Page 1903)	Fairchild Macrologic Bipolar	Fairchild Macrologic CMOS	Fujitsu MBM6800/MBM6802
General Structure	16-Bit CPU	4-Bit Slice	4-Bit Slice	8-Bit CPU
Type	I^2L	TTL	CMOS	NMOS
No. of Devices per CPU	1			1
CPU Size (Pins)	40	24	24	40
Supply Voltage	350 mA and 5V	5	3 to 15	5
CPU Power Dissipation (mw)	1000	800	to 5mw at 10V	600
Architecture Data Word Size (bits)	16	Multiple of 4	Multiple of 4	8
Instruction Word Size (bits)	16	3	4	8, 16, 24
Directly Addressable Instruction Words (No.)	32K (16-Bit)			65K
Clock Frequency (Hz/ext. phases required)	0-10 MHz/0 phase	to 14 MHz/1 phase	to 4.9 MHz (15V)/1 phase	1-2 MHz (2 phase)
Register to Register Add Time (μsec/data word)	1.5 (10 MHz clock)	0.10	0.086 (15V)	1 (2 MHz clock)
No. of Registers Arithmetic	0	0	1	2
Index	0	0	2	1 (16-Bit)
General Purpose	4	8	2	0
Return Stack Size (No. x bits)	External RAM	10x4 (9408), 16x4 (9406)		External RAM/128x8
Interrupts	Yes	Optional		Standard
Type	Masked 16 Level			Vectored, Multilevel
Direct Memory Access	Yes	Optional		Optional
BCD Arithmetic (Hardware)	No	No	No	Yes
Microprogrammable	No	Yes	Yes	No
Extended Temp. Range Available	−55°C to 125°C	−55°C to 125°C	−55°C to 125°C	No
Devices See System Components:	9440	Macrologic Bipolar	Macrologic CMOS	6800
Hardware Support Processor Cards (CPU system on a card)	Yes	Yes	No	No
Prototyping System (Hardware & software development system)	Yes	Yes	No	No
In-System Emulator (Tests system in place)	No	No	No	No
Software Support (from this manufacturer) Resident Assembler	Yes	No	No	No
Cross Assembler	Timesharing	Timesharing	No	No
Simulator	Timesharing	No	No	No
High Level Language	Fortran, Basic	No	No	No
Programs Debug	Yes	No	No	No
Diagnostic	Yes	No	No	No
Edit	Yes	No	No	No
User Library (>25 programs from user)	Future	No	No	No
Delivery Start (Qtr.-Year)	1 Qtr. 78	4th Qtr. 75	1 Qtr. 79	1 Qtr. 79
Alternate Sources	None	None		AMI, Fairchild, Motorola, Hitachi
Comments	Microcomputer performance. Multifunction instructions process several step, e.g. add/shift/check and skip.	Hardware stack with 9406, 10-Bit sequencer with 9408.		6802 has 6800, 6810, and 6875 on-chip.

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MICROPROCESSORS (cont)

Manufacturer Model For Detailed Data See:	Fujitsu MBM8048	Fujitsu MBM8049	General Instrument CP-1600/A CP-1610	General Instrument LP-8000
General Structure	8-Bit Microcomputer	8-Bit Microcomputer	16-Bit CPU	8-Bit CPU
Type	NMOS	NMOS	NMOS	PMOS
No. of Devices per CPU	1	1	1	1
CPU Size (Pins)	40	40	40	40
Supply Voltage	5	5	−3, 5, 12	−12, 5
CPU Power Dissipation (mw)	300	350	750	500
Architecture Data Word Size (bits)	8	8	16	8
Instruction Word Size (bits)	8, 16	8, 16	10, 20, 30	8, 16, 24
Directly Addressable Instruction Words (No.)	4K	4K	65K	65K
Clock Frequency (Hz/ext. phases required)	6 MHz/0 phase	6 MHz/0 phase	4 MHz/2 phase	600 kHz/1 phase
Register to Register Add Time (μsec/data word)	2.5	2.5	3.0	10.0
No. of Registers Arithmetic	16	16	0	1
Index	0	0	0	0
General Purpose	64	128	8	48
Return Stack Size (No. x bits)	8x16	8x16	Standard	1x8 or RAM
Interrupts	Yes	Yes	External RAM	Standard
Type	Dual, 1 Level, Vectored	Dual, 1 Level, Vectored	Vectored, Multilevel	Vectored, 1 Level
Direct Memory Access	No	No	Standard	No
BCD Arithmetic (Hardware)	Yes	Yes	No	Yes
Microprogrammable	No	No	No	No
Extended Temp. Range Available	No	No		
Devices See System Components:	8048	8049	1600	8000
Hardware Support Processor Cards (CPU system on a card)	No	No	Yes	Yes
Prototyping System (Hardware & software development system)	No	No	Yes	Yes
In-System Emulator (Tests system in place)	No	No	Yes	No
Software Support (from this manufacturer) Resident Assembler	No	No	Yes	Yes
Cross Assembler	No	No	Fortran IV	Fortran IV
Simulator	No	No	Fortran IV	Fortran IV
High Level Language	No	No	No	No
Programs Debug	No	No	Yes	Yes
Diagnostic	No	No	Yes	Yes
Edit	No	No	Yes	Yes
User Library (>25 programs from user)	No	No	No	No
Delivery Start (Qtr.-Year)	1 Qtr. 79	1 Qtr. 79	3 Qtr. 74	2 Qtr. 75
Alternate Sources	AMD, Intel, NEC Signetics	Intel		None
Comments			CP-1600 3.6 μsec add time with 3.3 MHz clock. CP-1610 6 μsec add time with 2.0 MHz clock.	

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MICROPROCESSORS (cont)

Manufacturer Model For Detailed Data See:	General Instrument PIC 1650	Harris HM6100 (Page 1918)	Harris HM6100A (Page 1918)	Hitachi HD46800/46802
General Structure	8-Bit Micromputer	12-Bit CPU	12-Bit CPU	8-Bit CPU
Type	NMOS	CMOS	CMOS	NMOS
No. of Devices per CPU	1	1	1	1
CPU Size (Pins)	40	40	40	40
Supply Voltage	5	5	4-11	5
CPU Power Dissipation (mw)	375	10	40	600
Architecture Data Word Size (bits)	8	12	12	8
Instruction Word Size (bits)	12	12	12	8, 16, 24
Directly Addressable Instruction Words (No.)	512	4K (Expandable to 32K)	4K (Expandable to 32K)	65K
Clock Frequency (Hz/ext. phases required)	1 MHz/0 phase	4 MHz/0 phase	8 MHz/0 phase	1-2 MHz/2 phase
Register to Register Add Time (μsec/data word)	4	5 (2.50 10V)	2.5	2 (1 MHz clock)
No. of Registers Arithmetic	0	2	2	2
Index	0	0	0	1 (16-Bit)
General Purpose	32	4	4	0
Return Stack Size (No. x bits)	2x9	None	None	External RAM/128x8
Interrupts	None	Standard	Standard	Standard
Type		Vectored, 1 Level	Vectored, 1 Level	Vectored, Multilevel
Direct Memory Access	None	Standard	Standard	Optional
BCD Arithmetic (Hardware)	No	No	No	Yes
Microprogrammable	Yes	No	No	No
Extended Temp. Range Available	Future	−55°C to 125°C	−55°C to 125°C	No
Devices See System Components:	1650	6100	6100	6800
Hardware Support Processor Cards (CPU system on a card)	No	Yes	Yes	Yes
Prototyping System (Hardware & software development system)	Yes	Yes	Yes	Yes
In-System Emulator (Tests system in place)	Yes	No	No	Yes
Software Support (from this manufacturer) Resident Assembler	No	Yes	Yes	Yes
Cross Assembler	Yes	Fortran IV	Fortran IV	Fortran IV
Simulator	Yes	Fopel III	Fopel	Fortran IV
High Level Language	No	Focal, Basic, Fortran	Focal, Basic, Fortran	Yes
Programs Debug	Yes	Yes	Yes	Yes
Diagnostic	Yes	Yes	Yes	Yes
Edit	Yes	Yes	Yes	Yes
User Library (>25 programs from user)	No			No
Delivery Start (Qtr.-Year)	2 Qtr. 77	1 Qtr. 76	1 Qtr. 76	2 Qtr. 76
Alternate Sources	None	Intersil	Intersil	Motorola, Fairchild, AMI, Fuitsu
Comments	Stand alone controller.			DMA through HALT and three state control. 6802 has 6800, 6810 and 6875 on-chip.

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MICROPROCESSORS (cont)

Manufacturer Model For Detailed Data See:	Hitachi HMCS42	Hitachi HMCS43/43C	Hitachi HMCS44/45	Hughes HCMP1802C/ HCMP1802
General Structure	4-Bit Microcomputer	4-Bit Microcomputer	4-Bit Microcomputer	8-Bit CPU
Type	PMOS	PMOS/CMOS	PMOS	CMOS
No. of Devices per CPU	1	1	1	1
CPU Size (Pins)	28	42	42/54	40
Supply Voltage	−10	−10/5	−10	4 to 6/3 to 12
CPU Power Dissipation (mw)	100	150/2	150	8 @ 5V/40 @ 10V
Architecture Data Word Size (bits)	4	4	4	8
Instruction Word Size (bits)	10	10	10	8, 16, 24
Directly Addressable Instruction Words (No.)	512	1024	2048	65K
Clock Frequency (Hz/ext. phases required)	100 kHz/0 phase	100 kHz/0 phase	600 kHz/0 phase	0-6.4 MHz/0 phase
Register to Register Add Time (μsec/data word)	10	10	20	2.5 (6.4 MHz clock)
No. of Registers Arithmetic	1	2	2	1
Index	0	0	0	0
General Purpose	32	80	160	32
Return Stack Size (No. x bits)	2x9	3x10	2x12	External RAM
Interrupts	None	Yes	Yes	Standard
Type		Dual	Dual	1 Level
Direct Memory Access	None	None	None	Standard (on-chip)
BCD Arithmetic (Hardware)	Yes	Yes	Yes	No
Microprogrammable	No	No	No	No
Extended Temp. Range Available	No	No	No	−55°C to 125°C Standard
Devices See System Components:	HMCS40	HMCS40	HMCS40	1800
Hardware Support Processor Cards (CPU system on a card)	No	No	No	Yes
Prototyping System (Hardware & software development system)	Yes	Yes	Yes	Yes
In-System Emulator (Tests system in place)	Yes	Yes	Yes	Yes
Software Support (from this manufacturer) Resident Assembler	No	No	No	Yes
Cross Assembler	Fortran IV	Fortran IV	Fortran IV	Fortran IV, Timesharing
Simulator	No	No	Fortran IV	Yes
High Level Language	No	No	No	No
Programs Debug	No	No	No	Yes
Diagnostic	No	No	No	Yes
Edit	No	No	No	Yes
User Library (>25 programs from user)	No	No	No	No
Delivery Start (Qtr.-Year)	2 Qtr. 78	1 Qtr. 78	1 Qtr. 77	3 Qtr. 77
Alternate Sources				RCA, SSS
Comments				

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MICROPROCESSORS (cont)

Manufacturer Model For Detailed Data See:	Intel 3000	Intel 4004	Intel 4040	Intel 8008
General Structure	2-Bit Slice	4-Bit CPU	4-Bit CPU	8-Bit CPU
Type	TTL	PMOS	PMOS	PMOS
No. of Devices per CPU	≥2	1	1	1
CPU Size (Pins)	28 and 40	16	24	18
Supply Voltage	5	15 (or −10, 5)	15 (or −10, 5)	−9, 5
CPU Power Dissipation (mw)	800	450	1000	420
Architecture Data Word Size (bits)	Multiple of 2	4	4	8
Instruction Word Size (bits)		8, 16	8, 16	8, 16, 24
Directly Addressable Instruction Words (No.)	512 (Microinstructions)	4K	4K	16K
Clock Frequency (Hz/ext. phases required)	to 6 MHz/1 phase	500 to 740 kHz/2 phase	500 to 740 kHz/2 phase	800 kHz/2 phase
Register to Register Add Time (μsec/data word)	0.15 (16 bits)	10.8	10.8	12.5
No. of Registers Arithmetic	2	1	1	1
Index	0	0	0	0
General Purpose	11	16	24	6
Return Stack Size (No. x bits)	None	3x12	7x12	7x14
Interrupts	Optional	None	Standard	Standard
Type	8 Level Priority (3214)		Vectored, 1 Level	Vectored, 8 Level
Direct Memory Access	No	None	None	
BCD Arithmetic (Hardware)	No	Yes	Yes	No
Microprogrammable	Yes	No	No	No
Extended Temp. Range Available	−55°C to 125°C	−40°C to 85°C	−55°C to 85°C	−55°C to 85°C
Devices See System Components:	3000	4004/4040	4004/4040	8008
Hardware Support Processor Cards (CPU system on a card)	No	Yes	Yes	Yes
Prototyping System (Hardware & software development system)	Yes	Yes	Yes	Yes
In-System Emulator (Tests system in place)	Yes	No	Yes	No
Software Support (from this manufacturer) Resident Assembler	No	Yes	Yes	Yes
Cross Assembler	CROMIS Microassembler	Fortran IV	Fortran IV	Fortran IV
Simulator	No	Fortran IV	Fortran IV	Fortran IV
High Level Language	No	No	No	PL/M (Fortran IV)
Programs Debug	No	Yes	Yes	Yes
Diagnostic	No	Yes	Yes	Yes
Edit	No	Yes	Yes	Yes
User Library (>25 programs from user)	No	Yes	Yes	Yes
Delivery Start (Qtr.-Year)	3 Qtr. 74	2 Qtr. 71	4 Qtr. 74	1 Qtr. 72
Alternate Sources	Signetics	Hitachi, National	None	None
Comments				8 Level interrupts with 8214 Priority Interrupt IC.

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MICROPROCESSORS (cont)

Manufacturer Model For Detailed Data See:	Intel 8021	Intel 8022	Intel 8035/8048/8748 (Page 1934)	Intel 8049
General Structure	8-Bit Microcomputer	8-Bit Microcomputer	8-Bit Microcomputer	8-Bit Microcomputer
Type	NMOS	NMOS	NMOS	NMOS
No. of Devices per CPU	1	1	1	1
CPU Size (Pins)	28	40	40	40
Supply Voltage	5	5	5	5
CPU Power Dissipation (mw)	150	400	325	500
Architecture Data Word Size (bits)	8	8	8	8
Instruction Word Size (bits)	8, 16	8, 16	8, 16	8, 16
Directly Addressable Instruction Words (No.)	1K	2K	4K	4K
Clock Frequency (Hz/ext. phases required)	3 MHz/0 phase	3 MHz/0 phase	6 MHz/0 phase	11 MHz/0 phase
Register to Register Add Time (μsec/data word)	10	10	2.5	1.36
No. of Registers Arithmetic	16	16	16	16
Index	0	0	0	0
General Purpose	64	64	64	128
Return Stack Size (No. x bits)	8x16	8x16	8x16	8x16
Interrupts	None	Yes	Yes	Yes
Type		Dual, 1 Level, Vectored	Dual, 1 Level, Vectored	Dual, 1 Level, Vectored
Direct Memory Access	No	No	No	No
BCD Arithmetic (Hardware)	Yes	Yes	Yes	Yes
Microprogrammable	No	No	No	No
Extended Temp. Range Available	−40°C to 85°C	−40°C to 85°C	−55°C to 125°C	
Devices See System Components:	8048	8048	8048	8048
Hardware Support Processor Cards (CPU system on a card)	Yes	No	Yes	Yes
Prototyping System (Hardware & software development system)	Yes	Yes	Yes	Yes
In-System Emulator (Tests system in place)	Yes	Yes	Yes	Yes
Software Support (from this manufacturer) Resident Assembler	Yes	Yes	Yes	Yes
Cross Assembler	No	No	No	No
Simulator	No	No	No	No
High Level Language	No	No	No	No
Programs Debug	Yes	Yes	Yes	Yes
Diagnostic	Yes	Yes	Yes	Yes
Edit	Yes	Yes	Yes	Yes
User Library (>25 programs from user)	Yes	Yes	Yes	Yes
Delivery Start (Qtr.-Year)	1 Qtr. 78	4 Qtr. 78	1 Qtr. 77	1 Qtr. 78
Alternate Sources	Signetics	None	AMD, NEC, Fujitsu, Signetics	Fujitsu
Comments	Software subset of 8048.	On-board A/D. Software subset of 8048.	8048 has ROM, 8748 U.V. PROM, 8035 external ROM.	8039 uses external ROM.

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MICROPROCESSORS (cont)

Manufacturer Model For Detailed Data See:	Intel 8080A	Intel 8085A (Page 1944)	Intel 8086 (Page 1947)	Intersil IM6100
General Structure	8-Bit CPU	8-Bit CPU	16-Bit CPU	12-Bit CPU
Type	NMOS	NMOS	NMOS	CMOS
No. of Devices per CPU	1	1	1	1
CPU Size (Pins)	40	40	40	40
Supply Voltage	±5, 12	5	5	5 to 10 (5 nominal)
CPU Power Dissipation (mw)	780	850	1500	10
Architecture Data Word Size (bits)	8	8	16	12
Instruction Word Size (bits)	8, 16, 24	8, 16, 24	8, 16,24, 32, 40, 48	12
Directly Addressable Instruction Words (No.)	65K	65K	1 MB	4K (Expandable to 32K)
Clock Frequency (Hz/ext. phases required)	2 MHz/2 phase (2.6 and 3 MHz opt.)	3 (5 with - 2 version)/0 phase	5 MHz/1 phase	4 MHz/0 phase
Register to Register Add Time (μsec/data word)	2 (2 MHz clock)	1.2 (3 MHz clock) 0.8 (5 MHz clock)	0.3	5 (2.5 at 10V)
No. of Registers Arithmetic	1	1	8	2
Index	0	0	2	0
General Purpose	6	7	14	4
Return Stack Size (No. x bits)	External RAM	External RAM	External RAM	None
Interrupts	Standard	Standard	Standard	Standard
Type	Vectored, Multilevel	Vectored, 4 Level + External	Vectored, Multilevel	Vectored, 1 Level
Direct Memory Access	Standard	Standard	Standard	Standard
BCD Arithmetic (Hardware)	Yes	Yes	Yes	No
Microprogrammable	No	No	No	No
Extended Temp. Range Available	−55°C to 125°C	−55°C to 125°C		−55°C to 125°C
Devices See System Components:	8080	8085A	8086	6100
Hardware Support Processor Cards (CPU system on a card)	Yes	Yes	Yes	Yes
Prototyping System (Hardware & software development system)	Yes	Yes	Yes	Yes
In-System Emulator (Tests system in place)	Yes	Yes	Yes	No
Software Support (from this manufacturer) Resident Assembler	Yes	Yes	Yes	Yes
Cross Assembler	Fortran IV	Fortran IV	No	Yes
Simulator	Fortran IV	Fortran IV	No	Forpal III
High Level Language	PL/M (Fortran IV)	PL/M, Fortran IV	PL/M-86	Yes
Programs Debug	Yes	Yes	Yes	Yes
Diagnostic	Yes	Yes	Yes	Yes
Edit	Yes	Yes	Yes	Yes
User Library (>25 programs from user)	Yes	Yes	Yes	Yes (DEC)
Delivery Start (Qtr.-Year)	4 Qtr. 73	1 Qtr. 77	2 Qtr. 78	2 Qtr. 75
Alternate Sources	AMD, Mitsubishi, National, NEC, Signetics, TI	AMD, Mitsubishi, NEC		Harris
Comments		8080A compatible with multiplexed bus operation.		Executive PDP-8, Instruction Set

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MICROPROCESSORS (cont)

Manufacturer Model For Detailed Data See:	Mitel MD46802	Mitsubishi M5L8080A	Mitsubishi M5L8085	Monolithic Memories 2901A
General Structure	8-Bit CPU	8-Bit CPU	8-Bit CPU	4-Bit Slice
Type	CMOS	NMOS	NMOS	TTL
No. of Devices per CPU	1	1	1	Varies
CPU Size (Pins)	40	40	40	40
Supply Voltage	5	±5, 12	5	5
CPU Power Dissipation (mw)	10	780	600	925
Architecture Data Word Size (bits)	8	8	8	Multiple of 4
Instruction Word Size (bits)	8, 16, 24	8, 16, 24	8, 16, 24	User defined
Directly Addressable Instruction Words (No.)	65K	65K	65K	User defined
Clock Frequency (Hz/ext. phases required)	0-6 MHz/0 phase	2 MHz/2 phase	3 MHz/0 phase	to 10 MHz/1 phase
Register to Register Add Time (μsec/data word)	1 (2 MHz clock)	2 (2 MHz clock)	1.3	0.145
No. of Registers Arithmetic	2	1	1	0
Index	1 (16-Bit)	0	0	0
General Purpose	0	6	7	17
Return Stack Size (No. x bits)	RAM	External RAM	External RAM	4x4, 5x5 (2909)
Interrupts	Standard	Standard	Standard	
Type	Vectored, Multilevel		Vectored, 4 Level	
Direct Memory Access	Optional	Standard	Standard	None
BCD Arithmetic (Hardware)	Yes	Yes	Yes	No
Microprogrammable	Yes	No	No	Yes
Extended Temp. Range Available	Yes	No	No	−55°C to 125°C
Devices See System Components:	6800	8080A	8085A	2900
Hardware Support Processor Cards (CPU system on a card)	Yes	Yes	Yes	No
Prototyping System (Hardware & software development system)	Yes	Yes	Yes	No
In-System Emulator (Tests system in place)	Yes	No	Yes	No
Software Support (from this manufacturer) Resident Assembler	No	Yes	Yes	Yes
Cross Assembler	No	Yes	Yes	No
Simulator	No	Yes	Yes	No
High Level Language	No	PL/M	PL/M	No
Programs Debug	No	Yes	Yes	No
Diagnostic	No	Yes	Yes	No
Edit	No	Yes	Yes	Yes
User Library (>25 programs from user)	No	Yes	Yes	No
Delivery Start (Qtr.-Year)	1 Qtr. 79	2 Qtr. 75	2 Qtr. 78	1 Qtr. 79
Alternate Sources	AMI, Motorola	AMD, Intel, National NEC, Signetics, TI	AMD, Intel, NEC	AMD, Fairchild, Motorola, National, NEC, Raytheon, Signetics
Comments	Timer on-chip 128 bytes RAM on-chip.		8080A compatible with multiplexed bus operation.	

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MICROPROCESSORS (cont)

Manufacturer Model For Detailed Data See:	Monolithic Memories 67000	MOS Technology 6500	Mostek F8 (MK3850)	Mostek MK3870/MK3872
General Structure	4-Bit Slice	8-Bit CPU	8-Bit CPU	8-Bit CPU
Type	TTL	NMOS	NMOS	NMOS
No. of Devices per CPU		1	1	1
CPU Size (Pins)	40	40 or 28	40	40
Supply Voltage	5	5	5, 12	5
CPU Power Dissipation (mw)	900	200	600	300
Architecture Data Word Size (bits)	Multiple of 4	8	8	8
Instruction Word Size (bits)	8	8, 16, 24	8, 16, 24	8, 16, 24
Directly Addressable Instruction Words (No.)		65K	65K	2K/4K
Clock Frequency (Hz/ext. phases required)	0 to 10 MHz/1 phase	to 2 MHz/1 phase	2 MHz/0 phase	4 MHz/0 phase
Register to Register Add Time (μsec/data word)	0.085 typ. (6701)	1	2	2
No. of Registers Arithmetic	0	1	1	1
Index	0	2	2	2
General Purpose	17	0	65	65
Return Stack Size (No. x bits)	1x8 (67110)	External RAM	1x8 or RAM	1x8 or RAM
Interrupts	67116	Standard	Standard	Standard
Type	16 Vectored	Vectored, 2 Level	Vectored, 1 Level/PSU	Vectored, 1 Level
Direct Memory Access	No	Optional	Optional (MK3854)	None
BCD Arithmetic (Hardware)	No	Yes	Yes	Yes
Microprogrammable	Yes	No	No	No
Extended Temp. Range Available	−55°C to 125°C	−55°C to 85°C		−40°C to 85°C
Devices See System Components:	67000	6500	F8	F8
Hardware Support Processor Cards (CPU system on a card)	No	Yes	Yes	Yes
Prototyping System (Hardware & software development system)	No	Yes	Yes	Yes
In-System Emulator (Tests system in place)	No	Yes	Yes	Yes
Software Support (from this manufacturer) Resident Assembler	No	Yes	Yes	Yes
Cross Assembler	Fortran IV	Fortran IV	Fortran IV	Fortran IV
Simulator	No	Fortran IV	Timesharing	No
High Level Language	No	No	No	No
Programs Debug	No	Yes	Yes	Yes
Diagnostic	No	Yes	Yes	Yes
Edit	No	No	Yes	Yes
User Library (>25 programs from user)	No	No	No	No
Delivery Start (Qtr.-Year)	4 Qtr. 75	3 Qtr. 75	3 Qtr. 75	1 Qtr. 77
Alternate Sources		Rockwell, Synertek	Fairchild, SGS	Fairchild, Motorola
Comments	RAM on-chip.	DMA based on a stopping CPU, but address bus connections are not 3 state.	64 bytes of RAM in CPU 1024 bytes of ROM in PSU programmable timer.	One chip microcomputer. Programmable hardware, timer on-chip.

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MICROPROCESSORS (cont)

Manufacturer Model For Detailed Data See:	Mostek MK3880 (Z80)	Motorola MC2901/A	Motorola MC2903	Motorola MC3870
General Structure	8-Bit CPU	4-Bit Slice	4-Bit Slice	8-Bit CPU
Type	NMOS	TTL	TTL	NMOS
No. of Devices per CPU	1	Varies	Varies	1
CPU Size (Pins)	40	40	48	40
Supply Voltage	5	5	5	5
CPU Power Dissipation (mw)	1100	925	1750	300
Architecture Data Word Size (bits)	8	Multiple of 4	Multiple of 4	8
Instruction Word Size (bits)	8, 16, 24, 36	9	User defined	8, 16, 24
Directly Addressable Instruction Words (No.)	65K		User defined	2K
Clock Frequency (Hz/ext. phases required)	2.5 MHz/2 phase (4 MHz opt.)	to 10 MHz/1 phase	to 10 MHz/1 phase	4 MHz/0 phase
Register to Register Add Time (μsec/data word)	1.6 (2.5 MHz dock)	0.125/0.145	0.145	2
No. of Registers Arithmetic	1	0	0	1
Index	2	0	0	2
General Purpose	14	17	17 (expandable)	65
Return Stack Size (No. x bits)	External RAM	4x4 (MC2900)	4x4, 5x5 (2909); 17x17 (2930)	1x8 or RAM
Interrupts	Standard	Optional	Optional (2924)	Standard
Type	Vectored, Multilevel	Vectored	Vectored	Vectored, 1 Level
Direct Memory Access	MK3883-DMA	Optional	Optional (2940)	None
BCD Arithmetic (Hardware)	Yes	No	No	Yes
Microprogrammable	No	Yes	Yes	No
Extended Temp. Range Available	−55°C to 125°C		−55°C to 125°C	
Devices See System Components:	Z80	2900	2900	F8
Hardware Support Processor Cards (CPU system on a card)	Yes	No	No	Yes
Prototyping System (Hardware & software development system)	Yes	No	No	Yes
In-System Emulator (Tests system in place)	Yes	No	No	Yes
Software Support (from this manufacturer) Resident Assembler	Yes	No	No	Yes
Cross Assembler	Fortran IV	No	No	Fortran IV
Simulator	Timesharing	No	No	No
High Level Language	PLZ	No	No	No
Programs Debug	Yes	No	No	Yes
Diagnostic	Yes	No	No	Yes
Edit	Yes	No	No	Yes
User Library (>25 programs from user)	No	No	No	No
Delivery Start (Qtr.-Year)	2 Qtr. 76	3 Qtr. 76	1 Qtr. 79	4 Qtr. 77
Alternate Sources	NEC, Zilog	AMD, Fairchild, National, NEC, Raytheon, Signetics	AMD, Fairchild, National	Fairchild, Mostek
Comments	8080A Software compatible with additional instructions. Vectored priority interrupt in peripheral devices.		Hardware multiply and divide; normalize; parity.	One chip microcomputer. Programmable hardware, timer on-chip.

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MICROPROCESSORS (cont)

Manufacturer Model For Detailed Data See:	Motorola MC6800/MC6802 (Pages 1995, 2002)	Motorola MC6801(E)	Motorola MC6809 (Page 2005)	Motorola MC10800
General Structure	8-Bit CPU	8/16-Bit CPU	8/16-Bit CPU	4-Bit Slice
Type	NMOS	NMOS	NMOS	ECL
No. of Devices per CPU	1	1	1	
CPU Size (Pins)	40	40	40	48
Supply Voltage	5	5	5	−2, −5.2
CPU Power Dissipation (mw)	600	1000	1000	
Architecture Data Word Size (bits)	8	8/16	8/16	Multiple of 4
Instruction Word Size (bits)	8, 16, 24	8, 16, 24	8, 16, 24, 32	
Directly Addressable Instruction Words (No.)	65K	65K	65K	
Clock Frequency (Hz/ext. phases required)	1-2 MHz/2 phase	1-2 MHz/2 phase	2 MHz/2 phase	0 to 6 MHz/1 phase
Register to Register Add Time (μsec/data word)	1 (2 MHZ clock)	2 (1 MHz clock)	1 (2 MHz clock)	0.041 typ. 16-Bit
No. of Registers Arithmetic	2	2	2	Ext.
Index	1 (16-Bit)	1	4	MC10803
General Purpose	0	1	4	MC10803
Return Stack Size (No. x bits)	External RAM/128x8	External RAM	External RAM	MC10801
Interrupts	Standard	Standard	Standard	
Type	Vectored, Multilevel	Vectored, Multilevel	Vectored, Multilevel	
Direct Memory Access	Optional	Optional	Optional	
BCD Arithmetic (Hardware)	Yes	Yes	Yes	Yes
Microprogrammable	No	No	No	Yes
Extended Temp. Range Available	No	Future	Future	No
Devices See System Components:	6800	6800	6800	10800
Hardware Support Processor Cards (CPU system on a card)	Yes	Yes	Yes	No
Prototyping System (Hardware & software development system)	Yes	Yes	Yes	No
In-System Emulator (Tests system in place)	Yes	Yes	Future	No
Software Support (from this manufacturer) Resident Assembler	Yes	Yes	Yes	No
Cross Assembler	Fortran IV	Future	Future	No
Simulator	Fortran IV	Future	Future	No
High Level Language	MPL (Fortran)	MPL (Fortran)	Pascal, Basic	No
Programs Debug	Yes	Yes	Yes	No
Diagnostic	Yes	Yes	Yes	No
Edit	Yes	Yes	Yes	No
User Library (>25 programs from user)	No	Yes	Yes	No
Delivery Start (Qtr.-Year)	2 Qtr. 74	4 Qtr. 76	1 Qtr. 79	2 Qtr. 76
Alternate Sources	AMI, Fairchild, Hitachi Fujitsu	Fairchild	Fairchild	Future
Comments	DMA through HALT and three state control. 6802 has 6800, 6810, and 6875 on-chip.	DMA through HALT. 128x8 RAM, 2048x8 ROM.	DMA through HALT, three-state control hardware multiply.	

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MICROPROCESSORS (cont)

Manufacturer Model For Detailed Data See:	Motorola MC68000	Motorola MC141000/MC141200 (Page 1956)	National IDM2901A/A-1 (Page 2015)	National INS4004 (FIPS)
General Structure	16-Bit CPU	4-Bit Microcomputer	4-Bit Slice	4-Bit CPU
Type	NMOS	CMOS	TTL	PMOS
No. of Devices per CPU	1	1	Varies	1
CPU Size (Pins)	64	28 or 40	40	16
Supply Voltage	5	3-6	5	15 (or −10, 5)
CPU Power Dissipation (mw)	1090 (typ.)	0.5-2.5	800	450
Architecture Data Word Size (bits)	16	4	Multiple of 4	4
Instruction Word Size (bits)	16, 32, 48, 64, 80	8	9	8, 16
Directly Addressable Instruction Words (No.)	16 MB	1K	User defined	4K
Clock Frequency (Hz/ext. phases required)	8 MHz/0 phase	0-600 kHz/0 phase	to 10 MHz/1 phase	500 to 740 kHz/2 phase
Register to Register Add Time (μsec/data word)	0.5	10 (600 kHz clock)	0.1	10.8
No. of Registers Arithmetic	8	1	0	1
Index	16 (32-Bit)	0	0	0
General Purpose	8	1	17	16
Return Stack Size (No. x bits)	External RAM	1x10	System dependent	3x12
Interrupts	Standard	None	System dependent	None
Type	Vectored, Multilevel		Vectored	
Direct Memory Access	Standard (on-chip)	No	System dependent	None
BCD Arithmetic (Hardware)	Standard	Yes	No	Yes
Microprogrammable	No	No	Yes	No
Extended Temp. Range Available	Future	−40°Cto 85°C Standard	Yes	
Devices See System Components:	68000	1000	2900	4004/4040
Hardware Support Processor Cards (CPU system on a card)	Future	No	No	No
Prototyping System (Hardware & software development system)	Future	Yes	No	No
In-System Emulator (Tests system in place)	Future	Yes	No	No
Software Support (from this manufacturer) Resident Assembler	Yes	No	No	No
Cross Assembler	Fortran IV	Yes	No	No
Simulator	Future	Timesharing	No	No
High Level Language	Pascal, Fortran IV	No	No	No
Programs Debug	Yes	Yes	No	No
Diagnostic	Yes	Yes	No	No
Edit	Yes	Yes	No	No
User Library (>25 programs from user)	No	No	No	No
Delivery Start (Qtr.-Year)	2 Qtr. 79	4 Qtr. 77	4 Qtr. 77	3 Qtr. 75
Alternate Sources		None	AMD, Fairchild, MMI, Motorola, National, NEC, Raytheon, Signetics	Intel
Comments	General purpose register machine, supports memory to memory operations.	A 48 pin version. MC141099, permits use of external PROM, RAM or ROM for program development.	μassembler available 2 Qtr. 79.	

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MICROPROCESSORS (cont)

Manufacturer Model For Detailed Data See:	National COP402/402M/402L (Page 2044)	National COP410L/411L (Pages 2034, 2036)	National COP420/420L/420C (Pages 2038, 2040, 2044)	National COP444L (Page 2044)
General Structure	4-Bit Microcontroller	4-Bit Microcontroller	4-Bit Microcontroller	4-Bit Microcontroller
Type	NMOS	NMOS	NMOS ("C" - CMOS)	NMOS
No. of Devices per CPU	1	1	1	1
CPU Size (Pins)	40	24/20	28	40/28
Supply Voltage	4.5-6.3 ("L"-4.5-9.5)	4.5-9.5	4.5-6.3/4.5-9.5/2.4-6.3	4.5-9.5
CPU Power Dissipation (mw)	140 ("L"-70)	25	125/35/125	55
Architecture Data Word Size (bits)	4	4	4	4
Instruction Word Size (bits)	8	8	8	8
Directly Addressable Instruction Words (No.)	1K External ("L"-2K)	512	1024	2048
Clock Frequency (Hz/ext. phases required)	Programmable (External or Internal)	Programmable (External or Internal)	Programmable (External or Internal)	Programmable (External or Internal)
Register to Register Add Time (μsec/data word)	4	16	4/16/16	16
No. of Registers Arithmetic	4	4	4	4
Index	1	1	1	1
General Purpose	64	32	64	128
Return Stack Size (No. x bits)	3x10	2x9	3x20	3x11
Interrupts	Standard ("M"-None)		Standard	Standard
Type	Vectored, 1 Level		Vectored, 1 Level	Vectored, 1 Level
Direct Memory Access				
BCD Arithmetic (Hardware)	Yes	Yes	Yes	Yes
Microprogrammable				
Extended Temp. Range Available	Future	Future	Future	Future
Devices See System Components:	COP400	COP400	COP400	COP400
Hardware Support Processor Cards (CPU system on a card)	Yes	Yes	Yes	Yes
Prototyping System (Hardware & software development system)	Yes	Yes	Yes	Yes
In-System Emulator (Tests system in place)	Yes	Yes	Yes	Yes
Software Support (from this manufacturer) Resident Assembler	Yes	Yes	Yes	Yes
Cross Assembler	PACE	PACE	PACE	PACE
Simulator				
High Level Language				
Programs Debug	Yes	Yes	Yes	Yes
Diagnostic	Yes	Yes	Yes	Yes
Edit	Yes	Yes	Yes	Yes
User Library (>25 programs from user)	Yes	Yes	Yes	Yes
Delivery Start (Qtr.-Year)	4 Qtr. 78	2 Qtr. 79	4 Qtr. 78, 2/3 Qtr. 79	3 Qtr. 79
Alternate Sources	Western Digital	Western Digital	Western Digital	Western Digital
Comments			COP421 Series also available. Identical to COP420 in 24-pin package.	

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MICROPROCESSORS (cont)

Manufacturer Model For Detailed Data See:	National INS2650	National INS8080A	National INS8900	National ISP-8A (SC/MP)
General Structure	8-Bit CPU	8-Bit CPU	16-Bit CPU	8-Bit CPU
Type	NMOS	NMOS	NMOS	NMOS
No. of Devices per CPU	1	1	1	1
CPU Size (Pins)	40	40	40	40
Supply Voltage	5	±5, 12	±5, 12	5
CPU Power Dissipation (mw)	525	780		420
Architecture Data Word Size (bits)	8	8	8 or 16	8
Instruction Word Size (bits)	8, 16, 24	8, 16, 24	16	8, 16
Directly Addressable Instruction Words (No.)	32K	65K	65K	65K
Clock Frequency (Hz/ext. phases required)	0 to 1.25 MHz/1 phase	2 MHz/2 phase (2.6 & 3 MHz opt.)	2 MHz/1 phase	4 MHz/0 phase
Register to Register Add Time (μsec/data word)	4.8	2 (2 MHz)	8	7
No. of Registers Arithmetic	0	1	4	1
Index	0	0	2	4
General Purpose	7	6	4	3
Return Stack Size (No. x bits)	8x15	External RAM	10x16	Software Stack
Interrupts	Standard	Standard	Standard	Standard
Type	Vectored	Vectored, Multilevel	Vectored, 6 Level	Vectored
Direct Memory Access	Standard	Standard	Optional	Standard
BCD Arithmetic (Hardware)	Standard	Yes	Standard	Standard
Microprogrammable	No	No	No	No
Extended Temp. Range Available	No	−40° to 85°C −55° to 125°C	−55°C to 85°C	−55°C to 85°C
Devices See System Components:	2650	8080	INS8900	SC/MP
Hardware Support Processor Cards (CPU system on a card)	Yes	Yes	Yes	Yes
Prototyping System (Hardware & software development system)	Yes	Yes	Yes	Yes
In-System Emulator (Tests system in place)	Yes	Yes	No	Yes
Software Support (from this manufacturer) Resident Assembler	Yes	Yes	Yes	Yes
Cross Assembler	Fortran IV, PDP-11	Yes	Fortran IV	Fortran IV, Timesharing
Simulator	Fortran IV	No	No	No
High Level Language	PLμS	Basic (LLL)	Basic	Tiny Basic
Programs Debug	Yes	Yes	Yes	Yes
Diagnostic	Yes	Yes	Yes	Yes
Edit	Yes	Yes	Yes	Yes
User Library (>25 programs from user)	No	No	Yes	Yes
Delivery Start (Qtr.-Year)		3 Qtr. 76	3 Qtr. 77	1 Qtr. 76
Alternate Sources	Signetics	AMD, Intel, Mitsubishi, NEC, Signetics, TI	None	Signetics
Comments		Hardware and software support thru independent company.		

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MICROPROCESSORS (cont)

Manufacturer Model For Detailed Data See:	National MM5781/82	National MM5799	National MM57140	NEC Micro μCOM-42
General Structure	4-Bit CPU	4-Bit Microcomputer	4-Bit Microcomputer	4-Bit Microcomputer
Type	PMOS	PMOS	PMOS	PMOS
No. of Devices per CPU	1	1	1	1
CPU Size (Pins)	28	28	28	42
Supply Voltage	8.5	8.5	8.5	10
CPU Power Dissipation (mw)	150	150	125	300
Architecture Data Word Size (bits)	4	4	4	4
Instruction Word Size (bits)	8	8	8	10
Directly Addressable Instruction Words (No.)	2K to 16K	1536 (internal)	630 (internal)	1920
Clock Frequency (Hz/ext. phases required)	400 kHz/0 phase	400 kHz/0 phase	280 kHz/0 phase	200 kHz/1 phase
Register to Register Add Time (μsec/data word)	10	10	14	10
No. of Registers Arithmetic	0	0	0	1
Index	0	0	0	0
General Purpose	3	3	3	96
Return Stack Size (No. x bits)	2x11	2x11	2x11	4x11
Interrupts	Standard	None	None	Yes
Type	1 Level			Dual
Direct Memory Access	None	None	None	None
BCD Arithmetic (Hardware)	Yes	Yes	Yes	Yes
Microprogrammable	No	No	No	No
Extended Temp. Range Available				No
Devices See System Components:	5781/82	5799	5799	μCOM-4
Hardware Support Processor Cards (CPU system on a card)	Yes	No	No	Yes
Prototyping System (Hardware & software development system)	Yes	Yes	Yes	Yes
In-System Emulator (Tests system in place)	Yes	No		No
Software Support (from this manufacturer) Resident Assembler	No	No	No	No
Cross Assembler	Yes	Yes	Yes	8080/Fortran IV
Simulator	Yes	Timesharing		No
High Level Language	No	No	No	No
Programs Debug	Yes	Yes	Yes	No
Diagnostic	Yes	Yes	Yes	No
Edit	Yes	Yes	Yes	Yes
User Library (>25 programs from user)	No	No	No	No
Delivery Start (Qtr.-Year)	4 Qtr. 75	2 Qtr. 76	1 Qtr. 77	1 Qtr. 77
Alternate Sources	None	None	None	None
Comments	2 chip calculator based system, expandable RAM, ROM, I/O.	1 chip calculator based system, expandable RAM, I/O.	1 chip calculator based system, expandable I/O.	

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MICROPROCESSORS (cont)

Manufacturer Model For Detailed Data See:	Panasonic MN1400	Raytheon Semi 2900	RCA CDP1802C/CDP2802	Rockwell PPS-4/1
General Structure	4-Bit Microcomputer	4-Bit Slice	8-Bit CPU	4-Bit CPU/Microcomputer
Type	NMOS	TTL	CMOS	PMOS
No. of Devices per CPU	1	Varies	1	1
CPU Size (Pins)	28/40/64	40	40	28/40/42/52
Supply Voltage	5	5	4 to 6/3 to 12	−15 (or −6.5 to 11)
CPU Power Dissipation (mw)	500	925	8 @ 5V/40 @ 10V	200
Architecture Data Word Size (bits)	4	Multiple of 4	8	4
Instruction Word Size (bits)	8	9	8, 16, 24	8, 16
Directly Addressable Instruction Words (No.)	768 or 1024 (internal)	User defined	65K	Various
Clock Frequency (Hz/ext. phases required)	0-300 kHz/0 phase	to 10 MHz/1 phase	0-6.4 MHz/0 phase	
Register to Register Add Time (μsec/data word)	10	0.125	2.5 (6.4 MHz clock)	
No. of Registers Arithmetic		0	1	1
Index		0	0	0
General Purpose		17	32	1
Return Stack Size (No. x bits)		4x4 (2909)	External RAM	
Interrupts		Optional	Standard	
Type			1 Level	
Direct Memory Access		Optional	Standard (on-chip)	
BCD Arithmetic (Hardware)	No	No	No	No
Microprogrammable	No	Yes	No	No
Extended Temp. Range Available	None	−55°C to 125°C	−55°C to 125°C Standard	
Devices See System Components:	1400	2900	1800	PPS-4, PPS-8
Hardware Support Processor Cards (CPU system on a card)		Yes	Yes	
Prototyping System (Hardware & software development system)		No	Yes	Yes
In-System Emulator (Tests system in place)		No	No	Yes
Software Support (from this manufacturer) Resident Assembler	No	No	Yes	Yes
Cross Assembler	Yes	Yes	Fortran IV, Timesharing	
Simulator	Yes	No	Yes	Yes
High Level Language	No	No	No	No
Programs Debug	Yes	No	Yes	Yes
Diagnostic	Yes	No	Yes	Yes
Edit	Yes	No	Yes	Yes
User Library (>25 programs from user)	No	No	No	
Delivery Start (Qtr.-Year)	4 Qtr. 77	1 Qtr. 76	1 Qtr. 76	2 Qtr. 76
Alternate Sources	None	AMD, Fairchild, Motorola, National, NEC, Signetics, MMI	Hughes, SSS	
Comments		Microassembler on timeshare.		1-chip parallel microcomputer, several memory options and instruction sets.

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MICROPROCESSORS (cont)

Manufacturer Model For Detailed Data See:	Rockwell PPS-4/2, PPS-4	Rockwell PPS-8	Rockwell R6500	Signetics N3000
General Structure	4-Bit CPU	8-Bit CPU	8-Bit Microcomputer	2-Bit Slice
Type	PMOS	PMOS	NMOS	TTL
No. of Devices per CPU	1	1	1	
CPU Size (Pins)	42	42	28 or 40	28 and 40
Supply Voltage	17 (or −12, 5)	17 (or −12, 5)	5	5
CPU Power Dissipation (mw)	225	225	700	800
Architecture Data Word Size (bits)	4	8	8	Multiple of 2
Instruction Word Size (bits)	8, 16 (Multifunction instr.)	8, 16, 24 (Multifunction instr.)	8, 16, 24	≥18
Directly Addressable Instruction Words (No.)	4K	16K	to 65K	512
Clock Frequency (Hz/ext. phases required)	(PPS-4) 256 kHz/2 phase (PPS-4/2) 199 kHz/0 or 2 phase	(PPS 8/2) 189 kHz/0 phase (PPS-8) 256 kHz/2 phase	1 and 2 MHz/0-2 phase	to 6 MHz/1 phase
Register to Register Add Time (μsec/data word)	5	(PPS-8/2) 5 (PPS-8) 4	1	
No. of Registers Arithmetic	0	1	1	2
Index	0	0	2	0
General Purpose	3	6	0	10
Return Stack Size (No. x bits)	2x12	32x8	1x8	None
Interrupts	Standard PPS-4	Standard	Standard	Optional
Type	1 Level	3 Level	2 Level	8 Level Priority
Direct Memory Access	None	Optional DMA Controller	Optional	No
BCD Arithmetic (Hardware)	No	No	Yes	No
Microprogrammable	No	No	No	Yes
Extended Temp. Range Available	−55°C to 125°C	−55°C to 125°C	No	No
Devices See System Components:	PPS-4, PPS-8	PPS-4, PPS-8	6500	3000
Hardware Support Processor Cards (CPU system on a card)	Yes	Yes	Yes	No
Prototyping System (Hardware & software development system)	Yes	Yes	Yes	No
In-System Emulator (Tests system in place)	Yes	Yes	Yes	No
Software Support (from this manufacturer) Resident Assembler	Yes	Yes	Yes	No
Cross Assembler	Fortran IV, Timesharing	Fortran IV, Timesharing	Yes	No
Simulator	Yes	Yes	Yes	No
High Level Language	No	No	No	No
Programs Debug	Yes	Yes	Yes	No
Diagnostic	Yes	Yes	Yes	No
Edit	Yes	Yes	Yes	No
User Library (>25 programs from user)	Yes	No	No	No
Delivery Start (Qtr.-Year)	PPS-4 3 Qtr. 72 PPS-4/2 3 Qtr. 75	PPS-8 1 Qtr. 75, PPS-8/2 2 Qtr. 76	3 Qtr. 77	3 Qtr. 75
Alternate Sources			MOS Technology, Synertek	Intel
Comments	The PPS-4/2 is a 2 chip clock, direct display drive, expanded I/O on CPU chip; 128-4 RAM, 2048x8 ROM, 16 I/O ports on separate memory-I/O chip.		Bus compatible with 6800.	Uses 74S182 for Look-Ahead Carry.

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MICROPROCESSORS (cont)

Manufacturer Model For Detailed Data See:	Signetics 2650A/B (Page 2302)	Signetics 8021	Signetics 8035/8048/8748 (Page 2310)	Signetics 8X02/2901-1 (Page 2280)
General Structure	8-Bit CPU	8-Bit Microcomputer	8-Bit Microcomputer	4-Bit Slice
Type	NMOS	NMOS	NMOS	TTL
No. of Devices per CPU	1	1	1	Varies
CPU Size (Pins)	40	28	40	28 and 40
Supply Voltage	5	5	5	5
CPU Power Dissipation (mw)	525	150	325	1320
Architecture Data Word Size (bits)	8	8	8	Multiple of 4
Instruction Word Size (bits)	8, 16, 24	8, 16	8, 16	$\geq$18
Directly Addressable Instruction Words (No.)	32K	1K	4K	User defined
Clock Frequency (Hz/ext. phases required)	0 to 2 MHz/1 phase(−1 type) 0 to 1.25 MHz/1 phase	3 MHz/0 phase	6 MHz/0 phase	
Register to Register Add Time (μsec/data word)	1.5 (B−1) 4.8 (A)	10	2.5	
No. of Registers Arithmetic	0	16	16	
Index	0	0	0	
General Purpose	7	64	64	16
Return Stack Size (No. x bits)	8x15	8x16	8x16	
Interrupts	Standard	None	Yes	Optional
Type	Vectored		Dual, 1 Level, Vectored	
Direct Memory Access	Standard	No	No	No
BCD Arithmetic (Hardware)	Standard	Yes	Yes	No
Microprogrammable	No	No	No	Yes
Extended Temp. Range Available	No		−55°C to 125°C	No
Devices See System Components:	2650	8048	8048	2900
Hardware Support Processor Cards (CPU system on a card)	Yes	Yes	Yes	No
Prototyping System (Hardware & software development system)	Yes	Yes	Yes	No
In-System Emulator (Tests system in place)	Yes	Yes	Yes	No
Software Support (from this manufacturer) Resident Assembler	Yes	Yes	Yes	No
Cross Assembler	Fortran IV, PDP-11	No	No	Yes
Simulator	Fortran IV	No	No	No
High Level Language	PLμS	No	No	No
Programs Debug	Yes	Yes	Yes	No
Diagnostic	Yes	Yes	Yes	No
Edit	Yes	Yes	Yes	
User Library (>25 programs from user)	No	No	No	No
Delivery Start (Qtr.-Year)	2 Qtr. 75	4 Qtr. 78	2 Qtr. 78	4 Qtr. 77
Alternate Sources	National	Intel	AMD, Fujitsu, Intel NEC	AMD, Fairchild, Motorola, National, NEC, Raytheon
Comments	Any of the general purpose registers can be used as an index register.			The 2901-1 can be used with 2909/2911 sequences as well as the 8X02.

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MICROPROCESSORS (cont)

Manufacturer Model For Detailed Data See:	Signetics 8X300 (Page 2282)	Signetics 8080A (Page 2312)	SMC SMC9980	SSS SCP1802L/SCP1802
General Structure	8-Bit CPU	8-Bit CPU	16-Bit CPU	8-Bit CPU
Type	TTL	NMOS	NMOS	CMOS
No. of Devices per CPU	1	1	1	1
CPU Size (Pins)	50	40	40	40
Supply Voltage	5	±5, 12	±5, 12	4-6/4-12
CPU Power Dissipation (mw)	2000	780	1000	4 @ 5V/60 @ 10V
Architecture Data Word Size (bits)	8	8	8	8
Instruction Word Size (bits)	16	8, 16, 24	16, 32, 48	8, 16, or 24
Directly Addressable Instruction Words (No.)	8K	65K	16K bytes	65K
Clock Frequency (Hz/ext. phases required)	8 MHz/phase	2 MHz/2 phase	2-3 MHz/phase	3.2 MHz/1 phase (L) 6.4 MHz/1 phase
Register to Register Add Time (μsec/data word)	0.25	2	8.8 (2 MHz clock)	5/2.5
No. of Registers Arithmetic		1	16	1
Index		0	15	1
General Purpose	8	6	16 (in memory)	32
Return Stack Size (No. x bits)		External RAM	None	External RAM
Interrupts	Yes	Standard	Standard	1
Type	Polled	Vectored, Multilevel	Vectored, 6 level	Vectored
Direct Memory Access	Yes	Standard	Standard	On-chip
BCD Arithmetic (Hardware)	No	Yes	No	No
Microprogrammable	No	No	No	No
Extended Temp. Range Available	Future			−55°C to 125°C std.
Devices See System Components:	8X300	8080	9900	1800
Hardware Support Processor Cards (CPU system on a card)	Yes		No	Yes
Prototyping System (Hardware & software development system)	Yes		No	Yes
In-System Emulator (Tests system in place)	Yes		No	Yes
Software Support (from this manufacturer) Resident Assembler	No		No	Yes
Cross Assembler	Yes		No	Yes
Simulator			No	No
High Level Language	No		No	Yes
Programs Debug	No		No	Yes
Diagnostic	Yes		No	Yes
Edit			No	Yes
User Library (>25 programs from user)	No		No	No
Delivery Start (Qtr.-Year)	3 Qtr. 76	4 Qtr. 77	2 Qtr. 79	3 Qtr. 77
Alternate Sources		AMD, Intel, National, NEC, TI	AMI, SMC	Hughes, RCA
Comments	Bipolar with fixed instructions.		8-Bit data bus, 16-Bit internal op. Software compatible TM9900.	MIL version available. 4 Qtr. 78.

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MICROPROCESSORS (cont)

Manufacturer Model For Detailed Data See:	Synertek Sy6500	Texas Instruments SBP0400A/SBP0401A	Texas Instruments SBP9900A	Texas Instruments SN54/74LS481
General Structure	8-Bit CPU	4-Bit Slice	16-Bit CPU	4-Bit Slice
Type	NMOS	I^2L	I^2L	TTL-LS
No. of Devices per CPU	1		1	
CPU Size (Pins)	40 or 28	40	64	48
Supply Voltage	5	200 mA at 0.85V	500 mA	5
CPU Power Dissipation (mw)	200	170	500	1000
Architecture Data Word Size (bits)	8	9 (Microinstruction Select)	16	Multiple of 4
Instruction Word Size (bits)	8, 16, 24		16, 32, 48	11
Directly Addressable Instruction Words (No.)	65K	(512 Microinstructions)	32K	Multiple of 4 Bits
Clock Frequency (Hz/ext. phases required)	to 2 MHz/1 phase	to 2 MHz/1 phase	0-3 MHz/1 phase	0-9 MHz/1 phase
Register to Register Add Time (μsec/data word)	1	0.5 (2 MHz clock)	4.67	0.11
No. of Registers Arithmetic	1	2	16	2
Index	2	0	15	0
General Purpose	0	8	16	16
Return Stack Size (No. x bits)	External RAM	None	None	None
Interrupts	Standard	Optional	Standard	Optional
Type	Vectored, 2 Level	Optional	Vectored, 16 Levels	
Direct Memory Access	Optional	Standard	Yes	Standard
BCD Arithmetic (Hardware)	Yes	Microprogrammable	No	Yes
Microprogrammable	No	(512 Microinstructions)	No	Yes
Extended Temp. Range Available	−55°C to 85°C	−55°C to 125°C	−55°C to 125°C Standard	−55°C to 125°C
Devices See System Components:	6500	SBP400	9900	54/74LS481
Hardware Support Processor Cards (CPU system on a card)	Yes	No	Yes	Yes
Prototyping System (Hardware & software development system)	Yes	Yes (hardware)	Yes	Future
In-System Emulator (Tests system in place)	Yes	No	Yes	No
Software Support (from this manufacturer) Resident Assembler	Yes	No	Yes	No
Cross Assembler	Fortran IV	Fortran microassembler	Yes	No
Simulator	Fortran IV	No	Timesharing	No
High Level Language	No	No	Fortran, Cobol	No
Programs Debug	Yes	No	Yes	No
Diagnostic	Yes	No	Yes	No
Edit	No	No	Yes	No
User Library (>25 programs from user)	No	No	Yes	No
Delivery Start (Qtr.-Year)	4 Qtr. 75	1 Qtr. 75	1 Qtr. 77	1 Qtr. 78
Alternate Sources	MOS Technology, Rockwell	None	None	None
Comments	DMA based on a stopping CPU, but address bus connections are not 3 state.	Current drain can be set from 0.001 to 200 mA.	Software compatible with 990 minicomputer.	24780 Micro- and Macro- instructions.

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MICROPROCESSORS (cont)

Manufacturer Model For Detailed Data See:	Texas Instruments SN74S481	Texas Instruments TMS1000/1200	Texas Instruments TMS1000C/TMS1200C	Texas Instruments TMS1070/1270
General Structure	4-Bit Slice	4-Bit Microcomputer	4-Bit Microcomputer	4-Bit Microcomputer
Type	TTL-S	PMOS	CMOS	PMOS
No. of Devices per CPU		1	1	1
CPU Size (Pins)	48	28 or 40	28 or 40	28 or 40
Supply Voltage	5	9 or 15	3-6	15
CPU Power Dissipation (mw)	2000	65/90	10 μW (typ.)	100
Architecture Data Word Size (bits)	Multiple of 4	4	4	4
Instruction Word Size (bits)		8	8	8
Directly Addressable Instruction Words (No.)		1K	1K	1K
Clock Frequency (Hz/ext. phases required)	0-15 MHz/1 phase	300 kHz/0 phase	1 MHz	300 kHz/0 phase
Register to Register Add Time (μsec/data word)	0.06	34 (350 kHz clock)		34 (350 kHz clock)
No. of Registers Arithmetic	2	1	1	1
Index	0	0	0	0
General Purpose	16	1	1	1
Return Stack Size (No. x bits)	None	1x10	1x10	1x10
Interrupts	Optional	None	1200C provides pseudo-interrupt capability	None
Type				
Direct Memory Access	Standard	None	None	None
BCD Arithmetic (Hardware)	Yes	Microprogrammable	Microprogrammable	Microprogrammable
Microprogrammable	Yes	Yes	Yes	Yes
Extended Temp. Range Available	Future		Future	Yes
Devices See System Components:	74S481	1000	1000	1000
Hardware Support Processor Cards (CPU system on a card)	Yes	No	Yes	No
Prototyping System (Hardware & software development system)	Future	Yes	Yes	Yes
In-System Emulator (Tests system in place)	No	Yes	Yes	No
Software Support (from this manufacturer) Resident Assembler	No	Yes	Yes	Yes
Cross Assembler	No	Timesharing	Timesharing	Yes
Simulator	No	Timesharing	Timesharing	Yes
High Level Language	No	No		No
Programs Debug	No	Yes	Yes	Yes
Diagnostic	No	Yes	Yes	Yes
Edit	No	Yes	Yes	Yes
User Library (>25 programs from user)	No			
Delivery Start (Qtr.-Year)	4 Qtr. 77	1 Qtr. 75	3 Qtr. 78	4 Qtr. 75
Alternate Sources	None	None	None	None
Comments	24780 Micro- and Macro- instructions.	A 64 pin version, TMS-1099/SE-1, permits use of external PROM, RAM or ROM for program development.	3 level subroutine nesting, 32 term output PLA. TMS1099C/SE-3 for program development.	35V output drive capability.

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MICROPROCESSORS (cont)

Manufacturer Model For Detailed Data See:	Texas Instruments TMS1100/1300	Texas Instruments TMS8080A	Texas Instruments TMS9900	Texas Instruments TMS9940
General Structure	4-Bit Microcomputer	8-Bit CPU	16-Bit CPU	16-Bit Microcomputer
Type	PMOS	NMOS	NMOS	NMOS
No. of Devices per CPU	1	1	1	1
CPU Size (Pins)	28 or 40	40	64	40
Supply Voltage	9 or 15	±5, 12	±5, 12	5
CPU Power Dissipation (mw)	90	1500	1000	1000
Architecture Data Word Size (bits)	4	8	16	16
Instruction Word Size (bits)	8	8, 16, 24	16, 32, 48	16, 32, 48
Directly Addressable Instruction Words (No.)	2K	65K	65K bytes/32K words	1K
Clock Frequency (Hz/ext. phases required)	300 kHz/0 phase	2 MHz/2 phase	3 MHz/4 phase	5 MHz/1 phase
Register to Register Add Time (μsec/data word)	34 (350 kHz clock)	2	4.67	
No. of Registers Arithmetic	1	1	16	16
Index	0	0	15	15
General Purpose	1	6	16 (in memory)	16
Return Stack Size (No. x bits)	1x10	External RAM	None	
Interrupts	None	Standard	Standard	Standard
Type		Vectored, 8 Level	Vectored, 16 Level	Masked, Prioritized, Vectored
Direct Memory Access	None	Standard	Standard	
BCD Arithmetic (Hardware)	Microprogrammable	Yes	No	Yes
Microprogrammable	Yes	No	No	12 XOPs
Extended Temp. Range Available	Yes	No	−25°C to 85°C	No
Devices See System Components:	1000	8080	9900	9900
Hardware Support Processor Cards (CPU system on a card)	No	No	Yes 990/4	Yes
Prototyping System (Hardware & software development system)	Yes	No	Yes	Yes
In-System Emulator (Tests system in place)	Yes	No	No	Yes
Software Support (from this manufacturer) Resident Assembler	Yes	No	Yes	Yes
Cross Assembler	Yes	Timesharing	Yes	Fortran IV
Simulator	Yes	Timesharing	Timesharing	Yes
High Level Language	No	No	Fortran, Cobol	Basic, Pascal
Programs Debug	Yes	Yes	Yes	Yes
Diagnostic	Yes	Yes	Yes	Yes
Edit	Yes	Yes	Yes	Yes
User Library (>25 programs from user)		No	Yes	Yes
Delivery Start (Qtr.-Year)	4 Qtr. 75	2 Qtr. 75	2 Qtr. 76	1 Qtr. 79
Alternate Sources	None	AMD, Intel, National, NEC, Signetics	AMI	AMI
Comments	A 64-pin version, TMS1098/SE-2 permits use of external PROM/RAM/ROM for program development.		Instructions include hardware multiply and divide and are software compatible with 990 minicomputers.	TMS9900 compatible with 128 bytes RAM 2K bytes ROM 16-Bit instruction set.

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MICROPROCESSORS (cont)

Manufacturer Model For Detailed Data See:	Texas Instruments TMS9980	Texas Instruments TMS9985	Toshiba TLCS-12A	Western Digital MP1600	Western Digital CP1600	Western Digital WD40	Zilog Z80
General Structure	16-Bit CPU	16-Bit CPU	12-Bit CPU	16-Bit CPU	8-Bit CPU	4-Bit Microcomputer	8-Bit CPU
Type	NMOS	NMOS	PMOS	NMOS	NMOS	PMOS	NMOS
No. of Devices per CPU	1	1	1	3	3	1	1
CPU Size (Pins)	40	40	36	40/device	40/device	28 or 40	40
Supply Voltage	±5, 12	5	±5	±5, 12	±5, 12	−8, 5	5
CPU Power Dissipation (mw)	1000	600	800	600	600		1100
Architecture Data Word Size (bits)	8	8 or 16	12	16	8 or 16	4	8, 16
Instruction Word Size (bits)	16, 32, 48	16, 32, 48	12, 24	16	16	10, 20	8, 16, 24, 32
Directly Addressable Instruction Words (No.)	16K bytes	65K	4K	65K	65K (84 Micro-instructions)	400 or 512	65K
Clock Frequency (Hz/ext. phases required)	2-3 MHz/ phase	5 MHz/ 1 phase	1.2 MHz/ 0 phase	3.3 MHz/ 4 phase	3.3 MHz/ 4 phase	100 kHz/ 0 phase	2.5 MHz/1 phase (4 MHz opt.)
Register to Register Add Time (μsec/data word)	8.8 (2 MHz)	2.4	13	2.7	0.3 (8-Bit) 0.6 (16-Bit)	60	1.6 (2.5 MHz clock)
No. of Registers Arithmetic	16	16	0	4	0	4	1
Index	15	15	0	2	0	0	2
General Purpose	16 (in memory)	16	7	2	26	5	14
Return Stack Size (No. x bits)	None	N/A		External RAM	External RAM	1x10	External Ram
Interrupts	Standard	6	Yes	Standard	Standard	None	Standard
Type	Vectored, 6 Level	Vectored, Prioritized		Vectored	Vectored, 4 Level		Vectored, Multilevel
Direct Memory Access	Standard	Yes	Optional	Standard	Standard	No	Z80-DMA
BCD Arithmetic (Hardware)	No	Yes	No	Standard	Micro-programmable	Yes	Yes
Microprogrammable	No	No	No	Yes	Yes	No	No
Extended Temp. Range Available		Yes		No	No	No	−55°C to 125°C
Devices See System Components:	9900	9900	TLCS-12	1600	1600	WD40	Z80
Hardware Support Processor Cards (CPU system on a card)	No	Yes	No	Yes	Yes	No	Yes
Prototyping System (Hardware & software development system)	Yes	Yes	Yes	Yes	Yes	No	Yes
In-System Emulator (Tests system in place)	No	Yes	No	No	Yes	Yes	Yes
Software Support (from this manufacturer) Resident Assembler	Yes	Yes		Yes	No	No	Yes
Cross Assembler	Timesharing	Yes	Yes	No	Timesharing, PDP-11	No	Fortran IV
Simulator	Timesharing	Yes	Yes	No	Timesharing, PDP-11	No	Timesharing
High Level Language	Fortran, Cobol	Pascal, Fortran	Yes	No	No	No	PL/Z
Programs Debug	Yes	Yes	Yes	Yes	Yes	No	Yes
Diagnostic	Yes	Yes	Yes	Yes	Yes	No	Yes
Edit	Yes	Yes	Yes	Yes	Yes	No	Yes
User Library (>25 programs from user)	Yes	No	Yes	No	No	No	No
Delivery Start (Qtr.-Year)	4 Qtr. 76	4 Qtr. 78	2 Qtr. 74	1 Qtr. 75	3 Qtr. 75	3 Qtr. 77	1 Qtr. 76
Alternate Sources	AMI, SMC	AMI	None	None	None	None	Mostek, NEC
Comments	8-Bit data bus, 16-Bit internal op. Software compatible TMS9900.				Can cross assemble and simulate with DEC PDP-11.	A 64-pin version, CR2872 permits use of external PROM, RAM or ROM for program development.	8080A Software compatible.

Tinted column indicates additional data is provided on the page noted.

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MICROPROCESSOR–System Components

This section presents the major microprocessor system devices organized into system groups, ie F8, 6800, 8080, etc. It includes those RAM's, ROM's and PROM's which are unique to a system. It omits most general purpose memories as they are listed in the Memory section. Similarly, buffers, line drivers, transceivers, UART's, etc. are covered briefly here as they are presented in depth in the Digital and Interface sections.

μCOM-4

Function	Device	Source	Line
Microcomputer			
	μCOM-42	**NEC Micro (2051)**	10
	μPD548	**NEC Micro (2051)**	
	μCOM-43	**NEC Micro (2059)**	
	μPD546	**NEC Micro (2059)**	
	μPD553	**NEC Micro (2059)**	
	μPD650	**NEC Micro (2059)**	
	μCOM-44	**NEC Micro (2059)**	
	μPD547	**NEC Micro (2059)**	
	μPD552	**NEC Micro (2059)**	
	μPD651	**NEC Micro (2059)**	20
	μCOM-45	**NEC Micro (2059)**	
	μPD550	**NEC Micro (2059)**	
	μPD554	**NEC Micro (2059)**	
	μPD652	**NEC Micro (2059)**	
	μCOM-46	NEC Micro	
	μPD551	NEC Micro	
Evaluation Devices			
	μPD555	**NEC Micro (2055)**	
	μPD556	**NEC Micro (2065)**	

COP400

Function	Device	Source	Line
Microcontroller (with ROM)			
	COP410L	**National (2034,2044)**	30
	COP411L	**National (2036,2044)**	
	COP420	**National (2044)**	
	COP420C	**National (2040)**	
	COP420L	**National (2038)**	
	COP421	**National (2044)**	
	COP421C	**National (2040)**	
	COP421L	**National (2038)**	40
	COP440	**National (2044)**	
	COP444L	**National (2044)**	
Microcontroller (external ROM)			
	COP402	**National (2044,2045)**	
	COP402L	**National (2045)**	
	COP402M	**National (2045)**	
Development System			
	COP400PDS	**National (2042)**	

F8

Function	Device	Source	Line
Central Processing Unit			
	3850	**Fairchild (1867,1871)**	50
	3850M	**† Fairchild (1871)**	
	F8	**Fairchild (1871)**	
	MK3850	Mostek	
Program Storage Unit			
	3851	**Fairchild (1867,1871)**	
	3851A	**Fairchild (1867)**	
	3851M	**† Fairchild (1867,1871)**	60
		(Continued)	

F8 (Cont'd.)

Function	Device	Source	Line
Program Storage Unit		(Cont'd.)	
	3856	**Fairchild (1867,1871)**	
	3856A	**Fairchild (1867,1871)**	
	38T56	**Fairchild (1867,1871)**	
	3857	**Fairchild (1867,1873)**	70
	38T57	**Fairchild (1867,1873)**	
	MK3851	Mostek	
Microcomputer (1 chip)			
	3870	**Fairchild (1863,1867)**	
	38E70	**Fairchild (1864)**	
	3872	Fairchild	
	3874	Fairchild	
	3876	Fairchild	80
	MC3870	**Motorola (1998)**	
	MK3870	Mostek	
	MK3872	Mostek	
Direct Memory Access			
	3854	**Fairchild (1867,1873)**	
	MK3854	Mostek	
Peripheral Input/Output Interface			
	3861	**Fairchild (1867,1874)**	90
	3861M	**† Fairchild (1867,1874)**	
	3871	**Fairchild (1867,1874)**	
	MK3861	Mostek	
	MK3871	Mostek	
Analog input, MUX, A/D converter			
	MP21	**Burr-Brown (659)**	
Dynamic Memory Interface			
	3852	**Fairchild (1867,1871)**	100
	MK3852	Mostek	
Static Memory Interface			
	3853	**Fairchild (1867,1871)**	
	3853M	**† Fairchild (1867,1871)**	
	MK3853	Mostek	
Development System			
	FORMULATOR	**Fairchild (1865,1875)**	110
	PEP	**Fairchild (1866)**	

HMCS-40

Function	Device	Source	Line
Microcomputer, 4-Bit			
	HCMS42	Hitachi	
	HMCS43	Hitachi	
	HMCS43C	Hitachi	
	HMCS44	Hitachi	
	HMCS45	Hitachi	

Macrologic Bipolar

Function	Device	Source	Line
Microprogram Sequencer			
	9408C	**Fairchild (1893)**	120
	9408AC	**Fairchild (1893)**	
		(Continued)	

Macrologic Bipolar (Cont'd.)

Function	Device	Source	Line
Microprogram Sequencer		(Cont'd.)	
	9408M	**† Fairchild (1893)**	
	9408AM	**† Fairchild (1893)**	
Arithmetic Logic Register-Stack			
	9405C	**Fairchild (1893)**	
	9405AC	**Fairchild (1893)**	
	9405M	**† Fairchild (1893)**	
	9405AM	**† Fairchild (1893)**	
Data Path Switch (for closing data path loops around arithmetic/logic networks such as 9405)			130
	9404C	**Fairchild (1893)**	
	9404M	**† Fairchild (1893)**	
Data Access Register (performs memory address arithmetic)			
	9407C	**Fairchild (1893)**	
	9407M	**† Fairchild (1893)**	
Buffer (16x4 First-In First-Out Memory. See also Memory-FIFO's)			
	9403C	**Fairchild (1893,1896)**	140
	9403M	**† Fairchild (1893,1896)**	
Buffer (64x4 First-In First-Out Memory. See also Memory-FIFO's)			
	9423C	**Fairchild (1893,1896)**	
	9423M	**† Fairchild (1893,1896)**	
Data Encryption, 4 device set			150
	9414-1	Fairchild	
	9414-2	Fairchild	
	9414-3	Fairchild	
	9414-4	Fairchild	
Display Controller			
	9412C	Fairchild	
	9412M	† Fairchild	
Program Stack (16x4 LIFO memory)			
	9406C	**Fairchild (1893)**	
	9406M	**† Fairchild (1893)**	160
CRC Generator/Checker (See also Interface-Error Checking Circuits)			
	9401C	**Fairchild (1893,1894)**	
	9401M	**† Fairchild (1893,1894)**	
	9411C	**Fairchild (1893,1894)**	
	9411M	**† Fairchild (1893,1894)**	170
RAM (16x4) Write-while-Read (See also Digital-TTL-Memories)			
	9410C	**Fairchild (1893)**	
	9410M	**† Fairchild (1893)**	

Macrologic CMOS

Function	Device	Source	Line
Arithmetic Logic Register Stack			
	F4705BC	Fairchild	
	F4705BM	† Fairchild	
Data Path Switch (for closing data path loops around arithmetic/logic networks such as the F4705)			
	F4704BC	Fairchild	180
	F4704BM	† Fairchild	

† Military Temperature Range (−55° to 125°C)

* Typical Values

MICROPROCESSOR–System Components (Cont'd)

Macrologic CMOS (Cont'd.)

Data Access Register (performs memory address arithmetic)
- F4707BC — Fairchild
- F4707BM — † Fairchild

Microprogram Sequencer
- F4708C — Fairchild
- F4708M — † Fairchild

Parallel/Serial First-In First-Out Memory (FIFO) (See also Memory-FIFO's)
- F4703BC — Fairchild
- F4703BM — † Fairchild

Program Stack (16x4 LIFO Memory)
- F4706BC — Fairchild
- F4706BM — † Fairchild

Programmable Bit Rate Generator (See also Digital-CMOS-Miscellaneous-Bit Rate Generator)
- F4702BC — Fairchild
- F4702BM — † Fairchild
- **HD4702-2 — Harris (1926)**
- **HD4702-9 — † Harris (1926)**
- **HD4702A-2 — † Harris (1926)**
- **HD4702A-9 — Harris (1926)**

RAM (16x4, clocked) Write-while-Read (See also Digital-CMOS-Memories)
- F4710BC — Fairchild
- F4710BM — † Fairchild

RAM (16x4) (See also Memory-RAM's)
- F4725BC — Fairchild
- F4725BM — † Fairchild

RAM (256x1) (See also Memory-RAM's)
- F4720C — Fairchild
- F4720M — † Fairchild

RAM (256X4) (See also Memory-RAMS)
- F4726BC — Fairchild
- F4726BM — † Fairchild

ROM (256X8) (See also Memory-ROMS)
- F4735BC — Fairchild
- F4735BM — † Fairchild

MicroNOVA

CPU
- MN601 — Data General
- MICRONOVA — Data General

I/O Transceiver
- MN629 — Data General

I/O Transceiver Buffer
- MN636 — Data General

Memory Bus Transceiver, Octal
- MN634 — Data General

Intelligent I/O Controller
- MN603 — Data General

Memory Address Driver
- MN633 — Data General

RAM (4096x1)
- MN606 — Data General

Sense Amplifier (for MN606)
- MN506 — Data General

M380

CPU
- M38 — SGS
- M380 — SGS

M380 (Cont'd.)

RAM/ROM/I/O
- M381 — SGS

RAM/I/O
- M383 — SGS

ROM/I/O
- M382 — SGS

INS8900

CPU
- INS8900 — National

Interface Latch Elements (ILE)
- DP8301 — National

CMOS Clock
- MM74C04 — National

Erasable PROM: See Memory PROMS

PPS-4, PPS-8

CPU (for PPS-4)
- 12660 — Rockwell

ROM-RAM (for PPS-4)
- A07XX — Rockwell
- A08XX — Rockwell
- A20XX — Rockwell

Microcomputer(PPS-4/1)
- MM75 — Rockwell
- MM76 — Rockwell
- MM76L — Rockwell
- MM76EL — Rockwell
- MM77 — Rockwell
- MM77L — Rockwell
- MM78 — Rockwell
- MM78L — Rockwell
- MM7899 — Rockwell

CPU Evaluation Circuit (for PPS-4/1)
- A7699 — Rockwell

CPU (for PPS-4/2)
- 11660 — Rockwell

ROM-RAM (for PPS-4/2)
- A17XX — Rockwell

CPU (for PPS-8)
- 11806 — Rockwell

CPU (for PPS-8/2)
- 12806 — Rockwell

ROM-RAM (for PPS 8/2)
- A21XX — Rockwell

Bus Interface Circuit (BIC)
- 10738 — Rockwell

Clock Generator (CLK) (for PPS-4, PPS-8)
- 10706 — Rockwell

Direct Memory Access Controller (DMA) (for PPS-8)
- 10817 — Rockwell

Display Controller (DC)
- 10814 — Rockwell

Floppy Disk Controller (FDC) (for PPS-8)
- 10936 — Rockwell

General Purpose Keyboard and Display Control (GPKD)
- 10788 — Rockwell

General Purpose Input/Output (GPI/O)
- 10696 — Rockwell

(Continued)

PPS-4, PPS-8 (Cont'd.)

General Purpose Input/Output (GPI/O) (Cont'd.)
- 11696 — Rockwell

Interval Timer
- 11049 — Rockwell

Keyboard/Printer Controller (KPC)
- 10815 — Rockwell

Printer Controller (PC)
- 10789 — Rockwell
- RC7000 — Rockwell

Victor Dot Matrix Printer Controller (VPC)
- 10736 — Rockwell
- 15380 — Rockwell

Parallel Data Controller (PDC) (for PPS-8, PPS-8/12)
- 10453 — Rockwell

Serial Data Controller (SDC)
- 10930 — Rockwell

Telecommunications Data Interface (includes modem)
- 10371 — Rockwell

RAM (256x4) (for PPS-4, PPS-4/2)
- 10432 — Rockwell

RAM (512x4) (for PPS-4, PPS-4/2)
- 10932 — Rockwell

RAM (256x8) (for PPS-8, PPS-8/2)
- 10809 — Rockwell

4K RAM Interface
- 10929 — Rockwell

ROM (1024x8)
- A05XX — Rockwell

ROM (2048x8)
- A52XX — Rockwell

ROM (4096x8)
- A66XX — Rockwell

ROM (8192x8)
- A88XX — Rockwell

SBA

Sequential Boolean Analyzer
- SBA — GI

SBA Development Device
- SBA-1 — GI

SBP0400

CPU, 4-Bit Slice
- SBP0400AC — TI
- SBP0400AM — † TI
- SBP0401AC — TI
- SBP0401AM — † TI

4-Bit Slice Control Element
- SN54S482 — † TI
- SN74S482 — TI

SC/MP

Microprocessor
- **SC/MP — National (2029,297)**
- **INS8060 — National (2029,297)**
- ISP-8A/500 — National
- ISP-8A/600 — National

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Values

Bold face indicates additional data is provided on the page noted.

MICROPROCESSOR–System Components (Cont'd)

SC/MP (Cont'd.)

Function	Device	Source	Line
Microprocessor (Cont'd.)			
	SC/MP	**Signetics (2314)**	
	ISP-8A/600	**Signetics (2314)**	
8-Bit I/O Port			
	INS8212	National	
Analog Input, Multiplexer, A/D Converter			
	MP20	**Burr-Brown (659)**	
	MP22	**Burr-Brown (659)**	
	INS8292	National	
Bit Programmable I/O			10
	INS8254	National	
UART			
	INS8280	National	
Programmable Communication Interface (USART. See also Interface Transmitters-Receivers)			
	INS8251	National	
Programmable Peripheral Interface			
	INS8255	National	
ROM/RAM and I/O			
	INS2656	National	20
RAM(128x8) and I/O			
	INS8154	National	
	ISP-8A/650	National	
ROM BASIC Interpreter			
	INS8295	National	

SX200

Microcomputer			
	SX200	Essex	

TLCS-12

CPU			
	T3190	Toshiba	
Input/Output Control Unit			30
	T3218	Toshiba	
Memory Control Unit			
	T3216	Toshiba	
Erasable PROM			
	T3181	Toshiba	
RAM (128x4)			
	T3151	Toshiba	

WD40

Microcontroller			
	CR1872	Western	
Prototyping Device			40
	CR2872	Western	

Z80

Note: the 6500, 6800 and 8080 peripheral circuits are compatible with the Z80 series.

CPU			
	3880	Fairchild	
	MK3880	Mostek	
	μPD780	**NEC Micro (2069)**	
	μPD780-1	**NEC Micro (2069)**	
	Z80-CPU	Zilog	
Counter Timer Circuit			50
	MK3882	Mostek	

(Continued)

Z80 (Cont'd.)

Counter Timer Circuit (Cont'd.)			
	Z80-CTC	Zilog	
Direct Memory Access Controller			
	MK3883	Mostek	
	Z80-DMA	Zilog	
Parallel Input/Output Controller			
	MK3881	Mostek	
	Z80-PIO	Zilog	
Serial Input/Output Controller			60
	MK3884	Mostek	
	Z80-SIO	Zilog	
Analog Input, Multiplexer, A/D Converter			
	MP20	**Burr-Brown (659)**	
	MP22	**Burr-Brown (659)**	

1000

Microcomputer			
	TMS1000	TI	
	TMS1070	TI	
	TMS1100	TI	
	TMS1200	TI	70
	TMS1270	TI	
	TMS1300	TI	
Microcomputer (CMOS)			
	MC141000	**Motorola (1956)**	
	MC141200	**Motorola (1956)**	
	TMS1000C	TI	
	TMS1200C	TI	
I/O Expander			
	TMS1024	TI	
	TMS1025	TI	80
Capacitive Input			
	TMS1976	TI	
Arithmetic Processor			
	TMS1018	TI	
Program Development Device (uses external memory)			
	TMS1098	TI	
	TMS1099	TI	
Program Development Device (uses external memory), CMOS			
	MC141099	**Motorola (1956)**	90
	TMS1099C	TI	

1400

Microcomputer			
	MN1400	Panasonic	
	MN1402	Panasonic	
	MN1403	Panasonic	
	MN1405	Panasonic	
	MN1430	Panasonic	
Microcomputer, external memory			
	MN1498	Panasonic	
Microcomputer, evaluator			100
	MN1499	Panasonic	

1600

See also 1600 below.

CPU			
	CP1600	GI	
	CP1600A	GI	
	CP1610	GI	

1600 (Cont'd.)

Dual D/A Converter (two 10-bit pulse-width modulated outputs)			
	DAC1600	GI	
18 Channel Analog Multiplexer			110
	MUX1600	GI	
Input/Output Buffer			
	IOB1680	GI	
ROM (2048x8), Graphics			
	RO3-9503	GI	
ROM (2048x10), Graphics			
	RO3-9501	GI	
	RO3-9502	GI	

1600

See also 1600 above.

CPU, 8-Bit			120
	CP1651	Western	
	CP1661	Western	
CPU, 16-Bit			
	MP1651	Western	
	MP1661	Western	
General Purpose Input/Output			
	CP1851	Western	
Microm			
	CP1631	Western	
Direct Memory Access Controller			130
	DM1881	Western	
	DM1883	Western	
Floppy Disc Controller/Transmitter			
	INS1771	National	
	INS1781	National	
	INS1791	National	
	FD1771	Western	
	FD1781	Western	
	FD1781-01	Western	
	FD1791	Western	140
Asynchronous/Synchronous Transmitter/Receiver (ASTRO) (See also Interface-Serial Transmitters-Receivers)			
	INS1671	National	
	COM1671	SMC	
	UC1671	Western	
	UC1971	Western	

1650

Microcomputer			
	PIC1650	GI	
	PIC1645	GI	150
	PIC1655	GI	
	PIC1670	GI	
Microcomputer Development Device			
	PIC1664	GI	

1800

CPU			
	HCMP1802	†Hughes	
	HCMP1802C	†Hughes	
	CDP1802	†RCA	
	CDP1802C	†RCA	
	CDP1804	†RCA	160
	CDP1804C	†RCA	
	SCP1802	†SSS	

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Values

MICROPROCESSOR–System Components (Cont'd)

Function	Device	Source	Line
1800		**(Cont'd.)**	
CPU		(Cont'd.)	
	SCP1802L	†SSS	
8-Bit Input/Output Port			
	HCMP1852	†Hughes	
	CDP1852	†RCA	
	SCP1852	†SSS	
4-Bit Buffer/Separator (for memory interface)			
	HCMP1856	†Hughes	
	CDP1856	†RCA	10
	SCP1856	†SSS	
Programmable I/O Interface			
	CDP1851	†RCA	
Multiply-Divide Circuit			
	CDP1855	†RCA	
Color Generator			
	CDP1862	†RCA	
Programmable Tone Generator			
	CDP1863	†RCA	
TV Interface (PAL)			20
	CDP1864	†RCA	
Latch/Decoder Memory Interface			
	CDP1866	†RCA	
	CDP1867	†RCA	
	CDP1868	†RCA	
4-Bit Bus Buffer/Separator (for I/O interface)			
	HCMP1857	†Hughes	
	CDP1857	†RCA	
	SCP1857	†SSS	
N-Bit Decoder (for I/O interface)			30
	HCMP1853	†Hughes	
	CDP1853	†RCA	
	SCP1853	†SSS	
4-Bit Latch with 1 of 4 Decoder			
	HCMP1858	†Hughes	
	CDP1858	†RCA	
	SCP1858	†SSS	
4-Bit Latch with dual 1 of 4 Decoders			
	HCMP1859	†Hughes	
	CDP1859	†RCA	40
	SCP1859	†SSS	
UART			
	HCMP1854	†Hughes	
	CDP1854	RCA	
	CDP1854A	†RCA	
	SCP1854	†SSS	
Video Display Controller			
	HCMP1861	†Hughes	
	CDP1861	†RCA	
RAM (32x8) (See also Memory-RAM's)			50
	HCMP1824	†Hughes	
	CDP1824	†RCA	
	SCP1824	†SSS	
RAM (128x8) (See also Memory-RAM's)			
	CDP1823	RCA	
RAM (256x4) (See also Memory-RAM's)			
	HCMP1822	†Hughes	
	CDP1822	RCA	
	SCP1822	†SSS	
RAM (1024x1) (See also Memory-RAM's)			60
	CDP1821	RCA	
RAM (1024x8) (See also Memory-RAMs)			
	CDP1825	RCA	

Function	Device	Source	Line
1800		**(Cont'd.)**	
ROM (512x8) (See also Memory-ROM's)			
	HCMP1831	†Hughes	
	HCMP1832	†Hughes	
	CDP1831	†RCA	
	CDP1832	†RCA	
	SCP1831	†SSS	
	SCP1832	†SSS	70
ROM (1024x8) (See also Memory-ROM's)			
	HCMP1833	†Hughes	
	HCMP1834	†Hughes	
	CDP1833	†RCA	
	CDP1834	†RCA	
	SCP1833	†SSS	
	SCP1834	†SSS	
ROM (2048x8) (See also memory-ROMs)			
	HCMP1835	†Hughes	
2000			
Microcomputer			80
	S2000	**AMI (1765)**	
	S2000A	**AMI (1765)**	
	S2150	AMI	
	S2150A	AMI	
	S2250	AMI	
	S2250A	AMI	
Development System			
	MDC	**AMI (1853)**	
2650			
Microprocessor			
	INS2650A	National	90
	INS2650A-1	National	
	2650A	**Signetics (2302)**	
	2650A-1	**Signetics (2302)**	
	2650B	**Signetics (2302)**	
	2650B-1	**Signetics (2302)**	
Hex Buffers/Inverters (See also Digital-TTL-Buffers/Inverters 8T95, 8T96, 8T97, 8T98)			
	MC8T95	Motorola	
	MC8T96	Motorola	
	MC8T97	Motorola	100
	MC8T98	Motorola	
	N8T95	**Signetics (2295)**	
	S8T95	**†Signetics (2295)**	
	N8T96	**Signetics (2295)**	
	S8T96	**†Signetics (2295)**	
	N8T97	**Signetics (2295)**	
	S8T97	**†Signetics (2295)**	
	N8T98	**Signetics (2295)**	
	S8T98	**†Signetics (2295)**	
Bidirectional Port, Latched			110
	N8T31	**Signetics (2290)**	
Programmable Communication Interface			
	INS2651	National	
	2651	**Signetics (2304)**	
Multi-Protocol Communications Circuit (includes SDLC, BiSync)			
	INS2652	National	
	2652	**Signetics (2306)**	
	2652-1	**Signetics (2306)**	
Programmable Peripheral Interface			120
	INS2655	National	
	2655	**Signetics (2308)**	
System Memory Interface (RAM, ROM, I/O)			
	INS2656	National	
		(Continued)	

Function	Device	Source	Line
2650		**(Cont'd.)**	
System Memory Interface (RAM, ROM, I/O)		(Cont'd.)	
	2656	Signetics	
Quad Transceivers (See also Interface-Line Transceivers)			
	N8T26	AMD	
	MC8T26A	Motorola	130
	MC8T28	Motorola	
	DS8T26A	National	
	DS8T28	National	
	N8T26	Signetics	
	N8T28	Signetics	
Development System			
	TWIN	**Signetics (2315)**	
2900			
Microprocessor, 4-Bit Slice			
	AM2901C	AMD	
	AM2901M	†AMD	140
	AM2901AC	AMD	
	AM2901AM	†AMD	
	AM2903C	AMD	
	AM2903M	†AMD	
	F2901AC	**Fairchild (1893)**	
	F2901AM	**†Fairchild (1893)**	
	9409	**Fairchild (1893)**	
	F2903C	Fairchild	
	F2903M	†Fairchild	
	9413	Fairchild	150
	2901AC	MMI	
	2901AM	†MMI	
	MC2901C	Motorola	
	MC2901M	†Motorola	
	MC2901AC	Motorola	
	MC2901AM	†Motorola	
	MC2903C	Motorola	
	MC2903M	†Motorola	
	IDM2901AC	**National (286)**	
	IDM2901AM	**†National (286)**	160
	IDM2900AC-1	National	
	IDM2900AM-1	†National	
	μPB2901A	NEC Micro	
	AM2901C	Raytheon	
	AM2901M	†Raytheon	
	AM2901AC	Raytheon	
	AM2901AM	†Raytheon	
	N2901A	**Signetics (2279)**	
	N2901-1	Signetics	
Look-Ahead Carry Generator			170
	AM2902C	AMD	
	AM2902M	†AMD	
	MC2902C	Motorola	
	MC2902M	†Motorola	
	IDM2902C	National	
	IDM2902M	†National	
	μPB2902A	NEC Micro	
	AM2902C	Raytheon	
	AM2902M	†Raytheon	
Microprogram Controller			180
	AM2910C	AMD	
	AM2910M	†AMD	
	F2910C	Fairchild	
	F2910M	†Fairchild	
	9420	Fairchild	
	MC2910C	Motorola	
	MC2910M	†Motorola	

† Military Temperature Range (−55° to 125°C)

* Typical Values

Bold face indicates additional data is provided on the page noted.

MICROPROCESSOR–System Components (Cont'd)

Function	Device	Source	Line
2900 (Cont'd.)			
Microprogram Sequencer			
	AM2909C	AMD	
	AM2909M	† AMD	
	AM2911C	AMD	
	AM2911M	† AMD	
	F2909C	Fairchild	
	F2909M	† Fairchild	
	F2911C	Fairchild	
	F2911M	† Fairchild	
	9419	Fairchild	
	9421	Fairchild	10
	2909C	MMI	
	2909M	† MMI	
	2911C	MMI	
	2911M	† MMI	
	MC2909C	Motorola	
	MC2909M	† Motorola	
	MC2911C	Motorola	
	MC2911M	† Motorola	
	IDM2909AC	National	
	IDM2909AM	† National	20
	IDM2911AC	National	
	IDM2911AM	† National	
	μPB2909A	NEC Micro	
	μPB2911A	NEC Micro	
	AM2909C	Raytheon	
	AM2909M	† Raytheon	
	AM2911C	Raytheon	
	AM2911M	† Raytheon	
Quad D Flip-Flop with Two Output Ports			
	AM2919C	AMD	30
	AM2919M	† AMD	
	2919C	MMI	
	2919M	† MMI	
Clock Generator and Driver			
	AM25LS2525C	AMD	
	AM25LS2525M	† AMD	
	AM2925C	AMD	
	AM2925M	† AMD	
Control Store Sequencer			
	N8X02	**Signetics (2280)**	40
DMA Address Generator			
	AM2940C	AMD	
	AM2940M	† AMD	
DMA Address Generator/Programmable Timer/Counter			
	AM2942C	AMD	
	AM2942M	† AMD	
Status and Shift Control Unit			
	AM2904C	AMD	
	AM2904M	† AMD	50
16-Way Branch Control Unit (use with 2909)			
	AM29803AC	AMD	
	AM29803AM	† AMD	
	IDM29803C	National	
	IDM29803M	† National	
One-of-Eight Decoder, with Polarity Control, Three-State			
	AM2921C	AMD	
	AM2921M	† AMD	
Next Address Control Unit (use with 2911)			60
	AM29811AC	AMD	
	AM29811AM	† AMD	
	IDM29811C	National	
	IDM29811M	† National	

Function	Device	Source	Line
2900 (Cont'd.)			
8-Bit Parallel I/O Port			
	AM2950C	AMD	
	AM2950M	† AMD	
	AM2951C	AMD	
	AM2951M	† AMD	
Priority Interrupt Encoder, Vectored			70
	AM2914C	AMD	
	AM2914M	† AMD	
	F2914C	Fairchild	
	F2914M	† Fairchild	
	9424	Fairchild	
Priority Interrupt Expander (for 2914)			
	AM2913C	AMD	
	AM2913M	† AMD	
Priority Encoder			
	IDM29902C	National	80
	IDM29902M	† National	
Program Control Unit (performs machine level addressing functions)			
	AM2930C	AMD	
	AM2930M	† AMD	
Programmable Multiplexer, 10-inputs, four 10x8 field programmable arrays, four 8:1 addressable multiplexers, four outputs			
	29693C	Raytheon	
	29693M	† Raytheon	90
Bus Transceivers (See also Interface-Line Transceivers)			
	AM2905C	AMD	
	AM2905M	† AMD	
	AM2906C	AMD	
	AM2906M	† AMD	
	AM2907C	AMD	
	AM2907M	† AMD	
	AM2915AC	AMD	
	AM2915AM	† AMD	100
	AM2916AC	AMD	
	AM2916AM	† AMD	
	AM2917AC	AMD	
	AM2917AM	† AMD	
	F2905C	Fairchild	
	F2905M	† Fairchild	
	F2906C	Fairchild	
	F2906M	† Fairchild	
	F2907C	Fairchild	
	F2907M	† Fairchild	110
	F2915AC	Fairchild	
	F2915AM	† Fairchild	
	F2916AC	Fairchild	
	F2916AM	† Fairchild	
	F2917AC	Fairchild	
	F2917AM	† Fairchild	
	9415	Fairchild	
	9416	Fairchild	
	9417	Fairchild	
	9425	Fairchild	120
	9426	Fairchild	
	9427	Fairchild	
	2905C	MMI	
	2905M	† MMI	
	2906C	MMI	
	2906M	† MMI	
	2907C	MMI	
	2907M	† MMI	
	2915AC	MMI	
	2915AM	† MMI	130
	2916AC	MMI	
	2916AM	† MMI	

(Continued)

Function	Device	Source	Line
2900 (Cont'd.)			
Bus Transceivers (See also Interface-Line Transceivers) (Cont'd.)			
	2917AC	MMI	
	2917AM	† MMI	
	MC2905C	Motorola	
	MC2905M	† Motorola	
	MC2906C	Motorola	
	MC2906M	† Motorola	140
	MC2907C	Motorola	
	MC2907M	† Motorola	
	MC2915AC	Motorola	
	MC2915AM	† Motorola	
	MC2916AC	Motorola	
	MC2916AM	† Motorola	
	MC2917AC	Motorola	
	MC2917AM	† Motorola	
	μPB2905A	NEC Micro	
	μPB2906A	NEC Micro	150
	μPB2907A	NEC Micro	
	μPB2915A	NEC Micro	
	μPB2916A	NEC Micro	
	μPB2917A	NEC Micro	
	AM2905C	Raytheon	
	AM2905M	† Raytheon	
	AM2906C	Raytheon	
	AM2906M	† Raytheon	
	AM2907C	Raytheon	
	AM2907M	† Raytheon	160
	AM2915AC	Raytheon	
	AM2915AM	† Raytheon	
	AM2916AC	Raytheon	
	AM2916AM	† Raytheon	
	AM2917AC	Raytheon	
	AM2917AM	† Raytheon	
8-Input Multiplexer, with control storage			
	AM2922C	AMD	
	AM2922M	AMD	
Quad D Register with both Standard and Three-State Outputs (See also Digital-TTL-Flip-Flops)			170
	AM2918C	AMD	
	AM2918M	† AMD	
	AM29LS18C	AMD	
	AM29LS18M	† AMD	
	2918C	MMI	
	2918M	† MMI	
	29LS18C	MMI	
	29LS18M	† MMI	
	MC2918C	Motorola	180
	MC2918M	† Motorola	
	μPB2918A	NEC Micro	
	AM2918C	Raytheon	
	AM2918M	† Raytheon	
Quad-Gated Flip-Flop			
	IDM29908C	National	
	IDM29908M	† National	
Octal D-type Flip-Flop, three state			
	IDM29901C	National	
	IDM29901M	† National	190
Octal D-Type Flip-Flop, Clear and Clock enable, Three-State			
	AM2920C	AMD	
	AM2920M	† AMD	
PROM (32x8) (See also Memory-PROM's)			
	AM29750AC	AMD	
	AM29750AM	† AMD	
	AM29751AC	AMD	
	AM29751AM	† AMD	
	IDM29750AC	National	200

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Values

MICROPROCESSOR–System Components (Cont'd)

Function	Device	Source	Line
2900 (Cont'd.)			
PROM (32x8) (See also Memory-PROM's) (Cont'd.)			
	IDM29750AM	† National	
	IDM29751AC	National	
	IDM29751AM	† National	
PROM(256x4) (See also Memory-PROMs)			
	AM29760AC	AMD	
	AM29760AM	† AMD	
	AM29761AC	AMD	
	AM29761AM	† AMD	
	IDM29760C	National	10
	IDM29760M	† National	
	IDM29761C	National	
	IDM29761M	† National	
RAM (16x4) Two output ports			
	AM29704C	AMD	
	AM29704M	† AMD	
	AM29705C	AMD	
	AM29705M	† AMD	
	IDM29704AC	National	
	IDM29704AM	† National	20
	IDM29705AC	National	
	IDM29705AM	† National	
RAM (16x4) (See also Memory-RAM's)			
	AM29700C	AMD	
	AM29700M	† AMD	
	AM29701C	AMD	
	AM29701M	† AMD	
	AM29702C	AMD	
	AM29702M	† AMD	
	AM29703C	AMD	30
	AM29703M	† AMD	
	IDM29702C	National	
	IDM29702M	† National	
	IDM29703C	National	
	IDM29703M	† National	
	IDM29903C	National	
RAM (256x1) (See also Memory-RAM's)			
	AM29720C	AMD	
	AM29720M	† AMD	
	AM29721C	AMD	40
	AM29721M	† AMD	
ROM (1024x8) (See also Memory-ROM's)			
	AM29882C	AMD	
	AM29883C	AMD	
3000			
Central Processing Element, 2-Bit slice			
	3002	Intel	
	M3002	† Intel	
	N3002	Signetics	
	S3002	† Signetics	
Microprogram Control Unit			50
	3001	Intel	
	M3001	† Intel	
	N3001	Signetics	
	S3001	† Signetics	
Parallel Bidirectional Bus Driver			
	3216	Intel	
	M3216	† Intel	
	3226	Intel	
	M3226	† Intel	
Interrupt Control Unit			60
	3214	Intel	
	M3214	† Intel	

Function	Device	Source	Line
3000 (Cont'd.)			
Look-Ahead Carry Generator			
	3003	Intel	
	M3003	† Intel	
Multimode Latch Buffer			
	3212	Intel	
	M3212	† Intel	
Development System			
	Intellec MDS	**Intel (1950)**	70
4004/4040			
CPU			
	HD35404	Hitachi	
	4004	Intel	
	4040	Intel	
	INS4004	National	
Clock Generator			
	4201	Intel	
	INS4201	National	
Programmable General Purpose I/O			
	4265	Intel	80
Programmable Keyboard/Display Device			
	4269	Intel	
Standard Memory and I/O Interface			
	4289	Intel	
	INS4008	National	
	INS4009	National	
10-Bit Shift Register/Output Expander			
	HD35403	Hitachi	
	4003	Intel	
	INS4003	National	90
Erasable PROM (256x8) (See also Memory-PROM's, 1702A)			
	4702	AMD	
	4702A	Intel	
	INS4702	National	
320-Bit RAM and 4-Bit Output Port			
	HD35402	Hitachi	
	4002	Intel	
	INS4002	National	
RAM (256x4) (See also Memory-RAM's, 2101 series)			100
	4101	Intel	
ROM (256x8) and 4-Bit I/O Port			
	HN35600	Hitachi	
	4001	Intel	
	INS4001	National	
ROM (1024x8) and I/O Ports			
	HN35800	Hitachi	
	4308	Intel	
ROM (2048x8) (See also Memory-ROM's, 2316A)			
	4316A	Intel	110
54/74LS481, 54/74S481			
4-Bit Microprocessor Slice			
	SN54LS481	† TI	
	SN74LS481	TI	
	SN74S481	TI	
Control Element (for next address generators)			
	SN54S482	† TI	
	SN74S482	TI	
Field Programmable Logic Array			
	SN54S330	† TI	
	SN74S330	TI	120

(Continued)

Function	Device	Source	Line
54/74LS481, 54/74S481 (Cont'd.)			
Field Programmable Logic Array (Cont'd.)			
	SN54S331	† TI	
	SN74S331	TI	
FIFO (See also Memory-FIFO's)			
	SN74S225	TI	
Erasable PROM (512x8) (See also Memory-PROM's)			
	SN54S472	**† TI (1708)**	
	SN74S472	**TI (1708)**	
RAM (256x4) (See also Memory-RAM's)			
	SN54S208	† TI	130
	SN74S208	TI	
5781/82			
Microprocessor			
	MM5782	National	
Control ROM (2048x8)			
	MM5781	National	
ROM (Calculator ROM)			
	MM57135	National	
	MM57136	National	
Shift Register Memory (1024-Bit)			
	MM57126	National	140
RAM Interface			
	MM5785	National	
5799			
Microprocessor			
	MM5799	National	
	MM57109	National	
	MM57140	National	
Printer Interface			
	MM5788	National	
Oscillator, Decoder, Driver			
	DS8664	National	150
RAM Interface			
	MM5785	National	
Shift Register Memory (1024-Bit)			
	MM57126	National	
6100			
CPU, 12-bit			
	HM6100	**† Harris (1918,1923)**	
	HM6100A	**Harris (1918)**	
	HM6100C	**† Harris (1918)**	
	IM6100A	Intersil	160
	IM6100C	Intersil	
Bidirectional Bus Driver			
	HD6432-2	**† Harris (737)**	
	HD6432-9	**Harris (737)**	
	HD6432A-2	**† Harris (737)**	
	HD6432A-9	**Harris (737)**	
Bus Driver; Latching, Three-State			
	HD6431-2	**† Harris (733)**	
	HD6431-9	**Harris (733)**	
	HD6431A-2	**† Harris (733)**	
	HD6431A-9	**Harris (733)**	170
Bus Separator/Driver(Octal organized as 4 pairs of bus separators)			
	HD6433-2	**† Harris (741)**	

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Values

Bold face indicates additional data is provided on the page noted.

MICROPROCESSOR–System Components (Cont'd)

Function	Device	Source		Line
6100 (Cont'd.)				
Bus Separator/Driver(Octal organized as 4 pairs of bus separators) (Cont'd.)				
	HD6433-9	**Harris**	**(741)**	
	HD6433A-2	**† Harris**	**(741)**	
	HD6433A-9	**Harris**	**(741)**	
One-of-Eight Decoder/Driver, Latched				
	HD6440-2	**† Harris**	**(745)**	
	HD6440-9	**Harris**	**(745)**	
	HD6440A-2	**† Harris**	**(745)**	
	HD6440A-9	**Harris**	**(745)**	10
Hex Buffer/Driver, Three-State				
	HD6495-2	† Harris		
	HD6495-9	Harris		
	HD6495A-2	**† Harris**	**(749)**	
	HD6495A-9	**Harris**	**(749)**	
	IM6100M	† Intersil		
Peripheral Interface Element				
	HD6101-2	† Harris		
	HD6101-5	Harris		
	HD6101A-2	† Harris		20
	HD6101A-9	Harris		
	HD6101C-9	Harris		
	IM6101A	Intersil		
	IM6101AM	† Intersil		
Universal Asynchronous Receiver-Transmitter (UART) (See also Interface-Serial Transmitters-Receivers)				
	HD6402-2	**† Harris**	**(1930)**	
	HD6402-9	**Harris**	**(1930)**	
	HD6402A-2	**† Harris**	**(1930)**	
	HD6402A-9	**Harris**	**(1930)**	30
	HD6402C-9	**Harris**	**(1930)**	
	HD6403-2	† Harris		
	HD6403-9	Harris		
	IM6402	Intersil		
	IM6402M	† Intersil		
	IM6403	Intersil		
	IM6403M	† Intersil		
Memory Extension, DMA, Interval Timer, Controller (MEDIC)				
	IM6102A	Intersil		40
	IM6102AM	† Intersil		
20-Bit I/O Port				
	IM6103	Intersil		
	IM6103M	† Intersil		
Programmable Bit Rate Generator (See also Digital-CMOS, Bit Rate Generator)				
	HD6405-2	**† Harris**	**(1926)**	
	HD6405-9	**Harris**	**(1926)**	
	HD6405A-2	**† Harris**	**(1926)**	
	HD6405A-9	**Harris**	**(1926)**	50
6500				
Note: The 6500 series is bus compatable with 6800 series devices				
CPU				
	MCS6502	MOS		
	MCS6503	MOS		
	MCS6504	MOS		
	MCS6505	MOS		
	MCS6506	MOS		
	MCS6512	MOS		
	MCS6514	MOS		60
	MCS6515	MOS		
	R6500/1	Rockwell		
	R6502	Rockwell		
	R6503	Rockwell		
			(Continued)	

Function	Device	Source		Line
6500 (Cont'd.)				
CPU (Cont'd.)				
	R6504	Rockwell		
	R6505	Rockwell		
	R6506	Rockwell		
	R6507	Rockwell		
	R6512	Rockwell		70
	R6513	Rockwell		
	R6514	Rockwell		
	R6515	Rockwell		
	SY6500	Synertek		
	SY6500/1	Synertek		
	SY6503	Synertek		
	SY6504	Synertek		
	SY6505	Synertek		
	SY6506	Synertek		
	SY6512	Synertek		80
	SY6513	Synertek		
	SY6514	Synertek		
	SY6515	Synertek		
RAM, ROM, I/O and Interval Timer				
	MCS6530	MOS		
	MCS6532	MOS		
	R6530	Rockwell		
	R6532	Rockwell		
	SY6530	Synertek		
RAM(128x8), I/O, and Timer				90
	R6532	Rockwell		
	SY6532	Synertek		
Analog Input, Multiplexer, A/D Converter				
	MP21	**Burr-Brown**	**(659)**	
Asynchronous Communications Interface Adapter				
	R6551	Rockwell		
	SY6551	Synertek		
CRT Controller				
	R6545	Rockwell		
	SY6545	Synertek		100
Mini-Floppy Disc Controller				
	R6542	Rockwell		
RAM(128x8), ROM, I/O, and Counter/Timer				
	R6531	Rockwell		
	SY6531	Synertek		
Peripheral Interface Adapter				
	MCS6520	MOS		
	MCS6522	MOS		
	R6520	Rockwell		
	R6522	Rockwell		110
	SY6520	Synertek		
	SY6522	Synertek		
ROM (2048x8) (See also Memory-ROM's)				
	R2316A	Rockwell		
	R2316B	Rockwell		
	SY6540	Synertek		
	SY6541	Synertek		
6800				
Note: The 6800 series is bus compatible with 6500 series devices.				
CPU				120
	S6800	**AMI**	**(1776,1780)**	
	S6800M	**† AMI**	**(1780)**	
	S68A00	**AMI**	**(1780)**	
	S68B00	**AMI**	**(1780)**	
			(Continued)	

Function	Device	Source		Line
6800 (Cont'd.)				
CPU (Cont'd.)				
	F6800	**Fairchild**	**(1886,1888)**	
	F68A00	**Fairchild**	**(1887)**	
	F68B00	**Fairchild**	**(1887)**	130
	F6809	**Fairchild**	**(1887)**	
	F68A09	**Fairchild**	**(1887)**	
	F68B09	**Fairchild**	**(1887)**	
	MBL6800E	Fujitsu		
	MBL6800H	Fujitsu		
	MBL6800N	Fujitsu		
	HD46800	Hitachi		
	HD468A00	Hitachi		
	MC6800	**Motorola**	**(2002)**	
	MC6800M	**† Motorola**	**(2002)**	140
	MC68A00	**Motorola**	**(2002)**	
	MC68B00	**Motorola**	**(2002)**	
	MC6809	**Motorola**	**(2005)**	
	MC68A09	**Motorola**	**(2005)**	
	MC68B09	**Motorola**	**(2005)**	
CPU (internal clock, 128x8 RAM)				
	S6802	**AMI**	**(1785)**	
	F6802	**Fairchild**	**(1887,1888)**	
	F68A02	**Fairchild**	**(1887)**	150
	F68B02	**Fairchild**	**(1887)**	
	MBL6802N	Fujitsu		
	MBL6802E	Fujitsu		
	MBL6802H	Fujitsu		
	HD46802	Hitachi		
	MC6802	**Motorola**	**(1995)**	
CPU(CMOS,internal clock, 128x8 RAM)				
	MD46802A	† Mitel		
	MD46802AE	Mitel		
CPU(External Clock)				160
	S6809	**AMI**	**(1789)**	
	F6809E	**Fairchild**	**(1887)**	
	F68A09E	**Fairchild**	**(1887)**	
	F68B09E	**Fairchild**	**(1887)**	
	MC6809E	**Motorola**	**(2005)**	
	MC68A09E	**Motorola**	**(2005)**	
	MC68B09E	**Motorola**	**(2005)**	
Microcomputer; Clock, Timer, RAM, ROM, I/O				
	S6801	**AMI**	**(1784)**	
	F6801	**Fairchild**	**(1887)**	170
	MC6801	Motorola		
Microcomputer (External clock); RAM, ROM, Timer, I/O				
	F6801E	**Fairchild**	**(1887)**	
	MC6801E	Motorola		
Microcomputer (External ROM); RAM, Clock, Timer, I/O				
	F6803	Fairchild		
	MC6803	**Motorola**	**(1993)**	
Microcomputer (EPROM); RAM, Clock, Timer, I/O				180
	MC68701	Motorola		
Priority Interrupt Controller				
	MB472	Fujitsu		
	MC6828	Motorola		
	MC8507	Motorola		
Analog Input, Multiplexer, A/D Converter				
	MP21	**Burr-Brown**	**(659)**	
Hex Buffers/Inverters (See also Digital-TTL-Buffers/Inverters 8T95, 8T96, 8T97, 8T98)				
	MB485	Fujitsu		190
			(Continued)	

† Military Temperature Range (−55° to 125°C)

* Typical Values

MICROPROCESSOR–System Components (Cont'd)

6800 (Cont'd.)

Hex Buffers/Inverters (See also Digital-TTL-Buffers/Inverters 8T95, 8T96, 8T97, 8T98) (Cont'd.)

Device	Source
MB486	Fujitsu
MB487	Fujitsu
MB488	Fujitsu
MC6885	Motorola
MC6886	Motorola
MC6887	Motorola
MC6888	Motorola

Triple Bidirectional Bus Switch (also MC3449)

Device	Source
MC6881	Motorola

Clock, 2 phase (MC6870/71 from Motorola Component Products Dept., Franklin Park, IL)

Device	Source
MB8867	Fujitsu
HD26501	Hitachi
MC6870	Motorola
MC6871	Motorola
MC6875	Motorola

Clock Buffer

Device	Source
MPQ6842	Motorola

CRT Controller

Device	Source	
F6845	**Fairchild**	**(1887)**
HD46502	Hitachi	
HD46505	Hitachi	
MC6845	**Motorola**	**(1983)**
MC6845M	**† Motorola**	**(1983)**
MC68A45	**Motorola**	**(1983)**
MC68B45	**Motorola**	**(1983)**
SY6545	Synertek	

Digital Modulator (for differential phase shift keying system)

Device	Source	
F6862	Fairchild	
MC6862	**Motorola**	**(1966)**

DMA Controller

Device	Source	
F6844	**Fairchild**	**(1887)**
HD46504	Hitachi	
MC6844	**Motorola**	**(1985)**
MC6844M	**† Motorola**	**(1985)**
MC68A44	**Motorola**	**(1985)**
MC68B44	**Motorola**	**(1985)**

Floppy Disc Controller

Device	Source	
F6843	**Fairchild**	**(1887)**
HD46503	Hitachi	
MC6843	**Motorola**	**(1987)**

Modem

Device	Source	
F6860	Fairchild	
F6862	Fairchild	
MC6860	Motorola	
MC6860L	**Motorola**	**(1968)**
MC6862	**Motorola**	**(1966)**

Programmable Timer

Device	Source	
S6840	**AMI**	**(1813)**
F6840	**Fairchild**	**(1887,1890)**
F68A40	**Fairchild**	**(1887)**
F68B40	**Fairchild**	**(1887)**
MBL6840	Fujitsu	
HD46840	Hitachi	
MC6840	**Motorola**	**(1989)**
MC6840M	**† Motorola**	**(1989)**
MC68A40	**Motorola**	**(1989)**
MC68B40	**Motorola**	**(1989)**

Synchronous Serial Data Adapter (SSDA)

Device	Source	
S6852	**AMI**	**(1822)**
F6852	**Fairchild**	**(1887,1891)**

(Continued)

6800 (Cont'd.)

Synchronous Serial Data Adapter (SSDA) (Cont'd.)

Device	Source	
F68A52	**Fairchild**	**(1887)**
F68B52	**Fairchild**	**(1887)**
MBL6852E	Fujitsu	
MBL6852H	Fujitsu	
MBL6852N	Fujitsu	
HD46852	Hitachi	
MC6852	**Motorola**	**(1973)**
MC6852M	**† Motorola**	**(1973)**
MC68A52	**Motorola**	**(1973)**
MC68B52	**Motorola**	**(1973)**

Synchronous Receiver/Transmitter (USRT, See also Interface-Serial Transmitters-Receivers)

Device	Source	
S2350	**AMI**	**(634)**

Asynchronous Communications Interface Adapter (ACIA)

Device	Source	
S6850	**AMI**	**(1818)**
S6850M	**† AMI**	**(1818)**
S68A50	**AMI**	**(1818)**
S68B50	**AMI**	**(1818)**
F6850	**Fairchild**	**(1887,1891)**
F68A50	**Fairchild**	**(1887)**
F68B50	**Fairchild**	**(1887)**
MBL6850E	Fujitsu	
MBL6850H	Fujitsu	
MBL6850N	Fujitsu	
HD46850	Hitachi	
HD468A50	Hitachi	
MC6850	**Motorola**	**(1977)**
MC6850M	**† Motorola**	**(1977)**
MC68A50	**Motorola**	**(1977)**
MC68B50	**Motorola**	**(1977)**
SY6551	Synertek	

Advanced Data Link Controller

Device	Source	
S6854	**AMI**	**(1826)**
S68A54	**AMI**	**(1826)**
F6854	**Fairchild**	**(1887)**
F68A54	**Fairchild**	**(1887)**
F68B54	**Fairchild**	**(1887)**
F6856	**Fairchild**	**(1887,1892)**
MBL6854	Fujitsu	
HD46854	Hitachi	
MC6854	**Motorola**	**(1971)**
MC68A54	**Motorola**	**(1971)**
MC68B54	**Motorola**	**(1971)**

General Purpose Interface Adapter (IEEE 488 bus)

Device	Source	
S68488	**AMI**	**(1834)**
F68488	**Fairchild**	**(1887,1890)**
MBL68488	Fujitsu	
HD68488	Hitachi	
MC68488	**Motorola**	**(1975)**
MC68488M	**† Motorola**	**(1975)**
MC68A488	**Motorola**	**(1975)**
MC68B488	**Motorola**	**(1975)**
HEF4738	Signetics	

Peripheral Interface Adapter, (PIA)

Device	Source	
S6820	**AMI**	**(1802)**
S6821	**AMI**	**(1798,1802)**
S6821M	**† AMI**	**(1798)**
S68A21	**AMI**	**(1798)**
S68B21	**AMI**	**(1798)**
F6820	**Fairchild**	**(1887)**

(Continued)

6800 (Cont'd.)

Peripheral Interface Adapter, (PIA) (Cont'd.)

Device	Source	
F6821	**Fairchild**	**(1887,1889)**
F68A21	**Fairchild**	**(1887)**
F68B21	**Fairchild**	**(1887)**
MBL6820E	Fujitsu	
MBL6820H	Fujitsu	
MBL6820N	Fujitsu	
MBL6821E	Fujitsu	
MBL6821H	Fujitsu	
MBL6821N	Fujitsu	
HD46821	Hitachi	
HD468A21	Hitachi	
MC6820	Motorola	
MC6821	**Motorola**	**(1991)**
MC6821M	**† Motorola**	**(1991)**
MC68A21	**Motorola**	**(1991)**
MC68B21	**Motorola**	**(1991)**

Bus Transceiver, (The 6880 is also called 8T26 and the 6889 the 8T28, See Interface-Transceivers)

Device	Source
MB424	Fujitsu
MC6880	Motorola
MC6889	Motorola

Erasable PROM (1024x8) See Memory-PROMs, 1024x8

Memory Controller, μP to 16K dynamic RAM(2 Device Set)

Device	Source
MC3480	Motorola
MC3482	Motorola

RAM (128x8) (See also Memory-RAM's)

Device	Source	
S6810	**AMI**	**(1790)**
S6810A	**AMI**	**(1790)**
S6810M	**† AMI**	**(1794)**
S68A10	**AMI**	**(1794)**
S68B10	**AMI**	**(1794)**
F6810	**Fairchild**	**(1887,1888)**
F68A10	**Fairchild**	**(1887)**
F68B10	**Fairchild**	**(1887)**
HM46810	Hitachi	
HM468A10	Hitachi	
MCM6810	Motorola	
MCM6810M	† Motorola	
MCM68A10	Motorola	
MCM68B10	Motorola	

ROM, I/O, Timer

Device	Source	
S6846	**AMI**	**(1817)**
F6846	**Fairchild**	**(1887,1890)**
MBL6846	Fujitsu	
HD46846	Hitachi	
MC6846	**Motorola**	**(1981)**
MC6846M	**† Motorola**	**(1981)**
MC68A46	**Motorola**	**(1981)**
MC68B46	**Motorola**	**(1981)**

ROM, I/O, Timer (CMOS)

Device	Source
MD46846A	† Mitel
MD46846AE	Mitel

ROM (1024x8) (See also Memory-ROM's)

Device	Source	
F6830	Fairchild	
F68308	**Fairchild**	**(1887,1889)**
F68A308	**Fairchild**	**(1887)**
F68B308	**Fairchild**	**(1887)**
HD46830	Hitachi	
MCM65308	Motorola	

(Continued)

† Military Temperature Range (–55° to 125°C)

* Typical Values

Bold face indicates additional data is provided on the page noted.

MICROPROCESSOR–System Components (Cont'd)

6800 (Cont'd.)

ROM (1024x8) (See also Memory-ROM's) (Cont'd.)

Device	Source	
MCM68A30A	**Motorola**	**(1530)**
MCM68B30A	Motorola	
MCM68A308	**Motorola**	**(1530)**
MCM68B308	Motorola	

ROM (2048x8) (See also Memory-ROM's)

Device	Source	
S6831	**AMI**	**(1215,1806)**
S6831A	**AMI**	**(1215,1806)**
S6831B	**AMI**	**(1215,1806)**
F68316	**Fairchild**	**(1887,1889)**
F68A316	**Fairchild**	**(1887)**
F68B316	**Fairchild**	**(1887)**
F68317	Fairchild	
MC6832	Motorola	
MCM68A316	Motorola	

ROM (4096x8) (See also Memory-ROMs)

Device	Source	
MCM68A332	Motorola	

Development System

Device	Source	
MDC	**AMI**	**(1853)**

8X300

Microprocessor

Device	Source	
N8X300	**Signetics**	**(1982)**
S8X300-1	**† Signetics**	**(2282)**
S8X300-2	**† Signetics**	**(2282)**

I/O Port, Synchronous, Field Programmable Address

Device	Source	
N8T32	**Signetics**	**(2291)**
S8T32	**† Signetics**	**(2291)**
N8T33	**Signetics**	**(2291)**
S8T33	**† Signetics**	**(2291)**

I/O Port, Asynchronous, Field Programmable Address

Device	Source	
N8T35	**Signetics**	**(2291)**
S8T35	**† Signetics**	**(2291)**
N8T36	**Signetics**	**(2291)**
S8T36	**† Signetics**	**(2291)**

I/O Port, Latched Bidirectional

Device	Source	
N8T31	**Signetics**	**(2290)**

Bus Expander, Addressable

Device	Source	
N8T39	**Signetics**	**(2292)**

Transparent Bus Expander

Device	Source	
N8T58	**Signetics**	**(2294)**

RAM, Static (256x8)

Device	Source	
N8X350	**Signetics**	**(1678)**

8000

Logic Processor

Device	Source
LP8000	GI

Clock Generator

Device	Source
LP1030	GI

Input/Output Buffer

Device	Source
LP1010	GI

Memory Interface

Device	Source
LP1000	GI

Program Memory (1024x8)

Device	Source
LP6000	GI

8008

CPU

Device	Source
8008	Intel

8-Bit I/O Port (See listing under 8080)

Device	Source
8212	Intel
μPB8212	**NEC Micro (2172)**

Bidirectional Bus Driver (See listing under 8080)

Device	Source
MB425	Fujitsu
MB426	Fujitsu
8216	Intel
8226	Intel
μPB8216	**NEC Micro (2184)**
μPB8226	**NEC Micro (2184)**

Analog input, MUX, A/D converter

Device	Source	
MP20	**Burr-Brown**	**(659)**

Programmable Interval Timer (See listing under 8080)

Device	Source
8253	Intel
μPD8253	**NEC Micro (2221)**

Programmable Peripheral Interface (See listing under 8080)

Device	Source
8255A	Intel
μPD8255	**NEC Micro (2229)**
μPD8255A-5	**NEC Micro (2229)**

Keyboard Display Controller (See listing under 8080)

Device	Source
8279	Intel

Priority Interrupt Control. (See listing under 8080)

Device	Source
8214	Intel
μPB8214	**NEC Micro (2178)**

Decoder, 1 of 8 (See listing under 8080)

Device	Source
8205	Intel

Programmable Communication Interface (See listing under 8080)

Device	Source
8251	AMD
8251	Intel
μPD8251	**NEC Micro (2204)**

8048

8-Bit Microcomputer (Mask Programmed ROM)

Device	Source	
8048	AMD	
MBL8048	Fujitsu	
MBL8049	Fujitsu	
8021	**Intel**	**(1936)**
8048	**Intel**	**(1934)**
8049	**Intel**	**(1935)**
μPD8021	**NEC Micro (2085)**	
μPD8048	**NEC Micro (2098)**	
μPD8049	**NEC Micro (2104)**	
8021	Signetics	
8048	**Signetics**	**(2310)**

8-Bit Microcomputer (Erasable PROM)

Device	Source	
μPD8741	**NEC Micro (2090)**	
8748	**Intel**	**(1934)**
8748-4	**Intel**	**(1934)**
μPD8748	**NEC Micro (2098)**	
8748	Signetics	

8-Bit Microcomputer (External ROM)

Device	Source	
8035	AMD	
8035	**Intel**	**(1934)**
8035-4	**Intel**	**(1934)**
8039	**Intel**	**(1935)**
8039-6	**Intel**	**(1935)**
μPD8035	**NEC Micro (2098)**	
μPD8039	**NEC Micro (2104)**	
8035	**Signetics**	**(2310)**

8048 (Cont'd.)

8-bit Microcomputer (Mask Programmed ROM, on-board A/D)

Device	Source	
8022	**Intel**	**(1937)**

PROM (Erasable), I/O

Device	Source	
8755A	**Intel**	**(1946)**
μPD8755A	**NEC Micro (2269)**	

RAM, I/O, Timer

Device	Source	
8155	AMD	
8155	**Intel**	**(1945)**
8155-2	**Intel**	**(1945)**
8156	**Intel**	**(1945)**
8156-2	**Intel**	**(1945)**
μPD8155	**NEC Micro (2164)**	
μPD8156	**NEC Micro (2164)**	

ROM, I/O

Device	Source	
8355	AMD	
8355	**Intel**	**(1946)**
8355-2	**Intel**	**(1946)**
μPD8355	**NEC Micro (2269)**	

Universal Peripheral Interface (Slave Microprocessor)

Device	Source	
8041	AMD	
8041	**Intel**	**(1939)**
8741	**Intel**	**(1939)**
μPD8041	**NEC Micro (2090)**	

I/O Expander for 8048 family

Device	Source	
8243	AMD	
8243	Intel	
μPD8243	**NEC Micro (2199)**	
8243	**Signetics**	**(2313)**

Analog Input, Multiplexer, A/D Converter

Device	Source	
MP21	**Burr-Brown**	**(659)**
MP22	**Burr-Brown**	**(659)**

Bidirectional Bus Driver. See 8216, 8226, etc. under 8080

Device	Source	
MB425	Fujitsu	
MB426	Fujitsu	
8216	Intel	
8226	Intel	
μPB8216	**NEC Micro (2184)**	
μPB8226	**NEC Micro (2184)**	

Programmable Communication Interface (USART) See 8251, etc. under 8080.

Device	Source	
8251	AMD	
8251	Intel	
μPD8251	**NEC Micro (2204)**	

Decoder, 1 of 8. See 8205, etc. under 8080.

Device	Source
8205	Intel

CRT Controller. See 8275, etc. under 8080.

Device	Source	
8275	**Intel**	**(1942)**

Floppy Disc Controller. See 8271, etc. under 8080.

Device	Source	
8271	**Intel**	**(1940)**
μPD372	NEC Micro	

Keyboard/Display Controller; See 8279, etc. under 8080.

8-Bit I/O Port. See 8212, etc. under 8080.

Device	Source	
8212	Intel	
μPB8212	**NEC Micro (2172)**	

Priority Interrupt Control. See 8214, etc. under 8080.

Device	Source	
8214	Intel	
μPB8214	**NEC Micro (2178)**	

Programmable Interrupt Controller. See 8259, etc. under 8080.

Device	Source	
8259	Intel	
8259-5	Intel	(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Values

MICROPROCESSOR–System Components (Cont'd)

8048 (Cont'd.)

Programmable Interrupt Controller. See 8259, etc. under 8080. (Cont'd.)

Device	Source
μPD8259	**NEC Micro (2244)**
μPD8259-5	**NEC Micro (2244)**

Programmable Interval Timer. See 8253, etc. under 8080.

Device	Source
8253	AMD
8253	Intel
μPD8253	**NEC Micro (2221)**

Programmable Peripheral Interface. See 8255, etc. under 8080.

Device	Source
8255A	AMD
8255A	Intel
μPD8255	**NEC Micro (2229)**
μPD8255A-5	**NEC Micro (2229)**

SDLC Protocol Controller. See 8273, etc. under 8080.

Device	Source
8273	**Intel (1941)**
μPD379	NEC Micro

Development System

Device	Source
Intellec MDS	**Intel (1950)**

8080

See also Z80

CPU

Device	Source
8080A	AMD
9080AC	AMD
9080AM	† AMD
8080A	Intel
8080A-1	Intel
8080A-2	Intel
M8080A	† Intel
M5L8080A	Mitsubishi
INS8080A	**National (238)**
INS8080A-1	**National (238)**
INS8080A-2	**National (238)**
μPD8080AF	**NEC Micro (2119)**
μPD8080AF-1	**NEC Micro (2119)**
μPD8080AF-2	**NEC Micro (2119)**
MSM3901	OKI
8080A	**Signetics (2312)**
TMS8080A	TI

Universal Peripheral Interface(Slave Microprocessor)

Device	Source
8041	AMD
8041	**Intel (1939)**
8741	**Intel (1939)**
μPD8041	**NEC Micro (2090)**
μPD8741	**NEC Micro (2090)**

I/O Expander for 8041/8741

Device	Source
8243	AMD
8243	Intel
8243	**Signetics (2313)**

Analog Input, 3¾ Digit DVM with multiplexed output

Device	Source
ADC3701	National
INS8294	National

Analog input, MUX, A/D converter

Device	Source
MP20	**Burr-Brown (659)**
MP22	**Burr-Brown (659)**
ADC0816	**National (1073,1074,1084)**
INS8292	National

Arithmetic Processing Unit

Device	Source
9511C	AMD
9511M	† AMD

8080 (Cont'd.)

Bus Driver (See also Digital-Misc., Bus Drivers; Interface-Line Drivers)

Device	Source
INS8202	National
INS8203	National

Bidirectional Bus Driver (See also Digital-Miscellaneous-Bus Drivers, Interface-Line Transceivers.)

Device	Source
3216	AMD
M3216	† AMD
3226	AMD
M3226	† AMD
8216	AMD
M8216	† AMD
8226	AMD
M8226	† AMD
MB425	Fujitsu
MB426	Fujitsu
8216	Intel
8226	Intel
M8216	† Intel
M5L8216	Mitsubishi
M5L8226	Mitsubishi
DP3216	National
DP3226	National
DP8216	National
DP8226	National
DP8304	National
DS8833	National
DS8835	National
INS8208	National
INS8216	National
INS8226	National
μPB8216	**NEC Micro (2184)**
μPB8226	**NEC Micro (2184)**

Clock Generator and Driver

Device	Source
8224C	AMD
8224M	† AMD
8224	Intel
M8224	† Intel
M5L8224	Mitsubishi
DP8224	National
INS8224	National
μPB8224	**NEC Micro (2188)**
SN54LS424	† TI
SN74LS424	TI

Asynchronous Communication Element

Device	Source
DP8250	**National (2016,297)**
INS8250	**National (2018)**
μPD369	NEC Micro
TR1983	Western

Programmable Communication Interface (USART) (See also Interface-Transmitters,Receivers)

Device	Source
9551C	AMD
9551M	† AMD
8251	AMD
8251	Intel
8251A	Intel
M8251	† Intel
INS1671	National
INS1971	National
INS8251	National
μPD8251	**NEC Micro (2204)**
μPD8251A	**NEC Micro (2204)**
2651	**Signetics (2304)**
8251	Signetics
TMS5501	TI

8080 (Cont'd.)

System Timing Controller

Device	Source
9513	AMD

Decoder, 1 of 8 (See also Digital-TTL-Decoders, 3222, 74LS138, etc.)

Device	Source
AM25LS138C	AMD
AM25LS138M	† AMD
8205	Intel
DM74LS138	National
INS82LS05	National
SN74LS138	TI

Display Controller

Device	Source
INS8247	National
INS8248	National

Programmable Direct Memory Access Controller

Device	Source
8257	AMD
9517C	AMD
9517M	† AMD
8257	Intel
8257-5	Intel
INS8257	National
μPD8257	**NEC Micro (2236)**

Cassette Controller

Device	Source
μPD371	NEC Micro

CRT Controller

Device	Source
8275	**Intel (1942)**
DP8350	**National (793,238,297)**
INS8277	National

Data-Encrytion Device (encrypts and decrypts data according to NBS standard)

Device	Source
8294	Intel

Dynamic RAM Controller

Device	Source
8202	**Intel (1938)**

Floppy Disc Controller

Device	Source
8271	**Intel (1940)**
INS1791	National
μPD372	NEC Micro

Keyboard Encoder (See also Interface-Keyboard Encoders)

Device	Source
INS8244	National
INS8245	National
INS8246	National

Keyboard Display Controller

Device	Source
8279	AMD
8279-5	AMD
8279	Intel
8279-5	Intel
M5L8279	Mitsubishi
M5L8279-5	Mitsubishi
μPD8279	**NEC Micro (2260)**
μPD8279-5	**NEC Micro (2260)**

General Interface Circuit (for DMA or interrupt exchanges)

Device	Source
μPC6001	SMC

GPIB Talker/Listener Interface

Device	Source
8291	**Intel (1943)**

8-Bit I/O Latch (see also Digital-CMOS and TTL, Latches)

Device	Source
INS82C06	National

8-Bit I/O Port

Device	Source
3212	AMD
M3212	† AMD
8212C	AMD
8212M	† AMD
MB471	Fujitsu

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Values

Bold face indicates additional data is provided on the page noted.

MICROPROCESSOR–System Components (Cont'd)

8080 (Cont'd.)

8-Bit I/O Port (Cont'd.)

Device	Source
8212	Intel
M8212	† Intel
M5L8212	Mitsubishi
DP8212	National
INS8212	National
μPB8212	**NEC Micro (2172)**
SN54S412	† TI
SN74S412	TI

8-Bit I/O Port, Bidirectional

Device	Source
DP8213	National

Multifunction I/O Controller, (asynchronous communications interface, I/O buffers, interrupt control, interval timers)

Device	Source
TMS5501	TI

Priority Interrupt Control

Device	Source
AM25LS2513C	AMD
AM2914C	AMD
AM2914M	† AMD
8214	Intel
M8214	† Intel
μPB8214	**NEC Micro (2178)**

Programmable Interrupt Controller

Device	Source
9519C	AMD
9519M	† AMD
8259	Intel
8259-5	Intel
INS8259	National
μPD8259	**NEC Micro (2244)**
μPD8259-5	**NEC Micro (2244)**

Programmable Interval Timer

Device	Source
8253	AMD
8253	Intel
INS8253	National
μPD8253	**NEC Micro (2221)**

Programmable Peripheral Interface

Device	Source
9555C	AMD
9555M	† AMD
8255A	Intel
M8255A	† Intel
M5L8255	Mitsubishi
INS8254	National
INS8255	National
μPD8255	**NEC Micro (2229)**
μPD8255A-5	**NEC Micro (2229)**
2655	**Signetics (2308)**
8255	Signetics

SDLC Protocol Controller

Device	Source
8273	**Intel (1941)**
INS1933	National
μPD379	NEC Micro
SD1933	Western

Multi-Protocol Communications Controller (SDLC, ADDCP, BiSync, DDCMP)

Device	Source
2652	**Signetics (2306)**
2652-1	**Signetics (2306)**

Advanced Protocol Controller (SDLC, ADCCP)

Device	Source
INS8283	National

Synchronous Receiver/Transmitter (BiSync, SDLC)

Device	Source
μPD379	NEC Micro

System Controller and Bus Driver

Device	Source
8228C	AMD
8228M	† AMD
8238C	AMD
8238M	† AMD

(Continued)

8080 (Cont'd.)

System Controller and Bus Driver (Cont'd.)

Device	Source
8228	Intel
M8228	† Intel
8238	Intel
M5L8228	Mitsubishi
DP8228	National
DP8238	National
INS8228	National
INS8238	National
μPB8228	**NEC Micro (2193)**
μPB8238	**NEC Micro (2193)**
SN74S428	TI
SN74S438	TI
TIM8228	TI
TIM8238	TI

RAM(128x8), ROM(2048x8), I/O

Device	Source
DP8356	National

RAM (128x8) with 16-Bit I/O

Device	Source
INS8154	National

Erasable PROM (256x8) (See also Memory-PROM's, 1702A series)

Device	Source
8702A	AMD
8702A	Intel
M5L1702A	Mitsubishi
MM1702AQ	National
μPD454	NEC Micro

Erasable PROM(512x8) (See also Memory-PROMs, 2704)

Device	Source
2704	AMD
S2704A	AMI

Erasable PROM (1024x8) (See memory-PROM's 2708)

RAM (256x4) (See also Memory-RAM's 2101, 2111 series)

Device	Source
8101	AMD
8111	AMD
8101A-4	Intel
8111A-4	Intel
INS74C920	National
MM8101A-4	National
MM8111A-4	National
μPD2101AL	**NEC Micro (1586)**
μPD2111	**NEC Micro (1595)**

RAM (1024x1) (See also Memory-RAM's 2101A series)

Device	Source
8102A-4	AMD
8102A-4	Intel
M8102A	† Intel
M58751	Mitsubishi
MM2102A	National
μPD2102AL	**NEC Micro (1591)**

RAM (4096x1) (See also Memory-RAM's 2107, 5280 series)

Device	Source
MB8107	Fujitsu
8107B-4	Intel
M58755	Mitsubishi
MM5270	National
μPD411	**NEC Micro (1547)**
TMS4060	TI

RAM: 16K and larger, See Memory—Static or Dynamic RAMs

ROM (256x8) (See also Memory-ROM's 1302)

Device	Source
8302	Intel
MM5213	National
DP8302	National

8080 (Cont'd.)

ROM (1024x8) (See also Memory-ROM's 2308)

Device	Source
9208	AMD
8308	Intel
M58730	Mitsubishi
μPD2308	NEC Micro

ROM (2048x8) (See also Memory-ROM's 2316A)

Device	Source
8316A	AMD
8316E	AMD
9216	AMD
8316A	Intel
M58731	Mitsubishi
MM2316A	National
MM8316A	National
MM8316E	National
μPD2316A	NEC Micro
μPD2316E	**NEC Micro (1633)**

ROM(4096x8) (See also Memory-ROMs)

Device	Source
MM8332	National
μPD2332	**NEC Micro (1637)**
TMS4732	TI

ROM(8192x8) (See also Memory-ROM's)

Device	Source
MM8364	National
MM8364E	National
μPD2364	**NEC Micro (1640)**

ROM, BASIC Interpreter

Device	Source
EA3280	EA
INS8298E	National

Floating Point Arithmetic

Device	Source
FP708	Novonics

Development System

Device	Source
Intellec MDS	**Intel (1950)**

8085A

Many devices for the 8080 are also suitable for the 8085

CPU

Device	Source
8085A	AMD
8085A	**Intel (1944)**
8085A-2	**Intel (1944)**
M5L8085	Mitsubishi
μPD8085A	**NEC Micro (2133)**

PROM (Erasable), I/O

Device	Source
8755A	**Intel (1946)**
μPD8755A	**NEC Micro (2269)**

RAM, I/O, Timer

Device	Source
8155	AMD
8155	**Intel (1945)**
8155-2	**Intel (1945)**
8156	**Intel (1945)**
8156-2	**Intel (1945)**
μPD8155	**NEC Micro (2164)**
μPD8156	**NEC Micro (2164)**

ROM, I/O

Device	Source
8355	AMD
8355	**Intel (1946)**
8355-2	**Intel (1946)**
μPD8355	**NEC Micro (2269)**

Analog Input, Multiplexer, A/D Converter

Device	Source
MP21	**Burr-Brown (659)**

Bidirectional Bus Driver. See 8216, 8226, etc. under 8080.

Device	Source
8216	Intel
8226	Intel
μPB8216	**NEC Micro (2184)**

† Military Temperature Range (−55° to 125°C)

* Typical Values

(Continued)

MICROPROCESSOR–System Components (Cont'd)

8085A (Cont'd.)

Bidirectional Bus Driver. See 8216, 8226, etc. under 8080. (Cont'd.)
- **μPB8226 — NEC Micro (2184)**

Programmable Communication Interface (USART)
- 8251 — AMD
- 8251 — Intel
- **μPD8251 — NEC Micro (2204)**

Decoder, 1 of 8. See 8205, etc. under 8080.
- 8205 — Intel

Programmable Direct Memory Access Controller.
- 8257 — AMD
- 8257 — Intel
- 8257-5 — Intel
- **μPD8257 — NEC Micro (2236)**

Cassette Controller
- μPD371 — NEC Micro

CRT Controller. See 8275, etc. under 8080.
- **8275-5 — Intel (1942)**

Floppy Disc Controller. See 8271, etc. under 8080.
- **8271 — Intel (1940)**
- μPD372 — NEC Micro

Keyboard Display Controller—See listing under 8080

8-Bit I/O Port. See 8212, etc. under 8080.
- MB471 — Fujitsu
- 8212 — Intel
- **μPB8212 — NEC Micro (2172)**

Priority Interrupt Control. See 8214, etc. under 8080.
- 8214 — Intel
- **μPB8214 — NEC Micro (2178)**

Programmable Interrupt Controller.
- 8259 — Intel
- 8259-5 — Intel
- **μPD8259 — NEC Micro (2244)**
- **μPD8259-5 — NEC Micro (2244)**

Programmable Interval Timer.
- 8253-5 — AMD
- 8253-5 — Intel
- **μPD8253 — NEC Micro (2221)**

Programmable Peripheral Interface.
- 8255A-5 — AMD
- 8255A-5 — Intel
- μPD8255A — NEC Micro

SDLC Protocol Controller. See 8273, etc. under 8080.
- **8273 — Intel (1941)**
- μPD379 — NEC Micro

GPIB Talker/Listener Interface
- **8291 — Intel (1943)**

ROM(2048x8) and I/O
- **μPD8355 — NEC Micro (2269)**

Erasable PROM, I/O
- **8755A — Intel (1946)**
- **μPD8755A — NEC Micro (2269)**

Universal Peripheral Interface(slave microprocessor)
- 8041 — AMD
- **8041 — Intel (1939)**
- **8741 — Intel (1939)**
- **μPD8041 — NEC Micro (2090)**
- **μPD8741 — NEC Micro (2090)**

I/O Expander
- 8243 — AMD
- 8243 — Intel
- **μPD8243 — NEC Micro (2199)**
- **8243 — Signetics (2313)**

8085A (Cont'd.)

RAM (1024x8) (See also: Memory-RAMs)
- 8185 — Intel

Development System
- **Intellec MDS — Intel (1950)**

8086

Many devices for the 8080 are also suitable for the 8086

CPU, 16-bit
- **8086 — Intel (1947)**

Octal Latch, Non-Inverting
- **8282 — Intel (1948)**

Octal Latch, Inverting
- **8283 — Intel (1948)**

Clock Generator
- **8284 — Intel (1948)**

Octal Bus Transceiver, Non-Inverting
- **8286 — Intel (1948)**

Octal Bus Transceiver, Inverting
- **8287 — Intel (1948)**

Bus Controller
- **8288 — Intel (1948)**

Programable Interrupt Controller
- 8259A — Intel

Development System
- **Intellec MDS — Intel (1950)**

9080-See 8080 Series

9440

CPU, 16-Bit
- **9440C — Fairchild (1903)**
- **9440M — † Fairchild (1903)**

Memory Control Unit
- 9441C — Fairchild

I/O Control Unit
- 9442C — Fairchild

9900

Microprocessor
- **S9900 — AMI (1840)**
- **S9980 — AMI (1851)**
- **S9981 — AMI (1851)**
- SMC9980 — SMC
- SBP9900AE — TI
- SBP9900AC — TI
- SBP9900AM — † TI
- TMS9900 — TI
- TMS9980A — TI
- TMS9981 — TI
- TMS9985 — TI

Microcomputer, 16-Bit
- **S9940 — AMI (1850)**
- TMS9940 — TI

Microcomputer, 16-Bit(Erasable PROM)
- TMS9940E — TI

Clock Generator and Driver (4-phase for 9900)
- S9904 — AMI
- SN54LS362 — † TI
- SN74LS362 — TI

(Continued)

9900 (Cont'd.)

Clock Generator and Driver (4-phase for 9900) (Cont'd.)
- TIM9904 — TI

Bubble Memory Controller
- TMS9916 — TI
- TMS9922 — TI

CRT Controller
- TMS9927 — TI

DMA Controller
- S9911 — AMI
- TMS9911 — TI

Floppy Disc Controller
- TMS9909 — TI

Data Selector/Multiplexer (See also Digital-TTL-Multiplexers 74LS251)
- μPB74LS251 — NEC America
- SN54LS251 — † TI
- SN74LS251 — TI
- TIM9905 — TI

GPIB Controller
- TMS9914 — TI

Priority Encoder (See also Digital-TTL-Miscellaneous, Priority Encoder, 74LS148)
- SN74LS148 — TI
- TIM9907 — TI

Priority Encoder, 8-Line to 3-Line, three state
- SN74LS348 — AMD
- SN74LS348 — TI
- TIM9908 — TI

Programmable Systems Interface (interrupt prioritization, I/O control and interval timing)
- **S9901 — AMI (1844)**
- TMS9901 — TI

Synchronous Communication Controller (Bi-Sync and SDLC)
- **S9903 — AMI (1848)**
- TMS9903 — TI

Asynchronous Communication Controller (UART) (See also Interface-Serial Transmitters-Receivers)
- **S9902 — AMI (1846)**
- TMS6011 — TI
- TMS9902 — TI

8-Bit Addressable Latch
- SN54LS259 — † TI
- SN74LS259 — TI
- TIM9906 — TI

Programmable Communications Register(CRU),I/O Expander
- SBP9960C — TI
- SBP9960M — † TI

Interrupt Controller/Timer
- SBP9961C — TI
- SBP9961M — † TI

Octal Fiber-Optics Serial Transmitter, Expandable
- SBP9962C — TI
- SBP9962M — † TI

Serial Fiber Optics Transmitter, with expandable octal demultiplexer
- SBP9963C — TI

SBP9963M
- SBP9963M — † TI

8-bit Parrallel Byte Multiplier
- SBP9708C — TI

(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Values

Bold face indicates additional data is provided on the page noted.

MICROPROCESSOR–System Components (Cont'd)

9900 (Cont'd.)

8-bit Parrallel Byte Multiplier (Cont'd.)
SBP9708M † TI

Memories: See Memory: PROMs, RAMs (Dynamic or Static), and ROMs

10800

Arithmetic Logic Unit, 4-Bit Slice
MC10800 Motorola

Microprogram Control Function
MC10801 Motorola

Memory Interface
MC10803 Motorola

Timing Function, 4 Phase
MC10802 Motorola

4-Bit Bidirectional Translator with Latch
MC10804 Motorola

5-Bit Bidirectional Translator with Latch
MC10805 Motorola

5-Bit ECL Transceiver with Latch
MC10807 Motorola

Dual Address Register(32x9 Stack)
MC10806 Motorola

Multibit Shifter(16-Bit Programmable Shifter)
MC10808 Motorola

Memories (See Digital-ECL-Memories and Memory-PROMs/ROMs)

14500

CPU, 1-Bit, Industrial Control Unit
MC14500B Motorola (2009)

Latch, 8-Bit
MC14597BA † Motorola
MC14597BC Motorola
MC14598BA † Motorola
MC14598BC Motorola
MC14599BA † Motorola
MC14599BC Motorola

141000: See 1000 series

67000

Microcontroller
5701 † MMI
6701 MMI

Microprogram Control Unit
57110 † MMI
67110 MMI

FIFO Memory (64x4) (See also Memory-FIFO's)
57401 † MMI (1472)
67401 MMI (1472)

Multiplier (8x8)
57588 † MMI
67558 MMI (495)

58840

Microcomputer, 4-bit, with 8-bit A/D
MP58840 Mitsubishi

58840 (Cont'd.)

Microcomputer Evaluator
M58842 Mitsubishi

68000

6800 devices are suitable for the 68000

Microprocessor, 16-bit
MC68000 Motorola

General Purpose

Analog Input, Multiplexer, A/D Converter
MP20 Burr-Brown (659)
MP21 Burr-Brown (659)
MP22 Burr-Brown (659)

Analog Input, Multiplexer, A/D (Analog to Pulse Width Output)
μA9708 Fairchild (944)

Analog Output, D/A Converter, Latched Input
NE5018 Signetics (808)

Analog Output, Dual D/A Converter
MP10 Burr-Brown (659)
MP11 Burr-Brown (659)

Arithmetic Processor
9511 AMD
9511-4 AMD
MM57109 National
TMS1018 TI

Arithmetic Processor, 4 function ASCII Floating Point Computations
CY-450 Cybernetic

Bubble Memory Controller
TMS9923 TI

Sequence Controller
57110 † MMI
67110 MMI

Display Controller (Dot), LED and Keyboard Interface
MTX-A1 Matrox

Display Controller (Segment), Keyboard Interface
MTX-B1 Matrox

Control Sequencer (to control fetch sequence of microinstructions)
N8X02 Signetics (2280)

CRT Controller
DP8350 National (793,238,297)

CRT Processor
SFF96364 NPC

CRT Processor, with external sync.
SFF96366 NPC

CRT Video Display Controller, Video Generator
CRT8002 SMC

CRT Video Timer-Controller, Programmable
HD46505 Hitachi
CRT5027 SMC
TMS9927 TI

CRT Video Timer-Controller, Programmable Interface
CRT5037 SMC

Direct Memory Access(16-Bit)
DM1883 Western

Priority Interrupt Controller
MC6828 Motorola
(Continued)

General Purpose (Cont'd.)

Priority Interrupt Controller (Cont'd.)
MC8507 Motorola

Floppy Disc Controller/Transmitter (IBM 3740 compatible)
HD46503 Hitachi
INS1771 National
μPD372 NEC Micro
T3444A Toshiba
FD1771 Western
FD1781 Western
FD1781-01 Western
FD1791 Western

Floppy Disc Controller, Two-Sided
T3444D Toshiba

Single/Double Density Floppy Disc Controller
μPD765 NEC Micro (2146)

Cassette Controller
HD46502 Hitachi
μPD371 NEC Micro
T3444B Toshiba

Printer Controller, for 5x7 dot matrix printer
CY-480 Cybernetic

Plasma Display Controller and ASCII Keyboard Interface
CY-300 Cybernetic

Synchronous Serial Data Adapter
F6852 Fairchild (1887,1891)
MC6852 Motorola (1973)

Asynchronous Communication Interface Adapter
S6850 AMI (1818)
S6850M † AMI (1818)
S68A50 AMI (1818)
S68B50 AMI (1818)
F6850 Fairchild (1887,1891)
F68A50 Fairchild (1887)
MC6850 Motorola (1977)
MC68A50 Motorola (1977)
MC68B50 Motorola (1977)

General Purpose Interface Adapter (IEEE488 Bus)
HEF4738 Signetics

TV Interface (64x64 color segments display)
M58741 Mitsubishi

TV Sync Generator (PAL)
2621 Signetics (2300)

TV Sync Generator (NTSC)
2622 Signetics (2300)

Peripheral Interface Adapter
S6820 AMI (1802)
S6821 AMI (1798,1802)
S6821M † AMI (1798)
S68A21 AMI (1798)
S68B21 AMI (1798)
F6820 Fairchild (1887)
F6821 Fairchild (1887,1889)
F68A21 Fairchild (1887)
F68B21 Fairchild (1887)
MCS6520 MOS
MCS6522 MOS
MC6820 Motorola
MC6821 Motorola (1991)
(Continued)

† Military Temperature Range (−55° to 125°C)

* Typical Values

MICROPROCESSOR–System Components (Cont'd)

Function	Device	Source	Line
General Purpose (Cont'd.)			
Peripheral Interface Adapter (Cont'd.)			
	MC68A21	**Motorola (1991)**	
	MC68B21	**Motorola (1991)**	
	SY6520	Synertek	
	SY6522	Synertek	
Video Display Generator			
	S68047	**AMI (1830)**	
	F6847	**Fairchild (1887)**	
	HD46847	Hitachi	
	MC6847	**Motorola (1979)**	10
Universal Video Interface			
	2637	Signetics	
Programmable Video Interface Controller			
	2636	**Signetics (2301)**	
Video Interface Controller (reads μP formatted data, supplies graphic signals to modulator)			
	MCS6560	MOS	
Addressable Peripheral Driver			
	NE590	**Signetics (807)**	
	NE591	**Signetics (807)**	20
Sound Generator			
	AY3-8910	GI	
	AY3-8912	GI	
	ICM7219	Intersil	
	SN76477	TI	
See also Interface-Error Checking Circuits Keyboard Encoders, Line Circuits, Memory and Peripheral Drivers, Serial Transmitters/Receivers; Memory-EAROMs, FIFOs, LIFOs, PLAs, PROMs, RAMs, ROMs			30

† Military Temperature Range (−55° to 125°C)

* Typical Values

Bold face indicates additional data is provided on the page noted.



"I need to know if this device exists, and if there are any alternate sources. Where do I start?"

- Memory IC
- RAM
- Static
- 1024x1
- CMOS
- 250 Nanoseconds
- 5 Volts

If you're spending hours to solve a problem similar to the one above, you're behind the times...



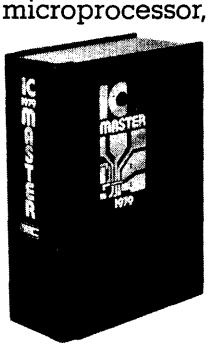
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The AMI S6800 Microcomputer Systems Family

Part No.	Description	Power Supplies	Input/Output	Packages
S6800	8-Bit Microprocessor (1.0MHz Clock Rate)	+5V	TTL	40 Pin SB
S68A00	8-Bit Microprocessor (1.5MHz Clock Rate)	+5V	TTL	40 Pin SB
S68B00	8-Bit Microprocessor (2.0MHz Clock Rate)	+5V	TTL	40 Pin SB
S6801	8-Bit Microcomputer	+5V	TTL	TBA
S6802	1024 Bit (128x8) Microprocessor		TTL	40 Pin
S6809	High Performance Monolithic Microprocessor	+5V	TTL	TBA
S6810A	1024 Bit (128x8) Static Read/Write Memory			24 Pin C, P
	(450ns Access Time)	+5V	DTL/TTL	40 Pin C, P
S6810A-1	1024 Bit (128x8) Static Read/Write Memory			
	(350ns Access Time)	+5V	TTL/CMOS	24 Pin C, P
S68A10	1024 Bit (128x8) Static Read/Write Memory			
	(360ns Access Time)	+5V	TTL	24 Pin SB
S68B10	1024 Bit (128x8) Static Read/Write Memory			
	(250ns Access Time)	+5V	TTL	24 Pin SB
S6820	Peripheral Interface Adapter (PIA)	+5V	TTL	40 Pin
S6821	Peripheral Interface Adapter (PIA)	+5V	TTL	40 Pin
S68A21	Peripheral Interface Adapter (PIA)	+5V	TTL/CMOS	40 Pin SB
S68B21	Peripheral Interface Adapter (PIA)	+5V	TTL/CMOS	40 Pin SB
S6831A	16,384 Bit (2048x8) ROM	+5V	TTL	24 Pin P, E, C
S6831B	16,384 Bit (2048x8) ROM	+5V	TTL	24 Pin P, E, C
S6834	4096 Bit (512x8) EPROM	+5V, -12V	Three-State	24 Pin C
S6840	Programmable Timer	+5V	TTL	28 Pin
S6846	NMOS Combination ROM, I/O, Timer	+5V	TTL	40 Pin P, C
S6850	Asynchronous Communication Interface Adapter	+5V	TTL	24 Pin S, E, P
S68A50	Asynchronous Communication Interface Adapter	+5V	TTL	24 Pin SB
S68B50	Asynchronous Communication Interface Adapter	+5V	TTL	24 Pin SB
S6852	Synchronous Serial Data Adapter (SSDA)	+5V	TTL	24 Pin C, P
S6854	Advanced Data Link Controller	+5V	TTL	24 Pin C, P
S68A54	Advanced Data Link Controller	+5V	TTL	24 Pin C, P
S68047	Video Display Generator	+5V	TTL	40 Pin P, S
S68488	General Purpose Interface Adapter (GPIA)	+5V	TTL	40 Pin P

The AMI S9900 Microcomputer Systems Family

Part No.	Description	Power Supplies	Input/Output	Packages
S9900	16-Bit Single Chip Microprocessor	+12V, ±5V	TTL	64 Pin Package
S9901	Programmable Systems Interface Circuit	+5V	TTL	40 Pin Package
S9902	Asynchronous Communications Controller (ACC)	+5V	TTL	18 Pin Package
S9903	Synchronous Communications Controller (SCC)	+5V	TTL	20 Pin Package
S9940	16-Bit Single Chip Microcomputer	+5V	TTL	18 Pin Package
S9980	16-Bit Single Chip Microcomputer	+5V	TTL	40 Pin Package
S9981	16-Bit Single Chip Microcomputer	+5V	TTL	40 Pin Package

(P) = Plastic Package, (E) = Cer-DIP Package, (C) = Ceramic Package, (S) = SLAM Package, (SB) = Side Brazed Package

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S2000 Single-Chip Microcomputer Family

AMI's S2000 family of single-chip microcomputers offers a wide range of capability to the user seeking flexible, adaptable system(s) at low cost. The S2000 family provides the ideal solution to appliance and industrial/process-control applications. With versatile keyboard-oriented inputs, and outputs which can drive either LED or fluorescent displays directly, the S2000 family is designed specifically to minimize system parts count and cost.

Table I. S2000 Family Features

	S2000	S2150	S2200	S2400
ROM (x8)	1K	1.5K	2K	4K
RAM (x4)	64	80	128	128
Interrupts	—	—	3	3
A/D CONV (8 Channel)	—	—	8-Bit	8-Bit
Counter/Timer	÷50/÷60	÷50/÷60	8-Bit	8-Bit
Max Subroutine Levels	3	3	5	5
Instructions	51	51	59	59
Cycle Time (μs)	4.5	4.5	4.5	4.5
High Voltage (Fluorescent Display Drive Version)	S2000A	S2150A	S2200A	S2400A

The S2000 family provides the advantages of computer architecture to low cost, minimum-parts-count display/keyboard oriented control systems.

S2000/2150 Features

- ☐ **1024 x 8 Program ROM On-Chip; Externally Expandable to 8192 x 8 — S2000**
- ☐ **1536 x 8 Program ROM On-Chip; Externally Expandable to 8192 x 8 — S2150**
- ☐ **64 x 4 Scratchpad RAM On Chip — S2000**
- ☐ **80 x 4 Scratchpad RAM On-Chip — S2150**
- ☐ **13 Outputs and Inputs, Plus 8 Bi-Directional Three-State Lines**
- ☐ **Touch Control™ Capacitive Touchplate Interface**
- ☐ **Seconds Timer for Both 60Hz and 50Hz Lines**
- ☐ **7-Segment Decoder and LED Display Drivers On Chip**
- ☐ **Single 9.0 Volt Supply**
- ☐ **Fast 4.5μs Execution Cycle**
- ☐ **Three-Level Subroutine Stack**
- ☐ **TTL-Compatible Outputs**
- ☐ **Reset, Test, and Single Step Modes**
- ☐ **Access to All Internal Registers and Memory for Debug and Test**
- ☐ **Crystal Input for Accurate Clocking — S2150**
- ☐ **Low Power RAM Retention, 20μA/Bit Typ @ 4V — S2150**

S2000A/2150A Vacuum Fluorescent Display

The S2000A/2150A are identical to the S2000/2150 but provide high voltage fluorescent display capability. The output buffer drive (V_{DD}) is changed to a vacuum fluorescent drive (V_{FD}) and typically tied to 32 volts. The D_0 through D_7 and A_0 through A_4 are changed from LED drivers (nominal 5 volts) to vacuum fluorescent drivers (nominal 26 volts).

S2200/2400 Features

The S2200/2400 provide a quantum jump in chip features beyond the S2000. In addition to all the features the S2000 offers, the S2200 gives the added flexibility of interrupts and the sophistication of an on-chip A/D or D/A converter capable of multiplexing 8 channels of analog data making it suitable for a wide range of applications.

- ☐ **2048 x 8 Program ROM On Chip Expandable to 8192 x 8 — S2200**
- ☐ **4096 x 8 Program ROM On-Chip; Externally Expandable to 8192 x 8 — S2400**
- ☐ **128 x 4 Scratchpad RAM On Chip**
- ☐ **RAM Save Power Down Mode (Mask Option)**
- ☐ **Two-Level Maskable Priority Interrupt System with Provision for Software Interrupt**
- ☐ **Programmable 8-Bit Timer/Event Counter On Chip**
- ☐ **13 Outputs, 9 Inputs, Plus 8 Bi-Directional Three-State Lines**
- ☐ **Touch Control™ Capacitive Switch Interface**
- ☐ **7-Segment Display Decoders and LED Drivers**
- ☐ **TTL-Compatible Outputs**
- ☐ **Single +9V Power Supply**
- ☐ **4.5μs Cycle Time**
- ☐ **59 Instructions — 52 Single Byte and Single Cycle**
- ☐ **3-Level Subroutine Stack**
- ☐ **2-Level Interrupt Stack**
- ☐ **Built-In Production Test Mode**
- ☐ **Single-Step Capability**
- ☐ **Power-Fail Detect, RAM Keep-Alive and Power-On Reset Circuitry**
- ☐ **8-Bit A/D Converter (Up to 8 Channels)**
- ☐ **D/A Converter Capability (Mask Option)**
- ☐ **Up to 256 General Purpose Flags**
- ☐ **6 Special Flags**
- ☐ **Table Look-Up Capability**
- ☐ **S2200A/2400A Vacuum Fluorescent Display Capability**

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S2000 Family

	S2000	S2000A	S2150	S2150A	S2200	S2200A	S2400	S2400A
Product Characteristics								
ROM (Bytes)	1K	1K	1.5K	1.5K	2K	2K	4K	4K
RAM (Nibbles)	64	64	80	80	128	128	128	128
A/D Converter (8-Bit)	—	—	—	—	YES	YES	YES	YES
Timer	50/60Hz	50/60Hz	50/60Hz	50/60Hz	PROG 8BIT	PROG 8BIT	PROG 8BIT	PROG 8BIT
Interrupts	—	—	—	—	3	3	3	3
Power Fail Detect	—	—	—	—	YES	YES	YES	YES
High Voltage Outputs	—	YES	—	YES	—	YES	—	YES
Crystal Clock Option	—	—	YES	YES	YES	YES	YES	YES
TouchControl Inputs	YES	YES	YES	YES	YES	YES	YES	YES
Levels of Subroutine	3	3	3	3	5	5	5	5
# of Flags	2	2	2	2	262	262	262	262
Power-Down RAM Option	—	—	YES	YES	YES	YES	YES	YES
D/A Converter Option	—	—	—	—	YES	YES	YES	YES
Zero — Crossing Detect	YES	YES	YES	YES	YES	YES	YES	YES
Cycle Time (μsec)	4.5	4.5	4.5	4.5	4.5	4.5	4.5	4.5
Instructions — Total	51	51	51	51	59	59	59	59
Single Cycle & Byte	49	49	49	49	52	52	52	52
Development Support								
Microcomputer Development Center	YES	YES	YES	YES	YES	YES	YES	YES
Logic Analyzer	YES	YES	YES	YES	YES	YES	YES	YES
Hardware Emulator	#2150	#2150A	#2150	#2150A	#2400	#2400A	#2400	#2400A

S2000 Family Support

The S2000 single-chip microcomputer family, unlike many microprocessors, does not leave the designer or industrial OEM unsupported. The S2000 Family features a proven array of development aids:

Microcomputer Development Center (MDC) — AMI's MDC is a fully equipped, dual-floppy disk-based microcomputer development facility, complete with FDOS-II Floppy-Disk-Operating and File Management System. Controlled from its CRT terminal, MDC provides instant access to program and data files resident on removable diskettes.

Development Software — The MDC's software includes self-diagnostics and a comprehensive Text Editor and PROM programmer package that support S2000 software development. In addition, S2000 software includes a MACRO Assembler, Loader, and Instruction Simulator.

Cross-Assemblers editor and simulator debug — Available on a major timesharing service.

Logic Analyzer — The MDC-140 Logic Analyzer is an advanced debug tool connected as a peripheral device of the AMI Microcomputer Development Center (MDC). Features include:

- Captures 1024 Events of 40 Parallel Inputs
- Captures Data Under Control of Programmable Start on Data Content
- Delay of −1024 to +64K Clock Periods
- Setup and Display of Captured Data Under Control of MDC Software
- Display Format is User-Definable; Captured Data Can Be Displayed in a Mix of Hex, Octal, Binary, ASCII and Special Formats for Support of S6800, S6820, S2000, 8080, etc.
- Four Clock Sources
- Input Voltage Range = −15 to +15 volts
- Adjustable Input Thresholds
- Data-Dependent Output for Triggering an Oscilloscope

SES-2150(A)/SES-2400(A) — The SES-2150/2400 Emulator boards are pin-for-pin substitutes for S2000 microcomputer family chips. The Emulator Boards use conventional UV erasable PROMs for program storage.

In addition, a specialized module is used to provide emulation of the S2150A/S2400A high voltage vacuum fluorescent display drivers.

Customer Assistance — AMI's S2000 Family Applications Engineering Staff is readily available for consultation regarding any aspects of S2000 Family usage. The AMI staff is also available to discuss any special modifications to the S2000 for high volume applications.

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S2000 Family Instruction Set Summary

The S2000 and S2150 contain 51 instructions, all single byte, with 49 that are single cycle. The S2200 and S2400 contain 59 instructions, of which 52 are single cycle and single byte.

Nearly all S2000/2150 instructions are common to the entire family, which allows the programmer to develop software expertise and easily move up the S2000 product line.

Register Instructions

S2000/2150	S2200/2400	
LAI X	LAI X	X→ACC, 0≤X≤15; (In S2000/2150 Select I and K Inputs also)
LAB	LAB	BL→ACC
LAE	LAE	E→ACC
XAB	XAB	BL↔ACC
XABU	XABU	BU↔ACC, (IN S2150, BITS 2, 1, AND 0; IN OTHERS, BITS 1 AND 0 ONLY)
XAE	XAE	ACC↔E
LBE Y	LBE Y	Y→BU, E→BL, 0≤Y≤3
LBZ Y	LBZ Y	Y→BU, 0→BL, 0≤Y≤3
LBF Y		Y→BU, 15→BL, 0≤Y≤3
LBEP Y		Y→BU, E+1→BL, 0≤Y≤3
	SRB	1→BA
	RRB	0→BA
	LMDI X+	X(6)→BA, X(5-4)→BU, X(3-0)→BL
	RAR	ACC(I)→ACC(I-1), ACC (0)→CARRY, CARRY→ACC(3)
	XAK	KSR↔ACC
	LANG	ACC→AR (3-0), RAM→AR(7-4)
	LNMA	ACC→NR(3-0), RAM→NR (7-4), THEN NR→BIN
	MOD	ACC→MOD(3-0), RAM→MOD(7-4)
	RBIN	BIN(3-0)→ACC; BIN(7-4)→RAM

RAM Instructions

S2000/2150	S2200/2400	
LAM Y*	LAM Y*	RAM→ACC, BU⊕Y→BU
XC Y*	XC Y*	RAM↔ACC, BU⊕Y→BU
XCI Y*	XCI Y*	ACC↔RAM, BL+1→BL, BU⊕Y→BU SKIP IF BL=0 (AFTER INCREMENT)
XCD Y*	XCD Y*	ACC↔RAM, BL-1→BL, BU⊕Y→BU SKIP IF BL=0 (BEFORE DECREMENT)
STM Z	STM Z	1→RAM BIT Z, 0≤Z≤3
RSM Z	RSM Z	0→RAM BIT Z, 0≤Z≤3
	LMA	ACC→RAM
	STMI Z+	1→RAM BIT Z, 0≤Z≤255, (RAM BANK 1)
	RSMI Z+	0→RAM BIT Z, 0≤Z≤255, (RAM BANK 1)

Input/Output Instructions

S2000/2150	S2200/2400	
INP	IND	D3-D0→ACC, D7-D4→RAM
OUT	OUT	ACC→D3-D0, RAM→D7-D4 (NOT LATCHED)
DISN	DISN	ACC→SEGMENT DECODER→DISPLAY LATCH→D6-D0, CARRY→DISPLAY LATCH→D7
DISB	DISB	ACC→DISPLAY LATCH→D3-D0, RAM→DISPLAY LATCH→D7-D4
MVS	MVS	A-LINE MASTER STROBE LATCH→A LINES
PSH	PSH	PRESET HIGH [BL]→MASTER STROBE LATCH
PSL	PSL	PRESET LOW [BL]→MASTER STROBE LATCH
EUR		(EUROPEAN) SET 50/60Hz AND DISPLAY LATCH POLARITY
	INK	K3-K0→ACC, K7-K4→RAM

+ 8 bits in the second byte of an instruction.

*Assembled code contains complement of those arguments (the assembler does it automatically).

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S2000/S2150 and S2200/S2400 Instruction Set Summary

Program Control Instructions

S2000/2150	S2200/2400	
PP X*	PP X*	IF PREVIOUS INSTRUCTION = PP, X→PPR (0≤X≤15) IF PREVIOUS INSTRUCTION = PP, X→PBR (0≤X≤7)
JMP X	JMP X	JUMP TO LOCATION X, X→LR (0≤X≤15) EXCEPT IF PREVIOUS INSTRUCTION = PP
JMS X	JMS X	JUMP TO SUBROUTINE AT X, LR + 1→L STACK, PR→P STACK, X→LR, 15→PR EXCEPT IF PREVIOUS INSTRUCTION = PP
RT	RT	L STACK→LR, P STACK→PR
RTS	RTS	L STACK→LR, P STACK→PR, SKIP INSTR.
NOP	NOP	NO OPERATION
	RTI	RETURN FROM INTERRUPT, RESTORE REGISTERS
	TLU	IF PREVIOUS INSTRUCTION WAS A PP, DO A TABLE LOOK-UP SEQUENCE: PC + 1→STACK RAM→PC(3 – 0), ACC→PC(7 – 4), PPR(3 – 2)→PC(9 – 8) ROM(7 – 4)→RAM, ROM(3 – 0)→ACC STACK→PC. IF PREVIOUS INSTRUCTION WAS NOT A PP, DO AN INDEXED SUBROUTINE CALL: PC + 1→STACK RAM→PC(3 – 0), ACC→PC(7 – 4)

Skip Instructions (Skip 1 Non-PP Instruction) (RAM = Memory at BU,BL)

S2000/2150	S2200/2400	
SZC	SZC	SKIP IF CARRY = 0
SZM Z	SZM Z	SKIP IF RAM BIT Z = 0, 0≤Z≤3
SZK	SZK	SKIP IF K BIT(S) = 0, (BIT(S) IN LAST LAI)
SBE	SBE	SKIP IF BL = E
SAM	SAM	SKIP IF ACC = RAM
SZI		SKIP IF I BIT(S) = 0, (BIT(S) IN LAST LAI)
SOS		SKIP IF SF = 1, 0→SF. (SF = 'SECONDS' FLAG OUTPUT OF ÷50/÷60 COUNTER)
TF1		SKIP IF FLAG 1 = 1
TF2		SKIP IF FLAG 2 = 1
	SZMI Z +	SKIP IF RAM BIT = 0, (IN RAM BANK 1) 0≤Z≤255
	SKFL X +	SKIP IF FLAG = 1

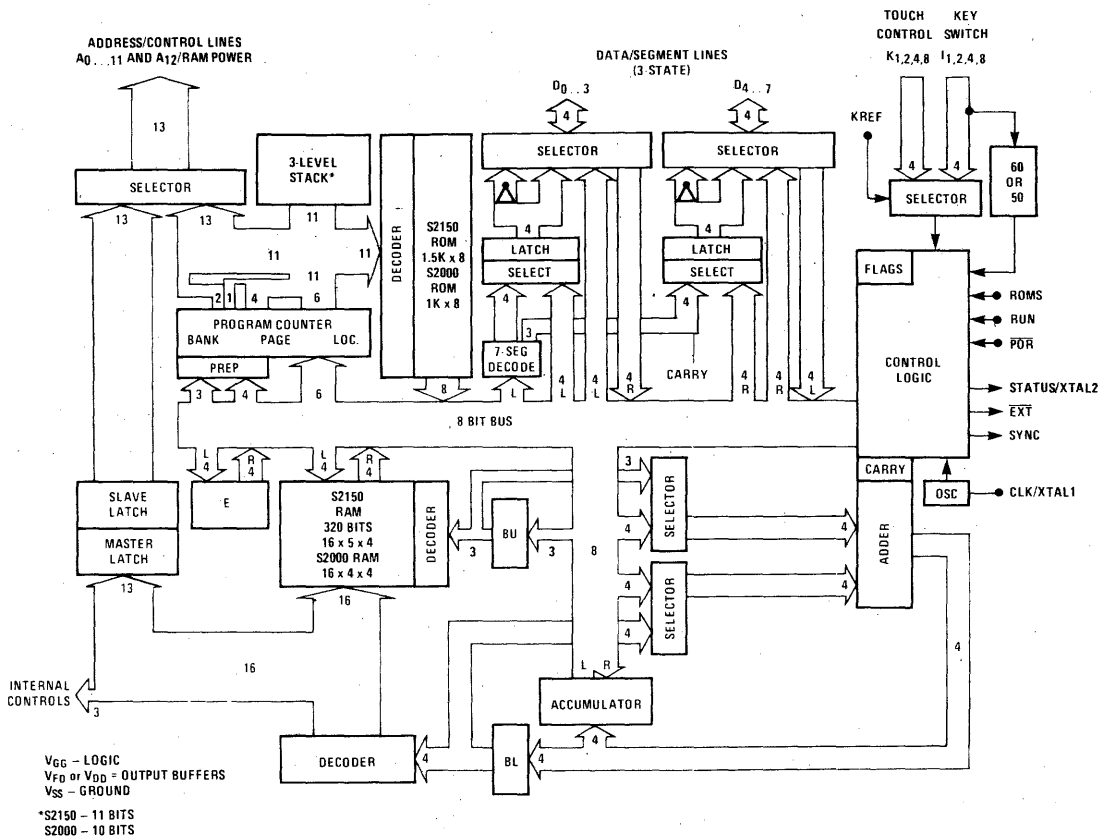
Arithmetic and Logical Instructions

S2000/2150	S2200/2400	
ADCS	ADCS	RAM + ACC + CARRY→ACC + C, SKIP IF SUM≤15
ADIS X	ADIS X	X + ACC→ACC, SKIP IF SUM ≤15, CARRY UNALTERED
ADD	ADD	ACC + RAM→ACC, CARRY UNALTERED
AND	AND	ACC & RAM→ACC
XOR	XOR	ACC ⊕ RAM→ACC
STC	STC	1→CARRY
RSC	RSC	0→CARRY
CMA	CMA	15 – ACC→ACC (LOGICAL 1's COMPLEMENT ACC)
SF1		1→FLAG 1
RF1		0→FLAG 1
SF2		1→FLAG 2
RF2		0→FLAG 2
	SFLG X +	1→FLAG X
	RFLG X +	0→FLAG X

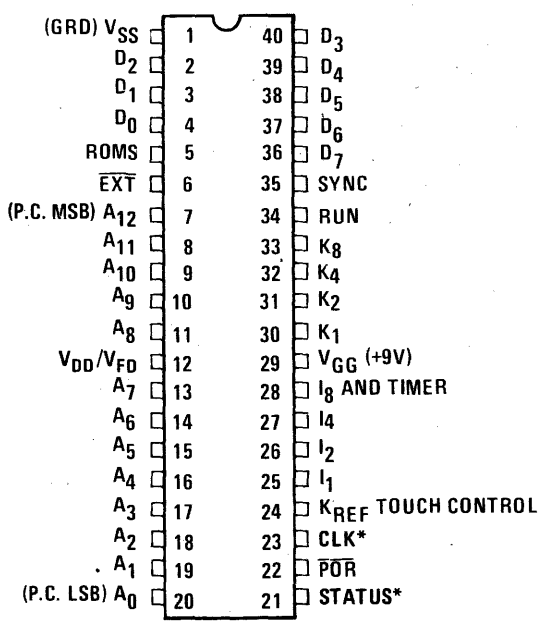
+ 8 bits in the second byte of an instruction.
*Assembled code contains complement of those arguments (assembler does it for you).

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AMI S2000/2150 Detailed Block Diagram



S2000/S2150 Pin Configuration



*May be used for crystal input on S2150/2150A

Pin Descriptions — S2000/2150

PIN NO.	NAME	DESCRIPTION
1	V_{SS}	Most negative power-supply input. Typically grounded.
29	V_{GG}	Most positive power-supply input. Typically +9V.
12	V_{DD} (S2000) V_{FD} (S2000A)	Power supply input for all output buffers. Typically tied to V_{GG} or to a +5V supply. Power supply input for HV drive. Typically +32V
4 – 2, 40 – 36	D0 – D7	D Lines for input and output. Output during instructions OUT, DISN, DISB. Input during INP. Float at reset time or after an MVS instruction; or if RUN pin is low; or after a PSL with BL = 14. Display Latch outputs (DISN, DISB) can be inverted using EUR.
20 – 13 11 – 7	A0 – A12	A Lines for addressing and control. Changed by MVS as set up by PSH/PSL. When external program ROM is used, these lines output the contents of the Program Counter during the first half of each instruction cycle.
5	ROMS	ROM source control. Tied to a logic 1 or 0 to indicate internal ROM only, or internal plus external. Tied to SYNC to override Bank 0 with an external program, and to inverted SYNC to verify internal ROM contents.
6	$\overline{EXT}$	Active-low strobe output for D Lines. Generated by an OUT instruction during time T7.*
35	SYNC	Synchronization output for external devices or for external ROM control. Continuous square wave, low in T1 and T3, high in T5 and T7.* $f_{CLK} \div f_{SYNC} = 4$ for S2000, 8 for S2150.
34	RUN	Run/Wait control for prototyping and single-step testing. Logic 1 to run, logic 0 to wait with D Lines floating.
22	$\overline{POR}$	Power-On-Reset. Needs only an external capacitor, typically .05 microfarad. A pull-up to V_{GG} (15μA nominal) is provided internally.
23	CLK	On-chip oscillator connection. Runs at ~850kHz when connected to V_{SS} through 47pf and to V_{GG} through 30kΩ on the S2000. Crystal control possible; consult AMI.
21	STATUS	Monitors internal status for special designs. Logic 1 vs. logic 0 indicates: (during T1)* D Lines floating or not floating; (T3) BL equal or not equal to 13 for multiplex control; (T5) Carry is 1 or 0; (T7) Next instruction will or won't be skipped. On the S2150 a mask option allows use as a crystal oscillator pin.
24	KREF	K Lines voltage comparator reference input. Typically +3.0V, supplied by an external resistor divider.
30 – 33	K1, K2 K4, K8	K Lines, tested by SZK instruction. Any combination of these lines, selected by the last executed LAI instruction, are gated into the signal input of the voltage comparator. Unselected K Lines are discharged to V_{SS}, at 160μA typical.
25 – 28	I1, I2, I4, I8	I Lines, with internal pull-ups of 100μA nominal. Any combination of these lines, selected by the last executed LAI instruction (S2000, S2150), are gated into a common node tested by the SZI instruction. I8 also clocks a seconds timer whose output is tested using SOS.

*T1 is the first quarter-cycle following the falling edge of the SYNC output, T3 is the second, T5 is the third, and T7 is the fourth.

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S2000/2150

Absolute Maximum Ratings (All voltages measured with respect to V_{SS})

Storage Temperature	−55°C to +125°C
Operating Temperature	0°C to +70°C
Operating Temperature (special request)	−40°C to +85°C
Maximum Positive Voltage	+18V
Maximum Negative Voltage	−0.3V
Maximum Output Currents	(See "Conditions" below)
I_{DD} Supply Current (depends on output loads)	+75mA
Total Average Power Dissipation	+700mW

S2000/2150

Electrical Characteristics

(V_{SS} = 0V, V_{GG} = +7.5V to +10.0V, V_{DD} = 5V*, T_A = 0°C to +70°C, f_{SYNC} = 125kHz to 225kHz)

	Parameter	Min.	Typ.	Max.	Units	Conditions
INPUTS	K_1 thru K_8					2.8 < K_{REF} < 3.2V
	Low Level	0		K_{REF} − 0.5	V	
	High Level	K_{REF} + 0.5		V_{GG}	V	
INPUTS	I_1 thru I_8, POR Schmitt-trigger					(Note 1)
	Low Level	0		1.7	V	
	High Level	5.3		V_{GG}	V	
INPUTS	ROMs, RUN					
	Low Level	0		0.8	V	
	High Level	3.5		V_{GG}		
INPUTS	D_0 thru D_7					
	Low Level	0		0.8	V	
	High Level − Program	5.0		V_{GG}	V	
	High Level − Data	3.5		V_{GG}	V	
OUTPUTS	A_0 thru A_3					
	High Level	3.5		*V_{DD}	V	I = −5mA**
	Low Level	0		0.8	V	I = +25mA**
OUTPUTS	A_4 thru A_{12} $\overline{EXT}$, SYNC, & S					
	High Level	3.5		*V_{DD}	V	I = −5mA**
	Low Level	0		0.6	V	I = +5mA**
OUTPUTS	D_0 thru D_7					
	High Level	3.5		*V_{DD}	V	I = −5mA**
	Low Level	0		1.0	V	I = +12mA**
I_{GG}	Supply Current		28	50	mA	
Δ RAM	RAM "Keep Alive"		20		μA/Bit	V_{RAM} = 4.0V
			30		μA/Bit	V_{RAM} = 9.0V

NOTE 1: There is an internal pull-up of 100μA nominal (15μA nominal on $\overline{POR}$) from each of these inputs to V_{GG}.

*V_{DD} may be connected to V_{GG} if single power supply operation is desired.

**At $V_{GG} \geq 8.5$VDC

Δ Available only on S2150/S2150A.

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S2000A/S2150A

Preliminary Electrical Specifications

Absolute Maximum Ratings (All voltages measured with respect to V_{SS})

Storage Temperature	− 55°C to + 125°C
Operating Temperature	0°C to + 70°C
Operating Temperature (special request)	− 40°C to + 85°C
Maximum Positive Voltage, V_{FD}, A_0-A_4, D_0-D_7	+ 33V
All other pins	+ 18V
Maximum Negative Voltage, any pin	− 0.3V
Maximum Output Currents	(See Conditions below)
Source Current, any pin	− 10mA
Total Average Power Dissipation	+ 700mW
Rate of Rise of V_{FD}	1.6V/msec.
Maximum Voltage at V_{FD} with respect to V_{GG}	+ 22V

S2000A/S2150A

Electrical Characteristics — Specifications noted only for parameters which change from the S2000/2150 to the S2000A/2150A.

(V_{SS} = 0V, V_{GG} = 7.5 to 10.0V, V_{FD} = V_{GG} + 22V, T_A = 0°C to + 70°C. f_{SYNC} = 125kHz to 225kHz)

	Parameter	Min.	Typ.	Max.	Units	Conditions
OUTPUTS	D_0 thru D_7, A_0 thru A_4					
	High Level	− 3.5			mA	V_{OUT} = V_{FD} − 6V**
	Low Level			0.6	V	I = 250μA**
OUTPUTS	A_5 thru A_{12}, EXT, SYNC, & STATUS					
	High Level	3.5			V	I = − 5mA**
	Low Level			0.6	V	I = + 5mA**
I_{GG}	Supply Current		28	50	mA	No Loads

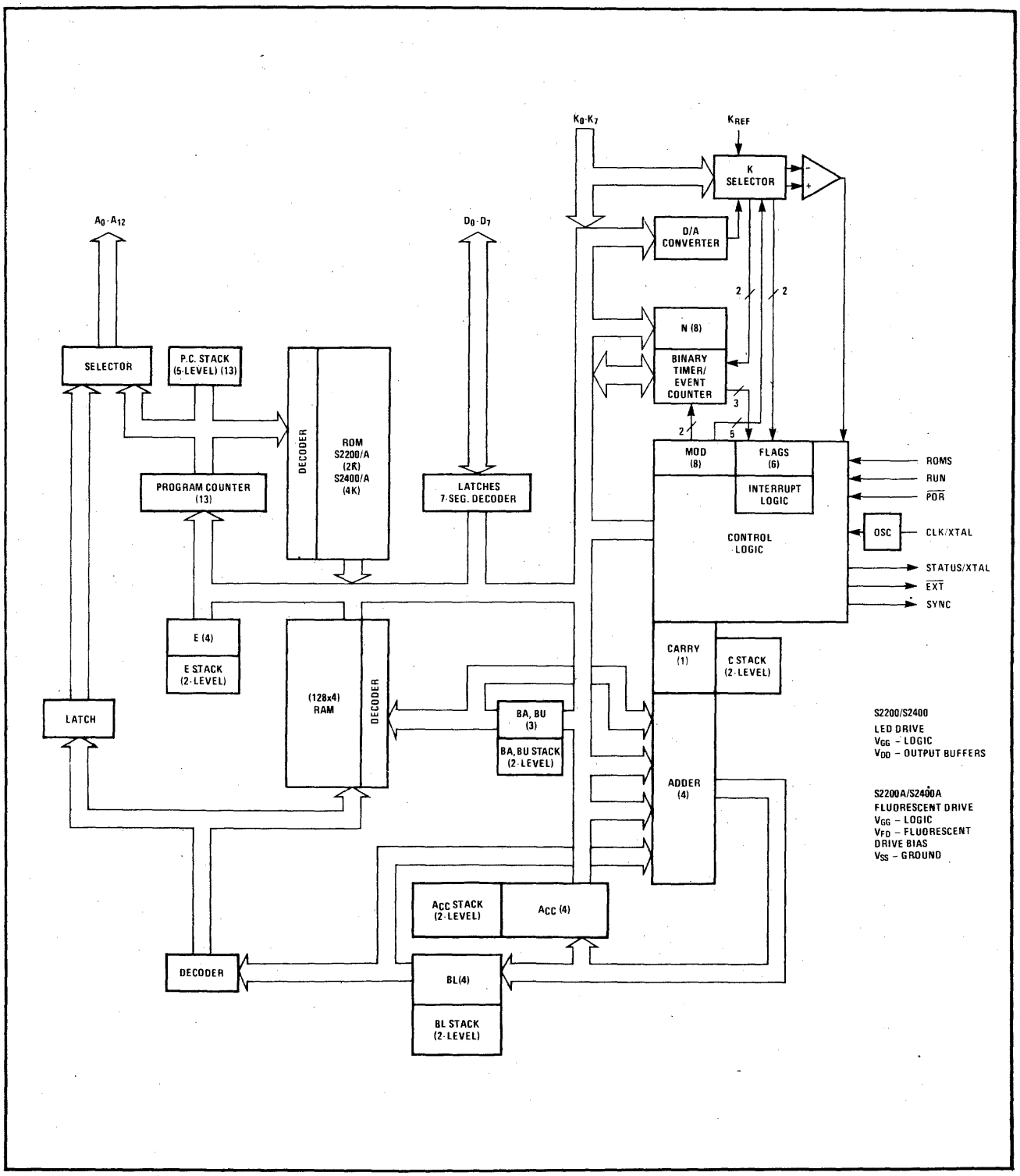
NOTE 1: The output buffers for lines A_5-A_{12} are supplied from V_{GG}.

NOTE 2: The high voltage parts, when biased with normal V_{FD}, are not TTL-compatible; when using external program ROM, it is necessary to interpose buffers.

NOTE 3: When applying power, V_{FD} must rise with or after V_{GG} at a rate not to exceed 1.6V/msec.

**At $V_{GG} \geq$ 8.5VDC

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S2200/2400 Block Diagram

For applications such as pulse width measurement, interval timing and event counting, the S2200/2400 has an 8-bit binary down-counter which counts 256 distinct states. The number of states (1 to 256) is controlled by the (Modulo-) N Register.

Another register, the MOD Register, controls the selection of inputs and outputs for the Programmable Counter/Timer, as well as the Display Latch output polarity and the voltage comparator's noninverting-input source.

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S2200/2400

Absolute Maximum Ratings (All voltages measured with respect to V_{SS})

Storage Temperature	−55°C to +125°C
Operating Temperature	0°C to +70°C
Operating Temperature (special request)	−40°C to +85°C
Maximum Positive Voltage	+18V
Maximum Negative Voltage	−0.3V
Maximum Output Currents	(See Conditions p. 12)
I_{DD} Supply Current (depends upon output loads)	+75mA
Total Maximum Power Dissipation	+700mW

Electrical Characteristics

(V_{SS} = 0V, V_{GG} = +7.5V to +10.0V; V_{DD} = +5V*, T_A = 0°C to +70°C, f_{SYNC} = 125kHz to 225kHz)

	Parameter	Min.	Typ.	Max.	Units	Conditions
INPUTS	K_0 thru K_7				V	For Touch-
	Low Level	0		K_{REF} − 0.5	V	Control and
	High Level	K_{REF} + 0.5		V_{GG}	V	Keyswitch Inputs
INPUT	K_{REF}	0		2/3 V_{GG}	V	
INPUTS	K_0 thru K_7					For A/D
	For A/D Conversion	0		2/3 V_{GG}	V	Conversion
	Logic Low Level			0.8	V	As Logic Inputs
	Logic High Level	3.5			V	
INPUT	$\overline{POR}$					
	Low Level ($\overline{POR}$ Reset)	0		1.0	V	
	High Level	1/2 V_{GG}		V_{GG}	V	
	Power Fail					
	—No Interrupt			V_{GG}	V	
	—Interrupt	V_{GG} + 1			V	
INPUTS	ROMs, RUN					(Note 1)
	Low Level	0		0.8	V	
	High Level	3.5		V_{GG}	V	
INPUTS	D_0 thru D_7					
	Low Level	0		0.8	V	
	High Level	4.5		V_{GG}	V	
OUTPUTS	A_0 thru A_3					
	High Level	3.5		*V_{DD}	V	I = −5mA**
	Low Level	0		0.8	V	I = +25mA**
OUTPUTS	A_4 thru A_{12} EXT, SYNC, & S					
	High Level	3.5		*V_{DD}	V	I = −5mA**
	Low Level	0		0.6	V	I = +5mA**
OUTPUTS	D_0 thru D_7					
	High Level	3.5		*V_{DD}	V	I = −5mA**
	Low Level	0		1.0	V	I = +12mA**
I_{GG}	Supply Current		28	50	mA	
I_{RAM}	RAM "Keep Alive" Current		20		μA/Bit	V_{RAM} = 4.0V

*V_{DD} may be connected to V_{GG} if single power supply operation is desired.
**At $V_{GG} \geq 8.5$VDC

Note 1: There is an internal pullup of 100μA nominal from each of these inputs to V_{GG}.

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S2200A/S2400A Preliminary Electrical Specifications

Absolute Maximum Ratings (All voltages measured with respect to V_{SS})

Storage Temperature	− 55°C to + 125°C
Operating Temperature	0°C to + 70°C
Operating Temperature (special request)	− 40°C to + 85°C
Maximum Positive Voltage, V_{FD}, A_0-A_4, D_0-D_7	+ 33V
All other pins	+ 18V
Maximum Negative Voltage	− 0.3V
Maximum Output Currents	(See Conditions below)
Source Current, any pin	− 10mA
Total Average Power Dissipation	+ 700mW
Rate of Rise of V_{FD}	1.6V/msec.

Electrical Characteristics — Specifications noted only for parameters which change from the S2200/2400 to the S2200A/2400A

(V_{SS} = 0V, V_{GG} = 7.5 + 10.0V, V_{FD} = V_{GG} + 22V, T_A = 0°C to + 70°C. f_{SYNC} = 125kHz to 225kHz)

	Parameter	Min.	Typ.	Max.	Units	Conditions
OUTPUTS	D_0 thru D_7, A_0 thru A_4					
	High Level	− 3.5			mA	V_{OUT} = V_{FD} − 6V**
	Low Level			0.6	V	I = 250μA**
OUTPUTS	A_5 thru A_{12}, EXT, SYNC, & STATUS					
	High Level	3.5			V	I = − 5mA**
	Low Level			0.6	V	I = + 5mA**
I_{GG}	Supply Current		28	50	mA	No Loads

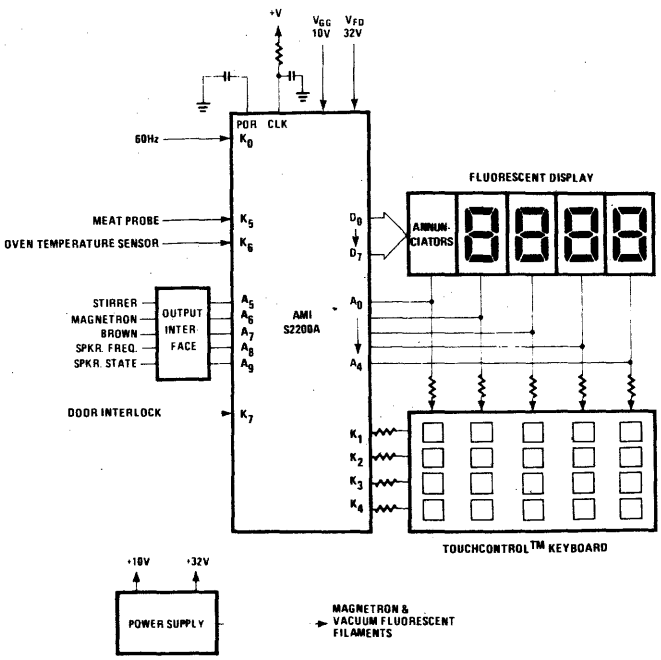
**At $V_{GG} \geq$ 8.5VDC

NOTE 1: The output buffers for lines A_5-A_{12} are supplied from V_{GG}.

NOTE 2: The high voltage parts, when biased with normal V_{FD}, are not TTL-compatible; when using external program ROM, it is necessary to interpose buffers.

NOTE 3: When applying power, V_{FD} must rise with or after V_{GG} at a rate not to exceed 1.6V/msec.

S2200A Typical Microwave/Standard Oven Application



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S6800 Microcomputer Systems

The AMI S6800

The AMI S6800 Microprocessing Family hardware includes a microprocessor, ROM and RAM memories, and data input/output circuits. These components may be assembled in a building block manner into a very simple microcomputer system or into any of progressively more complex systems, which can be used in many general or special purpose applications. The important feature of the S6800 family is that within any system all components are directly compatible in signal functions, circuit performance characteristics, and logic levels. All operate on a single +5V power supply.

It remains to the user to integrate the microcomputer into his own large system and to program it for a specific task. The task may be either simple or complex and either general in purpose or highly specialized for one application.

To facilitate system design and programming, AMI will provide a comprehensive set of reference documents, design and programming aids, a program library, and other applications support. For example, AMI will make available a comprehensive hardware and software reference manual, a S6800 program assembler, and a simulator. Such design and programming support is a continuing and expanding effort at AMI.

S6800 — 8-Bit Microprocessor

The S6800/S68A00/S68B00 is an 8-bit parallel processor with the ability to address up to 65K bytes of memory and execute instructions in two microseconds. It is manufactured using N-channel MOS technology and operates on a single +5V power supply. All inputs and outputs are TTL compatible. The MPU has six internal registers, four types of vectored interrupts and 72 basic instructions. The basic instructions can be used in different addressing modes to save instruction execution time and memory space.

Another important advantage that the S6800/S68A00/S68B00 has to offer in comparison with any other microcomputer system is input/output versatility. In any computer system, large or small, the CPU internal functions are determined by its architecture and the user usually has little opportunity or need to alter them. On the other hand, the I/O configuration is almost always determined by the user and subject to change as peripherals are added or other system alternations are introduced.

S68A10/S68B10 — 1024 Bit (128x8) Static Read/Write Memory

The S68A10 and S68B10 are static Read/Write memories designed and organized to be compatible with the S68A00 and S68B00 microprocessors. Interfacing to the S68A10 and S68B10 consists of an 8-bit bi-directional data bus, seven address lines, a single Read/Write control line, and six chip enable lines, four negative and two positive.

For ease of use, the S68A10 and S68B10 are totally static memories requiring no clocks or cell refresh. The S68A10 and S68B10 are fabricated with N-channel silicon gate depletion load technology to be fully DTL/TTL compatible with only a single +5V power supply required. The data, address and control line organization and functions of the S68A10 and S68B10 match those of the MPU.

S68A21/S68B21 — Peripheral Interface Adapter (PIA)

The S68A21/S68B21 are peripheral interface adapters that provide the univeral means of interfacing peripheral equipment to the S68A00 and S68B00 Microprocessing Units (MPU). These devices are capable of interfacing the MPU to peripheral through two 8-bit bi-directional peripheral data buses and four control lines. No external logic is required for interfacing to most peripheral devices.

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The functional configuration of the PIA is programmed by the MPU during system initialization. Each of the peripheral data lines can be programmed to act as an input or output, and each of the four control/interrupt lines may be programmed for one of several control modes. This allows a high degree of flexibility in the overall operation of the interface.

The PIA interfaces to the S68A00/S68B00 MPUs with an 8-bit bi-directional data bus, three chip select lines, two register select lines, two interrupt request lines, read/write line, enable line and reset line. These signals in conjunction with the S68A00/S68B00 VMA output permit the MPU to have complete control over the PIA. VMA may be utilized to gate the input signals to the PIA.

S6831/A/B/C — 16,384 Bit (2048x8) Read Only Memory

The S6831/A/B/C is a 16,384-bit Read Only Memory organized 2K words by 8 bits. This ROM has been designed to supply large bit storage, high performance memory for microprocessors and other demanding applications with simple interface requirements. The device will operate from a single +5V power supply and is manufactured with N-channel silicon gate depletion load technology. This device is available in all common high-density ROM pinouts.

S6834 — 4096 Bit (512x8) Erasable and Electrically Reprogrammable ROM

The S6834 is a high-speed, static, 512x8 bit, erasable and electrically programmable read only memory designed for use in bus-organized systems. Both input and output are TTL compatible during both read and write modes. Packaged in a 24-pin hermetically sealed dual in-line package, the bit pattern can be erased by exposing the chip to an ultra-violet light source through the transparent lid, after which a new pattern can be written. The device has +5V and -12V power supplies and is processed using a mature P-channel process.

S68A50/S68B50 — Asynchronous Communication Interface Adapter (ACIA)

The S68A50/S68B50 Asynchronous Communication Adapter (ACIA) provides the data formatting and control to interface serial asynchronous data communications to bus organized systems such as the S68A00/S68B00 Microprocessing Units.

The S68A50/S68B50 includes select enable, read/write, interrupt and bus interface logic to allow data transfer over an 8-bit bi-directional data bus. The parallel data of the bus system is serially transmitted and received by the asynchronous data interface, with proper formatting and error checking. The functional configuration of the ACIA is programmed via the data bus during system initialization. Word lengths, clock division ratios and transmit control through the Request-to-Send output may be programmed. For modem operation three control lines are provided.

Basic S6800 Microcomputer System

In a basic system built with the S6800 components the S6800/S68A00/S68B00 Microprocessor is supported by over 1K bytes of memory and controls one input/output interface circuit. The 1024-byte ROM is used to store the operating program, the 128-byte RAM provides working storage for the MPU, and the Peripheral Interface Adapter (PIA) provides two independently programmable 8-bit input/output ports for communicating with two peripheral devices.

The S6800 system is bus oriented. Eight lines from the data bus and 16 more lines make up the address bus. The MPU controls the bus and all other devices — the memories and the PIA — attach to the busses and wait for instructions from the MPU to supply or receive data.

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The basic system is a complete microcomputer, which can be used for a large variety of applications. It is simple but versatile, because it can be easily reprogrammed by changing the ROM. The user must provide only the two-phase clock signal source, a power-up/restart circuit, and a single +5V power supply to complete the hardware.

Expanding the S6800 System

The basic system can be altered or expanded in many different ways. For example, the S68A50/S68B50 Asynchronous Communication Interface Adapter (ACIA) can be substituted for the PIA, to enable the microcomputer to interface with a telecommunications modem. Or, additional memory can be added — either RAM or ROM — to expand the processing capability of the MPU. In general, the system can be expanded in a modular manner, by adding onto the bus as many as ten devices out of the S6800 family. These can be any combination of memory or input/output interface circuits. In this manner a system of nearly any complexity and configuration can be assembled. (Systems with more than ten devices on the bus require the addition of address and data bus buffers to operate at full speed.)

By building a microcomputer from the S6800 family of devices, advantage is taken of the compatibility of the devices. They all conform to the bus discipline, all are compatible in load levels, and the entire system runs on a common system clock. In effect you eliminate most all circuit design, save for the simple clock and power-up/restart circuits. Because you are dealing with only a small number of integrated circuits, circuit layout is simple and the entire microcomputer can be located on a single circuit card.

In some special purpose applications you may need to attach your own interface devices to the bus. As a result, more circuit design will be required, but you will find the S6800 MPU easy to work with. It has features that allow it to be used in many different systems. For example, by using the Halt, Three-State Control, and Data Bus Enable lines, you can easily design a direct memory access system in which either the MPU or a peripheral device can read or write into the RAM and utilize the bus on a priority basis. You can also design a multiprocessor system in which several MPUs can be attached to the same bus and share processing assignments as well as memory space.

S6800 Input/Output

One of the most important advantages that any S6800 system has to offer is its input/output versatility.

In a S6800 system the MPU relegates most of the I/O control to such I/O interfaces as the PIA or ACIA. Each of these circuits is programmable and can interface with peripheral devices without directly involving the MPU. For example, the MPU can preprogram a PIA to either output data to the MPU or to receive it. Thereafter, the PIA circuits assume all functions of interfacing with the peripherals and the MPU never has to look at the interface until service is required. It must service interrupts from the PIA, but never needs to wait for input data to become available or for output data to be accepted. This relieves the MPU of its I/O functions, makes it more efficient in its primary task of data processing, and significantly increases system throughput.

The I/O interfaces and memory are both located in the same address space with the S6800 system. The MPU can access any I/O device the same as a memory location — with address lines, instead of separate I/O control lines. Therefore, it can manipulate data in the I/O interface registers with the same programmed instructions as it uses for memory locations. This adds flexibility and increases system efficiency.

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The S6800 Instruction Set complements the above I/O addressing capability with specific instructions that can be used to access memory as well as I/O circuit registers and perform directly various manipulations on the data.

S6800 Instruction Set

The S6800 MPU has a set of 72 basic instructions. These include binary and decimal arithmetic functions as well as logical, shift, rotate, load, store, branch, interrupt, and stack manipulation functions. Most of the instructions have several variations and most can be used with several memory addressing modes. The total complex of instructions available to the programmer is actually 197.

An instruction can be from one to three bytes long, depending on the addressing mode used with the instruction. The first byte always contains the operation code, which designates the kind of operation the MPU will perform. In single byte instructions no memory address is required, because the operation is performed on one of the internal MPU registers. In multiple byte instructions the second and third byte can be the operand, or a memory address for the operand.

A noteworthy feature of the S6800 MPU is that some of the instructions can operate directly on any memory location. In other computer systems it is common that the processor fetches an operand from memory, stores it in the accumulator, then executes the operation in the ALU and finally writes the result back into the memory. The S6800 is able to accomplish the same with only a single instruction, because it operates with any external location in the same manner as with an internal register. For example, it can directly increment or decrement the contents of a memory location. Because the MPU addresses I/O devices just like a memory location, it can do the same with registers inside the PIA or ACIA. The ASL, ASR, LSR, and ROL are other examples of instructions which operate in this manner.

MPU Registers

Accumulators A and B — Two separate 8-bit accumulators that are used to hold operands and results of operations in the ALU.

Index Register — A 16-bit register used for memory address storage in Indexed Addressing operations.

Program Counter — A 16-bit register that holds the current program instruction address. Once the initial program starting address is loaded into the program counter, it is incremented under control of the MPU hardware.

Stack Pointer — A 16-bit register used for storage of the next available location in an external push-down/pop-up stack.

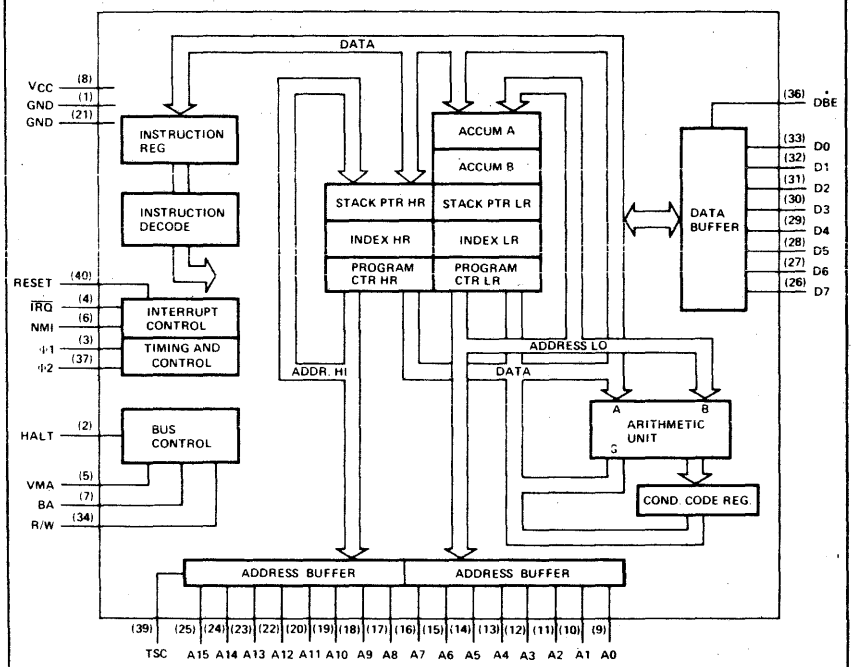
Condition Code Register — An 8-bit register that stores certain results of operations in the ALU. These bits are used as testable conditions for the conditional branch instructions. In addition, one bit position stores the interrupt mask bit and the two high order bits are unused.

Memory Register

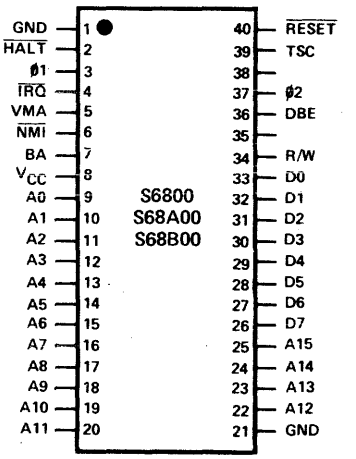
External Stack — The MPU uses a push-down/pop-up stack that can be located anywhere in RAM and be of any convenient size. It is accessed with the stack pointer address and has several uses. First, it always stores the MPU register contents following an interrupt and return addresses during subroutine execution. Second, it can also be used by the programmer to store data during program execution.

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8-BIT
MICROPROCESSOR



BLOCK DIAGRAM



PIN CONFIGURATION

FEATURES

- Eight-Bit Parallel Processing
- Bi-Directional Data Bus
- Sixteen-Bit Address Bus – 65536 Bytes of Addressing
- 72 Instructions – Variable Length
- Seven Addressing Modes – Direct, Relative, Immediate, Indexed, Extended, Implied and Accumulator
- Variable Length Stack
- Vectored Restart
- 2 Microsecond Instruction Execution
- Maskable Interrupt Vector
- Separate Non-Maskable Interrupt – Internal Registers Saved in Stack
- Six Internal Registers – Two Accumulators, Index Register, Program Counter, Stack Pointer and Condition Code Register
- Direct Memory Access (DMA) and Multiple Processor Capability
- Clock Rates – S6800 – 1.0 MHz
  S68A00 – 1.5 MHz
  S68B00 – 2.0 MHz
- Simple Bus Interface Without TTL
- Halt and Single Instruction Execution Capability

ADVANCED PRODUCT DESCRIPTION

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ABSOLUTE MAXIMUM RATINGS

Supply Voltage V_{CC}		Operating Temperature Range T_A	0°C to + 70°C
Input Voltage V_{IN}	- 0.3 to + 7.0V	Industrial Temperature Range	-40°C to +85°C
		Military Temperature Range	-55°C to +125°C
		Storage Temperature Range T_{stg}	- 55°C to + 150°C

ELECTRICAL CHARACTERISTICS

(V_{CC} = 5.0V, ± 5%, V_{SS} = 0, T_A unless otherwise noted.)

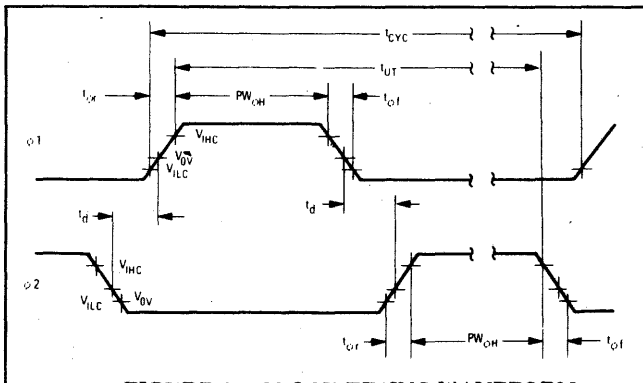
SYMBOL	CHARACTERISTICS		MIN	TYP	MAX	UNIT
V_{IH} V_{IHC}	Input High Voltage (Normal Operating Levels)	Logic $\phi1, \phi2$	V_{SS} + 2.0 V_{CC} - 0.6	– –	V_{CC} V_{CC} + 0.3	Vdc
V_{IL} V_{ILC}	Input Low Voltage (Normal Operating Levels)	Logic $\phi1, \phi2$	V_{SS} - 0.3 V_{SS} - 0.3	– –	V_{SS} + 0.8 V_{SS} + 0.4	Vdc
I_{IN}	Input Leakage Current (V_{IN} = 0 to 5.25V, V_{CC} = Max) (V_{IN} = 0 to 5.25V, V_{CC} = 0.0V)	 Logic* $\phi1, \phi2$	 – –	 1.0 –	 2.5 100	µAdc
I_{TSI}	Three-State (Off State) Input Current V_{IN} = 0.4 to 2.4V, V_{CC} = Max	D0 – D7 A0 – A15, R/W	– –	2.0 –	10 100	µAdc
V_{OH}	Output High Voltage (I_{LOAD} = - 205µAdc, V_{CC} = Min) (I_{LOAD} = - 145µAdc, V_{CC} = Min) (I_{LOAD} = - 100µAdc, V_{CC} = Min)	 D0 – D7 A0 – A15, R/W, VMA BA	 V_{SS} + 2.4 V_{SS} + 2.4 V_{SS} + 2.4	 – –	 – –	Vdc
V_{OL}	Output Low Voltage (I_{LOAD} = 1.6mAdc, V_{CC} = Min)		–	–	V_{SS} + 0.4	Vdc
P_D	Power Dissipation		–	0.5	1.0	W
C_{IN}	Capacitance # (V_{IN} = 0, T_A = 25°C, f = 1.0 MHz)	 $\phi1$ $\phi2$ D0 – D7 Logic Inputs	 – – – –	 – – 10 6.5	 35 70 12.5 10	pF
C_{OUT}		A0 – A15, R/W, VMA	–	–	12	pF
f	Frequency of Operation	S68A00 S68B00	0.1 0.1	 –	1.5 2.0	MHz
t_{CYC}	Clock Timing (Figure 1) Cycle Time	S68A00 S68B00	0.666 0.50	– –	10 10	µs
$PW_{\phi H}$	Clock Pulse Width Measured at V_{CC} - 0.6V	$\phi1, \phi2$ – S68A00 $\phi1, \phi2$ – S68B00	230 180	– –	9500 9500	ns
t_{UT}	Total $\phi1$ and $\phi2$ Up Time	S68A00 S68B00	600 440	– –	– –	ns
$t_{\phi r}, t_{\phi f}$	Measured between V_{SS} + 0.4 and V_{CC} - 0.6	Rise and Fall Times	5.0	–	100	ns
t_d	Measured at V_{OV} = V_{SS} + 0.6V	Delay Time or Clock separation	0	–	9100	ns

Except $\overline{IRQ}$ and $\overline{NMI}$, which require KΩ pullup load resistor for wire-OR capability at optimum operation.
#Capacitances are periodically sampled rather than 100% tested.

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READ/WRITE TIMING

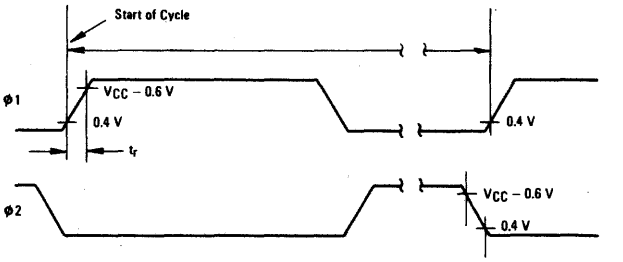
Symbol	Parameter	S6800			S68A00			S68B00			Units
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
t_{AD}	Address Delay										ns
	C = 90pF		100	300			180			150	
	C = 30pF						165			135	
t_{ACC}	Peripheral Read Access Time $t_{AC} = t_{UT} - (t_{AD} + t_{DSR})$			575			360			250	ns
t_{DSR}	Data Setup Time (Read)	100			60			40			ns
t_H	Input Data Hold Time	10	30		10			10			ns
t_H	Output Data Hold Time	10	25		10	25		10	25		ns
t_{AH}	Address Hold Time (Address, R/W, VMA)				10	75		10	75		ns
t_{EH}	Enable High Time for DBE Input	470			280			220			ns
t_{DDW}	Data Delay Time (Write)					165	200			160	ns
	Processor Controls										
t_{PCS}	Processor Control Setup Time			200	200			200			ns
t_{PC_r}; t_{PC_f}	Processor Control Rise and Fall Time						100			100	ns
t_{BA}	Bus Available Delay						270			270	ns
t_{TSE}	Three-State Enable						40			40	ns
t_{TSD}	Three-State Delay						270			270	ns
$t_{\overline{DBE}}$	Data Bus Enable Down Time During $\phi 1$ Up Time				150			70			ns
t_{DBE_r}, t_{DBE_f}	Data Bus Enable Rise and Fall Times						25			25	ns



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FIGURE 1 CLOCK TIMING WAVEFORM

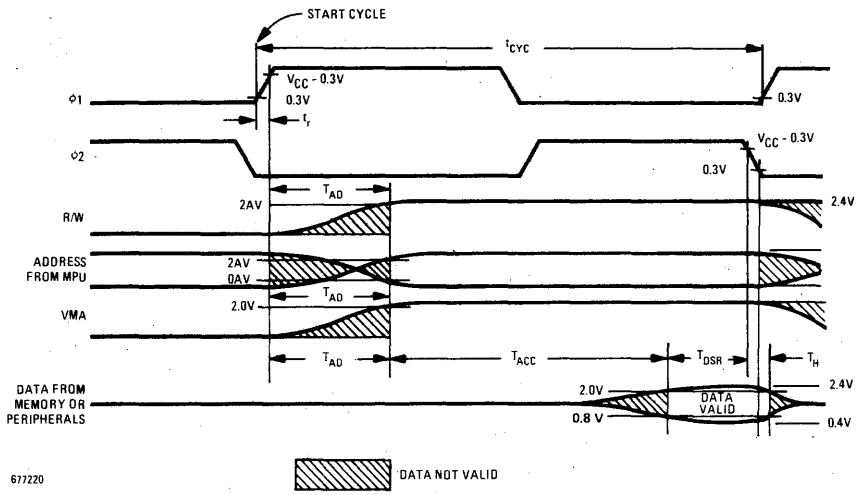
Measurement point for $\phi 1$ and $\phi 2$ are shown below.
Other measurements are the same as for MC6800.



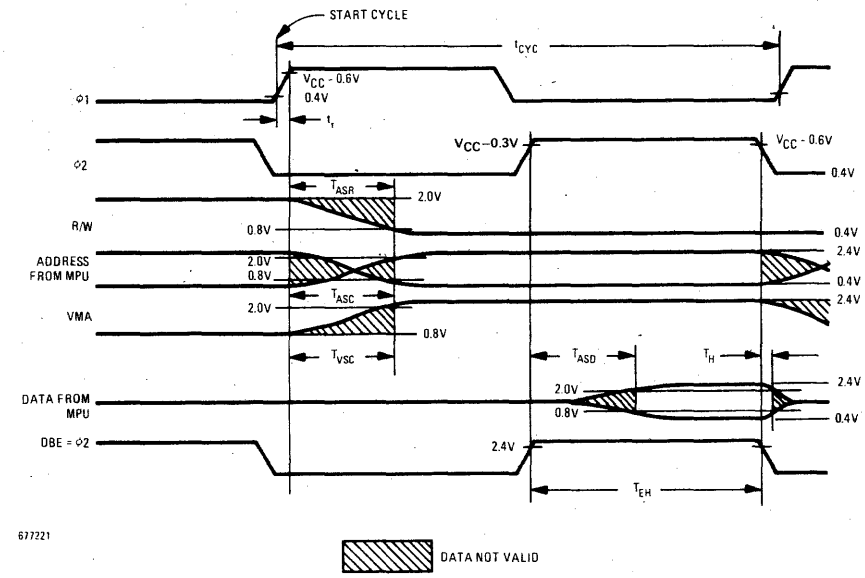
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FIGURE 2 READ/WRITE TIMING WAVEFORM

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READ DATA FROM MEMORY OR PERIPHERALS



WRITE DATA IN MEMORY OR PERIPHERALS

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MICROCOMPUTER UNIT (MCU)*

Features

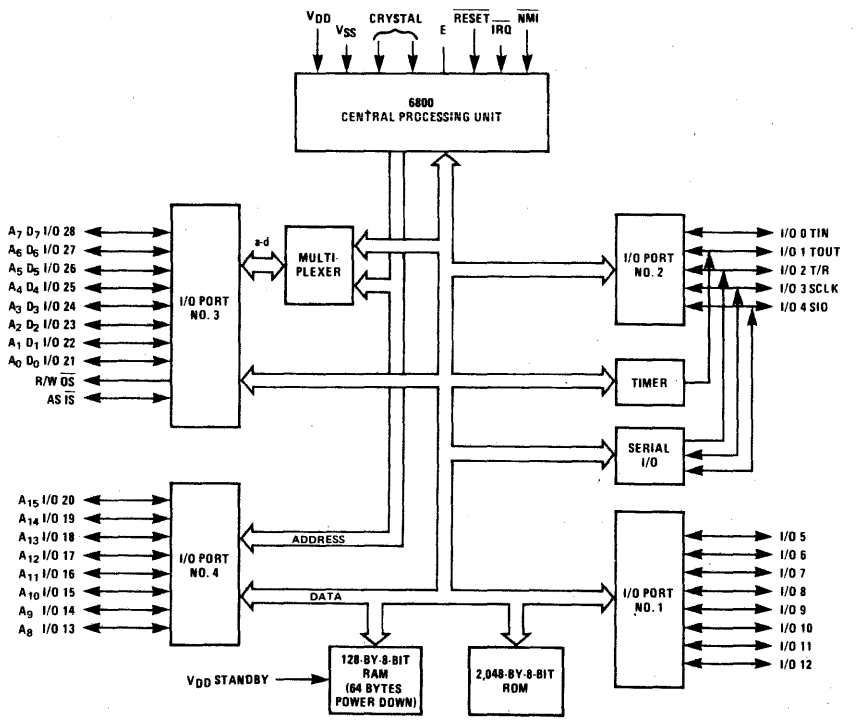
- Expanded S6800 instruction set
- Object code compatible with S6800
- Single chip or expandable to 65K words.
- 2K bytes of ROM
- 128 bytes of RAM (64 bytes retainable)
- 31 parallel I/O lines
- Internal Clock/Divide-by-Four mask option (S6801)
- External Clock/Divide-by-One mask option (S6801E)
- TTL compatible inputs and outputs
- Interrupt capability
- Hardware Multiply

General Description

The S6801 MCU is an 8-bit microcomputer system which is expandable, using the S6800 microprocessor family. The S6801 MCU is object code compatible with the S6800 instruction set with improved execution times of key instructions plus several new 16-bit and 8-bit instructions. The S6801 MCU can operate single chip or be expanded to 65K words. The S6801 MCU is TTL compatible and requires one + 5.0 volt power supply. The S6801 MCU has 2K bytes of ROM and 128 bytes of RAM on board. In addition, the S6801 MCU has on board serial and parallel I/O and three 16 stage timer function.

*Available 1st Quarter 1979

Block Diagram



ADVANCED PRODUCT DESCRIPTION

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MICROPROCESSOR WITH CLOCK AND RAM

Features

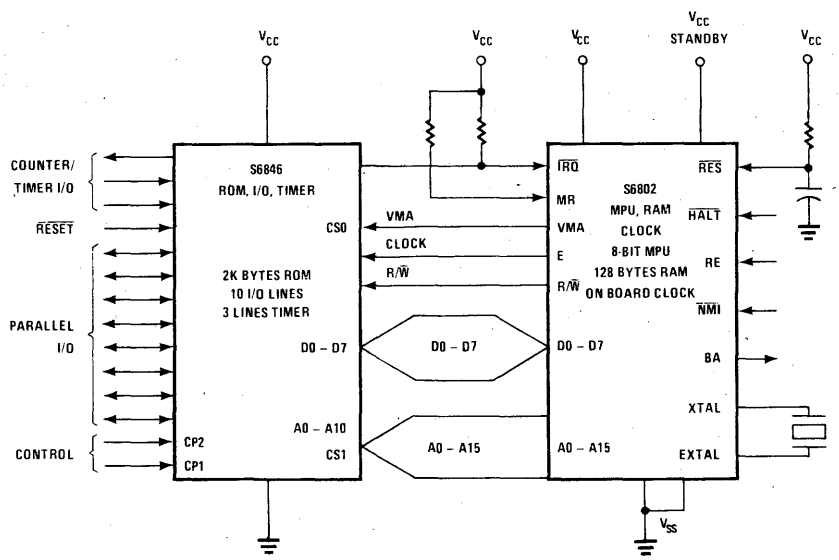
- ☐ On-Chip Clock Circuit
- ☐ 128 x 8 Bit On-Chip RAM
- ☐ 32 Bytes of RAM Are Retainable
- ☐ Software-Compatible with the S6800
- ☐ Expandable to 65K Words
- ☐ Standard TTL-Compatible Inputs and Outputs
- ☐ 8-Bit Word Size
- ☐ 16-Bit Memory Addressing
- ☐ Interrupt Capability

General Description

The S6802 is a monolithic 8-bit microprocessor that contains all the registers and accumulators of the present S6800 plus an internal clock oscillator and driver on the same chip. In addition, the S6802 has 128 bytes of RAM on board located at hex addresses 0000 to 007F. The first 32 bytes of RAM, at hex addresses 0000 to 001F, may be retained in a low power mode by utilizing V_{CC} standby, thus facilitating memory retention during a power-down situation.

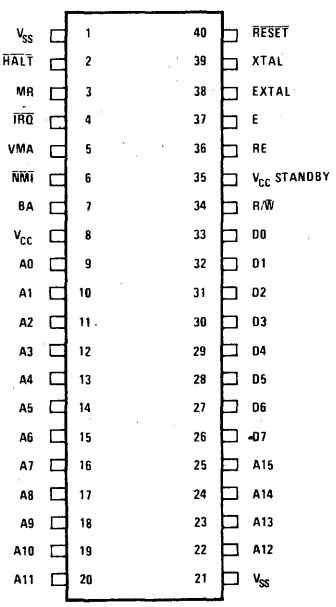
The S6802 is completely software compatible with the S6800 as well as the entire S6800 family of parts. Hence, the S6802 is expandable to 65K words. When the S6802 is interfaced with the S6846 ROM — I/O — Timer chip, as shown in the Block Diagram below, a basic 2-chip microcomputer system is realized.

Typical Microcomputer Block Diagram



BLOCK DIAGRAM OF A TYPICAL COST EFFECTIVE MICROCOMPUTER. THE MPU IS THE CENTER OF THE MICROCOMPUTER SYSTEM AND IS SHOWN IN A MINIMUM SYSTEM INTERFACING WITH A ROM COMBINATION CHIP. IT IS NOT INTENDED THAT THIS SYSTEM BE LIMITED TO THIS FUNCTION BUT THAT IT BE EXPANDABLE WITH OTHER PARTS IN THE S6800 MICROCOMPUTER FAMILY.

Pin Configuration



This is advance information and specifications are subject to change without notice

ADVANCED PRODUCT DESCRIPTION

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Absolute Maximum Ratings

Supply Voltage	-0.3V to + 7.0V
Input Voltage	-0.3V to + 7.0V
Operating Temperature Range	0°C to + 70°C
Storage Temperature Range	-55°C to + 150°C
Thermal Resistance	70°C/W

*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. Electrical Characteristics (V_{CC} = 5.0V ± 5%, V_{SS} = 0, T_A = 0°C to +70°C unless otherwise noted.)

Symbol	Parameter		Min.	Typ.	Max.	Unit
V_{IH}	Input High Voltage	Logic, EXtal	V_{SS} +2.0	—	V_{CC}	V
		$\overline{Reset}$	V_{SS} +4.0	—	V_{CC}	
V_{IL}	Input Leakage Voltage	Logic, EXtal, $\overline{Reset}$	V_{SS} -0.3	—	V_{SS} + 0.8	V
I_{IN}	Input Leakage Current (V_{IN} = 0 to 5.25V, V_{CC} = Max)	Logic*	—	1.0	2.5	μA
V_{OH}	Output High Voltage					V
	(I_{LOAD} = -205μA, V_{CC} = Min)	D0 — D7	V_{SS} +2.4	—	—	V
	(I_{LOAD} = -145μA, V_{CC} = Min)	A0—A15, R/$\overline{W}$, VMA,E	V_{SS} +2.4	—	—	V
	(I_{LOAD} = -100μA, V_{CC} = Min)	BA	V_{SS} +2.4	—	—	V
V_{OL}	Output Low Voltage (I_{LOAD} = 1.6mA, V_{CC} = Min)		—	—	V_{SS} + 0.4	V
P_D**	Power Dissipation		—	0.600	1.2	W
C_{IN}	Capacitance #					pF
	(V_{IN} = 0, T_A=25°C, f=1.0MHz	D0 — D7	—	10	12.5	
		Logic Inputs, EXtal	—	6.5	10	
C_{OUT}		A0 — A15, R/$\overline{W}$, VMA	—	—	12	pF

Clock Timing (V_{CC} = 5.0V ± 5%, V_{SS} = 0, T_A = 0°C to +70°C unless otherwise noted)

Symbol	Parameter		Min.	Typ.	Max.	Unit
f	Frequency of Operation	Input Clock÷4	0.1	—	1.0	MHz
f_{Xtal}		Crystal Frequency	1.0	—	4.0	
t_{CYC}	Cycle Time		1.0	—	10	μs
$PW_{\phi Hs}$	Clock Pulse Width		450	—	4500	ns
$PW_{\phi L}$	Measured at 2.4V					
t_ϕ	Fall Time		—	—	25	ns
	Measured between V_{SS} + 0.4V and V_{SS} -2.4V					

*Except $\overline{IRQ}$ and $\overline{NMI}$, which require 3KΩ pullup load resistors for wire-OR capability at optimum operation. Does not include EXtal and Xtal, which are crystal inputs.
**In power-down mode, maximum power dissipation is less than 40mW.
#Capacitances are periodically sampled rather than 100% tested.

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Read/Write Timing (Figures 1 through 5; Load Circuit of Figure 3).
(V_{CC} = 5.0V ± 5%, V_{SS} = 0, T_A = 0°C to + 70°C unless otherwise noted.)

Symbol	Parameters	Min.	Typ.	Max.	Unit
t_{AD}	Address Delay	—	—	270	ns
t_{ACC}	Peripheral Read Access Time ($t_{ACC} = t_{ut} - t_{DSR}$)	—	—	530	ns
t_{DSR}	Data Setup Time (Read)	100	—	—	ns
t_H	Input Data Hold Time	10	—	—	ns
t_{AH}	Address Hold Time (Address, R/$\overline{W}$, VMA)	20	—	—	ns
t_{DDW}	Data Delay Time (Write)	—	165	225	ns
	Processor Controls:				
t_{PCS}	Processor Control Setup Time	200	—	—	ns
t_{PCr}, t_{PCf}	Processor Control Rise and Fall Time (Measured between 0.8V and 2.0V)	—	—	100	ns

Figure 1. Read Data From Memory or Peripherals

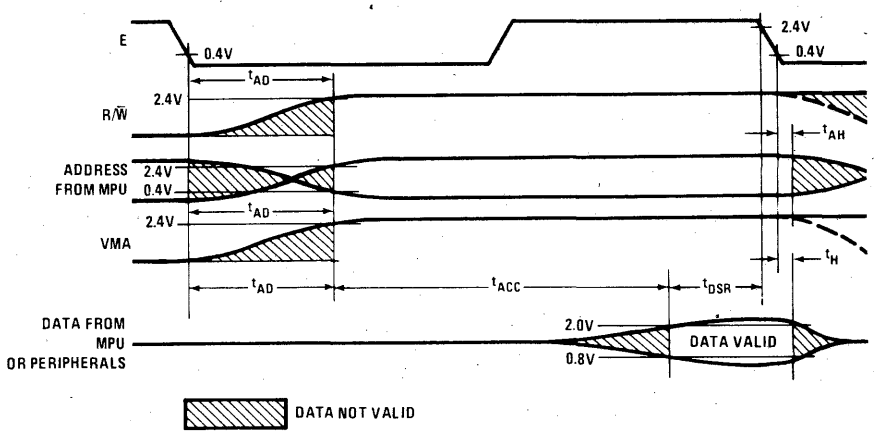


Figure 2. Write Data In Memory or Peripherals

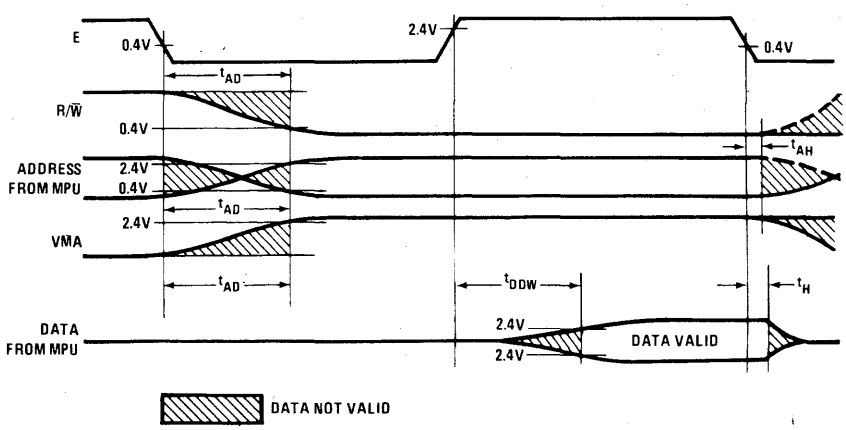
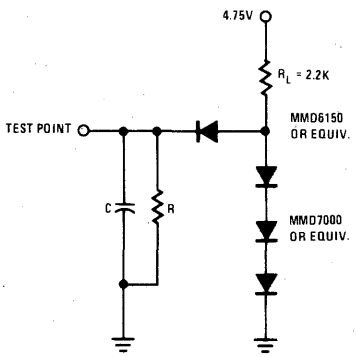


Figure 3. Bus Timing Test Load



C = 130pF FOR D0 – D7, E
= 90pF FOR A0 – A15, R/$\overline{W}$, AND VMA
= 30pF FOR BA
R = 11.7 KΩ FOR D0 – D7, E
= 16.5KΩ FOR A0 – A15, R/$\overline{W}$, AND VMA
= 24KΩ FOR BA

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Figure 4. Typical Data Bus Output Delay Versus Capacitive Loading

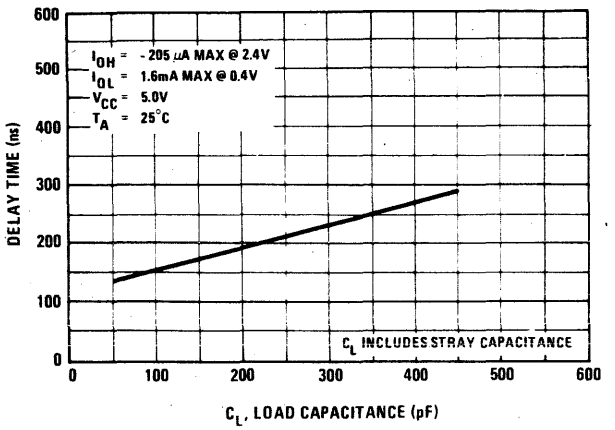


Figure 5. Typical Read/Write, VMA, and Address Output Delay Versus Capacitive Loading

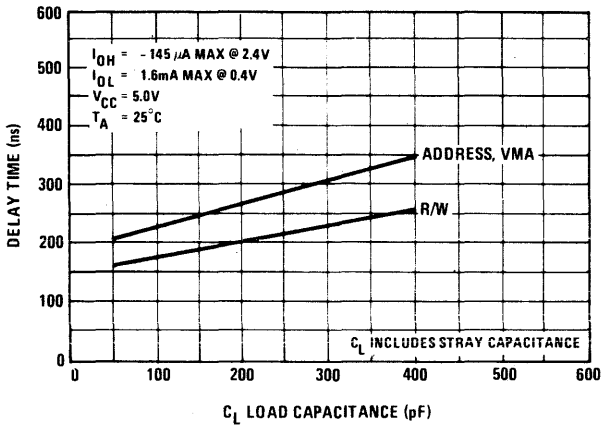
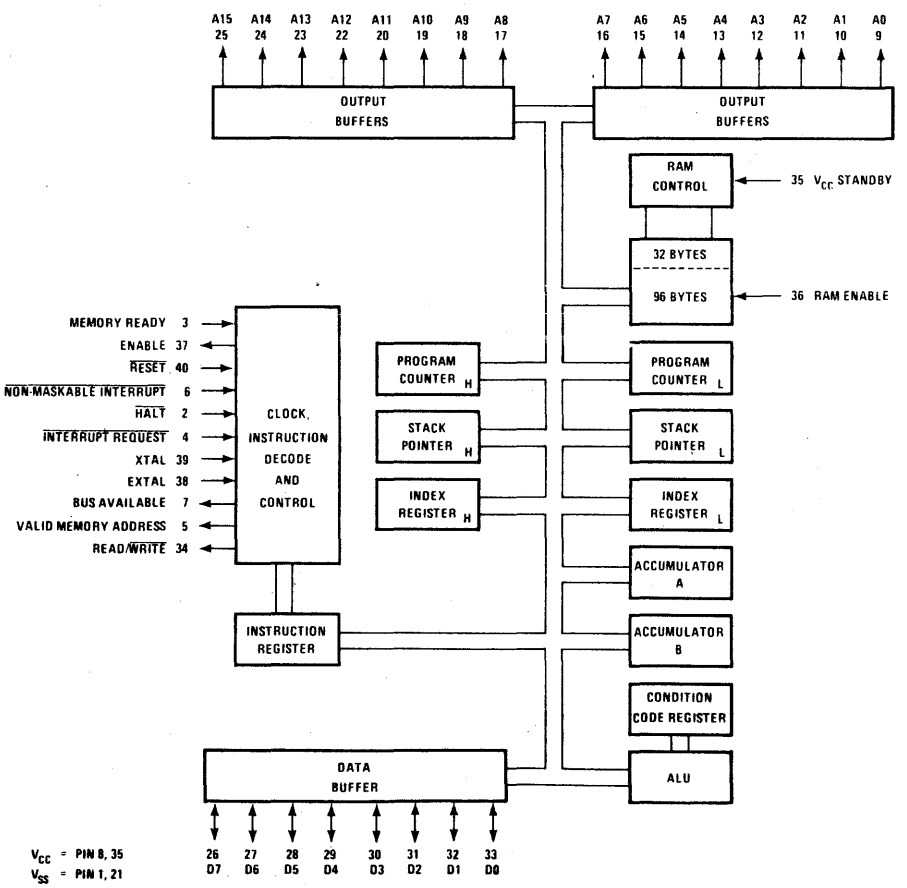


Figure 6. S6802 Expanded Block Diagram



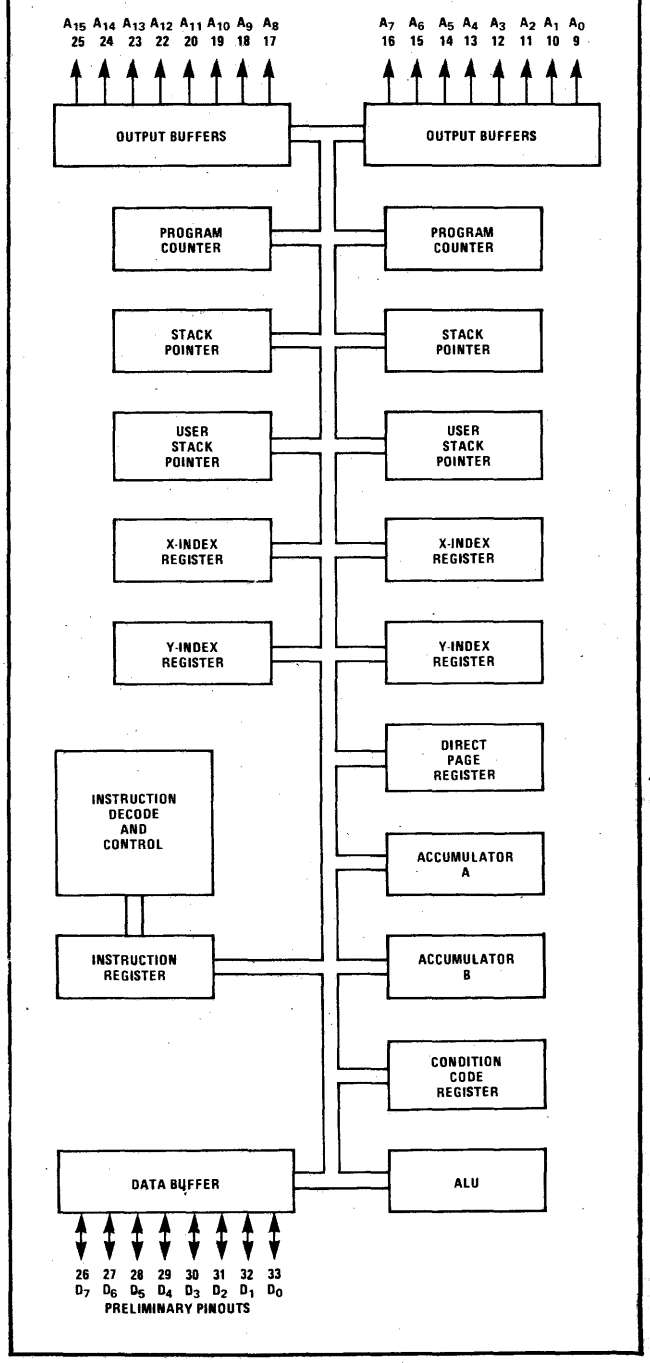
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HIGH PERFORMANCE MICROPROCESSOR*

Features

- Upward source compatible with S6800
- Bus compatible with S6800 family
- 2MHz Bus operation
- Pin-out compatible with S6800/S6802
- On-chip Oscillation/Clock Driver
- TTL compatible I/O
- 3 priority Interrupts
- Fast Interrupt — Cuts Response Time
- Interrupt acknowledge allows vectoring by device
- Memory Ready Signal for slow memory
- +5V Power Supply
- Expandable to 64 K words

Block Diagram



General Description

The S6809 is a monolithic microprocessor that contains all the registers of the S6800 plus an additional clock oscillator and driver on chip.

The S6809 gives the user 8- and 16-bit word capability, while retaining software compatibility with the basic S6800 family. Four 8-bit-wide registers and five 16-bit-wide ones process the data, with the 8-bit accumulators supplying routing computation.

The S6809 is compatible with the complete set of S6800 peripheral and memory devices. It is designed for the middle and high end of the microprocessor scale.

*Available 1st Quarter 1979

ADVANCED PRODUCT DESCRIPTION

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128x8 STATIC READ/WRITE MEMORY

Features

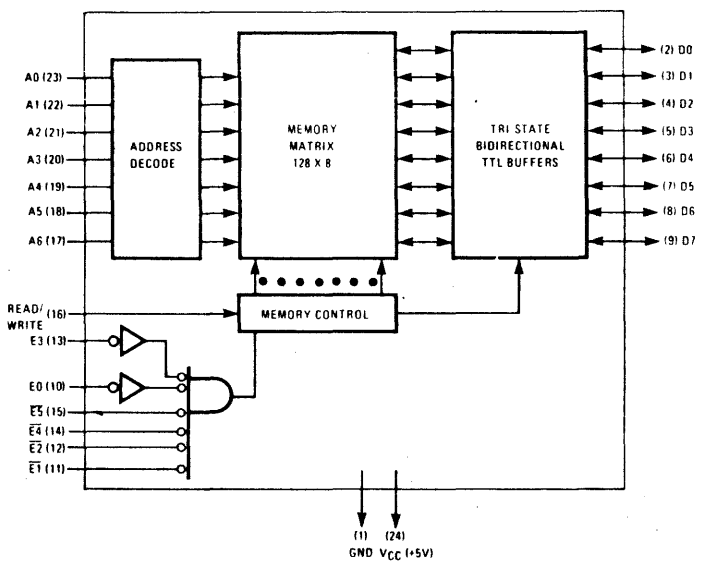
- ☐ Organized as 128 Bytes of 8 Bits
- ☐ Static Operation
- ☐ Bi-Directional Three-State Data Input/Output
- ☐ Six Chip Enable Inputs (Four Active Low, Two Active High)
- ☐ Single 5-Volt Power Supply
- ☐ TTL Compatible
- ☐ Maximum Access Time = 450ns for S6810A 350ns for S6810A – 1

General Description

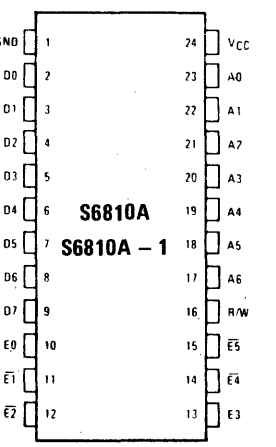
The S6810A is a static 128 x 8 Read/Write Memory designed and organized to be compatible with the S6800 Microprocessor. Interfacing to the S6810A consists of an 8-Bit Bidirectional Data Bus, Seven Address Lines, a single Read/Write Control line, and six Chip Enable lines – four negative and two positive.

For ease of use, the S6810A is a totally static memory requiring no clocks or cell refresh. The S6810A is fabricated with N-channel silicon gate depletion mode technology to be fully DTL/TTL compatible with only a single +5 volt power supply required.

Block Diagram



Pin Configuration



ADVANCED PRODUCT DESCRIPTION

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Absolute Maximum Ratings

NOTES:

1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to RECOMMENDED OPERATING CONDITIONS. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.
2. This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields, however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

Supply Voltage V_{CC}	-0.3 to +7.0V
Input Voltage V_{IN}	-0.3 to +7.0V
Operating Temperature Range T_A	0°C to +70°C
Storage Temperature Range T_{stg}	-55°C to +150°C

DC (Static) Characteristics

V_{CC} = 5.0V ± 5%; T_A = 0°C to +70°C unless otherwise noted

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
V_{IH}	Input High Voltage	2.0	—	5.25	V	
V_{IL}	Input Low Voltage	-0.3	—	0.8	V	
I_{IN}	Input Current (A_n, R/W, E_n, $\overline{E}_n$) (V_{IN} = 0 to 5.25V)	—	—	2.5	μA	
V_{OH}	Output High Voltage (I_{OH} = 205 μA)	2.4	—	—	V	
V_{OL}	Output Low Voltage (I_{OL} = 1.6mA)	—	—	0.4	V	
I_{LIH}	Output Leakage Current (D0 — D7) (V_0 = 2.4V, E = 0.8V, $\overline{E}$ = 2.0V)	—	—	10	μA	
I_{LOL}	Output Leakage Current (D0 — D7) (V_0 = 0.4V, E = 0.8V, $\overline{E}$ = 2.0V)	—	—	10	μA	
I_{CC}	Supply Current (V_{CC} = 5.25V, T_A = 0°C)					
	S6810A	—	—	80	mA	
	S6810A — 1	—	—	80	mA	
C_{IN}	Input Capacitance*	—	—	7.5	pF	f=1.0MHz, T_A=25°C
C_{OUT}	Output Capacitance*	—	—	—	—	f=1.0MHz, T_A=25°C

*This parameter periodically sampled rather than 100% tested.

AC (Dynamic) Characteristics

V_{CC} = 5.0V ± 5%, T_A = 0°C to +70°C

Symbol	Parameter		Min.	Max.	Unit
t_{AS}	Address Setup Time		20	—	ns
t_{AH}	Address Hold Time		0	—	ns
t_{CS}	Chip Enable Pulse Width	S6810A	230	—	ns
		S6810A — 1	180	—	ns

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Read Cycle

(All timing with low input pulse 0.8V, high input pulse 2.0V, $t_r = t_f = 20$ns, Load of Figure 1)

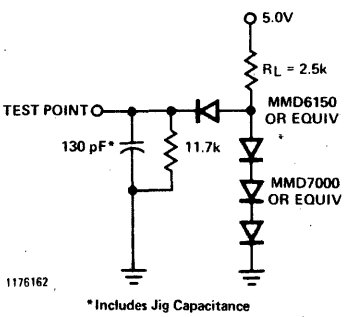
Symbol	Parameter		Min.	Max.	Unit
$t_{CYC\ (R)}$	Read Cycle Time	S6810A	450	—	ns
		S6810A – 1	350	—	ns
t_{DD}	Output Disable Delay Time	S6810A	10	—	ns
		S6810A – 1	10	—	ns
t_{ACC}	Read Access Time	S6810A	—	450	ns
		S6810A – 1	—	350	ns
t_{RCS}	Read to Select Delay Time	S6810A	0	—	ns
		S6810A – 1	0	—	ns

Write Cycle

(All timing with low input pulse 0.80, high input pulse 2.0V, $t_r = t_f = 20$ns, Load of Figure 1)

Symbol	Parameter		Min.	Max.	Unit
$t_{CYC\ (W)}$	Write Cycle Time	S6810A	450	—	ns
		S6810A – 1	350	—	ns
t_{WP}	Write Pulse Width	S6810A	300	—	ns
		S6810A – 1	250	—	ns
t_{DS}	Data Setup Time	S6810A	190	—	ns
		S6810A – 1	150	—	ns
t_{WCS}	Write to Select Delay Time	S6810A	0	—	ns
		S6810A – 1	0	—	ns

Figure 1. AC Test Load



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Timing Characteristics

Figure 2. Read Cycle Timing

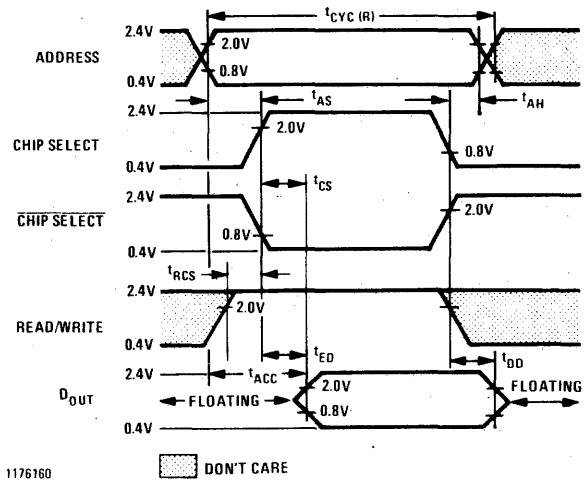
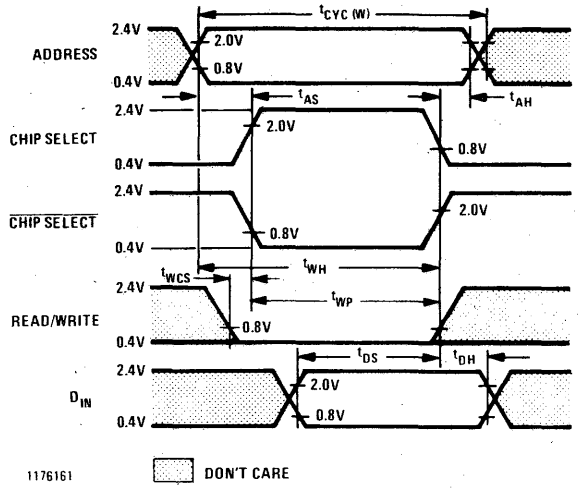
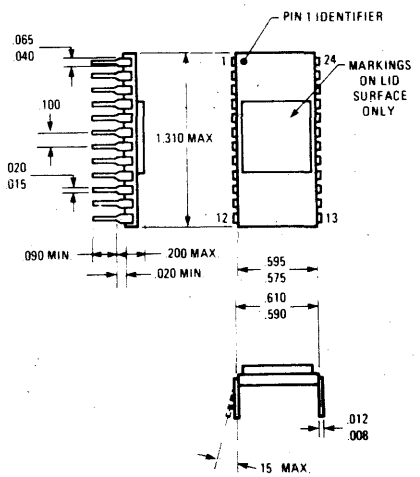


Figure 3. Write Cycle Timing



Physical Dimensions



Ordering Information

Order No.	No. Pins	Package	Temp. Range	Description
S6810AP	40	Plastic	0 — 70°C	NMOS 128 x 8 Static RAM, T_{AA}=450ns Max
S6810A	24	Ceramic	0 — 70°C	NMOS 128 x 8 Static RAM, T_{AA}=450ns Max
S6810A-1P	24	Plastic	0 — 70°C	NMOS 128 x 8 Static RAM, T_{AA}=350ns Max
S6810A-1	24	Ceramic	0 — 70°C	NMOS 128 x 8 Static RAM, T_{AA}=350ns Max

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128 × 8 STATIC READ/WRITE MEMORY

Features

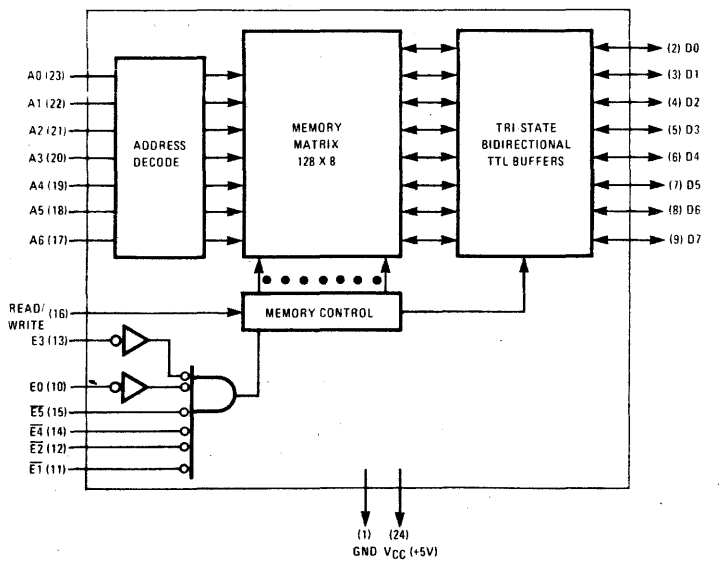
- Organized as 128 Bytes of 8 Bits
- Static Operation
- Bidirectional Three-State Data Input/Output
- Six Chip Enable Inputs (Four Active Low, Two Active High)
- Single 5 Volt Power Supply
- TTL Compatible
- Maximum Access Time:
  —360ns for S68A10
  —250ns for S68B10

General Description

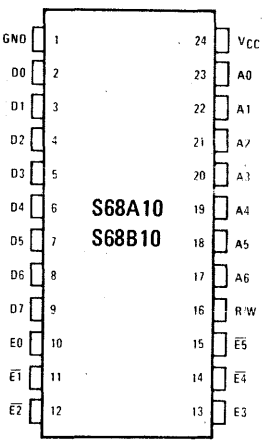
The S68A10 and S68B10 are static 128x8 Read/Write Memories designed and organized to be compatible with the S68A00 and S68B00 Microprocessors. Interfacing to the S68A10 and S68B10 consists of an 8-bit bidirectional data bus, seven address lines, a single Read/Write control line, and six chip enable lines, four negative and two positive.

For ease of use, the S68A10 and S68B10 are a totally static memory requiring no clocks or cell refresh. The S68A10 and S68B10 are fabricated with N-channel silicon gate depletion load technology to be fully DTL/TTL compatible with only a single +5 volt power supply required.

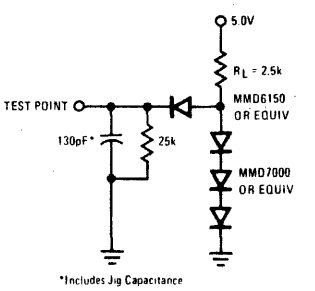
Block Diagram



Pin Configuration



AC Test Load



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Absolute Maximum Ratings

Supply Voltage	-0.3V to +7.0V
Input Voltage	-0.3V to +7.0V
Operating Temperature Range	0°C to +70°C
Industrial Temperature Range	-40°C to +85°C
Military Temperature Range	-55°C to +125°C
Storage Temperature Range	-55°C to +150°C

DC Characteristics (V_{CC} = +5.0V ±5%, V_{SS} = 0, T_A = 0°C to +70°C unless otherwise noted.)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
I_{IN}	Input Current (A_n, R/W, CS_n, $\overline{CS}_n$)			2.5	μAdc	V_{IN} = 0V to 5.25V
V_{OR}	Output High Voltage	2.4			Vdc	I_{OH} = -205μA
V_{OL}	Output Low Voltage			0.4	Vdc	I_{OL} = 1.0mA
I_{LO}	Output Leakage Current (Three-State)			10	μAdc	CS = 0.8V or $\overline{CS}$ = 2.0V, V_{OUT} = 0.4V to 2.4V
I_{CC}	Supply Current			80	mAdc	V_{CC} = 5.25V, all other pins grounded, T_A = 0°C

AC Characteristics

Read Cycle (V_{CC} = +5.0V ±5%, V_{SS} = 0, T_A = 0°C to +70°C unless otherwise noted.)

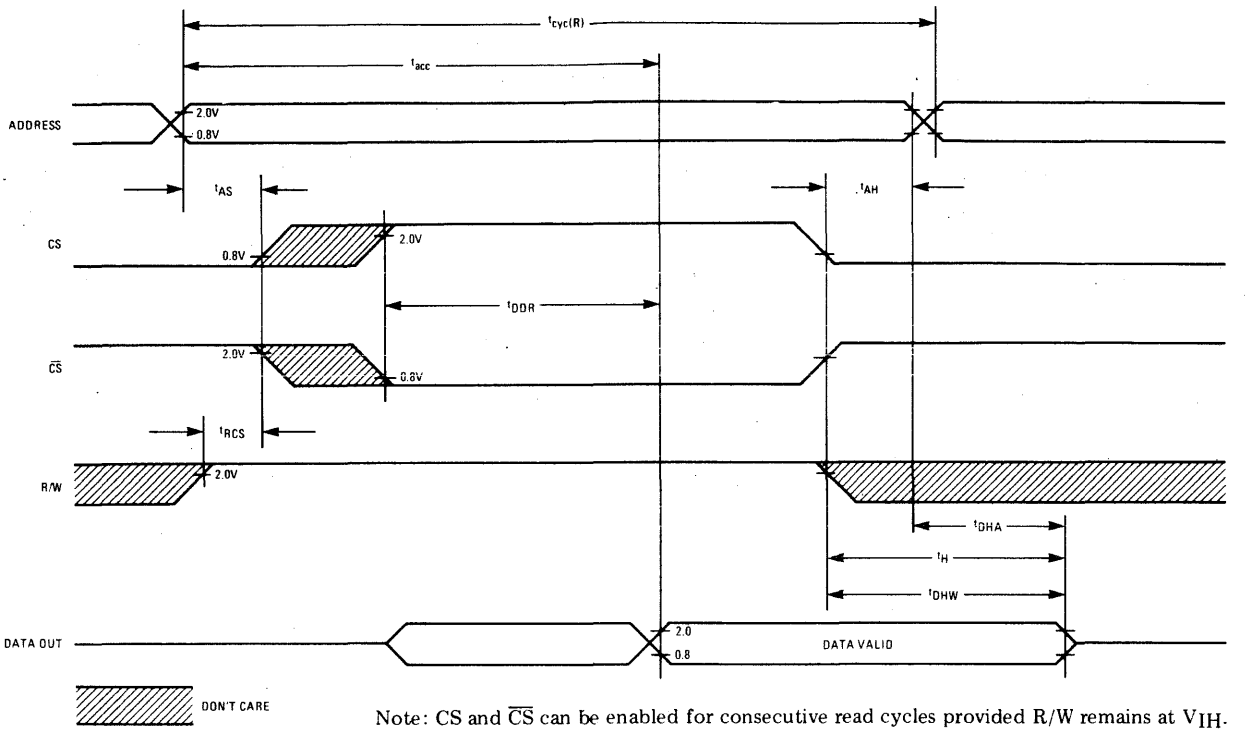
		S68A10		S68B10		
Symbol	Parameter	Min.	Max.	Min.	Max.	Units
$t_{cyc(R)}$	Read Cycle Time	360		250		ns
t_{acc}	Access Time		360		250	ns
t_{AS}	Address Setup Time	20		20		ns
t_{AH}	Address Hold Time	0		0		ns
t_{DDR}	Data Delay Time (Read)		220		180	ns
t_{RCS}	Read to Select Delay Time	0		0		ns
t_{DHA}	Data Hold from Address	10		10		ns
t_H	Output Hold Time	10		10		ns
t_{DHW}	Data Hold from Write	10	60	10	60	ns

Write Cycle (V_{CC} = +5.0V ±5%, V_{SS} = 0, T_A = 0°C to +70°C unless otherwise noted.)

		S68A10		S68B10		
Symbol	Parameter	Min.	Max.	Min.	Max.	Units
$t_{cyc(W)}$	Write Cycle Time	360		250		ns
t_{AS}	Address Setup Time	20		20		ns
t_{AH}	Address Hold Time	0		0		ns
t_{CS}	Chip Select Pulse Width	250		210		ns
t_{WCS}	Write to Chip Select Delay Time	0		0		ns
t_{DSW}	Data Setup Time (Write)	80		60		ns
t_H	Input Hold Time	10		10		ns

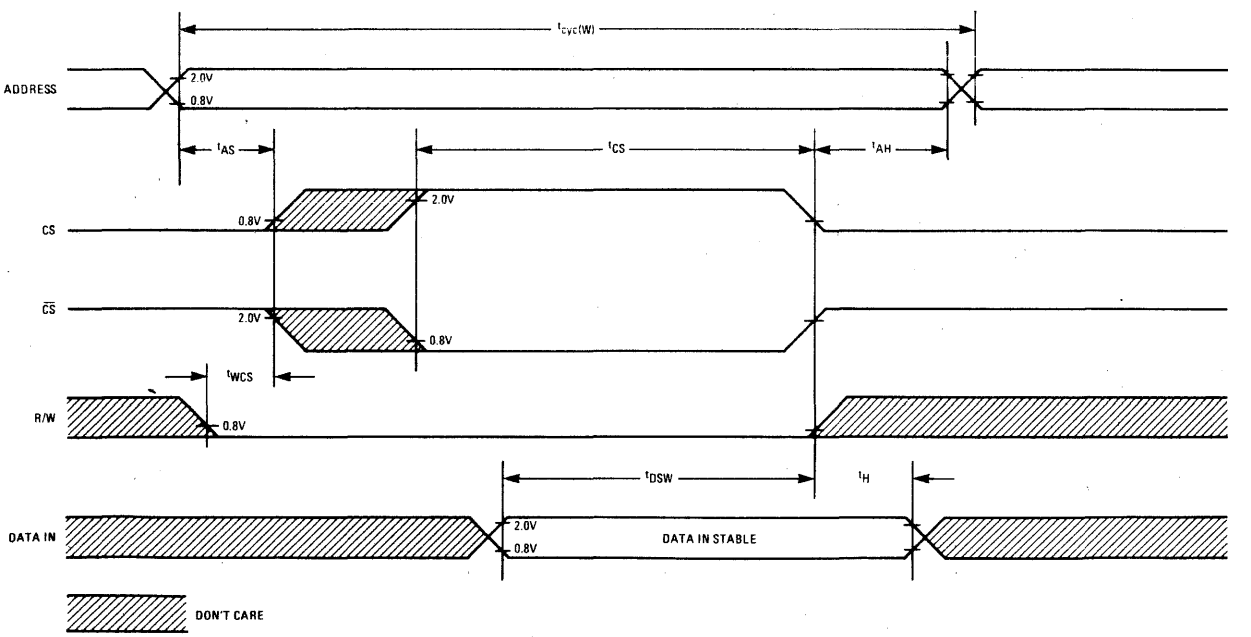
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Read Cycle Timing



Note: CS and $\overline{CS}$ can be enabled for consecutive read cycles provided R/W remains at V_{IH}.

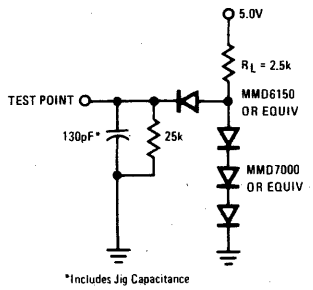
Write Cycle Timing



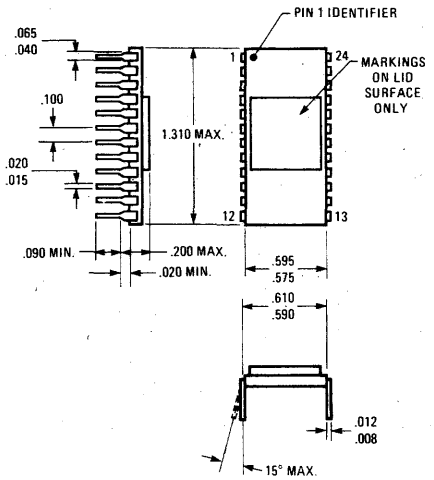
Note: CS and $\overline{CS}$ can be enabled for consecutive write cycles provided R/W is strobed to V_{IH} before or coincident with the Address change, and remains high for time t_{AS}.

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AC Test Load



Physical Dimensions



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Peripheral Interface Adapter (PIA)

Features

- 8-Bit Bidirectional Data Bus for Communication with the MPU
- Two Bidirectional 8-Bit Buses for Interface to Peripherals
- Two Programmable Control Registers
- Two Programmable Data Direction Registers
- Four Individually-Controlled Interrupt Input Lines: Two Usable as Peripheral Control Outputs
- Handshake Control Logic for Input and Output Peripheral Operation
- High-Impedance Three-State and Direct Transistor Drive Peripheral Lines
- Program Controlled Interrupt and Interrupt Disable Capability
- CMOS Compatible Peripheral Lines

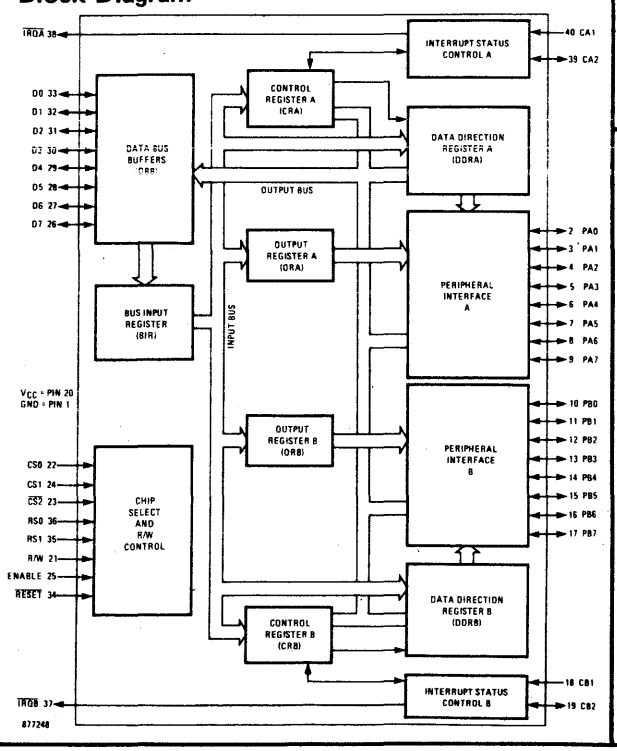
General Description

The S68A21/S68B21 are peripheral Interface Adapters that provide the universal means of interfacing peripheral equipment to the S68A00 and the S68B00 Microprocessing Units (MPU). This device is capable of interfacing the MPU to peripherals through two 8-bit bidirectional peripheral data buses and four control lines. No external logic is required for interfacing to most peripheral devices.

The functional configuration of the PIA is programmed by the MPU during system initialization. Each of the peripheral data lines can be programmed to act as an input or output, and each of the four control/interrupt lines may be programmed for one of several control modes. This allows a high degree of flexibility in the overall operation of the interface.

The PIA interfaces to the S68A00/S68B00 MPUs with an eight-bit bidirectional data bus, three chip select lines, two register select lines, two interrupt request lines, read/write line, enable line and reset line. These signals, in conjunction with the S68A00/S68B00 VMA output, permit the MPU to have complete control over the PIA. VMA may be utilized to gate the input signals to the PIA.

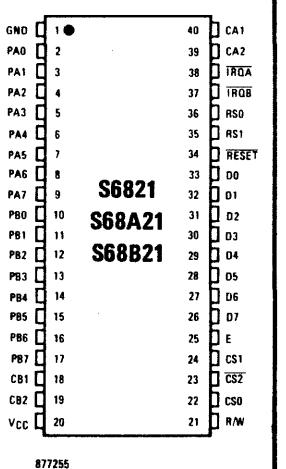
Block Diagram



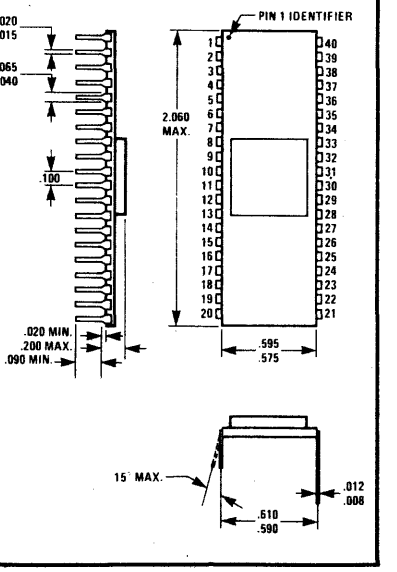
Absolute Maximum Ratings

Supply Voltage	-0.3V to +7.0V
Input Voltage	-0.3V to +7.0V
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	-55°C to +150°C

Pin Configuration



Physical Dimensions



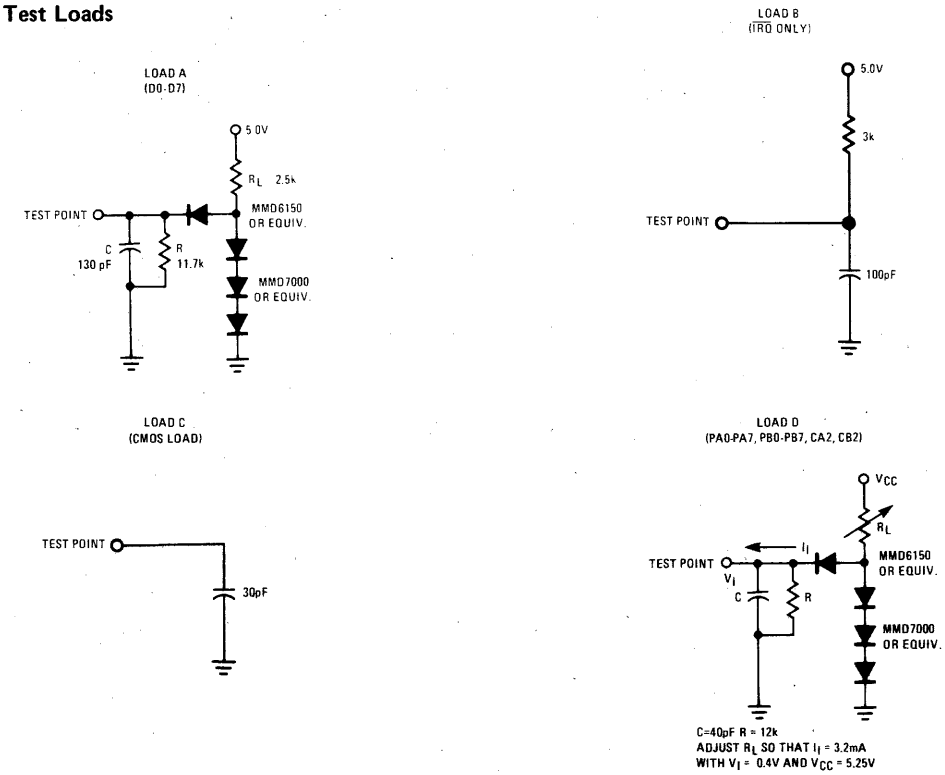
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Electrical Characteristics (V_{CC} = +5.0V ±5%, V_{SS} = 0, T_A = 0°C to +70°C unless otherwise noted.)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
V_{IH}	Input High Voltage	V_{SS}+2.0		V_{CC}	Vdc	
V_{IL}	Input Low Voltage	V_{SS}- 0.3		V_{SS}+0.8	Vdc	
I_{in}	Input Leakage Current R/W, $\overline{Reset}$, RS0, RS1, CS0, $\overline{CS2}$, CS1, CA1, CB1, Enable		1.0	2.5	μAdc	V_{in} = 0Vdc to +5.25Vdc
I_{TSI}	Three-State (Off State) Input Current D0-D7, PB0-PB7, CB2		2.0	10	μAdc	V_{in} = 0.4Vdc to 2.4Vdc
I_{IH}	Input High Current PA0-PA7, CA2	- 200	- 400		μAdc	V_{IH} = 2.4Vdc
I_{IL}	Input Low Current PA0-PA7, CA2		- 1.3	- 2.4	mAdc	V_{IL} = 0.4Vdc
V_{OH}	Output High Voltage					
	D0-D7	V_{SS}+2.4			Vdc	I_{Load} = - 205μAdc
	Other Outputs	V_{SS}+2.4			Vdc	I_{Load} = - 200μAdc
V_{OL}	Output Low Voltage					
	D0-D7			V_{SS}+0.4	Vdc	I_{Load} = 1.6mAdc
	Other Outputs			V_{SS}+0.4	Vdc	I_{Load} = 3.2mAdc
I_{OH}	Output High Current (Sourcing)					
	D0-D7	- 205			μAdc	V_{OH} = 2.4Vdc
	Other Outputs	- 100			μAdc	
	PB0-PB7, CB2	- 1.0	- 2.5	- 10	mAdc	V_O = 1.5Vdc, the current for driving other than TTL, e.g., Darlington Base
I_{LOH}	Output Leakage Current (Off State) $\overline{IRQA}$, $\overline{IRQB}$		1.0	10	μAdc	V_{OH} = 2.4Vdc
P_D	Power Dissipation			550	mW	
C_{in}	Capacitance					
	D0-D7			12.5	pF	V_{in} = 0, T_A = +25°C,
	PA0-PA7, PB0-PB7, CA2, CB2			10	pF	f = 1.0MHz
	Enable, R/W, $\overline{Reset}$, RS0, RS1, CS0, CS1, $\overline{CS2}$, CA1, CB1			7.5	pF	
C_{out}	$\overline{IRQA}$, $\overline{IRQB}$			5.0	pF	

Note: The PA0-PA7 Peripheral Data lines and the CA2 Peripheral Control line can drive two standard TTL loads. In the input mode, the internal pullup resistor on these lines represents a maximum of 1.5 standard TTL loads.

Bus Timing Test Loads



A.C. (Dynamic) Characteristics Loading = 30pF and one TTL load for PA0-PA7, PB0-PB7, CA2, CB2
= 130pF and one TTL load for D0-D7, $\overline{IRQA}$, $\overline{IRQB}$
(V_{CC} = +5.0V ±5%, T_A = 0°C to +70°C unless otherwise noted.)

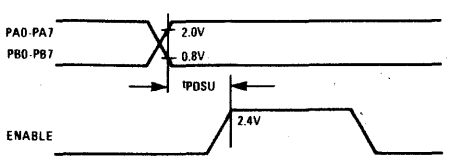
Read Timing Characteristics (Figure 1)

Timing Characteristics (V_{CC} = +5.0V ± 5%, V_{SS} = 0, T_A = 0°C to +70°C unless otherwise noted.)

Symbol	Parameter	S6821		S68A21		S68B21		Units	Conditions
		Min.	Max.	Min.	Max.	Min.	Max.		
t_{PDSU}	Peripheral Data Setup Time	200		135		100		ns	
t_{PDH}	Peripheral Data Hold Time	0		0		0		ns	
t_{CA2}	Delay Time, Enable Negative Transition to CA2 Negative Transition		1.0		0.670		0.5	μs	
t_{RS1}	Delay Time, Enable Negative Transition to CA2 Positive Transition		1.0		0.670		0.5	μs	
t_r, t_f	Rise and Fall Times for CA1 and CA2 Input Signals		1.0		1.0		1.0	μs	
t_{RS2}	Delay Time from CA1 Active Transition to CA2 Positive Transition		2.0		1.35		1.0	μs	
t_{PDW}	Delay Time, Enable Negative Transition to Peripheral Data Valid		1.0		0.670		0.5	μs	
t_{CMOS}	Delay Time, Enable Negative Transition to Peripheral CMOS Data Valid PA0-PA7, CA2		2.0		1.35		1.0	μs	V_{CC} – 30% V_{CC}; Figure 6, Load C
t_{CB2}	Delay Time, Enable Positive Transition to CB2 Negative Transition		1.0		0.670		0.5	μs	
t_{DC}	Delay Time, Peripheral Data Valid to CB2 Negative Transition	20		20		20		ns	
t_{RS1}	Delay Time, Enable Positive Transition to CB2 Positive Transition		1.0		0.670		0.5	μs	
PW_{CT}	Peripheral Control Output Pulse Width, CA2/CB2	550		550		550		ns	
t_r, t_f	Rise and Fall Time for CB1 and CB2 Input Signals		1.0		1.0		1.0	μs	
t_{RS2}	Delay Time, CB1 Active Transition to CB2 Positive Transition		2.0		1.35		1.0	μs	
t_{IR}	Interrupt Release Time, $\overline{IRQA}$ and $\overline{IRQB}$		1.6		1.1		0.85	μs	
t_{RS3}	Interrupt Response Time		1.0		1.0		1.0	μs	
PW_I	Interrupt Input Pulse Width	500		500		500		ns	
t_{RL}	Reset Low Time*	1.0		0.66		0.5		μs	

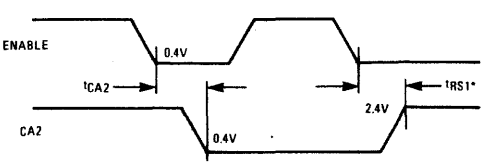
*The Reset line must be high a minimum of 1.0μs before addressing the PIA.

Peripheral Data Setup Time
(Read Mode)



877259

CA2 Delay Time
(Read Mode; CRA-5 = CRA-3 = 1, CRA-4 = 0)



*Assumes part was deselected during the previous E pulse.

877260

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Bus Timing Characteristics (V_{CC} = +5.0V ± 5%, V_{SS} = 0V, T_A = 0°C to +70°C unless otherwise noted.)

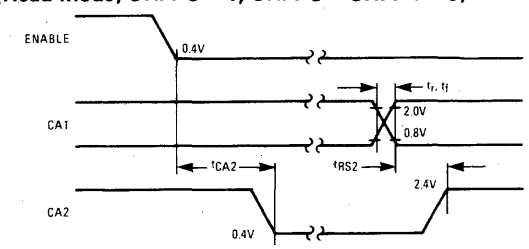
Read

Symbol	Parameter	S6821 Min.	S6821 Max.	S68A21 Min.	S68A21 Max.	S68B21 Min.	S68B21 Max.	Units
t_{cycE}	Enable Cycle Time	1.0		0.666		0.50		μs
PW_{EH}	Enable Pulse Width, High	0.45		0.280		0.22		μs
PW_{EL}	Enable Pulse Width, Low	0.43		0.280		0.21		μs
t_{AS}	Setup Time, Address and R/W Valid to Enable Positive Transition	160		140		70		ns
t_{DDR}	Data Delay Time		320		220		180	ns
t_H	Data Hold Time	10		10		10		ns
t_{AH}	Address Hold Time	10		10		10		ns
t_{Er}, t_{Ef}	Rise and Fall Time for Enable Input		25		25		25	ns

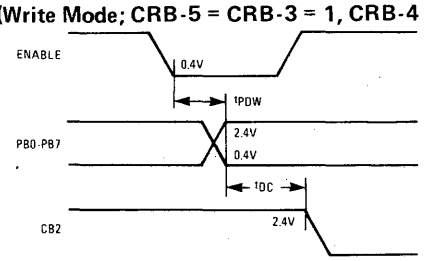
Write

Symbol	Parameter	S6821 Min.	S6821 Max.	S68A21 Min.	S68A21 Max.	S68B21 Min.	S68B21 Max.	Units
t_{cycE}	Enable Cycle Time	1.0		0.666		0.50		μs
PW_{EH}	Enable Pulse Width, High	0.45		0.280		0.22		μs
PW_{EL}	Enable Pulse Width, Low	0.43		0.280		0.21		μs
t_{AS}	Setup Time, Address and R/W Valid to Enable Positive Transition	160		140		70		ns
t_{DSW}	Data Setup Time	195		80		60		ns
t_H	Data Hold Time	10		10		10		ns
t_{AH}	Address Hold Time	10		10		10		ns
t_{Er}, t_{Ef}	Rise and Fall Time for Enable Input		25		25		25	ns

CA2 Delay Time
(Read Mode; CRA-5 = 1, CRA-3 = CRA-4 = 0)

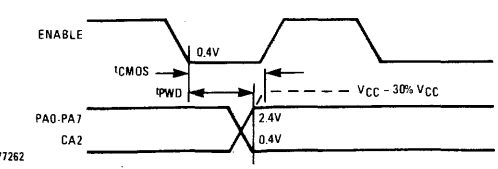


Peripheral Data and CB2 Delay Times
(Write Mode; CRB-5 = CRB-3 = 1, CRB-4 = 0)

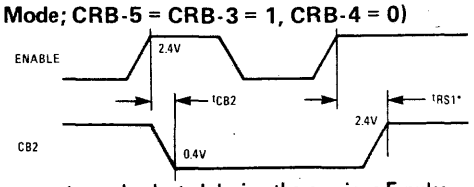


CB2 Note: CB2 goes low as a result of the positive transition of Enable.

Peripheral CMOS Data Delay Times
(Write Mode: CRA-5 = CRA-3 = 1, CRA-4 = 0)



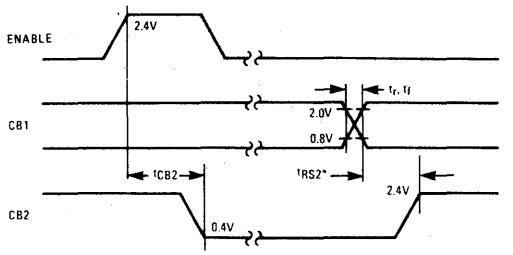
CB2 Delay Time
(Write Mode; CRB-5 = CRB-3 = 1, CRB-4 = 0)



*Assumes part was deselected during the previous E pulse.

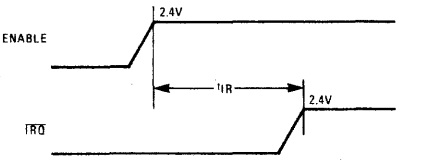
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CB2 Delay Time
(Write Mode; CRB-5 = 1, CRB-3 = CRB-4 = 0)



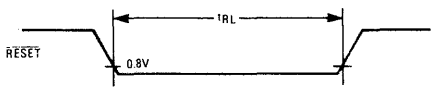
877265 *Assumes part was deselected during any previous E pulse.

$\overline{IRQ}$ Release Time



877266

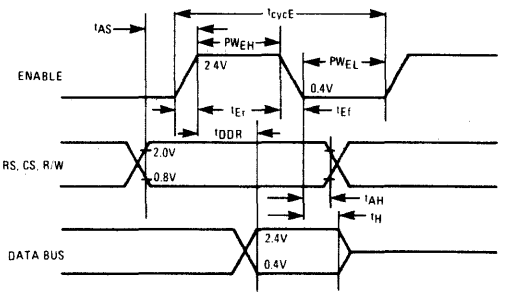
$\overline{RESET}$ Low Time



*The $\overline{Reset}$ line must be a V_{IH} for a minimum of 1.0μs before addressing the PIA.

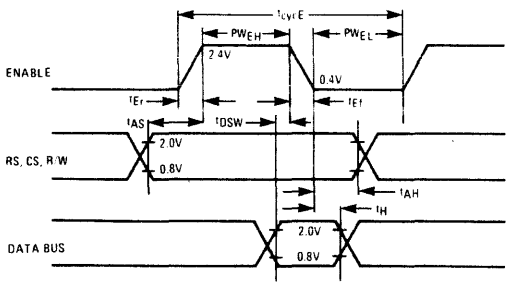
877267

Bus Read Timing Characteristics
(Read Information from PIA)



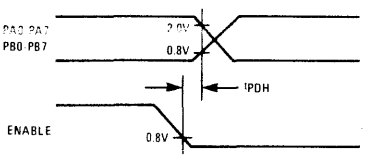
877268

Bus Write Timing Characteristics
(Write Information into PIA)



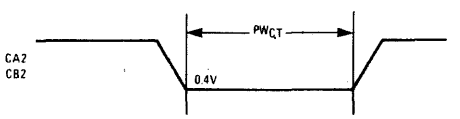
877269

Peripheral Data Hold Time
(Read Mode)



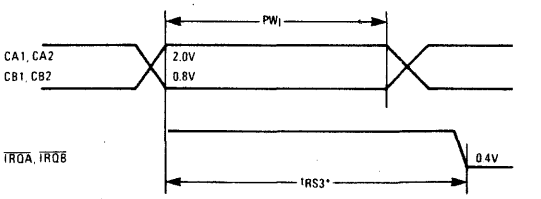
877270

Peripheral Control Output Pulse Width



877271

Interrupt Pulse Width and $\overline{IRQ}$ Response



877272 *Assumes Interrupt Enable Bits are set.

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Application Information

Initialization

A low reset line has the effect of zeroing all PIA registers. This will set PA0-PA7, PB0-PB7, CA2 and CB2 as inputs, and all interrupts disabled. The PIA must be configured during the restart program which follows the reset.

Register Addressing

There are six locations within the PIA accessible to the MPU data bus: two Peripheral Registers, two Data Direction Registers, and two Control Registers. Selection of these locations is controlled by the RS0 and RS1 inputs together with bit 2 in the Control Register, as shown in Table 1.

Table 1. Internal Addressing

RS1	RS0	Control Register Bit CRA-2	Control Register Bit CRB-2	Location Selected
0	0	1	X	Peripheral Register A
0	0	0	X	Data Direction Register A
0	1	X	X	Control Register A
1	0	X	1	Peripheral Register B
1	0	X	0	Data Direction Register B
1	1	X	X	Control Register B

X = Don't Care

Data Direction Registers (DDRA and DDRB)

The two Data Direction Registers allow the MPU to control the direction of data through each corresponding peripheral data line. All Data Direction Register bits set at "0" configure the corresponding peripheral data line as an input; all "1's" result in an output.

Control Registers (CRA and CRB)

The two Control Registers (CRA and CRB) allow the MPU to control the operation of the four peripheral control lines, CA1, CA2, CB1 and CB2. In addition, they allow the MPU to enable the interrupt lines and monitor the status of the interrupt flags. Bits 0 through 5 of the two registers may be written or read by the MPU when the proper chip select and register select signals are applied. Bits 6 and 7 of the two registers are read only and are modified by external interrupts occurring on control lines CA1, CA2, CB1 or CB2. The format of the control words is shown in Table 2.

Table 2. Control Word Format

	7	6	5	4	3	2	1	0
CRA	IRQA1	IRQA2	CA2 Control			DDRA Access	CA1 Control	
CRB	IRQB1	IRQB2	CB2 Control			DDRB Access	CB1 Control	

Data Direction Access Control Bit (CRA-2 and CRB-2) — Bit 2 in each Control Register (CRA and CRB) allows selection of either a Peripheral Interface Register or the Data Direction Register when the proper register select signals are applied to RS0 and RS1.

Control of CA1 and CB1 Interrupt Input Lines (CRA-0, CRB-0, CRA-1 and CRB-1) — The two lowest order bits of the control registers are used to control the interrupt input lines CA1 and CB1. Bits CRA-0 and CRB-0 are used to enable the MPU interrupt signals $\overline{IRQA}$ and $\overline{IRQB}$, respectively. Bits CRA-1 and CRB-1 determine the active transition of the interrupt input signals CA1 and CB1 (Table 3).

Control of CA2 and CB2 Peripheral Control Lines (CRA-3, CRA-4, CRA-5, CRB-3, CRB-4 and CRB-5) — Bits 3, 4 and 5 of the two control registers are used to control the CA2 and CB2 Peripheral Control lines. These bits determine if the control lines will be an interrupt input or an output control signal. If bit CRA-5 (CBR-5) is low, CA2 (CB2) is an interrupt input line similar to CA1 (CB1) (Table 4). When CRA-5 (CRB-5) is high, CA2 (CB2) becomes an output signal that may be used to control peripheral data transfers. When in the output mode, CA2 and CB2 have slightly different characteristics (Tables 5 and 6).

Interrupt Flags (CRA-6, CRA-7, CRB-6 and CRB-7) — The four interrupt flag bits are set by active transitions of signals on the four Interrupt and Peripheral Status lines when those lines are programmed to be interrupt inputs. These bits cannot be set directly from the MPU Data Bus and are reset indirectly by a Read Peripheral Data Operation on the appropriate section.

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Table 3. Control of Interrupt Inputs CA1 and CB1

CRA-1 (CRB-1)	CRA-0 (CRB-0)	Interrupt Input CA1 (CB1)	Interrupt Flag CRA-7 (CRB-7)	MPU Interrupt Request $\overline{IRQA}$ ($\overline{IRQB}$)
0	0	↓ Active	Set high on ↓ of CA1 (CB1)	Disabled — $\overline{IRQ}$ remains high
0	1	↓ Active	Set high on ↓ of CA1 (CB1)	Goes low when the interrupt flag bit CRA-7 (CRB-7) goes high
1	0	↑ Active	Set high on ↑ of CA1 (CB1)	Disabled — $\overline{IRQ}$ remains high
1	1	↑ Active	Set high on ↑ of CA1 (CB1)	Goes low when the interrupt flag bit CRA-7 (CRB-7) goes high

Notes:
1. ↑ indicates positive transition (low to high).
2. ↓ indicates negative transition (high to low).
3. The Interrupt flag bit CRA-7 is cleared by an MPU Read of the A Data Register, and CRB-7 is cleared by an MPU Read of the B Data Register.
4. If CRA-0 (CRB-0) is low when an interrupt occurs (Interrupt disabled) and is later brought high, $\overline{IRQA}$ ($\overline{IRQB}$) occurs on the positive transition of CRA-0 (CRB-0).

Table 4. Control of CA2 and CB2 as Interrupt Inputs CRA-5 (CRB-5) is Low

CRA-5 (CRB-5)	CRA-4 (CRB-4)	CRA-3 (CRB-3)	Interrupt Input CA2 (CB2)	Interrupt Flag CRA-6 (CRB-6)	MPU Interrupt Request $\overline{IRQA}$ ($\overline{IRQB}$)
0	0	0	↓ Active	Set high on ↓ of CA2 (CB2)	Disabled — $\overline{IRQ}$ remains high
0	0	1	↓ Active	Set high on ↓ of CA2 (CB2)	Goes low when the interrupt flag bit CRA-6 (CRB-6) goes high
0	1	0	↑ Active	Set high on ↑ of CA2 (CB2)	Disabled — $\overline{IRQ}$ remains high
0	1	1	↑ Active	Set high on ↑ of CA2 (CB2)	Goes low when the interrupt flag bit CRA-6 (CRB-6) goes high

Notes:
1. ↑ indicates positive transition (low to high).
2. ↓ indicates negative transition (high to low).
3. The Interrupt flag bit CRA-6 is cleared by an MPU Read of the A Data Register and CRB-6 is cleared by an MPU Read of the B Data Register.
4. If CRA-3 (CRB-3) is low when an interrupt occurs (Interrupt disabled) and is later brought high, $\overline{IRQA}$ ($\overline{IRQB}$) occurs on the positive transition of CRA-3 (CRB-3).

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Basic System Configuration

The Microprocessing Unit (MPU) may be configured with a Read Only Memory (ROM), Random Access Memory (RAM), a Peripheral Interface Adapter (PIA), restart circuitry and clock circuitry to form a minimum functional system (Figure 16). Such a system can easily be adapted for a number of small scale applications by simply changing the content of the ROM.

Two-Phase Clock Circuitry and Timing — The MPU requires a two-phase non-overlapping clock which has a frequency range as high as 1MHz. In addition to the two phases, this circuit should also generate an enable Signal E, and its complement E, to enable ROMs, RAMs, PIAs and ACIAs. This Enable signal and its complement are obtained by ANDing $\phi 2$ and VMA (Valid Memory Address).

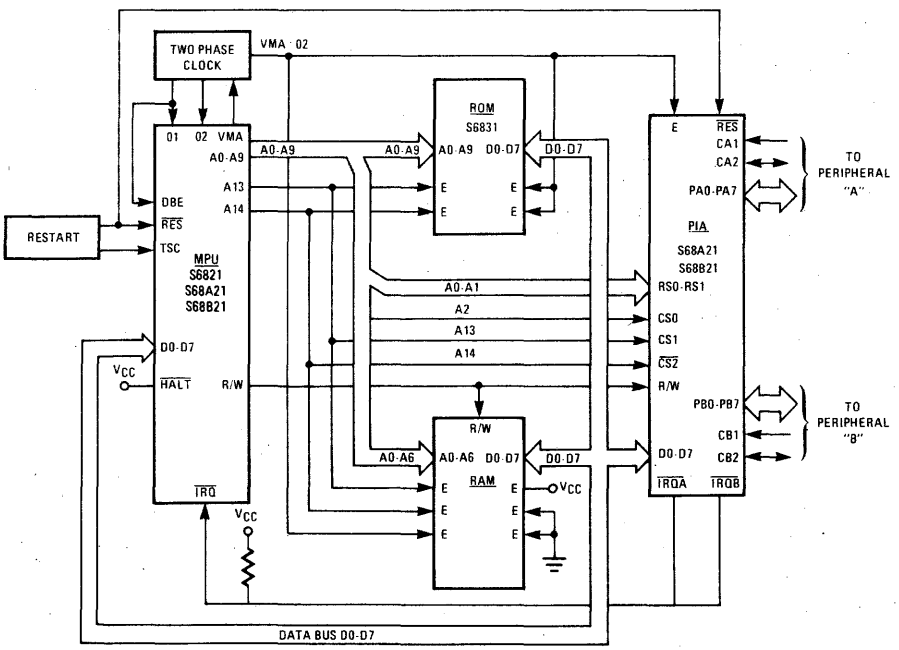
Chip Selection and Addressing — The minimum system configuration permits direct selection of the ROM, RAM, ACIA and PIA without the use of special TTL select logic. This is accomplished by simply wiring the address lines A13, A14 to the Enable or chip select lines on the memories and PIA. This permits the devices to be addressed as follows:

Device	A14	A13	Hex Addresses
RAM	0	0	0000-007F
PIA	0	1	2004-2007 (Registers)
ROM	1	1	6000-63FF

Other addressing schemes can be utilized which use any combination of two of the lines A10 through A14 for chip selection.

Peripheral Control — All control and timing for the peripherals that are connected to the PIA is accomplished by software routines under the control of the MPU.

Figure 16. Minimum System Implementation



877258

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16,384 BIT (2048x8) STATIC NMOS ROM

Features

- ☐ Single +5V Power Supply
- ☐ Directly TTL Compatible Inputs
- ☐ Three-State TTL Compatible Outputs
- ☐ Three Programmable Enables
- ☐ Access Time: 450ns Maximum
- ☐ S6831A: Intel 2316A Pin Compatible
- ☐ S6831B: 2716 EPROM Pin Compatible
- ☐ Low Power: Supply Current is 80mA Maximum

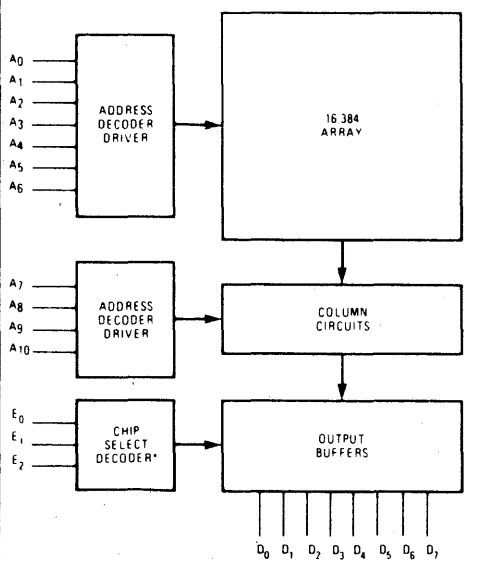
General Description

The AMI 6831 family of 16,384 bit mask programmable Read-Only-Memories offers fully static operation with a single + 5V power supply. The device is fully TTL compatible on all inputs and three-state outputs. The three enables are mask programmable, the active level is specified by the user.

The S6831 family is available in two pin configurations. One of these, the S6813A, is the pin configuration of a popular ROM: the Intel 2316A. The second pin configuration, the S6813B, is pin compatible with the 2708 and 2716 EPROMs. Software developed in EPROMs can be put in low cost ROM for high volume production.

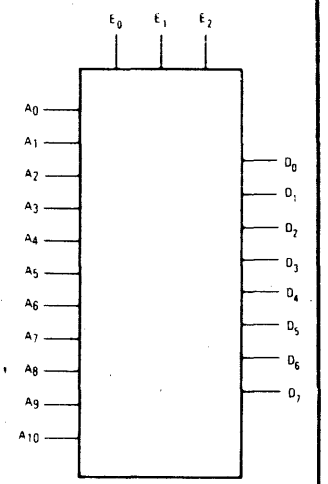
The device is organized as 2048 words by 8 bits, a configuration particularly suitable for microprocessors. The S6831 family is manufactured with an N-channel silicon gate depletion load technology.

Block Diagram



*PROGRAMMABLE CHIP SELECTS

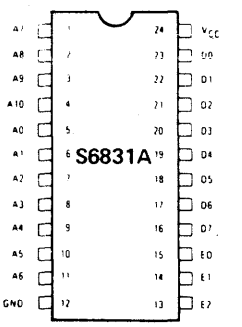
Logic Symbol



Pin Names

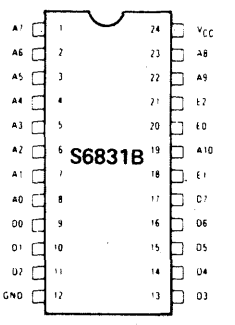
$A_0 - A_{10}$	Address Inputs
$D_0 - D_7$	Data Outputs
$E_0 - E_2$	Chip Select Inputs
V_{CC}	+5V Power Supply

Pin Configurations



Pin Compatible with:

AMD	AM9217
EA	EA2316A/8316A
GI	RO-3-8316
INTEL	2316A/8316A
MOSTEK	MK31000
NATIONAL	MM2316A
NEC	μPD2316A
SYNERTEK	SY2316A



Pin Compatible with:

AMD	AM9218
EA	EA2316E/8316E
FSC	68316E
GI	RO-3-9316
INTEL	2316E/8316E
MOTOROLA	MCM68316E
MOSTEK	MK-34000
NATIONAL	MM2316E
NEC	μPD2316E
SIGNETICS	2616
SYNERTEK	SY2316B

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Absolute Maximum Ratings*

Ambient Temperature Under Bias	-10°C to 80°C
Storage Temperature	-65°C to 150°C
Output or Supply Voltage	-0.5V to 7V
Input Voltage	-0.5V to 5.5V
Power Dissipation	1W

*Comment: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or at any other condition above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

D.C. Characteristics: V_{CC} = +5V ± 5%; T_A = 0°C to +70°C

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
V_{OL}	Output LOW Voltage			0.4	V	I_{OL} = 2.1 mA
V_{OH}	Output HIGH Voltage	2.4			V	I_{OH} = -100μA
V_{IL}	Input LOW Voltage	-0.5		0.8	V	
V_{IH}	Input HIGH Voltage	2.0		V_{CC}	V	
I_{LI}	Input Leakage Current			10	μA	V_{IN} = 0 to 5.25V
I_{LO}	Output Leakage Current			10	μA	V_{OUT} = 0.4 to 2.4V, Chip Deselected
I_{CC}	Power Supply Current			70	mA	V_{CC} = Max. T_A = 25°C
				80	mA	V_{CC} = Max. T_A = 0°C

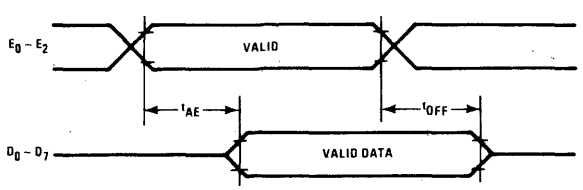
Capacitance: f = 1.0 MHz; T_A = 25°C

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
C_{IN}	Input Capacitance			7.5	pF	V_{IN} = 0V
C_{OUT}	Output Capacitance			10	pF	V_{OUT} = 0V

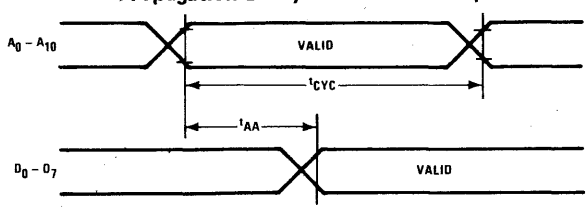
A.C. Characteristics: V_{CC} = +5V ± 5%; T_A = 0°C to +70°C

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
t_{CYC}	Read Cycle Time	450			ns	See Test Circuit & Waveforms
t_{AA}	Address Access Time			450	ns	
t_{AE}	Enable Access Time			200	ns	
t_{OFF}	Output Disable Time	10		150	ns	

Propagation Delay From Chip Enable



Propagation Delay from Address Inputs



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A.C. Test Conditions

Output Load	1 TTL Gate and C_L = 100 pF
Input Pulse Levels	0.8 to 2.4V
Input Rise and Fall Times (10% to 90%)	20 ns

Timing Measurement Reference Level

Input	1V and 2.2V
Output	0.8V and 2.0V

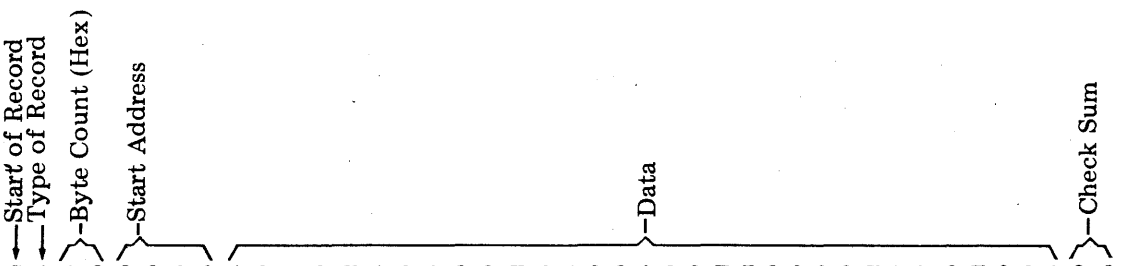
Custom Programming

The preferred method of pattern submission is the AMI Hex format as described below, with its built-in address space mapping and error checking. This is the format produced by the AMI Assembler. The format is as follows and may be on paper tape, punched cards or other media readable by AMI.

Position	Description
1	**Start of record (Letter S)**
2	**Type of record** 0 — Header record (comments) 1 — Data record 9 — End of file record
3, 4	**Byte Count** Since each data byte is represented as two hex characters, the byte count must be multiplied by two to get the number of characters to the end of the record. (This includes checksum and address data.) Records may be of any length defined in each record by the byte count.
5, 6, 7, 8	**Address Value** The memory location where the first data byte of this record is to be stored. Addresses should be in ascending order.
9, . . ., N	**Data** Each data byte is represented by two hex characters. Most significant character first.
N+1, N+2	**Checksum** The one's complement of the additive summation (without carry) of the data bytes, the address, and the byte count.

Example:

```
S 1 1 3 0 0 0 0 4 9 E 9 F 1 0 3 2 0 F 0 4 9 3 1 3 9 F 7 2 0 0 0 F 5 E 0 F 0 0 1 2 6
S 9 0 3 0 0 0 0 F C
```



NOTES:

1. Only positive logic formats for E_0, E_1, E_2 are accepted. 1 = V_{HIGH}; 0 = V_{LOW}
2. A "0" indicates the chip is enabled by a logic 0.
   A "1" indicates the chip is enabled by a logic 1.
3. Paper tape format is the same as the card format above except:
   a. The record should be a maximum of 80 characters.
   b. Carriage return and line feed after each record followed by another record.
   c. There should NOT be any extra line feed between records at all.
   d. After the last record, four (4) $$$$ (dollar) signs should be punched with carriage return and line feed indicating end of file.

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ERASABLE AND ELECTRICALLY REPROGRAMMABLE READ ONLY MEMORY

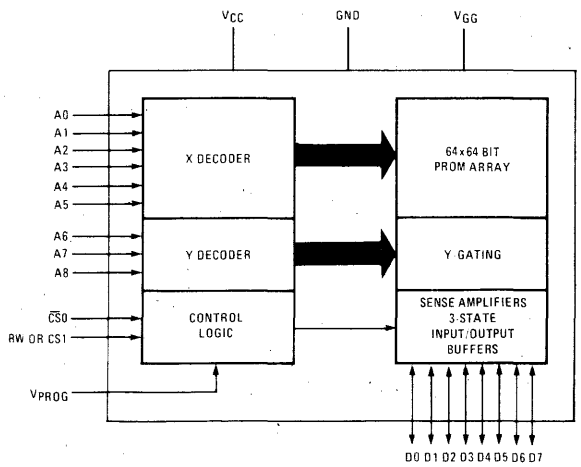
Features

- ☐ On-Board Programmability
- ☐ Fast Access Time — 575ns Typ.
- ☐ Pin Configuration Similar to the S6830 1K x 8 Bit ROM
- ☐ High Speed Programming — Less than 1 Minute for All 4096 Bits
- ☐ Programmed with R/W, CS and V_{PROG} Pins
- ☐ Completely TTL Compatible — Excluding the V_{PROG} Pin
- ☐ Ultraviolet Light Erasable — Less than 10 Minutes
- ☐ Static Operation — No Clocks Required
- ☐ Three-State Data I/O
- ☐ Standard Power Supplies +5V and −12V
- ☐ Mature P-Channel Process

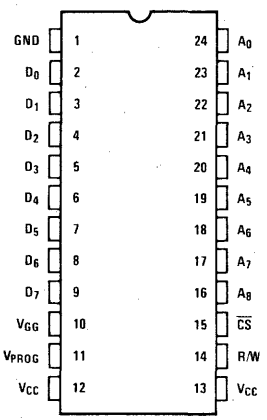
General Description

The S6834 is a high speed, static, 512 x 8 bit, erasable and electrically programmable read only memory designed for use in bus-organized systems. Both input and output are TTL compatible during both read and write modes. Packaged in a 24 pin hermetically sealed dual in-line package the bit pattern can be erased by exposing the chip to an ultra-violet light source through the transparent lid, after which a new pattern can be written.

Block Diagram



Pin Configuration



Typical Applications

- ☐ ROM Program Debugging
- ☐ Code Translation
- ☐ Microprogramming
- ☐ Look-up Tables
- ☐ Random Logic Replacement
- ☐ Programmable Waveforms
- ☐ Character Generation
- ☐ Electronic Keyboards

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DC (STATIC) CHARACTERISTICS (V_{CC} = +5.0V ± 5%, V_{GG} = −12.0V ± 5% T_A = 0 – 70°C unless otherwise noted).

SYMBOL	CHARACTERISTIC	MIN	MAX	UNIT
V_{IL}	INPUT VOLTAGE LOW		0.8	V
V_{IH}	INPUT VOLTAGE HIGH	V_{CC} −2.25	V_{CC} to .3	V
V_{OL}	OUTPUT VOLTAGE LOW I_{OL} = 1.6 ma		0.4	V
V_{OH}	OUTPUT VOLTAGE HIGH I_{OH} = 200μA	2.4		V
I_{LI}	INPUT LEAKAGE CURRENT		10	μa
I_{LO}	OUTPUT LEAKAGE CURRENT CS = 5V		20	μa
I_{GG}	V_{GG} SUPPLY CURRENT		45	ma
I_{CC}	V_{CC} SUPPLY CURRENT		50	ma
P_D	POWER DISSIPATION		750	mw

NOTE: Program input V_{PROG} may be tied to V_{CC} during the Read.

AC (DYNAMIC) CHARACTERISTICS (Loading is as shown in Figure 1 unless otherwise noted).

SYMBOL	CHARACTERISTIC	MIN	MAX (6834)	MAX (6834–1)	UNIT
T_{ACC}	ACCESS TIME		575	750	ns
T_{CO}	CHIP SELECT TO OUTPUT DELAY		300	400	ns
T_{DD}	CHIP DESELECT TO OUTPUT DELAY		250	325	ns

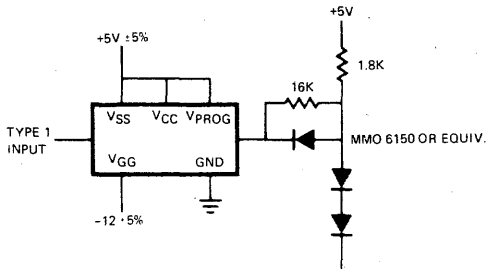
PROGRAM CHARACTERISTICS (R/W G_{nd}, Program pulse rise and fall time (10% to 90%) are both at 1μs max).

SYMBOL	CHARACTERISTICS	MIN	MAX	UNIT
T_{AS}	ADDRESS SET UP TIME	10		μs
T_{CSS}	CHIP SELECT SET UP TIME	10		μs
T_{DS}	DATA SET UP TIME	10		μs
T_{AH}	ADDRESS HOLD TIME	10		μs
T_{CSH}	CHIP SELECT HOLD TIME	10		μs
T_{DH}	DATA HOLD TIME	10		μs
T_{PWL}	PROGRAM PULSE WIDTH LOW	3	5	ms
T_{PWH}	PROGRAM PULSE WIDTH HIGH	500		μs
V_{PROG}*	PROGRAM AMPLITUDE	−55	−50	V
I_{PROG}	PROGRAM CURRENT		35	ma
T_{WS}	WRITE SET UP TIME	10		μs
T_{WH}	WRITE HOLD TIME	5		μs
T_{RS}	READ SET UP TIME	10		μs

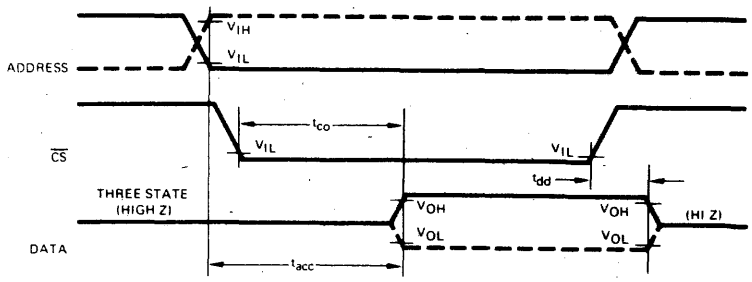
*Note that in the WRITE mode the MIN value of V_{PROG} should not be exceeded and that chip select, address, and data lines may remain at TTL level, as in the READ mode.

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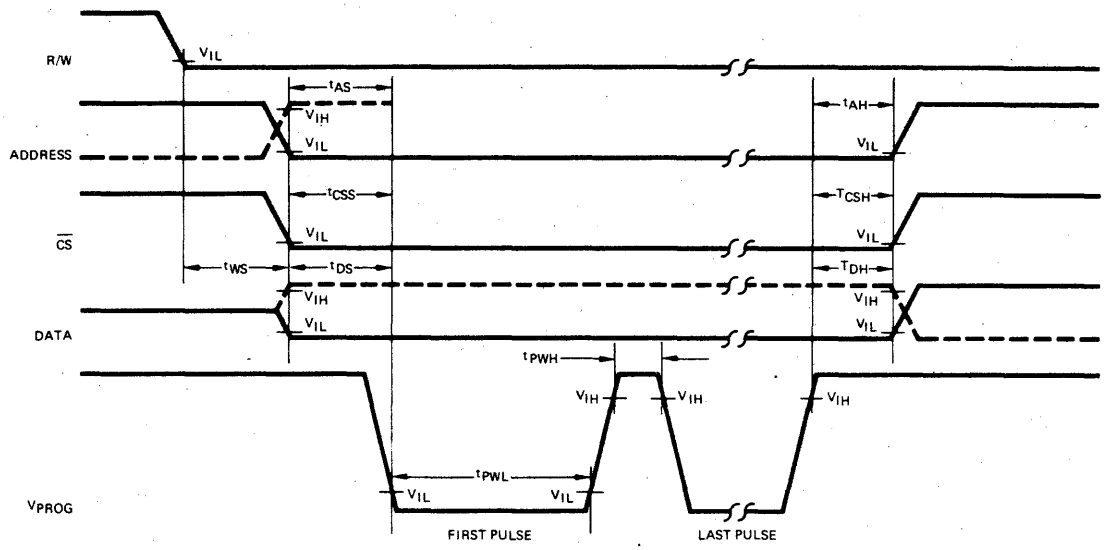
TEST CONDITIONS



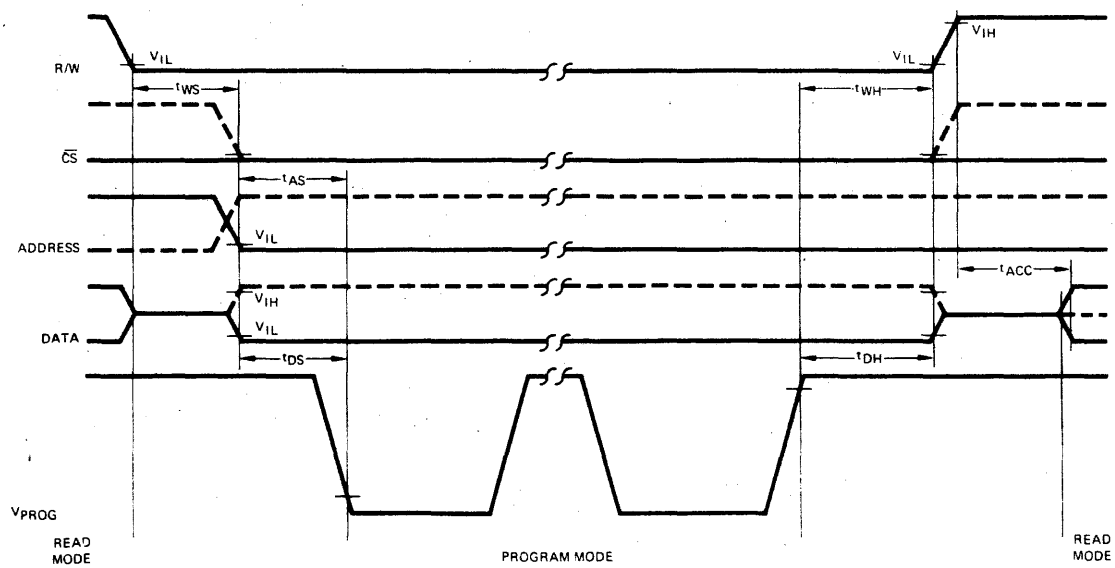
READ CYCLE TIMING WAVEFORMS



PROGRAMMING CYCLE TIMING WAVEFORMS



READ/PROGRAM/READ CYCLE TIMING WAVEFORM



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CONTROL FUNCTION TRUTH TABLE

CS	R/W	V_{PROG}	MODE	OUTPUTS
0	0	V_{PROG}	Write	Active Data Inputs
0	1	V_{CC}	Read	Active
1	X	X	Standby	Floating

OPERATION

Initially, and after each erasure, all bits of the 6834 are in the logic "0" state (output 0 volts). Data is stored by selectively programming a logic "1" into the desired bit locations. The R/W input (pin 14) is used to select the desired mode of operation. When the R/W input is at logic "0" the chip is in the write enable mode of operation. The outputs (0_1 –0_8) are disabled (floating) with the corresponding pins becoming the data inputs ($0_1 \rightarrow D_{IN\ 1}$ etc.). The word address is selected in the same manner as in the read mode. Data to be programmed are presented 8 bits in parallel and after the address and data are set up a programming pulse (V_P –50 volts) is applied. V_{PROG} electrically writes the data into the memory array. Writing may be inhibited by deselecting the chip with the CS input at a logic "1" during the write cycle. This feature allows true "on board" programming in bus organized systems where the R/W and V_{PROG} inputs are common and the device to be programmed is selected by means of the chip select input as during read operations.

The amount of program energy required to insure memory retention may be defined as a function of the number of program pulses (N) times the program pulse width (t_{pw}) ($N \times t_{pw} \geqslant 60$ msec). This means if a 3 ms pulse is used, 20 program pulses are required, and if a 5 ms pulse is used 12 program pulses are required.

The read operation is accomplished by a logic "1" at the R/W input with the program input connected to V_{SS} potential. True data (data out = data in) is valid after the address is stable. The CS input will disable (float) the outputs when at a logic "1" to allow or tie capability.

Erasure is accomplished by exposing the array to a high intensity ultra-violet light source (such as, Ultra-Violet Products, Inc. Lamp Model S52 or UVS-54) for a period of 7 to 10 minutes. The clear optical lid should be approximately one inch away from the lamp tubes.

INTERFACE DESCRIPTION

Pin	Label	Function
(2)	D0	**Data Lines** – with the R/W line selected for Read (V_{IH}), the Data Lines (D0 through D7) are set to reflect the contents of the selected memory location. When the R/W line is set for Write (V_{IL}), the Data Lines are input to the addressed location of the 6834 when V_{PROG} is present. The Data Bus output drivers are three-state devices that remain in the high impedance (off) state when CS is in the V_{IH} state of when R/W is in the V_{IL} state.
(3)	D1	
(4)	D2	
(5)	D3	
(6)	D4	
(7)	D5	
(8)	D6	
(9)	D7	
(14)	R/W	**Read/Write** – When this input line is set to V_{IH}, the device is in the Read mode, a low (V_{IL}) signal puts it into the Write mode.
(15)	CS	**Chip Select** – This input line must be set to V_{IL} for a Read or Write operation to be performed. When it is High (V_{IH}) the output data bus is set to a high-impedance three-state condition and disables the Write operation.
(11)	V_{PROG}	**Program** – In the Write mode, a programming pulse (–50V dc) at this input causes the data at the Data Lines to be stored in the selected address. This pin should be tied to V_{CC} for normal Read operations.
(24)	A0	**Address Lines** – These lines select the 8 bit word in memory for Read or Write operation
(23)	A1	
(22)	A2	
(21)	A3	
(20)	A4	
(19)	A5	
(18)	A6	
(17)	A7	
(16)	A8	

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PROGRAMMABLE TIMER

Features

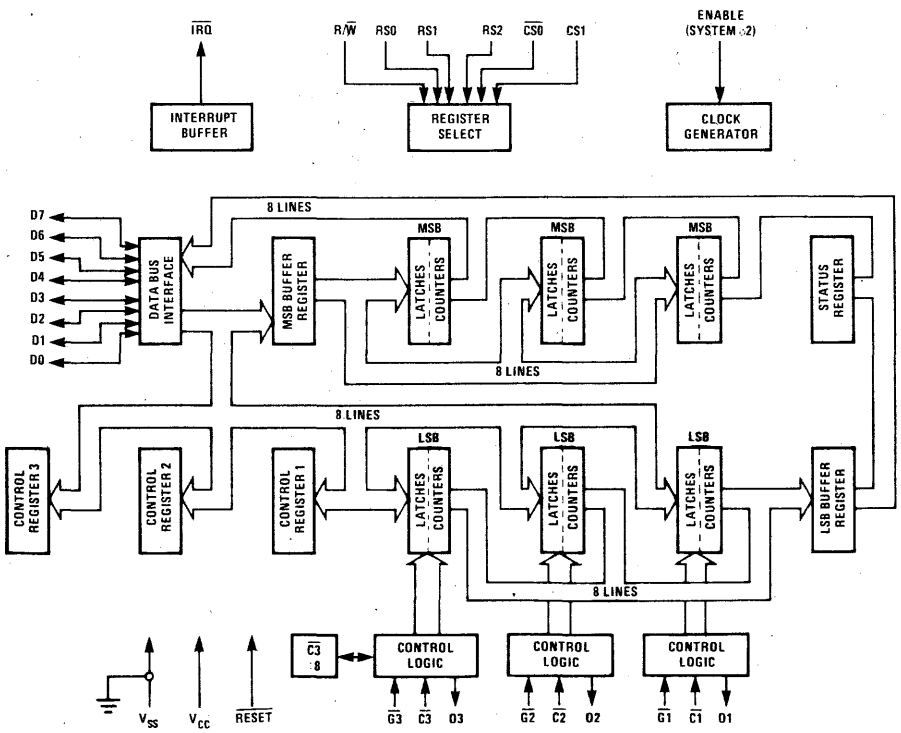
- ☐ Operates from a Single 5 Volt Power Supply
- ☐ Fully TTL Compatible
- ☐ Single System Clock Required (Enable)
- ☐ Selectable Prescaler on Timer 3 Capable of a 4MHz Input
- ☐ Programmable Interrupts ($\overline{IRQ}$) Output to MPU
- ☐ Readable Down Counter Indicates Counts to Go to Time-Out
- ☐ Selectable Gating for Frequency or Pulse-Width Comparison
- ☐ $\overline{RESET}$ Input
- ☐ Three Asynchronous External Clock and Gate/Trigger Inputs Internally Synchronized
- ☐ Three Maskable Outputs

General Description

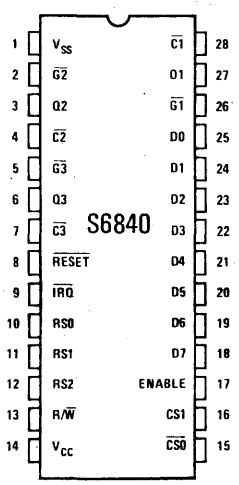
The S6840 is a programmable subsystem component of the S6800 family designed to provide variable system time intervals.

The S6840 has three 16-bit binary counters, three corresponding control registers and a status register. These counters are under software control and may be used to cause system interrupts and/or generate output signals. The S6840 may be utilized for such tasks as frequency measurements, event counting, interval measuring and similar tasks. The device may be used for square wave generation, gated delay signals, single pulses of controlled duration, and pulse width modulation as well as system interrupts.

Block Diagram



Pin Configuration



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Absolute Maximum Ratings

Supply Voltage V_{CC}	-0.3 to +7.0V
Input Voltage V_{IN}	-0.3 to +7.0V
Operating Temperature Range T_A	0°C to +70°C
Storage Temperature Range T_{stg}	-55°C to +150°C
Thermal Resistance θ_{JA}	82.5°C/W

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

Electrical Characteristics (V_{CC} = 5.0V ± 5%, V_{SS} = 0, T_A = 0°C to +70°C unless otherwise noted)

Symbol	Characteristic	Min.	Typ.	Max.	Unit	Condition
V_{IH}	Input High Voltage	V_{SS} +2.0		V_{CC}	V	
V_{IL}	Input Low Voltage	V_{SS} - 0.3		V_{SS} +0.8	μA	
I_{IN}	Input Leakage Current		1.0	2.5	μA	V_{IN}=0 to 5.25V
I_{TSI}	Three-State (Off State) Input Current D0 — D7		2.0	10	μA	V_{IN} = 0.4 to 2.4V
V_{OH}	Output High Voltage				V	
	D0 — D7	V_{SS} +2.4				I_{LOAD} = -205μA
	Other Outputs	V_{SS} +2.4				I_{LOAD} = -200μA
V_{OL}	Output Low Voltage				V	
	D0 — D7			V_{SS} +0.4		I_{LOAD} = 1.6mA
	01 — 03, $\overline{IRQ}$			V_{SS} +0.4		I_{LOAD} = 3.2mA
I_{LOH}	Output Leakage Current (Off State) $\overline{IRQ}$		1.0	10	μA	V_{OH} = 2.4V
P_D	Power Dissipation			550	mW	
C_{IN}	Input Capacitance				pF	V_{IN}=0, T_A=25°C,
	D0 — D7			12.5		f = 1.0MHz
	All Others			7.5		
C_{OUT}	Output Capacitance				pF	
	$\overline{IRQ}$			5.0		V_{IN}=0, T_A=25°C,
	01, 02, 03			10		f = 1.0MHz

Bus Timing Characteristics

Read (See Figures 1 and 7)

Symbol	Characteristic	Min.	Max.	Unit	Condition
t_{CYCE}	Enable Cycle Time	1.0	1.0	μs	
PW_{EH}	Enable Pulse Width, High	0.45	4.5	μs	
PW_{EL}	Enable Pulse Width, Low	0.43		μs	
t_{AS}	Setup Time, Address and R/$\overline{W}$ valid to enable positive transition	160		ns	
t_{DDR}	Data Delay Time		320	ns	
t_H	Data Hold Time	10		ns	
t_{AH}	Address Hold Time	10		ns	
t_{Er}, t_{Ef}	Rise and Fall Time for Enable input		25	ns	

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Bus Timing Characteristics (Continued)
Write (See Figures 2 and 7)

Symbol	Characteristic	Min.	Max.	Unit	Condition
t_{CYCE}	Enable Cycle Time	1.0	10	μs	
PW_{EH}	Enable Pulse Width, High	0.45	4.5	μs	
PW_{EL}	Enable Pulse Width, Low	0.43		μs	
t_{AS}	Setup Time, Address and R/$\overline{W}$ valid to enable positive transition	160		ns	
t_{DSW}	Data Setup Time	195		ns	
t_H	Data Hold Time	10		ns	
t_{AH}	Address Hold Time	10		ns	
t_{Er}, t_{Ef}	Rise and Fall Time for Enable input		25	ns	

AC Operating Characteristics

Symbol	Characteristic	Min.	Max.	Unit	Condition
t_r, t_f	Input Rise and Fall Times $\overline{C}$, $\overline{G}$ and $\overline{Reset}$		1.0*	μs	
PW_L	Input Pulse Width Low (Figure 3) $\overline{C}$, $\overline{G}$ and $\overline{Reset}$	$t_{CYCE}+t_{su}+t_{hd}$		ns	
PW_H	Input Pulse Width High (Figure 4) $\overline{C}$, $\overline{G}$	$t_{CYCE}+t_{su}+t_{hd}$		ns	
t_{su}	Input Setup Time (Figure 5) (Synchronous Mode) $\overline{C}$, $\overline{G}$ and $\overline{Reset}$ $\overline{C3}$ (÷8 Prescaler Mode only)	200		ns	
t_{hd}	Input Hold Time (Figure 5) (Synchronous Mode) $\overline{C}$, $\overline{G}$ and $\overline{Reset}$ $\overline{C3}$ (÷8 Prescaler Mode only)	50		ns	
t_{co}	Load A TTL		700	ns	V_{OH}=2.4V
t_{cm}	Load C MOS		450	ns	V_{OH}=2.4V
t_{cmos}	Load C CMOS		2.0	μs	V_{OH}=0.7V_{DD}
t_{IR}	Interrupt Release Time		1.6	μs	

*t_r and $t_f \leq$ 1 x Pulse Width or 1.0μs, whichever is smaller.

Table 1. Register Selection

REGISTER SELECT INPUTS			OPERATIONS	
RS2	RS1	RS0	R/$\overline{W}$ = 0	R/$\overline{W}$ = 1
0	0	0	CR20 = 0 WRITE CONTROL REGISTER #3 CR20 = 1 WRITE CONTROL REGISTER #1	NO OPERATION
0	0	1	WRITE CONTROL REGISTER #2	READ STATUS REGISTER
0	1	0	WRITE MSB BUFFER REGISTER	READ TIMER #1 COUNTER
0	1	1	WRITE TIMER #1 LATCHES	READ LSB BUFFER REGISTER
1	0	0	WRITE MSB BUFFER REGISTER	READ TIMER #2 COUNTER
1	0	1	WRITE TIMER #2 LATCHES	READ LSB BUFFER REGISTER
1	1	0	WRITE MSB BUFFER REGISTER	READ TIMER #3 COUNTER
1	1	1	WRITE TIMER #3 LATCHES	READ LSB BUFFER REGISTER

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Figure 1. Bus Read Timing Characteristics (Read Information from PTM)

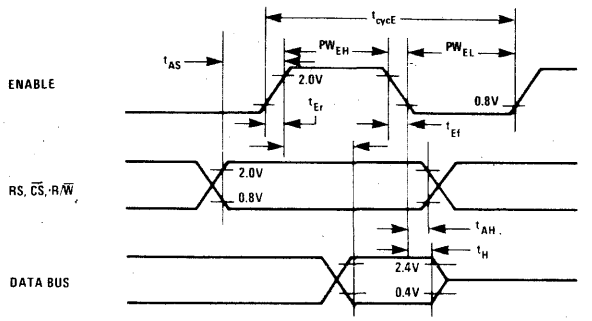


Figure 2. Bus Write Timing Characteristics (Write Information into PTM)

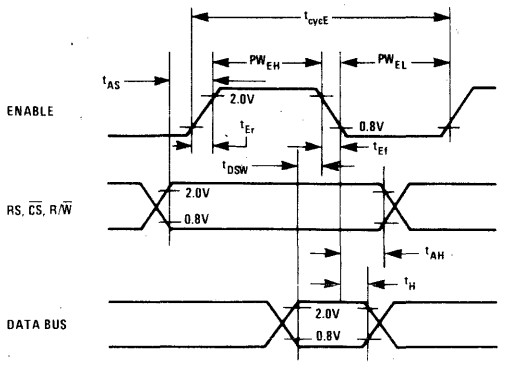


Figure 3. Input Pulse Width Low

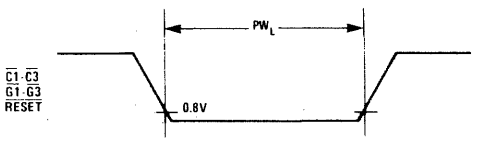


Figure 4. Input Pulse Width High

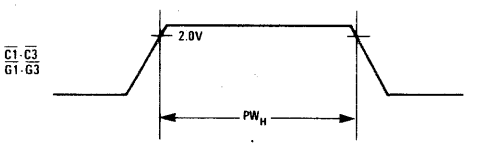


Figure 5. Input Setup and Hold Times

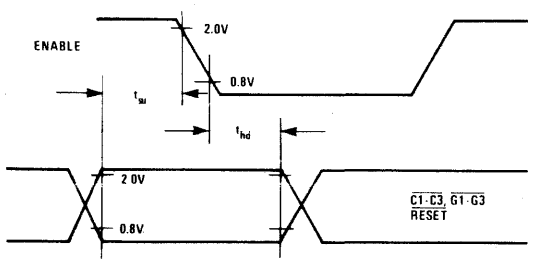


Figure 6. Output Delay

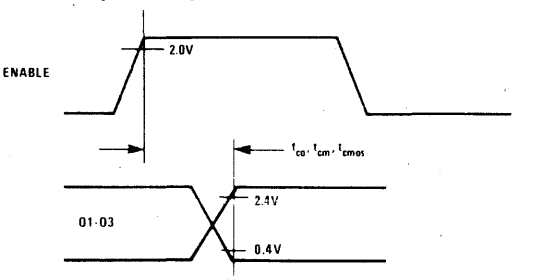
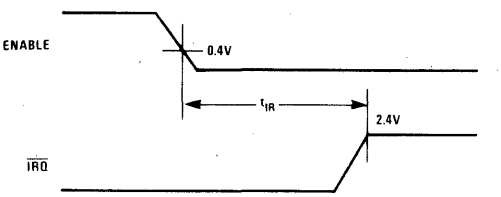


Figure 7. $\overline{IRQ}$ Release Time



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ROM-I/O-TIMER

Features

- 2048x8-Bit Bytes of Mask-Programmable ROM
- 8-Bit Bidirectional Data Port for Parallel Interface Plus Two Control Lines
- Programmable Interval Timer-Counter Functions
- Programmable I/O Peripheral Data, Control and Direction Registers
- Compatible with the Complete S6800 Microcomputer Product Family
- TTL-Compatible Data and Peripheral Lines
- Single 5 Volt Power Supply

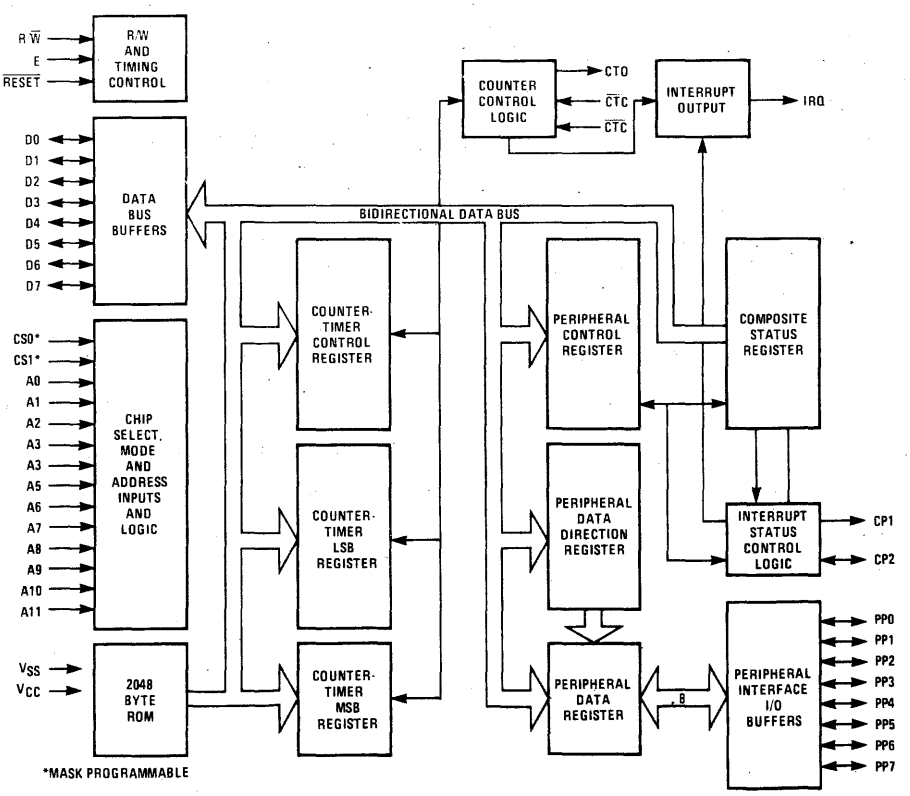
General Description

The S6846 combination chip provides the means, in conjunction with the S6802, to develop a basic 2-chip microcomputer system. The S6846 consists of 2048 bytes of mask-programmable ROM, an 8-bit bidirectional data port with control lines, and a 16-bit programmable timer-counter.

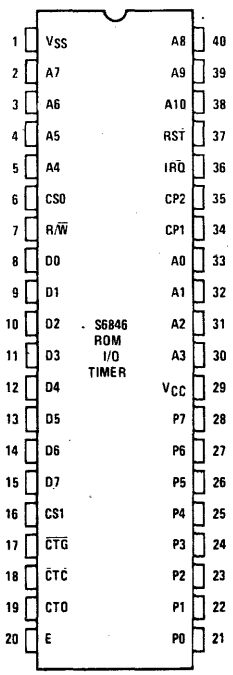
This device is capable of interfacing with the S6802 (basic S6800, clock and 128 bytes of RAM) as well as the S6800 if desired. No external logic is required to interface with most peripheral devices.

The S6846 combination chip may be partitioned into three functional operating sections: programmed storage, timer-counter functions, and a parallel I/O port.

Block Diagram



Pin Configuration



ADVANCED PRODUCT DESCRIPTION

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Asynchronous Communication Interface Adapter (ACIA)

Features

- 8 Bit Bidirectional Data Bus for Communication with MPU
- False Start Bit Deletion
- Peripheral/Modem Control Functions
- Double Buffered Receiver and Transmitter
- One or Two Stop Bit Operation
- Eight and Nine-Bit Transmission with Optional Even and Odd Parity
- Parity, Overrun and Framing Error Checking
- Programmable Control Register
- Optional ÷1, ÷16, and ÷64 Clock Modes
- Up to 500,000 bps Transmission

Absolute Maximum Ratings

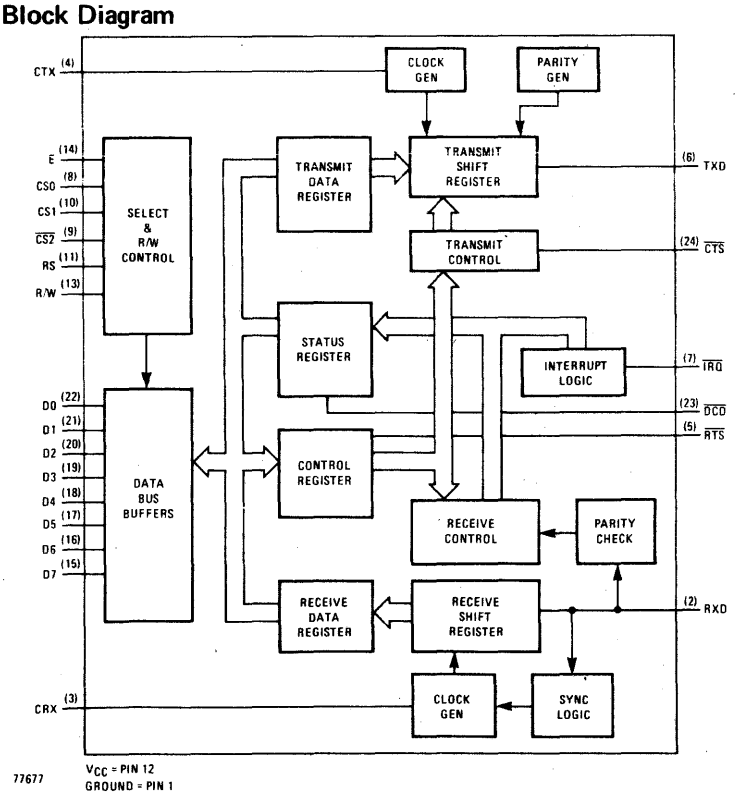
Supply Voltage	-0.3V to +7.0V
Input Voltage	-0.3V to +7.0V
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	-55°C to +150°C

General Description

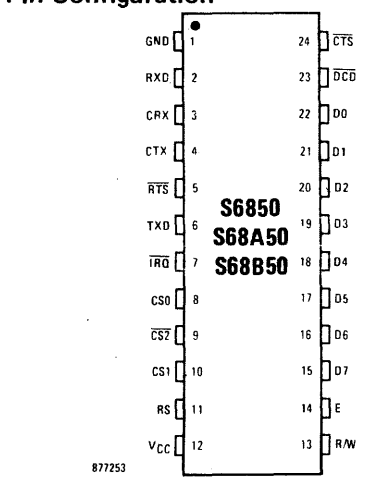
The S68A50/S68B50 Asynchronous Communications Interface Adapter (ACIA) provides the data formatting and control to interface serial asynchronous data communications to bus organized systems such as the S68A00/S68B00 Microprocessing Units.

The S68A50/S68B50 includes select enable, read/write, interrupt and bus interface logic to allow data transfer over an eight-bit bidirectional data bus. The parallel data of the bus system is serially transmitted and received by the asynchronous data interface, with proper formatting and error checking. The functional configuration of the ACIA is programmed via the data bus during system initialization. Word lengths, clock division ratios and transmit control through the Request to Send output may be programmed. For modem operation three control lines are provided.

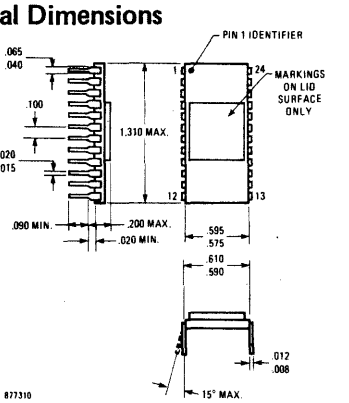
Block Diagram



Pin Configuration



Physical Dimensions



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Electrical Characteristics (V_{CC} = +5.0V ±5%, V_{SS} = 0, T_A = 0°C to +70°C unless otherwise noted.)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
V_{IH}	Input High Voltage (normal operating level)	V_{SS}+2.0		V_{CC}	Vdc	
V_{IL}	Input Low Voltage (normal operating level)	V_{SS}-0.3		V_{SS}+0.8	Vdc	
I_{IN}	Input Leakage Current R/W, ES, CS0, CS1, $\overline{CS2}$, Enable		1.0	2.5	μAdc	V_{IN} = 0Vdc to 5.25Vdc
I_{TSI}	Three-State (Off State) Input Current D0-D7		2.0	10	μAdc	V_{IN} = 0.4Vdc to 2.4Vdc
V_{OH}	Output High Voltage (all outputs except IRQ)					
	D0-D7	V_{SS}+2.4			Vdc	I_{LOAD} = -205μAdc, Enable Pulse Width <25μs
	Tx Data, $\overline{RTS}$	V_{SS}+2.4			Vdc	I_{LOAD} = -100μAdc, Enable Pulse Width <25μs
V_{OL}	Output Low Voltage (Enable pulse width < 25μs)			V_{SS}+0.4	Vdc	I_{LOAD} = 1.6mAdc, Enable Pulse Width <25μs
I_{LOH}	Output Leakage Current (Off State) $\overline{IRQ}$		1.0	10	μAdc	V_{OH} = 2.4Vdc
P_D	Power Dissipation		300	525	mW	
C_{IN}	Input Capacitance					
	D0-D7		10	12.5	pF	
	E,Tx,CLK,Rx Clk,R/W,RS,Rx Data, CS0,$\overline{CS1}$,$\overline{CS2}$,RXD,CTS,$\overline{DCD}$,CTX,CRX		7.0	7.5	pF	V_{IN} = 0, T_A = 25°C, f = 1.0MHz
C_{OUT}	Output Capacitance $\overline{RTS}$,Tx Data			10	pF	
	$\overline{IRQ}$			5.0	pF	
PW_{CL}	Minimum Clock Pulse Width, Low ÷16, ÷64 Modes	600			ns	
PW_{CH}	Minimum Clock Pulse Width, High ÷16, ÷64 Modes	600			ns	
f_C	Clock Frequency ÷1 Mode			500	kHz	
	÷16, ÷64 Modes			800	kHz	
t_{TDD}	Clock-to-Data Delay for Transmitter			1.0	μs	
t_{RDSU}	Receive Data Setup Time ÷1 Mode	500			ns	
t_{RDH}	Receive Data Hold Time ÷1 Mode	500			ns	
t_{IR}	Interrupt Request Release Time			1.2	μs	
t_{RTS}	Request-to-Send Delay Time			1.0	μs	
t_r,t_f	Input Transition Times (Except Enable)			1.0*	μs	

*1.0μ or 10% of the pulse width, whichever is smaller.

Bus Timing Characteristics (V_{CC} = +5.0V ±5%, V_{SS} = 0, T_A = 0°C to +70°C unless otherwise noted.)

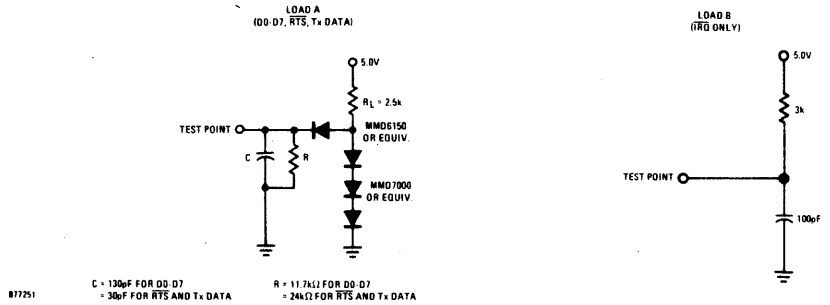
Read

Symbol	Parameter	S68A50		S68B50		Units
		Min.	Max.	Min.	Max.	
t_{cycF}	Enable Cycle Time	0.666		0.50		μs
PW_{EH}	Enable Pulse Width, High	0.28	25	0.22	25	μs
PW_{EL}	Enable Pulse Width, Low	0.28		0.21		μs
t_{AS}	Setup Time, Address and R/W Valid to Enable Positive Transition	140		70		ns
t_{DDR}	Data Delay Time		220		180	ns
t_H	Data Hold Time	10		10		ns
t_{AH}	Address Hold Time	10		10		ns
t_{Er}, t_{Ef}	Rise and Fall Time for Enable Input		25		25	ns

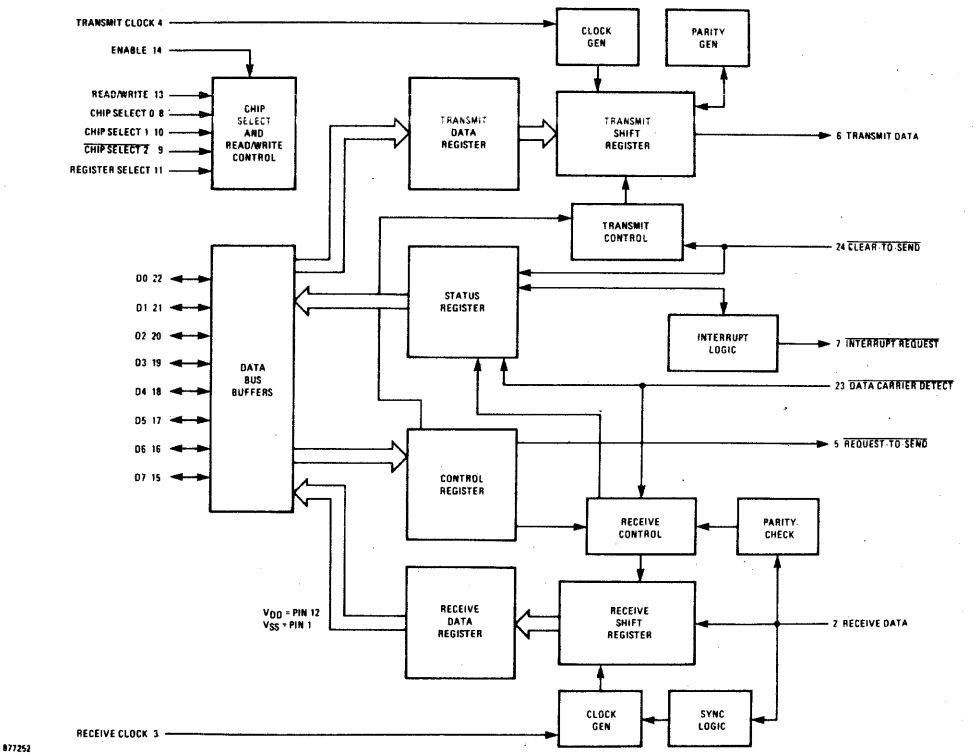
Write

Symbol	Parameter	S68A50 Min.	S68A50 Max.	S68B50 Min.	S68B50 Max.	Units
t_{cycE}	Enable Cycle Time	0.666		0.50		μs
PW_{EH}	Enable Pulse Width, High	0.28	25	0.22	25	μs
PW_{EL}	Enable Pulse Width, Low	0.28		0.21		μs
t_{AS}	Setup Time, Address and R/W Valid to Enable Positive Transition	140		70		ns
t_{DSW}	Data Setup Time	80		60		ns
t_H	Data Hold Time	10		10		ns
t_{AH}	Address Hold Time	10		10		ns
t_{Fr}, t_{Ef}	Rise and Fall Time for Enable Input		25		25	ns

Bus Timing Test Loads



Expanded Block Diagram



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Figure 1. Clock Pulse Width, Low State

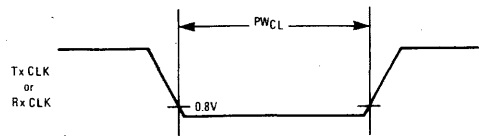


Figure 2. Clock Pulse Width, High State

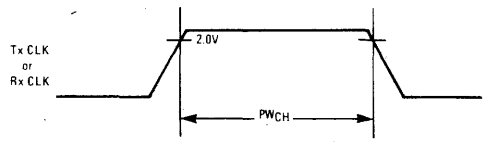


Figure 3. Transmit Data Output Delay

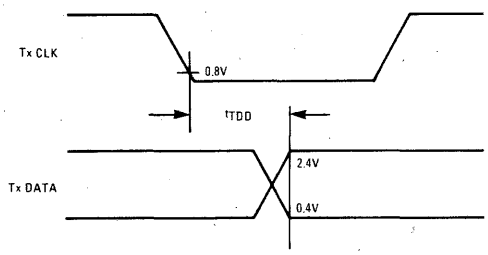


Figure 4. Receive Data Setup Time (÷1 Mode)

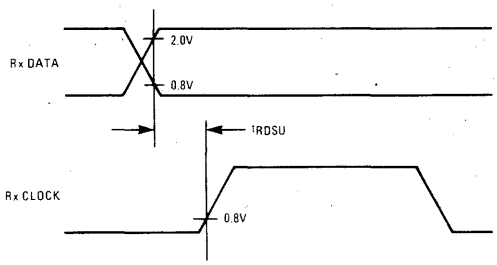


Figure 5. Receive Data Hold Time (÷1 Mode)

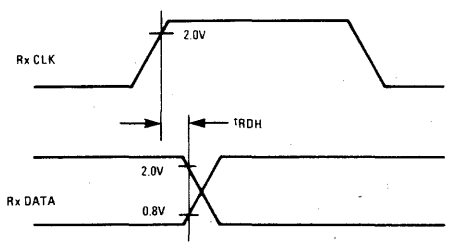


Figure 6. Request-to Send Delay and Interrupt-Request Release Times

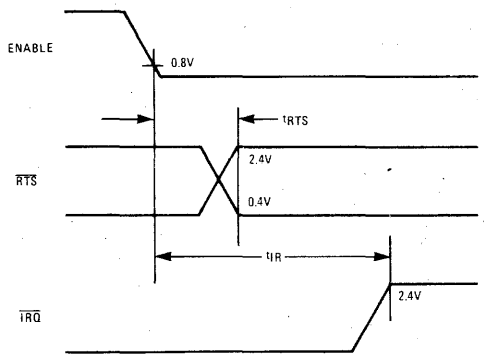


Figure 7. Bus Read Timing Characteristics (Read Information from ACIA)

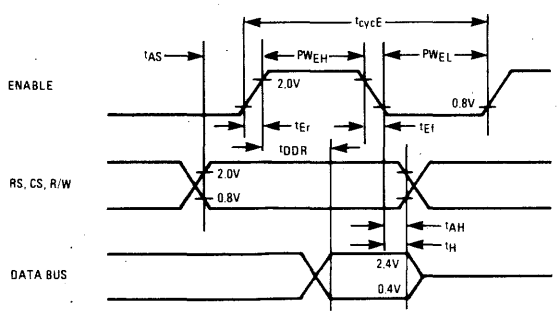
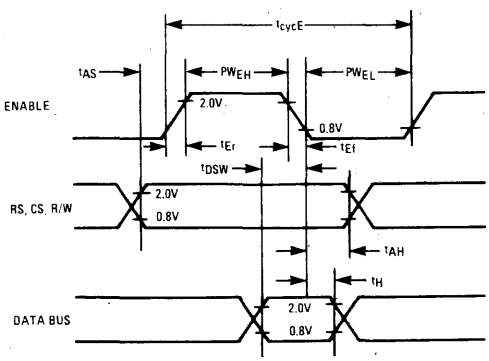


Figure 8. Bus Write Timing Characteristics (Write Information into ACIA)



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SYNCHRONOUS SERIAL DATA ADAPTER (SSDA)

Features

- ☐ Programmable Interrupts from Transmitter, Receiver, and Error Detection Logic
- ☐ Character Synchronization on One or Two Sync Codes
- ☐ External Synchronization Available for Parallel-Serial Operation
- ☐ Programmable Sync Code Register
- ☐ Up to 600kbps Transmission
- ☐ Peripheral/Modem Control Functions
- ☐ Three Bytes of FIFO Buffering on Both Transmit and Receive
- ☐ Seven, Eight, or Nine Bit Transmission
- ☐ Optional Even and Odd Parity
- ☐ Parity, Overrun, and Underflow Status

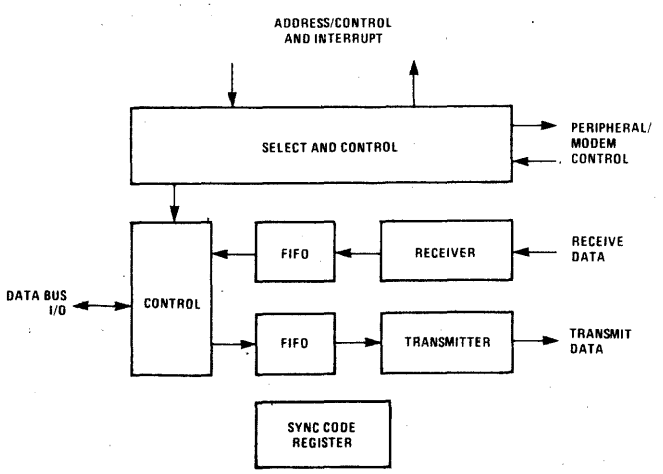
General Description

The S6852 Synchronous Serial Data Adapter provides a bi-directional serial interface for synchronous data information interchange. It contains interface logic for simultaneously transmitting and receiving standard synchronous communications characters in bus organized systems such as the S6800 Microprocessor systems.

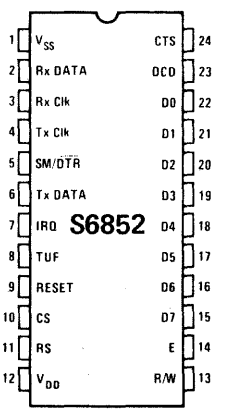
The bus interface of the S6852 includes select, enable, read/write, interrupt, and bus interface logic to allow data transfer over an 8-bit bi-directional data bus. The parallel data of the bus system is serially transmitted and received by the synchronous data interface with synchronization, fill character insertion/deletion, and error checking. The functional configuration of the SSDA is programmed via the data bus during system initialization. Programmable control registers provide control for variable word lengths, transmit control, receive control, synchronization control, and interrupt control. Status, timing and control lines provide peripheral or modem control.

Typical applications include floppy disk controllers, cassette or cartridge tape controllers, data communications terminals, and numerical control systems.

Block Diagram



Pin Configuration



ADVANCED PRODUCT DESCRIPTION

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Maximum Ratings

Supply Voltage	-0.3V to +7.0V
Input Voltage	-0.3V to +7.0V
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	-55°C to +150°C
Thermal Resistance	+70°C/W

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

Electrical Characteristics (V_{CC} = +5.0V ±5%, V_{SS} = 0, T_A = 0°C to 70°C unless otherwise noted.)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
V_{IH}	Input High Voltage	V_{SS} + 2.0			Vdc	
V_{IL}	Input Low Voltage			V_{SS} + 0.8	Vdc	
I_{in}	Input Leakage Current — Tx Clk, Rx Clk, Rx Data, Enable, $\overline{Reset}$, RS, R/$\overline{W}$, $\overline{CS}$, $\overline{DCD}$, $\overline{CTS}$		1.0	2.5	μAdc	V_{in} = 0Vdc to 5.25Vdc
I_{TSI}	Three-State (Off State) Input Current — D0-D7		2.0	10	μAdc	V_{in} = 0.4Vdc to 2.4Vdc, V_{CC} = 5.25Vdc
V_{OH}	Output High Voltage — D0-D7	V_{SS} + 2.4			Vdc	I_{Load} = -205μAdc, Enable Pulse Width <25μs
	Tx Data, $\overline{DTR}$, TUF	V_{SS} + 2.4				I_{Load} = -100μAdc, Enable Pulse Width <25μs
V_{OL}	Output Low Voltage			V_{SS} + 0.4	Vdc	I_{Load} = 1.6mAdc, Enable Pulse Width <25μs
I_{LOH}	Output Leakage Current (Off State) — $\overline{IRQ}$		1.0	10	μAdc	V_{OH} = 2.4Vdc
P_D	Power Dissipation		300	525	mW	
C_{in}	Input Capacitance — D0-D7			12.5	pF	V_{in} = 0, T_A = 25°C, f = 1.0MHz
	Other Inputs			7.5		
C_{out}	Output Capacitance — Tx Data, SM/$\overline{DTR}$, TUF, $\overline{IRQ}$			10	pF	V_{in} = 0, T_A = 25°C, f = 1.0MHz
				5.0		
PW_{CL}	Minimum Clock Pulse Width, Low	700			ns	Figure 1
PW_{CH}	Minimum Clock Pulse Width, High	700			ns	Figure 2
f_C	Clock Frequency			600	kHz	
t_{RDSU}	Receive Data Setup Time	350			ns	Figure 3, 7
t_{RDH}	Receive Data Hold Time	350			ns	Figure 3
t_{SM}	Sync Match Delay Time			1.0	μs	Figure 3
t_{TDD}	Clock-to-Data Delay for Transmitter			1.0	μs	Figure 4
t_{TUF}	Transmitter Underflow			1.0	μs	Figure 4, 6
t_{DTR}	$\overline{DTR}$ Delay Time			1.0	μs	Figure 5
t_{IR}	$\overline{Interrupt\ Request}$ Release Time			1.2	μs	Figure 5
t_{Res}	$\overline{Reset}$ Minimum Pulse Width	1.0			μs	
t_{CTS}	$\overline{CTS}$ Setup Time			200	ns	Figure 6
t_{DCD}	$\overline{DCD}$ Setup Time			500	ns	Figure 7
t_r, t_f	Input Rise and Fall Times (except Enable)			1.0*	μs	0.8V to 2.0V

*1.0μs or 10% of the pulse width, whichever is smaller.

Figure 1. Clock Pulse Width, Low-State

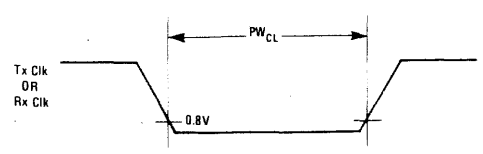
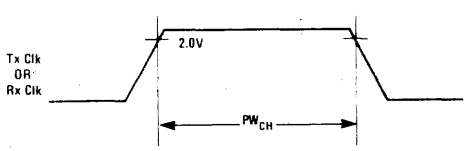


Figure 2. Clock Pulse Width, High-State



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Bus Timing Characteristics

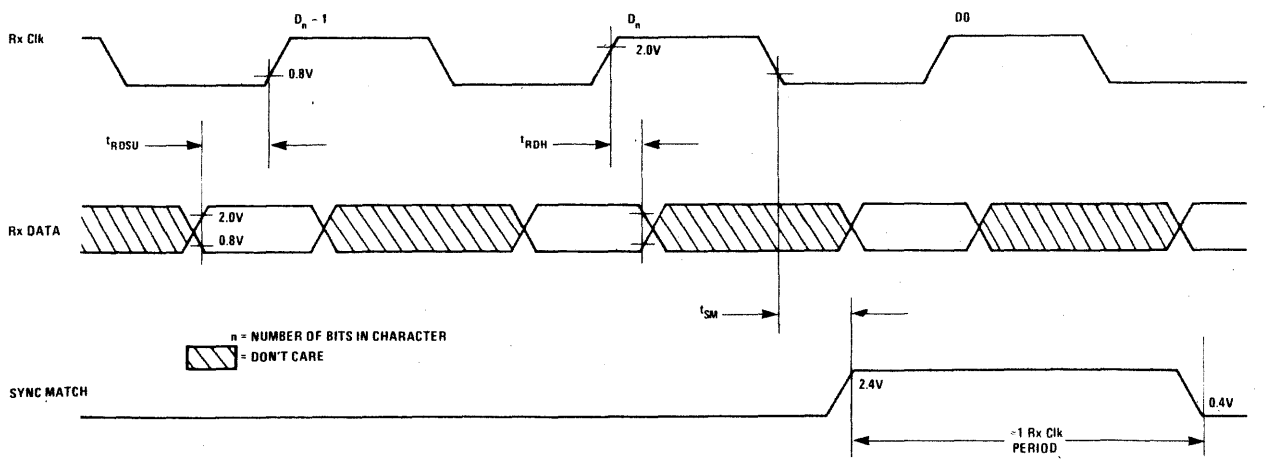
Read

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
t_{cycE}	Enable Cycle Time	1.0			μs	
PW_{EH}	Enable Pulse Width, High	0.45		25	μs	
PW_{EL}	Enable Pulse Width, Low	0.43			μs	
t_{AS}	Setup Time, Address and R/W valid to Enable positive transition	160			ns	Figures 8 and 10
t_{DDR}	Data Delay Time			320	ns	
t_H	Data Hold Time	10			ns	
t_{AH}	Address Hold Time	10			ns	
t_{Er}, t_{Ef}	Rise and Fall Time for Enable input			25	ns	

Write

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
t_{cycE}	Enable Cycle Time	1.0			μs	
PW_{EH}	Enable Pulse Width, High	0.45		25	μs	
PW_{EL}	Enable Pulse Width, Low	0.43			μs	
t_{AS}	Setup Time, Address and R/W valid to Enable positive transition	160			ns	Figures 9 and 10
t_{DSW}	Data Setup Time	195			ns	
t_H	Data Hold Time	10			ns	
t_{AH}	Address Hold Time	10			ns	
t_{Er}, t_{Ef}	Rise and Fall Time for Enable input			25	ns	

Figure 3. Receive Data Setup and Hold Times and Sync Delay Time



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Figure 4. Transmit Data Output Delay and Transmitter Underflow Delay Time

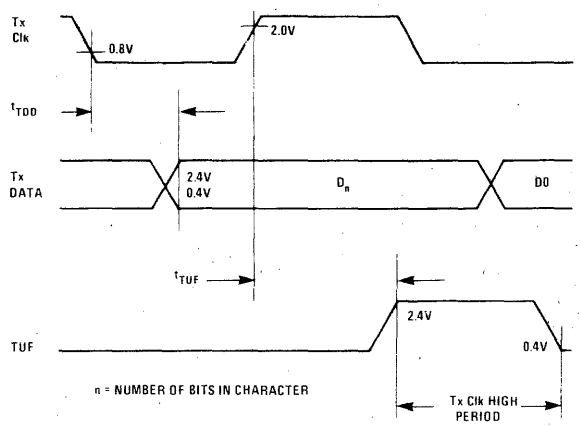


Figure 5. Data Terminal Ready and Interrupt Request Release Times

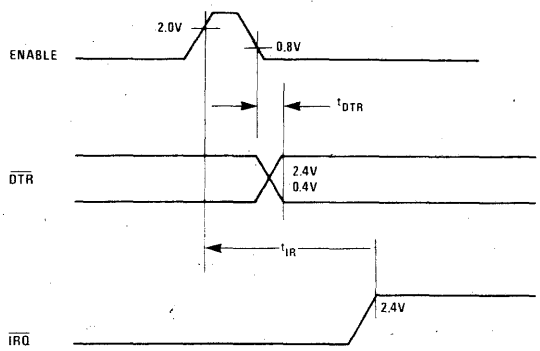


Figure 6. Clear-To-Send Setup Time

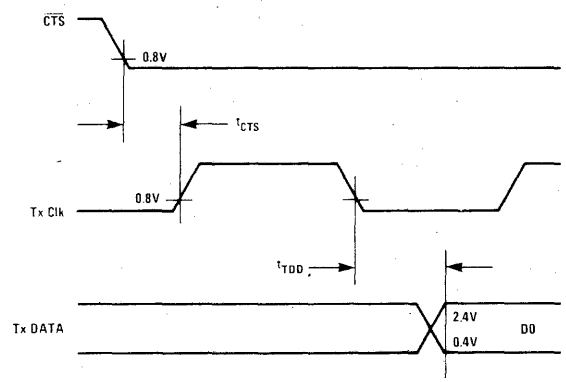


Figure 7. Data Carrier Detect Setup Time

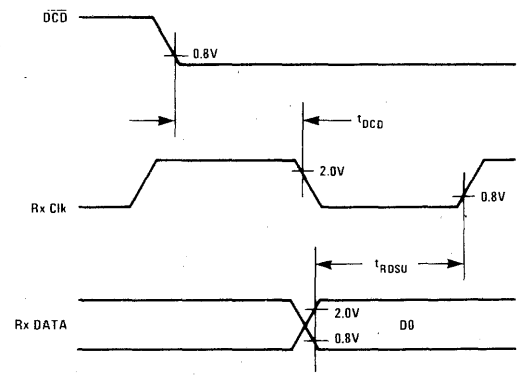


Figure 8. Bus Read Timing Characteristics (Read Information from SSDA)

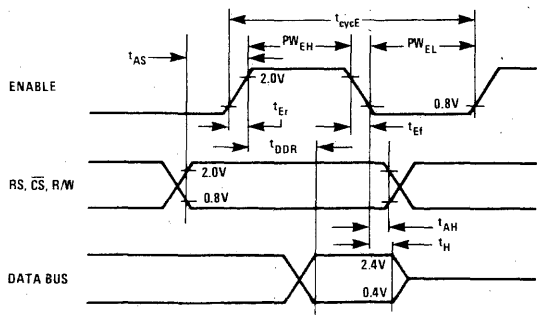
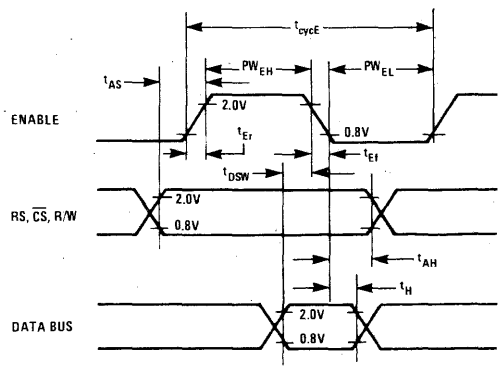


Figure 9. Bus Write Timing Characteristics (Write Information into SSDA)



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ADVANCED DATA LINK CONTROLLER

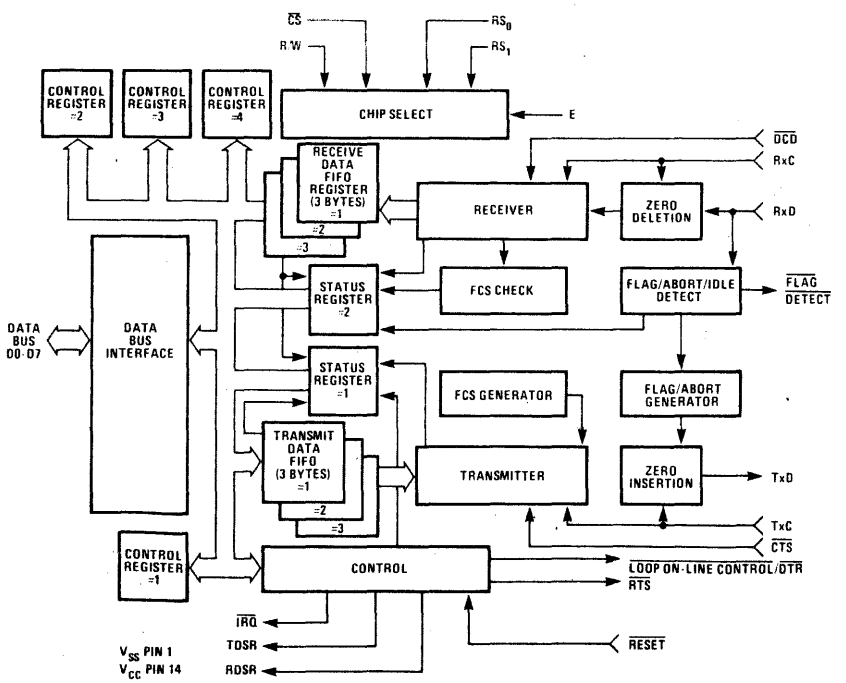
Features

- ☐ S6800 Compatible
- ☐ Protocol Features
  - ☐ Automatic Flag Detection and Synchronization
  - ☐ Zero Insertion and Deletion
  - ☐ Extendable Address, Control and Logical Control Fields (Optional)
  - ☐ Variable Word Length Info Field — 5, 6, 7, or 8-bits
  - ☐ Automatic Frame Check Sequence Generation and Check
  - ☐ Abort Detection and Transmission
  - ☐ Idle Detection and Transmission
- ☐ Loop Mode Operation
- ☐ Loop Back Self-Test Mode
- ☐ NRZ/NRZI Modes
- ☐ Quad Data Buffers for Each Rx and Tx
- ☐ Prioritized Status Register (Optional)
- ☐ MODEM/DMA/Loop Interface
- ☐ MIL-STD-883, Class B and C Devices Available

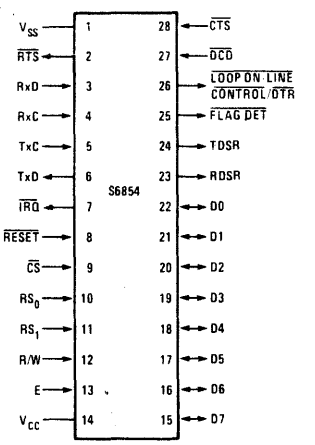
General Description

The S6854 ADLC performs the complex MPU/data communication link function for the "Advanced Data Communication Control Procedure" (ADCCP). High Level Data Link Control (HDLC) and Synchronous Data Link Control (SDLC) standards. The ADLC provides key interface requirements with improved software efficiency. The ADLC is designed to provide the data communications interface for both primary and secondary stations in stand-alone, polling, and loop configurations.

Block Diagram



Pin Configuration



ADVANCED PRODUCT DESCRIPTION

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Absolute Maximum Ratings*

Supply Voltage	-0.3V to +7.0V
Input Voltage	-0.3V to +7.0V
Operating Temperature Range	0°C to +70°C
Industrial Temperature Range	-40°C to +85°C
Military Temperature Range	-55°C to +125°C
Storage Temperature Range	-55°C to +150°C
Thermal Resistance	+70°C/W

*This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

Electrical Characteristics (V_{CC} = 5.0V ± 5%, V_{SS} = 0, T_A = 0°C to 70°C unless otherwise noted.)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
V_{IH}	Input High Voltage	V_{SS}+2.0			Vdc	
V_{IL}	Input Low Voltage			V_{SS}+0.8	Vdc	
I_{IN}	Input Leakage Current All Inputs Except D0 — D7		1.0	2.5	μAdc	V_{IN}=0 to 5.25Vdc
I_{TSI}	Three-State (Off State) Input Current D0 — D7		2.0	10	μAdc	V_{IN}=0.4 to 2.4Vdc V_{CC} = 5.25Vdc
V_{OH}	Output High Voltage D0 — D7 All Others	 V_{SS}+2.4 V_{SS}+2.4			Vdc	 I_{LOAD}=-205μAdc I_{LOAD}=-100μAdc
V_{OL}	Output Low Voltage			V_{SS}+0.4	Vdc	I_{LOAD}=1.6mAdc
I_{LOH}	Output Leakage Current (Off State) $\overline{IRQ}$		1.0	10	μAdc	V_{OH}=2.4Vdc
P_D	Power Dissipation			850	mW	
C_{IN}	Capacitance D0 — D7 All Other Inputs			 12.5 7.5	pF	V_{IN} = 0, T_A=25°C, f = 1.0MHz
C_{OUT}	 $\overline{IRQ}$ All Others			 5.0 10	pF	

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Symbol	Parameter	S6854 Min.	S6854 Max.	S68A54 Min.	S68A54 Max.	Unit	Conditions
PW_{CL}	Minimum Clock Pulse Width, Low	700		450		ns	
PW_{CH}	Minimum Clock Pulse Width, High	700		450		ns	
f_C	Clock Frequency		0.66		1.0	MHz	
t_{RDSU}	Receive Data Setup Time	250		200		ns	
t_{RDH}	Receive Data Hold Time	120		100		ns	
t_{RTS}	Request-to-Send Delay Time		680		460	ns	
t_{TDD}	Clock-to-Data Delay for Transmitter		460		320	ns	
t_{FD}	Flag Detect Delay Time		680		460	ns	
t_{DTR}	DTR Delay Time		680		460	ns	
t_{LOC}	Loop On-Line Control Delay Time		680		460	ns	
t_{RDSR}	RDSR Delay Time		540		400	ns	
t_{TDSR}	TDSR Delay Time		540		400	ns	
t_{IR}	Interrupt Request Release Time		1.2		0.9	μs	
t_{RES}	Reset Minimum Pulse Width	1.0		0.65		μs	
t_r, t_f	Input Rise and Fall Times Except Enable		1.0*		1.0*	μs	0.8V to 2.0V

*1.0μs or 10% of the pulse width, whichever is smaller.

Bus Timing Characteristics (V_{CC} = 5.0V ± 5%, V_{SS} = 0, T_A = 0°C to +70°C unless otherwise noted.)

Read

Symbol	Parameter	S6854 Min.	S6854 Max.	S68A54 Min.	S68A54 Max.	Unit
t_{CYC}	Enable Cycle Time	1.0		0.666		μs
PW_{EH}	Enable Pulse Width, High	0.45		0.28		μs
PW_{EL}	Enable Pulse Width, Low	0.43		0.28		μs
t_{AS}	Setup Time, Address and R/W Valid to Enable positive transition	160		140		ns
t_{DDR}	Data Delay Time		320		220	ns
t_H	Data Hold Time	10		10		ns
t_{AH}	Address Hold Time	10		10		ns
t_{Er}, t_{Ef}	Rise and Fall Time for Enable input		25		25	ns

Write

t_{CYCE}	Enable Cycle Time	1.0		0.666		μs
PW_{EH}	Enable Pulse Width, High	0.45		0.28		μs
PW_{EL}	Enable Pulse Width, Low	0.43		0.28		μs
t_{AS}	Setup Time, Address and R/W Valid to Enable positive transition	160		140		ns
t_{DSW}	Data Setup Time	195		80		ns
t_H	Data Hold Time	10		10		ns
t_{AH}	Address Hold Time	10		10		ns
t_{Er}, t_{Ef}	Rise and Fall Time for Enable input		25		25	ns

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Figure 1. Bus Timing Test Loads

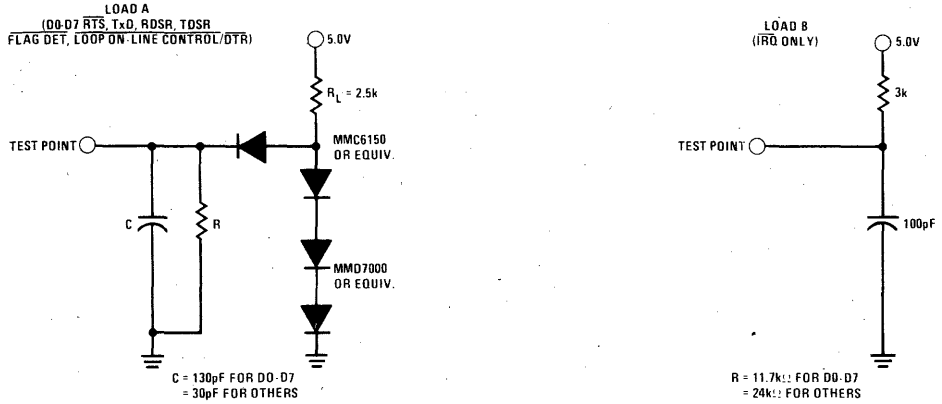


Figure 2. Receiver Data Setup/Hold, Flag Detect and Loop On-Line Control Delay Timing

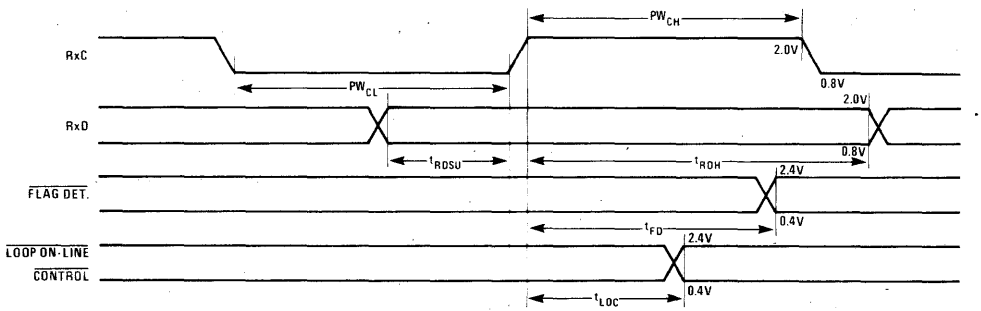


Figure 3. Transmit Data Output Delay and Request to Send Delay Timing

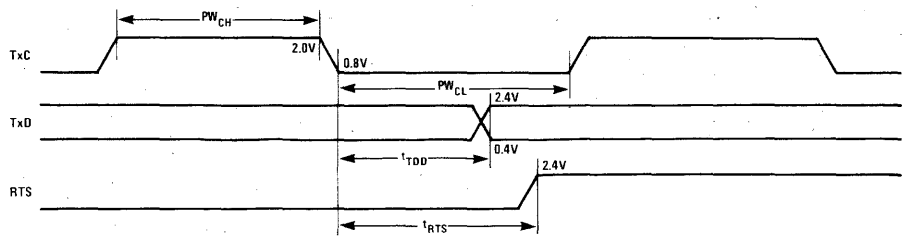
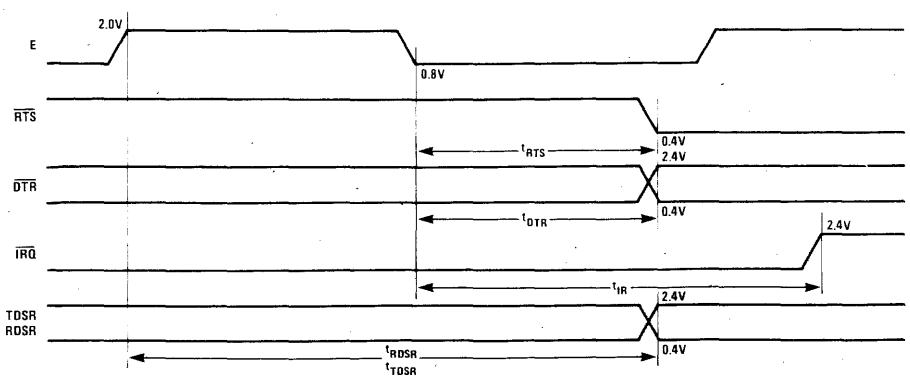


Figure 4. TDSR/RDSR Delays, IRQ Release Delay, RTS and DTR Delay Timing



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S68047

VIDEO DISPLAY GENERATOR

August 1978

Features

- ☐ 32 x 16 (512 total) Alphanumeric Two Color Display on Black Background with Internal or External Character Generator ROM.
- ☐ Two Semigraphics Modes with Display Densities Ranging from 64 x 32 to 64 x 48 in 8 and 4 Color Sets Respectively, plus Black.
- ☐ Full Graphics Modes with Display Densities Ranging from 64 x 64 to 256 x 192 in 2 and 4 Colors.
- ☐ Full NTSC Compatible Composite Video with Choice of Interlaced and Non-interlaced Display Versions.
- ☐ Provides Microprocessor Compatible Interface Signals.
- ☐ Generates Display Refresh RAM Addresses.
- ☐ NMOS Device, Single 5V Supply, TTL Compatible Logic Levels.
- ☐ Color Set Select Pin Can Give 8 Color Displays in Full Graphics Mode.

General Description

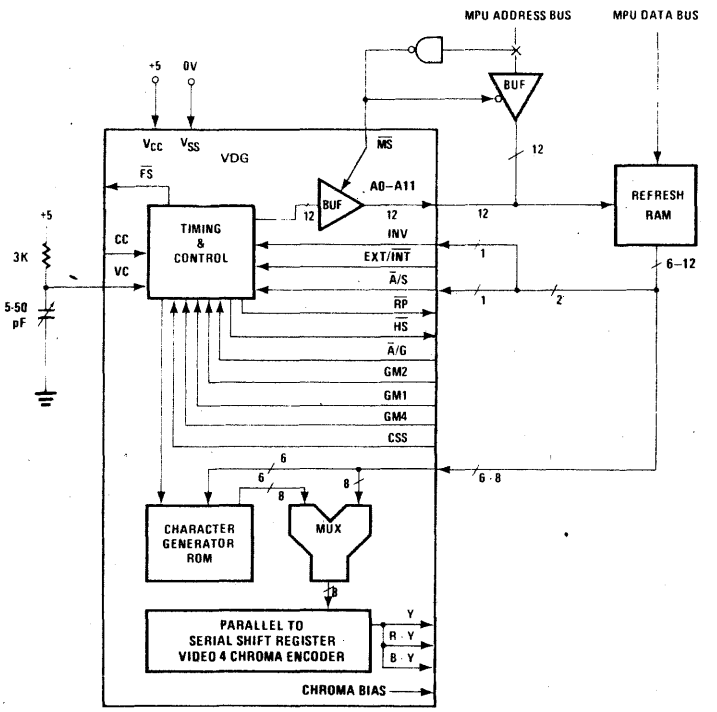
The S68047 Video Display Generator (VDG) is designed to produce composite video suitable for display on a standard American NTSC compatible black/white television or color televison or monitor.

There are three major types of display which the S68047 can generate. These include an alphanumerics mode of which there are two types, each with normal or inverted video; a semigraphics mode of which there are also two types; and full graphics mode of which there are eight types.

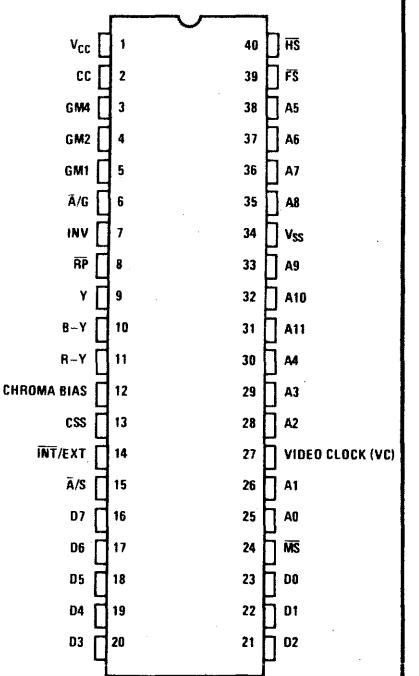
Alphanumeric Modes

The alphanumeric modes, internal and external, enable the S68047 to display a matrix of 32 x 16 (512 total) characters. The internal mode utilizes an on-chip 64 ASCII character ROM to display each character in a 5 x 7 dot matrix font. In the external alphanumeric

Block Diagram



Pin Configuration



MICROPROCESSOR AMI

ADVANCED PRODUCT DESCRIPTION

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General Description (Continued)

mode, an external memory is required, either ROM or RAM, which is used to display the 32 x 16 character matrix with each character located within an 8 x 12 dot matrix of customized font. Switching between internal and external alphanumerics modes and normal and inverted video can be accomplished on a character by character basis.

Semigraphic Modes

The two semigraphic modes, semigraphic 4 (SG4) and semigraphic 6 (SG6), subdivide each of the 512 (32 x 16) character blocks of 8 x 12 dots each into 2 x 2 and 2 x 3 smaller blocks respectively. In SG4 each block is created from 4 x 6 dots and in SG6 each block consists of 4 x 4 dots. In addition the SG4 and SG6 modes can each be displayed in 8 and 4 colors plus black.

Display switching from alphanumerics to semigraphics modes or vice versa during a raster display is called minor mode switching and can take place on a character basis.

Graphics Modes

The eight full graphics modes are divided into two major groups, 4 color and 2 color. The 4 color graphics provide 4 display densities ranging from 64 x 64 for Graphics 0 through to 128 x 192 elements for Graphics 6. The 2 color graphics also provide 4 display densities ranging from 128 x 64 for Graphics 1 through to 256 x 192 elements for Graphics 7. The latter display has the highest density of the eight graphics modes. The amount of display memory increases proportionately with increasing density of display to a maximum of 6K bytes for Graphics 7. Switching between either the alphanumeric modes or semigraphics modes and any of the full graphics modes is called major mode switching. Major mode switching can only occur at the end of every twelfth raster line scan.

Applications

Anywhere data can be more usefully presented graphically on a CRT and for a minimum cost, the VDG in conjunction with a microprocessor based controller can utilize a standard American NTSC compatible TV or monitor for such a purpose. Applications are extremely broad ranging from educational systems, video games, small low cost business/home computers to process control monitors and medical diagnostic displays.

The different modes of operation permit various cost/display presentation tradeoffs. The alphanumerics modes allow use of the TV screen as a video teletype at the most limited level of operation. Only 512 bytes, one for each character, need to be stored, each byte being a minimum of six bits wide per the ASCII code. If video inversion switching or alpha to semigraphics switching is required per character then two extra bits are required in the display RAM as shown in Fig. 5. The semigraphics modes each offer an intermediate range of graphics densities with tradeoffs in density versus color. Typical semigraphics display capabilities are bar graphs, charts, mini displays, etc. which with minor mode switching to alphanumerics modes allow annotation or captioning of the resultant display. The various graphics modes provide greater density displays with greater freedom of display presentations. The tradeoffs in increasing density are with increasing display memory size and color versus density. A minimum Graphics 0 provides a display density of 64 x 64 (4096) elements, each element being composed of a matrix of 12 (4 x 3) dots with a selection of four colors per element. Since each of the even numbered 4 color graphics modes map two bits of the data word to one picture element, each data word of memory provides four picture elements. Thus Graphics 0 requires 4096/4 = 1024 bytes of display RAM, Graphics 2 requires 8192/4 = 2048 and so on. Graphics 1, like all the odd numbered 2 color graphics modes, maps one bit of data word to one picture element. Each data word therefore maps eight elements. Graphics 1 density of 128 x 8 (8192) elements therefore requires 8192/8 = 1024 bytes of display RAM and Graphics 7, the densest display, requires 49, 152/8 = 6144 bytes of RAM. At the higher density graphics displays, the rate of change of elements approaches the maximum dot frequency of 6MHz. This video rate taxes the capabilities of most commercially available television sets and thus the quality of the display system (television or monitor) should be commensurate with the highest video rate to be used.

Electrical Specifications

Absolute Maximum Ratings

Supply Voltage	7.0V
Input Voltage	-0.3V to +7.0V
Operating Temperature	0°C to 70°C
Storage Temperature	-65°C to 150°C

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DC (Static) Characteristics (V_{CC} = 5.0V ± 5% ; T_A = 25°C, unless otherwise specified).

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
V_{IH}	Input Voltage High	2.0		V_{CC}	V	
V_{IH}	Input Voltage High (Color Clock only)	4.0		V_{CC}	V	
V_{IL}	Input Voltage Low	-0.3		+0.6	V	
I_{IN}	Input Leakage Current (all inputs)		1.0	2.5	μA	V_{IN} = 0 - 5.25V; V_{CC} = 0V
$I_{L(TS)}$	Tri-State Output Leakage Current (A0 — A11)			10	μA	V_{CC} = 5.25V; $\overline{MS}$ = 0V; V_{IN} = 0.4 -2.4V
I_{LO}	Output Leakage Current ($\overline{HS}$, $\overline{FS}$, $\overline{RP}$)			10	μA	V_{IN} = 2.4V; V_{CC} = 0V
V_{OH}	Output Voltage High (A0 — A11, $\overline{HS}$, $\overline{FS}$, $\overline{RP}$)	2.4			V	I_{OH} = -100μA ($\overline{HS}$, $\overline{FS}$, $\overline{RP}$); 0μA (A_0 - A_{11}); CL = 30pF
V_{OL}	Output Voltage Low (A0 — A11, $\overline{HS}$, $\overline{FS}$, $\overline{RP}$)			0.4	V	I_{OL} = 1.6mA ($\overline{HS}$, $\overline{FS}$, $\overline{RP}$); 0mA (A_0 - A_{11}); CL = 30pF
I_{CC}	V_{CC} Supply Current		45		mA	V_{CC} = 5V; T_A = 25°C
C_{IN}	Input Capacitance			10	pF	V_{IN} = 0, T_A = 25°C; f = 1.0MHz
C_{OUT}	Output Capacitance			12	pF	V_{IN} = 0, T_A = 25°C; f = 1.0MHz

AC Electrical Characteristics (V_{CC} = 5.0V ± 5%; T_A = 0 - 70°C except where noted).

Alpha Internal Mode (Figure 1)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
f_{vc}	Video Clock Frequency	5.6	6.0	6.4	MHz	
t_{ch}	Character Time	1.43	1.33	1.25	μs	
t_{ACC}	Access-Time of External Refresh RAM			0.7	μs	
t_{dot}	Dot Time	178	166	156	ns	

Alpha External Mode (Figure 1)

NOTE: All parameters are the same as in Alpha Internal Mode except t_{ACC}

t_{ACC}	Access-time of Refresh RAM + Access-time of External ROM			0.7	μs	

Semigraphics Mode (Figure 1)

t_{pic}	Picture Element Duration	712	664	624	ns	

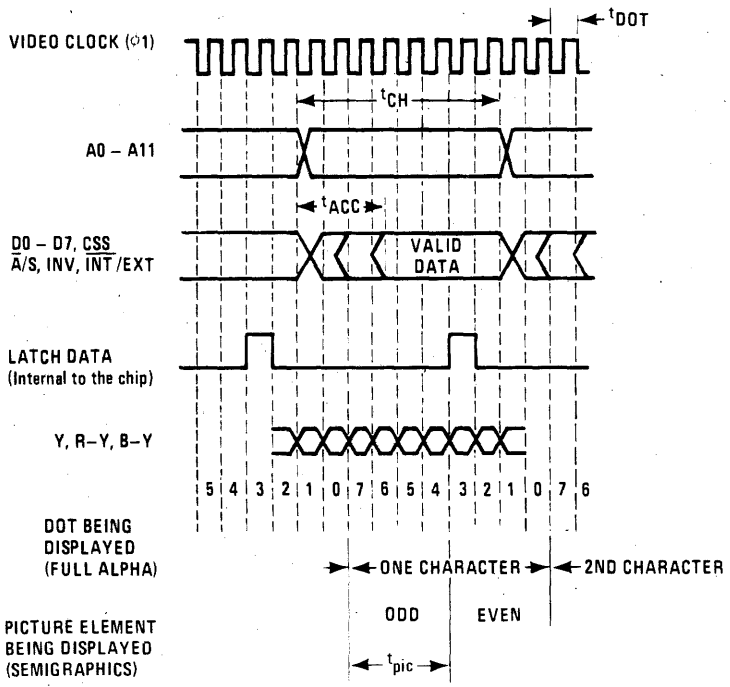
NOTE: All other parameters are the same as in Alpha Internal Mode.

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Color Sub-carrier Input

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
f_{CC}	Frequency		3.579545 ±10 Hz		MHz	
t_r	Rise Time			10	ns	
t_f	Fall Time			10	ns	
PW_{CC}	Pulse Width		140		ns	
V_{IL}	Zero Level			0.6	V	
V_{IH}	One Level	4.0			V	
DR	Duty Ratio	40%	50%	60%		

Figure 1. Refresh RAM Interface Timing



Composite Video Timing (Figure 2)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
t_{SYNC}	Sync duration		4.888889		μs	
t_{fp}	Front Porch duration		1.536508		μs	
t_{BLANK}	Horizontal Blank Duration			11.44	μs	
t_{rs}, t_{fs}	Rise time and Fall time of Horizontal Sync			250	ns	
t_{rv}, t_{fv}	Rise time and Fall time of Horizontal Blank			340	ns	

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S68488

GENERAL PURPOSE INTERFACE ADAPTER

Features

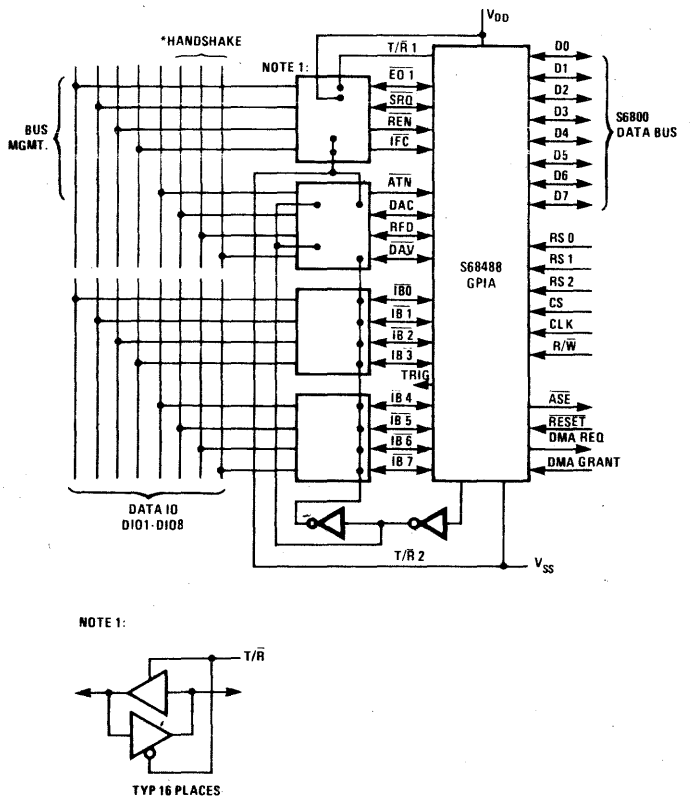
- ☐ Single or Dual Primary Address Recognition
- ☐ Secondary Address Capability
- ☐ Complete Source and Acceptor Handshakes
- ☐ Programmable Interrupts
- ☐ RFD Holdoff to Prevent Data Overrun
- ☐ Operates with DMA Controller
- ☐ Serial and Parallel Polling Capability
- ☐ Talk-Only or Listen-Only Capability
- ☐ Selectable Automatic Features to Minimize Software
- ☐ Synchronization Trigger Output
- ☐ S6800 Bus Compatible

General Description

The S68488 GPIA provides the means to interface between the IEEE488 standard instrument bus and the S6800. The 488 instrument bus provides a means for controlling and moving data from complex systems of multiple instruments.

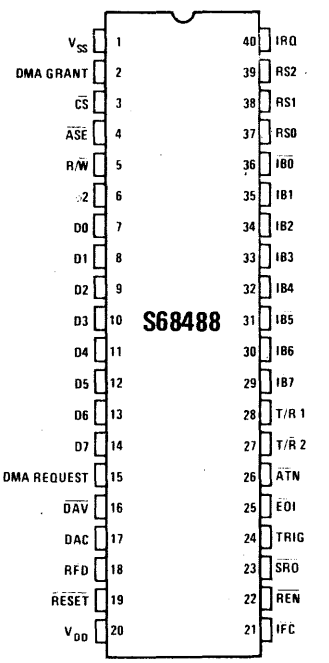
The S68488 will automatically handle all handshake protocol needed on the instrument bus.

Block Diagram



*The 3-wire handshake described is the subject of patents owned by Hewlett-Packard Co.

Pin Configuration



ADVANCED PRODUCT DESCRIPTION

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Functional Description

The IEEE 488 instrument bus standard is a bit-parallel, byte-serial bus structure designed for communiation to and from intelligent instruments. Using this standard, many instruments may be interconnected and remotely and automatically controlled or programmed. Data may be taken from, sent to, or transferred between instruments. A bus controller dictates the role of each device by making the attention line true and sending talk or listen addresses on the instrument bus data lines; those devices which have matching addresses are activated. Device addresses are set into each GPIA from switches or jumpers on a PC board by a microprocessor as a part of the initialization sequence.

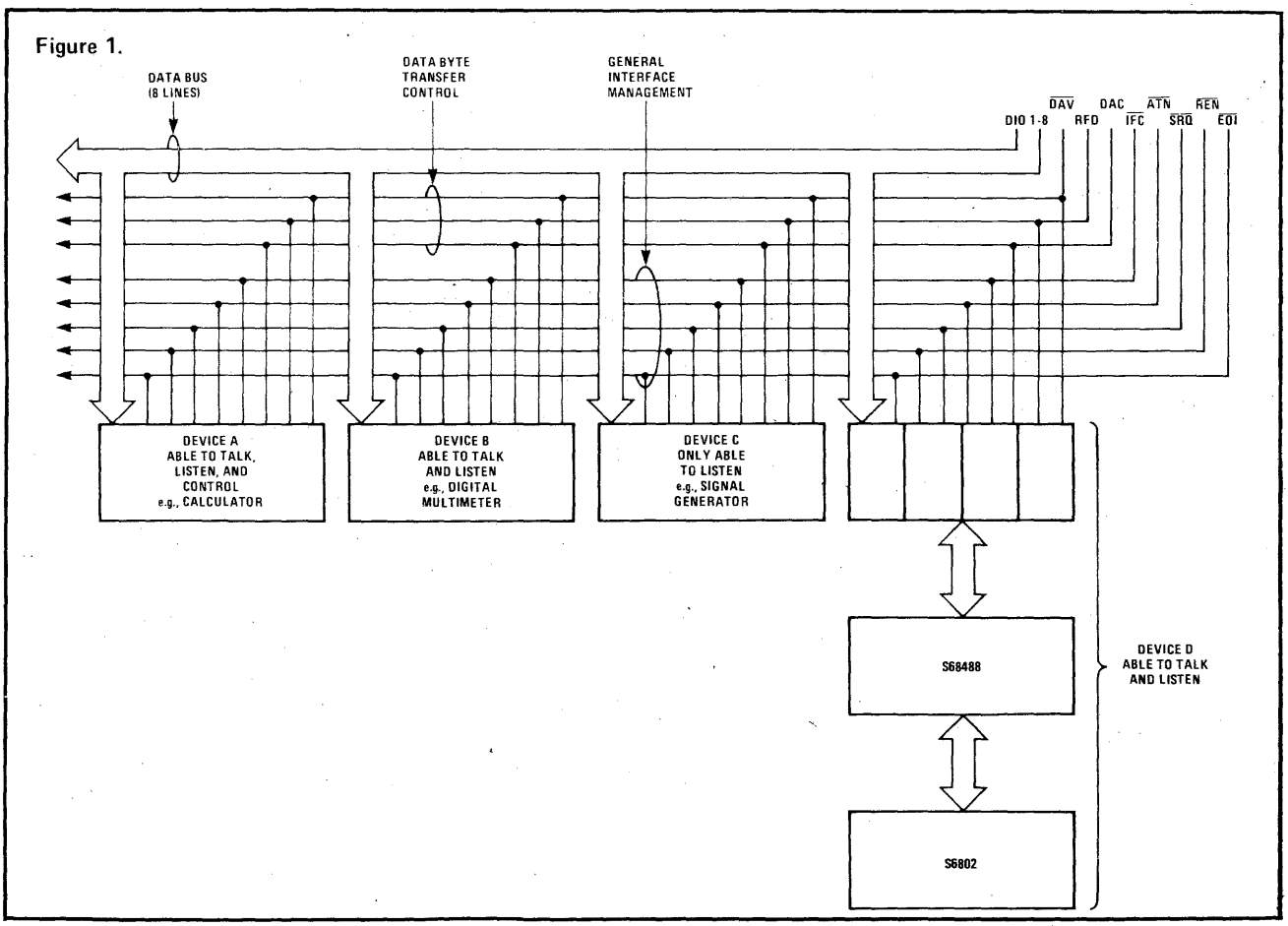
When the controller makes the attention line true, instrument bus commands may also be sent to single or multiple GPIAs.

Information is transmitted on the instrument bus data lines under sequential control of the three handshake lines. No step in the sequence can be initiated until the previous step is completed. Information transfer can proceed as fast as the devices can respond, but no faster than the slowest device presently addressed as active. This permits several devices of different speeds to receive the same data concurrently.

The GPIA is designed to work with standard 488 bus driver Ics (S3448As) to meet the complete electrical specifications of the IEEE488 bus. Additionally, a powered-off instrument may be powered-on without disturbing the 488 bus. With some additional logic, the GPIA could be used with other microprocessors.

The S68488 GPIA has been designed to interface between the S6800 microprocessor and the complex protocol of the IEEE488 instrument bus. Many instrument bus protocol functions are handled automatically by the GPIA and require no additional MPU action. Other functions require minimum MPU response due to a large number of internal registers conveying information on the state of the GPIA and the instrument bus.

Figure 1.



Maximum Ratings

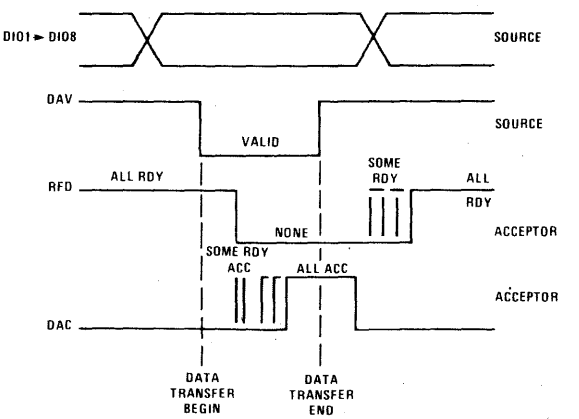
Supply Voltage	-0.3Vdc to +7.0Vdc
Input Voltage	-0.3Vdc to +7.0Vdc
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	-55°C to +150°C
Thermal Resistance	+82.5°C/W

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields, however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high-impedance circuit.

Electrical Characteristics (V_{CC} = 5.0V ±5%, V_{SS} = 0, T_A = 0°C to +70°C unless otherwise noted)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Conditions
V_{IH}	Input High Voltage	V_{SS} + 2.0		V_{CC}	Vdc	
V_{IL}	Input Low Voltage	V_{SS} - 0.3		V_{SS} + 0.8		
I_{IN}	Input Leakage Current		1.0	2.5	μAdc	V_{IN} = 0 to 5.25V
I_{TSI}	Three-State (Off State) Input Current D0-D7		2.0	10	μAdc	V_{IN} = 0.4 to 2.4V
V_{OH}	Output High Voltage D0-D7	V_{SS} + 2.4			Vdc	I_{load} = -205μA
V_{OL}	Output Low Voltage D0-D7			V_{SS} + 0.4	Vdc	I_{load} = 1.6mA
	$\overline{IRQ}$			V_{SS} + 0.4		I_{load} = 3.2mA
I_{LOH}	Output Leakage Current (Off State) $\overline{IRQ}$		1.0	10	μAdc	V_{OH} = 2.4Vdc
P_D	Power Dissipation		600		mW	
C_{IN}	Input Capacitance D0-D7			12.5	pF	V_{IN} = 0,
	All Others			7.5		T_A = 25°C,
						f = 1.0MHz

Figure 2. Source and Acceptor Handshake



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Figure 3. Bus Read Timing Characteristics (Read Information from GPIA)

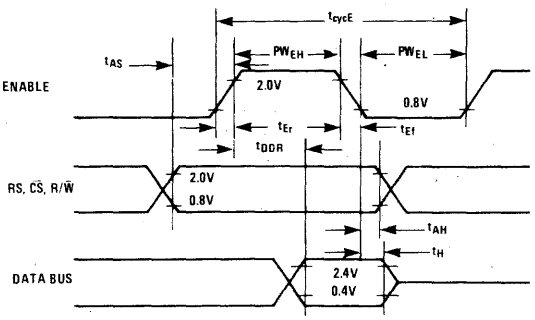


Figure 4. Bus Write Timing Characteristics (Write Information into GPIA)

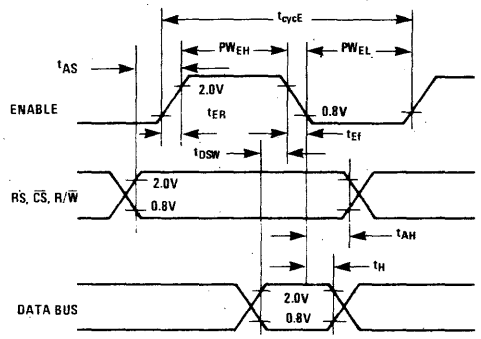
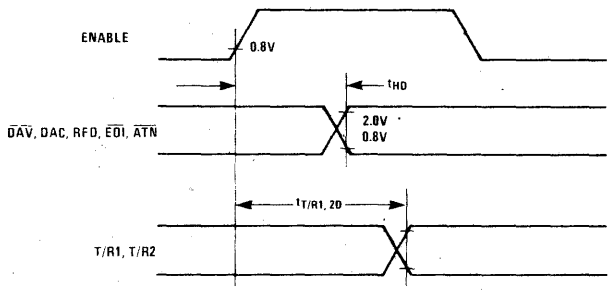


Figure 5. Output Bus Timing



A.C. Time Values

Symbol*	Parameter		Min.	Typ.	Max.	Unit	Conditions
T_1	Settling Time for Multiple Message	SH		⩾2		μs**	
t_2	Response to $\overline{ATN}$	SH, AH, T, L		⩽200		ns	
T_3	Interface Message Accept Time †	AH		>0		∮	
t_4	Response to $\overline{IFC}$ or $\overline{REN}$ False	T, TE, L, LE		<100		μs	
t_5	Response to $\overline{ATN} \bullet \overline{EOI}$	PP		⩽200		ns	

* Time values specified by a lower case t indicate the maximum time allowed to make a state transition. Time values specified by an upper case T indicate the minimum time that a function must remain in a state before exiting.

** If three-state drivers are used on the $\overline{DIO} - \overline{DAV}$ and $\overline{EOI}$ lines, T_1 may be:
(1) ⩾1100ns
(2) Or ⩾700ns if it is known that within the controller $\overline{ATN}$ is driven by a three-state driver.
(3) Or ⩾500ns for all subsequent bytes following the first sent after each false transition of $\overline{ATN}$ [the first byte must be sent in accordance with (1) or (2)].

† Time required for interface functions to accept, not necessarily respond to interface messages.

∮ Implementation dependent.

MPU bus clock rate — The current 6800 bus clock is ⩽ 1MHz but part should operate at 1.5MHz (design goal), with appropriate settling times (T1).

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MDC BASIC INTERPRETER

September 1978

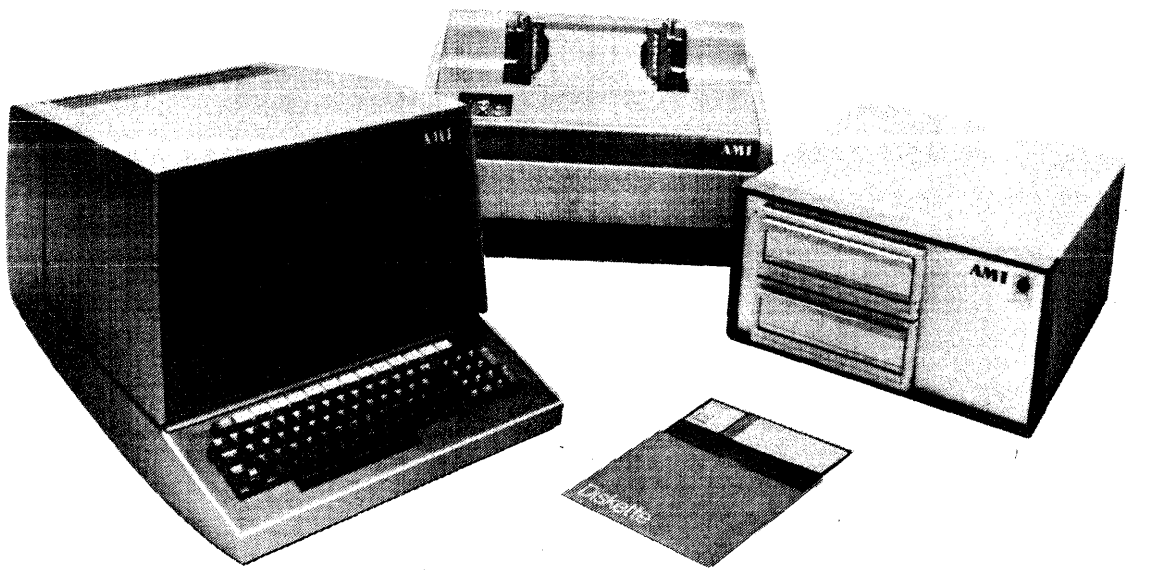
Features

- ☐ **Reduces Software Effort**
- ☐ **Easy Source Code Manipulation**
- ☐ **Instant Program Corrections**
- ☐ **Full Debug Package**
- ☐ **Allows Calls to Machine-Language Subroutine**

General Description

The MDC BASIC Interpreter (SFT27100) operates with AMI's MDC-100 Microcomputer development system to provide an easy to use high level language for performing computation and control functions in the MDC.

MDC BASIC (supplied on floppy disk) is used to edit, translate, debug and execute user-written ASCII source programs in read/write memory (RAM). Each BASIC statement is translated from its ASCII format and then executed by the BASIC interpreter on a line-by-line basis. Because the interpreter executes each line, the need to translate to machine code is avoided. This approach eases source code manipulation, because it is always in memory, and allows instant revision of the program when errors are detected.



ADVANCED PRODUCT DESCRIPTION

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Functional Description

MDC BASIC operates in two modes. In program mode each statement is preceded by a line number. This causes the source statement to be stored in memory for later execution. Statements are stored in increasing order based upon the line number. If no line number precedes the statement, it is executed immediately without being placed in memory. This latter mode, known as "direct" or "immediate", is a means of rapidly gaining solutions to problems where complexity is not great enough to require a program solution. In addition, all control commands are entered in direct mode.

These commands specify actions which alter the status of the user's program; for example, they direct the retrieval, storing and execution on programs. Program statements are summarized in Table 1; control commands are summarized in Table 2.

The BASIC interpreter is loaded in RAM from $20 to $3000.MDC BASIC relies on the intrinsic functions of the MDC-100 for all I/O.

Table 1

ABS — ABSolute value function
ASC — string to ASCII decimal functions
ATAN — arc tangent function
CHR$ — decimal ASCII to string function
CLOSEFILE — close open file verb
CNO (N) — change closed OLD to NEW
COS — COSine function
DATA — internal data list statement
DEF FNA (X) — built in function
DIGITS — numeric display precision
DIM — reserve array storage statement
END — end BASIC program statement
EOFF (N) — test end of file function
EXP (X) — EXPonential base e function
FOR — loop control statement
GOTO — unconditional transfer statement
GOSUB — subroutine call statement
INPUT — request input statement
INT — integer function
LEFT$ — extract substring function
LEN — length of string function
LET — assignment statement
LOG (X) — log base 10 function
MID$ — extract substring function
NEXT — close FOR loop statement
ON — case statement for GOSUB, GOTO
OPENFILE — open data file
PEEK — display memory function
POKE — modify memory function
POS — current print POSition function
PRINT — output statement
READ — read from DATA list statement
REM — REMark (comment) statement
RESTORE — rewind DATA list statement
RESTR (N) — rewind file statement
RETURN — return from GOSUB call
RIGHT$ — extract substring function
RND — RaNDom number function
SGN — SiGNum function
SIN — SINe function
STOP — halt execution statement
STRING — set global string length verb
STR$ — convert numeric to string function
SQR — SQuaRe root function
TAB — print space to column function
TAN — TANgent function
TRACEOFF — cease line trace verb
TRACEON — initiate line trace verb
VAL — convert string to numeric function
USER — call machine language routine

Table 2

ATTACH —
FILETABLE — display file table verb
LIB (N) — display disk directory verb
LINE — set display width verb
LOAD — fetch binary program file from disk
PATCH — return to FDOS verb
PORT — change control port verb
RUN — begin execution of program
SCRATCH — delete current program
TRACEOFF — cease line trace verb
TRACEON — initiate line trace verb
NEW — delete current program verb

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16-BIT MICROPROCESSOR

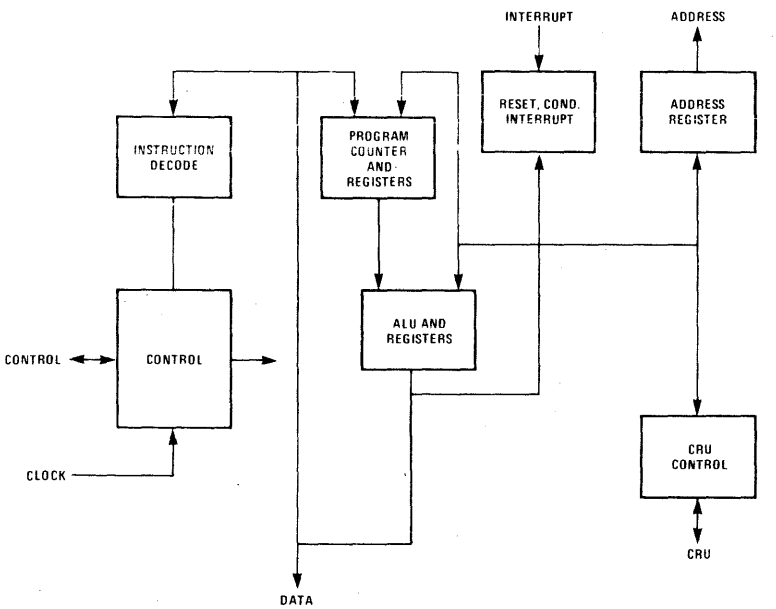
Features

- ☐ 16-Bit Instruction Word
- ☐ Full Minicomputer Instruction Set Capability including Multiply and Divide
- ☐ Up to 65,536 Bytes of Memory
- ☐ 3.3MHz Speed
- ☐ Advanced Memory-to-Memory Architecture
- ☐ Separate Memory, I/O and Interrupt-Bus Structures
- ☐ 16 General Registers
- ☐ 16 Prioritized Interrupts
- ☐ Programmed and DMA I/O Capability
- ☐ N-Channel Silicon-Gate Technology

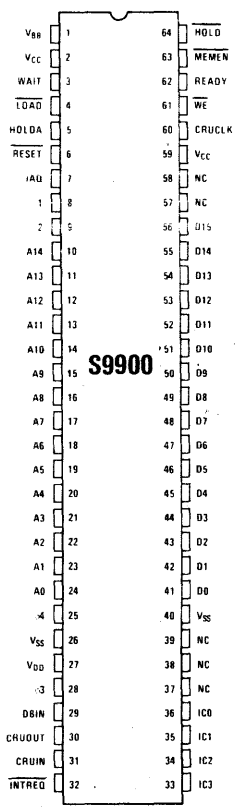
General Description

The S9900 microprocessor is a single-chip 16-bit central processing unit (CPU) produced using N-channel silicon-gate MOS technology. The instruction set of the S9900 includes the capabilities offered by full minicomputers. The unique memory-to-memory architecture features multiple register files, resident in memory, which allow faster response to interrupts and increased programming flexibility. The separate bus structure simplifies the system design effort. AMI provides a compatible set of MOS memory and support circuits to be used with an S9900 system. The system is fully supported by software and complete prototyping systems.

Block Diagram



Pin Configuration



ADVANCED PRODUCT DESCRIPTION

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S9900 Electrical and Mechanical Specifications

Absolute Maximum Ratings Over Operating Free-Air Temperature Range (unless otherwise noted)*

Supply Voltage, V_{CC} (See Note 1) ..... −0.3V to +20V
Supply Voltage, V_{DD} (See Note 1) ..... −0.3V to +20V
Supply Voltage, V_{SS} (See Note 1) ..... −0.3V to +20V
All Input Voltages (See Note 1) ..... −0.3V to +20V
Output Voltage (with Respect to V_{SS}) ..... −2V to +7V
Continuous Power Dissipation ..... +1.2W
Operating Free-Air Temperature Range ..... 0°C to +70°C
Storage Temperature Range ..... −55°C to +150°C

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Under absolute maximum ratings voltage values are with respect to the most negative supply, V_{BB} (substrate), unless otherwise noted. Throughout the remainder of this section, voltage values are with respect to V_{SS}.

Recommended Operating Conditions

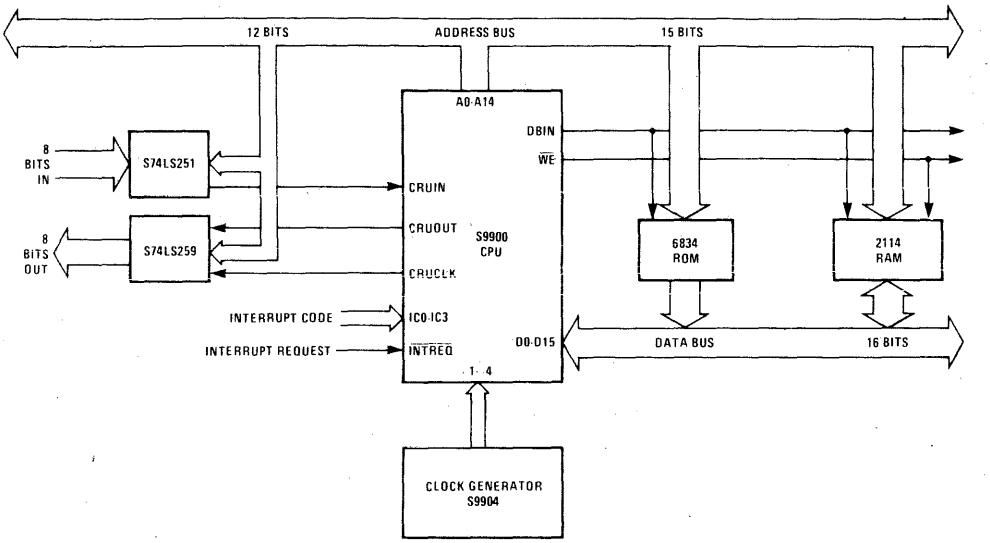
Symbol	Parameter	Min.	Nom.	Max.	Unit	Conditions
V_{BB}	Supply voltage	-5.25	-5	-4.75	V	
V_{CC}	Supply voltage	4.75	5	5.25	V	
V_{DD}	Supply voltage	11.4	12	12.6	V	
V_{SS}	Supply voltage		0		V	
V_{IH}	High-level input voltage (all inputs except clocks)	2.2	2.4	V_{CC}+1	V	
$V_{IH(\phi)}$	High-level clock input voltage	V_{DD}-2		V_{DD}	V	
V_{IL}	Low-level input voltage (all inputs except clocks)	-1	0.4	0.8	V	
$V_{IL(\phi)}$	Low-level clock input voltage	-0.3	0.3	0.6	V	
T_A	Operating free-air temperature	0		70	°C	

Timing Requirements Over Full Range of Recommended Operating Conditions (See Figures 1 and 2)

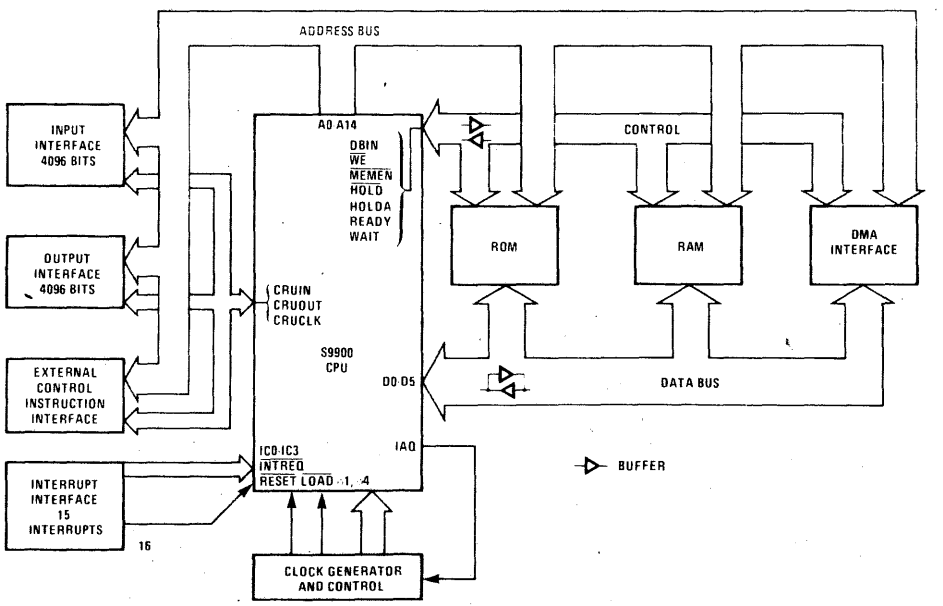
Symbol	Parameter	Min.	Nom.	Max.	Unit	Conditions
$t_{c(\phi)}$	Clock cycle time	0.3	0.333	0.5	μs	
$t_{r(\phi)}$	Clock rise time	10	12		ns	
$t_{f(\phi)}$	Clock fall time	10	12		ns	
$t_{w(\phi)}$	Pulse width, any clock high	40	45	100	ns	
$t_{\phi 1L, \phi 2H}$	Delay time, clock 1 low to clock 2 high (time between clock pulses)	0	5		ns	
$t_{\phi 2L, \phi 3H}$	Delay time, clock 2 low to clock 3 high (time between clock pulses)	0	5		ns	
$t_{\phi 3L, \phi 4H}$	Delay time, clock 3 low to clock 4 high (time between clock pulses)	0	5		ns	
$t_{\phi 4L, \phi 1H}$	Delay time, clock 4 low to clock 1 high (time between clock pulses)	0	5		ns	
$t_{\phi 1H, \phi 2H}$	Delay time, clock 1 high to clock 2 high (time between leading edges)	70	80		ns	
$t_{\phi 2H, \phi 3H}$	Delay time, clock 2 high to clock 3 high (time between leading edges)	70	80		ns	
$t_{\phi 3H, \phi 4H}$	Delay time, clock 3 high to clock 4 high (time between leading edges)	70	80		ns	
$t_{\phi 4H, \phi 1H}$	Delay time, clock 4 high to clock 1 high (time between leading edges)	70	80		ns	
t_{su}	Data or control setup time before clock 1	30			ns	
t_h	Data hold time after clock 1	10			ns	

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Minimum S9900 System

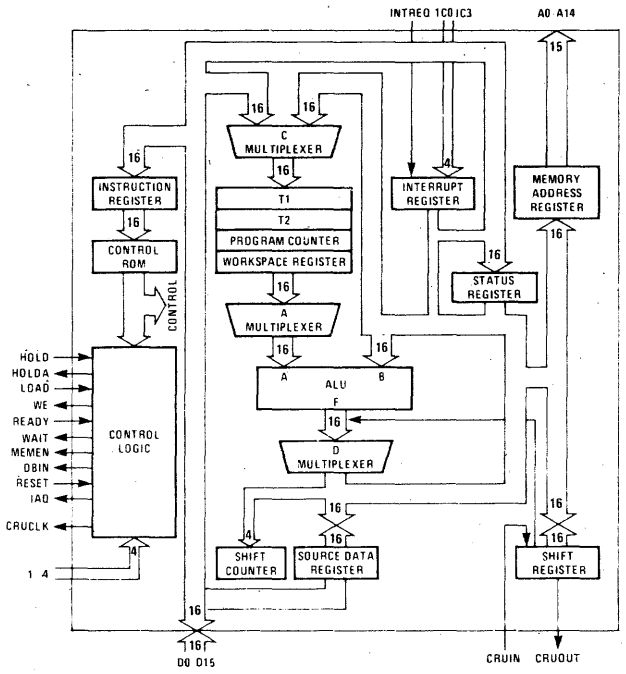


Maximum S9900 System



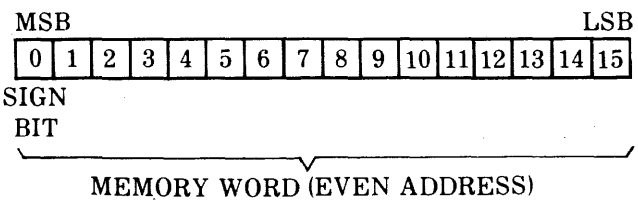
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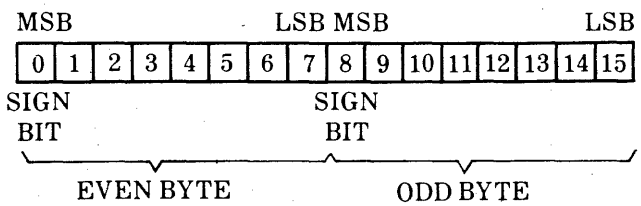
Architecture



Registers and Memory

The S9900 employs an advanced memory-to-memory architecture. Blocks of memory designated as workspace replace internal-hardware registers with program-data registers. The memory word of the S9900 is 16 bits long. Each word is also defined as 2 bytes of 8 bits. The instruction set of the S9900 allows both word and byte operands. Thus, all memory locations are on even address boundaries and byte instructions can address either the even or odd byte. The memory space is 65,536 bytes or 32,768 words. The word and byte formats are shown below.





The S9900 memory map is shown in Figure 8. The first 32 words are used for interrupt trap vectors. The next contiguous block of 32 memory words is used by the extended operation (XOP) instruction for trap vectors. The last two memory words, $FFFC_{16}$ and $FFFE_{16}$, are used for the trap vector of the LOAD signal. The remaining memory is then available for programs, data, and workspace registers. If desired, any of the special areas may also be used as general memory.

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Programmable Systems Interface Circuit

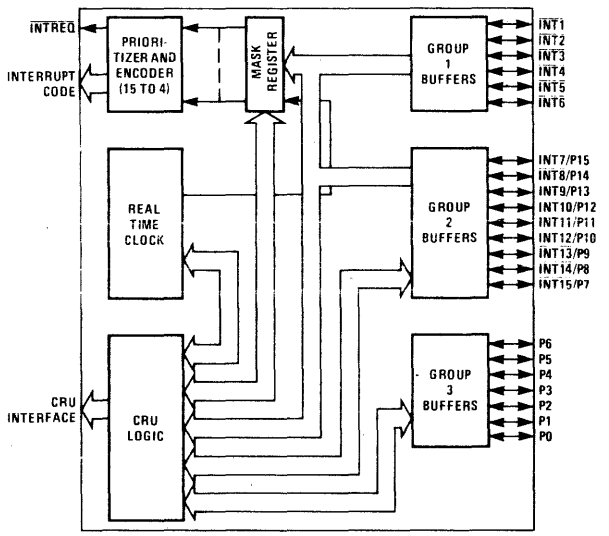
Features

- N-channel Silicon-Gate Process
- 9900 Series CRU Peripheral
- Performs Interrupt and I/O Interface Functions
  - 6 Dedicated Interrupt Input Lines
  - 7 Dedicated I/O Ports
  - 9 Ports Programmable as Interrupts or I/O
- Easily Stacked for Interrupt and I/O Expansion
- Interval and Event Timer
- Single 5V Supply

General Description

The S9901 Programmable Systems Interface is a multifunctioned component designed to provide low cost interrupts and I/O ports in a 9900/9980 microprocessor system. It is fabricated with N-channel silicon-gate technology and is completely TTL compatible on all inputs including the power supply (+5V) and single-phase clock. Figure 1 is a block diagram of the S9901. The Programmable Systems Interface provides a 9900/9980 system with interrupt control, I/O ports, and a real-time clock as shown in Figure 2.

Figure 1. Block Diagram



S9901 Pin Configuration

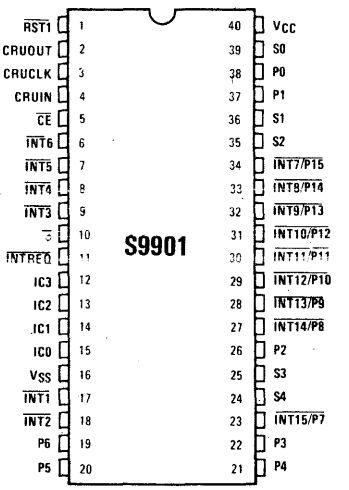
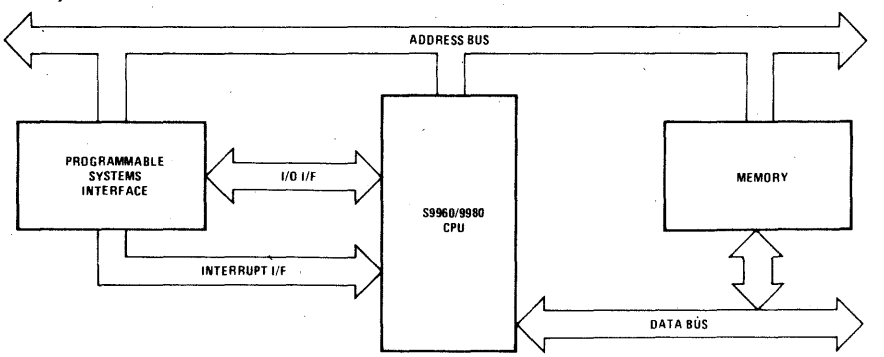


Figure 2. 9900/9980 System



ADVANCED PRODUCT DESCRIPTION

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S9901 PIN ASSIGNMENTS AND FUNCTIONS

SIGNATURE	PIN	I/O	DESCRIPTION
$\overline{\text{INTREQ}}$	11	OUT	INTERRUPT Request. When active (low) $\overline{\text{INTREQ}}$ indicates that an enabled interrupt has been received. $\overline{\text{INTREQ}}$ will stay active until all enabled interrupt inputs are removed.
IC0 (MSB)	15	OUT	Interrupt Code lines. IC0-IC3 output the binary code corresponding to the highest priority enabled interrupt. If no enabled interrupts are active IC0-IC3 = (1, 1, 1, 1).
IC1	14	OUT	
IC2	13	OUT	
IC3 (LSB)	12	OUT	
$\overline{\text{CE}}$	5	IN	Chip Enable. When active (low) data may be transferred through the CRU interface to the CPU. $\overline{\text{CE}}$ has no effect on the interrupt control section.
S0	39	IN	Address select lines. The data bit being accessed by the CRU interface is specified by the 5-bit code appearing on S0-S4.
S1	36	IN	
S2	36	IN	
S3	25	IN	
S4	24	IN	
CRUIN	4	OUT	CRU data in (to CPU). Data specified by S0-S4 is transmitted to the CPU by CRUIN. When $\overline{\text{CE}}$ is not active CRUIN is in a high-impedance state.
CRUOUT	2	IN	CRU data out (from CPU). When $\overline{\text{CE}}$ is active, data present on the CRUOUT input will be sampled during CRUCLK and written into the command bit specified by S0-S4.
CRUCLK	3	IN	CRU Clock (from CPU). CRUCLK specifies that valid data is present on the CRUOUT line.
$\overline{\text{RST}}1$	1	IN	Power Up Reset. When active (low) $\overline{\text{RST}}1$ resets all interrupt masks to "0", disables the clock, and programs all I/O ports to inputs. $\overline{\text{RST}}1$ has a Schmitt-Trigger input to allow implementation with an RC circuit as shown in Figure 6.
V_{CC}	40		Supply Voltage. +5V nominal.
V_{SS}	16		Ground Reference.
$\overline{\phi}$	10		System clock ($\overline{\phi}3$ in S9900 system, $\overline{\text{CKOUT}}$ in S9980 system).
$\overline{\text{INT}}1$	17	IN	Group 1, interrupt inputs. When active (low) the signal is ANDed and its corresponding mask bit and if enabled sent to the interrupt control section. INT1 has highest priority.
$\overline{\text{INT}}2$	18	IN	
$\overline{\text{INT}}3$	9	IN	
$\overline{\text{INT}}4$	8	IN	
$\overline{\text{INT}}5$	7	IN	
$\overline{\text{INT}}6$	6	IN	
$\overline{\text{INT}}7$/P15	34	I/O	Group 2, programmable interrupt (active low) or I/O pins (true logic). Each pin is individually programmable as an interrupt, an input port, or an output port.
$\overline{\text{INT}}8$/P14	33	I/O	
$\overline{\text{INT}}9$/P13	32	I/O	
$\overline{\text{INT}}10$/P12	31	I/O	
$\overline{\text{INT}}11$/P11	30	I/O	
$\overline{\text{INT}}12$/P10	29	I/O	
$\overline{\text{INT}}13$/P9	28	I/O	
$\overline{\text{INT}}14$/P8	27	I/O	
$\overline{\text{INT}}15$/P7	23	I/O	
P0	38	I/O	Group 3, I/O ports (true logic). Each pin is individually programmable as an input port or an output port.
P1	37	I/O	
P2	26	I/O	
P3	22	I/O	
P4	21	I/O	
P5	20	I/O	
P6	19	I/O	

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Asynchronous Communications Controller (ACC)

Features

- 5- to 8-Bit Character Length
- 1, 1 1/2, or 2 Stop Bits
- Even, Odd, or No Parity
- Fully Programmable Data Rate Generation
- Interval Timer with Resolution from 64 to 16,320 μs
- Fully TTL Compatible, Including Single Power Supply.

General Description

The S9902 Asynchronous Communication Controller (ACC) is a peripheral device for the S9900 family of microprocessors. The ACC provides an interface between the microprocessor and a serial asynchronous communication channel, performing the timing and data serialization and deserialization, thus facilitating the control of the asynchronous channel by the microprocessor.

Figure 1. Block Diagram

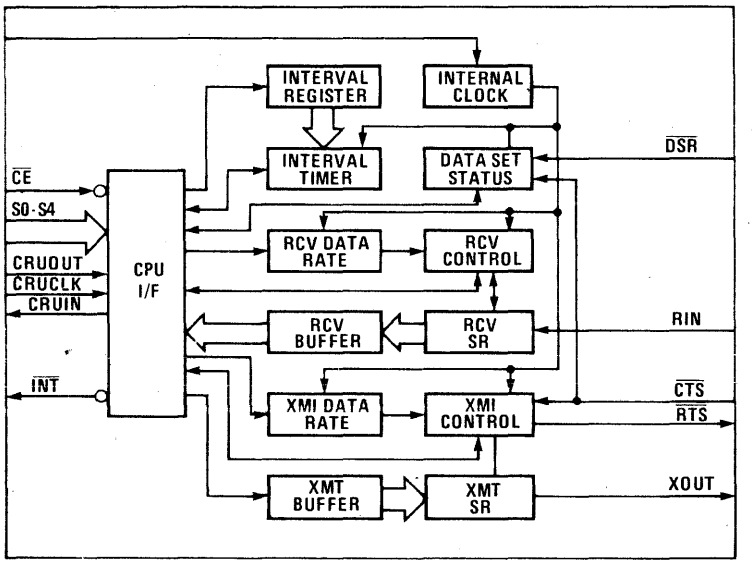
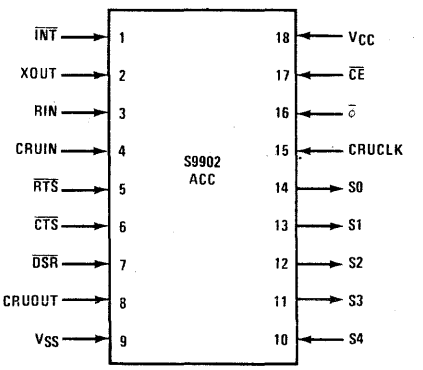
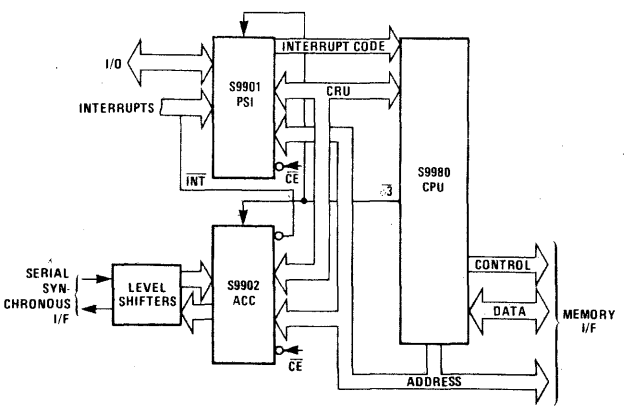


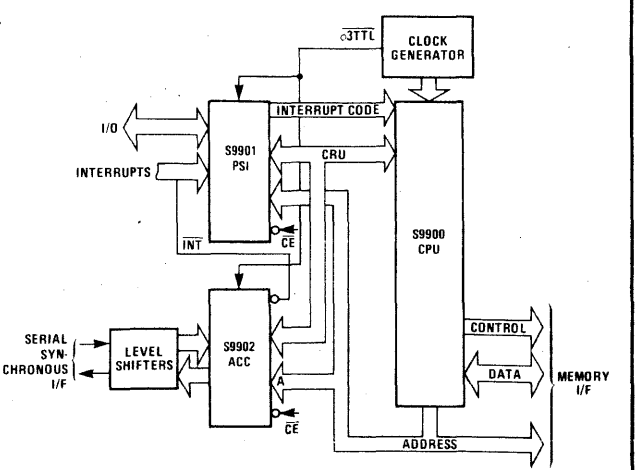
Figure 2. Pin Configuration



S9902 ACC IN A S9900 SYSTEM



S9902 ACC IN A S9980 SYSTEM



ADVANCED PRODUCT DESCRIPTION

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S9902 Pin Description

Table 1 defines the S9902 pin assignments and describes the function of each pin as shown in Figure 2.

Table 1

Signature	Pin	I/O	Description
$\overline{INT}$	1	O	Interrupt — when active (low), the $\overline{INT}$ output indicates that at least one of the interrupt conditions has occured.
XOUT	2	O	Transmitter serial data output line — XOUT remains inactive (high) when S9902 is not transmitting.
RIN	3	I	Receiver serial data input line — RCV — must be held in the inactive (high) state when not receiving data. A transition from high to low will activate the receiver circuitry.
CRUIN	4	O	Serial data output pin from S9902 to CRUIN input pin of the CPU.
$\overline{RTS}$	5	O	Request-to-send output from S9902 to modem. This output is enabled by the CPU and remains active (low) during transmission from the S9902.
$\overline{CTS}$	6	I	Clear-to-send input from modem to S9902. When active (low), it enables the transmitter section of S9902.
$\overline{DSR}$	7	I	Data set ready input from modem to S9902. This input generates an interrupt when going On or Off.
CRUOUT	8	I	Serial data input line to S9902 from CRUOUT line of the CPU.
V_{SS}	9	I	Ground reference voltage.
S4 (LSB)	10	I	
S3	11	I	
S2	12	I	
S1	13	I	Address bus S0-S4 are the lines that are addressed by the CPU to select a particular S9902 function.
S0	14	I	
CRUCLK	15	I	CRU Clock. When active (high), S9902 from CRUOUT line of the CPU.
$\overline{\phi}$	16	I	TTL Clock.
$\overline{CE}$	17	I	Chip enable — when CE is inactive (high), the S9902 address decoding is inhibited which prevents execution of any S9902 command function. CRUIN remains at high-impedance when $\overline{CE}$ is inactive (high).
V_{CC}	18	I	Supply voltage (+5V nominal).

Device Interface

The relationship of the ACC to other components in the system is shown in Figures 4 and 5. The ACC is connected to the asychronous channel through level shifters which translate the TTL inputs and outputs to the appropriate levels (e.g., RS-232C, TTY current loop, etc.). The microprocessor transfers data to and from the ACC via the Communication Register Unit (CRU).

CPU Interface

The ACC interfaces to the CPU through the Communication Register Unit (CRU). The CRU interface consists of five address-select lines (S0-S4), chip enable ($\overline{CE}$), and three CRU control lines (CRUIN, CRUOUT, and CRUCLK). When $\overline{CE}$ becomes active (low), the five select lines address the CRU bit being accessed. When data is being transferred to the ACC from the CPU, CRUOUT contains the valid datum which is strobed by CRUCLK. When ACC data is being read, CRUIN is the datum output by the ACC.

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SYNCHRONOUS COMMUNICATIONS CONTROLLER

Features

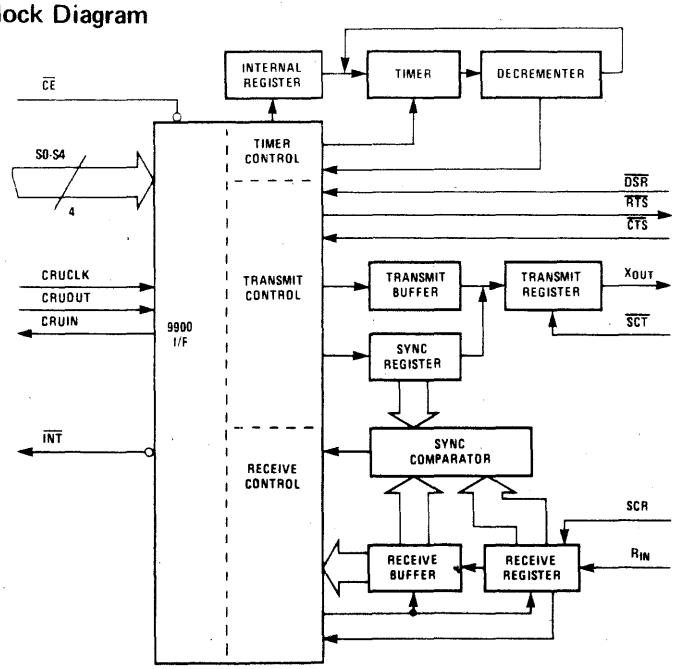
- ☐ **Versatile CRU interface to synchronous and asynchronous serial devices for the S99XX series of microprocessors**
- ☐ **DC to 250 KBPS data rate, half- or full-duplex**
- ☐ **Dynamic character length selection**
- ☐ **Line protocols include BI-SYNC, SDLC, and HDLC, as well as others**
- ☐ **Programmable-polynominal CRC generation and detection**
- ☐ **Interface to unclocked or NRZI data with 32x clocks**
- ☐ **Two programmable sync registers**
- ☐ **Interval timer [64μs to 16.32ms] on chip**
- ☐ **Automatic zero insert and delete for SDLC and HDLC**
- ☐ **Single +5V supply, 20-pin DIP, all inputs and outputs TTL compatible**
- ☐ **N-channel Silicon-Gate technology**

General Description

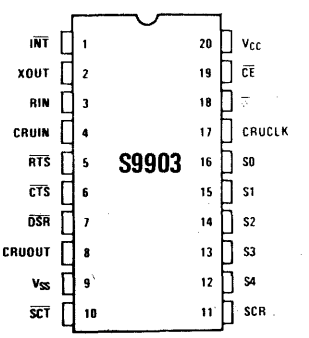
The S9903 is a versatile device which provides the system designer with a wide range of capabilities in synchronous and asynchronous communications control. The S9903 operates in a multi-mode configuration that allows a broad range in the degree of active participation required in the control of high-speed serial communications. Most synchronous data-link control protocols can be supported through software control of sync and fill characters, timing, CRC generation and detection, etc. Established protocols such as BI-SYNC, SDLC, and HDLC are implemented directly in hardware, with others implemented through various combinations of hardware and software.

Universal applicability is further assured through the capability for dynamic character length selection from 5- to 9-bit data words plus parity. Definition and operation of all communications control is under software control and as such make upgrading to another protocol simply a matter of changing software with no hardware changes required.

Block Diagram



Pin Configuration

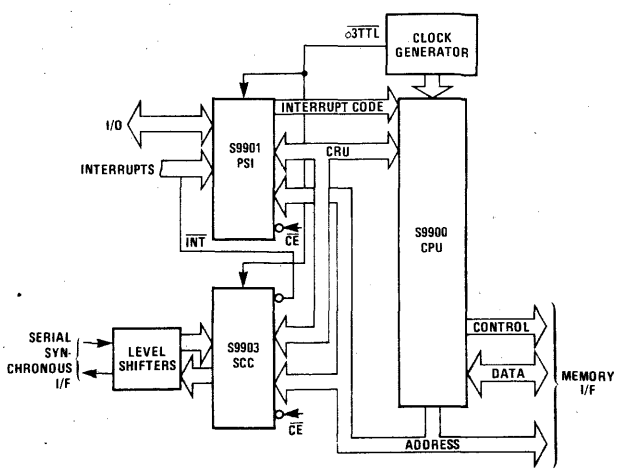


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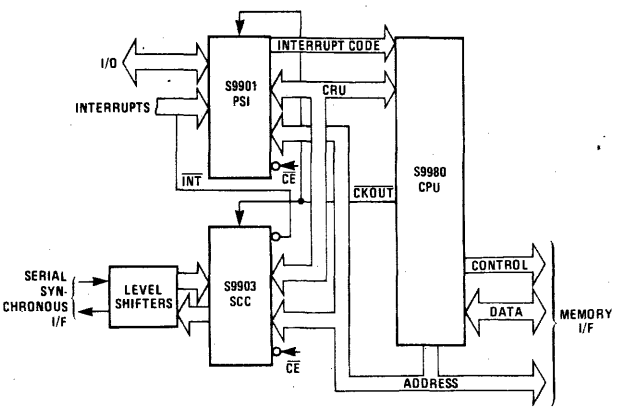
S9903 PIN ASSIGNMENTS AND FUNCTIONS

SIGNATURE	PIN	I/O	DESCRIPTION
$\overline{INT}$	1	OUT	Interrupt — When active (low), the $\overline{INT}$ output indicates that at least one of the interrupt conditions has occurred.
XOUT	2	OUT	Transmitter serial data output line.
RIN	3	IN	Receiver serial data input line.
CRUIN	4	OUT	Serial Data Output line from S9903 to CRUIN input line of the CPU.
$\overline{RTS}$	5	OUT	Request to Send output from S9903 to modem. This output is enabled by the CPU and remains active (low) during data transmission from S9903.
$\overline{CTS}$	6	IN	Clear-to-send input from modem to S9903. When active (low), it enables the transmitter section of the S9903.
$\overline{DSR}$	7	IN	Data Set Ready input from modem to S9903. This input generates an interrupt when going On or Off.
CRUOUT	8	IN	Serial data input line to S9903 from CRUOUT line of the CPU.
V_{SS}	9	IN	Ground Reference Voltage
$\overline{SCT}$	10	IN	Transmit clock — Transmitter data is shifted out on one-to-zero transition of $\overline{SCT}$.
SCR	11	IN	Receiver clock — Receiver serial data (RIN) is sampled at zero-to-one transition of SCR.
S4(LSB)	12	IN	Address bus S0-S4 are the lines that are addressed by the CPU to select a particular S9903 function.
S3	13	IN	
S2	14	IN	
S1	15	IN	
S0(MSB)	16	IN	
CRUCLK	17	IN	CRU Clock. When active (high), S9903 samples the input data on CRUOUT line.
$\overline{\phi}$	18	IN	TTL Clock
$\overline{CE}$	19	IN	Chip Enable — When $\overline{CE}$ is inactive (high), the S9903 address decoding is inhibited. CRUIN remains at high impedance when $\overline{CE}$ is inactive (high).
V_{CC}	20	IN	Supply voltage (+5V nominal)

S9903 SCC IN A S9900 SYSTEM



S9903 SCC IN A S9980 SYSTEM



MICROPROCESSOR

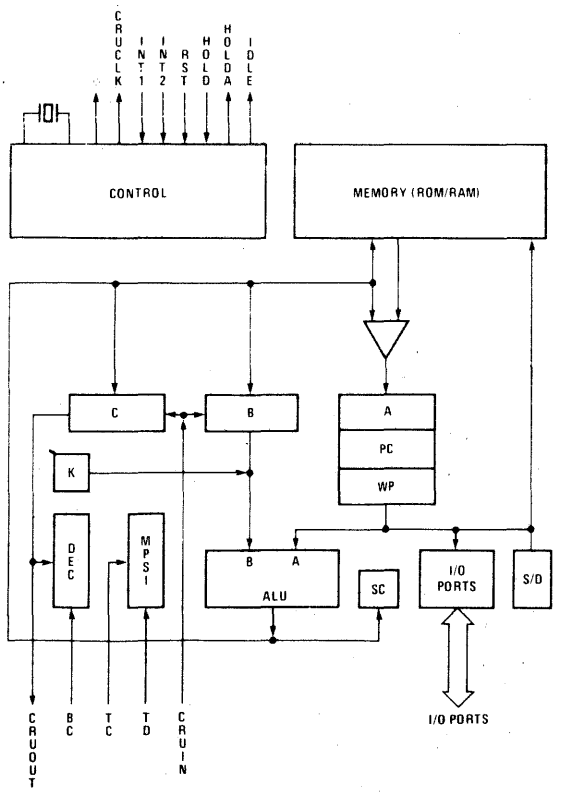
Features

- ☐ **16-Bit Instruction Word**
- ☐ **Minicomputer Instruction Set Including Multiply and Divide**
- ☐ **2048 Bytes of ROM on Chip**
- ☐ **128 Bytes of RAM on Chip**
- ☐ **16 General Purpose Registers**
- ☐ **4 Prioritized Interrupts**
- ☐ **On Chip Timer/Event Counter**
- ☐ **32 Bits General Purpose I/O**
- ☐ **256 Bits I/O Expansion**
- ☐ **Multiprocessor System Interface**
- ☐ **Single 5 Volt Power Supply**
- ☐ **Power Down Capability for Low Stand-by Power**
- ☐ **N-Channel Silicon Gate MOS**

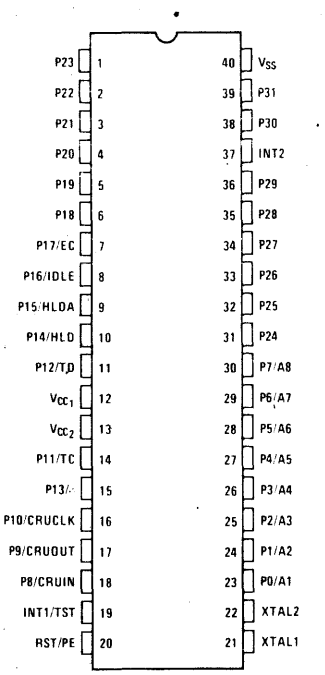
General Description

The S9940 is a single-chip, 16-bit microcomputer containing a CPU, memory (RAM and ROM), and extensive I/O. The instruction set of the S9940 is a subset of the S9900 instruction set and includes capabilities offered by minicomputers. The unique memory-to-memory architecture features multiple register files, resident in the RAM, which allow faster response to interrupts, and increased programming flexibility. The memory consists of 128 bytes of RAM and 2048 bytes of ROM. The S9940 implements four levels of interrupts, including an internal decrementer which can be programmed as a timer or an event counter. All members of the S9900 family of peripheral circuits are compatible with the S9940.

Block Diagram



Pin Configuration



ADVANCED PRODUCT DESCRIPTION

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16-BIT MICROPROCESSOR

Features

- ☐ 16-Bit Instruction Word
- ☐ Full Minicomputer Instruction Set Capability Including Multiply and Divide
- ☐ Up to 16,384 Bytes of Memory
- ☐ 8-Bit Memory Data Bus
- ☐ Advanced Memory-to-Memory Architecture
- ☐ Separate Memory, I/O, and Interrupt-Bus Structures
- ☐ 16 General Registers
- ☐ 4 Prioritized Interrupts
- ☐ Programmed and DMA I/O Capability
- ☐ On-Chip 4-Phase Clock Generator
- ☐ 40-Pin Package
- ☐ N-Channel Silicon-Gate Technology

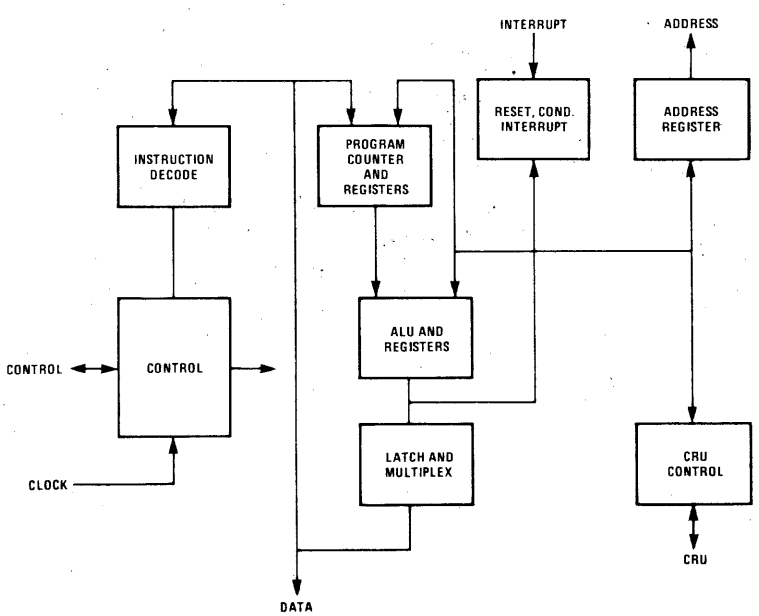
The S9980A and the S9981 although very similar, have several differences which are:

1. The S9980A requires a V_{BB} supply (pin 21) while the S9981 has an internal charge pump to generate V_{BB} from V_{CC} and V_{DD}.
2. The S9981 has an optional on-chip crystal oscillator in addition to the external clock mode of the S9980A.
3. The pin-outs are not compatible for D0-D7, INT0-INT2, and $\overline{\phi 3}$.

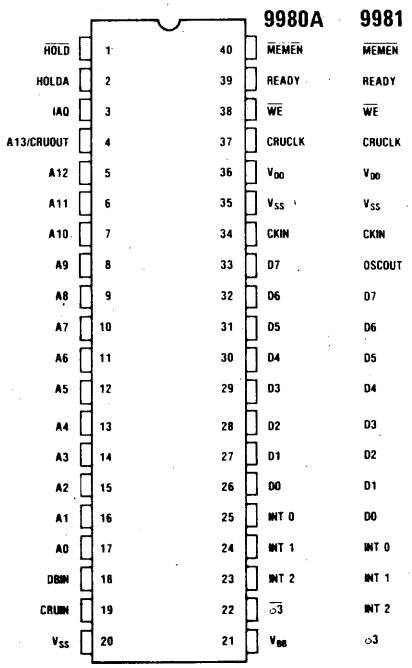
Description

The S9980A/S9981 is a software-compatible member of AMI's 9900 family of microprocessors. Designed to minimize the system cost for smaller systems, the S9980A/S9981 is a single-chip 16-bit central processing unit (CPU) which has an 8-bit data bus, on-chip clock, and is packaged in a 40-pin package (see Figure 1). The instruction set of the S9980A/S9981 includes the capabilities offered by full minicomputers and is exactly the same as the 9900's. The unique memory-to-memory architecture features multiple register files, resident in memory, which allow faster response to interrupts and increased programming flexibility. The separate bus structure simplifies the system design effort.

Block Diagram



Pin Configuration



ADVANCED PRODUCT DESCRIPTION

©IC MASTER 1979

S9980A/S9981 Electrical and Mechanical Specifications

Absolute Maximum Ratings Over Operating Free-Air Temperature Range (unless otherwise noted)*

Supply voltage, V_{CC} (see Note 1) ..... – 0.3V to 15V
Supply voltage, V_{DD} (see Note 1) ..... – 0.3V to 15V
Supply voltage, V_{BB} (see Note 1) (9980A only) ..... – 5.25V to 0V
All input voltages (see Note 1) ..... – 0.3V to 15V
Output voltage (see Note 1) ..... – 2V to 7V
Continuous power dissipation ..... + 1.4W
Operating free-air temperature range ..... 0°C to 70°C
Storage temperature range ..... – 55°C to 150°C

*Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions" section of this specification is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: Under absolute maximum ratings voltage values are with respect to V_{SS}.

Recommended Operating Conditions

Symbol	Parameter	Min.	Nom.	Max.	Unit	Conditions
V_{BB}	Supply voltage (9980A only)	– 5.25	– 5	– 4.75	V	
V_{CC}	Supply voltage	4.75	5	5.25	V	
V_{DD}	Supply voltage	11.4	12	12.6	V	
V_{SS}	Supply voltage		0		V	
V_{IH}	High-level input voltage	2.2	2.4	V_{CC} + 1	V	
V_{IL}	Low-level input voltage	– 1	0.4	0.8	V	
T_A	Operating free-air temperature	0	20	70	°C	

Electrical Characteristics Over full Range of Recommended Operating Conditions (unless otherwise noted)

Symbol	Parameter		Min.	Typ.*	Max.	Unit	Conditions
	Input current	Data bus during DBIN			± 75		$V_I = V_{SS}$ to V_{CC}
		$\overline{WE}$, $\overline{MEMEN}$, $\overline{DBIN}$ during HOLDA			± 75	μA	$V_I = V_{SS}$ to V_{CC}
		Any other inputs			± 10		
V_{OH}	High-level output voltage		2.4			V	
V_{OL}	Low-level output voltage				0.5 0.65	V	I_O = mA I_O = 3.2mA
I_{BB}	Supply current from V_{BB} (9980A only)				1	mA	
I_{CC}	Supply current from V_{CC}			50 40	60 50	mA	0°C 70°C
I_{DD}	Supply current from V_{DD}			70 65	80 75	mA	0°C 70°C
C_I	Input capacitance (any inputs except data bus)			15		pF	f = 1MHz, unmeasured pins at V_{SS}
C_{DB}	Data bus capacitance			25		pF	f = 1MHz, unmeasured pins at V_{SS}
C_O	Output capacitance (any output except data bus)			15		pF	f = 1MHz, unmeasured pins at V_{SS}

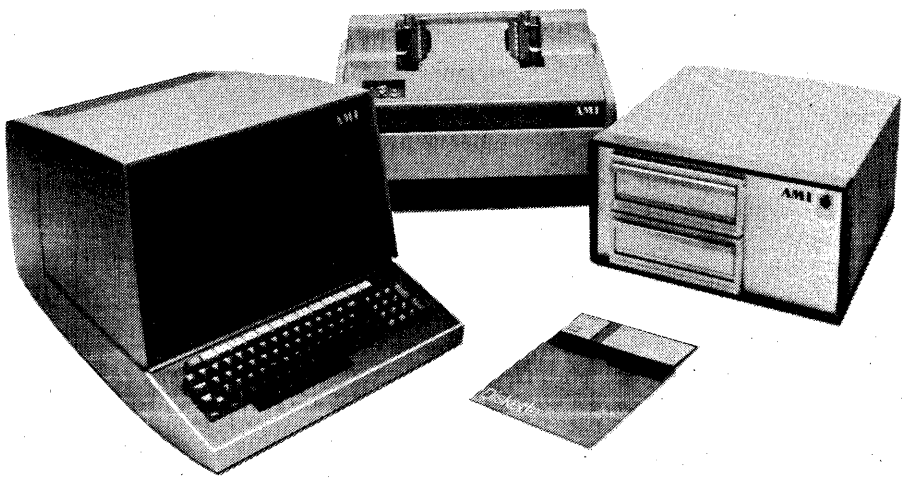
*All typical values are at T_A = 25°C and nominal voltages.

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AMI Microcomputer Development Center

An intelligent stand-alone software debugging station, serving completely the combined needs of the design engineer and the programmer. It consists of a S6800 based CRT/keyboard microcomputer terminal, a dual drive floppy disk memory, and an optional hard copy printer.

A program in development (or in operation) can be viewed on the CRT and edited on the keyboard. Program files can be assembled and stored in the floppy disk memory, under control of the disk memory operating system software. The modular bus oriented card cage in the CRT terminal provides versatile facilities for developing and testing 6800 hardware.



CRT/Keyboard Terminal

- ☐ **Capability for generating 256 unique ASCII input characters**
- ☐ **12-inch diagonal CRT display — 25 lines of 80 characters**
- ☐ **16K bytes of user available RAM, expandable to 48K**
- ☐ **Full cursor and editing controls**
- ☐ **Special function controls**
- ☐ **Peripheral interconnects**

Logic Analyzer

- ☐ **General-purpose logic analyzer**
- ☐ **Plugs into MDC-100**
- ☐ **Trace memory hold 1024 steps**
- ☐ **All patterns 40 channels wide**
- ☐ **Two separate event qualifiers**
- ☐ **Data-dependent clock**
- ☐ **Outbound trigger**

Floppy Disk Memory

- ☐ **IBM 3740 data format compatible**
- ☐ **Data storage capacity of 256,256 bytes per diskette**
- ☐ **Fully supported by FDOS-II Disk Operating and File Management System software**

Optional Matrix Printer

- ☐ **132 column**
- ☐ **Dot matrix, impact printing**
- ☐ **120 or 180 characters per second**

S2000 Support

S2000 Designers can use the DEV-2000 Development Board to provide a direct link between the MDC and the user's prototype. As stand-alone systems, the S2000 designer can use the capabilities of either the low-cost SES-2000 hardware emulator — which is a pin-for-pin substitute for an S2000 microcomputer chip and contains its own EPROM memory — or the TES-S2000 functional go/no-go tester.

MDC Hardware Capabilities

The AMI MDC is a multifunction development center that single-handedly satisfies your requirements for software development, hardware development, and prototype checkout. The MDC can also double as a stand-alone communications terminal, a general purpose data processing system, or as an incoming parts tester.

Software Development — write, debug and operate S6800 and S2000 programs on the CRT terminal, using its internal RAM and the dual drive floppy disk for storage. The MDC comes with a full complement of support software, including the FDOS-II Disk Operating and File Management System, a Text Editor, an Assembler, Debugger, Trace, Telecommunications and Utilities.

Hardware Development — breadboard such cicruitry as interfaces or memories right on the MDC wirewrap prototyping board and plug into the CRT terminal card cage to operate with the MDC's S6800-based central processor in solving development problems. Use the control panel type functions of the CRT terminal for single step, stop-on-address, display, alter, and other similar program operations. The bus oriented card cage, position interchangeable plug-in card modules, and an extender card provide the flexibility to make hardware development easy. There is also a complete keyboard control led PROM programmer within the CRT terminal.

Prototype Checkout — with the advantages of a real-time test environment, rapid test program retrieval, single or multiple step execution, and hardware as well as software breakpoints, the checkout of prototype S2000 and S6800 circuitry is easy and efficient.

Stand-alone Communications Terminal — the CRT terminal has both RS-232 and current loop interfaces, supported by telecommunications firmware, for operation as a general purpose stand-alone intelligent terminal.

MDC Software Capabilities

The AMI MDC offers total facilities for rapidly developing applications and systems software. The entire MDC software system is at the user's instant disposal — a few simple keystrokes are needed to instantly access and execute any program. The FDOS-II disk based operating system provides complete system resource control to the programmer.

FDOS-II Disk Operating and File Management System — contains a resident module for bootstrapping the floppy disk memory and for disk I/O handling. It also contains an executive that performs all of the disk memory command line interpretations, file management and operational functions of the dual disk system. In addition, there are utility I/O and EPROM programming routines in FDOS-II.

The Text Editor — program provides the means for rapidly creating, examining and modifying stored files. The total capability of MDC's Text Editor exceeds that of many large minicomputer systems, and includes such features as storing searches and string substitutions.

The Symbolic Assembler — translates assembler language statements into executable machine language code. In conjunction with FDOS-II Operating and File Management Systems, assembling has been reduced to a series of simple operator keystrokes. Results of the assembly, automatically stored on disk, are immediately available for reference or execution.

MDC's Extensive Debug Program — effectively automates the functions of a computer control panel. Given control by simply pressing the DEBUG key or via program traps, Debug immediately responds with the display of machine and program status. Addition functions include:

- Register/data display and modification
- Instruction/subroutine step
- User definable debug macros
- Snapshot debug data of a running program
- Breakpoints (stop-on-address compare)
- Comment and header line displays

MDC's Trace Package — gives Debug the ability to display a trace of machine register contents, instruction mnemonics and operands before execution of any instruction or subroutine in the user's program. Microprocessor debugging has never been made easier.

MDC's Test Programs — are a set of self-test and diagnostics which verify that the hardware associated with the MDC is operating correctly. The programs are also helpful in isolating malfunctioning components. The program for testing the basic hardware is resident in EPROM and is activated by the keyboard TEST key.

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Microcomputer Development Center

Features

- ☐ Intelligent Terminal Based
- ☐ Compact System
- ☐ Interactive Software
- ☐ S6800/S2000 Family
- ☐ Self-Test Firmware
- ☐ Integral PROM Programming

The AMI MDC is a complete Microcomputer Development Center which couples the ease of use of the intelligent terminal with the modularity required in today's environment. The system provides immediate access to a sophisticated resident Micromonitor, an extensive debug program, as well as communications and self-test programs.

MDC 100

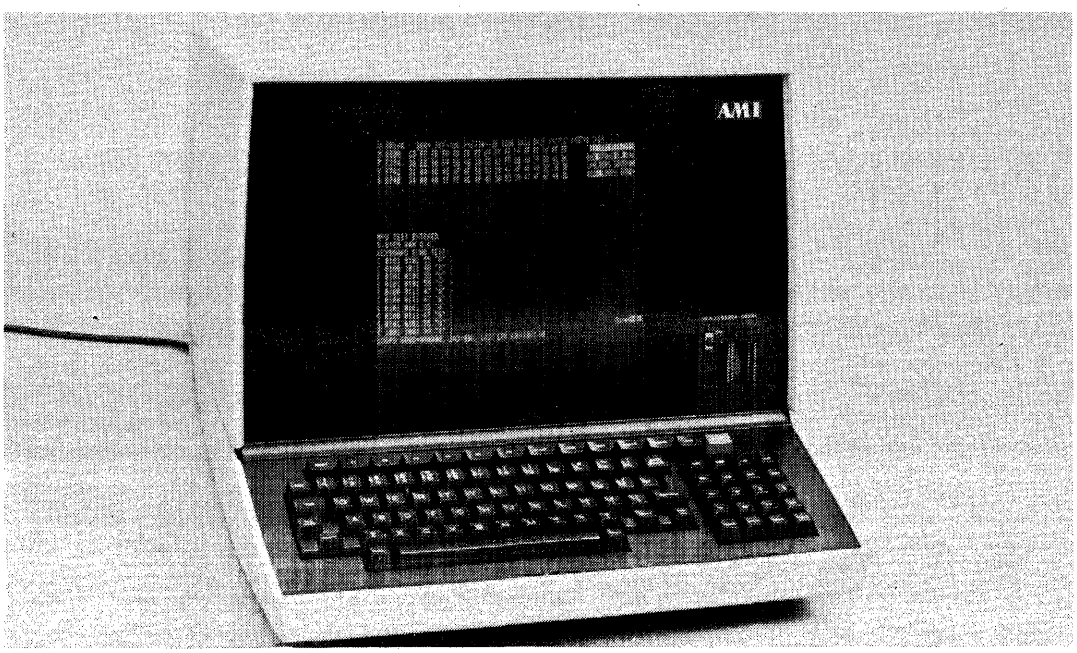
This configuration of AMI's Microcomputer system incorporates the intelligent terminal and dual floppy disk drives to form a full development center for software and hardware development and prototype check-out. The powerful support software includes the FDOSII Disk Operating and File Management System, a Text Editor, an Assembler, Debugger, Trace, Telecommunications and Utilities. Through the Operating System, the MDC 100 can be quickly configured to assemble and/or compile and debug programs for AMI's S6800 or S2000 Families of microprocessors. An integral EPROM Programmer allows the MDC System to be used to quickly and efficiently transfer programs from the expandible RAM Storage (16K supplied) to permanent storage.

MDC 102

The MDC 102 couples the MDC 100 with a highly efficient Dot Matrix printer to provide the hard copy necessary for off-line program evaluation. The printer is the MDC 202, one of three printer options offered in the MDC Series. The MDC 202 features 120cps print speed with 132 character print columns using a 7 x 7 Dot Matrix.

MDC 104

The MDC 104 is an AMI Microcomputer Development Center configuration which adds the powerful prototyping tool of the Logic Analyzer to the development capabilities of the MDC 100. The Analyzer is indispensable when isolating critical timing errors and hardware/software sequence discrepancies during the final integration phases of prototype development.



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The MDC Logic Analyzer is a hardware/software system for capturing and displaying up to 40 parallel signals from an external digital system which is being tested or debugged. The MDC Logic Analyzer is especially general in its display formatting which can be user-defined. With 40 signal inputs plus a clock, it can be used with most microprocessor and peripheral ICs without requiring personality modules.

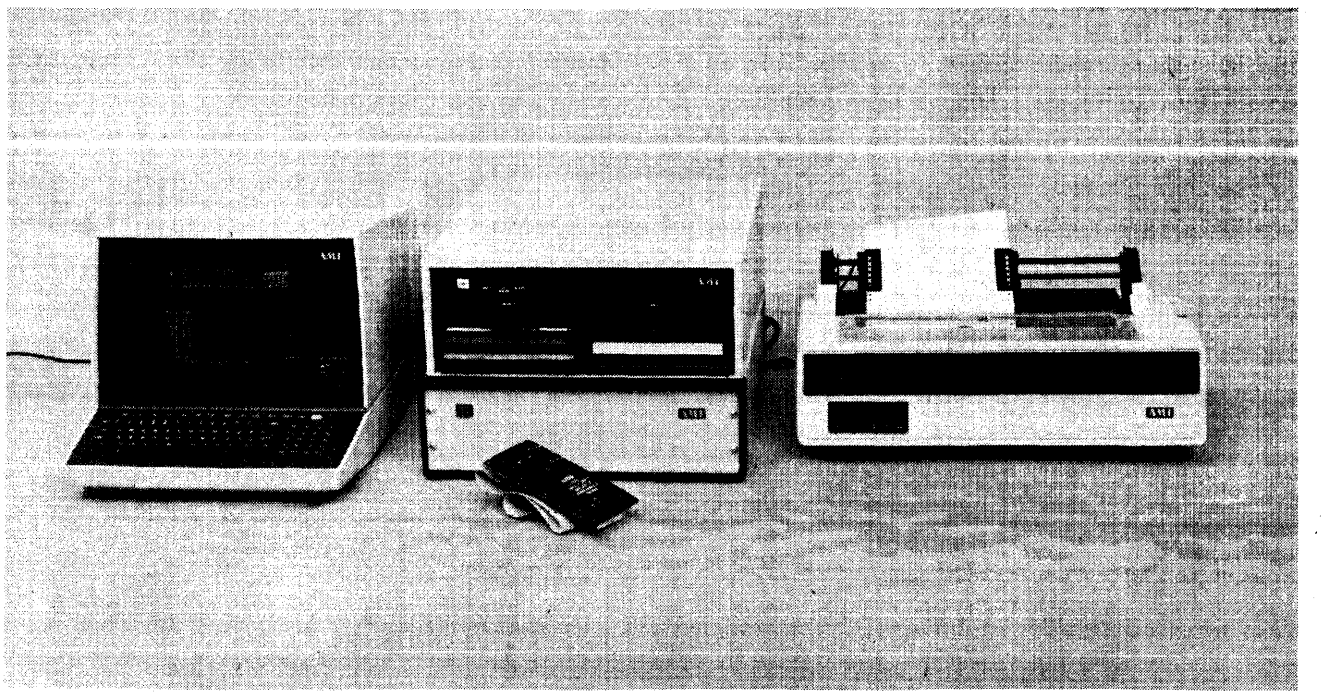
The hardware of the Logic Analyzer allows capturing up to 1024 events of 40 parallel inputs, programmable data-dependent start and clock signals, and a trigger for an external oscilloscope or counter. The two starting qualifiers, the dependent clock, and the trigger may each consist of the 40 input signals in any combination of 1, 0, or "don't care" states.

The end of the capturing process may be delayed up to 65K clock pulses from the start. User inputs may be from -15 to +15 volts with adjustable thresholds at frequencies up to 10MHz for TTL signals.

The software package provided links the capabilities of the MDC 100 and the Logic Analyzer. It provides completely user-defined formatting and display of captured data and data-dependent qualifiers with user-defined fields displayed in binary, hexadecimal, octal, ASCII, or user-defined signal names. A special disassembly mode is available for 6800/6802 instruction mnemonics and operands.

Formats may be saved on and read from floppy disk files and modified dynamically. A set of pre-defined formats are provided for use with the pinouts of the S6800 microprocessor family and S2000 microcomputer.

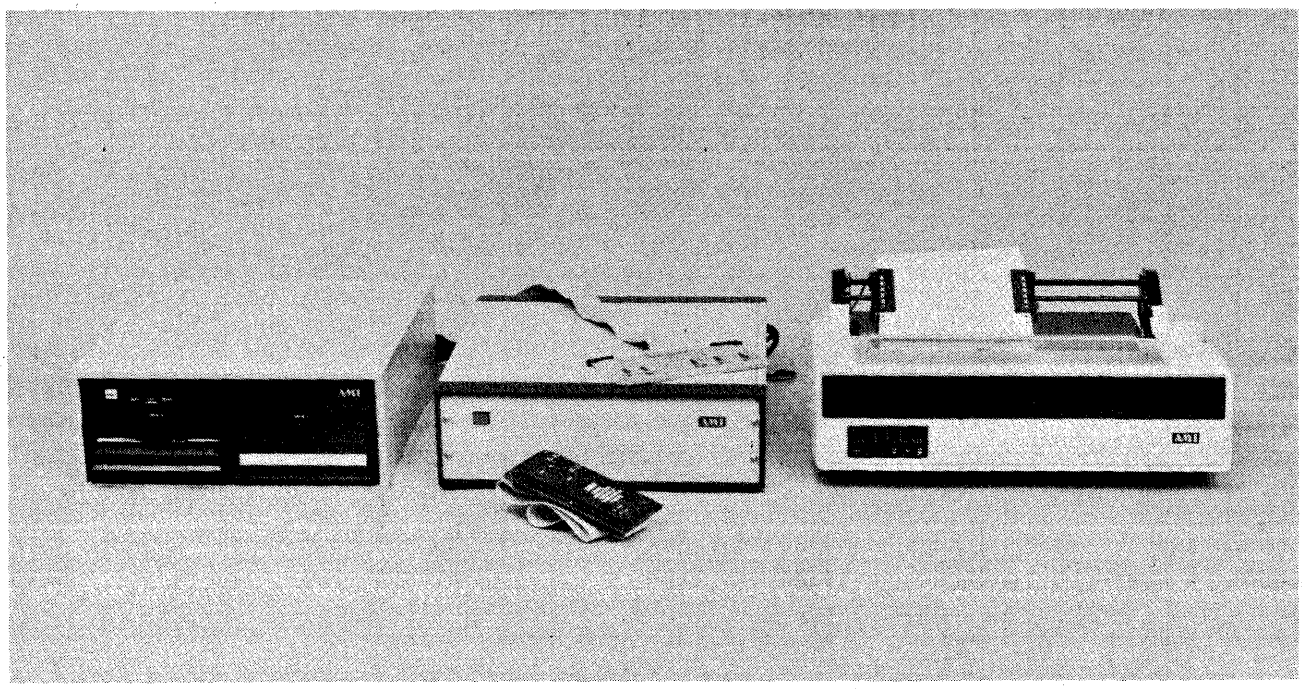
The Logic Analyzer consists of trace RAM, control logic, power supply, an interface card for the MDC, a comparator/probe control card, user clock and trigger leads, 40 channels of probes (separately or in one clip) and interconnecting cables. The unit is available as an optional item to be added to existing systems as the MDC 140.



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MDC 106

As an all inclusive Development Center the MDC 106 offers total design support. The powerful MDC 100 system with a Dot Matrix printer and the Logic Analyzer provide a complete development package for integrating software and hardware. The MDC 106 offers the tools necessary to move rapidly through software development and debug to full hardware analysis and debug for rapid development of microcomputer-based products.



SES SERIES

STATIC EMULATOR MODULES

Features

- ☐ Full Microcomputer Emulation
- ☐ Erasable Program Memory
- ☐ Fully-Tested Operational System
- ☐ System Socket Compatible

The SES Series of boards provide pin-for-pin emulation of single-chip microcomputers. The board offers the full operational capabilities of the single-chip microcomputer coupled with the flexibility of board level design. The Series incorporates on-board Erasable PROM to provide ease of program modification in prototype environment.

SES 2000/2000A

The SES 2000 is an emulator board for the popular S2000 single-chip microcomputer. This board level unit is configured to plug directly into the system socket that would normally hold the mask programmed S2000. Through the use of the SES 2000, system hardware and program configurations can be quickly and efficiently accomplished in the prototype stages. The board is also suited for integration into preproduction systems allowing full freedom of modification through memory changes in standard EPROMs. For systems utilizing the S2000A, which is capable of driving high voltage vacuum fluorescent displays, the SES 2000A provides the system emulation of the S2000A. Program implementation and functional operation is the same as that found in the SES 2000.

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SES 2150/2150A

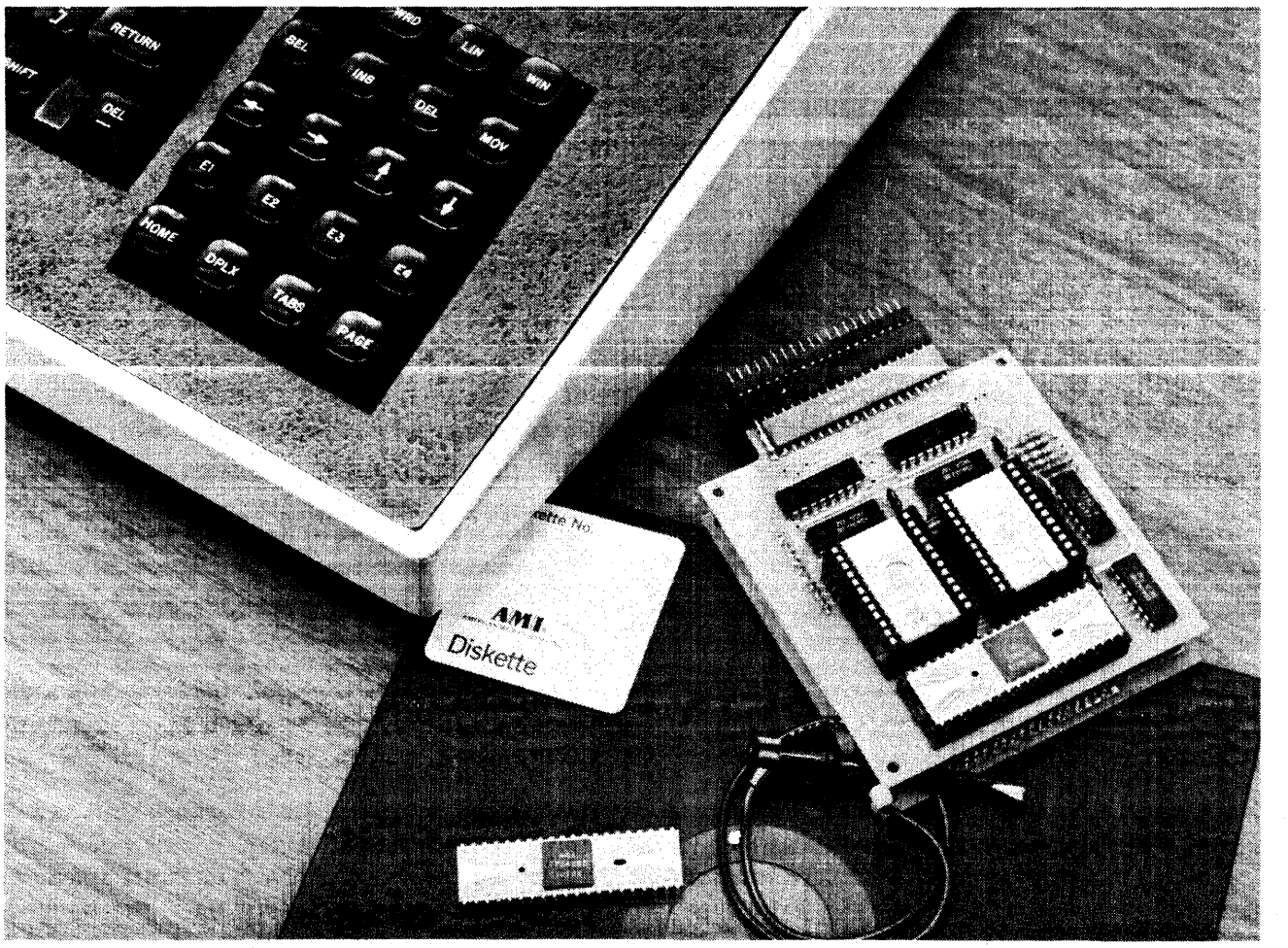
The SES 2150 provides full emulation for the S2150. This system unit incorporates an expanded EPROM on-board to match the 1.5K byte ROM memory capabilities of the single-chip microcomputer.

The SES 2150A broad level system allows the implementation and emulation of the high voltage version of the S2150 and the S2150A. All the features of the SES 2000 series are offered in this unit to assist in prototype and preproduction development.

SES 2400/2400A

An advanced emulator board capable of emulating the functions of the S2200 and the S2400 single-chip microcomputers. Full functional capabilities are provided including D/A and A/D input/output functions. On-board EPROM provides a full compliment of user-modifiable program memory.

The SES 2400A emulator board provides the high voltage interface necessary to emulate the S2200A and the S2400A single-chip microcomputers.



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MICROCOMPUTER BOARDS/KITS

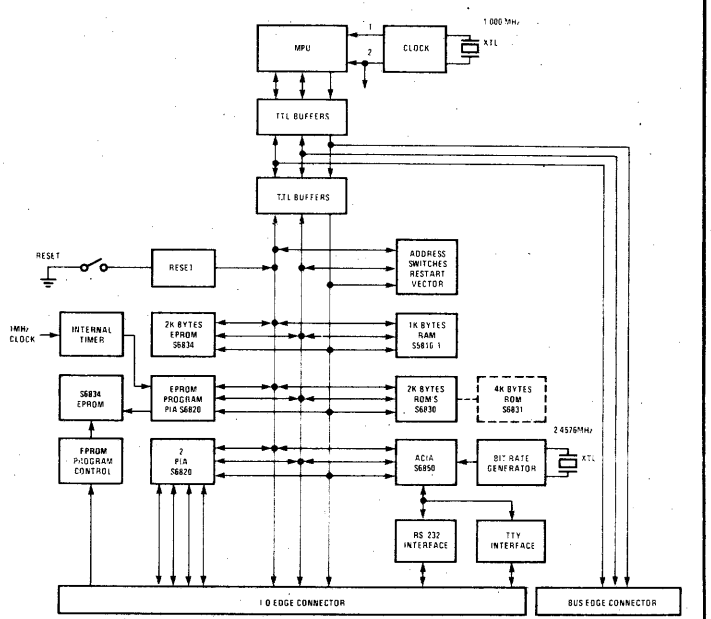
Features

- ☐ **Expandable to 4K Bytes ROM**
- ☐ **Expandable to 2K Bytes EPROM**
- ☐ **Expandble to 1K Bytes RAM**
- ☐ **EPROM Programming for S6834**
- ☐ **Expandable to 3 PIA's = 58 I/O Lines**
- ☐ **TTY Current Loop or RS232 Interface**
- ☐ **ROM Subroutine Program Library**
- ☐ **Selectable DMA Mode**

General Description

The EVK Series Board is a single PCB, hardware/software system that can be used as a general purpose microcomputer. It allows system development using a functionally compatible system and reduced development time. With this system the basic 6800 family of parts can also be evaluated. The 10-1/2"x12" card has two edge connectors, one for the MPU Bus and one for the I/O. The EVK 300 is a fully assembled and tested board, while the EVK 200, EVK 100 and EVK 99 are in kit form. All kits are fully expandable to EVK 300 capabilities.

Series Block Diagram



EVK Capabilities

	ROM	RAM	EPROM	PIA	TTY CURR LOOP	ROM SUB-ROUTINE PROG. LIBRARY	TOTALLY BUFFERED MPU LINES	SGL +5V P.S.	RESTART ADDRESS SELECTION	SELECT-ABLE DMA MODE	INTERVAL TIMER	TINY BASIC
EVK 99	2K bytes	512 bytes	–	1	✓		✓	✓	✓			
EVK 100	2K bytes	512 bytes	–	–	✓	✓	✓	✓	✓			
EVK 200	4K bytes	1K bytes	512 bytes	3	✓	✓	✓	✓	✓	✓	✓	
EVK 300	4K bytes	1K bytes	2K bytes	3	✓	✓	✓	✓	✓	✓	✓	*✓

*AMI 6800 Tiny BASIC

– A high level interpretive language derived from the standard Dartmouth BASIC. Furnished to EVK 300 users at no charge upon submittal of warranty registration.

ADVANCED PRODUCT DESCRIPTION

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System Specifications

All of the S6800 microprocessor lines are available at the bus edge connector and are buffered to allow 40mA of drive capacity for expanding the development system. The standard system clock is adjustable from 300kHz to 1MHz by using the potentiometers on the board. An optional 1MHz crystal may be selected to control the accuracy for those applications requiring critical timings.

An on-board interval timer gives 1ms and 100μs timing marks for general use and for EPROM programming. Three types of DMA operation are possible using the EVK Board: Halt Processor, Cycle Steal or Multiplexing.

Memory

Memory and I/O addresses are assigned to the upper 8K bytes of the available memory space. (See memory map for address assignments.) This gives the system developer the flexibility to use the remaining 56K bytes as he wishes. All of the memory and I/O on the board may be disabled externally by an edge connector line called MEMORY DISABLE, leaving the MPU free to operate totally in an external memory.

The S6830 ROMs contain the Prototype Operating Library (PROTO) and a ROM Subroutine Library $(RS)^3$. An optional Assembler/Disassembler (M/AD) S6831 ROM is available to operate with PROTO. The 2K of EPROM locations may also be used for program verification.

The RAM is assigned to the upper 1K of available memory space. The PROTO and $(RS)^3$ programs require about 256 bytes of this RAM so the rest is available for general programming. With all restart vectors automatically assigned to the upper memory addresses, restart vectoring is forced from a set of 16 switches. This allows the restart address to be vectored to any memory location.

The RAM has further been divided into two 512 byte sections such that the upper 512 bytes remain fixed in the assigned address block and the lower 512 bytes are moveable through a switch selection option. 512 bytes of RAM are relocatable to the lowest address space to take advantage of the S6800's direct addressing mode. This is only recommended if no external memory is added. When adding external memory, it is advisable to use the RAM in the upper address space and the external memory as the low addresses.

I/O

An S6850 ACIA is used to provide a 20mA current loop interface to a TTY or RS232 terminal. A 20mA current loop interface and an EIA RS232 interface are both available on the board. A bit rate generator allows operation using any of the standard communication frequencies (see table) so a large variety of terminal types can be used.

Three S6820 PIAs allow up to 58 I/O lines, giving flexibility in I/O through the parallel interfaces.

EPROM Programming

Unique to the AMI EVK Board is the ability to program S6834 EPROMs (512 x 8) on the board. The programming software can program an EPROM from any memory location, RAM, ROM or EPROM. It can verify a word and, if desired, change a single bit in the EPROM, provided that the change is from LOW to HIGH.

Software

The EVK Board Software is comprised of a TTY Operating Program (PROTO) and is supported by a ROM Subroutine Library $(RS)^3$.

Specifications

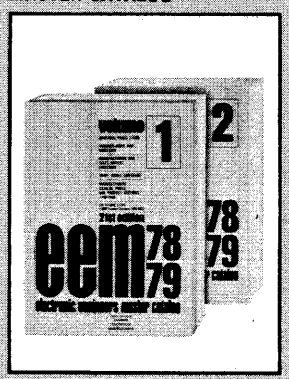
Power	+5VDC @ 3.5A
with EPROMs	−12VDC @ 150mA
System Clock	1MHz ±.1%
Word Size	
Instruction	8, 16 or 24 bits
Data	8 bits
Memory Addressing	
RAM	Low 0000-7DFF High FC00-FDFF Fixed FE00-FFFF
EPROMs	E000-E3FF, E400-E7FF
ROM	E800-F7FF
I/O	F800-FBFF
Bus Structure	
16 Address	
8 Data	
6 Control	
Parallel I/O	up to 58 lines
Interrupts	Vectored via software
Timer	
Input	1MHz or async adjustable
Mode	Continuous
Physical Characteristics	
Width	10.5 in.
Height	12.0 in.
Connectors	
Bus − I/O	86-pin − Stanford Applied Engineering SAC-43D/1-2 or equivalent, 2 sets.

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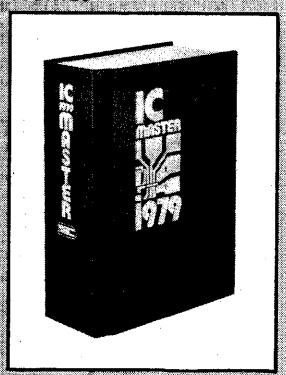
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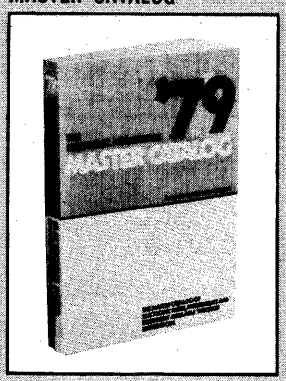
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F8/3870 • F6800 • 9440
MICROFLAME BIT SLICE

FAIRCHILD MICROCOMPUTERS

Fairchild microcomputers cover the spectrum from 8-bit MOS microprocessors to bit-slices and 16-bit bipolar machines.

- 1-Chip F3870 MicroMachine-2™/the multichip F8 family with software and compatibility.
- 2-Chip F6802/6846 combination plus a powerful bus oriented F6800 family well supported by a large variety of peripheral devices.
- Three high-performance bipolar bit-slice families:
  Macrologic
  2900
  8-bit ECL (90LSI)
- 16-bit bipolar 9440 Microflame™ microprocessor that brings minicomputer capabilities to the microprocessor world.

These products are supported by training courses for the design engineer who must learn to design the microprocessor into a working system and for those designers who need to complement their hardware capabilities with software (instruction set) or those software types who must gain an intimate knowledge of the hardware. All courses emphasize lots of hand-on time backed by examples to enhance students' working familiarity with each microprocessor.

Courses are offered at Mountain View, California or on site courses may be arranged with a local Farchild sales office or distributor.

HOW TO ENROLL — Call or write the Training Center at (415) 962-3710, M/S 20-1028.

FAIRCHILD F3870 — The 8-bit single chip F3870 Microcomputer is ideal for high volume, low cost applications, featuring a single +5V power supply, 2048 bytes of ROM, 64 bytes of scratchpad RAM, 32-bits of I/O, and a programmable timer and interrupt.

FAIRCHILD F6800 — The 8-bit MOS F6800 family offers a complete and continuously expanding range of microprocessor devices with a powerful instruction set. On the low end there is the F6802/6846 2-chip combination that features a processor chip combination with 128 bytes of on board RAM of which 32 bytes have a power down feature.

The F6800 family is supported by a large array of pheripheral devices which include: ROM, RAM, EPROM, Synchronous and Asynchronous Controller for date communications, Timers, Direct Memory Access (DMA), CRT Controller, the 68488 for the IEEE Standard Bus Controller.

FAIRCHILD BIT-SLICES — In 1975, Fairchild announced the Macrologic bipolar bit-slice microprocessor family. To broaden our product lines and strengthen our leadership position in 1978 Fairchild added the 2900 family. In addition and to satisfy the ultimate requirement in performance, we are introducing an 8-bit ECL F100K compatible microprocessor family (90LSI). The Fairchild bit-slice course will cover basic microprogramming concepts and techniques, survey the three most powerful bipolar bit-slice families — Macrologic, 2900, and 90LSI — and offer the student some hands-on experience.

FAIRCHILD 9440 MICROFLAME — The 9440 MICROFLAME is a 16-bit bipolar microprocessor that executes a minicomputer multifunction instruction set with minicomputing performance — e.g., fast throughput, flexible addressing, direct memory access and sophisticated priority interrupt handling. The development of the MICROFLAME microprocessor was undertaken several years ago after the establishment of the high-performance I^3L (Isoplanar Integrated Injection Logic) technology. For the first time, the potential for real bipolar performances (less than 10ns propagation delays) in LSI configurations became a reality. Also, it was soon apparent that a 10 MHz clock-rate microprocessor could be developed using I^3L technology in combination with proven logic and circuit design. Thus, the decision was made to develop a microprocessor that would bring minicomputer capabilities to the microprocessor world.

FAIRCHILD

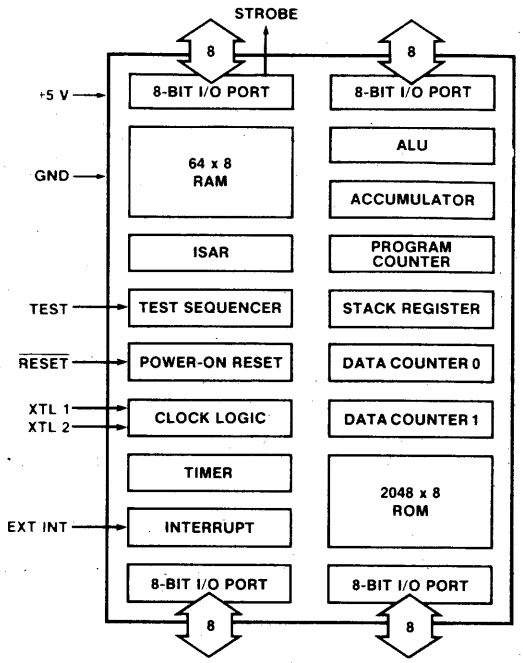
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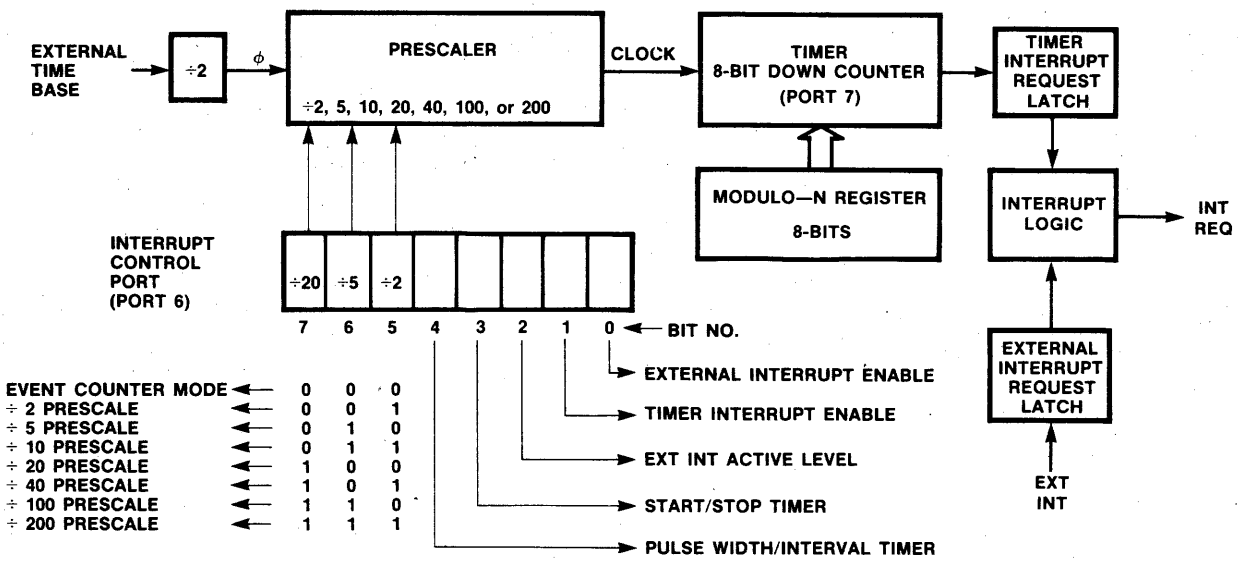
F3870 FAMILY

F3870 — These devices are complete 8-bit microcomputers on single MOS integrated circuits. The family can execute the F8 instruction set of more than 70 commands, allowing expansion into multi-chip configurations with software compatibility. The devices feature read only memory, 64 bytes of scratchpad RAM, a programmable binary timer, 32 bits of I/O, and a single +5 V power supply requirement.

Members of the family differ in memory type and size. The F3870 has 2048 bytes of mask programmed ROM while the F38E70 has 2048 bytes of PROM. The 3872 has 4032 bytes of masked ROM plus 64 bytes of RAM. The additional RAM is addressed from the program and data counters, not the ISAR. The F3874 contains 4096 bytes of masked programmed ROM.

Utilizing ion-implanted, n-channel silicon-gate technology and advanced circuit design techniques, Fairchild's single-chip microcomputers offer maximum cost effectiveness in a wide range of control and logic replacement applications.





TIMER AND INTERRUPT CONTROL FOR F3870

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F38E70

SINGLE-CHIP COMPUTER

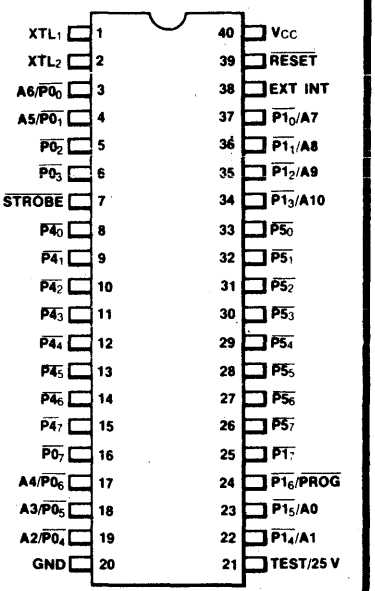
FAIRCHILD MICROCOMPUTER FAMILY

GENERAL DESCRIPTION–The Fairchild single-chip microcomputer series offers a variety of circuits for the high-volume, cost-sensitive markets. The F38E70 is a complete 8-bit microcomputer on a single MOS integrated circuit. The F38E70 is functionally identical to the F3870 except the F38E70 has 2K bytes of EPROM in place of 2K bytes of ROM. The F38E70 can execute the F8 instruction set of more than 70 commands. The device features 2048 bytes of EPROM, 64 bytes of scratch-pad RAM, a programmable binary timer, 32 bits of I/O, and a single +5 V power supply requirement.

Utilizing Fairchild's double-ion-implant, n-channel technology and advanced circuit design techniques, the single-chip F38E70 offers maximum cost effectiveness in many low-to-medium volume systems. When production volume requires large quantities, the transition to the mask programmed F3870 is very straightforward with no circuit design changes.

- **SINGLE-CHIP MICROCOMPUTER**
- **SOFTWARE COMPATIBLE WITH F8 FAMILY**
- **2048-BYTE EPROM**
- **64-BYTE SCRATCHPAD RAM**
- **32-BITS (FOUR PORTS) TTL COMPATIBLE I/O**
- **PROGRAMMABLE BINARY TIMER**
  - **INTERVAL TIMER MODE**
  - **PULSE WIDTH MEASUREMENT MODE**
  - **EVENT COUNTER MODE**
- **EXTERNAL INTERRUPT**
- **CRYSTAL, LC, RC, EXTERNAL, OR INTERNAL TIME BASE**
- **LOW POWER (375 mW TYP)**
- **SINGLE +5 V ±10% POWER SUPPLY**
- **+25 V PROGRAMMING SUPPLY**
- **SIMPLE EPROM PROGRAMMING**

CONNECTION DIAGRAM
DIP (TOP VIEW)

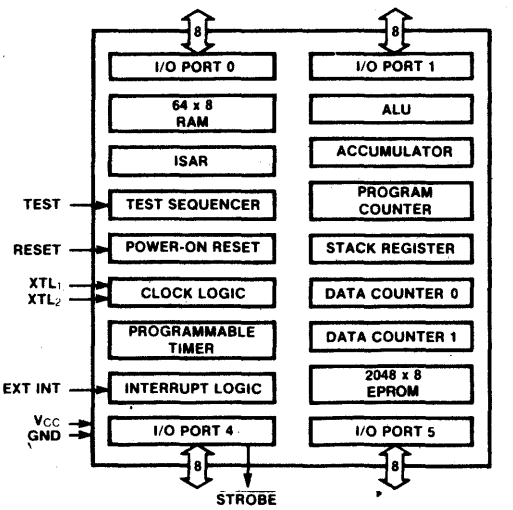


PIN NAMES

PIN NAME	DESCRIPTION	TYPE
$\overline{P0_0}$-$\overline{P0_7}$	I/O Port 0/address*	Bidirectional
$\overline{P1_0}$-$\overline{P1_7}$	I/O Port 1/address*	Bidirectional
$\overline{P4_0}$-$\overline{P4_7}$	I/O Port 4/Data Out*	Bidirectional
$\overline{P5_0}$-$\overline{P5_7}$	I/O Port 5/Data In	Bidirectional
$\overline{STROBE}$	Ready Strobe	Output
EXT INT	External Interrupt	Input
$\overline{RESET}$	External Reset	Input
TEST	Test Line/Prog Voltage	Input
XTL_1, XTL_2	Time Base	Input
V_{CC}, GND	Power Supply Lines	Input

*As shown in the connection diagram, some Port 0 and Port 1 pins are address inputs for programming the F38E70 EPROM section. Port 4 and 5 DATA OUT and DATA IN refer to the programming and test modes.

F38E70



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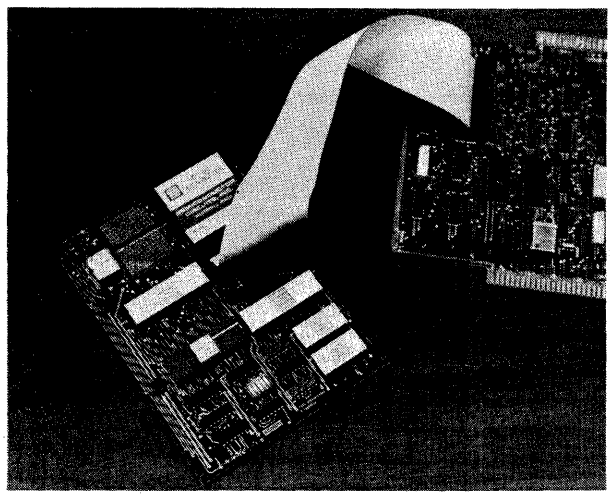
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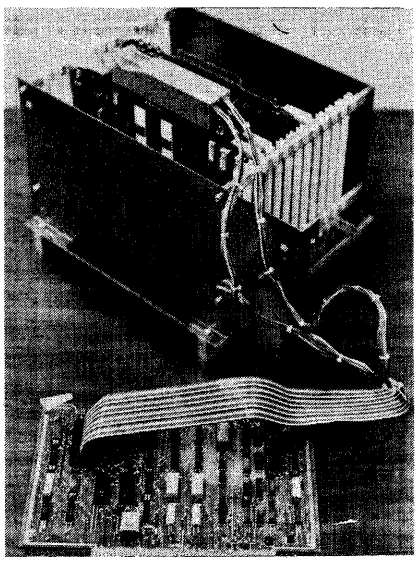
F3870 DEVELOPMENT SUPPORT — The Formulator family of develpment equipment supports the F3870, the one-chip micromachine manufactured by Fairchild. The Formulator Operating System, Utility Programs, and the Fairbug Monitor are totally compatible with the F3870, since it shares the same instruction set with the Formulator. A Simulation (Quad I/O) Module and an In-Circuit Emulation (ICE) cable are available to extend the Formulator features to the user's prototype or production breadboard. This creates a powerful design tool for creating the user's own F3870 software. In addition, the F3870 Emulator, a single stand-alone module for emulating the final F3870 software in PROMs, is available for building prototype systems.

F3870 SIMULATION — The non-microprocessor elements of the user's hardware configuration can be assembled on a breadboard and connected to Mark I, II, IIFD, III or IIIFD via the ICE cable plugged into a 40-pin socket on the user's board. The cable connector on the Processor Module in the Formulator provides I/O ports 0 and 1, while the Simulation (Quad I/O) Module provides I/O ports 4 and 5. This system provides real-world simulation of the user's components in their actual environment with the vital microprocessor signals, including the complete software debugging features of the Formulator, cabled to the external breadboard.

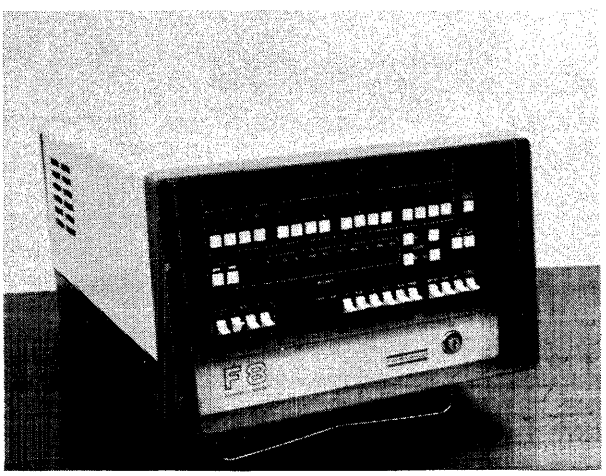
F3870 EMULATOR — After F3870 ROM codes are frozen, a smaller, easier-to-handle and less expensive tool is required. To accomplish this design-in task, Fairchild has developed the F3870 Emulator. The F3870 Emulator contains sockets for two 2708s or two 2716 EROMs in place of the F3870 on-chip ROM so ROM codes can be verified and easily changed. The F3870 Emulator plugs directly into the F3870 40-pin socket in the production prototype using a short Emulator cable. The printed circuit module is approximately 5" by 7".



Formulator Mark III System



Mark III System With F3870 Quad I/O Simulation Module Connected To User Demo Card

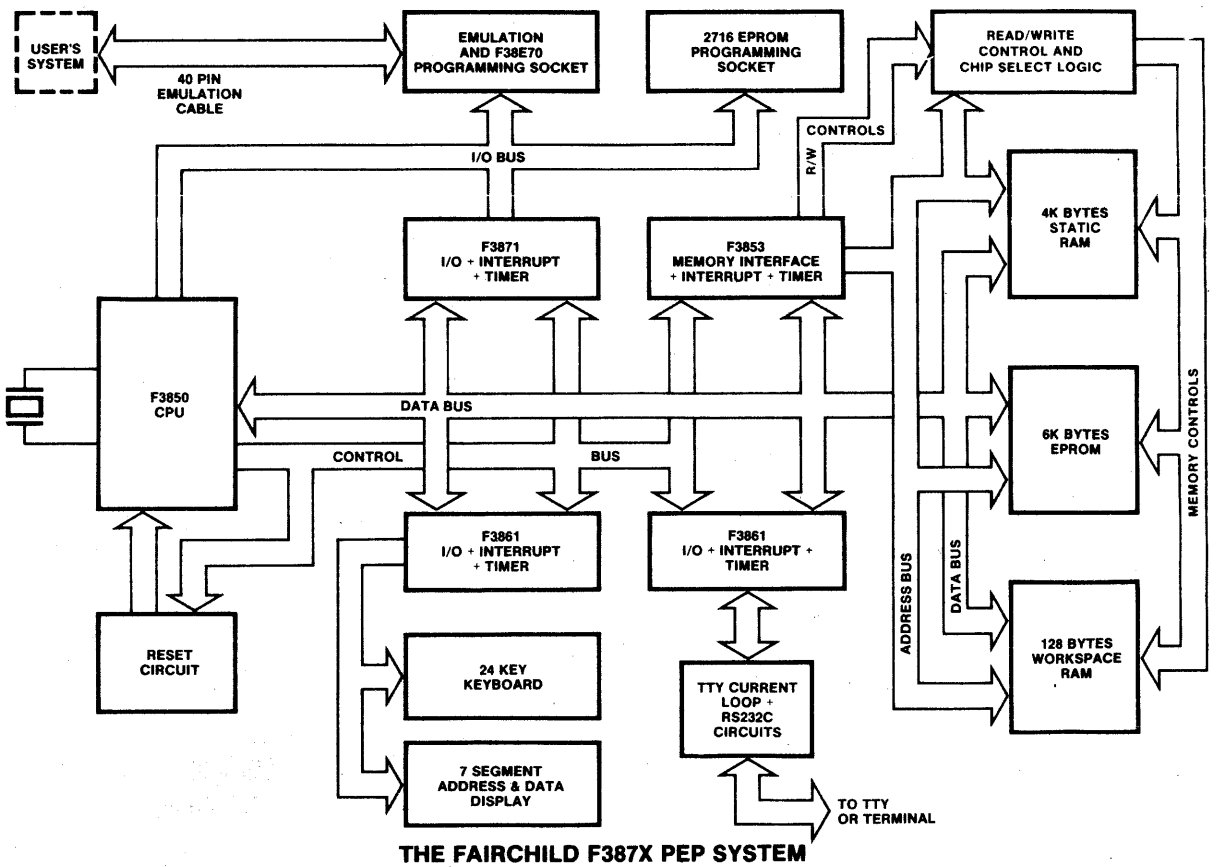


F3870 Emulation Module Connected To Sample System

PART NUMBER	DESCRIPTION	NUMBER I/O PORTS	ROM (BYTES)	SCRATCHPAD RAM (BYTES)	EX RAM (BYTES)	PKG
F3870 Series						
F3870	Single-Chip Computer	4	2K	64		D,P
F38E70	Single-Chip Computer with EPROM	4	2K EPROM	64		D,P
F3872	Single-Chip Computer	4	4K	128	64Δ	D,P
F3874	Single-Chip Computer	4	4K	64		D,P
F3876	Single-Chip Computer	4	2K	128	64Δ	D,P

The F387X PEP System Hardware Features

- Full In-Circuit Emulation of F3870, F3874 and F3876 Single Chip Microprocessors Using the Fairchild F8 System. (Emulation Cable Included.)
- Includes a 2K Firmware Monitor in an F8 PSU.
- Versatile On-Card Keyboard for Command and Data Entry.
- On-card 7-Segment Address and Data Display Using Large .8" Digits
- Programming Socket for the F38E70 Single Chip EPROM Microprocessor.
- Programming Socket for 2716 EPROMs.
- Crystal Controlled System Clocks.
- 2K Bytes of Executable Static RAM (2114s).
- Sockets for an Additional 2K Bytes of Static RAM (2114s).
- Sockets for 6K of Executable EPROM (2716 Type).
- Separate 128 Byte Static Memory for Monitor Workspace.
- Flexible Memory Map Strapping Options.
- Serial I/O Circuits for TTY 20 mA Current Loop or EIA RS232C.
- Four General Purpose Programmable Timers.
- Four General Purpose Interrupt Controls.
- Spare 8-Bit I/O Port for Support of a High Speed Paper Tape Reader.
- LED Indication of "Store Mode" Keyboard Operation.
- LED Indication of "Function Shift Mode" Keyboard Operation.



THE FAIRCHILD F387X PEP SYSTEM

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F3870 — The following is the text of an article that will be printed in *Progress*. It may have information that you would find valuable.

F3870 DESIGN INNOVATION — The F3870 is Fairchild's new single chip microcomputer. The F3870 has on a single chip all of the basic computer components including memory, central processing unit and input/output. F3870 includes:

2048 x 8 ROM
64 x 8 RAM
32 bits TTL compatible I/O including strobe
Programmable Binary Timer with three modes
Two-level prioritized vectored interrupts
Five clock modes
Single 5 V + 10% Power Supply
275 mW power consumption

The circuit is fabricated with Fairchild's advanced triple implant n-channel silicon technology.

Figure 1 shows the architectural organization of the F3870. Notice that all communication with the outside world is through I/O ports and the interrupt line since the data and address busses are not brought out in the 40 pin package.

There are several attributes that make the F3870 a unique and powerful single-chip computer. Figure 2 illustrates the I/O logic for one-bit.

The I/O ports are designed to be inherently bidirectional. In the standard I/O circuit shown, the input or output function is determined by the instruction executed. An output instruction will latch the data and either pull down the I/O pin to ground or let it be pulled up to +5V through the 6 resistor. The data input is the wired OR of the output state and the input on the I/O pin. Therefore, to perform an input function, a "0" is written to the output latch, allowing the I/O pin to be pulled up to V_{CC} through the 6 k resistor. The input to the I/O pin can then pull down the I/O line through the 6 k resistor to input a "1" to selected bits in I/O port latch, a masking operation is performed on the input data by pulling the output bit low preventing input on the selected bits. The I/O logic is very nice for bus oriented systems since I/O ports can also be tied to open collector TTL outputs as pull down devices. However, an I/O port should never be pulled up, since the rating of the output device will be exceeded and the chip will be destroyed.

Figure 3 illustrates how multiple F3870's can be connected along a common communication bus bia the bidirectional ports. In the system shown, the control and timing busses are used to communicate priority and bus control information between three processors. When one processor is selected as the control processor, the other F3870's write "0" to their ports on the communication bus. The processor in control can then output information on to the communication bus and the devices can read. Timing to initiate the transfer is via the timing bus and another I/O port. Transfer can also be initiated using the output strobe line and the interrupt logic.

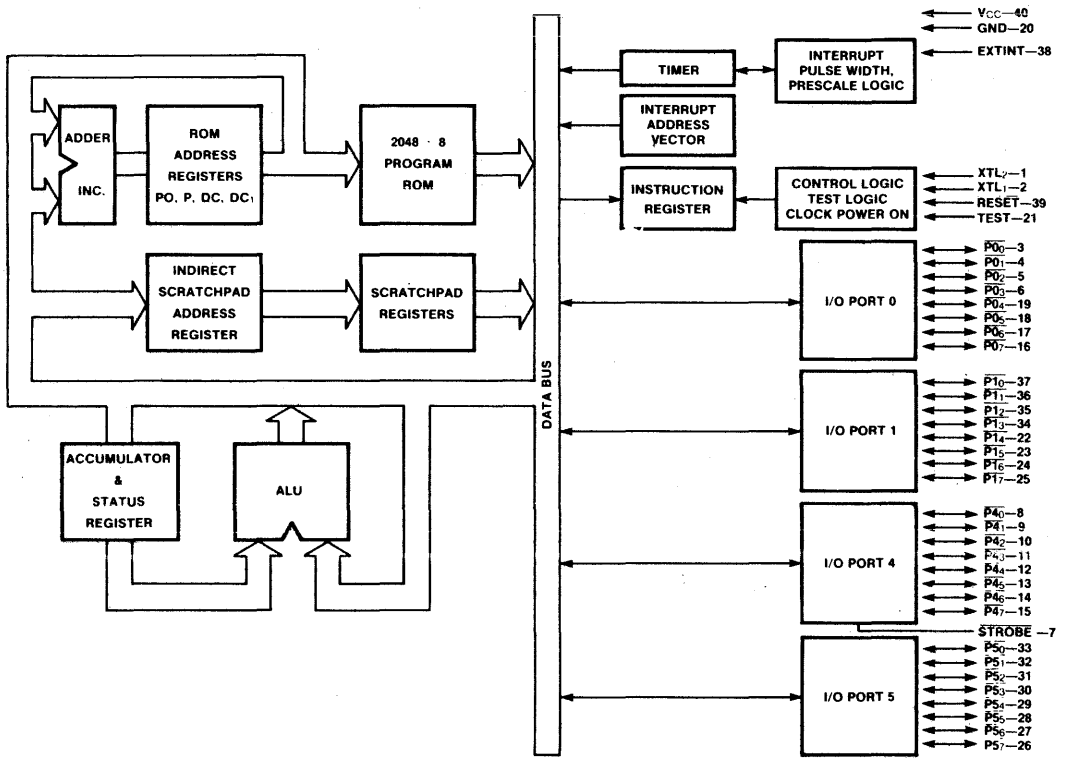
A UNIQUE ROM DESIGN — Probably the most important attribute of the F3870 is the low cost. The low selling price is direct relation to the manufacturing cost. In the production of LSI circuits manufacturing costs is a very strong function of chip size. The smaller the size of the chip, the more possible good chips on a wafer. The F3870 is the smallest full performance 8-bit single chip microcomputer in the world. The die size is 172 mills by 208 mills. To a large extent the small die size is due to the very efficient ROM design. The new ROM technique is shown in Figure 4. Figure 4 shows eight ROM bits. Information is programmed at the factory by a ION implant stage rather than a conventional gate oxide cut. To read a bit, the column select transistor is turned on and the row select logic turns on all the devices in a column except the one to be read. The logic attempts to turn off the one being read. If the transistor has been implanted it cannot be turned off and read as a one. The layout of the ROM is shown in Figure 5. Notice that adjacent bits share a common source and drain diffusion. Also notice that no contacts are required to the diffusions except for the top and bottom devices in a column. A single bit cell area is indicated by the shaded regions for F3870, the area is approximately 100 square microns. This compares with conventional ROMs cell area of approximately 196 square microns. The almost two to one savings in area is reason that the F3870 has twice as much ROM as most of its competitors.

THE REGULATED BACK BIAS GENERATOR — The diagram for a conventional MOS transistor is shown in Figure 6. A back bias voltage is often applied to the substrate to speed up the device and change its threshold. Back bias supplies are commonly found in high-speed RAMs. For single 5 V supply devices no back bias is used, and most single supply parts are therefore lower performance. To alleviate the problem of single power supply performance the F3870 uses a regulated on chip

back bias power supply. A simplified diagram of this supply drawn in Figure 7. A 1 MHz oscillator generates the two phases required by the power supply. A switch turns the oscillator on or off as needed to maintain the correct amount of back bias voltage for maximum circuit performance. The circuit operates by charging up the capacitors and transferring charge through the diodes.

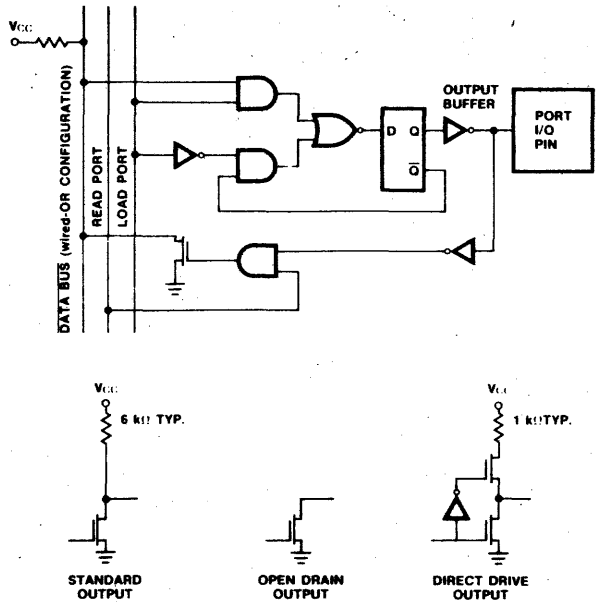
The regulator of the oscillator has other benefits besides improving the speed of the F3870, the regulator also makes the device able to work with a power supply spec of ±10%. Also, the regulator tends to track with temperature making extended temperature operation easier to achieve. And finally, the regulator follows process changes and aging in the circuit resulting in a chip that is lower cost to build and has enhanced long term reliability.

COST AND PERFORMANCE — The reasons that the F3870 is the dominant force in single chip microcomputers are cost and performance. The architecture and logic is designed for very high performance. The addressing modes available enable very compact programs with high-speed execution. The strobe, I/O port, and interrupt logic allows high-speed hand shaking and data transfer through the bidirectional I/O ports, to make all of the high performance features cost effective, create ROM design and the on chip regulated back bias supply are used. The F3870 has all the attributes required of a successful microcomputer — low cost, high performance, excellent support and multiple sourcing.



PIN NAME	TYPE	DESCRIPTION
$\overline{P0_0}$-$\overline{P0_7}$ $\overline{P1_0}$-$\overline{P1_7}$ $\overline{P4_0}$-$\overline{P4_7}$ $\overline{P5_0}$-$\overline{P5_7}$	INPUT/OUTPUT	32 lines which can be individually used as either TTL compatible inputs or as latched outputs.
$\overline{STROBE}$	OUTPUT	This pin, which is normally HIGH, provides a single LOW pulse after valid data is present on the $\overline{P4_0}$-$\overline{P4_7}$ pins during an output instruction.
$\overline{RESET}$	INPUT	$\overline{RESET}$ may be used to externally reset the F3870. When pulled LOW the F3870 will reset. When then allowed to go HIGH the F3870 will begin program execution at the program location H '0000'.

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Ports 0 And 1 Are Standard Output Type Only

Ports 4 And 5 May Both Be Any Of The Three Output Options

The STROBE Output Is Always Configured Similar To A Standard Output Except That It Is Capable Of Driving Three TTL Loads

Fig. 2 I/O Pin Conceptual Diagram With Output Buffer Options

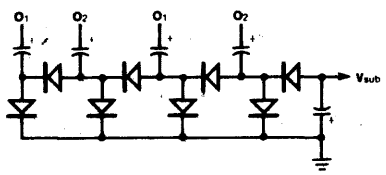


Fig. 7 Back-Biased Power Supply

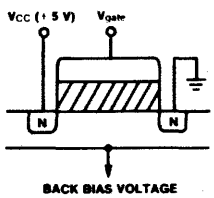


Fig. 6 Simple MOS Transistor

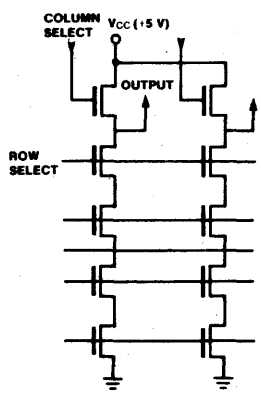


Fig. 4 ROM Design

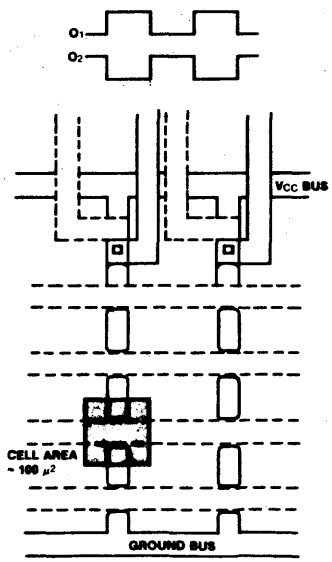


Fig. 5 ROM Layout

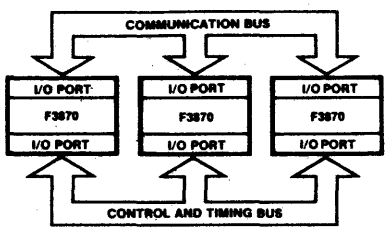


Fig. 3 Multiple F3870s

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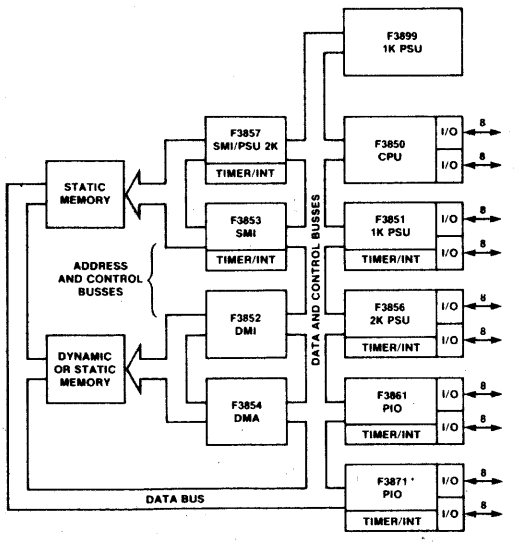
PORT ADDRESSING

F8 MICROPROCESSOR FAMILY

Item	DEVICE NO.	PORT A		PORT B		PORT C		PORT D		TIMER INTERRUPT VECTOR ADDRESS	PORT TYPES
		ADDR.	FUNC.	ADDR.	FUNC.	ADDR.	FUNC.	ADDR.	FUNC.		
1	**F3850**	0	I/O	1	I/O						Standard
2	**F3851**	XXXXXX00	I/O	XXXXXX01	I/O	XXXXXX10	Control	XXXXXX11	Timer	Mask Option	Mask Option
3	**F3851A**	4	I/O	5	I/O	6	Control	7	Timer	H'0020'	Standard
4	**F3852**	H'OC'		H'OD'	Control	H'OE'		H'OF'			
5	**F3852/ SL31116**	H'EC'		H'ED'	Control	H'EE'		H'EF'			
6	**F3853**	H'OC'	Interrupt Vector Addr. Lo	H'OD'	Interrupt Vector Addr.Hi	H'OE'	Control	H'OF'	Timer	Software Programmable	
7	**F3854**	1111YY00	DMA Mem. Addr. Lo	1111YY01	DMA Mem. Addr. Hi	1111YY10	Control Hi Count	1111YY11	Lo Count		
8	**F3856**	XXXXXX00	I/O	XXXXXY01	I/O	XXXXXX10	Control	XXXXXX11	Timer	Mask Option	Mask Option
9	**F38T56**	XXXXXX00	I/O	XXXXXY01	I/O	XXXXXX10	Control	XXXXXX11	Timer	Mask Option	Mask Option
10	**F3856A**	8	I/O	9	I/O	H'OA'	Control	H'OB'	Timer	H'0024'	Standard
11	**F3857/ 38T57**					XXXXXX10	Control	XXXXXX11	Timer	Mask Option	Mask Option
12	**F3861A**	4	I/O	5	I/O	6	Control	7	Timer	H'0600'	Standard
13	**F3861B**	8	I/O	9	I/O	H'A'	Control	H'B'	Timer	H'0340'	Standard
14	**F3861C**	H'20'	I/O	H'21'	I/O	H'22'	Control	H'23'	Timer	H'0320'	Standard
15	**F3861D**	H'24'	I/O	H'25'	I/O	H'26'	Control	H'27'	Timer	H'0360'	Standard
16	**F3861E**	4	I/O	5	I/O	6	Control	7	Timer	H'0020'	Standard
17	**F3871E**	4	I/O	5	I/O	6	Control	7	Timer	H'0020'	Standard
18	**F3871F**	4	I/O	5	I/O	6	Control	7	Timer	H'0020'	Direct Drive
19	**F3871G**	4	I/O	5	I/O	6	Control	7	Timer	H'0020'	Open Drain
20	**F3871H**	8	I/O	9	I/O	H'A'	Control	H'B'	Timer	H'0420'	Standard

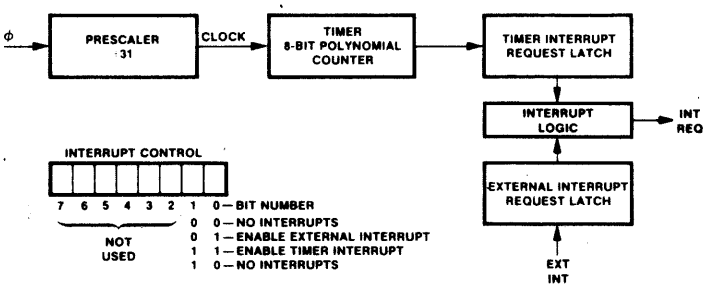
1. XXXXXX is a Mask Option
2. YY is a Pin Strap Option (1111YY00)
3. The External Interrupt Address Vector is the Timer Address + H'0080'
4. Three different types of timers and control ports exist. For further detail see Figures 1, 2, and 3.
5. F38T56 and F38T57 have F3871-type timer and strobe.logic.

F8 MICROPROCESSOR FAMILY

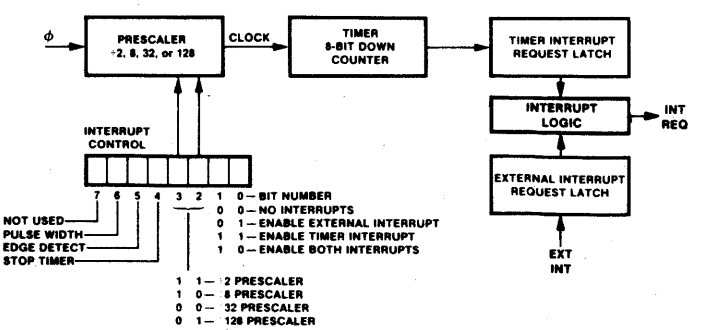


F8 FAMILY TIMERS

Timer and Interrupt Control for F3851, F3853 and F3861



Timer and Interrupt Control for F3856, F3857 and F3871



Fairchild

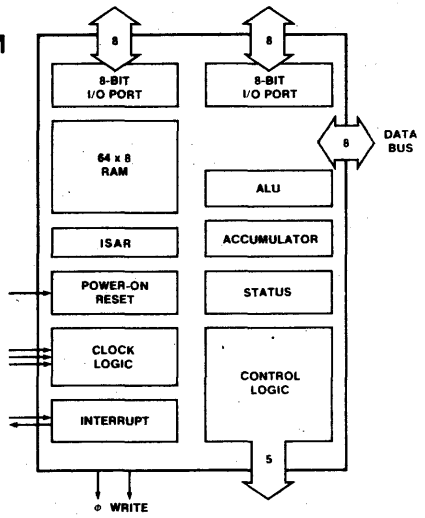
MICROPROCESSOR

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3850 Central Processing Unit (CPU)

Fairchild's F8 CPU contains all of the functions needed to provide the most inexpensive solution to your design problems. The 3850 has 64 bytes of RAM, 16 bits of bidirectional I/O and a complete set of easy to understand instructions with both binary and decimal arithmetic operations.

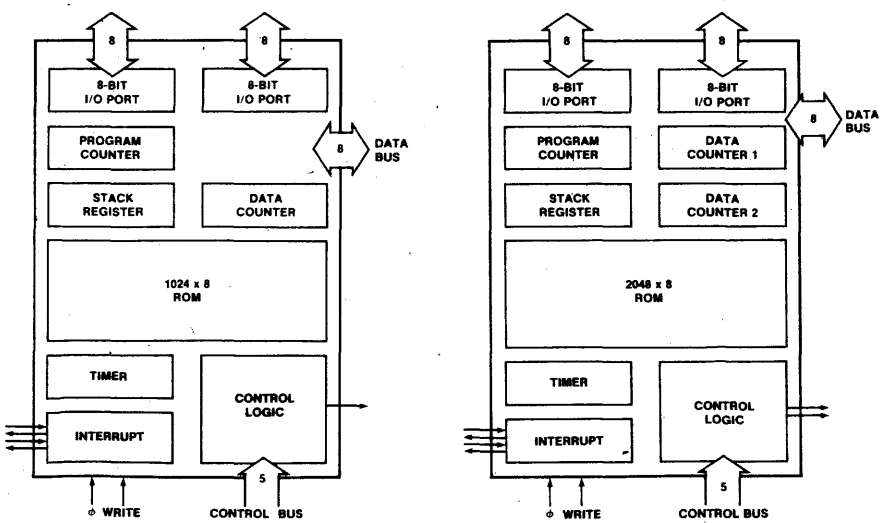
3850
CPU BLOCK DIAGRAM



3851/3856/38T56* Program Storage Units (PSUs)

The 3851 PSU contains 1K of program storage and the 3856 2K. Both provide 16 bits of bidirectional I/O, a timer and external interrupt and a vectorized, prioritized interrupt structure. Additional PSUs may be added as required and I/O expansion naturally follows.

*Uses special timer, see page



3851 3856

PSU BLOCK DIAGRAM

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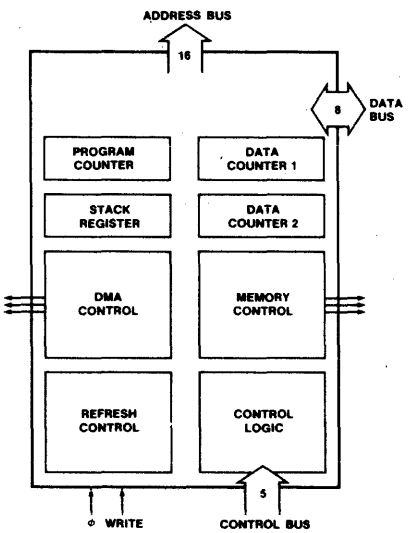
3852/3853/3857/38T57* Memory Interface Circuits

Additional memory can be easily added to the system by using any of the three Memory Interface Circuits. Each device generates the 16 address lines and signals necessary to interface with up to 65K bytes of RAM, PROM or ROM memory and they all may be used in conjunction with any standard semiconductor memory device.

The 3852 Dynamic Memory Interface (DMI) provides memory refresh and DMA logic which run transparent to the CPU without any degradation in the system throughput time.

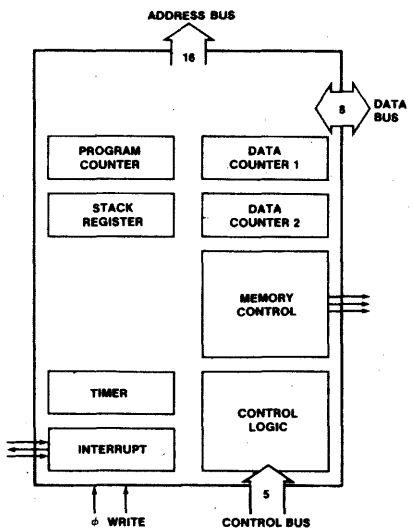
*Uses special timer, see page

3852
DMI BLOCK DIAGRAM



The 3853 Static Memory Interface (SMI) provides a programmable timer and external interrupt capability with a software loadable interrupt vector address in addition to the 16 address lines and memory control logic.

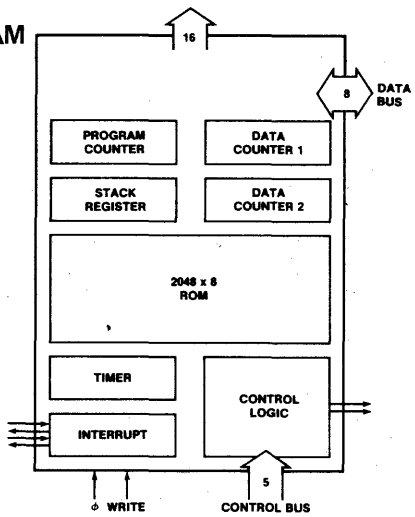
3853
SMI BLOCK DIAGRAM



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The 3857/38T57 Program Storage and Memory Interface (PSMI) provides 2K of ROM, an external interrupt and timer with masked interrupt vector as well as 16 address lines and memory control logic.

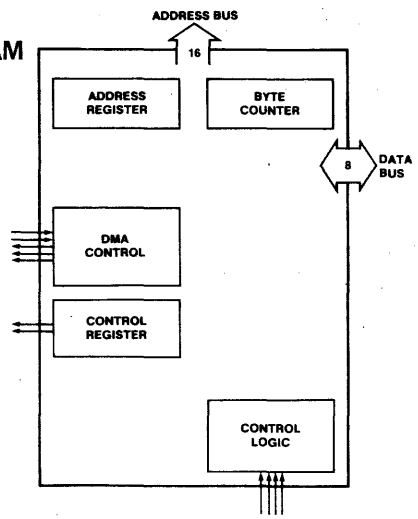
3857/38T57
PSMI BLOCK DIAGRAM



3854 Direct Memory Access (DMA)

The DMA circuits provide a high-speed data path between a system memory and the peripheral electronics with up to 500 kilo bytes of transparent data transfer per second. These circuits can transfer data blocks of up to 4096 bytes and can interrupt the CPU when this data transfer is complete or can be programmed to continue transferring until stopped.

3854
DMA BLOCK DIAGRAM



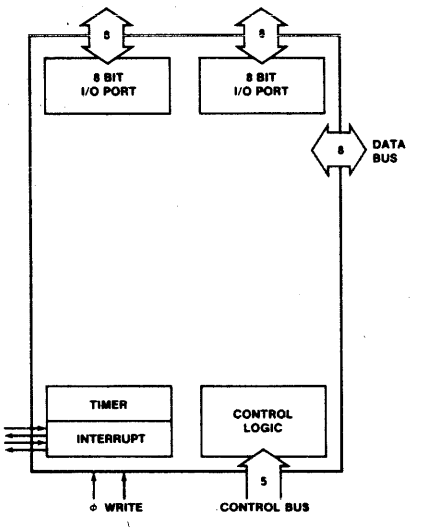
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3861/3871 Peripheral Input/Output

The 3861 PIO circuit contains all of the logic of the 3851 PSU without the 1K ROM. The 3861 is available in five versions as listed below.

TYPE	I/O PORTS	INTERRUPT ADDRESS VECTOR	
		TIMER	EXTERNAL
A	4-7	0600	0680
B	8-13	0340	03C0
C	20-23	0320	03A0
D	24-27	0360	03E0
E	4-7	0020	00A0

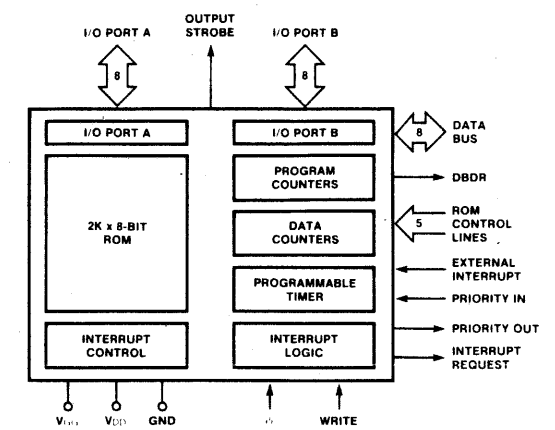
3861
PIO BLOCK DIAGRAM



The 3871 contains an improved timer and event counter. The 3871 is available in four versions as listed below.

TYPE	I/O PORTS	PORT TYPE	INTERRUPT ADDRESS VECTOR	
			TIMER	EXTERNAL
E	4-7	Standard	0020	00A0
F	4-7	Direct Drive	0020	00A0
G	4-7	Open Drain	0020	00A0
H	8-B	Standard	0420	04A0

3871
PIO BLOCK DIAGRAM



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THE FORMULATOR LINE OF F8 AND F3870 DESIGN AIDS

INTRODUCTION

The Microprocessor system designer can now create his own hardware and software development systems for the F8 and F3870 by selecting modular subassemblies from Fairchild's Formulator line of F8 and F3870 design aids. He may start development with a Mark I singleboard system, then expand to more sophisticated Mark II or Mark IIFD development systems that can handle both software and hardware development. Or he may graduate to a complete Formulator Mark III with intelligent front panel, power supply, and accessories or to the top of the line Formulator Mark IIIFD with floppy disk drives.

Three growth packages plus a selection of optional modules provide a practical method for upgrading the single-board Mark I to either the Mark II or Mark IIFD or to the maximum system configuration Mark III or Mark IIIFD. Using the growth packages, the designer can begin sophisticated system application programs at very low cost and then upgrade his development tools in relatively inexpensive steps, if he desires to do so at a later time.

The most elementary configuration, called the Formulator Mark I, includes a Processor module that contains an F8 CPU, Program Storage Unit that includes Fairbug monitor, Dynamic and Static Memory Interface circuits, 1024 bytes of random access memory, and the necessary buffers and other components for hardware development. It also includes a 13-slot card cage, an I/O cable kit, and a power cable.

The second level, the Formulator Mark II, includes all of the Mark I components plus a memory board with 16 kilobytes of RAM and the complete Formulator Operating System, designated FOS. FOS gives the user complete software development capability, including an assembler, editor, and debug package, and drivers for a teletype or the TI Silent 733 terminal.

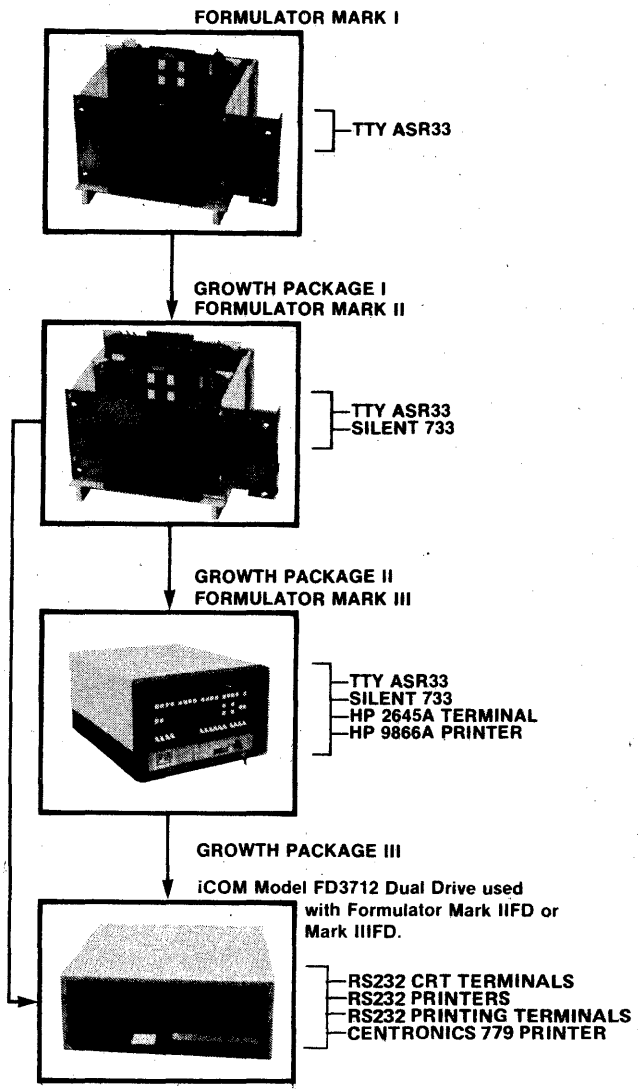
The third level, the Formulator Mark IIFD, consists of the Mark II with the addition of interface cards and cables for an iCOM FD3712 dual-drive floppy disk system and Fairchild F8-DOS-III Floppy Disk Operating System.

The fourth level, the Formulator Mark III, includes an intelligent front panel, a serial communications module, a quad I/O module, an attractive cabinet, and a power supply. Also included are 16 kilobytes of RAM, the Formulator Processor Module, and the Formulator Operating System.

The top of the line is the Formulator Mark IIIFD. This microcomputer is identical to the Mark III with the addition of the iCOM dual drive floppy disk and interface.

Three growth packages are available for Mark I, Mark II, and Mark III expansion. Growth Package I upgrades the Mark I system to the Mark II level. Growth Package II converts the Mark II to the full Mark III level. Growth Package III upgrades either the Mark II or Mark III to the Mark IIFD or the Mark IIIFD floppy disk configurations.

Other boards are available as options for all five Formulator configurations to increase the flexibility of the units by adding to their capabilities. These include 4-kilobyte RAM, 4-kilobyte PROM, and 16-kilobyte RAM boards, as well as and I/O light board, a communications board with UART, a parallel-byte board for peripheral interface, and a PROM programmer.



FORMULATOR GROWTH PATHS

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FORMULATOR SUPPORT

In addition to the optional boards, peripherals, cables, and other accessories, the Mark I, Mark II, and Mark III Formulator systems are supported by a wide range of documentation, and an intensive training program.

FORMULATOR DOCUMENTATION

The Formulator user has access to a full range of reference and instructional manuals to aid him in his system design and programming.

F8 USER'S GUIDE

The F8 User's Guide is a detailed description of the F8 family of microprocessor devices. Microprocessor systems are discussed, with the configurations of the F8 circuits examined in depth. The User's Guide also outlines the F8 instruction set. Detailed specifications of each member of the F8 microprocessor family is given, including functional descriptions, logic diagrams, signal load levels, and timing diagrams for each circuit. Typical F8 system configurations are also presented.

GUIDE TO PROGRAMMING

The Guide to Programming is written for logic designers with little or no background in computer programming. It introduces machine and assembly language programming to the potential user of microprocessors and microcomputer systems. Introductory topics include flowcharting, memory allocation, source and object programs, and assembly language. More advanced topics include programmed /O, interrupts, programmable timers, subroutines, macros, data manipulation, and programmed direct memory access channels. Numerous examples of these programming techniques are given.

FORMULATOR USER'S GUIDE

The Formulator User's Guide fully describes the operation of the Formulator Development System. It covers the Mark I, Mark II, and Mark III hardware configurations and contains a detailed description of the Formulator software—the monitor, the editor, the assembler, and the debug program. The F8 DOS-III User's Guide is also available for Mark IIFD and Mark IIIFD systems.

FORMULATOR HARDWARE REFERENCE MANUAL

This book presents an in-depth technical description of the F8 Formulator System, its component subsystems, and options. The technical description includes general functional characteristics, theory of operation, and detailed description of interface signals.

F8 TRAINING CLASS

To help applications engineers start designing with the F8 microprocessor, Fairchild offers an intensive four-day training course. Lectures are presented dealing with F8 features, architecture, and programming. In laboratory sessions, students prepare and run small F8 programs using the Formulator development systems.

SOFTWARE SUPPORT

FOS— FORMULATOR OPERATING SYSTEM

The software for the Formulator products is specifically designed to assist engineers and programmers during the development phase of a microcomputer-based system. Designated the Formulator Operating System (FOS), this software package consists of a monitor, an editor, an assembler, a linking loader, a debug package, and several utility programs.

The editor assists the user in the creation of a source file, which the assembler then converts into an object file ready for loading into the system. This object file may, at the option of the user, be a relocatable file. If several such relocatable object files exist, they may be combined by the linking loader and assigned absolute addresses at loading.

The debug portion of FOS allows users to test for fast and efficient program testing, for setting software breakpoints, and for examining and altering memory, registers, and I/O ports.

Unlike other development systems with limited storage capability, the Formulator has enough memory so that the editor, relocating assembler, and debug packages are simultaneously resident, with transfer from one to the other controlled by the monitor. Thus, a program may be created, edited, assembled, and debugged without ever having to reload the system software, since the user may switch from the editor to the assembler to the debug program directly from the monitor.

The Formulator software also includes utility programs which perform specific functions. One, for instance, generates a file for producing a ROM code. Another creates a file needed by a PROM programmer. These utility programs are loaded into the system under the control of the monitor.

The combined effect of the interrelated portions of the Formulator Operating System is the rapid generation and checkout of F8 and F3870 microcomputer-based systems. These programs greatly simplify the effort required to develop and alter the end user software, making it easy to design and debug a system breadboard, easy in terms of reduced time and manpower.

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FOS SUMMARY			
Disk Monitor	**Editor**	**Relocating Assembler**	**Real-Time Debugger**
Assemble (Relocating)	Move Line	No-List Option	Symbolic Debugging
Load (Linking)	Copy Line	No-Object Option	Set Up to 8 Breakpoint
Edit Mode	Bottom	Error Messages	Clear Breakpoint
Load (Absolute)	Change	Invalid Label	Clear All Breakpoints
DeBug Mode	Delete	Duplicate Label	Continue Execution
Assign Virtual I/O	File	Invalid Op Code	Go To Location
Burn PROM	Find String	Operand Error	Return to Monitor
Convert	Insert	Syntax Error	Single Step
ROM Dump	Locate String	Undefined Symbol	Trace On Long
	Next	Expression Storage	Trace on Short
	Replace	Overflow	Trace Off
	Tab	Relocatability	Display Memory
	Top	Error	Display Register
	Type	Pseudo Operand	Display Port
	Up	Error	Store Memory
		Cross Reference	Store Register
			Store Port

FDOS–FORMULATOR DISK OPERATING SYSTEM

The software for the Formulator products is specifically designed to assist engineers and programmers during the development phase of a microcomputer-based system. Designated the F8 DOS-III, this software package consists of a floppy-disk monitor, an editor, a relocating assembler, a linking loader, a debug package, and utility programs.

The disk monitor provides all of the necessary commands for fast and efficient file management during the creation, editing, assembly, and debugging of applications programs.

The editor assists the user in the creation of a source file, which the assembler then converts into an object file ready for loading into the system. This object file may, at the option of the user, be a relocatable file. If several such relocatable object files exist, they may be combined by the linking loader and assigned absolute addresses at loading.

The debug portion of F8-DOS-III provides for fast and efficient testing. Under Software Control, the user can set software and hardware breakpoints, and examine and alter memory, registers, and I/O ports.

Unlike development systems with limited storage capability, the Formulator Mark IIFD has enough memory so that the editor, assembler, and debug packages are resident as needed with transfer from one to the other controlled by the disk monitor. Thus, a program may be created, edited, assembled, and debugged without ever having to externally reload the system software, since the user may switch from the editor to the assembler to the debug program directly from the disk monitor.

The Formulator software also includes utility programs which perform specific functions. One, for instance, generates a file for producing a ROM code; another creates a file needed by a PROM programmer. These utility programs are loaded into the system under the control of the disk monitor.

The combined effect of the interrelated portions of the F8 DOS-III is the rapid generation and checkout of F8 and F3870 microcomputer-based systems. These programs greatly simplify the effort required to develop and alter the end-user software, making it easy to design and debug a system breadboard, easy in terms of reduced time and manpower.

ICOM® Advertised FD3700 Series Features	F8-DOS-III SUMMARY			
	Disk Monitor	**Editor**	**Relocating Assembler**	**Real-Time Debugger**
Fully IBM 3740 media and format compatible	Assemble (Relocating)	Move Line	No-List Option	Symbolic Debugging
Full formatter and controller built-in	Load (Linking)	Copy Line	No-Object Option	Set Up to 8 Breakpoint
Full sector Read/Write buffers allow	List Directory	Bottom	Error Messages	Clear Breakpoint
asynchronous or DMA data transfer	Print File	Change	Invalid Label	Clear All Breakpoints
Drive and diskette Write Protect capability	Rename File	Delete	Duplicate Label	Continue Execution
Positive latching door mechanism	Create File	File	Invalid Op Code	Go To Location
Up to 4 drives with no software or hardware	Delete File	Find String	Operand Error	Return to Monitor
modifications	Copy File	Insert	Syntax Error	Single Step
MTBF in excess of 2300 hours (FD 3712 dual	Merge Files	Locate String	Undefined Symbol	Trace On Long
drive)	Copy Disk	Next	Expression Storage	Trace on Short
Plug-in convenience allows MTTR of 18	Edit Mode	Replace	Overflow	Trace Off
minutes	Load (Absolute)	Tab	Relocatability	Display Memory
Front panel LED status indicators	DeBug Mode	Top	Error	Display Register
LED drive select indicators	Assign Virtual I/O	Type	Pseudo Operand	Display Port
Fully retracting head and pressure pad for	Burn PROM	Up	Error	Store Memory
maximum diskette life	Convert		Cross Reference	Store Register
50 pin flat ribbon cable with 3M interface	ROM Dump			Store Port
connector—FD 360 compatible				

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FORMULATOR MARK I

The first member of the Formulator family, the Formulator Mark I, is a basic microcomputer development tool providing the hardware necessary to build F8 or F3870 prototype systems. Included in the basic system is the Formulator Processor Module with the F8 CPU, Static Memory Interface, Dynamic Memory Interface, and Program Storage Unit devices. The Fairbug debug program, a 1K-byte monitor debug package, is included in the Program Storage Unit on the Processor Module. Fairbug provides the Mark I with sufficient debug capability to load a program, examine registers, monitor and alter memory locations, store a program on an external file, and generate a tape suitable for burning PROM memory devices. The Mark I also comes equipped with a 13-slot card cage and motherboard for attaching the modular Formulator printed circuit boards. Three slots are wired for the console control modules and one is dedicated to the Processor Module. The other nine connectors are general purpose slots which can accept additional Formulator modules for system expansion. Cables and documentation are also included in the F8 Formulator Mark I system, including a peripheral interface cable which can connect the Mark I to a Teletype ASR33 or TI Silent 733 for external communication.

Hardware

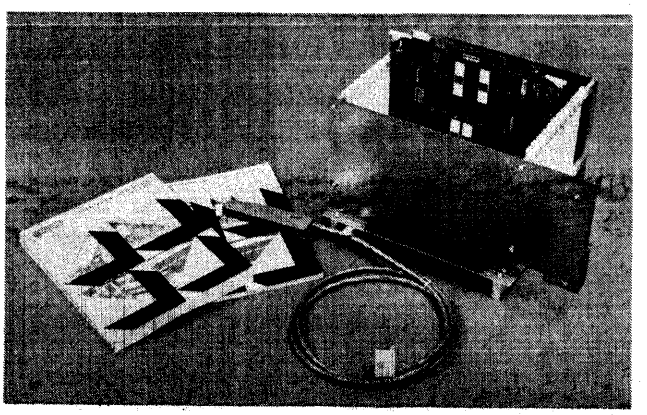
- Formulator Processor Module
- Formulator Card Cage and Motherboard
- Processor Module to Peripheral Cable
- Power Cable
- Cable Kit

Software

- Fairbug Debug Program

Documentation

- Formulator User's Guide
- Formulator Hardware Reference Manual
- Formulator Mark I Systems Coverage Manual
- Formulator Utilities Manual



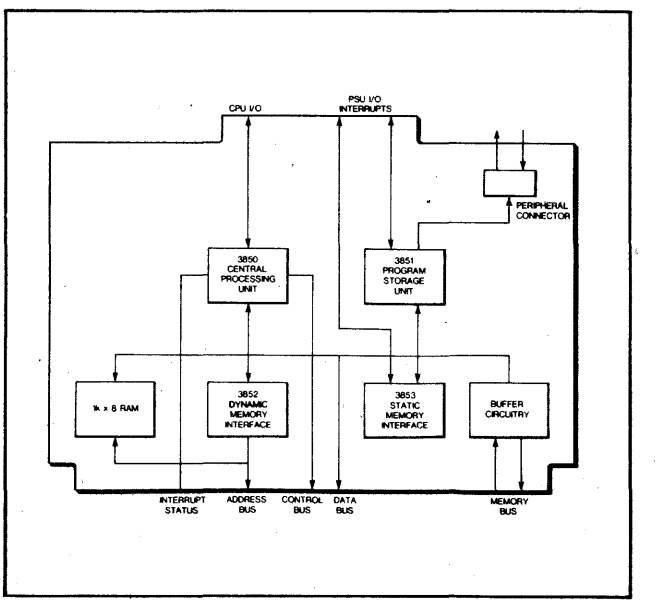
THE FORMULATOR PROCESSOR MODULE

The Formulator Processor Module is the heart of the Formulator family of development systems. As illustrated in the block diagram below, the 10½" × 7½" Processor Module contains a Central Processor Unit (F3850 CPU), a Program Storage Unit (F3851A PSU) with the Fairbug monitor, a Static Memory Interface circuit (F3853 SMI), a Dynamic Memory Interface circuit (F3852 DMI), a 1K-byte RAM memory, and a peripheral interface circuit. Also included is the circuitry necessary to drive the Formulator bus for easy expansion of system functions. The 32 bidirectional I/O lines are brought out to the top edge connector; bus signals are brought to a connector on the bottom of the board. The board connector plugs into the Formulator motherboard where the signals are bussed to twelve other sockets. The peripheral interface signals are brought out to a special connector mounted on the Processor Module. They include both a 20 mA current loop and an RS232 interface circuit.

Two interrupt levels are available on the Formulator Processor Module, one from the F3851A PSU and the other from the F3853 SMI. The on-board F3852 DMI allows dynamic memory refresh and direct memory access functions to be incorporated into expanded memory systems.

Switches on the Processor Module change the page address of the 1K-byte RAM memory. Additional switches are provided to change the port addresses of the PSU circuit, enable and disable the Fairbug program, select the clock mode (LC, crystal, or external), enable the interrupt priority, and select serial interface devices (RS232 or current loop).

The Fairbug program, located in the F3851A PSU communicates with an ASCII serial device, reads data from a parallel paper tape reader, and punches tape. The Fairbug program also performs a debug function allowing users to examine and alter internal registers and memory.



PROCESSOR MODULE

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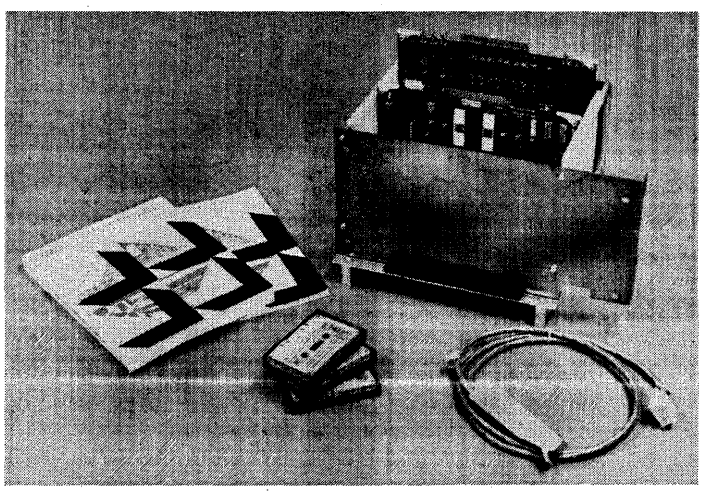
FORMULATOR MARK II

The second member is the Formulator Mark II. This unit is a low cost microcomputer software and hardware development tool. It includes the basic hardware required to develop a system, as well as the necessary software tools to develop F8 and F3870 code. The Mark II consists of all the components of the Mark I, namely the Processor Module, card cage and motherboard, cable kit, and the Fairbug debug program, as well as an additional 16K-byte RAM module. Also a part of the Mark II is the Formulator Operating System, including the editor, relocating assembler, and debug package to allow the generation of the source codes and to create and check out the object codes. Peripheral interfaces are also available to connect the Mark II to a TI Silent 733 or Teletype ASR33.

Hardware
- Formulator Processor Module
- 16K-Byte RAM Module
- Formulator Card Cage and Motherboard
- Processor Module to Peripheral Cable
- Power Cable
- Cable Kit

Software
- Formulator Operating System
- Fairbug Debug Program

Documentation
- Formulator User's Guide
- Formulator Hardware Reference Manual
- Formulator Systems Coverage Manual
- Formulator Utilities Manual



FORMULATOR MARK IIFD

The third member is the Formulator Mark IIFD, a floppy-disk based low-cost microcomputer software and hardware development tool. It includes the basic hardware required to develop a system, as well as the necessary software tools to develop F8 and F3870 code. The Mark IIFD consists of all the components of the Mark I, namely the Processor Module, card cage and motherboard, cable kit, and the Fairbug debug program, as well as an additional 16K-byte RAM Module. The F8-DOS-III is also a part of the Mark IIFD. It includes a floppy-disk file manager, editor, relocating assembler, and debug package to generate the source codes and to create and check out the object codes. The Mark IIFD can communicate with teletype ASR33 and other standard RS232 CRT or printing terminals.

Hardware
- Parallel Interface Module Prom Boot Loader Module
- Formulator Processor Module
- 16K-Byte RAM Module
- Formulator Card Cage and Motherboard
- Processor Module to Peripheral Cable
- Power Cable
- Cable Kit

Software
- F8-DOS-III Floppy Disk Operating System
- Fairbug Debug Program

Documentation
- Formulator User's Guide
- Formulator Hardware Reference Manual
- Formulator Systems Coverage Manual
- Formulator Utilities Manual
- DOS Users Guide

FORMULATOR MARK III

The fourth level of microprocessor development equipment is the Formulator Mark III, offering all of the design assistance required to develop F8 or F3970 based systems. The combination of hardware, software, and firmware offered by the Mark III assists the designer from the generation of source programs through the development of a prototype system. The Mark III is a modular microcomputer that accommodates a variety of memory, input/output, and communication configurations to form a new and powerful development system. It contains all of the components of the Mark II—the Processor Module, card cage and motherboard, cable kit, the Fairbug debug program, 16K bytes of RAM, and the Formulator Operating System. In addition, the Mark III includes a Quad I/O Module with four I/O ports and two interrupts, a Communications Module with an on-board UART, a universal breadboard for building user hardware configurations, an extender module, and an intelligent operator's panel. Power supplies for the Mark iii may be either 100 volts, 115 volts, or 220 volts at 50/60 Hz. Peripheral interfaces are available to connect the Mark III with a TI Silent 733, a Teletype ASR33, or an HP 2645A Mini-Data Station.

Hardware

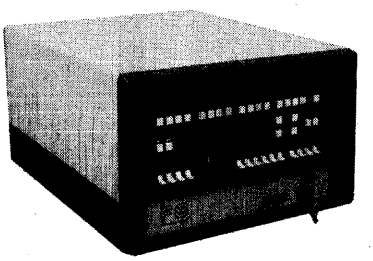
- Formulator Mainframe
- Designer's Console with Firmware
- Formulator Processor Module
- 16K-Byte RAM Module
- Quad I/O Port Module
- Communications Module
- Universal Breadboard
- Extender Module
- Cable Kit
- User I/O Cable Assembly
- Communications Module to Peripheral Cable

Software

- Fairbug Debug Program
- Formulator Operating System

Documentation

- Formulator User's Guide
- Formulator Hardware Reference Manual
- Formulator Systems Coverage Manual
- Formulator Utilities Manual



INTELLIGENT OPERATOR'S PANEL

Perhaps the most unique feature of the Mark III Formulator is the intelligent operator's panel, an array of lights and switches designed to give the user access to all registers and memory locations within the microcomputer, thus enabling an important interaction between the user and the system hardware and software.

The benefits of having a firmware controlled front panel are extensive. In addition to performing the normal front panel operations, such as examining and loading the contents of memory, the user's console can also perform some very complicated functions. Chief among these are the front panel's initial program load capability, its test function, and the real time hardware breakpoint feature.

The self test function is initiated by the user by merely depressing a single switch on the front panel. The console then begins to check the electronics in the Formulator. When an error condition is detected, the LED indicators on the display indicate the type of error and its location.

Another feature of the front panel is its ability, under operator control, to set a hardware breakpoint and to vary the number of times a memory location may be accessed before the break-in program execution occurs. This aids the user in performing fast, efficient debugging of his software.

MARK III FORMULATOR OPERATING SYSTEM

Like the Mark II Formulator Operating System, the Mark III FOS consists of a monitor, an editor, an assembler, a linking loader, a debug package, and several utility programs. In addition to the functions performed by each of these portions of the FOS in a Mark II system, the Mark III FOS includes the capability to set hardware breakpoints. It also contains a trace feature in the debug package which lets the user turn tracepoints on and off during the debug operation.

Two identical versions of the Formulator Operating System are available with the Formulator Mark III. One operates in the lower portion of memory and another operates in upper memory. The Low Memory Operating System resides in memory locations 1000 to 3FFF (Hex). Most of the lower 4K bytes of memory is reserved for user programs. The High Memory Operating System occupies locations with the hexadecimal addresses D000 to FFFF and uses the portion of memory from C000 to D000 to store the symbol table. With this system, the user has up to 48K bytes of continuous memory addresses available, eliminating the need for splitting programs larger than 4K bytes.

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FORMULATOR MARK IIIFD

The top of the line in microprocessor development equipment is the floppy-disk-based Formulator Mark IIIFD, offering all of the design assistance required to develop F8 or F3870 based systems. The combination of hardware, software, and firmware offered by the Mark IIIFD assists the designer from the generation of source programs through the development of a prototype system. The Mark IIIFD is a modular microcomputer that accommodates a variety of memory, input/output, and communication configurations to form a new and powerful development system. It contains all of the components of the Mark IIFD, the Processor Module, card cage and motherboard, cable kit, the Fairbug debug program, parallel interface, PROM boot loader, 16K bytes of RAM, and the F8-DOS-III disk operating system. In addition, the Mark IIIFD includes a quad I/O module with four I/O ports and two interrupts, a communications module with an on-board UART, a universal breadboard for building user hardware configurations, an extender module, and an intelligent operator's panel. Power supplies for the Mark IIIFD may be either 100 volts, 115 volts or 220 volts at 50/60 Hz. The Mark IIIFD can communicate with teletype ASR33 or other standard RS232 glass or printing terminals.

Hardware

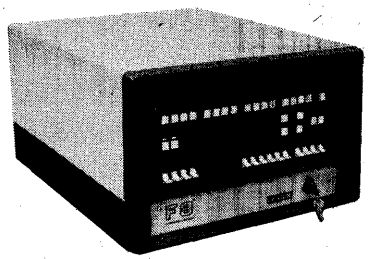
- Formulator Mainframe
- Designer's Console with Firmware
- Formulator Processor Module
- Parallel Interface Module
- PROM Boot Loader Module
- 16K-Byte RAM Module
- Quad I/O Port Module
- Communications Module
- Universal Breadboard
- Extender Module
- Cable Kit
- User I/O Cable Assembly
- Communications Module to Peripheral Cable

Software

- F8-DOS-III Floppy Disk Operating System
- Fairbug

Documentation

- Formulator User's Guide
- Formulator Hardware Reference Manual
- Formulator Systems Coverage
- Formulator Utilities Manual
- FDOS Users Guide

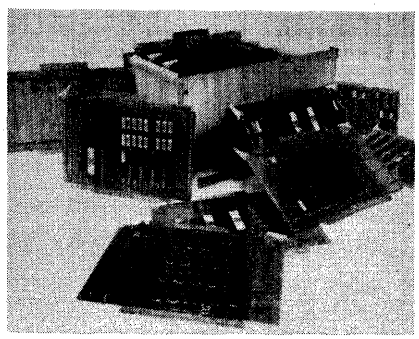


OPTIONAL FORMULATOR MODULES

Expansion of the Formulator microcomputers need not occur along the path indicated by the growth packages. Optional Formulator modules are available to expand RAM, PROM I/O, and communications, so the user can develop a custom system which is perfectly suited to his specific needs. These optional modules may be attached to the Formulator via the 13 card slots in the motherboard. The first three slots are dedicated to front panel operations of the Mark III. Another slot is reserved for the Processor Module. The remaining nine slots are linked on a common bus whose signals are compatible with the modules themselves. Additional system functions may be easily added to any Formulator system by simply plugging in one of the modules. Thus, the initial Formulator investment is preserved. Nothing needs to be discarded as demands upon the system increase. Unless otherwise noted, all of the following optional modules are available to update any Mark I, Mark II, Mark IIFD, Mark III, or Mark IIIFD system to meet expanded requirements.

Optional Modules

- 4K-Byte RAM Module
- 16K-Byte RAM Module
- Quad I/O Port Module
- 4K-Byte PROM Module
- Communications Module
- Byte Parallel Interface Module
- ROM Simulation Module
- Universal Breadboard
- Extender Module
- I/O Light Display Board



4K-BYTE RAM MODULE

The 4K-Byte Ram Module simplifies memory expansion in the Formulator Development Systems. Fully compatible with all Formulator bus signals, this board adds 4096 bytes of random access memory (using 2102 type static RAMs) to a system. Switches mounted on the printed circuit board allow the user to select the upper four address bits, so multiple memory modules may be used in a system. A write-protect switch puts the memory in a read-only mode at the user's discretion. Board dimensions are 10½" × 7½".

EXTENDER MODULE

During the checkout of the user's own breadboard systems, the Formulator Extender Module can be used to facilitate access to the user's hardware configuration contained on the universal breadboard. The 10½" × 7½" extender module plugs directly into the Formulator motherboard, and the module to be examined attaches to the 100-pin connector on the top edge of the extender card. Thus, the user's module is elevated above the other modules in the Formulator card cage for easy access.

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16K-BYTE RAM MODULE

The 16K-Byte RAM Module provides additional modularly expandable memory for the Formulator Development System. Fully compatible with all Formulator bus signals, this board adds 16 kilobytes of random access memory (4K N-MOS Dynamic RAM) to a system. Switches mounted on the printed circuit board allow the user to select the upper two address bits, so multiple memory modules may be used in a system. Four write-protect switches put the memory in a 'read only' mode at the user's discretion. The refresh of the dynamic memory is controlled by the F3852 Dynamic Memory Interface circuit mounted on the Processor Module. The refresh cycles are performed during unused data bus periods, and do not interfere with normal system timing. The board dimensions are 10½" × 7½".

4K-BYTE PROM MODULE

Additional memory expansion in the Formulator systems may be easily performed with the use of the 4K-Byte PROM Module. This board adds 4096 bytes of nonvolatile memory storage capability. It provides 16 sockets for the Fairchild 93446 TTL fuseable link 512 × 4-bit PROMs configured in a 4-kilobyte array. Four switches mounted on the printed circuit board allow the memory page to be switch selectable. All data bus and control bus signals are compatible with the Formulator system, so the board plus directly into the Formulator motherboard. The 93446 PROM devices may be programmed by the Formulator PROM Programmer. The board dimensions are 10½" × 7½".

ROM Simulation Module

The ROM Simulation Module allows the user to interface the F3851A and F3856 Program Storage Units to the Formulator systems. Two of these 40-pin devices may be inserted in each ROM Simulation Module, creating an excellent environment for checking out ROM codes stored on the PSUs.

BYTE PARALLEL INTERFACE MODULE

The Byte Parallel Interface Module interfaces the Formulator system to external devices in a parallel format. This 10½" × 7½" module creates a data bus and a control bus for passing information to and from the system. The bidirectional data bus can be used for either 8- or 16-bit parallel words. The 8-bit control bus synchronizes data transfer to and from the Formulator system. The F8 I/O ports. One level of F8 interrupt logic and one F8 interval timer are also available to the user. On-board switches select the F8 interrupt address vector and the F8 I/O port addresses. The signal levels for the device interface are given below.

Receive

V_{IL}	I_{IL}	V_{IH}	I_{IH}	V_{CC}
0.4V	−0.2mA	5.25V	25 μA	5.25V

Drive

V_{OL}	I_{OL}	V_{OH}	I_{OH}	V_{CC}
0.5V	48mA	2.4V	−10mA	4.75V

QUAD I/O PORT MODULE

The Quad I/O Port Module makes expanding the Formulator I/O capability an easy task. This board uses existing F8 I/O ports, so actual F8 signal levels are brought out to the edge connector on the top of the module. This module has two F8 circuits, each with two I/O ports, one interrupt level, and one programmable timer. Thus, a total of four ports (32 bits), two interrupt levels, and two timers are available to the user. Switches mounted on the card allow the user to select the I/O port addresses and the interrupt vector addresses for each F8 circuit. Thus, since each board may use different I/O ports, multiple boards may be used in a system. The board dimensions are 10½" × 7½".

COMMUNICATIONS MODULE

The Communications Module provides the electrical interface for any one of three types of serial peripheral devices, a standard teletype 20 mA current loop, RS-232 interface, or a TTL compatible device. An on board UART (Universal Asynchronous Receiver Transmitter) is used to perform the conversion between the 8-bit parallel microcomputer data and the serial signal, thus permitting high speed data transfer. Thirteen baud rates, ranging from 50 to 9600 baud, can be set from switches mounted on the card. A crystal is used to ensure accurate timing. The UART-microcomputer interface is maintained via two F8 I/O ports, also located on the printed circuit board. The F8 timer and interrupt logic are also available to the user, with the interrupt address vector and F8 I/O port numbers switch selectable. Board dimensions are 10½" × 7½".

I/O LIGHT DISPLAY BOARD

The I/O Light Display Board monitors the status of the F8 I/O signals of either the Formulator Processor Module or the Formulator Quad I/O Module. Mounted on the printed circuit cards are red LEDs, grouped in two rows of twenty, allowing up to four I/O ports plus power supplies to be viewed simultaneously. On-board drivers provide sufficient current levels to drive the LEDs. Additional lights on the board show the status of the external interrupts. The board dimensions are 10½" × 4½".

UNIVERSAL BREADBOARD

The universal breadboard is an empty Formulator module board which can aid in the development of the user's own breadboards. It is a 10½" × 7½" Formulator motherboard-compatible module which is predrilled to accept standard 14, 16, 18, 22, 24, and 40-pin dual inline packages. It will accomodate forty-four 16-pin packages. With the universal breadboard, the Formulator user may design his own breadboard configuration of non-microprocessor circuits while in constant contact with the microprocessor development tools of the Formulator.

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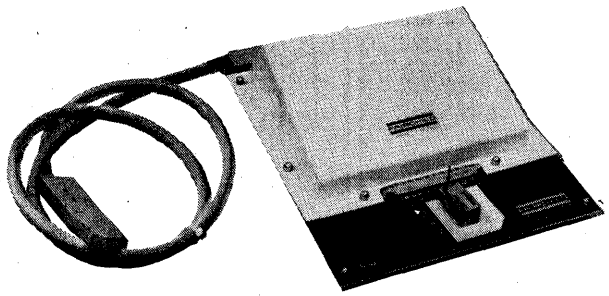
PROM PROGRAMMER

The ability to easily program permanent memory devices is essential to any microprocessor design. The Formulator PROM Programmer connects to a Quad I/O Module within either a Formulator Mark II or a Formulator Mark III, permitting the programming of any of the following fuseable link or ultraviolet light eraseable PROMs from a pattern stored in the Formulator memory.

The 11" × 12" × 4" PROM Programmer is driven by a utility program contained within the Formulator Operating System and features a simple, easy to use command set. The commands, entered into the PROM Programmer from the Formulator peripheral via the keyboard, allow the user to transfer data from a PROM to memory, burn a PROM, verify a PROM pattern, manually enter a single byte of data, and display PROM locations using the system software. The programming idiosyncrasies of each PROM are contained in software look-up tables to relieve the user of intricate repetitious set-up. The procedure is simply to identify the PROM type (like 93448) and the PROM parameter look-up table is automatically invoked, defining such things as number of words, word bit length, burn time, wait time, retry conditions, etc. The programming is convenient enough to allow the PROM Programmer to be used in a production environment.

Included in the basic system are two socket boards, one for the Fairchild 93436/93446 PROMs and one for the 93438/93448 PROMs. Socket boards for the ultraviolet eraseable devices are also available. A cable to the Quad I/O Module and a power cord are also included in the basic unit.

Fairchild Fusible Link PROMS	Ultraviolet Eraseable PROMs
93436 (512 × 4)	2704 (512 × 8)
93446 (512 × 4)	2708 (1024 × 8)
93438 (512 × 8)	2716
93448 (512 × 8)	

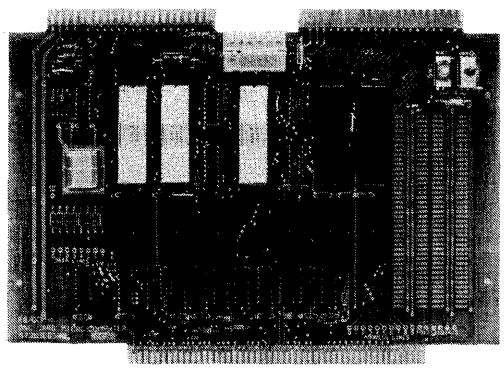


OCM-1 ONE-CARD MICROCOMPUTER

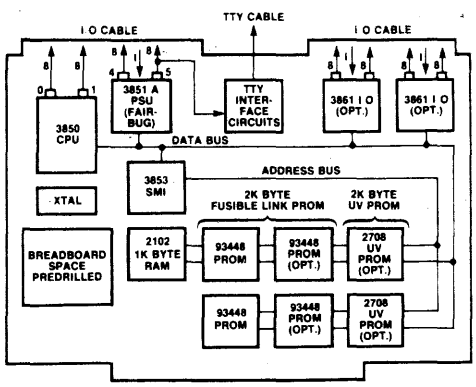
The OCM-1 is a complete microcomputer system contained on a single printed circuit board and offering the following features:

- 64-byte scratch pad memory
- 1K-byte RAM
- 8K-byte ROM (1K supplied, sockets provided for balance)
- 4K-byte EPROM (sockets provided)
- 4K-byte PROM (sockets provided)
- Up to four programmable timers
- Up to four programmable interrupts
- RS232 interface (current loop optional)
- 2 MHz clock
- Self-contained Fairbug teletype operating system
- Up to 64 individually programmable, bidirectional, latched I/O lines.

The unit is based on the F8 microcomputer and is fully supported by the Formulator family of program development aids. In addition, the OCM-1 contains a built-in teletype operating system, called Fairbug I, contained in the F3851A Program Storage Unit. Using an OCM-1-to-TTY cable assembly, the board can be directly coupled to a teletype or RS232 terminal to display or alter memory location, to load and punch paper tape, or to make entries from the keyboard or by program instruction. An alternative built-in operating system, K-D Bug, contained in the F3856A PSU is also available. It provides all of the Fairbug I functions plus a resident monitor to facilitate operation with a low-cost calculator-style keyboard and LED display. A Fairbug user's guide is provided with the OCM-1. The K-D Bug should be ordered as a separate item.



OCM-1 Module



OCM-1 Block Diagram

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The OCM-1 processor section includes the 3850 Central Processing Unit, the F3853 Static Memory Interface, a 2 MHz clock, and reset circuitry.

The OCM-1 memory section contains the capability for the use of five different types of storage including 64 bytes of scratch pad, 1K bytes of RAM, sockets for 2K bytes of EROM (2708), sockets for 2K bytes of fusible link PROM (93448), and the Fairbug I operating system.

The I/O portion of the system is contained in the F3850 Central Processing Unit and a F3851A Program Storage Unit, each containing two 8-bit I/O ports. Two sockets are provided for inserting standard F8 PIO circuits (F3861 or F3871) or, if more ROM is required, standard PSUs (F3851 or F3856) may be inserted. In either case, four additional I/O ports are provided bringing the maximum total to eight I/O ports (64 lines). Only single-byte instructions are required to individually program these lines for either input or output functions. Latches on each line reduce external hardware cost. A circuit on the board gives the OCM-1 the capability of communicating with a teletype, RS232 device or 20mA current loop.

In its standard configuration, the OCM-1 contains two interrupts and two timers, one in the F3851A PSU and one in the F3853 SMI. Two additional interrupts and timers may be added by plugging the two additional PIOs into their sockets. A "daisy-chained" priority system determines which interrupt will be serviced if two or more requests are made simultaneously.

The OCM-1 requires three power supply voltages: +12 V @ 0.255 A, −5 V @ 0.4 A and −5 V @ 0.09 A. The −5V supply is used only for the 2708 EROM devices. All supply voltages are ± 5 % maximum.

The entire microcomputer is contained on a single board (epoxy glass with solder mask) measuring approximately 7.5 inches by 10.5 inches. It includes a 2-inch by 4-inch predrilled breadboarding area for users who want to develop unique system configurations. In addition, a Formulator-compatible 100-pin edge connector, a special connector for TTY or terminal, and two 44-pin edge connectors for F8 signals, are contained on the board. A switch to enable the Fairbug operating system is also provided. The OCM-1 is delivered completed with OCM-1 Users Manual, Fairbug Users Guide and F8 Guide to Programming.

F387X PEP SYSTEM—PROGRAMMING EMULATING PROTOTYPING SYSTEM

A standalone single board system with Keyboard Display, Firmware Monitor, PROM Programming facilities is described previously in this section.

F3870 DEVELOPMENT SUPPORT

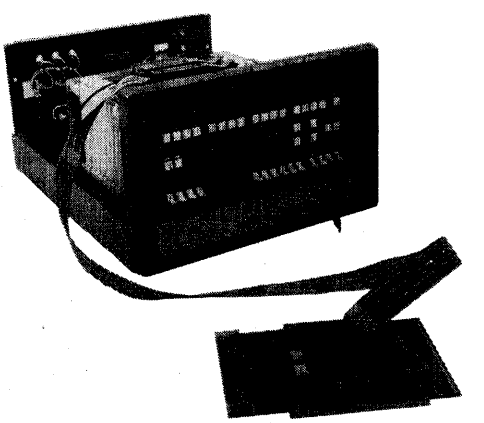
The F8 Formulator family of development equipment also supports the F3870, the one-chip microcomputer manufactured by Fairchild. The Formulator Operating System, utility program, and the Fairbug monitor are completely compatible with the F3870, since it shares the same instruction set with the Formulator. A Simulation (Quad I/O) Module and an In-Circuit Emulation (ICE) cable are available to extend the Formulator features to the user's prototype or production breadboard. This creates a powerful design tool for creating the user's own F3870 software. In addition, the F3870 Emulator, a single stand-alone module for emulating the final F3870 software in PROMs, is available for building prototype systems.

F3870 SIMULATION

The non-microprocessor elements of the user's hardware configuration can be assembled on a breadboard and connected to Mark I, II, IIFD, III or IIIFD via the ICE cable plugged into a 40-pin socket on the user's board. The cable connector on the Processor Module in the Formulator provides I/O ports 0 and 1, while the Simulation (Quad I/O) Module provides I/O ports 4 and 5. This system provides real-world simulation of the user's components in their actual environment with the vital microprocessor signals, including the complete software debugging features of the Formulator, cabled to the external breadboard.

F3870 EMULATOR

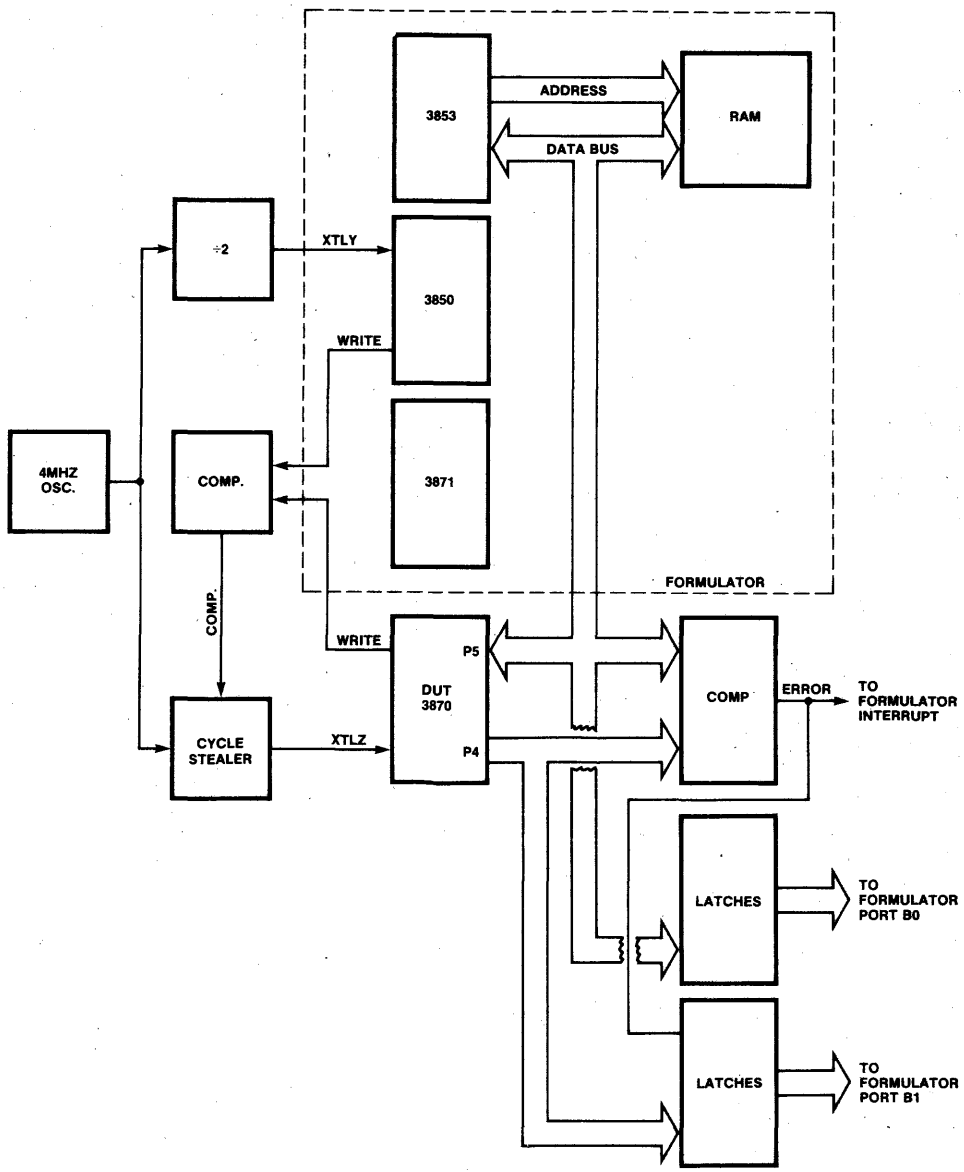
After F3870 ROM codes are frozen, a smaller, easier-to-handle and less expensive tool is required. To accomplish this design-in task, Fairchild has developed the F3870 Emulator. The F3870 Emulator contains sockets for two 2708s or two 2716 EROMs in place of the F3870 on-chip ROM so ROM codes can be verified and easily changed. The F3870 Emulator plugs directly into the F3870 40-pin socket in the production prototype using a short Emulator cable. The printed circuit module is approximately 5″ by 7 ″.



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F387X Functional Tester

- Complete function testing for F387X
- Available as an accessory for the Formulator development system
- No "Gold device" needed
- Load ROM code to RAM then compare to F387X
- GO/NO GO or complete diagnostic printout available
- Low cost system
- Complete software test program provided for Formulator Mark II or Mark III



Formulator Tester for F3870

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F6800

MICROPROCESSING UNIT (MPU)

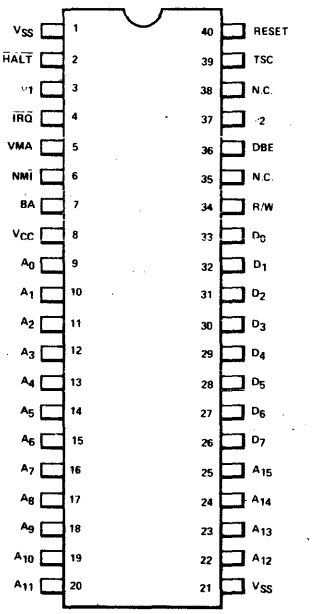
FAIRCHILD F6800 MICROCOMPUTER FAMILY

GENERAL DESCRIPTION – The F6800 is a monolithic 8-bit microprocessor forming the central control function for Fairchild's F6800 family. Compatible with TTL, the F6800, as with all F6800 system parts, requires only one 5.0 V power supply and no external TTL devices for bus interface.

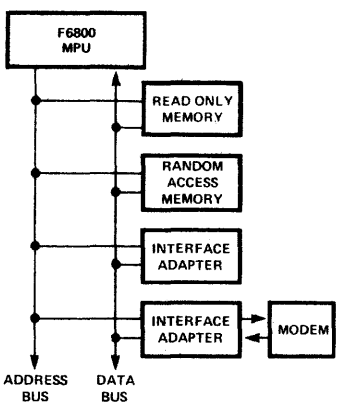
The F6800 is capable of addressing 65K bytes of memory with its 16-bit address lines. The 8-bit data bus is bi-directional as well as 3-state, making direct memory addressing and multiprocessing applications possible. Two temperature ranges are available. The F6800 is 0°C to 70°C and the F6800C is –40°C to +85°C.

- **8-BIT PARALLEL PROCESSING**
- **BI-DIRECTIONAL DATA BUS**
- **16-BIT ADDRESS BUS – 65K BYTES OF ADDRESSING**
- **72 INSTRUCTIONS – VARIABLE LENGTH**
- **SEVEN ADDRESSING MODES – DIRECT, RELATIVE, IMMEDIATE, INDEXED, EXTENDED, IMPLIED AND ACCUMULATOR**
- **VARIABLE LENGTH STACK**
- **VECTORED RESTART**
- **MASKABLE INTERRUPT VECTOR**
- **SEPARATE NON-MASKABLE INTERRUPT – INTERNAL REGISTERS SAVED IN STACK**
- **SIX INTERNAL REGISTERS – TWO ACCUMULATORS, INDEX REGISTER, PROGRAM COUNTER, STACK POINTER AND CONDITION CODE REGISTER**
- **DIRECT MEMORY ADDRESSING (DMA) AND MULTIPLE PROCESSOR CAPABILITY**
- **CLOCK RATES 1 MHz, 1.5 MHz, 2 MHz**
- **SIMPLE BUS INTERFACE WITHOUT TTL**
- **HALT AND SINGLE INSTRUCTION EXECUTION CAPABILITY**
- **TWO TEMPERATURE RANGES – F6800 0°C TO 70°C**
  F6800C –40°C TO +85°C

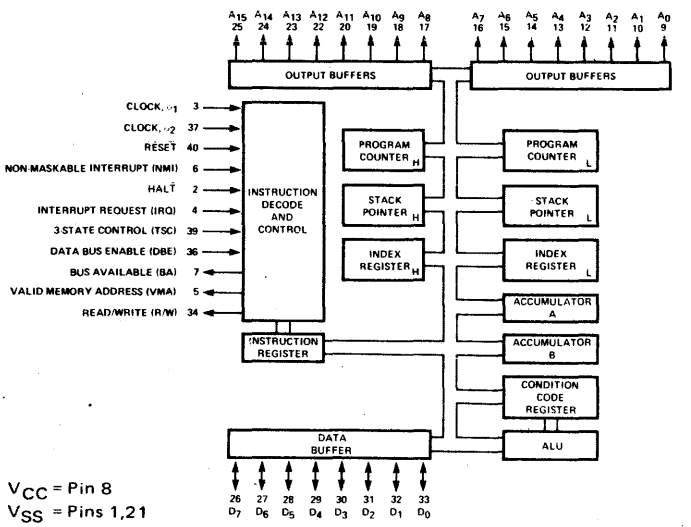
CONNECTION DIAGRAM
DIP (Top View)



F6800 MICROCOMPUTER FAMILY BLOCK DIAGRAM



F6800 BLOCK DIAGRAM



464 ELLIS STREET, MOUNTAIN VIEW, CALIFORNIA 94042 (415) 962-5011/TWX 910-379-6435

FAIRCHILD

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Manufactured under one or more of the following U.S. Patents: 2981877, 3015048, 3025589, 3064167, 3108359, 3117260, other patents pending

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F6800 MICROPROCESSOR FAMILY

DEVICE NO.	Function	Power Supply V	P_D Max (Typ) mW	Cycle Time ns	Access Time ns	Memory Size	Package(s)
F6800	MPU, Address, Interrupt	5.0	(600)	1000			6I,8P
F68A00	MPU, Address, Interrupt	5.0	(500)	667			6I,8P
F68B00	MPU, Address, Interrupt	5.0	(500)	500			6I,8P
F6801(1)	Single Chip Microcomputer with 128x8 RAM	5.0	(500)	500		2Kx8 (ROM)	6I,8P
F6802	MPU, Address, RAM Interrupt	5.0	(600)[3]	1000		128x8 (RAM)	6I,8P
F6803	MPU, Internal Clock	5.0	(500)	500		128x8 RAM	6I,8P
F6803E	MPU, External Clock	5.0	(500)	500	128x8	6I,8P RAM	
F6809(2)	MPU, Address, Interrupt	5.0		500/1K			6I,8P
F6810	Statis RAM	5.0	(400)		460	128x8	7R,9N
F68A10	Static RAM	5.0	(400)		360	128x8	7R,9N
F68B10	Static RAM	5.0	(400)		250	128x8	7R,9N
F6814	Static RAM	5.0	(350)		200	1024x4	7T,9M
F6816	Dynamic RAM	5.0	(465)		200	4Kx1	62,8K,8R
F6820/21	Parallel I/O 16 lines	5.0	550	1000			6I,8P
F68A21	Parallel I/O 16 lines	5.0	550	667			6I,8P
F68B21	Parallel I/O 16 lines	5.0	550	500			6I,8P
F68308	Mask Prog ROM	5.0	(650)		500	1Kx8	7R,9N
F68A308	Mask Prog ROM	5.0	(650)		360	1Kx8	7R,9N
F68B308	Mask Prog ROM	5.0	(650)		250	1Kx8	7R,9N
F68316	Mask Prog ROM	5.0			500	2Kx8	7R,9N
F68A316	Mask Prog ROM	5.0			360	2Kx8	7R,9N
F68B316	Mask Prog ROM	5.0			250	2Kx8	7R,9N
F6840	Programmable Timer	5.0	550	1000			8E,9Y
F68A40	Programmable Timer	5.0	550	667			8E,9Y
F68B40	Programmable Timer	5.0	550	500			8E,9Y
F6843(1)	Floppy Disk Interface	5.0					6I,8P
F6844(1)	Direct Memory Access	5.0					6I,8P
F6845(1)	CRT Controller	5.0					6I,8P
F6846	ROM, I/O, Timer	5.0	800	1000		2Kx8	6I,8P
F68A46	ROM, I/O, Timer	5.0	800	667		2Kx8	6I,8P
F68B46	ROM, I/O, Timer	5.0	800	500		2Kx8	6I,8P
F6847	Video Sync Generator	5.0					6I,8P
F68488	GPIA (IEEE Bus)	5.0	(600)	1000			6I,8P

DEVICE NO.	Function	Power Supply V	P_D Max (Typ) mW	Cycle Time ns	Access Time ns	Memory Size	Package(s)
F6850	Async Data Adapter	5.0	(300)	1000			7R,9N
F68A50	Async Data Adapter	5.0	(300)	667			7R,9N
F68B50	Async Data Adapter	5.0	(300)	500			7R,9N
F6852	Sync Data Adapter	5.0	(300)	1000			7R,9N
F68A52	Sync Data Adapter	5.0	(300)	667			7R,9N
F68B52	Sync Data Adapter	5.0	(300)	500			7R,9N
F6854	Advanced Data Link CTL	5.0	750	1000			8E,9Y
F68A54	Advanced Data Link CTL	5.0	750	667			8E,9Y
F68B54	Advanced Data Link CTL	5.0	750	500			8E,9Y
F68708	EPROM	5.0	800		450	1Kx8	QA
F68716	EPROM	5.0	500		450	2Kx8	QA

MICROPROCESSOR PERIPHERALS

Function	DEVICE NO.	Temperature(3)	No. of Pins	Package(s)
USART	F3843	C	28	8E,9Y
Synchronous Protocol Communications Controller	F3846(1) F6856	C	40	6I,8P

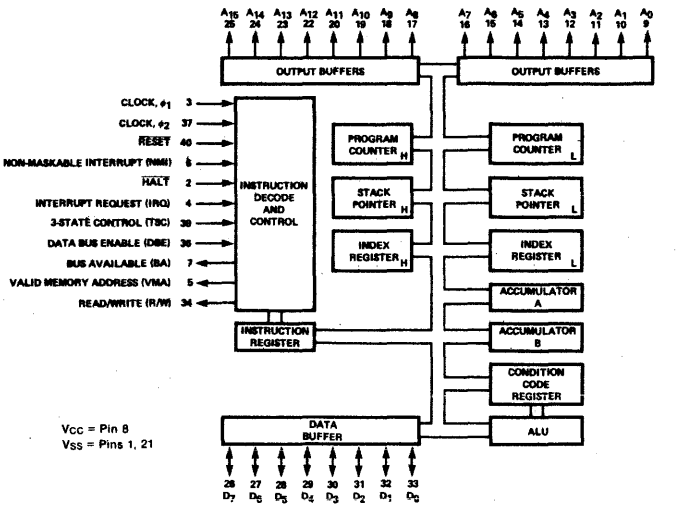
1. To be announced.
2. F6809 supports the F6800 instruction set but also has enhanced instructions and additional hardware features.
3. C = Commercial temperature range.

F6800 MICROPROCESSING UNIT (MPU)

GENERAL DESCRIPTION – The F6800 is a monolithic 8-bit microprocessor forming the central control function for Fairchild's F6800 family. Compatible with TTL, the F6800, as with all F6800 system parts, requires only one 5.0 V power supply and no external TTL devices for bus interface.

The F6800 is capable of addressing 65K bytes of memory with its 16-bit address lines. The 8-bit data bus is bi-directional as well as 3-state, making direct memory addressing and multiprocessing applications possible. Two temperature ranges are available. The F6800 is 0°C to 70°C and the F6800C is –40°C to +85°C.

- 8-BIT PARALLEL PROCESSING
- BI-DIRECTIONAL DATA BUS
- 16-BIT ADDRESS BUS – 65K BYTES OF ADDRESSING
- 72 INSTRUCTIONS – VARIABLE LENGTH
- SEVEN ADDRESSING MODES – DIRECT, RELATIVE, IMMEDIATE, INDEXED, EXTENDED, IMPLIED AND ACCUMULATOR
- VARIABLE LENGTH STACK
- VECTORED RESTART
- MASKABLE INTERRUPT VECTOR
- SEPARATE NON-MASKABLE INTERRUPT – INTERNAL REGISTERS SAVED IN STACK
- SIX INTERNAL REGISTERS – TWO ACCUMULATORS, INDEX REGISTER, PROGRAM COUNTER, STACK POINTER AND CONDITION CODE REGISTER
- DIRECT MEMORY ADDRESSING (DMA) AND MULTIPLE PROCESSOR CAPABILITY
- CLOCK RATES 1 MHz, 1.5 MHz, 2 MHz
- SIMPLE BUS INTERFACE WITHOUT TTL
- HALT AND SINGLE INSTRUCTION EXECUTION CAPABILITY
- TWO TEMPERATURE RANGES – F6800 0°C TO 70°C
  F6800C –40°C TO +85°C



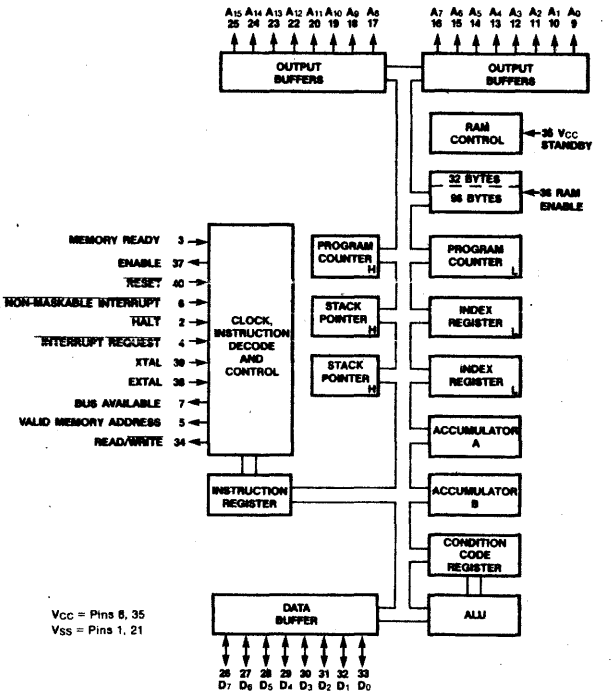
F6800 MPU

F6802 MICROPROCESSING UNIT (MPU) WITH RAM AND CLOCK

GENERAL DESCRIPTION—The F6802 is a monolithic 8-bit microprocessor that contains all the registers and accumulators of the present F6800 plus an internal clock oscillator and driver on the same chip. In addition, the F6802 has 128 bytes of RAM on board located at hex addresses 0000 to 007F. The first 32 bytes of RAM, at hex addresses 0000 to 001F, may be retained in a low power mode by utilizing V_{CC} standby, thus facilitating memory retention during a power-down situation.

The F6802 is completely software compatible with the F6800 as well as the entire F6800 family of parts. Hence, the F6802 is expandable to 64K words.

- ON-CHIP CLOCK CIRCUIT
- 128 x 8-BIT ON-CHIP RAM
- 32 BYTES OF RAM ARE RETAINABLE
- SOFTWARE-COMPATIBLE WITH THE F6800
- EXPANDABLE TO 64K WORDS
- STANDARD TTL-COMPATIBLE INPUTS AND OUTPUTS
- 8-BIT WORD SIZE
- 16-BIT MEMORY ADDRESSING
- INTERRUPT CAPABILITY
- TWO TEMPERATURES RANGES – F6802 0°C to 70°C
  F6802C –40°C to 85°C



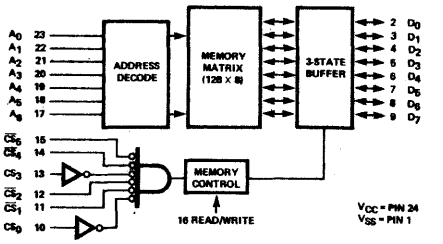
F6802 MPU

F6810 RANDOM ACCESS MEMORY (RAM)

GENERAL DESCRIPTION – F6810 is a byte-organized memory designed for use in bus-organized systems. It is fabricated with N-channel silicon-gate technology. For ease of use, the device operates from a single power supply, has compatibility with TTL and DTL, and needs no clocks or refreshing because of static operation.

The memory is compatible with the F6800 Microcomputer Family, providing random storage in byte increments. Memory expansion is provided through multiple Chip Select inputs.

- ORGANIZED AS 128 BYTES OF EIGHT BITS
- STATIC OPERATION
- BI-DIRECTIONAL 3-STATE DATA INPUT/OUTPUT
- SIX CHIP SELECT INPUTS (FOUR ACTIVE LOW, TWO ACTIVE HIGH)
- SINGLE 5 V POWER SUPPLY
- TTL COMPATIBLE
- MAXIMUM ACCESS TIME = 350 ns – F6810-1
  450 ns – F6810



F6810 RAM

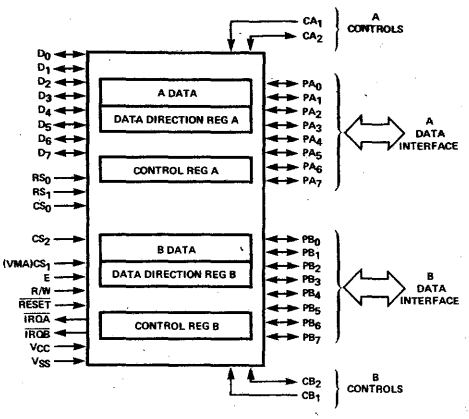
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F6821 PERIPHERAL INTERFACE ADAPTOR (PIA)

GENERAL DESCRIPTION — The F6821 Peripheral Interface Adapter provides the universal means of interfacing peripheral equipment to the F6800 Microprocessing Unit (MPU). This device is capable of interfacing the MPU to peripherals through two 8-bit bi-directional peripheral data buses and four control lines. No external logic is required for interfacing to most peripheral devices.

The functional configuration of the PIA is programmed by the MPU during system initialization. Each of the peripheral data lines can be programmed to act as an input or output, and each of the four control/interrupt lines may be programmed for one of several control modes. This allows a high degree of flexibility in the overall operation of the interface.

- 8-BIT BI-DIRECTIONAL DATA BUS FOR COMMUNICATION WITH THE MPU
- TWO BI-DIRECTIONAL 8-BIT BUSES FOR INTERFACE TO PERIPHERALS
- TWO PROGRAMMABLE CONTROL REGISTERS
- TWO PROGRAMMABLE DATA DIRECTION REGISTERS
- FOUR INDIVIDUALLY-CONTROLLED INTERRUPT INPUT LINES; TWO USABLE AS PERIPHERAL CONTROL OUTPUTS
- HANDSHAKE CONTROL LOGIC FOR INPUT AND OUTPUT PERIPHERAL OPERATION
- HIGH IMPEDANCE 3-STATE AND DIRECT TRANSISTOR DRIVE PERIPHERAL LINES
- PROGRAM CONTROLLED INTERRUPT AND INTERRUPT DISABLE CAPABILITY
- CMOS DRIVE CAPABILITY ON SIDE A PERIPHERAL LINES



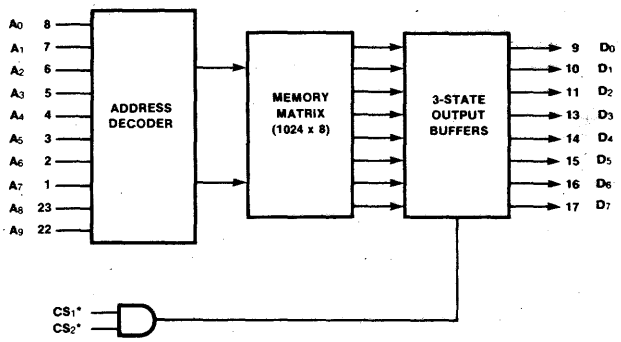
F6821 PIA

F68308 READ ONLY MEMORY (ROM)

GENERAL DESCRIPTION — The F68308 is a mask-programmable byte-organized memory designed for use in bus-organized systems. It is fabricated with n-channel silicon-gate technology. For ease of use, the device operates from a single power supply, has compatibility with TTL and DTL, and needs no clocks or refreshing because of static operation.

The memory is compatible with the F6800 Microcomputer Family, providing read only storage in byte increments. Memory expansion is provided through multiple Chip Select inputs. The active level of the Chip Select inputs and the memory content are defined by the customer.

- ORGANIZED AS 1024 BYTES OF 8 BITS
- STATIC OPERATION
- 3-STATE DATA OUTPUT
- MASK-PROGRAMMABLE CHIP SELECTS FOR SIMPLIFIED MEMORY EXPANSION
- SINGLE 5 V POWER SUPPLY
- TTL COMPATIBLE
- MAXIMUM ACCESS TIME = 500 ns
- 350 mW TYPICAL POWER DISSIPATION
- PIN COMPATIBLE WITH 2708 EPROM



*Active level defined by the customer.

VCC = Pin 24
GND = Pin 12

F68308 ROM

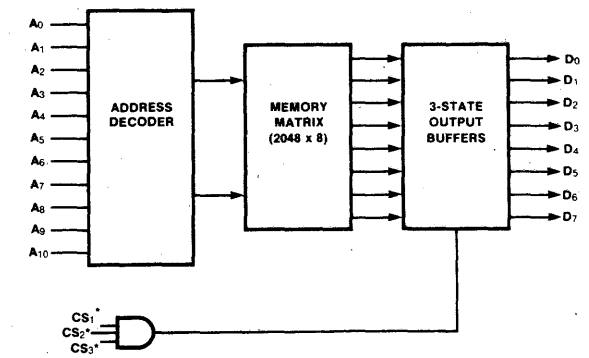
F68316 READ ONLY MEMORY (ROM)

GENERAL DESCRIPTION — The Fairchild F68316 is a mask-programmable byte-organized MOS Read Only Memory designed for use in bus-organized systems requiring non-volatile data storage. It is fabricated with n-channel silicon-gate technology. For ease of use, the F68316 operates from a single 5 V power supply, inputs and outputs are TTL and DTL compatible, and the device needs no clocks or refreshing because of its static operation.

The F68316 is compatible with Fairchild's F6800 Microcomputer Family providing read only storage in byte increments. To facilitate memory expansion, the device contains three programmable Chip Select inputs providing any combination of active HIGH or LOW or an optional DON'T CARE state coupled with output OR-TIE capability. Chip select code and memory content are defined by the user and are fixed during the masking process.

The F68316 provides maximum circuit density, reliability and performance yet maintains low power dissipation and yields significant cost advantages over an EPROM approach.

- COMPLETELY STATIC OPERATION
- 2048 x 8-BIT BUS COMPATIBLE ORGANIZATION
- SINGLE 5 VOLT POWER SUPPLY
- TTL AND DTL COMPATIBLE INPUTS
- 3-STATE DATA OUTPUTS
- OR-TIE CAPABILITY
- THREE PROGRAMMABLE CHIP SELECTS FOR SIMPLIFIED MEMORY EXPANSION
- MAXIMUM ACCESS TIME = 500 ns
- PIN COMPATIBLE WITH F2708 PROM
- DIRECTLY COMPATIBLE WITH 2316E



VCC = Pin 24
GND = Pin 12

*Active level defined by the user.

F68316 ROM

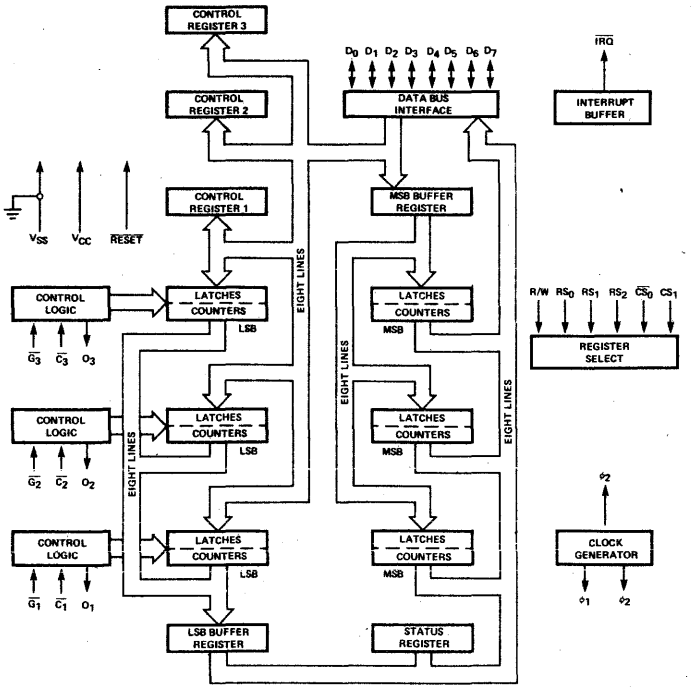
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F6840 PROGRAMMABLE TIMER (PTM)

GENERAL DESCRIPTION—The F6840 is a programmable subsystem component of the F6800 family designed to provide variable system time intervals.

The F6840 has three 16-bit binary counters, three corresponding control registers and a status register. These counters are under software control and may be used to cause system interrupts and/or generate output signals. The F6840 may be utilized for such tasks as frequency measurements, event counting, interval measuring and similar tasks. The device may be used for square wave generation, gated delay signals, single pulses of controlled duration, and pulse width modulation as well as system interrupts.

- OPERATES FROM A SINGLE 5 VOLT POWER SUPPLY
- FULLY TTL COMPATIBLE
- SINGLE SYSTEM CLOCK REQUIRED (ENABLE)
- SELECTABLE PRESCALER ON TIMER 3 CAPABLE OF A 4 MHz INPUT
- PROGRAMMABLE INTERRUPTS ($\overline{IRQ}$) OUTPUTS TO MPU
- READABLE DOWN COUNTER INDICATES COUNTS TO GO TO TIME-OUT
- SELECTABLE GATING FOR FREQUENCY OR PULSE-WIDTH COMPARISON
- $\overline{RESET}$ INPUT
- THREE ASYNCHRONOUS EXTERNAL CLOCK AND GATE/TRIGGER INPUTS INTERNALLY SYNCHRONIZED
- THREE MASKABLE OUTPUTS



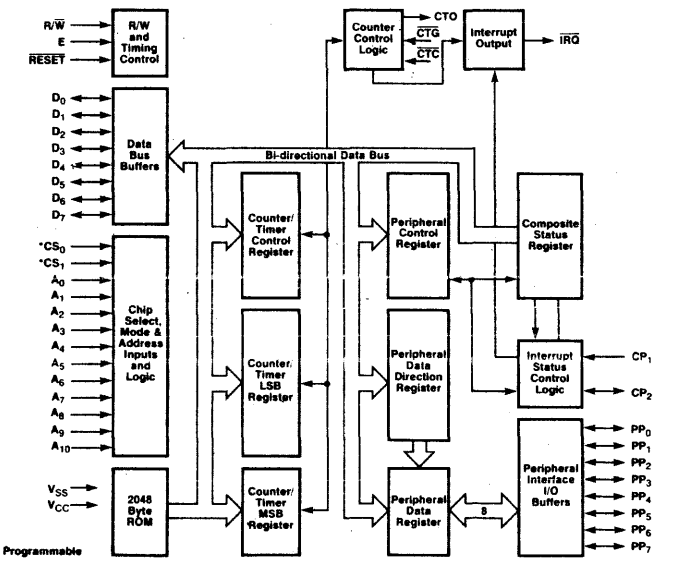
F6840 PTM

F6846 ROM-I/O-TIMER

GENERAL DESCRIPTION–The F6846 combination chip provides the means, in conjunction with the F6802, to develop a basic 2-chip microcomputer system. The F6846 consists of 2048 bytes of mask programmable ROM, an 8-bit bi-directional data port with control lines, and a 16-bit programmable timer-counter.

This device is capable of interfacing with the F6802 (basic F6800, clock and 128 bytes of RAM) as well as the F6800 if desired. No external logic is required to interface with most peripheral devices.

- 2048 8-BIT BYTES OF MASK-PROGRAMMABLE ROM
- 8-BIT BI-DIRECTIONAL DATA PORT FOR PARALLEL INTERFACE PLUS TWO CONTROL LINES
- PROGRAMMABLE INTERVAL TIMER-COUNTER FUNCTIONS
- PROGRAMMABLE I/O PERIPHERAL DATA, CONTROL AND DIRECTION REGISTERS
- COMPATIBLE WITH THE COMPLETE F6800 MICROCOMPUTER PRODUCT FAMILY
- TTL-COMPATIBLE DATA AND PERIPHERAL LINES
- SINGLE 5 VOLT POWER SUPPLY



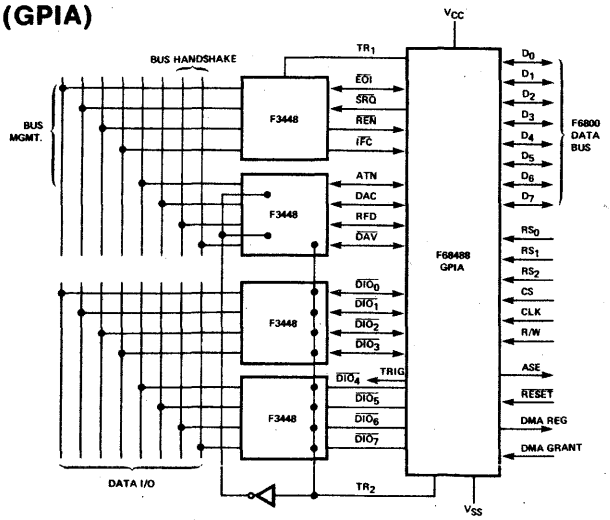
F6846 RIOT

F68488 GENERAL PURPOSE INTERFACE ADAPTER (GPIA)

GENERAL DESCRIPTION—The F68488 GPIA provides the means to interface between the IEEE 488 standard instrument bus and the F6800. The 488 instrument bus provides a means for controlling and moving data from complex systems of multiple instruments.

The F68488 will automatically handle all handshake protocol needed on the instrument bus.

- SINGLE OR DUAL PRIMARY ADDRESS RECOGNITION
- SECONDARY ADDRESS CAPABILITY
- COMPLETE SOURCE AND ACCEPTOR HANDSHAKES
- PROGRAMMABLE INTERRUPTS
- RFD HOLD-OFF TO PREVENT DATA OVERRUN
- OPERATES WITH DMA CONTROLLER
- SERIAL AND PARALLEL POLLING CAPABILITY
- TALK-ONLY OR LISTEN-ONLY CAPABILITY
- SELECTABLE AUTOMATIC FEATURES TO MINIMIZE SOFTWARE
- SYNCHRONIZATION TRIGGER OUTPUT
- F6800 BUS COMPATIBLE



F68488 GPIA INTERFACE

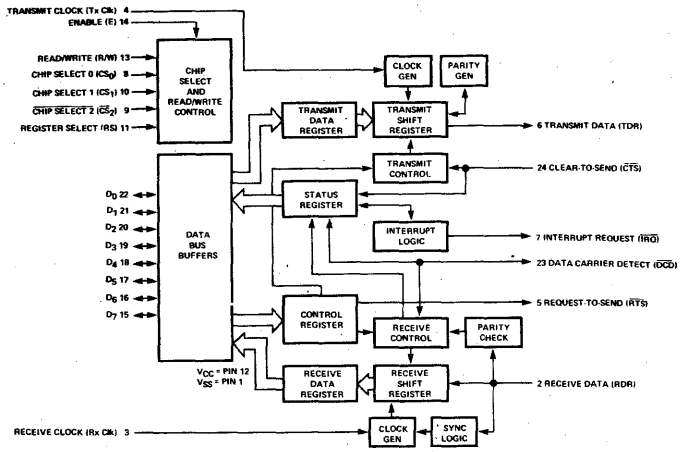
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F6850 ASYNCHRONOUS COMMUNICATIONS INTERFACE ADAPTOR (ACIA)

GENERAL DESCRIPTION – The F6850 Asynchronous Communications Interface Adapter (ACIA) provides the data formatting and control to interface serial asynchronous data communications information to bus organized systems such as the F6800 Microprocessing Unit.

The bus interface of the F6850 includes select, enable, read/write, interrupt and bus interface logic to allow data transfer over an 8-bit bi-directional data bus. The parallel data of the bus system is serially transmitted and received by the asynchronous data interface, with proper formatting and error checking. The functional configuration of the ACIA is programmed via the data bus during system initialization. A programmable Control Register provides variable word lengths, clock division ratios, transmit control, receive control, and interrupt control. For peripheral or modem operation, three control lines are provided. These lines allow the ACIA to interface directly with the F6860 0-600 bps digital modem.

- 8 AND 9-BIT TRANSMISSION
- OPTIONAL EVEN AND ODD PARITY
- PARITY, OVERRUN AND FRAMING ERROR CHECKING
- PROGRAMMABLE CONTROL REGISTER
- OPTIONAL ÷1, ÷16, AND ÷64 CLOCK MODES
- UP TO 500 kbps TRANSMISSION
- FALSE-START BIT DELETION
- PERIPHERAL/MODEM CONTROL FUNCTIONS
- DOUBLE BUFFERED
- ONE OR TWO STOP BIT OPERATION



F6850 ACIA

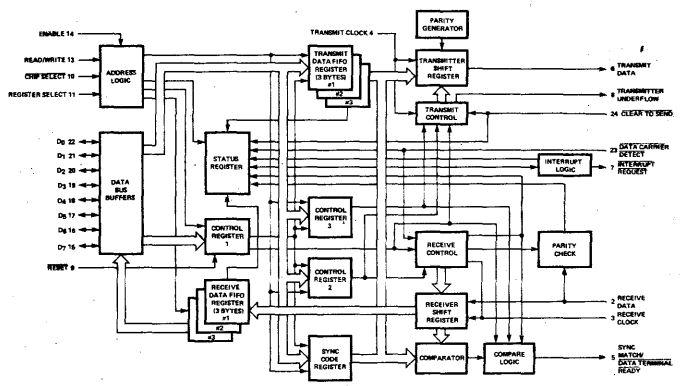
F6852 SYNCHRONOUS SERIAL DATA ADAPTOR (SSDA)

GENERAL DESCRIPTION – The F6852 Synchronous Serial Data Adapter provides a bi-directional serial interface for synchronous data information interchange. It contains interface logic for simultaneously transmitting and receiving standard synchronous communications characters in bus organized systems such as the F6800 Microprocessor systems.

The bus interface of the F6852 includes Select, Enable, Read/Write, Interrupt, and bus interface logic to allow data transfer over an 8-bit bi-directional data bus. The parallel data of the bus system is serially transmitted and received by the synchronous data interface with synchronization, fill character insertion/deletion, and error checking. The functional configuration of the SSDA is programmed via the data bus during system initialization. Programmable control registers provide control for variable word lengths, transmit control, receive control, synchronization control, and interrupt control. Status, timing and control lines provide peripheral or modem control.

Typical applications include floppy disk controllers, cassette or cartridge tape controllers, data communications terminals, and numerical control systems.

- PROGRAMMABLE INTERRUPTS FROM TRANSMITTER, RECEIVER, AND ERROR DETECTION LOGIC
- CHARACTER SYNCHRONIZATION ON ONE OR TWO SYNC CODES
- EXTERNAL SYNCHRONIZATION AVAILABLE FOR PARALLEL-SERIAL OPERATION
- PROGRAMMABLE SYNC CODE REGISTER
- UP TO 600 KBPS TRANSMISSION
- PERIPHERAL/MODEM CONTROL FUNCTIONS
- THREE BYTES OF FIFO BUFFERING ON BOTH TRANSMIT AND RECEIVE
- SEVEN, EIGHT, OR NINE BIT TRANSMISSION
- OPTIONAL EVEN AND ODD PARITY
- PARITY, OVERRUN, AND UNDERFLOW STATUS



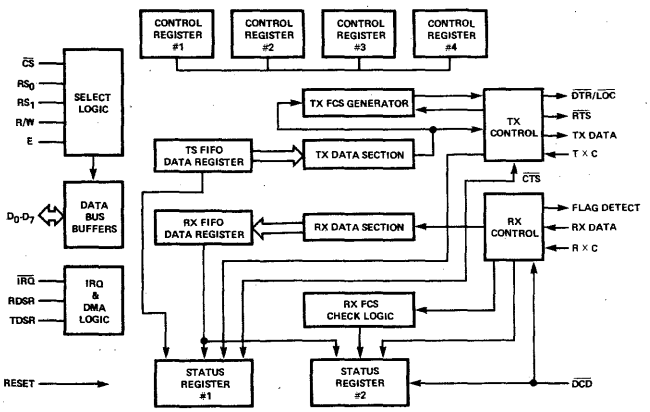
VCC = Pin 12
VSS = Pin 1

F6852 SSDA

F6854 ADVANCED DATA LINE CONTROLLER (ADLC)

GENERAL DESCRIPTION—The F6854/F68A54 ADLC perform the complex MPU/data communication link function for the Advanced Data Communication Control Procedure (ADCCP), High Level Data Link Control (HDLC) and Synchronous Data Link Control (SDLC) standards. The ADLC provides key interface requirements with improved software efficiency. The ADLC is designed to provide the data communications interface for both primary and secondary stations in stand alone, polling and loop configurations.

- F6800 COMPATIBLE
- PROTOCOL FEATURES
  - AUTOMATIC FLAG DETECTION AND SYNCHRONIZATION
  - ZERO INSERTION AND DELETION
  - AUTOMATIC ADDRESS FIELD EXTENSION (OPTIONAL)
  - EXTENDED CONTROL FIELD (OPTIONAL)
  - AUTO EXTENDABLE LOGIC CONTROL FIELD (OPTIONAL)
  - VARIABLE WORD LENGTH INFO FIELD—5, 6, 7, OR 8-BIT
  - AUTOMATIC FRAME CHECK SEQUENCE GENERATION AND CHECK
  - ABORT DETECTION AND TRANSMISSION
  - IDLE DETECTION AND TRANSMISSION
- MODEM/DATA CHANNEL CONTROL LINES
- LOOP MODE
- SINGLE 5 V POWER SUPPLY
- ENHANCED SPEED OPTION—F68A54

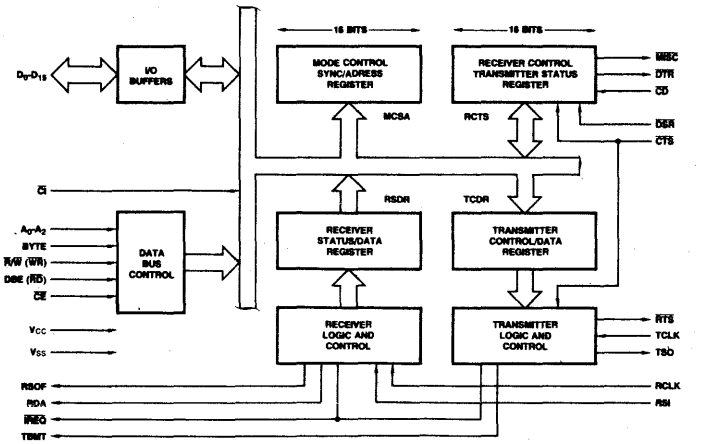


F6854 ADLC

F6856 SYNCHRONOUS PROTOCOL COMMUNICATIONS CONTROLLER (SPCC)

DESCRIPTION — The F3846/F6856 Synchronous Protocol Communications Controller (SPCC) is a monolithic n-channel MOS-LSI circuit designed to satisfy the major interface requirements for Bit Oriented (BOP) and Byte Control Protocols (BCP). The SPCC converts parallel data from the CPU to a continuous serial data stream for transmission. Simultaneously, it converts received serial data to parallel data for the CPU. The SPCC is organized to interface with either an 8 or 16-bit bi-directional data bus, is fully TTL compatible and operates from a single +5 V suppyl.

- F6800 AND 8080 BUS COMPATIBLE
- DC TO 1M BPS DATA RATE
- LINE CONTROL PROTOCOLS
  - BIT ORIENTED PROTOCOLS (BOP): SDLC, ADCCP, HDLC
  - BYTE CONTROL PROTOCOLS (BCP): BISYNC, DDCMP AND OTHER BCP
- BIT ORIENTED PROTOCOLS
  - AUTOMATIC DETECTION AND GENERATION OF SPECIAL CONTROL SEQUENCES, i.e., FLAG, ABORT, GO-AHEAD
  - ZERO INSERTION AND DELETION
  - PRIMARY OR SECONDARY STATION SELECT
  - GLOBAL ADDRESS
  - AUTOMATIC EXTENDED ADDRESS
  - ONE OR TWO CONTROL BYTES
  - DATA CHARACTER LENGTH OF 5 TO 8-BITS WITH 1 TO 8-BIT RESIDUAL LAST CHARACTER
  - CCITT-CRC ERROR DETECTION
  - IBM RETAIL STORE LOOP MODE
- BYTE CONTROL PROTOCOL – BISYNC
  - SPECIAL CHARACTER GENERATION: DLE, SYNC
  - SPECIAL CHARACTER DETECTION: DLE, SYNC, SOH, STX, ITB, ETB, ETX
  - USASCII OR EBCDIC
  - NON-TRANSPARENT MODE AND TRANSPARENT MODE
  - 8-BIT CHARACTER LENGTH
  - AUTOMATIC FILL CHARACTER INSERTION WITH SELECTABLE STRIPPING
  - CCITT OR CRC-16 ERROR DETECTION
- BYTE CONTROL PROTOCOLS – DDCMP AND OTHER
  - PROGRAMMABLE SYNC CHARACTERS
  - 5 TO 8-BIT CHARACTER LENGTH
  - SELECTABLE CRC ERROR DETECTION
  - AUTOMATIC FILL CHARACTER INSERTION WITH SELECTABLE STRIPPING
- DIRECTLY ADDRESSABLE PARAMETER CONTROL REGISTERS: MODE, SYNC/ADDRESS, TRANSMITTER CONTROL AND RECEIVER CONTROL
- SEPARATE ADDRESSABLE STATUS AND DATA REGISTERS FOR RECEIVER AND TRANSMITTER
- MODEM HANDSHAKE SIGNALS: $\overline{RTS}$, $\overline{CTS}$, DTR, $\overline{DSR}$ AND CARRIER DETECT ($\overline{CD}$)
- NRZ OR NRZI (ZERO COMPLIMENTING)
- FULL OR HALF DUPLEX OPERATION
- SELF TEST LOOP MODE
- 8 OR 16-BIT BI-DIRECTIONAL 3-STATE DATA BUS
- TTL COMPATIBLE
- SINGLE +5 V SUPPLY
- 40-PIN PACKAGE



F6856 SPCC

F3843 UNIVERSAL SYNCHRONOUS ASYNCHRONOUS RECEIVER TRANSMITTER (USART)

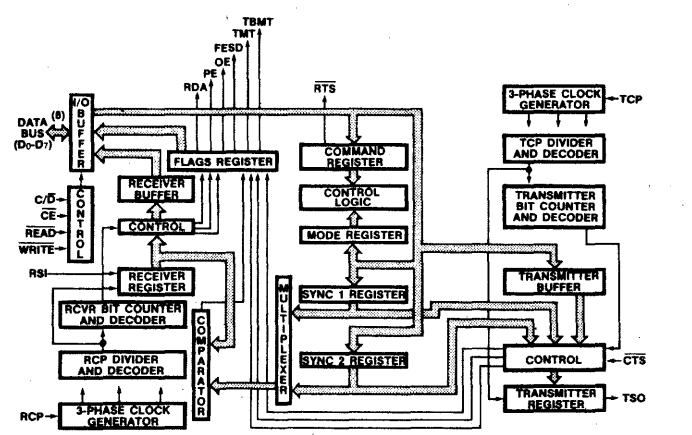
GENERAL DESCRIPTION—The F3843 is a programmable, full duplex Universal Synchronous or Asynchronous Receiver and Transmitter (USART) designed for use in data communications systems. This device provides the interface between the bus-oriented format of the controller and the serial format of the peripheral unit. The programming inputs of the USART determine the transmission mode, character length, framing format, parity mode and baud rate.

The F3843 is manufactured with the n-channel Isoplanar silicon gate process, and is available in both plastic and ceramic 28-pin dual in-line packages as well as in commercial and military temperature ranges.

- 5, 6, 7, or 8-BIT SELECTABLE CHARACTER LENGTH
- ODD OR EVEN PARITY GENERATION AND CHECKING
- SELECTED NUMBER OF STOP BITS (1, 1 1/2, 2) IN ASYNCHRONOUS MODE
- SEPARATE RECEIVER AND TRANSMITTER CLOCKS
- SELECTABLE CLOCK RATES (16x, 32x, or 64x BAUD RATES)
- STATIC OPERATION—NO MINIMUM FREQUENCY
- MAXIMUM BAUD RATES: (3843-1DC)

  1x CLOCK (SYNC MODE) - 320K BAUD
  16x CLOCK (ASYNC MODE) - 20K BAUD
  32x CLOCK (ASYNC MODE) - 10K BAUD
  64x CLOCK (ASYNC MODE) - 5K BAUD

- ERROR FLAGS: OVERRUN, PARITY, AND FRAMING ERRORS
- HARDWARE AND SOFTWARE STATUS FLAGS FOR BOTH RECEIVER AND TRANSMITTER STATUS
- DOUBLE BUFFERED, FULL DUPLEX OPERATION
- EXTERNAL OR INTERNAL (ONE OR TWO SYNC WORDS) SYNCHRONIZATION
- TTL COMPATIBLE INPUTS AND OUTPUTS
- 3-STATE DATA BUS WITH OR-TIE CAPABILITY



F3843 USART

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BIPOLAR MICROCOMPUTER PRODUCTS

The Fairchild line of bipolar microcomputer products includes the established 9400 4-Bit LSTTL/I^3L family and the F2900 4-Bit LSTTL family. These components, when used in microprogrammed controller/computer applications, offer the benefits of MSI/LSI and microprogramming.

The 9400 family consists of two sub-groups:

1. Devices produced for dedicated peripheral systems such as 9401/411 Cyclic Redundancy Checker/Generator and the 9403/9423 Serial-Parallel high speed FIFO.
2. Devices for microprogrammed controller applications Data Path Switch/ALRS and the I^3L 9408 Microprogram Sequencer.

4-BIT BIPOLAR MICROPROCESSOR FAMILY

LSI PERIPHERAL LOGIC ELEMENTS

Item	DEVICE NO.	Functional Description	Power Supply V	Maximum Frequency MHz (Typ)	Power mW (Typ)	Logic/ Connection Diagram	Package(s)
1	**9401/9411**	16-Bit Cyclic Redundancy Generator/Checker	5.0	18	350	P26	7A,9A
2	**9403**	16x4-Bit Serial/Parallel FIFO Buffer Memory	5.0	10	575	P27	6Q,9U
3	**9423**	64x4-Bit Serial/Parallel FIFO Buffer Memory	5.0	8.0	750	P27	6Q,9U

BIT SLICE MICROPROCESSORS

Item	DEVICE NO.	Functional Description	Power Supply V	Maximum Frequency MHz (Typ)	Power mW (Typ)	Logic/ Connection Diagram	Package(s)
4	**9404**	Data Path Switch	5.0	10	300	P28	6Q,9U
5	**9405A**	4-Bit Arithmetic Logic Register Stack (CPU slice with 8 Registers)	5.0	13	550	P29	6Q,9U
6	**9406**	16x4 push-down pop-up Program Stack	5.0	10	500	P30	6Q,9U
7	**9407**	Data Access Register (PC, SP and operand pointer)	5.0	10	450	P31	6Q,9U
8	**9408**	10-Bit Microprogram Sequencer/Controller (pipeline capability)	5.0	7.0	650	P32	6I,8P
9	**9408A**	10-Bit Microprogram Sequencer/Controller (pipeline capability)	5.0	10	650	P32	6I,8P
10	**9410**	Register Stack (16x4 RAM with output latch)	5.0	25	375	P33	7D,9M
11	**F2901A/ 9409**	4-Bit CPU Slice, (16 Registers)	5.0	10	800	P47	6I,8P

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9401

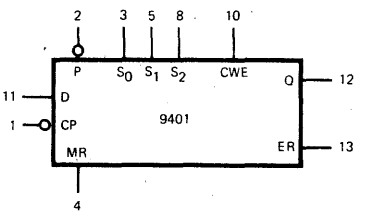
CRC GENERATOR/CHECKER

FAIRCHILD TTL MACROLOGIC

DESCRIPTION - The 9401 Cycle Redundancy Check (CRC) Generator/Checker provides an advanced tool for implementing the most widely used error detection scheme in serial digital data handling systems. A 3-bit control input selects one-of-eight generator polynomials. The list of polynomials includes CRC-16 and CRC-CCITT as well as their reciprocals (reverse polynomials). Automatic right justification is incorporated for polynomials of degree less than 16. Separate clear and preset inputs are provided for floppy disc and other applications. The Error output indicates whether or not a transmission error has occurred. Another control input inhibits feedback during check word transmission. The 9401 is fully compatible with all TTL families.

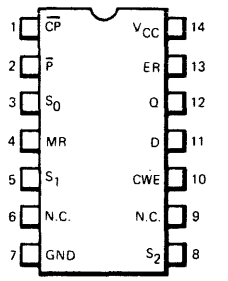
- **GUARANTEED 10 MHz DATA RATE**
- **EIGHT SELECTABLE POLYNOMIALS**
- **ERROR INDICATOR**
- **SEPARATE PRESET AND CLEAR CONTROLS**
- **AUTOMATIC RIGHT JUSTIFICATION**
- **FULLY COMPATIBLE WITH ALL TTL LOGIC FAMILIES**
- **14-PIN PACKAGE**
- **TYPICAL APPLICATIONS:**
  - **FLOPPY AND OTHER DISC STORAGE SYSTEMS**
  - **DIGITAL CASSETTE AND CARTRIDGE SYSTEMS**
  - **DATA COMMUNICATION SYSTEMS**

LOGIC SYMBOL



V_{CC} = Pin 14
GND = Pin 7

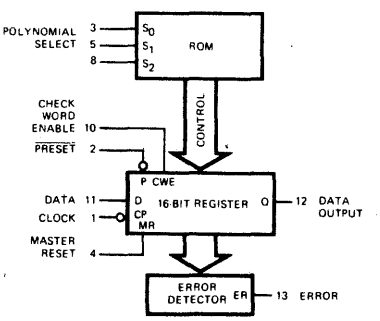
CONNECTION DIAGRAM
DIP (TOP VIEW)



Pins 6 and 9 not connected.

NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package.

BLOCK DIAGRAM



V_{CC} = Pin 14
GND = Pin 7

PIN NAMES

		LOADING (Note a)	
		HIGH	LOW
$S_0 - S_2$	Polynomial Select Inputs	1.0 U.L.	0.23 U.L.
$\overline{D}$	Data Input	1.0 U.L.	0.23 U.L.
$\overline{CP}$	Clock (Operates on HIGH-to-LOW Transition) Input	1.0 U.L.	0.23 U.L.
$\overline{CWE}$	Check Word Enable Input	1.0 U.L.	0.23 U.L.
$\overline{P}$	Preset (Active LOW) Input	1.0 U.L.	0.23 U.L.
MR	Master Reset (Active HIGH) Input	1.0 U.L.	0.23 U.L.
Q	Data Output (Note b)	10 U.L.	5 U.L.
ER	Error Output (Note b)	10 U.L.	5 U.L.

NOTES:
a. 1 TTL Unit Load (U.L.) = 40 μA HIGH/1.6 mA LOW.
b. The output LOW drive factor is 2.5 U.L. for Military (XM) and 5 U.L. for Commercial (XC) Temperature Ranges.

FAIRCHILD

464 ELLIS STREET, MOUNTAIN VIEW, CALIFORNIA 94042 (415) 962-5011/TWX 910-379-6435

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Manufactured under one or more of the following U.S. Patents: 2981877, 3015048, 3025589, 3064167, 3108359, 3117260; other patents pending.

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FUNCTIONAL DESCRIPTION – The 9401 is a 16-bit programmable device which operates on serial data streams and provides a means of detecting transmission errors. Cyclic encoding and decoding schemes for error detection are based on polynomial manipulation in modulo arithmetic. For encoding, the data stream (message polynomial) is divided by a selected polynomial. This division results in a remainder which is appended to the message as check bits. For error checking, the bit stream containing both data and check bits is divided by the same selected polynomial. If there are no detectable errors, this division results in a zero remainder. Although it is possible to choose many generating polynomials of a given degree, standards exist that specify a small number of useful polynomials. The 9401 implements the polynomials listed in *Table 1* by applying the appropriate logic levels to the select pins S_0, S_1 and S_2.

The 9401 consists of a 16-bit register, a Read Only Memory (ROM) and associated control circuitry as shown in the block diagram. The polynomial control code presented at inputs S_0, S_1 and S_2 is decoded by the ROM, selecting the desired polynomial by establishing shift mode operation on the register with Exclusive OR gates at appropriate inputs. To generate the check bits, the data stream is entered via the Data inputs (D), using the HIGH-to-LOW transition of the Clock input ($\overline{CP}$). This data is gated with the most significant output (Q) of the register, and controls the Exclusive OR gates *(Figure 1)*. The Check Word Enable (CWE) must be held HIGH while the data is being entered. After the last data bit is entered, the CWE is brought LOW and the check bits are shifted out of the register and appended to the data bits using external gating *(Figure 2)*.

To check an incoming message for errors, both the data and check bits are entered through the D input with the CWE input held HIGH. The 9401 is not in the data path, but only monitors the message. The Error Output becomes valid after the last check bit has been entered into the 9401 by a HIGH-to-LOW transition of $\overline{CP}$. If no detectable errors have occurred during the data transmission, the resultant internal register bits are all LOW and the Error Output (ER) is LOW. If a detectable error has occurred, ER is HIGH.

A HIGH on the Master Reset input (MR) asynchronously clears the register. A LOW on the Preset input ($\overline{P}$) asynchronously sets the entire register if the control code inputs specify a 16-bit polynomial; in the case of 12 or 8-bit check polynomials only the most significant 12 or 8 register bits are set and the remaining bits are cleared.

TABLE 1

SELECT CODE			POLYNOMIAL	REMARKS
S_2	S_1	S_0		
L	L	L	$X^{16}+X^{15}+X^2+1$	CRC-16
L	L	H	$X^{16}+X^{14}+X+1$	CRC-16 REVERSE
L	H	L	$X^{16}+X^{15}+X^{13}+X^7+X^4+X^2+X^1+1$	
L	H	H	$X^{12}+X^{11}+X^3+X^2+X+1$	CRC-12
H	L	L	$X^8+X^7+X^5+X^4+X+1$	
H	L	H	X^8+1	LRC-8
H	H	L	$X^{16}+X^{12}+X^5+1$	CRC-CCITT
H	H	H	$X^{16}+X^{11}+X^4+1$	CRC-CCITT REVERSE

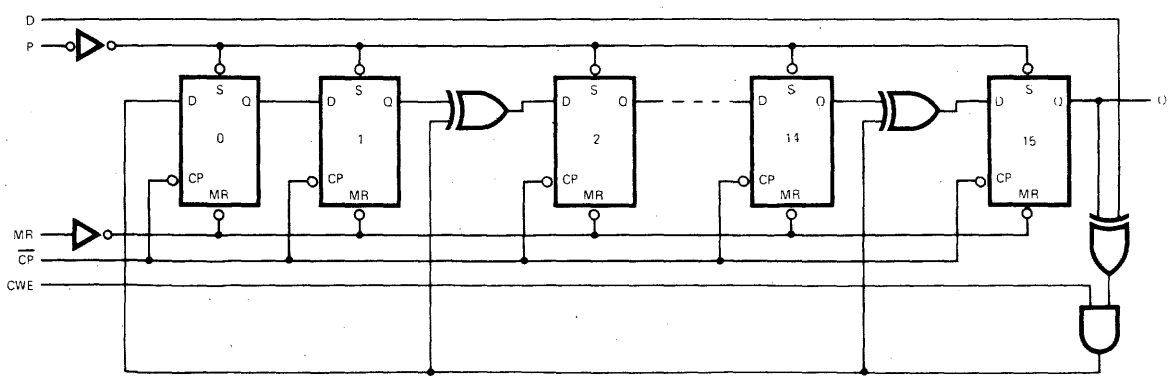


Fig. 1
EQUIVALENT CIRCUIT FOR $X^{16}+X^{15}+X^2+1$

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9403/9423

FIRST-IN FIRST-OUT (FIFO) BUFFER MEMORY

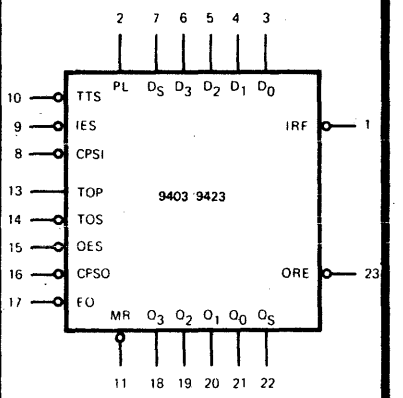
FAIRCHILD TTL MACROLOGIC

DESCRIPTION - The 9403/9423 is an expandable fall-through type high-speed First-In First-Out (FIFO) Buffer Memory optimized for high speed disc or tape controllers and communication buffer applications. It is organized as 16 or 64 words by four bits and may be expanded to any number of words or any number of bits (in multiples of four). Data may be entered or extracted asynchronously in serial or parallel, allowing economical implementation of buffer memories.

The 9403/9423 has 3-state outputs which provide added versatility and is fully compatible with all TTL families.

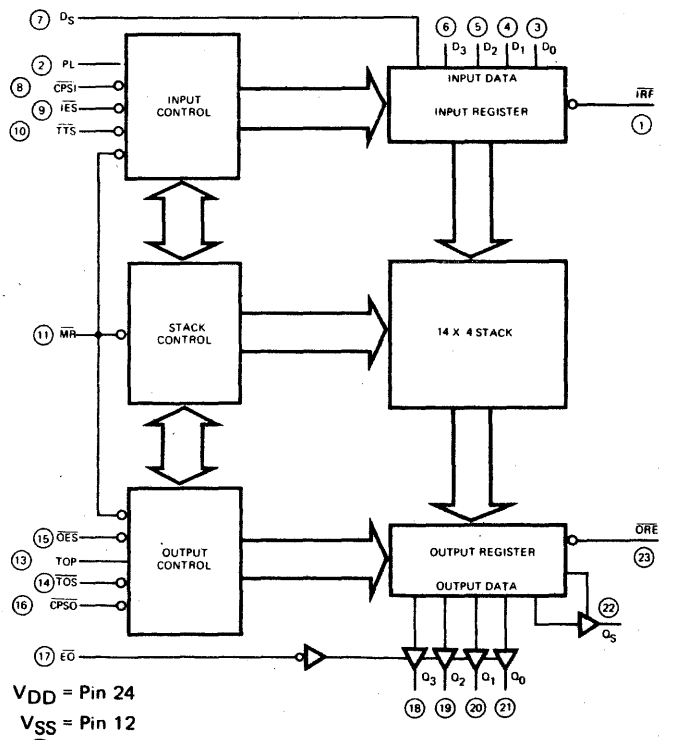
- 10 MHz SERIAL OR PARALLEL DATA RATE
- SERIAL OR PARALLEL INPUT
- SERIAL OR PARALLEL OUTPUT
- EXPANDABLE WITHOUT EXTERNAL LOGIC
- 3-STATE OUTPUTS
- FULLY COMPATIBLE WITH ALL TTL FAMILIES
- SLIM 24-PIN PACKAGE

LOGIC SYMBOL



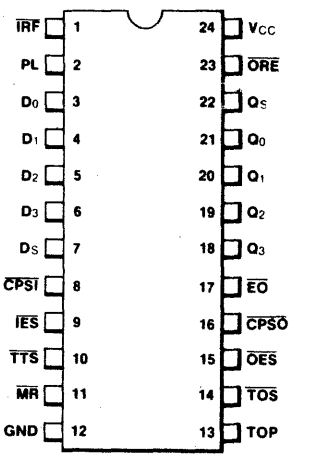
V_{CC} = Pin 24
GND = Pin 12

BLOCK DIAGRAM



V_{DD} = Pin 24
V_{SS} = Pin 12
◯ = Pin Numbers

CONNECTION DIAGRAM
DIP (TOP VIEW)



NOTE:
The Flatpak version has the same pinouts (Connection Diagram) as the Dual In-line Package.

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FAIRCHILD

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PIN NAMES

PIN NAME	DESCRIPTION	COMMENTS
$D_0 - D_3$	Parallel Data Inputs	
D_S	Serial Data Input	
PL	Parallel Load Input	HIGH on PL enables $D_0 - D_3$. Not edge triggered. Ones catching.
$\overline{CPSI}$	Serial Input Clock	Edge triggered. Activates on falling edge.
$\overline{IES}$	Serial Input Enable	Enables serial and parallel input when LOW.
$\overline{TTS}$	Transfer to Stack Input	A LOW on this pin initiates fall through.
$\overline{OES}$	Serial Output Enable Input	Enables serial and parallel output when LOW.
$\overline{TOS}$	Transfer Out Serial Input	A LOW on this pin enables a word to be transferred from the stack to the output register. (TOP must be HIGH also for the transfer to occur). Not edge triggered.
TOP	Transfer Out Parallel Input	A HIGH on this pin enables a word to be transferred from the stack to the output register. ($\overline{TOS}$ must be LOW for the transfer to occur). Not edge triggered.
$\overline{MR}$	Master Reset	Active LOW.
$\overline{EO}$	Output Enable	Active LOW.
$\overline{CPSO}$	Serial Output Clock Input	Edge triggered. Activates on falling edge.
$Q_0 - Q_3$	Parallel Data Outputs	
Q_S	Serial Data Output	
$\overline{IRF}$	Input Register Full Output	LOW when input register is full (Note b).
$\overline{ORE}$	Output Register Empty Output	HIGH when output register contains valid data.

FUNCTIONAL DESCRIPTION - As shown in the block diagram the 9403/9423 consists of three sections:

1. An Input Register with parallel and serial data inputs as well as control inputs and outputs for input handshaking and expansion.
2. A 4-bit wide, 14 or 62 word deep fall-through stack with self-contained control logic.
3. An Output Register with parallel and serial data outputs as well as control inputs and outputs for output handshaking and expansion.

Since these three sections operate asynchronously and almost independently, they will be described separately below:

Input Register (Data Entry):
The Input Register can receive data in either bit-serial or in 4-bit parallel form. It stores this data until it is sent to the fall-through stack and generates the necessary status and control signals.

Figure 1 is a conceptual logic diagram of the input section. As described later, this 5-bit register is initialized by setting the F3 flip-flop and resetting the other flip-flops. The Q-output of the last flip-flop (FC) is brought out as the "Input Register Full" output ($\overline{IRF}$). After initialization this output is HIGH.

Parallel Entry - A HIGH on the PL input loads the $D_0 - D_3$ inputs into the $F_0 - F_3$ flip-flops and sets the FC flip-flop. This forces the $\overline{IRF}$ output LOW indicating that the input register is full. During parallel entry, the $\overline{CPSI}$ input must be LOW. If parallel expansion is not being implemented, $\overline{IES}$ must be LOW to establish row mastership (see Expansion section).

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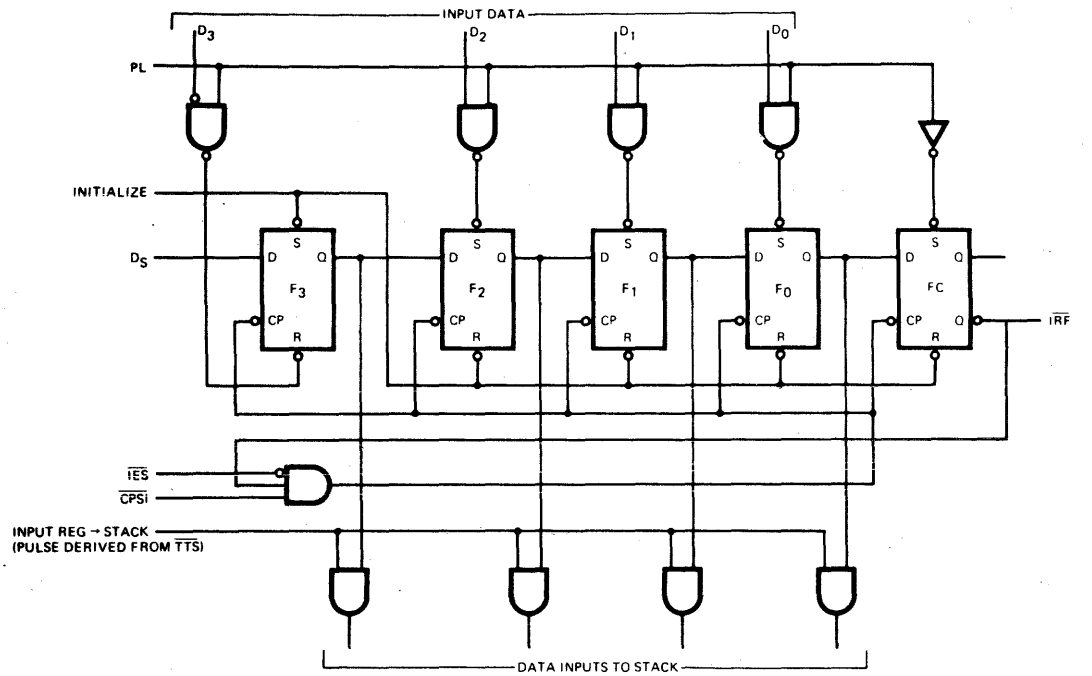


Fig. 1
CONCEPTUAL INPUT SECTION

Serial Entry - Data on the D_S input is serially entered into the F_3, F_2, F_1, F_0, FC shift register on each HIGH-to-LOW transition of the CPSI clock input, provided IES and PL are LOW.

After the fourth clock transition, the four data bits located in the four flip-flops F_0 - F_3. The FC flip-flop is set, forcing the $\overline{IRF}$ output LOW and internally inhibiting $\overline{CPSI}$ clock pulses from effecting the register. *Figure 2* illustrates the final positions in a 9403 resulting from a 64-bit serial bit train. B_0 is the first bit, B_{63} the last bit. Similar operation can be developed for 9423.

Transfer to the Stack -The outputs of Flip-Flops F_0 - F_3 feed the stack. A LOW level on the $\overline{TTS}$ input initiates a "fall-through" action. If the top location of the stack is empty, data is loaded into the stack and the input register is re-initialized. Note that this initialization is postponed until PL is LOW again. Thus, automatic FIFO action is achieved by connecting the $\overline{IRF}$ output to the $\overline{TTS}$ input.

An RS Flip-Flop (the Request Initialization Flip-Flop shown in *Figure 10*) in the control section records the fact that data has been transferred to the stack. This prevents multiple entry of the same word into the stack despite the fact the $\overline{IRF}$ and $\overline{TTS}$ may still be LOW. The Request Initialization Flip-Flop is not cleared until PL goes LOW. Once in the stack, data falls through the stack automatically, pausing only when it is necessary to wait for an empty next location. In the 9403, as in most modern FIFO designs, the $\overline{MR}$ input only initializes the stack control section and does not clear the data.

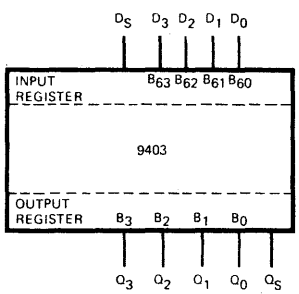


Fig. 2
FINAL POSITIONS IN A 9403 RESULTING FROM A 64-BIT SERIAL TRAIN

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Output Register (Data Extraction) – The Output Register receives 4-bit data words from the bottom stack location, stores it and outputs data on a 3-state 4-bit parallel data bus or on a 3-state serial data bus. The output section generates and receives the necessary status and control signals. *Figure 3* is a conceptual logic diagram of the output section.

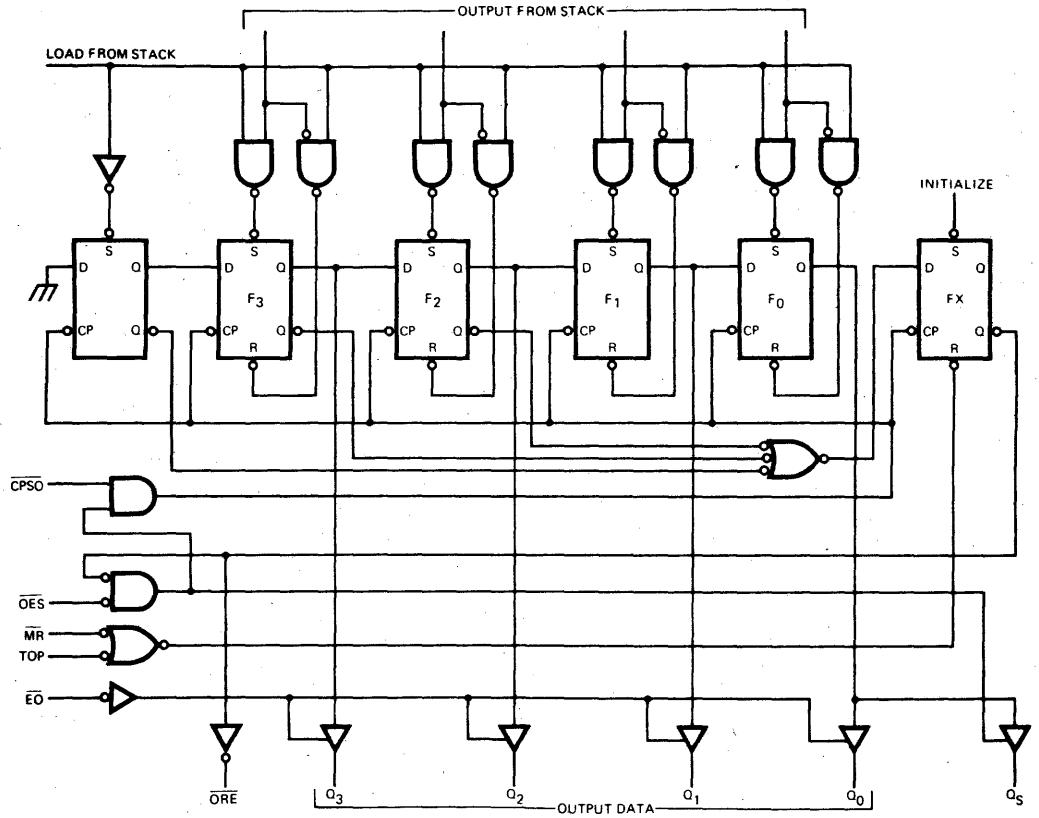


Fig. 3
CONCEPTUAL OUTPUT SECTION

Parallel Data Extraction – When the FIFO is empty after a LOW pulse is applied to $\overline{MR}$, the Output Register Empty ($\overline{ORE}$) output is LOW. After data has been entered into the FIFO and has fallen through to the bottom stack location, it is transferred into the Output Register provided the "Transfer Out Parallel" (TOP) input is HIGH. As a result of the data transfer $\overline{ORE}$ goes HIGH, indicating valid data on the data outputs (provided the 3-state buffer is enabled). TOP can now be used to clock out the next word. When TOP goes LOW, $\overline{ORE}$ will go LOW indicating that the output data has been extracted, but the data itself remains on the output bus until the next HIGH level at TOP permits the transfer of the next word (if available) into the Output Register. During parallel data extraction $\overline{CPSO}$ should be LOW. $\overline{TOS}$ should be grounded for single slice operation or connected to the appropriate $\overline{ORE}$ for expanded operation (see Expansion section).

TOP is not edge triggered. Therefore, if TOP goes HIGH before data is available from the stack, but data does become available before TOP goes LOW again, that data will be transferred into the Output Register. However, internal control circuitry prevents the same data from being transferred twice. If TOP goes HIGH and returns to LOW before data is available from the stack, ORE remains LOW indicating that there is no valid data at the outputs.

Serial Data Extraction – When the FIFO is empty after a LOW pulse is applied to $\overline{MR}$, the Output Register Empty ($\overline{ORE}$) output is LOW. After data has been entered into the FIFO and has fallen through to the bottom stack location, it is transferred into the Output Register provided $\overline{TOS}$ is LOW and TOP is HIGH. As a result of the data transfer $\overline{ORE}$ goes HIGH indicating valid data in the register. The 3-state Serial Data Output, Q_S, is automatically enabled and puts the first data bit on the output bus. Data is serially shifted out on the HIGH-to-LOW transition of $\overline{CPSO}$. To prevent false shifting, $\overline{CPSO}$ should be LOW when the new word is being loaded into the Output Register. The fourth transition empties the shift register, forces $\overline{ORE}$ output LOW and disables the serial output, Q_S (refer to *Figure 3*). For serial operation the $\overline{ORE}$ output may be tied to the $\overline{TOS}$ input, requesting a new word from the stack as soon as the previous one has been shifted out.

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Horizontal and Vertical Expansion - The 9403 and 9423 can be expanded in both the horizontal and vertical directions without any external parts and without sacrificing any of its FIFO's flexibility for serial/parallel input and output. The interconnections necessary to form a 31-word by 16-bit FIFO are shown in *Figure 4*. Using the same technique, any FIFO of (15m + 1) words by (4n) bits can be constructed, where m is the number of devices in a column and n is the number of devices in a row.

Figures 5 and *6* show the timing diagrams for serial data entry and extraction for the 31-word by 16-bit FIFO shown in *Figure 4*. The final position of data after serial insertion of 496 bits into the FIFO array of *Figure 4* is shown in *Figure 7*.

All applications shown for 9403 can be adapted to the 9423 with the depth of the stock being 64 locations rather than the 16 locations of 9403.

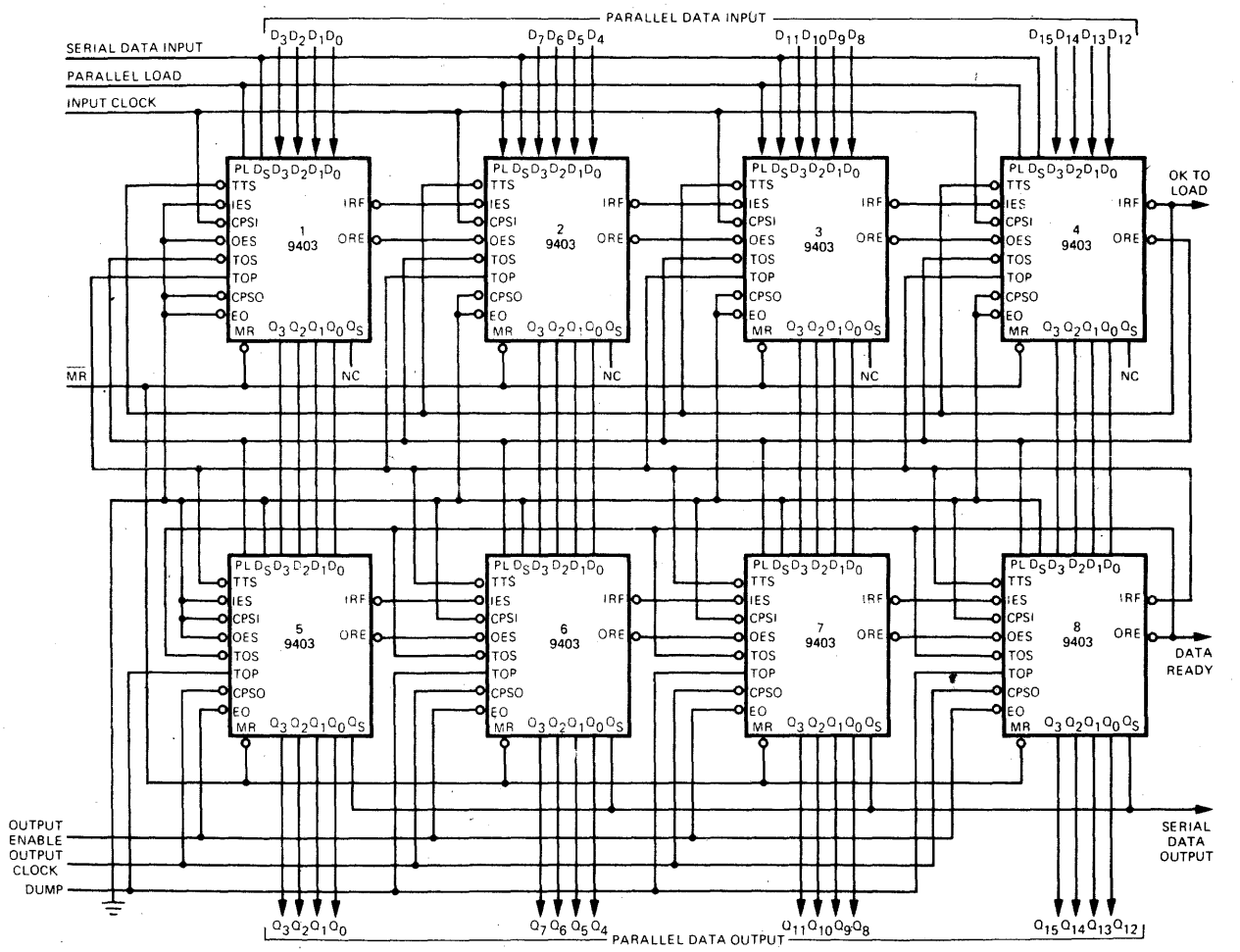


Fig. 4
A 31 X 16 FIFO ARRAY

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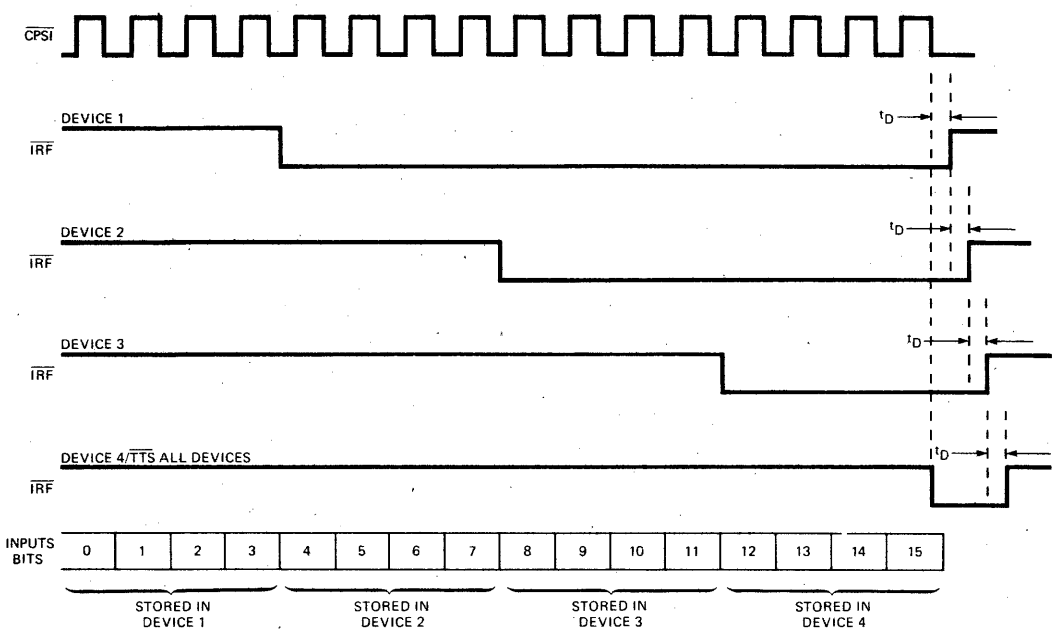


Fig. 5
SERIAL DATA ENTRY FOR ARRAY OF FIG. 6

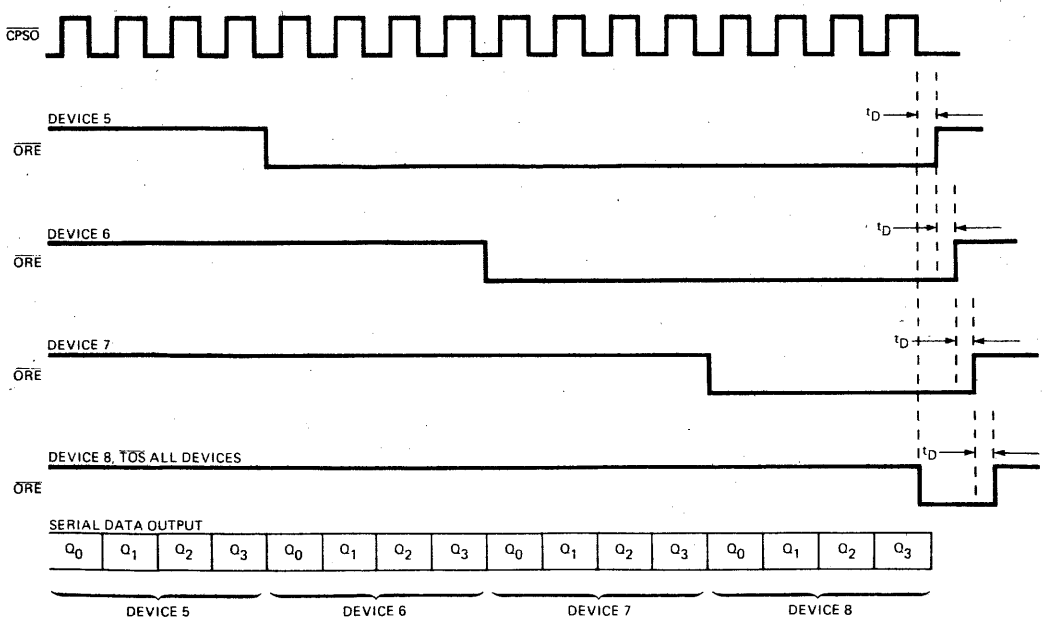


Fig. 6
SERIAL DATA EXTRACTION FOR ARRAY OF FIG. 6

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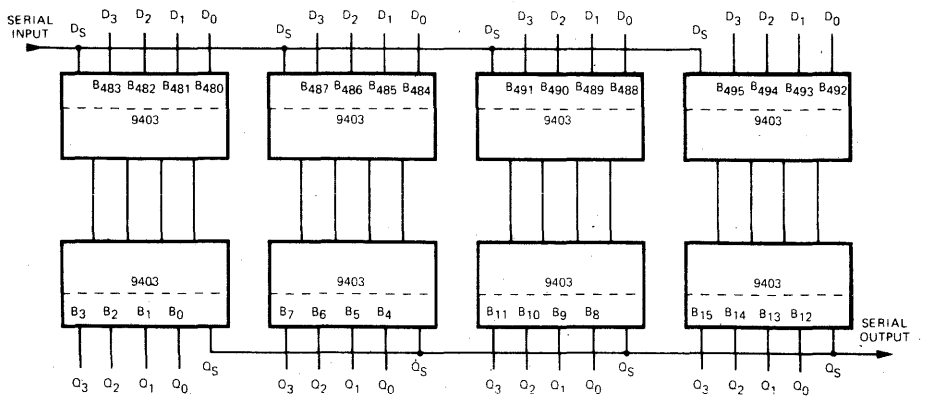


Fig. 7
FINAL POSITION OF A 496-BIT SERIAL INPUT

Interlocking Circuitry – Most conventional FIFO designs provide status signals analogous to $\overline{IRF}$ and $\overline{ORE}$. However, when these devices are operated in arrays, variations in unit to unit operating speed require external gating to assure all devices have completed an operation. The 9403 incorporates simple but effective "master/slave" interlocking circuitry to eliminate the need for external gating.

In the 9403 array of *Figure 4* devices 1 and 5 are defined as "row masters" and the other devices are slaves to the master in their row. No slave in a given row will initialize its Input Register until it has received LOW on its $\overline{IES}$ input from a row master or a slave of higher priority.

In a similar fashion, the $\overline{ORE}$ outputs of slaves will not go HIGH until their $\overline{OES}$ inputs have gone HIGH. This interlocking scheme ensures that new input data may be accepted by the array when the $\overline{IRF}$ output of the final slave in that row goes LOW and that output data for the array may be extracted when the $\overline{ORE}$ of the final slave in the output row goes HIGH.

The row master is established by connecting its $\overline{IES}$ input to ground while a slave receives its $\overline{IES}$ input from the $\overline{IRF}$ output of the next higher priority device. When an array of 9403 FIFOs is initialized with a LOW on the $\overline{MR}$ inputs of all devices, the $\overline{IRF}$ outputs of all devices will be HIGH. Thus, only the row master receives a LOW on the $\overline{IES}$ input during initialization. *Figure 8* is a conceptual logic diagram of the internal circuitry which determines master/slave operation. Whenever $\overline{MR}$ and $\overline{IES}$ are LOW, the Master Latch is set. Whenever $\overline{TTS}$ goes LOW the Request Initialization Flip-Flop will be set. If the Master Latch is HIGH, the Input Register will be immediately initialized and the Request Initialization Flip-Flop reset. If the Master Latch is reset, the Input Register is not initialized until $\overline{IES}$ goes LOW. In array operation, activating the $\overline{TTS}$ initiates a ripple input register initialization from the row master to the last slave.

A similar operation takes place for the output register. Either a $\overline{TOS}$ or TOP input initiates a load-from-stack operation and sets the ORE Request Flip-Flop. If the Master Latch is set, the last Output Register Flip-Flop is set and $\overline{ORE}$ goes HIGH. If the Master Latch is reset, the $\overline{ORE}$ output will be LOW until an $\overline{OES}$ input is received.

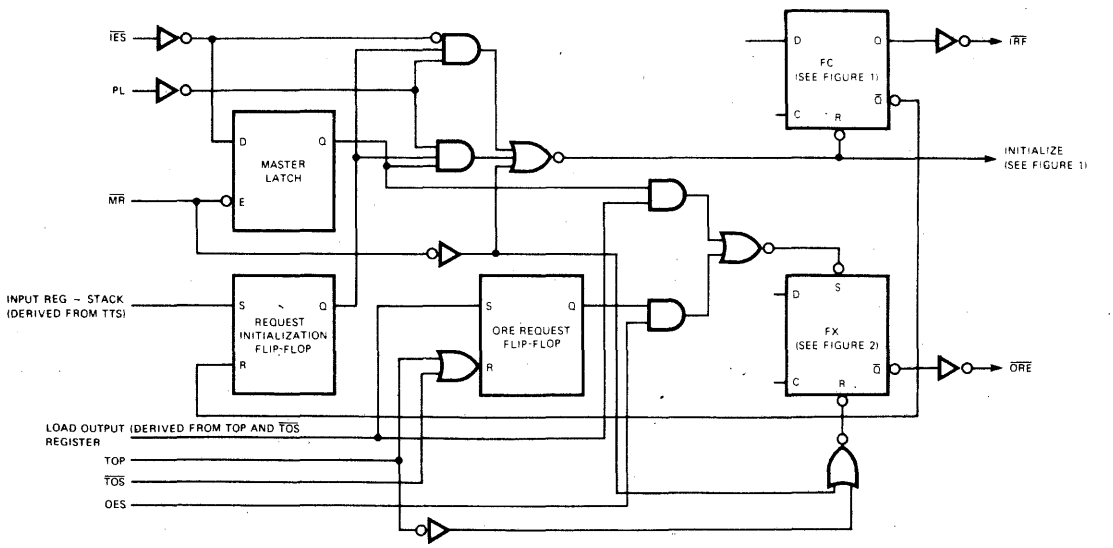


Fig. 8
CONCEPTUAL DIAGRAM, INTERLOCKING CIRCUITRY

Fairchild cannot assume responsibility for use of any circuitry described other than circuitry entirely embodied in a Fairchild product. No other circuit patent licenses are implied.

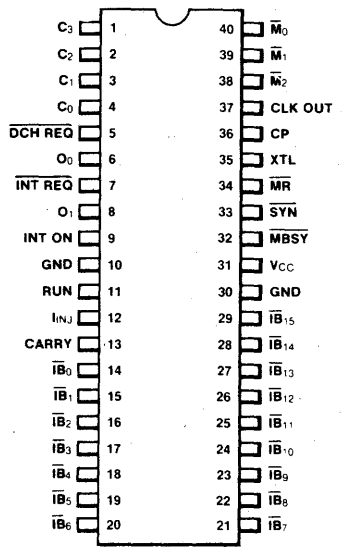
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9440 MICROFLAME™
16-BIT BIPOLAR MICROPROCESSOR

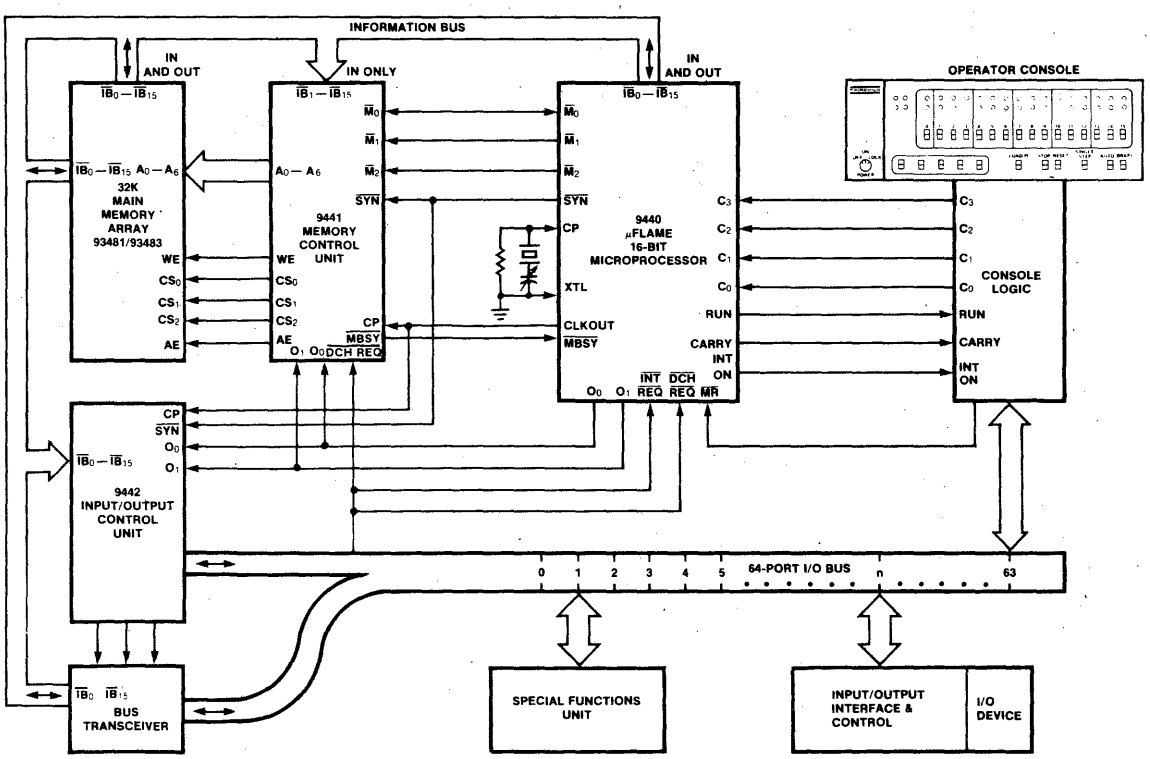
GENERAL DESCRIPTION — The 9440 MICROFLAME single-chip 16-bit bipolar processor, packaged in a 40-pin DIP, is implemented using Fairchild's Isoplanar Integrated Injection Logic technology (I^3L™). Though structurally different from the CPUs of the Data General NOVA line of minicomputers, the 9440 offers comparable performance and executes the same instruction set.

- **EIGHT 16-BIT ON-CHIP REGISTERS**
- **64 DIRECTLY ADDRESSABLE I/O DEVICES, EACH WITH THREE BIDIRECTIONAL I/O PORTS**
- **PRIORITY INTERRUPT HANDLING WITH UP TO 16 PRIORITY LEVELS**
- **FAST DIRECT MEMORY ACCESS AT MEMORY SPEEDS**
- **16-BIT 3-STATE BIDIRECTIONAL INFORMATION BUS**
- **FLEXIBLE OPERATOR CONSOLE CONTROL USING ONLY FOUR LINES**
- **POWERFUL, WIDELY USED INSTRUCTION SET**
- **MULTIFUNCTION INSTRUCTIONS FOR EFFICIENT MEMORY USAGE**
- **FOUR CLASSES OF INSTRUCTIONS; TOTAL OF 2192 DIFFERENT INSTRUCTIONS**
- **EIGHT ADDRESSING MODES, 32K 16-BIT WORDS (64K BYTES) ADDRESSING RANGE**
- **5 V POWER SUPPLY**
- **TTL INPUTS AND OUTPUTS**
- **TYPICAL 1 W POWER DISSIPATION**
- **FULL MILITARY TEMPERATURE RANGE VERSION**
- **SINGLE-CLOCK STATIC OPERATION, ON-CHIP OSCILLATOR, DC TO 12 MHz CLOCK RATE**
- **COMPATIBLE HIGH SPEED MEMORIES AVAILABLE (93481/93483)**
- **TOTAL SOFTWARE WITH FIRE™ SOFTWARE PACKAGE**

CONNECTION DIAGRAM
DIP (TOP VIEW)



SYSTEM DIAGRAM



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Fairchild MICROPROCESSOR

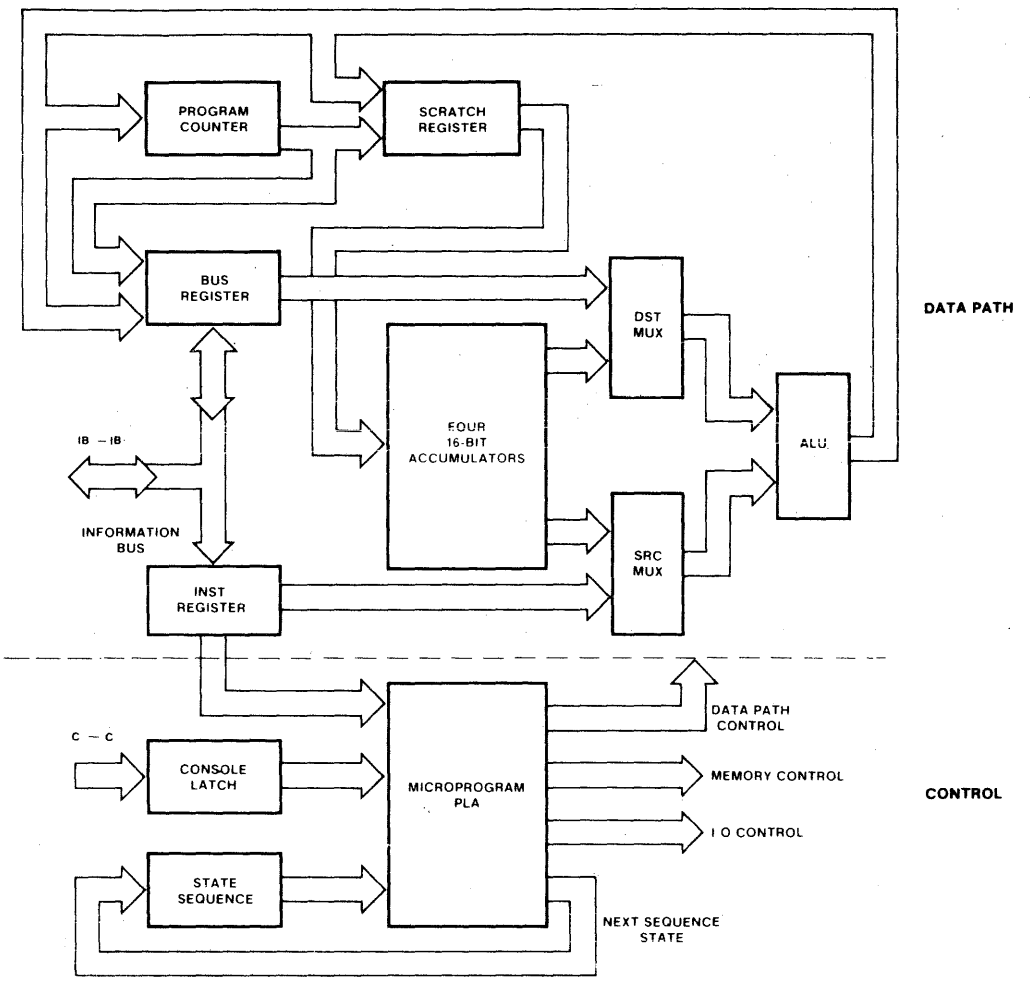


Fig. 1 9440 MICROFLAME CPU Block Diagram

9440 ARCHITECTURE *(Figure 1)*
The 9440 single-chip 16-bit bipolar processor, packaged in a 40-pin DIP, is implemented using Fairchild's Isoplanar Integrated Injection Logic technology (I3L.™). Though structurally different from the CPUs of the NOVA line of minicomputers, the 9440, as a microprocessor, offers comparable performance and executes the same instruction set.

The processor is a stored program machine using homogeneous external memory, i.e., instructions and data are stored in the same memory. Although the processor handles 16 bits of information, only 15 bits are used for addressing the memory. Thus, the intrinsic memory capacity of a 9440 system is 32,768 16-bit words.

The 9440 consists of a collection of data paths and all the necessary control circuitry. It governs peripheral I/O equipment, performs the arithmetic, logic and data handling operations and sequences the program.

Data Paths — The data path portion includes a bank of four 16-bit general-purpose registers (accumulators AC0 - AC3), two multiplexers, an ALU, and four 16-bit special registers — scratch register, bus register, instruction register and program counter. Internal data flows between the various registers via 4-bit-wide data paths.

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The accumulators store the operands required for all arithmetic/logic operations. Accumulators AC2 and AC3 are also used as index registers and AC3 serves as the subroutine linkage register as well. All input-output data transfers take place through the accumulators; however, a word in a memory location may be incremented or decremented without accumulator participation. Data can be moved in either direction between the memory and any accumulator.

The destination and source multiplexers are connected to all four accumulators and select source and destination registers for each operation. The multiplexers also receive other inputs from the bus and instruction registers, which permit the ALU to be used for effective-address calculations and other purposes.

The ALU is four bits wide and operates on two 16-bit words in four consecutive steps, taking one 4-bit nibble per step. By adding the associated Carry bit to the 16-bit result from the ALU, a 17-bit word is formed which may be rotated either left or right.

Data from the ALU to the destination accumulator is held in the scratch register for one cycle. The bus register is connected to the bidirectional information bus and can either supply or receive 16 bits of data in parallel. The instruction register is loaded with 16 bits in parallel, directly from the information bus during an instruction-fetch operation. The 15-bit program counter determines the sequence in which instructions are executed. It is incremented to take instructions from consecutive locations and the instruction sequence can be altered at any time by changing the PC contents (jump-class instruction) or by incrementing PC twice (skip-class instruction).

Control — Control signals are supplied to the data path by the internal mask-programmed logic arrray (PLA). For each of 72 different data-path operations, there is a 24-bit output word in the PLA selected according to the combination of 19 input lines. These are defined in *Figure 2*.

The 9440 operates with an on-chip oscillator when a crystal is tied between CP and XTL or it can be driven by an external oscillator via the CP input. The on-chip clock logic circuit generates the internal clock signal, a synchronization signal ($\overline{SYN}$), and several other timing pulses.

A macro-instruction in the 9440 consists of several microcycles, each with a corresponding one-of-16 sequence-control state. Each microcycle consists of several phases, or nanocycles, four of which are devoted to controlling the data-path circuitry. During each of these phases, the data path circuitry operates on a 4-bit nibble out of the 16 bits of the operands and clocks its various registers at half the oscillator rate. Another phase provides the time delay required for a new output word of the PLA to become valid after the PLA inputs are changed.

The bus register and the instruction register are loaded from the information bus at different times during the execution cycle.

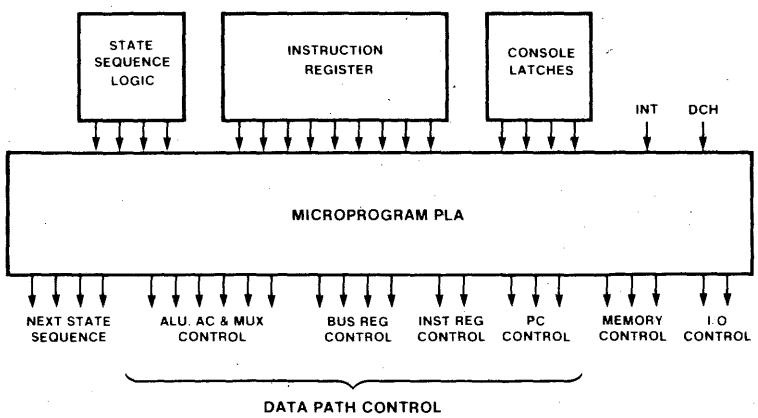


Fig. 2 Programmed Logic Array

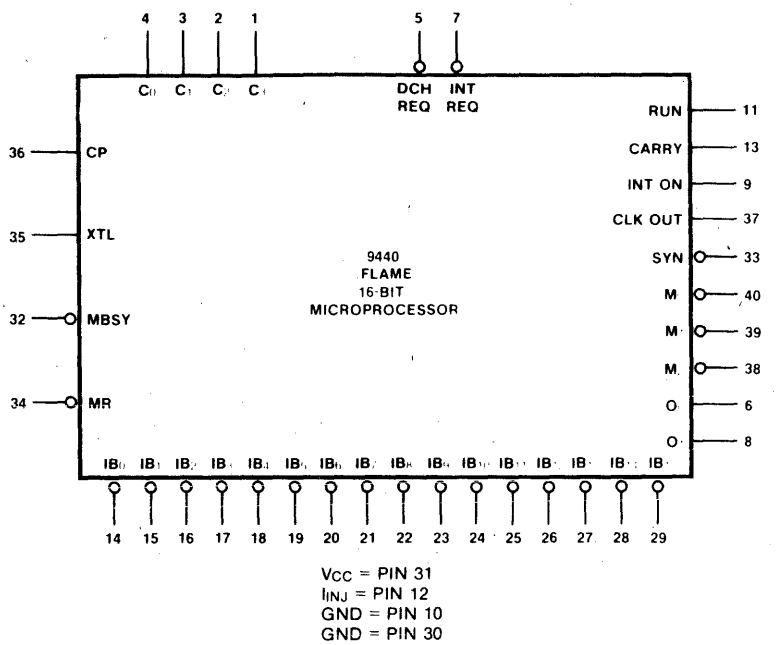


Fig. 3 Logic Symbol

9440 SIGNAL DESCRIPTIONS *(Figure 3)*

Information Bus — $\overline{IB}_0$-$\overline{IB}_{15}$ (Inputs/Outputs) — The 16-bit bidirectional 3-state information bus is used to transfer address, data and instruction information between the processor and main memory, and to transfer data and control information to and from I/O devices. A LOW level defines a binary '1'.

Status Lines — RUN, CARRY, INT ON — These lines are used to convey the status information of the processor mainly for display on an operator console.

RUN (Output) — A HIGH level on this line indicates that the 9440 is not in the WAIT state and is executing instructions or performing console operations.

CARRY (Output) — Shows the current status of the 9440 Carry flip-flop. A HIGH level is a binary '1'.

INT ON (Output) — Shows the state of the 9440 Interrupt Enable flip-flop. A HIGH level indicates that the 9440 is enabled to accept interrupts.

Operator Console Control — C_0-C_3, $\overline{MR}$ — Using the operator console, a special I/O device, the operator controls 9440 operation via the four C lines and the Master Reset line.

C_0-C_3 (Inputs) — The various console operations are coded on the Control lines as shown below. These lines must be active long enough for the 9440 to respond to the command and indicated by RUN going to the high state, and should be disabled immediately thereafter.

$\overline{MR}$ (Input) — When a LOW level is applied to Master Reset, the 9440 halts immediately and goes to a wait state. All internal registers are unaffected. The Interrupt-Enable flip-flop is cleared.

Input/Output Control — O_0-O_1, $\overline{INT\ REQ}$, $\overline{DCH\ REQ}$ — I/O devices communicate with the 9440 through the common information bus under either program or interrupt control. Also, high-speed devices can gain access to main memory via the data channel (DMA mode).

O_0, O_1 (Outputs) — To avoid conflicts on the information bus, the I/O devices are sent synchonization signals. A code, defining one of four functions, is conveyed to each I/O device over O_0 and O_1, which are valid before and during $\overline{SYN}$.

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C_3	C_2	C_1	C_0	OPERATION
L	L	L	L	Examine AC0
L	L	L	H	Examine AC1
L	L	H	L	Examine AC2
L	L	H	H	Examine AC3
L	H	L	L	Examine Next
L	H	L	H	Examine Memory
L	H	H	L	Deposit Memory
L	H	H	H	Halt
H	L	L	L	Deposit AC0
H	L	L	H	Deposit AC1
H	L	H	L	Deposit AC2
H	L	H	H	Deposit AC3
H	H	L	L	Load PC
H	H	L	H	Continue
H	H	H	L	Deposit Next
H	H	H	H	No operation

Console-Operation Code

O_1	O_0	FUNCTION
L	L	Instruction Fetch
L	H	Data Channel Acknowledge
H	L	I/O Execute
H	H	No Operation

I/O-Device Code

$\overline{\text{INT REQ}}$ (Input) — The I/O devices can interrupt normal program flow by activating the Interrupt Request input. The 9440 recognizes an interrupt request at the end of the current instruction provided its Interrupt-Enable flip-flop is set.

$\overline{\text{DCH REQ}}$ (Input) — The I/O devices can gain direct access to the main memory by activating the Data Channel Request input. After the device is granted data channel access, it can control memory operation using the $\overline{M}_0$-$\overline{M}_2$ lines.

Of the four functions which can interrupt the normal flow if instruction execution, MASTER RESET ($\overline{\text{MR}}$) is the highest priority, followed in order by $\overline{\text{DCH REQ}}$, $\overline{\text{INT REQ}}$ and the Console HALT Command.

Memory Control — $\overline{M}_0$-$\overline{M}_2$, $\overline{\text{MBSY}}$ — The processor controls the main memory via the three open-collector Memory Control lines ($\overline{M}_0$-$\overline{M}_2$) and synchronizes itself to the memory cycle time indicated by the Memory-Busy ($\overline{\text{MBSY}}$) signal.

$\overline{M}_0$ (Input/Output) — A LOW level on $\overline{M}_0$ indicates a memory Read operation.

$\overline{M}_1$ (Input/Output) — A LOW level on $\overline{M}_1$ indicates a memory Write operation.

$\overline{M}_2$ (Input/Output) — A LOW level on $\overline{M}_2$ indicates that the memory address register must be loaded on or before the HIGH-to-LOW transition of $\overline{\text{SYN}}$.

During DMA operation, the 9440 is not driving the $\overline{M}$ lines. An external device can control memory by applying a LOW level on the appropriate $\overline{M}$ line.

$\overline{\text{MBSY}}$ (Input) — A LOW level on $\overline{\text{MBSY}}$ indicates a memory operation is in progress. When the 9440 starts a memory cycle, $\overline{\text{MBSY}}$ must be HIGH. If it is LOW, the processor clock logic will defer putting out $\overline{\text{SYN}}$ until $\overline{\text{MBSY}}$ becomes HIGH. For LD MAR or Write memory operations, the 9440 activates $\overline{\text{SYN}}$ and then waits for $\overline{\text{MBSY}}$ to respond with a LOW level. For a Read operation, the 9440 waits for $\overline{\text{MBSY}}$ to go LOW and back HIGH before it proceeds.

Timing — CP, XTL, CLK OUT, $\overline{\text{SYN}}$ —

CP (Input) — The 9440 can operate with an on-chip oscillator when a crystal is tied between CP and XTL or it can operate from an external clock (CP).

XTL (Input) — The XTL input is used only when operating with a crystal.

CLK OUT (Output) — The internal oscillator is available to the outside world on CLK OUT.

$\overline{\text{SYN}}$ (Output) — $\overline{\text{SYN}}$ is an active LOW synchronization signal for memory and I/O devices. It is activated once for each processor microcycle.

Power — V_{CC}, I_{INJ}, GND

V_{CC} requires 5 V, I_{INJ} requires 300 mA current source at 1.0 V.

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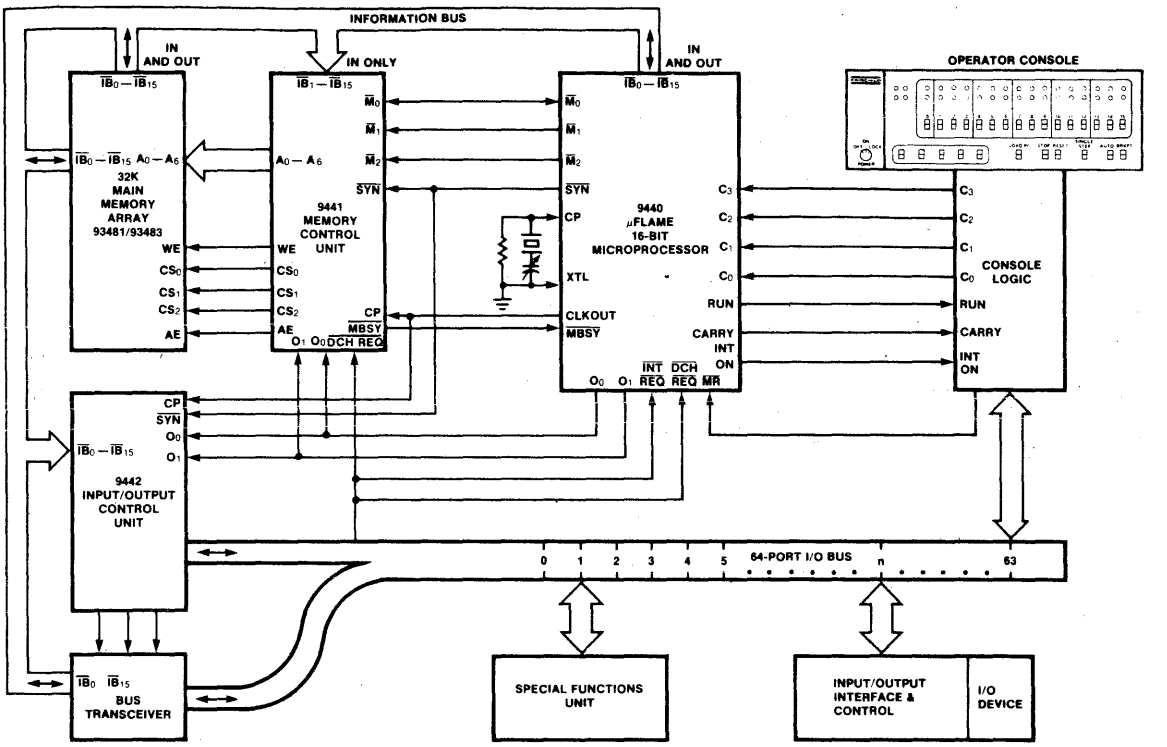


Fig. 4 9440 Microflame System

9440 SYSTEM

The 9440 CPU is a powerful machine that acts as the heart of a minicomputer-class microprocessor. However, to maximize performance, any CPU must be surrounded by support devices. A perfectly matched system can be built as shown in *Figure 4*.

Here, in addition to the 9440 CPU, the system contains the 9441 Memory Control Unit, the 9442 Input/Output Control Unit, the Special Functions Unit and an array of 93481 or 93483 I3L dynamic memories as follows:

9441 Memory Control Unit contains a 15 bit memory address register, refresh address counter and a 7-bit address multiplexer. It provides the timing and control signals to operate the I3L dynamic memory (93481, 93483) for read, write, refresh and DMA operations.

9442 Input/Output Control Unit responds to I/O instructions and generates the timing and control signals for 9440 peripheral devices.

93481 4K I3L bipolar dynamic memory. Single 5 V supply, 100 ns performance, compatible semiconductor memory.

93483 16K I3L bipolar dynamic memory. Single 5 V supply, 100 ns performance, compatible semiconductor memory.

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9440 INSTRUCTION EXECUTION

NO	INSTRUCTION OR OPERATION	CYCLE TYPE AND SEQUENCE*								EXECUTION TIME (μs) @		
		FETCH	READ	WRITE	LD MAR	I/O OUT	I/O IN	WAIT	DCH	8 MHz	10 MHz	12 MHz
1	Jump	1								1.875	1.5	1.25
2	Jump Indirect	3	1	2						5.50	4.4	3.66
3	Jump to Subroutine	1								1.875	1.5	1.25
4	JSR Indirect	3	1	2						5.50	4.4	3.66
5	Increment and Skip if Zero	3	1	2						5.50	4.4	3.66
6	ISZ Indirect	5	1,3	2,4						9.125	7.3	6.07
7	Decrement and Skip if Zero	3	1	2						5.50	4.4	3.66
8	DSZ Indirect	5	1,3	2,4						9.125	7.3	6.07
9	Load Accumulator	2	1							3.75	3.0	2.50
10	LDA Indirect	4	1,3	2						7.375	5.9	4.91
11	Store Accumulator	3	1	2						5.50	4.4	3.66
12	STA Indirect	5	1,3	2,4						9.125	7.3	6.07
13	Complement	1								1.875	1.5	1.25
14	Negate	1								1.875	1.5	1.25
15	Move	1								1.875	1.5	1.25
16	Increment	1								1.875	1.5	1.25
17	Add Complement	1								1.875	1.5	1.25
18	Subtract	1								1.875	1.5	1.25
19	Add	1								1.875	1.5	1.25
20	AND	1								1.875	1.5	1.25
21	ALU with Skip	1,2								3.75	3.0	2.50
22	I/O Data In	2					1			3.125	2.5	2.08
23	I/O Data Out	2				1				3.125	2.5	2.08
24	Skip on Busy or Done	2					1			3.125	2.5	2.08
25	Interrupt	5	3	2,4	1					9.0	7.2	5.98
26	Data Channel								1	1.25	1.0	0.83
27	Wait							1		1.25	1.0	0.83
28	Examine Accumulator					2	1	3		2.50	2.0	1.66
29	Deposit Accumulator					2	1	3		3.125	2.5	1.66
30	Load PC		2				1	3		3.125	2.5	2.08
31	Examine Memory		2				1	3		3.125	2.5	2.08
32	Examine Next		2				1	3		3.125	2.5	2.08
33	Deposit Memory			3	2		1	4		4.75	3.8	3.15
34	Deposit Next			3	2		1	4		4.75	3.8	3.15
35	Continue	2					1			3.125	2.5	2.08

*e.g., No. 6, ISZ Indirect:
1st cycle — READ
2nd cycle — WRITE
3rd cycle — READ
4th cycle — WRITE
5th cycle — FETCH

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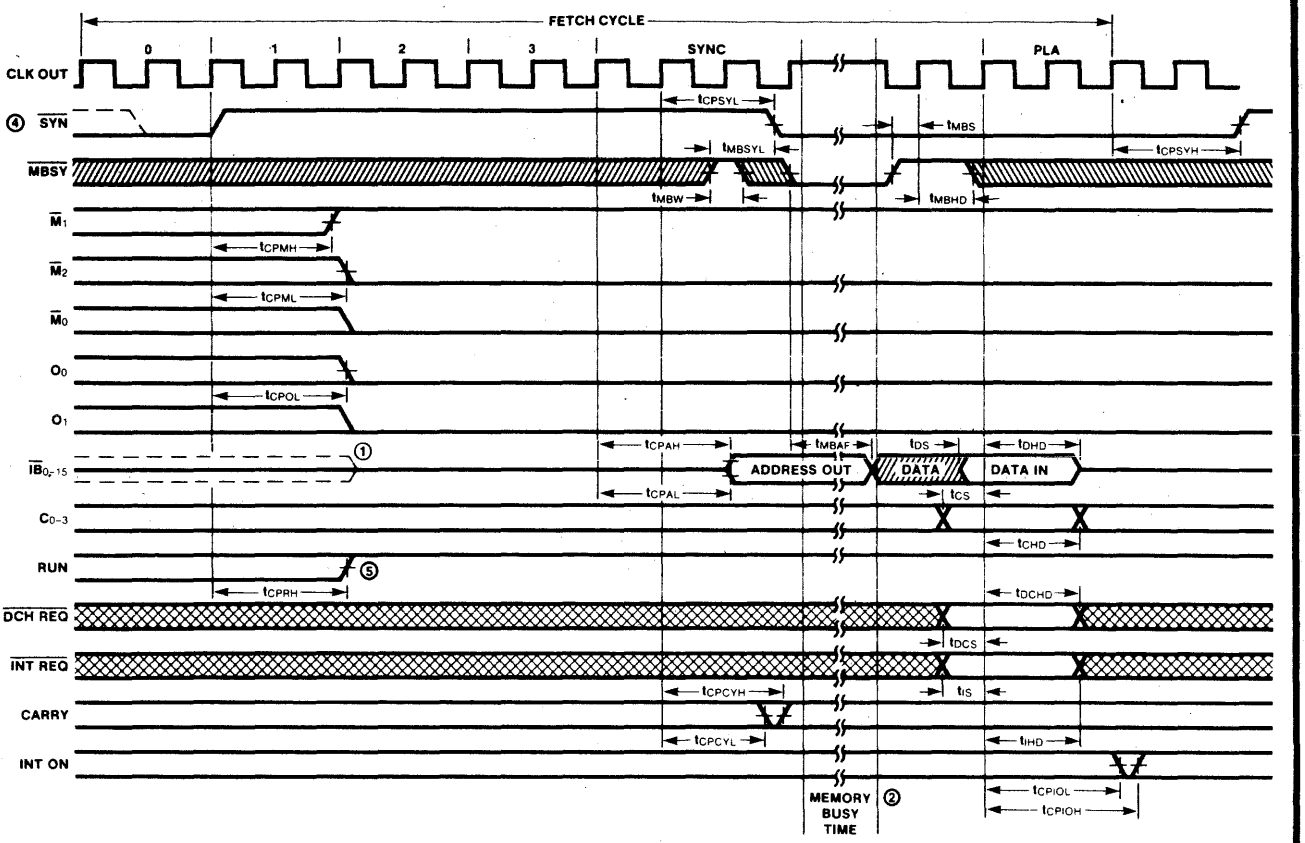
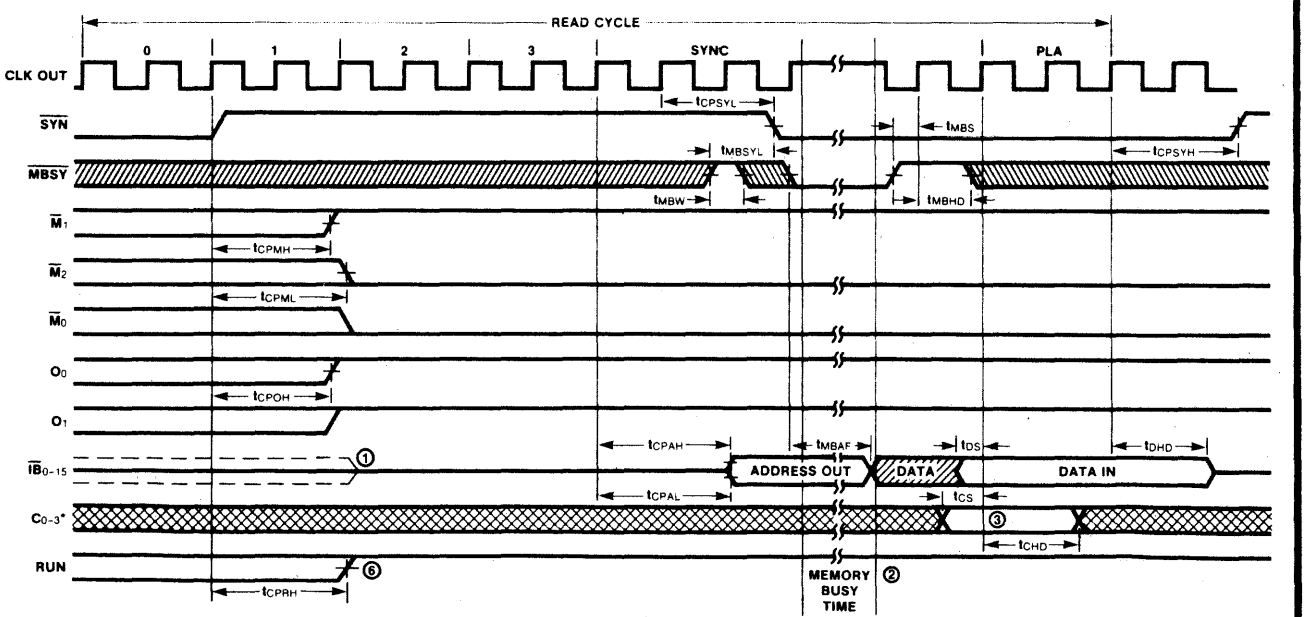


Fig. 5 Fetch Cycle

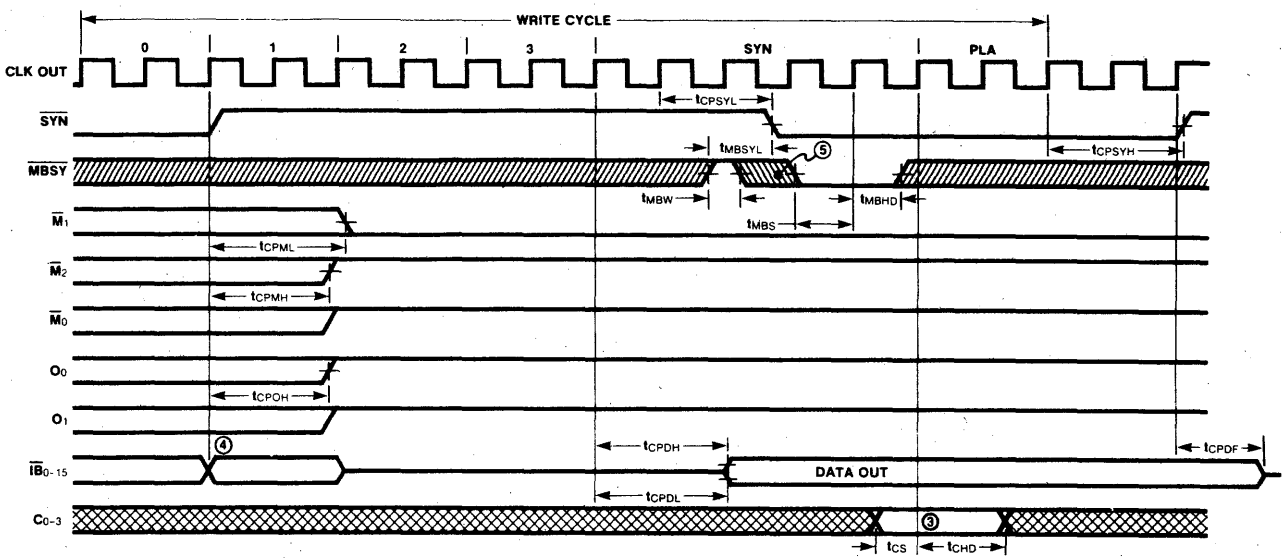


RUN, $\overline{\text{DCH REQ}}$, $\overline{\text{INT REQ}}$, CARRY, INT ON unaffected during this cycle.

Fig. 6 Read Cycle

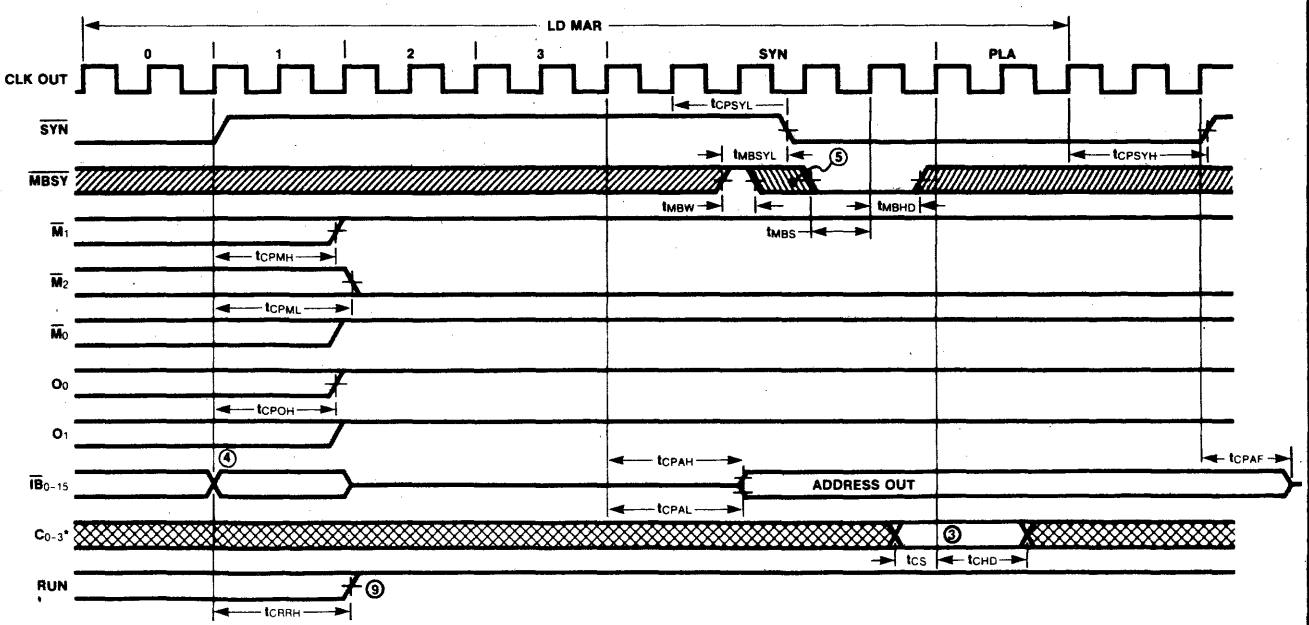
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NOTES:
1. The Information Bus is driven as a result of the previous cycle.
2. The Fetch and Read cycles will be stretched out for slower memories.
3. Applies to console operation using this cycle type.
4. When the previous cycle was an I/O IN or I/O OUT cycle.
5. For a CONTINUE operation (#35 in the "9440 Instruction Execution" table on page 18).
6. For a LOAD PC, EXAMINE MEMORY or EXAMINE NEXT operations (#30, 31, 32 in the "9440 Instruction Execution" table on page 18).
7. The Information Bus is driven as a result of the previous cycle.
8. The 9440 waits for $\overline{MBSY}$ to go LOW. By holding $\overline{MBSY}$ HIGH, the user may idle the processor.
9. For DEPOSIT MEMORY or DEPOSIT NEXT operations (#33, 34 in the "9440 Instruction Execution" table on page 18).
10. For EXAMINE ACCUMULATOR or DEPOSIT ACCUMULATOR operations (#28, 29 in the "9440 Instruction Execution" table on page 18).



RUN, $\overline{DCH\ REQ}$, $\overline{INT\ REQ}$, CARRY, INT ON unaffected during this cycle.

Fig. 7 Write Cycle



$\overline{DCH\ REQ}$, $\overline{INT\ REQ}$, CARRY, INT ON unaffected during this cycle.

Fig. 8 Load Memory Address Register Cycle

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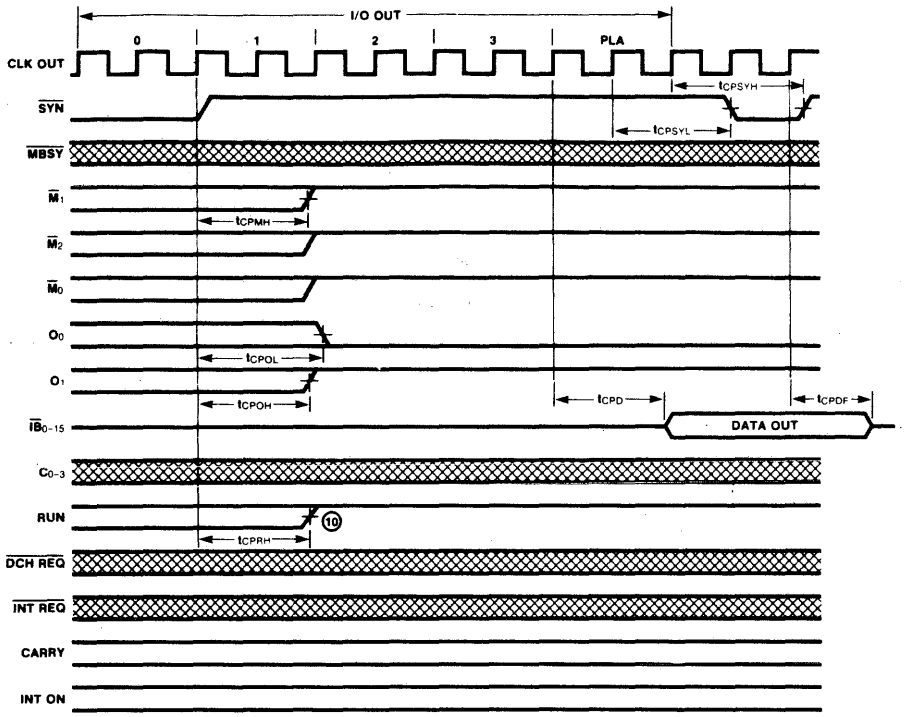


Fig. 9 I/O Out Cycle

NOTES:
11. During $\overline{DCH}$, the 9440 is not driving the $\overline{M}$ lines. An external device can control the memory when a LOW is applied to the appropriate $\overline{M}$ line.
12. The 9440 floats the $\overline{IB}_{0-15}$. The Information Bus is available to the I/O devices, the Console, and the memory as needed.
13. For all the CONSOLE operations (#28-35 in the "9440 Instruction Execution" table on page 18).
14. For CONSOLE operations (#28-34 in the "9440 Instruction Execution" table on page 18).

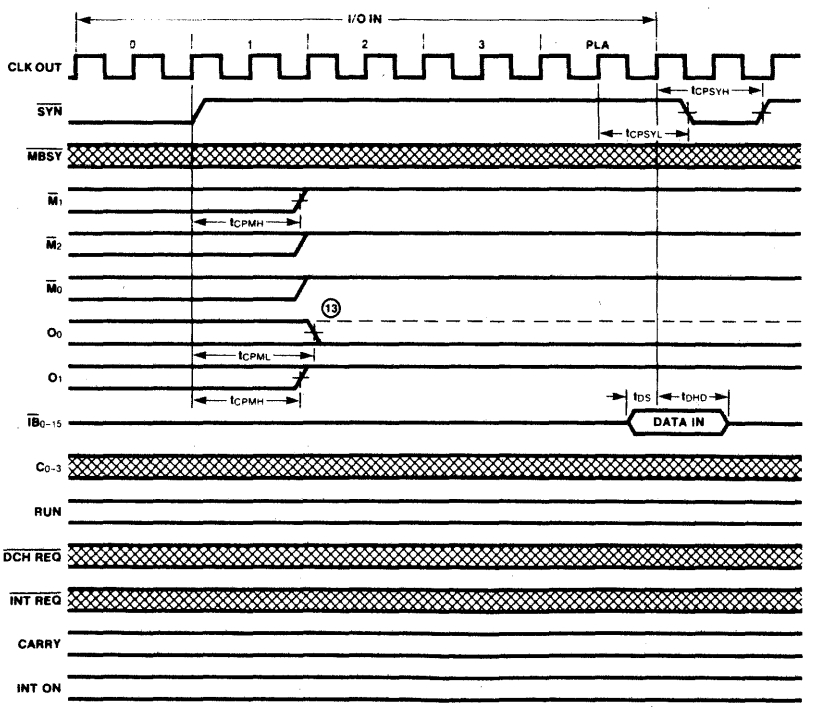


Fig. 10 I/O In Cycle

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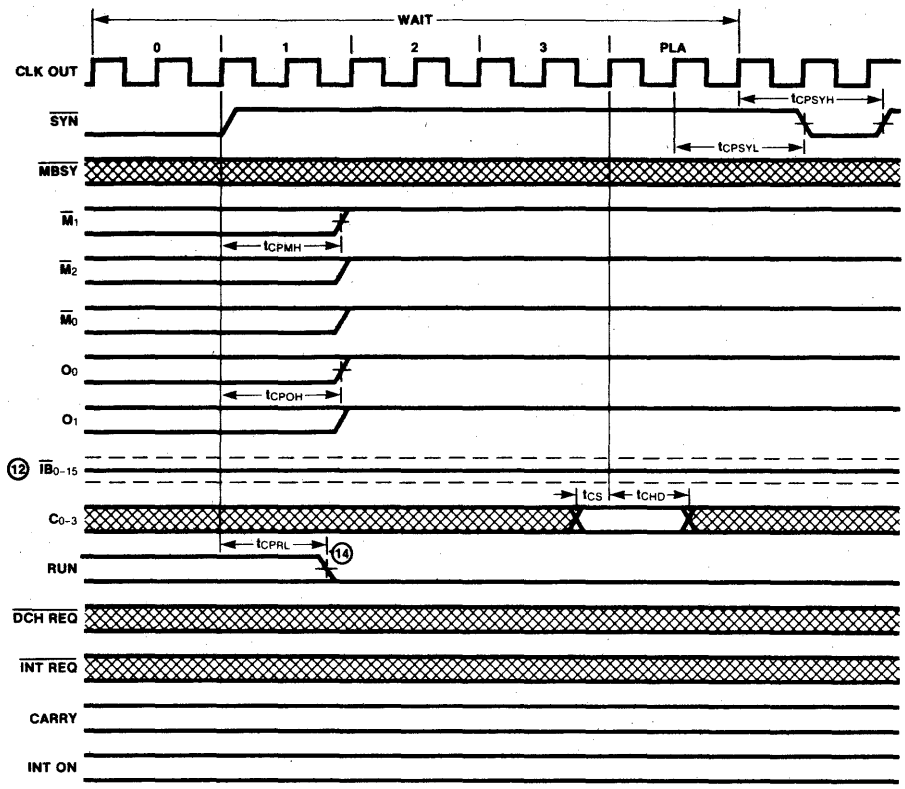


Fig. 11 Wait Cycle

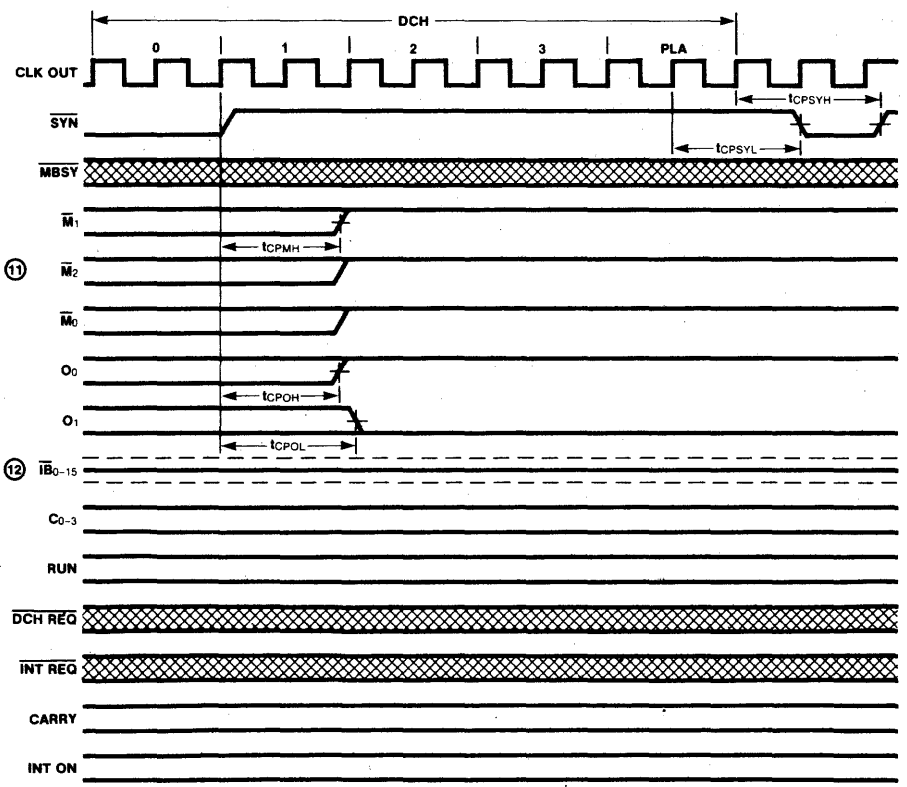
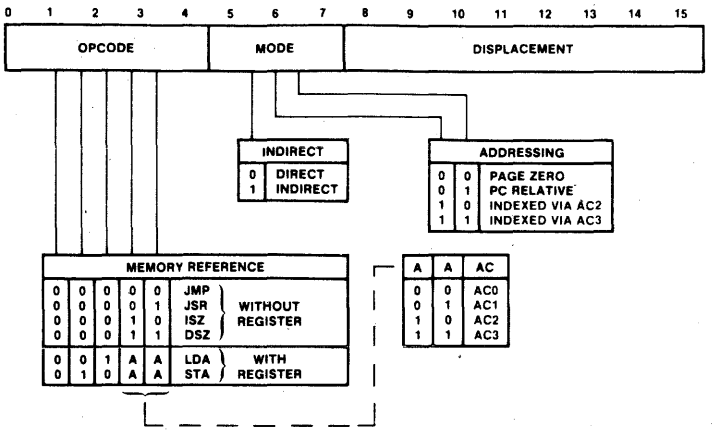


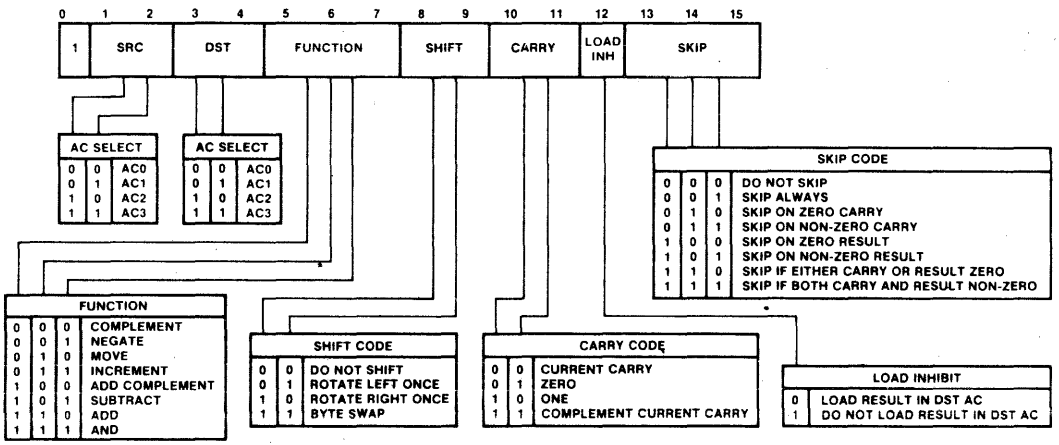
Fig. 12 Data Channel Request Cycle

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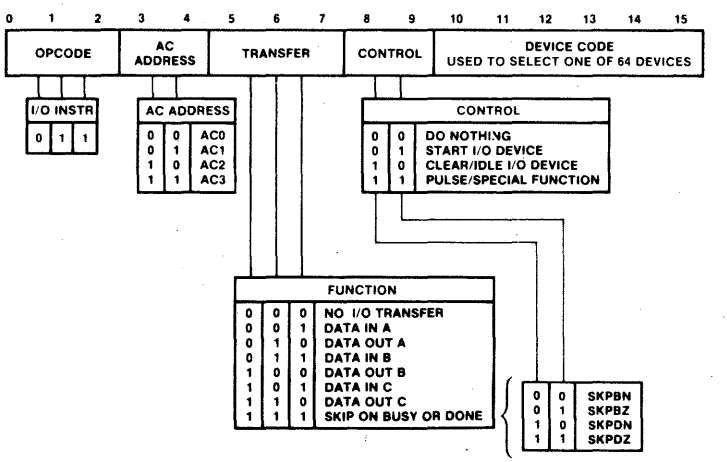
9440 INSTRUCTIONS



Memory Reference instructions without register are used for branching (JMP, JSR) without involving accumulators. These instructions are also used for modifying memory (ISZ, DSZ). Memory Reference instructions with register are used to move 16-bit words between the memory and the accumulators.



Arithmetic/Logic instructions perform arithmetic (ADD, ADC, INC, NEG, SUB) or Boolean (AND, COM, MOV) operations on the contents of two registers. The result of each operation together with the Carry bit can be rotated and tested for skip conditions as part of the same arithmetic/logic instruction; loading in the destination register is optional.



Input/Output instructions move data between the 9440 accumulators and three buffers in the peripheral device interface. These instructions also perform control functions in the I/O device and test the status flags in both the peripheral circuitry and the central processor.

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FAIRCHILD INTEGRATED REAL-TIME EXECUTIVE (FIRE) SOFTWARE

The instruction set resident in the 9440 MICROFLAME CPU will be familiar to those who have had experience with the NOVA instruction set. It consists of 2192 different instructions divided into four convenient classes — Memory Reference with or without register, Arithmetic/Logic, and Input/Output.

A comprehensive FIRE software system has been developed to thoroughly support the MICROFLAME-based products in a variety of applications. It includes programs that range from the simplest bootstrap and binary loaders (FIRE-LOAD) to the most sophisticated FIRE-FORTRAN and FIRE-IDOS. Also, a cross macro-assembler, a cross linking loader and a cross simulator debugger are available on a worldwide time-sharing basis for program development.

The basic software package, FIRE 1, includes FIRE-DIAGNOSTICS, FIRE-LOAD bootstrap and binary loaders and FIREBUG interactive assembler, debugger and editor. FIRE-DIAGNOSTICS programs, for trouble-shooting the FIRE family of products, consist of a Toggle-In Memory Address test and Memory Tester (FIRE-TOGGLE), an Instruction Timer (FIRE-TIMER), a System Exerciser (FIRE-EX), and Memory Diagnostic (FIRE-MEM).

FIRE-TOGGLE

The Toggle-In Memory Address test and the Memory Tester programs are each short enough (approximately 10 words) to enter via the console switches. The Memory Address test program tests the memory addressing by writing into the memory locations and reading each location on a second pass. The Memory Tester program performs a non-destructive memory test; that is, the original content of each word is restored after testing that the word may be written into the memory and read back.

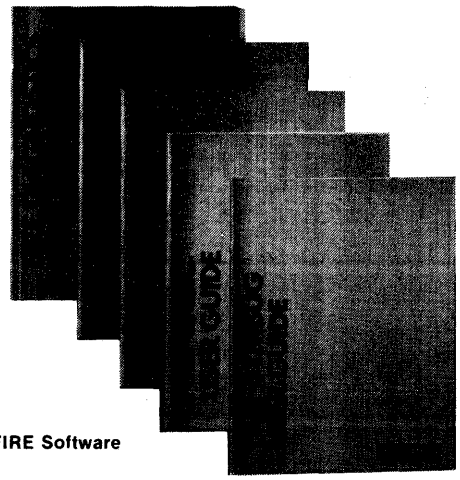
These tests are normally used for two reasons. Firstly, they give a measure of confidence that the CPU and memory work. In this sense, they are useful for verifying that the system is functional after, for instance, swapping memory boards. Secondly, if the system fails, therefore precluding the loading of more advanced diagnostics, these tests can help to identify which device is at fault, the CPU,the memory or the I/O.

FIRE-TIMER

The FIRE-TIMER program is used to determine the instruction execution times. It uses the I/O terminal device as the standard with which to measure the times and to report the results. The instruction timer is most useful for detecting clock drift and for demonstration purposes.

FIRE-EX

The FIRE-EX System Exerciser program is the primary tool for testing and debugging the CPU, I/O terminal device (TTI and TTO), and high-speed paper tape reader and punch (PTR and PTP). In addition, most memory faults should be detected. The program performs and exhaustive test of the CPU's ability to perform all non-I/O instructions, then executes detailed tests on memory and each I/O device, and finally tests all I/O devices and memory simultaneously. Using the console switches, the operator determines the I/O devices to be tested and the testing sequences to be performed.



FIRE Software

FIRE-MEM

The FIRE-MEM Memory Diagnostic program is designed to thoroughly test the system main memory. The tests performed are the True/Complement Address test, the Checkerboard Test, the Walking Well test, and the Ping-Pong test. The console switches are used to select the tests to be performed and to control typing of error messages. The FIRE-MEM program moves around in the memory to test each area completely.

FIRE-LOAD

The FIRE-LOAD Bootstrap and Binary Loader program is used to load data from paper tapes into the memory in absolute binary format. Each record from the tape is read into a buffer and checksum checked before any data are stored. This prevents data from being stored in the wrong place due to a read error on the address word.

FIREBUG

The FIREBUG Interactive Entry and Debugging program acts as a position-independent, stand-alone mini executive that is available on various media, including PROMs. With the PROM version of FIREBUG, the MICROFLAME-based system can be controlled without the usual operator console. FIREBUG is used to enter, modify, list, punch, load, assemble, disassemble, debug, and monitor symbolic assembly language programs. Debugging and monitoring of programs is greatly aided by the program's powerful multiple breakpoints and trace capabilities. The FIREBUG program is position-independent and can be moved to any available location after loading in main memory. All FIREBUG program operations can be performed from the terminal keyboard. Once FIREBUG software is loaded into the system, the computer console is no longer required. One can start and stop program execution, examine and modify all registers and memory locations without resort to front panel switches.

ADDITIONAL FIRE PROGRAMS

Other components of the FIRE software package include an advanced debugger (FIRE-SYMBUG), a text editor (FIRE-EDIT), an extended BASIC language interpreter (FIRE-BASIC), a macro-assembler (FIRE-MACRO) with relocatable loader (FIRE-RELOAD), an extended ANSII-77 FORTRAN IV compiler (FIRE-FORTRAN), a floppy-disk operating system (FIRE-FDOS), an interactive disk operating system (FIRE-IDOS) and the companion program libraries (FIRE-LIBE).

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FIRE COMPUTERS
To capitalize on the FIRE family's distinctive characteristics, a set of computer boards has been developed to meet a broad range of data-processing requirements for immediate application in users' systems:

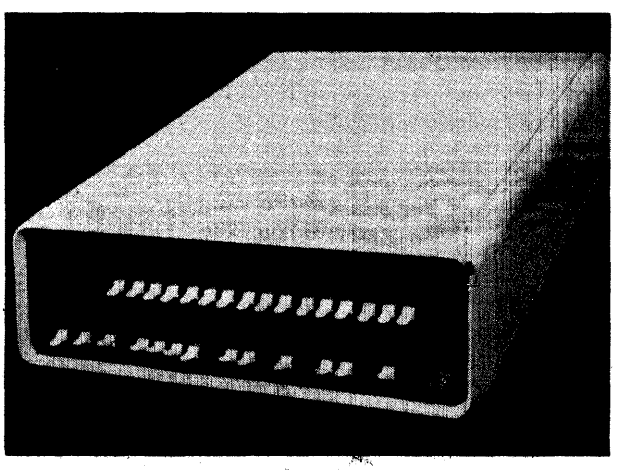
- SPARK-16 for small, low-cost memory requirements
- BLAZE-16 with NOVA 3 capabilities for large, high-performance requirements.

Instruction execution times are given in *Table 1* for both the FIRE family and the NOVA computers.

SPARK-16 Microcomputer Board *(Figure 14)*
SPARK-16 is a double-sided 8" x 10" pc board designed as a vehicle for evaluating the 9440 MICROFLAME CPU. It may also be used as a stand-alone microcomputer for applications that require small amounts of memory. It includes the following:

- 16-bit 9440 MICROFLAME CPU
- 4K words of bipolar dynamic RAM (93481s)
- 2K words of autoload PROM (loaded with the FIREBUG Autoload program)
- Memory control with DMA capability
- Logic for a serial port — current loop (TTY) or RS232C interface
- 100-pin edge connector with the 9440 bus
- Connector for TTY/RS232C
- Control switches and display (Autoload, Continue, Halt, Reset).

SPARK-16 requires only a single 5 V, 4.5 A supply and a TTY or CRT terminal. When the Reset and Autoload switches are activated, FIREBUG provides a system ready to accept commands interactively from the terminal. Similar PROM resident programs, such as BABY BASIC, will be available as optional replacements for FIREBUG PROMs.



FOCVS XVI Computer Box

BLAZE-16 Minicomputer Board Set *(Figure 15)*
BLAZE-16 is a 16-bit microprogrammed minicomputer, implemented with the Macrologic bit-slice microprocessor set. It is compatible with the NOVA 3, as well as the 9440 MICROFLAME microprocessor, and executes the same instruction set. Implemented on two 15" x 15" pc boards, BLAZE-16 includes the subsystems listed on page 13.

Board 1 — BLAZE-16/C

- Macrologic microprogrammed CPU
- Memory control logic
- A 16K word memory array (using 93481 4K x 1 RAMs)
- Memory parity logic
- Memory mapping logic (up to 256K words addressing)
- Autoload logic and FIREBUG PROMs
- Input/Output bus converter

Board 2 — BLAZE-16/M

- A 16K word memory array (using 93481 4K x 1 RAMs)
- TTY/RS232C interface logic
- High-speed paper tape reader/punch interface logic
- Real-time clock.

The BLAZE-16 CPU can essentially be divided into two major parts — a 16-bit-wide data path and a microprogram control. The data path consists of four 9405A arithmetic logic register stacks, each with eight registers/accumulators, and four 9404 data path switches. A 9408 I^3L microprogram sequencer controls the 1024-word by 48-bit microprogram, which resides in twelve 1024 x 4 ROMs. In addition to the basic FIRE instruction set, the BLAZE-16 microprogram handles the multiply and divide instructions and the stack handling operations. It includes a self-test routine and 15 operator-console routines. About 70% of the microprogram memory is free for user microprogramming and future instruction-set expansion. BLAZE-16 operates in a pipeline mode with a 200 ns microcycle. A 16-bit-wide bidirectional bus, common to all peripheral devices as is that of the 9440-based system, transfers both addresses and data between the CPU and main memory. The memory arrays are designed to accommodate the 93483 16K x 1 bipolar RAMs, which expands BLAZE-16 to a 128K-word minicomputer system.

FOCVS XVI AND THERMOSTAT
The FOCVS XVI computer box features a 9-slot chassis, regulated power supply and a front-panel computer console. It is attractively designed for stand-alone use or to fit into a standard RETMA rack on chassis slides. The front panel console latches and displays the data and address; it has control switches for examining the memory and accumulator contents, for depositing data and for setting hardware breakpoints. Lights and control switches are also provided for examining and debugging the microprogram when FOCVS is used with BLAZE-16. The chassis accommodates up-to-nine standard 15" x 15" pc boards including BLAZE-16, and the NOVA-compatible controller and interface boards. The THERMOSTAT is a hand-held console designed for use in MICROFLAME-based systems without front-panel console control. □

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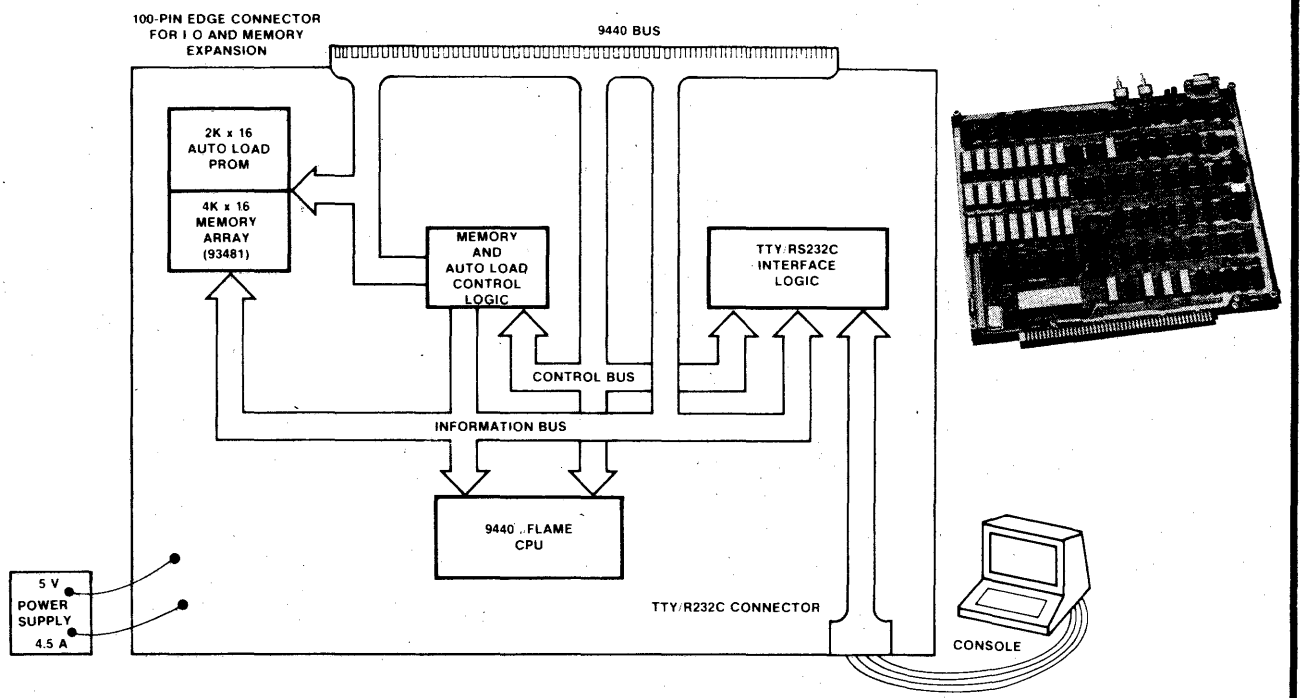


Fig. 14 SPARK-16 Microcomputer Board

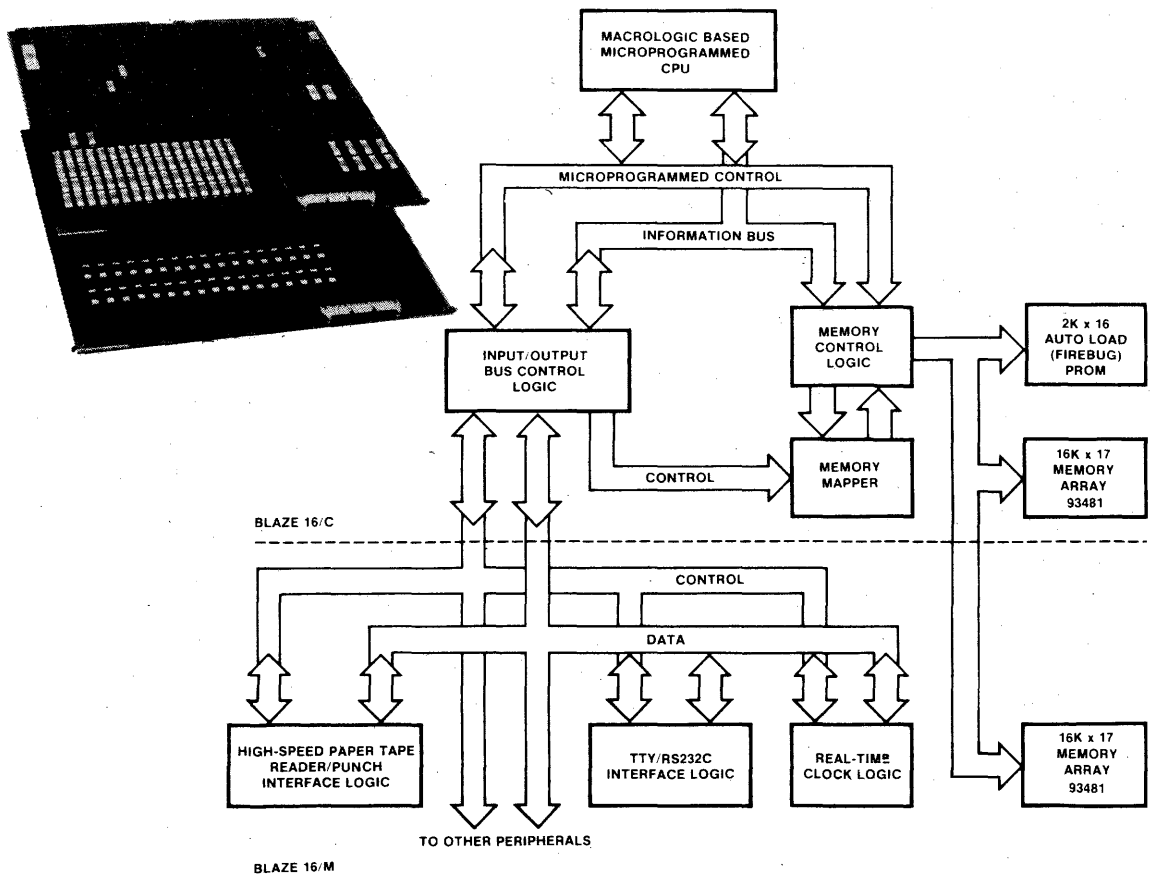


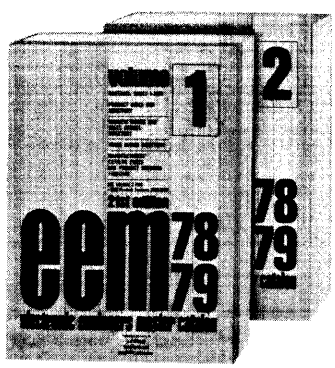
Fig. 15 BLAZE-16 Minicomputer

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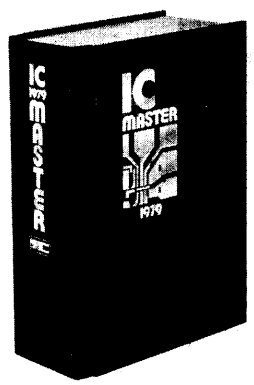
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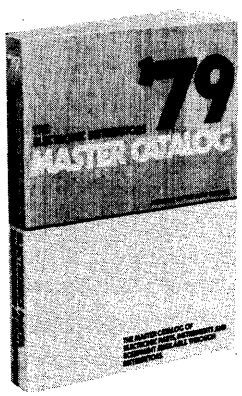


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THE HM-6100 MICROPROCESSOR

GENERAL DESCRIPTION

The HM-6100 is a single address, fixed 12-bit word length microprocessor that emulates the software operation of Digital Equipment Corporation's PDP-8/E. It is a monolithic circuit which is constructed using the Harris self-aligned, silicon-gate CMOS process. Operation is completely static from DC to 8MHz using a single supply (4-11V) with very low power consumption. The HM-6100 has a basic addressing capacity of 4096 12-bit words, but with optional hardware it can be extended to 32K. It performs a 12-bit ADD instruction in 2.5μ sec using a + 10V supply and in 5μsec using a 5V supply. An on-chip oscillator requires only an external crystal for operation, thereby eliminating the need for an external clock generator. All inputs and outputs permit simple interfaces to all TTL logic families. The HM-6100 is available in industrial or military temperature grades as well as Hi-Rel MIL-STD-883, Class B screened devices.

UNIQUE FEATURES

Unlike most other microprocessors which use multiple-byte instructions, the HM-6100 uses single-word instructions, affecting higher thru-put and shortening program size. Its system organization includes 128 directly addressable global registers located in the first page of RAM memory. As many as 25 register operations including register-register move and operate commands allow simple implementation of stack pointers, interrupt vectors, auto-indexing, etc. These features and more are summarized below:

SINGLE-WORD INSTRUCTIONS
Memory referenced instructions combine both operation code and operand address in a single 12-bit word. This eliminates "immediate" instructions which minimizes program size and speeds execution.

RELOCATABLE MEMORY ORGANIZATION
Memory space is divided into blocks of 4096 words which are subdivided into 32 pages of 128 words each. Any memory reference instruction within a particular page specifies an operand address that is relative to the starting location of that page. Pages can be simply relocated by specifying a new starting address.

GLOBAL REGISTERS
The first 128 words of memory (page 0) are considered to be global registers since they are directly accessible from any memory location within the 4K address field.

AUTO-INDEXED REGISTERS
Memory locations 10_8-17_8 function as general purpose auto-indexed registers if they are used to store an indirect address. When the CPU fetches this address, the contents of the register will be incremented and maintained. This feature is particularly useful in memory search routines, data movement, data counters and pointers.

SINGLE-WORD I/O TRANSFER
A single instruction provides both I/O device address and control to an input-output device. The instruction format allows 9 bits to be user defined to accommodate a number of I/O configurations.

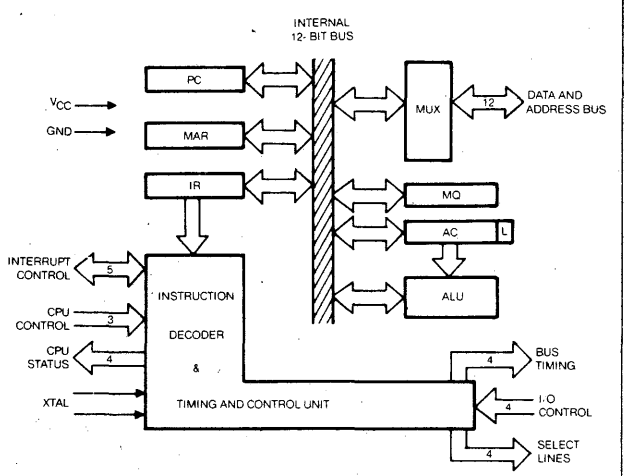
CONTROL PANEL FOR SYSTEM DEBUG
The HM-6100 can support a dedicated control panel memory. This feature is very useful in system debugging as it allows direct access to control panel monitor programs. Access is obtained on an interrupt basis by asserting the control panel request line ($\overline{\text{CPREQ}}$). In this way, control panel memory may occupy the same addressing space as the user program, yet be "transparent". The control panel request input is a true non-maskable interrupt and will be acknowledged even if the CPU is in the halt state.

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ARCHITECTURE

The HM-6100 architecture as shown in Figure 3 has three programmable 12-bit registers, an arithmetic logic unit (ALU) and associated timing and control circuitry to provide bus control, CPU control, DMA access and interrupt control.

Figure 3 HM-6100 ARCHITECTURE



INTERNAL DESCRIPTION

ACCUMULATOR/LINK (AC/L)

The AC is a programmable 12-bit register with which arithmetic and logical operations are performed. It is the source of destination for all programmed data transfers. The LINK is a 1-bit flip-flop that serves as a high-order extension of the AC.

MQ REGISTER (MQ)

The MQ is a programmable 12-bit temporary register. The contents of the AC may be transferred to the MQ. The MQ can be OR'ed with the AC and the result stored in the AC. The contents of the AC and MQ may also be exchanged.

PROGRAM COUNTER (PC)

The PC is a programmable 12-bit register which contains the address of the memory location from which the next instruction is fetched. Being 12-bits wide, the PC defines an address space of 4096 memory words. However, the PC can be effectively extended to address up to 32K memory words by using the HD-6102 MEDIC chip. The PC can be programmed from an external device to provide vectored interrupts.

MEMORY ADDRESS REGISTER (MAR)

The MAR is a 12-bit register which contains the address of the memory location that is currently being accessed. It is also used to control data transfers to and from memory and peripherals.

ALU

The ALU performs both arithmetic and logical operations such as 2's complement binary ADD, AND, OR and Complement. It can shift left or right, rotate or swap bytes. The AC always provides one input to the ALU while the second input is any one of the other registers.

INSTRUCTION REGISTER (IR)

The 12-bit IR contains the instruction that is to be executed by the CPU. The IR outputs to the Timing and Control Unit for instruction decoding.

MULTIPLEXER

The 12-bit bidirectional multiplexer handles data, address and instruction transfers on the DX bus on a time multiplexed basis.

TIMING AND CONTROL UNIT

This unit contains all ALU and register transfer logic as well as instruction decode circuitry and all memory and external device control logic. It also provides external timing and control signals to simplify CPU communication with peripherals, memory and control panel.

EXTERNAL INTERFACE

DATA AND ADDRESS BUS (DX) (12)

Bidirectional multiplexed bus used to communicate with external memory and I/O devices.

BUS TIMING (4)

Used by external logic to decode various time-multiplexed events such as read/write operations and external addresses from the DX bus.

SELECT LINES (4)

Used in conjunction with Bus Timing signals to enable main memory, control panel memory, or I/O devices.

CPU CONTROL (3)

Used to Reset, Halt or single-step the CPU. Additionally, the $\overline{\text{WAIT}}$ input allows slow memory or I/O devices to be synchronized to the CPU. The $\overline{\text{WAIT}}$ input can be used to effectively power strobe the CPU.

INTERRUPT CONTROL (5)

Used to interrupt normal CPU operation for servicing control panel memory, I/O devices, or high speed data transfers between external devices (Direct Memory Access interrupt).

CPU STATUS (4)

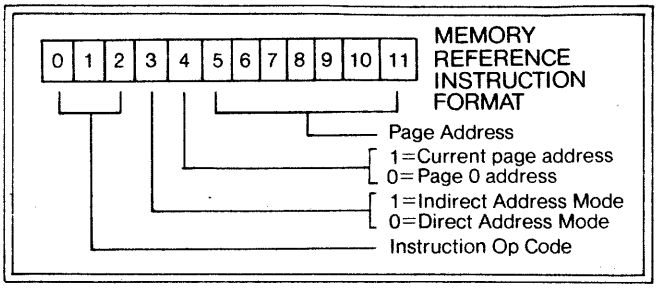
These signals specify the following: 1) Direct/Indirect addressing mode; 2) Fetch/Execute status of machine cycle; 3) Link status; 4) Run/Halt CPU status.

I/O CONTROL (4)

Used to control data transfers between the PC or AC and external Input-Output devices.

MEMORY ADDRESSING MODES

The HM-6100 uses a single 12-bit word for fast execution times, precision, and optimum software efficiency. All memory referenced instructions have the following object code format:



DIRECT ADDRESSING

The seven address bits (5-11) specify one word from a 128 word page. The memory page bit (4) specifies that word to be either in Page 0 (0$_8$ to 177$_8$) or within the current page of the instruction being executed. This allows global access to 128 general purpose memory locations in Page 0 (bit 4 = 0), in addition to 128 words within the current page (bit 4 = 1). This single instruction scheme requires no software overhead which is sometimes required in other processors utilizing 2- and 3-byte instructions.

INDIRECT ADDRESSING

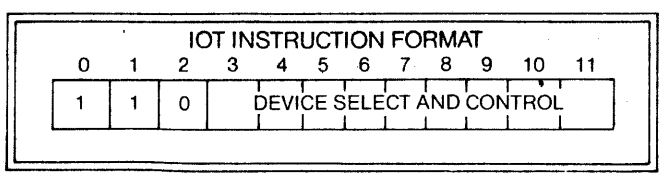
Standard indirect addressing is offered. The CPU simply interprets the contents of the memory location that is pointed to by the page address as the effective address. A memory reference instruction can access an indirect memory address either on page 0 or on the current page.

AUTO-INDEXED, INDIRECT ADDRESSING

When RAM locations 10$_8$ to 17$_8$ on page 0 are indirectly addressed, their contents are auto-incremented and returned. This simplifies sequential memory accessing. Data tables can be read sequentially by addressing the table through any one of these locations. Similarly, data movement is made easy by executing an indirect read and then an indirect write through any two of these locations.

INPUT-OUTPUT TRANSFER INSTRUCTION (IOT) FORMAT

All I/O transfer instructions have single-word formats with an octal OPCODE of six as shown below. The remaining nine bits (3-11) are user defined to provide device selection and control.



The only codes which cannot be used for I/O transfers are 6000$_8$ to 6007$_8$. They are reserved for internal processor interrupt control.

Three types of I/O transfers may be used: 1) *Programmed Data Transfers* provide a means of communicating with relatively slow peripherals such as teletypes, cassettes, card readers, CRT displays, etc. 2) *Interrupt Transfers* use the interrupt system with external hardware to service several peripherals on a vectored priority basis. 3) *Direct Memory Access (DMA) Transfers* provide a means for transferring high speed data between memory and peripherals under external control.

For typical IOT instructions refer to the HM-6100 Instruction Set Summary.

HM-6100 CPU PINS AND SIGNALS

The CPU pins and signals are illustrated in Figure 4. The 12-bit bidirectional bus is shown as DX0- DX11 with DXO being the most-significant bit. Each pin is briefly described in Table 1 below:

Figure 4

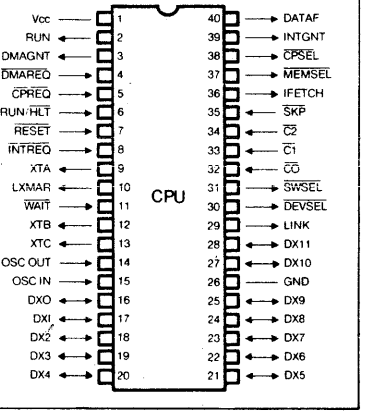


TABLE 1. PIN FUNCTION LIST

PIN NAME	DESCRIPTION	FUNCTION
DX0-DX11	Multiplexed Data and Address Bus	Data and Address Bus
XTA, XTB, XTC	External timing output signals for decoding bus operations	Bus Timing
LXMAR	Output for latching an address into an external device	
$\overline{DEVSEL}$	I/O device select output	Select Lines
$\overline{SWSEL}$	Read select for an input device	
$\overline{MEMSEL}$	Memory select output	
$\overline{CPSEL}$	Control Panel memory select output	
RUN/$\overline{HLT}$	CPU Run/Halt input	CPU Control
$\overline{RESET}$	CPU Reset input	
$\overline{WAIT}$	CPU input to synchronize slow external devices on the bus	
$\overline{DMAREQ}$	DMA request input	Interrupt Control
DMAGNT	DMA grant output, bus is floated	
$\overline{INTREQ}$	I/O interrupt request input	
INTGNT	Interrupt grant output	
$\overline{CPREQ}$	Interrupt request for Control Panel memory access	
IFETCH	Signifies an instruction fetch cycle	CPU Status
DATAF	Signifies the execute phase for indirect addressing	
LINK	Accumulator extension bit	
RUN	CPU Run/Halt status	
$\overline{C0}$ $\overline{C1}$ $\overline{C2}$ $\overline{SKP}$	Externally controlled inputs which define transfer operations between I/O devices, and the AC or PC	I/O Control
OSC OUT	Crystal or external clock input	Power and Clock
OSC IN	Crystal or external clock input	
VCC, GND	Power supply inputs	

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HM-6100 SPECIFICATIONS

Harris thoroughly tests all of its microprocessor products at various operating frequencies and supply voltages. The HM-6100 parameters shown below are specified at room temperature, TA = +25°C, only. For complete specifications over the military and industrial temperature ranges contact your nearest Harris representative for data sheets.

DC CHARACTERISTICS (TA=+25°C)

			HM-6100A VCC=+10V		HM-6100 VCC=+5V		HM-6100C VCC=+5V		
PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	MIN	MAX	MIN	MAX	UNITS
Input Voltage Logical "1" Logical "0"	 VIH VIL		 70%VCC	 20%VCC	 70%VCC	 20%VCC	 70%VCC	 0.8	 V V
Input Leakage	IIL	0<VIN<VCC	−1.0	+1.0	−1.0	+1.0	−10	+10	μA
Output Voltage Logical "1" Logical "0"	 VOH VOL	 IOH=0 IOL=0	 VCC−0.01	 +.01	 VCC−0.01	 +.01	 VCC−0.01	 +.01	 V V
Supply Current	ICC	At operating freq. (fmax)		10		2.5		5.0	mA

AC CHARACTERISTICS (TA=+25°C)

		HM-6100A VCC=+10V		HM-6100 VCC=+5V		HM-6100C VCC=+5V		
PARAMETER	SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	UNITS
Crystal Frequency	fMAX		8.0		4.0		3.33	MHz
Major State Time	TS	250		500		600		ns
LXMAR Pulse Width	TL	110		220		270		ns
Address Setup Time	tAS	30		80		100		ns
Address Hold Time	tAH	75		150		100		ns
Access Time From LXMAR	tAL	225		450		500		ns
Output Enable Time	tEN	125		250		300		ns
Read Pulse Width	tRP	350		700		800		ns
Write Pulse Width	tWP	100		200		250		ns
Data Setup Time	tDS	80		160		180		ns
Data Hold Time	tDH	50		125		150		ns
DEVSEL Write Plus Width	tWPD	110		220		270		ns
DEVSEL Enable Time	tEND	150		300		350		ns
DEVSEL Data Setup Time	tDSD	−25		−50		−70		ns
DEVSEL Data Hold Time	tDHD	75		150		150		ns

INSTRUCTION EXECUTION TIMES (+25°C)

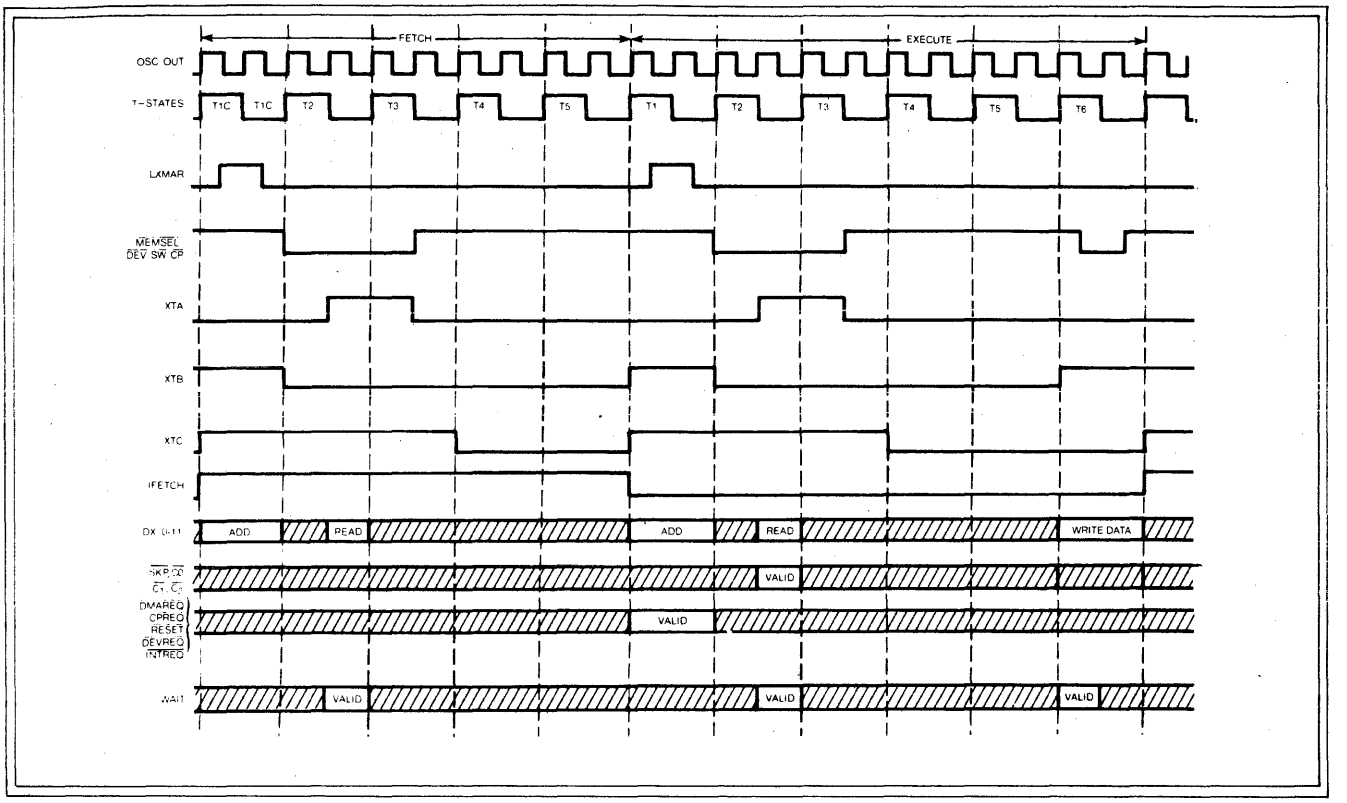
	NUMBER OF STATES	EXECUTION TIME (μS)		
TYPE	(AVERAGE)	6100A	6100	6100C
Memory Referenced	15	3.75	7.50	9.00
Register Operate	10	2.50	5.00	6.00
Input-Output	17	4.25	8.50	10.20

For a complete listing of the instruction set see Instruction Set Summary.

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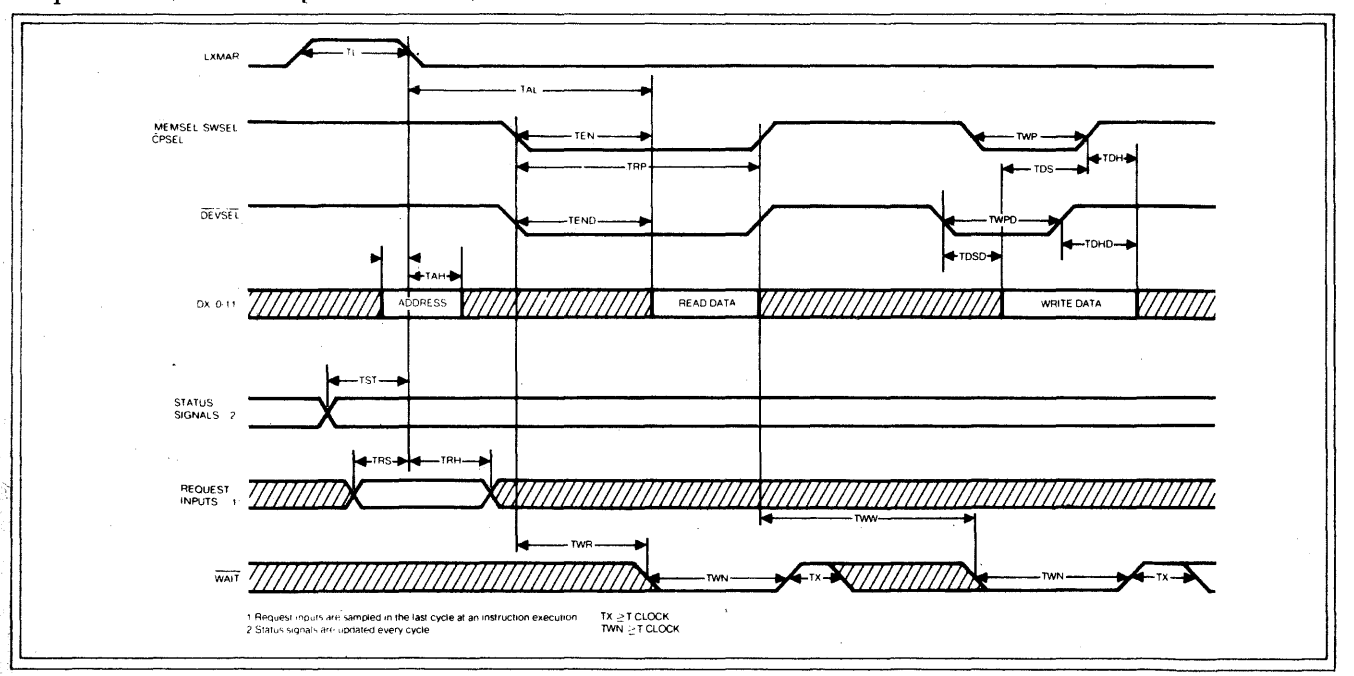
STATIC TIMING

The following illustrates the timing of the CPU when its operating frequency is low enough that propagation delays can be ignored. It effectively shows the timing of the CPU when it is single-clocked.



DYNAMIC TIMING

The dynamic or high frequency timing illustrates the propagation delays at specified operating frequencies. (Refer to specifications.) It defines the interface requirements for memory and I/O devices on the bus.



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PRODUCT OVERVIEW

MINIMUM SYSTEM

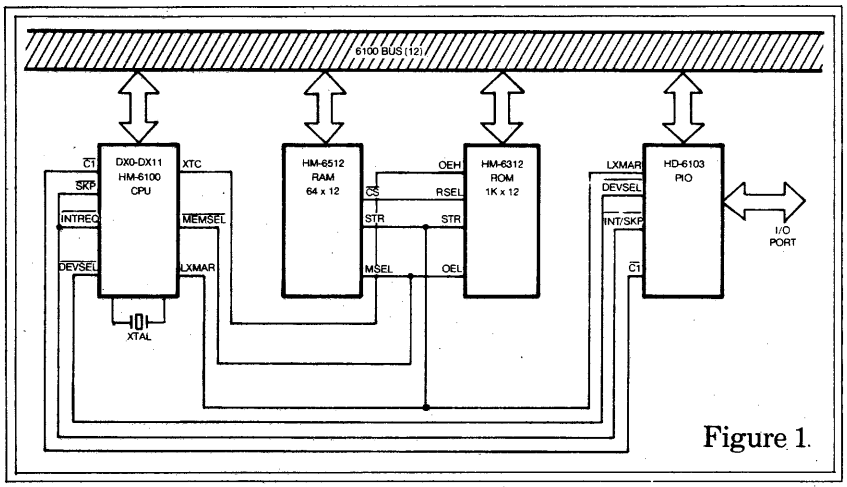


Figure 1.

4K RAM SYSTEM

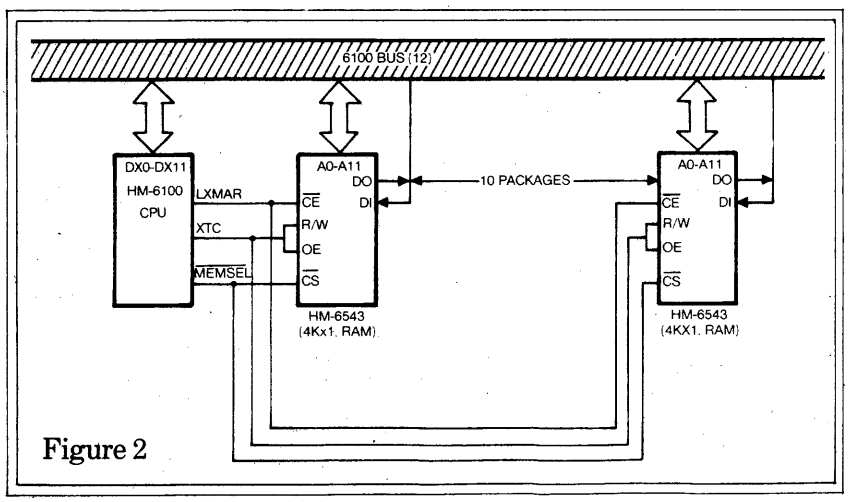


Figure 2

The Harris 12-bit CMOS microcomputer components have been optimized for low operating power, wide operating voltage range, high operating speed and direct compatibility with the HM-6100 microprocessor bus. For example, the minimum system shown in Figure 1 consists of only four packages, yet offers 64 X 12 random access memory (RAM), 1024 X 12 read only memory (ROM) and a 20-bit parallel I/O port. Using higher density CMOS memories, a complete 4K RAM system can be built with only twelve HM-6543s as shown in Figure 2. For larger system capability, the HD-6102 extends the address field of the HM-6100 CPU to 32K. Harris also offers a complete line of high speed CMOS Bus Drivers for increasing system drive capability as well as a diversified line of CMOS communications products. These and other CMOS microcomputer products are summarized below.

MINIMUM CMOS SYSTEM

- ☐ HM-6100—Low Power 12-bit CPU
- ☐ HM-6512—64 X 12 Static RAM
- ☐ HM-6312—1024 X 12 Static ROM
- ☐ HD-6103—Parallel Input-Output Port

CMOS MEMORY

Static RAMs
- ☐ HM-6561—256 X 4
- ☐ HM-6562—256 X 4
- ☐ HM-6511—64 X 12
- ☐ HM-6512—64 X 12
- ☐ HM-6518—1024 X 1
- ☐ HM-6508—1024 X 1
- ☐ HM-6504—4096 X 1
- ☐ HM-6533—1024 X 4
- ☐ HM-6543—4096 X 1

Static PROMs
- ☐ HM-6661—256 X 4
- ☐ HM-6611—256 X 4

Static ROM
- ☐ HM-6312—1024X12—

CMOS INPUT-OUTPUT PRODUCTS

- ☐ HD-6101—Peripheral Interface Element (PIE)
- ☐ HD-6102—Memory Extension/DMA/Interval Timer/Controller (MEDIC)
- ☐ HD-6103—Parallel Input-Output Port (PIO)

CMOS COMMUNICATIONS PRODUCTS

- ☐ HD-6402—Universal Asynchronous Receiver/Transmitter (UART)
- ☐ HD-6405/4702—Programable Bit Rate Generator
- ☐ HD-15530/15531—Manchester Encoder/Decoder

CMOS BUS DRIVER GROUP

- ☐ HD-6431—Hex Three-State Latched Bus Driver
- ☐ HD-6432—Hex Three-State Bidirectional Bus Driver
- ☐ HD-6433—Quad Three-State Bus Separator/Driver
- ☐ HD-6440—One-of-eight Latched Decoder-Driver
- ☐ HD-6495—Hex Three-State Buffer Driver

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SUPPORT SYSTEMS

Harris supports its microprocessor-based systems through an extensive variety of proven PDP-8 software and development systems. The latest PDP-8 development system, the DECstation 78, incorporates LSI technology to reduce size, weight and cost of first generation PDP-8s. It supports a number of peripherals including dual floppy disks, high speed printers, MODEMs, etc.

For machine language programming and prototyping of the HM-6100 system, Harris offers an inexpensive fully assembled, single board microcomputer with interactive keyboard and display.

DECstation 78 DEVELOPMENT SYSTEM

The DECstation 78 is recommended for full software support and can be purchased from Harris with a service contract agreement from DEC. It is a fully integrated, compact, inexpensive minicomputer and display system that offers all the best features of the PDP-8 and more. Some of its features are:

OS/78 OPERATING SYSTEM
Supports a number of high-level programming languages such as BASIC and FORTRAN IV, and provides a comprehensive set of software tools and utility programs.

DISPLAY AND MINICOMPUTER SYSTEM
Consists of a single compact unit, housing both the 6100-based microcomputer and CRT terminal for maximum processing capability at minimum cost. (See photograph)

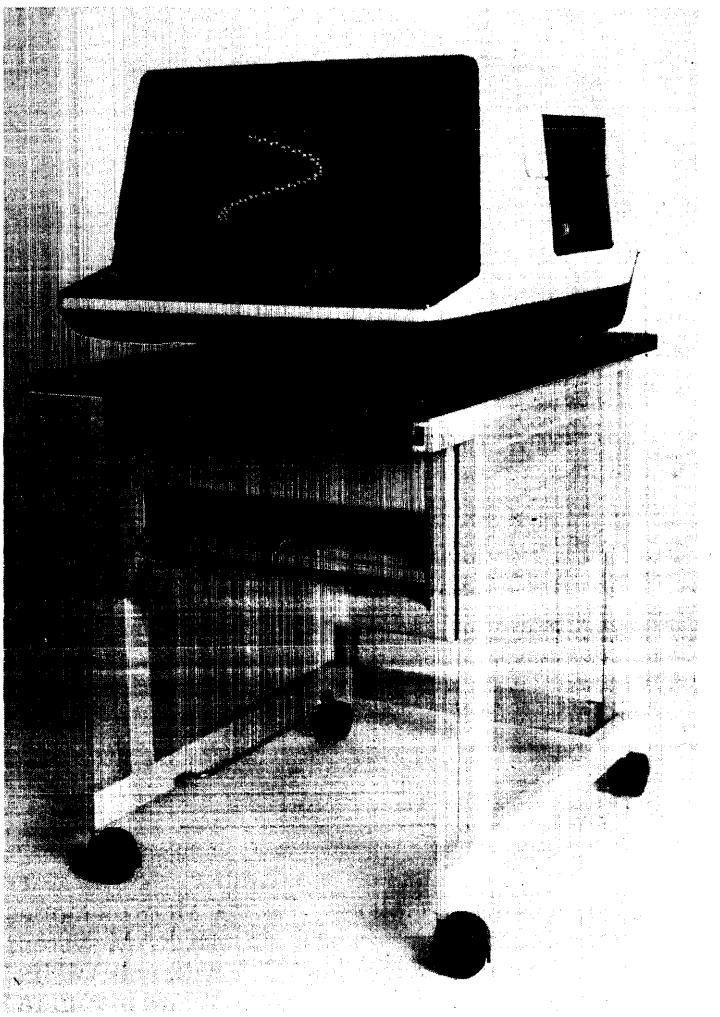
FLOPPY DISK UNIT
Includes two drives, a microprogrammed controller module and a READ/WRITE electronics module and is capable of storing 128,128 12-bit words per drive in industry standard format.

ASYNCHRONOUS COMMUNICATIONS INTERFACE
Two serial EIA RS-232C asynchronous interface ports are suitable for primary and secondary communications applications.

PARALLEL I/O PORT
Supports printers and custom interfaces and provides bidirectional 12-bit transfers at rates up to 15K words per second.

ELECTRONIC PROGRAM INJECTION PORT
Provides high-speed program loading under the control of a pre-programmed ROM unit—an inexpensive way of customizing the DECstation 78 for use in fixed function environments.

The DECstation 78 is a full capability minicomputer system designed for easy user installation. It requires no special wiring or electronic expertise to assemble.



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MICRO-12 CMOS MICROCOMPUTER SYSTEM

The Harris MICRO-12 (HB-61000) is a fully assembled and tested all CMOS single board 12-bit microcomputer. (See photograph) It consists of the following:

- ☐ ROM Monitor (1K x 12)
- ☐ 256 Word RAM Memory—expandable to 1K
- ☐ Allocated breadboard space
- ☐ 16-key Keyboard
- ☐ 8-digit LED Display
- ☐ TTY/Cassette Interface
- ☐ RS-232 Interface

The ROM Monitor program uses a 1024 X 12 CMOS ROM (HM-6312) for system monitoring and display control. It does not occupy any of the user RAM memory space, since it resides in control panel memory. The ROM Monitor supports the following commands:

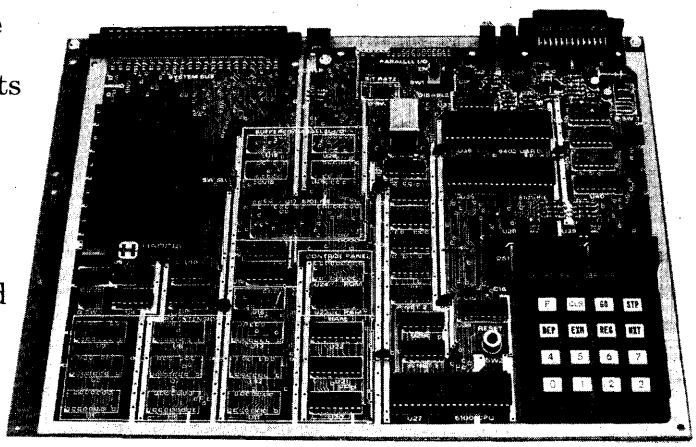
MONITOR COMMANDS

- ☐ **Examine**—Displays the contents of a selected memory location
- ☐ **Deposit**—Alters the contents of a selected memory location
- ☐ **Register-Examine**—Displays PC, AC, MQ and Link
- ☐ **Next**—Increments PC
- ☐ **Execute**—Starts user program
- ☐ **Single Cycle**—Executes a single instruction
- ☐ **Clear**—Clears AC, MQ and Link and sets PC to 7777_8
- ☐ **Function**—Sets keyboard for function commands

FUNCTION COMMANDS

- ☐ **Binary Load**—Loads user program in binary format from TTY or Tape Cassette
- ☐ **Binary Punch**—Outputs user program in binary format to TTY or Tape Cassette
- ☐ **Octal Listing**—Prints user program to TTY
- ☐ **Breakpoint Set**—Sets four independent breakpoints

The MICRO-12 is supplied complete with a documentation package consisting of details on using the system, theory of operation, circuit diagrams and a listing of the ROM Monitor program.



SUPPORT SOFTWARE

PAL 8 (ABSOLUTE ASSEMBLER)
An 8K, two pass assembler designed to run under the OS/78 operating systems. It accepts source files in PAL language and generates absolute binary files.

MACREL (RELOCATABLE ASSEMBLER)
A macro-assembler that produces relocatable program sections. Ideal for large system usage to reduce software development time.

FOPAL III (CROSS ASSEMBLER)
A cross assembler written in standard FORTRAN. It is functionally identical to the PDP-8/E PAL III Assembler, supplied with the Extended Software Package. Call factory for more information.

DECUS (DIGITAL EQUIPMENT COMPUTER USERS SOCIETY)
Provides a vehicle through which HM-6100 users can exchange ideas and information. This organization makes readily available an extensive library of proven user programs which in many cases can reduce your development efforts.

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HD-4702/6405

CMOS PROGRAMMABLE BIT RATE GENERATOR

Features

- HD-4702 – PROVIDES 13 COMMONLY USED BIT RATES
- HD-6405 – PROVIDES 15 COMMONLY USED BIT RATES
- USES A 2.4576MHz CRYSTAL/INPUT FOR STANDARD FREQUENCY OUTPUT (16 TIMES BIT RATE)
- TTL COMPATIBLE – OUTPUT WILL SINK 1.6mA
- LOW POWER DISSIPATION HD-6405 4.0mW TYP. @ 2.4576MHz
  HD-4702 4.5mW TYP. @ 2.4576MHz
- CONFORMS TO EIA RS-404
- ONE HD-4702 OR HD-6405 CONTROLS UP TO EIGHT TRANSMISSION CHANNELS
- INITIALIZATION CIRCUIT FACILITATES DIAGNOSTIC FAULT ISOLATION
- ON-CHIP INPUT PULL-UP CIRCUIT – HD-4702 ONLY

Description

The HD-4702/6405 Bit Rate Generator provides the necessary clock signals for digital data transmission systems, such as UART. It generates 13(HD-4702) or 15(HD-6405) commonly used bit rates using an on-chip crystal oscillator or an external input. For conventional operation generating 16 output clock pulses per bit period, the input clock frequency must be 2.4576MHz (i.e. 9600 Baud x 16 x 16, since there is an internal ÷16 prescaler). A lower input frequency will result in a proportionally lower output frequency.

The HD-4702/6405 can provide multi-channel operation with a minimum of external logic by having the clock frequency CO and the ÷8 prescaler outputs Q_0, Q_1, Q_2 available externally. All signals have a 50% duty cycle except 1800 Baud and 2000 Baud which has less than 0.39% distortion and 3600 Baud which has less than 0.78% distortion.

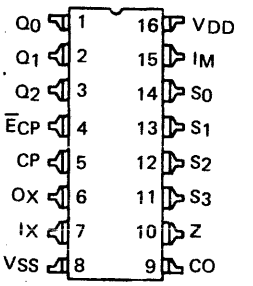
The four rate select inputs (S_0-S_3) select which bit rate is at the output (Z). The table lists select code and output bit rate. Two of the 16 for the HD-4702 and one of the 16 for the HD-6405 do not select an internally generated frequency, but select an input into which the user can feed either a different frequency, or a static level (High or Low) to generate "ZERO BAUD".

The bit rate most commonly used in modern data terminals (110, 150, 300, 1200, 2400 Baud) require that no more than one input be grounded for the HD-4702, which is easily achieved with a single, 5-position switch.

The HD-4702/6405 has an initialization circuit which generates a common master reset for all flip-flops. This signal is derived from a digital differentiator that senses the first high level on the CP input after the $\overline{E}_{CP}$ input goes low. When $\overline{E}_{CP}$ is high, selecting the crystal input, CP must be low. A high level on CP would apply a continuous reset.

For the HD-4702, all inputs except I_X have on-chip pull-up circuits which provide TTL compatibility and eliminate the need to tie a permanently high input to V_{DD}.

Pinout



PIN NAMES

$\overline{CP}$	External Clock Input
$\overline{E}_{CP}$	External Clock Enable Input (Active Low)
I_X	Crystal Input
IM	Multiplexed Input
S_0 - S_3	Rate Select Inputs
CO	Clock Output
OX	Crystal Drive Output
Q_0 - Q_2	Scan Counter Outputs
Z	Bit Rate Output

Truth Tables

TABLE 1
CLOCK MODES AND INITIALIZATION

I_X	E_{CP}	CP	OPERATION
⎍⎍	H	L	Clocked from I_X
X	L	⎍⎍	Clocked from CP
X	H	H	Continuous Reset
X	L	⎍	Reset During 1st CP = HIGH Time

NOTE: Actual output frequency is 16 times the indicated Output Rate, assuming a clock frequency of 2.4576MHz.

H = HIGH Level
L = LOW Level
X = Don't care
⎍ = 1st HIGH Level Clock Pulse after E_{CP} goes LOW
⎍⎍ = Clock Pulse

TABLE 2
TRUTH TABLE FOR RATE SELECT INPUTS

S_3 S_2 S_1 S_0	OUTPUT RATE (Z) HD-4702	OUTPUT RATE (Z) HD-6405
L L L L	MUX INPUT (I_M)	MUX INPUT (I_M)
L L L H	MUX INPUT (I_M)	2000 BAUD
L L H L	50 BAUD	50 BAUD
L L H H	75 BAUD	75 BAUD
L H L L	134.5 BAUD	134.5 BAUD
L H L H	200 BAUD	200 BAUD
L H H L	600 BAUD	600 BAUD
L H H H	2400 BAUD	3600 BAUD
H L L L	9600 BAUD	9600 BAUD
H L L H	4800 BAUD	4800 BAUD
H L H L	1800 BAUD	1800 BAUD
H L H H	1200 BAUD	1200 BAUD
H H L L	2400 BAUD	2400 BAUD
H H L H	300 BAUD	300 BAUD
H H H L	150 BAUD	150 BAUD
H H H H	110 BAUD	110 BAUD

Harris Semiconductor
MICROPROCESSOR

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ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+12.0V
Input or Output Voltage Applied	GND -0.3 to V_{CC} +0.3
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	
Industrial HD-4702A-9/6405A-9	-40°C to +85°C
Military HD-4702A-2/6405A-2	-55°C to +125°C
Operating Voltage Range	+4V to +11V

ELECTRICAL CHARACTERISTICS

D.C.: V_{CC} = 10V ± 10%; T_A = Industrial or Military.
A.C.: V_{CC} = 10V; T_A = 25°C.

	SYMBOL	PARAMETER	HD-4702A-2/ 6405A-2 MIN	TYP	MAX	HD-4702A-9/ 6405A-9 MIN	TYP	MAX	UNITS	TEST CONDITIONS
D.C.	V_{IH}	Input High Voltage	70% V_{CC}			70% V_{CC}			V	
	V_{IL}	Input Low Voltage			20% V_{CC}			20% V_{CC}	V	
	V_{OH1}	Output High Voltage	V_{CC} -0.1			V_{CC} -0.1			V	$I_{OH} \leq -1\mu A$
	V_{OL1}	Output Low Voltage	GND +0.1			GND +0.1			V	$I_{OL} \leq +1\mu A$
	I_{IH}	Input High Current	-1		+1	-1		+1	μA	$V_I = V_{DD}$, All other pins = 0V
	I_{IL}	INPUT LOW CURRENT HD-4702 (all other inputs)		-110	-170		-110	-170	μA	
	I_{ILX}	(IX inputs)	-1		+1	-1		+1	μA	V_I = 0, All other pins = V_{DD}
	I_{IL}	HD-6405 - All pins	-1		10	-1		10	μA	
	I_{OHX}	OUTPUT HIGH (OX)	0.2			0.2			mA	V_{OUT} = 9.5
	I_{OH}	CURRENT (all other outputs)	0.6			0.6			mA	V_{OUT} = 9.5
	I_{OLX}	OUTPUT LOW (OX)	0.2			0.2			mA	V_{OUT} = .5V
	I_{OL}	CURRENT (all other outputs)	3.2			3.2			mA	V_{OUT} = .5V
		SUPPLY CURRENT HD-4702A			1000			3000	μA	$\overline{E}_{CP} = V_{DD}$, CP = 0, All other inputs = GND
		HD-4702A			500			1000	μA	$\overline{E}_{CP} = V_{DD}$, CP = 0, All other inputs = V_{DD}
		HD-6405A			500			500	μA	$\overline{E}_{CP} = V_{DD}$, CP = 0, All other inputs = V_{DD} or GND
A.C.	t_{PLH} t_{PHL}	Propagation Delay, IX to CO			150 125			150 125	ns ns	$C_L \leq$ 7pF on OX
	t_{PLH} t_{PHL}	Propagation Delay, CP to CO			110 100			110 100	ns ns	C_L = 15pF Input Transition Times ≤ 20ns
	t_{PLH} t_{PHL}	Propagation Delay, CO to Q_n			⑤			⑤	ns ns	
	t_{PLH} t_{PHL}	Propagation Delay, CO to Z			40 35			40 35	ns ns	
	t_{TLH} t_{THL}	Output Transition Time (except OX)			40 20			40 20	ns ns	
	t_{PLH} t_{PHL}	Propagation Delay, IX to CO			175 140			175 140	ns ns	$C_L \leq$ 7pF on OX
	t_{PLH} t_{PHL}	Propagation Delay, CP to CO			130 110			130 110	ns ns	C_L = 50pF Input Transition Times ≤ 20ns
	t_{PLH} t_{PHL}	Propagation Delay, CO to Q_n			⑤			⑤	ns ns	
	t_{PLH} t_{PHL}	Propagation Delay, CO to Z			45 40			45 40	ns ns	
	t_{TLH} t_{THL}	Output Transition Time (except OX)			80 40			80 40	ns ns	
	t_s t_h	Set-Up Time, Select to CO Hold Time, Select to CO	175 0			175 0			ns ns	$C_L \leq$ 7pF on OX
	t_s t_h	Set-Up Time, IM to CO Hold Time, IM to CO	175 20			175 20			ns ns	C_L = 15pF Input Transition Times ≤ 20ns
	$t_{WCP(L)}$ $t_{WCP(H)}$	Minimum Clock Pulse-Width Low and High	60 60			60 60			ns ns	
	$t_{WCP(L)}$ $t_{WCP(H)}$	Minimum IX Pulse Width, Low and High	80 80			80 80			ns ns	

1. Input Current and Quiescent Power Supply Current are relatively higher for this device because of active pull-up circuits on all inputs except IX. This is done for TTL compatibility.
2. Propagation Delays (t_{PLH} and t_{PHL}) and Output Transistion Times (t_{TLH} and t_{THL}) will change with Output Load Capacitance (C_L). Set-Up Times (t_s), Hold Times (t_h), and Mininum Pulse Widths (t_w) do not vary with load capacitance.
3. The first High Level Clock Pulse after $\overline{E}_{CP}$ goes Low and must be at least 350ns long to guarantee reset of all Counters.
4. It is recommended that input rise and fall times to the Clock Inputs (CP, IX) be less than 15ns.
5. For multichannel operation, Propagation Delay (CO to Q_n) plus Set-Up Time, Select to CO, is guaranteed to be ≤ 190ns.

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ABSOLUTE MAXIMUM RATINGS

Supply Voltage		+8.0V
Input or Output Voltage Applied		GND -0.3V to V_{CC} +0.3V
Storage Temperature Range		-65°C to +150°C
Operating Temperature Range		
Industrial	HD-4702-9/6405-9	-40°C to +85°C
Military	HD-4702-2/6405-2	-55°C to +125°C
Operating Voltage Range		+4 to +7V

ELECTRICAL CHARACTERISTICS

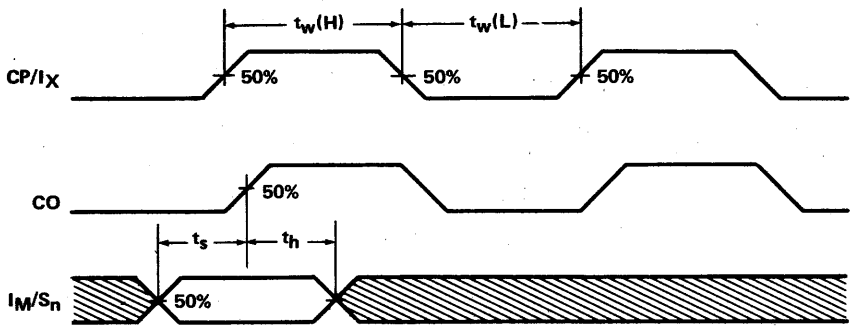
D.C.: V_{CC} = 5V ± 10%; T_A = Industrial or Military.
A.C.: V_{CC} = 5V; T_A = 25°C.

	SYMBOL	PARAMETER	HD-4702-2/ 6405-2 MIN	TYP	MAX	HD-4702-9/ 6405-9 MIN	TYP	MAX	UNITS	TEST CONDITIONS
D.C.	V_{IH}	Input High Voltage	V_{CC} -1.5			V_{CC} -1.5			V	
	V_{IL}	Input Low Voltage			1.5			1.5	V	
	V_{OH1}	Output High Voltage	V_{CC} -.05			V_{CC} -.05			V	$I_{OH} \leq -1\mu A$
	V_{OL1}	Output Low Voltage			0.05			0.05	V	$I_{OL} \leq +1\mu A$
	I_{IH}	Input High Current	-1		+1	-1		+1	µA	$V_I = V_{DD}$, All other pins = 0V
	I_{IL}	INPUT HD-4702 (all other LOW inputs)		-30	-50		-30	-50	µA	
	I_{ILX}	CURRENT (I_X inputs)	-1		+1	-1		+1	µA	V_I = 0, All other pins = V_{DD}
	I_{IL}	HD-6405 - All pins	-1		+1	-1		+1	µA	
	I_{OHX}	OUTPUT (O_X)	-0.1			-0.1			mA	$V_{OUT} = V_{CC}$ -.5
	I_{OH1}	HIGH (all other outputs)	-1.0			-1.0			mA	V_{OUT} = 2.5V
	I_{OH2}	CURRENT (all other outputs)	-0.3			-0.3			mA	$V_{OUT} = V_{CC}$ -.5
	I_{OLX}	OUTPUT (O_X)	0.1			0.1			mA	V_{OUT} = .4V
	I_{OL}	LOW CURRENT (all other outputs)	1.6			1.6			mA	V_{OUT} = .4V
										Input at 0 or V_{DD} per Logic Function or Truth Table
	I_{CC}	SUPPLY CURRENT HD-4702			500			1500	µA	$\overline{E}_{CP} = V_{DD}$, CP = 0, All other inputs = GND
		HD-4702			150			1000	µA	$\overline{E}_{CP} = V_{DD}$, CP = 0, All other inputs = V_{DD}
		HD-6405			150			150	µA	$\overline{E}_{CP} = V_{DD}$, CP = 0, All other inputs = V_{DD} or GND
A.C.	t_{PLH} t_{PHL}	Propagation Delay, I_X to CO			300 250			300 250	ns ns	$C_L \leq 7pF$ on O_X
	t_{PLH} t_{PHL}	Propagation Delay, CP to CO			215 195			215 195	ns ns	C_L = 15pF Input Transition Times ≤ 20ns
	t_{PLH} t_{PHL}	Propagation Delay, CO to Q_n			⑤			⑤	ns ns	
	t_{PLH} t_{PHL}	Propagation Delay, CO to Z			75 65			75 65	ns ns	
	t_{TLH} t_{THL}	Output Transition Time (except O_X)			80 40			80 40	ns ns	
	t_{PLH} t_{PHL}	Propagation Delay, I_X to CO			350 275			350 275	ns ns	$C_L \leq 7pF$ on O_X
	t_{PLH} t_{PHL}	Propagation Delay, CP to CO			260 220			260 220	ns ns	C_L = 50pF Input Transition Times ≤ 20ns
	t_{PLH} t_{PHL}	Propagation Delay, CO to Q_n			⑤			⑤	ns ns	
	t_{PLH} t_{PHL}	Propagation Delay, CO to Z			85 75			85 75	ns ns	
	t_{TLH} t_{THL}	Output Transition Time (except O_X)			160 75			160 75	ns ns	
	t_s t_h	Set-Up Time, Select to CO Hold Time, Select to CO	350 0			350 0			ns ns	$C_L \leq 7pF$ on O_X
	t_s t_h	Set-Up Time, I_M to CO Hold Time, I_M to CO	350 0			350 0			ns ns	C_L = 15pF Input Transition Times ≤ 20ns
	$t_{wCP(L)}$ $t_{wCP(H)}$	Minimum Clock Pulse-Width Low and High	120 120			120 120			ns ns	
	$t_{wCP(L)}$ $t_{wCP(H)}$	Minimum I_X Pulse Width, Low and High	160 160			160 160			ns ns	

1. Input Current and Quiescent Power Supply Current are relatively higher for this device because of active pull-up circuits on all inputs except I_X. This is done for TTL compatibility.
2. Propagation Delays (t_{PLH} and t_{PHL}) and Output Transistion Times (t_{TLH} and t_{THL}) will change with Output Load Capacitance (C_L). Set-Up Times (t_s), Hold Times (t_h), and Mininum Pulse Widths (t_w) do not vary with load capacitance.
3. The first High Level Clock Pulse after $\overline{E}_{CP}$ goes Low and must be at least 350ns long to guarantee reset of all Counters.
4. It is recommended that input rise and fall times to the Clock Inputs (CP, I_X) be less than 15ns.
5. For multichannel operation, Propagation Delay (CO to Q_n) plus Set-Up Time, Select to CO, is guaranteed to be ≤ 367ns.

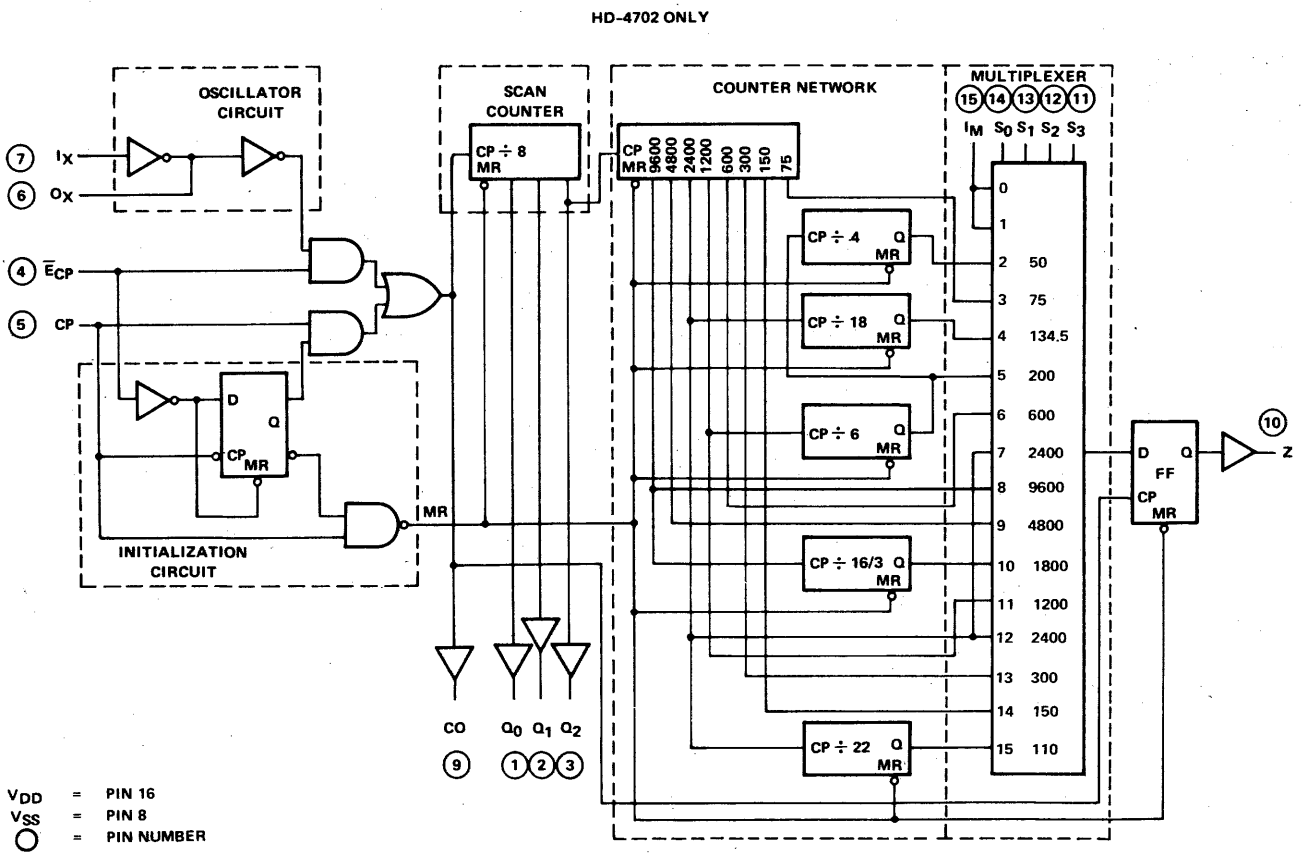
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Switching Waveforms



NOTE: Set-Up and Hold Times are shown as positive values but may be specified as negative values.

Block Diagram



HD4702/6405 PG 4

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HARRIS
SEMICONDUCTOR
PRODUCTS DIVISION
A DIVISION OF HARRIS CORPORATION

HD-6402

CMOS/LSI Universal Asynchronous Receiver Transmitter (UART)

Features

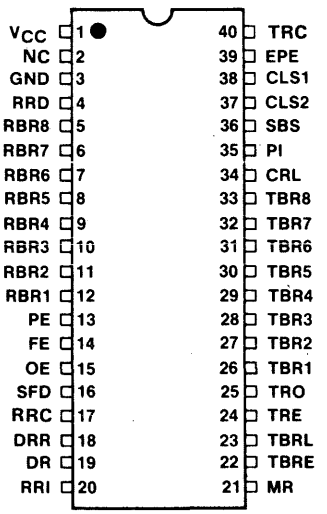
- OPERATION FROM D.C. TO 4.0MHz @10.0 VOLTS
- LOW POWER-TYR. 10mW @ 2.0MHz AND 5.0 VOLTS
- 4 TO 11 VOLT OPERATION
- PROGRAMMABLE WORD LENGTH, STOP BITS AND PARITY
- AUTOMATIC DATA FORMATTING AND STATUS GENERATION
- COMPATIBLE WITH INDUSTRY STANDARD UART'S
- SINGLE POWER SUPPLY

Description

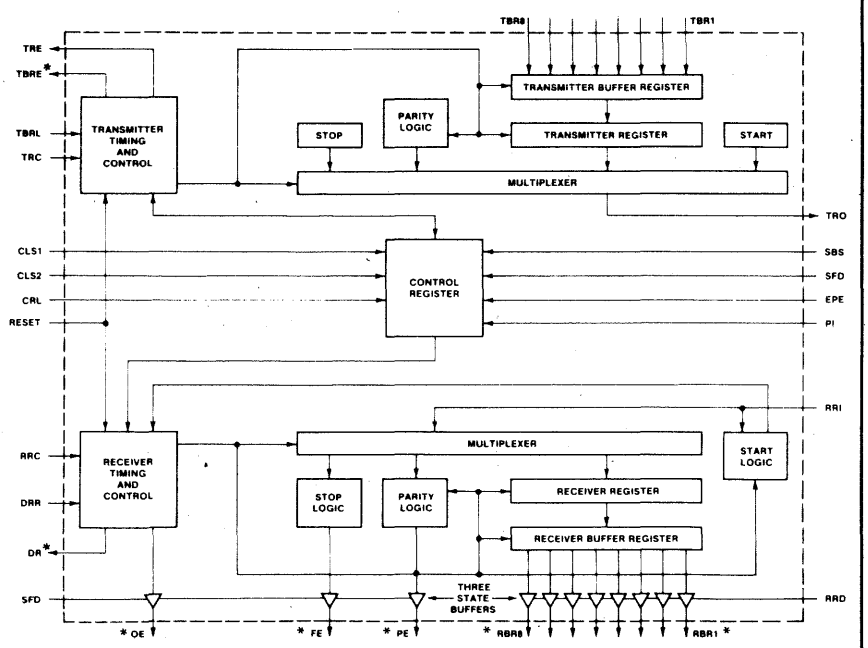
The HD-6402 is a CMOS/LSI subsystem for interfacing computers or microprocessors to an asynchronous serial data channel. The receiver converts serial start, data, parity and stop bits to parallel data verifying proper code transmission, parity, and stop bits. The transmitter converts parallel data into serial form and automatically adds start, parity, and stop bits. The data word length can be 5, 6, 7 or 8 bits. Parity may be odd or even. Parity checking and generation can be inhibited. The stop bits may be one or two or one and one-half when transmitting 5 bit code.

The HD-6402 can be used in a wide range of applications including modems, printers, peripherals and remote data aquisition systems. CMOS/LSI technology permits operation clock frequencies up to 4.0MHz (250K Baud) an improvement of 10 to 1 over previous PMOS UART designs. Power requirements, by comparison, are reduced from 300mW to 10mW. Status logic increases flexibility and simplifies the user interface.

Pinout



Functional Diagram



* These outputs are three state

Control Definition

CONTROL WORD					CHARACTER FORMAT			
CLS2	CLS1	PI	EPE	SBS	START BIT	DATA BITS	PARITY BIT	STOP BITS
0	0	0	0	0	1	5	ODD	1
0	0	0	0	1	1	5	ODD	1.5
0	0	0	1	0	1	5	EVEN	1
0	0	0	1	1	1	5	EVEN	1.5
0	0	1	X	0	1	5	NONE	1
0	0	1	X	1	1	5	NONE	1.5
0	1	0	0	0	1	6	ODD	1
0	1	0	0	1	1	6	ODD	2
0	1	0	1	0	1	6	EVEN	1
0	1	0	1	1	1	6	EVEN	2
0	1	1	X	0	1	6	NONE	1
0	1	1	X	1	1	6	NONE	2
1	0	0	0	0	1	7	ODD	1
1	0	0	0	1	1	7	ODD	2
1	0	0	1	0	1	7	EVEN	1
1	0	0	1	1	1	7	EVEN	2
1	0	1	X	0	1	7	NONE	1
1	0	1	X	1	1	7	NONE	2
1	1	0	0	0	1	8	ODD	1
1	1	0	0	1	1	8	ODD	2
1	1	0	1	0	1	8	EVEN	1
1	1	0	1	1	1	8	EVEN	2
1	1	1	X	0	1	8	NONE	1
1	1	1	X	1	1	8	NONE	2

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ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+12.0V
Input or Output Voltage Applied	GND -0.3V to VCC +0.3V
Storage Temperature Range	-65°C to 150°C
Operating Temperature Range	
Industrial HD-6402A-9	-40°C to +85°C
Military HD-6402A-2	-55°C to +125°C

ELECTRICAL CHARACTERISTICS

$V_{CC} = 10.0V \pm 0.5V$, T_A = Industrial or Military

D.C.

SYMBOL	PARAMETER	MINIMUM	TYPICAL	MAXIMUM	UNITS	CONDITIONS
V_{IH}	Logical "1" Input Voltage	70% V_{CC}			V	
V_{IL}	Logical "0" Input Voltage			20% V_{CC}	V	
I_{IL}	Input Leakage	-1.0		1.0	μA	$0V \leq V_{IN} \leq V_{CC}$
V_{OH}	Logical "1" Output Voltage*	V_{CC} -0.01			V	$I_{OUT} = 0$
V_{OL}	Logical "0" Output Voltage*			GND +0.01	V	$I_{OUT} = 0$
I_O	Output Leakage	-1.0		1.0	μA	$0V \leq V_O \leq V_{CC}$
I_{CC}	Supply Current		5.0	500	μA	$V_{CC} = 10.5V$, $V_{IN} = V_{CC}$ or GND
C_{IN}	Input Capacitance*		7.0	8.0	pF	
C_O	Output Capacitance*		6.0	10.0	pF	

*Guaranteed but not 100% tested.

A.C.

		$V_{CC} = 10.0V$ ① $T_A = 25°C$			$V_{CC} = 10V \pm 0.5V$ T_A = Industrial or Military				
SYMBOL	PARAMETER	MIN	TYP	MAX	MIN	TYP	MAX	UNITS	CONDITIONS
f_{clock}	Clock Frequency	D.C.		6.0	D.C.		4.0	MHz	
t_{pw}	Pulse Widths CRL, DRR, TBRL	75			100			ns	$C_L = 50pF$
t_{pw}	Pulse Width MR	350			400			ns	See Switching Time
t_{SET}	Input Data Setup Time	40			40			ns	Waveforms 1, 2, 3
t_{HOLD}	Input Data Hold Time	30			30			ns	
t_{pd}	Output Propagation Delays			50			70	ns	

NOTE 1: All devices guaranteed at worst case limits. Room temperature, 10V data provided for information-not guaranteed.

Switching Waveforms

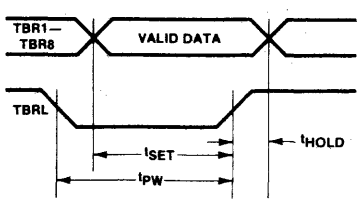


FIGURE 1
Data Input Cycle

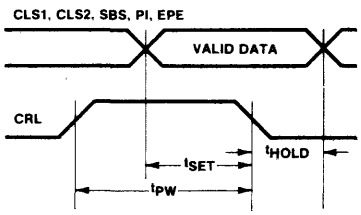


FIGURE 2
Control Register Load Cycle

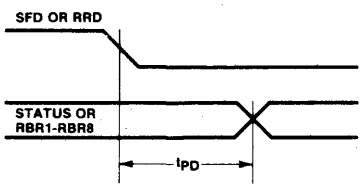


FIGURE 3
Status Flag Output Delays or Data Output Delays

HD 6402 PG 2

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ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+8.0V
Input or Output Voltage Applied	GND -0.3V to V_{CC} +0.3V
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	
Industrial HD-6402-9	-40°C to +85°C
Military HD-6402-2	-55°C to +125°C

ELECTRICAL CHARACTERISTICS

V_{CC} = 5.0V ± 10%. T_A = Industrial or Military

D.C.

SYMBOL	PARAMETER	MINIMUM	TYPICAL	MAXIMUM	UNITS	CONDITIONS
V_{IH}	Logical "1" Input Voltage	70% V_{CC}			V	
V_{IL}	Logical "0" Input Voltage			20% V_{CC}	V	
I_{IL}	Input Leakage	-1.0		1.0	μA	$0V \leq V_{IN} \leq V_{CC}$
V_{OH}	Logical "1" Output Voltage	2.4			V	$I_{OH} = -0.2mA$
V_{OL}	Logical "0" Output Voltage			0.45	V	$I_{OL} = 2.0mA$
I_O	Output Leakage	-1.0		1.0	μA	$0V \leq V_O \leq V_{CC}$
I_{CC}	Supply Current		1.0	100	μA	V_{IN} = GND or V_{CC}; V_{CC} = 5.5V, Output Open
C_{IN}	Input Capacitance*		7.0	8.0	pF	
C_O	Output Capacitance*		8.0	10.0	pF	

*Guaranteed but not 100% tested

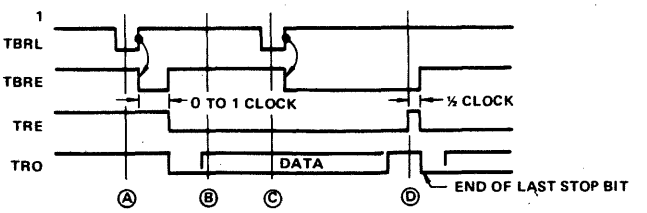
A.C.

		V_{CC} = 5.0V ① T_A = 25°C			V_{CC} = 5.0V ± 10% T_A = Indust. or Mil.				
SYMBOL	PARAMETER	MIN	TYP	MAX	MIN	TYP	MAX	UNITS	CONDITIONS
f_{clock}	Clock Frequency	D.C.		3.0	D.C.		2.0	MHz	
t_{pw}	Pulse Widths CRL, DRR, TBRL	150			150			ns	C_L = 50pF
t_{pw}	Pulse Width MR	350			400			ns	See Switching Time
t_{SET}	Input Data Setup Time	50			50			ns	Waveforms 1, 2, 3
t_{HOLD}	Input Data Hold Time	60			60			ns	
t_{pd}	Output Propagation Delays			125			160	ns	

NOTE 1: All devices guaranteed at worst case limits. Room temperature, 5V data provided for information-not guaranteed.

Transmitter Operation

The transmitter section accepts parallel data, formats it and transmits it in serial form on the TROutput terminal. Ⓐ Data is loaded into the transmitter buffer register from the inputs TR1 through TR8 by a logic low on the TBRLoad input. Valid data must be present at least t_{SET} prior to and t_{HOLD} following the rising edge of TBRL. If words less than 8 bits are used, only the least significant bits are used. The character is right justified into the least significant bit, TR1. Ⓑ The rising edge of TBRL clears TBREmpty. 0 to 1 clock cycles later, data is transferred to the transmitter register; TREmpty is cleared; TBR-Empty is set high; and serial data transmission is started. Output data is clocked by TRClock. The clock rate is 16 times the data rate. Ⓒ A second pulse on TBRLoad loads data into the transmitter buffer register. Data transfer to the transmitter register is delayed until transmission of the current character is complete. Ⓓ Data is automatically transferred to the transmitter register and transmission of that character begins one clock cycle later.



TRANSMITTER TIMING (NOT TO SCALE)

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ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+8.0V
Input or Output Voltage Applied	GND -0.3V to V_{CC} +0.3V
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range (Industrial -9)	-40°C to +85°C

ELECTRICAL CHARACTERISTICS $V_{CC} = 5.0V \pm 5\%$. T_A = Industrial

	SYMBOL	PARAMETER	MINIMUM	TYPICAL	MAXIMUM	UNITS	CONDITIONS
D.C.	V_{IH}	Logical "1" Input Voltage	V_{CC} -2.0			V	
	V_{IL}	Logical "0" Input Voltage			0.8	V	
	I_{IL}	Input Leakage	-10.0		+10.0	μA	$0V \leq V_{IN} \leq V_{CC}$
	V_{OH}	Logical "1" Output Voltage	2.4			V	I_{OH} = -0.2mA
	V_{OL}	Logical "0" Output Voltage			0.45	V	I_{OL} = 2.0mA
	I_O	Output Leakage	-10.0		+10.0	μA	$0V \leq V_O \leq V_{CC}$
	I_{CC}	Supply Current		1.0	800	μA	V_{IN} = GND or V_{CC}, V_{CC} = 5.25V, Output Open
	C_{IN}	Input Capacitance*		7.0	8.0	pF	
	C_O	Output Capacitance*		8.0	10.0	pF	

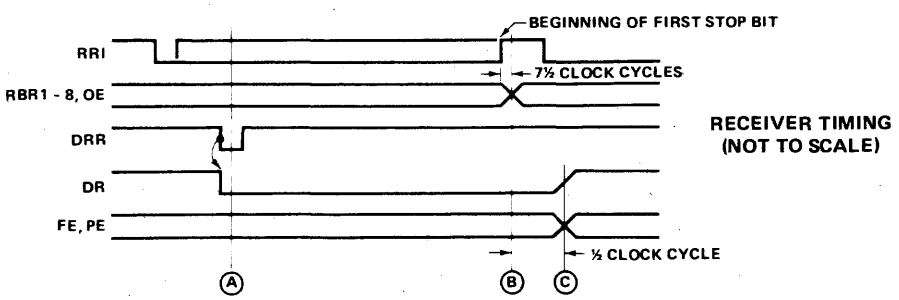
*Guaranteed but not 100% tested.

		V_{CC} = 5.0V ① T_A = 25°C			V_{CC} = 5.0V ± 5% T_A = Industrial				
SYMBOL	PARAMETER	MIN	TYP	MAX	MIN	TYP	MAX	UNITS	CONDITIONS
A.C.	f_{clock} Clock Frequency	D.C.		2.0	D.C.		1.0	MHz	
	t_{pw} Pulse Widths CRL, DRR, TBRL	200			225			ns	C_L = 50pF
	t_{pw} Pulse Width MR	500			600			ns	See Switching Time
	t_{SET} Input Data Setup Time	60			75			ns	Waveforms 1, 2, 3
	t_{HOLD} Input Data Hold Time	75			90			ns	
	t_{pd} Output Propagation Delays			150			190	ns	

NOTE 1: All devices guaranteed at worst case limits. Room temperature, 5V data provided for information-not guaranteed.

Receiver Operation

Data is received in serial form at the RInput. When no data is being received, RInput must remain high. The data is clocked through the RRClock. The clock rate is 16 times the data rate. Ⓐ A low level on DRReset clears the DReady line. Ⓑ During the first stop bit data is transferred from the receiver register to the RBRegister. If the word is less than 8 bits, the unused most significant bits will be a logic low. The output character is right justified to the least significant bit RBR1. A logic high on OError indicates overruns. An overrun occurs when DReady has not been cleared before the present character was transferred to the RBRegister. Ⓒ ½ clock cycle later DReady is reset to a logic high, PError and FError are evaluated. A logic high on FError indicates an invalid stop bit was received, a framing error. A logic high on PError indicates a parity error.



RECEIVER TIMING (NOT TO SCALE)

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8048/8648/8748/8035

SINGLE COMPONENT 8-BIT MICROCOMPUTER

- 8048 Mask Programmable ROM
- 8648 One-Time Factory Programmable EPROM
- 8748 User Programmable/Erasable EPROM
- 8035 External ROM or EPROM

- 8-Bit CPU, ROM, RAM, I/O in Single Package
- Interchangeable ROM and EPROM Versions
- Single 5V Supply
- 2.5 μsec and 5.0 μsec Cycle Versions: All Instructions 1 or 2 Cycles
- Over 90 Instructions: 70% Single Byte
- 1K x 8 ROM/EPROM
  64 x 8 RAM
  27 I/O Lines
- Interval Timer/Event Counter
- Easily Expandable Memory and I/O
- Compatible with 8000 Series Peripherals
- Single Level Interrupt

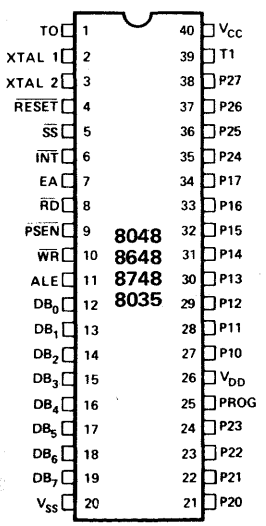
The Intel® 8048/8648/8748/8035 is a totally self-sufficient 8-bit parallel computer fabricated on a single silicon chip using Intel's N-channel silicon gate MOS process.

The 8048 contains a 1K x 8 program memory, a 64 x 8 RAM data memory, 27 I/O lines, and an 8-bit timer/counter in addition to onboard oscillator and clock circuits. For systems that require extra capability, the 8048 can be expanded using standard memories and MCS-80™ (8080A) peripherals. The 8035 is the equivalent of an 8048 without program memory. The 8035L has the RAM power down mode of the 8048 while the 8035 does not.

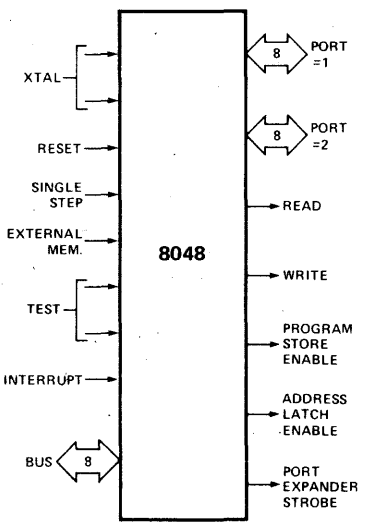
To reduce development problems to a minimum and provide maximum flexibility, three interchangeable pin-compatible versions of this single component microcomputer exist: the 8748 with user-programmable and erasable EPROM program memory for prototype and preproduction systems, the 8048 with factory-programmed mask ROM program memory for low cost, high volume production, and the 8035 without program memory for use with external program memories.

This microprocessor is designed to be an efficient controller as well as an arithmetic processor. The 8048 has extensive bit handling capability as well as facilities for both binary and BCD arithmetic. Efficient use of program memory results from an instruction set consisting mostly of single byte instructions and no instructions over 2 bytes in length.

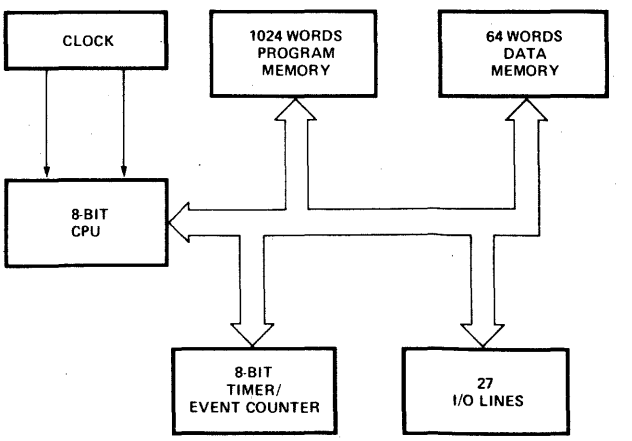
PIN CONFIGURATION



LOGIC SYMBOL



BLOCK DIAGRAM



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NEW HIGH PERFORMANCE 8049/8039/8039-6 SINGLE COMPONENT 8-BIT MICROCOMPUTER

*8049 Mask Programmable ROM
*8039 External ROM or EPROM
*New 11 MHz Operation

- 8-Bit CPU, ROM, RAM, I/O in Single Package
- Single 5V ± 10% Supply
- 1.36 μsec Cycle; All Instructions 1 or 2 Cycles
- Over 90 Instructions: 70% Single Byte
- Pin Compatible with 8048/8748
- 2K x 8 ROM
  128 x 8 RAM
  27 I/O Lines
- Interval Timer/Event Counter
- Easily Expandable Memory and I/O
- Compatible with MCS Memory and I/O
- Single Level Interrupt

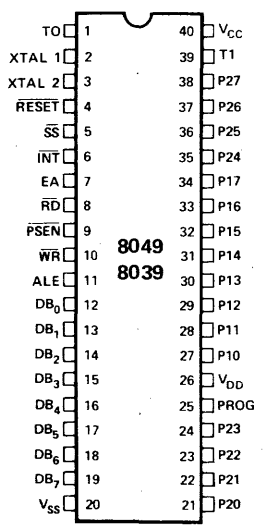
The Intel® 8049/8039/8039-6 is a totally self-sufficient 8-bit parallel computer fabricated on a single silicon chip using Intel's N-channel silicon gate MOS process.

The 8049 contains a 2K x 8 program memory, a 128 x 8 RAM data memory, 27 I/O lines, and an 8-bit timer/counter in addition to on board oscillator and clock circuits. For systems that require extra capability, the 8049 can be expanded using standard memories and MCS-80™/MCS-85™ peripherals. The 8039 is the equivalent to an 8049 without program memory. The 8039-6 is a lower speed (6MHz) version of the 8039.

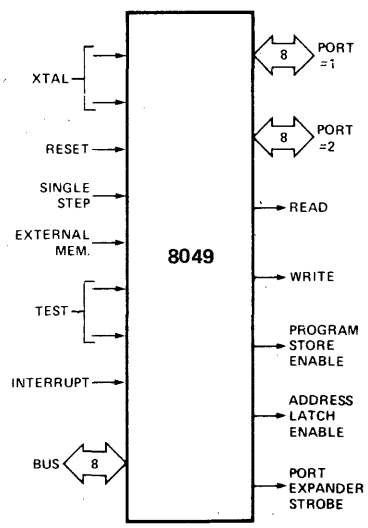
To reduce development problems to a minimum and provide maximum flexibility, two interchangeable pin-compatible versions of this single component microcomputer exist: the 8049 with factory-programmed mask ROM program memory for low-cost high volume production, and the 8039 without program memory for use with external program memories in prototype and preproduction systems.

This microprocessor is designed to be an efficient controller as well as an arithmetic processor. The 8049 has extensive bit handling capability as well as facilities for both binary and BCD arithmetic. Efficient use of program memory results from an instruction set consisting mostly of single byte instructions and no instructions over two bytes in length.

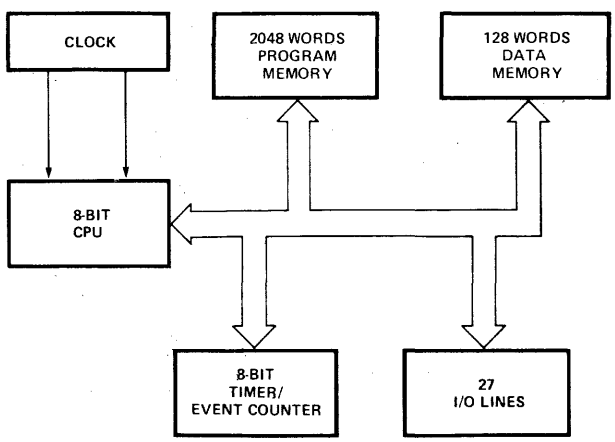
PIN CONFIGURATION



LOGIC SYMBOL



BLOCK DIAGRAM



Intel MICROPROCESSOR

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8021
SINGLE COMPONENT 8-BIT MICROCOMPUTER

- 8-Bit CPU, ROM, RAM, I/O in Single 28-Pin Package
- Single 5V Supply (+4.5V to 6.5V)
- 10 μsec Cycle; All Instructions 1 or 2 Cycles
- Instructions —8748 Subset
- High Current Drive Capability—2 Pins
- 1K × 8 ROM
  64 × 8 RAM
  21 I/O Lines
- Interval Timer/Event Counter
- Clock Generated With Single Resistor or Inductor
- Zero-Cross Detection Capability
- Easily Expandable I/O

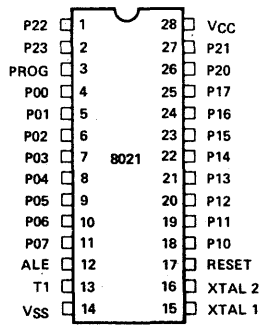
The Intel® 8021 is a totally self-sufficient 8-bit parallel computer fabricated on a single silicon chip using Intel's N-channel silicon gate MOS process. The features of the 8021 include a subset of the 8048 optimized for low cost, high volume applications, plus additional I/O flexibility and power.

The 8021 contains a 1K X 8 program memory, a 64 X 8 data memory, 21 I/O lines, and an 8-bit timer/event counter, in addition to on-board oscillator and clock circuits. For systems that require extra I/O capability, the 8021 can be expanded using the 8243 or discrete logic.

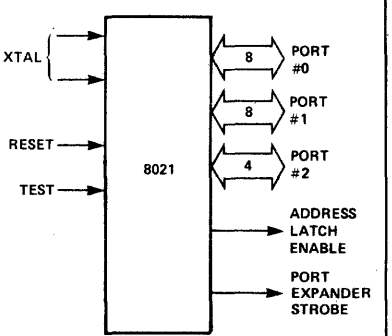
This microprocessor is designed to be an efficient controller as well as an arithmetic processor. The 8021 has bit handling capability as well as facilities for both binary and BCD arithmetic. Efficient use of program memory results from an instruction set consisting mostly of single byte instructions and no instructions over two bytes in length.

To minimize development problems and maximize flexibility, an 8021 system can be easily designed using the 8021 emulation board, EMB-21. The EMB-21 contains a 40-pin socket which can accommodate either the 8748 shipped with the board or an ICE-48 plug. Also, the necessary discrete logic to reproduce the 8021's additional I/O features is included.

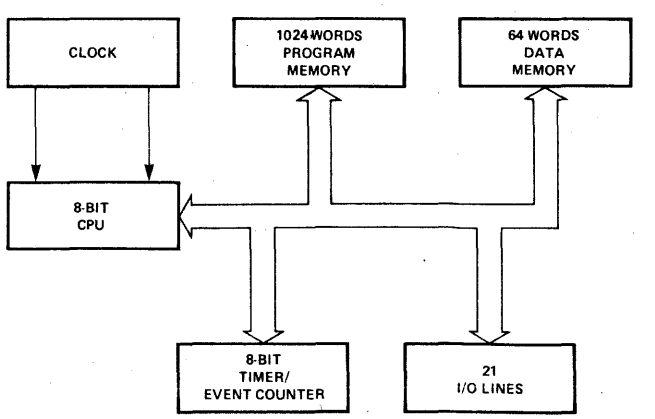
PIN CONFIGURATION



LOGIC SYMBOL



BLOCK DIAGRAM



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8022

SINGLE COMPONENT 8-BIT MICROCOMPUTER WITH ON-CHIP A/D CONVERTER

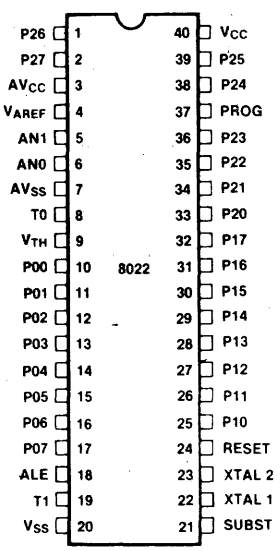
- 8-Bit CPU, ROM, RAM, I/O in Single 40-Pin Package
- On-Chip 8-Bit A/D Converter; Two Input Channels
- 8 Comparator Inputs (Port 0)
- Zero-Cross Detection Capability
- Single 5V Supply (4.5V to 6.5V)
- High Current Drive Capability — 2 Pins
- Two Interrupts — External and Timer
- 2K × 8 ROM, 64 × 8 RAM, 28 I/O Lines
- 10 μsec Cycle; All Instructions 1 or 2 Cycles
- Instructions — 8048 Subset
- Interval Timer/Event Counter
- Clock Generated with Single Resistor, Inductor, or Crystal
- Easily Expandable I/O

The Intel® 8022 is the newest member of the MCS-48™ family of single chip 8-bit microcomputers. It is designed to satisfy the requirements of low cost, high volume applications which involve analog signals, capacitive touchpanel keyboards, and/or large ROM space. The 8022 addresses these applications by integrating many new functions on-chip, such as A/D conversion, comparator inputs and zero-cross detection.

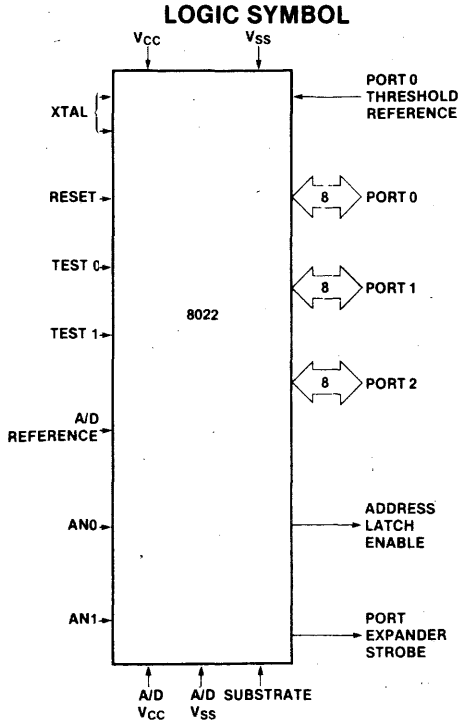
The features of the 8022 include 2K bytes of program memory (ROM), 64 bytes of data memory (RAM), 28 I/O lines, an on-chip 8-bit A/D converter with two input channels, an 8-bit port with comparator inputs for interfacing to low voltage capacitive touchpanels or other non-TTL interfaces, external and timer interrupts, and zero-cross detection capability. In addition, it contains the 8-bit interval timer/event counter, on-board oscillator and clock circuitry, single 5V power supply requirement, and easily expandable I/O structure common to all members of the MCS-48 family.

The 8022 is designed to be an efficient controller as well as an arithmetic processor. It has bit handling capability plus facilities for both binary and BCD arithmetic. Efficient use of program memory results from using the MCS-48 instruction set which consists mostly of single byte instructions and has extensive conditional jump and direct table lookup capability. Program memory usage is further reduced via the 8022's hardware implementation of the A/D converter which simplifies interfacing to analog signals.

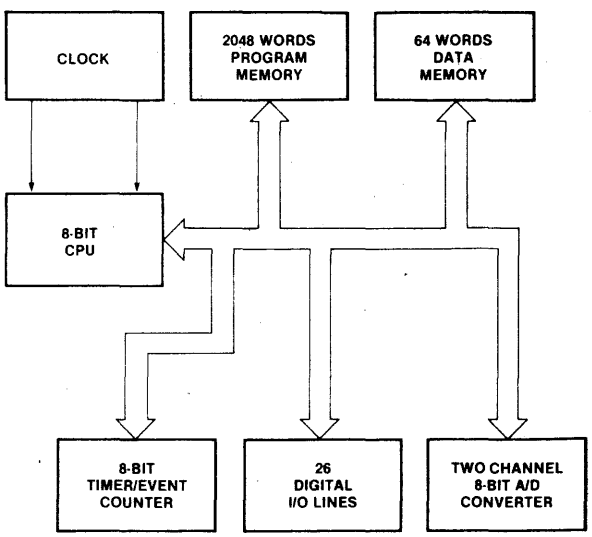
PIN CONFIGURATION



LOGIC SYMBOL



BLOCK DIAGRAM



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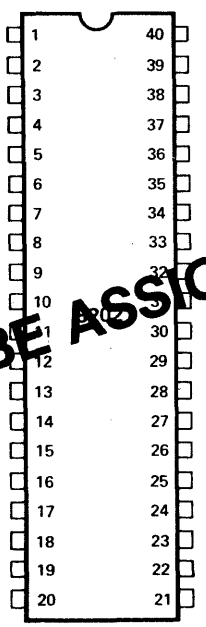
ADVANCE INFORMATION
Characteristics are subject to change without notice.

8202
DYNAMIC RAM CONTROLLER

- **Provides All Signals Necessary to Control 2104A, 2116, or 2117 Dynamic Memories**
- **Directly Addresses and Drives Up to 64K Bytes Without External Drivers**
- **Provides Address Multiplexing and Strobes**
- **Provides a Refresh Timer and a Refresh Counter**
- **Refresh Cycles May be Internally or Externally Requested**
- **Provides High Speed Refresh/Memory Access Request Arbitration**
- **Provides Transparent Refresh Capability**
- **Fully Compatible with Intel® 8080A and 8085A Microprocessors**
- **Decodes 8085A Status for Advanced Read Capability**
- **Provides System Acknowledge and Transfer Acknowledge Signals**
- **Internal or External Clock Capability**

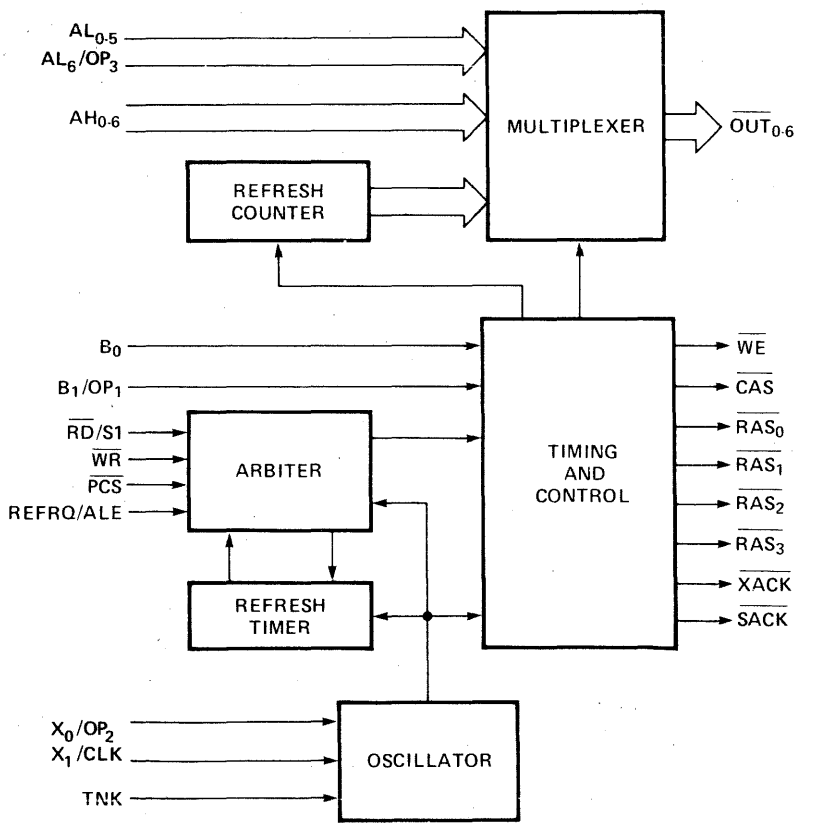
The 8202 is a Dynamic RAM System Controller designed to provide all signals necessary to use 2104A, 2116, or 2117 Dynamic RAMs in microcomputer systems. The 8202 provides multiplexed addresses and address strobes, as well as refresh/access arbitration. Refresh cycles can be started internally or externally.

PIN CONFIGURATION



TO BE ASSIGNED

8202 BLOCK DIAGRAM



MICROPROCESSOR Intel

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8041/8741
UNIVERSAL PERIPHERAL INTERFACE
8-BIT MICROCOMPUTER

- **Fully Compatibnle with MCS-80™, MCS-85™ and MCS-48™ Microprocessor Families**
- **Single Level Interrupt**
- **8-Bit CPU plus ROM, RAM, I/O, Timer and Clock in a Single Package**
- **Single 5V Supply**
- **Alternative to Custom LSI**
- **Pin Compatible ROM and EPROM Versions**
- **1K × 8 ROM/EPROM, 64 × 8 RAM, 18 Programmable I/O Pins**
- **Asynchronous Data Register for Interface to Master Processor**
- **Expandable I/O**

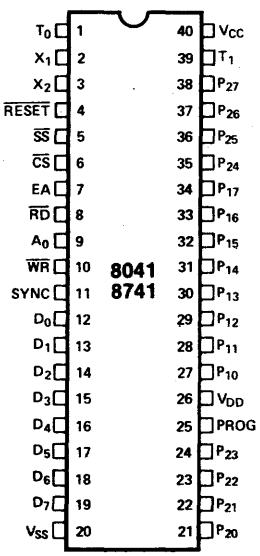
The Intel® 8041/8741 is a general purpose, programmable interface device designed for use with a variety of 8-bit microprocessor systems. It contains a low cost microcomputer with program memory, data memory, 8-bit CPU, I/O ports, timer/counter, and clock in a single 40-pin package. Interface registers are included to enable the UPI device to function as a peripheral controller in MCS-80™, MCS-85™, MCS-48™, and other 8-bit systems.

The UPI-41™ has 1K words of program memory and 64 words of data memory on-chip. To allow full user flexibility the program memory is available as ROM in the 8041 version or as UV-erasable EPROM in the 8741 version. The 8741 and the 8041 are fully pin compatible for easy transition from prototype to production level designs.

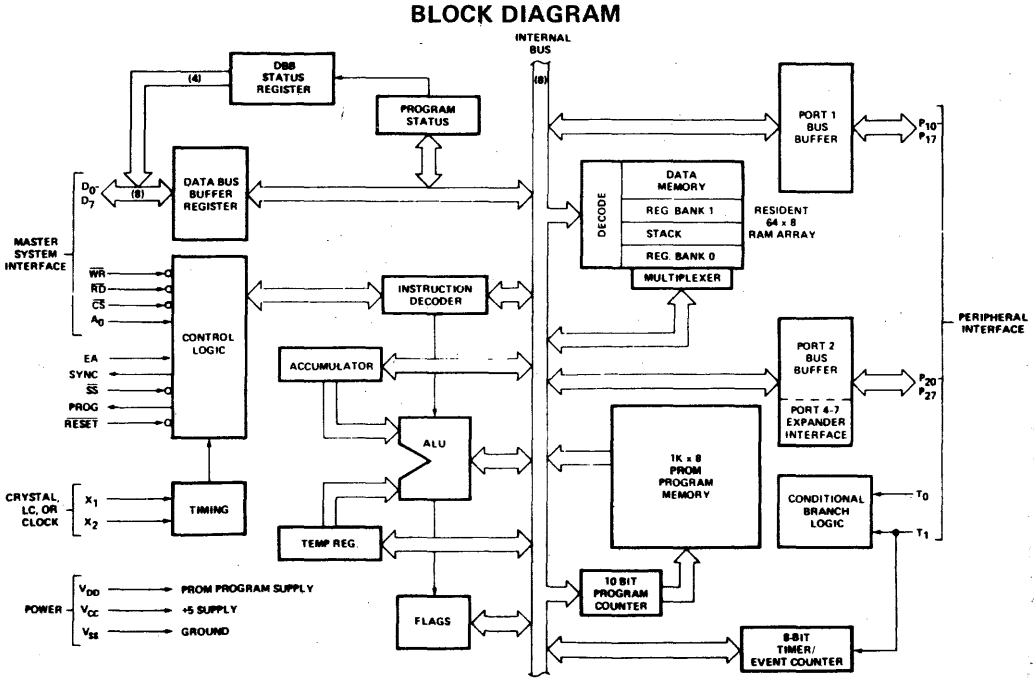
The device has two 8-bit, TTL compatible I/O ports and two test inputs. Individual port lines can function as either inputs or outputs under software control. I/O can be expanded with the 8243 device which is directly compatible and has 16 I/O lines. An 8-bit programmable timer/counter is included in the UPI device for generating timing sequences or counting external inputs. Additional UPI features include: single 5V supply, low power standby mode (in the 8041), single-step mode for debug (in the 8741), single level interrupt, and dual working register banks.

Because it's a complete microcomputer, the UPI provides more flexibility for the designer than conventional LSI interface devices. It is designed to be an efficient controller as well as an arithmetic processor. Applications include keyboard scanning, printer control, display multiplexing and similar functions which involve interfacing peripheral devices to microprocessor systems.

PIN CONFIGURATION



BLOCK DIAGRAM



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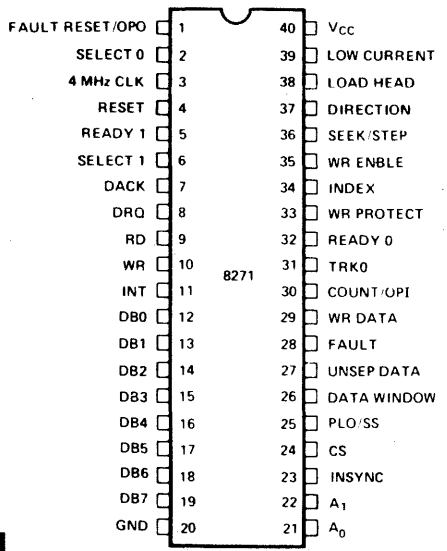
PRELIMINARY
Notice: This is not a final specification. Some parametric limits are subject to change.

8271
PROGRAMMABLE FLOPPY DISK CONTROLLER

- **IBM 3740 Soft Sectored Format Compatible**
- **Programmable Record Lengths**
- **Multi-Sector Capability**
- **Maintain Dual Drives with Minimum Software Overhead Expandable to 4 Drives**
- **Automatic Read/Write Head Positioning and Verification**
- **Internal CRC Generation and Checking**
- **Programmable Step Rate, Settle-Time, Head Load Time, Head Unload Index Count**
- **Fully MCS-80 and MCS-85 Compatible**
- **Single +5V Supply**
- **40-Pin Package**

The Intel® 8271 Programmable Floppy Disk Controller (FDC) is an LSI component designed to interface one to 4 floppy disk drives to an 8-bit microcomputer system. Its powerful control functions minimize both hardware and software overhead normally associated with floppy disk controllers.

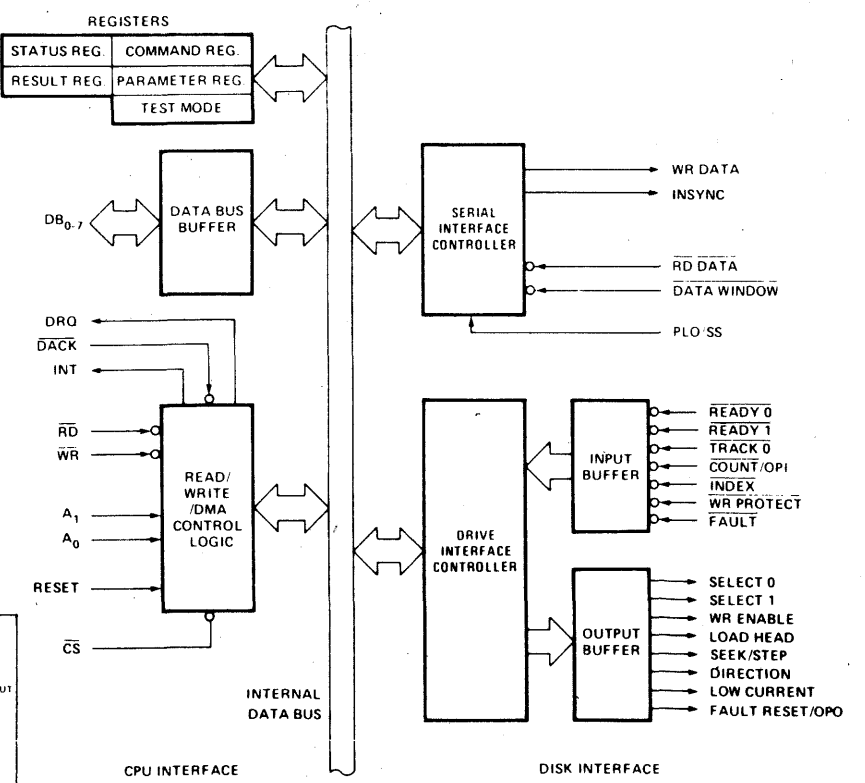
PIN CONFIGURATION



PIN NAMES

$DB_7 - DB_0$	DATA BUS (BI DIRECTIONAL)	PLO/SS	PLO/SINGLE SHOT
CLK	CLOCK INPUT (TTL)	DATA WINDOW	DATA WINDOW
SELECT 1, 0	SELECT 1, 0	UNSEP DATA	UNSEPARATED DATA
FAULT RESET/OPO	FAULT RESET/OPTIONAL OUTPUT	FAULT	FAULT
RESET	CHIP RESET	WR DATA	WRITE DATA
READY 1, 0	READY 1, 0	COUNT/OPI	COUNT/OPTIONAL INPUT
DACK	DMA ACKNOWLEDGE	TRK 0	TRACK 0
DRQ	DMA REQUEST	WR PROTECT	WRITE PROTECT
RD	CPU READ INPUT	INDEX	INDEX
WR	CPU WRITE INPUT	WR ENABLE	WRITE ENABLE
INT	INTERRUPT	SEEK/STEP	SEEK/STEP
$A_{1,0}$	REGISTER SELECT	DIRECTION	DIRECTION
INSYNC	READ DATA INSYNC	LOAD HEAD	LOAD HEAD
CS	CHIP SELECT	LOW CURRENT	LOW CURRENT

BLOCK DIAGRAM



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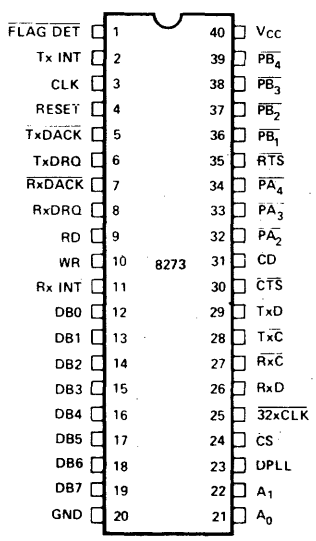
PRELIMINARY
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8273
PROGRAMMABLE HDLC/SDLC PROTOCOL CONTROLLER

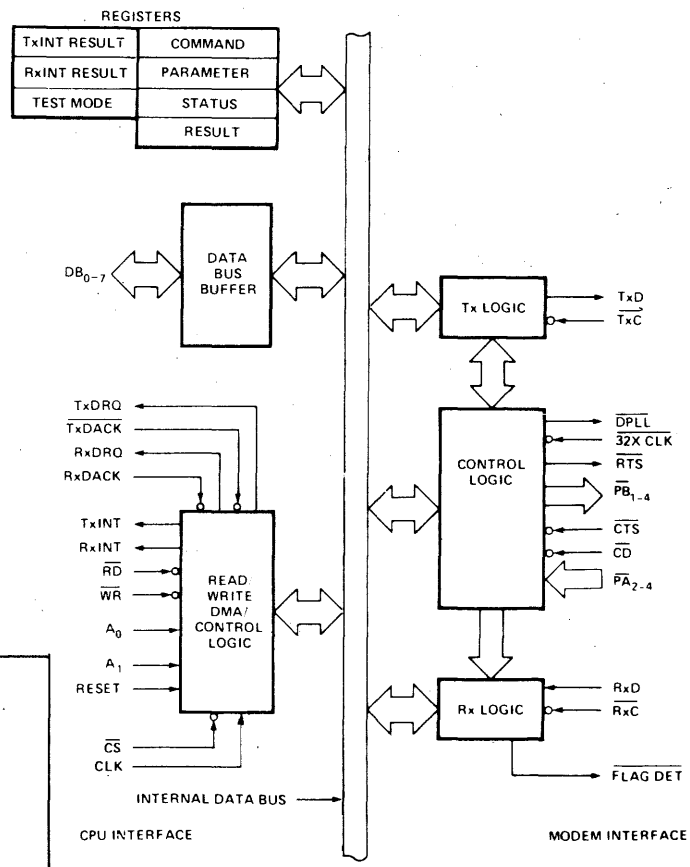
- **HDLC/SDLC Compatible**
- **Frame Level Commands**
- **Full Duplex, Half Duplex, or Loop SDLC Operation**
- **Up to 64K Baud Transfers**
- **Two User Programmable Modem Control Ports**
- **Automatic FCS (CRC) Generation and Checking**
- **Programmable NRZI Encode/Decode**
- **N-Bit Reception Capability**
- **Digital Phase Locked Loop Clock Recovery**
- **Minimum CPU Overhead**
- **Fully Compatible with 8080/8085 CPUs**
- **Single +5V Supply**
- **40-Pin Package**

The Intel® 8273 Programmable HDLC/SDLC Protocol Controller is a dedicated device designed to support the ISO/C-CITT's HDLC and IBM's SDLC communication line protocols. It is fully compatible with Intel's new high performance microcomputer systems such as the MCS-85™. A frame level command set is achieved by a unique microprogrammed dual processor chip architecture. The processing capability supported by the 8273 relieves the system CPU of the low level real-time tasks normally associated with controllers.

PIN CONFIGURATION



BLOCK DIAGRAM



PIN NAMES

DB0–DB7	DATA BUS (8 BITS)	$\overline{CS}$	CHIP SELECT
$\overline{FLAG\ DET}$	FLAG DETECT	$\overline{32xCLK}$	32 TIMES CLOCK
TxINT	TRANSMITTER INTERRUPT	Rx D	RECEIVER DATA
CLK	CLOCK INPUT	$\overline{Rx\ C}$	RECEIVER CLOCK
$\overline{RESET}$	RESET	$\overline{Tx\ C}$	TRANSMITTER CLOCK
$\overline{Tx\ DACK}$	TRANSMITTER DMA ACKNOWLEDGE	Tx D	TRANSMITTER DATA
TxDRQ	TRANSMITTER DMA REQUEST	$\overline{CTS}$	CLEAR TO SEND
$\overline{RD}$	READ INPUT	$\overline{CD}$	CARRIER DETECT
$\overline{WR}$	WRITE INPUT	$\overline{PA_2}$–$\overline{PA_4}$	GP INPUT PORTS
$\overline{Rx\ DACK}$	RECEIVER DMA ACKNOWLEDGE	$\overline{PB_1}$–$\overline{PB_4}$	GP OUTPUT PORTS
Rx DRQ	RECEIVER DMA REQUEST	$\overline{RTS}$	REQUEST TO SEND
Rx INT	RECEIVER INTERRUPT	V_{CC}	+5 VOLT SUPPLY
A0–A1	COMMAND REGISTER SELECT ADDRESS	GND	GROUND
$\overline{DPLL}$	DIGITAL PHASE LOCKED LOOP		

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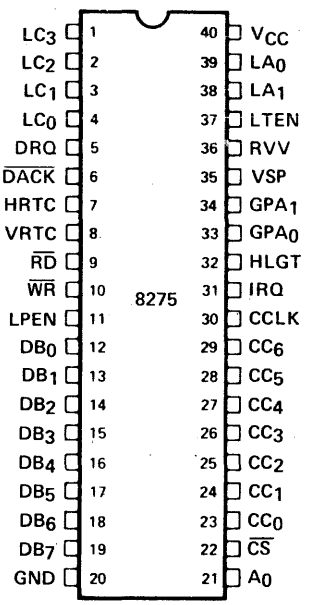
PRELIMINARY
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8275
PROGRAMMABLE CRT CONTROLLER

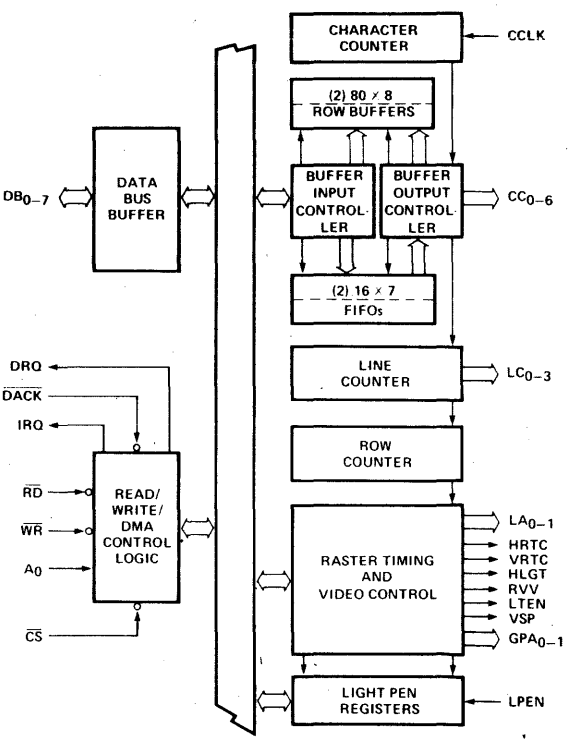
- **Programmable Screen and Character Format**
- **6 Independent Visual Field Attributes**
- **11 Visual Character Attributes (Graphic Capability)**
- **Cursor Control (4 Types)**
- **Light Pen Detection and Registers**
- **Fully MCS-80™ and MCS-85™ Compatible**
- **Dual Row Buffers**
- **Programmable DMA Burst Mode**
- **Single +5V Supply**
- **40-Pin Package**

The Intel® 8275 Programmable CRT Controller is a single chip device to interface CRT raster scan displays with Intel® microcomputer systems. Its primary function is to refresh the display by buffering the information from main memory and keeping track of the display position of the screen. The flexibility designed into the 8275 will allow simple interface to almost any raster scan CRT display with a minimum of external hardware and software overhead.

PIN CONFIGURATION



BLOCK DIAGRAM



PIN NAMES

DB0 1	BI DIRECTIONAL DATA BUS	LC0–3	LINE COUNTER OUTPUTS
DRQ	DMA REQUEST OUTPUT	LA0–1	LINE ATTRIBUTE OUTPUTS
DACK	DMA ACKNOWLEDGE INPUT	HRTC	HORIZONTAL RETRACE OUTPUT
IRQ	INTERRUPT REQUEST OUTPUT	VRTC	VERTICAL RETRACE OUTPUT
RD	READ STROBE INPUT	HLGT	HIGHLIGHT OUTPUT
WR	WRITE STROBE INPUT	RVV	REVERSE VIDEO OUTPUT
A0	REGISTER ADDRESS INPUT	LTEN	LIGHT ENABLE OUTPUT
CS	CHIP SELECT INPUT	VSP	VIDEO SUPPRESS OUTPUT
CCLK	CHARACTER CLOCK INPUT	GPA0–1	GENERAL PURPOSE ATTRIBUTE OUTPUTS
CC0 6	CHARACTER CODE OUTPUTS	LPEN	LIGHT PEN INPUT

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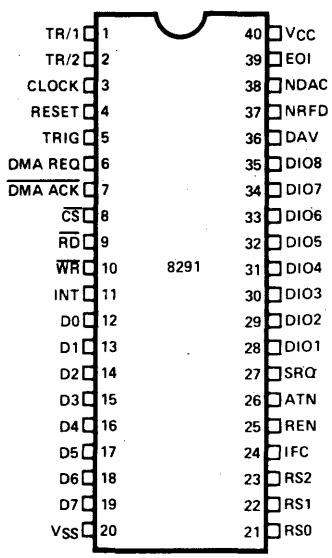
PRELIMINARY
Notice: This is not a final specification. Some parametric limits are subject to change.

8291
GPIB TALKER/LISTENER

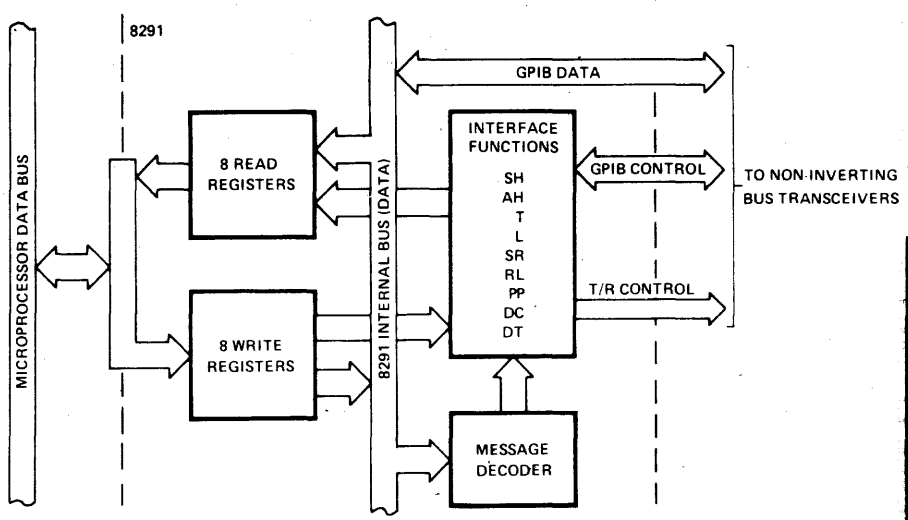
- Designed to Interface Microprocessors (e.g., 8080, 8085, 8086, 8048) to an IEEE Standard 488 Digital Interface Bus
- Programmable Data Transfer Rate
- Complete Source and Acceptor Handshake
- Complete Talker and Listener Functions with Extended Addressing
- Service Request, Parallel Poll, Device Clear, Device Trigger, Remote/Local Functions
- Selectable Interrupts
- On-Chip Primary and Secondary Address Recognition
- Automatic Handling of Addressing and Handshake Protocol
- Provision for Software Implementation of Additional Features
- 1-5 MHz Clock Range
- 16 Registers (8 Read, 8 Write), 2 for Data Transfer, the Rest for Interface Function Control, Status, etc.
- Directly Interfaces to External Non-Inverting Transceivers for Connection to the GPIB
- Provides Three Addressing Modes, Allowing the Chip to be Addressed Either as a Major or a Minor Talker/Listener with Primary or Secondary Addressing
- DMA Handshake Provision Allows for Bus Transfers without CPU Intervention
- Trigger Output Pin
- On-Chip EOS (End of Sequence) Message Recognition Facilitates Handling of Multi-Byte Transfers

The 8291 GPIB Talker/Listener is a microprocessor-controlled chip designed to interface microprocessors (e.g., 8080, 8085, 8086, 8048) to an IEEE Standard 488 Instrumentation Interface Bus. It implements all of the Standard's Talker/Listener interface functions.

PIN CONFIGURATION



BLOCK DIAGRAM



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8085A/8085A-2
SINGLE CHIP 8-BIT N-CHANNEL MICROPROCESSORS

- **Single +5V Power Supply**
- **100% Software Compatible with 8080A**
- **1.3 μs Instruction Cycle (8085A); 0.8 μs (8085A-2)**
- **On-Chip Clock Generator (with External Crystal, LC or RC Network)**
- **On-Chip System Controller; Advanced Cycle Status Information Available for Large System Control**
- **Four Vectored Interrupt Inputs (One is non-Maskable) Plus an 8080A-compatible interrupt**
- **Serial In/Serial Out Port**
- **Decimal, Binary and Double Precision Arithmetic**
- **Direct Addressing Capability to 64k Bytes of Memory**

The Intel® 8085A is a complete 8 bit parallel Central Processing Unit (CPU). Its instruction set is 100% software compatible with the 8080A microprocessor, and it is designed to improve the present 8080A's performance by higher system speed. Its high level of system integration allows a minimum system of three IC's [8085A (CPU), 8156 (RAM/IO) and 8355/8755A (ROM/PROM/IO)] while maintaining total system expandability. The 8085A-2 is a faster version of the 8085A.

The 8085A incorporates all of the features that the 8224 (clock generator) and 8228 (system controller) provided for the 8080A, thereby offering a high level of system integration.

The 8085A uses a multiplexed data bus. The address is split between the 8 bit address bus and the 8 bit data bus. The on-chip address latches of 8155/8156/8355/8755A memory products allow a direct interface with the 8085A.

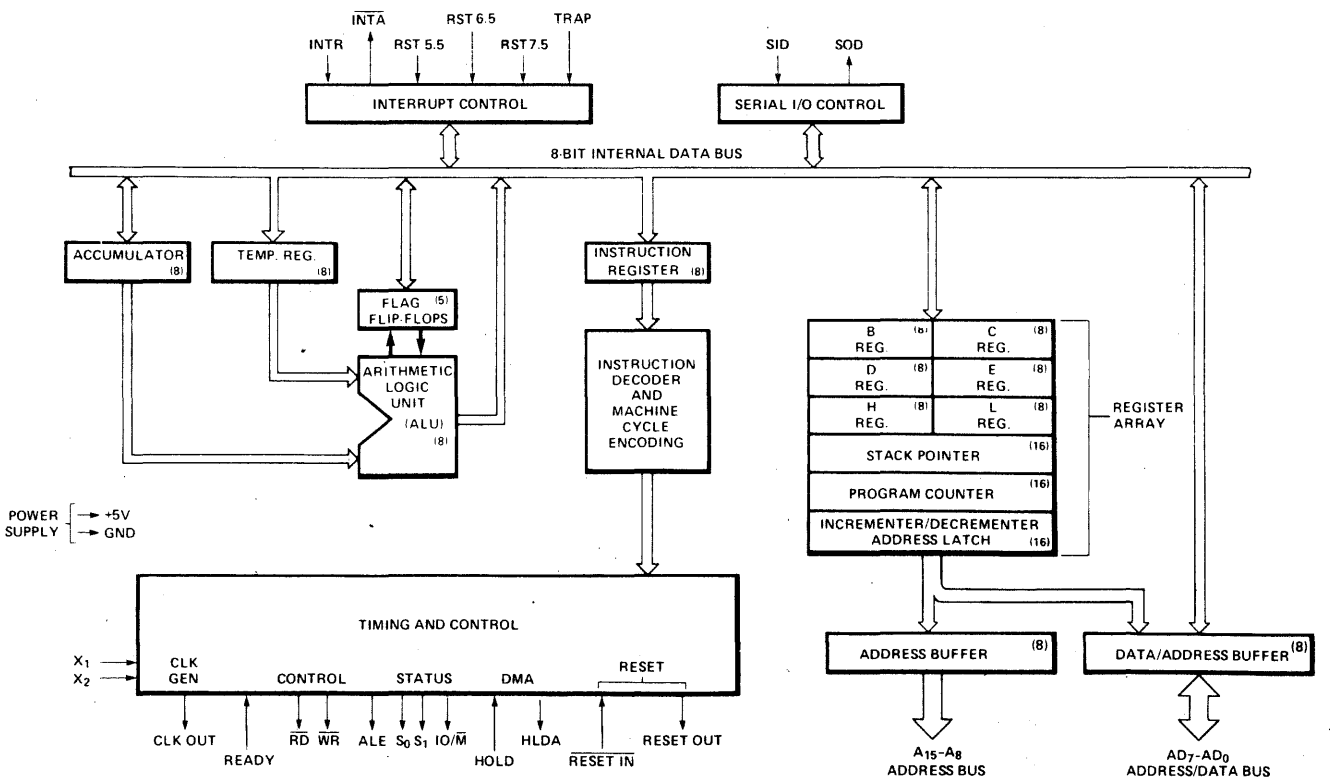


Figure 1. 8085A CPU Functional Block Diagram

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8155/8156/8155-2/8156-2
2048 BIT STATIC MOS RAM WITH I/O PORTS AND TIMER

8085A	8085A-2	Compatible CPU / Chip Enable
8155	8155-2	ACTIVE LOW
8156	8156-2	ACTIVE HIGH

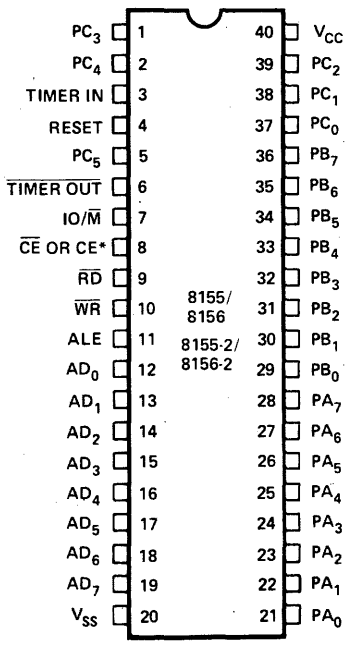
- 256 Word x 8 Bits
- Single +5V Power Supply
- Completely Static Operation
- Internal Address Latch
- 2 Programmable 8 Bit I/O Ports
- 1 Programmable 6-Bit I/O Port
- Programmable 14-Bit Binary Counter/ Timer
- Multiplexed Address and Data Bus
- 40 Pin DIP

The 8155 and 8156 are RAM and I/O chips to be used in the MCS-85™ microcomputer system. The RAM portion is designed with 2048 static cells organized as 256 x 8. They have a maximum access time of 400 ns to permit use with no wait states in 8085A CPU. The 8155-2 and 8156-2 have maximum access times of 330 ns for use with the 8085A-2.

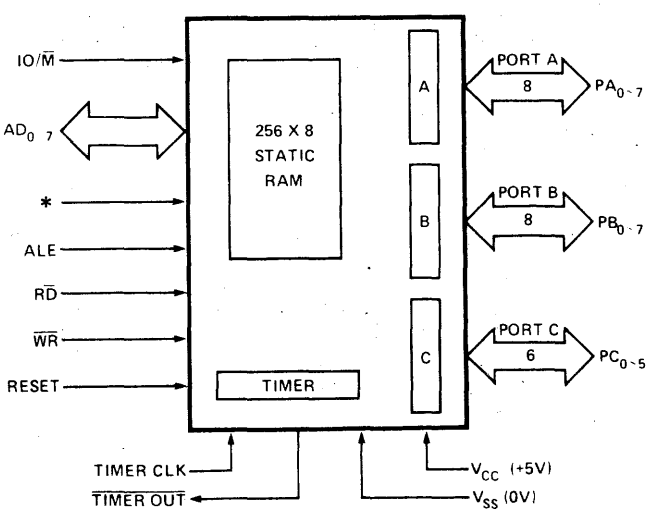
The I/O portion consists of three general purpose I/O ports. One of the three ports can be programmed to be status pins, thus allowing the other two ports to operate in handshake mode.

A 14-bit programmable counter/timer is also included on chip to provide either a square wave or terminal count pulse for the CPU system depending on timer mode.

PIN CONFIGURATION



BLOCK DIAGRAM



*: 8155/8155-2 = $\overline{CE}$, 8156/8156-2 = CE

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8755A*/8355*/8355-2**
16,384-BIT ROM WITH I/O

***Directly Compatible with 8085A CPU**

****Directly Compatible with 8085A-2**

- **2048 Words x 8 Bits**
- **Single +5V Power Supply**
- **Internal Address Latch**
- **2 General Purpose 8-Bit I/O Ports**
- **Each I/O Port Line Individually Programmable as Input or Output**
- **Multiplexed Address and Data Bus**
- **Pin Compatible ROM (8355, 8355-2) and EPROM (8755A) Versions**
- **40-Pin DIP**

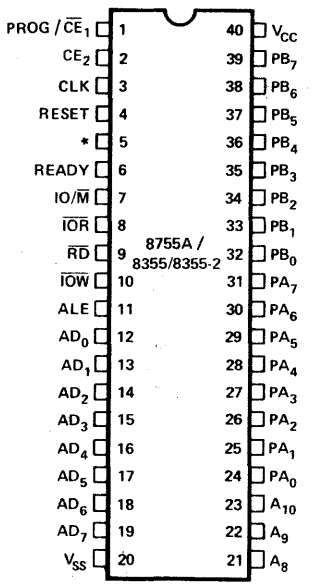
The Intel® 8755A is an erasable and electrically reprogrammable ROM (EPROM) and I/O chip to be used in the MCS-85™ microcomputer system. The EPROM portion is organized as 2048 words by 8 bits. It has a maximum access time of 450 ns to permit use with no wait states in an 8085A CPU.

The Intel® 8355 is a ROM and I/O chip to be used in the MCS-85™ microcomputer system. The ROM portion is organized as 2048 words by 8 bits. It has a maximum access time of 400 ns to permit use with no wait states in the 8085A CPU.

The I/O portion consists of 2 general purpose I/O ports. Each I/O port has 8 port lines, and each I/O port line is indivdually programmable as input or output.

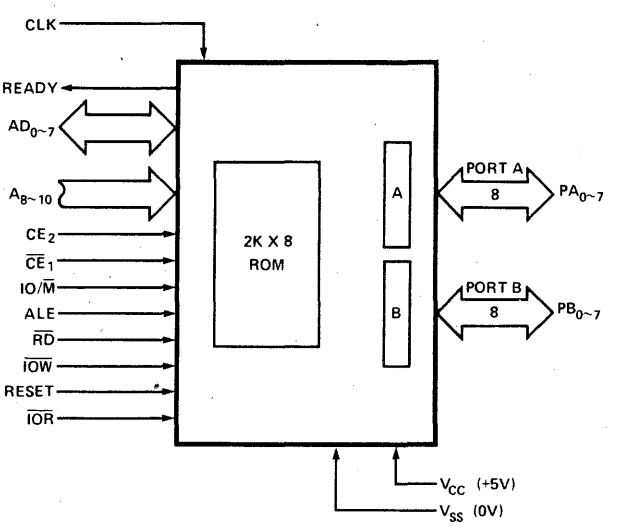
The 8355-2 has a 300ns access time for compatibility with the 8085A-2 microprocessor.

PIN CONFIGURATION



*8755A: V_{DD} (PROGRAMMING VOLTAGE)
8355: NO CONNECT

BLOCK DIAGRAM



Intel

MICROPROCESSOR

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8086
16-BIT HMOS MICROPROCESSOR

- **Direct Addressing Capability to 1 MByte of Memory**
- **Assembly Language Compatible with 8080/8085**
- **14 Word, By 16-Bit Register Set with Symmetrical Operations**
- **24 Operand Addressing Modes**
- **Bit, Byte, Word, and Block Operations**
- **8-and 16-Bit Signed and Unsigned Arithmetic in Binary or Decimal Including Multiply and Divide**
- **5 MHz Clock Rate**
- **MULTIBUS™ Compatible System Interface**

The Intel® 8086 is a new generation, high performance microprocessor implemented in N-channel, depletion load, silicon gate technology (HMOS), and packaged in a 40-pin CerDIP package. The processor has attributes of both 8- and 16-bit microprocessors. It addresses memory as a sequence of 8-bit bytes, but has a 16-bit wide physical path to memory for high performance.

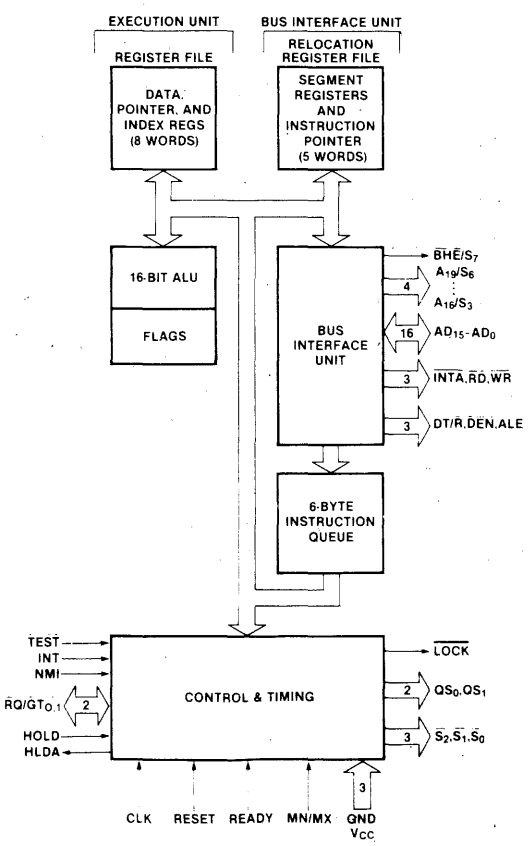
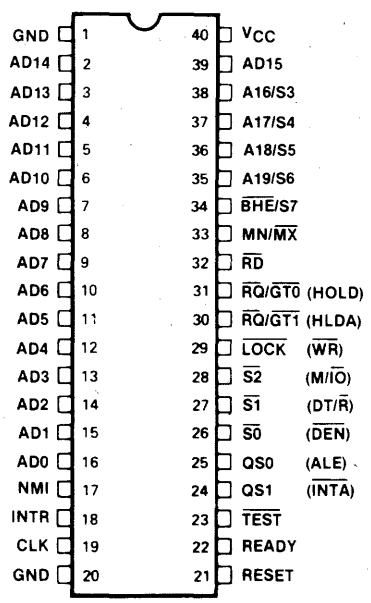


Figure 1. 8086 CPU Functional Block Diagram



40 LEAD

Figure 2. 8086 Pin Diagram

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8282/8283/8284/8286/8287/8288 BIPOLAR SYSTEM SUPPORT COMPONENTS FOR MCS-86

- **8282/8283: 8-Bit Latches (3-State, 8283 Inverting)**
- **8284: Clock Generator and Driver for 8080 CPU**
- **8286/8287: 8-Bit Parallel Bidirectional Bus Drivers (3-State, 8287 Inverting)**
- **8288: Bus Controller for 8086 CPU — Generates MULTIBUS™ Compatible Control Signals. Facilitates Interface of 8086 to a Multi-Master Bus.**

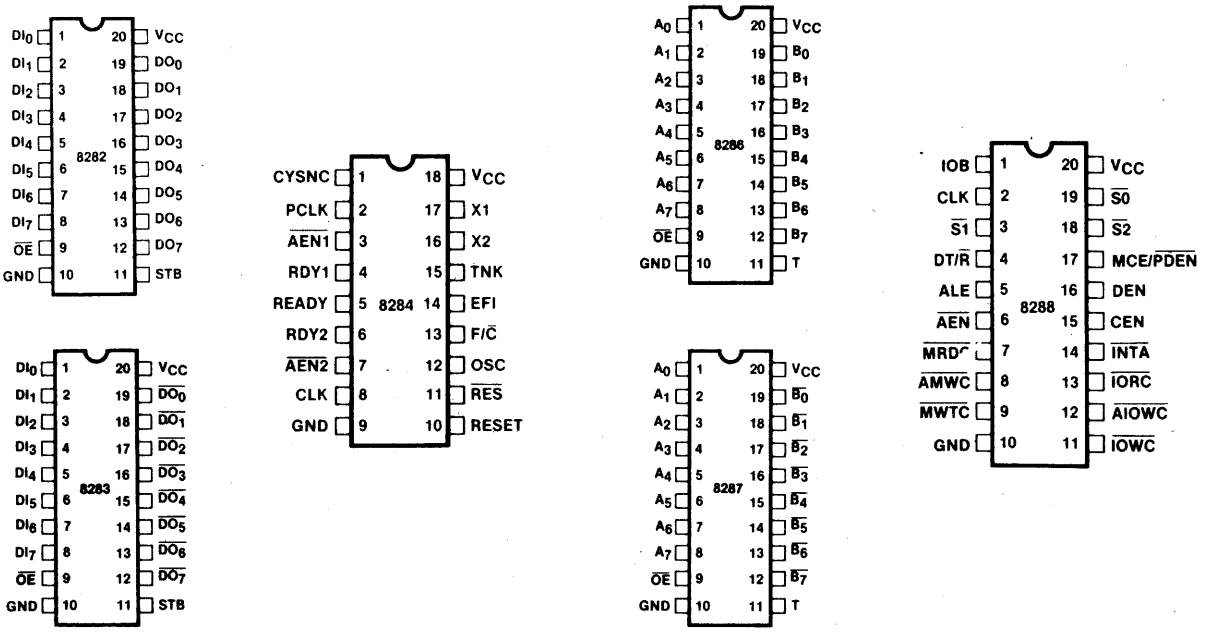
The 8282 and 8283 are 8-bit bipolar latches with 3-state output buffers. They can be used to implement latches, buffers, or multiplexers. The 8283 inverts the input data at its outputs while the 8282 does not. Thus, all of the principal peripheral and input/output functions of a microcomputer system can be implemented with these devices.

The 8284 is a bipolar clock generator/driver designed to provide clock signals for the 8086 CPU and peripherals. It also contains READY logic for operation with two MULTIBUS™ systems and provides the 8086's required READY synchronization and timing. Reset logic with hysteresis and synchronization is also provided.

The 8286 and 8287 are 8-bit bipolar transceivers with 3-state outputs. The 8287 inverts the input data at its outputs while the 8286 does not. Thus, a wide variety of applications for buffering in microcomputer systems can be met.

The Intel® 8288 Bus Controller is a 20-pin bipolar component for use with medium-to-large 8086 processing systems. The bus controller provides command and control timing generation as well as bipolar bus drive capability while optimizing system performance.

PIN CONFIGURATIONS



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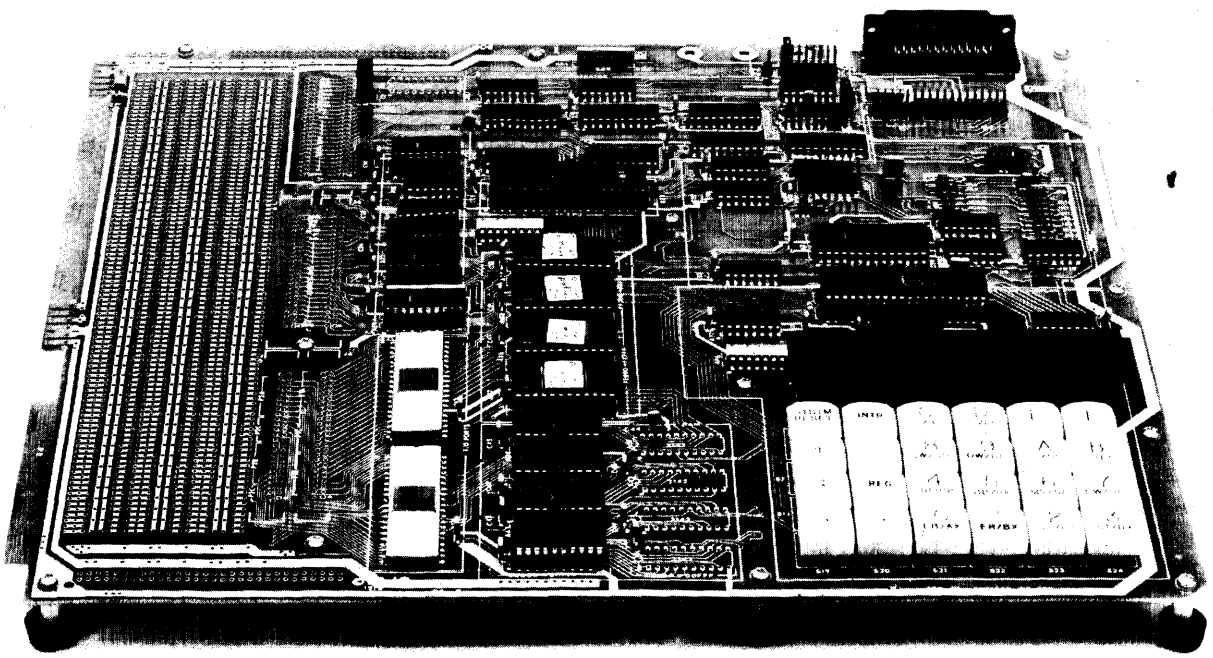
SDK-86
MCS-86™ SYSTEM DESIGN KIT

- **Complete Single Board Microcomputer System Including CPU, Memory and I/O**
- **Easy to Assemble Kit-Form**
- **High-Performance 8086 16-Bit CPU**
- **Interfaces Directly with TTY or CRT**
- **Interactive LED Display and Keyboard**
- **Wire-Wrap Area for Custom Interfaces**
- **Extensive System Monitor Software in ROM**
- **Comprehensive Design Library Included**

The MCS-86 System Design Kit (SDK-86) is a complete, single board 8086 microcomputer system in kit form. It contains all necessary components, including LED Display, Keyboard, resistors, caps, crystal and miscellaneous hardware to complete construction. Included are preprogrammed ROMs that contain the system monitor for general software utilities and system diagnostics.

The SDK-86 includes 8-digit LED display and a mnemonic 24-key keyboard for direct insertion, examination and execution of a user's program. In addition, it can be directly interfaced with a teletype terminal, CRT terminal, or the serial port of an Intellec® system.

The SDK-86 is a high-performance prototype system that has designed-in flexibility for simple interface to the user's application.



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MODEL 230
INTELLEC® SERIES II
MICROCOMPUTER DEVELOPMENT SYSTEM

Complete Microcomputer Development Center for Intel MCS-80™, MCS-85™ and MCS-48™ microprocessor families

Integral CRT with detachable upper/lower case "typewriter-style " full ASCII keyboard

64K bytes RAM memory

1 million bytes (expandable to 2.5M bytes) of diskette storage

LSI electronics board with CPU, RAM, ROM, I/O and interrupt circuitry

Built-in interfaces for High-Speed Paper Tape Reader/Punch, Printer and Universal PROM Programmer

Powerful ISIS-II Diskette Operating System Software with Relocating Macro Assembler, Linker and Locater

"Self-Test" Diagnostic capability

Standard MULTIBUS™ with multiprocessor and DMA capability

Eight-level nested, maskable priority interrupt system

Compatible with standard Intellec/iSBC Expansion Modules

Software compatible with previous Intellec Systems

Supports PL/M and FORTRAN high level languages

The Intellec Series II Model 230 Microcomputer Development System is a complete center for the development of microcomputer-based products. It includes a CPU, 64K bytes of RAM, 4K bytes of ROM memory, a 2000-character CRT, detachable full ASCII keyboard and dual double-density diskette drives providing over 1 million bytes of on-line data storage.

Powerful ISIS-II Diskette Operating System software allows the Model 230 to be used quickly and efficiently for assembly and/or compilation and debugging of programs for Intel's MCS-80, MCS-85 or MCS-48 microprocessor families without the need for handling paper tape. ISIS-II performs all file handling operations for the user, leaving him free to concentrate on the details of his own application. When used in conjunction with an optional in-circuit emulator (ICE™) module, the Model 230 provides all the hardware and software development tools necessary for the rapid development of a microcomputer-based product.

UPP-103*
UNIVERSAL PROM PROGRAMMER

Intellec® Development System Peripheral for PROM programming and verification

Personality cards available for programming all Intel® PROM families

Zero insertion force sockets for both 16-pin and 24-pin PROMs

Universal PROM Mapper software provides powerful data manipulation and programming commands

Flexible power source for system logic and programming pulse generation

Holds 2 personality cards to facilitate programming operations using several PROM types

The Universal PROM Programmer (UPP) is an Intellec® System peripheral capable of programming and verifying the following Intel Programmable ROMs (PROMs): 1702A, 2704, 2708, 2716, 3601, 3602, 3602A, 3621, 3622, 3622A, 3604, 3604A, 3604AL, 3604L-6, 3605, 3608, 3624, 3624A, 3625, 3628, 8702A, 8704, and 8708. In addition, the UPP programs the PROM memory portions of the 8748 Microcomputer and the 8755 PROM and I/O chip. Programming and verification operations are initiated from the Intellec Development System console and are controlled by the Universal PROM Mapper (UPM) program.

*This UPP103 replaces the UPP101, UPP102.

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INTELLEC PROMPT 48
MCS-48 MICROCOMPUTER DESIGN AID

Complete low cost design aid and EPROM programmer for revolutionary MCS-48 single component computers

Simplifies microcomputing, allowing user to enter, run, debug, and save machine language programs with calculator-like ease

Utilizes two removable 8-bit MCS-48 CPUs
- **— 8748 CPU with erasable, reprogrammable on-chip program memory**
- **— 8035 CPU with off-chip program memory**

1K-byte erasable, reprogrammable on-chip (8748), expandable program memory, 1K-byte RAM in PROMPT system

64 bytes RAM on-chip, expandable register memory

256 bytes expandable RAM data memory in PROMPT system

27 on-chip TTL compatible expandable I/O lines

On-chip clock, internal timer/event counter, two vectored interrupts, eight level stack control

Single +5V DC system power requirement

Integral keyboard and displays (no teletypewriter or CRT terminal required)

Extensive PROMPT 48 monitor, allowing system I/O, bus, and memory expansion

Compatible with Intellec microcomputer development systems

Includes comprehensive design library

The Intellec Prompt 48 MCS-48 Microcomputer Design Aid is a low cost, fully-assembled design aid for the revolutionary 8748 single component microcomputer. PROMPT 48 simplifies the programming of MCS-48 systems — programs may be entered and debugged with calculator-like ease on the large, informative display and keyboard panel. The comprehensive design library with tutorial manual is ideal for newcomers to microcomputing. PROMPT 48's panel connector allows easy access to I/O ports and system bus. Thus users can expand program memory beyond the 1K bytes provided internally. PROMPT 48 can serve as an economical 8748 Specialized PROM Programmer (SPP) peripheral in Intellec microcomputer development systems.



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ICE-48
MCS-48 IN-CIRCUIT EMULATOR

Emulates 8048, 8748, 8035, and 8021 Microcomputers

Extends Intellec microcomputer development system debug power to user configured system via external cable and 40-pin plug, replacing system MCS-48 device

Emulates user system MCS-48 device in real time

Shares static RAM memory with user system for program debug

Provides hardware comparators for user designated break conditions

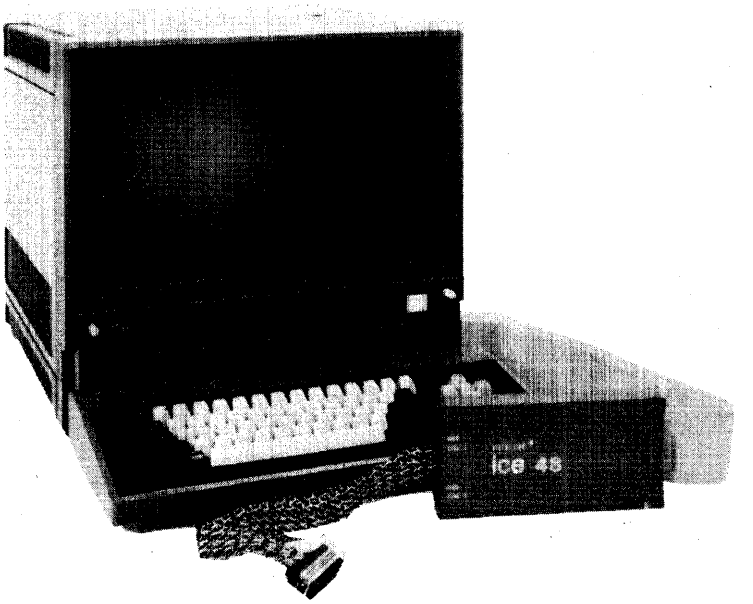
Eliminates need for extraneous debugging tools residing in user system

Collects bus, register, and MCS-48 status information on instructions emulated

Provides capability to examine and alter MCS-48 registers, memory, and flag values, and to examine pin and port values

Integrates hardware and software efforts early to save development time

The ICE-48 MCS-48 In-Circuit Emulator module is an intellec-resident module that interfaces with any MCS-48 system. The MCS-48 family consists of the 8048, 8748, 8035, and 8021 microcomuters. The ICE-48 module interfaces with an MCS-48 system through a cable terminating in an MCS-48 pin-compatible plug which replaces the MCS-48 device in the system. With the ICE-48 plug in place, the designer has the capability to execute the system in real time while collecting up to 255 instruction cycles of real-time trace data. In addition, he can single step the system program to monitor more closely the program logic during execution. Static RAM memory is available through the ICE-48 module to emulate MCS-48 program and data memory. The designer can display and alter the contents of data and replacement RAM control memory, internal MCS-48 registers and flags, and I/O ports. Powerful debug capability is extended into the MCS-48 system while ICE-48 debug hardware and software remain inside the Intellec system. Symbolic reference capability allows the designer to use meaningful symbols rather than absolute values when examining and modifying memory, registers, flags, and I/O ports in this system.



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ICE-85™
MCS-85™ IN-CIRCUIT EMULATOR

Connects the Intellec® System Resources to the user-configured system via a 40-pin adaptor plug

Executes user system software in real-time

Allows user-configured system to share Intellec® memory and I/O facilities

Provides 1023 states of 8085 trace data plus 18 additional logic signals via an External Trace Module

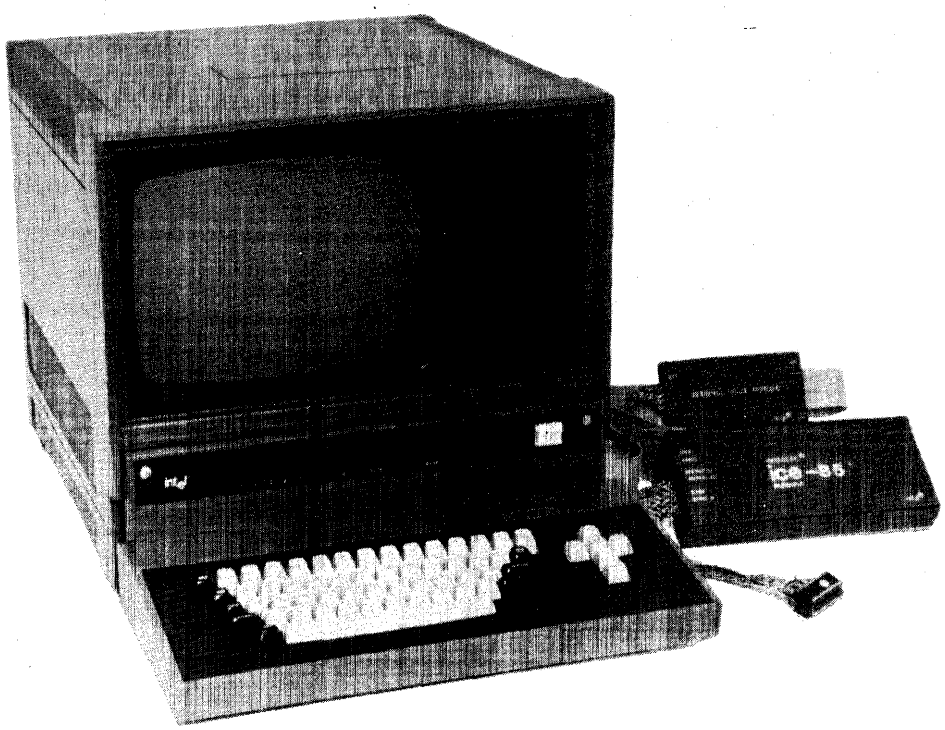
Offers full symbolic debugging capability for both assembly language and Intel's high-level compiler language, PL/M-80

Displays trace data from the user's 8085 in assembler mnemonics and allows personality groupings of data sampled by the external 18-channel trace module

Extends ICE capabilities to the rest of the prototype system peripheral circuitry by allowing the user to execute his own peripheral chip analysis routines

Provides ability to examine and alter MCS-85™ registers, memory, flag values, interrupt bits and I/O ports

The ICE-85 module resides in the Intellec® Microcomputer Development System and interfaces to the user system's 8085. In addition, an external trace module provides access to user system peripheral circuitry via a user-configured DIP clip for peripheral ICs or may be attached to as many as 18 separate prototype signal nodes via individual probe clips. Using the ICE-85 module, the designer can execute prototype software in real-time or single-step mode and can substitute Intellec® system memory and I/O for user system equivalent. ICE capability can be extended to the rest of the user system peripheral circuitry by allowing the user to create and execute a library of user-defined peripheral chip analyzer routines. All user access to the prototype system software may be done symbolically by assigning names to program locations and data, I/O ports and groups of external trace signals. For the first time, in-circuit emulation extends beyond the user's prototype CPU to the entire user's system, allowing In-System Emulation.



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PL/M-80
HIGH LEVEL PROGRAMMING LANGUAGE
INTELLEC® RESIDENT COMPILER

Cuts software development and maintenance costs

Speeds project completion

Improves product reliability

Eases enhancements as system capabilities expand

Produces relocatable and linkable object code

Resident operation on Intellec® Microcomputer Development System and Intellec® Series II Microcomputer Development Systems

Sophisticated code optimization reduces application memory requirements

PL/M-80 is an advanced, high-level programming language for Intel® 8080 and 8085 Microprocessors, iSBC-80 OEM Computer Systems and Intellec® Microcomputer Development Systems. PL/M has been substantially enhanced since its introduction in 1973 and has become one of the most effective and powerful microprocessor systems implementation tools available. It is easy to learn, facilitates rapid program development and debugging, and significantly reduces maintenance costs.

PL/M is a powerful, high-level algorithmic language in which program statements can naturally express the algorithm to be programmed. This frees programmers to concentrate on their system development without having to deal with assembly language details (such as register allocation, meanings of assembler mnemonics, etc.).

The PL/M compiler efficiently converts free-form PL/M programs into equivalent 8080/8085 instructions. Substantially fewer PL/M statements are necessary for a given application than if it were programmed at the assembly language or machine code level.

Since PL/M programs are problem oriented and more compact, programming in PL/M results in a high degree of productivity during development efforts. This translates into significant reductions in software development and maintenance costs for the user.

FORTRAN-80
8080/8085 ANS FORTRAN 77
INTELLEC RESIDENT COMPILER

Provides resident operation on Intellec Microcomputer Development System and Intellec Series II microcomputer development systems

Meets and exceeds ANS FORTRAN 77 Subset Language Specification

Produces relocatable and linkable object code compatible with resident PL/M-80 and 8080/8085 macroassembler

Supports Intel floating point standard

Provides full FORTRAN 77 language I/O support when used with ISIS-II runtime library

Sophisticated code optimization insures efficient program implementation

Supports full symbolic debugging with ICE-80 and ICE-85

FORTRAN-80 is a computer industry standard, high level programming language and compiler that translates FORTRAN statements into relocatable object modules. When the object modules are linked together and located into absolute program modules, they are suitable for execution on Intel 8080/8085 microprocessors, iSBC-80 OEM computer systems, and Intellec microcomputer development systems. FORTRAN-80 meets and exceeds the ANS FORTRAN 77 Language Subset Specification[1]. The compiler operates on Intellec microcomputer development systems under ISIS-II disk operating systems and produces efficient relocatable object modules compatible for linkage with PL/M-80 and 8080/8085 macroassembler modules. The ANS FORTRAN 77 language specification offers many powerful extensions to the FORTRAN language that are especially well suited to Intel 8080/8085 microprocessor software development. Because FORTRAN-80 conforms to the ANS FORTRAN 77 standard, the user is assured of compatibility with existing FORTRAN software meeting the standard as well as a guarantee of upward compatibility to other computer systems supporting an ANS FORTRAN 77 compiler.

[1] ANSI X3J3/90

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MCS-48™ DISKETTE-BASED SOFTWARE SUPPORT PACKAGE

Extends Intellec® Microcomputer Development System to support MCS-48™ development

MCS-48 Assembler provides conditional assembly and macro capability

Takes advantage of powerful ISIS-II file handling and storage capabilities

The MCS-48™ Diskette-based Software Support Package (MDS-D48) comes on an Intel® ISIS-II System Diskette and contains the MCS-48 Assembler (ASM48), and the diskette version of the Universal PROM Mapper.

The MCS-48 Assembler (ASM48) translates symbolic 8048 assembly language instructions into the appropriate machine operation codes. In addition to eliminating the errors of hand translation, the ability to refer to program addresses with symbolic names makes it easier to modify programs when adding or deleting instructions. Conditional assembly permits the programmer to specify portions of the master source document which should be included or deleted in variations on a basic system design, such as the code required to handle optional external devices.

Macro capability allows the programmer to define a routine through the use of a single label. ASM48 will assemble the code required by the reserved routine whenever the Macro label is inserted in the text.

Output from the ASM48 is in standard Intel® Hex format. It may be loaded directly to an ICE-48 module for integrated hardware/software debugging. It may also be loaded into the Intellec Development System for 8748 PROM programming using the Universal PROM Programmer.

MDS-EM1 8021 EMULATION BOARD

EPROM functional equivalent of 8021 — single component 8-bit microcomputer

Based on 8748 — user programmable/erasable EPROM 8-bit computer

Operates with ICE-48™ to provide full in-circuit debugging of 8021 prototype system

Connects to prototype system through 8021 pin compatible plug

On-card 3.0 MHz or external TTL driven clock

Portable 4" × 7" microcomputer circuit assembly

The MDS-EM1 emulator board is a ready-to-use 4" × 7" microcomputer circuit assembly that emulates the Intel 8021 microcomputer. A 12-inch flat-cable assembly connects the board to the 8021 socket in a prototype system. The board is designed so that it can be mounted either as a stand-alone unit, or within the prototype assembly.

The 8021 microcomputer has 1K × 8 mask-programmable ROM program memory and 64 by 8 RAM data memory. The MDS-EM1 is controlled by an Intel 8748, with 1K of EPROM program memory and a 64 byte data memory. The EPROM can be programmed and erased repeatedly during hardware and software development. The MDS-EM1 has several ancillary circuits that perform the following functions which are specific to the 8021:

Zero crossing detector

Crystal controlled clock/buffer

Port Ø simulator

For prototype debugging, the 8748 can be removed from its socket and replaced with a cable to an INTEL ICE-48. When used with the MDS-EM1, ICE-48 emulates the 8021 in real-time, or single-steps the 8021 program at the user's command. A full range of capabilities for examining and modifying 8021 memory and status are supplied through ICE-48.

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Semiconductors
3501 ED BLUESTEIN BLVD., AUSTIN, TEXAS 78721

MC14 1000
MC14 1200
MC14 1099

Advance Information

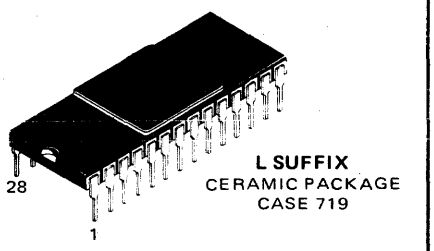
CMOS LSI
(LOW-POWER COMPLEMENTARY MOS)

ONE CHIP MICROCOMPUTERS

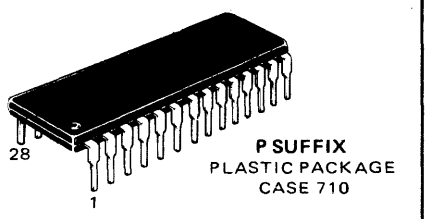
ONE CHIP MICROCOMPUTERS

The MC141000 family is a series of 4-bit CMOS Microcomputers designed for dedicated applications. The CMOS technology of the MC141000 family provides the flexibility of microcomputers, for battery-powered and battery-backed-up applications. The MC141000 and MC141200 include ROM, RAM, and I/O for self-contained configurations in 28 and 40-pin packages. The 48-pin MC141099 has RAM and I/O with provision for external program memory. The MC141099 serves lower-volume applications such as prototyping or pilot production of MC141000 and MC141200 systems.

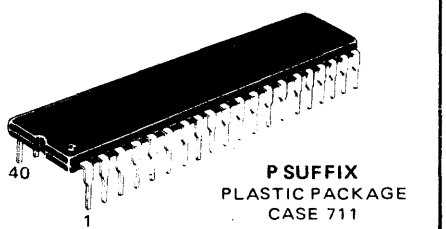
FEATURES		MC141000	MC141200	MC141099
Package Pin Count		28 Pins	40 Pins	48 Pins
Instruction Read Only Memory		1024 X 8 (8,192 Bits)		None
Data Random Access Memory		64 X 4 (256 Bits)		
"R" Individually Addressed Outputs		11	16	16
"O" Parallel Latched Data Outputs		8 Bits		5 Bits
"R" and "O" Output Drive		Source 20 mA		
Maximum-Rated Voltage		6.5 V		
Working Registers		Static 2-4 Bits Each		
Instruction Set		See Table 2		
External Address Lines		None		10
On-Chip Oscillator		Yes		
Maximum Power Dissipation	5 V, 600 kHz	11.5 mW		
	5 V, 100 kHz	2.8 mW		
	3 V, 200 kHz	1.5 mW		
	3 V, 30 kHz	0.36 mW		



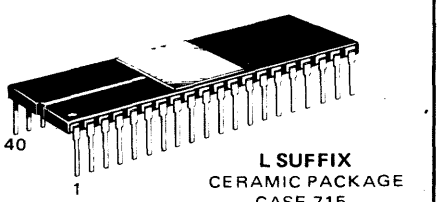
L SUFFIX
CERAMIC PACKAGE
CASE 719



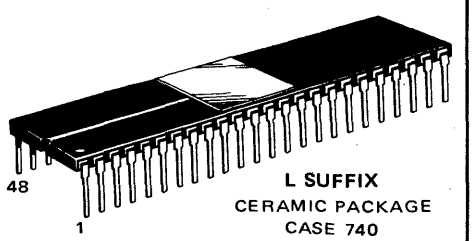
P SUFFIX
PLASTIC PACKAGE
CASE 710



P SUFFIX
PLASTIC PACKAGE
CASE 711



L SUFFIX
CERAMIC PACKAGE
CASE 715



L SUFFIX
CERAMIC PACKAGE
CASE 740

APPLICATIONS

- Appliance Controllers
- Calculators
- Toys
- Radio Controllers
- Communications Controllers
- Data Terminals
- Cash Registers
- Heating/Air-Conditioning Controllers
- Remote Sensing System
- Printing Controllers
- Security Systems
- Power Systems Control
- Automotive Control

The above applications of the MC141000 family demonstrate its wide potential. Motorola accepts customer programs or will contract complete program development given the specifications for the application. Customer hardware and software support is available for developing programs and debugging systems. This consists of one board and a software package using the M6800 EXORciser. Contact your local sales office for details.

ORDERING INFORMATION

MC14XXXX — Suffix Denotes
- L Ceramic Package
- P Plastic Package

This is advance information and specifications are subject to change without notice.

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ADI-513
(Replaces NP-83 R1)

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MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +6.5	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin, All Inputs	I	10	mAdc
DC Current Drain, V_{DD} Pin	I	250	mAdc
DC Current Drain, V_{SS} Pin	I	20	mAdc
Operating Temperature Range	T_A	-40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C
Total Power Dissipation	P_D	See Figure 1	mW

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$.

RECOMMENDED OPERATING CONDITIONS (V_{SS} = 0)

Parameter	Symbol	Value	Unit
DC Supply Voltage — High Speed Clock Full Range Operation	V_{DD}	+4.75 to +6.0 +3.0 to +6.0	Vdc
Clock Frequency — V_{DD} = 5.0 Vdc ± 5% V_{DD} = 3.0 Vdc Min.	f_{Clk}	DC to 600 DC to 200	kHz

ELECTRICAL CHARACTERISTICS (V_{DD} = +5.0 V, V_{SS} Gnd, T_A = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
Input Current — K Inputs and INIT	I_{in}				μAdc
(V_{in} = 5.0 V)		75	100	135	
(V_{in} = 0.0 V)		–	-0.00001	-0.3	
Input Current — I Inputs (MC141099 Only)	I_{in}				μAdc
(V_{in} = 5.0 V)		–	0.00001	0.3	
(V_{in} = 0.0 V)		–	-0.00001	-0.3	
Input Voltage — I Inputs (MC141099 Only)					Vdc
	V_{IL}	–	–	0.8	
	V_{IH}	2.0	–	–	
Input Voltage — Other Inputs					Vdc
	V_{IL}	–	–	1.5	
	V_{IH}	3.5	–	–	
Output Drive — R and O Outputs					mAdc
(V_{OH} = 2.4 V) — See Figure 2	I_{OH}	-20	–	–	
(V_{OL} = 0.4 V, T_A = 85°C, V_{DD} = 4.75 V)	I_{OL}	1.6	–	–	
Output Drive — PA and PC Outputs (MC141099 Only)					μAdc
(V_{OH} = 4.6 V) (T_A = 85°C, V_{DD} = 4.75 V)	I_{OH}	-100	–	–	
(V_{OL} = 0.4 V)	I_{OL}	100	–	–	
Average Supply Current	I_{DD}	–	–	See Figure 3	μAdc
Static Supply Current (V_{DD} = 6.0 V)	I_{DD}	–	60	300	μAdc
Oscillator Frequency (V_{DD} = 4.75 V)	f_{Clk}	No Limit	–	600	kHz
Internal Oscillator Frequency for R_{ext} = 30 kΩ	f_{Clk}	400	500	600	kHz
Input Capacitance — K Inputs and INIT	C_{in}	–	–	7.5	pF
Input Capacitance — Clock Input	C_{io}	–	–	30	pF

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FIGURE 1 – TOTAL POWER DISSIPATION

Care must be taken to ensure that the maximum power dissipation of the package is not exceeded.

$$T_{stg} = T_A + (P_D)(\theta_{JA})$$

where T_{stg} is maximum storage temperature (150°C)

T_A is ambient operating temperature

P_D is total power dissipation:

$$P_D = (I_{DD})(V_{DD}) + (I_{OH})(V_{DD} - V_{OH}) + (I_{OL})(V_{OL} - V_{SS})$$

(I_{OH} and I_{OL} are the sum of all output pins)

	θ_{JA} Value	
	Ceramic	Plastic
28-Pin Package	58	98
40-Pin Package	50	95
48-Pin Package	50	–

FIGURE 2 – MINIMUM OUTPUT SOURCE CURRENT versus OUTPUT VOLTAGE (R and O Outputs)

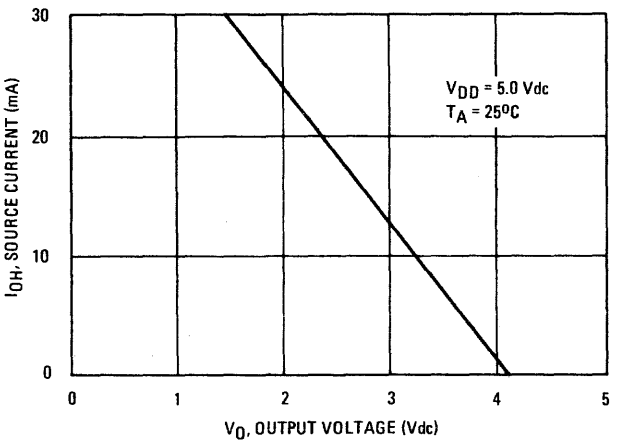
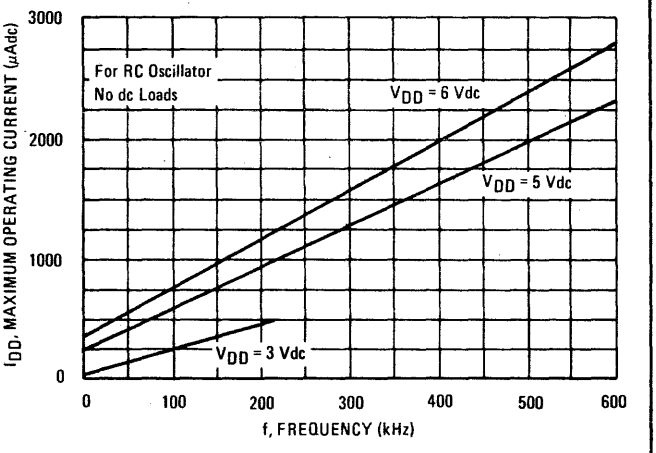
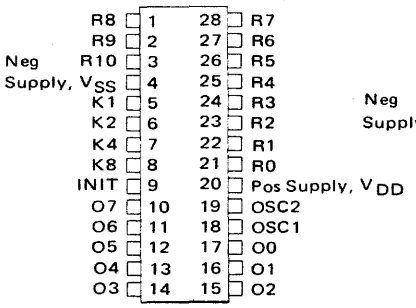


FIGURE 3 – MAXIMUM OPERATING CURRENT versus OSCILLATOR FREQUENCY

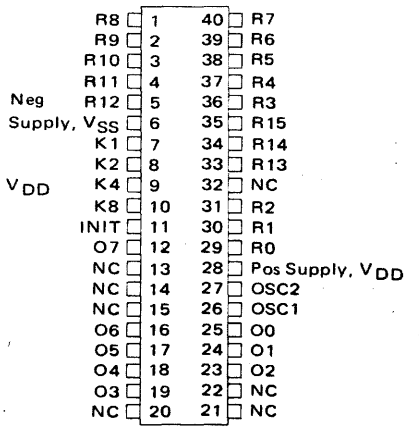


PIN ASSIGNMENTS

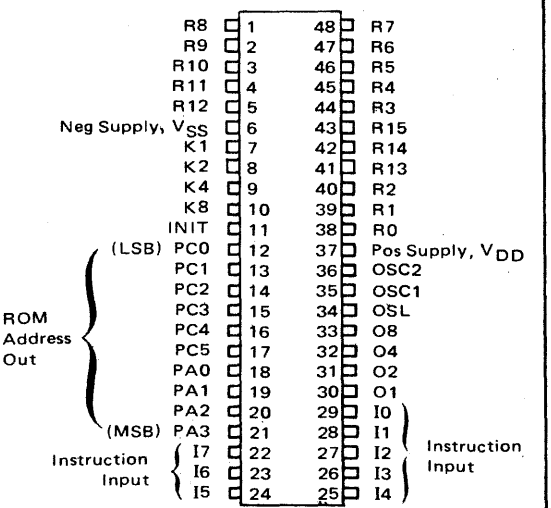
MC141000



MC14 1200

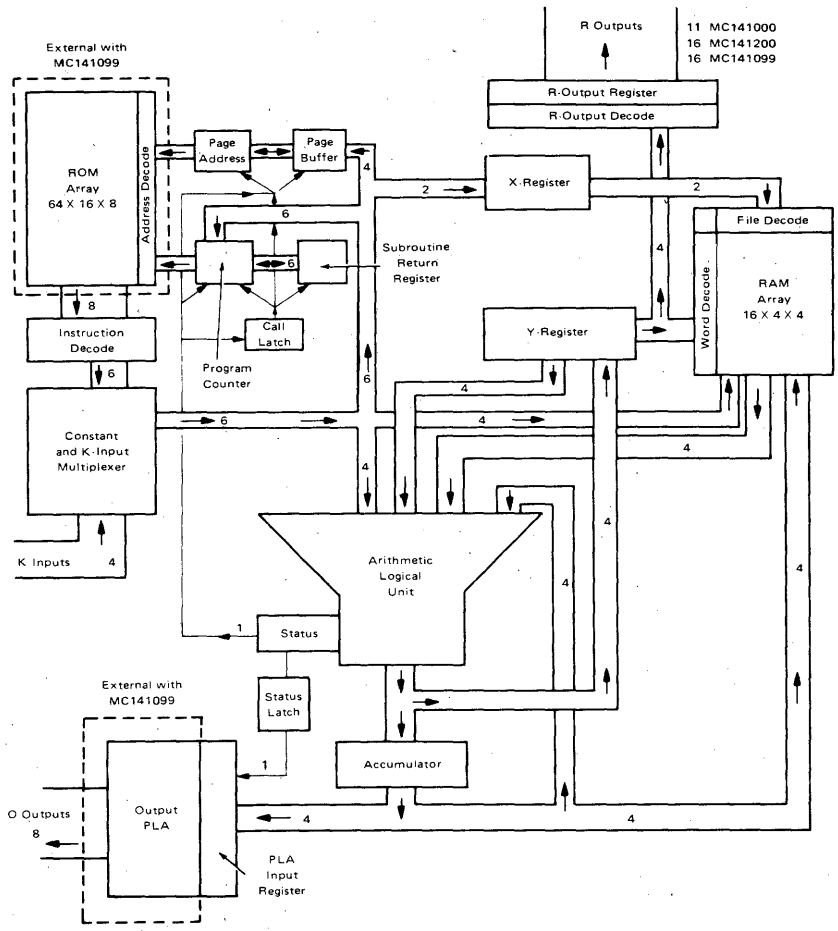


MC141200



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FIGURE 4 – FUNCTIONAL BLOCK DIAGRAM – MC141000/MC141200/MC141099



The block diagram above shows the resources available to the MC141000/1200/1099 programmer. They are:

A The accumulator is used to store the result of an ALU operation for subsequent operations.

ALU The arithmetic logical unit performs calculation and decision-making tasks.

K Inputs The K lines are the data input port. Since there are only four input lines, they are usually multiplexed under control of the R lines. The inputs are diode protected and have a pull-down resistor of approximately 50 kΩ; therefore, open inputs are read as a logic low.

O Outputs The eight outputs of the PLA are connected to output drivers which comprise the O outputs. These output drivers may be manufactured as open emitter, active sink, or push-pull at the user's option.

PLA The output programmable logic array is user-defined to specify the state of each of the eight O outputs for each of the 32 possible PLAIR outputs.

PLAIR The programmable logic array input register is a 5-bit latch which latches the four accumulator bits and the output of the status latch.

RAM Variable data is stored in the 64-word, 4-bit per word Random Access Memory. Data is accessed by decoding a 2-bit file address (X register) and 4-bit word address (Y register).

ROM Array The user's instructions are mask programmed into the Read Only Memory (ROM). Instructions are addressed by a page address register (PA) and program counter (PC). A single subroutine return register (SRR) and page buffer register (PB) permit a subroutine call to any location within the ROM.

R Outputs The output of the Y register is decoded to select one of the R-output lines which can then be set or reset under program control. The R lines are used as control lines to scan keyboards and displays, perform handshakes, and interface external logic. The R outputs may be manufactured as open emitter, active sink, or push-pull at the user's option.

S All branches and subroutine calls are dependent on the state of status logic. It may be set or reset on logical or arithmetic operations and is set by the remainder of the instructions.

SL The status latch stores the state of the status logic in order to preserve it for subsequent O output operations.

NOTE: S and SL are NOT identical.

Y Register The Y register is a multipurpose regiser used to address a word in a RAM file, to select an R output for manipulation by subsequent instructions, or as a general-purpose counting and storage register.

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MICROCOMPUTER OPERATION

The MC141000/1200/1099 program controls data input, storage, processing, and output. The microcomputer internal organization is shown in Figure 4. The processing of data occurs in the arithmetic logic unit (ALU). K-input data enters the ALU and is stored in the 4-bit accumulator. The accumulator output accesses the output latches, RAM storage, or the ALU input. Data is stored in the 256-bit RAM, organized into 64 words, 4 bits per word. The 4-bit words are grouped into four 16-word files addressed by a 2-bit X register. The 4-bit Y register addresses one of the 16 words in a file.

The 43 basic instructions handle I/O, constant data from the ROM, bit control, internal data transfer, arithmetic processing, logic comparison, conditional and nonconditional branching and subroutines.

The system designer has access for mask programming the following functions:

1. ROM – 1024 Words of 8 Bits
2. Programmable Logic Array for O Outputs
3. Output Drivers

The MC141000 microcomputer consists of seven subsystems:

1. Read Only Memory (ROM)
2. Random Access Memory (RAM)
3. Output Ports
4. Input Port
5. Arithmetic Logical Unit (ALU)
6. The Instruction Decoder
7. Clock

The following paragraphs describe how each of these subsystems is controlled by the instruction set. Every instruction occupies a single memory byte and is executed in one instruction cycle (six clock cycles).

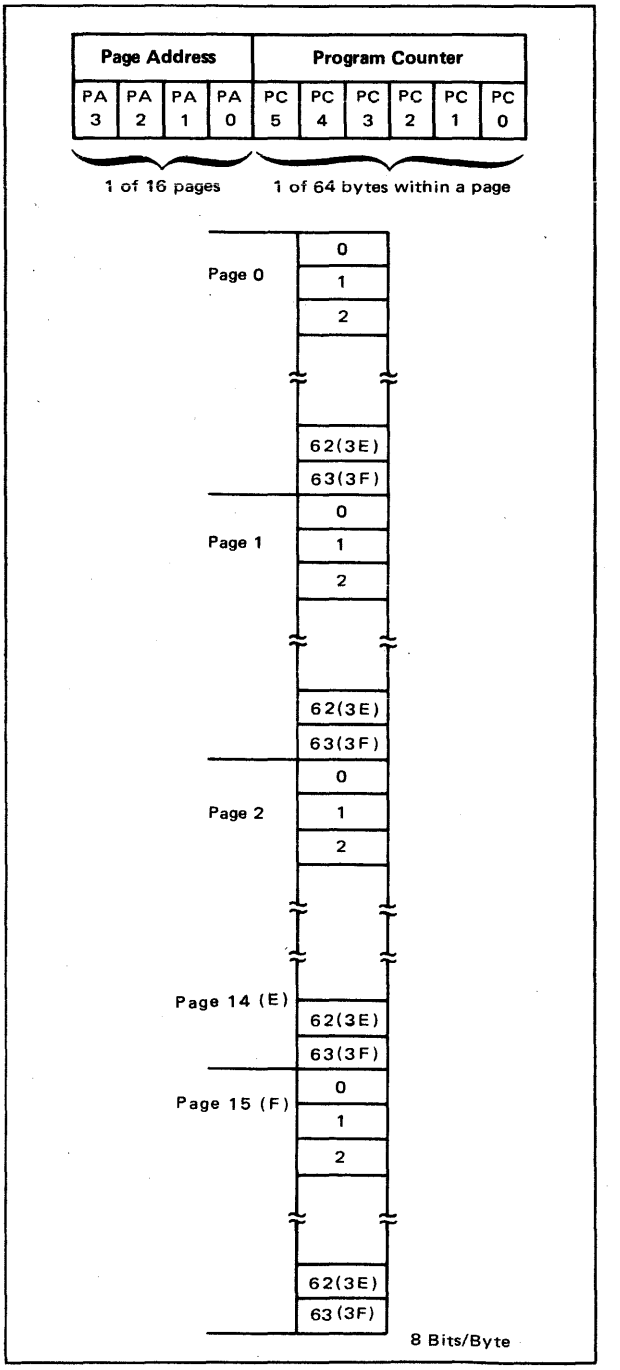
ROM ARRAY

The ROM in the MC141000/1200 consists of 8192 bits of mask-programmed memory organized as 1024 8-bit instructions. It is divided into 16 pages of 64 instructions per page. See Figure 5.

Instructions within ROM are addressed by the page address register (PA) which contains the page number, and the program counter (PC) which contains the location of the instruction relative to the beginning of the page. The PC is incremented prior to fetching the next instruction (unless diverted by a BRanch or CALL) so each instruction is accessed in the numerical order of its address. A carry from the PC is not added to the PA so the program "wraps around" within the page rather than executing the first instruction of the following page. Upon power up, the PC is set to zero and the PA and PB are set to 15.

The MC141099 addresses an external ROM program via ten address output lines. These are 6 bits from PC (PC0–PC5) and 4 bits from PA (PA0–PA3). The 8-bit instruction bytes are received by the MC141099 from an external ROM on 8 TTL compatible instruction input lines (I0–I7).

FIGURE 5 – ROM ORGANIZATION



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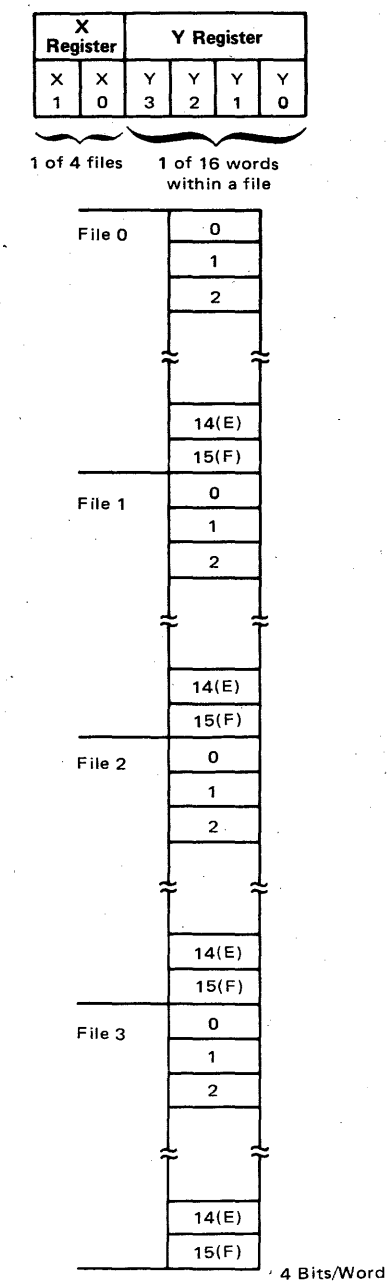
RANDOM ACCESS MEMORY – RAM

RAM consists of 256 bits organized into 64 4-bit words. For purposes of addressing, the 4-bit words are organized into four files of 16 4-bit words per file, Figure 6.

The X register is decoded to select 1 of the 4 RAM files; and the Y register is decided to address 1 of the 16 words in the selected file.

Individual bits within the RAM can be set, reset and tested under program control.

FIGURE 6 – RAM ORGANIZATION



OUTPUT PORTS

Two output ports (R and O) are included in the microcomputer. The MC141000 has eleven R outputs and the MC141200 and MC141099 each have sixteen R outputs. The MC141000 and MC141200 each have eight O outputs, while the MC141099 has five. The number of R outputs is the only difference between the MC141000 and the MC141200.

R-output lines are used primarily as control or "handshake" lines, and to multiplex external hardware. The R output which is to be operated on is selected by a binary decode of the contents of the Y register. Set R and reset R instructions change the state of one R output at a time.

The eight O-output lines on the MC141000 and MC141200 are the decoded outputs of the contents of the 5-bit PLAIR. Since the PLAIR is loaded from the A and the SL, these registers must be "set up" prior to an output operation. The status latch can only be loaded by the YNEA (Y register not equal to accumulator) instruction while the contents of the accumulator may be modified by numerous other instructions. The MC141099 brings out the 5-bit PLAIR to allow external decoding. An external PROM/EPROM could be used to simulate the PLA. Figure 7 shows how EPROMS may be used with MC141099 to emulate an MC14100 or an MC141200.

In a typical application, the first four R lines might be used as digit selects for outputting a four-digit decimal number using the PLA programmed as a seven-segment decode as shown in Figure 8.

The MC141000/1200 outputs may be mask programmed in any of three configurations. Figure 9 shows the open emitter circuit capable of sourcing 20 mA at V_O = 2.4 V and V_{DD} = 5.0 V, which will drive an LED. Figure 10 is the open drain circuit capable of sinking 1.6 mA over temperature, which will drive one TTL load or four LSTTL loads. The source and sink devices are combined in the active push-pull circuit of Figure 11. The MC141099 also has outputs as in Figure 11.

INPUTS

The input lines consist of the four K-input lines and the initialize (INIT) line. All inputs are static-protected CMOS inputs with pulldown of about 50 kΩ. Thus, an open input is equivalent to logic 0. The circuit is shown in Figure 12.

When power is applied, the registers shown in Table 1 are loaded as shown for power up. All other internal registers and RAM come up in an arbitrary state.

After power is applied, the initialize (INIT) input may be used to reinitialize the processor. Internally, INIT has

TABLE 1 – POWER UP AND INITIALIZE CONDITIONS

	PC	PA	PB	CL	PLAIR	R Outputs
Power Up	0	F_{16}	F_{16}	0	0	0
Initialize	0	$\overline{K}$	$\overline{K}$	0	0	0

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a 50 kΩ pull-down resistor which holds the INIT line low. It must be held high for a minimum of 6 full clock cycles and then returned to the low state. If a mechanical switch or other mechanical device is used to control INIT, it may be necessary to include a method of contact debounce to ensure a valid INIT pulse.

A valid INIT pulse causes the registers to be initialized as shown in the table. The contents of registers other than those shown remain unchanged during initialize. Note that the PA and PB are loaded with the 1's complement of the K-input lines (K8 = MSB). This feature allows the MC141000 to be initialized to the first instruction on any page by controlling the K inputs. This is useful where the same circuit may be used for several applications. Since the K inputs have 50 kΩ pull-down resistors, open inputs are a 0 (unless driven from another device) and the 1's complement (F_{16}) is loaded into PA and PB.

ARITHMETIC LOGICAL UNIT (ALU)

The ALU is the calculating and decision-making portion of the MC141000/1200/1099 hardware and consists of a 4-bit adder/comparator and the status logic.

The adder/comparator can add, subtract, compare two numbers, add +1, −1, 6, 8, and 10.

The status logic is selectively set or reset by add, subtract, increment, decrement, compare and bit-test operations. Other instructions always set the status logic to a 1.

INSTRUCTION DECODE

The instruction decode logic latches every instruction fetched from ROM and configures the internal logic to execute the current instruction. The instruction set is listed in Table 2.

CLOCK

The internal oscillator cirucit operates with quartz crystals, ceramic resonators, an external resistor and from an external clock source. These oscillator circuit connections are shown in Figures 13, 14, and 15. Figure 16 shows the typical oscillation frequency with an external resistor. The discrete component values used with the quartz crystal and ceramic resonator oscillators may vary depending upon crystal/resonator manufacturer.

FIGURE 9 – OPEN EMITTER OUTPUT CIRCUIT

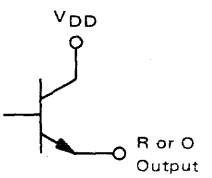


FIGURE 10 – OPEN DRAIN OUTPUT CIRCUIT

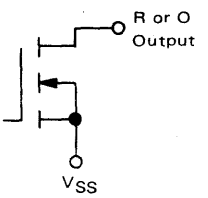


FIGURE 11 – ACTIVE PUSH-PULL OUTPUT CIRCUIT

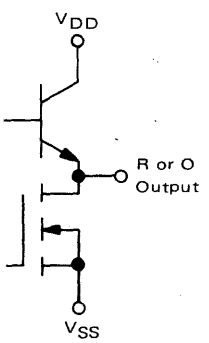
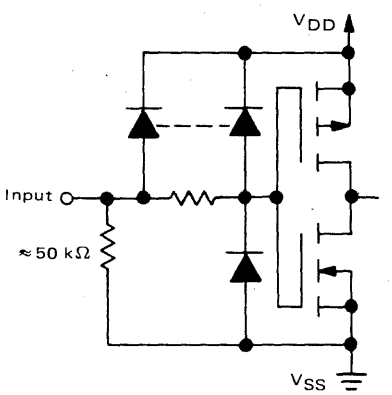
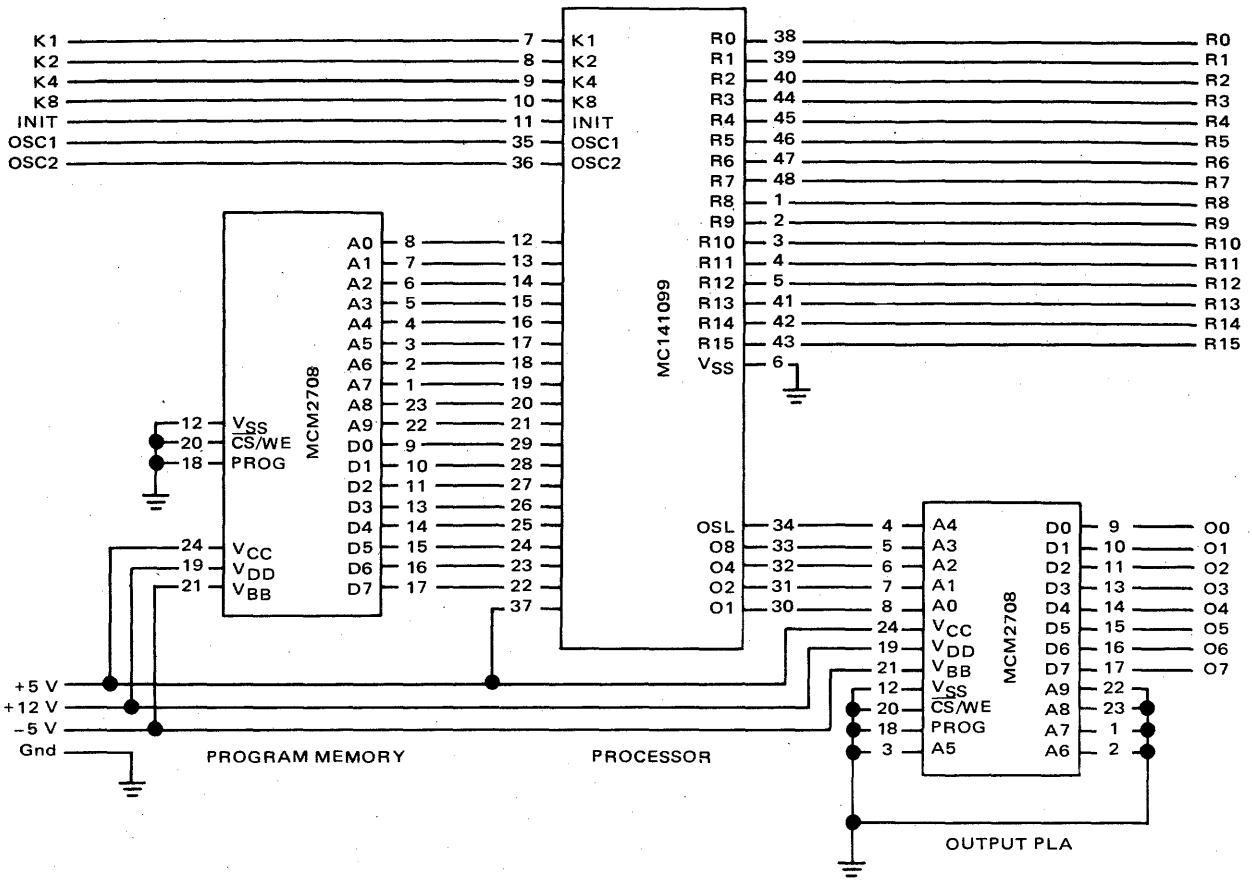


FIGURE 12 – INPUT CIRCUIT WITH PULLDOWN AND STATIC PROTECTION



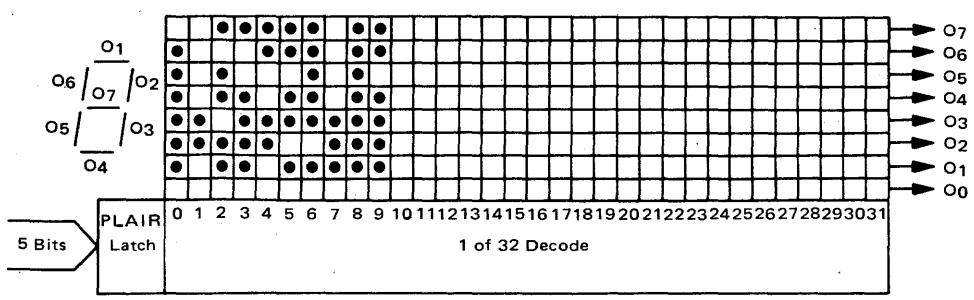
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FIGURE 7 – USING THE MC141099 TO EMULATE MC141000/MC141200 IN REAL-TIME



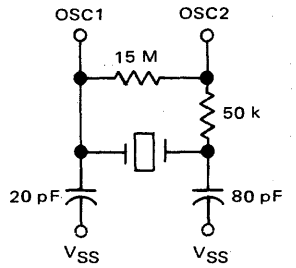
NOTE: The OPLA EPROM outputs may require buffers depending on the requirements of the user's circuit. The EPROM outputs are TTL compatible.

FIGURE 8 – OUTPUT PLA EXAMPLE – 7-SEGMENT DISPLAY DECODE



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FIGURE 13 – EXTERNAL COMPONENTS FOR QUARTZ CRYSTAL OR CERAMIC RESONATOR OSCILLATOR



Component values typical for 500 kHz crystal.

FIGURE 14 – OSCILLATOR CIRCUIT WITH ONE EXTERNAL RESISTOR

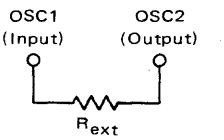


FIGURE 15 – EXTERNAL CLOCK SOURCE INPUT

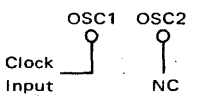
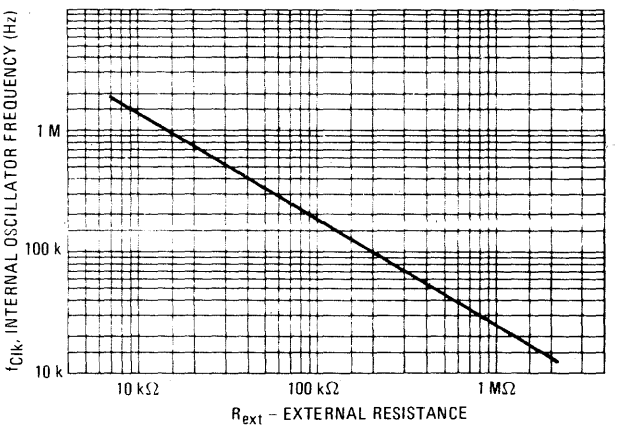


FIGURE 16 – TYPICAL OSCILLATOR FREQUENCY versus EXTERNAL RESISTANCE



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TABLE 2 – MC141000/1200/1099 INSTRUCTION SET

Opcode	Mnemonic	Description
0111 (C)	ALEC	If accumulator is less than or equal to I(C) field, status = 1.
00101001	ALEM	If accumulator is less than or equal to M(X,Y), status = 1.
00100101	AMAAC	Add memory to accumulator. Accumulator = result, status = carry.
00000110	A6AAC	Add 6 to accumulator. Accumulator = result, status = carry.
00000001	A8AAC	Add 8 to accumulator. Accumulator = result, status = carry.
00000101	A10AAC	Add 10 to accumulator. Accumulator = result, status = carry.
10 (W)	BR	Branch to label if status = 1.
11 (W)	CALL	Call subroutine if status = 1.
00101111	CLA	Clear contents of accumulator.
00001011	CLO	Clear PLA Input Register.
00000000	COMX	Complement X-Register.
00101101	CPAIZ	Complement accumulator, then add 1. If accumulator = 0, status = 1.
00000111	DAN	Decrement accumulator. If no borrow, status = 1.
00101010	DMAN	Load M(X, Y) into accumulator and decrement. If no borrow, status = 1.
00101100	DYN	Decrement Y-register. If no borrow, status = 1.
00001110	IA	Increment accumulator.
00101000	IMAC	Load M(X, Y) into accumulator and increment. Status = carry.
00101011	IYC	Increment Y-Register. Status = carry.
00001001	KNEZ	If K-inputs not equal to zero, status = 1.
0001 (C)	LDP	Load page buffer with I(C) field.
001111 (B)	LDX	Load X-register with I(B) field.
00100110	MNEZ	If M(X, Y) not equal to zero, status = 1.
001101 (B)	RBIT	Reset bit I(B) of M(X,Y).
00001111	RETN	Return from subroutine.
00001100	RSTR	Reset R-line specified by Y-register.
00100111	SAMAN	Subtract accumulator from memory. Accumulator = result. If no borrow, status = 1.
001100 (B)	SBIT	Set Bit I(B) of M(X,Y).
00001101	SETR	Set R-line specified by Y-register.
00000011	TAM	Transfer accumulator contents to M(X,Y).
00100000	TAMIY	Transfer accumulator contents to M(X,Y), increment Y-register.
00000100	TAMZA	Transfer accumulator contents to M(X,Y), zero accumulator.
00100100	TAY	Transfer accumulator contents to Y-register.
001110 (B)	TBIT1	If bit I(B) of M(X,Y) is one, status = 1.
0100 (C)	TCY	Transfer I(C) field to Y-register.
0110 (C)	TCMIY	Transfer I(C) field to M(X,Y), increment Y-register.
00001010	TDO	Transfer status latch and accumulator to PLA input register.
00001000	TKA	Tranfer K-inputs to accumulator.
00100001	TMA	Transfer M(X,Y) to accumulator.
00100010	TMY	Transfer M(X,Y) to Y-register.
00100011	TYA	Transfer Y-register contents to accumulator.
00101110	XMA	Exchange contents of M(X,Y) and accumulator.
00000010	YNEA	If Y-register is not equal to accumulator, status and status latch = 1.
0101 (C)	YNEC	If Y-register is not equal to I(C) field, status = 1.

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MOTOROLA
Semiconductors
3501 ED BLUESTEIN BLVD., AUSTIN, TEXAS 78721

MC6862

(0 to 70°C; L or P Suffix)

MC6862C

(-40 to 85°C; L Suffix only)

2400 bps DIGITAL MODULATOR

The MC6862 is a MOS subsystem designed to be integrated into a wide range of equipment utilizing serial data communication.

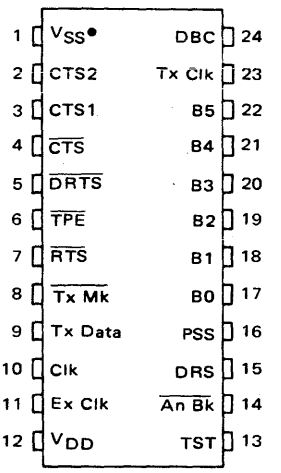
The modulator provides the necessary modulation and control functions to implement a serial data communication link over a voice grade channel, utilizing differential phase shift keying (DPSK) at bit rates of 1200 or 2400 bps. Phase options are provided for both the U.S. and international markets. The MC6862 can be implemented into a wide range of data handling systems, including stand-alone modems, data storage devices, remote data communication terminals, and I/O interfaces for counters.

N-channel silicon gate technology permits the MC6862 to operate using a single voltage supply and be fully TTL compatible.

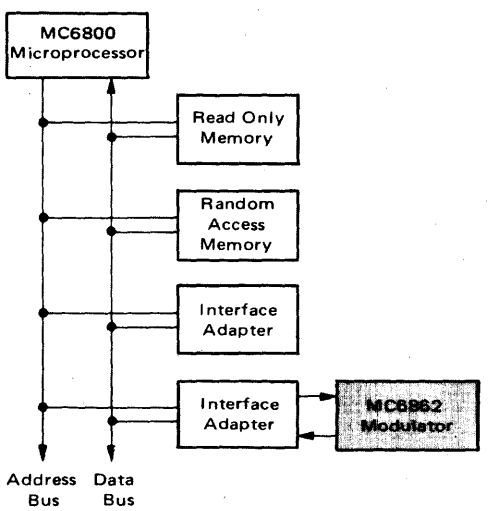
The modulator is compatible with the M6800 microcomputer family, and provides medium-speed data communications capability.

- Clear-to-Send Delay Options
- 511-Bit CCITT Test Pattern
- Terminal Interfaces Are TTL Compatible
- Compatible Functions for 201B/C Data Sets
- CCITT and U.S. Phase Options
- 1200/2400 bps Operation
- Answer Back Tone

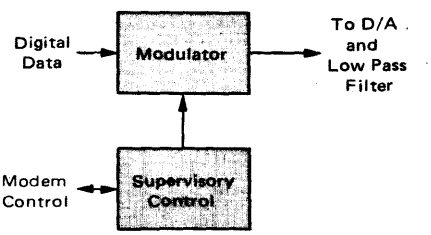
PIN ASSIGNMENT



M6800 MICROCOMPUTER FAMILY
BLOCK DIAGRAM



MC6862 DIGITAL MODULATOR
BLOCK DIAGRAM



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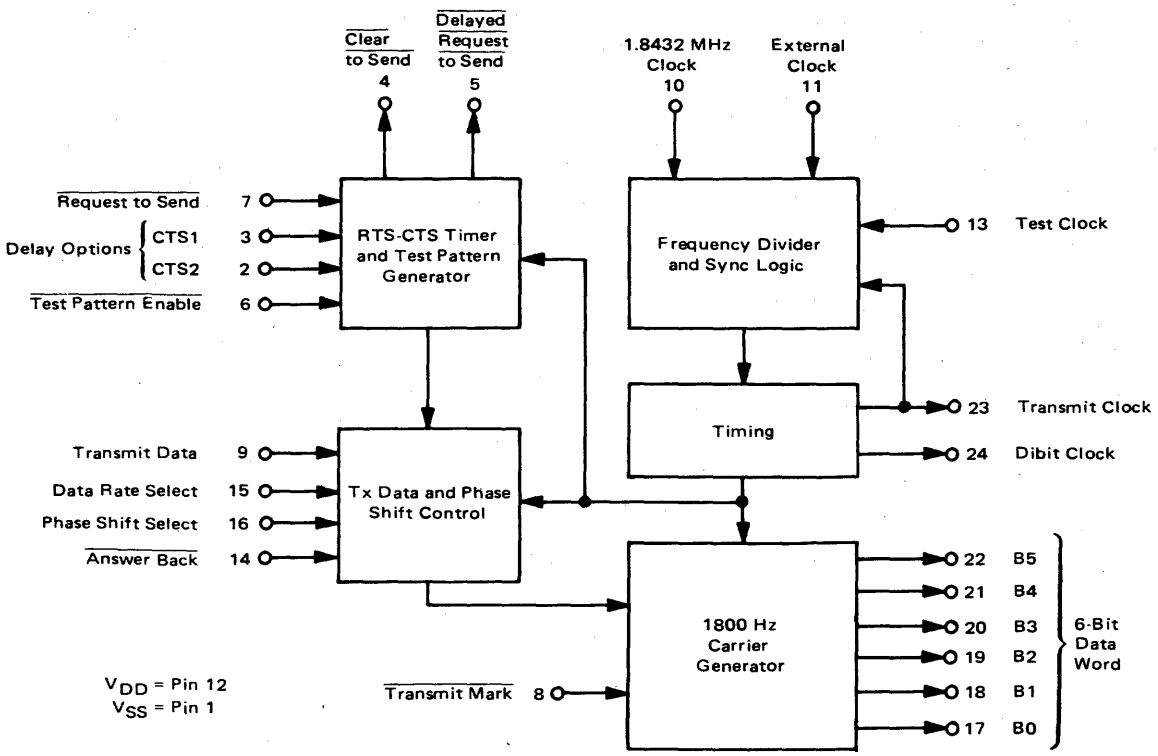
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ELECTRICAL CHARACTERISTICS (V_{DD} = 5.0 ±0.25 Vdc, V_{SS} = 0, T_A = 0 to 70°C, all outputs loaded as shown in Figure 1 unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Input High Voltage	V_{IH}	V_{SS} + 2.0	–	V_{DD}	Vdc
Input Low Voltage	V_{IL}	V_{SS}	–	V_{SS} + 0.8	Vdc
Input Current (V_{in} = V_{SS}) CTS1, CTS2, PSS, DRS, $\overline{An\ Bk}$, and $\overline{Tx\ MK}$ $\overline{RTS}$ and $\overline{TPE}$	I_{in}	– –	– –	-0.2 -1.6	mAdc
Input Leakage Current (V_{in} = 5.25 Vdc, V_{DD} = V_{SS})	I_{IL}	–	–	2.5	µAdc
Output High Voltage (I_{OH} = -0.04 mAdc, Load A) (I_{OH} = 0.0 mAdc, Load B)	V_{OH1} V_{OH2}	V_{SS} + 2.4 V_{DD}-0.5 V	– –	V_{DD} V_{DD}	Vdc
Output Low Voltage (I_{OL} = 1.6 mAdc, Load A)	V_{OL}	V_{SS}	–	V_{SS} + 0.4	Vdc
Input Capacitance (f = 0.1 MHz, T_A = 25°C)	C_{in}	–	5.0	–	pF
V_{DD} Supply Current (All Inputs at V_{SS} except Pin 13 = 57.6 kHz and ALL Outputs Open)	I_{DD}	–	40	60	mAdc
Input Transition Times, All Inputs Except 1.8432 MHz Input (From 10% to 90% points)	t_r t_f	– –	– –	1.0* 1.0*	µs
Input Transition Times, 1.8432 MHz Input (From 0.8 V to 2.0 V)	t_r t_f	– –	– –	40 40	ns
Input Clock Duty Cycle, 1.8432 MHz Input (Measured at 1.5 V level)	D.C.	30	–	70	%
Tx Data Setup Time (Figure 2)	t_S	35	–	–	µs
Tx Data Hold Time (Figure 2)	t_H	35	–	–	µs
Output Transition Times (From 10% to 90% Points)	t_r t_f	– –	– –	5.0 5.0	µs

*Maximum Input Transition Times are ≤ 0.1 x Pulse Width or the specified maximum of 1.0 µs, whichever is smaller.

BLOCK DIAGRAM



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MOTOROLA
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MC6860L

0-600 bps DIGITAL MODEM

The MC6860 is a MOS subsystem designed to be integrated into a wide range of equipment utilizing serial data communications.

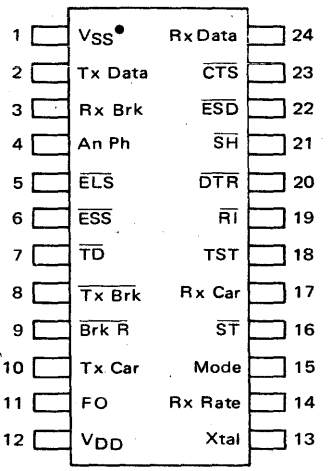
The modem provides the necessary modulation, demodulation and supervisory control functions to implement a serial data communications link, over a voice grade channel, utilizing frequency shift keying (FSK) at bit rates up to 600 bps. The MC6860 can be implemented into a wide range of data handling systems, including stand alone modems, data storage devices, remote data communication terminals and I/O interfaces for minicomputers.

N-channel silicon gate technology permits the MC6860 to operate using a single voltage supply and be fully TTL compatible.

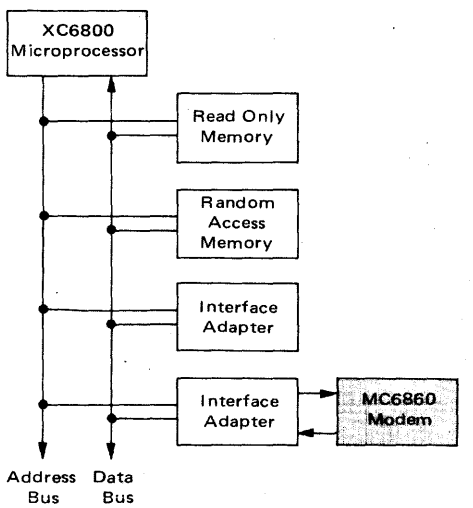
The modem is compatible with the M6800 microcomputer family, interfacing directly with the Asynchronous Communications Interface Adapter to provide low-speed data communications capability.

- Originate and Answer Mode
- Crystal or External Reference Control
- Modem Self Test
- Terminal Interfaces TTL-Compatible
- Full-Duplex or Half-Duplex Operation
- Automatic Answer and Disconnect
- Compatible Functions for 100 Series Data Sets
- Compatible Functions for 1001A/B Data Couplers

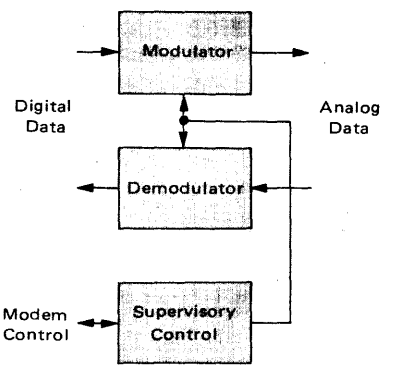
PIN ASSIGNMENT



M6800 MICROCOMPUTER FAMILY BLOCK DIAGRAM



MC6860 DIGITAL MODEM BLOCK DIAGRAM

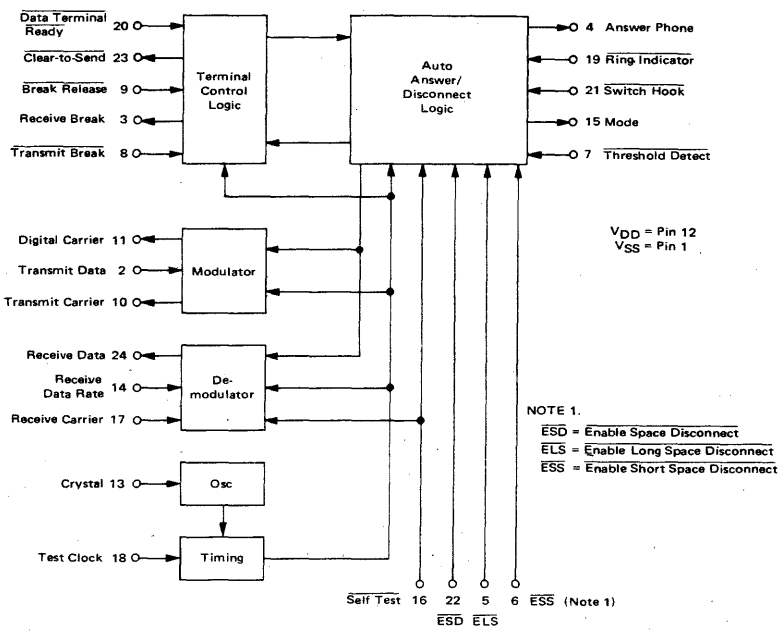


MICROPROCESSOR Motorola

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BLOCK DIAGRAM



ELECTRICAL CHARACTERISTICS (V_{DD} = 5.0 ±0.25 Vdc, all voltages referenced to V_{SS} = 0, T_A = 0 to 70°C, all outputs loaded as shown in Figure 1 unless otherwise noted.)

Characteristic	Symbol	Min	Typ	Max	Unit
Input High Voltage, All Inputs Except Crystal	V_{IH}	2.0	–	V_{DD}	Vdc
Input Low Voltage, All Inputs Except Crystal	V_{IL}	V_{SS}	–	0.80	Vdc
Crystal Input Voltage (Crystal Input Driven from an External Reference, Input Coupling Capacitor = 200 pF, Duty Cycle = 50 ±5%)	V_{in}	1.5	–	2.0	V_{p-p}
Input Current (V_{in} = V_{SS}) All Inputs Except Rx Car, Tx Data, $\overline{TD}$, TST, $\overline{RI}$, $\overline{SH}$	I_{in}	–	–	-0.2	mAdc
$\overline{RI}$, $\overline{SH}$ Inputs		–	–	-1.6	
Input Leakage Current (V_{in} = 7.0 Vdc, V_{DD} = V_{SS}, T_A = 25°C)	I_{IL}	–	–	1.0	µAdc
Output High Voltage, All Outputs Except An Ph and Tx Car (I_{OH1} = -0.04 mAdc, Load A)	V_{OH1}	2.4	–	V_{DD}	Vdc
Output Low Voltage, All Outputs Except An Ph and Tx Car (I_{OL1} = 1.6 mAdc, Load A)	V_{OL1}	V_{SS}	–	0.40	Vdc
Output High Current, An Ph (V_{OH2} = 0.8 Vdc, Load B)	I_{OH2}	0.30	–	–	mAdc
Output Low Voltage, An Ph (I_{OL2} = 0, Load B)	V_{OL2}	V_{SS}	–	0.30	Vdc
Input Capacitance (f = 0.1 MHz, T_A = 25°C)	C_{in}	–	5.0	–	pF
Output Capacitance (f = 0.1 MHz, T_A = 25°C)	C_{out}	–	10	–	pF
Transmit Carrier Output Voltage (Load C)	V_{CO}	0.20	0.35	0.50	V(RMS)
Transmit Carrier Output 2nd Harmonic (Load C)	V_{2H}	-25	-32	–	dB
Input Transition Times, All Inputs Except Crystal (Operating in the Crystal Input Mode; from 10% to 90% Points)	t_r	–	–	1.0*	µs
	t_f	–	–	1.0*	
Input Transition Times, Crystal Input (Operating in External Input Reference Mode)	t_r	–	–	30	ns
	t_f	–	–	30	
Output Transition Times, All Outputs Except Tx Car (From 10% to 90% Points)	t_r	–	–	5.0	µs
	t_f	–	–	5.0	
V_{DD} Supply Current (All Inputs at V_{SS} and All Outputs Open)	I_{DD}	–	30	65	mAdc

*Maximum Input Transition Times are ≤ 0.1 x Pulse Width or the specified maximum of 1.0 µs, whichever is smaller.

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FIGURE 2 – TYPICAL MC6860 SYSTEM CONFIGURATION

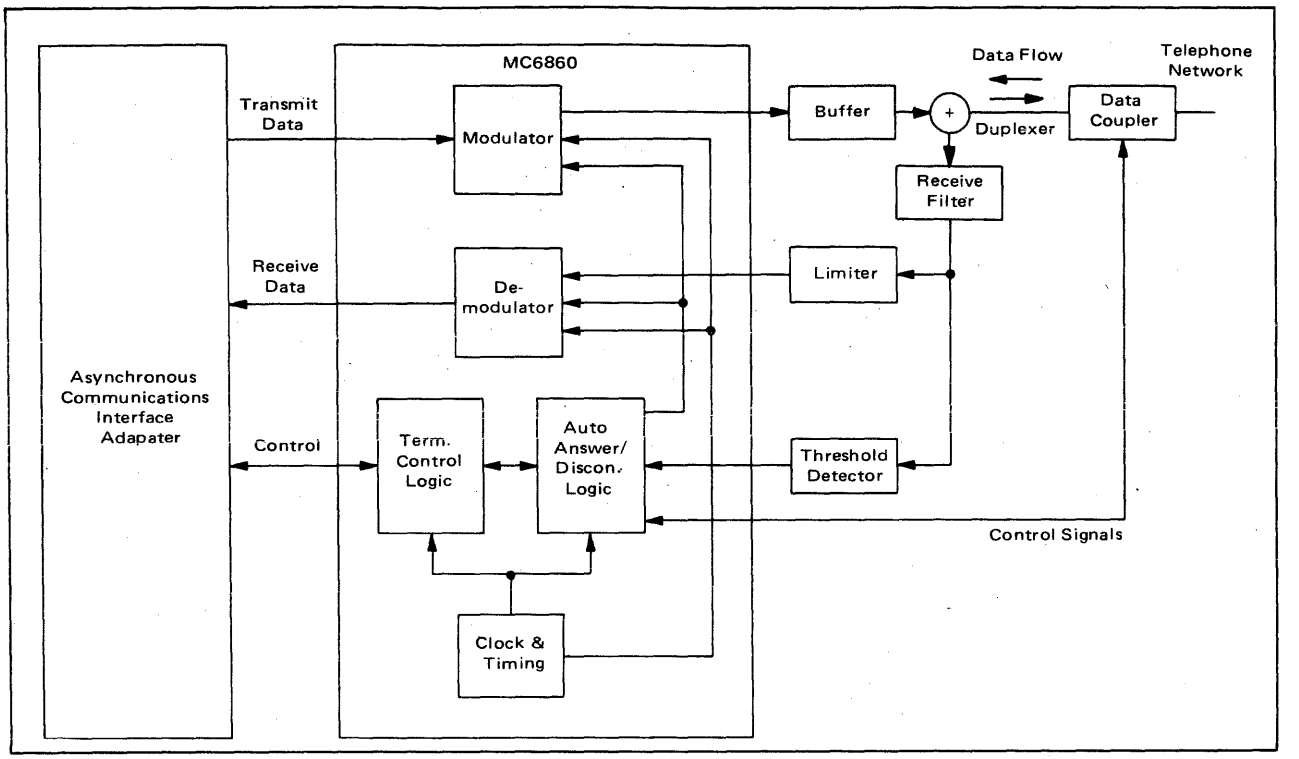
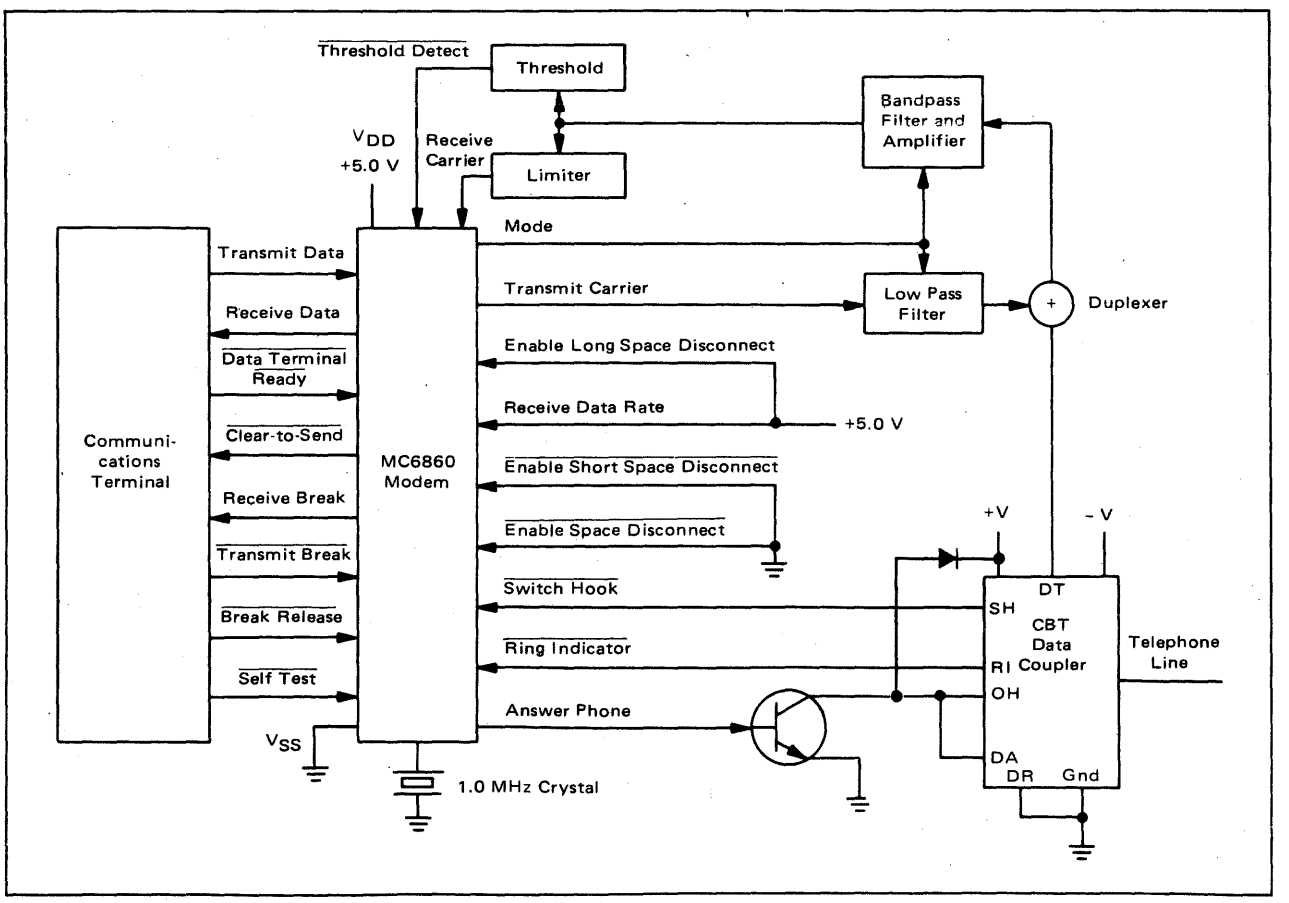


FIGURE 3 – I/O INTERFACE CONNECTIONS FOR MC6860 (ORIGINATE/ANSWER MODEM)



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MC6854 (1.0 MHz) MC68A54 (1.5 MHz)
MC68B54 (2.0 MHz)

ADVANCED DATA LINK CONTROLLER (ADLC)

The MC6854 ADLC performs the complex MPU/data communication link function for the "Advanced Data Communication Control Procedure" (ADCCP), High Level Data Link Control (HDLC) and Synchronous Data Link Control (SDLC) standards. The ADLC provides key interface requirements with improved software efficiency. The ADLC is designed to provide the data communications interface for both primary and secondary stations in stand-alone, polling, and loop configurations.

- M6800 Compatible
- Protocol Features
  - Automatic Flag Detection and Synchronization
  - Zero Insertion and Deletion
  - Extendable Address, Control and Logical Control Fields (Optional)
  - Variable Word Length Info Field – 5, 6, 7, or 8-bits
  - Automatic Frame Check Sequence Generation and Check
  - Abort-Detection and Transmission
  - Idle Detection and Transmission
- Loop Mode Operation
- Loop Back Self-Test Mode
- NRZ/NRZI Modes
- Quad Data Buffers for Each Rx and Tx
- Prioritized Status Register (Optional)
- MODEM/DMA/Loop Interface
- MIL-STD-883, Class B and C Devices Available

FIGURE 11 – I/O PIN DESCRIPTION

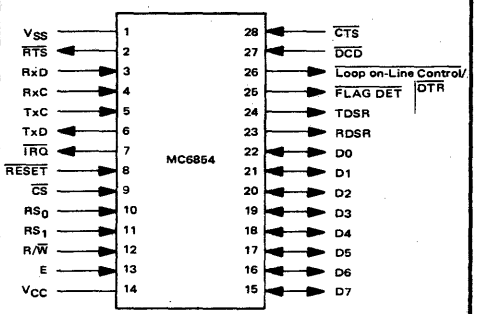
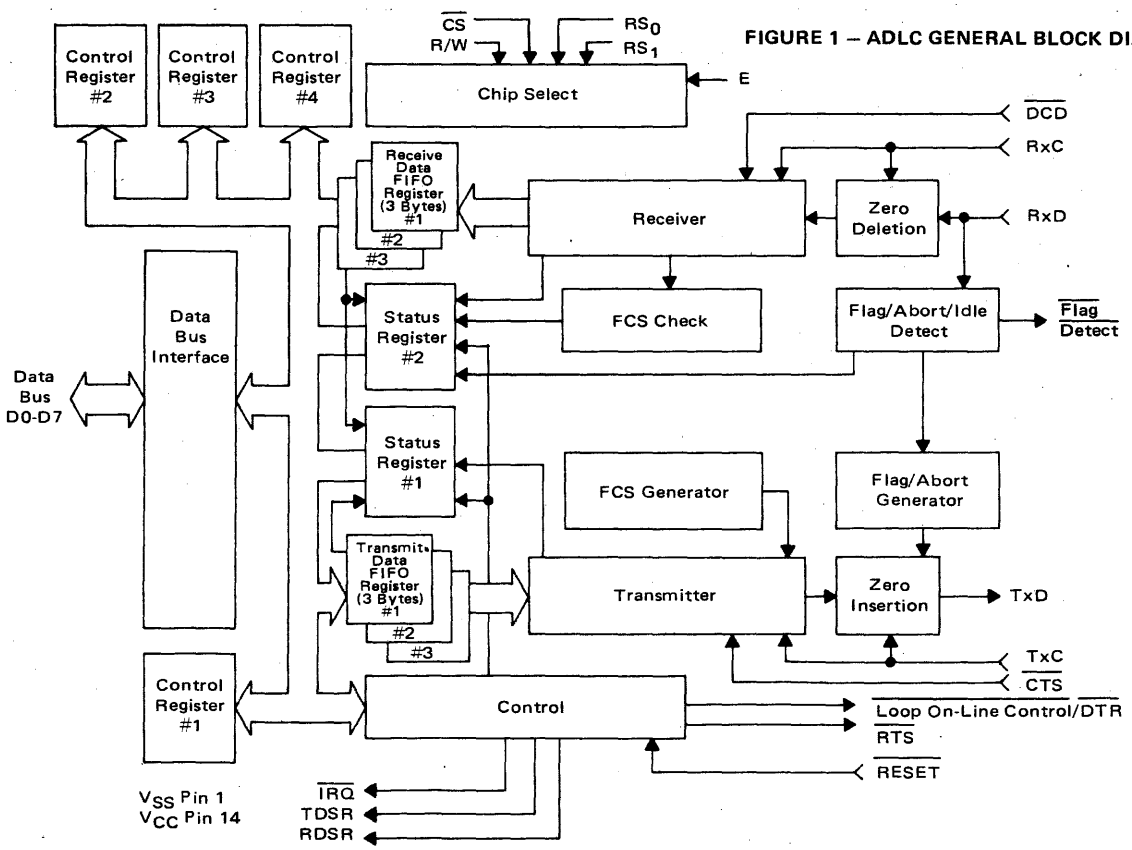


FIGURE 1 – ADLC GENERAL BLOCK DIAGRAM



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DS9495
(Replaces ADI-432)

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FIGURE 8A – ADLC TRANSMITTER STATE DIAGRAM
(C_ib_i refers to control register bit)

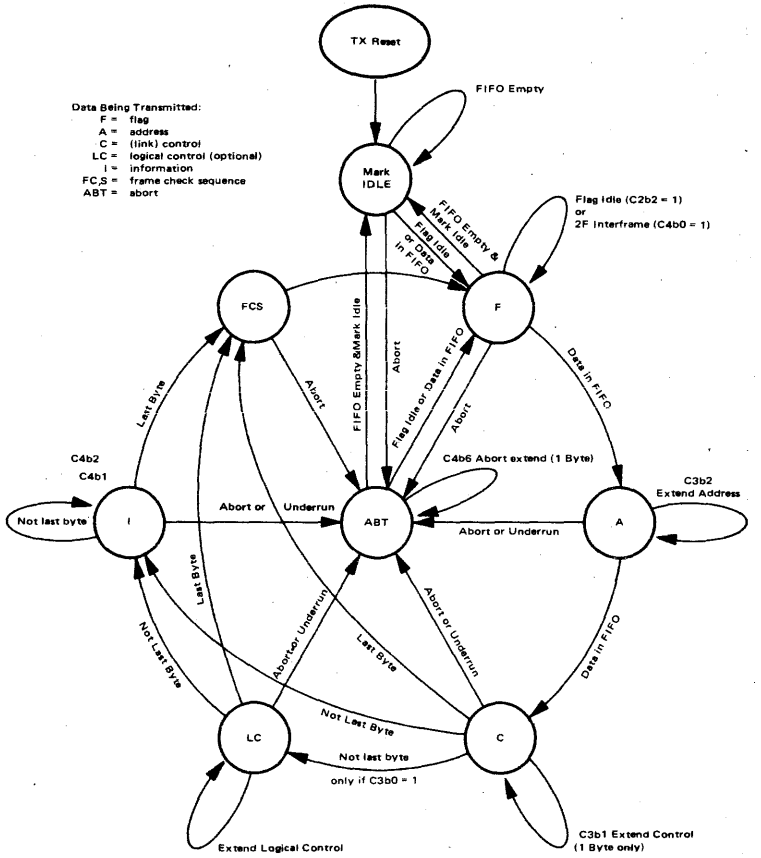
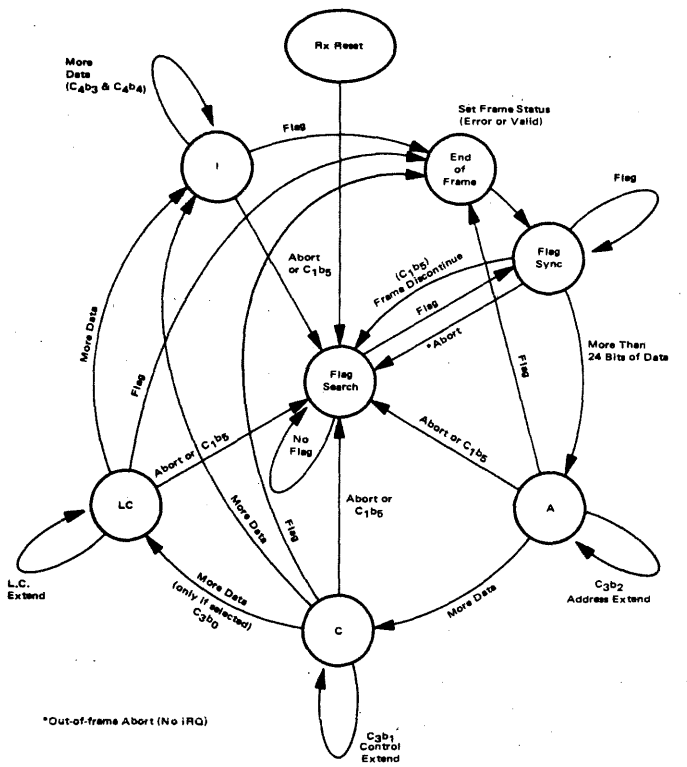


FIGURE 8B – ADLC RECEIVER STATE DIAGRAM



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MC6852
(1.0 MHz)

MC68A52
(1.5 MHz)

MC68B52
(2.0 MHz)

SYNCHRONOUS SERIAL DATA ADAPTER (SSDA)

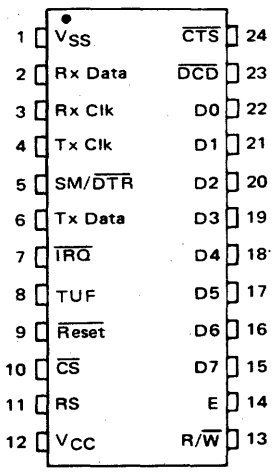
The MC6852 Synchronous Serial Data Adapter provides a bi-directional serial interface for synchronous data information interchange. It contains interface logic for simultaneously transmitting and receiving standard synchronous communications characters in bus organized systems such as the M6800 Microprocessor systems.

The bus interface of the MC6852 includes select, enable, read/write, interrupt, and bus interface logic to allow data transfer over an 8-bit bi-directional data bus. The parallel data of the bus system is serially transmitted and received by the synchronous data interface with synchronization, fill character insertion/deletion, and error checking. The functional configuration of the SSDA is programmed via the data bus during system initialization. Programmable control registers provide control for variable word lengths, transmit control, receive control, synchronization control, and interrupt control. Status, timing and control lines provide peripheral or modem control.

Typical applications include floppy disk controllers, cassette or cartridge tape controllers, data communications terminals, and numerical control systems.

- Programmable Interrupts from Transmitter, Receiver, and Error Detection Logic
- Character Synchronization on One or Two Sync Codes
- External Synchronization Available for Parallel-Serial Operation
- Programmable Sync Code Register
- Up to 600 kbps Transmission
- Peripheral/Modem Control Functions
- Three Bytes of FIFO Buffering on Both Transmit and Receive
- Seven, Eight, or Nine Bit Transmission
- Optional Even and Odd Parity
- Parity, Overrun, and Underflow Status

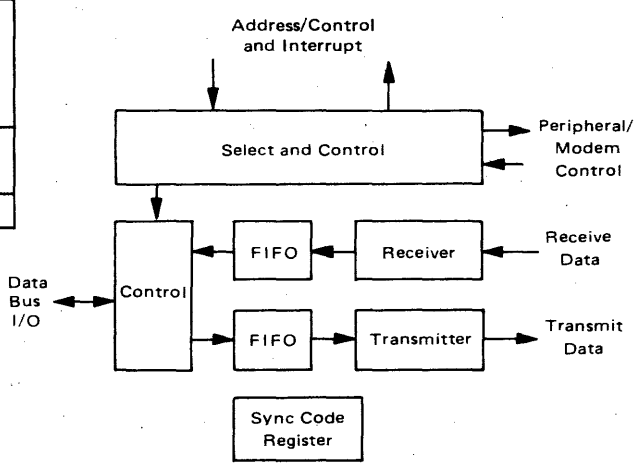
PIN ASSIGNMENT



ORDERING INFORMATION

Speed	Device	Temperature Range
1.0 MHz	MC6852P,L	0 to 70°C
	MC6852CP,CL	–40 to +85°C
MIL-STD-883B	MC6852BJCS	–55 to +125°C
MIL-STD-883C	MC6852CJCS	
1.5 MHz	MC68A52P,L	0 to +70°C
	MC68A52CP,CL	–40 to +85°C
2.0 MHz	MC68B52P,L	0 to +70°C

MC6852 SYNCHRONOUS SERIAL DATA ADAPTER BLOCK DIAGRAM



MICROPROCESSOR

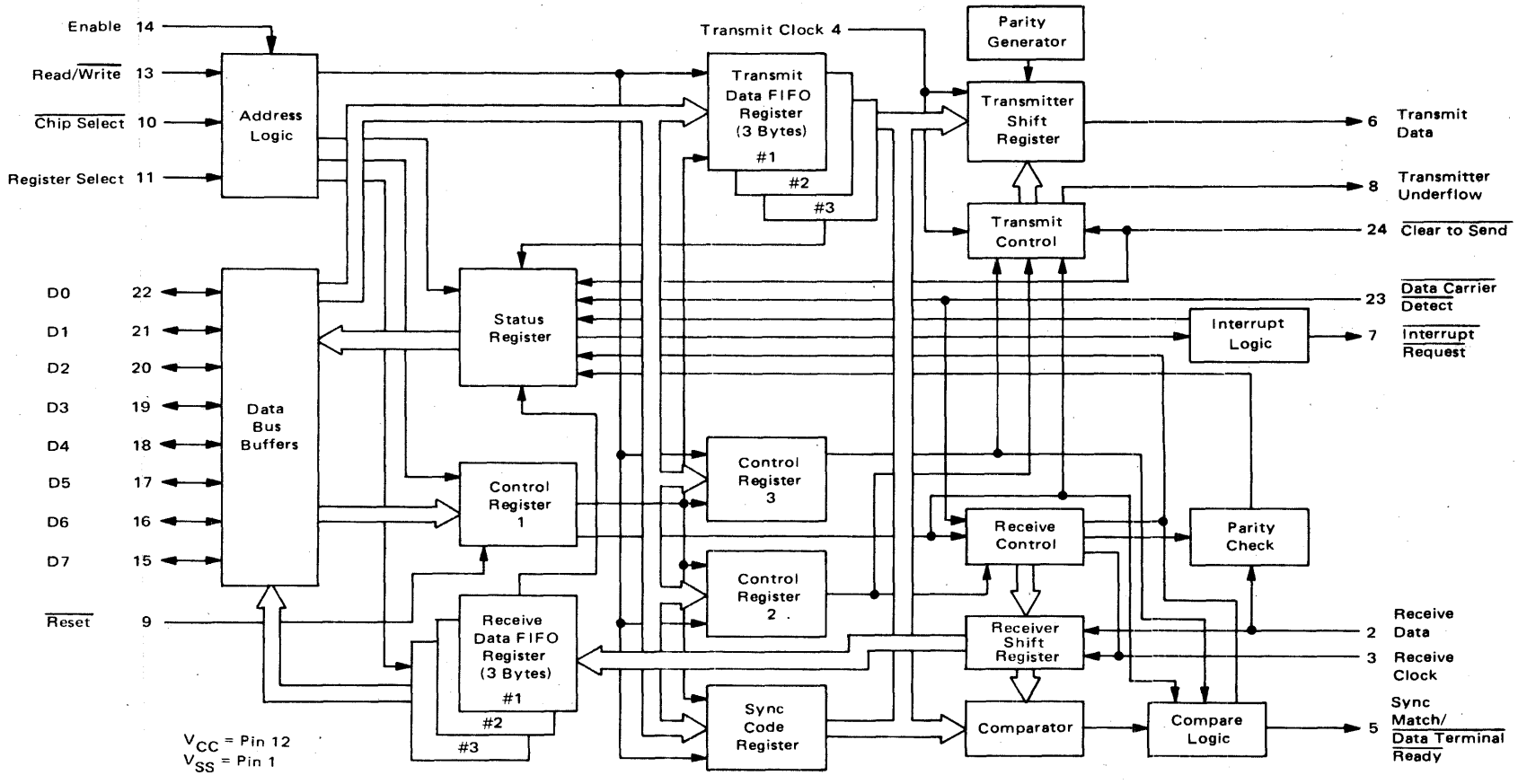
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DS 9494 R1

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EXPANDED BLOCK DIAGRAM



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MC68488

GENERAL PURPOSE INTERFACE ADAPTER

The MC68488 GPIA provides the means to interface between the IEEE488 standard instrument bus and the MC6800. The 488 instrument bus provides a means for controlling and moving data from complex systems of multiple instruments.

The MC68488 will automatically handle all handshake protocol needed on the instrument bus.

- Single or dual primary address recognition
- Secondary address capability
- Complete source and acceptor handshakes
- Programmable interrupts
- RFD holdoff to prevent data overrun
- Operates with DMA controller
- Serial and parallel polling capability
- Talk-only or listen-only capability
- Selectable automatic features to minimize software
- Synchronization trigger output
- M6800 bus compatible

FIGURE 4 – PIN ASSIGNMENT

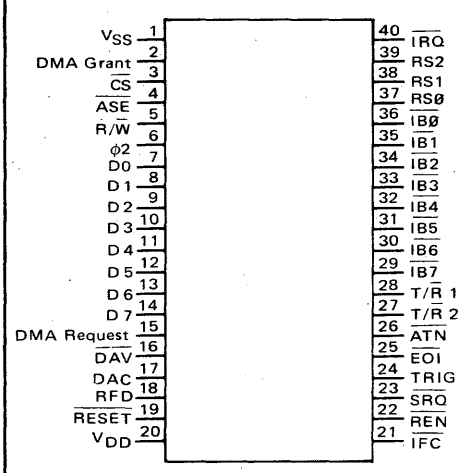
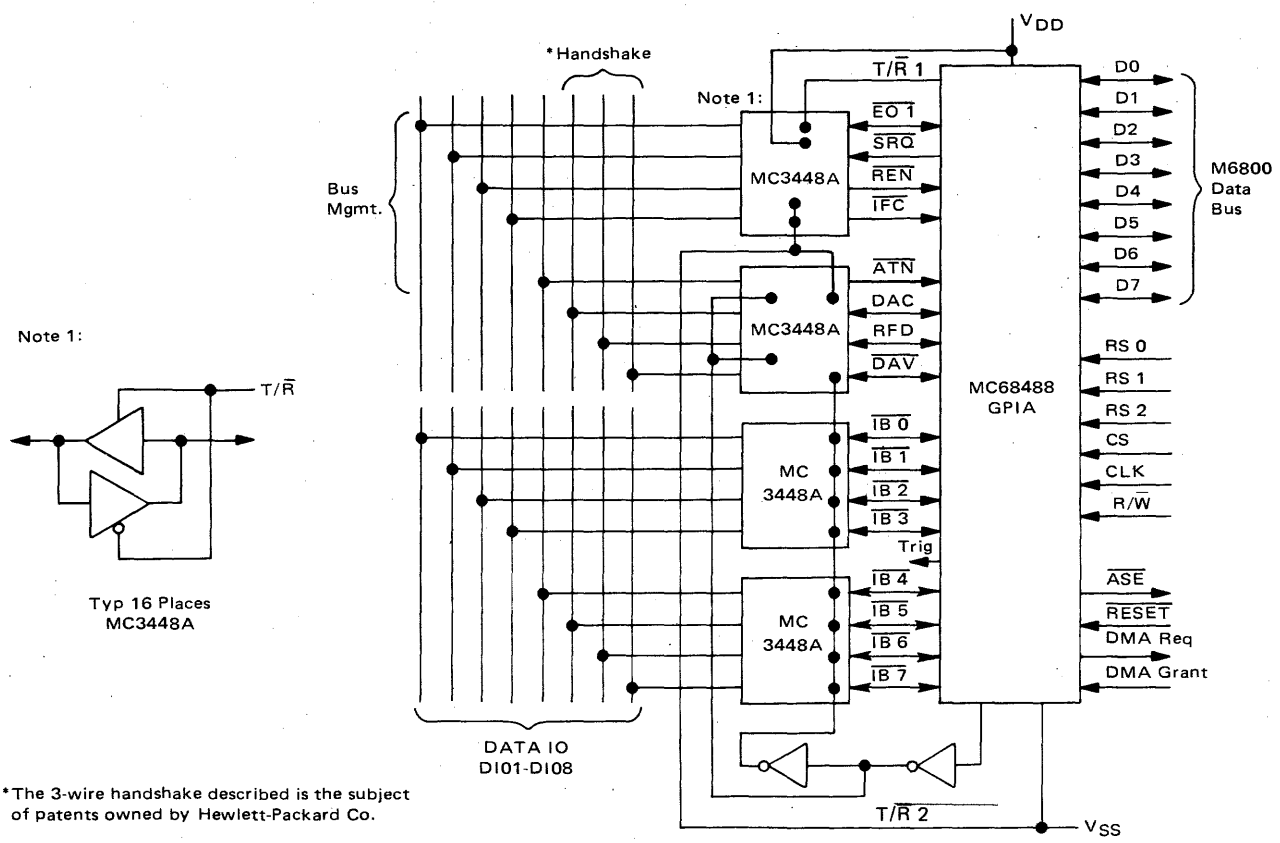


FIGURE 1



*The 3-wire handshake described is the subject of patents owned by Hewlett-Packard Co.

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ADI-462
(Replaces NP-69)

GENERAL DESCRIPTION

The IEEE 488 instrument bus standard is a bit-parallel, byte-serial bus structure designed for communication to and from intelligent instruments. Using this standard, many instruments may be interconnected and remotely and automatically controlled or programmed. Data may be taken from, sent to, or transferred between instruments. A bus controller dictates the role of each device by making the attention line true and sending talk or listen addresses on the instrument bus data lines; those devices which have matching addresses are activated. Device addresses are set into each GPIA from switches or jumpers on a PC board by a microprocessor as a part of the initialization sequence.

When the controller makes the attention line true, instrument bus commands may also be sent to single or multiple GPIA's.

Information is transmitted on the instrument bus data lines under sequential control of the three handshake lines. No step in the sequence can be initiated until the previous step is completed. Information transfer can proceed as fast as the devices can respond, but no faster than the slowest device presently addressed as active. This permits several devices of different speeds to receive the same data concurrently.

The GPIA is designed to work with standard 488-bus driver IC's (MC3448A's) to meet the complete electrical specifications of the IEEE 488 bus. Additionally, a powered-off instrument may be powered-on without disturbing the 488 bus. With some additional logic, the GPIA could be used with other microprocessors.

The MC68488 GPIA has been designed to interface between the MC6800 microprocessor and the complex protocol of the IEEE 488 instrument bus. Many instrument bus protocol functions are handled automatically by the GPIA and require no additional MPU action. Other functions require minimum MPU response due to a large number of internal registers conveying information on the state of the GPIA and the instrument bus.

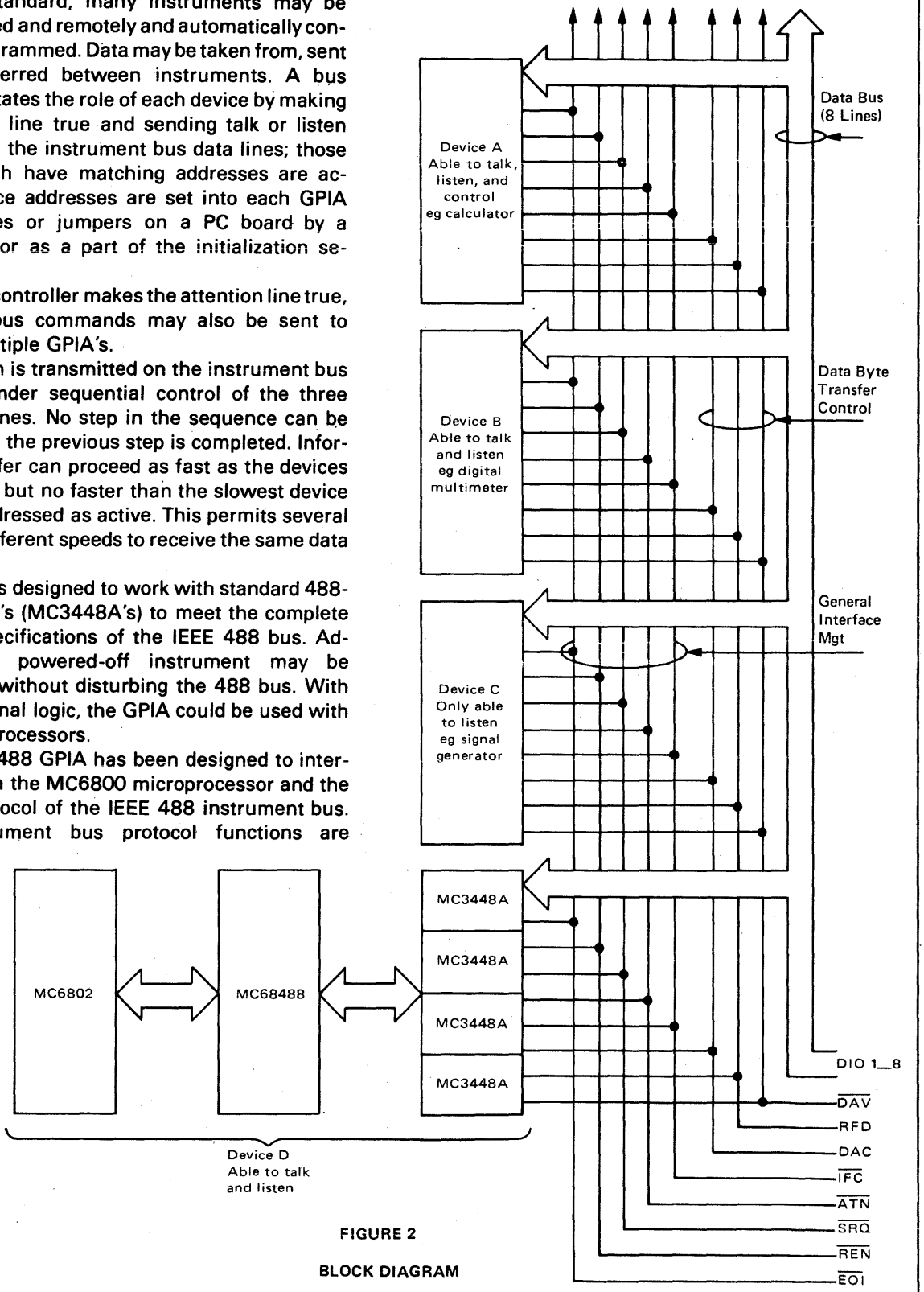


FIGURE 2

BLOCK DIAGRAM

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MC6850

(0 to 70°C; L or P Suffix)

MC6850C

(-40 to 85°C; L Suffix only)

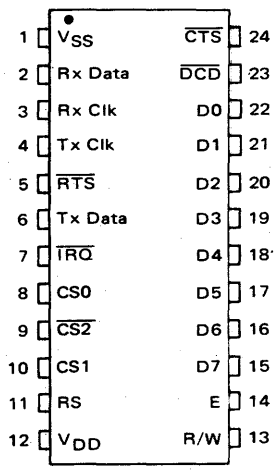
ASYNCHRONOUS COMMUNICATIONS INTERFACE ADAPTER (ACIA)

The MC6850 Asynchronous Communications Interface Adapter provides the data formatting and control to interface serial asynchronous data communications information to bus organized systems such as the MC6800 Microprocessing Unit.

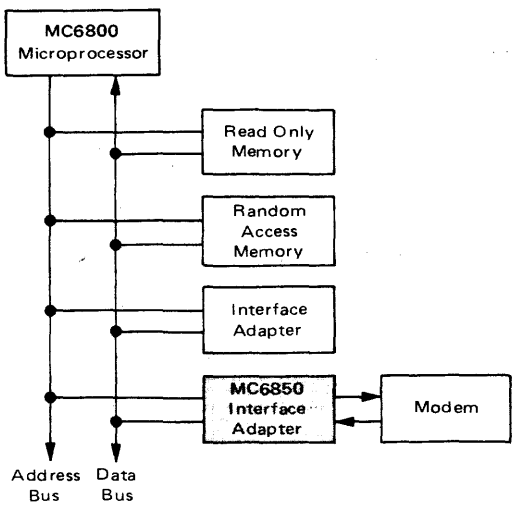
The bus interface of the MC6850 includes select, enable, read/write, interrupt and bus interface logic to allow data transfer over an 8-bit bi-directional data bus. The parallel data of the bus system is serially transmitted and received by the asynchronous data interface, with proper formatting and error checking. The functional configuration of the ACIA is programmed via the data bus during system initialization. A programmable Control Register provides variable word lengths, clock division ratios, transmit control, receive control, and interrupt control. For peripheral or modem operation three control lines are provided. These lines allow the ACIA to interface directly with the MC6860L 0-600 bps digital modem.

- Eight and Nine-Bit Transmission
- Optional Even and Odd Parity
- Parity, Overrun and Framing Error Checking
- Programmable Control Register
- Optional ÷1, ÷16, and ÷64 Clock Modes
- Up to 500 kbps Transmission
- False Start Bit Deletion
- Peripheral/Modem Control Functions
- Double Buffered
- One or Two Stop Bit Operation

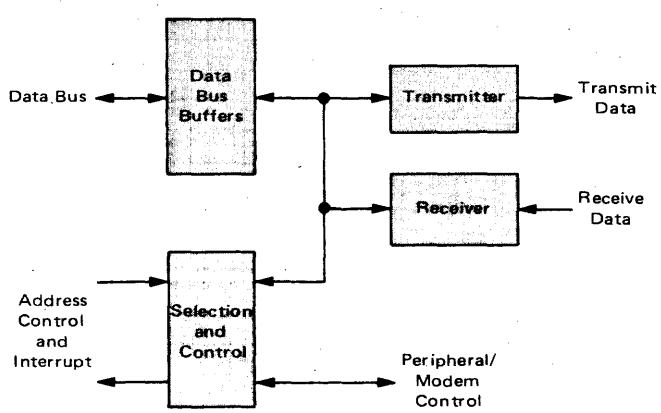
PIN ASSIGNMENT



M6800 MICROCOMPUTER FAMILY BLOCK DIAGRAM



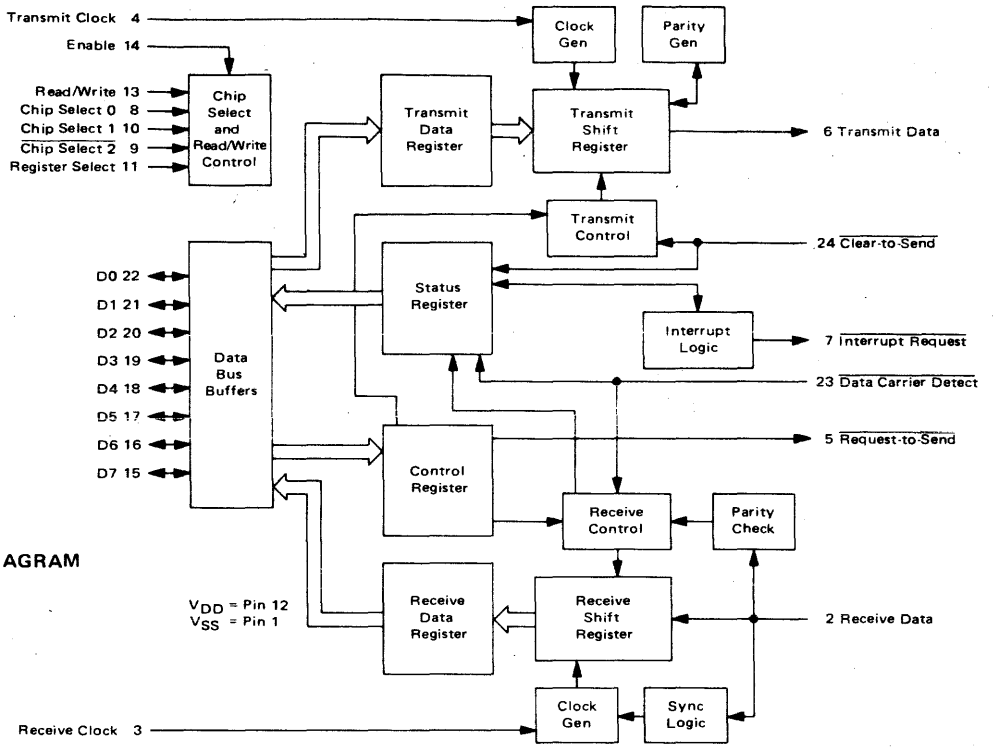
MC6850 ASYNCHRONOUS COMMUNICATIONS INTERFACE ADAPTER BLOCK DIAGRAM



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EXPANDED BLOCK DIAGRAM

ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V ±5%, V_{SS} = 0, T_A = 0 to 70°C unless otherwise noted.)

Characteristic		Symbol	Min	Typ	Max	Unit
Input High Voltage		V_{IH}	V_{SS} + 2.0	–	V_{CC}	Vdc
Input Low Voltage		V_{IL}	V_{SS} -0.3	–	V_{SS} + 0.8	Vdc
Input Leakage Current (V_{in} = 0 to 5.25 Vdc)	R/W,CS0,CS1,$\overline{CS2}$,Enable	I_{in}	–	1.0	2.5	µAdc
Three-State (Off State) Input Current (V_{in} = 0.4 to 2.4 Vdc)	D0-D7	I_{TSI}	–	2.0	10	µAdc
Output High Voltage	D0-D7	V_{OH}				Vdc
(I_{Load} = -205 µAdc, Enable Pulse Width <25 µs)			V_{SS} + 2.4	–	–	
(I_{Load} = -100 µAdc, Enable Pulse Width <25 µs)	Tx Data, $\overline{RTS}$		V_{SS} + 2.4	–	–	
Output Low Voltage (I_{Load} = 1.6 mAdc, Enable Pulse Width <25 µs)		V_{OL}	–	–	V_{SS} + 0.4	Vdc
Output Leakage Current (Off State) (V_{OH} = 2.4 Vdc)	$\overline{IRQ}$	I_{LOH}	–	1.0	10	µAdc
Power Dissipation		P_D	–	300	525	mW
Input Capacitance		C_{in}				pF
(V_{in} = 0, T_A = 25°C, f = 1.0 MHz)	D0-D7		–	10	12.5	
	E, Tx Clk, Rx Clk, R/W, RS, Rx Data, CS0, CS1, $\overline{CS2}$, $\overline{CTS}$, $\overline{DCD}$		–	7.0	7.5	
Output Capacitance (V_{in} = 0, T_A = 25°C, f = 1.0 MHz)	$\overline{RTS}$, Tx Data	C_{out}	–	–	10	pF
	$\overline{IRQ}$		–	–	5.0	
Minimum Clock Pulse Width, Low (Figure 1)	÷16, ÷64 Modes	PW_{CL}	600	–	–	ns
Minimum Clock Pulse Width, High (Figure 2)	÷16, ÷64 Modes	PW_{CH}	600	–	–	ns
Clock Frequency	÷1 Mode	f_C	–	–	500	kHz
	÷16, ÷64 Modes		–	–	800	
Clock-to-Data Delay for Transmitter (Figure 3)		t_{TDD}	–	–	1.0	µs
Receive Data Setup Time (Figure 4)	÷1 Mode	t_{RDSU}	500	–	–	ns
Receive Data Hold Time (Figure 5)	÷1 Mode	t_{RDH}	500	–	–	ns
$\overline{Interrupt\ Request}$ Release Time (Figure 6)		t_{IR}	–	–	1.2	µs
$\overline{Request\text{-}to\text{-}Send}$ Delay Time (Figure 6)		t_{RTS}	–	–	1.0	µs
Input Transition Times (Except Enable)		t_r,t_f	–	–	1.0*	µs

*1.0 µs or 10% of the pulse width, whichever is smaller.

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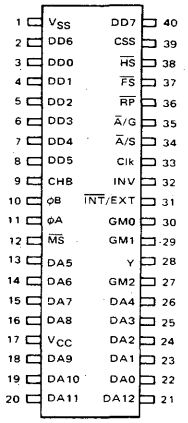
MC6847
NONINTERLACE
MC6847Y
INTERLACE

VIDEO DISPLAY GENERATOR (VDG)

The Motorola MC6847 Video Display Generator (VDG) provides a means of interfacing the Motorola M6800 microprocessor family (or similar products) to a commercially available color or black and white television receiver. Applications of the VDG include video games, bioengineering displays, education, communications and any place graphics are required.

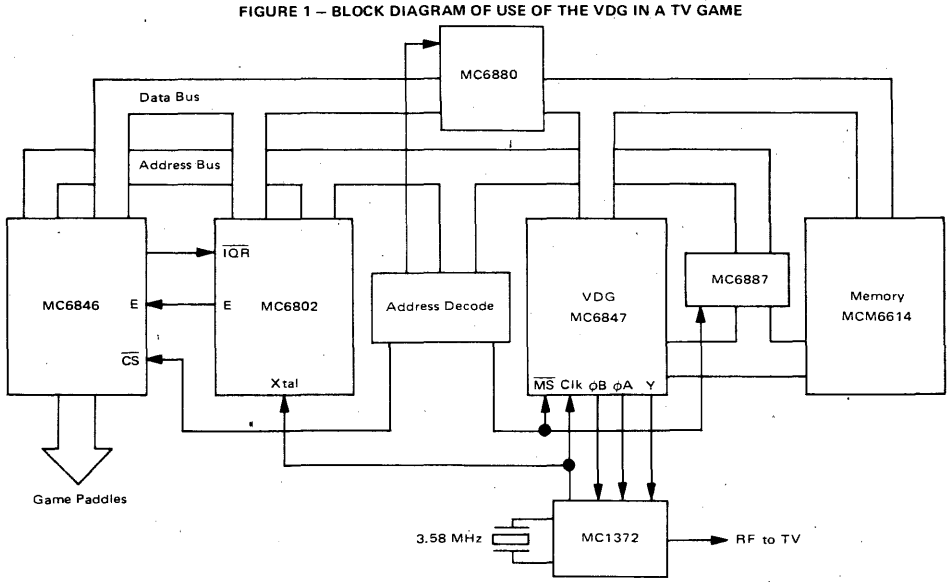
The VDG reads data from memory and produces a composite video signal which will allow the generation of alphanumeric or graphic displays. The generated composite video may be up modulated to either Channel 3 or 4 by using the compatible MC1372 (TV Chroma and Video modulator). The up modulated signal is suitable for application to the antenna of a color TV. A typical TV game is indicated in Figure 1.

PIN ASSIGNMENT



- Generates four different alphanumeric display modes and eight graphic display modes
- Compatible with the M6800 family
- Compatible with the MC1372 modulator
- The alphanumeric modes display 32 characters per line by 16 lines
- An internal multiplexer allows the use of either the internal ROM or an external character generator
- An external character generator can be used to extend the internal character set for "limited graphic" shapes
- A Mask Programmable internal character generator ROM is available on special order (Appendix A)
- One display mode offers 8-color 64 x 32 density graphics in an alphanumeric display mode
- One display mode offers 4-color 64 x 48 density graphics in an alphanumeric display mode
- All alphanumeric modes have a selectable video inverse
- Generates full composite video signal
- Generates R-Y and B-Y signals for external color modulator
- Full-graphic modes offer 64 x 64, 128 x 64, 128 x 96, 128 x 192, or 256 x 192 densities
- Full-graphic modes allow 2-color or 4-color data structures
- Full-graphic modes use one of two 4-color sets or one of two 2-color sets
- Available in either an interlace mode (NTSC Standard) or a non-interlace mode

FIGURE 1 – BLOCK DIAGRAM OF USE OF THE VDG IN A TV GAME



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TABLE 3 – DETAILED DESCRIPTION OF VDG MODES

VDG PINS									COLOR			TV SCREEN		VDG DATA BUS	COMMENTS
MS	A/G	A/S	INT/EXT	GM2	GM1	GM0	CSS	INV	Character Color	Background	Border	Display Mode	Detail		
1	0	0	0	X	X	X	0	0	Green	Black	Black	32 Characters in columns 16 Characters in rows	8 dots, 12 dots, 7, 5	extra, ASCII code	The ALPHA-NUMERIC INTERNAL mode uses an internal character generator which contains the following five dot by seven dot characters: @ABCDEFGHIJK LMNOPQRSTUVWXYZ [/] ↑ ← SP ! # $ % & ' ( ) * + , - . / 0123456789 : ; < = > ? The six bit ASSCII code leaves two bits free and these may be externally connected to the mode pins (A/G, A/S, INT/EXT, GM2, GM1, GM0, CSS or INV).
								1	Black	Green					
							1	0	Orange	Black					
								1	Black	Orange					
1	0	0	1	X	X	X	0	0	Green	Black	Black	32 Characters in columns 16 Characters in rows		one row of custom characters	The ALPHA-NUMERIC EXTERNAL mode uses an external character generator as well as a row counter. Thus, custom character fonts are graphic symbol sets with up to 256 different eight dot X 12 dot "characters" may be displayed.
								1	Black	Green					
							1	0	Orange	Black					
								1	Black	Orange					
1	0	1	0	X	X	X	X	X	Lx C2 C1 C0 Color 0 X X X Black 1 0 0 0 Green 1 0 0 1 Yellow 1 0 1 0 Blue 1 0 1 1 Red 1 1 0 0 Buff 1 1 0 1 Cyan 1 1 1 0 Magenta 1 1 1 1 Orange		Black	64 Display elements in columns 32 Display elements in rows	L_3 L_2 / L_1 L_0 one element	C_2 C_1 C_0 L_3 L_2 L_1 L_0	The SEMIGRAPHICS FOUR mode uses an internal "course graphics" generator in which a rectangle (eight dots by twelve dots) is divided into four equal parts. The luminance of each part is determined by a corresponding bit on the VDC data bus. The color of illuminated parts is determined by three bits.
1	0	1	1	X	X	X	0	X	Lx C1 C0 Color 0 X X Black 1 0 0 Green 1 0 1 Yellow 1 1 0 Blue 1 1 1 Red 0 X X Black 1 0 0 Buff 1 0 1 Cyan 1 1 0 Magenta 1 1 1 Orange		Black	64 Display elements in columns 48 Display elements in rows	L_5 L_4 / L_3 L_2 / L_1 L_0	C_1 C_0 L_5 L_4 L_3 L_2 L_1 L_0	The SEMIGRAPHIC SIX mode is similar to the SEMIGRAPHIC FOUR mode with the following differences: The eight dot by twelve dot rectangle is divided into six equal parts. Color is determined by the two remaining bits.
							1	X							
1	1	X	X	0	0	0	0	X	C1 C0 Color 0 0 Green 0 1 Yellow 1 0 Blue 1 1 Red 0 0 Buff 0 1 Cyan 1 0 Magenta 1 1 Orange		Green	64 Display elements in columns 64 Display elements in rows	E_3 E_2 E_1 E_0	C_1 C_0 C_1 C_0 C_1 C_0 C_1 C_0	The GRAPHICS ONE C mode uses a maximum of 1024 bytes of display RAM in which one pair of bits specifies one picture element.
							1	X			Buff				
1	1	X	X	0	0	1	0	X	Lx 0 Color 1 Black 0 Green 1 Buff		Green Buff	128 Display elements in columns 64 Display elements in rows	L_7 L_6 L_5 L_4 L_3 L_2 L_1 L_0	L_7 L_6 L_5 L_4 L_3 L_2 L_1 L_0	The GRAPHICS ONE R mode uses a maximum of 1024 bytes of display RAM in which one bit specifies one picture element.
							1	X							
1	1	X	X	0	1	0	0	X	Same color as Graphics one C		Green	128 Display elements in columns 64 Display elements in rows	E_3 E_2 E_1 E_0	C_1 C_0 C_1 C_0 C_1 C_0 C_1 C_0	The GRAPHICS TWO C mode uses a maximum of 2048 bytes of display RAM in which one pair of bits specifies one picture element.
							1	X			Buff				
1	1	X	X	0	1	1	0	X	Same color as Graphics one R		Green	128 Display elements in columns 96 Display elements in rows	L_7 L_6 L_5 L_4 L_3 L_2 L_1 L_0	L_7 L_6 L_5 L_4 L_3 L_2 L_1 L_0	The GRAPHICS TWO R mode uses a maximum of 1536 bytes of display RAM in which one bit specifies one picture element.
							1	X			Buff				
1	1	X	X	1	0	0	0	X	Same color as Graphics one C		Green	128 Display elements in columns 96 Display elements in rows	E_3 E_2 E_1 E_0	C_1 C_0 C_1 C_0 C_1 C_0 C_1 C_0	The GRAPHICS THREE C mode uses a maximum of 3072 bytes of display RAM in which one pair of bytes specifies one picture element.
							1	X			Buff				
1	1	X	X	1	0	1	0	X	Same color as Graphics one R		Green	128 Display elements in columns 192 Display elements in rows	L_7 L_6 L_5 L_4 L_3 L_2 L_1 L_0	L_7 L_6 L_5 L_4 L_3 L_2 L_1 L_0	The GRAPHICS THREE R mode uses a maximum of 3072 bytes of display RAM in which one bit specifies one picture element.
							1	X			Buff				
1	1	X	X	1	1	0	0	X	Same color as Graphics one C		Green	128 Display elements in columns 192 Display elements in rows	E_3 E_2 E_1 E_0	C_1 C_0 C_1 C_0 C_1 C_0 C_1 C_0	The GRAPHICS SIX C mode uses a maximum of 6144 bytes of display RAM in which one pair of bits specifies one picture element.
							1	X			Buff				
1	1	X	X	1	1	1	0	X	Same color as Graphics one R		Green	256 Display elements in columns 192 Display elements in rows	L_7 L_6 L_5 L_4 L_3 L_2 L_1 L_0	L_7 L_6 L_5 L_4 L_3 L_2 L_1 L_0	The GRAPHICS SIX R mode uses a maximum of 6144 bytes of display RAM in which one bit specifies one picture element.
							1	X			Buff				

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MC6846

ROM–I/O–TIMER

The MC6846 combination chip provides the means, in conjunction with the MC6802, to develop a basic 2-chip microcomputer system. The MC6846 consists of 2048 bytes of mask-programmable ROM, an 8-bit bidirectional data port with control lines, and a 16-bit programmable timer-counter.

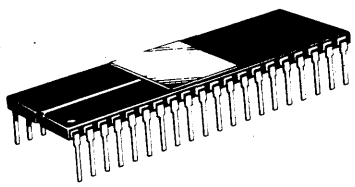
This device is capable of interfacing with the MC6802 (basic MC6800, clock and 128 bytes of RAM) as well as the MC6800 if desired. No external logic is required to interface with most peripheral devices.

- 2048 8-Bit Bytes of Mask-Programmable ROM
- 8-Bit Bidirectional Data Port for Parallel Interface plus Two Control Lines
- Programmable Interval Timer-Counter Functions
- Programmable I/O Peripheral Data, Control and Direction Registers
- Compatible with the Complete M6800 Microcomputer Product Family
- TTL-Compatible Data and Peripheral Lines
- Single 5-Volt Power Supply

MOS

(N-CHANNEL, SILICON-GATE, DEPLETION LOAD)

ROM–I/O–TIMER



L SUFFIX
CERAMIC PACKAGE
CASE 715

NOT SHOWN:
P SUFFIX
PLASTIC PACKAGE
CASE 711

FIGURE 1 – TYPICAL MICROCOMPUTER

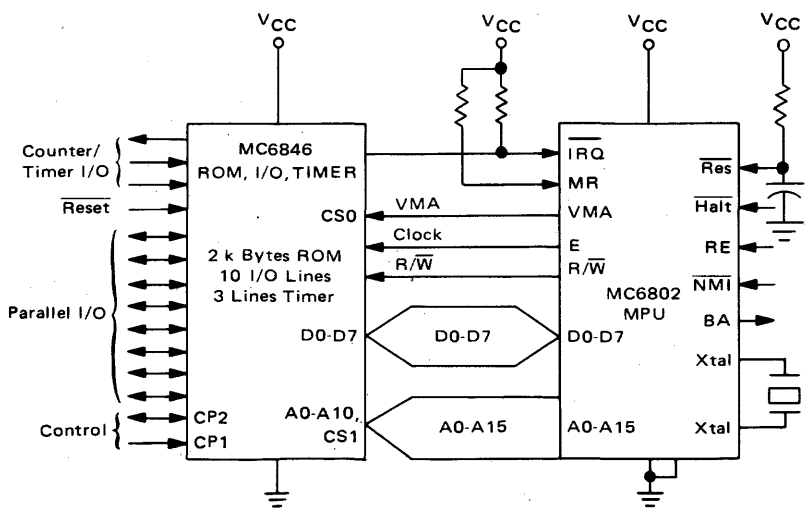
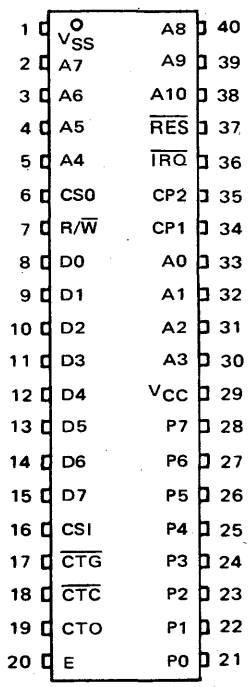


Figure 1 is a block diagram of a typical cost effective microcomputer. The MPU is the center of the microcomputer system and is shown in a minimum system interfacing with a ROM combination chip. It is not intended that this system be limited to this function but that it be expandable with other parts in the M6800 Microcomputer family.

ROM – I/O – TIMER



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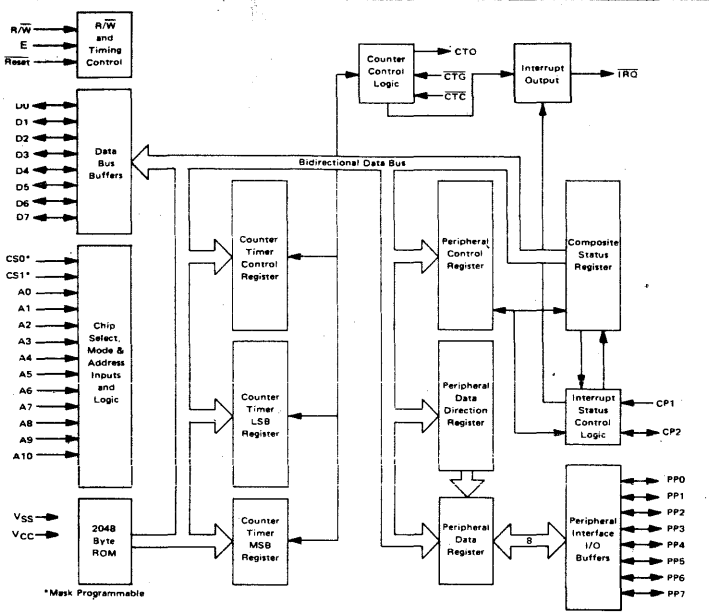


FIGURE 2 – MC6846 BLOCK DIAGRAM

ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V ± 5%, V_{SS} = 0, T_A = 0 to 70°C unless otherwise noted.)

Characteristic		Symbol	Min	Typ	Max	Unit
Input High Voltage	All Inputs	V_{IH}	V_{SS} + 2.0	–	V_{CC}	Vdc
Input Low Voltage	All Inputs	V_{IL}	V_{SS} – 0.3	–	V_{SS} + 0.8	Vdc
Clock Overshoot/Undershoot – Input High Level		V_{OS}	V_{CC} – 0.5	–	V_{CC} + 0.5	Vdc
– Input Low Level			V_{SS} – 0.5	–	V_{SS} + 0.5	
Input Leakage Current	R/W, Reset, CS0, CS1	I_{in}	–	1.0	2.5	μAdc
(V_{in} = 0 to 5.25 Vdc)	CP1, CTG, CTC, E, A0-A10					
Three-State (Off State) Input Current	D0-D7	I_{TSI}	–	2.0	10	μAdc
(V_{in} 0.4 to 2.4 Vdc)	PP0-PP7, CP2					
Output High Voltage		V_{OH}				Vdc
(I_{Load} = -205 μAdc,)	D0-D7		V_{SS} + 2.4	–	–	
(I_{Load} = -200 μAdc)	Other Outputs		V_{SS} + 2.4	–	–	
Output Low Voltage		V_{OL}				Vdc
(I_{Load} = 1.6 mAdc)	D0-D7		–	–	V_{SS} + 0.4	
(I_{Load} = 3.2 mAdc)	Other Outputs		–	–	V_{SS} + 0.4	
Output High Current (Sourcing)		I_{OH}				μAdc
(V_{OH} = 2.4 Vdc)	D0-D7		-205	–	–	
	Other Outputs		-200	–	–	
(V_O = 1.5 Vdc, the current for driving other than TTL, e.g., Darlington Base)	CP2, PP0-PP7		-1.0	–	-10	mAdc
Output Low Current (Sinking)		I_{OL}				mAdc
(V_{OL} = 0.4 Vdc)	D0-D7		1.6	–	–	
	Other Outputs		3.2	–	–	
Output Leakage Current (Off State) (V_{OH} = 2.4 Vdc)	IRQ	I_{LOH}	–	–	10	μAdc
Power Dissipation		P_D	–	–	1000	mW
Capacitance		C_{in}	–	–	20	pF
(V_{in} = 0, T_A = 25°C, f = 1.0 MHz)	D0-D7		–	–	12.5	
	PP0-PP7, CP2		–	–	10	
	A0-A10, R/W, Reset, CS0, CS1, CP1, CTC, CTG, IRQ		–	–	7.5	
	PP0-PP7, CP2, CT0	C_{out}		–	5.0	pF
				–	10	
Frequency of Operation		f	0.1	–	1.0	MHz
Clock Timing						
Cycle Time		t_{cycE}	1.0	–	–	μs
Reset Low Time		t_{RL}	2	–	–	μs
Interrupt Release		t_{IR}	–	–	1.6	μs

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MC6845

CRT CONTROLLER (CRTC)

The MC6845 CRT Controller performs the interface to raster scan CRT displays. It is intended for use in processor-based controllers for CRT terminals in stand-alone or cluster configurations.

The CRTC is optimized for hardware/software balance in order to achieve integration of all key functions and maintain flexibility. For instance, all keyboard functions, R/W, cursor movements, and editing are under processor control; whereas the CRTC provides video timing and Refresh Memory Addressing.

- Applications include "glass-teletype," smart, programmable, intelligent CRT terminals; video games; information display.
- Alphanumeric, semi-graphic, and full graphic capability.
- Fully programmable via processor data bus. Can generate timing for almost any alphanumeric screen density, e.g. 80 x 24, 72 x 64, 132 x 20, etc.
- Single +5 volt supply. TTL/6800 compatible I/O.
- Hardware scroll (paging or by line or by character)
- Compatible with CPU's and MPU's which provide a means for synchronizing external devices.
- Cursor register and compare circuitry.
- Cursor format and blink are programmable.
- Light pen register.
- Line buffer-less operation. No external DMA required. Refresh Memory is multiplexed between CRTC and MPU.
- Programmable interlace or non-interlace scan.
- 14-bit wide refresh address.

PIN ASSIGNMENT

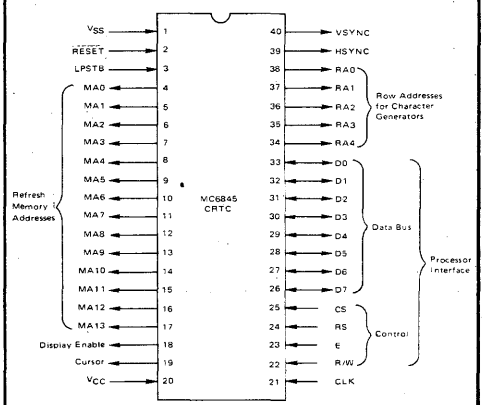
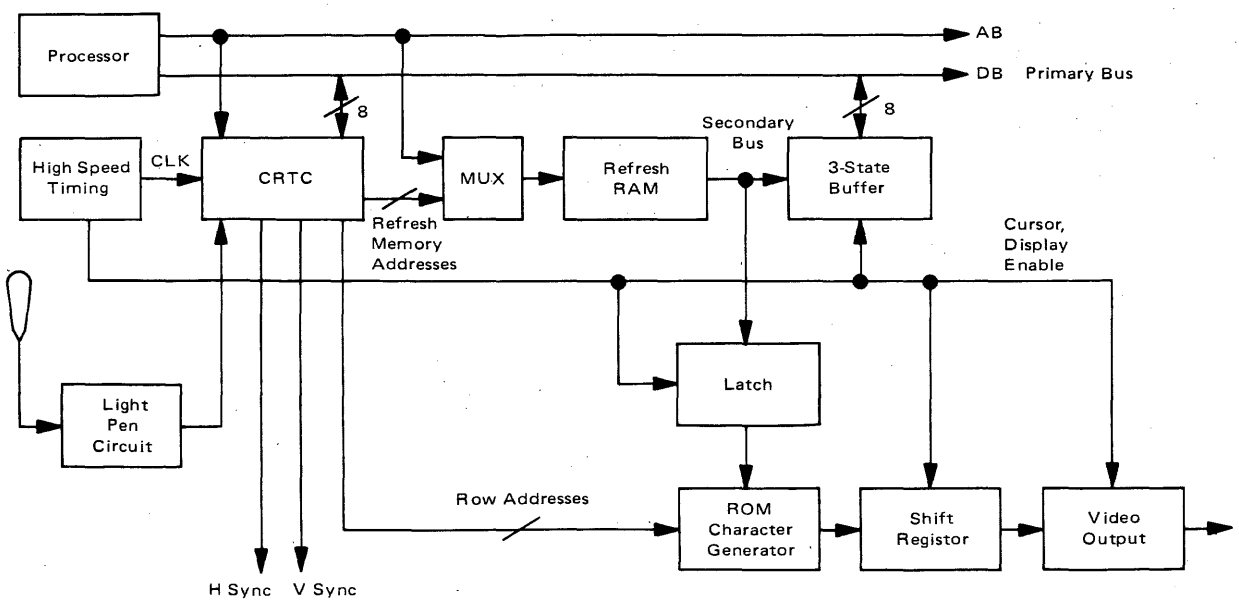


FIGURE 1 – TYPICAL CRT CONTROLLER APPLICATION



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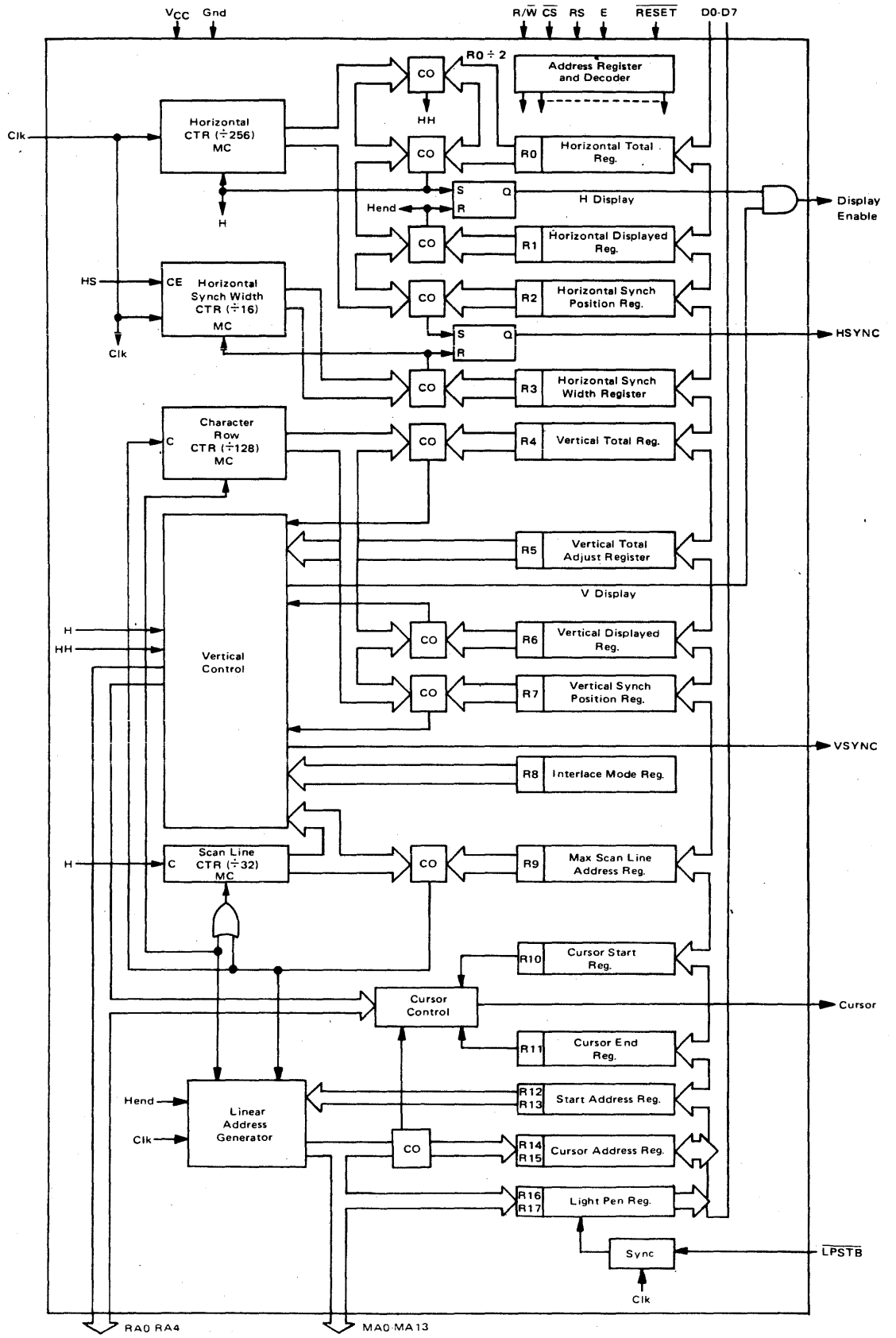
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FIGURE 8 – CRTC FUNCTIONAL BLOCK DIAGRAM



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MC6844

DIRECT MEMORY ACCESS CONTROLLER (DMAC)

The MC6844 Direct Memory Access Controller (DMAC) performs the function of transferring data directly between memory and peripheral device controllers. It controls the address and data buses in place of the MPU in bus organized systems such as the M6800 Microprocessor System.

The bus interface of the MC6844 includes select, read/write, interrupt, transfer request/grant, and bus interface logic to allow the data transfer over an 8-bit bidirectional data bus. The functional configuration of the DMAC is programmed via the data bus. The internal structure provides for control and handling of four individual channels, each of which is separately configured. Programmable control registers provide control for the transfer location and length, individual channel control and transfer mode configuration, priority of servicing, data chaining, and interrupt control. Status and control lines provide control to the peripheral controllers.

The mode of transfer for each channel can be programmed as cycle-stealing or a burst transfer mode.

Typical applications would be with the Floppy Disk Controller (FDC) and the Advanced Data Link Controller (ADLC).

- Four DMA Channels, Each Having a 16-Bit Address Register and a 16-Bit Byte Count Register
- 1 M Byte/Sec Maximum Data Transfer Rate
- Selection of Fixed or Rotating Priority Service Control
- Separate Control Bits for Each Channel
- Data Chain Function
- Address Increment or Decrement Update
- Programmable Interrupts and DMA End to Peripheral Controllers

PIN ASSIGNMENT

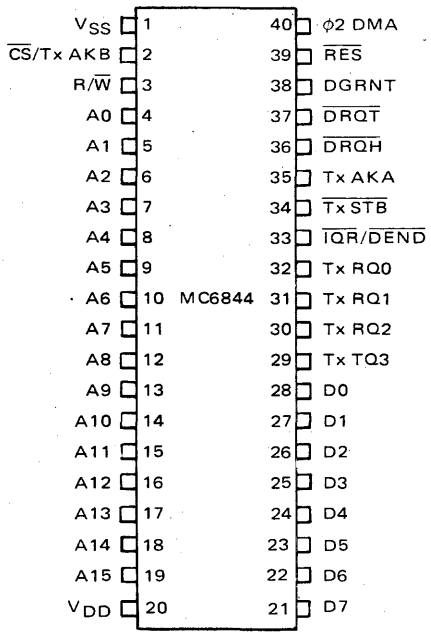


FIGURE 1 – M6800 MICROCOMPUTER FAMILY BLOCK DIAGRAM

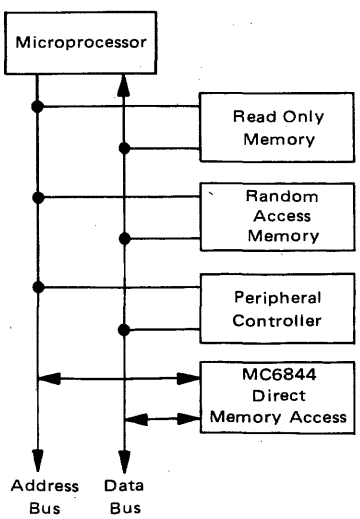
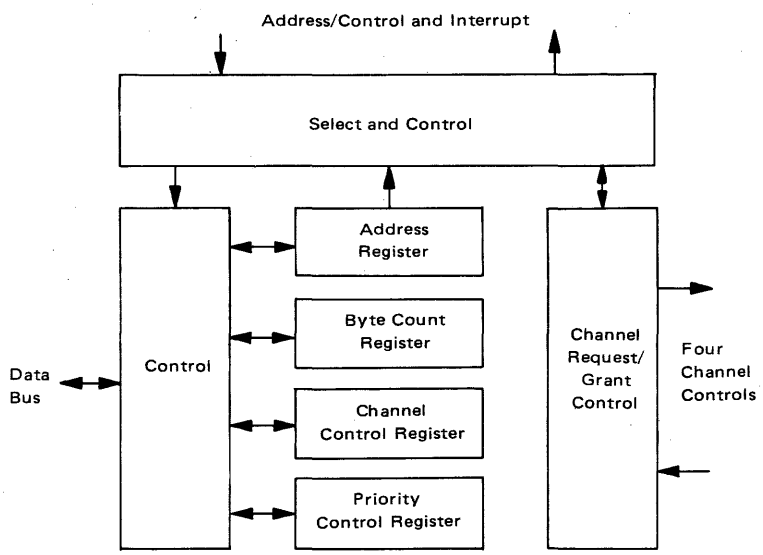


FIGURE 2 – DIRECT MEMORY ACCESS CONTROLLER BLOCK DIAGRAM

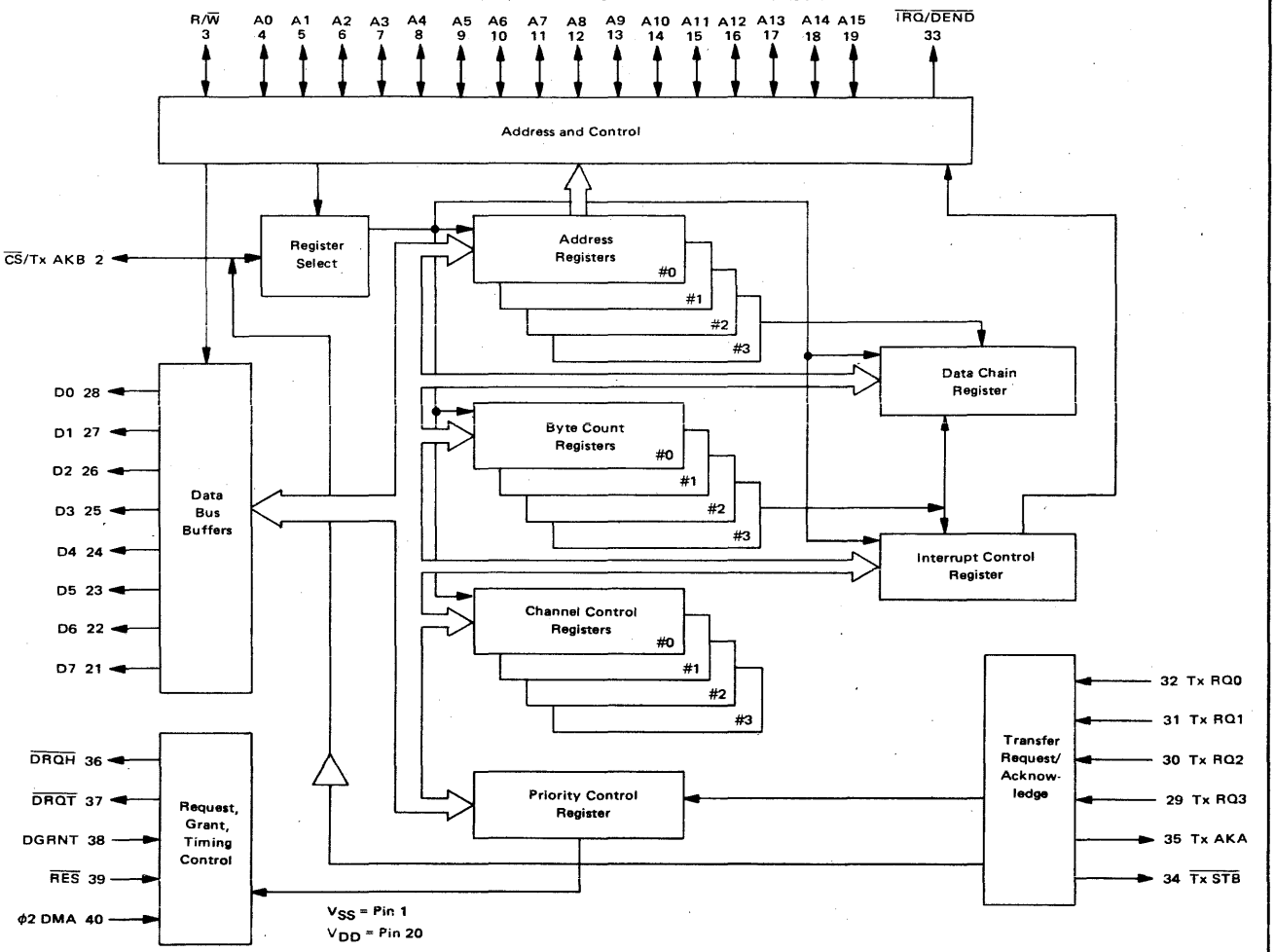


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FIGURE 3 – EXPANDED BLOCK DIAGRAM



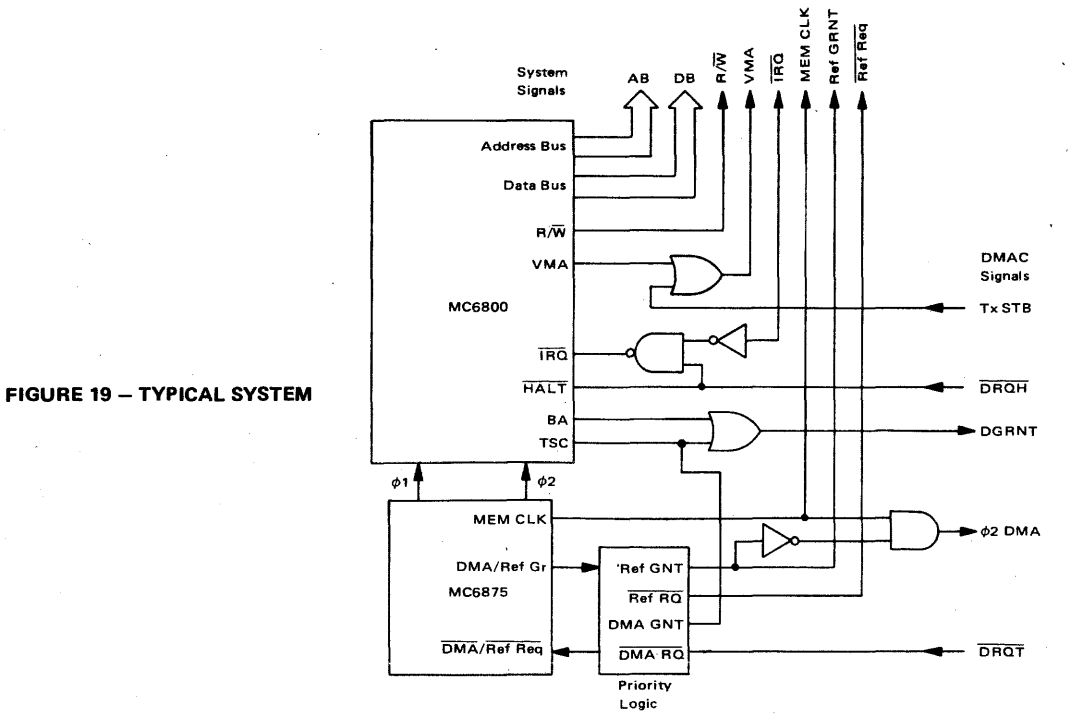


FIGURE 19 – TYPICAL SYSTEM

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MC6843

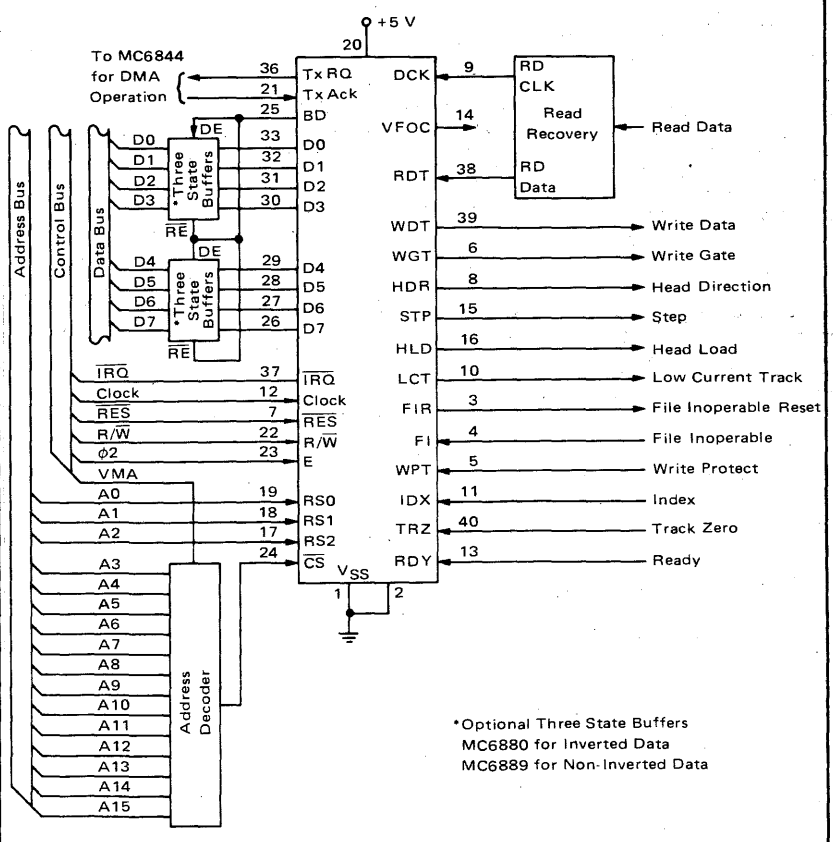
FLOPPY DISK CONTROLLER (FDC)

The MC6843 Floppy Disk Controller performs the complex MPU/Floppy interface function. The FDC was designed to optimize the balance between the "Hardware/Software" in order to achieve integration of all key functions and maintain flexibility.

The FDC can interface a wide range of drives with a minimum of external hardware. Multiple drives can be controlled with the addition of external multiplexing rather than additional FDC's.

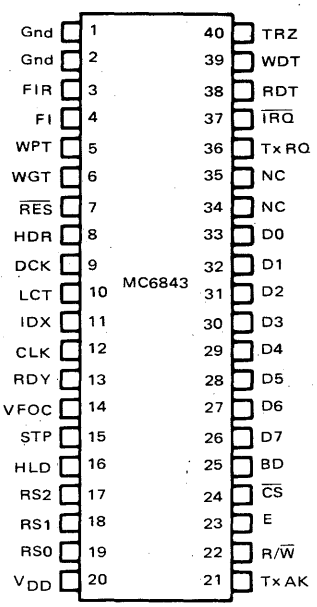
- Format compatible with IBM3740
- User Programmable read/write format
- Ten powerful macro commands
- Macro End Interrupt allows parallel processing of MPU and FDC
- Controls multiple Floppies with external multiplexing
- Direct interface with MC6800
- Programmable step and settling times enable operation with a wide range of Floppy drives
- Offers both Programmed Controlled I/O (PCIO) and DMA data transfer mode
- Free-Format read or write
- Single 5-volt power supply
- All registers directly accessible

FIGURE 1 – SYSTEM BLOCK DIAGRAM



*Optional Three State Buffers
MC6880 for Inverted Data
MC6889 for Non-Inverted Data

FIGURE 2 – PIN ASSIGNMENT



MACRO COMMANDS

Hex Code	Instruction	Hex Code	Instruction
2	STZ	A	FFR
3	SEK	B	FFW
4	SSR	C	MSR
5	SSW	D	MSW
6	RCR		
7	SWD		

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FIGURE 17 –
INTERNAL BLOCK DIAGRAM

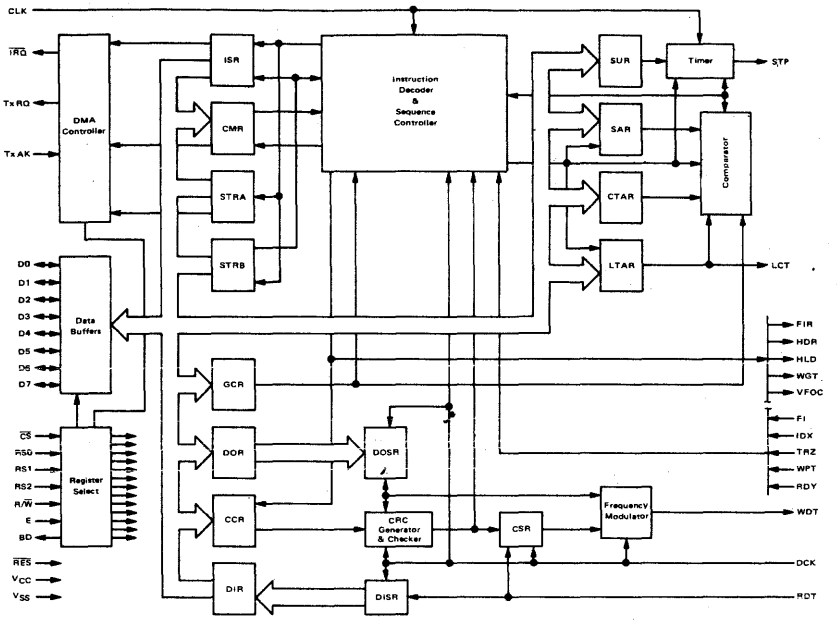


FIGURE 17 – INTERNAL BLOCK DIAGRAM

TABLE 7 – PROGRAMMING REFERENCE DATA

Table 7 is a summary of the information in the data sheet and can be used as a reference when programming the MC6843.

Registers	Hex Address	R/W Mode	Data Bits							
			Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DOR	0	WO	8 Bits of Data Used for a Disk Write Operation							
			Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
DIR	0	RO	8 Bits of Data Used for a Disk Read Operation							
			Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CTAR	1	R/W	Not Used	7 Bit Track Address of Current Head Position						
			Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CMR	2	WO	Function Interrupt Mask	ISR3 Interrupt Mask	DMA Flag	FWF	*	*	*	* Macro Command
			Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ISR	2	RO	Not Used				* STRB	Status * Sense Request	Settling * Time Complete	Macro * Command Complete
			Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SUR	3	WO	Track to Track Seek Time				Head Settling Time			
			Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
STRA	3	RO	* Busy	Index	Track * Not Equal	Write Protect	Track Zero	Drive Ready	Delete * Data Mark Detected	Data * Transfer Request
			Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SAR	4	WO	Not Used			5 Bit Sector Address				
			Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
STRB	4	RO	* Hard Error	* Write Error	File Inoperable	* Seek Error	Sector * Address Undetected	Data * Mark Undetected	* CRC Error	* Data Transfer
			Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
GCR	5	WO	Not Used	7 Bit Count for Track Number on SEK or Sector Count for MSR or MSW.						
			Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CCR	6	WO	Not Used						Shift CRC	CRC Enable
			Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
LTAR	7	WO	Not Used	7 Bit Search Track Address						

RO – Read Only
WO – Write Only
R/W – Read/Write

*Cleared by Reset

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MC6840

PROGRAMMABLE TIMER MODULE (PTM)

The MC6840 is a programmable subsystem component of the M6800 family designed to provide variable system time intervals.

The MC6840 has three 16-bit binary counters, three corresponding control registers and a status register. These counters are under software control and may be used to cause system interrupts and/or generate output signals. The MC6840 may be utilized for such tasks as frequency measurements, event counting, interval measuring and similar tasks. The device may be used for square wave generation, gated delay signals, single pulses of controlled duration, and pulse width modulation as well as system interrupts.

- Operates from a Single 5 Volt Power Supply
- Fully TTL Compatible
- Single System Clock Required (Enable)
- Selectable Prescaler on Timer 3 Capable of a 4 MHz Input
- Programmable Interrupts ($\overline{IRQ}$) Output to MPU
- Readable Down Counter Indicates Counts to Go to Time-Out
- Selectable Gating for Frequency or Pulse-Width Comparison
- $\overline{RESET}$ Input
- Three Asynchronous External Clock and Gate/Trigger Inputs Internally Synchronized
- Three Maskable Outputs

PIN ASSIGNMENT

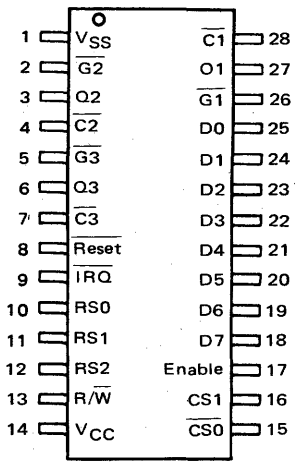
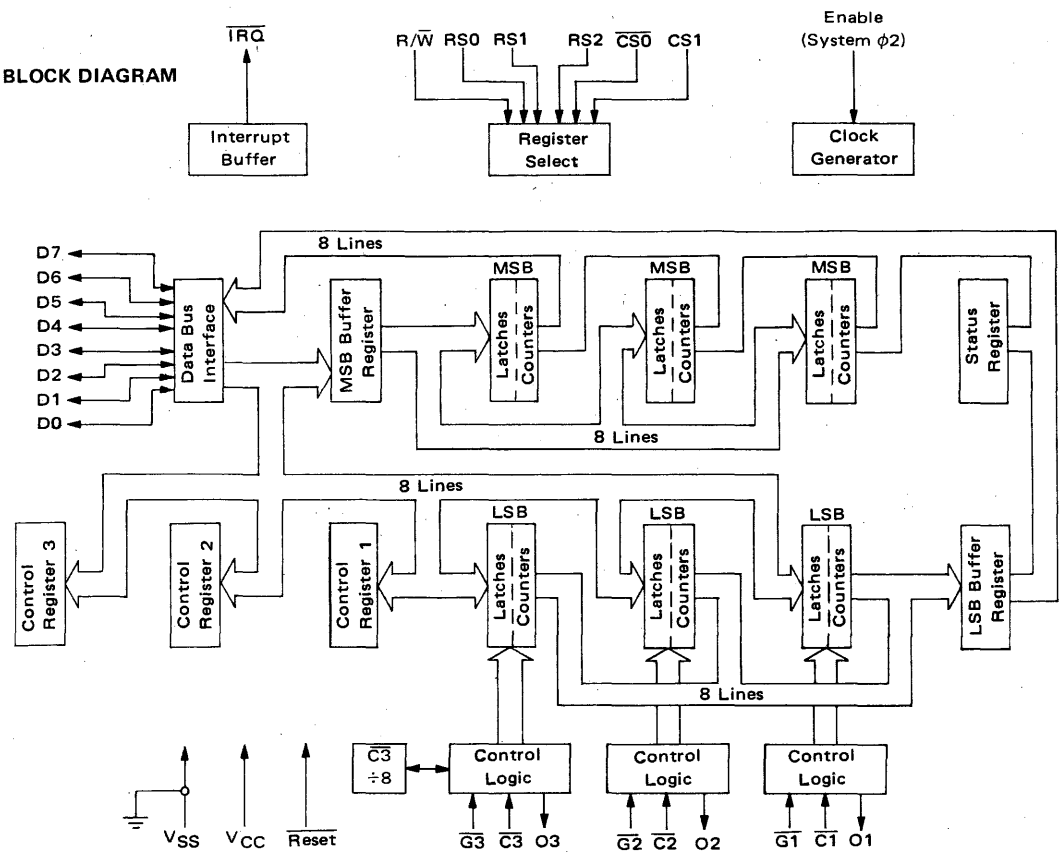


FIGURE 1 – BLOCK DIAGRAM



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ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V ±5%, V_{SS} = 0, T_A = 0 to 70°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
Input High Voltage		V_{IH}	V_{SS} +2.0	–	V_{CC}	Vdc
Input Low Voltage		V_{IL}	V_{SS} -0.3	–	V_{SS} +0.8	
Input Leakage Current (V_{in} = 0 to 5.25 V)		I_{in}	–	1.0	2.5	μAdc
Three-State (Off State) Input Current (V_{in} = 0.4 to 2.4 V)	D0–D7	I_{TSI}	–	2.0	10	μAdc
Output High Voltage		V_{OH}				Vdc
(I_{load} = -205 μA)	D0–D7		V_{SS} +2.4	–	–	
(I_{load} = -200 μA)	Other Outputs		V_{SS} +2.4	–	–	
Output Low Voltage		V_{OL}				Vdc
(I_{load} = 1.6 mA)	D0–D7		–	–	V_{SS} +0.4	
(I_{load} = 3.2 mA)	O1–O3, $\overline{IRQ}$		–	–	V_{SS} +0.4	
Output Leakage Current (Off State) (V_{OH} = 2.4 Vdc)	$\overline{IRQ}$	I_{LOH}	–	1.0	10	μAdc
Power Dissipation		P_D	–	–	550	mW
Input Capacitance		C_{in}				pF
(V_{in} = 0, T_A = 25°C, f = 1.0 MHz)	D0–D7		–	–	12.5	
	All others		–	–	7.5	
Output Capacitance		C_{out}				pF
(V_{in} = 0, T_A = 25°C, f = 1.0 MHz)	$\overline{IRQ}$		–	–	5.0	
	O1, O2, O3		–	–	10	

BUS TIMING CHARACTERISTICS

Characteristic	Symbol	Min	Max	Unit
READ (See Figures 2 and 8)				
Enable Cycle Time	t_{cycE}	1.0	10	μs
Enable Pulse Width, High	PW_{EH}	0.45	4.5	μs
Enable Pulse Width, Low	PW_{EL}	0.43	–	μs
Setup Time, Address and R/$\overline{W}$ valid to enable positive transition	t_{AS}	160	–	ns
Data Delay Time	t_{DDR}	–	320	ns
Data Hold Time	t_H	10	–	ns
Address Hold Time	t_{AH}	10	–	ns
Rise and Fall Time for Enable input	t_{Er}, t_{Ef}	–	25	ns
WRITE (See Figures 3 and 8)				
Enable Cycle Time	t_{cycE}	1.0	10	μs
Enable Pulse Width, High	PW_{EH}	0.45	4.5	μs
Enable Pulse Width, Low	PW_{EL}	0.43	–	μs
Setup Time, Address and R/$\overline{W}$ valid to enable positive transition	t_{AS}	160	–	ns
Data Setup Time	t_{DSW}	195	–	ns
Data Hold Time	t_H	10	–	ns
Address Hold Time	t_{AH}	10	–	ns
Rise and Fall Time for Enable input	t_{Er}, T_{Ef}	–	25	ns

AC OPERATING CHARACTERISTICS

Characteristic		Symbol	Min	Max	Unit
Input Rise and Fall Times	$\overline{C}$, $\overline{G}$ and $\overline{Reset}$	t_r, t_f	–	1.0*	μs
Input Pulse Width Low (Figure 4)	$\overline{C}$, $\overline{G}$ and $\overline{Reset}$	PW_L	$t_{cycE} + t_{su} + t_{hd}$	–	ns
Input Pulse Width High (Figure 5)	$\overline{C}$, $\overline{G}$	PW_H	$t_{cycE} + t_{su} + t_{hd}$	–	ns
Input Setup Time (Figure 6)	$\overline{C}$, $\overline{G}$ and $\overline{Reset}$	t_{su}	200	–	ns
(Synchronous Mode)	$\overline{C3}$ (÷8 Prescaler Mode only)		–	–	
Input Hold Time (Figure 6)	$\overline{C}$, $\overline{G}$ and $\overline{Reset}$	t_{hd}	50	–	ns
(Synchronous Mode)	$\overline{C3}$ (÷8 Prescaler Mode only)		–	–	
Output Delay, O1–O3 (Figure 7)					
(V_{OH} = 2.4 V, Load A)	TTL	t_{co}	–	700	ns
(V_{OH} = 2.4 V, Load C)	MOS	t_{cm}	–	450	ns
(V_{OH} = 0.7 V_{DD}, Load C)	CMOS	t_{cmos}	–	2.0	μs
Interrupt Release Time		t_{IR}	–	1.6	μs

*t_r and $t_f \leq$ 1 x Pulse Width or 1.0 μs, whichever is smaller.

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MC6821
(1.0 MHz)
MC68A21
(1.5 MHz)
MC68B21
(2.0 MHz)

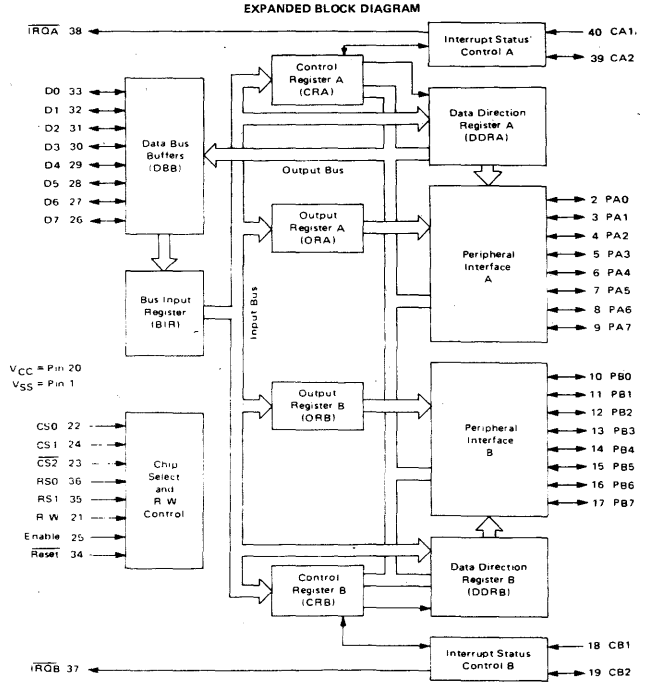
PERIPHERAL INTERFACE ADAPTER (PIA)

The MC6821 Peripheral Interface Adapter provides the universal means of interfacing peripheral equipment to the MC6800 Microprocessing Unit (MPU). This device is capable of interfacing the MPU to peripherals through two 8-bit bidirectional peripheral data buses and four control lines. No external logic is required for interfacing to most peripheral devices.

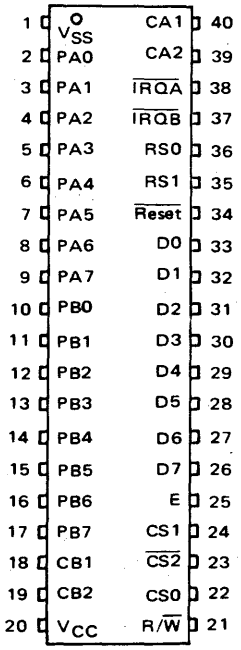
The functional configuration of the PIA is programmed by the MPU during system initialization. Each of the peripheral data lines can be programmed to act as an input or output, and each of the four control/interrupt lines may be programmed for one of several control modes. This allows a high degree of flexibility in the over-all operation of the interface.

- 8-Bit Bidirectional Data Bus for Communication with the MPU
- Two Bidirectional 8-Bit Buses for Interface to Peripherals
- Two Programmable Control Registers
- Two Programmable Data Direction Registers
- Four Individually-Controlled Interrupt Input Lines; Two Usable as Peripheral Control Outputs
- Handshake Control Logic for Input and Output Peripheral Operation
- High-Impedance 3-State and Direct Transistor Drive Peripheral Lines
- Program Controlled Interrupt and Interrupt Disable Capability
- CMOS Drive Capability on Side A Peripheral Lines
- Two TTL Drive Capability on All A and B Side Buffers
- TTL-Compatible
- Static Operation

EXPANDED BLOCK DIAGRAM



PIN ASSIGNMENT



ORDERING INFORMATION

Speed	Device	Temperature Range
1.0 MHz	MC6821P, L	0 to +70°C
	MC6821CP, CL	-40 to +85°C
MIL-STD-883B MIL-STD-883C	MC6821BQCS MC6821CQCS	- 55 to +125°C
1.5 MHz	MC68A21P, L	0 to +70°C
	MC68A21CP, CL	-40 to +85°C
2.0 MHz	MC68B21P, L	0 to +70°C

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ELECTRICAL CHARACTERISTICS (V_{CC} = 5.0 V ±5%, V_{SS} = 0, T_A = T_L to T_H unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
BUS CONTROL INPUTS (R/$\overline{W}$, Enable, $\overline{Reset}$, RS0, RS1, CS0, CS1, $\overline{CS2}$)					
Input High Voltage	V_{IH}	V_{SS} + 2.0	–	V_{CC}	Vdc
Input Low Voltage	V_{IL}	V_{SS} – 0.3	–	V_{SS} + 0.8	Vdc
Input Leakage Current (V_{in} = 0 to 5.25 Vdc)	I_{in}	–	1.0	2.5	μAdc
Capacitance (V_{in} = 0, T_A = 25°C, f = 1.0 MHz)	C_{in}	–	–	7.5	pF
INTERRUPT OUTPUTS ($\overline{IRQA}$, $\overline{IRQB}$)					
Output Low Voltage (I_{Load} = 3.2 mAdc)	V_{OL}	–	–	V_{SS} + 0.4	Vdc
Output Leakage Current (Off State) (V_{OH} = 2.4 Vdc)	I_{LOH}	–	1.0	10	μAdc
Capacitance (V_{in} = 0, T_A = 25°C, f = 1.0 MHz)	C_{out}	–	–	5.0	pF
DATA BUS (D0-D7)					
Input High Voltage	V_{IH}	V_{SS} + 2.0	–	V_{CC}	Vdc
Input Low Voltage	V_{IL}	V_{SS} – 0.3	–	V_{SS} + 0.8	Vdc
Three-State (Off State) Input Current (V_{in} = 0.4 to 2.4 Vdc)	I_{TSI}	–	2.0	10	μAdc
Output High Voltage (I_{Load} = –205 μAdc)	V_{OH}	V_{SS} + 2.4	–	–	Vdc
Output Low Voltage (I_{Load} = 1.6 mAdc)	V_{OL}	–	–	V_{SS} + 0.4	Vdc
Capacitance (V_{in} = 0, T_A = 25°C, f = 1.0 MHz)	C_{in}	–	–	12.5	pF
PERIPHERAL BUS (PA0-PA7, PB0-PB7, CA1, CA2, CB1, CB2)					
Input Leakage Current (V_{in} = 0 to 5.25 Vdc) R/$\overline{W}$, $\overline{Reset}$, RS0, RS1, CS0, CS1, $\overline{CS2}$, CA1, CB1, Enable	I_{in}	–	1.0	2.5	μAdc
Three-State (Off State) Input Current (V_{in} = 0.4 to 2.4 Vdc) PB0-PB7, CB2	I_{TSI}	–	2.0	10	μAdc
Input High Current (V_{IH} = 2.4 Vdc) PA0-PA7, CA2	I_{IH}	–200	–400	–	μAdc
Darlington Drive Current V_O = 1.5 Vdc PB0-PB7,CB2	I_{OH}	–1.0	–	–10	mAdc
Input Low Current (V_{IL} = 0.4 Vdc) PA0-PA7, CA2	I_{IL}	–	–1.3	–2.4	mAdc
Output High Voltage	V_{OH}				Vdc
(I_{Load} = –200 μAdc) PA0-P7, PB0-PB7, CA2, CB2		V_{SS} + 2.4	–	–	
(I_{Load} = –10 μAdc) PA0-PA7, CA2		V_{CC} – 1.0	–	–	
Output Low Voltage (I_{Load} = 3.2 mAdc)	V_{OL}	–	–	V_{SS} + 0.4	Vdc
Capacitance (V_{in} = 0, T_A = 25°C, f = 1.0 MHz)	C_{in}	–	–	10	pF
POWER REQUIREMENTS					
Power Dissipation	P_D	–	–	550	mW

BUS TIMING CHARACTERISTICS (V_{CC} = 5.0 V ±5%, V_{SS} = 0, T_A = T_L to T_H unless otherwise specified.)

Characteristic	Symbol	MC6821		MC68A21		MC68B21		Unit	Ref. Fig. No.
		Min	Max	Min	Max	Min	Max		
Enable Cycle Time	t_{cycE}	1000	–	666	–	500	–	ns	1
Enable Pulse Width, High	PW_{EH}	450	–	280	–	220	–	ns	1
Enable Pulse Width, Low	PW_{EL}	430	–	280	–	210	–	ns	1
Enable Pulse Rise and Fall Times	t_{Er}, t_{Ef}	–	25	–	25	–	25	ns	1
Setup Time, Address and R/W valid to Enable positive transition	t_{AS}	160	–	140	–	70	–	ns	2, 3
Address Hold Time	t_{AH}	10	–	10	–	10	–	ns	2, 3
Data Delay Time, Read	t_{DDR}	–	320	–	220	–	180	ns	2, 4
Data Hold Time, Read	t_{DHR}	10	–	10	–	10	–	ns	2, 4
Data Setup Time, Write	t_{DSW}	195	–	80	–	60	–	ns	3, 4
Data Hold Time, Write	t_{DHW}	10	–	10	–	10	–	ns	3, 4

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MC6803
Internal-Clock

MC6803E
External-Clock

The MC6803 is an 8-bit microcomputer which employs a multiplexed address and data system allowing expandability to 65K words. The MC6803 is object code compatible with the M6800 instruction set and includes improved execution times of key instructions. There are several new 16-bit and 8-bit instructions including an 8 by 8 multiply with 16-bit result. The MC6803 has 128 bytes of RAM, internal clock, UART, parallel I/O, and three function 16-bit timer all on-board. The MC6803E version is also available for use with an external clock. The MC6803 internal clock version requires only the addition of an external crystal for MCU operation. The MC6803 internal clock's divide by four circuitry allows for use of the inexpensive 3.58 MHz color burst crystal. The MC6803 MCU is fully TTL compatible and requires only one +5.0 volt power supply.

- Expanded M6800 Instruction Set
- Full Object Code Compatibility With M6800 MPU/s
- Multiplexed Address and Data
- Compatible With Existing M6800 Peripherals
- 8 x 8 Multiply With 16-bit Result
- Up to 13 Parallel I/O Lines
- 128 Bytes On-Board RAM
- On-Board RAM Retainable With V_{CC} Standby
- UART (Serial I/O) On-Board
- 16-bit Timer On-Board
- Internal Clock/Divide by Four Circuitry (MC6803)
- External Clock/Divide by One Circuitry (MC6803E)
- Full TTL Compatibility
- Full Interrupt Capability

MC6803 MCU PROGRAMMING MODEL

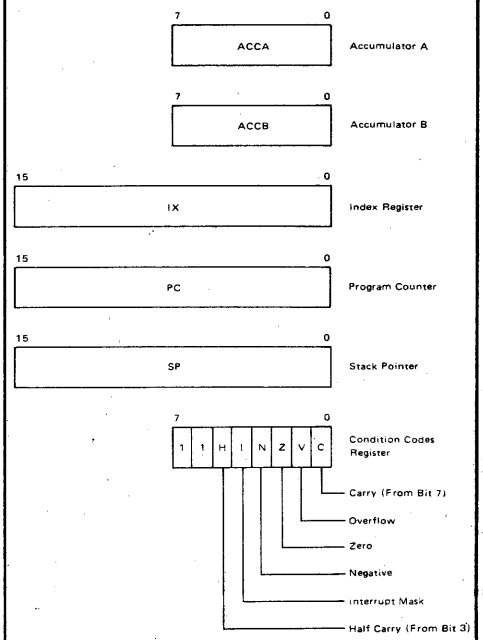
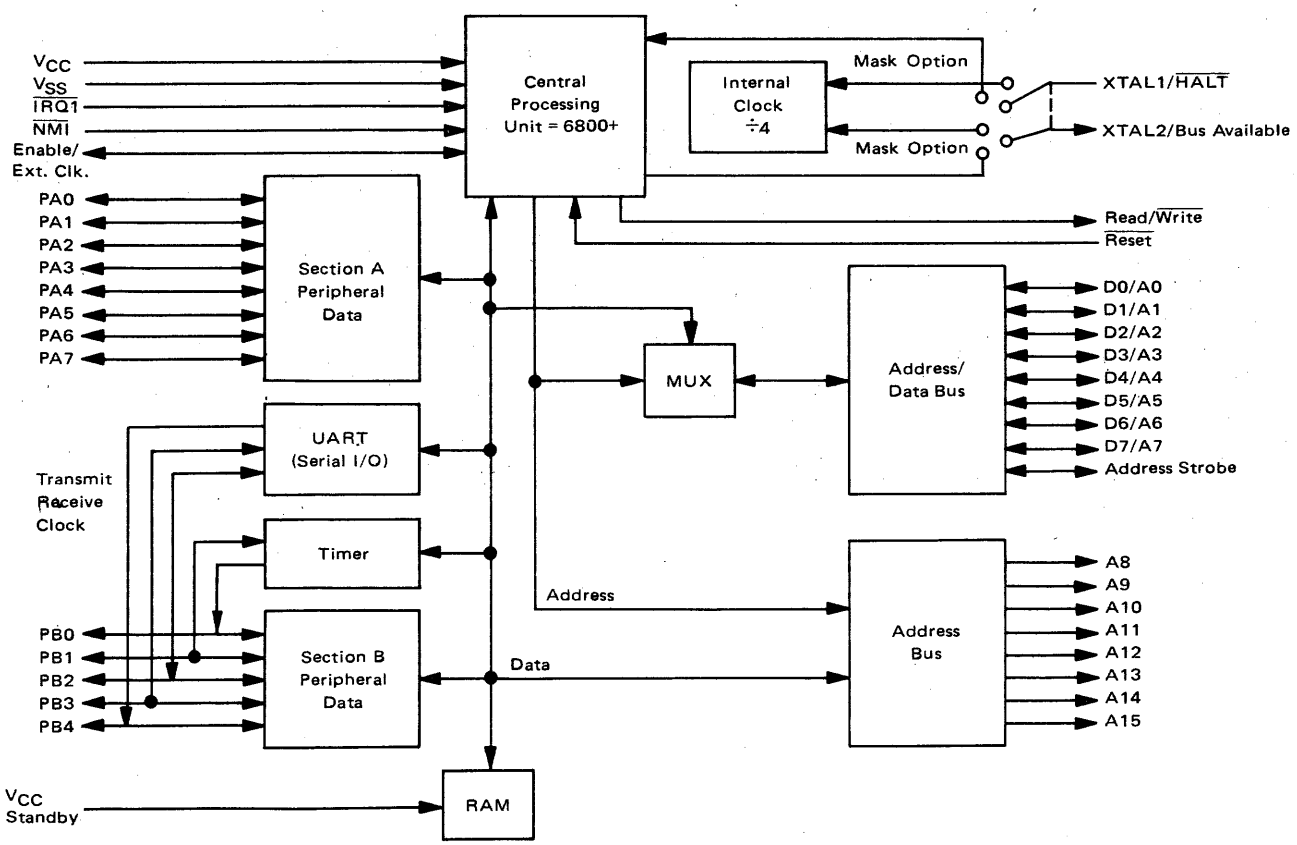


FIGURE 1 – BLOCK DIAGRAM



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TABLE 2 – MC6803 MCU PROGRAMMING MODE

The execution time of key instructions has been reduced.
Table 2 shows instruction execution times in machine cycles.

	ACCX	Immediate	Direct	Extended	Indexed	Inherent	Relative
ABA	•	•	•	•	•	2	•
ABX	•	•	•	•	•	3	•
ADC	•	2	3	4	4	•	•
ADD	•	2	3	4	4	•	•
ADDD	•	4	5	6	6	•	•
AND	•	2	3	4	4	•	•
ASL	2	•	•	6	6	•	•
ASLD	•	•	•	•	•	3	•
ASR	2	•	•	6	6	•	•
BCC	•	•	•	•	•	•	3
BCS	•	•	•	•	•	•	3
BEQ	•	•	•	•	•	•	3
BGE	•	•	•	•	•	•	3
BGT	•	•	•	•	•	•	3
BHI	•	•	•	•	•	•	3
BIT	•	2	3	4	4	•	•
BLE	•	•	•	•	•	•	3
BLS	•	•	•	•	•	•	3
BLT	•	•	•	•	•	•	3
BMI	•	•	•	•	•	•	3
BNE	•	•	•	•	•	•	3
BPL	•	•	•	•	•	•	3
BRA	•	•	•	•	•	•	3
BSR	•	•	•	•	•	•	6
BVC	•	•	•	•	•	•	3
BVS	•	•	•	•	•	•	3
CBA	•	•	•	•	•	2	•
CLC	•	•	•	•	•	2	•
CLI	•	•	•	•	•	2	•
CLR	2	•	•	6	6	•	•
CLV	•	•	•	•	•	2	•
CMP	•	2	3	4	4	•	•
COM	2	•	•	6	6	•	•
CPX	•	4	5	6	6	•	•
DAA	•	•	•	•	•	2	•
DEC	2	•	•	6	6	•	•
DES	•	•	•	•	•	3	•
DEX	•	•	•	•	•	3	•
EOR	•	2	3	4	4	•	•
INC	2	•	•	6	6	•	•
INS	•	•	•	•	•	3	•

	ACCX	Immediate	Direct	Extended	Indexed	Inherent	Relative
INX	•	•	•	•	•	3	•
JMP	•	•	•	3	3	•	•
JSR	•	•	5	6	6	•	•
LDA	•	2	3	4	4	•	•
LDD	•	3	4	5	5	•	•
LDS	•	3	4	5	5	•	•
LDX	•	3	4	5	5	•	•
LSR	2	•	•	6	6	•	•
LSRD	•	•	•	•	•	3	•
MUL	•	•	•	•	•	10	•
NEG	2	•	•	6	6	•	•
NOP	•	•	•	•	•	2	•
ORA	•	2	3	4	4	•	•
PSH	3	•	•	•	•	•	•
PSHX	•	•	•	•	4	•	•
PUL	4	•	•	•	•	•	•
PULX	•	•	•	•	•	5	•
ROL	2	•	6	6	•	•	•
ROR	2	•	6	6	•	•	•
RTI	•	•	•	•	•	10	•
RTS	•	•	•	•	•	5	•
SBA	•	•	•	•	•	2	•
SBC	•	2	3	4	4	•	•
SEC	•	•	•	•	•	2	•
SEI	•	•	•	•	•	2	•
SEV	•	•	•	•	•	2	•
STA	•	•	3	4	4	•	•
STD	•	•	4	5	5	•	•
STS	•	•	4	5	5	•	•
STX	•	•	4	5	5	•	•
SUB	•	2	3	4	4	•	•
SUBD	•	4	5	6	6	•	•
SWI	•	•	•	•	•	12	•
TAB	•	•	•	•	•	2	•
TAP	•	•	•	•	•	2	•
TBA	•	•	•	•	•	2	•
TPA	•	•	•	•	•	2	•
TST	2	•	•	6	6	•	•
TSX	•	•	•	•	•	3	•
TXS	•	•	•	•	•	3	•
WAI	•	•	•	•	•	9	•

An MC6803 and an MC6803E system configuration are shown in figures 3 and 4 respectively. The MC6803 MCU is expandable to a full 65K words allowing for a system containing several peripherals plus memory.

FIGURE 3 – MC6803 SYSTEM CONFIGURATION

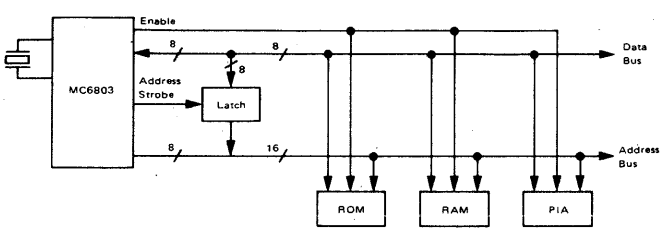
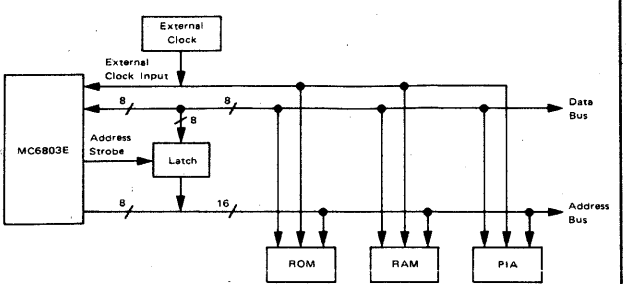


FIGURE 4 – MC6803E SYSTEM CONFIGURATION



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MC6802

MICROPROCESSOR WITH CLOCK AND RAM

The MC6802 is a monolithic 8-bit microprocessor that contains all the registers and accumulators of the present MC6800 plus an internal clock oscillator and driver on the same chip. In addition, the MC6802 has 128 bytes of RAM on board located at hex addresses 0000 to 007F. The first 32 bytes of RAM, at hex addresses 0000 to 001F, may be retained in a low power mode by utilizing V_{CC} standby, thus facilitating memory retention during a power-down situation.

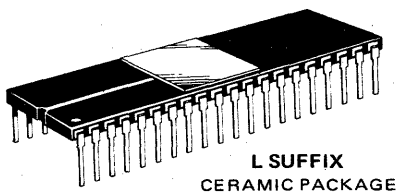
The MC6802 is completely software compatible with the MC6800 as well as the entire M6800 family of parts. Hence, the MC6802 is expandable to 65K words.

- On-Chip Clock Circuit
- 128 x 8 Bit On-Chip RAM
- 32 Bytes of RAM Are Retainable
- Software-Compatible with the MC6800
- Expandable to 65K words
- Standard TTL-Compatible Inputs and Outputs
- 8 Bit Word Size
- 16 Bit Memory Addressing
- Interrupt Capability

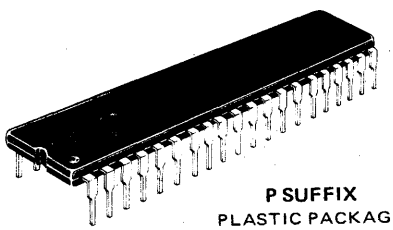
MOS

(N-CHANNEL, SILICON-GATE, DEPLETION LOAD)

MICROPROCESSOR WITH CLOCK AND RAM



L SUFFIX
CERAMIC PACKAGE
CASE 715



P SUFFIX
PLASTIC PACKAGE
CASE 711

FIGURE 1 – TYPICAL MICROCOMPUTER

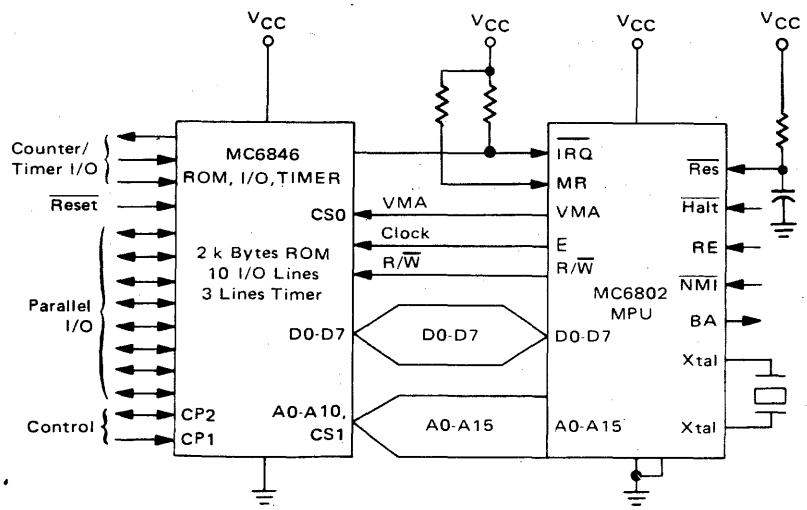
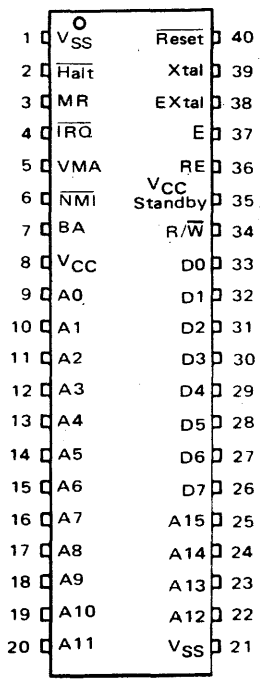


Figure 1 is a block diagram of a typical cost effective microcomputer. The MPU is the center of the microcomputer system and is shown in a minimum system interfacing with a ROM combination chip. It is not intended that this system be limited to this function but that it be expandable with other parts in the M6800 Microcomputer family.

PIN ASSIGNMENT



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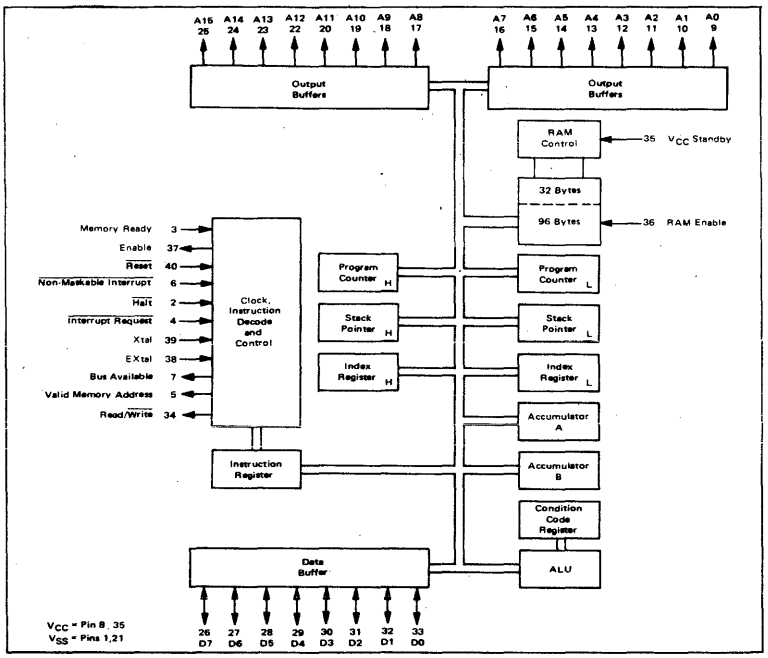


FIGURE 7 – MC6802
EXPANDED BLOCK DIAGRAM

TABLE 4 – INDEX REGISTER AND STACK MANIPULATION INSTRUCTIONS

		IMMED			DIRECT			INDEX			EXTND			IMPLIED				COND. CODE REG.					
																		5	4	3	2	1	0
POINTER OPERATIONS	MNEMONIC	OP	~	#	OP	~	#	OP	~	#	OP	~	#	OP	~	#	BOOLEAN/ARITHMETIC OPERATION	H	I	N	Z	V	C
Compare Index Reg	CPX	8C	3	3	9C	4	2	AC	6	2	BC	5	3				$X_H - M, X_L - (M+1)$	•	•	⑦	↕	⑧	•
Decrement Index Reg	DEX													09	4	1	$X - 1 \rightarrow X$	•	•	•	↕	•	•
Decrement Stack Pntr	DES													34	4	1	$SP - 1 \rightarrow SP$	•	•	•	•	•	•
Increment Index Reg	INX													08	4	1	$X + 1 \rightarrow X$	•	•	•	↕	•	•
Increment Stack Pntr	INS													31	4	1	$SP + 1 \rightarrow SP$	•	•	•	•	•	•
Load Index Reg	LDX	CE	3	3	DE	4	2	EE	6	2	FE	5	3				$M \rightarrow X_H, (M+1) \rightarrow X_L$	•	•	⑨	↕	R	•
Load Stack Pntr	LDS	8E	3	3	9E	4	2	AE	6	2	BE	5	3				$M \rightarrow SP_H, (M+1) \rightarrow SP_L$	•	•	⑨	↕	R	•
Store Index Reg	STX				DF	5	2	EF	7	2	FF	6	3				$X_H \rightarrow M, X_L \rightarrow (M+1)$	•	•	⑨	↕	R	•
Store Stack Pntr	STS				9F	5	2	AF	7	2	BF	6	3				$SP_H \rightarrow M, SP_L \rightarrow (M+1)$	•	•	⑨	↕	R	•
Indx Reg → Stack Pntr	TXS													35	4	1	$X - 1 \rightarrow SP$	•	•	•	•	•	•
Stack Pntr → Indx Reg	TSX													30	4	1	$SP + 1 \rightarrow X$	•	•	•	•	•	•

TABLE 5 – JUMP AND BRANCH INSTRUCTIONS

		RELATIVE			INDEX			EXTND			IMPLIED				COND. CODE REG.						
															5	4	3	2	1	0
OPERATIONS	MNEMONIC	OP	~	#	OP	~	#	OP	~	#	OP	~	#	BRANCH TEST	H	I	N	Z	V	C
Branch Always	BRA	20	4	2										None	•	•	•	•	•	•
Branch If Carry Clear	BCC	24	4	2										C = 0	•	•	•	•	•	•
Branch If Carry Set	BCS	25	4	2										C = 1	•	•	•	•	•	•
Branch If = Zero	BEQ	27	4	2										Z = 1	•	•	•	•	•	•
Branch If ≥ Zero	BGE	2C	4	2										$N \oplus V = 0$	•	•	•	•	•	•
Branch If > Zero	BGT	2E	4	2										$Z + (N \oplus V) = 0$	•	•	•	•	•	•
Branch If Higher	BHI	22	4	2										C + Z = 0	•	•	•	•	•	•
Branch If ≤ Zero	BLE	2F	4	2										$Z + (N \oplus V) = 1$	•	•	•	•	•	•
Branch If Lower Or Same	BLS	23	4	2										C + Z = 1	•	•	•	•	•	•
Branch If < Zero	BLT	2D	4	2										$N \oplus V = 1$	•	•	•	•	•	•
Branch If Minus	BMI	2B	4	2										N = 1	•	•	•	•	•	•
Branch If Not Equal Zero	BNE	26	4	2										Z = 0	•	•	•	•	•	•
Branch If Overflow Clear	BVC	28	4	2										V = 0	•	•	•	•	•	•
Branch If Overflow Set	BVS	29	4	2										V = 1	•	•	•	•	•	•
Branch If Plus	BPL	2A	4	2										N = 0	•	•	•	•	•	•
Branch To Subroutine	BSR	8D	8	2											•	•	•	•	•	•
Jump	JMP				6E	4	2	7E	3	3				See Special Operations	•	•	•	•	•	•
Jump To Subroutine	JSR				AD	8	2	BD	9	3					•	•	•	•	•	•
No Operation	NOP										01	2	1	Advances Prog. Cntr. Only	•	•	•	•	•	•
Return From Interrupt	RTI										3B	10	1		⑩					
Return From Subroutine	RTS										39	5	1		•	•	•	•	•	•
Software Interrupt	SWI										3F	12	1	See Special Operations	•	•	•	•	•	•
Wait for Interrupt*	WAI										3E	9	1		•	⑪	•	•	•	•

*WAI puts Address Bus, R/W, and Data Bus in the three-state mode while VMA is held low.

TABLE 3 – ACCUMULATOR AND MEMORY INSTRUCTIONS

OPERATIONS	MNEMONIC	IMMED OP	IMMED ~	IMMED =	DIRECT OP	DIRECT ~	DIRECT =	INDEX OP	INDEX ~	INDEX =	EXTND OP	EXTND ~	EXTND =	IMPLIED OP	IMPLIED ~	IMPLIED =	BOOLEAN/ARITHMETIC OPERATION (All register labels refer to contents)	5 H	4 I	3 N	2 Z	1 V	0 C
Add	ADDA	8B	2	2	9B	3	2	AB	5	2	BB	4	3				A + M → A	↕	•	↕	↕	↕	↕
	ADDB	CB	2	2	DB	3	2	EB	5	2	FB	4	3				B + M → B	↕	•	↕	↕	↕	↕
Add Acmltrs	ABA													1B	2	1	A + B → A	↕	•	↕	↕	↕	↕
Add with Carry	ADCA	89	2	2	99	3	2	A9	5	2	B9	4	3				A + M + C → A	↕	•	↕	↕	↕	↕
	ADCB	C9	2	2	D9	3	2	E9	5	2	F9	4	3				B + M + C → B	↕	•	↕	↕	↕	↕
And	ANDA	84	2	2	94	3	2	A4	5	2	B4	4	3				A · M → A	•	•	↕	↕	R	•
	ANDB	C4	2	2	D4	3	2	E4	5	2	F4	4	3				B · M → B	•	•	↕	↕	R	•
Bit Test	BITA	85	2	2	95	3	2	A5	5	2	B5	4	3				A · M	•	•	↕	↕	R	•
	BITB	C5	2	2	D5	3	2	E5	5	2	F5	4	3				B · M	•	•	↕	↕	R	•
Clear	CLR							6F	7	2	7F	6	3				00 → M	•	•	R	S	R	R
	CLRA													4F	2	1	00 → A	•	•	R	S	R	R
	CLRB													5F	2	1	00 → B	•	•	R	S	R	R
Compare	CMPA	81	2	2	91	3	2	A1	5	2	B1	4	3				A – M	•	•	↕	↕	↕	↕
	CMPB	C1	2	2	D1	3	2	E1	5	2	F1	4	3				B – M	•	•	↕	↕	↕	↕
Compare Acmltrs	CBA													11	2	1	A – B	•	•	↕	↕	↕	↕
Complement, 1's	COM							63	7	2	73	6	3				$\overline{M}$ → M	•	•	↕	↕	R	S
	COMA													43	2	1	$\overline{A}$ → A	•	•	↕	↕	R	S
	COMB													53	2	1	$\overline{B}$ → B	•	•	↕	↕	R	S
Complement, 2's (Negate)	NEG							60	7	2	70	6	3				00 – M → M	•	•	↕	↕	①	②
	NEGA													40	2	1	00 – A → A	•	•	↕	↕	①	②
	NEGB													50	2	1	00 – B → B	•	•	↕	↕	①	②
Decimal Adjust, A	DAA													19	2	1	Converts Binary Add. of BCD Characters into BCD Format	•	•	↕	↕	↕	③
Decrement	DEC							6A	7	2	7A	6	3				M – 1 → M	•	•	↕	↕	4	•
	DECA													4A	2	1	A – 1 → A	•	•	↕	↕	4	•
	DECB													5A	2	1	B – 1 → B	•	•	↕	↕	4	•
Exclusive OR	EORA	88	2	2	98	3	2	A8	5	2	B8	4	3				A⊕M → A	•	•	↕	↕	R	•
	EORB	C8	2	2	D8	3	2	E8	5	2	F8	4	3				B⊕M → B	•	•	↕	↕	R	•
Increment	INC							6C	7	2	7C	6	3				M + 1 → M	•	•	↕	↕	⑤	•
	INCA													4C	2	1	A + 1 → A	•	•	↕	↕	⑤	•
	INCB													5C	2	1	B + 1 → B	•	•	↕	↕	⑤	•
Load Acmltr	LDAA	86	2	2	96	3	2	A6	5	2	B6	4	3				M → A	•	•	↕	↕	R	•
	LDAB	C6	2	2	D6	3	2	E6	5	2	F6	4	3				M → B	•	•	↕	↕	R	•
Or, Inclusive	ORAA	8A	2	2	9A	3	2	AA	5	2	BA	4	3				A + M → A	•	•	↕	↕	R	•
	ORAB	CA	2	2	DA	3	2	EA	5	2	FA	4	3				B + M → B	•	•	↕	↕	R	•
Push Data	PSHA													36	4	1	A → M_{SP}, SP – 1 → SP	•	•	•	•	•	•
	PSHB													37	4	1	B → M_{SP}, SP – 1 → SP	•	•	•	•	•	•
Pull Data	PULA													32	4	1	SP + 1 → SP, M_{SP} → A	•	•	•	•	•	•
	PULB													33	4	1	SP + 1 → SP, M_{SP} → B	•	•	•	•	•	•
Rotate Left	ROL							69	7	2	79	6	3				M	•	•	↕	↕	⑥	↕
	ROLA													49	2	1	A	•	•	↕	↕	⑥	↕
	ROLB													59	2	1	B	•	•	↕	↕	⑥	↕
Rotate Right	ROR							66	7	2	76	6	3				M	•	•	↕	↕	⑥	↕
	RORA													46	2	1	A	•	•	↕	↕	⑥	↕
	RORB													56	2	1	B	•	•	↕	↕	⑥	↕
Shift Left, Arithmetic	ASL							68	7	2	78	6	3				M	•	•	↕	↕	⑥	↕
	ASLA													48	2	1	A	•	•	↕	↕	⑥	↕
	ASLB													58	2	1	B	•	•	↕	↕	⑥	↕
Shift Right, Arithmetic	ASR							67	7	2	77	6	3				M	•	•	↕	↕	⑥	↕
	ASRA													47	2	1	A	•	•	↕	↕	⑥	↕
	ASRB													57	2	1	B	•	•	↕	↕	⑥	↕
Shift Right, Logic	LSR							64	7	2	74	6	3				M	•	•	R	↕	⑥	↕
	LSRA													44	2	1	A	•	•	R	↕	⑥	↕
	LSRB													54	2	1	B	•	•	R	↕	⑥	↕
Store Acmltr.	STAA				97	4	2	A7	6	2	B7	5	3				A → M	•	•	↕	↕	R	•
	STAB				D7	4	2	E7	6	2	F7	5	3				B → M	•	•	↕	↕	R	•
Subtract	SUBA	80	2	2	90	3	2	A0	5	2	B0	4	3				A – M → A	•	•	↕	↕	↕	↕
	SUBB	C0	2	2	D0	3	2	E0	5	2	F0	4	3				B – M → B	•	•	↕	↕	↕	↕
Subtract Acmltrs.	SBA													10	2	1	A – B → A	•	•	↕	↕	↕	↕
Subtr. with Carry	SBCA	82	2	2	92	3	2	A2	5	2	B2	4	3				A – M – C → A	•	•	↕	↕	↕	↕
	SBCB	C2	2	2	D2	3	2	E2	5	2	F2	4	3				B – M – C → B	•	•	↕	↕	↕	↕
Transfer Acmltrs	TAB													16	2	1	A → B	•	•	↕	↕	R	•
	TBA													17	2	1	B → A	•	•	↕	↕	R	•
Test, Zero or Minus	TST							6D	7	2	7D	6	3				M – 00	•	•	↕	↕	R	R
	TSTA													4D	2	1	A – 00	•	•	↕	↕	R	R
	TSTB													5D	2	1	B – 00	•	•	↕	↕	R	R
																		H	I	N	Z	V	C

ADDRESSING MODES — BOOLEAN/ARITHMETIC OPERATION — COND. CODE REG.

LEGEND:

OP Operation Code (Hexadecimal);
~ Number of MPU Cycles;
= Number of Program Bytes;
+ Arithmetic Plus;
– Arithmetic Minus;
· Boolean AND;
M_{SP} Contents of memory location pointed to be Stack Pointer;
+ Boolean Inclusive OR;
⊕ Boolean Exclusive OR;
$\overline{M}$ Complement of M;
→ Transfer Into;
0 Bit = Zero;
00 Byte = Zero;

Note – Accumulator addressing mode instructions are included in the column for IMPLIED addressing

CONDITION CODE SYMBOLS:

H Half-carry from bit 3;
I Interrupt mask
N Negative (sign bit)
Z Zero (byte)
V Overflow, 2's complement
C Carry from bit 7
R Reset Always
S Set Always
↕ Test and set if true, cleared otherwise
• Not Affected

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MOTOROLA Semiconductors
3501 ED BLUESTEIN BLVD., AUSTIN, TEXAS 78721

MC3870

0° to 70°C

SINGLE-CHIP MICROCONTROLLER

The MC3870 is a complete 8-bit microcomputer on a single MOS integrated circuit. Utilizing ion-implanted, N-channel silicon-gate technology and advanced circuit design techniques, the single-chip 3870 offers maximum cost effectiveness in a wide range of control and logic replacement applications.

- Software Compatible with F8 Family
- 2048 Byte Mask Programmable ROM
- 64 Byte Scratchpad RAM
- 32 Bits (4 Ports) TTL Compatible I/O
- Programmable Binary Timer
  - Interval Timer Mode
  - Pulse Width Measurement Mode
  - Event Counter Mode
- External Interrupt
- Crystal, LC, RC, External, or Internal Time Base
- Low Power (275 mW Typ.)
- Single +5 Volt ±10% Power Supply

PIN CONNECTIONS

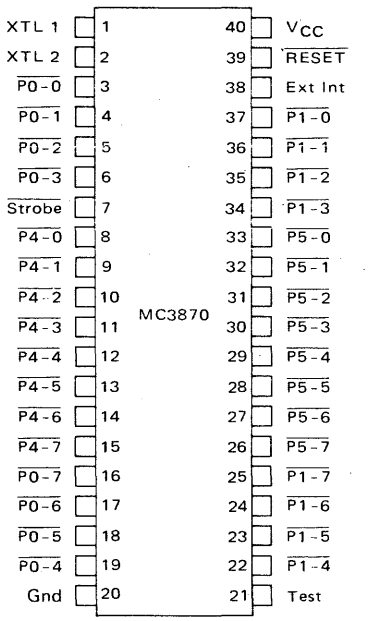
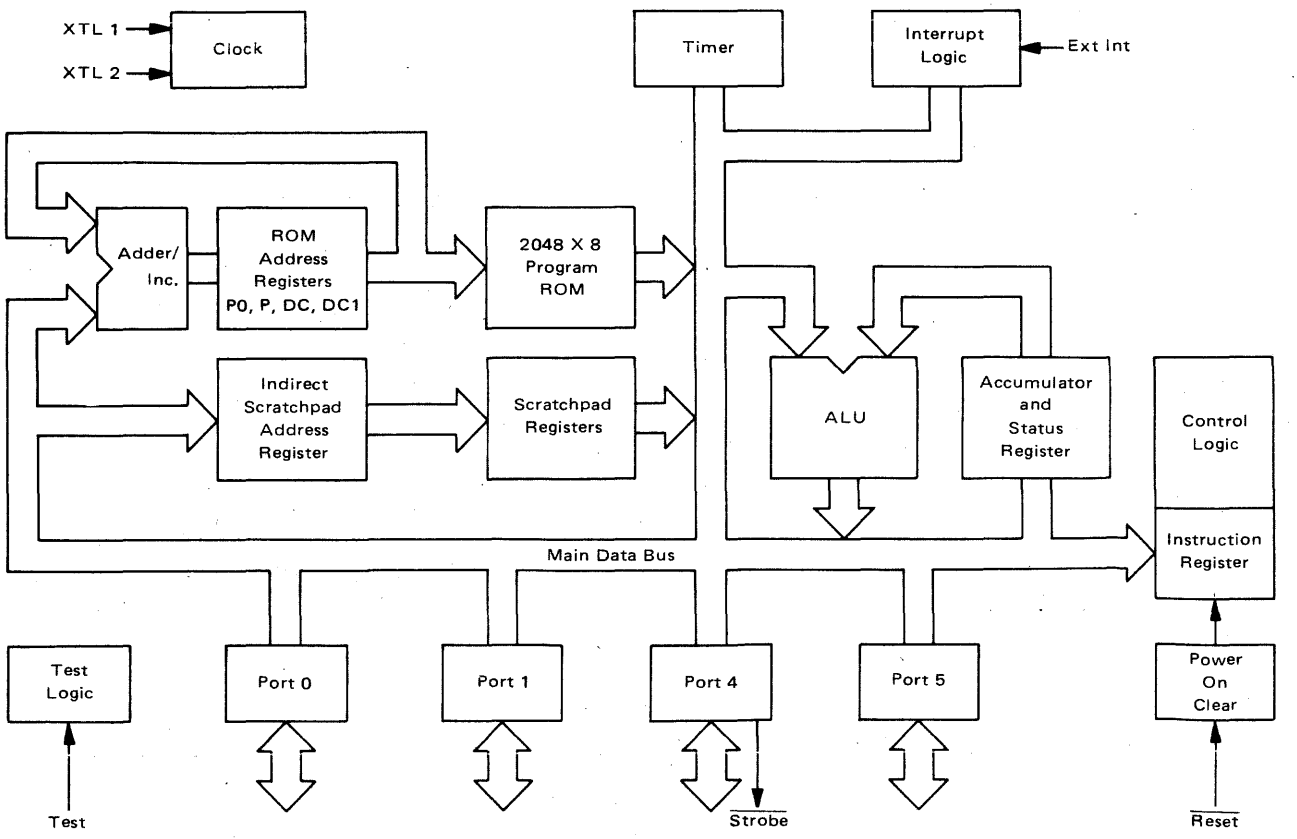


FIGURE 1 - Block Diagram



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ADI-445

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MC3870 INSTRUCTION SET
(F8 COMPATIBLE)

ACCUMULATOR GROUP INSTRUCTIONS

Operation	Mnemonic Op Code	Operand	Function	Machine Code	Bytes	Cycles	Status Bits OVF	ZERO	CRY	SIGN
ADD CARRY	LNK		ACC←(ACC) + CRY	19	1	1	1/0	1/0	1/0	1/0
ADD IMMEDIATE	AI	ii	ACC←(ACC) + H'ii'	24ii	2	2.5	1/0	1/0	1/0	1/0
AND IMMEDIATE	NI	ii	ACC←(ACC) ∧ H'ii'	21ii	2	2.5	0	1/0	0	1/0
CLEAR	CLR		ACC←H'00'	70	1	1	–	–	–	–
COMPARE IMMEDIATE	CI	ii	H'ii' + $(\overline{ACC})$ + 1	25ii	2	2.5	1/0	1/0	1/0	1/0
COMPLEMENT	COM		ACC←(ACC) ⊕ H'FF'	18	1	1	0	1/0	0	1/0
EXCLUSIVE OR IMMEDIATE	XI	ii	ACC←(ACC) ⊕ H'ii'	23ii	2	2.5	0	1/0	0	1/0
INCREMENT	INC		ACC←(ACC) + 1	1F	1	1	1/0	1/0	1/0	1/0
LOAD IMMEDIATE	LI	ii	ACC←H'ii'	20ii	2	2.5	–	–	–	–
LOAD IMMEDIATE SHORT	LIS	i	ACC←H'0i'	7i	1	1	–	–	–	–
OR IMMEDIATE	OI	ii	ACC←(ACC) ∨ H'ii'	22ii	2	2.5	0	1/0	0	1/0
SHIFT LEFT ONE	SL	1	SHIFT LEFT 1	13	1	1	0	1/0	0	1/0
SHIFT LEFT FOUR	SL	4	SHIFT LEFT 4	15	1	1	0	1/0	0	1/0
SHIFT RIGHT ONE	SR	1	SHIFT RIGHT 1	12	1	1	0	1/0	0	1
SHIFT RIGHT FOUR	SR	4	SHIFT RIGHT 4	14	1	1	0	1/0	0	1

BRANCH INSTRUCTIONS

In all conditional branches $PC_0 \leftarrow (PC_0) + 2$ if the test condition is not met. Execution is complete in 3.0 cycles.

Operation	Mnemonic Op Code	Operand	Function	Machine Code	Bytes	Cycles	Status Bits OVF	ZERO	CRY	SIGN
BRANCH ON CARRY	BC	aa	$PC_0 \leftarrow [(PC_0) + 1] + H'aa'$ if CRY = 1	82aa	2	3.5	–	–	–	–
BRANCH ON POSITIVE	BP	aa	$PC_0 \leftarrow [(PC_0) + 1] + H'aa'$ if SIGN = 1	81aa	2	3.5	–	–	–	–
BRANCH ON ZERO	BZ	aa	$PC_0 \leftarrow [(PC_0) + 1] + H'aa'$ if ZERO = 1	84aa	2	3.5	–	–	–	–
BRANCH ON TRUE	BT	taa	$PC_0 \leftarrow [(PC_0) + 1] + H'aa'$ if any test is true	8taa	2	3.5	–	–	–	–

t = TEST CONDITION

2^2	2^1	2^0
ZERO	CRY	SIGN

BRANCH IF NEGATIVE	BM	aa	$PC_0 \leftarrow [(PC_0) + 1] + H'aa'$ if SIGN = 0	91aa	2	3.5	–	–	–	–
BRANCH IF NO CARRY	BNC	aa	$PC_0 \leftarrow [(PC_0) + 1] + H'aa'$ if CARRY = 0	92aa	2	3.5	–	–	–	–
BRANCH IF NO OVERFLOW	BNO	aa	$PC_0 \leftarrow [(PC_0) + 1] + H'aa'$ if OVF = 0	98aa	2	3.5	–	–	–	–
BRANCH IF NOT ZERO	BNZ	aa	$PC_0 \leftarrow [(PC_0) + 1] + H'aa'$ if ZERO = 0	94aa	2	3.5	–	–	–	–
BRANCH IF FALSE TEST	BF	taa	$PC_0 \leftarrow [(PC_0) + 1] + H'aa'$ if all false test bits	9taa	2	3.5	–	–	–	–

t = TEST CONDITION

2^3	2^2	2^1	2^0
OVF	ZERO	CRY	SIGN

BRANCH IF ISAR (LOWER) ≠ 7	BR7	aa	$PC_0 \leftarrow [(PC_0) + 1] + H'aa'$ if ISARL ≠ 7	8Faa	2	2.5	–	–	–	–
			$PC_0 \leftarrow (PC_0) + 2$ if ISARL = 7			2.0	–	–	–	–
BRANCH RELATIVE	BR	aa	$PC_0 \leftarrow [(PC_0 + 1] + H'aa'$	90aa	2	3.5	–	–	–	–
JUMP*	JMP	aaaa	$PC_0 \leftarrow H'aaaa'$	29aaaa	3	5.5	–	–	–	–

*Privileged instruction

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MEMORY REFERENCE INSTRUCTIONS In all Memory Reference Instructions, the Data Counter is incremented DC←DC + 1

Operation	Mnemonic OP Code	Operand	Function	Machine Code	Bytes	Cycles	Status Bits OVF	ZERO	CRY	SIGN
ADD BINARY	AM		ACC←(ACC) + [(DC)]	88	1	2.5	1/0	1/0	1/0	1/0
ADD DECIMAL	AMD		ACC←(ACC) + [(DC)]	89	1	2.5	1/0	1/0	1/0	1/0
AND	NM		ACC←(ACC)∧[(DC)]	8A	1	2.5	0	1/0	0	1/0
COMPARE	CM		[(DC)] + ($\overline{ACC}$) + 1	8D	1	2.5	1/0	1/0	1/0	1/0
EXCLUSIVE OR	XM		ACC←(ACC) ⊕ [(DC)]	8C	1	2.5	0	1/0	0	1/0
LOAD	LM		ACC←[(DC)]	16	1	2.5	–	–	–	–
LOGICAL OR	OM		ACC←(ACC)∨[(DC)]	8B	1	2.5	0	1/0	0	1/0
STORE	ST		(DC)←(ACC)	17	1	2.5	–	–	–	–

ADDRESS REGISTER GROUP INSTRUCTIONS

Operation	Mnemonic OP Code	Operand	Function	Machine Code	Bytes	Cycles	Status Bits OVF	ZERO	CRY	SIGN
ADD to DATA COUNTER	ADC		DC←(DC) + (ACC)	8E	1	2.5	–	–	–	–
CALL to SUBROUTINE*	PK		PC_0U←(r12); PC_0L←(r13); PC_1←(PC_0)	OC	1	4	–	–	–	–
CALL to SUBROUTINE IMMEDIATE*	PI	aaaa	PC_1←(PC_0); PC_0←H'aaaa'	28aaaa	3	6.5	–	–	–	–
EXCHANGE DC	XDC		DC_0⇆DC_1	2C	1	2	–	–	–	–
LOAD DATA COUNTER	LR	DC,Q	DCU←(r14); DCL←(r15)	0F	1	4	–	–	–	–
LOAD DATA COUNTER	LR	DC,H	DCU←(r10); DCL←(r11)	10	1	4	–	–	–	–
LOAD DC IMMEDIATE	DCI	aaaa	DC←H'aaaa'	2Aaaaa	3	6	–	–	–	–
LOAD PROGRAM COUNTER	LR	PO,Q	PC_0U←(r14); PC_0L←(r15)	OD	1	4	–	–	–	–
LOAD STACK REGISTER	LR	P,K	PC_1U←(r12); PC_1L←(r13)	09	1	4	–	–	–	–
RETURN FROM SUBROUTINE*	POP		PC_0←(PC_1)	1C	1	2	–	–	–	–
STORE DATA COUNTER	LR	Q,DC	r14←(DCU); r15←(DCL)	OE	1	4	–	–	–	–
STORE DATA COUNTER	LR	H,DC	r10←(DCU); r11←(DCL)	11	1	4	–	–	–	–
STORE STACK REGISTER	LR	K,P	r12←(PC_1U); r13←(PC_1L)	08	1	4	–	–	–	–

SCRATCHPAD REGISTER INSTRUCTIONS (Refer to Scratchpad Addressing Modes)

Operation	Mnemonic OP Code	Operand	Function	Machine Code	Bytes	Cycles	Status Bits OVF	ZERO	CRY	SIGN
ADD BINARY	AS	r	ACC←(ACC) + (r)	Cr	1	1	1/0	1/0	1/0	1/0
ADD DECIMAL	ASD	r	ACC←(ACC) + (r)	Dr	1	2	1/0	1/0	1/0	1/0
DECREMENT	DS	r	r←(r) + H'FF'	3r	1	1.5	1/0	1/0	1/0	1/0
LOAD	LR	A,r	ACC←(r)	4r	1	1	–	–	–	–
LOAD	LR	A,KU	ACC←(r12)	00	1	1	–	–	–	–
LOAD	LR	A,KL	ACC←(r13)	01	1	1	–	–	–	–
LOAD	LR	A,QU	ACC←(r14)	02	1	1	–	–	–	–
LOAD	LR	A,QL	ACC←(r15)	03	1	1	–	–	–	–
LOAD	LR	r,A	r←(ACC)	5r	1	1	–	–	–	–
LOAD	LR	KU,A	r12←(ACC)	04	1	1	–	–	–	–
LOAD	LR	KL,A	r13←(ACC)	05	1	1	–	–	–	–
LOAD	LR	QU,A	r14←(ACC)	06	1	1	–	–	–	–
LOAD	LR	QL,A	r15←(ACC)	07	1	1	–	–	–	–
AND	NS	r	ACC←(ACC)∧(r)	Fr	1	1	0	1/0	0	1/0
EXCLUSIVE OR	XS	r	ACC←(ACC) ⊕ (r)	Er	1	1	0	1/0	0	1/0

*Privileged Instruction.

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MISCELLANEOUS INSTRUCTIONS

Operation	Mnemonic OP Code	Operand	Function	Machine Code	Bytes	Cycles	Status Bits OVF	ZERO	CRY	SIGN
DISABLE INTERRUPT	DI		RESET ICB	1A	1	2	–	–	–	–
ENABLE INTERRUPT*	EI		SET ICB	1B	1	2	–	–	–	–
INPUT	IN	aa	ACC←(INPUT PORT aa)	26aa	2	4	0	1/0	0	1/0
INPUT SHORT	INS	a	ACC←(INPUT PORT a)	Aa	1	4***	0	1/0	0	1/0
LOAD ISAR	LR	IS,A	ISAR←(ACC)	0B	1	1	–	–	–	–
LOAD ISAR LOWER	LISL	a	ISARL←a	1101a**	1	1	–	–	–	–
LOAD ISAR UPPER	LISU	a	ISARU←a	01100a**	1	1	–	–	–	–
LOAD STATUS REGISTER*	LR	W,J	W←(r9)	1D	1	2	1/0	1/0	1/0	1/0
NO-OPERATION	NOP		PC_0←(PC_0) + 1	2B	1	1	–	–	–	–
OUTPUT	OUT	aa	OUTPUT PORT aa←(ACC)	27aa	2	4	–	–	–	–
OUTPUT SHORT	OUTS	a	OUTPUT PORT a←(ACC)	Ba	1	4***	–	–	–	–
STORE ISAR	LR	A,IS	ACC←(ISAR)	0A	1	1	–	–	–	–
STORE STATUS REG	LR	J,W	r9←(W)	1E	1	1	–	–	–	–

*Privileged Instruction
**3-Bit Octal Digit
***2 Machine Cycles for CPU Ports

NOTES

Each lowercase character represents a Hexadecimal digit.
Each cycle equals 4 machine clock periods.
Lowercase denotes variables specified by programmer.

Function Definitions

←	is replaced by
( )	the contents of
(–)	Binary "1"s complement of
+	Arithmetic Add (Binary or Decimal)
⊕	Logical OR exclusive
∧	Logical AND
∨	Logical OR inclusive
H'	Hexadecimal digit

Register Names

a	Address Variable
A	Accumulator
DC	Data Counter (Indirect Address Register)
DC_0	Data Counter #0 (Indirect Address Register #0)
DC_1	Data Counter #1 (Indirect Address Register #1)
DCL	Least significant 8 bits of Data Counter Addressed
DCU	Most significant 8 bits of Data Counter Addressed
H	Scratchpad Register #10 and #11
i and ii	Immediate Operand
ICB	Interrupt Control Bit
IS	Indirect Scratchpad Address Register
ISAR	Indirect Scratchpad Address Register
ISARL	Least significant 3 bits of ISAR
ISARU	Most significant 3 bits of ISAR
J	Scratchpad Register #9
K	Registers #12 and #13
KL	Register #13
KU	Register #12
PC_0	Program Counter
PC_0L	Least signfiicant 8 bits of Program Counter
PC_0U	Most significant 8 bits of Program Counter
PC_1	Stack Register
PC_1L	Least significant 8 bits of Program Counter
PC_1U	Most signficant 8 bits of Active Stack Register
Q	Registers #14 and #15
QL	Register #15
QU	Register #14
r	Scratchpad Register (any address through 11)
W	Status Register

Scratchpad Addressing Modes (Machine Code Format)

r C	(Hexadecimal), Register Addressed by ISAR (Unmodified)
r D	(Hexadecimal), Register Addressed by ISAR, ISARL Incremented
r E	(Hexadecimal), Register Addressed by ISAR, ISARL Decremented
r F	(No operation performed)
r O through B	(Hexadecimal), Register 0 through 11 addressed directly from the Instruction

Status Register

–	No change in condition
1/0	is set to "1" or "0" depending on conditions
CRY	Carry Flag
OVF	Overflow Flag
SIGN	Sign of Result Flag
ZERO	Zero Flag

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MC6800
(1.0 MHz)
MC68A00
(1.5 MHz)
MC68B00
(2.0 MHz)

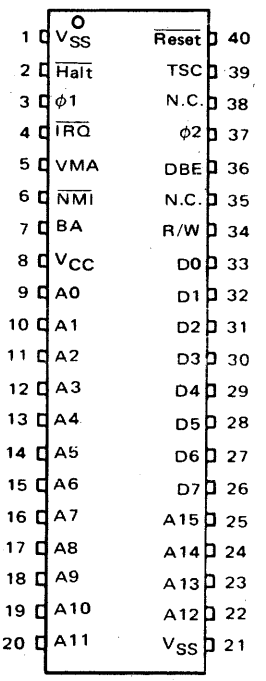
8-BIT MICROPROCESSING UNIT (MPU)

The MC6800 is a monolithic 8-bit microprocessor forming the central control function for Motorola's M6800 family. Compatible with TTL, the MC6800, as with all M6800 system parts, requires only one +5.0-volt power supply, and no external TTL devices for bus interface.

The MC6800 is capable of addressing 65K bytes of memory with its 16-bit address lines. The 8-bit data bus is bidirectional as well as 3-state, making direct memory addressing and multiprocessing applications realizable.

- Eight-Bit Parallel Processing
- Bidirectional Data Bus
- Sixteen-Bit Address Bus – 65K Bytes of Addressing
- 72 Instructions – Variable Length
- Seven Addressing Modes – Direct, Relative, Immediate, Indexed, Extended, Implied and Accumulator
- Variable Length Stack
- Vectored Restart
- Maskable Interrupt Vector
- Separate Non-Maskable Interrupt – Internal Registers Saved in Stack
- Six Internal Registers – Two Accumulators, Index Register, Program Counter, Stack Pointer and Condition Code Register
- Direct Memory Addressing (DMA) and Multiple Processor Capability
- Simplified Clocking Characteristics
- Clock Rates as High as 2.0 MHz
- Simple Bus Interface Without TTL
- Halt and Single Instruction Execution Capability

PIN ASSIGNMENT



ORDERING INFORMATION

Speed	Device	Temperature Range
1.0 MHz	MC6800P, L	0 to 70°C
	MC6800CP, CL	-40 to +85°C
MIL-STD-883B MIL-STD-883C	MC6800BQCS MC6800CQCS	-55 to +125°C
1.5 MHz	MC68A00P, L	0 to +70°C
	MC68A00CP, CL	-40 to +85°C
2.0 MHz	MC68B00P, L	0 to +70°C

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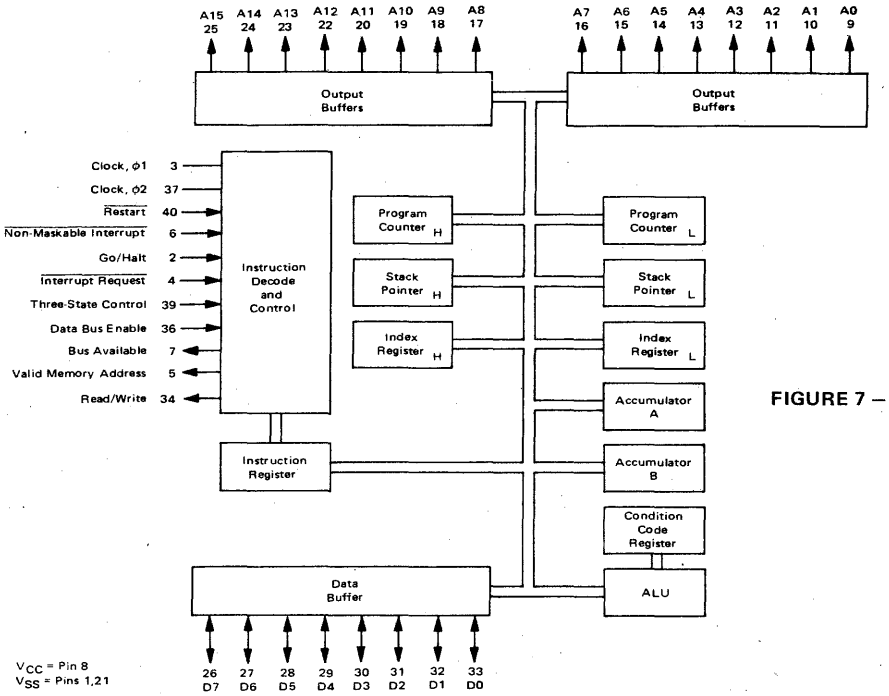


FIGURE 7 – EXPANDED BLOCK DIAGRAM

TABLE 6 – HEXADECIMAL VALUES OF MACHINE CODES

00	*		40	NEG	A		80	SUB	A	IMM	C0	SUB	B	IMM
01	NOP		41	*			81	CMP	A	IMM	C1	CMP	B	IMM
02	*		42	*			82	SBC	A	IMM	C2	SBC	B	IMM
03	*		43	COM	A		83	*			C3	*		
04	*		44	LSR	A		84	AND	A	IMM	C4	AND	B	IMM
05	*		45	*			85	BIT	A	IMM	C5	BIT	B	IMM
06	TAP		46	ROR	A		86	LDA	A	IMM	C6	LDA	B	IMM
07	TPA		47	ASR	A		87	*			C7	*		
08	INX		48	ASL	A		88	EOR	A	IMM	C8	EOR	B	IMM
09	DEX		49	ROL	A		89	ADC	A	IMM	C9	ADC	B	IMM
0A	CLV		4A	DEC	A		8A	ORA	A	IMM	CA	ORA	B	IMM
0B	SEV		4B	*			8B	ADD	A	IMM	CB	ADD	B	IMM
0C	CLC		4C	INC	A		8C	CPX	A	IMM	CC	*		
0D	SEC		4D	TST	A		8D	BSR		REL	CD	*		
0E	CLI		4E	*			8E	LDS		IMM	CE	LDX		IMM
0F	SEI		4F	CLR	A		8F	*			CF	*		
10	SBA		50	NEG	B		90	SUB	A	DIR	D0	SUB	B	DIR
11	CBA		51	*			91	CMP	A	DIR	D1	CMP	B	DIR
12	*		52	*			92	SBC	A	DIR	D2	SBC	B	DIR
13	*		53	COM	B		93	*			D3	*		
14	*		54	LSR	B		94	AND	A	DIR	D4	AND	B	DIR
15	*		55	*			95	BIT	A	DIR	D5	BIT	B	DIR
16	TAB		56	ROR	B		96	LDA	A	DIR	D6	LDA	B	DIR
17	TBA		57	ASR	B		97	STA	A	DIR	D7	STA	B	DIR
18	*		58	ASL	B		98	EOR	A	DIR	D8	EOR	B	DIR
19	DAA		59	ROL	B		99	ADC	A	DIR	D9	ADC	B	DIR
1A	*		5A	DEC	B		9A	ORA	A	DIR	DA	ORA	B	DIR
1B	ABA		5B	*			9B	ADD	A	DIR	DB	ADD	B	DIR
1C	*		5C	INC	B		9C	CPX		DIR	DC	*		
1D	*		5D	TST	B		9D	*			DD	*		
1E	*		5E	*			9E	LDS		DIR	DE	LDX		DIR
1F	*		5F	CLR	B		9F	STS		DIR	DF	STX		DIR
20	BRA	REL	60	NEG		IND	A0	SUB	A	IND	E0	SUB	B	IND
21	*		61	*			A1	CMP	A	IND	E1	CMP	B	IND
22	BHI	REL	62	*			A2	SBC	A	IND	E2	SBC	B	IND
23	BLS	REL	63	COM		IND	A3	*			E3	*		
24	BCC	REL	64	LSR		IND	A4	AND	A	IND	E4	AND	B	IND
25	BCS	REL	65	*			A5	BIT	A	IND	E5	BIT	B	IND
26	BNE	REL	66	ROR		IND	A6	LDA	A	IND	E6	LDA	B	IND
27	BEQ	REL	67	ASR		IND	A7	STA	A	IND	E7	STA	B	IND
28	BVC	REL	68	ASL		IND	A8	EOR	A	IND	E8	EOR	B	IND
29	BVS	REL	69	ROL		IND	A9	ADC	A	IND	E9	ADC	B	IND
2A	BPL	REL	6A	DEC		IND	AA	ORA	A	IND	EA	ORA	B	IND
2B	BMI	REL	6B	*			AB	ADD	A	IND	EB	ADD	B	IND
2C	BGE	REL	6C	INC		IND	AC	CPX		IND	EC	*		
2D	BLT	REL	6D	TST		IND	AD	JSR		IND	ED	*		
2E	BGT	REL	6E	JMP		IND	AE	LDS		IND	EE	LDX		IND
2F	BLE	REL	6F	CLR		IND	AF	STS		IND	EF	STX		IND
30	TSX		70	NEG		EXT	B0	SUB	A	EXT	F0	SUB	B	EXT
31	INS		71	*			B1	CMP	A	EXT	F1	CMP	B	EXT
32	PUL	A	72	*			B2	SBC	A	EXT	F2	SBC	B	EXT
33	PUL	B	73	COM		EXT	B3	*			F3	*		
34	DES		74	LSR		EXT	B4	AND	A	EXT	F4	AND	B	EXT
35	TXS		75	*			B5	BIT	A	EXT	F5	BIT	B	EXT
36	PSH	A	76	ROR		EXT	B6	LDA	A	EXT	F6	LDA	B	EXT
37	PSH	B	77	ASR		EXT	B7	STA	A	EXT	F7	STA	B	EXT
38	*		78	ASL		EXT	B8	EOR	A	EXT	F8	ADC	B	EXT
39	RTS		79	ROL		EXT	B9	ADC	A	EXT	F9	ADC	B	EXT
3A	*		7A	DEC		EXT	BA	ORA	A	EXT	FA	ORA	B	EXT
3B	RTI		7B	*			BB	ADD	A	EXT	FB	ADD	B	EXT
3C	*		7C	INC		EXT	BC	CPX		EXT	FC	*		
3D	*		7D	TST		EXT	BD	JSR		EXT	FD	*		
3E	WAI		7E	JMP		EXT	BE	LDS		EXT	FE	LDX		EXT
3F	SWI		7F	CLR		EXT	BF	STS		EXT	FF	STX		EXT

Notes: 1. Addressing Modes:

A	= Accumulator A
B	= Accumulator B
REL	= Relative
IND	= Indexed
IMM	= Immediate
DIR	= Direct

2. Unassigned code indicated by "*"

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TABLE 7 – ACCUMULATOR AND MEMORY OPERATIONS

The accumulator and memory operations and their effect on the CCR are shown in Table 7.
Included are Arithmetic Logic, Data Test and Data Handling instructions.

		ADDRESSING MODES															BOOLEAN/ARITHMETIC OPERATION	COND. CODE REG.					
		IMMED			DIRECT			INDEX			EXTND			IMPLIED			(All register labels	5	4	3	2	1	0
OPERATIONS	MNEMONIC	OP	~	#	OP	~	#	OP	~	#	OP	~	#	OP	~	#	refer to contents)	H	I	N	Z	V	C
Add	ADDA	8B	2	2	9B	3	2	AB	5	2	BB	4	3				A + M → A	↕	•	↕	↕	↕	↕
	ADDB	CB	2	2	DB	3	2	EB	5	2	FB	4	3				B + M → B	↕	•	↕	↕	↕	↕
Add Acmltrs	ABA													1B	2	1	A + B → A	↕	•	↕	↕	↕	↕
Add with Carry	ADCA	89	2	2	99	3	2	A9	5	2	B9	4	3				A + M + C → A	↕	•	↕	↕	↕	↕
	ADCB	C9	2	2	D9	3	2	E9	5	2	F9	4	3				B + M + C → B	↕	•	↕	↕	↕	↕
And	ANDA	84	2	2	94	3	2	A4	5	2	B4	4	3				A · M → A	•	•	↕	↕	R	•
	ANDB	C4	2	2	D4	3	2	E4	5	2	F4	4	3				B · M → B	•	•	↕	↕	R	•
Bit Test	BITA	85	2	2	95	3	2	A5	5	2	B5	4	3				A · M	•	•	↕	↕	R	•
	BITB	C5	2	2	D5	3	2	E5	5	2	F5	4	3				B · M	•	•	↕	↕	R	•
Clear	CLR							6F	7	2	7F	6	3				00 → M	•	•	R	S	R	R
	CLRA													4F	2	1	00 → A	•	•	R	S	R	R
	CLRB													5F	2	1	00 → B	•	•	R	S	R	R
Compare	CMPA	81	2	2	91	3	2	A1	5	2	B1	4	3				A – M	•	•	↕	↕	↕	↕
	CMPB	C1	2	2	D1	3	2	E1	5	2	F1	4	3				B – M	•	•	↕	↕	↕	↕
Compare Acmltrs	CBA													11	2	1	A – B	•	•	↕	↕	↕	↕
Complement, 1's	COM							63	7	2	73	6	3				M → M	•	•	↕	↕	R	S
	COMA													43	2	1	A → A	•	•	↕	↕	R	S
	COMB													53	2	1	B → B	•	•	↕	↕	R	S
Complement, 2's (Negate)	NEG							60	7	2	70	6	3				00 – M → M	•	•	↕	↕	①	②
	NEGA													40	2	1	00 – A → A	•	•	↕	↕	①	②
	NEGB													50	2	1	00 – B → B	•	•	↕	↕	①	②
Decimal Adjust, A	DAA													19	2	1	Converts Binary Add. of BCD Characters into BCD Format	•	•	↕	↕	↕	③
Decrement	DEC							6A	7	2	7A	6	3				M – 1 → M	•	•	↕	↕	4	•
	DECA													4A	2	1	A – 1 → A	•	•	↕	↕	4	•
	DECB													5A	2	1	B – 1 → B	•	•	↕	↕	4	•
Exclusive OR	EORA	88	2	2	98	3	2	A8	5	2	B8	4	3				A⊕M → A	•	•	↕	↕	R	•
	EORB	C8	2	2	D8	3	2	E8	5	2	F8	4	3				B⊕M → B	•	•	↕	↕	R	•
Increment	INC							6C	7	2	7C	6	3				M + 1 → M	•	•	↕	↕	⑤	•
	INCA													4C	2	1	A + 1 → A	•	•	↕	↕	⑤	•
	INCB													5C	2	1	B + 1 → B	•	•	↕	↕	⑤	•
Load Acmltr	LDAA	86	2	2	96	3	2	A6	5	2	B6	4	3				M → A	•	•	↕	↕	R	•
	LDAB	C6	2	2	D6	3	2	E6	5	2	F6	4	3				M → B	•	•	↕	↕	R	•
Or, Inclusive	ORAA	8A	2	2	9A	3	2	AA	5	2	BA	4	3				A + M → A	•	•	↕	↕	R	•
	ORAB	CA	2	2	DA	3	2	EA	5	2	FA	4	3				B + M → B	•	•	↕	↕	R	•
Push Data	PSHA													36	4	1	A → M_{SP}, SP – 1 → SP	•	•	•	•	•	•
	PSHB													37	4	1	B → M_{SP}, SP – 1 → SP	•	•	•	•	•	•
Pull Data	PULA													32	4	1	SP + 1 → SP, M_{SP} → A	•	•	•	•	•	•
	PULB													33	4	1	SP + 1 → SP, M_{SP} → B	•	•	•	•	•	•
Rotate Left	ROL							69	7	2	79	6	3				M	•	•	↕	↕	⑤	↕
	ROLA													49	2	1	A	•	•	↕	↕	⑤	↕
	ROLB													59	2	1	B (C b7 b0)	•	•	↕	↕	⑤	↕
Rotate Right	ROR							66	7	2	76	6	3				M	•	•	↕	↕	⑥	↕
	RORA													46	2	1	A	•	•	↕	↕	⑥	↕
	RORB													56	2	1	B (C b7 b0)	•	•	↕	↕	⑥	↕
Shift Left, Arithmetic	ASL							68	7	2	78	6	3				M	•	•	↕	↕	⑥	↕
	ASLA													48	2	1	A (0 C b7 b0)	•	•	↕	↕	⑥	↕
	ASLB													58	2	1	B (0 C b7 b0)	•	•	↕	↕	⑥	↕
Shift Right, Arithmetic	ASR							67	7	2	77	6	3				M	•	•	↕	↕	⑥	↕
	ASRA													47	2	1	A (b7 b0 C)	•	•	↕	↕	⑥	↕
	ASRB													57	2	1	B (b7 b0 C)	•	•	↕	↕	⑥	↕
Shift Right, Logic	LSR							64	7	2	74	6	3				M	•	•	R	↕	⑥	↕
	LSRA													44	2	1	A (0 b7 b0 C)	•	•	R	↕	⑥	↕
	LSRB													54	2	1	B (0 b7 b0 C)	•	•	R	↕	⑥	↕
Store Acmltr.	STAA				97	4	2	A7	6	2	B7	5	3				A → M	•	•	↕	↕	R	•
	STAB				D7	4	2	E7	6	2	F7	5	3				B → M	•	•	↕	↕	R	•
Subtract	SUBA	80	2	2	90	3	2	A0	5	2	B0	4	3				A – M → A	•	•	↕	↕	↕	↕
	SUBB	C0	2	2	D0	3	2	E0	5	2	F0	4	3				B – M → B	•	•	↕	↕	↕	↕
Subtract Acmltrs.	SBA													10	2	1	A – B → A	•	•	↕	↕	↕	↕
Subtr. with Carry	SBCA	82	2	2	92	3	2	A2	5	2	B2	4	3				A – M – C → A	•	•	↕	↕	↕	↕
	SBCB	C2	2	2	D2	3	2	E2	5	2	F2	4	3				B – M – C → B	•	•	↕	↕	↕	↕
Transfer Acmltrs	TAB													16	2	1	A → B	•	•	↕	↕	R	•
	TBA													17	2	1	B → A	•	•	↕	↕	R	•
Test, Zero or Minus	TST							6D	7	2	7D	6	3				M – 00	•	•	↕	↕	R	R
	TSTA													4D	2	1	A – 00	•	•	↕	↕	R	R
	TSTB													5D	2	1	B – 00	•	•	↕	↕	R	R
																		H	I	N	Z	V	C

LEGEND:

OP	Operation Code (Hexadecimal);	+	Boolean Inclusive OR;
~	Number of MPU Cycles;	⊕	Boolean Exclusive OR;
#	Number of Program Bytes;	M	Complement of M;
+	Arithmetic Plus;	→	Transfer Into;
–	Arithmetic Minus;	0	Bit = Zero;
·	Boolean AND;	00	Byte = Zero;
M_{SP}	Contents of memory location pointed to be Stack Pointer;		

Note – Accumulator addressing mode instructions are included in the column for IMPLIED addressing

CONDITION CODE SYMBOLS:

H	Half-carry from bit 3;
I	Interrupt mask
N	Negative (sign bit)
Z	Zero (byte)
V	Overflow, 2's complement
C	Carry from bit 7
R	Reset Always
S	Set Always
↕	Test and set if true, cleared otherwise
•	Not Affected

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MC6809(E)
(1.0 MHz)

MC68A09(E)
(1.5 MHz)

MC68B09(E)
(2.0 MHz)

HIGH-PERFORMANCE MICROPROCESSOR

■ MC6800 COMPATIBLE

- Hardware — Interfaces With All M6800 Peripherals
- Software — Upward Compatible Instruction Set and Addressing Modes

■ HARDWARE FEATURES

- On-Chip Oscillator (MC6809)
- Optional ÷1 External Clock Inputs (MC6809E)
- MRDY Input Extends Data Access Times for Use With Slow Memory
- $\overline{BREQ}$/TSC Allows Quick Access to Bus for DMA and Memory Refresh
- Last Instruction Cycle Output for Identification of Opcode Fetch (MC6809E)
- Fast Interrupt Request Input Stacks Only Program Counter and Condition Code
- Interrupt Acknowledge Output Allows Vectoring by Device
- Busy Output Eases Multiprocessor Design (MC6809E)

■ ARCHITECTURAL FEATURES

- Two 8-Bit Accumulators Can Be Concatenated to Form One 16-Bit Accumulator
- Two 16-Bit Index Registers
- Two 16-Bit Indexable Stack Pointers
- Direct Page Register Allows Direct Addressing Throughout Memory Space

■ INSTRUCTION SET

- Extended Range Branches
- 16-Bit Arithmetic
- Push/Pull Any Register or Set of Registers To/From Either Stack
- 8 X 8 Unsigned Multiply
- Transfer/Exchange Any Two Registers of Equal Size
- Enhanced Pointer Register Manipulation

■ ADDRESSING MODES

- All MC6800 Modes, Plus PC Relative, Extended Indirect, Indexed Indirect, and PC Relative Indirect
- Direct Addressing Available for All Memory Access Instructions
- Index Mode Options Include Accumulator or Up to 16-Bit Constant Offset, and Auto-Increment/Decrement (by 1 or 2) With Any of the Four Pointer Registers

FIGURE 1 – BLOCK DIAGRAMS

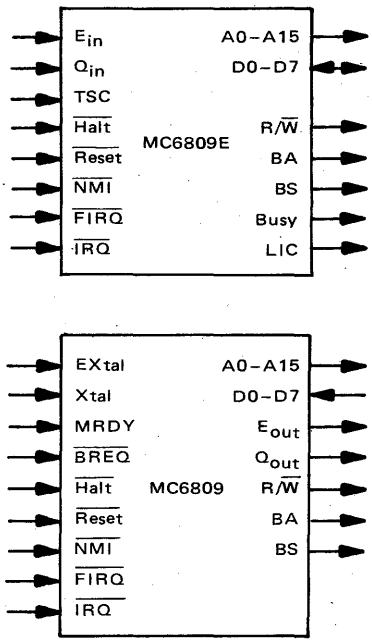
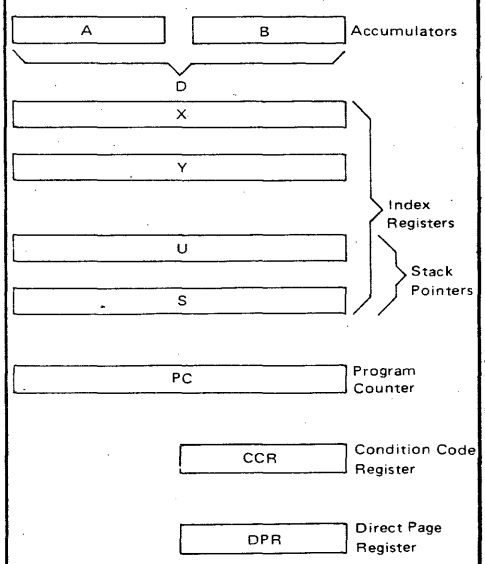


FIGURE 3 – PROGRAMMING MODEL



MICROPROCESSOR

Motorola

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TABLE 2 – 8-BIT ACCUMULATOR AND MEMORY INSTRUCTIONS

Mnemonic(s)	Operation	Addressing Modes								
		Implied	Immediate	Direct	Extended	Extended Indirect	Indexed	Indexed Indirect	Relative	Relative Indirect
ADCA, ADCB	Add memory to accumulator with carry	–	X	X	X	X	X	X	X	X
ADDA, ADDB	Add memory to accumulator	–	X	X	X	X	X	X	X	X
ANDA, ANDB	And memory with accumulator	–	X	X	X	X	X	X	X	X
ASL	Arithmetic shift left memory location	–	–	X	X	X	X	X	X	X
ASLA, ASLB	Arithmetic shift left accumulator	X	–	–	–	–	–	–	–	–
ASR	Arithmetic shift right memory location	–	–	X	X	X	X	X	X	X
ASRA, ASRB	Arithmetic shift right accumulator	X	–	–	–	–	–	–	–	–
BITA, BITB	Bit test memory with accumulator	–	X	X	X	X	X	X	X	X
CLR	Clear memory location	–	–	X	X	X	X	X	X	X
CLRA, CLRB	Clear accumulator	X	–	–	–	–	–	–	–	–
CMPA, CMPB	Compare memory with accumulator	–	X	X	X	X	X	X	X	X
COM	Complement memory location	–	–	X	X	X	X	X	X	X
COMA, COMB	Complement accumulator	X	–	–	–	–	–	–	–	–
DAA	Decimal adjust A-accumulator	X	–	–	–	–	–	–	–	–
DEC	Decrement memory location	–	–	X	X	X	X	X	X	X
DECA, DECB	Decrement accumulator	X	–	–	–	–	–	–	–	–
EORA, EORB	Exclusive or memory with accumulator	–	X	X	X	X	X	X	X	X
EXG R1, R2	Exchange R1 with R2 (R1, R2 = A, B, CC, DP)	X	–	–	–	–	–	–	–	–
INC	Increment memory location	–	–	X	X	X	X	X	X	X
INCA, INCB	Increment accumulator	X	–	–	–	–	–	–	–	–
LDA, LDB	Load accumulator from memory	–	X	X	X	X	X	X	X	X
LSL	Logical shift left memory location	–	–	X	X	X	X	X	X	X
LSLA, LSLB	Logical shift left accumulator	X	–	–	–	–	–	–	–	–
LSR	Logical shift right memory location	–	–	X	X	X	X	X	X	X
LSRA, LSRB	Logical shift right accumulator	X	–	–	–	–	–	–	–	–
MUL	Unsigned multiply (AXB → D)	X	–	–	–	–	–	–	–	–
NEG	Negate memory location	–	–	X	X	X	X	X	X	X
NEGA, NEGB	Negate accumulator	X	–	–	–	–	–	–	–	–
ORA, ORB	Or memory with accumulator	–	X	X	X	X	X	X	X	X
ROL	Rotate memory location left	–	–	X	X	X	X	X	X	X
ROLA, ROLB	Rotate accumulator left	X	–	–	–	–	–	–	–	–
ROR	Rotate memory location right	–	–	X	X	X	X	X	X	X
RORA, RORB	Rotate accumulator right	X	–	–	–	–	–	–	–	–
SBCA, SBCB	Subtract memory from accumulator with borrow	–	X	X	X	X	X	X	X	X
STA, STB	Store accumulator to memory	–	–	X	X	X	X	X	X	X
SUBA, SUBB	Subtract memory from accumulator	–	X	X	X	X	X	X	X	X
TST	Test memory location	–	–	X	X	X	X	X	X	X
TSTA, TSTB	Test accumulator	X	–	–	–	–	–	–	–	–
TFR, R1, R2	Transfer R1 to R2 (R1, R2 = A, B, CC, DP)	X	–	–	–	–	–	–	–	–

NOTE: A and B may be pushed to (pulled from) either stack with PSHS, PSHU (PULS, PULU) instructions. See Table 3.

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TABLE 3 – 16-BIT ACCUMULATOR AND MEMORY INSTRUCTIONS

Mnemonic(s)	Operation	Addressing Modes								
		Implied	Immediate	Direct	Extended	Extended Indirect	Indexed	Indexed Indirect	Relative	Relative Indirect
ADDD	Add memory to D accumulator	–	X	X	X	X	X	X	X	X
CMPD	Compare memory with D accumulator	–	X	X	X	X	X	X	X	X
EXG D, R	Exchange D with X, Y, S, U, or PC	X	–	–	–	–	–	–	–	–
LDD	Load D accumulator from memory	–	X	X	X	X	X	X	X	X
SEX	Sign Extend	X	–	–	–	–	–	–	–	–
STD	Store D accumulator to memory	–	–	X	X	X	X	X	X	X
SUBD	Subract memory from D accumulator	–	X	X	X	X	X	X	X	X
TFR D, R	Transfer D to X, Y, S, U, or PC	X	–	–	–	–	–	–	–	–
TFR R, D	Transfer X, Y, S, U, or PC to D	X	–	–	–	–	–	–	–	–

TABLE 4 – INDEX REGISTER/STACK POINTER INSTRUCTIONS

Mnemonic(s)	Operation	Addressing Modes								
		Implied	Immediate	Direct	Extended	Extended Indirect	Indexed	Indexed Indirect	Relative	Relative Indirect
CMPS, CMPU	Compare memory with stack pointer	–	X	X	X	X	X	X	X	X
CMPX, CMPY	Compare memory with index register	–	X	X	X	X	X	X	X	X
EXG R1, R2	Exchange D, X, Y, S, U, or PC with D, X, Y, S, U, or PC	X	–	–	–	–	–	–	–	–
LEAS, LEAU	Load effective address into stack pointer	–	–	–	–	X	X	X	X	X
LEAX, LEAY	Load effective address into index register	–	–	–	–	X	X	X	X	X
LDS, LDU	Load stack pointer from memory	–	X	X	X	X	X	X	X	X
LDX, LDY	Load index register from memory	–	X	X	X	X	X	X	X	X
PSHS	Push any register(s) onto hardware stack (except S)	X	–	–	–	–	–	–	–	–
PSHU	Push any register(s) onto user stack (except U)	X	–	–	–	–	–	–	–	–
PULS	Pull any register(s) from hardware stack (except S)	X	–	–	–	–	–	–	–	–
PULU	Pull any register(s) from hardware stack (except U)	X	–	–	–	–	–	–	–	–
STS, STU	Store stack pointer to memory	–	–	X	X	X	X	X	X	X
STX, STY	Store index register to memory	–	–	X	X	X	X	X	X	X
TFR R1, R2	Transfer D, X, U, or PC to D, X, S, U, or PC	X	–	–	–	–	–	–	–	–
ABX	Add B-accumulator to X (unsigned)	X	–	–	–	–	–	–	–	–

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TABLE 5 – BRANCH INSTRUCTIONS

Mnemonic(s)	Operation	Addressing Modes								
		Implied	Immediate	Direct	Extended	Extended Indirect	Indexed	Indexed Indirect	Relative	Relative Indirect
BCC, LBCC	Branch if carry clear	–	–	–	–	–	–	–	X	–
BCS, LBCS	Branch if carry set	–	–	–	–	–	–	–	X	–
BEQ, LBEQ	Branch if equal	–	–	–	–	–	–	–	X	–
BGE, LBGE	Branch if greater than or equal (signed)	–	–	–	–	–	–	–	X	–
BGT, LBGT	Branch if greater (signed)	–	–	–	–	–	–	–	X	–
BHI, LBHI	Branch if higher (unsigned)	–	–	–	–	–	–	–	X	–
BHS, LBHS	Branch if higher or same (unsigned)	–	–	–	–	–	–	–	X	–
BLE, LBLE	Branch if less than or equal (signed)	–	–	–	–	–	–	–	X	–
BLO, LBLO	Branch if lower (unsigned)	–	–	–	–	–	–	–	X	–
BLS, LBLS	Branch if lower or same (unsigned)	–	–	–	–	–	–	–	X	–
BLT, LBLT	Branch if less than (signed)	–	–	–	–	–	–	–	X	–
BMI, LBMI	Branch if minus	–	–	–	–	–	–	–	X	–
BNE, LBNE	Branch if not equal	–	–	–	–	–	–	–	X	–
BPL, LBPL	Branch if plus	–	–	–	–	–	–	–	X	–
BRA, LBRA	Branch always	–	–	–	–	–	–	–	X	–
BRN, LBRN	Branch never (3, 5 Cycle NOP)	–	–	–	–	–	–	–	X	–
BSR, LBSR	Branch to subroutine	–	–	–	–	–	–	–	X	–
BVC, LBVC	Branch if overflow clear	–	–	–	–	–	–	–	X	–
BVS, LBVS	Branch if overflow set	–	–	–	–	–	–	–	X	–

TABLE 6 – MISCELLANEOUS INSTRUCTIONS

Mnemonic(s)	Operation	Addressing Modes								
		Implied	Immediate	Direct	Extended	Extended Indirect	Indexed	Indexed Indirect	Relative	Relative Indirect
ANDCC	AND condition code register	–	X	–	–	–	–	–	–	–
CWAI	AND condition code register, then wait for interrupt	–	X	–	–	–	–	–	–	–
NOP	No operation	X	–	–	–	–	–	–	–	–
ORCC	OR condition code register	–	X	–	–	–	–	–	–	–
JMP	Jump	–	–	X	X	X	X	X	X	X
JSR	Jump to subroutine	–	–	X	X	X	X	X	X	X
RTI	Return from interrupt	X	–	–	–	–	–	–	–	–
RTS	Return from subroutine	X	–	–	–	–	–	–	–	–
SWI, SWI2, SWI3	Software interrupt (absolute indirect)	X	–	–	–	–	–	–	–	–
SYNC	Synchronize with interrupt line	X	–	–	–	–	–	–	–	–

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MOTOROLA Semiconductors
3501 ED BLUESTEIN BLVD., AUSTIN, TEXAS 78721

MC14500B

INDUSTRIAL CONTROL UNIT

The MC14500B Industrial Control Unit (ICU) is a single bit CMOS processor. The ICU is designed for use in systems requiring decisions based on successive single bit information. An external ROM stores the control program. With a program counter (and output latches and input multiplexers, if required) the ICU in a system forms a stored program controller that replaces combinatorial logic. Applications include relay logic processing, serial data manipulation and control. The ICU also may control an MPU or be controlled by an MPU.

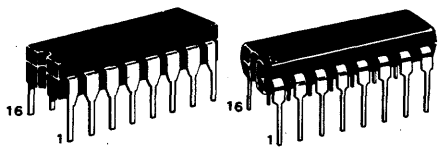
- 16 Instructions
- DC to 1.0 MHz Operation at V_{DD} = 5 V
- On Chip Clock (Oscillator)
- Executes One Instruction per Clock Cycle
- 3 V to 18 V Operation
- Noise Immunity Typically 45% of V_{DD}
- Quiescent Current 5.0 μAdc Typical at V_{DD} = 5 V
- Capable of Driving One Low-Power Schottky Load or Two Low-Power TTL Loads over Full Temperature Range

Detailed operation and applications are given in the "MC14500B Industrial Control Unit" handbook.

CMOS LSI

(LOW-POWER COMPLEMENTARY MOS)

INDUSTRIAL CONTROL UNIT



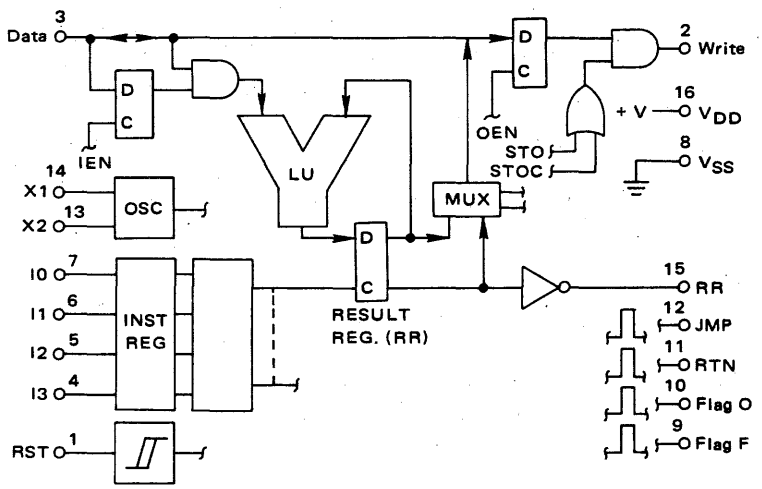
L SUFFIX
CERAMIC PACKAGE
CASE 620

P SUFFIX
PLASTIC PACKAGE
CASE 648

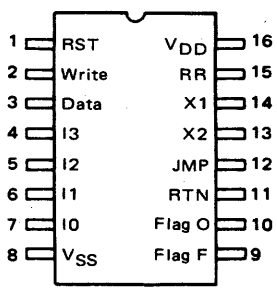
ORDERING INFORMATION

MC14XXXB — Suffix Denotes
- L Ceramic Package
- P Plastic Package
- A Extended Operating Temperature Range
- C Limited Operating Temperature Range

BLOCK DIAGRAM



PIN ASSIGNMENT



MAXIMUM RATINGS (Voltages referenced to V_{SS})

Rating	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	-0.5 to +18	Vdc
Input Voltage, All Inputs	V_{in}	-0.5 to V_{DD} + 0.5	Vdc
DC Current Drain per Pin	I	10	mAdc
Operating Temperature Range — AL Device CL/CP Device	T_A	-55 to +125 -40 to +85	°C
Storage Temperature Range	T_{stg}	-65 to +150	°C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range $V_{SS} \leq (V_{in}$ or $V_{out}) \leq V_{DD}$.

This is advance information and specifications are subject to change without notice.

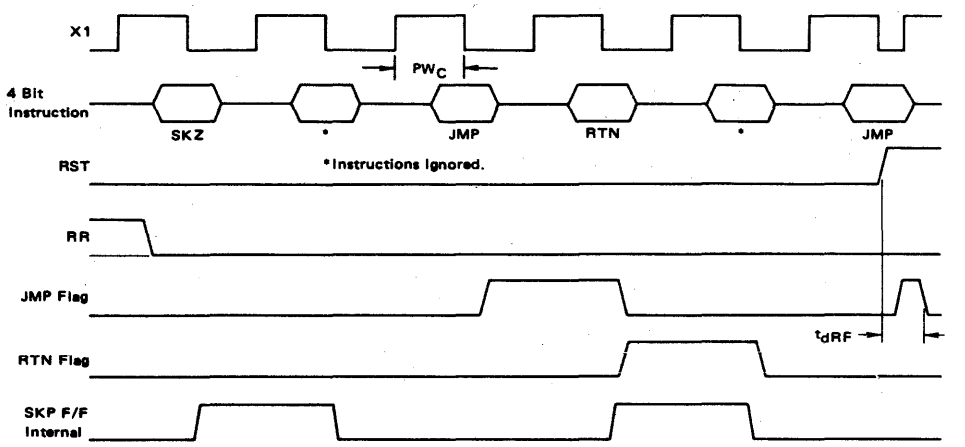
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DS 9466
Formerly ADI-437

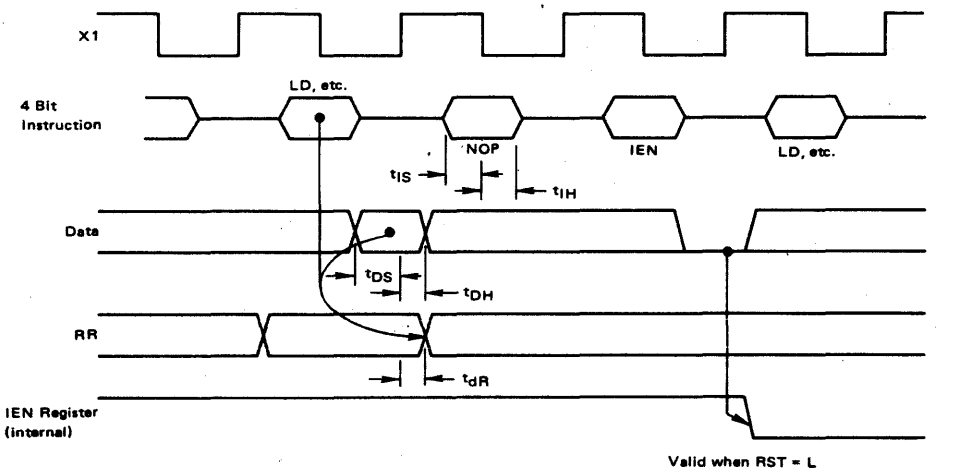
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TIMING WAVEFORMS

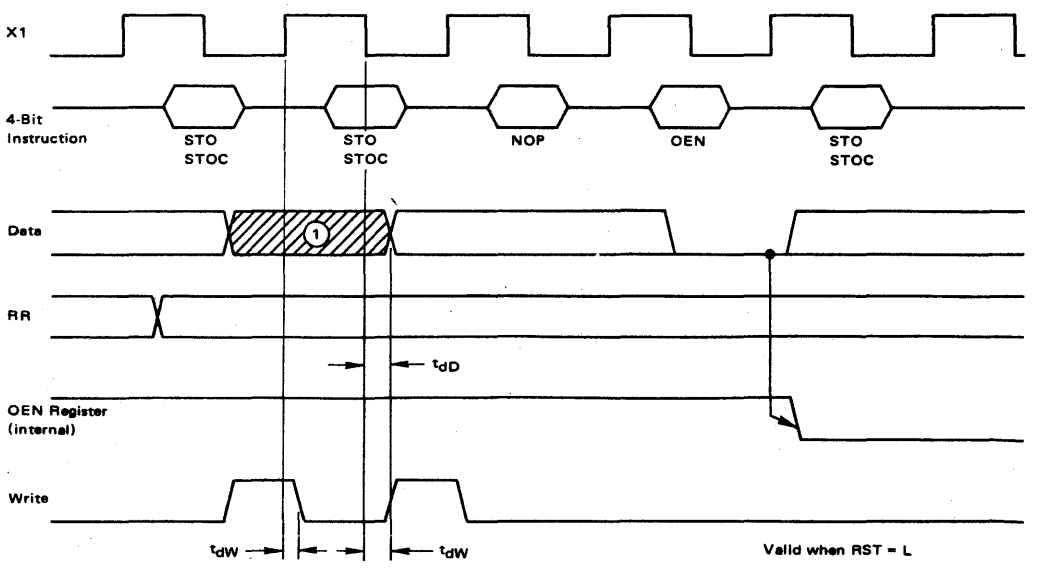
Instructions SKZ, JMP, RTN RR, IEN, OEN remain unaffected



Instructions LD, LDC, AND, ANDC, OR, ORC, XNOR, IEN



Instructions STO, STOC, OEN



NOTE 1. Valid output data.

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ELECTRICAL CHARACTERISTICS

Characteristic		Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Output Voltage	"0" Level	V_{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
V_{in} = V_{DD} or 0			10	–	0.05	–	0	0.05	–	0.05	
			15	–	0.05	–	0	0.05	–	0.05	
	"1" Level	V_{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
V_{in} = 0 or V_{DD}			10	9.95	–	9.95	10	–	9.95	–	
			15	14.95	–	14.95	15	–	14.95	–	
Input Voltage #	"0 Level"	V_{IL}									Vdc
RST, D, X2											
(V_O = 4.5 or 0.5 Vdc)			5.0	–	1.5	–	2.25	1.5	–	1.5	
(V_O = 9.0 or 1.0 Vdc)			10	–	3.0	–	4.50	3.0	–	3.0	
(V_O = 13.5 or 1.5 Vdc)			15	–	4.0	–	6.75	4.0	–	4.0	
	"1" Level	V_{IH}									Vdc
(V_O = 0.5 or 4.5 Vdc)			5.0	3.5	–	3.5	2.75	–	3.5	–	
(V_O = 1.0 or 9.0 Vdc)			10	7.0	–	7.0	5.50	–	7.0	–	
(V_O = 1.5 or 13.5 Vdc)			15	11.0	–	11.0	8.25	–	11.0	–	
Input Voltage #	"0" Level	V_{IL}									Vdc
I0, I1, I2, I3											
(V_O = 4.5 or 0.5 Vdc)			5.0	–	0.8	–	1.1	0.8	–	0.8	
(V_O = 9.0 or 1.0 Vdc)			10	–	1.6	–	2.2	1.6	–	1.6	
(V_O = 13.5 or 1.5 Vdc)			15	–	2.4	–	3.4	2.4	–	2.4	
	"1" Level	V_{IH}									Vdc
(V_O = 0.5 or 4.5 Vdc)			5.0	2.0	–	2.0	1.9	–	2.0	–	
(V_O = 1.0 or 9.0 Vdc)			10	6.0	–	6.0	3.1	–	6.0	–	
(V_O = 1.5 or 13.5 Vdc)			15	10	–	10	4.3	–	10	–	
Output Drive Current	Source	I_{OH}									mAdc
Data, Write (AL/CL/CP Device)											
(V_{OH} = 4.6 Vdc)			5.0	-1.0	–	-1.0	-2.0	–	-1.0	–	
(V_{OH} = 9.5 Vdc)			10	–	–	–	-6.0	–	–	–	
(V_{OH} = 13.5 Vdc)			15	–	–	–	-12	–	–	–	
(V_{OL} = 0.4 Vdc)	Sink	I_{OL}	5.0	1.6	–	1.6	3.2	–	1.6	–	mAdc
(V_{OL} = 0.5 Vdc)			10	–	–	–	6.0	–	–	–	
(V_{OL} = 1.5 Vdc)			15	–	–	–	12	–	–	–	
Output Drive Current	Source	I_{OH}									mAdc
Other Outputs (AL Device)											
(V_{OH} = 2.5 Vdc)			5.0	-3.0	–	-2.4	-4.2	–	-1.7	–	
(V_{OH} = 4.6 Vdc)			5.0	-0.64	–	-0.51	-0.88	–	-0.36	–	
(V_{OH} = 9.5 Vdc)			10	-1.6	–	-1.3	-2.25	–	-0.9	–	
(V_{OH} = 13.5 Vdc)			15	-4.2	–	-3.4	8.8	–	-2.4	–	
(V_{OL} = 0.4 Vdc)	Sink	I_{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)			10	1.6	–	1.3	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)			15	4.2	–	3.4	8.8	–	2.4	–	
Output Drive Current	Source	I_{OH}									mAdc
Other Outputs (CL/CP Device)											
(V_{OH} = 2.5 Vdc)			5.0	-2.5	–	-2.1	-4.2	–	-1.7	–	
(V_{OH} = 4.6 Vdc)			5.0	-0.52	–	-0.44	-0.88	–	-0.36	–	
(V_{OH} = 9.5 Vdc)			10	-1.3	–	-1.1	-2.25	–	-0.9	–	
(V_{OH} = 13.5 Vdc)			15	-3.6	–	-3.0	-8.8	–	-2.4	–	
(V_{OL} = 0.4 Vdc)	Sink	I_{OL}	5.0	0.52	–	0.44	0.88	–	0.36	–	mAdc
(V_{OL} = 0.5 Vdc)			10	1.3	–	1.1	2.25	–	0.9	–	
(V_{OL} = 1.5 Vdc)			15	3.6	–	3.0	8.8	–	2.4	–	

Characteristic	Symbol	V_{DD} Vdc	T_{low}* Min	T_{low}* Max	25°C Min	25°C Typ	25°C Max	T_{high}* Min	T_{high}* Max	Unit
Input Current, RST (AL/CL/CP Device)	I_{in}	15	25	–	–	150	–	–	250	µAdc
Input Current (AL Device)	I_{in}	15	–	±0.1	–	±0.00001	±0.1	–	±1.0	µAdc
Input Current (CL/CP Device)	I_{in}	15	–	±0.3	–	±0.00001	±0.3	–	±1.0	µAdc
Input Capacitance (Data)	C_{in}	–	–	–	–	15	–	–	–	pF
Input Capacitance (All Other Inputs) (V_{in} = 0)	C_{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (AL Device)	I_{DD}	5.0	–	5.0	–	0.005	5.0	–	150	µAdc
(Per Package)		10	–	10	–	0.010	10	–	300	
		15	–	20	–	0.015	20	–	600	
Quiescent Current (CL/CP Device)	I_{DD}	5.0	–	20	–	0.005	20	–	150	µAdc
(Per Package)		10	–	40	–	0.010	40	–	300	
		15	–	80	–	0.015	80	–	600	
**Total Supply Current at an External Load Capacitance (C_L) on All Outputs	I_T	–	I_T = (1.5 µA/kHz) f + I_{DD} I_T = (3.0 µA/kHz) f + I_{DD} I_T = (4.5 µA/kHz) f + I_{DD}							µAdc

* T_{low} = -55°C for AL Device, -40°C for CL/CP Device.
T_{high} = +125°C for AL Device, +85°C for CL/CP Device.

** The formulas given are for the typical characteristics only at 25°C.

Noise immunity specified for worst-case input combination.

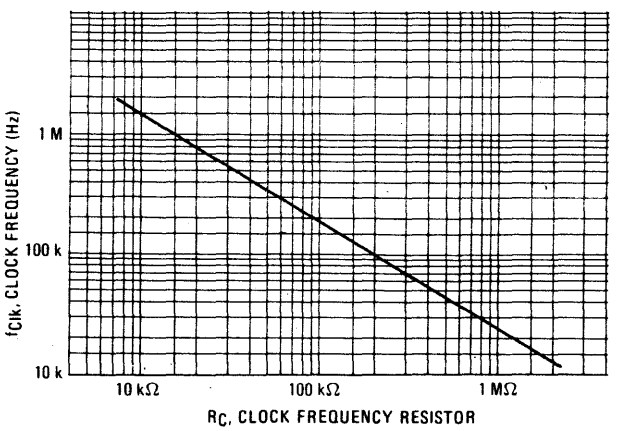
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SWITCHING CHARACTERISTICS (T_A = 25°C; $t_r = t_f$ = 20 ns for X and I inputs; C_L = 50 pF for JMP, X1, RR, Flag O, Flag F; C_L = 130 pF + 1TTL load for Data and Write.)

Characteristic	Symbol	V_{DD} Vdc	All Types Min	Typ	Max	Unit
Propagation Delay Time X1 to RR	t_{dR}	5.0	–	250	500	ns
		10	–	125	250	
		15	–	100	200	
X1 to Flag F, Flag O, RTN, JMP	t_{dF}	5.0	–	200	400	ns
		10	–	100	200	
		15	–	85	170	
X1 to Write	t_{dW}	5.0	–	225	450	ns
		10	–	125	250	
		15	–	100	200	
X1 to Data	t_{dD}	5.0	–	250	500	ns
		10	–	120	240	
		15	–	100	200	
RST to RR	t_{dRRR}	5.0	–	250	500	ns
		10	–	125	250	
		15	–	100	200	
RST to X1	t_{dRX}	5.0	–	450	Note 1	ns
		10	–	200		
		15	–	150		
RST to Flag F, Flag O, RTN, JMP	t_{dRF}	5.0	–	400	800	ns
		10	–	200	400	
		15	–	150	300	
RST to Write, Data	t_{dRW}	5.0	–	450	900	ns
		10	–	225	450	
		15	–	175	350	
Minimum Clock Pulse Width, X1	PW_C	5.0	–	200	400	ns
		10	–	100	200	
		15	–	90	180	
Minimum Reset Pulse Width, RST	PW_R	5.0	–	250	500	ns
		10	–	125	250	
		15	–	100	200	
Setup Time – Instruction	t_{IS}	5.0	400	200	–	ns
		10	250	125	–	
		15	180	90	–	
Data	t_{DS}	5.0	200	100	–	ns
		10	100	50	–	
		15	80	40	–	
Hold Time – Instruction	t_{IH}	5.0	100	0	–	ns
		10	50	0	–	
		15	50	0	–	
Data	t_{DH}	5.0	200	100	–	ns
		10	100	50	–	
		15	100	50	–	

NOTE 1. Maximum Reset Delay may extend to one-half clock period.

FIGURE 1 – TYPICAL CLOCK FREQUENCY versus RESISTOR (R_C)



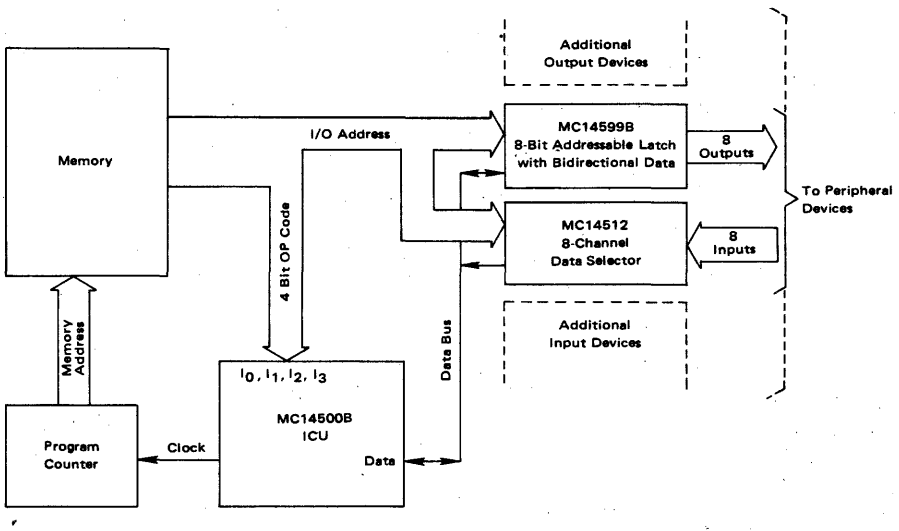
Pin No.	Function	Symbols
1	Chip Reset	RST
2	Write Pulse	Write
3	Data In/Out	Data
4	MSB Instruction Word	I_3
5	Bit 2 Instruction Word	I_2
6	Bit 1 Instruction Word	I_1
7	LSB Instruction Word	I_0
8	Negative Supply (Ground)	V_{SS}
9	Flag on NOP F	Flag F
10	Flag on NOP O	Flag O
11	Subroutine Return Flag	RTN
12	Jump Instruction Flag	JMP
13	Oscillator Input	X2
14	Oscillator Output	X1
15	Result Register	RR
16	Positive Supply	V_{DD}

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TABLE 1. MC14500B INSTRUCTION SET

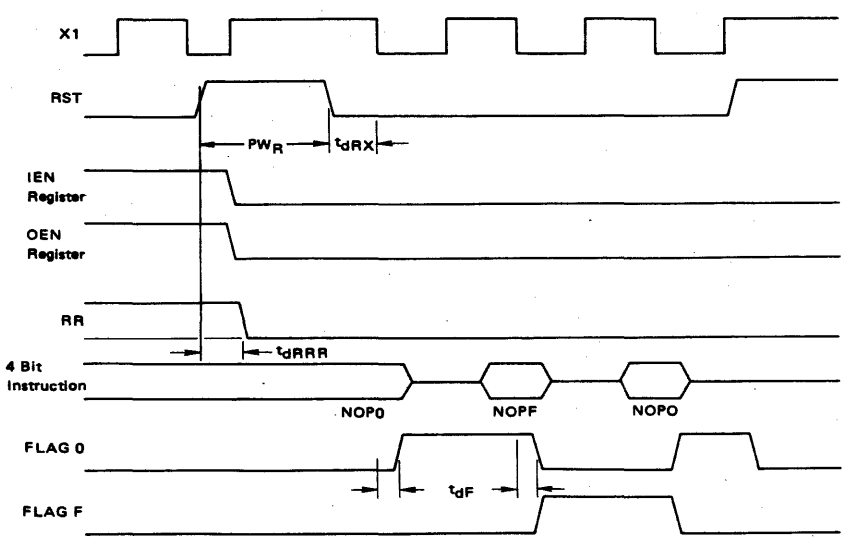
Instruction Code	Mnemonic	Action
0 0000	NOPO	No change in registers. RR → RR, Flag O → ⎍
1 0001	LD	Load result register. Data → RR
2 0010	LDC	Load complement. $\overline{\text{Data}}$ → RR
3 0011	AND	Logical AND. RR·Data → RR
4 0100	ANDC	Logical AND complement. RR·$\overline{\text{Data}}$ → RR
5 0101	OR	Logical OR. RR + Data → RR
6 0110	ORC	Logical OR complement. RR + $\overline{\text{Data}}$ → RR
7 0111	XNOR	Exclusive NOR. If RR = Data, RR → 1
8 1000	STO	Store. RR → Data Pin, Write → ⎍
9 1001	STOC	Store complement. $\overline{\text{RR}}$ → Data Pin, Write → ⎍
A 1010	IEN	Input enable. Data → IEN Register
B 1011	OEN	Output enable. Data → OEN Register
C 1100	JMP	Jump. JMP Flag → ⎍
D 1101	RTN	Return. RTN Flag → ⎍ and skip next instruction
E 1110	SKZ	Skip next instruction if RR = 0
F 1111	NOPF	No change in registers. RR → RR, Flag F → ⎍

FIGURE 2 – OUTLINE OF A TYPICAL ORGANIZATION FOR A MC14500B-BASED SYSTEM



TIMING WAVEFORMS

Instructions NOPO, NOPF
RR, IEN, OEN remain unaffected



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ABBREVIATIONS OF COMPANY NAMES

AD	Analog Devices
AMD	Advanced Micro Devices
AMI	American Microsystems, Inc.
Amperex	Amperex Electronics Corp.
Analogic	Analogic Corp.
Beckman	Beckman Instruments, Helipot Division
BEI	BEI Electronics
Burr-Brown	Burr-Brown Research
Cermetek	Cermetek
Cherry	Cherry Semiconductor
CMA	Consumer Microcircuits of America
Cybernetic	Cybernetic Micro Systems
Data General	Data General
Datel	Datel Systems
DDC	Data Devices Corp.
Delco	Delco Electronics
Dionics	Dionics Inc.
EA	Electronic Arrays
EMM/Semi	EMM Semi, Div. of Electronic Memories & Magnetics
Essex	Essex International
Exar	Exar Integrated Systems
Fairchild	Fairchild
Ferranti	Ferranti Electric
Fujitsu	Fujitsu
GI	General Instrument
Harris	Harris Semiconductor
Hitachi	Hitachi America Ltd.
Holt	Holt Inc.
Hughes	Hughes Aircraft Solid State Products
Hybrid Sys	Hybrid Systems
HyComp	HyComp
IMI	International Microcircuits, Inc.
Intech/FMI	Intech/Function Modules Inc.
Intel	Intel
Interdesign	Interdesign
Intersil	Intersil
IPI	Integrated Photomatrix, Inc.
Lambda	Lambda Electronics
LSI	LSI Computer Systems
Maruman	Maruman Integrated Circuits
Master Logic	Master Logic
Matrox	Matrox Electronics Systems
Micro Net	Micro Networks
Micropac	Micropac Industries
Micro Power	Micro Power Systems
Micro Tech	Microcircuits Technology
Mitel	Mitel Semiconductor
Mitsubishi	Mitsubishi Electric Co.
MMI	Monolithic Memories, Inc.
Monosil	Monosil
MOS	MOS Technology
Mostek	Mostek
Motorola	Motorola Semiconductor
National	National Semiconductor
NCR	NCR Corp., Microelectronics Division
NEC America	NEC America
NEC Micro	NEC Microcomputers
Nitron	Nitron
Nortec	Nortec Electronics
Novonics	Novonics
NPC	Nucleonic Products Co.
OEI	Optical Electronics, Inc.
OKI	OKI Semiconductor
Panasonic	Panasonic, Matsushita Electric Corp.
Photo Therm	Photo Therm
Plessey	Plessey Semiconductors
PMI	Precision Monolithics, Inc.
Raytheon	Raytheon Semiconductor
RCA	RCA Solid State Division
Reticon	Reticon
RIFA	RIFA
Rockwell	Rockwell Microelectronic Devices
RTC	Real Time Corp.
Sanken	Sanken Electric
Sanyo	Sanyo Electric
SGS	SGS-Ates Semiconductor
Siemens	Siemens
Signetics	Signetics (Philips)
Silicon G	Silicon General
Siliconix	Siliconix
Silicon Sys.	Silicon Systems, Inc.
Silitronics	Silitronics
SMC	Standard Microsystems
Solitron	Solitron Devices
Sprague	Sprague Electric Company
Supertex	Supertex, Inc.
SSM	Solid State Microtechnology for Music
SSS	Solid State Scientific
Synertek	Synertek
Telaris	Telaris
Teledyne C	Teledyne Crystalonics
Teledyne P	Teledyne Philbrick
Teledyne S	Teledyne Semiconductor
Telefunken	AEG-Telefunken
TI	Texas Instruments
TMX	TMX
Toshiba	Toshiba
Trans-Data	Trans-Data
TRW	TRW
Unitrode	Unitrode
Western	Western Digital
Zilog	Zilog

National Semiconductor

IDM2901A-1 4-Bit Bipolar Microprocessor

General Description

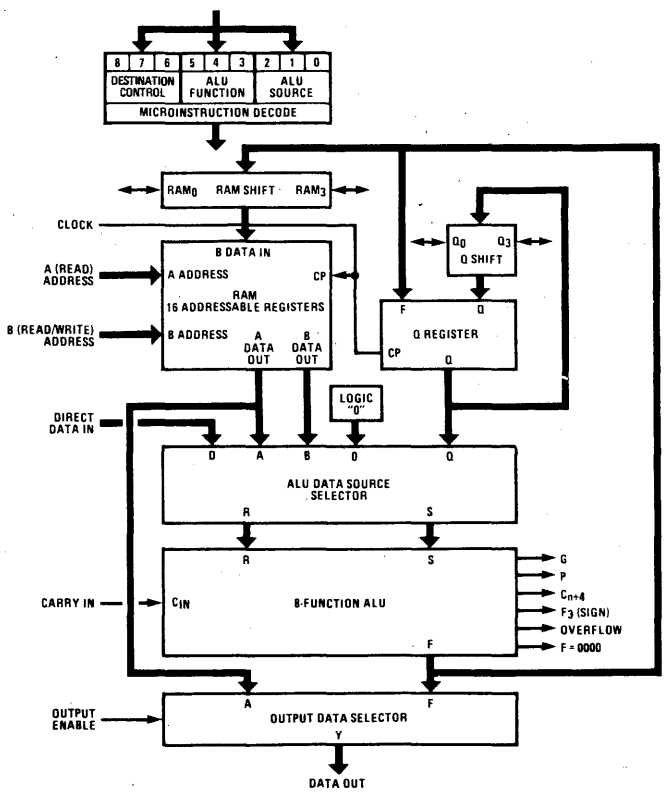
The IDM2901A-1 4-bit bipolar microprocessor slice is a cascadable device designed for use in Central Processing Units, programmable microprocessors, peripheral controllers, and other "high-speed" applications where economy, hardware/software flexibility, and easy expansion are system prerequisites. The building-block architecture and microinstruction format of the IDM2901A-1 permits efficient emulation of most digital-based systems.

As shown in the simplified block diagram, the IDM2901A-1 device consists of a 16-word by 4-bit 2-port RAM, a high-speed ALU, and the required shifting, decoding, and multiplexing circuits. The 9-bit microinstruction word is organized into three groups of three bits each — the first group (bits 0 - 2) selects ALU source operands, the second group (bits 3 - 5) selects the ALU function, and the last group (bits 6 - 8) selects the destination register within the ALU. The slice microprocessor is cascadable with full look-ahead or ripple carry; all outputs are TRI-STATE® and four status-flag outputs are available. To minimize power consumption and to maximize speed and reliability, the 40-pin LSI chip is fabricated using state-of-the-art (Low-Power Schottky) technology.

Features and Benefits

- **Multiple-address architecture** — improves system speed by providing simultaneous yet independent access to two working registers.
- **Multifunction ALU** — performs addition, two subtraction operations, and five logic functions on two source operands.
- **Flexible data-source selection** — for every ALU function, data is selected from five source ports for a total of 203 source operand pairs.
- **Left/right shift independent of ALU** — an arithmetic operation and a left or right shift can be obtained on the same machine cycle.
- **Four status flags** — carry, overflow, zero, and functional sign are available as outputs.
- **Expandable** — Connect any number of IDM2901A-1s together for longer word lengths.
- **Microprogrammable** — three groups of 3 bits each for source operand, ALU function, and destination control.

Block Diagram



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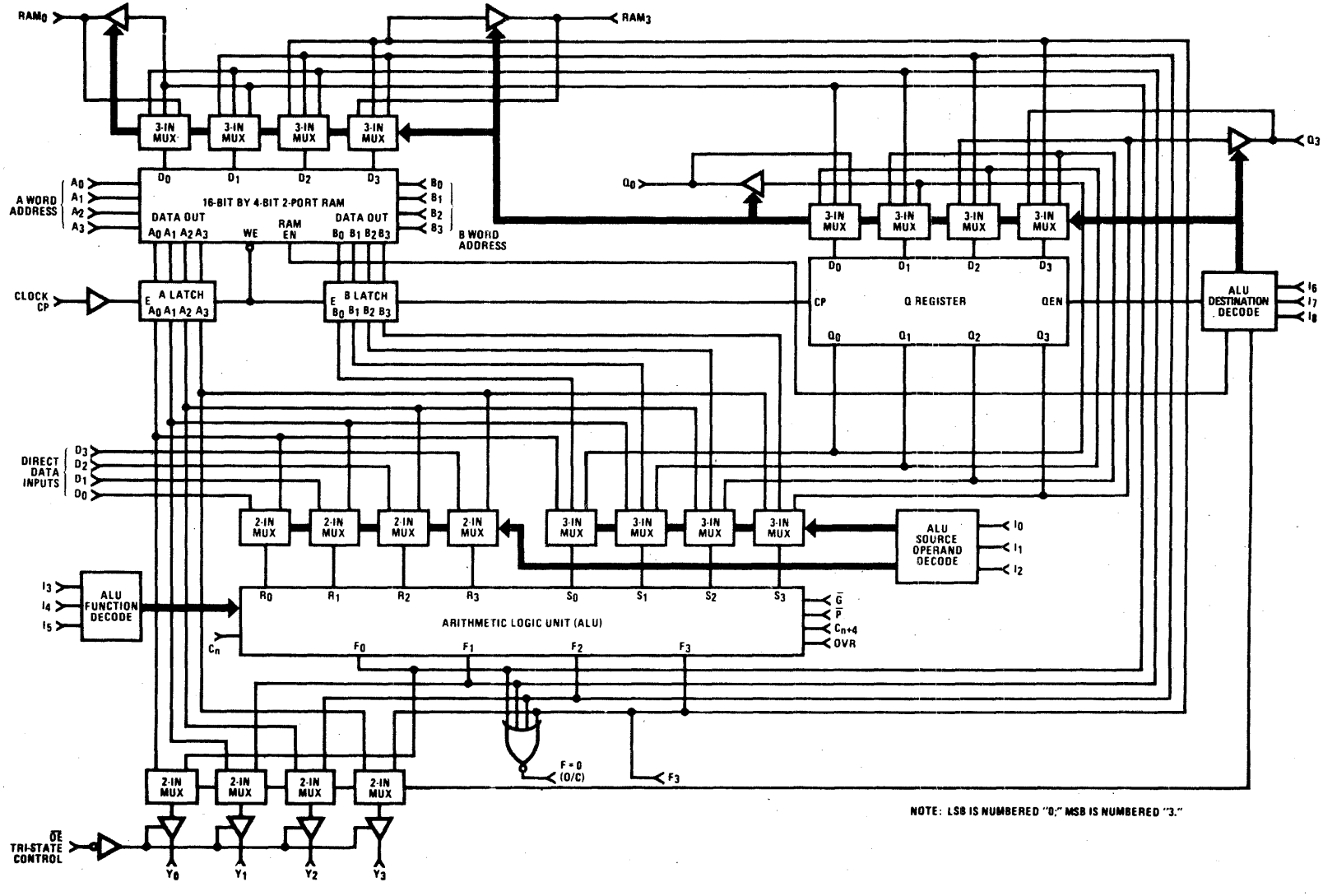


Figure 1. IDM2901A-1 Microprocessor, Detailed Block Diagram

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Guaranteed Operating Conditions Over Temperature and Voltage

When operated in a system, the timing requirements for the IDM2901A-1 are defined in tables 1, 2, and 3. Table 1 provides clock characteristics of the IDM2901A-1, table 2 gives the combinational delay times from input to output, and table 3 specifies setup and hold times. If used according to the specified delay and setup times, the device is guaranteed to function properly over the entire operating range. Table 3 defines the time prior to the end of the cycle (low-to-high transition of clock pulse) that each input must be stable to guarantee that the correct data is written into one of the internal registers.

Table 1. Cycle Time and Clock Characteristics

Time	IDM2901A-1	
	DC, NC	DM, DM/883
Read-Modify-Write Cycle (time from selection of A, B registers to end of cycle)	60 ns	75 ns
Maximum Clock Frequency to Shift Q Register (50% duty cycle)	16 MHz	16 MHz
Minimum Clock Low Time	25 ns	30 ns
Minimum Clock High Time	25 ns	30 ns
Minimum Clock Period	60 ns	75 ns

Table 2. Maximum Combinational Propagation Delays (all in ns; $C_L \leq 50$ pF)

	Commercial IDM2901A-1 DC, NC (0°C to +70°C; 5V ± 5%)								Military IDM2901A-1 DM, DM/883 (−55°C to +125°C; 5V ± 10%)							
To Output / From Input	Y	F_3	C_{n+4}	G/P	F=0 R_L = 470	OVR	Shift Outputs RAM_0 RAM_3	Shift Outputs Q_0 Q_3	Y	F_3	C_{n+4}	G/P	F=0 R_L = 470	OVR	Shift Outputs RAM_0 RAM_3	Shift Outputs Q_0 Q_3
A, B	50	50	50	45	55	60	55	–	60	60	60	60	65	75	65	–
D (arithmetic mode)	32	32	32	30	32	40	35	–	40	40	40	40	40	50	45	–
D (I = X37)	32	32	–	–	32	–	35	–	40	40	–	–	40	–	45	–
C_n	25	22	16	–	30	25	35	–	32	30	20	–	40	35	45	–
$I_{2,1,0}$	40	35	35	30	40	45	45	–	50	45	45	40	50	55	55	–
$I_{5,4,3}$	35	35	35	32	40	45	45	–	45	45	45	40	50	55	55	–
$I_{8,7,6}$	25	–	–	–	–	–	30	30	35	–	–	–	–	–	35	35
OE Enable/Disable	20/20	–	–	–	–	–	–	–	25/25	–	–	–	–	–	–	–
A Bypassing ALU (I = 2xx)	40	–	–	–	–	–	–	–	50	–	–	–	–	–	–	–
Clock ↓ (Note 6)	50	45	45	40	50	55	55	30	60	55	55	50	60	65	65	35

Table 3. Maximum Setup and Hold Times (all in ns) — Note 1

		Commercial IDM2901A-1 DC, NC (0°C to +70°C, 5V ± 5%)		Military IDM2901A-1 DM, DM/883 (−55°C to +125°C, 5V ± 10%)	
From Input	Notes	Setup Time	Hold Time	Setup Time	Hold Time
A, B Source	2, 3, 4, 5	60, $t_{pw}L$ + 20	0	75, $t_{pw}L$ + 25	0
B Destination	2, 4	$t_{pw}L$ + 15	0	$t_{pw}L$ + 15	0
D (arithmetic mode)		40	0	50	0
D (I = X37)	5	40	0	50	0
C_n		35	0	40	0
$I_{2,1,0}$		45	0	55	0
$I_{5,4,3}$		45	0	55	0
$I_{8,7,6}$	4	$t_{pw}L$ + 15	0	$t_{pw}L$ + 15	0
$RAM_{0,3}/Q_{0,3}$		15/10	0	25/15	0

Note 1: See figures 9 and 10.

Note 2: If the B address is used as a source operand, allow for the "A, B Source" setup time; if it is used only for the destination address, use the "B Destination" setup time.

Note 3: Where two numbers are shown, both must be met.

Note 4: "$t_{pw}L$" is the clock low time.

Note 5: DVO is the fastest way to load the RAM from the D inputs. This function is obtained with I = X37.

Note 6: Using Q register as source operand in arithmetic mode. Clock is not normally in critical speed path when Q is not a source.

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National Semiconductor

Preliminary
JULY 1978

INS8250 Asynchronous Communications Element

General Description

The INS8250 is a programmable Asynchronous Communications Element (ACE) chip contained in a standard 40-pin dual-in-line package. The chip, which is fabricated using N-channel silicon gate technology, functions as a serial data input/output interface in a microcomputer system. The functional configuration of the INS8250 is programmed by the system software via a TRI-STATE® 8-bit bidirectional data bus.

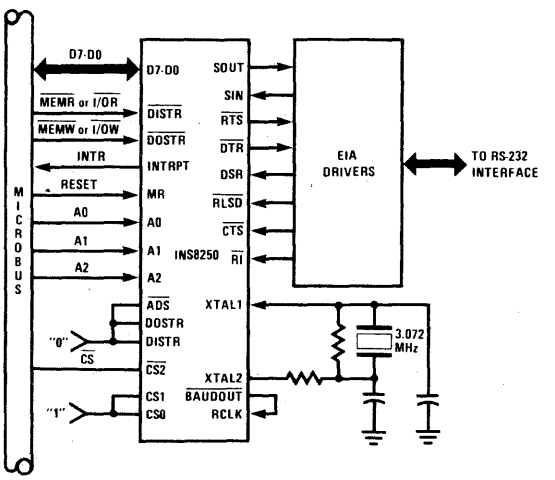
The INS8250 performs serial-to-parallel conversion on data characters received from a peripheral device or a MODEM, and parallel-to-serial conversion on data characters received from the CPU. The CPU can read the complete status of the INS8250 at any time during the functional operation. Status information reported includes the type and condition of the transfer operations being performed by the INS8250, as well as any error conditions (parity, overrun, framing, or break interrupt).

In addition to providing control of asynchronous data communications, the INS8250 includes a programmable Baud Generator that is capable of dividing the timing reference clock input by divisors of 1 to $(2^{16} - 1)$, and producing a 16x clock for driving the internal transmitter logic. Provisions are also included to use this 16x clock to drive the receiver logic. Also included in the INS8250 is a complete MODEM-control capability, and a processor-interrupt system that may be software tailored to the user's requirements to minimize the computing time required to handle the communications link.

Features

- Designed to be Easily Interfaced to Most Popular Microprocessors.
- Adds or Deletes Standard Asynchronous Communication Bits (Start, Stop, and Parity) to or from Serial Data Stream
- Full Double Buffering Eliminates Need for Precise Synchronization
- Independently Controlled Transmit, Receive, Line Status, and Data Set Interrupts
- Programmable Baud Rate Generator Allows Division of Any Input Clock by 1 to $(2^{16} - 1)$ and Generates the Internal 16x Clock
- Independent Receiver Clock Input
- MODEM Control Functions (CTS, RTS, DSR, DTR, RI, and Carrier Detect)
- Fully Programmable Serial-Interface Characteristics
  - 5-, 6-, 7-, or 8-Bit Characters
  - Even, Odd, or No-Parity Bit Generation and Detection
  - 1-, 1½-, or 2-Stop Bit Generation
  - Baud Rate Generation (DC to 56k Baud)
- False Start Bit Detection
- Complete Status Reporting Capabilities
- TRI-STATE TTL Drive Capabilities for Bidirectional Data Bus and Control Bus
- Line Break Generation and Detection
- Internal Diagnostic Capabilities
  - Loopback Controls for Communications Link Fault Isolation
  - Break, Parity, Overrun, Framing Error Simulation
- Full Prioritized Interrupt System Controls
- Single +5-Volt Power Supply
- MICROBUS™* Compatible

INS8250 MICROBUS Configuration



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Absolute Maximum Ratings

Temperature Under Bias . . . . . 0°C to +70°C
Storage Temperature . . . . . −65°C to +150°C
All Input or Output Voltages with Respect to V_{SS} . . . . −0.5 V to +7.0 V
Power Dissipation . . . . . 400 mW

Absolute maximum ratings indicate limits beyond which permanent damage may occur. Continuous operation at these limits is not intended; operation should be limited to those conditions specified under DC Electrical Characteristics.

DC Electrical Characteristics

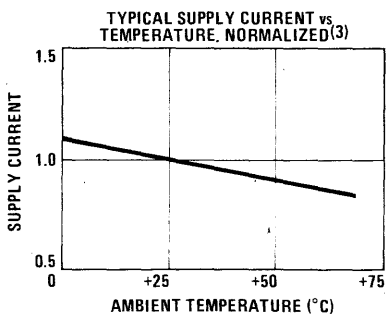
T_A = 0°C to +70°C, V_{CC} = +5 V ± 5%, V_{SS} = 0 V, unless otherwise specified.

Symbol	Parameter	Min	Typ	Max	Units	Test Conditions
V_{ILX}	Clock Input Low Voltage	−0.5		0.8	V	
V_{IHX}	Clock Input High Voltage	2.0		V_{CC}	V	
V_{IL}	Input Low Voltage	−0.5		0.8	V	
V_{IH}	Input High Voltage	2.0		V_{CC}	V	
V_{OL}	Output Low Voltage			0.4	V	I_{OL} = 1.6 mA on all outputs,
V_{OH}	Output High Voltage	2.4			V	I_{OH} = −100 μA
I_{CC} (AV)	Avg Power Supply Current (V_{CC})		65	80	mA	
I_{IL}	Input Leakage			±10	μA	
I_{CL}	Clock Leakage			±10	μA	

Capacitance

T_A = 25°C, V_{CC} = V_{SS} = 0 V

Symbol	Parameter	Min	Typ	Max	Units	Test Conditions
C_{XIN}	Clock Input Capacitance		15	20	pF	
C_{XOUT}	Clock Output Capacitance		20	30	pF	f_C = 1 MHz
C_{IN}	Input Capacitance		6	10	pF	Unmeasured pins returned to V_{SS}
C_{OUT}	Output Capacitance		10	20	pF	



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AC Electrical Characteristics

$T_A = 0°C$ to $\pm 70°C$, $V_{CC} = +5\ V \pm 5\%$

Symbol	Parameter	Min	Max	Units	Test Conditions
t_{AW}	Address Strobe Width	90	–	ns	
t_{AS}	Address Setup Time	110	–	ns	
t_{AH}	Address Hold Time	0	–	ns	
t_{CS}	Chip Select Setup Time	110	–	ns	
t_{CH}	Chip Select Hold Time	0	–	ns	
t_{CSS}	Chip Select Output Delay from Strobe	0	90	ns	-@ 100 pF loading
t_{DID}	$\overline{DISTR}$/DISTR Strobe Delay	0	–	ns	
t_{DIW}	$\overline{DISTR}$/DISTR Strobe Width	175	–	ns	
t_{RC}	Read Cycle Delay	1735	–	ns	
RC	Read Cycle = $t_{AW} + t_{DID} + t_{DIW} + t_{RC}$	2000	–	ns	
t_{DD}	$\overline{DISTR}$/DISTR to Driver Disable Delay	–	150	ns	-@ 100 pF loading
t_{DDD}	Delay from $\overline{DISTR}$/DISTR to Data	–	250	ns	-@ 100 pF loading
t_{HZ}	$\overline{DISTR}$/DISTR to Floating Data Delay	100	–	ns	-@ 100 pF loading
t_{DOD}	$\overline{DOSTR}$/DOSTR Strobe Delay	50	–	ns	
t_{DOW}	$\overline{DOSTR}$/DOSTR Strobe Width	175	–	ns	
t_{WC}	Write Cycle Delay	1785	–	ns	
WC	Write Cycle – $t_{AW} + t_{DOD} + t_{DOW} + t_{WC}$	2100	–	ns	
t_{DS}	Data Setup Time	175	–	ns	
t_{DH}	Data Hold Time	60	–	ns	
t_{CSC}*	Chip Select Output Delay from Select	–	200	ns	-@ 100 pF loading
t_{RA}*	Address Hold Time from $\overline{DISTR}$/DISTR	50	–	ns	
t_{RCS}*	Chip Select Hold Time from $\overline{DISTR}$/DISTR	50	–	ns	
t_{AR}*	$\overline{DISTR}$/DISTR Delay from Address	110	–	ns	
t_{CSR}*	$\overline{DISTR}$/DISTR Delay from Chip Select	110	–	ns	
t_{WA}*	Address Hold Time from $\overline{DOSTR}$/DOSTR	50	–	ns	
t_{WCS}*	Chip Select Hold Time from $\overline{DOSTR}$/DOSTR	50	–	ns	
t_{AW}*	$\overline{DOSTR}$/DOSTR Delay from Address	160	–	ns	
t_{CSW}*	$\overline{DOSTR}$/DOSTR Delay from Select	160	–	ns	
t_{MRW}	Master Reset Pulse Width	25	–	μs	

*Applicable only when $\overline{ADS}$ input is tied permanently low.

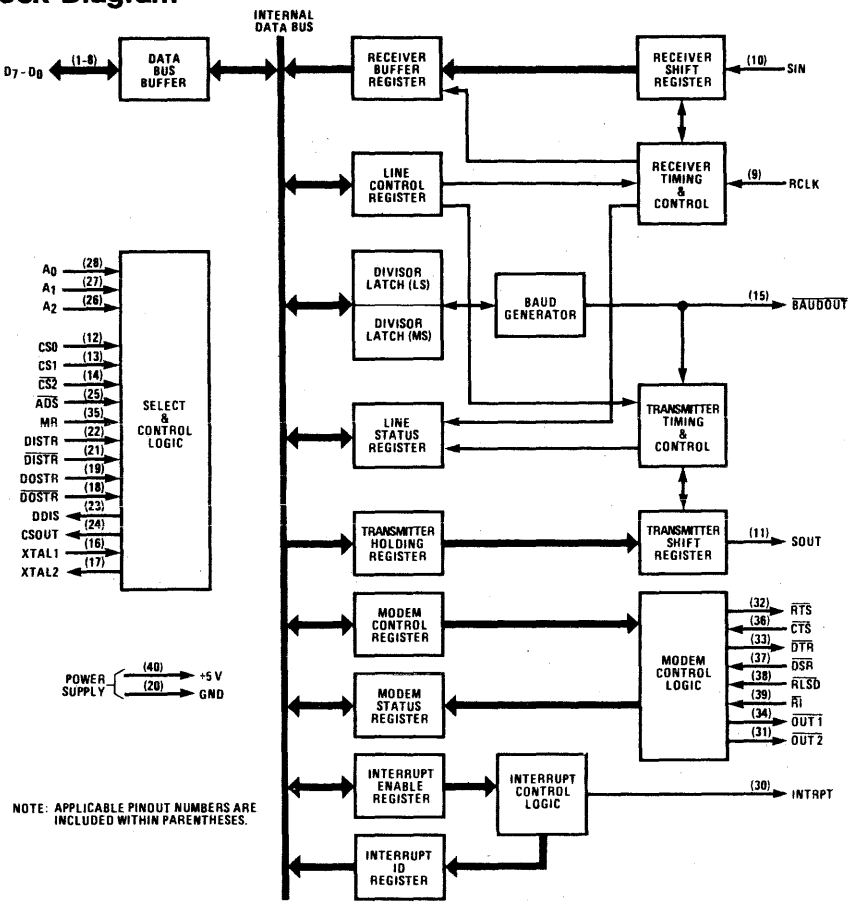
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AC Electrical Characteristics (cont'd.)

Symbol	Parameter	Min	Max	Units	Test Conditions
BAUD GENERATOR					
N	Baud Rate Divisor	1	$2^{16}-1$		
t_{BLD}	Baud Output Negative Edge Delay		250 typ	ns	100 pF Load
t_{BHD}	Baud Output Positive Edge Delay		250 typ	ns	100 pF Load
t_{LW}	Baud Output Down Time	425 typ		ns	100 pF Load
t_{HW}	Baud Output Up Time	330 typ		ns	100 pF Load
RECEIVER					
t_{SCD}	Delay from RCLK to Sample Time		2 typ	μs	
t_{SINT}	Delay from Stop to Set Interrupt		2 typ	μs	100 pF Load
t_{RINT}	Delay from $\overline{\text{DISTR}}$/DISTR (RD RBR/RDLSR) to Reset Interrupt		1 typ	μs	100 pF Load
TRANSMITTER					
t_{HR}	Delay from $\overline{\text{DOSTR}}$/DOSTR (WR THR) to Reset Interrupt		1 typ	μs	100 pF Load
t_{IRS}	Delay from Initial INTR Reset to Transmit Start		16 typ	$\overline{\text{BAUDOUT}}$ Cycles	
t_{SI}	Delay from Initial Write to Interrupt		24 typ	$\overline{\text{BAUDOUT}}$ Cycles	
t_{SS}	Delay from Stop to Next Start		1 typ	μs	
t_{STI}	Delay from Stop to Interrupt (THRE)		8 typ	$\overline{\text{BAUDOUT}}$ Cycles	
t_{IR}	Delay from $\overline{\text{DISTR}}$/DISTR (RD IIR) to Reset Interrupt (THRE)		1 typ	μs	100 pF Load
MODEM CONTROL					
t_{MDO}	Delay from DOSTR/$\overline{\text{DOSTR}}$ (WR MCR) to Output		1 typ	μs	100 pF Load
t_{SIM}	Delay to Set Interrupt from MODEM Input		1 typ	μs	100 pF Load
t_{RIM}	Delay to Reset Interrupt from $\overline{\text{DISTR}}$/DISTR (RD MSR)		1 typ	μs	100 pF Load

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INS8250 Block Diagram



INS8250 Functional Pin Description

The following describes the function of all INS8250 input/output pins. Some of these descriptions reference internal circuits.

NOTE

In the following descriptions, a low represents a logic 0 (0 volt nominal) and a high represents a logic 1 (+2.4 volts nominal).

INPUT SIGNALS

Chip Select (CS0, CS1, $\overline{CS2}$), Pins 12 - 14: When CS0 and CS1 are high and $\overline{CS2}$ is low, the chip is selected. Chip selection is complete when the decoded chip select signal is latched with an active (low) Address Strobe ($\overline{ADS}$) input. This enables communication between the INS8250 and the CPU.

Data Input Strobe (DISTR, $\overline{DISTR}$), Pins 22 and 21: When DISTR is high or $\overline{DISTR}$ is low while the chip is selected, allows the CPU to read status information or data from a selected register of the INS8250.

NOTE

Only an active DISTR or $\overline{DISTR}$ input is required to transfer data from the INS8250 during a read operation. Therefore, tie either the DISTR input permanently low or the $\overline{DISTR}$ input permanently high, if not used.

Data Output Strobe (DOSTR, $\overline{DOSTR}$), Pins 19 and 18: When DOSTR is high or $\overline{DOSTR}$ is low while the chip is selected, allows the CPU to write data or control words into a selected register of the INS8250.

NOTE

Only an active DOSTR or $\overline{DOSTR}$ input is required to transfer data to the INS8250 during a write operation. Therefore, tie either the DOSTR input permanently low or the $\overline{DOSTR}$ input permanently high, if not used.

Address Strobe ($\overline{ADS}$), Pin 25: When low, provides latching for the Register Select (A0, A1, A2) and Chip Select (CS0, CS1, $\overline{CS2}$) signals.

NOTE

An active $\overline{ADS}$ input is required when the Register Select (A0, A1, A2) signals are not stable for the duration of a read or write operation. If not required, tie the $\overline{ADS}$ input permanently low.

Register Select (A0, A1, A2), Pins 26 - 28: These three inputs are used during a read or write operation to select an INS8250 register to read from or write into as indicated in the table below. Note that the state of the Divisor Latch Access Bit (DLAB), which is the most significant bit of the Line Control Register, affects the selection of certain INS8250 registers. The DLAB must be set high by the system software to access the Baud Generator Divisor Latches.

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DLAB	A_2	A_1	A_0	Register
0	0	0	0	Receiver Buffer (read), Transmitter Holding Register (write)
0	0	0	1	Interrupt Enable
X	0	1	0	Interrupt Identification (read only)
X	0	1	1	Line Control
X	1	0	0	MODEM Control
X	1	0	1	Line Status
X	1	1	0	MODEM Status
X	1	1	1	None
1	0	0	0	Divisor Latch (least significant byte)
1	0	0	1	Divisor Latch (most significant byte)

Master Reset (MR), Pin 35: When high, clears all the registers (except the Receiver Buffer, Transmitter Holding, and Divisor Latches), and the control logic of the INS8250. Also, the state of various output signals (SOUT, INTRPT, $\overline{OUT\,1}$, $\overline{OUT\,2}$, $\overline{RTS}$, $\overline{DTR}$) are affected by an active MR input. (Refer to table 1.)

Receiver Clock (RCLK), Pin 9: This input is the 16x baud rate clock for the receiver section of the chip.

Serial Input (SIN), Pin 10: Serial data input from the communications link (peripheral device, MODEM, or data set).

Clear to Send ($\overline{CTS}$), Pin 36: The $\overline{CTS}$ signal is a MODEM control function input whose condition can be tested by the CPU by reading bit 4 (CTS) of the MODEM Status Register. Bit 0 (DCTS) of the MODEM Status Register indicates whether the $\overline{CTS}$ input has changed state since the previous reading of the MODEM Status Register.

NOTE

Whenever the CTS bit of the MODEM Status Register changes state, an interrupt is generated if the MODEM Status Interrupt is enabled.

Data Set Ready ($\overline{DSR}$), Pin 37: When low, indicates that the MODEM or data set is ready to establish the communications link and transfer data with the INS8250. The $\overline{DSR}$ signal is a MODEM-control function input whose condition can be tested by the CPU by reading bit 5 (DSR) of the MODEM Status Register. Bit 1 (DDSR) of the MODEM Status Register indicates whether the $\overline{DSR}$ input has changed state since the previous reading of the MODEM Status Register.

NOTE

Whenever the DSR bit of the MODEM Status Register changes state, an interrupt is generated if the MODEM Status Interrupt is enabled.

Received Line Signal Detect ($\overline{RLSD}$), Pin 38: When low, indicates that the data carrier has been detected by the MODEM or data set. The $\overline{RLSD}$ signal is a MODEM-control function input whose condition can be tested by the CPU by reading bit 7 (RLSD) of the MODEM Status Register. Bit 3 (DRLSD) of the MODEM Status Register indicates whether the $\overline{RLSD}$ input has changed state since the previous reading of the MODEM Status Register.

NOTE

Whenever the RLSD bit of the MODEM Status Register changes state, an interrupt is generated if the MODEM Status Interrupt is enabled.

Ring Indicator ($\overline{RI}$), Pin 39: When low, indicates that a telephone ringing signal has been received by the MODEM or data set. The $\overline{RI}$ signal is a MODEM-control function input whose condition can be tested by the CPU by reading bit 6 (RI) of the MODEM Status Register. Bit 2 (TERI) of the MODEM Status Register indicates whether the $\overline{RI}$ input has changed from a low to a high state since the previous reading of the MODEM Status Register.

NOTE

Whenever the RI bit of the MODEM Status Register changes from a high to a low state, an interrupt is generated if the MODEM Status Interrupt is enabled.

V_{CC}, Pin 40: +5-volt supply.

V_{SS}, Pin 20: Ground (0-volt) reference.

OUTPUT SIGNALS

Data Terminal Ready ($\overline{DTR}$), Pin 33: When low, informs the MODEM or data set that the INS8250 is ready to communicate. The DTR output signal can be set to an active low by programming bit 0 (DTR) of the MODEM Control Register to a high level. The $\overline{DTR}$ signal is set high upon a Master Reset operation.

Request to Send ($\overline{RTS}$), Pin 32: When low, informs the MODEM or data set that the INS8250 is ready to transmit data. The $\overline{RTS}$ output signal can be set to an active low by programming bit 1 (RTS) of the MODEM Control Register. The $\overline{RTS}$ signal is set high upon a Master Reset operation.

Output 1 ($\overline{OUT\,1}$), Pin 34: User-designated output that can be set to an active low by programming bit 2 ($\overline{OUT\,1}$) of the MODEM Control Register to a high level. The $\overline{OUT\,1}$ signal is set high upon a Master Reset operation.

Output 2 ($\overline{OUT\,2}$), Pin 31: User-designated output that can be set to an active low by programming bit 3 ($\overline{OUT\,2}$) of the MODEM Control Register to a high level. The $\overline{OUT\,2}$ signal is set high upon a Master Reset operation.

Chip Select Out (CSOUT), Pin 24: When high, indicates that the chip has been selected by active CS0, CS1, and $\overline{CS2}$ inputs. No data transfer can be initiated until the CSOUT signal is a logic 1.

Driver Disable (DDIS), Pin 23: Goes low whenever the CPU is reading data from the INS8250. A high-level DDIS output can be used to disable an external transceiver (if used between the CPU and INS8250 on the $D_7 - D_0$ Data Bus) at all times, except when the CPU is reading data.

Baud Out ($\overline{BAUDOUT}$), Pin 15: 16x clock signal for the transmitter section of the INS8250. The clock rate is equal to the main reference oscillator frequency divided by the specified divisor in the Baud Generator Divisor Latches. The $\overline{BAUDOUT}$ may also be used for the receiver section by tying this output to the RCLK input of the chip.

Interrupt (INTRPT), Pin 30: Goes high whenever any one of the following interrupt types has an active high condition and is enabled via the IER: Receiver Error Flag; Received Data Available; Transmitter Holding Register Empty; and MODEM Status. The INTRPT signal is reset low upon the appropriate interrupt service or a Master Reset operation.

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Serial Output (SOUT), Pin 11: Composite serial data output to the communications link (peripheral, MODEM or data set). The SOUT signal is set to the Marking (logic 1) state upon a Master Reset operation.

INPUT/OUTPUT SIGNALS

Data (D_7 - D_0) Bus, Pins 1 - 8: This bus comprises eight TRI-STATE input/output lines. The bus provides bidirectional communications between the INS8250 and the CPU. Data, control words, and status information are transferred via the D_7 - D_0 Data Bus.

External Clock Input/Output (XTAL 1, XTAL 2), Pins 16 and 17: These two pins connect the main timing reference (crystal or signal clock) to the INS8250.

Pin Configuration

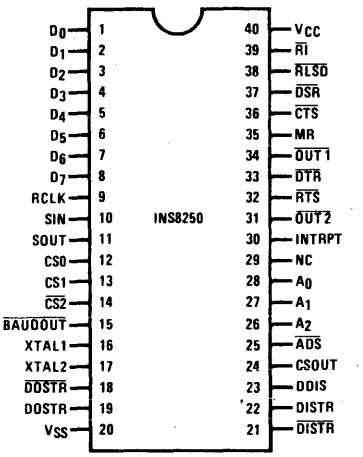


Table 1. ACE Reset Functions

Register/Signal	Reset Control	Reset State
Interrupt Enable Register	Master Reset	All Bits Low (0 - 3 forced and 4 - 7 permanent)
Interrupt Identification Register	Master Reset	Bit 0 is High, Bits 1 and 2 Low Bits 3 - 7 are Permanently Low
Line Control Register	Master Reset	All Bits Low
MODEM Control Register	Master Reset	All Bits Low
Line Status Register	Master Reset	All Bits Low, Except Bits 5 & 6 are High
MODEM Status Register	Master Reset	Bits 0 - 3 Low Bits 4 - 7 — Input Signal
SOUT	Master Reset	High
INTRPT (RCVR Errs)	Read LSR/MR	Low
INTRPT (RCVR Data Ready)	Read RBR/MR	Low
INTRPT (THRE)	Read IIR/Write THR/MR	Low
INTRPT (Modem Status Changes)	Read MSR/MR	Low
$\overline{\text{OUT 2}}$	Master Reset	High
$\overline{\text{RTS}}$	Master Reset	High
$\overline{\text{DTR}}$	Master Reset	High
$\overline{\text{OUT 1}}$	Master Reset	High

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INS8250 Accessible Registers

The system programmer may access or control any of the INS8250 registers summarized in table 2 via the CPU. These registers are used to control INS8250 operations and to transmit and receive data.

INS8250 LINE CONTROL REGISTER

The system programmer specifies the format of the asynchronous data communications exchange via the Line Control Register. In addition to controlling the format, the programmer may retrieve the contents of the Line Control Register for inspection. This feature simplifies system programming and eliminates the need for separate storage in system memory of the line characteristics. The contents of the Line Control Register are indicated in table 2 and are described below.

Bits 0 and 1: These two bits specify the number of bits in each transmitted or received serial character. The encoding of bits 0 and 1 is as follows:

Bit 1	Bit 0	Word Length
0	0	5 Bits
0	1	6 Bits
1	0	7 Bits
1	1	8 Bits

Bit 2: This bit specifies the number of Stop bits in each transmitted or received serial character. If bit 2 is a logic 0, 1 Stop bit is generated or checked in the transmit or receive data, respectively. If bit 2 is a logic 1 when a 5-bit word length is selected via bits 0 and 1, 1½ Stop bits are generated or checked. If bit 2 is a logic 1 when either a 6-, 7-, or 8-bit word length is selected, 2 Stop bits are generated or checked.

Table 2. Summary of INS8250 Accessible Registers

	Register Address									
	0 DLAB = 0	0 DLAB = 0	1 DLAB = 0	2	3	4	5	6	0 DLAB = 1	1 DLAB = 1
Bit No.	Receiver Buffer Register (Read Only)	Transmitter Holding Register (Write Only)	Interrupt Enable Register	Interrupt Identification Register (Read Only)	Line Control Register	MODEM Control Register	Line Status Register	MODEM Status Register	Divisor Latch (LS)	Divisor Latch (MS)
	RBR	THR	IER	IIR	LCR	MCR	LSR	MSR	DLL	DLM
0	Data Bit 0*	Data Bit 0	Enable Received Data Available Interrupt (ERBFI)	"0" if Interrupt Pending	Word Length Select Bit 0 (WLS0)	Data Terminal Ready (DTR)	Data Ready (DR)	Delta Clear to Send (DCTS)	Bit 0	Bit 8
1	Data Bit 1	Data Bit 1	Enable Transmitter Holding Register Empty Interrupt (ETBEI)	Interrupt ID Bit (0)	Word Length Select Bit 1 (WLS1)	Request to Send (RTS)	Overrun Error (OR)	Delta Data Set Ready (DDSR)	Bit 1	Bit 9
2	Data Bit 2	Data Bit 2	Enable Receiver Line Status Interrupt (ELSI)	Interrupt ID Bit (1)	Number of Stop Bits (STB)	Out 1	Parity Error (PE)	Trailing Edge Ring Indicator (TERI)	Bit 2	Bit 10
3	Data Bit 3	Data Bit 3	Enable MODEM Status Interrupt (EDSSI)	0	Parity Enable (PEN)	Out 2	Framing Error (FE)	Delta Receive Line Signal Detect (DRLSD)	Bit 3	Bit 11
4	Data Bit 4	Data Bit 4	0	0	Even Parity Select (EPS)	Loop	Break Interrupt (BI)	Clear to Send (CTS)	Bit 4	Bit 12
5	Data Bit 5	Data Bit 5	0	0	Stick Parity	0	Transmitter Holding Register Empty (THRE)	Data Set Ready (DSR)	Bit 5	Bit 13
6	Data Bit 6	Data Bit 6	0	0	Set Break	0	Transmitter Shift Register Empty (TSRE)	Ring Indicator (RI)	Bit 6	Bit 14
7	Data Bit 7	Data Bit 7	0	0	Divisor Latch Access Bit (DLAB)	0	0	Received Line Signal Detect (RLSD)	Bit 7	Bit 15

* Bit 0 is the least significant bit. It is the first bit serially transmitted or received.

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Bit 3: This bit is the Parity Enable bit. When bit 3 is a logic 1, a Parity bit is generated (transmit data) or checked (receive data) between the last data word bit and Stop bit of the serial data. (The Parity bit is used to produce an even or odd number of 1s when the data word bits and the Parity bit are summed.)

Bit 4: This bit is the Even Parity Select bit. When bit 3 is a logic 1 and bit 4 is a logic 0, an odd number of logic 1s is transmitted or checked in the data word bits and Parity bit. When bit 3 is a logic 1 and bit 4 is a logic 1, an even number of bits is transmitted or checked.

Bit 5: This bit is the Stick Parity bit. When bit 3 is a logic 1 and bit 5 is a logic 1, the Parity bit is transmitted and then detected by the receiver as a logic 0 if bit 4 is a logic 1 or as a logic 1 if bit 4 is a logic 0.

Bit 6: This bit is the Set Break Control bit. When bit 6 is a logic 1, the serial output (SOUT) is forced to the Spacing (logic 0) state and remains there regardless of other transmitter activity. The set break is disabled by setting bit 6 to a logic 0. This feature enables the CPU to alert a terminal in a computer communications system.

Bit 7: This bit is the Divisor Latch Access Bit (DLAB). It must be set high (logic 1) to access the Divisor Latches of the Baud Rate Generator during a Read or Write operation. It must be set low (logic 0) to access the Receiver Buffer, the Transmitter Holding Register, or the Interrupt Enable Register.

INS8250 PROGRAMMABLE BAUD RATE GENERATOR

The INS8250 contains a programmable Baud Rate Generator that is capable of taking any clock input (DC to 3.1 MHz) and dividing it by any divisor from 1 to $(2^{16}-1)$. The output frequency of the Baud Generator is 16x the Baud rate [divisor # = (frequency input) ÷ (baud rate x 16)]. Two 8-bit latches store the divisor in a 16-bit binary format. These Divisor Latches must be loaded during initialization in order to insure desired operation of the Baud Rate Generator. Upon loading either of the Divisor Latches, a 16-bit Baud counter is immediately loaded. This prevents long counts on initial load.

Tables 3 and 4 illustrate the use of the Baud Rate Generator with crystal frequencies of 1.8432 MHz and 3.072 MHz respectively. For baud rates of 38400 and below the error obtained is minimal. The accuracy of the desired baud rate is dependent on the crystal frequency chosen.

NOTE

The maximum operating frequency of the Baud Generator is 3.1 MHz. However, when using divisors of 3 and below, the maximum frequency is equal to the divisor in MHz. For example, if the divisor is 1, then the maximum frequency is 1 MHz. In no case should the data rate be greater than 56k Baud.

LINE STATUS REGISTER

This 8-bit register provides status information to the CPU concerning the data transfer. The contents of the Line Status Register are indicated in table 2 and are described below.

Bit 0: This bit is the receiver Data Ready (DR) indicator. Bit 0 is set to a logic 1 whenever a complete incoming character has been received and transferred into the Receiver Buffer Register. Bit 0 may be reset to a logic 0 either by the CPU reading the data in the Receiver Buffer Register or by writing a logic 0 into it from the CPU.

Bit 1: This bit is the Overrun Error (OE) indicator. Bit 1 indicates that data in the Receiver Buffer Register was not read by the CPU before the next character was transferred into the Receiver Buffer Register, thereby destroying the previous character. The OE indicator is reset whenever the CPU reads the contents of the Line Status Register.

Bit 2: This bit is the Parity Error (PE) indicator. Bit 2 indicates that the received data character does not have the correct even or odd parity, as selected by the even-parity-select bit. The PE bit is set to a logic 1 upon detection of a parity error and is reset to a logic 0 whenever the CPU reads the contents of the Line Status Register.

Table 3. Baud Rates Using 1.8432 MHz Crystal

Desired Baud Rate	Divisor Used to Generate 16x Clock	Percent Error Difference Between Desired & Actual
50	2304	–
75	1536	–
110	1047	0.026
134.5	857	0.058
150	768	–
300	384	–
600	192	–
1200	96	–
1800	64	–
2000	58	0.69
2400	48	–
3600	32	–
4800	24	–
7200	16	–
9600	12	–
19200	6	–
38400	3	–
56000	2	2.86

NOTE: 1.8432 MHz is the standard 8080 frequency divided by 10.

Table 4. Baud Rates Using 3.072 MHz Crystal

Desired Baud Rate	Divisor Used to Generate 16x Clock	Percent Error Difference Between Desired & Actual
50	3840	–
75	2560	–
110	1745	0.026
134.5	1428	0.034
150	1280	–
300	640	–
600	320	–
1200	160	–
1800	107	0.312
2000	96	–
2400	80	–
3600	53	0.628
4800	40	–
7200	27	1.23
9600	20	–
19200	10	–
38400	5	–

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Bit 3: This bit is the Framing Error (FE) indicator. Bit 3 indicates that the received character did not have a valid Stop bit. Bit 3 is set to a logic 1 whenever the Stop bit following the last data bit or parity bit is detected as a zero bit (Spacing level).

Bit 4: This bit is the Break Interrupt (BI) indicator. Bit 4 is set to a logic 1 whenever the received data input is held in the Spacing (logic 0) state for longer than a full word transmission time (that is, the total time of Start bit + data bits + Parity + Stop bits).

NOTE

Bits 1 through 4 are the error conditions that produce a Receiver Line Status interrupt whenever any of the corresponding conditions are detected.

Bit 5: This bit is the Transmitter Holding Register Empty (THRE) indicator. Bit 5 indicates that the INS8250 is ready to accept a new character for transmission. In addition, this bit causes the INS8250 to issue an interrupt to the CPU when the Transmit Holding Register Empty Interrupt enable is set high. The THRE bit is set to a logic 1 when a character is transferred from the Transmitter Holding Register into the Transmitter Shift Register. The bit is reset to logic 0 concurrently with the loading of the Transmitter Holding Register by the CPU.

Bit 6: This bit is the Transmitter Shift Register Empty (TSRE) indicator. Bit 6 is set to a logic 1 whenever the Transmitter Shift Register is idle. It is reset to logic 0 upon a data transfer from the Transmitter Holding Register to the Transmitter Shift Register. Bit 6 is a read-only bit.

Bit 7: This bit is permanently set to logic 0.

INTERRUPT IDENTIFICATION REGISTER

The INS8250 has an on-chip interrupt capability that allows for complete flexibility in interfacing to all the popular microprocessors presently available. In order to provide minimum software overhead during data character transfers, the INS8250 prioritizes interrupts into four levels. The four levels of interrupt conditions are as follows: Receiver Line Status (priority 1); Received Data Ready (priority 2); Transmitter Holding Register Empty (priority 3); and MODEM Status (priority 4).

Information indicating that a prioritized interrupt is pending and the type of that interrupt are stored in the Interrupt Identification Register (refer to table 5). The Interrupt Identification Register (IIR), when addressed during chip-select time, freezes the highest priority interrupt pending and no other interrupts are acknowledged until the particular interrupt is serviced by the CPU. The contents of the IIR are indicated in table 2 and are described below.

Bit 0: This bit can be used in either a hardwired prioritized or polled environment to indicate whether an interrupt is pending. When bit 0 is a logic 0, an interrupt is pending and the IIR contents may be used as a pointer to the appropriate interrupt service routine. When bit 0 is a logic 1, no interrupt is pending and polling (if used) continues.

Bits 1 and 2: These two bits of the IIR are used to identify the highest priority interrupt pending as indicated in table 5.

Bits 3 through 7: These five bits of the IIR are always logic 0.

Table 5. Interrupt Control Functions

Interrupt Identification Register			Interrupt Set and Reset Functions			
Bit 2	Bit 1	Bit 0	Priority Level	Interrupt Type	Interrupt Source	Interrupt Reset Control
0	0	1	—	None	None	—
1	1	0	Highest	Receiver Line Status	Overrun Error or Parity Error or Framing Error or Break Interrupt	Reading the Line Status Register
1	0	0	Second	Received Data Available	Receiver Data Available	Reading the Receiver Buffer Register
0	1	0	Third	Transmitter Holding Register Empty	Transmitter Holding Register Empty	Reading the IIR Register (if source of interrupt) or Writing into the Transmitter Holding Register
0	0	0	Fourth	MODEM Status	Clear to Send or Data Set Ready or Ring Indicator or Received Line Signal Detect	Reading the MODEM Status Register

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INTERRUPT ENABLE REGISTER

This 8-bit register enables the four types of interrupts of the INS8250 to separately active the chip Interrupt (INTRPT) output signal. It is possible to totally disable the interrupt system by resetting bits 0 through 3 of the Interrupt Enable Register. Similarly, by setting the appropriate bits of this register to a logic 1, selected interrupts can be enabled. Disabling the interrupt system inhibits the Interrupt Identification Register and the active (high) INTRPT output from the chip. All other system functions operate in their normal manner, including the setting of the Line Status and MODEM Status Registers. The contents of the Interrupt Enable Register are indicated in table 2 and are described below.

Bit 0: This bit enables the Received Data Available Interrupt when set to logic 1.

Bit 1: This bit enables the Transmitter Holding Register Empty Interrupt when set to logic 1.

Bit 2: This bit enables the Receiver Line Status Interrupt when set to logic 1.

Bit 3: This bit enables the MODEM Status Interrupt when set to logic 1.

Bits 4 through 7: These four bits are always logic 0.

MODEM CONTROL REGISTER

This 8-bit register controls the interface with the MODEM or data set (or a peripheral device emulating a MODEM). The contents of the MODEM Control Register are indicated in table 2 and are described below.

Bit 0: This bit controls the Data Terminal Ready ($\overline{DTR}$) output. When bit 0 is set to a logic 1, the $\overline{DTR}$ output is forced to a logic 0. When bit 0 is reset to a logic 0, the $\overline{DTR}$ output is forced to a logic 1.

NOTE

The $\overline{DTR}$ output of the INS8250 may be applied to an EIA inverting line driver (such as the DS1488) to obtain the proper polarity input at the succeeding MODEM or data set.

Bit 1: This bit controls the Request to Send ($\overline{RTS}$) output. Bit 1 affects the $\overline{RTS}$ output in a manner identical to that described above for bit 0.

Bit 2: This bit controls the Output 1 ($\overline{OUT\ 1}$) signal, which is an auxiliary user-designated output. Bit 2 affects the $\overline{OUT\ 1}$ output in a manner identical to that described above for bit 0.

Bit 3: This bit controls the Output 2 ($\overline{OUT\ 2}$) signal, which is an auxiliary user-designated output. Bit 3 affects the $\overline{OUT\ 2}$ output in a manner identical to that described above for bit 0.

Bit 4: This bit provides a loopback feature for diagnostic testing of the INS8250. When bit 4 is set to logic 1, the following occur: the transmitter Serial Output (SOUT) is set to the Marking (logic 1) state; the receiver Serial Input (SIN) is disconnected; the output of the Transmitter Shift Register is "looped back" into the Receiver Shift Register input; the four MODEM Control inputs ($\overline{CTS}$, $\overline{DSR}$, $\overline{RLSD}$, and $\overline{RI}$) are disconnected; and the four MODEM Control outputs ($\overline{DTR}$, $\overline{RTS}$, $\overline{OUT\ 1}$, and $\overline{OUT\ 2}$) are internally connected to the four MODEM Control inputs. In the diagnostic mode, data that is transmitted is immediately received. This feature allows the processor to verify the transmit- and receive-data paths of the INS8250.

In the diagnostic mode, the receiver and transmitter interrupts are fully operational. The MODEM Control Interrupts are also operational but the interrupts' sources are now the lower four bits of the MODEM Control Register instead of the four MODEM Control inputs. The interrupts are still controlled by the Interrupt Enable Register.

The INS8250 interrupt system can be tested by writing into the lower six bits of the Line Status Register and the lower four bits of the MODEM Status Register. Setting any of these bits to a logic 1 generates the appropriate interrupt (if enabled). The resetting of these interrupts is the same as in normal INS8250 operation. To return to normal operation, the registers must be reprogrammed for normal operation and then bit 4 of the MODEM Control Register must be reset to logic 0.

Bits 5 through 7: These bits are permanently set to logic 0.

MODEM STATUS REGISTER

This 8-bit register provides the current state of the control lines from the MODEM (or peripheral device) to the CPU. In addition to this current-state information, four bits of the MODEM Status Register provide change information. These bits are set to a logic 1 whenever a control input from the MODEM changes state. They are reset to logic 0 whenever the CPU reads the MODEM Status Register.

The contents of the MODEM Status Register are indicated in table 2 and are described below.

Bit 0: This bit is the Delta Clear to Send (DCTS) indicator. Bit 0 indicates that the $\overline{CTS}$ input to the chip has changed state since the last time it was read by the CPU.

Bit 1: This bit is the Delta Data Set Ready (DDSR) indicator. Bit 1 indicates that the $\overline{DSR}$ input to the chip has changed state since the last time it was read by the CPU.

Bit 2: This bit is the Trailing Edge of Ring Indicator (TERI) detector. Bit 2 indicates that the $\overline{RI}$ input to the chip has changed from an On (logic 1) to an Off (logic 0) condition.

Bit 3: This bit is the Delta Received Line Signal Detector (DRLSD) indicator. Bit 3 indicates that the $\overline{RLSD}$ input to the chip has changed state.

NOTE

Whenever bit 0, 1, 2, or 3 is set to logic 1, a MODEM Status interrupt is generated.

Bit 4: This bit is the complement of the Clear to Send ($\overline{CTS}$) input. If bit 4 (loop) of the MCR is set to a 1, this bit is equivalent to RTS in the MCR.

Bit 5: This bit is the complement of the Data Set Ready ($\overline{DSR}$) input. If bit 4 of the MCR is set to a 1, this bit is equivalent to DTR in the MCR.

Bit 6: This bit is the complement of the Ring Indicator ($\overline{RI}$) input. If bit 4 of the MCR is set to a 1, this bit is equivalent to OUT 1 in the MCR.

Bit 7: This bit is the complement of the Received Line Signal Detect ($\overline{RLSD}$) input. If bit 4 of the MCR is set to a 1, this bit is equivalent to OUT 2 of the MCR.

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INS8060 Single-Chip 8-Bit N-Channel Microprocessor (SC/MP Family)

General Description

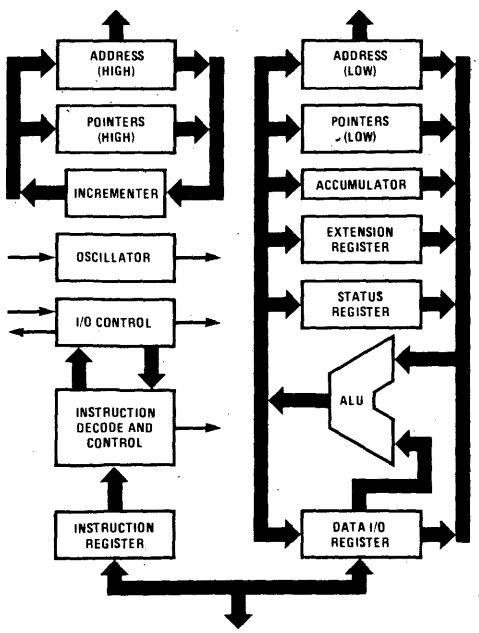
The INS8060 is the N-channel version of National's SC/MP family (an acronym for Simple, Cost-effective MicroProcessor). This family consists of single-chip, 8-bit microprocessors packaged in standard 40-pin dual-in-line packages. N-channel, silicon gate, depletion mode standard-process technology gives the INS8060 high performance, high reliability, and high producibility.

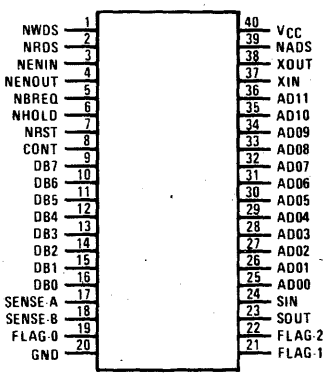
The INS8060 is intended for use in general-purpose applications where cost per function is the most significant criterion. But cost efficiency is only a part of the INS8060's story. It goes on to include a variety of useful functions that are not even provided by some of the expensive microprocessors, like self-contained timing circuitry, 16-bit (65k) addressing capability, serial or parallel data-transfer capability and common memory/peripheral instructions. The built-in features in conjunction with the low initial cost describe what the INS8060 really is — a microprocessor specifically designed to provide the simplest and most efficient solution to many application requirements.

Features

- Simple interfacing
  - Bidirectional TRI-STATE® 8-bit data bus
  - TTL-compatible input/output interface
- Silicon-gate N-channel ion-implant process
- Direct Memory Access (DMA) and multiprocessor capabilities
  - Handshake bus-access control on chip
- Simplified programming
  - Multiple addressing modes — program-counter-relative, immediate data, indexed, auto-indexed, and implied
- Direct control output
  - Three user-accessible control-flag outputs
- Simple I/O hardware
  - Separate serial-data input and output ports
  - Two sense inputs
  - Direct interfacing to standard memory parts
- Simple timing hardware
  - On-chip clock generator
- Interface flexibility
  - Capability to interface with memories or peripherals of any speed
- Large system capability
  - Address capability to 65k bytes of memory
- Simplified power requirements
  - Single 5-volt supply
  - Low power
- Low Cost
  - Plastic package

Block and Connection Diagrams





INS8060 Pin Configuration

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DA-B2M88/Printed in U.S.A.

Functional Description

The INS8060 is a self-contained general-purpose microprocessor designed for ease of implementation in stand-alone, DMA (Direct Memory Access), and multiprocessor applications. Communications between the INS8060 and external memory/peripheral devices are effected via a 12-bit dedicated address bus and an 8-bit bidirectional data bus. During the address interval of each input/output cycle, the INS8060 employs both busses to provide a 16-bit address output: the 12 least significant address bits are sent out over the 12-bit address bus and the 4 most significant address bits (DB3-DB0) are sent out over the 8-bit data bus along with 4 status bits (DB7-DB4). Separate strobe outputs from the INS8060 (NADS, NWDS, NRDS) indicate when valid address information is present on the two busses, and when valid input/output memory or peripheral data are present on the 8-bit bus. To further extend application flexibility serial data input/output ports are also provided so that serial data transfers can be effected under program control. The remaining input/output signals shown in figure 1 are dedicated to general-purpose control and status functions, including initialization, bus management, microprocessor halt, interrupt request, input/output cycle extension, and user-specified hardware/software interface functions. A detailed description of each input/output signal is provided in table 1.

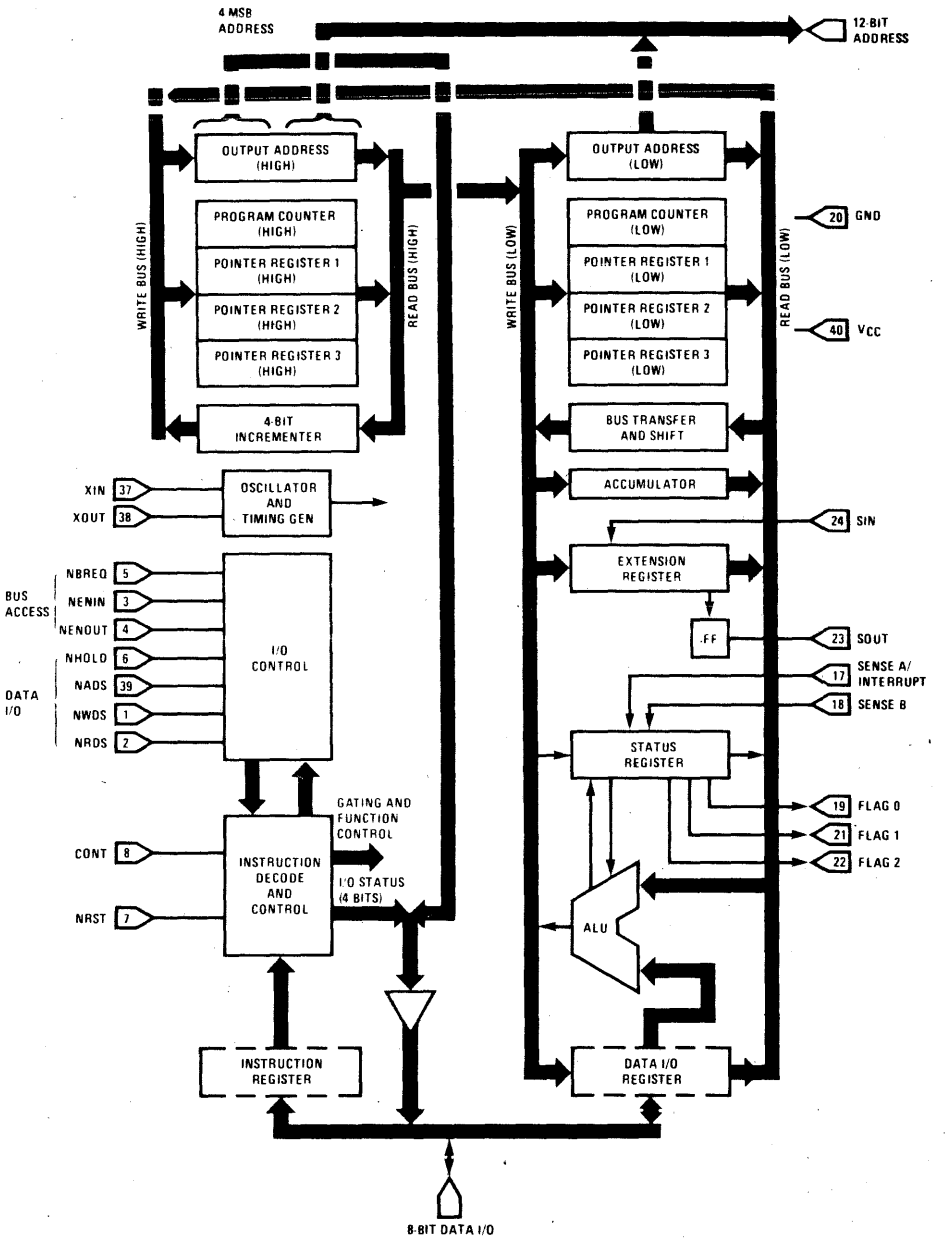


FIGURE 1. INS8060 Detailed Block Diagram

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TABLE 1. Input/Output Signal Description

Signal Mnemonic	Functional Name	Description
NRST	Reset Input	Set high for normal operation. When set low, aborts in-process operations. When returned high, internal control circuit zeroes all programmer-accessible registers; then, first instruction is fetched from memory location 0001_{16}.
CONT	Continue Input	When set high, enables normal execution of program stored in external memory. When set low, the INS8060 operation is suspended (after completion of current instruction) without loss of internal status.
NBREQ	Bus Request Input/Output	Associated with the INS8060 internal allocation logic for system bus. Can be used as bus request output or bus busy input. Requires external load resistor to V_{CC}.
NENIN	Enable Input	Associated with the INS8060 internal allocation logic for system bus. When set low, the INS8060 is granted access to system busses. When set high, places the INS8060's bus pins in high-impedance (TRI-STATE®) mode.
NENOUT	Enable Output	Associated with INS8060 internal allocation logic for system bus. Set low when NENIN is low and the INS8060 is not using system busses (NBREQ-high). Set high at all other times.
NADS	Address Strobe Output	Active-low strobe. While low, indicates that valid address and status output are present on system busses.
NRDS	Read Strobe Output	Active-low strobe. On trailing edge, data are input to the INS8060 from 8-bit bidirectional data bus. High-impedance (TRI-STATE®) output when input/output cycle is not in progress.
NWDS	Write Strobe Output	Active-low strobe. While low, indicates that valid output data are present on 8-bit bidirectional data bus. High-impedance (TRI-STATE®) output when input/output cycle not in progress.
NHOLD	Input/Output Cycle Extend Input	When set low prior to trailing edge of NRDS or NWDS strobe, stretches strobe to extend input/output cycle; that is, strobe is held low until NHOLD signal is returned high.
SENSE A	Sense/Interrupt Request Input	Serves as interrupt request input when the INS8060 internal IE (Interrupt Enable) flag is set. When IE flag is reset, serves as user-designated sense condition input. Sense condition testing is effected by copying status register to accumulator.
SENSE B	Sense Input	User-designated sense-condition input. Sense-condition testing is effected by copying status register to accumulator.
SIN	Serial Input to E Register	Under software control, data on this line are right-shifted into E register by execution of SIO instruction.
SOUT	Serial Output from E Register	Under software control, data are right-shifted onto this line from E register by execution of SIO instruction. Each data bit remains latched until execution of next SIO instruction.
FLAGS 0, 1, 2	Flag Outputs	User-designated general-purpose flag outputs of status register. Under program control, flags can be set and reset by copying accumulator to status register.
AD00-AD11	Address Bit 00 through Address Bit 11	Twelve TRI-STATE® address output lines. The INS8060 outputs 12 least significant address bits on this bus when NADS strobe is low. Address bits are then held valid until trailing edge of read (NRDS) or write (NWDS) strobes. After trailing edge of NRDS or NWDS strobe, bus is set to high-impedance (TRI-STATE®) mode until next NADS strobe.

NOTE:

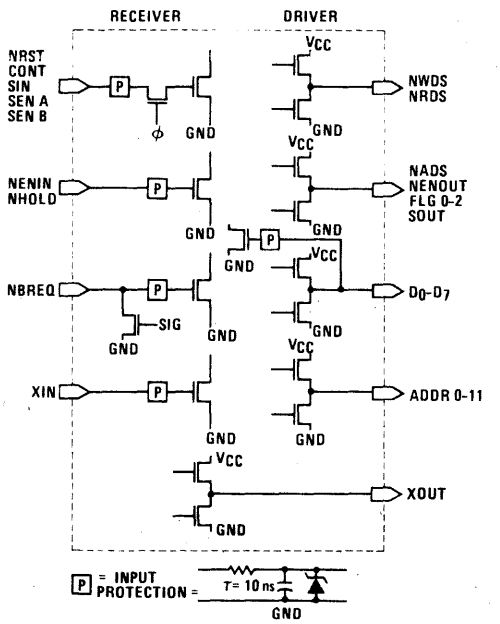
The 8-bit bidirectional data bus is set to the high-impedance (TRI-STATE®) mode except when it is actually in use by the INS8060 (NADS, NRDS, or NWDS low). During the addressing interval of each input/output cycle (NADS low), the INS8060 provides address and status outputs over the bus; during the ensuing data-transfer interval (NRDS or NWDS low), 8-bit input or output data bytes are routed over the bus.

TABLE 1. Input/Output Signal Description (Continued)

Signal Mnemonic/ Pin Designation	Output at NADS Time		Input at NRDS Time	Output at NWDS Time
	Functional Name	Description		
DB0	Address Bit 12	Fourth most significant bit of 16-bit address.	Input data are expected on the eight (DB0-DB7) lines.	Output data are valid on the eight (DB0-DB7) lines.
DB1	Address Bit 13	Third most significant bit of 16-bit address.		
DB2	Address Bit 14	Second most significant bit of 16-bit address.		
DB3	Address Bit 15	Most significant bit of 16-bit address.		
DB4	R-Flag	When high, data input cycle is starting; when low, data output cycle is starting.		
DB5	I-Flag	When high, first byte of instruction is being fetched.		
DB6	D-Flag	When high, indicates delay cycle is starting; that is, second byte of DLY instruction is being fetched.		
DB7	H-Flag	When high, indicates that Halt Instruction has been executed. (In some system configurations, the H-Flag output is latched and, in conjunction with the CONTinue input, provides a programmed halt.)	**Note:** The DB0 through DB7 (AD12-HFLG) lines are a high-impedance (open circuit) load when the INS8060 does not have access to the input/output bus.	

DRIVERS AND RECEIVERS

Equivalent circuits for the INS8060 drivers and receivers are shown below. All inputs have static charge protection circuits consisting of an RC filter and voltage clamp. These devices still should be handled with care, as the protection circuits can be destroyed by excessive static charge.



INS8060 Driver and Receiver Equivalent Circuits

TIMING CONTROL

All necessary timing signals are provided by a three-stage inverter ring oscillator contained on the INS8060 chip. Two control pins, XIN and XOUT, permit the frequency of the oscillator to be controlled by any of the following methods:

1. Leave the XOUT pin unterminated and drive the XIN pin with an externally generated TTL clock that conforms to the parameters shown in figure 2A. For this method, the frequency of the oscillator is equal to the frequency of the external clock input.
2. Connect a resistor-capacitor feedback network between the XIN and XOUT pins and GND as shown in figure 2B.
3. Connect a crystal with low-pass filter network between the XIN and XOUT pins and GND as shown in figure 2C (for above 1 megahertz) or figure 2D (for 1 megahertz or below). For this method, the frequency of the oscillator is equal to the resonant frequency of the crystal and the low-pass filter prevents unwanted harmonic oscillations.

In addition to illustrating appropriate frequency-control networks for the on-chip oscillator, figures 2A through 2D also show how an optional driver may be used to derive a system clock from the oscillator signal present at the XOUT pin.

In the discussions that follow, instruction execution and input/output timing are described in terms of microcycles.

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The time interval of a microcycle is four times the period of the oscillator; that is:

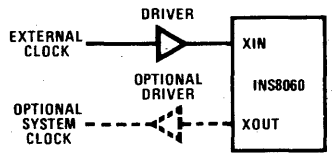
period of one microcycle = $2T_C$

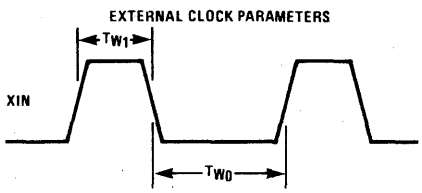
$$T_C = 2\left(\frac{1}{f_{osc}}\right) = 2\left(\frac{1}{f_{res}}\right) = 2\left(\frac{1}{f_{XIN}}\right)$$

where:

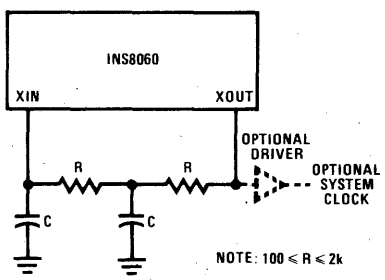
T_C = time period for two cycles of on-chip or external oscillator
f_{osc} = frequency on on-chip oscillator
f_{res} = resonant frequency of crystal connected between XIN and XOUT pins
f_{XIN} = frequency of external clock applied to XIN pin

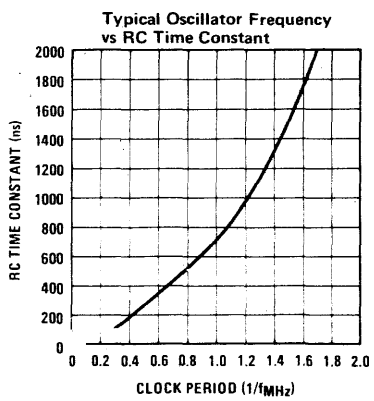
A. External Clock Input



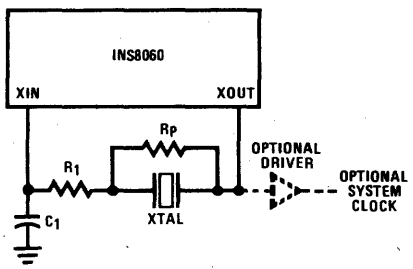


B. Resistor-Capacitor Feedback Network





C. Crystal with Low-Pass Filter (Above 1MHz)

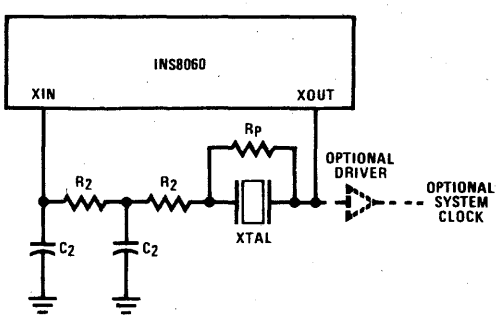


Suggested values for Crystal with Low-Pass Filter Network (Above 1 MHz)

Crystal	Rp	C_1	R_1
2MHz	100kΩ	56pF	1kΩ
3.58MHz	100kΩ	27pF	1kΩ
4MHz	100kΩ	27pF	1kΩ

XTAL is parallel resonant with maximum series resonance equal to 1kΩ.

D. Crystal with Low-Pass Filter (1MHz or Below)



Suggested values for Crystal with Low-Pass Filter Network (1 MHz or Below)

Crystal	Rp	C_2	R_2
100 kHz	1 MΩ	1000 pF	2 kΩ
200 kHz	1 MΩ	1000 pF	1 kΩ
500 kHz	1 MΩ	1000 pF	1 kΩ
700 kHz	1 MΩ	500 pF	2 kΩ
1 MHz	1 MΩ	120 pF	1 kΩ

FIGURE 2. Frequency Control Networks for On-Chip Oscillator

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ADVANCE INFORMATION
SEPTEMBER 1978

COP410L Single-Chip N-Channel Microcontroller

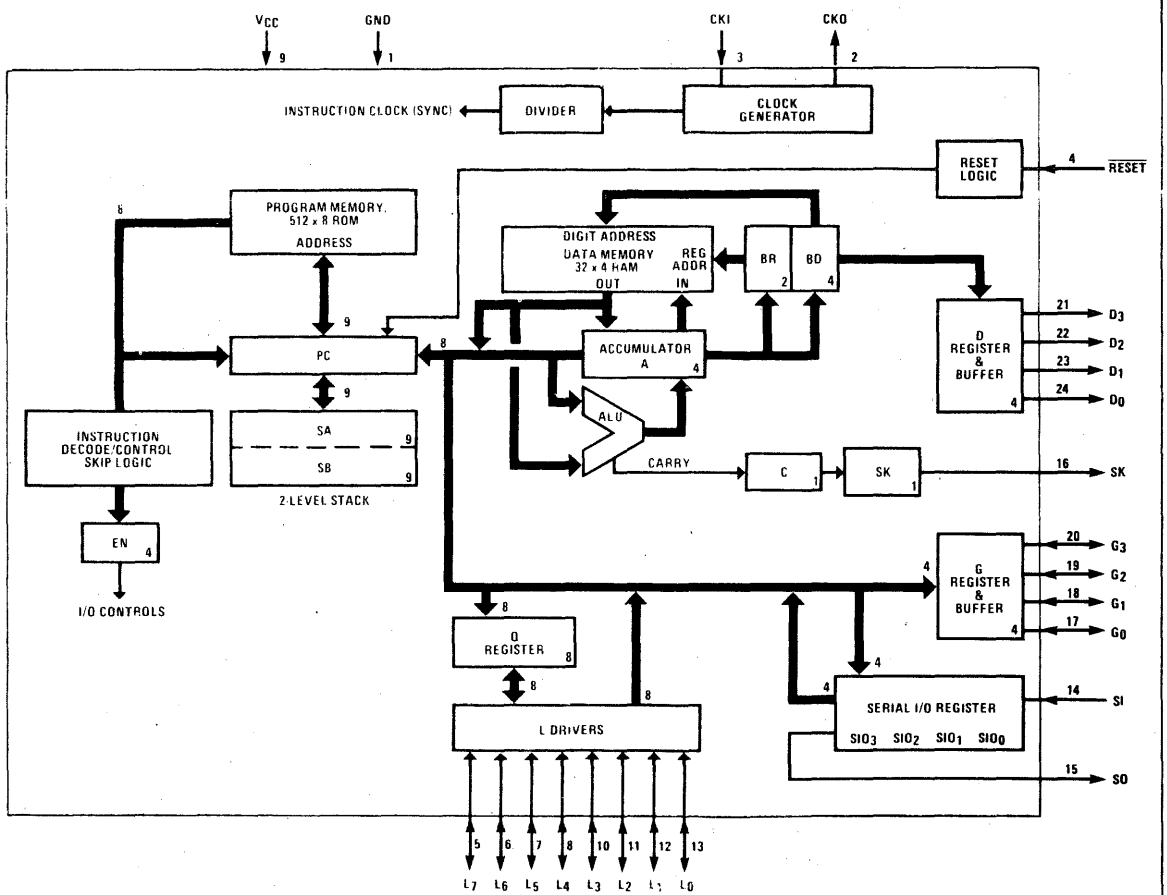
General Description

The COP410L Single-Chip N-Channel Microcontroller is a member of the Control Oriented Processor (COP) family, fabricated using N-channel, silicon gate MOS technology. It is a complete microcomputer containing all system timing, internal logic, ROM, RAM and I/O necessary to implement dedicated control functions in a variety of applications. Features include single supply operation, a variety of output configuration options, with an instruction set, internal architecture and I/O scheme designed to facilitate keyboard input, display output and BCD data manipulation. It is an appropriate choice for use in numerous human interface control environments. Standard test procedures and reliable high-density fabrication techniques provide the medium to large volume customers with a customized Control Oriented processor at a low end-product cost.

Features

- Low cost
- Powerful instruction set
- 512 x 8 ROM, 32 x 4 RAM
- 19 I/O lines
- Two-level subroutine stack
- 16μs instruction time
- Single wide-range supply (4.5 - 9.5V)
- Low current drain (6mA max)
- Internal binary counter register with serial I/O capability
- General purpose and TRI-STATE® outputs
- LSTTL/CMOS compatible in and out
- Direct drive of LED digit and segment lines
- Software/hardware compatible with other members of COP400 family
- Extended temperature range device available (-40°C to +85°C)

COP410L Block Diagram

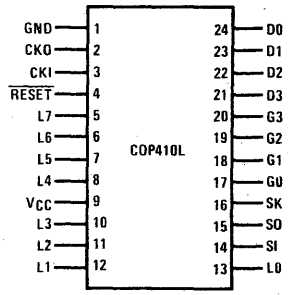


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Connection Diagrams



Functional Characteristics

Oscillator

There are four basic clock oscillator configurations:

a. Ceramic Resonator Controlled Oscillator.

b. External Oscillator.

c. RC Controlled Oscillator.

d. Externally Synchronized Oscillator.

I/O Options

COP outputs have the following optional configurations:

a. **Standard** — an active device to ground in conjunction with a pull-up to V_{CC}, compatible with LSTTL and CMOS input requirements.

b. **Open-Drain** — an active device to ground only, allowing external pull-up as required by the user's application.

c. **Push-Pull** — an active device to ground in conjunction with a pull-up paralleled by an active device to V_{CC}. This configuration has been provided to allow for fast rise and fall times when driving capacitive loads.

d. **LED Direct Segment Drive** — an active device to ground and to V_{CC}, meeting the typical current sourcing requirements of the segments of an LED display.

e. **LED Direct Digit Drive** — a high-current device to ground, meeting the current sinking needs of a small LED digit.

f. **TRI-STATE® Push-Pull** — an active device to ground and V_{CC} intended to meet the requirements associated with connection of these outputs to a data bus shared by other bus drivers.

CKO Pin Options

In a resonator controlled oscillator system, CKO is used as an output to the resonator network. As an option CKO can be a general purpose input. As another option, CKO can be a RAM power supply pin (V_R), allowing its connection to a standby/backup power supply to maintain the integrity of RAM data with minimum power drain (1.5mA maximum at 3.3V).

COP410L Instruction Set

ARITHMETIC INSTRUCTIONS

ASC		Add with Carry, Skip on Carry
ADD		Add A to RAM
AISC	y	Add Immediate, Skip on Carry (y≠0)
CLRA		Clear A
COMP		Ones complement of A to A
NOP		No Operation
RC		Reset C
SC		Set C
XOR		Exclusive-OR A with RAM

TRANSFER OF CONTROL INSTRUCTIONS

JID		Jump Indirect
JMP		Jump
JP		Jump within Page
JSRP		Jump to Subroutine Page
JSR		Jump to Subroutine
RET		Return from Subroutine
RETSK		Return from Subroutine, then Skip

MEMORY REFERENCE INSTRUCTIONS

CQMA		Copy Q to RAM, A
LD	r	Load RAM into A, Exclusive-OR Br with r
LQID		Load Q Indirect
RMB	n	Reset RAM Bit n
SMB	n	Set RAM Bit n
STII	y	Store Memory Immediate and Increment Bd
X	r	Exchange RAM with A, Exclusive-OR Br with r
XAD	r,d	Exchange A with RAM pointed to directly by r,d
XDS	r	Exchange RAM with A and Decrement Bd, Exclusive-OR Br with r
XIS	r	Exchange RAM with A and Increment Bd, Exclusive-OR Br with r

REGISTER REFERENCE INSTRUCTIONS

CAB		Copy A to Bd
CBA		Copy Bd to A
LBI	r,d	Load B Immediate with r,d
LEI	y	Load EN Immediate

TEST INSTRUCTIONS

SKC		Skip is C is True
SKE		Skip if A Equals RAM
SKGZ		Skip if G is Zero (all 4 bits)
SKGBZ	n	Skip if G Bit is Zero
SKMBZ	n	Skip if RAM Bit is Zero

INPUT/OUTPUT INSTRUCTIONS

ING	Input G ports to A
INL	Input L Ports to RAM, A
OBD	Output Bd to D Output
OMG	Output RAM to G Ports
XAS	Exchange A with SIO

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ADVANCE INFORMATION
SEPTEMBER 1978

COP411L Single-Chip N-Channel Microcontroller

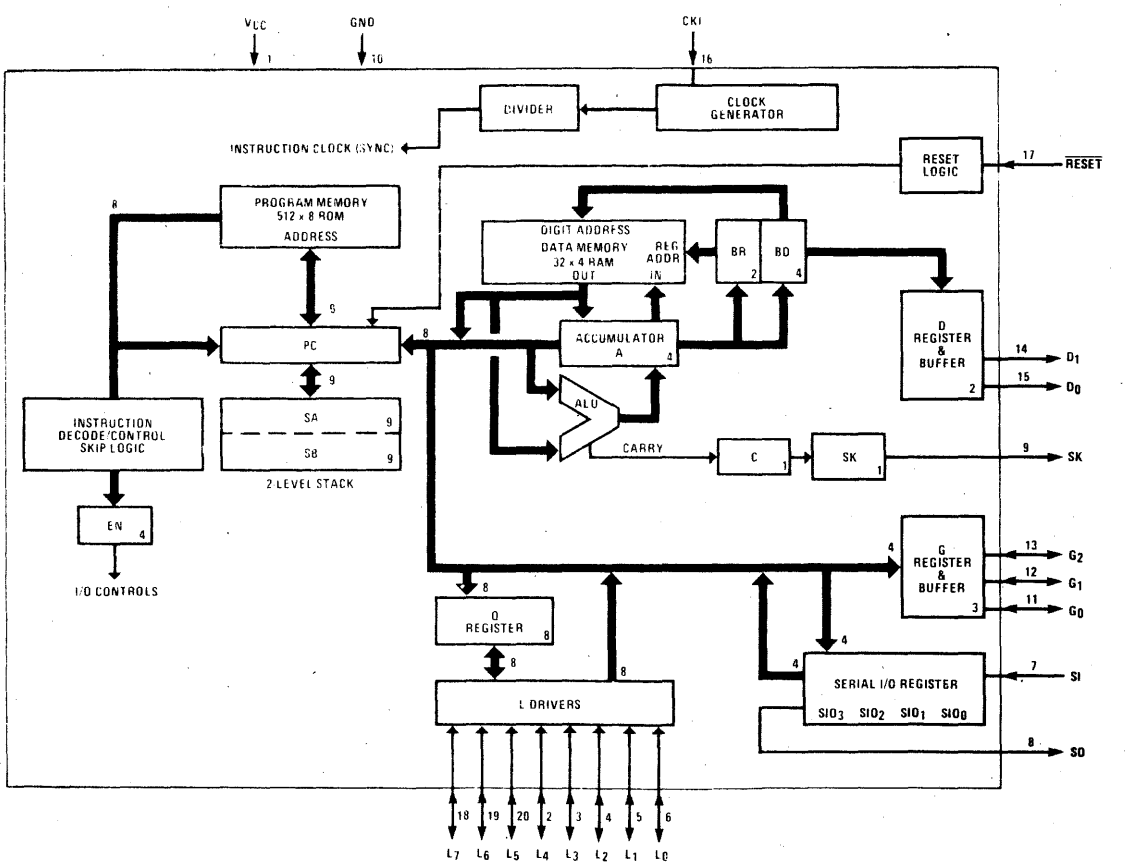
General Description

The COP411L Single-Chip N-Channel Microcontroller is the smallest and lowest-cost member of the Control Oriented Processor (COP) family, fabricated using N-channel, silicon gate MOS technology. It is a complete microcomputer containing all system timing, internal logic ROM, RAM and I/O necessary to implement dedicated control functions in a variety of applications. Features include single supply operation, a variety of output configuration options, with an instruction set, internal architecture and I/O scheme designed to facilitate keyboard input, display output and BCD data manipulation. It is an appropriate choice for use in numerous human interface control environments. Standard test procedures and reliable high-density fabrication techniques provide the medium to large volume customers with a customized Control Oriented processor at a low end-product cost.

Features

- Lowest cost!
- Narrow, 20-pin dual-in-line package
- Powerful instruction set
- 512 x 8 ROM, 32 x 4 RAM
- 16 I/O lines
- Two-level subroutine stack
- 16 μs instruction time
- Single wide-range supply (4.5 - 9.5 V)
- Low current drain (6 mA max)
- Internal binary counter register with serial I/O capability
- General purpose and TRI-STATE* outputs
- LSTTL/CMOS compatible in and out
- LED direct drive outputs
- Software/hardware compatible with other members of COP400 family
- Extended temperature range device available (- 40 °C to + 85 °C)

COP411L Block Diagram

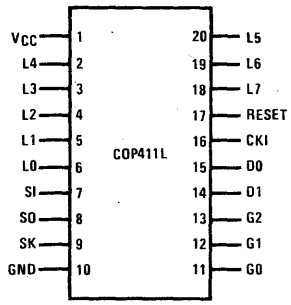


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Connection Diagram



Functional Characteristics

Oscillator

There are two basic clock oscillator configurations:

a. External Oscillator.

b. RC Controlled Oscillator.

I/O Options

COP outputs have the following optional configurations:

a. **Standard** — an active device to ground in conjunction with a pull-up to V_{CC}, compatible with LSTTL and CMOS input requirements.

b. **Open-Drain** — an active device to ground only, allowing external pull-up as required by the user's application.

c. **Push-Pull** — an active device to ground in conjunction with a pull-up paralleled by an active device to V_{CC}. This configuration has been provided to allow for fast rise and fall times when driving capacitive loads.

d. **LED Direct Segment Drive** — an active device to ground and to V_{CC}, meeting the typical current sourcing requirements of the segments of an LED display.

e. **LED Direct Digit Drive** — a high-current device to ground, meeting the current sinking needs of a small LED digit.

f. **TRI-STATE® Push-Pull** — an active device to ground and V_{CC} intended to meet the requirements associated with connection of these outputs to a data bus shared by other bus drivers.

COP411L Instruction Set

ARITHMETIC INSTRUCTIONS

ASC		Add with Carry, Skip on Carry
ADD		Add A to RAM
AISC	y	Add Immediate, Skip on Carry (y≠0)
CLRA		Clear A
COMP		Ones complement of A to A
NOP		No Operation
RC		Reset C
SC		Set C
XOR		Exclusive-OR A with RAM

TRANSFER OF CONTROL INSTRUCTIONS

JID		Jump Indirect
JMP		Jump
JP		Jump within Page
JSRP		Jump to Subroutine Page
JSR		Jump to Subroutine
RET		Return from Subroutine
RETSK		Return from Subroutine, then Skip

MEMORY REFERENCE INSTRUCTIONS

CQMA		Copy Q to RAM, A
LD	r	Load RAM into A, Exclusive-OR Br with r
LQID		Load Q Indirect
RMB	n	Reset RAM Bit n
SMB	n	Set RAM Bit n
STII	y	Store Memory Immediate and Increment Bd
X	r	Exchange RAM with A, Exclusive-OR Br with r
XAD	r,d	Exchange A with RAM pointed to directly by r,d
XDS	r	Exchange RAM with A and Decrement Bd, Exclusive-OR Br with r
XIS	r	Exchange RAM with A and Increment Bd, Exclusive-OR Br with r

REGISTER REFERENCE INSTRUCTIONS

CAB		Copy A to Bd
CBA		Copy Bd to A
LBI	r,d	Load B Immediate with r,d
LEI	y	Load EN Immediate

TEST INSTRUCTIONS

SKC		Skip is C is True
SKE		Skip if A Equals RAM
SKGZ		Skip if G is Zero (all 4 bits)
SKGBZ	n	Skip if G Bit is Zero
SKMBZ	n	Skip if RAM Bit is Zero

INPUT/OUTPUT INSTRUCTIONS

ING		Input G Ports to A
INL		Input L Ports to RAM, A
OBD		Output Bd to D Output
OMG		Output RAM to G Ports
XAS		Exchange A with SIO

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ADVANCE INFORMATION
SEPTEMBER 1978

COP420L/COP421L Single-Chip N-Channel Microcontrollers

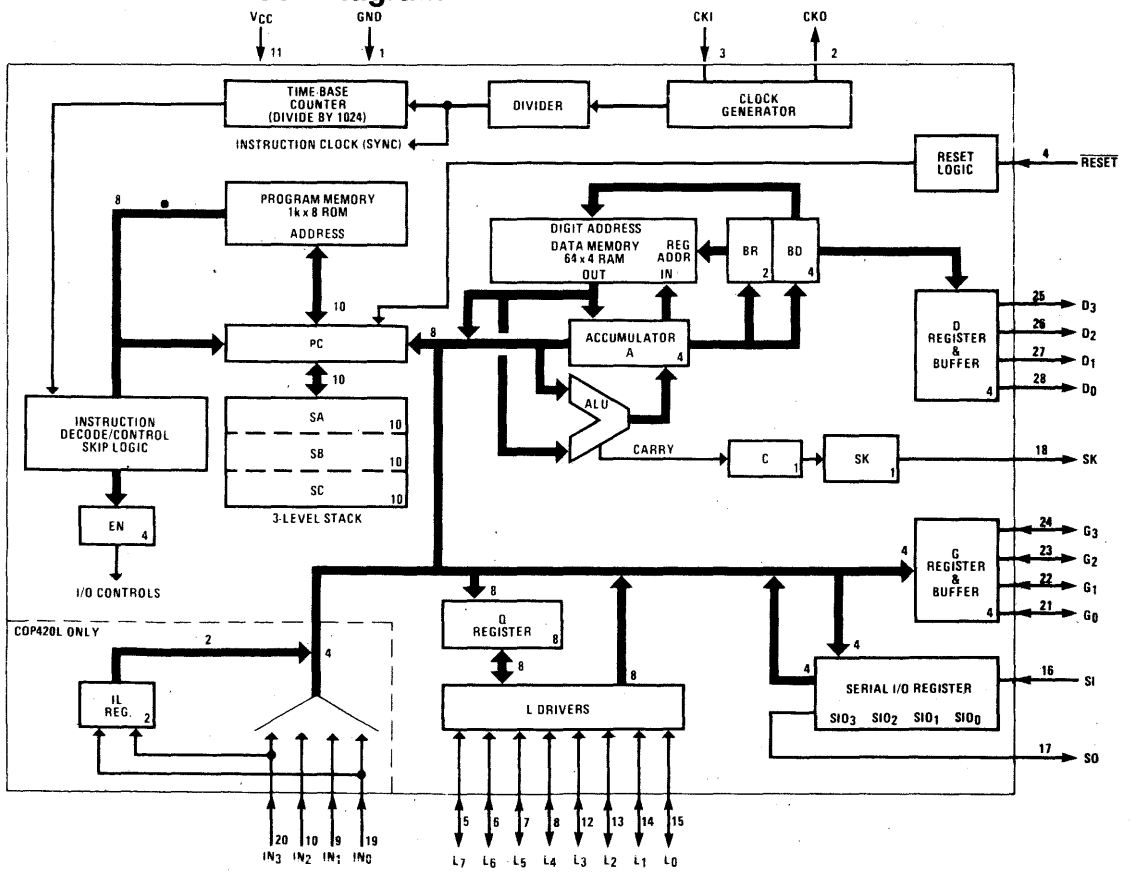
General Description

The COP420L and COP421L Single-Chip N-Channel Microcontrollers are members of the Control Oriented Processor (COP) family, fabricated using N-channel, silicon gate MOS technology. They are complete microcomputers containing all system timing, internal logic, ROM, RAM and I/O necessary to implement dedicated control functions in a variety of applications. Features include single supply operation, a variety of output configuration options, with an instruction set, internal architecture and I/O scheme designed to facilitate keyboard input, display output and BCD data manipulation. The COP421L is identical to the COP420L, except with 19 I/O lines instead of 23. They are an appropriate choice for use in numerous human interface control environments. Standard test procedures and reliable high-density fabrication techniques provide the medium to large volume customers with a customized Control Oriented processor at a low end-product cost.

Features

- Low cost
- Powerful instruction set
- 1k x 8 ROM, 64 x 4 RAM
- 23 I/O lines (COP420L)
- True vectored interrupt, plus restart
- Three-level subroutine stack
- 16 μs instruction time
- Single wide-range supply (4.5 - 9.5V)
- Low current drain (8 mA max)
- Internal time-base counter for real-time processing
- Internal binary counter register with serial I/O capability
- General purpose and TRI-STATE® outputs
- LS TTL/CMOS compatible in and out
- Direct drive of LED digit and segment lines
- Software/hardware compatible with other members of COP400 family
- Extended temperature range device available (−40 °C to +85 °C)

COP420L/421L Block Diagram

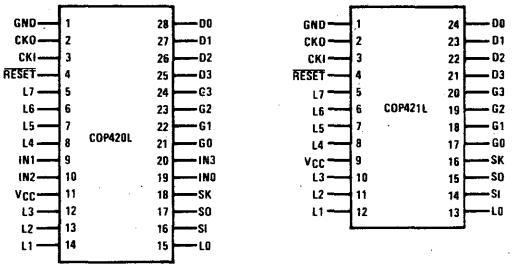


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Connection Diagrams



Functional Characteristics

Oscillator

There are four basic clock oscillator configurations:

a. Crystal Controller Oscillator.

b. External Oscillator.

c. RC Controlled Oscillator.

d. Externally Synchronized Oscillator.

I/O Options

COP outputs have the following optional configurations:

a. **Standard** — an active device to ground in conjunction with a pull-up to V_{CC}, compatible with LSTTL and CMOS input requirements.

b. **Open-Drain** — an active device to ground only, allowing external pull-up as required by the user's application.

c. **Push-Pull** — an active device to ground in conjunction with a pull-up paralleled by an active device to V_{CC}. This configuration has been provided to allow for fast rise and fall times when driving capacitive loads.

d. **LED Direct Segment Drive** — an active device to ground and to V_{CC}, meeting the typical current sourcing requirements of the segments of an LED display.

e. **LED Direct Digit Drive** — a high-current device to ground, meeting the current sinking needs of a small LED digit.

f. **TRI-STATE® Push-Pull** — an active device to ground and V_{CC} intended to meet the requirements associated with connection of these outputs to a data bus shared by other bus drivers.

CKO Pin Options

In a crystal controlled oscillator system, CKO is used as an output to the crystal network. As an option CKO can be a general purpose input. As another option, CKO can be a RAM power supply pin (V_R), allowing its connection to a standby/backup power supply to maintain the integrity of RAM data with minimum power drain (3mA maximum at 3.3V).

COP420L/421L Instruction Set

ARITHMETIC INSTRUCTIONS	ASC		Add with Carry, Skip on Carry
	ADD		Add A to RAM
	ADT		Add Ten to A
	AISC	y	Add Immediate, Skip on Carry (y≠0)
	CASC		Complement and Add with Carry, Skip on Carry
	CLRA		Clear A
	COMP		Ones complement of A to A
	NOP		No Operation
	RC		Reset C
	SC		Set C
	XOR		Exclusive-OR A with RAM
TRANSFER OF CONTROL INSTRUCTIONS	JID		Jump Indirect
	JMP		Jump
	JP		Jump within Page
	JSRP		Jump to Subroutine Page
	JSR		Jump to Subroutine
	RET		Return from Subroutine
	RETSK		Return from Subroutine, then Skip
MEMORY REFERENCE INSTRUCTIONS	CAMQ		Copy A, RAM to Q
	CQMA		Copy Q to RAM, A
	LD	r	Load RAM into A, Exclusive-OR Br with r
	LDD	r,d	Load A with RAM pointed to directly by r,d
	LQID		Load Q Indirect
	RMB	n	Reset RAM Bit n
	SMB	n	Set RAM Bit n
	STII	y	Store Memory Immediate and Increment Bd
	X	r	Exchange RAM with A, Exclusive-OR Br with r
	XAD	r,d	Exchange A with RAM pointed to directly by r,d
	XDS	r	Exchange RAM with A and Decrement Bd, Exclusive-OR Br with r
	XIS	r	Exchange RAM with A and Increment Bd, Exclusive-OR Br with r
REGISTER REFERENCE INSTRUCTIONS	CAB		Copy A to Bd
	CBA		Copy Bd to A
	LBI	r,d	Load B Immediate with r,d
	LEI	y	Load EN Immediate
	XABR		Exchange A with Br
TEST INSTRUCTIONS	SKC		Skip is C is True
	SKE		Skip if A Equals RAM
	SKGZ		Skip if G is Zero (all 4 bits)
	SKGBZ	n	Skip if G Bit is Zero
	SKMBZ	n	Skip if RAM Bit is Zero
	SKT		Skip on Timer
INPUT/OUTPUT INSTRUCTIONS	ING		Input G ports to A
	ININ		Input IN Inputs to A
	INIL		Input IL Latches to A
	INL		Input L Ports to RAM, A
	OBD		Output Bd to D Output
	OGI	y	Output to G Ports Immediate
	OMG		Output RAM to G Ports
	XAS		Exchange A with SIO

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ADVANCE INFORMATION
SEPTEMBER 1978

COP420C/COP421C Single-Chip CMOS Microcontrollers

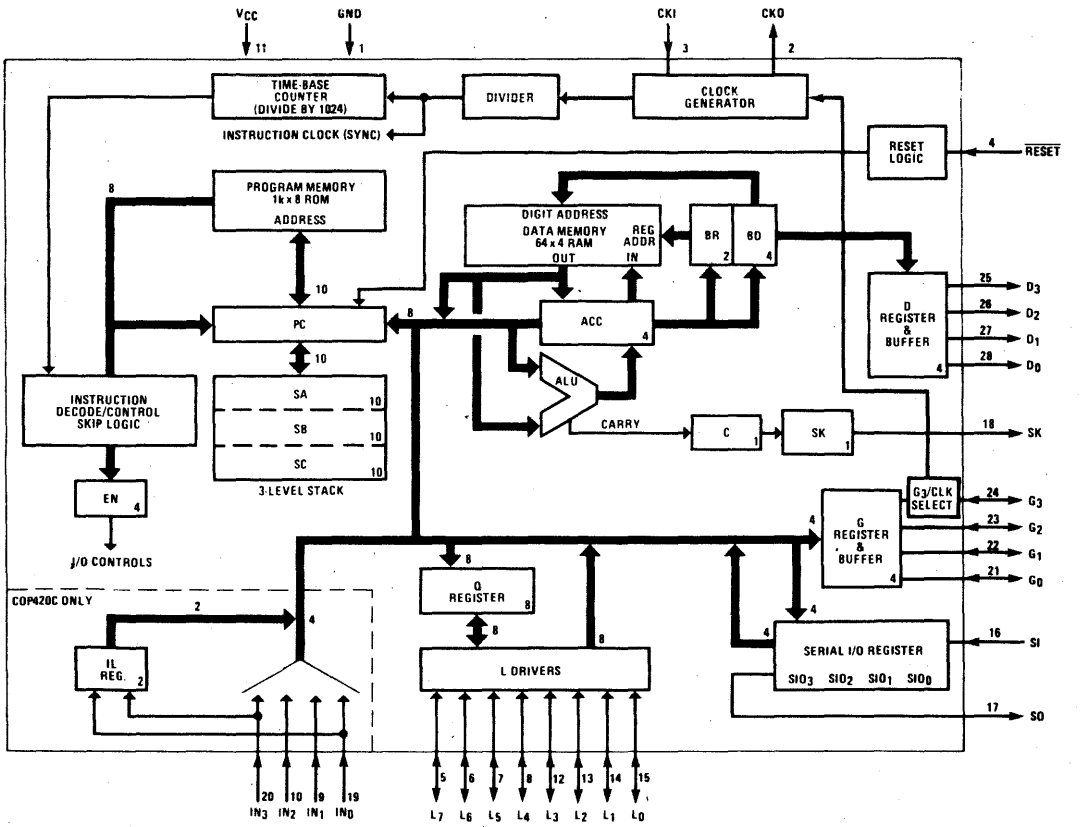
General Description

The COP420C and COP421C Single-Chip CMOS Microcontrollers are members of the Control Oriented Processor (COP) family, fabricated using Complementary MOS technology. They are complete microcomputers containing all system timing, internal logic, ROM, RAM and I/O necessary to implement dedicated control functions in a variety of applications. Features include single supply operation, a variety of output configuration options, with an instruction set, internal architecture and I/O scheme designed to facilitate keyboard input, display output and BCD data manipulation. The COP421C is identical to the COP420C, except with 19 I/O lines instead of 23. They are an appropriate choice for use in numerous human interface control environments. Standard test procedures and reliable high-density fabrication techniques provide the medium to large volume customers with a customized Control Oriented processor at a low end-product cost.

Features

- Lowest power dissipation (65 μW)
- Full Military temperature range (−55 °C to +125 °C)
- Powerful instruction set
- 1k x 8 ROM, 64 x 4 RAM
- 23 I/O lines (COP420C)
- True vectored interrupt, plus restart
- Three-level subroutine stack
- 16 μs instruction time, plus software selectable oscillators
- Single supply operation (2.4 - 6.3 V)
- Internal time-base counter for real-time processing
- Internal binary counter register with serial I/O capability
- General purpose and TRI-STATE® outputs
- TTL/CMOS compatible in and out
- LED direct drive outputs
- MICROBUS™ compatible
- Software/hardware compatible with other members of COP400 family

COP420C/421C Block Diagram

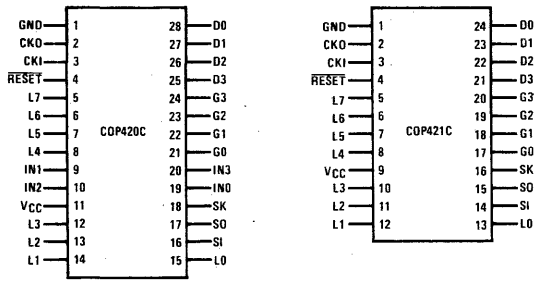


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Connection Diagrams



Functional Characteristics

Oscillator

There are four basic clock oscillator configurations:

a. Crystal Controlled Oscillator.

b. External Oscillator.

c. RC Controlled Oscillator.

d. Externally Synchronized Oscillator.

Optionally, the user may connect a 32kHz watch crystal to CKO/CKI, and a 16μs RC combination to G3; he may then software-select between the RC oscillator for faster processing, or the crystal for minimum current drain (25μA) while maintaining a real-time clock.

I/O Options

COP outputs have the following optional configurations:

a. **Standard** — an active device to ground in conjunction with an active device to V_{CC}, compatible with LSTTL and CMOS input requirements.

b. **Open-Drain** — an active device to ground only, allowing external pull-up as required by the user's application.

c. **LED Direct Drive** — an active device to ground and to V_{CC}, meeting the typical current sourcing requirements of the segments of an LED display. The sourcing device is clamped to limit current flow.

d. **TRI-STATE® Push-Pull** — an active device to ground and V_{CC} intended to meet the requirements associated with the MICROBUS™ option. These outputs are TRI-STATE® outputs, allowing for connection of these outputs to a data bus shared by other bus drivers.

CKO Pin Options

In a crystal controlled oscillator system, CKO is used as an output to the crystal network. As an option CKO can be a general purpose input, read into bit 2 of A (accumulator) upon execution of an INIL instruction.

Power Drain

When operating at a 16μs instruction cycle, the 420C will draw 600μA at 5V. When operating at minimum speed/power (e.g., from a 32kHz watch crystal), current drain is 25μA at 2.4V (50μA at 5V), and the instruction cycle is 244μs.

COP420C/421C Instruction Set

ARITHMETIC INSTRUCTIONS

ASC		Add with Carry, Skip on Carry
ADD		Add A to RAM
ADT		Add Ten to A
AISC	y	Add Immediate, Skip on Carry (y≠0)
CASC		Complement and Add with Carry, Skip on Carry
CLRA		Clear A
COMP		Ones complement of A to A
NOP		No Operation
RC		Reset C
SC		Set C
XOR		Exclusive-OR A with RAM

TRANSFER OF CONTROL INSTRUCTIONS

JID		Jump Indirect
JMP		Jump
JP		Jump within Page
JSRP		Jump to Subroutine Page
JSR		Jump to Subroutine
RET		Return from Subroutine
RETSK		Return from Subroutine, then Skip

MEMORY REFERENCE INSTRUCTIONS

CAMQ		Copy A, RAM to Q
CQMA		Copy Q to RAM, A
LD	r	Load RAM into A, Exclusive-OR Br with r
LDD	r,d	Load A with RAM pointed to directly by r,d
LQID		Load Q Indirect
RMB	n	Reset RAM Bit n
SMB	n	Set RAM Bit n
STII	y	Store Memory Immediate and Increment Bd
X	r	Exchange RAM with A, Exclusive-OR Br with r
XAD	r,d	Exchange A with RAM pointed to directly by r,d
XDS	r	Exchange RAM with A and Decrement Bd, Exclusive-OR Br with r
XIS	r	Exchange RAM with A and Increment Bd, Exclusive-OR Br with r

REGISTER REFERENCE INSTRUCTIONS

CAB		Copy A to Bd
CBA		Copy Bd to A
LBI	r,d	Load B Immediate with r,d
LEI	y	Load EN Immediate
XABR		Exchange A with Br

TEST INSTRUCTIONS

SKC		Skip is C is True
SKE		Skip if A Equals RAM
SKGZ		Skip if G is Zero (all 4 bits)
SKGBZ	n	Skip if G Bit is Zero
SKMBZ	n	Skip if RAM Bit is Zero
SKT		Skip on Timer

INPUT/OUTPUT INSTRUCTIONS

ING		Input G ports to A
ININ		Input IN Inputs to A
INIL		Input IL Latches to A
INL		Input L Ports to RAM, A
OBD		Output Bd to D Output
OGI	y	Output to G Ports Immediate
OMG		Output RAM to G Ports
XAS		Exchange A with SIO

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ADVANCE INFORMATION
SEPTEMBER 1978

COP400-PDS Product Development System

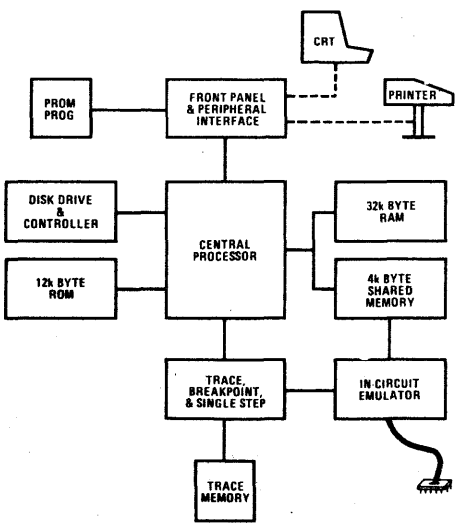
General Description

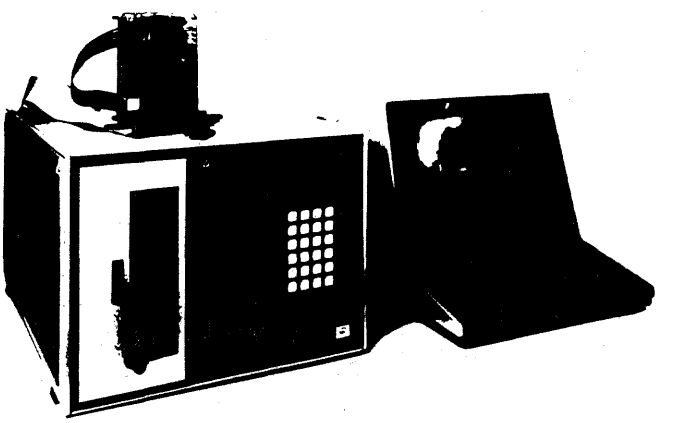
Finally, a single development tool which supports microcontroller development activities through every phase from concept to production. The COP400 Product Development System is built around a powerful 16-bit microcomputer to allow rapid execution of sophisticated, efficient utilities. The system meets the *total* product development need. An editor and assembler are provided to handle source code entry, conversion to object code and maintenance of documentation. The emulator card attachment allows object code to be executed under the careful control of the COPMONITOR debug utility. A cable can be connected from the PDS to the final product; in this mode, the full power and versatility of the PDS is extended to the product-to-be during its research and development phase. When a program is complete and ready to be committed to production, the PDS generates a transmittal disk that NSC will use to assure accurate masking of the final components. The usefulness of the PDS does not end there: a fixture is available for the incoming functional test of the ROM programmed COP400 devices. Thus, the COP400-PDS actively supports every step of a microcontroller product development activity.

Features

- Supports the entire COP400 microcontroller family
- A *total* concept-to-production tool
- Low cost
- 32k bytes R/W memory
- 12k bytes PROM (firmware)
- Disk-based
- Macro-assembler
- RS-232 and current loop peripheral interfaces
- Automatic baud rate selection (110-9600)
- Comprehensive in-circuit emulation (ICE), with single-step, breakpoint & trace
- Functional test module for incoming inspection
- ROM pattern transmission by disk

System Diagram





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COP400 Product Development System

FIRMWARE (ROM)

Executive

- Entered on a power-up or initialization.
- Provides for system definition.
- Allows loading and executing disk based programs by file name.

Diagnostics

- Memory address, bit and word test.
- CPU operation.
- Disk read test.
- Diagnostics are called by pressing diag. button on front panel.

SOFTWARE (Disk)

File Manager

- Create and delete disk files.
- Control file directory.
- Protect disk files.
- Pack disk files.
- Copy disk to disk.

DSKIT

- Initialize disk.
- Disk read/write diagnostic.

COP Monitor

- In-circuit emulator (ICE).
- Software breakpoints.
- External hardware breakpoint (2 lines).
- Lists user specified registers when selected breakpoint is detected.
- Real-time trace operation displays 256 address sequences. Synchronization may be pre, post or center and may be software or external event initiated.
- Mnemonic modification of object code.
- Single step.
- Step-list-restart.
- PROM programmer is built into the COP400-PDS front panel.
- UV erasable PROMs (MM5204Q).
- Single supply bipolar PROMs (DM74S296).

Editor

- Read text from disk or terminal.
- Display text on terminal.
- Write edited text to disk or printer.
- Generate source code for assemblers.
- Extensive word processing functions.
- Edit source files larger than the edit buffer.

Macro Assembler

- Macro generation capabilities.
- Listing controls.
- Conditional assembly operators.
- Wide variety of directives.
- Diagnostic messages that include error position in source line.
- MASKTRAN creates a disk file for transmission of customer ROM patterns and device I/O options to National Semiconductor.

PERIPHERALS

- The COP400-PDS will interface to a wide range of peripheral devices.
- Both RS-232 and current loop ports are provided.
- Console interface.
- Printer interface (RS-232 serial).
- Emulator card for in-circuit emulation.
- Functional test module for incoming inspection.

SYSTEM COMPONENTS

COP400-PDS

- Host microprocessor.
- 32k byte R/W memory.
- Single disk drive.
- System power supply.
- 12k byte ROM (all firmware described).
- Emulator cable.
- External connectors (3).
- Two master diskettes (all software described).
- Operator's Manual.
- PROM programmer.

Emulator Card

An emulator card is ordered separately for each of the COPS family of devices to be used. The emulator card allows real-time emulation in your applications circuitry using PROM memory or the development system R/W memory for program storage.

- PC assembly with the appropriate COP400 ROMless device and its support circuitry.
- Sockets for UV erasable or fusible link PROMs.
- In-circuit emulation cable with emulated COP device plug.
- The emulator card is shipped assembled and tested.

Video Display Terminal

The video display unit operates at baud rates from 110 to 9600. It provides keyboard input and video output for source program entry and editing, and system software operation.

Ordering Information

U.S. Version (60 Hz, 120 V_{AC}):
Part Number COP400-PDS.

European Version (50 Hz, 220 V_{AC}):
Part Number COP400-PDSE

- Video display terminal:
  Part Number COP400-842.
- COP420 emulator board:
  Part Number COP400-E02
- Master diskettes:
  Part Number COP400-D01.
- Operator's Manual:
  Publication Number 420305548-001.
- Incoming inspection test unit Part number COP400-T01 Available March 1979.

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NATIONAL SEMICONDUCTOR COP400 MICROCONTROLLER FAMILY GUIDE

SEPTEMBER 1978

	Specifications \ COP:	ROMless Devices			Single-Chip Microcontrollers										
		402	402M	404L	410L	411L	420	420L	420C	421	421L	421C	440	444L
MEMORY	ROM x 8	up to 1024 ext.		up to 2048 ext.	512		1024			1024			2048	
	RAM x 4	64		128	32*		64*			64*			128*	
INPUTS/OUTPUTS	Inputs	4			0		4			0			8	4
	Bidirectional TRI-STATE™ I/O	8			8		8			8			8	
	Bidirectional I/O	4			4	3	4			4			8	4
	Outputs	4			4	2	4			4			8	4
	Serial I/O and External Event Counter	Yes			Yes		Yes			Yes			Yes	
GENERAL	Interrupt	Yes	No	Yes	No		Yes			No			Yes	
	Stack Levels	3			2		3			3			3	
	MICROBUS™ Option	No	Yes	No	No		Yes	No	Yes	No			Yes	No
	Instruction Cycle (μs)	4		16	16		4	16		4	16		4	16
POWER/PKG	Supply Voltage	4.5-6.3		4.5-9.5	4.5-9.5		4.5-6.3	4.5-9.5	2.4-6.3	4.5-6.3	4.5-9.5	2.4-6.3	4.5-6.3	4.5-9.5
	Supply Current (mA)	28		14	5		25	7	**	25	7	**	35	11
	Package Size (pins)	40			24	20	28			24			40	28

*RAM keep-alive option (except 420C/421C). **Fast: 600μA. Slow: 25μA. Sleep: 5μA.

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SEPTEMBER 1978

COP402/COP402M ROMless N-Channel Microcontrollers

General Description

The COP402 and COP402M ROMless Microcontrollers are members of the Control Oriented Processor (COP) family, fabricated using N-channel silicon gate MOS technology. Each part contains CPU, RAM and I/O, and is identical to a COP420 device, except the ROM has been removed; pins have been added to output the ROM address and to input ROM data. In a system, the COP402 or 402M will perform exactly as the COP420; this important benefit facilitates development and debug of a COP420 program prior to masking the final part. These devices are also appropriate in low volume applications, or when the program may require changing. The COP402M is identical to the COP402, except the MICROBUS™ interface option has been implemented.

The COP402 may also be used to emulate the COP410L, 411L, 420L or 420C by appropriately reducing the clock frequency.

Features

- Low cost
- Exact circuit equivalent of COP420
- Standard 40-pin dual-in-line package
- Interfaces with standard PROM or ROM
- 64×4 RAM, addresses up to 1k×8 ROM
- MICROBUS™ compatible (COP402M)
- Powerful instruction set
- True vectored interrupt, plus restart
- Three-level subroutine stack
- 4.0μs instruction time
- Single supply operation (4.5V to 6.3V)
- Internal time-base counter for real-time processing
- Internal binary counter register with serial I/O capability
- Software/hardware compatible with other members of COP400 family

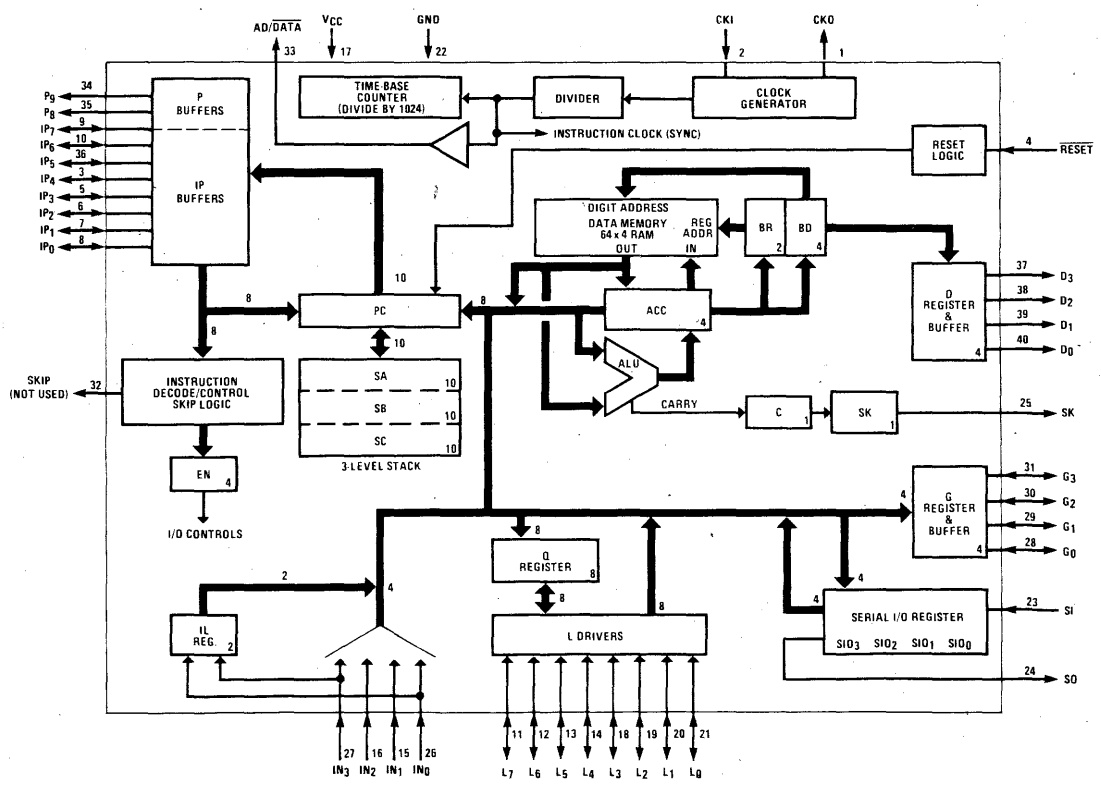


Figure 1. COP402/402M Block Diagram

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Absolute Maximum Ratings

Voltage at Any Pin Relative to GND	−0.5V to +7V
Ambient Operating Temperature	0°C to +70°C
Ambient Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C
Power Dissipation	0.75 Watt at 25°C 0.4 Watt at 70°C

Absolute maximum ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications are not ensured when operating the device at absolute maximum ratings.

DC Electrical Characteristics $0°C \leq T_A \leq +70°C$, $4.5V \leq V_{CC} \leq 6.3V$ unless otherwise noted.

Parameter	Conditions	Min	Max	Units
Operating Voltage (V_{CC})		4.5	6.3	V
Operating Supply Current	$V_{CC} = 5V$, $T_A = 25°C$ (all inputs and outputs open)		30	mA
Input Voltage Levels				
CKI Input Levels				
Logic High (V_{IH})		2.0		V
Logic Low (V_{IL})			0.4	V
RESET Input Levels				
Logic High		0.7 V_{CC}		V
Logic Low			0.6	V
RESET Hysteresis		1.0		V
SO Input Level (Test mode)		2.0	3.0	V
All Other Inputs				
Logic High	V_{CC} = max	3.0		V
Logic High	$V_{CC} = 5V \pm 5\%$	2.0		V
Logic Low			0.8	V
Output Voltage Levels (Note 2)				
TTL Operation	$V_{CC} = 5V \pm 5\%$			
Logic High (V_{OH})	$I_{OH} = 100\mu A$	2.4		V
Logic Low (V_{OL})	$I_{OL} = -1.6mA$		0.4	V
CMOS Operation				
Logic High (V_{OH})	$I_{OH} = 10\mu A$	$V_{CC} - 1$		V
Logic Low (V_{OL})	$I_{OL} = -10\mu A$		0.2	V
Output Current Levels				
LED Direct Drive Output	$V_{CC} = 6V$			
Logic High (I_{OH})	$V_{OH} = 2.0V$	2.5	14	mA
TRI-STATE® Output Leakage Current		−10	+10	μA

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AC Electrical Characteristics $0°C \leq T_A \leq +70°C$, $4.5V \leq V_{CC} \leq 6.3V$ unless otherwise noted.

Parameter	Conditions	Min	Max	Units
Instruction Cycle Time — t_C	figure 3	4	10	μs
CKI Using Crystal (figure 8)				
Input Frequency — f_I	÷16 mode	1.6	4	MHz
Duty Cycle (Note 2)	figure 3a	30	55	%
INPUTS: (figure 3a)				
IN_3-IN_0, G_3-G_0, L_7-L_0				
t_{SETUP}		1.7		μs
t_{HOLD}		100		ns
SI, IP_7-IP_0				
t_{SETUP}		0.3		μs
t_{HOLD}		100		ns
OUTPUTS:				
COP TO CMOS PROPAGATION DELAY	$4.5V \leq V_{CC} \leq 6.3V$, $C_L = 50pF$, $V_{OH} = 0.7V_{CC}$, $V_{OL} = 0.3V_{CC}$			
SK as a Logic-Controlled Clock				
t_{PD1}			1.1	μs
t_{PD0}			0.3	μs
SO, SK as a Data Output				
t_{PD1}			1.4	μs
t_{PD0}			0.3	μs
t_{PD1}	$V_{OH} = 2V$		0.7	μs
D_3-D_0, G_3-G_0				
t_{PD1}			1.6	μs
t_{PD0}			0.6	μs
L_7-L_0 (LED Direct Drive)				
t_{PD1}	$V_{OH} = 2V$		2.4	μs
t_{PD0}			0.4	μs
COP TO TTL PROPAGATION DELAY	fanout = 1 Standard TTL Load, $V_{CC} = 5V \pm 5\%$, $C_L = 50pF$, $V_{OH} = 2.4V$, $V_{OL} = 0.4V$			
AD/$\overline{DATA}$				
t_{PD1}			0.5	μs
t_{PD0}			0.5	μs
SKIP				
t_{PD1}			0.6	μs
t_{PD0}			0.6	μs

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AC Electrical Characteristics (continued) $0°C \leq T_A \leq +70°C$, $4.5V \leq V_{CC} \leq 6.3V$ unless otherwise noted.

Parameter	Conditions	Min	Max	Units
OUTPUTS (cont.):				
SK as a Logic-Controlled Clock				
t_{PD1}			0.8	μs
t_{PD0}			0.8	μs
SK as a Data Output, SO				
t_{PD1}			1.0	μs
t_{PD0}			1.0	μs
D_3-D_0, G_3-G_0				
t_{PD1}			1.3	μs
t_{PD0}			1.3	μs
L_7-L_0				
t_{PD1}			1.4	μs
t_{PD0}			0.4	μs
IP_7-IP_0, P_9, P_8				
t_{PD1}			1.5	μs
t_{PD0}			1.5	μs
CKO (figure 3a)				
t_{PD1}			0.2	μs
t_{PD0}			0.2	μs
MICROBUS™ TIMING (COP402M)	C_L = 50pF, V_{CC} = 5V ± 5%			
A. Read Operation (figure 4)				
Chip Select Stable before $\overline{RD}$ — t_{CSR}		50		ns
Chip Select Hold Time for $\overline{RD}$ — t_{RCS}		5		ns
$\overline{RD}$ Pulse Width — t_{RR}		300		ns
Data Delay from $\overline{RD}$ — t_{RD}			250	ns
$\overline{RD}$ to Data Floating — t_{DF}			200	ns
B. Write Operation (figure 5)				
Chip Select Stable before $\overline{WR}$ — t_{CSW}		20		ns
Chip Select Hold Time for $\overline{WR}$ — t_{WCS}		20		ns
$\overline{WR}$ Pulse Width — t_{WW}		300		ns
Data Setup Time for $\overline{WR}$ — t_{DW}		200		ns
Data Hold Time for $\overline{WR}$ — t_{WD}		40		ns
INTR Transition Time from $\overline{WR}$ — t_{WI}			700	ns

Note 1: Duty Cycle = $t_{WI}/(t_{WI} + t_{WO})$.

Note 2: See figure 11 for additional I/O characteristics.

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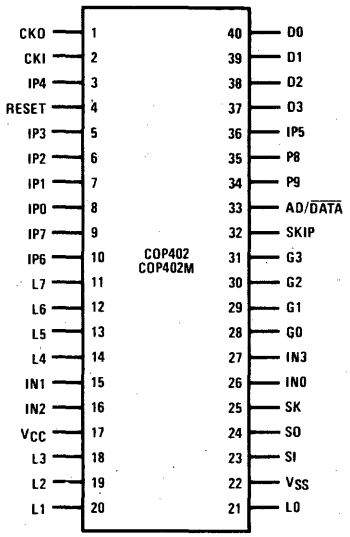


Figure 2. Connection Diagram

Pin	Description
L_7-L_0	8 bidirectional I/O ports with TRI-STATE®
G_3-G_0	4 bidirectional I/O ports
D_3-D_0	4 general purpose outputs
IN_3-IN_0	4 general purpose inputs
SI	Serial input (or counter input)
SO	Serial output (or general purpose output)
SK	Logic-controlled clock (or general purpose output)
AD/$\overline{\text{DATA}}$	Address out/data in flag

Pin	Description
SKIP	Instruction skip output
CKI	System oscillator input
CKO	System oscillator output
$\overline{\text{RESET}}$	System reset input
V_{CC}	Power supply
GND	Ground
IP7-IP0	8 bidirectional ROM address and data ports
P8, P9	2 ROM address outputs

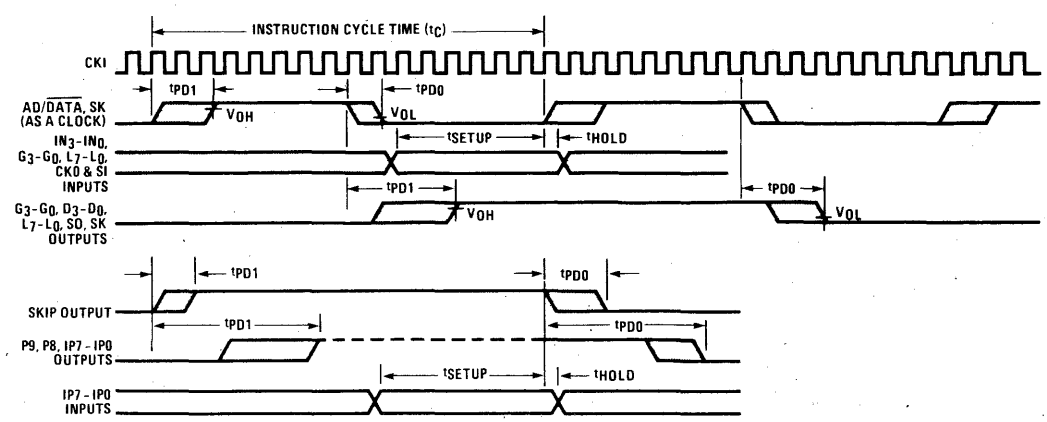


Figure 3a. Input/Output Timing Diagrams (Crystal ÷ 16 Mode)

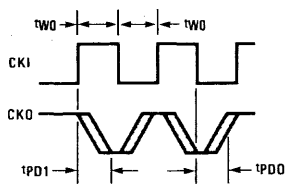


Figure 3b. CKO Output Timing

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- Memory IC
- RAM
- Static
- 1024x1
- CMOS
- 250 Nanoseconds
- 5 Volts

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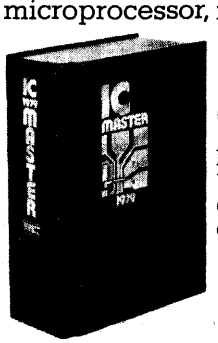
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UTP

μCOM-42 4-BIT SINGLE CHIP MICROCOMPUTER

DESCRIPTION

The μCOM-42 (Part No. μPD548) is a single chip microcomputer that is ideally suited for Electronic Cash Register (ECR), Point of Sale (POS) and Electronic Scale applications.

Containing a 4-bit Parallel ALU, ROM for program storage and RAM for data storage, the μCOM-42 provides an economical and simple solution to many Vending/Calculating requirements.

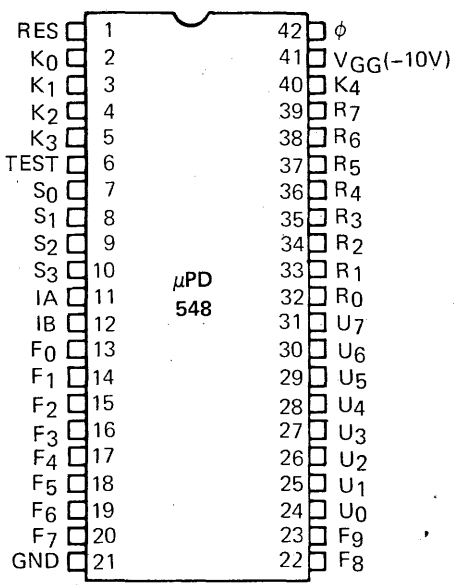
Because of its extensive instruction set and five input/output ports, the μCOM-42 is capable of controlling an 8 x 4 keyboard, an 8 digit display and low cost ECR-type printers.

Finally, the on-chip RAM space can be augmented by an external CMOS RAM for applications requiring low power data retention.

FEATURES

- Stand Alone 4-bit Microcomputer
- All 72 Instructions are Single Byte
- 10 μsec Instruction Cycle
- 1920 x 10-Bit Program Memory (ROM)
- 96 x 4-Bit Data Memory (RAM)
- 4-Level Stack
- 2 Interrupt Request Lines
- I/O Compatible with TTL
- 10 Discrete Output Ports (F_0-F_9)
- Two 8-Bit Output Ports (U_0-U_7, R_0-R_7)
- One 4-Bit Input Port (K_0-K_3)
- One 4-Bit Input/Output Port (S_0-S_3)
- One Single Bit Testable Input Port (K_4)
- Single Phase TTL Level Clock (200 KHz Max.)
- Single Supply, −10V PMOS Technology
- 42 Pin Plastic Dual-in-Line Package

PIN CONFIGURATION

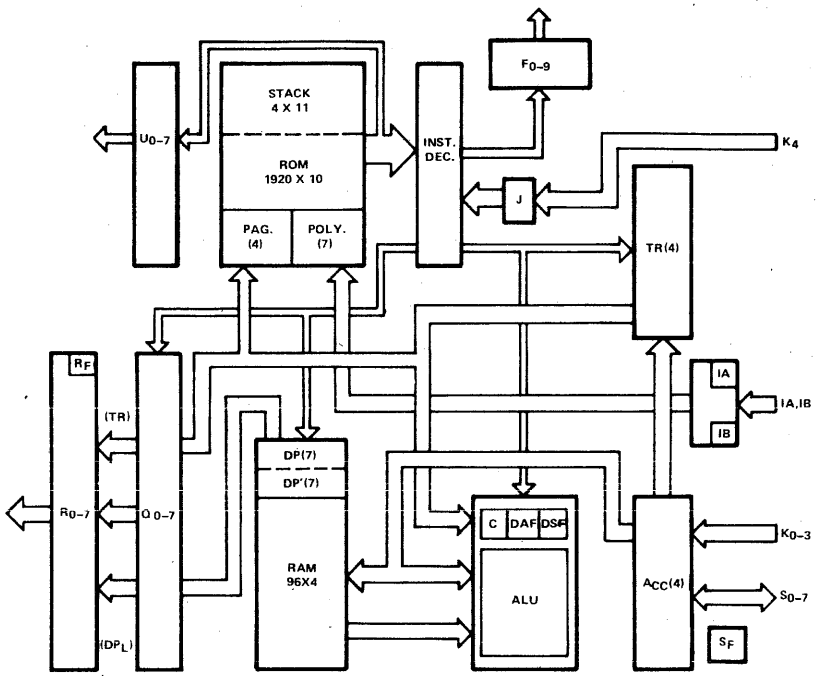


PIN NAMES

RES	Reset
K_0–K_3	Input Port K
TEST	Input for Testing (Normally V_{GG})
S_0–S_3	Input/Output Port S
IA, IB	Interrupt Input Ports
F_0–F_9	Output Port F
U_0–U_7	Output Port U
R_0–R_7	Output Port R
K_4	Input Port for Condition Test
φ	Clock Input

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BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

Program Counter

The 11-bit program counter is composed of two sections, a 4-bit page register and a 7-bit polynomial counter. The page register selects one page out of 15, each consisting of 128 words addressed by the 7-bit polynomial counter. The contents of the page register are independent of the operation of the polynomial counter, so that it is not affected by polynomial counter overflow.

Stack Register

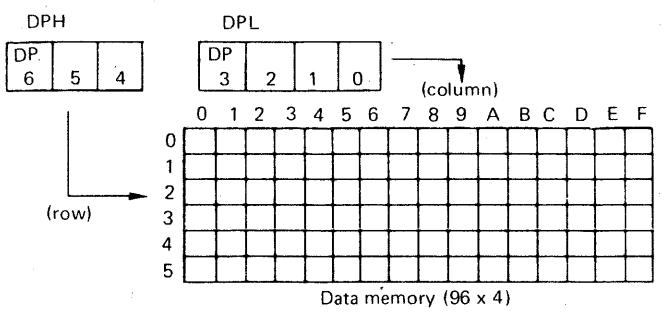
In order to store the program counter contents upon an interrupt or subroutine call, four 11-bit stack registers are provided to enable a combination of subroutine calls and interrupt nesting to four levels. The stack register is a LIFO (Last in, First-Out) type.

ROM (Read Only Memory)

The on-chip ROM consists of 1,920 words of ten bits each and is divided into 15 pages. A page is selected by the page register, the upper four bits of the program counter. Each page consists of 128 words addressed by the polynomial counter, the lower seven bits of the program counter.

RAM (Data Memory)

The data memory is a 96 x 4-bit RAM addressed by a 7-bit data pointer (DP). The RAM is divided into six rows of 16 4-bit columns each. The 7-bit data pointer consists of an upper 3-bit register (DPH) which selects the row address and a lower 4-bit register (DPL) which selects the column address.



Data memory (96 x 4)

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FUNCTIONAL DESCRIPTION (CONT.)

Internal Registers

The Accumulator (ACC) is connected with the ALU and the carry flip-flop (C) and is able to perform either binary or decimal arithmetic by testing the decimal addition flip-flop (DAF) and the decimal subtraction flip-flop (DSF). Constants are loaded into the ACC as immediate data from ROM and variable data are loaded from or exchanged with RAM. The ACC is also connected with the temporary register (TR), the parallel I/O port S and the parallel input port K. The TR is an auxiliary register used for temporary storage of 4-bit data. The Q register is an 8-bit serial-in/parallel-out shift register designed for display digit strobing and generation of printer hammer triggers.

I/O Ports

The R port is an 8-bit parallel port that may be loaded from the Q register for digit strobing or loaded with the 4-bit TR and the 4-bit DPL for external RAM addressing. The U port is an 8-bit parallel port that is loaded with immediate data. It is usually used for outputting segment information for display and digit information for key scanning. The K port is a 4-bit input port that is usually used for key scan input. The K4 port is a single bit port that is testable by software. The S port is a 4-bit parallel I/O port that is typically used as the data bus to external RAM. The F port consists of ten discrete output lines that can be individually set or reset under program control.

Interrupt Ports

Two interrupt input lines, IA and IB, are available to accept an interrupt request when interrupts are enabled. IA has a higher priority level than IB. Thus when concurrent interrupts occur on both IA and IB only the IA interrupt is accepted and both are disabled. But a single IB interrupt disables only the IB interrupt and leaves IA enabled.

INSTRUCTION SET

The μCOM-42 has a powerful 72, 10-bit word, instruction set. All instructions are single words. There are a number of multi-function instructions which reduce the number of program steps. In addition, automatic data pointer modification, single word subroutine calls and N-way branch capability all help improve operation speed and reduce ROM requirements. The μCOM-42 instruction set is summarized below.

MNEMONIC	CYCLES	DESCRIPTION	CONDITIONS FOR SKIP
CMA	1	$A_{CC} \leftarrow (\overline{A_{CC}})$	
CIA	1	$A_{CC} \leftarrow (\overline{A_{CC}}) + 1$	
INA	1/2	$A_{CC} \leftarrow (A_{CC}) + 1$	Carry = 1
DEA	1/2	$A_{CC} \leftarrow (A_{CC}) - 1$	Borrow ≠ 1
RFC	1	$C \leftarrow 0$	
SFC	1	$C \leftarrow 1$	
DSM	1	Decimal Subtract Mode	
DAM	1	Decimal Add Mode	
AD	1/2	$A_{CC} \leftarrow (A_{CC}) + [DP]$	Carry = 1
ADC	1	$A_{CC}, C \leftarrow (A_{CC}) + [DP] + (C)$	
ADI	1/2	$A_{CC} \leftarrow (A_{CC}) + I_3 I_2 I_1 I_0$	Carry = 1
LM	1	$A_{CC} \leftarrow [DP]$ $DP_H \leftarrow (DP_H) \veebar M_2 M_1 M_0$	
XM	1	$(A_{CC}) \leftrightarrow [DP]$ $DP_H \leftarrow (DP_H) \veebar M_2 M_1 M_0$	
XMI	1/2	$(A_{CC}) \leftrightarrow [DP]$ $DP_H \leftarrow (DP_H) \veebar M_2 M_1 M_0$ $DP_L \leftarrow (DP_L) + 1$	$(DP_L) = 8$ or $(DP_L) = 0$
XMD	1/2	$(A_{CC}) \leftrightarrow [DP]$; $DP_H \leftarrow (DP_H)$ $M_2M_1M_0$; $DP_L \leftarrow (DP_L) - 1$	$(DP_L) = F$ or $(DP_L) = 7$
LI	1	$A_{CC} \leftarrow I_3 I_2 I_1 I_0$	
LDI	1	$DP \leftarrow I_6$–I_0	
IND	1/2	$DP_L \leftarrow (DP_L) + 1$	$(DP_L) = 8$ or $(DP_L) = 0$
DED	1/2	$DP_L \leftarrow (DP_L) - 1$	$(DP_L) = F$ or $(DP_L) = 7$
XDP	1	$(DP) \leftrightarrow (DP')$	
ZAG	1	$000DP_L \leftarrow (DP)$	

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MNEMONIC	CYCLES	DESCRIPTION	CONDITIONS FOR SKIP
XTA	1	$(A_{CC}) \leftrightarrow (TR)$	
LTI	1	$TR \leftarrow I_3\ I_2\ I_1\ I_0$	
QS1	1	$Q_{n+1} \leftarrow Q_n,\ Q_0 \leftarrow 1$	
QS0	1	$Q_{n+1} \leftarrow Q_n,\ Q_0 \leftarrow 0$	
SB	1	$[DP, B_1, B_0] \leftarrow 1$	
RB	1	$[DP, B_1, B_0] \leftarrow 0$	
SBT	1/2	Skip if $[DP, B_1, B_0] = 1$	$B_1\ B_0 = 1$
SC	1/2	Skip if $(C) = 1$	$(C) = 1$
SEM	1/2	Skip if $(A_{CC}) = [DP]$	$(A_{CC}) = [DP]$
SEI	1/2	Skip if $(A_{CC}) = I_3\ I_2\ I_1\ I_0$	$(A_{CC}) = I_3\ I_2\ I_1\ I_0$
SK4	1/2	Skip if $K_4 = 1$	$K_4 = 1$
JPT	1	$PC \leftarrow (TR), P_{6-0}$	
JPA	1	$PC_{6-4} \leftarrow P_{6-4}$ $PC_{3-0} \leftarrow P_{3-0} V\ (A_{CC})$	
JCP	1	$PC_{6-0} \leftarrow P_{6-0}$	
CAL	1	$[STACK] \leftarrow (PC)$ $PC \leftarrow 1000\ P_6\ P_5\ P_4\ P_3\ P_2\ P_1\ P_0$	
RT	1	$PC \leftarrow [STACK]$	
RTS	2	$PC \leftarrow [STACK]$ $PC \leftarrow (PC) + 1$	
EIA	1	Enable IA port	
DIA	1	Disable IA port	
EIB	1	Enable IB port	
DIB	1	Disable IB port	
OIU	1	$U_{7-0} \leftarrow I_{7-0}$ $R_{7-0} \leftarrow (Q_{7-0})$	
ERO	1	Enable R port	
DRO	1	Disable R port	
OQR	1	$R \leftarrow (Q)$	
OTR	1	$R_{7-4} \leftarrow (TR), R_{3-0} \leftarrow (DP_L)$	
SFS	1	$S \leftarrow (A_{CC})$	
RFS	1	S port Input Mode	
IS	1	$A_{CC} \leftarrow S$	
IK	1	$A_{CC} \leftarrow K$	
RF1	1	$F_1 \leftarrow 0$	
SF1	1	$F_1 \leftarrow 1$	
RF2	1	$F_2 \leftarrow 0$	
SF2	1	$F_2 \leftarrow 1$	
RF3	1	$F_3 \leftarrow 0$	
SF3	1	$F_3 \leftarrow 1$	
RF4	1	$F_4 \leftarrow 0$	
SF4	1	$F_4 \leftarrow 1$	
RF5	1	$F_5 \leftarrow 0$	
SF5	1	$F_5 \leftarrow 1$	
RF6	1	$F_6 \leftarrow 0$	
SF6	1	$F_6 \leftarrow 1$	
RF7	1	$F_7 \leftarrow 0$	
SF7	1	$F_7 \leftarrow 1$	
RF8	1	$F_8 \leftarrow 0$	
SF8	1	$F_8 \leftarrow 1$	
RF9	1	$F_9 \leftarrow 0$	
SF9	1	$F_9 \leftarrow 1$	
RF0	1	$F_0 \leftarrow 0$	
SF0	1	$F_0 \leftarrow 1$	
NOP	1	No Operation	

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EVACHIP-42

DESCRIPTION

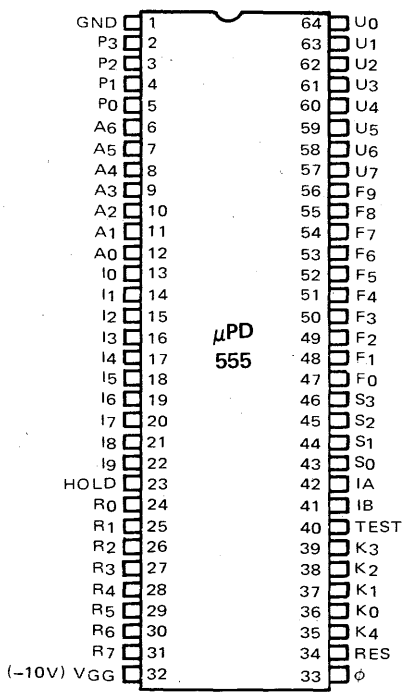
The μPD555 is a system evaluation chip designed to support both hardware and softwa debugging of the μCOM-42 (μPD548) one-chip microcomputer system.

The μPD555 and the μPD548 have the same functionality in all aspects except that the μPD555 does not contain a read only memory, but provides addressing capability to external memory and HOLD function for step-by-step operation.

FEATURES

- 4-Bit Parallel Processor
- Powerful 72 Instruction Set Including Decimal/Binary Arithmetic Operations
- 10 μs Instruction Cycle Time
- Addressing Capability up to 1920 Words by 10-Bits of External Program Memory
- 96 Words by 4-Bit Data Memory On Chip
- 4-Level Subroutines
- Two Interrupt Input Lines (IA and IB)
- HOLD Capability
- A Variety of Input/Output Ports –
  - 10 Discrete Output Ports (F_9-F_0)
  - Two 8-Bit Output Ports (U_7-U_0, R_7-R_0)
  - 4-Bit Input Port (K_3-K_0)
  - 4-Bit Input/Output Port (S_3-S_0)
    I/O Level Compatible with μPD5101
  - 1-Bit Test Input Line
- P-Channel MOS
- Open Drain Output
- Single Power Supply: −10V
- Available in a 64 Pin Ceramic Dual-in-Line Package

PIN CONFIGURATION

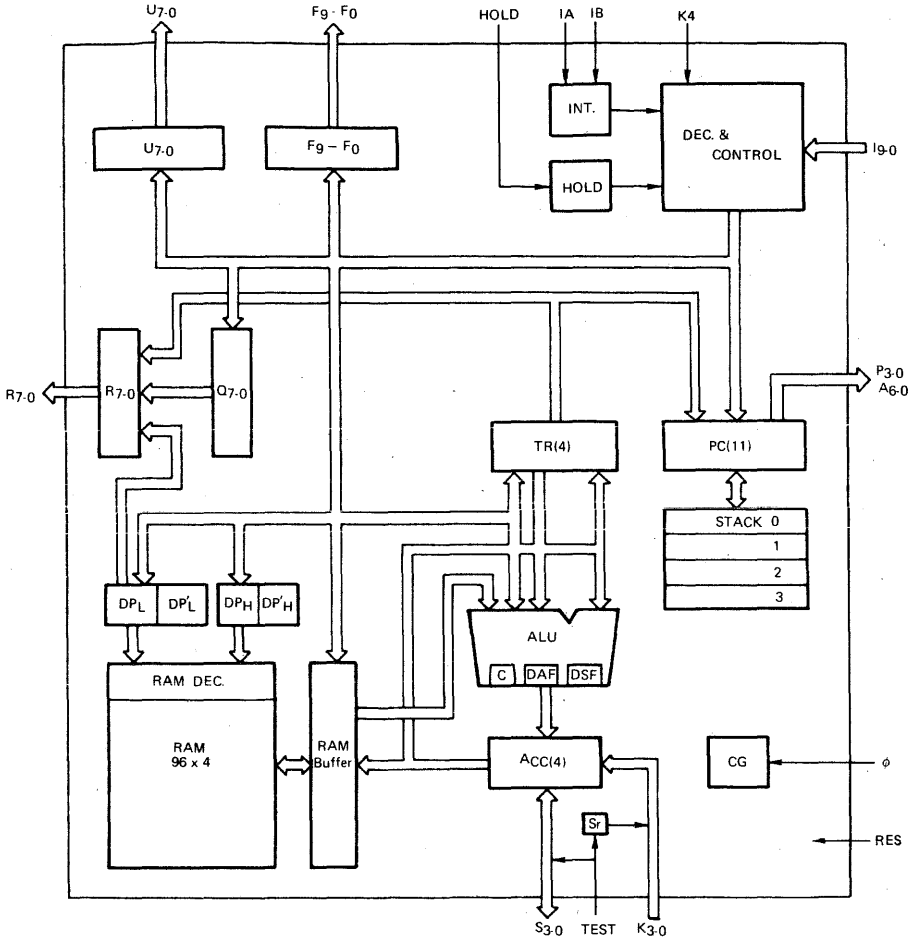


PIN NAMES

$P_0 - P_3$	Page Output
$A_0 - A_6$	Address Output
$I_0 - I_9$	Instruction Input
HOLD	HOLD Input
$R_0 - R_7$	Output Port R
φ	Clock Input
RES	Reset Input
K4	K4 Test Input Line
$K_0 - K_3$	K Input Port
TEST	IC Test Input
IA, IB	Interrupt Input
$S_0 - S_3$	Input/Output Port S
$F_0 - F_9$	Output Port F
$U_0 - U_7$	Output Port U

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BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	−10°C to +70°C
Storage Temperature	−40°C to +125°C
Supply Voltage V_{GG}	−15 to +0.3 Volts
All Input Voltages	−20 to +0.3 Volts
All Output Voltages	−20 to +0.3 Volts

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

CAPACITANCE

T_a = 25°C

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input Capacitance	C_I			15	pf	f = 1 MHz
Output Capacitance	C_O			15	pf	
Input/Output Capacitance	C_{IO}			15	pf	

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DC CHARACTERISTICS

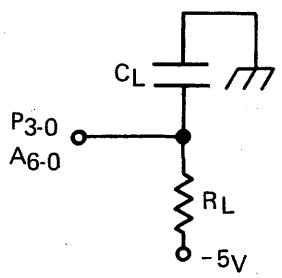
T_a = −10°C to +70°C; V_{GG} = −10V ± 10%, unless otherwise noted.

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
High Level Input Voltage	V_{IH}	0		−2.0	V	
Low Level Input Voltage	V_{IL1}	−4.3			V	S, ϕ, I_{9-0}
	V_{IL2}	−7.0			V	Except S, ϕ, I_{9-0}
High Level Input Leakage Current	I_{LIH}			+10	μA	V_I = −1V
Low Level Input Leakage Current	I_{LIL}			−10	μA	V_I = −11V
High Level Output Current	I_{OH}	−1.0			mA	V_O = −1V, except S port
Low Level Output Leakage Current	I_{LOL1}			−30	μA	V_O = −11V, except S port
High Level Output Voltage	V_{OH}			−1.75	V	I_{OH} = −100 μA, S port
Low Level Output Leakage Current	I_{LOL2}			−10	μA	V_O = −5V, S port
Power Supply Current	I_{GG}		−30	−60	mA	

AC CHARACTERISTICS

T_a = −10°C to +70°C, V_{GG} = −10V ± 10%, unless otherwise noted.

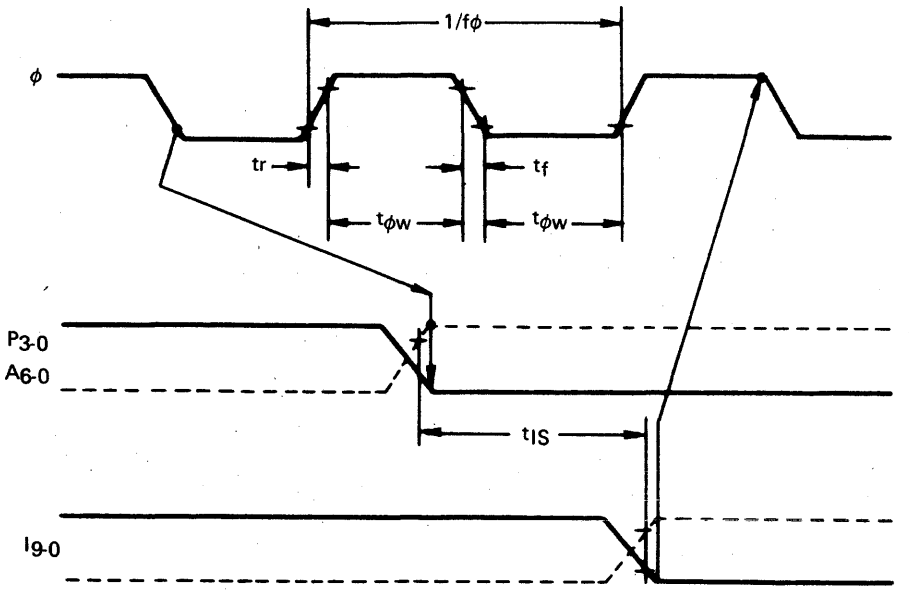
PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Clock Frequency	f_ϕ	100		200	KHz	
Clock Pulse Width	$t_{\phi W}$	2.25				
Clock Rise and Fall Times	tr, tf			0.5	μs	
Input Setup Time from Output	t_{IS}			2.5	μs	C_L = 100 pF, R_L = 5.1 KΩ



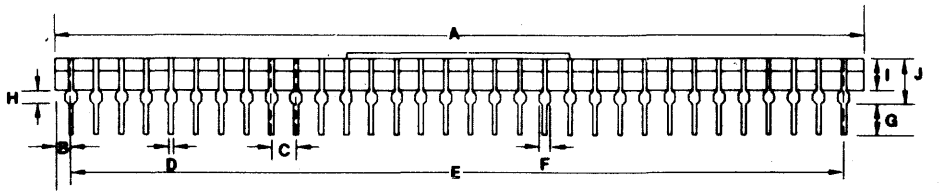
LOAD CIRCUIT

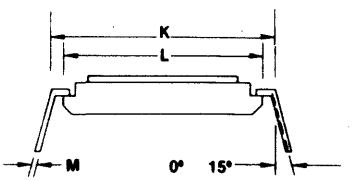
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TIMING WAVEFORM



PACKAGE OUTLINE
μPD555D





ITEM	MILLIMETERS	INCHES
A	82.0 MAX	3.23 MAX
B	1.6	0.063
C	2.54	0.1
D	0.43 ± 0.1	0.017 ± 0.004
E	78.8	3.1
F	1.27	0.05
G	3.2 MIN	0.13 MIN
H	1.3 MIN	0.05 MIN
I	3.9	0.154
J	5.2 MAX	0.205 MAX
K	22.96	0.904
L	20.3	0.8
M	0.3 ± 0.1	0.012 ± 0.004

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μCOM-43/44/45 4-BIT SINGLE CHIP MICROCOMPUTERS

DESCRIPTION

The μCOM-43 Family consists of three device types designed to offer a full range of cost/performance tradeoffs. All three devices share compatible hardware and instruction set. The μCOM-43 Family is designed for general purpose controller applications and offers ideal devices for industrial controls, appliance controls, games, etc.

All three devices contain the functional blocks necessary to enable their use for both industrial and non-industrial controller applications. These blocks include: a 4-bit parallel ALU; 8-bit wide ROM for program storage; 4-bit wide RAM for data storage; stack register for subroutines; extensive I/O; and an on-chip clock generator.

The instruction set of the μCOM-43 Family is designed to perform controller-oriented functions and for efficient use of the fixed program memory space. The instruction set includes a number of multifunction instructions, powerful I/O instructions including single bit manipulation, and test-and-skip instructions for conditional processing.

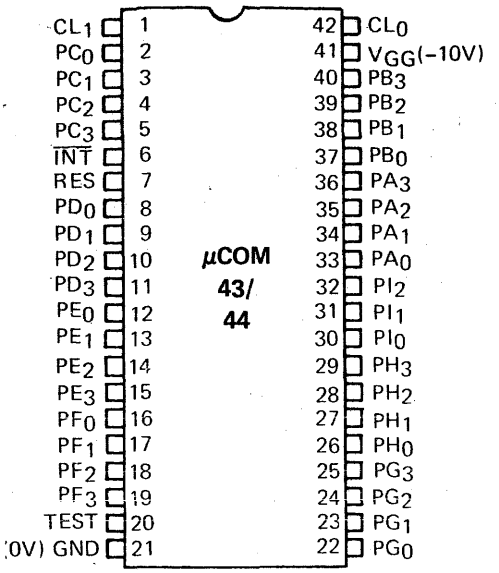
The three device types comprising the μCOM-43 Family are differentiated by ROM/RAM size and I/O lines. The μCOM-43 has 2000 x 8 ROM, 96 x 4 RAM and 35 I/O lines. The μCOM-44 has 1000 x 8 ROM, 64 x 4 RAM and 35 I/O lines. The μCOM-45 has 1000 x 8 or 640 x 8 ROM, 32 x 4 RAM and 21 I/O lines. In addition, the μCOM-43 has real hardware interrupt, 3 level stack and programmable timer, while the μCOM-44/45 have pseudo-interrupt capability and a single level stack.

FEATURES

- Stand Alone 4-Bit Microcomputers for Control Applications
- Powerful Instruction Set Capable of: Binary Addition; Decimal Addition and Subtraction; Logical Operations
- 10 μs Instruction Cycle
- Choice of ROM Size: 2000 x 8 – μCOM-43
1000 x 8 – μCOM-44
1000 x 8 – μCOM-45
640 x 8
- Choice of RAM Size: 96 x 4 – μCOM-43
64 x 4 – μCOM-44
32 x 4 – μCOM-45
- Choice of I/O Power: 35 lines – μCOM-43
35 lines – μCOM-44
21 lines – μCOM-45
- All Capable of Single Bit Manipulation and 4-Bit Parallel Processing.
- Interrupt Capability
- On-Chip Clock Generator
- Open Drain Outputs
- Choice of PMOS or CMOS Technology, Both Requiring Single Supplies
- Available in 42 Pin or 28 Pin Plastic Dual-in-Line Packages

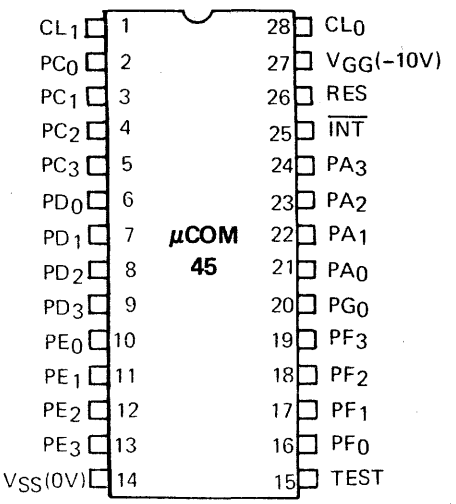
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PIN CONFIGURATIONS



PIN NAMES

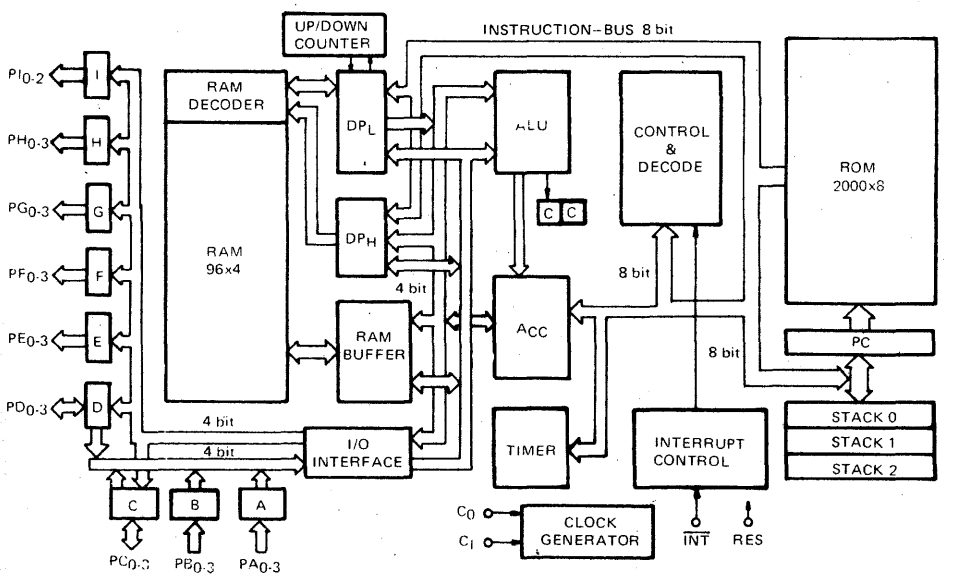
CL_0–CL_1	External Clock Source
PC_0–PC_3	Input/Output Port C
$\overline{INT}$	Interrupt Input
RES	Reset
PD_0–PD_3	Input/Output Port D
PE_0–PE_3	Output Port E
PF_0–PF_3	Output Port F
TEST	Input for Testing (Normally GND)
PG_0–PG_3	Output Port G
PH_0–PH_3	Output Port H
PI_0–PI_3	Output Port I
PA_0–PA_3	Input Port A
PB_0–PB_3	Input Port B



PIN NAMES

CL_0–CL_1	External Clock Source
PC_0–PC_3	Input/Output Port C
PD_0–PD_3	Input/Output Port D
PE_0–PE_3	Output Port E
PF_0–PF_3	Output Port F
PG_0	Output Port G
PA_0–PA_3	Input Port A
$\overline{INT}$	Interrupt Input
RES	Reset

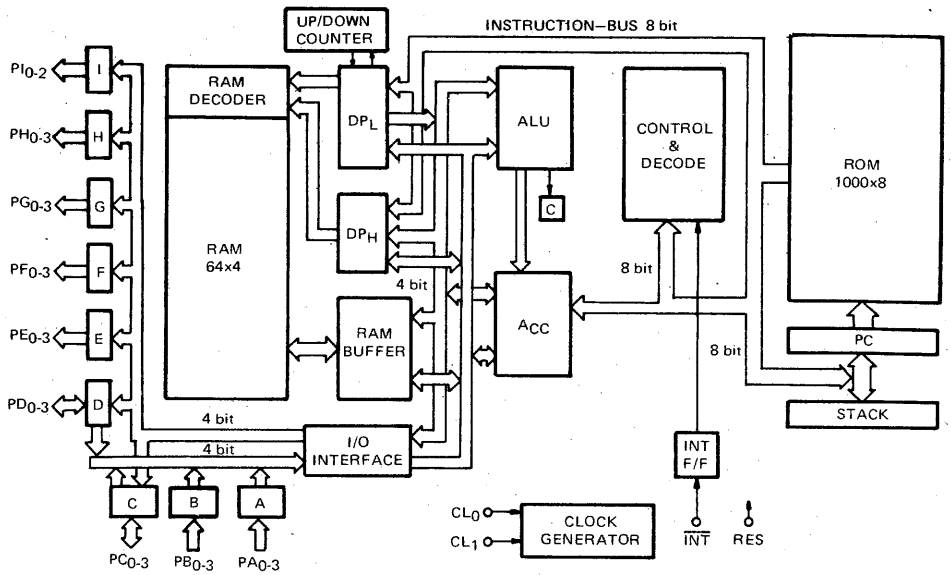
BLOCK DIAGRAM μCOM-43



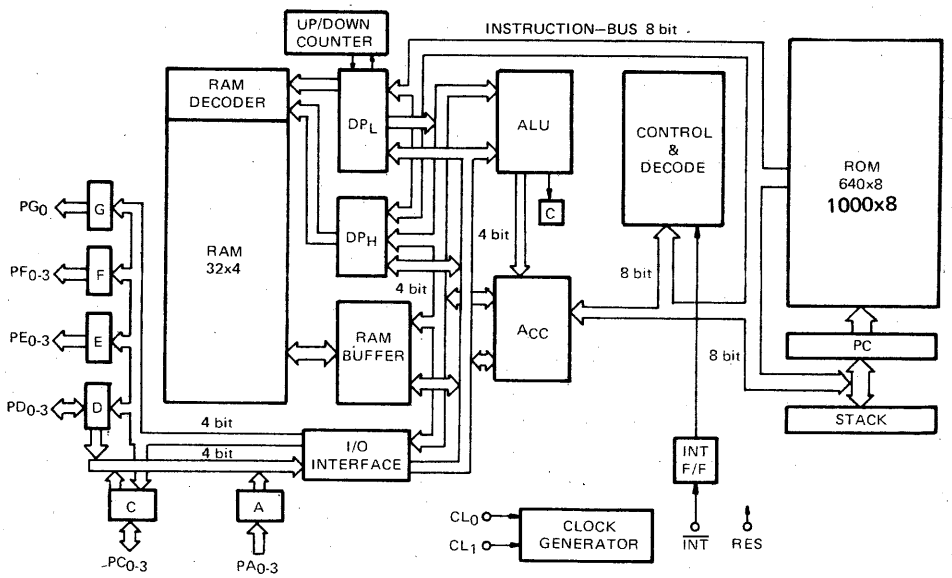
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BLOCK DIAGRAMS

μCOM-44



μCOM-45



FUNCTIONAL DESCRIPTION

Program Counter

The 11-bit program counter (10-bit for μCOM-44/45) is organized as a 3-bit register (2-bit for μCOM-44/45) and an 8-bit binary up-counter (lower eight bits). The contents of the upper register specify one of the fields of the ROM. The 8-bit binary counter is divided so that the contents of the higher two bits specify one of four pages in a field and the lower six bits specify one of 64 addresses in a page. The contents of the lower eight bits of the program counter (8-bit binary up-counter) are simply incremented to execute the instructions sequentially. In a field, a page is automatically extended to the next one and four pages (256 bytes) are automatically executed.

Stack Register

The stack register is a last-in-first-out (LIFO) push down stack register organized as 3 words x 11 bits (1 word x 10 bits for μCOM-44/45). This register is used to save the contents of the program counter (return address) when a subroutine is called or an interrupt is acknowledged.

ROM (Read-Only Memory)

The user's application program is stored in the 8-bit wide mask programmable read-only memory (ROM). The ROM is organized into fields and pages. The 2000 word ROM of the μCOM-43 has eight fields, the 1000 word ROM of the μCOM-44/45 has four fields and the 640 word ROM of the low-end μCOM-45 has two fields. Each field is divided into four pages of 64 words each, and each word consists of eight bits.

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FUNCTIONAL DESCRIPTION (CONT.)

RAM (Data Memory)

The RAM is organized in a multi-row by 16 column configuration. It is addressed by a data pointer of which the higher bits (DPH) address the row and the lower bits (DPL) address the column. The exact RAM size for each device is shown below.

	RAM	ROW/COLUMN ORGANIZATION	DPH	DPL
μCOM-43	96 x 4	6 x 16	3	4
μCOM-44	64 x 4	4 x 16	2	4
μCOM-45	32 x 4	2 x 16	1	4

Internal Registers

The ALU (Arithmetic Logic Unit) and the ACC (Accumulator) form the heart of the μCOM-43 Family microcomputer system. The ALU performs arithmetic and logical operations and tests for operation results. The result of an operation by the ALU is stored in the ACC and in the carry F/F. The ACC is a 4-bit register which stores ALU results and other data to be processed. The carry F/F is a single bit flip-flop which indicates when a carry bit is generated during addition.

Flag Register (μCOM-43 Only)

A 4-bit word in the RAM can be specifically used as a software controlled general purpose flag register. The individual flag bits can be set or reset and tested for either a 1 or a 0. This can be done directly without modifying the RAM data pointer.

Working Registers (μCOM-43 Only)

There are six words in RAM that can be used as 4-bit general purpose working registers. These registers can be directly manipulated without modification of the data pointer and are used for data transfer and exchange between the data pointer and the working register, and between the ACC and the working register.

Programmable Interval Timer (μCOM-43 Only)

The μCOM-43 contains a software programmable interval timer composed of a 6-bit polynomial counter and a 6-bit programmable binary counter.

The initial setting of the timer is done using the timer set instruction STM, with the timer starting to count at the end of the STM instruction execution. The STM instruction contains six binary bits of immediate data which is loaded in the 6-bit programmable binary counter upon STM instruction execution. By varying the 6-bit immediate data, one of 64 time intervals can be programmed.

I/O Ports

The μCOM-43/44 have 35 input/output ports (μCOM-45 has 21) for communication with and control of the external world. These ports are organized into nine input/output ports (A to I). Eight ports (A to H) are composed of four bits each and the last port (I) is composed of three bits.

Input Ports	(4 bits each): A, B ①
Input/Output Ports	(4 bits each): C, D
Output Ports	(4 bits each): E, F, G ②, H ①
Output Ports	(3 bits): I ①

Notes: ① Not on μCOM-45.

② G Port on μCOM-45 is a single line.

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FUNCTIONAL DESCRIPTION (CONT.)

In order to provide flexible and efficient use of these I/O ports, a variety of input/output instructions are provided which enable single bit set/reset, single bit test and conditional skip, 4-bit parallel input/output and 8-bit immediate parallel output. The I/O instructions are divided into two types, the ones dedicated to specific ports and the ones that use the 4-bit data in the DPL to select a desired port. The former include such instructions as IA and OE that specifically access port A and E, respectively. The latter require that a 4-bit code assigned to the desired port be loaded into the DPL using data pointer manipulation instructions prior to I/O instruction execution.

INSTRUCTION SET

The μCOM-43 has an 80 instruction set. The μCOM-44/45 have a 58 instruction subset of the μCOM-43. The majority of the 22 instruction difference is related to added hardware features of the μCOM-43. The instruction set is summarized below.

MNEMONIC	BYTES	CYCLES	DESCRIPTION	CONDITION FOR SKIP
CLA	1	1	$A_{CC} \leftarrow 0$	
CMA	1	1	$A_{CC} \leftarrow (A\overline{CC})$	
CIA	1	1	$A_{CC} \leftarrow (A\overline{CC})+1$	
INC	1	1/2-3	$A_{CC} \leftarrow (A_{CC})+1$; skip if Carry	Carry
DEC	1	1/2-3	$A_{CC} \leftarrow (A_{CC})-1$; skip if Borrow	Borrow
CLC	1	1	$C \leftarrow 0$	
STC	1	1	$C \leftarrow 1$	
XC	1	1	$(C) \rightleftharpoons (C')$	
RAR	1	1	$(A_{CCn-1}) \leftarrow (A_{CCn})$; $C \leftarrow (A_{CC0})$, $(A_{CC3}) \leftarrow (C)$	
INM	1	1/2-3	$[(DP)] \leftarrow [(DP)]+1$; skip if $[(DP)]=0$	$[(DP)]=0$
DEM	1	1/2-3	$[(DP)] \leftarrow [(DP)]-1$; skip if $[(DP)]=F$	$[(DP)]=F$
AD	1	1/2-3	$A_{CC} \leftarrow (A_{CC})+[(DP)]$; skip if Carry	Carry
ADS	1	1/2-3	A_{CC}, $C \leftarrow (A_{CC})+[(DP)]+(C)$; skip if Carry	Carry
ADC	1	1	A_{CC}, $C \leftarrow (A_{CC})+[(DP)]+(C)$	
DAA	1	1	$A_{CC} \leftarrow (A_{CC})+6$	
DAS	1	1	$A_{CC} \leftarrow (A_{CC})+10$	
EXL	1	1	$A_{CC} \leftarrow (A_{CC}) \forall [(DP)]$	
LI	1	1	$A_{CC} \leftarrow I_3 I_2 I_1 I_0$	
S	1	1	$[(DP)] \leftarrow (A_{CC})$	
L	1	1	$A_{CC} \leftarrow [(DP)]$	
LM	1	1	$A_{CC} \leftarrow [(DP)]$; $DP_H \leftarrow (DP_H) \forall 0M_1M_0$	
X	1	1	$(A_{CC}) \rightleftharpoons [(DP)]$	
XM	1	1	$(A_{CC}) \rightleftharpoons [(DP)]$; $DP_H \leftarrow (DP_H) \forall 0M_1M_0$	
XD	1	1/2-3	$(A_{CC}) \rightleftharpoons [(DP)]$; $DP_L \leftarrow (DP_L)-1$; skip if $(DP_L)=F$	$(DP_L)=F$
XMD	1	1/2-3	$(A_{CC}) \rightleftharpoons [(DP)]$; $DP_H \leftarrow (DP_H) \forall 0M_1M_0$; $DP_L \leftarrow (DP_L)-1$; skip if $(DP_L)=F$	$(DP_L)=F$
XI	1	1/2-3	$(A_{CC}) \rightleftharpoons [(DP)]$; $DP_L \leftarrow (DP_L)+1$; skip if $(DP_L)=0$	$(DP_L)=0$
XMI	1	1/2-3	$(A_{CC}) \rightleftharpoons [(DP)]$; $DP_H \leftarrow (DP_H) \forall 0M_1M_0$; $DP_L \leftarrow (DP_L)+1$; skip if $(DP_L)=0$	$(DP_L)=0$
LDI	2	2	$DP \leftarrow I_6-I_0$	
LDZ	1	1	$DP_H \leftarrow 0$; $DP_L \leftarrow I_3 I_2 I_1 I_0$	
DED	1	1/2-3	$DP_L \leftarrow (DP_L)-1$; skip if $(DP_L)=F$	$(DP_L)=F$
IND	1	1/2-3	$DP_L \leftarrow (DP_L)+1$; skip if $(DP_L)=0$	$(DP_L)=0$
TAL	1	1	$DP_L \leftarrow (A_{CC})$	
TLA	1	1	$A_{CC} \leftarrow (DP_L)$	

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MNEMONIC	BYTES	CYCLES	DESCRIPTION	CONDITION FOR SKIP
XHX	1	2	$(X) \rightleftharpoons (DP_H)$	
XLY	1	2	$(Y) \rightleftharpoons (DP_L)$	
THX	1	2	$X \leftarrow (DP_H)$	
TLY	1	2	$Y \leftarrow (DP_L)$	
XAZ	1	2	$(Z) \rightleftharpoons (A_{CC})$	
XAW	1	2	$(W) \rightleftharpoons (A_{CC})$	
TAZ	1	2	$Z \leftarrow (A_{CC})$	
TAW	1	2	$W \leftarrow (A_{CC})$	
XHR	1	2	$(R) \rightleftharpoons (DP_H)$	
XLS	1	2	$(S) \rightleftharpoons (DP_L)$	
SMB	1	1	$[(DP, B_1B_0)] \leftarrow 1$	
RMB	1	1	$[(DP, B_1B_0)] \leftarrow 0$	
TMB	1	1/2-3	skip if $[(DP, B_1B_0)]=1$	$[(DP, B_1B_0)]=1$
TAB	1	1/2-3	skip if $(A_{CC}(B_1B_0))=1$	$(A_{CC}(B_1B_0))=1$
CMB	1	1/2-3	skip if $(A_{CC}(B_1B_0))=[(DP, B_1B_0)]$	$(A_{CC}(B_1B_0))=[(DP, B_1B_0)]$
SFB	1	2	FLAG $(B_1B_0) \leftarrow 1$	
RFB	1	2	FLAG $(B_1B_0) \leftarrow 0$	
FBT	1	2/3-4	skip if (FLAG $(B_1B_0))=1$	(FLAG$(B_1B_0))=1$
FBF	1	2/3-4	skip if (FLAG $(B_1B_0))=0$	(FLAG$(B_1B_0))=0$
CM	1	1/2-3	skip if $(A_{CC})=[(DP)]$	$(A_{CC})=[(DP)]$
CI	2	2/3-4	skip if $(A_{CC})=I_3I_2I_1I_0$	$(A_{CC})=I_3I_2I_1I_0$
CLI	2	2/3-4	skip if $(DP_L)=I_3I_2I_1I_0$	$(DP_L)=I_3I_2I_1I_0$
TC	1	1/2-3	skip if (C)=1	(C)=1
TIT	1	1/2-3	skip if (INT F/F)=1; INT F/F←0	(INT F/F)=1
JCP	1	1	$PC_{5-0} \leftarrow P_5\text{-}P_0$	
JMP	2	2	$PC \leftarrow P_{10}\text{-}P_0$	
JPA	1	2	$PC_{5-0} \leftarrow A_3A_2A_1A_000$	
EI	1	1	INTE F F←1	
DI	1	1	INTE F F←0	
CZP	1	1	STACK←(PC) $PC \leftarrow 00000P_3P_2P_1P_000$	
CAL	2	2	STACK←(PC); $PC \leftarrow P_{10}\text{-}P_0$	
RT	1	2	PC←(STACK)	
RTS	1	3-4	PC←(STACK); PC←(PC)+1,2	Unconditional
STM	2	2	TM F F←0; TIMER$\leftarrow I_5\text{-}I_0$	
TTM	1	1/2-3	skip if (TM F/F)=1	(TM F/F)=1
SEB	1	2	PORT E $(B_1B_0) \leftarrow 1$	
REB	1	1	PORT E $(B_1B_0) \leftarrow 0$	
SPB	1	1	PORT $(DP_L, B_1B_0) \leftarrow 1$	
RPB	1	1	PORT $(DP_L, B_1B_0) \leftarrow 0$	
TPA	1	2/3-4	skip if (PORT A $(B_1B_0))=1$	(PORT A $(B_1B_0))=1$
TPB	1	1/2-3	skip if (PORT $(DL_L, B_1B_0))=1$	(PORT $(DP_L, B_1B_0)=1$
OE	1	2	PORT E$\leftarrow (A_{CC})$	
OP	1	1	PORT $(DP_L) \leftarrow (A_{CC})$	
OCD	2	2	PORT C,D$\leftarrow I_7\text{-}I_0$	
IA	2	2	$A_{CC} \leftarrow$(PORT A)	
IP	1	1	$A_{CC} \leftarrow$(PORT (DP_L))	
NOP	1	1	No Operation	

These instructions apply only to the μCOM-43.

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EVACHIP-43

DESCRIPTION

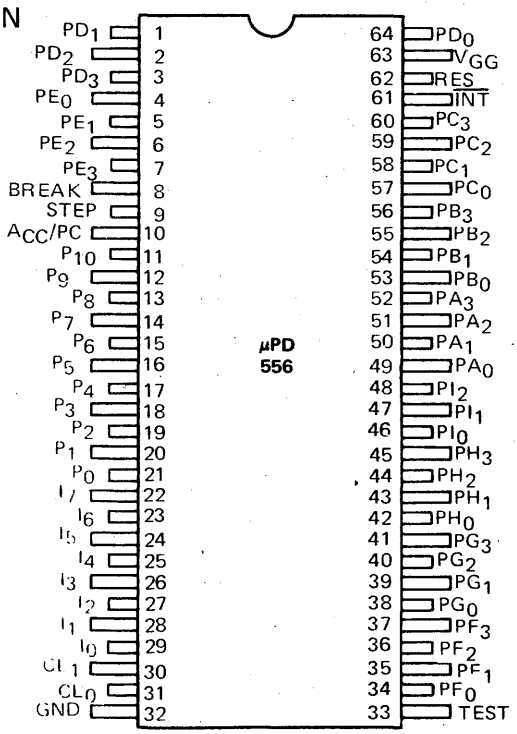
The μPD556 is an evaluation chip for the μCOM-43/44/45 single chip microcomputers. Designed to be used for both hardware and software debugging, the EVACHIP-43 is functionally equivalent to the μCOM-43, except that it does not contain on-chip ROM. Instead, it is able to address external memory. In addition, in order to facilitate debugging, the μPD556 is capable of displaying the contents of the internal accumulator and data pointer and of being single stepped.

When the μPD556 is being used to evaluate μCOM-44/45 designs, the external memory capacity should be restricted to that of the respective on-chip ROM and the instructions should be restricted to the 58 comprising the μCOM-44/45 instruction set.

FEATURES

- 4-bit Parallel Processor
- Full 80 Instruction Set of μCOM-43
- 10 μs Instruction Cycle
- Capable of addressing 2K x 8-bits of external program memory
- Single step capability
- Full Functionality of μCOM-43
- Single supply: -10V PMOS Technology
- Available in a 64-pin Ceramic Quad-in-Line Package

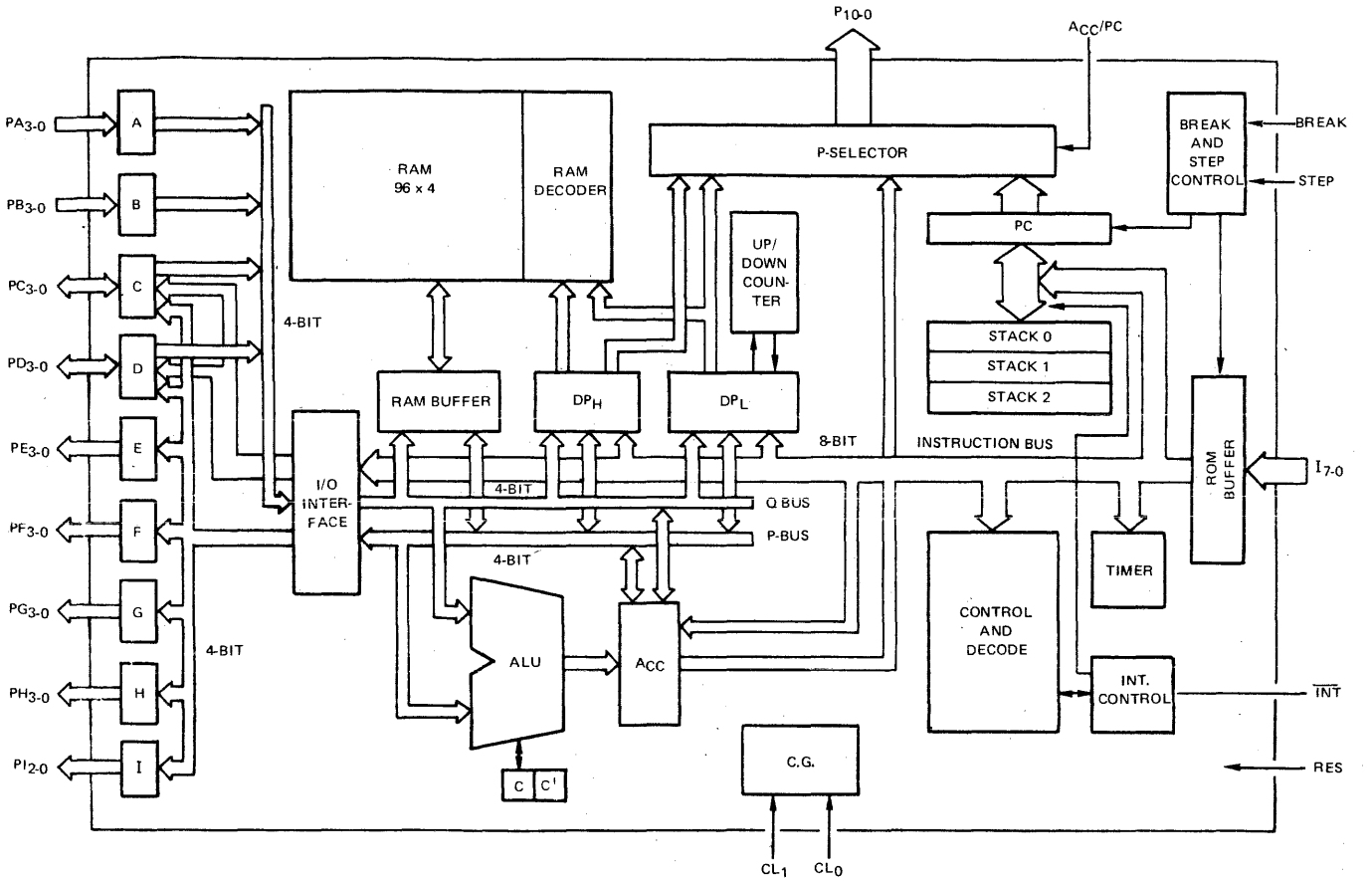
PIN CONFIGURATION



PIN NAMES

PF_0 – PF_3	Output Port F
PG_0 – PG_3	Output Port G
PH_0 – PH_3	Output Port H
PI_0 – PI_2	Output Port I
PA_0 – PA_3	Input Port A
PB_0 – PB_3	Input Port B
PC_0 – PC_3	Input/Output Port C
$\overline{INT}$	Interrupt Input
RES	Reset
PD_0 – PD_3	Input/Output Port D
PE_0 – PE_3	Output Port E
BREAK	Hold Input
STEP	Single Step Input
A_{CC}/PC	Display A_{CC}/PC Input
P_0 – P_{10}	PC Output
I_0 – I_7	Instruction Input
CL_0 – CL_1	External Clock Source
TEST	Tied to V_{SS} (GND)

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ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	−10°C to +70°C
Storage Temperature	−40°C to +125°C
Supply Voltage V_{GG}	−15 to +0.3 Volts
All Input Voltages	−15 to +0.3 Volts
All Output Voltages	−15 to +0.3 Volts
Output Current	−4 mA ①

Note: ① All output pins.

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

CAPACITANCE

T_a = 25°C

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input Capacitance	C_I			15	pf	f = 1 MHz
Output Capacitance	C_O			15	pf	
Input/Output Capacitance	C_{IO}			15	pf	

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DC CHARACTERISTICS ①

$T_a = -10$ to $+70°C$; $V_{GG} = -10V \pm 10\%$

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input High Voltage	V_{IH}	0		-2.0	V	Port A to D, I_7 to I_0, BREAK, STEP, $\overline{INT}$, RES, and A_{CC}/PC
Input Low Voltage	V_{IL}	-4.3		V_{GG}	V	Port A to D, I_7 to I_0, BREAK, STEP, $\overline{INT}$, RES, and A_{CC}/PC
Clock High Voltage	V_{OH}	0		-0.8	V	CL_0 Input
Clock Low Voltage	V_{OL}	-6.0		V_{GG}	V	CL_0 Input
Input Leakage Current High	I_{LIH}			+10	μA	Port A and B, I_7 to I_0 $\overline{INT}$, RES, BREAK, STEP
				+30	μA	A_{CC}/PC, $V_I = -1V$ Port C and D, $V_I = -1V$
Input Leakage Current Low	I_{LIL}			-10	μA	Port A and B, I_7 to I_0 $\overline{INT}$, RES, BREAK, STEP
				-30	μA	A_{CC}/PC, $V_I = -11V$ Port C and D, $V_I = -11V$
Clock Input Leakage High	I_{LOH}			+200	μA	CL_0 Input, $V_{OH} = 0V$
Clock Input Leakage Low	I_{LOL}			-200	μA	CL_0 Input, $V_{OL} = -11V$
Output High Voltage	V_{OH1}			-1.0	V	Port C to I, P_{10} to P_0 $I_{OH} = -1.0$ mA
	V_{OH2}			-2.3	V	Port C to I, P_{10} to P_0 $I_{OH} = -3.3$ mA
Output Leakage Current Low	I_{LOL}			-30	μA	Port C to I, P_{10} to P_0 $V_O = -11V$
Supply Current	I_{GG}		-30	-50	mA	

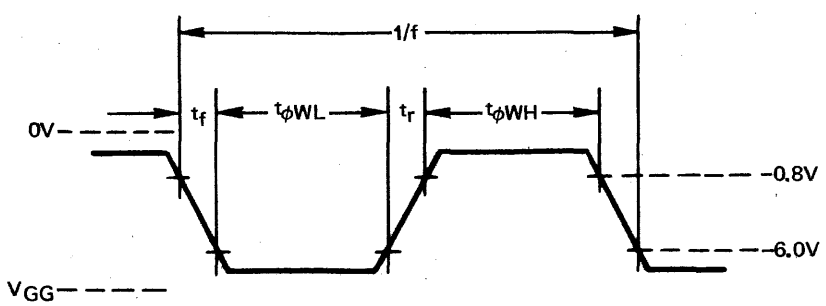
Note: ① Relative to $V_{SS} = 0V$

AC CHARACTERISTICS

$T_a = -10°C$ to $+70°C$; $V_{GG} = -10V \pm 10\%$

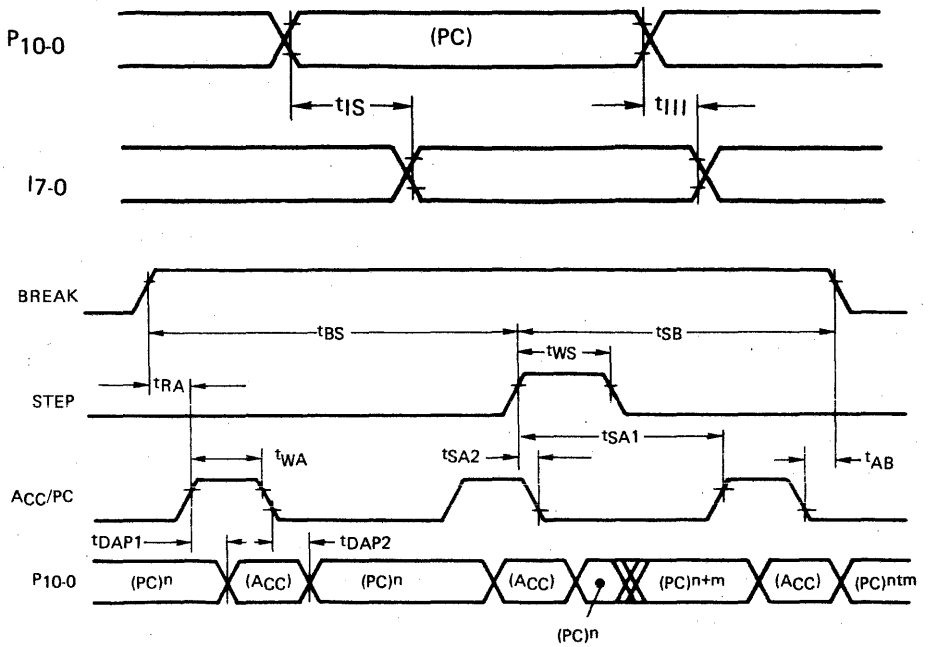
PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Frequency	f	150		440	KHz	
Clock Rise and Fall Times	t_r, t_f	0		0.3	μs	
Clock Pulse Width High	$t\phi WH$	0.5		5.6	μs	
Clock Pulse Width Low	$t\phi WL$	0.5		5.6	μs	
Input Setup Time	t_{IS}			5	μs	
Input Hold Time	t_{IH}	0			μs	
BREAK to STEP Interval	t_{BS}	80			tcy	
STEP to RUN Interval	t_{SB}	80			tcy	
STEP Pulse Width	t_{WS}	12			tcy	
BREAK to A_{CC} Interval	t_{BA}	80			tcy	
A_{CC}/PC Pulse Width	t_{WA}	12			tcy	
STEP to A_{CC} Interval	t_{SA1}	80			tcy	
PC to STEP Overlap	t_{SA2}			2	tcy	
PC to RUN Interval	t_{AB}	0			μs	
A_{CC}/PC → P_{10}-P_0 Delay	t_{DAP1}			6	tcy	
	t_{DAP2}			6	tcy	

CLOCK WAVEFORM

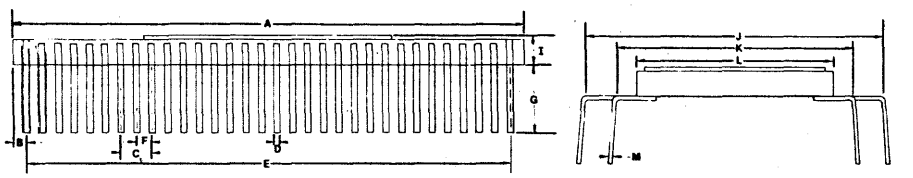


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TIMING WAVEFORM



PACKAGE OUTLINE μPD556B



ITEM	MILLIMETERS	INCHES
A	41.5	1.634 MAX
B	1.05	0.042
C	2.54	0.1
D	0.5 ± 0.1	0.2 ± 0.004
E	39.4	1.55
F	1.27	0.05
G	5.4 MIN	0.21 MIN
I	2.35 MAX	0.13 MAX
J	24.13	0.95
K	19.05	0.75
L	15.9	0.626
M	0.25 ± 0.05	0.01 ± 0.002

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8-BIT N-CHANNEL MICROPROCESSOR COMPLETELY Z80™ COMPATIBLE

DESCRIPTION

The μPD780 and μPD780-1 processors are single chip microprocessors developed from third generation technology. Their increased computational power produces higher system through-put and more efficient memory utilization, surpassing that of any second generation microprocessor. The single voltage requirement of the μPD780 and μPD780-1 processors makes it easy to implement them into a system. All output signals are fully decoded and timed to either standard memory or peripheral circuits. An N-channel, ion implanted, silicon gate MOS process is utilized in implementing the circuit.

The block diagram shows the functions of the processor and details the internal register structure. The structure contains 26 bytes of Read/Write (R/W) memory available to the programmer. Included in the registers are two sets of six general purpose registers, which may be used as 8-bit registers individually, or as 16-bit register pairs. Also included are two sets of accumulator and flag registers.

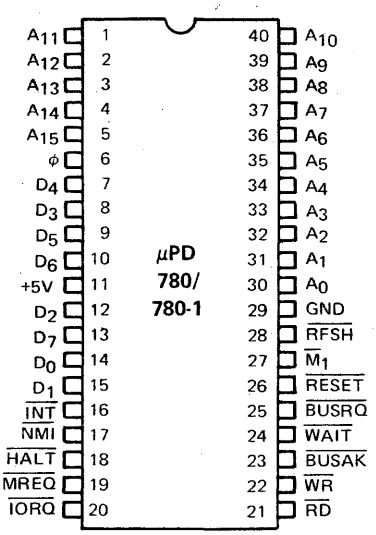
Through a group of exchange instructions the programmer has access to either set of main or alternate registers. The alternate register permits foreground/background mode of operation, or may be used for fast interrupt response. A 16-bit stack pointer is also included in each processor, simplifying implementation of multiple level interrupts, permitting unlimited subroutine nesting, and simplifying many types of data handling.

The two 16-bit index registers simplify implementation of relocatable code and manipulation of tabular data. The Refresh register will automatically refresh external dynamic memories. A powerful interrupt response mode will use the I register to form the upper 8-bits of a pointer to an interrupt service address table, while the interrupting apparatus supplies the lower 8-bits of the pointer. An indirect call will then be made to service this address.

FEATURES

- Single Chip, N-Channel Silicon Gate Processor
- 158 Instructions — Including all 78 of the 8080A Instructions, Permitting Total Software Compatibility
- New 4-, 8-, and 16-Bit Operations Featuring Useful Addressing Modes such as Indexed, Bit and Relative
- 17 Internal Registers
- Three Modes of Rapid Interrupt Response, and One Non-Maskable Interrupt
- Directly Connects Standard Speed Dynamic or Static Memories, with Minimum Support Circuitry
- Single-Phase +5 Volt Clock and 5 VDC Supply
- TTL Compatibility
- Automatic Dynamic RAM Refresh Circuitry
- Available in Plastic Package

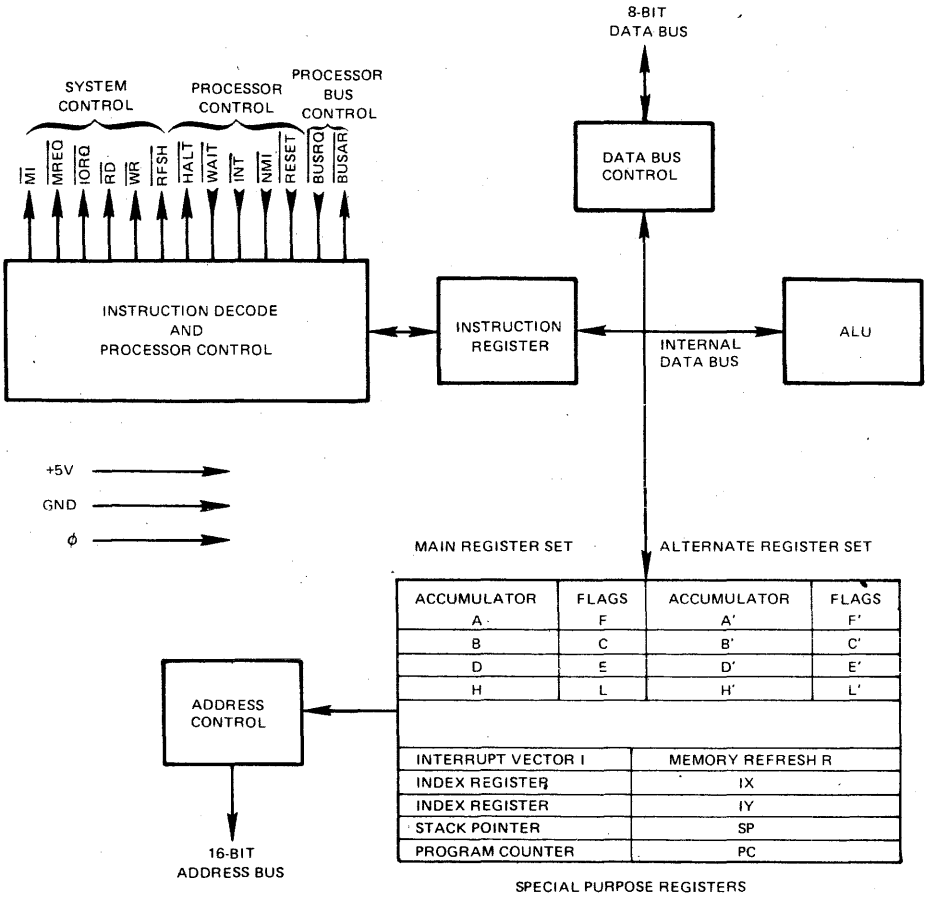
PIN CONFIGURATION



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BLOCK DIAGRAM



PIN IDENTIFICATION

PIN NO.	PIN SYMBOL	PIN NAME	FUNCTION
1-5, 30-40	A_0-A_{15}	Address Bus	3-State Output, active high. Pins A_0-A_{15} constitute a 16-bit address bus, which provides the address for memory and I/O device data exchanges. Memory capacity 65,536 bytes. A_0-A_7 is also needed as refresh cycle.
7-10, 12-15	D_0-D_7	Data Bus	3-State input/output, active high. Pins D_0-D_7 compose an 8-bit, bidirectional data bus, used for data exchanges with memory and I/O devices.
27	$\overline{M_1}$	Machine Cycle One	Output, active low. $\overline{M_1}$ indicates that the machine cycle in operation is the op code fetch cycle of an instruction execution.
19	$\overline{MREQ}$	Memory Request	3-State output, active low. $\overline{MREQ}$ indicates that a valid address for a memory read or write operation is held in the address.
20	$\overline{IORQ}$	Input/Output Request	3-State output, active low. The I/O request signal indicates that the lower half of the address bus holds a valid address for an I/O read or write operation. The $\overline{IORQ}$ signal is also used to acknowledge an interrupt command, indicating that an interrupt response vector can be placed on the data bus.
21	$\overline{RD}$	Memory Read	3-State output, active low. $\overline{RD}$ indicates that the processor is requesting data from memory or an I/O device. The memory or I/O device being addressed should use this signal to gate data onto the data bus.

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PIN IDENTIFICATION (CONT.)

PIN NO.	PIN SYMBOL	PIN NAME	FUNCTION
22	$\overline{WR}$	Memory Write	3-State output, active low. The memory write signal indicates that the processor data bus is holding valid data to be stored in the addressed, memory or I/O device.
28	$\overline{RFSH}$	Refresh	Output, active low. $\overline{RFSH}$ indicates that a refresh address for dynamic memories is being held in the lower 7-bits of the address bus. The $\overline{MREQ}$ signal should be used to implement a refresh read to all dynamic memories.
18	$\overline{HALT}$	Halt State	Output, active low. $\overline{HALT}$ indicates that the processor has executed a HALT software instruction, and will not resume operation until either a non-maskable or a maskable (with mask enabled) interrupt has been implemented. The processor will execute NOP's while halted, to maintain memory refresh activity.
24	$\overline{WAIT}$	Wait	Input, active low. $\overline{WAIT}$ indicates to the processor that the memory or I/O devices being addressed are not ready for a data transfer. As long as this signal is active, the processor will reenter wait states.
16	$\overline{INT}$	Interrupt Request	Input, active low. The $\overline{INT}$ signal is produced by I/O devices. The request will be honored upon completion of the current instruction, if the interrupt enable flip-flop (IFF) is enabled by the internal software. There are three modes of interrupt response. Mode 0 is identical to 8080 interrupt response mode. The Mode 1 response is a restart location at 0038_H. Mode 2 is for simple vectoring to an interrupt service routine anywhere in memory.
17	$\overline{NMI}$	Non-Maskable Interrupt	Input, active low. The non-maskable interrupt has a higher priority than $\overline{INT}$. It is always acknowledged at the end of the current instruction, regardless of the status of the interrupt enable flip-flop. When the $\overline{NMI}$ signal is given, the μPD780 processor automatically restarts to location 0066_H.
26	$\overline{RESET}$	Reset	Input, active low. The $\overline{RESET}$ signal causes the processor to reset the interrupt enable flip-flop (IFF), clear PC and I and R registers, and set interrupt to 8080A mode. During the reset time, the address bus and data bus go to a state of high impedance, and all control output signals become inactive, after which processing continues at 0000H.
25	$\overline{BUSRQ}$	Bus Request	Input, active low. $\overline{BUSRQ}$ has a higher priority than $\overline{NMI}$, and is always honored at the end of the current machine cycle. It is used to allow other devices to take control over the processor address bus, data bus signals; by requesting that they go to a state of high impedance.
23	$\overline{BUSAK}$	Bus Acknowledge	Output, active low. $\overline{BUSAK}$ is used to inform the requesting device that the processor address bus, data bus and 3-state control bus signals have entered a state of high impedance, and the external device can now take control of these signals.

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ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	0°C to +70°C
Storage Temperature	-65°C to +150°C
Voltage on any Pin	-0.3 to +7 Volts ①
Power Dissipation	1.5W

Note: ① With Respect to Ground.

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

DC CHARACTERISTICS

T_a = 0°C to +70°C; V_{CC} = +5V ± 5% unless otherwise specified.

PARAMETER		SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Clock Input Low Voltage		V_{ILC}	-0.3		0.45	V	
Clock Input High Voltage		V_{IHC}	V_{cc}-0.2		V_{cc}	V	
Input Low Voltage		V_{IL}	-0.3		0.8	V	
Input High Voltage		V_{IH}	2.0		V_{cc}	V	
Output Low Voltage		V_{OL}	*		0.4	V	I_{OL} = 1.8 mA
Output High Voltage		V_{OH}	2.4			V	I_{OH} = -250 μA
Power Supply Current	μPD780	I_{CC}			150	mA	t_c = 400 ns
	μPD780-1	I_{CC}		90	200	mA	t_c = 250 ns
Input Leakage Current		I_{LI}			10	μA	V_{IN} = 0 to V_{cc}
Tri-State Output Leakage Current in Float		I_{LOH}			10	μA	V_{OUT} = 2.4 to V_{cc}
Tri-State Output Leakage Current in Float		I_{LOL}			-10	μA	V_{OUT} = 0.4 V
Data Bus Leakage Current in Input Mode		I_{LD}			±10	μA	$0 \leq V_{IN} \leq V_{cc}$

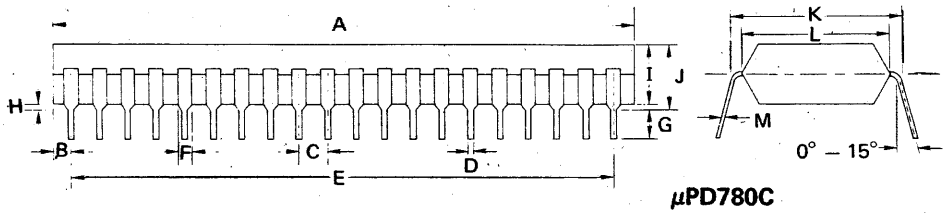
CAPACITANCE

T_a = 25°C

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Clock Capacitance	C_ϕ			35	pF	f_c = 1 MHz
Input Capacitance	C_{IN}			5	pF	Unmeasured Pins
Output Capacitance	C_{OUT}			10	pF	Returned to Ground

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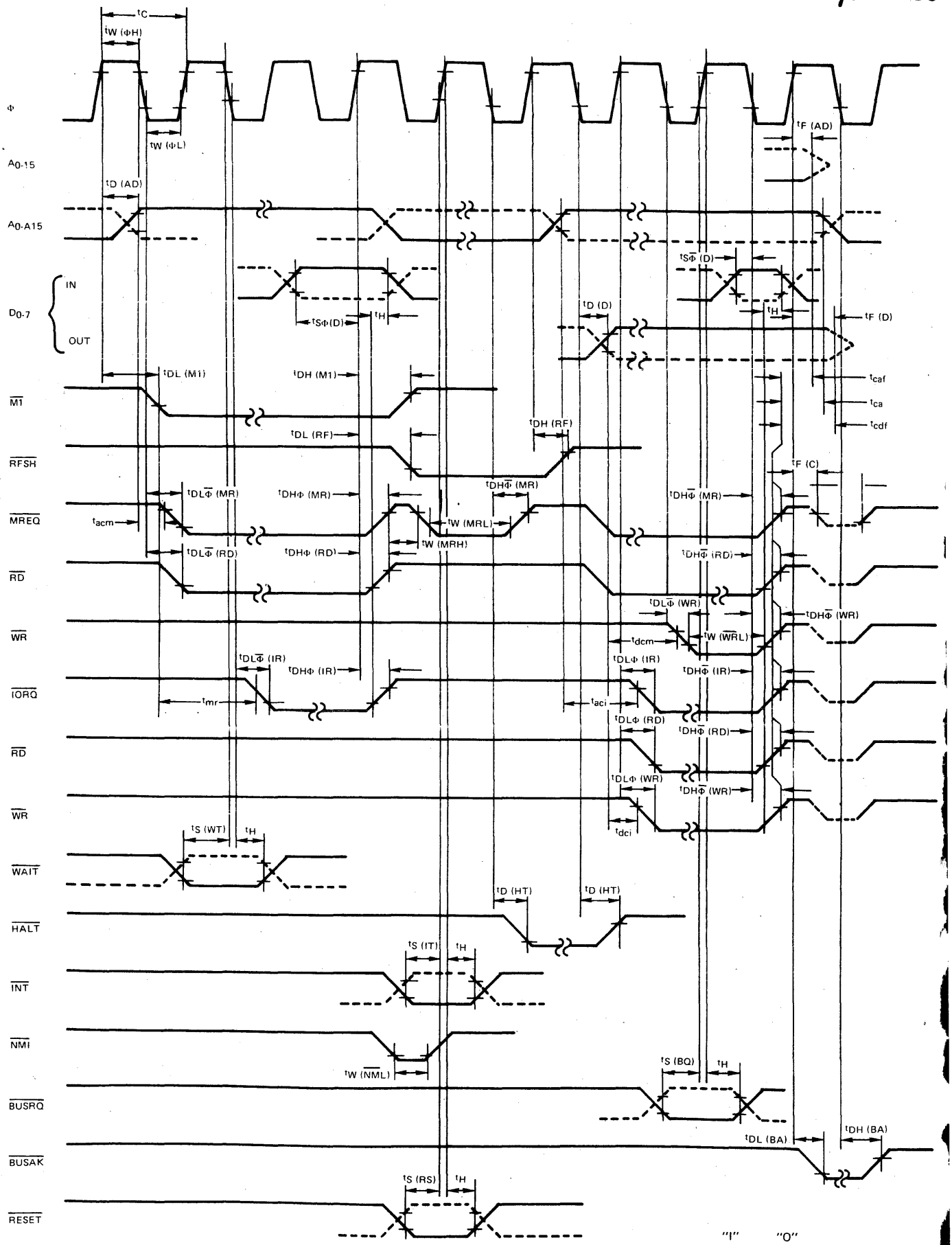
PACKAGE OUTLINES
μPD780C
μPD780C-1



μPD780C
μPD780C-1
(Plastic)

ITEM	MILLIMETERS	INCHES
A	51.5 MAX	2.028 MAX
B	1.62	0.064
C	2.54 ± 0.1	0.10 ± 0.004
D	0.5 ± 0.1	0.019 ± 0.004
E	48.26	1.9
F	1.2 MIN	0.047 MIN
G	2.54 MIN	0.10 MIN
H	0.5 MIN	0.019 MIN
I	5.22 MAX	0.206 MAX
J	5.72 MAX	0.225 MAX
K	15.24	0.600
L	13.2	0.520
M	$0.25^{+0.1}_{-0.05}$	$0.010^{+0.004}_{-0.002}$

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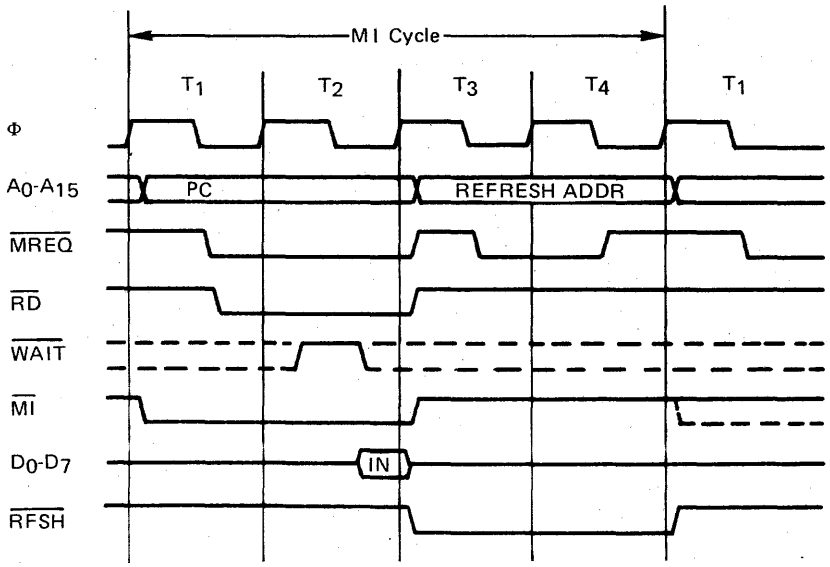
	"I"	"O"
CLOCK	4.2V	0.8V
OUTPUT	2.0V	0.8V
INPUT	2.0V	0.8V
FLOAT	ΔV	±0.5V

Note: ① Timing measurements are made at the following voltages unless otherwise specified:

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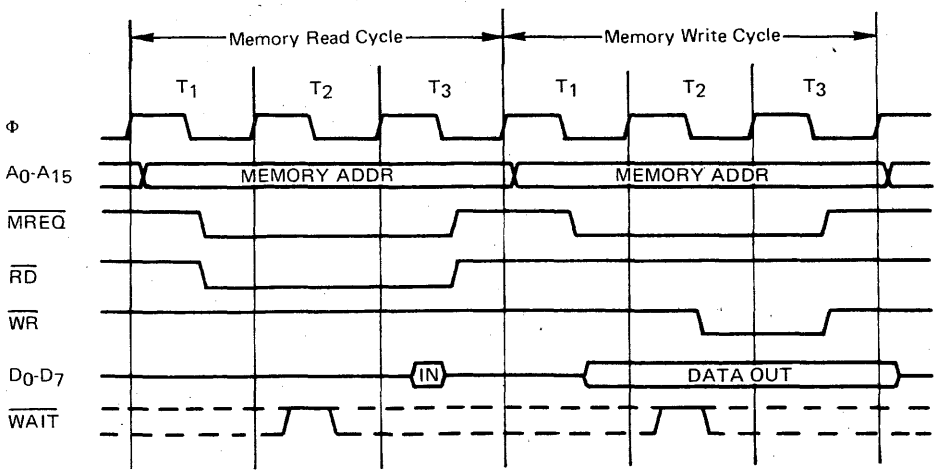
Instruction Op Code Fetch

The contents of the program counter (PC) are placed on the address bus at the start of the cycle. $\overline{MREQ}$ goes active one-half clock cycle later, and the falling edge of this signal can be used directly as a chip enable to dynamic memories. The memory data should be enabled onto the processor data bus when $\overline{RD}$ goes active. The processor takes data with the rising edge of the clock state T_3. The processor internally decodes and executes the instruction, while clock states T_3 and T_4 of the fetch cycle are used to refresh dynamic memories. The refresh control signal $\overline{RFSH}$ indicates that a refresh read should be done to all dynamic memories.



Memory Read or Write Cycles

This diagram illustrates the timing of memory read or write cycles other than an op code fetch (M_1 cycle). The function of the $\overline{MREQ}$ and $\overline{RD}$ signals is exactly the same as in the op code fetch cycle. When a memory write cycle is implemented, the $\overline{MREQ}$ becomes active and is used directly as a chip enable for dynamic memories, when the address bus is stable. The $\overline{WR}$ line is used directly as a R/W pulse to any type of semiconductor memory, and is active when data on the data bus is stable.

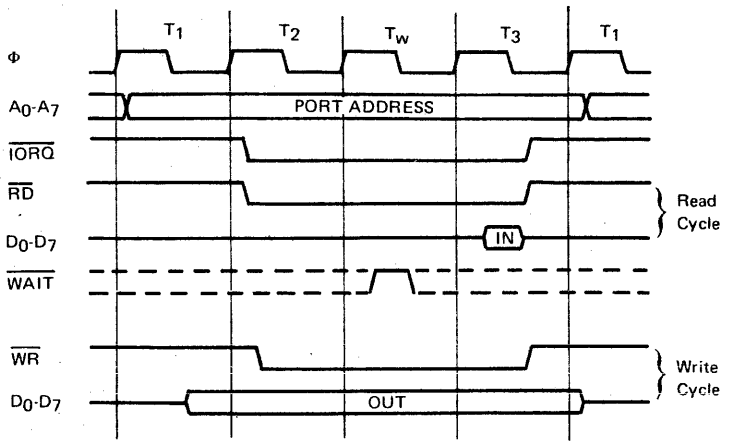


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TIMING WAVEFORMS (CONT.)

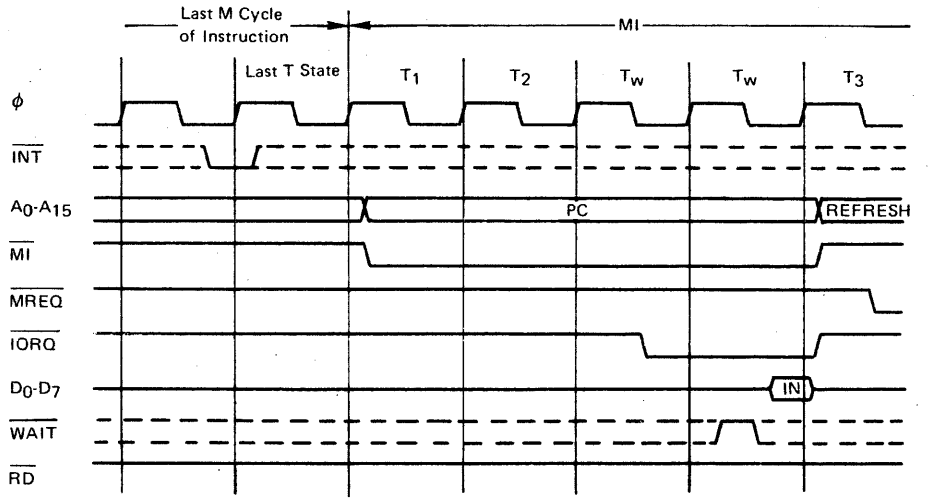
Input or Output Cycles

This illustrates the timing for an I/O read or I/O write operation. A single wait-state (T_W) is automatically inserted in I/O operations to allow sufficient time for an I/O port to decode its address and activate the $\overline{WAIT}$ line, if necessary.



Interrupt Request/Acknowledge Cycle

The processor samples the interrupt signal with the rising edge of the last clock at the end of any instruction. A special M_1 cycle is started when an interrupt is accepted. During the M_1 cycle, the $\overline{IORQ}$ (instead of $\overline{MREQ}$) signal becomes active, indicating that the interrupting device can put an 8-bit vector on the data bus. Two wait states (T_W) are automatically added to this cycle. This makes it easy to implement a ripple priority interrupt scheme.



INSTRUCTION SET

The following summary shows the assembly language mnemonic and the symbolic operation performed by the instructions of the μPD780 and μPD780-1 processors. The instructions are divided into 16 categories:

Miscellaneous Group	8-Bit Loads
Rotates and Shifts	16-Bit Loads
Bit Set, Reset and Test	Exchanges
Input and Output	Memory Block Moves
Jumps	Memory Block Searches
Calls	8-Bit Arithmetic and Logic
Restarts	16-Bit Arithmetic
Returns	General Purpose Accumulator and Flag Operations

The addressing Modes include combinations of the following:

Indexed	Immediate
Register	Immediate Extended
Implied	Modified Page Zero
Register Indirect	Relative
Bit	Extended

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INSTRUCTION SET TABLE

MNEMONIC	SYMBOLIC OPERATION	DESCRIPTION	NO. BYTES	NO. T STATES	FLAGS C	Z	P/V	S	N	H	OP CODE 76 543 210
ADC HL, ss	HL ← HL + ss + CY	Add with carry reg. pair ss to HL	1	11	↕	↕	V	↕	0	X	11 101 101 Ⓐ 01 ss1 010
ADC A, r	A ← A + r + CY	Add with carry Reg. r to ACC	1	4	↕	↕	V	↕	0	↕	10 001 rrr Ⓑ
ADC A,n	A ← A + n + CY	Add with carry value n to ACC		7	↕	↕	V	↕	0	↕	11 001 110 nn nnn nnn
ADC A, (HL)	A ← A + (HL) + CY	Add with carry loc. (HL) to ACC		7	↕	↕	V	↕	0	↕	10 001 110
ADC A, (IX + d)	A ← A + (IX + d) + CY	Add with carry loc. (IX + d) to ACC		19	↕	↕	V	↕	0	↕	11 011 101 10 001 110 dd ddd ddd
ADC A, (IY + d)	A ← A + (IY + d) + CY	Add with carry loc. (IY + d) to ACC		19	↕	↕	V	↕	0	↕	11 111 101 10 001 110 dd ddd ddd
ADD A, n	A ← A + n	Add value n to ACC	2	7	↕	↕	V	↕	0	↕	11 000 110 nn nnn nnn
ADD A, r	A ← A + r	Add Reg. r to ACC	1	4	↕	↕	V	↕	0	↕	10 000 rrr Ⓑ
ADD A, (HL)	A ← A + (HL)	Add location (HL) to ACC	1	7	↕	↕	V	↕	0	↕	10 000 110
ADD A, (IX + d)	A ← A + (IX + d)	Add location (IX + d) to ACC	3	19	↕	↕	V	↕	0	↕	11 011 101 10 000 110 dd ddd ddd
ADD A, (IY + d)	A ← A + (IY + d)	Add location (IY + d) to ACC	3	19	↕	↕	V	↕	0	↕	11 111 101 10 000 110 dd ddd ddd
ADD HL, ss	HL ← HL + ss	Add Reg. pair ss to HL	1	11	↕	•	•	•	0	X	00 ss 1 001 Ⓐ
ADD IX, pp	IX ← IX + pp	Add Reg. pair pp to IX	2	15	↕	•	•	•	0	X	11 011 101 Ⓒ 00 pp1 001
ADD IY, rr	IY ← IY + rr	Add Reg. pair rr to IY	2	15	↕	•	•	•	0	X	11 111 101 Ⓓ 00 rr1 001
AND r	A ← A∧r	Logical 'AND' of Reg. r ∧ ACC		4	0	↕	P	↕	0	↕	10 100 rrr Ⓑ
AND n	A ← A∧n	Logical 'AND' of value n ∧ ACC		7	0	↕	P	↕	0	↕	11 100 110 nn nnn nnn
AND (HL)	A ← A∧(HL)	Logical 'AND' of loc. (HL) ∧ ACC		7	0	↕	P	↕	0	↕	10 100 110
AND (IX + d)	A ← A∧(IX + d)	Logical 'AND' of loc. (IX + d) ∧ ACC		19	0	↕	P	↕	0	↕	11 011 101 10 100 110 dd ddd ddd
AND (IY + d)	A ← A∧(IY + d)	Logical 'AND' of loc. (IY + d) ∧ ACC		19	0	↕	P	↕	0	↕	11 111 101 10 100 110 dd ddd ddd
BIT b, (HL)	Z ← $\overline{(HL)}_b$	Test BIT b of location (HL)	2	12	•	↕	X	X	0	1	11 001 011 Ⓔ 01 bbb 110
BIT b, (IX + d)	Z ← $\overline{(IX + d)}_b$	Test BIT b at location (IX + d)	4	20	•	↕	X	X	0	1	11 011 101 Ⓔ 11 001 011 dd ddd ddd 01 bbb 110
BIT b, (IY + d)	Z ← $\overline{(IY + d)}_b$	Test BIT b at location (IY + d)	4	20	•	↕	X	X	0	1	11 111 101 Ⓔ 11 001 011 dd ddd ddd 01 bbb 110
BIT b, r	Z ← $\overline{r}_b$	Test BIT of Reg. r	2	8	•	↕	X	X	0	1	11 001 011 Ⓑ Ⓔ 01 bbb rrr
CALL cc, nn	If condition cc false continue, else same as CALL nn	Call subroutine at location nn if condition cc is true	3	10	•	•	•	•	•	•	11 ←cc→ 100 Ⓗ nn nnn nnn nn nnn nnn
CALL nn	(SP – 1) ← PC_H (SP – 2) ← PC_L PC ← nn	Unconditional call subroutine at location nn	3	17	•	•	•	•	•	•	11 001 101 nn nnn nnn nn nnn nnn
CCF	CY ← CY	Complement carry flag	1	4	↕	•	•	•	0	X	00 111 111
CP r	A – r	Compare Reg. r with ACC		4	↕	↕	V	↕	1	↕	10 111 rrr Ⓑ
CP n	A – n	Compare value n with ACC		7	↕	↕	V	↕	1	↕	11 111 110 nn nnn nnn
CP (HL)	A – (HL)	Compare loc. (HL) with ACC		7	↕	↕	V	↕	1	↕	10 111 110
CP (IX + d)	A – (IX + d)	Compare loc. (IX + d) with ACC		19	↕	↕	V	↕	1	↕	11 011 101 10 111 110 dd ddd ddd
CP (IY + d)		Compare loc. (IY + d) with ACC		19	↕	↕	V	↕	1	↕	11 111 101 10 111 110 dd ddd ddd
CPD	A – (HL) HL ← HL – 1 BC ← BC – 1	Compare location (HL) and ACC, decrement HL and BC	2	16	•	↕②	↕①	↕	1	↕	11 101 101 10 101 001
CPDR	A – (HL) HL ← HL – 1 BC ← BC – 1 until A = (HL) or BC = 0	Compare location (HL) and ACC, decrement HL and BC, repeat until BC = 0	2	21 if BC = 0 and A ≠ (HL) 16 if BC = 0 or A = (HL)	•	↕②	↕①	↕	1	↕	11 101 101 10 111 001

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MNEMONIC	SYMBOLIC OPERATION	DESCRIPTION	NO. BYTES	NO. T STATES	FLAGS C	Z	P/V	S	N	H	OP CODE 76 543 210
CPI	A – (HL) HL ← HL + 1 BC ← BC – 1	Compare location (HL) and ACC, increment HL and decrement BC	2	16	•	‡②	‡①	‡	1	‡	11 101 101 10 100 001
CPIR	A – (HL) HL ← HL + 1 BC ← BC – 1 until A = (HL) or BC = 0	Compare location (HL) and ACC, increment HL, decrement BC Repeat until BC = C	2	21 if BC = 0 and A ≠ (HL) 16 if BC = 0 or A = (HL)	•	‡②	‡①	‡	1	‡	11 101 101 10 110 001
CPL	A ← A	Complement ACC (1's comp.)	1	4	•	•	•	•	1	1	00 101 111
DAA		Decimal adjust ACC	1	4	‡	‡	P	‡	•	‡	00 100 111
DEC r	r ← r – 1	Decrement Reg. r		4	•	‡	V	‡	1	‡	00 rrr 101Ⓑ
DEC (HL)	(HL) ← (HL) – 1	Decrement loc. (HL)		11	•	‡	V	‡	1	‡	00 110 101
DEC (IX + d)	(IX + d) ← (IX + d) – 1	Decrement loc. (IX + d)		23	•	‡	V	‡	1	‡	11 011 101 00 110 101 dd ddd ddd
DEC (IY + d)	(IY + d) ← (IY + d) – 1	Decrement loc. (IY + d)		23	•	‡	V	‡	1	‡	11 111 101 00 110 101 dd ddd ddd
DEC iX	IX ← IX – 1	Decrement IX	2	10	•	•	•	•	•	•	11 011 101 00 101 011
DEC IY	IY ← IY – 1	Decrement IY	2	10	•	•	•	•	•	•	11 111 101 00 101 011
DEC ss	ss ← ss – 1	Decrement Reg. pair ss	1	6	•	•	•	•	•	•	00 ss1 011Ⓐ
DI	IFF ← 0	Disable interrupts	1	4	•	•	•	•	•	•	11 110 011
DJNZ, e	B ← B – 1 if B = 0 continue if B ≠ 0 PC ← PC + e	Decrement B and jump relative if B = 0	2	8	•	•	•	•	•	•	00 010 000 ◄—e-2—►
EI	IFF ← 1	Enable interrupts	1	4	•	•	•	•	•	•	11 111 011
EX (SP), HL	H ↔ (SP + 1) L ↔ (SP)	Exchange the location (SP) and HL	1	19	•	•	•	•	•	•	11 100 011
EX (SP), IX	IX_H ↔ (SP + 1) IX_L ↔ (SP)	Exchange the location (SP) and IX	2	23	•	•	•	•	•	•	11 011 101 11 100 011
EX (SP), IY	IY_H ↔ (SP + 1) IY_L ↔ (SP)	Exchange the location (SP) and IY	2	23	•	•	•	•	•	•	11 111 101 11 100 011
EX AF, AF'	AF ↔ AF'	Exchange the contents of AF, AF'	1	4	•	•	•	•	•	•	00 001 000
EX DE, HL	DE ↔ HL	Exchange the contents of DE and HL	1	4	•	•	•	•	•	•	11 101 011
EXX	BC ↔ BC' DE ↔ DE' HL ↔ HL'	Exchange the contents of BC, DE, HL with contents of BC', DE', HL', respectively	1	4	•	•	•	•	•	•	11 011 001
HALT	Processor Halted	HALT (wait for interrupt or reset)	1	4	•	•	•	•	•	•	01 110 110
IM 0		Set Interrupt mode 0	2	8	•	•	•	•	•	•	11 101 101 01 000 110
IM 1		Set Interrupt mode 1	2	8	•	•	•	•	•	•	11 101 101 01 010 110
IM 2		Set Interrupt mode 2	2	8	•	•	•	•	•	•	11 101 101 01 011 110
IN A, (n)	A ← (n)	Load ACC with input from device n	2	11	•	•	•	•	•	•	11 011 011 nn nnn nnn
IN r, (C)	r ← (C)	Load Reg. r with input from device (C)	2	12	•	‡	P	‡	0	‡	11 101 101Ⓘ 01 rrr 000
INC (HL)	(HL) ← (HL) + 1	Increment location (HL)	1	11	•	‡	V	‡	0	‡	00 110 100
INC IX	IX ← IX + 1	Increment IX	2	10	•	•	•	•	•	•	11 011 101 00 100 011
INC (IX + d)	(IX + d) ← (IX + d) + 1	Increment location (IX + d)	3	23	•	‡	V	‡	0	‡	11 011 101 00 110 100 dd ddd ddd
INC IY	IY ← IY + 1	Increment IY	2	10	•	•	•	•	•	•	11 111 101 00 100 011
INC (IY + d)	(IY + d) ← (IY + d) + 1	Increment location (IY + d)	3	23	•	‡	V	‡	0	‡	11 111 101 00 110 100 dd ddd ddd
INC r	r ← r + 1	Increment Reg. r	1	4	•	‡	V	‡	0	‡	00 rrr 100Ⓑ
INC ss	ss ← ss + 1	Increment Reg. pair ss	1	6	•	•	•	•	•	•	00 ss0 011Ⓐ
IND	(HL) ← (C) B ← B – 1 HL ← HL – 1	Load location (HL) with input from port (C), decrement HL and B	2	16	•	‡③	X	X	1	X	11 101 101 10 101 010

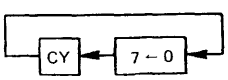
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MNEMONIC	SYMBOLIC OPERATION	DESCRIPTION	NO. BYTES	NO. T STATES	FLAGS C	Z	P/V	S	N	H	OP CODE 76 543 210
INDR	(HL) ← (C) B ← B – 1 HL ← HL – 1 until B = 0	Load location (HL) with input from port (C), decrement HL and decrement B, repeat until B = 0	2	21	•	1	X	X	1	X	11 101 101 10 111 010
INI	(HL) ← (C) B ← B – 1 HL ← HL + 1	Load location (HL) with input from port (C); and increment HL and decrement B	2	16	•	③	X	X	1	X	11 101 101 10 100 010
INIR	(HL) ← (C) B ← B – 1 HL ← HL + 1 until B = 0	Load location (HL) with input from port (C), increment HL and decrement B, repeat until B = 0	2	21	•	1	X	X	1	X	11 101 101 10 110 010
JP (HL)	PC ← HL	Unconditional jump to (HL)	1	4	•	•	•	•	•	•	11 101 001
JP (IX)	PC ← IX	Unconditional jump to (IX)	2	8	•	•	•	•	•	•	11 011 101 11 101 001
JP (IY)	PC ← IY	Unconditional jump to (IY)	2	8	•	•	•	•	•	•	11 111 101 11 101 001
JP cc, nn	If cc true PC ← nn else-continue	Jump to location nn if condition cc is true	3	10	•	•	•	•	•	•	11 ←cc→ 010 Ⓗ nn nnn nnn nn nnn nnn
JP nn	PC ← nn	Unconditional jump to location nn	3	10	•	•	•	•	•	•	11 000 011 nn nnn nnn nn nnn nnn
JR C, e	If C = 0 continue If C = 1 PC ← PC + e	Jump relative to PC + e, if carry = 1	2	7 if condition met. 12, if not	•	•	•	•	•	•	00 111 000 ←e-2→
JR e	PC ← PC + e	Unconditional jump relative to PC + e	2	12	•	•	•	•	•	•	00 011 000 ←e-2→
JR NC, e	If C = 1 continue If C = 0 PC ← PC + e	Jump relative to PC + e if carry = 0	2	7	•	•	•	•	•	•	00 110 000 ←e-2→
JR NZ, e	If Z = 1 continue	Jump relative to PC + e if non-zero (Z = 0)	2	7	•	•	•	•	•	•	00 100 000 ←e-2→
JR Z, e	If Z = 0 continue	Jump relative to PC + e if zero (Z = 1)	2	7	•	•	•	•	•	•	00 101 000 ←e-2→
LD A, (BC)	A ← (BC)	Load ACC with location (BC)	1	7	•	•	•	•	•	•	00 001 010
LD A, (DE)	A ← (DE)	Load ACC with location (DE)	1	7	•	•	•	•	•	•	00 011 010
LD A, I	A ← I	Load ACC with I	2	9	•	↕	IFF	↕	0	0	11 101 101 01 010 111
LD A, (nn)	A ← (nn)	Load ACC with location nn	3	13	•	•	•	•	•	•	00 111 010 nn nnn nnn nn nnn nnn
LD A, R	A ← R	Load ACC with Reg. R	2	9	•	↕	IFF	↕	0	0	11 101 101 01 011 111
LD (BC), A	(BC) ← A	Load location (BC) with ACC	1	7	•	•	•	•	•	•	00 000 010
LD (DE), A	(DE) ← A	Load location (DE) with ACC	1	7	•	•	•	•	•	•	00 010 010
LD (HL), n	(HL) ← n	Load location (HL) with value n	2	10	•	•	•	•	•	•	00 110 110 nn nnn nnn
LD ss, nn	ss ← nn	Load Reg. pair ss with value nn	4	20	•	•	•	•	•	•	00 ss0 001 Ⓐ nn nnn nnn nn nnn nnn
LD HL, (nn)	H ← (nn + 1) L ← (nn)	Load HL with location (nn)	3	16	•	•	•	•	•	•	00 101 010 nn nnn nnn nn nnn nnn
LD (HL), r	(HL) ← r	Load location (HL) with Reg. r	1	7	•	•	•	•	•	•	01 110 rrr Ⓑ
LD I, A	I ← A	Load I with ACC	2	9	•	•	•	•	•	•	11 101 101 01 000 111
LD IX, nn	IX ← nn	Load IX with value nn	4	19	•	•	•	•	•	•	11 011 101 00 100 001 nn nnn nnn nn nnn nnn
LD IX, (nn)	IX_H ← (nn + 1) IX_L ← (nn)	Load IX with location (nn)	4	20	•	•	•	•	•	•	11 011 101 00 101 010 nn nnn nnn nn nnn nnn
LD (IX + d), n	(IX + d) ← n	Load location (IX + d) with value n	4	19	•	•	•	•	•	•	11 011 101 00 110 110 dd ddd ddd nn nnn nnn
LD (IX + d), r	(IX + d) ← r	Load location (IX + d) with Reg. r	3	19	•	•	•	•	•	•	11 011 101 Ⓑ 01 110 rrr dd ddd ddd

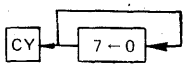
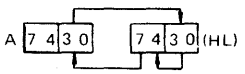
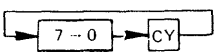
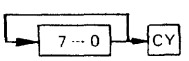
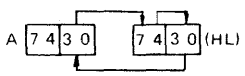
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MNEMONIC	SYMBOLIC OPERATION	DESCRIPTION	NO. BYTES	NO. T STATES	FLAGS C	Z	P/V	S	N	H	OP CODE 76 543 210
LD IY, nn	IY ← nn	Load IY with value nn	4	14	•	•	•	•	•	•	11 111 101 00 100 001 nn nnn nnn nn nnn nnn
LD IY, (nn)	IY_H ← (nn + 1) IY_L ← (nn)	Load IY with location (nn)	4	20	•	•	•	•	•	•	11 111 101 00 101 010 nn nnn nnn nn nnn nnn
LD ss, (nn)	ss_H ← (nn + 1) ss_L ← (nn)	Load Reg. pair dd with location (nn)	4	20	•	•	•	•	•	•	11 101 101 Ⓐ 01 ss1 011 nn nnn nnn nn nnn nnn
LD (IY + d), n	(IY + d) ← n	Load (IY + d) with value n	4	19	•	•	•	•	•	•	11 111 101 00 110 110 dd ddd ddd nn nnn nnn
LD (IY + d), r	(IY + d) ← r	Load location (IY + d) with Reg. r	3	19	•	•	•	•	•	•	11 111 101 Ⓑ 01 110 rrr dd ddd ddd
LD (nn), A	(nn) ← A	Load location (nn) with ACC	3	13	•	•	•	•	•	•	00 110 010 nn nnn nnn nn nnn nnn
LD (nn), ss	(nn + 1) ← ss_H (nn) ← ss_L	Load location (nn) with Reg. pair dd	4	20	•	•	•	•	•	•	11 101 101 Ⓐ 01 ss0 011 nn nnn nnn nn nnn nnn
LD (nn), HL	(nn + 1) ← H (nn) ← L	Load location (nn) with HL	3	16	•	•	•	•	•	•	00 100 010 nn nnn nnn nn nnn nnn
LD (nn), IX	(nn + 1) ← IX_H (nn) ← IX_L	Load location (nn) with IX	4	20	•	•	•	•	•	•	11 011 101 00 100 010 nn nnn nnn nn nnn nnn
LD (nn), IY	(nn + 1) ← IY_H (nn) ← IY_L	Load location (nn) with IY	4	20	•	•	•	•	•	•	11 111 101 00 100 010 nn nnn nnn nn nnn nnn
LD R, A	R ← A	Load R with ACC	2	9	•	•	•	•	•	•	11 101 101 01 001 111
LD r, (HL)	r ← (HL)	Load Reg. r with location (HL)	1	7	•	•	•	•	•	•	01 rrr 110 Ⓑ
LD r, (IX + d)	r ← (IX + d)	Load Reg. r with location (IX + d)	3	19	•	•	•	•	•	•	11 011 101 Ⓑ 01 rrr 110 dd ddd ddd
LD r, (IY + d)	r ← (IY + d)	Load Reg. r with location (IY + d)	3	19	•	•	•	•	•	•	11 111 101 Ⓑ 01 rrr 110 dd ddd ddd
LD r, n	r ← n	Load Reg. r with value n	2	7	•	•	•	•	•	•	00 rrr 110 Ⓑ nn nnn nnn
LD, r, r'	r ← r'	Load Reg. r with Reg. r	1	4	•	•	•	•	•	•	01 rrr r'r'r' Ⓕ
LD SP, HL	SP ← HL	Load SP with HL	1	6	•	•	•	•	•	•	11 111 001
LD SP, IX	SP ← IX	Load SP with IX	2	10	•	•	•	•	•	•	11 011 101 11 111 001
LD SP, IY	SP ← IY	Load SP with IY	2	10	•	•	•	•	•	•	11 111 101 11 111 001
LDD	(DE) ← (HL) DE ← DE − 1 HL ← HL − 1 BC ← BC − 1	Load location (DE) with location (HL), decrement DE, HL and BC	2	16	•	•	↕	•	0	0	11 101 101 10 101 000
LDDR	(DE) ← (HL) DE ← DE − 1 HL ← HL − 1 BC ← BC − 1 until BC = 0	Load location (DE) with location (HL)	2	21	•	•	0	•	0	0	11 101 101 10 111 000
LDI	(DE) ← (HL) DE ← DE + 1 HL ← HL + 1 BC ← BC − 1	Load location (DE) with location (HL), increment DE, HL; decrement BC	2	16	•	•	↕①	•	0	0	11 101 101 10 100 000
LDIR	(DE) ← (HL) DE ← DE + 1 HL ← HL + 1 BC ← BC − 1 until BC = 0	Load location (DE) with location (HL), increment DE, HL; decrement BC and repeat until BC = 0	2	21 if BC ≠ 0 16 if BC = 0	•	•	0	•	0	0	11 101 101 10 110 000
NEG	A ← 0 − A	Negate ACC (2's complement)	2	8	↕	↕	V	↕	1	↕	11 101 101 01 000 100

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MNEMONIC	SYMBOLIC OPERATION	DESCRIPTION	NO. BYTES	NO. T STATES	FLAGS C	Z	P/V	S	N	H	OP CODE 76 543 210
NOP		No operation	1	4	•	•	•	•	•	•	00 000 000
OR r	A ← AV r	Logical 'OR' of Reg. r and ACC		4	0	↕	P	↕	0	↕	10 110 rrr (B)
OR n	A ← AV n	Logical 'OR' of value n and ACC		7	•	↕	P	↕	0	↕	11 110 110 nn nnn nnn
OR (HL)	A ← AV (HL)	Logical 'OR' of loc. (HL) and ACC		7	•	↕	P	↕	0	↕	10 110 110
OR (IX + d)	A ← (IX + d)	Logical 'OR' of loc. (IX + d) Λ ACC		19	•	↕	P	↕	0	↕	11 011 101 10 110 110 dd ddd ddd
OR (IY + d)	A ← AV (IY + d)	Logical 'OR' of loc. (IY + d) Λ ACC		19	•	↕	P	↕	0	↕	11 111 101 10 110 110 dd ddd ddd
OTDR	(C) ← (HL) B ← B − 1 HL ← HL − 1 until B = 0	Load output port (C) with contents of location (HL), decrement HL and B, repeat until B = 0	2	21 if B ≠ 0 16 if B = C	•	1	X	X	1	X	11 101 101 10 111 011
OTIR	(C) ← (HL) B ← B − 1 HL ← HL + 1 until B = 0	Load output port (C) with location (HL), increment HL, decrement B, repeat until B = 0	2	21 if B ≠ 0 16 if B = C	•	1	X	X	1	X	11 101 101 10 110 011
OUT (C), r	(C) ← r	Load output port (C) with Reg. r	2	12	•	•	•	•	•	•	11 101 101 (B) 01 rrr 001
OUT (n), A	(n) ← A	Load output port (n) with ACC	2	11	•	•	•	•	•	•	11 010 011 nn nnn nnn
OUTD	(C) ← (HL) B ← B − 1 HL ← HL − 1	Load output port (C) with location (HL), increment HL and decrement B	2	16	•	↕ (3)	X	X	1	X	11 101 101 10 101 011
OUTI	(C) ← (HL) B ← B − 1 HL ← HL + 1	Load output port (C) with location (HL), increment HL and decrement B	2	16	•	↕ (3)	X	X	1	X	11 101 101 10 100 011
POP IX	IX_H ← (SP + 1) IX_L ← (SP)	Load IX with top of stack	2	14	•	•	•	•	•	•	11 011 101 11 100 001
POP IY	IY_H ← (SP + 1) IY_L ← (SP)	Load IY with top of stack	2	14	•	•	•	•	•	•	11 111 101 11 100 001
POP qq	qq_H ← (SP + 1) qq_L ← (SP)	Load Reg. pair qq with top of stack	1	10	•	•	•	•	•	•	11 qq0 001 (G)
PUSH IX	(SP − 2) ← IX_L (SP − 1) ← IX_H	Load IX onto stack	2	15	•	•	•	•	•	•	11 011 101 11 100 101
PUSH IY	(SP − 2) ← IY_L (SP − 1) ← IY_H	Load IY onto stack	2	15	•	•	•	•	•	•	11 111 101 11 100 101
PUSH qq	(SP − 2) ← qq_L (SP − 1) ← qq_H	Load Reg. pair qq onto stack	1	11	•	•	•	•	•	•	11 qq0 101 (G)
RES b, r	S_b ← 0	Reset Bit b of Reg. r		8	•	•	•	•	•	•	11 001 011 (B) 10 bbb rrr (E)
RES b, (HL)	S_b ← 0, (HL)	Reset Bit b of loc. (HL)		15	•	•	•	•	•	•	11 001 011 10 bbb 110
RES b, (IX + d)	S_b ← 0, (IX + d)	Reset Bit b of loc. (IX + d)		23	•	•	•	•	•	•	11 011 101 11 001 011 dd ddd ddd 10 bbb 110
RES b, (IY + d)	S_b ← 0, (IY + d)	Reset Bit b of loc. (IY + d)		23	•	•	•	•	•	•	11 111 101 11 001 011 dd ddd ddd 10 bbb 110
RET	PC_L ← (SP) PC_H ← (SP + 1)	Return from subroutine	1	10	•	•	•	•	•	•	11 001 001
RET cc	If condition cc is false cont. else (PC_L ← (SP) PC_H ← (SP + 1)	Return from subroutine if condition cc is true	1	5 if CC false 11 if CC true	•	•	•	•	•	•	11 ←cc→ 000 (H)
RETI		Return from interrupt	2	14	•	•	•	•	•	•	11 101 101 01 001 101
RETN		Return from non-maskable interrupt	2	14	•	•	•	•	•	•	11 101 101 01 000 101
RL r		Rotate left through carry Reg. r		2	↕	↕	P	↕	0	0	11 001 011 (B) 00 010 rrr
RL (HL)		Rotate left through carry loc. (HL)		4	↕	↕	P	↕	0	0	11 001 011 00 010 110
RL (IX + d)	 m = r, (HL), (IX + d), (IY + d), A	Rotate left through carry loc. (IX + d)		6	↕	↕	P	↕	0	0	11 011 101 11 001 011 dd ddd ddd 00 010 110
RL (IY + d)		Rotate left through carry loc. (IY + d)		6	↕	↕	P	↕	0	0	11 111 101 11 001 011 dd ddd ddd 00 010 110
RLA		Rotate left ACC through carry	1	4	↕	•	•	•	0	0	00 010 111

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MNEMONIC	SYMBOLIC OPERATION	DESCRIPTION	NO. BYTES	NO. T STATES	FLAGS C	Z	P/V	S	N	H	OP CODE 76 543 210
RLC (HL)		Rotate location (HL) left circular	2	15	↕	↕	P	↕	0	0	11 001 011 00 000 110
RLC (IX + d)		Rotate location (IX + d) left circular	4	23	↕	↕	P	↕	0	0	11 011 101 11 001 011 dd ddd ddd 00 000 110
RLC (IY + d)	 m ≡ r, (HL), (IX + d), (IY + d), A	Rotate location (IY + d) left circular	4	23	↕	↕	P	↕	0	0	11 111 101 11 001 011 dd ddd ddd 00 000 110
RLC r		Rotate Reg. r left circular	2	8	↕	↕	P	↕	0	0	11 001 011 (B) 00 000 r r r
RLCA		Rotate left circular ACC	1	4	↕	•	•	•	0	0	00 000 111
RLD		Rotate digit left and right between ACC and location (HL)	2	18	•	↕	P	↕	0	0	11 101 101 01 101 111
RR r		Rotate right through carry Reg. r		2	↕	↕	P	↕	0	0	11 001 011 (B) 00 011 r r r
RR (HL)		Rotate right through carry loc. (HL)		4	↕	↕	P	↕	0	0	11 001 011 00 011 110
RR (IX + d)		Rotate right through carry loc. (IX + d)		6	↕	↕	P	↕	0	0	11 011 101 11 001 011 dd ddd ddd 00 011 110
RR (IY + d)	 m ≡ r, (HL), (IX + d), (IY + d), A	Rotate right through carry loc. (IY + d)		6	↕	↕	P	↕	0	0	11 111 101 11 001 011 dd ddd ddd 00 011 110
RRA		Rotate right ACC through carry	1	4	↕	•	•	•	0	0	00 011 111
RRC r		Rotate Reg. r right circular		2	↕	↕	P	↕	0	0	11 001 011 (B) 00 001 r r r
RRC (HL)		Rotate loc. (HL) right circular		4	↕	↕	P	↕	0	0	11 001 011 00 001 110
RRC (IX + d)		Rotate loc. (IX + d) right circular		6	↕	↕	P	↕	0	0	11 011 101 11 001 011 dd ddd ddd 00 001 110
RRC (IY + d)	m ≡ r, (HL), (IX + d), (IY + d), A	Rotate loc. (IY + d) right circular		6	↕	↕	P	↕	0	0	11 111 101 11 001 011 dd ddd ddd 00 001 110
RRCA		Rotate right circular ACC	1	4	↕	•	•	•	0	0	00 001 111
RRD		Rotate digit right and left between ACC and location (HL)	2	18	•	↕	P	↕	0	0	11 101 101 01 100 111
RST$_t$	(SP − 1) ← PC$_H$ (SP − 2) ← PC$_L$ PC$_H$ ← 0, PC$_L$ ← T	Restart to location T	1	11	•	•	•	•	•	•	11 t t t 111
SBC A, r	A ← A − r − CY	Subtract Reg. r from ACC w/carry	1	4	↕	↕	V	↕	1	↕	10 011 r r r (B)
SBC A, n	A ← A − n − CY	Subtract value n from ACC with carry		7	↕	↕	V	↕	1	↕	11 011 110 n n n n n n n
SBC A, (HL)	A ← A − (HL) − CY	Sub. loc. (HL) from ACC w/carry		7	↕	↕	V	↕	1	↕	10 011 110
SBC A, (IX + d)	A ← A − (IX + d) − CY	Subtract loc. (IX + d) from ACC with carry		19	↕	↕	V	↕	1	↕	11 011 101 10 011 110 dd ddd ddd
SBC A, (IY + d)	A ← A − (IY + d) − CY	Subtract loc. (IY + d) from ACC with carry		19	↕	↕	V	↕	1	↕	11 111 101 10 011 110 dd ddd ddd
SBC HL, ss	HL ← HL − ss − CY	Subtract Reg. pair ss from HL with carry	2	15	↕	↕	V	↕	1	X	11 101 101 (A) 01 s s 0 010
SCF	CY ← 1	Set carry flag (C = 1)	1	4	1	•	•	•	0	0	00 110 111
SET b, (HL)	(HL)$_b$ ← 1	Set Bit b of location (HL)	2	15	•	•	•	•	•	•	11 001 011 (E) 11 b b b 110
SET b, (IX + d)	(IX + d)$_b$ ← 1	Set Bit b of location (IX + d)	4	23	•	•	•	•	•	•	11 011 101 (E) 11 001 011 dd ddd ddd 11 b b b 110

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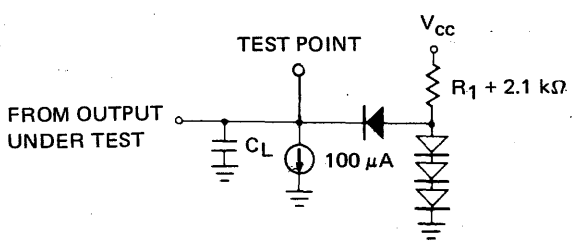
AC CHARACTERISTICS

T_a = 0°C to +70°C; V_{CC} = +5V ± 5%, unless otherwise specified.

PARAMETER	SYMBOL	LIMITS μPD780 MIN	LIMITS μPD780 MAX	LIMITS μPD780-1 MIN	LIMITS μPD780-1 MAX	UNIT	TEST CONDITIONS
Clock Period	t_c	0.4	⑫	0.25	⑫	μs	
Clock Pulse Width, Clock High	$t_{w(\Phi H)}$	180		110		ns	
Clock Pulse Width, Clock Low	$t_{w(\Phi L)}$	180	2000	110	2000	ns	
Clock Rise and Fall Time	$t_{r,f}$		30		30	ns	
Address Output Delay	$t_{D(AD)}$		145		110	ns	
Delay to Float	$t_{F(AD)}$		110		90	ns	
Address Stable Prior to $\overline{MREQ}$ (Memory Cycle)	t_{acm}	①		①		ns	C_L = 50 pF
Address Stable Prior to $\overline{IORQ}$, $\overline{RD}$ or $\overline{WR}$ (I/O Cycle)	t_{aci}	②		②		ns	
Address Stable from $\overline{RD}$ or $\overline{WR}$	t_{ca}	③		③		ns	
Address Stable from $\overline{RD}$ or $\overline{WR}$ During Float	t_{caf}	④		④		ns	
Data Output Delay	$t_{D(D)}$		230		150	ns	
Delay to Float During Write Cycle	$t_{F(D)}$		90		90	ns	
Data Setup Time to Rising Edge of Clock During M1 Cycle	$t_{S\Phi(D)}$	50		35		ns	
Data Setup Time to Falling Edge of Clock During M2 to M5 Cycles	$t_{S\bar{\Phi}(D)}$	60		50		ns	C_L = 200 pF
Data Stable Prior to $\overline{WR}$ (Memory Cycle)	t_{dcm}	⑤		⑤		ns	
Data Stable Prior to $\overline{WR}$ (I/O Cycle)	t_{dci}	⑥		⑥		ns	
Data Stable from $\overline{WR}$	t_{cdf}	⑦		⑦		ns	
Any Hold Time for Setup Time	t_H	0			0	ns	
$\overline{MREQ}$ Delay from Falling Edge of Clock to $\overline{MREQ}$ Low	$t_{DL\bar{\Phi}(MR)}$		100		85	ns	
$\overline{MREQ}$ Delay from Rising Edge of Clock to $\overline{MREQ}$ High	$t_{DH\Phi(MR)}$		100		85	ns	
$\overline{MREQ}$ Delay from Falling Edge of Clock to $\overline{MREQ}$ High	$t_{DH\bar{\Phi}(MR)}$		100		85	ns	
Pulse Width, $\overline{MREQ}$ Low	$t_{w(\overline{MRL})}$	⑧		⑧		ns	
Pulse Width, $\overline{MREQ}$ High	$t_{w(\overline{MRH})}$	⑨		⑨		ns	
$\overline{IORQ}$ Delay from Rising Edge of Clock to $\overline{IORQ}$ Low	$t_{DL\Phi(IR)}$		90		75	ns	
$\overline{IORQ}$ Delay from Falling Edge of Clock to $\overline{IORQ}$ Low	$t_{DL\bar{\Phi}(IR)}$		110		85	ns	
$\overline{IORQ}$ Delay from Rising Edge of Clock to $\overline{IORQ}$ High	$t_{DH\Phi(IR)}$		100		85	ns	
$\overline{IORQ}$ Delay from Falling Edge of Clock to $\overline{IORQ}$ High	$t_{DH\bar{\Phi}(IR)}$		110		85	ns	C_L = 50 pF
$\overline{RD}$ Delay from Rising Edge of Clock to $\overline{RD}$ Low	$t_{DL\Phi(RD)}$		100		85	ns	
$\overline{RD}$ Delay from Falling Edge of Clock to $\overline{RD}$ Low	$t_{DL\bar{\Phi}(RD)}$		130		95	ns	
$\overline{RD}$ Delay from Rising Edge of Clock to $\overline{RD}$ High	$t_{DH\Phi(RD)}$		100		85	ns	
$\overline{RD}$ Delay from Falling Edge of Clock to $\overline{RD}$ High	$t_{DH\bar{\Phi}(RD)}$		110		85	ns	
$\overline{WR}$ Delay from Rising Edge of Clock to $\overline{WR}$ Low	$t_{DL\Phi(WR)}$		80		65	ns	
$\overline{WR}$ Delay from Falling Edge of Clock to $\overline{WR}$ Low	$t_{DL\bar{\Phi}(WR)}$		90		80	ns	
$\overline{WR}$ Delay from Falling Edge of Clock to $\overline{WR}$ High	$t_{DH\Phi(WR)}$		100		80	ns	
Pulse Width to $\overline{WR}$ Low	$t_{w(\overline{WRL})}$	⑩		⑩		ns	
$\overline{MI}$ Delay from Rising Edge of Clock to $\overline{MI}$ Low	$t_{DL(MI)}$		130		100	ns	C_L = 30 pF
$\overline{MI}$ Delay from Rising Edge of Clock to $\overline{MI}$ High	$t_{DH(MI)}$		130		100	ns	
$\overline{RFSH}$ Delay from Rising Edge of Clock to $\overline{RFSH}$ Low	$t_{DL(RF)}$		180		130	ns	
$\overline{RFSH}$ Delay from Rising Edge of Clock to $\overline{RFSH}$ High	$t_{DH(RF)}$		150		120	ns	
$\overline{WAIT}$ Setup Time to Falling Edge of Clock	$t_{S(WT)}$	70		70		ns	
$\overline{HALT}$ Delay Time from Falling Edge of Clock	$t_{D(HT)}$		300		300	ns	C_L = 50 pF
$\overline{INT}$ Setup Time to Rising Edge of Clock	$t_{S(IT)}$	80		80		ns	
Pulse Width, $\overline{NMI}$ Low	$t_{w(\overline{NML})}$	80		80		ns	
$\overline{BUSRQ}$ Setup Time to Rising Edge of Clock	$t_{S(BQ)}$	80		50		ns	
$\overline{BUSAK}$ Delay from Rising Edge of Clock to $\overline{BUSAK}$ Low	$t_{DL(BA)}$		120		100	ns	C_L = 50 pF
$\overline{BUSAK}$ Delay from Falling Edge of Clock to $\overline{BUSAK}$ High	$t_{DH(BA)}$		110		100	ns	
$\overline{RESET}$ Setup Time to Rising Edge of Clock	$t_{S(RS)}$	90		60		ns	
Delay to Float ($\overline{MREQ}$, $\overline{IORQ}$, $\overline{RD}$ and $\overline{WR}$)	$t_{F(C)}$		100		80	ns	
$\overline{MI}$ Stable Prior to $\overline{IORQ}$ (Interrupt Ack.)	t_{mr}	⑪		⑪		ns	

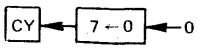
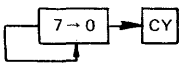
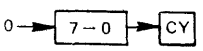
Notes:
① $t_{acm} = t_{w(\Phi H)} + t_f - 65$ (75)*
② $t_{aci} = t_c - 70$ (80)*
③ $t_{ca} = t_{w(\Phi L)} + t_r - 50$ (40)*
④ $t_{caf} = t_{w(\Phi L)} + t_r - 45$ (60)*
⑤ $t_{dcm} = t_c - 170$ (210)*
⑥ $t_{dci} = t_{w(\Phi L)} + t_r - 170$ (210)*
⑦ $t_{cdf} = t_{w(\Phi L)} + t_r - 70$ (80)*
⑧ $t_{w(\overline{MRL})} = t_c - 30$ (40)*
⑨ $t_{w(\overline{MRH})} = t_{w(\Phi H)} + t_f - 20$ (30)*
⑩ $t_{w(\overline{WR})} = t_c - 30$ (40)*
⑪ $t_{mr} = 2t_c + t_{w(\Phi H)} + t_f - 65$ (80)*
⑫ $t_c = t_{w(\Phi H)} + t_{w(\Phi L)} + t_r + t_f$

*These values apply to the μPD780.



LOAD CIRCUIT FOR OUTPUT

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MNEMONIC	SYMBOLIC OPERATION	DESCRIPTION	NO. BYTES	NO. T STATES	FLAGS C	Z	P/V	S	N	H	OP CODE 76 543 210
SET b, (IY + d)	$(IY + d)_b \leftarrow 1$	Set Bit b of location (IY + d)	4	23	•	•	•	•	•	•	11 111 101 Ⓔ 11 001 011 dd ddd ddd 11 bbb 110
SET b, r	$r_b \leftarrow 1$	Set Bit b of Reg. r	2	8	•	•	•	•	•	•	11 001 011 Ⓑ 11 bbb rrr
SLA r		Shift Reg. r left arithmetic		8	↕	↕	P	↕	0	0	11 001 011 Ⓑ 00 100 rrr
SLA (HL)		Shift loc. (HL) left arithmetic		15	↕	↕	P	↕	0	0	11 001 011 00 100 110
SLA (IX + d)	m ≡ r, (HL), (IX + d), (IY + d)	Shift loc. (IX + d) left arithmetic		23	↕	↕	P	↕	0	0	11 011 101 11 001 011 dd ddd ddd 00 100 110
SLA (IY + d)		Shift loc. (IY + d) left arithmetic		23	↕	↕	P	↕	0	0	11 111 101 11 001 011 dd ddd ddd 00 100 110
SRA r		Shift Reg. r right arithmetic		8	↕	↕	P	↕	0	0	11 001 011 Ⓑ 00 101 rrr
SRA (HL)		Shift loc. (HL) right arithmetic		15	↕	↕	P	↕	0	0	11 001 011 00 101 110
SRA (IX + d)	m ≡ r, (HL), (IX + d), (IY + d)	Shift loc. (IX + d) right arithmetic		23	↕	↕	P	↕	0	0	11 011 101 11 001 011 dd ddd ddd 00 101 110
SRA (IY + d)		Shift loc. (IY + d) right arithmetic		23	↕	↕	P	↕	0	0	11 111 101 11 001 011 dd ddd ddd 00 101 110
SRL r		Shift Reg. r right logical		8	↕	↕	P	↕	0	0	11 001 011 Ⓑ 00 111 rrr
SRL (HL)		Shift loc. (HL) right logical		15	↕	↕	P	↕	0	0	11 001 011 00 111 110
SRL (IX + d)	m ≡ r, (HL), (IX + d), (IY + d)	Shift loc. (IX + d) right logical		23	↕	↕	P	↕	0	0	11 011 101 11 001 011 dd ddd ddd 00 111 110
SRL (IY + d)		Shift loc. (IY + d) right logical		23	↕	↕	P	↕	0	0	11 111 101 11 001 011 dd ddd ddd 00 111 110
SUB r	A ← A − r	Subtract Reg. r from ACC		4	↕	↕	V	↕	1	↕	10 010 rrr Ⓑ
SUB n	A ← A − n	Subtract value n from ACC		7	↕	↕	V	↕	1	↕	11 010 110 nn nnn nnn
SUB (HL)	A ← A − (HL)	Subtract loc. (HL) from ACC		7	↕	↕	V	↕	1	↕	10 010 110
SUB (IX + d)	A ← A − (IX + d)	Subtract loc. (IX + d) from ACC		19	↕	↕	V	↕	1	↕	11 011 101 10 010 110 dd ddd ddd
SUB (IY + d)	A ← A − (IY + d)	Subtract loc. (IY + d) from ACC		19	↕	↕	V	↕	1	↕	11 111 101 10 010 110 dd ddd ddd
XOR r	A ← A∀r	Exclusive 'OR' Reg. r and ACC		4	↕	↕	P	↕	1	↕	10 101 rrr Ⓑ
XOR n	A ← A∀n	Exclusive 'OR' value n and ACC		7	↕	↕	P	↕	1	↕	11 101 110 nn nnn nnn
XOR (HL)	A ← A∀ (HL)	Exclusive 'OR' loc. (HL) and ACC		7	↕	↕	P	↕	1	↕	10 101 110
XOR (IX + d)	A ← A∀ (IX + d)	Exclusive 'OR' loc. (IX + d) and ACC		19	↕	↕	P	↕	1	↕	11 011 101 10 101 110 dd ddd ddd
XOR (IY + d)	A ← A∀ (IY + d)	Exclusive 'OR' loc. (IY + d) and ACC		19	↕	↕	P	↕	1	↕	11 111 101 10 101 110 dd ddd ddd

FLAG NOTES:

① P/V flag is 0 if B-1=0, else P/V=1

② Z=1 if A=(HL), else Z=0

③ If B-1=0, Z flag set, else reset

FLAG DEFINITIONS:

• = Flag not affected
0 = Flag reset
1 = Flag set
X = Flag unknown
↕ = Flag affected according to result of operation
V = Overflow set
P = Parity set
IFF = Interrupt flip-flop set

Ⓐ

Reg	ss
BC	00
DE	01
HL	10
SP	11

Ⓑ

Reg	r
A	111
B	000
C	001
D	010
E	011
H	100
L	101

Ⓒ

Reg	pp
BC	00
DE	01
IX	10
SP	11

Ⓓ

Reg	rr
BC	00
DE	01
IY	10
SP	11

Ⓔ

Bit	b
0	000
1	001
2	010
3	011
4	100
5	101
6	110
7	111

Ⓕ

Reg	r,r'
A	111
B	000
C	001
D	010
E	011
H	100
L	101

Ⓖ

Reg	qq
BC	00
DE	01
HL	10
AF	11

Ⓗ

CC	Condition		Relevant Flag
000	NZ	Non Zero	Z
001	Z	Zero	Z
010	NC	Non Carry	C
011	C	Carry	C
100	PO	Parity Odd	P/V
101	PE	Parity Even	P/V
110	P	Sign Positive	S
111	M	Sign Negative	S

Ⓘ

Reg	r
B	000
C	001
D	010
E	011
H	100
L	101
F	110
A	111

FLAG DESCRIPTION:

C = Carry/Link
Z = Zero
P/V = Parity/Overflow
S = Sign
N = Add/Subtract
H = Half Carry

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SINGLE CHIP 8-BIT MICROCOMPUTER

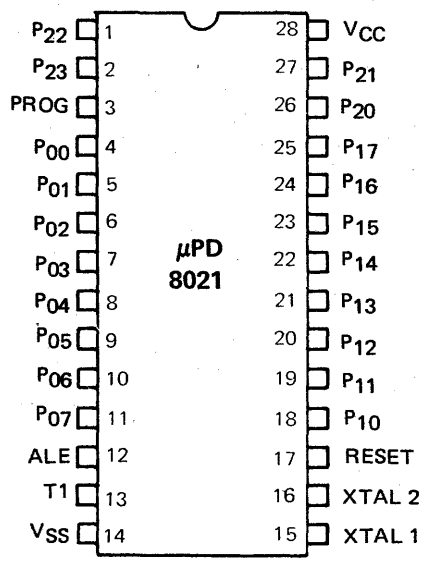
DESCRIPTION

The NEC μPD8021 is a stand alone 8-bit parallel microcomputer incorporating the following features usually found in external peripherals. The μPD8021 contains: 1K x 8-bits of mask ROM program memory, 64 x 8 bits of RAM data memory, 21 I/O lines, an 8-bit interval timer/event counter, and internal clock circuitry.

FEATURES

- 8-Bit Processor, ROM, RAM, I/O, Timer/Counter
- Single +5V Supply (+4.5V to +6.5V)
- NMOS Silicon Gate Technology
- 10 μs Cycle Time
- All Instructions 1 or 2 Cycles
- Instructions are Subset of μPD8048/8748/8035
- High Current Drive Capability — 2 I/O Pins
- Clock Generation Using Single Resistor or Inductor
- Zero-Cross Detection Capability
- Expandable I/O Using μPD8243's
- Available in 28 Pin Plastic Package

PIN CONFIGURATION



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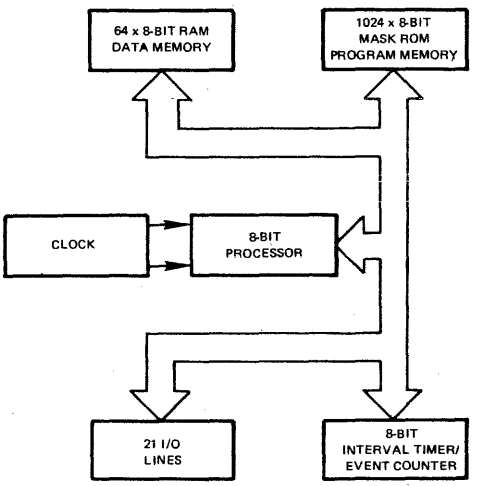
μPD8021

FUNCTIONAL DESCRIPTION

The NEC μPD8021 is a single component, 8-bit, parallel microprocessor using N-channel silicon gate MOS technology. The self-contained 1K x 8-bit ROM, 64 x 8-bit RAM, 8-bit timer/counter, and clock circuitry allow the μPD8021 to operate as a single-chip microcomputer in applications ranging from controllers to arithmetic processors.

The instruction set, a subset of the μPD8048/8748/8035, is optimum for high-volume, low cost applications where I/O flexibility and instruction set power are required. The μPD8021 instruction set is comprised mostly of single-byte instructions with no instructions over two bytes.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature . . . . . 0°C to +70°C
Storage Temperature (Ceramic Package) . . . . . -65°C to +150°C
(Plastic Package) . . . . . -65°C to +125°C
Voltage on Any Pin . . . . . -0.5 to +7 Volts ①
Power Dissipation. . . . . 1 Watt

Note: ① With Respect to Ground.

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

DC CHARACTERISTICS

T_a = 0°C to +70°C; V_{CC} = +5.5V ± 1V; V_{SS} = 0V

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input Low Voltage (All Except XTAL 1, XTAL 2)	V_{IL}	-0.5		+ 0.8	V	
Input High Voltage (All Except XTAL 1, XTAL 2)	V_{IH}	2.0		V_{CC}	V	V_{CC} = 5.0V ± 10%
Input High Voltage (All Except XTAL 1, XTAL 2)	V_{IH1}	3.0		V_{CC}	V	V_{CC} = 5.5V ± 1V
Output Low Voltage	V_{OL}			0.45	V	I_{OL} = 1.6 mA
Output Low Voltage (P_{10}, P_{11})	V_{OL1}			2.5	V	I_{OL} = 7 mA
Output High Voltage (All Unless Open Drain)	V_{OH}	2.4			V	I_{OH} = 50 μA
Output Leakage Current (Open Drain Option – Port 0)	I_{OL}			-10	μA	$V_{CC} \geq V_{IN} \geq V_{SS}$ +0.45V
V_{CC} Supply Current	I_{CC}			60	mA	

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PIN IDENTIFICATION

PIN NO.	PIN SYMBOL	FUNCTION
1-2, 26-27	P_{20}-P_{23} (Port 2)	P_{20}-P_{23} comprise the 4-bit bi-directional I/O port which is also used as the expander bus for the μPD8243.
3	PROG	PROG is the output strobe pin for the μPD8243.
4-11	P_{00}-P_{07} (Port 0)	One of the two 8-bit quasi bi-directional I/O ports.
12	ALE	Address Latch Enable output (active-high). Occurring once every 30 input clock periods, ALE can be used as an output clock.
13	T1	Testable input using transfer functions JT1 and JNT1. T1 can be made the counter/timer input using the STRT CNT instruction. T1 also provides zero-cross sensing for low-frequency AC input signals.
14	V_{SS}	Processor's ground potential.
15	XTAL 1	One side of frequency source input using resistor, inductor, crystal or external source. (non-TTL compatible V_{IH}).
16	XTAL 2	The other side of frequency source input.
17	RESET	RESET initializes the processor, setting program counter to zero and clearing status flip-flops.
18-25	P_{10}-P_{17} (Port 1)	The second of two 8-bit quasi bi-directional I/O ports.
28	V_{CC}	+5V power supply input.

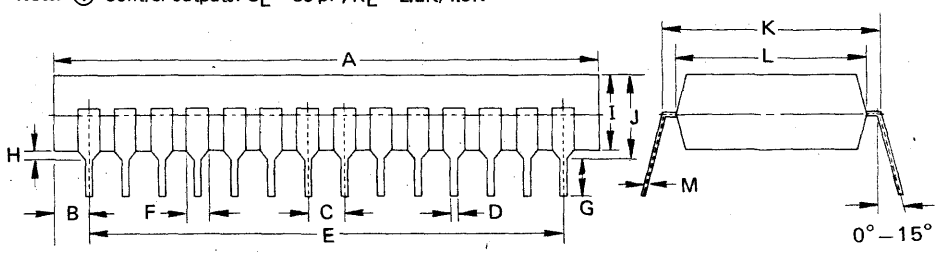
AC CHARACTERISTICS

$T_a = 0°C$ to $+70°C$; $V_{CC} = 5.5V \pm 1V$; $V_{SS} = 0V$

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Cycle Time	T_{CY}	10.0		50.0	μs	3 MHz XTAL = 10 μs ①
Oscillator Frequency Variation (Resistor Mode)	Δ_F	−20		+20	%	F = 2.5 MHz ①

Note: ① Control outputs: $C_L = 80$ pF; $R_L = 2.2K/4.3K$

PACKAGE OUTLINE μPD8021C



ITEM	MILLIMETERS	INCHES
A	38.0 MAX.	1.496 MAX.
B	2.49	0.098
C	2.54	0.10
D	0.5 ± 0.1	0.02 ± 0.004
E	33.02	1.3
F	1.5	0.059
G	2.54 MIN.	0.10 MIN.
H	0.5 MIN.	0.02 MIN.
I	5.22 MAX.	0.205 MAX.
J	5.72 MAX.	0.225 MAX.
K	15.24	0.6
L	13.2	0.52
M	$0.25^{+0.10}_{-0.05}$	$0.01^{+0.004}_{-0.002}$

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MNEMONIC	FUNCTION	DESCRIPTION	INSTRUCTION CODE D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	CYCLES	BYTES	FLAG C
ACCUMULATOR													
ADD A, = data	(A) ← (A) + data	Add immediate the specified Data to the Accumulator.	0	0	0	0	0	0	1	1	2	2	•
			d_7	d_6	d_5	d_4	d_3	d_2	d_1	d_0			
Add A, Rr	(A) ← (A) + (Rr) for r = 0 - 7	Add contents of designated register to the Accumulator.	0	1	1	0	1	r	r	r	1	1	•
ADD A, @ Rr	(A) ← (A) + ((Rr)) for r = 0 - 1	Add indirect the contents the data memory location to the Accumulator.	0	1	1	0	0	0	0	r	1	1	•
ADDC A, = data	(A) ← (A) + (C) + data	Add immediate with carry the specified data to the Accumulator.	0	0	0	1	0	0	1	1	2	2	•
			d_7	d_6	d_5	d_4	d_3	d_2	d_1	d_0			
ADDC A, Rr	(A) ← (A) + (C) + (Rr) for r = 0 - 7	Add with carry the contents of the designated register to the Accumulator.	0	1	1	1	1	r	r	r	1	1	•
ADDC A, @ Rr	(A) ← (A) + (C) + ((Rr)) for r = 0 - 1	Add indirect with carry the contents of data memory location to the Accumulator.	0	1	1	1	0	0	0	r	1	1	•
ANL A, = data	(A) ← (A) AND data	Logical and specified Immediate Data with Accumulator.	0	1	0	1	0	0	1	1	2	2	
			d_7	d_6	d_5	d_4	d_3	d_2	d_1	d_0			
ANL A, Rr	(A) ← (A) AND (Rr) for r = 0 - 7	Logical and contents of designated register with Accumulator.	0	1	0	1	1	r	r	r	1	1	
ANL A, @ Rr	(A) ← (A) AND ((Rr)) for r = 0 - 1	Logical and Indirect the contents of data memory with Accumulator.	0	1	0	1	0	0	0	r	1	1	
CPL A	(A) ← NOT (A)	Complement the contents of the Accumulator.	0	0	1	1	0	1	1	1	1	1	
CLR A	(A) ← 0	CLEAR the contents of the Accumulator.	0	0	1	0	0	1	1	1	1	1	
DA A		DECIMAL ADJUST the contents of the Accumulator.	0	1	0	1	0	1	1	1	1	1	•
DEC A	(A) ← (A) - 1	DECREMENT by 1 the Accumulator's contents.	0	0	0	0	0	1	1	1	1	1	
INC A	(A) ← (A) + 1	Increment by 1 the Accumulator's contents.	0	0	0	1	0	1	1	1	1	1	
ORL A, = data	(A) ← (A) OR data	Logical OR specified immediate data with Accumulator	0	1	0	0	0	0	1	1	2	2	
			d_7	d_6	d_5	d_4	d_3	d_2	d_1	d_0			
ORL A, Rr	(A) ← (A) OR (Rr) for r = 0 - 7	Logical OR contents of designated register with Accumulator.	0	1	0	0	1	r	r	r	1	1	
ORL A @ Rr	(A) ← (A) OR ((Rr)) for r = 0 - 1	Logical OR Indirect the contents of data memory location with Accumulator.	0	1	0	0	0	0	0	r	1	1	
RL A	(AN + 1)← (AN) (A_0) ← (A_7) for N = 0 - 6	Rotate Accumulator left by 1-bit without carry.	1	1	1	0	0	1	1	1	1	1	
RLC A	(AN + 1) ← (AN); N = 0 - 6 (A_0) ← (C) (C) ← (A_7)	Rotate Accumulator left by 1-bit through carry.	1	1	1	1	0	1	1	1	1	1	•
RR A	(AN) ← (AN + 1); N = 0 - 6 (A_7) ← (A_0)	Rotate Accumulator right by 1-bit without carry.	0	1	1	1	0	1	1	1	1	1	
RRC A	(AN) ← (AN + 1); N = 0 - 6 (A_7) ← (C) (C) ← (A_0)	Rotate Accumulator right by 1-bit through carry.	0	1	1	0	0	1	1	1	1	1	•
SWAP A	(A_{4-7}) ⇄ (A_0 - 3)	Swap the 24-bit nibbles in the Accumulator.	0	1	0	0	0	1	1	1	1	1	
XRL A, = data	(A) ← (A) XOR data	Logical XOR specified immediate data with Accumulator.	1	1	0	1	0	0	1	1	2	2	
			d_7	d_6	d_5	d_4	d_3	d_2	d_1	d_0			
XRL A, Rr	(A) ← (A) XOR (Rr) for r = 0 - 7	Logical XOR contents of designated register with Accumulator.	1	1	0	1	1	r	r	r	1	1	
XRL A, @ Rr	(A) ← (A) XOR ((Rr)) for r = 0 - 1	Logical XOR Indirect the contents of data memory location with Accumulator.	1	1	0	1	0	0	0	r	1	1	
BRANCH													
DJNZ Rr, addr	(Rr) ← (Rr) - 1; r = 0 - 7 If (Rr) ≠ 0 (PC 0 - 7) ← addr	Decrement the specified register and test contents.	1	1	1	0	1	r	r	r	2	2	
			a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0			
JC addr	(PC 0 - 7) ← addr if C = 1 (PC) ← (PC) + 2 if C = 0	Jump to specified address if carry flag is set.	1	1	1	1	0	1	1	0	2	2	
			a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0			
JMP addr	(PC 8 - 10) ← addr 8 - 10 (PC 0 - 7) ← addr 0 - 7 (PC 11) ← DBF	Direct Jump to specified address within the 2K address block.	a_{10}	a_9	a_8	0	0	1	0	0	2	2	
			a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0			
JMPP @ A	(PC 0 - 7) ← ((A))	Jump indirect to specified address with address page.	1	0	1	1	0	0	1	1	2	1	
JNC addr	(PC 0 - 7) ← addr if C = 0 (PC) ← (PC) + 2 if C = 1	Jump to specified address if carry flag is low.	1	1	1	0	0	1	1	0	2	2	
			a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0			
JNT1 addr	(PC 0 - 7) ← addr if T1 = 0 (PC) ← (PC) + 2 if T1 = 1	Jump to specified address if Test 1 is low.	0	1	0	0	0	1	1	0	2	2	
			a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0			
JNZ addr	(PC 0 - 7) ← addr if A = 0 (PC) ← (PC) + 2 if A = 0	Jump to specified address if Accumulator is non-zero.	1	0	0	1	0	1	1	0	2	2	
			a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0			
JTF addr	(PC 0 - 7) ← addr if TF = 1 (PC) ← (PC) + 2 if TF = 0	Jump to specified address if Timer Flag is set to 1.	0	0	0	1	0	1	1	0	2	2	
			a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0			
JT1 addr	(PC 0 - 7) ← addr if T1 = 1 (PC) ← (PC) + 2 if T1 = 0	Jump to specified address if Test 1 is a 1.	0	1	0	1	0	1	1	0	2	2	
			a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0			
JZ addr	(PC 0 - 7) ← addr if A = 0 (PC) ← (PC) + 2 if A = 0	Jump to specified address if Accumulator is 0.	1	1	0	0	0	1	1	0	2	2	
			a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0			

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MNEMONIC	FUNCTION	DESCRIPTION	INSTRUCTION CODE D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	CYCLES	BYTES	FLAG C
DATA MOVES													
MOV A, = data	(A) ← data	Move Immediate the specified data into the Accumulator.	0 d_7	0 d_6	1 d_5	0 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2	
MOV A, Rr	(A) ← (Rr); r = 0 - 7	Move the contents of the designated registers into the Accumulator.	1	1	1	1	1	r	r	r	1	1	
MOV A, @ Rr	(A) ← ((Rr)); r = 0 - 1	Move Indirect the contents of data memory location into the Accumulator.	1	1	1	1	0	0	0	r	1	1	
MOV Rr, = data	(Rr) ← data; r = 0 - 7	Move Immediate the specified data into the designated register.	1 d_7	0 d_6	1 d_5	1 d_4	1 d_3	r d_2	r d_1	r d_0	2	2	
MOV Rr, A	(Rr) ← (A); r = 0 - 7	Move Accumulator Contents into the designated register.	1	0	1	0	1	r	r	r	1	1	
MOV @ Rr, A	((Rr)) ← (A); r = 0 - 1	Move Indirect Accumulator Contents into data memory location.	1	0	1	0	0	0	0	r	1	1	
MOV @ Rr, = data	((Rr)) ← data; r = 0 - 1	Move Immediate the specified data into data memory.	1 d_7	0 d_6	1 d_5	1 d_4	0 d_3	0 d_2	0 d_1	r d_0	2	2	
MOVP A, @ A	(PC 0 - 7) ← (A) (A) ← ((PC))	Move data in the current page into the Accumulator.	1	0	1	0	0	0	1	1	2	1	
XCH A, Rr	(A) ⇄ (Rr); r = 0 - 7	Exchange the Accumulator and designated register's contents.	0	0	1	0	1	r	r	r	1	1	
XCH A, @ Rr	(A) ⇄ ((Rr)); r = 0 - 1	Exchange Indirect contents of Accumulator and location in data memory.	0	0	1	0	0	0	0	r	1	1	
XCHD A, @ Rr	(A 0 - 3) ⇄ ((Rr)) 0 - 3)); r = 0 - 1	Exchange Indirect 4-bit contents of Accumulator and data memory.	0	0	1	1	0	0	0	r	1	1	
FLAGS													
CPL C	(C) ← NOT (C)	Complement Content of carry bit.	1	0	1	0	0	1	1	1	1	1	•
CLR C	(C) ← 0	Clear content of carry bit to 0.	1	0	0	1	0	1	1	1	1	1	•
INPUT/OUTPUT													
ANLD Pp, A	(P_p) ← (P_p) AND (A 0 - 3) p = 4 - 7	Logical and contents of Accumulator with designated port (4 – 7).	1	0	0	1	1	1	p	p	2	1	
IN A, P_p	(A) ← (P_p); p = 1 - 2	Input data from designated port (1 - 2) into Accumulator.	0	0	0	0	1	0	p	p	2	1	
MOVD A, P_p	(A 0 - 3) ← (P_p); p = 4 - 7 (A 4 - 7) ← 0	Move contents of designated port (4 - 7) into Accumulator.	0	0	0	0	1	1	p	p	2	1	
MOVD P_p, A	(P_p) ← A 0 - 3; p = 4 - 7	Move contents of Accumulator to designated port (4 - 7).	0	0	1	1	1	1	p	p	1	1	
ORLD P_p, A	(P_p) ← (P_p) OR (A 0 - 3) p = 4 - 7	Logical or contents of Accumulator with designated port (4 - 7).	1	0	0	0	1	1	p	p	1	1	
OUTL P_p, A	(P_p) ← (A); p = 1 - 2	Output contents of Accumulator to designated port (1 - 2).	0	0	1	1	1	0	p	p	1	1	
REGISTERS													
INC Rr	(Rr) ← (Rr) + 1; r = 0 - 7	Increment by 1 contents of designated register.	0	0	0	1	1	r	r	r	1	1	
INC @ Rr	((Rr)) ← ((Rr)) + 1; r = 0 - 1	Increment Indirect by 1 the contents of data memory location.	0	0	0	1	0	0	0	r	1	1	
SUBROUTINE													
CALL addr	((SP)) ← (PC), (PSW 4 - 7) (SP) ← (SP) + 1 (PC 8 - 10) ← addr 8 - 10 (PC 0 - 7) ← addr 0 - 7 (PC 11) ← DBF	Call designated Subroutine.	a_{10} a_7	a_9 a_6	a_8 a_5	1 a_4	0 a_3	1 a_2	0 a_1	0 a_0	2	2	
RET	(SP) ← (SP) - 1 (PC) ← ((SP))	Return from Subroutine without restoring Program Status Word.	1	0	0	0	0	0	1	1	2	1	
TIMER/COUNTER													
MOV A, T	(A) ← (T)	Move contents of Timer/Counter into Accumulator.	0	1	0	0	0	0	1	0	1	1	
MOV T, A	(T) ← (A)	Move contents of Accumulator into Timer/Counter.	0	1	1	0	0	0	1	0	1	1	
STOP TCNT		Stop Count for Event Counter.	0	1	1	0	0	1	0	1	1	1	
STRT CNT		Start Count for Event Counter.	0	1	0	0	0	1	0	1	1	1	
STRT T		Start Count for Timer.	0	1	0	1	0	1	0	1	1	1	
MISCELLANEOUS													
NOP		No Operation performed.	0	0	0	0	0	0	0	0	1	1	

Notes: ① Instruction Code Designations r and p form the binary representation of the Registers and Ports involved.
② The dot under the appropriate flag bit indicates that its content is subject to change by the instruction it appears in.
③ References to the address and data are specified in bytes 2 and/or 1 of the instruction.
④ Numerical Subscripts appearing in the FUNCTION column reference the specific bits affected.

Symbol Definitions

SYMBOL	DESCRIPTION
A	The Accumulator
addr	Program Memory Address (12 bits)
C	Carry Flag
CLK	Clock Signal
CNT	Event Counter
D	Nibble Designator (4 bits)
data	Number or Expression (8 bits)
P	"In-Page" Operation Designator
P_p	Port Designator (p = 1, 2 or 4 - 7)
Rr	Register Designator (r = 0, 1 or 0 - 7)

SYMBOL	DESCRIPTION
T	Timer
T_1	Testable Flag 1
X	External RAM
=	Prefix for Immediate Data
@	Prefix for Indirect Address
$	Program Counter's Current Value
(x)	Contents of External RAM Location
((x))	Contents of Memory Location Addressed by the Contents of External RAM Location
←	Replaced By

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UNIVERSAL PROGRAMMABLE PERIPHERAL INTERFACE 8-BIT MICROCOMPUTERS

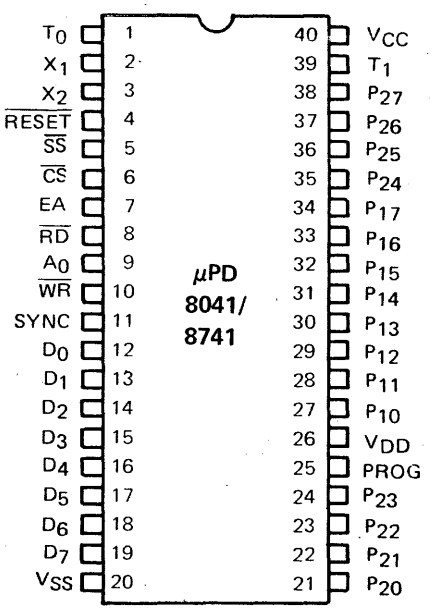
DESCRIPTION

The μPD8041 and μPD8741 are 8-bit single component microcomputers which function as general purpose programmable interfaces between the host processor and many various peripheral devices. The μPD8041 and μPD8741 differ only in their internal program memories. The μPD8041 contains 1024 x 8 bytes of mask ROM, while the μPD8741 contains 1024 x 8 bytes of UV EPROM. Some of the features offered by both devices include 64 x 8 bytes of RAM data memory, an 8-bit programmable counter/timer, 16 TTL compatible I/O lines, and two test inputs.

FEATURES

- Fully Compatible with 8080A, 8085A, and 8048 Families
- Single +5V Supply
- Fully Compatible ROM and EPROM Versions
- 1024 x 8 ROM/EPROM, 64 x 8 RAM
- 18 Programmable I/O Lines
- Expandable I/O
- Two Single Level Interrupts
- Single Package: 8-Bit Processor, ROM, RAM, Timer, I/O and Clock
- Asynchronous Data Register for Master Processor Interface
- Available in Both Plastic and Ceramic 40-Pin Packages

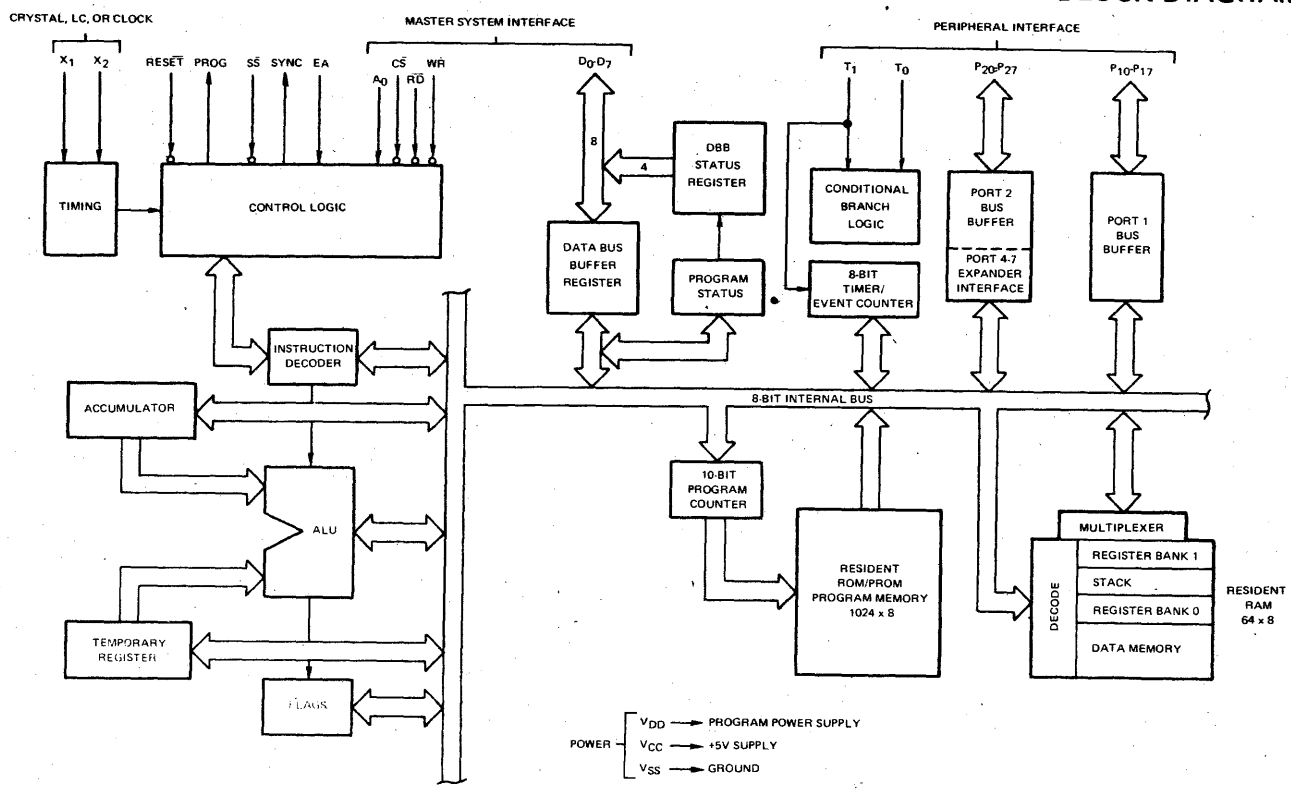
PIN CONFIGURATION



*All data pertaining to the μPD8741 is preliminary.

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BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	0°C to +70°C
Storage Temperature (Ceramic Package)	−65°C to +150°C
Storage Temperature (Plastic Package)	−65°C to +125°C
Voltage on Any Pin	−0.5 to +7 Volts ①
Power Dissipation	1.5 Watt

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note: ① With respect to ground.

*T_a = 25°C

DC CHARACTERISTICS

T_a = 0°C to +70°C; $V_{DD} = V_{CC}$ = +5V ± 5%; V_{SS} = 0V

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input Low Voltage (All except X_1 and X_2)	V_{IL}	−0.5		+0.8	V	
Input High Voltage (All except X_1, X_2, $\overline{RESET}$)	V_{IH1}	2.0		V_{CC}	V	
Input High Voltage (X_1, X_2, $\overline{RESET}$)	V_{IH2}	3.0		V_{CC}	V	
Output Low Voltage (D_0-D_7, SYNC)	V_{OL1}			0.45	V	I_{OL} = 2.0 mA
Output Low Voltage (All other outputs except PROG)	V_{OL2}			0.45	V	I_{OL} = 1.6 mA
Output Low Voltage (PROG)	V_{OL3}			0.45	V	I_{OL} = 1.0 mA
Output High Voltage (D_0-D_7)	V_{OH1}	2.4			V	I_{OH} = −400 μA
Output High Voltage (All other outputs)	V_{OH2}	2.4			V	I_{OH} = −50 μA
Input Leakage Current (T_0, T_1, $\overline{RD}$, $\overline{WR}$, $\overline{CS}$, EA, A_0)	I_{IL}			±10	μA	$V_{SS} < V_{IN} < V_{CC}$
Output Leakage Current (D_0-D_7; High Z State)	I_{OL}			±10	μA	V_{SS} + 0.45 < $V_{IN} < V_{CC}$
V_{DD} Supply Current	I_{DD}			25	mA	
Total Supply Current	$I_{CC} + I_{DD}$			135	mA	
Low Input Source Current (P_{10}-P_{17}; P_{20}-P_{27})	I_{LI1}			0.4	mA	V_{IL} = 0.8V
Low Input Source Current (SS; $\overline{RESET}$)	I_{LI2}			0.2	mA	V_{IL} = 0.8V

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PIN IDENTIFICATION

PIN NO.	PIN SYMBOL	FUNCTION
1,39	T_0, T_1	Testable input pins using conditional transfer functions JT0, JNT0, JT1, JNT1. T_1 can be made the counter/timer input using the STRT CNT instruction. The PROM programming and verification on the 8741 uses T_0.
2	X_1	One side of the crystal input for external oscillator or frequency source.
3	X_2	The other side of the crystal input.
4	$\overline{RESET}$	Active-low input for processor initialization. $\overline{RESET}$ is also used for PROM programming, verification, and power down.
5	$\overline{SS}$	Single Step input (active-low). $\overline{SS}$ together with SYNC output allows the μPD8741 to "single-step" through each instruction in program memory.
6	$\overline{CS}$	Chip Select input (active-low). $\overline{CS}$ is used to select the appropriate μPD8041/8741 on a common data bus.
7	EA	External Access input (active-h[illegible]). A logic "1" at this input commands the μPD8041/8741 to perform all program memory fetches from external memory.
8	$\overline{RD}$	Read strobe input (active-low). $\overline{RD}$ will pulse low when the master processor reads data and status words from the DATA BUS BUFFER or Status Register.
9	A_0	Address input which the master processor uses to indicate if a byte transfer is a command or data.
10	$\overline{WR}$	Write strobe input (active-low). $\overline{WR}$ will pulse low when the master processor writes data or status words to the DATA BUS BUFFER or Status Register.
11	SYNC	The SYNC output pulses once for each μPD8041/8741 instruction cycle. It can function as a strobe for external circuitry. SYNC can also be used together with $\overline{SS}$ to "single-step" through each instruction in program memory.
12-19	D_0-D_7 BUS	The 8-bit, bi-directional, tri-state DATA BUS BUFFER lines by which the μPD8041/8741 interfaces to the 8-bit master system data bus.
20	V_{SS}	Processor's ground potential.
21-24, 35-38	P_{20}-P_{27}	PORT 2 is the second of two 8-bit, quasi-bi-directional I/O ports. P_{20}-P_{23} contain the four most significant bits of the program counter during external memory fetches. P_{20}-P_{23} also serve as a 4-bit I/O bus for the μPD8243, INPUT/OUTPUT EXPANDER.
25	PROG	Program Pulse. PROG is used in programming the μPD8741. It is also used as an output strobe for the μPD8243.
26	V_{DD}	V_{DD} is the programming supply voltage for programming the μPD8741. It is +5V for normal operation of the μPD8041/8741. V_{DD} is also the Low Power Standby input for the ROM version.
27-34	P_{10}-P_{17}	PORT 1 is the first of two 8-bit quasi-bi-directional I/O ports.
40	V_{CC}	Primary power supply. V_{CC} must be +5V for programming and operation of the μPD8741 and for the operation of the μPD8041.

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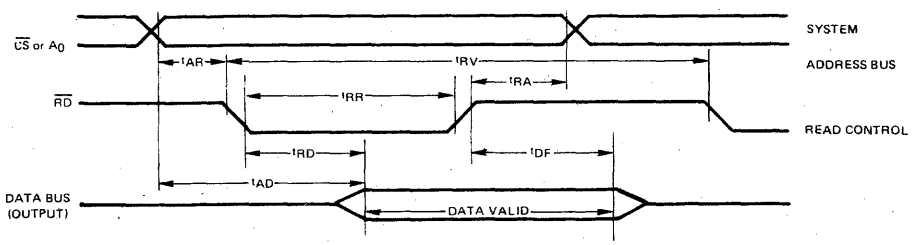
AC CHARACTERISTICS

T_a = 0°C to +70°C; V_{DD} = V_{CC} = +5V; V_{SS} = 0V

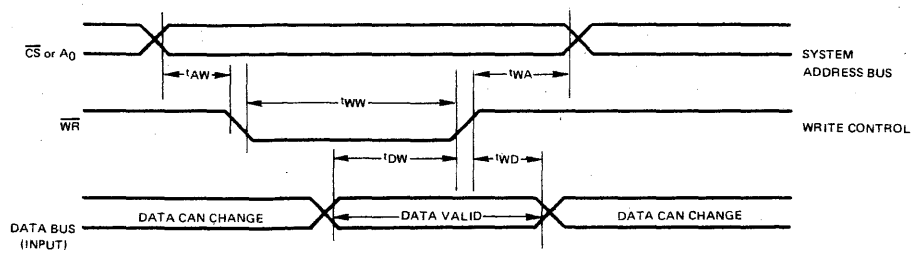
PARAMETER	SYMBOL	LIMITS μPD8041 MIN	LIMITS μPD8041 MAX	LIMITS μPD8741 MIN	LIMITS μPD8741 MAX	UNITS	TEST CONDITIONS
DBB READ							
$\overline{CS}$, A_0 Setup to $\overline{RD}$ ↓	t_{AR}	0		60		ns	
$\overline{CS}$, A_0 Hold after $\overline{RD}$ ↑	t_{RA}	0		30		ns	
$\overline{RD}$ Pulse Width	t_{RR}	250		300	2 x t_{CY}	ns	t_{CY} = 2.5 μs
$\overline{CS}$, A_0 to Data Out Delay	t_{AD}		150		370	ns	
$\overline{RD}$ ↓ to Data Out Delay	t_{RD}		150		200	ns	
$\overline{RD}$ ↑ to Data Float Delay	t_{DF}	10		10		ns	
			100		140	ns	
Recovery Time between Reads and/or Writes	t_{RV}	1		1		μs	
Cycle Time	t_{CY}	2.5		2.5		μs	6 MHz Crystal
DBB WRITE							
$\overline{CS}$, A_0 Setup to $\overline{WR}$ ↓	t_{AW}	0		60		ns	
$\overline{CS}$, A_0 Hold after $\overline{WR}$ ↑	t_{WA}	0		30		ns	
$\overline{WR}$ Pulse Width	t_{WW}	250		300	2 x t_{CY}	ns	t_{CY} = 2.5 μs
Data Setup to $\overline{WR}$ ↑	t_{DW}	150		250		ns	
Data Hold after $\overline{WR}$ ↑	t_{WD}	0		30		ns	

TIMING WAVEFORMS

READ OPERATION – DATA BUS BUFFER REGISTER

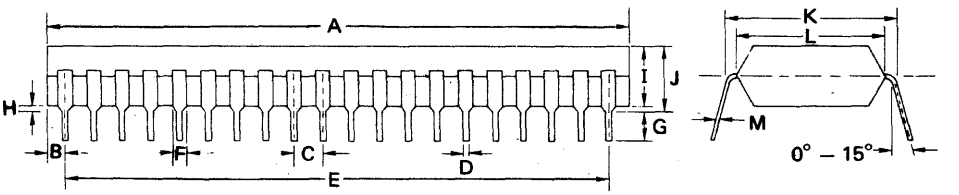


WRITE OPERATION – DATA BUS BUFFER REGISTER



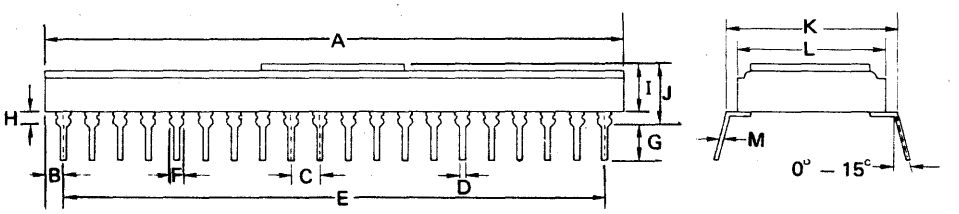
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PACKAGE OUTLINE
μPD8041C/D
μPD8741C/D



(Plastic)

ITEM	MILLIMETERS	INCHES
A	51.5 MAX	2.028 MAX
B	1.62	0.064
C	2.54 ± 0.1	0.10 ± 0.004
D	0.5 ± 0.1	0.019 ± 0.004
E	48.26	1.9
F	1.2 MIN	0.047 MIN
G	2.54 MIN	0.10 MIN
H	0.5 MIN	0.019 MIN
I	5.22 MAX	0.206 MAX
J	5.72 MAX	0.225 MAX
K	15.24	0.600
L	13.2	0.520
M	$0.25^{+0.1}_{-0.05}$	$0.010^{+0.004}_{-0.002}$



(Ceramic)

ITEM	MILLIMETERS	INCHES
A	51.5 MAX	2.028 MAX
B	1.62	0.064
C	2.54 ± 0.1	0.100 ± 0.004
D	0.50 ± 0.1	0.0197 ± 0.004
E	48.26 ± 0.2	1.900 ± 0.008
F	1.27	0.050
G	3.2 MIN	0.126 MIN
H	1.0 MIN	0.04 MIN
I	4.2 MAX	0.17 MAX
J	5.2 MAX	0.205 MAX
K	15.24 ± 0.1	0.6 ± 0.004
L	$13.5^{+0.2}_{-0.25}$	$0.531^{+0.008}_{-0.010}$
M	0.30 ± 0.1	0.012 ± 0.004

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MNEMONIC	FUNCTION	DESCRIPTION	INSTRUCTION CODE D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	CYCLES	BYTES	FLAGS C	AC	F0	F1	IBF	OBF
ACCUMULATOR																		
ADD A, = data	(A) ← (A) + data	Add Immediate the specified Data to the Accumulator.	0	0	0	0	0	0	1	1	2	2	•					
			d_7	d_6	d_5	d_4	d_3	d_2	d_1	d_0								
ADD A, Rr	(A) ← (A) + (Rr) for r = 0 – 7	Add contents of designated register to the Accumulator.	0	1	1	0	1	r	r	r	1	1	•					
ADD A, @ Rr	(A) ← (A) + ((Rr)) for r = 0 – 1	Add Indirect the contents the data memory location to the Accumulator.	0	1	1	0	0	0	0	r	1	1	•					
ADDC A, = data	(A) ← (A) + (C) + data	Add Immediate with carry the specified data to the Accumulator.	0	0	0	1	0	0	1	1	2	2	•					
			d_7	d_6	d_5	d_4	d_3	d_2	d_1	d_0								
ADDC A, Rr	(A) ← (A) + (C) + (Rr) for r = 0 – 7	Add with carry the contents of the designated register to the Accumulator.	0	1	1	1	1	r	r	r	1	1	•					
ADDC A, @ Rr	(A) ← (A) + (C) + ((Rr)) for r = 0 – 1	Add Indirect with carry the contents of data memory location to the Accumulator.	0	1	1	1	0	0	0	r	1	1	•					
ANL A, = data	(A) ← (A) AND data	Logical and specified Immediate Data with Accumulator.	0	1	0	1	0	0	1	1	2	2						
			d_7	d_6	d_5	d_4	d_3	d_2	d_1	d_0								
ANL A, Rr	(A) ← (A) AND (Rr) for r = 0 – 7	Logical and contents of designated register with Accumulator.	0	1	0	1	1	r	r	r	1	1						
ANL A, @ Rr	(A) ← (A) AND ((Rr)) for r = 0 – 1	Logical and Indirect the contents of data memory with Accumulator.	0	1	0	1	0	0	0	r	1	1						
CPL A	(A) ← NOT (A)	Complement the contents of the Accumulator.	0	0	1	1	0	1	1	1	1	1						
CLR A	(A) ← 0	CLEAR the contents of the Accumulator.	0	0	1	0	0	1	1	1	1	1						
DA A		DECIMAL ADJUST the contents of the Accumulator.	0	1	0	1	0	1	1	1	1	1	•					
DEC A	(A) ← (A) – 1	DECREMENT by 1 the accumulator's contents.	0	0	0	0	0	1	1	1	1	1						
INC A	(A) ← (A) + 1	Increment by 1 the accumulator's contents.	0	0	0	1	0	1	1	1	1	1						
ORL A, = data	(A) ← (A) OR data	Logical OR or specified immediate data with Accumulator	0	1	0	0	0	0	1	1	2	2						
			d_7	d_6	d_5	d_4	d_3	d_2	d_1	d_0								
ORL A, Rr	(A) ← (A) OR (Rr) for r = 0 – 7	Logical OR contents of designated register with Accumulator.	0	1	0	0	1	r	r	r	1	1						
ORL A, @ Rr	(A) ← (A) OR ((Rr)) for r = 0 – 1	Logical OR Indirect the contents of data memory location with Accumulator.	0	1	0	0	0	0	0	r	1	1						
RL A	(AN + 1) ← (AN) (A_0) ← (A_7) for N = 0 – 6	Rotate Accumulator left by 1-bit without carry.	1	1	1	0	0	1	1	1	1	1						
RLC A	(AN + 1) ← (AN); N = 0 – 6 (A_0) ← (C) (C) ← (A_7)	Rotate Accumulator left by 1-bit through carry.	1	1	1	1	0	1	1	1	1	1	•					
RR A	(AN) ← (AN + 1); N = 0 – 6 (A_7) ← (A_0)	Rotate Accumulator right by 1-bit without carry.	0	1	1	1	0	1	1	1	1	1						
RRC A	(AN) ← (AN + 1); N = 0 – 6 (A_7) ← (C) (C) ← (A_0)	Rotate Accumulator right by 1-bit through carry.	0	1	1	0	0	1	1	1	1	1	•					
SWAP A	(A_{4-7}) ⇄ (A_0 – 3)	Swap the 2 4-bit nibbles in the Accumulator.	0	1	0	0	0	1	1	1	1	1						
XRL A, = data	(A) ← (A) XOR data	Logical XOR specified immediate data with Accumulator.	1	1	0	1	0	0	1	1	2	2						
			d_7	d_6	d_5	d_4	d_3	d_2	d_1	d_0								
XRL A, Rr	(A) ← (A) XOR (Rr) for r = 0 – 7	Logical XOR contents of designated register with Accumulator.	1	1	0	1	1	r	r	r	1	1						
XRL A, @ Rr	(A) ← (A) XOR ((Rr)) for r = 0 – 1	Logical XOR Indirect the contents of data memory location with Accumulator.	1	1	0	1	0	0	0	r	1	1						
BRANCH																		
DJNZ Rr, addr	(Rr) ← (Rr) – 1; r = 0 – 7 If (Rr) ≠ 0: (PC 0 – 7) ← addr	Decrement the specified register and test contents.	1	1	1	0	1	r	r	r	2	2						
			a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0								
JBb addr	(PC 0 – 7) ← addr if Bb = 1 (PC) ← (PC) + 2 if Bb = 0	Jump to specified address if Accumulator bit is set.	b_2	b_1	b_0	1	0	0	1	0	2	2						
			a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0								
JC addr	(PC 0 – 7) ← addr if C = 1 (PC) ← (PC) + 2 if C = 0	Jump to specified address if carry flag is set.	1	1	1	1	0	1	1	0	2	2						
			a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0								
JF0 addr	(PC 0 – 7) ← addr if F0 = 1 (PC) ← (PC) + 2 if F0 = 0	Jump to specified address if Flag F0 is set.	1	0	1	1	0	1	1	0	2	2						
			a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0								
JF1 addr	(PC 0 – 7) ← addr if F1 = 1 (PC) ← (PC) + 2 if F1 = 0	Jump to specified address if Flag F1 is set.	0	1	1	1	0	1	1	0	2	2						
			a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0								
JMP addr	(PC 8 – 10) ← addr 8 – 10 (PC 0 – 7) ← addr 0 – 7 (PC 11) ← DBF	Direct Jump to specified address within the 2K address block.	a_{10}	a_9	a_8	0	0	1	0	0	2	2						
			a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0								
JMPP @ A	(PC 0 – 7) ← ((A))	Jump indirect to specified address with with address page.	1	0	1	1	0	0	1	1	2	1						
JNC addr	(PC 0 – 7) ← addr if C = 0 (PC) ← (PC) + 2 if C = 1	Jump to specified address if carry flag is low.	1	1	1	0	0	1	1	0	2	2						
			a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0								
JNIBF addr	(PC 0 – 7) ← addr if IBF = (PC) ← (PC) + 2 if IBF = 1	Jump to specified address if input buffer full flag is low.	1	1	0	1	0	1	1	0	2	2						
			a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0								
JOBF	(PC 0 – 7) ← addr if OBF = 1 (PC) ← (PC) + 2 if OBF = 0	Jump to specified address if output buffer full flag is set.	1	0	0	0	0	1	1	0	2	2						
			a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0								

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MNEMONIC	FUNCTION		INSTRUCTION CODE D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	CYCLES	BYTES	FLAGS C	AC	F0	F1	IBF	OBF
BRANCH (CONT.)																		
JNT0 addr	(PC 0 – 7) ← addr if T0 = 0 (PC) ← (PC) + 2 if T0 = 1	Jump to specified address if Test 0 is low.	0 a_7	0 a_6	1 a_5	0 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2						
JNT1 addr	(PC 0 – 7) ← addr if T1 = 0 (PC) ← (PC) + 2 if T1 = 1	Jump to specified address if Test 1 is low.	0 a_7	1 a_6	0 a_5	0 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2						
JNZ addr	(PC 0 – 7) ← addr if A ≠ 0 (PC) ← (PC) + 2 if A = 0	Jump to specified address if accumulator is non-zero.	1 a_7	0 a_6	0 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2						
JTF addr	(PC 0 – 7) ← addr if TF = 1 (PC) ← (PC) + 2 if TF = 0	Jump to specified address if Timer Flag is set to 1.	0 a_7	0 a_6	0 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2						
JT0 addr	(PC 0 – 7) ← addr if T0 = 1 (PC) ← (PC) + 2 if T0 = 0	Jump to specified address if Test 0 is a 1.	0 a_7	0 a_6	1 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2						
JT1 addr	(PC 0 – 7) ← addr if T1 = 1 (PC) ← (PC) + 2 if T1 = 0	Jump to specified address if Test 1 is a 1.	0 a_7	1 a_6	0 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2						
JZ addr	(PC 0 – 7) ← addr if A = 0 (PC) ← (PC) + 2 if A ≠ 0	Jump to specified address if Accumulator is 0.	1 a_7	1 a_6	0 a_5	0 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2						
CONTROL																		
EN I		Enable the External Interrupt input.	0	0	0	0	0	1	0	1	1	1						
DIS I		Disable the External Interrupt input.	0	0	0	1	0	1	0	1	1	1						
SEL RB0	(BS) ← 0	Select Bank 0 (locations 0 – 7) of Data Memory.	1	1	0	0	0	1	0	1	1	1						
SEL RB1	(BS) ← 1	Select Bank 1 (locations 24 – 31) of Data Memory.	1	1	0	1	0	1	0	1	1	1						
DATA MOVES																		
MOV A, = data	(A) ← data	Move Immediate the specified data into the Accumulator.	0 d_7	0 d_6	1 d_5	0 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2						
MOV A, Rr	(A) ← (Rr); r = 0 – 7	Move the contents of the designated registers into the Accumulator.	1	1	1	1	1	r	r	r	1	1						
MOV A, @ Rr	(A) ← ((Rr)); r = 0 – 1	Move Indirect the contents of data memory location into the Accumulator.	1	1	1	1	0	0	0	r	1	1						
MOV A, PSW	(A) ← (PSW)	Move contents of the Program Status Word into the Accumulator.	1	1	0	0	0	1	1	1	1	1						
MOV Rr, = data	(Rr) ← data; r = 0 – 7	Move Immediate the specified data into the designated register.	1 d_7	0 d_6	1 d_5	1 d_4	1 d_3	r d_2	r d_1	r d_0	2	2						
MOV Rr, A	(Rr) ← (A); r = 0 – 7	Move Accumulator Contents into the designated register.	1	0	1	0	1	r	r	r	1	1						
MOV @ Rr, A	((Rr)) ← (A); r = 0 – 1	Move Indirect Accumulator Contents into data memory location.	1	0	1	0	0	0	0	r	1	1						
MOV @ Rr, = data	((Rr)) ← data; r = 0 – 1	Move Immediate the specified data into data memory.	1 d_7	0 d_6	1 d_5	1 d_4	0 d_3	0 d_2	0 d_1	r d_0	2	2						
MOV PSW, A	(PSW) ← (A)	Move contents of Accumulator into the program status word.	1	1	0	1	0	1	1	1	1	1						
MOVP A, @ A	(PC 0 – 7) ← (A) (A) ← ((PC))	Move data in the current page into the Accumulator.	1	0	1	0	0	0	1	1	2	1						
MOVP3 A, @ A	(PC 0 – 7) ← (A) (PC 8 – 10) ← 011 (A) ← ((PC))	Move Program data in Page 3 into the Accumulator.	1	1	1	0	0	0	1	1	2	1						
XCH A, Rr	(A) ⇄ (Rr); r = 0 – 7	Exchange the Accumulator and designated register's contents.	0	0	1	0	1	r	r	r	1	1						
XCH A, @ Rr	(A) ⇄ ((Rr)); r = 0 – 1	Exchange Indirect contents of Accumulator and location in data memory.	0	0	1	0	0	0	0	r	1	1						
XCHD A, @ Rr	(A 0 – 3) ⇄ ((Rr)) 0 – 3)); r = 0 – 1	Exchange Indirect 4-bit contents of Accumulator and data memory.	0	0	1	1	0	0	0	r	1	1						
FLAGS																		
CPL C	(C) ← NOT (C)	Complement Content of carry bit.	1	0	1	0	0	1	1	1	1	1	•					
CPL F0	(F0) ← NOT (F0)	Complement Content of Flag F0.	1	0	0	1	0	1	0	1	1	1			•			
CPL F1	(F1) ← NOT (F1)	Complement Content of Flag F1	1	0	1	1	0	1	0	1	1	1				•		
CLR C	(C) ← 0	Clear content of carry bit to 0.	1	0	0	1	0	1	1	1	1	1	•					
CLR F0	(F0) ← 0	Clear content of Flag 0 to 0.	1	0	0	0	0	1	0	1	1	1			•			
CLR F1	(F1) ← 0	Clear content of Flag 1 to 0.	1	0	1	0	0	1	0	1	1	1				•		

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MNEMONIC	FUNCTION	DESCRIPTION	INSTRUCTION CODE D7	D6	D5	D4	D3	D2	D1	D0	CYCLES	BYTES	FLAGS C	AC	F0	F1	IBF	OBF
INPUT/OUTPUT																		
ANL Pp, # data	(Pp) ← (Pp) AND data p = 1 – 2	Logical and Immediate specified data with designated port (1 or 2)	1	0	0	1	1	0	p	p	2	2						
			d_7	d_6	d_5	d_4	d_3	d_2	d_1	d_0								
ANLD Pp, A	(Pp) ← (Pp) AND (A 0 – 3) p = 4 – 7	Logical and contents of Accumulator with designated port (4 – 7).	1	0	0	1	1	1	p	p	2	1						
IN A, Pp	(A) ← (Pp); p = 1 – 2	Input data from designated port (1 – 2) into Accumulator.	0	0	0	0	1	0	p	p	2	1						
IN A, DBB	(A) ← (DBB)	Input strobed DBB data into Accumulator and clear IBF	0	0	1	0	0	0	1	0	1	1					•	
MOVD A, Pp	(A 0 – 3) ← (Pp); p = 4 – 7 (A 4 – 7) ← 0	Move contents of designated port (4 – 7) into Accumulator.	0	0	0	0	1	1	p	p	2	1						
MOVD Pp, A	(Pp) ← A 0 – 3; p = 4 – 7	Move contents of Accumulator to designated port (4 – 7).	0	0	1	1	1	1	p	p	1	1						
ORLD Pp, A	(Pp) ← (Pp) OR (A 0 – 3) p = 4 – 7	Logical or contents of Accumulator with designated port (4 – 7).	1	0	0	0	1	1	p	p	1	1						
ORL Pp, # data	(Pp) ← (Pp) OR data p = 1 – 2	Logical or Immediate specified data with designated port (1 – 2)	1	0	0	0	1	0	p	p	2	2						
			d_7	d_6	d_5	d_4	d_3	d_2	d_1	d_0								
OUT DBB, A	(DBB) (A)	Output contents of Accumulator onto DBB and set OBF.	0	0	0	0	0	0	1	0	1	1						•
OUTL Pp, A	(Pp) ← (A); p = 1 – 2	Output contents of Accumulator to designated port (1 – 2).	0	0	1	1	1	0	p	p	1	1						
REGISTERS																		
DEC Rr (Rr)	(Rr) ← (Rr) – 1; r = 0 – 7	Decrement by 1 contents of designated register.	1	1	0	0	1	r	r	r	1	1						
INC Rr	(Rr) ← (Rr) +1; r = 0 – 7	Increment by 1 contents of designated register.	0	0	0	1	1	r	r	r	1	1						
INC @ Rr	((Rr)) ← ((Rr)) + 1; r = 0 – 1	Increment Indirect by 1 the contents of data memory location.	0	0	0	1	0	0	0	r	1	1						
SUBROUTINE																		
CALL addr	((SP)) ← (PC), (PSW 4 – 7) (SP) ← (SP) + 1 (PC 8 – 10) ← addr 8 – 10 (PC 0 – 7) ← addr 0 – 7 (PC 11) ← DBF	Call designated Subroutine.	a_{10}	a_9	a_8	1	0	1	0	0	2	2						
			a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0								
RET	(SP) ← (SP) – 1 (PC) ← ((SP))	Return from Subroutine without restoring Program Status Word.	1	0	0	0	0	0	1	1	2	1						
RETR	(SP) ← (SP) – 1 (PC) ← ((SP)) (PSW 4 – 7) ← ((SP))	Return from Subroutine restoring Program Status Word.	1	0	0	1	0	0	1	1	2	1						
TIMER/COUNTER																		
EN TCNTI		Enable Internal interrupt Flag for Timer/Counter output.	0	0	1	0	0	1	0	1	1	1						
DIS TCNTI		Disable Internal interrupt Flag for Timer/Counter output.	0	0	1	1	0	1	0	1	1	1						
MOV A, T	(A) ← (T)	Move contents of Timer/Counter into Accumulator.	0	1	0	0	0	0	1	0	1	1						
MOV T, A	(T) ← (A)	Move contents of Accumulator into Timer/Counter.	0	1	1	0	0	0	1	0	1	1						
STOP TCNT		Stop Count for Event Counter.	0	1	1	0	0	1	0	1	1	1						
STRT CNT		Start Count for Event Counter.	0	1	0	0	0	1	0	1	1	1						
STRT T		Start Count for Timer.	0	1	0	1	0	1	0	1	1	1						
MISCELLANEOUS																		
NOP		No Operation performed.	0	0	0	0	0	0	0	0	1	1						

Notes: ① Instruction Code Designations r and p form the binary representation of the Registers and Ports involved.

② The dot under the appropriate flag bit indicates that its content is subject to change by the instruction it appears in.

③ References to the address and data are specified in bytes 2 and/or 1 of the instruction.

④ Numerical Subscripts appearing in the FUNCTION column reference the specific bits affected.

Symbol Definitions:

SYMBOL	DESCRIPTION
A	The Accumulator
AC	The Auxiliary Carry Flag
addr	Program Memory Address (12 bits)
Bb	Bit Designator (b = 0 – 7)
BS	The Bank Switch
BUS	The BUS Port
C	Carry Flag
CLK	Clock Signal
CNT	Event Counter
D	Nibble Designator (4 bits)
data	Number or Expression (8 bits)
DBF	Memory Bank Flip-Flop
F_0, F_1	Flags 0, 1
I	Interrupt
P	"In-Page" Operation Designator
IBF	Input Buffer Full Flag

SYMBOL	DESCRIPTION
P_p	Port Designator (p = 1, 2 or 4 – 7)
PSW	Program Status Word
Rr	Register Designator (r = 0, 1 or 0 – 7)
SP	Stack Pointer
T	Timer
TF	Timer Flag
T_0, T_1	Testable Flags 0, 1
X	External RAM
#	Prefix for Immediate Data
@	Prefix for Indirect Address
$	Program Counter's Current Value
(x)	Contents of External RAM Location
((x))	Contents of Memory Location Addressed by the Contents of External RAM Location.
←	Replaced By
OBF	Output Buffer Full
DBB	Data Bus Buffer

The information presented in this document is believed to be accurate and reliable. The information is subject to change without notice.

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NEC
μPD8048
μPD8748*
μPD8035

μPD8048 FAMILY OF SINGLE CHIP 8-BIT MICROCOMPUTERS

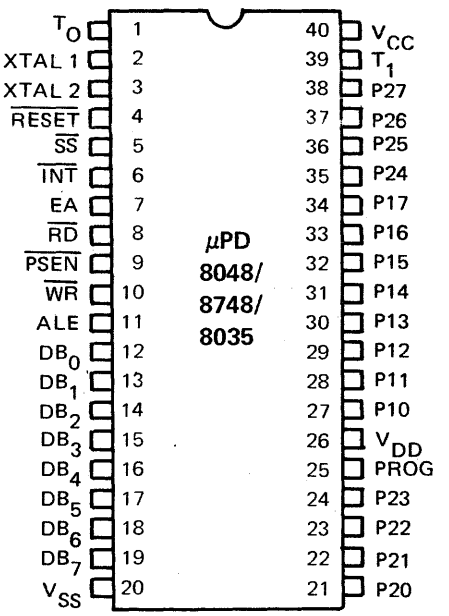
DESCRIPTION

The μPD8048 family of single chip 8-bit microcomputers is comprised of the μPD8048, μPD8748 and μPD8035. The processors in this family differ only in their internal program memory options: the μPD8048 with 1K x 8 bytes of mask ROM, the μPD8748 with 1K x 8 bytes of UV erasable EPROM and the μPD8035 with external memory.

FEATURES

- Fully Compatible With Industry Standard 8048/8748/8035
- NMOS Silicon Gate Technology Requiring a Single +5V Supply
- 2.5 μs Cycle Time. All Instruction 1 or 2 Bytes
- Interval Timer/Event Counter
- 64 x 8 Byte RAM Data Memory
- Single Level Interrupt
- 96 Instructions: 70% Single Byte
- 27 I/O Lines
- Internal Clock Generator
- 8 Level Stack
- Compatible With 8080A/8085A Peripherals
- Available in Both Ceramic and Plastic 40 Pin Packages

PIN CONFIGURATION



*All data pertaining to the μPD8748 is preliminary.

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μPD8048 FAMILY

FUNCTIONAL DESCRIPTION

The NEC μPD8048, μPD8748 and μPD8035 are single component, 8-bit, parallel microprocessors using N-channel silicon gate MOS technology. The μPD8048/8748/8035 efficiently function in control as well as arithmetic applications. The flexibility of the instruction set allows for the direct set and reset of individual data bits within the accumulator and the I/O port structure. Standard logic function implementation is facilitated by the large variety of branch and table look-up instructions.

The μPD8048/8748/8035 instruction set is comprised of 1 and 2 byte instructions with over 70% single-byte and requiring only 1 or 2 cycles per instruction with over 50% single-cycle.

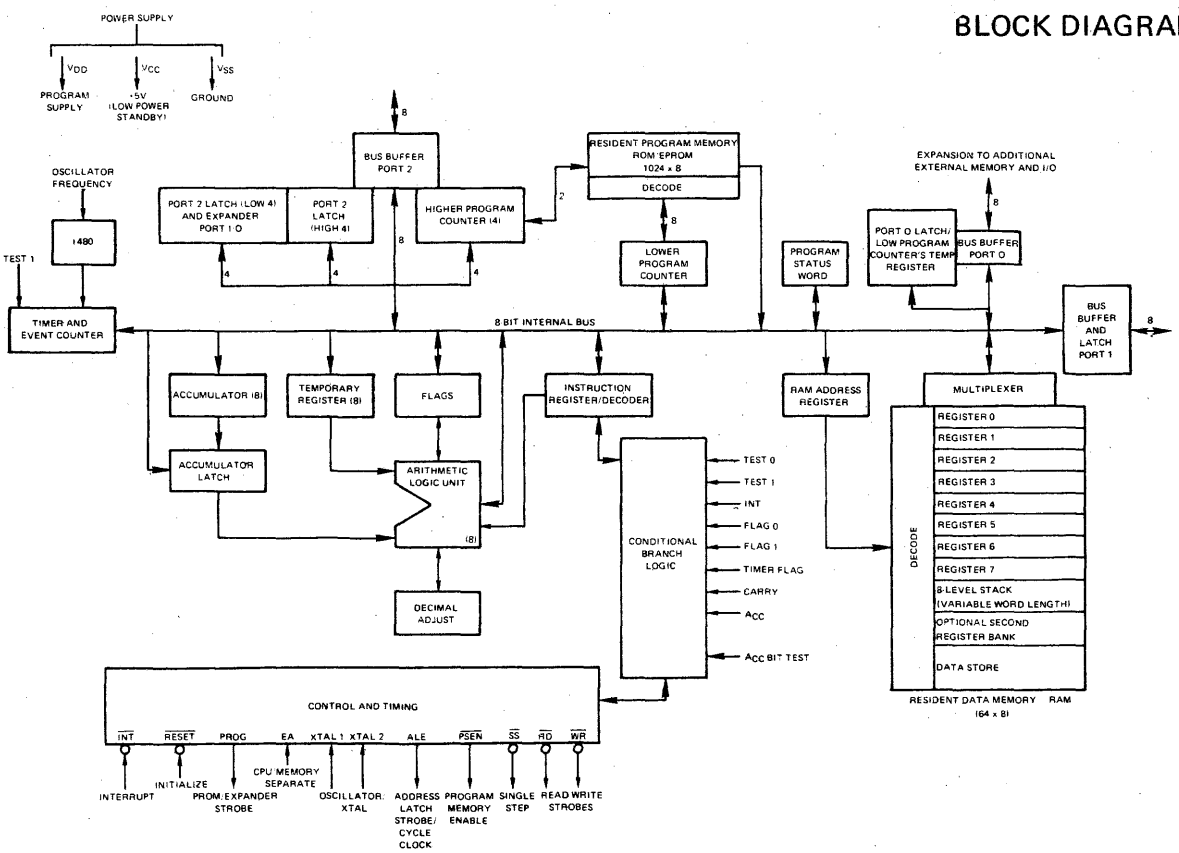
The μPD8048 series of microprocessors will function as stand alone microcomputers. Their functions can easily be expanded using standard 8080A/8085A peripherals and memories.

The μPD8048 contains the following functions usually found in external peripheral devices: 1024 x 8 bits of ROM program memory; 64 x 8 bits of RAM data memory; 27 I/O lines; an 8-bit interval timer/event counter; oscillator and clock circuitry.

The μPD8748 differs from the μPD8048 only in its 1024 x 8-bit UV erasable EPROM program memory instead of the 1024 x 8-bit ROM memory. It is useful in preproduction or prototype applications where the software design has not yet been finalized or in system designs whose quantities do not require a mask ROM.

The μPD8035 is intended for applications using external program memory only. It contains all the features of the μPD8048 except the 1024 x 8-bit internal ROM. The external program memory can be implemented using standard 8080A/8085A memory products.

BLOCK DIAGRAM



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PIN IDENTIFICATION

PIN NO.	PIN SYMBOL	FUNCTION
1	T_0	Testable input using conditional transfer functions JT0 and JNT0. The internal State Clock (CLK) is available to T_0 using the ENTO CLK instruction. T_0 can also be used during programming as a testable flag.
2	XTAL 1	One side of the crystal input for external oscillator or frequency (non TTL compatible V_{IH}).
3	XTAL 2	The other side of the crystal input.
4	$\overline{RESET}$	Active low input for processor initialization. $\overline{RESET}$ is also used for PROM programming verification and power-down (non TTL compatible V_{IH}).
5	$\overline{SS}$	Single Step input (active-low). $\overline{SS}$ together with ALE allows the processor to "single-step" through each instruction in program memory.
6	$\overline{INT}$	Interrupt input (active-low). $\overline{INT}$ will start an interrupt if an enable interrupt instruction has been executed. A reset will disable the interrupt. $\overline{INT}$ can be tested by issuing a conditional jump instruction.
7	EA	External Access input (active-high). A logic "1" at this input commands the processor to perform all program memory fetches from external memory.
8	$\overline{RD}$	READ strobe output (active-low). $\overline{RD}$ will pulse low when the processor performs a BUS READ. $\overline{RD}$ will also enable data onto the processor BUS from a peripheral device and function as a READ STROBE for external DATA MEMORY.
9	$\overline{PSEN}$	Program Store Enable output (active-low). $\overline{PSEN}$ becomes active only during an external memory fetch.
10	$\overline{WR}$	WRITE strobe output (active-low). $\overline{WR}$ will pulse low when the processor performs a BUS WRITE. $\overline{WR}$ can also function as a WRITE STROBE for external DATA MEMORY.
11	ALE	Address Latch Enable output (active-high). Occurring once each cycle, the falling edge of ALE latches the address for external memory or peripherals. ALE can also be used as a clock output.
12 – 19	$D_0 - D_7$ BUS	8-bit, bidirectional port. Synchronous reads and writes can be performed on this port using $\overline{RD}$ and $\overline{WR}$ strobes. The contents of the $D_0 - D_7$ BUS can be latched in a static mode. During an external memory fetch, the $D_0 - D_7$ BUS holds the least significant bits of the program counter. $\overline{PSEN}$ controls the incoming addressed instruction. Also, for an external RAM data store instruction the $D_0 - D_7$ BUS, controlled by ALE, $\overline{RD}$ and $\overline{WR}$, contains address and data information.
20	V_{SS}	Processor's GROUND potential.
21 – 24, 35 – 38	$P_{20} - P_{27}$: PORT 2	Port 2 is the second of two 8-bit quasi-bidirectional ports. For external data memory fetches, the four most significant bits of the program counter are contained in $P_{20} - P_{23}$. Bits $P_{20} - P_{23}$ are also used as a 4-bit I/O bus for the μPD8243, INPUT/OUTPUT EXPANDER.
25	PROG	Program Pulse. A +25V pulse applied to this input is used for programming the μPD8748. PROG is also used as an output strobe for the μPD8243.
26	V_{DD}	Programming Power Supply. V_{DD} must be set to +25V for programming the μPD8748, and to +5V for the ROM and PROM versions for normal operation. V_{DD} functions as the Low Power Standby input for the μPD8048.
27 – 34	$P_{10} - P_{17}$: PORT 1	Port 1 is one of two 8-bit quasi-bidirectional ports.
39	T1	Testable input using conditional transfer functions JT1 and JNT1. T1 can be made the counter/timer input using the STRT CNT instruction.
40	V_{CC}	Primary Power Supply. V_{CC} must be +5V for programming and operation of the μPD8748, and for operation of the μPD8035 and μPD8048.

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ABSOLUTE MAXIMUM RATINGS*

Operating Temperature . . . . . 0°C to +70°C
Storage Temperature (Ceramic Package) . . . . . −65°C to +150°C
Storage Temperature (Plastic Package) . . . . . −65°C to +125°C
Voltage on Any Pin . . . . . − 0.5 to +7 Volts ①
Power Dissipation . . . . . 1.5 W

Note: ① With respect to ground.

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

DC CHARACTERISTICS

T_a = 0°C to +70°C; V_{CC} = V_{DD} = +5V ± 5%; V_{SS} = 0V

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN	TYP	MAX		
Input Low Voltage (All Except XTAL 1, XTAL 2)	V_{IL}	-0.5		0.8	V	
Input High Voltage (All Except XTAL 1, XTAL 2, $\overline{RESET}$)	V_{IH}	2.0		V_{CC}	V	
Input High Voltage (RESET, XTAL 1, XTAL 2)	V_{IH1}	3.0		V_{CC}	V	
Output Low Voltage (BUS, $\overline{RD}$, $\overline{WR}$, $\overline{PSEN}$, ALE)	V_{OL}			0.45	V	I_{OL} = 2.0 mA
Output Low Voltage (All Other Outputs Except PROG)	V_{OL1}			0.45	V	I_{OL} = 1.6 mA
Output Low Voltage (PROG)	V_{OL2}			0.45	V	
Output High Voltage (BUS, $\overline{RD}$, $\overline{WR}$, $\overline{PSEN}$, ALE)	V_{OH}	2.4			V	I_{OH} = −100 μA
Output High Voltage (All Other Outputs)	V_{OH1}	2.4			V	I_{OH} = −50 μA
Input Leakage Current (T_1, EA, INT)	I_{IL}			±10	μA	$V_{SS} \leq V_{IN} \leq V_{CC}$
Output Leakage Current (BUS, T_0 – High Impedance State)	I_{OL}			-10	μA	$V_{CC} \geq V_{IN} \geq V_{SS}$ + 0.45V
Power Down Supply Current	I_{DD}		10	20	mA	T_a = 25°C
Total Supply Current	$I_{DD} + I_{CC}$		65	135	mA	T_a = 25°C

DC CHARACTERISTICS PROGRAMMING THE μPD8748

T_a = 25°C ± 5°C; V_{CC} = +5V ± 5%; V_{DD} = +25V ± 1V

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN	TYP	MAX		
V_{DD} Program Voltage High-Level	V_{DDH}	24.0		26.0	V	
V_{DD} Voltage Low-Level	V_{DDL}	4.75		5.25	V	
PROG Voltage High-Level	V_{PH}	23.5		24.5	V	
PROG Voltage Low-Level	V_{PL}			0.2	V	
EA Program or Verify Voltage High-Level	V_{EAH}	21.5		24.5	V	
EA Voltage Low-Level	V_{EAL}			5.25	V	
V_{DD} High Voltage Supply Current	I_{DD}			30.0	mA	
PROG High Voltage Supply Current	I_{PROG}			16.0	mA	
EA High Voltage Supply Current	I_{EA}			1.0	mA	

PRELIMINARY

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AC CHARACTERISTICS

READ, WRITE AND INSTRUCTION FETCH – EXTERNAL DATA AND PROGRAM MEMORY

T_a = 0°C to +70°C; V_{CC} = V_{DD} = +5V ± 5%; V_{SS} = 0V

PARAMETER	SYMBOL	LIMITS MIN	TYP	MAX	UNIT	TEST CONDITIONS
ALE Pulse Width	t_{LL}	400			ns	
Address Setup before ALE	t_{AL}	150			ns	
Address Hold from ALE	t_{LA}	80			ns	
Control Pulse Width ($\overline{PSEN}$, $\overline{RD}$, $\overline{WR}$)	t_{CC}	900			ns	
Data Setup before $\overline{WR}$	t_{DW}	500			ns	
Data Hold after $\overline{WR}$	t_{WD}	120			ns	C_L = 20 pF
Cycle Time	t_{CY}	2.5		15.0	μs	6 MHz XTAL
Data Hold	t_{DR}	0		200	ns	
$\overline{PSEN}$, $\overline{RD}$ to Data In	t_{RD}			500	ns	
Address Setup before $\overline{WR}$	t_{AW}	230			ns	
Address Setup before Data In	t_{AD}			950	ns	
Address Float to $\overline{RD}$, $\overline{PSEN}$	t_{AFC}	0			ns	

Notes: ① For Control Outputs: C_L = 80 pF
② For Bus Outputs: C_L = 150 pF
③ t_{CY} = 2.5 μs

PORT 2 TIMING

T_a = 0°C to +70°C; V_{CC} = +5V ± 5%

PARAMETER	SYMBOL	LIMITS MIN	TYP	MAX	UNIT	TEST CONDITIONS
Port Control Setup before Falling Edge of $\overline{PROG}$	t_{CP}	110			ns	
Port Control Hold after Falling Edge of $\overline{PROG}$	t_{PC}	140			ns	
$\overline{PROG}$ to Time P2 Input must be Valid	t_{PR}			810	ns	
Output Data Setup Time	t_{DP}	220			ns	
Output Data Hold Time	t_{PD}	65			ns	
Input Data Hold Time	t_{PF}			150	ns	
$\overline{PROG}$ Pulse Width	t_{PP}	1510			ns	
Port 2 I/O Data Setup	t_{PL}	400			ns	
Port 2 I/O Data Hold	t_{LP}	150			ns	

PROGRAMMING SPECIFICATIONS – μPD8748

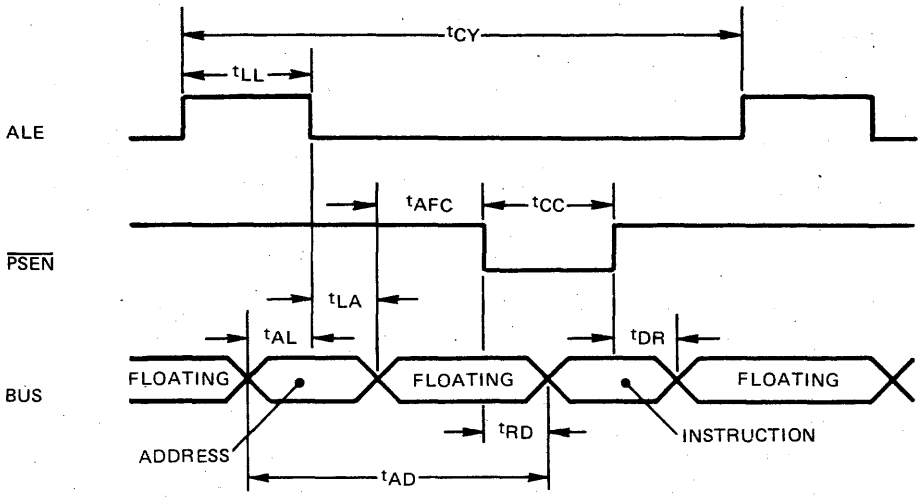
T_a = 25°C ± 5°C; V_{CC} = +5V ± 5%; V_{DD} = +25V ± 1V

PARAMETER	SYMBOL	LIMITS MIN	TYP	MAX	UNIT	TEST CONDITIONS
Address Setup Time before $\overline{RESET}$ ↑	t_{AW}	4 t_{CY}				
Address Hold Time after $\overline{RESET}$ ↑	t_{WA}	4 t_{CY}				
Data In Setup Time before $\overline{PROG}$ ↑	t_{DW}	4 t_{CY}				
Data In Hold Time after $\overline{PROG}$ ↓	t_{WD}	4 t_{CY}				
$\overline{RESET}$ Hold Time to VERIFY	t_{PH}	4 t_{CY}				
V_{DD}	t_{VDDW}	4 t_{CY}				
V_{DD} Hold Time after PROG ↓	t_{VDDH}	0				
Program Pulse Width	t_{PW}	50		60	ms	
Test 0 Setup Time before Program Mode	t_{TW}	4 t_{CY}				
Test 0 Hold Time after Program Mode	t_{WT}	4 t_{CY}				
Test 0 to Data Out Delay	t_{DO}			4 t_{CY}		
$\overline{RESET}$ Pulse Width to Latch Address	t_{WW}	4 t_{CY}				
V_{DD} and $\overline{PROG}$ Rise and Fall Times	t_r, t_f	0.5		2.0	μs	
Processor Operation Cycle Time	t_{CY}	5.0			μs	
$\overline{RESET}$ Setup Time before EA ↑	t_{RE}	4 t_{CY}				

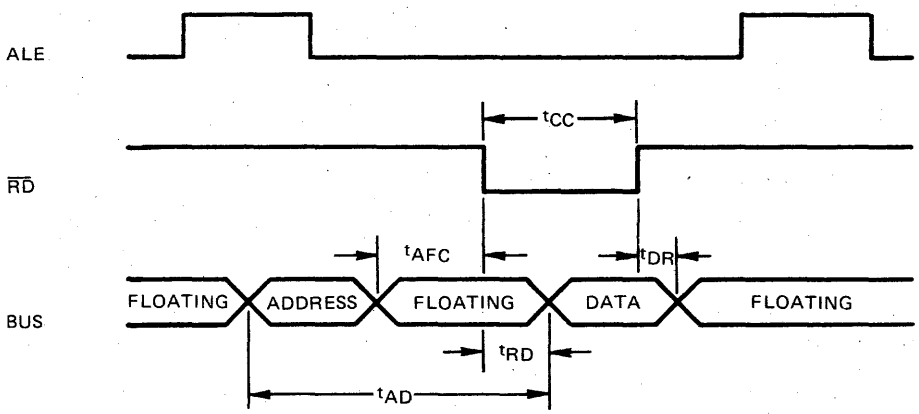
PRELIMINARY

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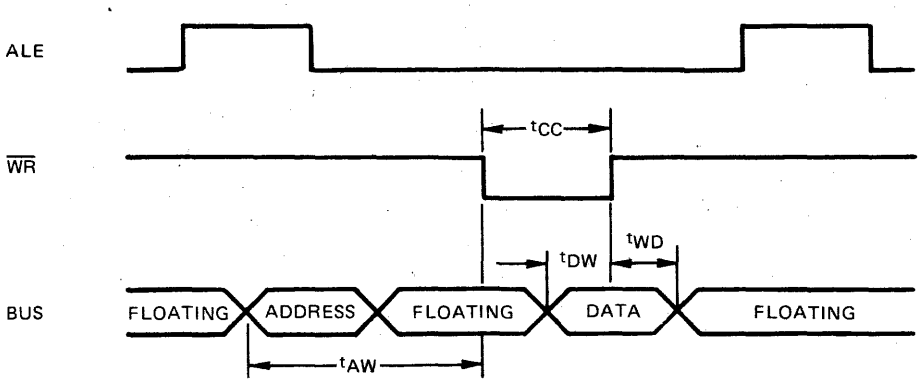
TIMING WAVEFORMS



INSTRUCTION FETCH FROM EXTERNAL MEMORY



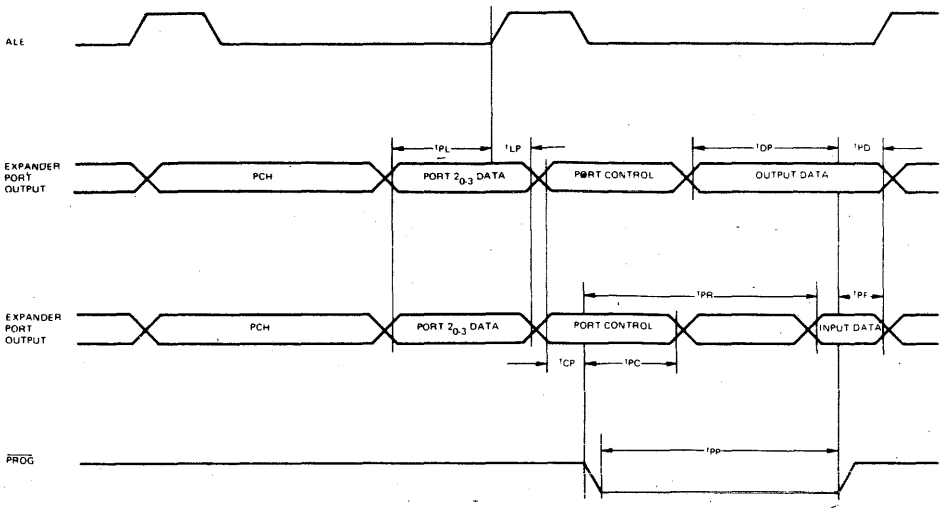
READ FROM EXTERNAL DATA MEMORY



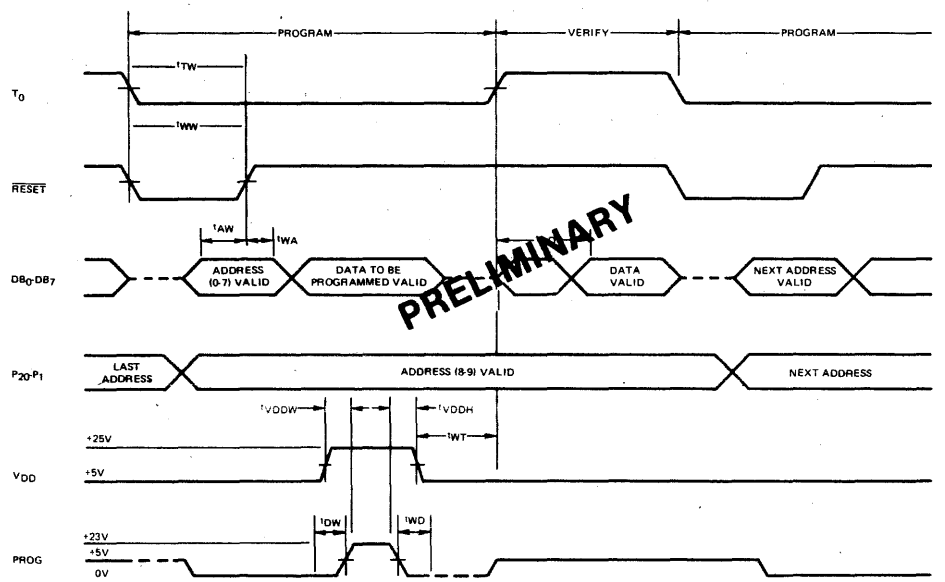
WRITE TO EXTERNAL MEMORY

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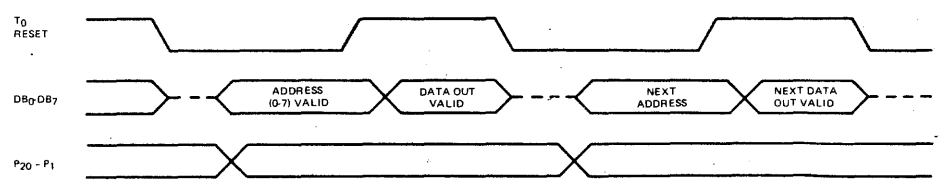
TIMING WAVEFORMS (CONT.)



PORT 2 TIMING



PROGRAM/VERIFY TIMING (μPD8748 ONLY)



VERIFY MODE TIMING (μPD8048/8748 ONLY)

Notes: ① Conditions $\overline{CS}$ TTL Logic "1", A0 TTL Logic "0" must be met. (use 10K resistor to V_{CC} for $\overline{CS}$, and 10K resistor to V_{SS} for A0)

② t_{CY} 5 μs can be achieved using a 3 MHz frequency source (LC, XTAL or external) at the XTAL 1 and XTAL 2 inputs.

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MNEMONIC	FUNCTION	DESCRIPTION	INSTRUCTION CODE D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	CYCLES	BYTES	FLAGS C	AC	F0	F1
ACCUMULATOR																
ADD A, = data	(A) ← (A) + data	Add Immediate the specified Data to the Accumulator.	0 d_7	0 d_6	0 d_5	0 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2	•			
ADD A, Rr	(A) ← (A) + (Rr) for r = 0 – 7	Add contents of designated register to the Accumulator.	0	1	1	0	1	r	r	r	1	1	•			
ADD A, @ Rr	(A) ← (A) + ((Rr)) for r = 0 – 1	Add Indirect the contents the data memory location to the Accumulator.	0	1	1	0	0	0	0	r	1	1	•			
ADDC A, = data	(A) ← (A) + (C) + data	Add Immediate with carry the specified data to the Accumulator.	0 d_7	0 d_6	0 d_5	1 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2	•			
ADDC A, Rr	(A) ← (A) + (C) + (Rr) for r = 0 – 7	Add with carry the contents of the designated register to the Accumulator.	0	1	1	1	1	r	r	r	1	1	•			
ADDC A, @ Rr	(A) ← (A) + (C) + ((Rr)) for r = 0 – 1	Add Indirect with carry the contents of data memory location to the Accumulator.	0	1	1	1	0	0	0	r	1	1	•			
ANL A, = data	(A) ← (A) AND data	Logical and specified Immediate Data with Accumulator.	0 d_7	1 d_6	0 d_5	1 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2				
ANL A, Rr	(A) ← (A) AND (Rr) for r = 0 – 7	Logical and contents of designated register with Accumulator.	0	1	0	1	1	r	r	r	1	1				
ANL A, @ Rr	(A) ← (A) AND ((Rr)) for r = 0 – 1	Logical and Indirect the contents of data memory with Accumulator.	0	1	0	1	0	0	0	r	1	1				
CPL A	(A) ← NOT (A)	Complement the contents of the Accumulator.	0	0	1	1	0	1	1	1	1	1				
CLR A	(A) ← 0	CLEAR the contents of the Accumulator.	0	0	1	0	0	1	1	1	1	1				
DA A		DECIMAL ADJUST the contents of the Accumulator.	0	1	0	1	0	1	1	1	1	1	•			
DEC A	(A) ← (A) – 1	DECREMENT by 1 the accumulator's contents.	0	0	0	0	0	1	1	1	1	1				
INC A	(A) ← (A) + 1	Increment by 1 the accumulator's contents.	0	0	0	1	0	1	1	1	1	1				
ORL A, = data	(A) ← (A) OR data	Logical OR specified immediate data with Accumulator	0 d_7	1 d_6	0 d_5	0 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2				
ORL A, Rr	(A) ← (A) OR (Rr) for r = 0 – 7	Logical OR contents of designated register with Accumulator.	0	1	0	0	1	r	r	r	1	1				
ORL A, @ Rr	(A) ← (A) OR ((Rr)) for r = 0 – 1	Logical OR Indirect the contents of data memory location with Accumulator.	0	1	0	0	0	0	0	r	1	1				
RL A	(AN + 1) ← (AN) (A_0) ← (A_7) for N = 0 – 6	Rotate Accumulator left by 1-bit without carry.	1	1	1	0	0	1	1	1	1	1				
RLC A	(AN + 1) ← (AN); N = 0 – 6 (A_0) ← (C) (C) ← (A_7)	Rotate Accumulator left by 1-bit through carry.	1	1	1	1	0	1	1	1	1	1	•			
RR A	(AN) ← (AN + 1); N = 0 – 6 (A_7) ← (A_0)	Rotate Accumulator right by 1-bit without carry.	0	1	1	1	0	1	1	1	1	1				
RRC A	(AN) ← (AN + 1); N = 0 – 6 (A_7) ← (C) (C) ← (A_0)	Rotate Accumulator right by 1-bit through carry.	0	1	1	0	0	1	1	1	1	1	•			
SWAP A	(A_{4-7}) ↔ (A_0 – 3)	Swap the 2 4-bit nibbles in the Accumulator.	0	1	0	0	0	1	1	1	1	1				
XRL A, = data	(A) ← (A) XOR data	Logical XOR specified immediate data with Accumulator.	1 d_7	1 d_6	0 d_5	1 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2				
XRL A, Rr	(A) ← (A) XOR (Rr) for r = 0 – 7	Logical XOR contents of designated register with Accumulator.	1	1	0	1	1	r	r	r	1	1				
XRL A, @ Rr	(A) ← (A) XOR ((Rr)) for r = 0 – 1	Logical XOR Indirect the contents of data memory location with Accumulator.	1	1	0	1	0	0	0	r	1	1				
BRANCH																
DJNZ Rr, addr	(Rr) ← (Rr) – 1; r = 0 – 7 If (Rr) ≠ 0: (PC 0 – 7) ← addr	Decrement the specified register and test contents.	1 a_7	1 a_6	1 a_5	0 a_4	1 a_3	r a_2	r a_1	r a_0	2	2				
JBb addr	(PC 0 – 7) ← addr if Bb = 1 (PC) ← (PC) + 2 if Bb = 0	Jump to specified address if Accumulator bit is set.	b_2 a_7	b_1 a_6	b_0 a_5	1 a_4	0 a_3	0 a_2	1 a_1	0 a_0	2	2				
JC addr	(PC 0 – 7) ← addr if C = 1 (PC) ← (PC) + 2 if C = 0	Jump to specified address if carry flag is set.	1 a_7	1 a_6	1 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				
JF0 addr	(PC 0 – 7) ← addr if F0 = 1 (PC) ← (PC) + 2 if F0 = 0	Jump to specified address if Flag F0 is set.	1 a_7	0 a_6	1 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				
JF1 addr	(PC 0 – 7) ← addr if F1 = 1 (PC) ← (PC) + 2 if F1 = 0	Jump to specified address if Flag F1 is set.	0 a_7	1 a_6	1 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				
JMP addr	(PC 8 – 10) ← addr 8 – 10 (PC 0 – 7) ← addr 0 – 7 (PC 11) ← DBF	Direct Jump to specified address within the 2K address block.	a_{10} a_7	a_9 a_6	a_8 a_5	0 a_4	0 a_3	1 a_2	0 a_1	0 a_0	2	2				
JMPP @ A	(PC 0 – 7) ← ((A))	Jump indirect to specified address with with address page.	1	0	1	1	0	0	1	1	2	1				
JNC addr	(PC 0 – 7) ← addr if C = 0 (PC) ← (PC) + 2 if C = 1	Jump to specified address if carry flag is low.	1 a_7	1 a_6	1 a_5	0 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				
JNI addr	(PC 0 – 7) ← addr if I = 0 (PC) ← (PC) + 2 if I = 1	Jump to specified address if interrupt is low.	1 a_7	0 a_6	0 a_5	0 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				

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MNEMONIC	FUNCTION	DESCRIPTION	INSTRUCTION CODE D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	CYCLES	BYTES	FLAGS C	AC	F0	F1
BRANCH (CONT.)																
JNT0 addr	(PC 0 – 7) ← addr if T0 = 0 (PC) ← (PC) + 2 if T0 = 1	Jump to specified address if Test 0 is low.	0 a_7	0 a_6	1 a_5	0 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				
JNT1 addr	(PC 0 – 7) ← addr if T1 = 0 (PC) ← (PC) + 2 if T1 = 1	Jump to specified address if Test 1 is low.	0 a_7	1 a_6	0 a_5	0 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				
JNZ addr	(PC 0 – 7) ← addr if A ≠ 0 (PC) ← (PC) + 2 if A = 0	Jump to specified address if accumulator is non-zero.	1 a_7	0 a_6	0 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				
JTF addr	(PC 0 – 7) ← addr if TF = 1 (PC) ← (PC) + 2 if TF = 0	Jump to specified address if Timer Flag is set to 1.	0 a_7	0 a_6	0 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				
JT0 addr	(PC 0 – 7) ← addr if T0 = 1 (PC) ← (PC) + 2 if T0 = 0	Jump to specified address if Test 0 is a 1.	0 a_7	0 a_6	1 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				
JT1 addr	(PC 0 – 7) ← addr if T1 = 1 (PC) ← (PC) + 2 if T1 = 0	Jump to specified address if Test 1 is a 1.	0 a_7	1 a_6	0 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				
JZ addr	(PC 0 – 7) ← addr if A = 0 (PC) ← (PC) + 2 if A ≠ 0	Jump to specified address if Accumulator is 0.	1 a_7	1 a_6	0 a_5	0 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				
CONTROL																
EN I		Enable the External Interrupt input.	0	0	0	0	0	1	0	1	1	1				
DIS I		Disable the External Interrupt input.	0	0	0	1	0	1	0	1	1	1				
ENT0 CLK		Enable the Clock Output pin T0.	0	1	1	1	0	1	0	1	1	1				
SEL MB0	(DBF) ← 0	Select Bank 0 (locations 0 – 2047) of Program Memory.	1	1	1	0	0	1	0	1	1	1				
SEL MB1	(DBF) ← 1	Select Bank 1 (locations 2048 – 4095) of Program Memory.	1	1	1	1	0	1	0	1	1	1				
SEL RB0	(BS) ← 0	Select Bank 0 (locations 0 – 7) of Data Memory.	1	1	0	0	0	1	0	1	1	1				
SEL RB1	(BS) ← 1	Select Bank 1 (locations 24 – 31) of Data Memory.	1	1	0	1	0	1	0	1	1	1				
DATA MOVES																
MOV A, = data	(A) ← data	Move Immediate the specified data into the Accumulator.	0 d_7	0 d_6	1 d_5	0 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2				
MOV A, Rr	(A) ← (Rr); r = 0 – 7	Move the contents of the designated registers into the Accumulator.	1	1	1	1	1	r	r	r	1	1				
MOV A, @ Rr	(A) ← ((Rr)); r = 0 – 1	Move Indirect the contents of data memory location into the Accumulator.	1	1	1	1	0	0	0	r	1	1				
MOV A, PSW	(A) ← (PSW)	Move contents of the Program Status Word into the Accumulator.	1	1	0	0	0	1	1	1	1	1				
MOV Rr, = data	(Rr) ← data; r = 0 – 7	Move Immediate the specified data into the designated register.	1 d_7	0 d_6	1 d_5	1 d_4	1 d_3	r d_2	r d_1	r d_0	2	2				
MOV Rr, A	(Rr) ← (A); r = 0 – 7	Move Accumulator Contents into the designated register.	1	0	1	0	1	r	r	r	1	1				
MOV @ Rr, A	((Rr)) ← (A); r = 0 – 1	Move Indirect Accumulator Contents into data memory location.	1	0	1	0	0	0	0	r	1	1				
MOV @ Rr, = data	((Rr)) ← data; r = 0 – 1	Move Immediate the specified data into data memory.	1 d_7	0 d_6	1 d_5	1 d_4	0 d_3	0 d_2	0 d_1	r d_0	2	2				
MOV PSW, A	(PSW) ← (A)	Move contents of Accumulator into the program status word.	1	1	0	1	0	1	1	1	1	1				
MOVP A, @ A	(PC 0 – 7) ← (A) (A) ← ((PC))	Move data in the current page into the Accumulator.	1	0	1	0	0	0	1	1	2	1				
MOVP3 A, @ A	(PC 0 – 7) ← (A) (PC 8 – 10) ← 011 (A) ← ((PC))	Move Program data in Page 3 into the Accumulator.	1	1	1	0	0	0	1	1	2	1				
MOVX A, @ R	(A) ← ((Rr)); r = 0 – 1	Move Indirect the contents of external data memory into the Accumulator.	1	0	0	0	0	0	0	r	2	1				
MOVX @ R, A	((Rr)) ← (A); r = 0 – 1	Move Indirect the contents of the Accumulator into external data memory.	1	0	0	1	0	0	0	r	2	1				
XCH A, Rr	(A) ⇄ (Rr); r = 0 – 7	Exchange the Accumulator and designated register's contents.	0	0	1	0	1	r	r	r	1	1				
XCH A, @ Rr	(A) ⇄ ((Rr)); r = 0 – 1	Exchange Indirect contents of Accumulator and location in data memory.	0	0	1	0	0	0	0	r	1	1				
XCHD A, @ Rr	(A 0 – 3) ⇄ ((Rr) 0 – 3)); r = 0 – 1	Exchange Indirect 4-bit contents of Accumulator and data memory.	0	0	1	1	0	0	0	r	1	1				
FLAGS																
CPL C	(C) ← NOT (C)	Complement Content of carry bit.	1	0	1	0	0	1	1	1	1	1	•			
CPL F0	(F0) ← NOT (F0)	Complement Content of Flag F0.	1	0	0	1	0	1	0	1	1	1			•	
CPL F1	(F1) ← NOT (F1)	Complement Content of Flag F1	1	0	1	1	0	1	0	1	1	1				•
CLR C	(C) ← 0	Clear content of carry bit to 0.	1	0	0	1	0	1	1	1	1	1	•			
CLR F0	(F0) ← 0	Clear content of Flag 0 to 0.	1	0	0	0	0	1	0	1	1	1			•	
CLR F1	(F1) ← 0	Clear content of Flag 1 to 0.	1	0	1	0	0	1	0	1	1	1				•

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MNEMONIC	FUNCTION	DESCRIPTION	INSTRUCTION CODE D7	D6	D5	D4	D3	D2	D1	D0	CYCLES	BYTES	FLAGS C	AC	F0	F1
INPUT/OUTPUT																
ANL BUS, = data	(BUS) ← (BUS) AND data	Logical and Immediate-specified data with contents of BUS.	1 d_7	0 d_6	0 d_5	1 d_4	1 d_3	0 d_2	0 d_1	0 d_0	2	2				
ANL Pp, = data	(Pp) ← (Pp) AND data p = 1 – 2	Logical and Immediate specified data with designated port (1 or 2)	1 d_7	0 d_6	0 d_5	1 d_4	1 d_3	0 d_2	p d_1	p d_0	2	2				
ANLD Pp, A	(Pp) ← (Pp) AND (A 0 – 3) p = 4 – 7	Logical and contents of Accumulator with designated port (4 – 7).	1	0	0	1	1	1	p	p	2	1				
IN A, Pp	(A) ← (Pp); p = 1 – 2	Input data from designated port (1 – 2) into Accumulator.	0	0	0	0	1	0	p	p	2	1				
INS A, BUS	(A) ← (BUS)	Input strobed BUS data into Accumulator.	0	0	0	0	1	0	0	0	2	1				
MOVD A, Pp	(A 0 – 3) ← (Pp); p = 4 – 7 (A 4 – 7) ← 0	Move contents of designated port (4 – 7) into Accumulator.	0	0	0	0	1	1	p	p	2	1				
MOVD Pp, A	(Pp) ← A 0 – 3; p = 4 – 7	Move contents of Accumulator to designated port (4 – 7).	0	0	1	1	1	1	p	p	1	1				
ORL BUS, = data	(BUS) ← (BUS) OR data	Logical or Immediate specified data with contents of BUS.	1 d_7	0 d_6	0 d_5	0 d_4	1 d_3	0 d_2	0 d_1	0 d_0	2	2				
ORLD Pp, A	(Pp) ← (Pp) OR (A 0 – 3) p = 4 – 7	Logical or contents of Accumulator with designated port (4 – 7).	1	0	0	0	1	1	p	p	1	1				
ORL Pp, = data	(Pp) ← (Pp) OR data p = 1 – 2	Logical or Immediate specified data with designated port (1 – 2)	1 d_7	0 d_6	0 d_5	0 d_4	1 d_3	0 d_2	p d_1	p d_0	2	2				
OUTL BUS, A	(BUS) ← (A)	Output contents of Accumulator onto BUS.	0	0	0	0	0	0	1	0	1	1				
OUTL Pp, A	(Pp) ← (A); p = 1 – 2	Output contents of Accumulator to designated port (1 – 2).	0	0	1	1	1	0	p	p	1	1				
REGISTERS																
DEC Rr (Rr)	(Rr) ← (Rr) – 1; r = 0 – 7	Decrement by 1 contents of designated register.	1	1	0	0	1	r	r	r	1	1				
INC Rr	(Rr) ← (Rr) +1; r = 0 – 7	Increment by 1 contents of designated register.	0	0	0	1	1	r	r	r	1	1				
INC @ Rr	((Rr)) ← ((Rr)) + 1; r = 0 – 1	Increment Indirect by 1 the contents of data memory location.	0	0	0	1	0	0	0	r	1	1				
SUBROUTINE																
CALL addr	((SP)) ← (PC), (PSW 4 – 7) (SP) ← (SP) + 1 (PC 8 – 10) ← addr 8 – 10 (PC 0 – 7) ← addr 0 – 7 (PC 11) ← DBF	Call designated Subroutine.	a_{10} a_7	a_9 a_6	a_8 a_5	1 a_4	0 a_3	1 a_2	0 a_1	0 a_0	2	2				
RET	(SP) ← (SP) – 1 (PC) ← ((SP))	Return from Subroutine without restoring Program Status Word.	1	0	0	0	0	0	1	1	2	1				
RETR	(SP) ← (SP) – 1 (PC) ← ((SP)) (PSW 4 – 7) ← ((SP))	Return from Subroutine restoring Program Status Word.	1	0	0	1	0	0	1	1	2	1				
TIMER/COUNTER																
EN TCNTI		Enable Internal interrupt Flag for Timer/Counter output.	0	0	1	0	0	1	0	1	1	1				
DIS TCNTI		Disable Internal interrupt Flag for Timer/Counter output.	0	0	1	1	0	1	0	1	1	1				
MOV A, T	(A) ← (T)	Move contents of Timer/Counter into Accumulator.	0	1	0	0	0	0	1	0	1	1				
MOV T, A	(T) ← (A)	Move contents of Accumulator into Timer/Counter.	0	1	1	0	0	0	1	0	1	1				
STOP TCNT		Stop Count for Event Counter.	0	1	1	0	0	1	0	1	1	1				
STRT CNT		Start Count for Event Counter.	0	1	0	0	0	1	0	1	1	1				
STRT T		Start Count for Timer.	0	1	0	1	0	1	0	1	1	1				
MISCELLANEOUS																
NOP		No Operation performed.	0	0	0	0	0	0	0	0	1	1				

Notes: ① Instruction Code Designations r and p form the binary representation of the Registers and Ports involved.

② The dot under the appropriate flag bit indicates that its content is subject to change by the instruction it appears in.

③ References to the address and data are specified in bytes 2 and/or 1 of the instruction.

④ Numerical Subscripts appearing in the FUNCTION column reference the specific bits affected.

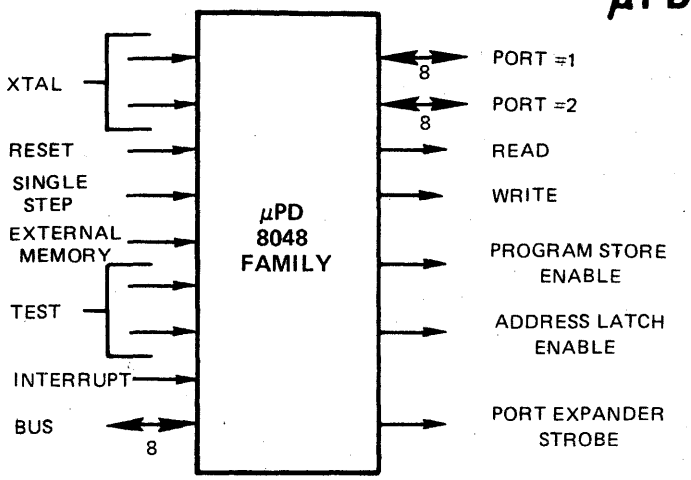
Symbol Definitions:

SYMBOL	DESCRIPTION
A	The Accumulator
AC	The Auxiliary Carry Flag
addr	Program Memory Address (12 bits)
Bb	Bit Designator (b = 0 – 7)
BS	The Bank Switch
BUS	The BUS Port
C	Carry Flag
CLK	Clock Signal
CNT	Event Counter
D	Nibble Designator (4 bits)
data	Number or Expression (8 bits)
DBF	Memory Bank Flip-Flop
F_0, F_1	Flags 0, 1
I	Interrupt
P	"In-Page" Operation Designator

SYMBOL	DESCRIPTION
P_p	Port Designator (p = 1, 2 or 4 – 7)
PSW	Program Status Word
Rr	Register Designator (r = 0, 1 or 0 – 7)
SP	Stack Pointer
T	Timer
TF	Timer Flag
T_0, T_1	Testable Flags 0, 1
X	External RAM
=	Prefix for Immediate Data
@	Prefix for Indirect Address
$	Program Counter's Current Value
(x)	Contents of External RAM Location
((x))	Contents of Memory Location Addressed by the Contents of External RAM Location.
←	Replaced By

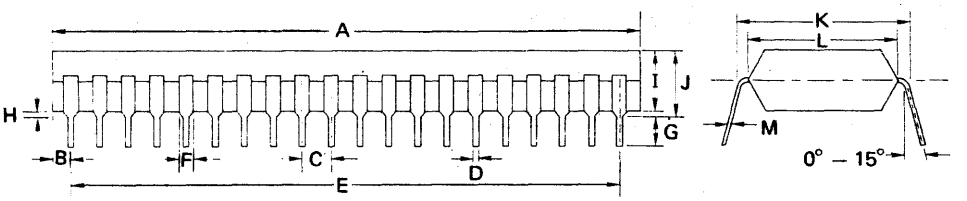
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LOGIC SYMBOL



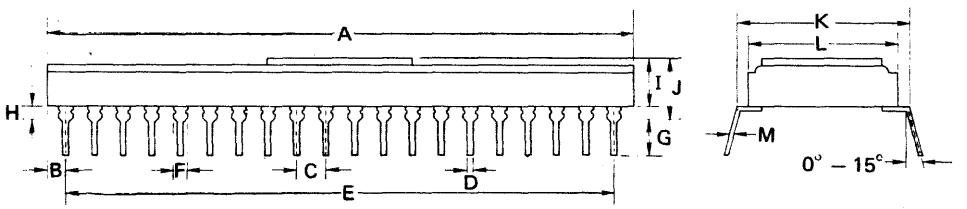
PACKAGE OUTLINES

μPD8048C/D
μPD8748D
μPD8035C/D



Plastic

ITEM	MILLIMETERS	INCHES
A	51.5 MAX	2.028 MAX
B	1.62	0.064
C	2.54 ± 0.1	0.10 ± 0.004
D	0.5 ± 0.1	0.019 ± 0.004
E	48.26	1.9
F	1.2 MIN	0.047 MIN
G	2.54 MIN	0.10 MIN
H	0.5 MIN	0.019 MIN
I	5.22 MAX	0.206 MAX
J	5.72 MAX	0.225 MAX
K	15.24	0.600
L	13.2	0.520
M	$0.25^{+0.1}_{0.05}$	$0.010^{+0.004}_{0.002}$



Ceramic

ITEM	MILLIMETERS	INCHES
A	51.5 MAX	2.028 MAX
B	1.62	0.064
C	2.54 ± 0.1	0.100 ± 0.004
D	0.50 ± 0.1	0.0197 ± 0.004
E	48.26 ± 0.2	1.900 ± 0.008
F	1.27	0.050
G	3.2 MIN	0.126 MIN
H	1.0 MIN	0.04 MIN
I	4.2 MAX	0.17 MAX
J	5.2 MAX	0.205 MAX
K	15.24 ± 0.1	0.6 ± 0.004
L	$13.5^{+0.2}_{-0.25}$	$0.531^{+0.008}_{-0.010}$
M	0.30 ± 0.1	0.012 ± 0.004

SP8048-7-78-GN-CAT

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NEC

μPD8049
μPD8039

PRELIMINARY

SINGLE CHIP 8-BIT MICROCOMPUTERS

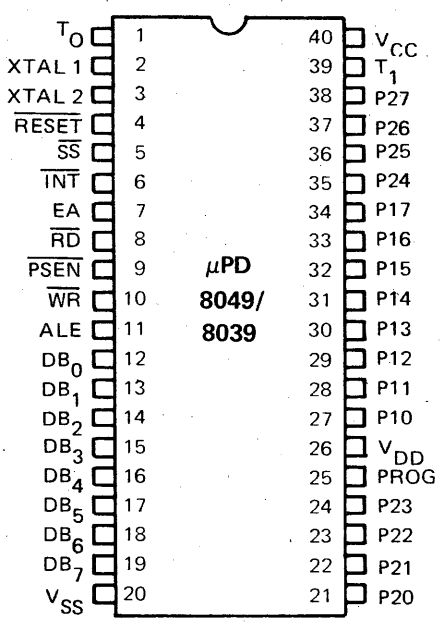
DESCRIPTION

The NEC μPD8049 and μPD8039 are single chip 8-bit microcomputers. The processors differ only in their internal program memory options: the μPD8049 with 2K x 8 bytes of mask ROM and the μPD8039 with external program memory.

FEATURES

- Fully Compatible with Industry Standard 8049/8039
- Pin Compatible with the μPD8048/8748/8035
- NMOS Silicon Gate Technology Requiring a Single +5V Supply
- 2.5 μs Cycle Time. All Instructions 1 or 2 Bytes
- Interval Timer/Event Counter
- 2K x 8 Bytes of ROM, 128 x 8 Bytes of RAM
- Single Level Interrupt
- 96 Instructions: 70 Percent Single Byte
- 27 I/O Lines
- Internal Clock Generator
- Compatible with 8080A/8085A Peripherals
- Available in Both Ceramic and Plastic 40-Pin Packages

PIN CONFIGURATION



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μPD8049/8039

FUNCTIONAL DESCRIPTION

The NEC μPD8049 and μPD8039 are single component, 8-bit, parallel microprocessors using N-channel silicon gate MOS technology. The μPD8049 and μPD8039 efficiently function in control as well as arithmetic applications. The flexibility of the instruction set allows for the direct set and reset of individual data bits within the accumulator and the I/O port structure. Standard logic function implementation is facilitated by the large variety of branch and table look-up instructions.

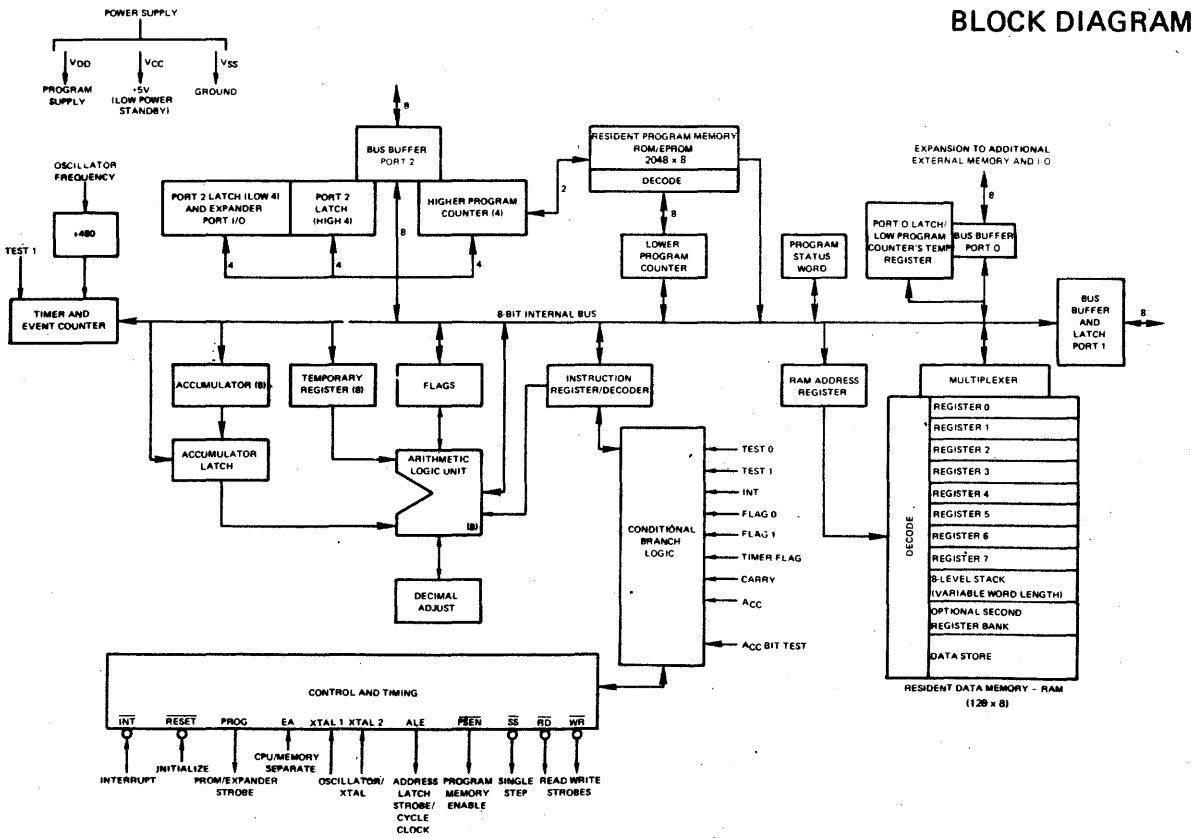
The μPD8049 and μPD8039 instruction set is comprised of 1 and 2 byte instructions with over 70 percent single-byte and requiring only 1 or 2 cycles per instruction with over 50 percent single-cycle.

The μPD8049 and μPD8039 microprocessors will function as stand-alone microcomputers. Their functions can easily be expanded using standard 8080A/8085A peripherals and memories.

The μPD8049 contains the following functions usually found in external peripheral devices: 2048 x 8 bits of mask ROM program memory; 128 x 8 bits of RAM data memory; 27 I/O lines; an 8-bit interval timer/event counter; and oscillator and clock circuitry.

The μPD8039 is intended for applications using external program memory only. It contains all the features of the μPD8049 except the 2048 x 8-bit internal ROM. The external program memory can be implemented using standard 8080A/8085A memory products.

BLOCK DIAGRAM



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PIN IDENTIFICATION

PIN NO.	PIN SYMBOL	FUNCTION
1	T_0	Testable input using conditional transfer functions JT0 and JNT0. The internal State Clock (CLK) is available to T_0 using the ENTO CLK instruction. T_0 can also be used during programming as a testable flag.
2	XTAL 1	One side of the crystal input for external oscillator or frequency (non TTL compatible V_{IH}).
3	XTAL 2	The other side of the crystal input.
4	$\overline{RESET}$	Active low input for processor initialization. $\overline{RESET}$ is also used for PROM programming verification and power-down (non TTL compatible V_{IH}).
5	$\overline{SS}$	Single Step input (active-low). $\overline{SS}$ together with ALE allows the processor to "single-step" through each instruction in program memory.
6	$\overline{INT}$	Interrupt input (active-low). $\overline{INT}$ will start an interrupt if an enable interrupt instruction has been executed. A reset will disable the interrupt. $\overline{INT}$ can be tested by issuing a conditional jump instruction.
7	EA	External Access input (active-high). A logic "1" at this input commands the processor to perform all program memory fetches from external memory.
8	$\overline{RD}$	READ strobe output (active-low). $\overline{RD}$ will pulse low when the processor performs a BUS READ. $\overline{RD}$ will also enable data onto the processor BUS from a peripheral device and function as a READ STROBE for external DATA MEMORY.
9	$\overline{PSEN}$	Program Store Enable output (active-low). $\overline{PSEN}$ becomes active only during an external memory fetch.
10	$\overline{WR}$	WRITE strobe output (active-low). $\overline{WR}$ will pulse low when the processor performs a BUS WRITE. $\overline{WR}$ can also function as a WRITE STROBE for external DATA MEMORY.
11	ALE	Address Latch Enable output (active-high). Occurring once each cycle, the falling edge of ALE latches the address for external memory or peripherals. ALE can also be used as a clock output.
12 – 19	$D_0 - D_7$ BUS	8-bit, bidirectional port. Synchronous reads and writes can be performed on this port using $\overline{RD}$ and $\overline{WR}$ strobes. The contents of the $D_0 - D_7$ BUS can be latched in a static mode. During an external memory fetch, the $D_0 - D_7$ BUS holds the least significant bits of the program counter. PSEN controls the incoming addressed instruction. Also, for an external RAM data store instruction the $D_0 - D_7$ BUS, controlled by ALE, $\overline{RD}$ and $\overline{WR}$, contains address and data information.
20	V_{SS}	Processor's GROUND potential.
21 – 24, 35 – 38	$P_{20} - P_{27}$: PORT 2	Port 2 is the second of two 8-bit quasi-bidirectional ports. For external data memory fetches, the four most significant bits of the program counter are contained in $P_{20} - P_{23}$. Bits $P_{20} - P_{23}$ are also used as a 4-bit I/O bus for the μPD8243, INPUT/OUTPUT EXPANDER.
25	PROG	PROG is the output strobe for the μPD8243 I/O expander.
26	V_{DD}	V_{DD} is +5V for normal operation. It also functions as low power standby pin.
27 – 34	$P_{10} - P_{17}$: PORT 1	Port 1 is one of two 8-bit quasi-bidirectional ports.
39	T1	Testable input using conditional transfer functions JT1 and JNT1. T1 can be made the counter/timer input using the STRT CNT instruction.
40	V_{CC}	Primary Power supply. V_{CC} is +5V during normal operation.

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ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	0°C to +70°C
Storage Temperature (Ceramic Package)	-65°C to +150°C
Storage Temperature (Plastic Package)	-65°C to +125°C
Voltage on Any Pin	- 0.5 to +7 Volts ①
Power Dissipation	1.5 W

Note: ① With respect to ground.

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

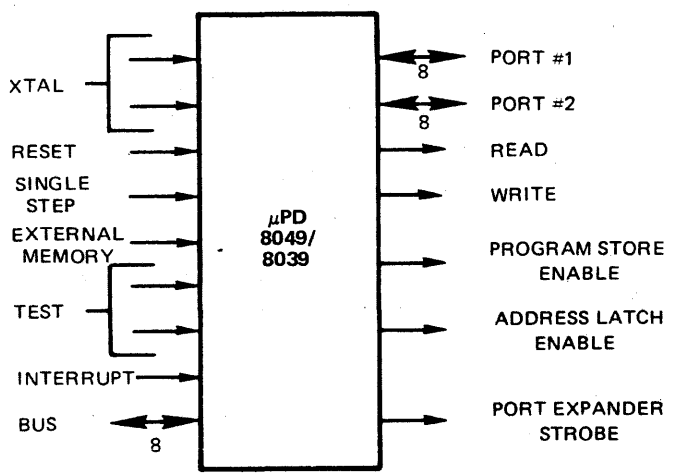
*T_a = 25°C

DC CHARACTERISTICS

T_a = 0°C to +70°C; V_{CC} = V_{DD} = +5V ± 5%; V_{SS} = 0V

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input Low Voltage (All Except XTAL 1, XTAL 2)	V_{IL}	-0.5		0.8	V	
Input High Voltage (All Except XTAL 1, XTAL 2, $\overline{RESET}$)	V_{IH}	2.0		V_{CC}	V	
Input High Voltage ($\overline{RESET}$, XTAL 1, XTAL 2)	V_{IH1}	3.0		V_{CC}	V	
Output Low Voltage (BUS, $\overline{RD}$, $\overline{WR}$, $\overline{PSEN}$, ALE)	V_{OL}			0.45	V	I_{OL} = 2.0 mA
Output Low Voltage (All Other Outputs Except PROG)	V_{OL1}			0.45	V	I_{OL} = 1.6 mA
Output Low Voltage (PROG)	V_{OL2}			0.45	V	
Output High Voltage (BUS, $\overline{RD}$, $\overline{WR}$, $\overline{PSEN}$, ALE)	V_{OH}	2.4			V	I_{OH} = -100 μA
Output High Voltage (All Other Outputs)	V_{OH1}	2.4			V	I_{OH} = -50 μA
Input Leakage Current (T_1, EA, INT)	I_{IL}			±10	μA	$V_{SS} \leq V_{IN} \leq V_{CC}$
Output Leakage Current (BUS, T_0 – High Impedance State)	I_{OL}			-10	μA	$V_{CC} \geq V_{IN} \geq V_{SS}$ + 0.45V
Power Down Supply Current	I_{DD}		20	50	mA	T_a = 25°C
Total Supply Current	I_{DD} + I_{CC}		75	140	mA	T_a = 25°C

LOGIC SYMBOL



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AC CHARACTERISTICS

READ, WRITE AND INSTRUCTION FETCH – EXTERNAL DATA AND PROGRAM MEMORY

T_a = 0°C to +70°C; V_{CC} = V_{DD} = +5V ± 5%; V_{SS} = 0V

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
ALE Pulse Width	t_{LL}	400			ns	
Address Setup before ALE	t_{AL}	150			ns	
Address Hold from ALE	t_{LA}	80			ns	
Control Pulse Width ($\overline{PSEN}$, $\overline{RD}$, $\overline{WR}$)	t_{CC}	900			ns	
Data Setup before $\overline{WR}$	t_{DW}	500			ns	
Data Hold after $\overline{WR}$	t_{WD}	120			ns	C_L = 20 pF
Cycle Time	t_{CY}	2.5		15.0	μs	6 MHz XTAL
Data Hold	t_{DR}	0		200	ns	
$\overline{PSEN}$, $\overline{RD}$ to Data In	t_{RD}			500	ns	
Address Setup before $\overline{WR}$	t_{AW}	230			ns	
Address Setup before Data In	t_{AD}			950	ns	
Address Float to $\overline{RD}$, $\overline{PSEN}$	t_{AFC}	0			ns	

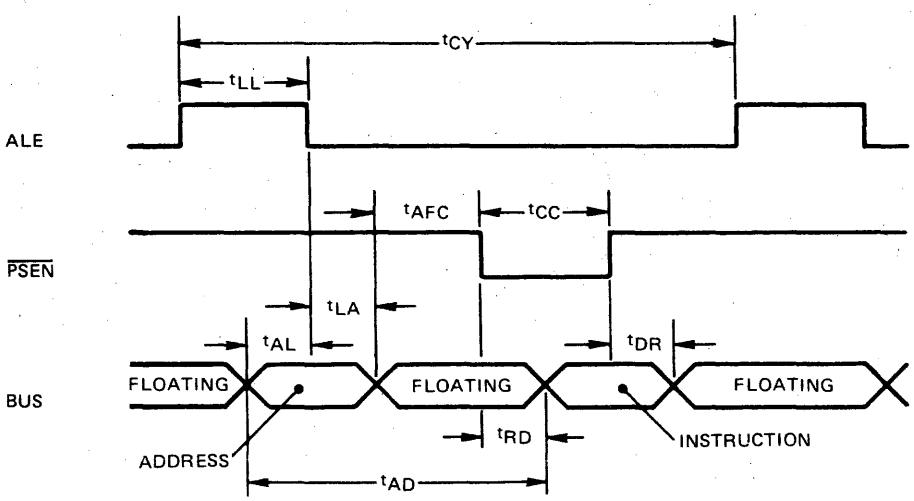
Notes: ① For Control Outputs: C_L = 80 pF
② For Bus Outputs: C_L = 150 pF
③ t_{CY} = 2.5 μs

PORT 2 TIMING

T_a = 0°C to +70°C; V_{CC} = +5V ± 5%; V_{SS} = 0V

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Port Control Setup before Falling Edge of PROG	t_{CP}	110			ns	
Port Control Hold after Falling Edge of PROG	t_{PC}	140			ns	
PROG to Time P2 Input must be Valid	t_{PR}			810	ns	
Output Data Setup Time	t_{DP}	220			ns	
Output Data Hold Time	t_{PD}	65			ns	
Input Data Hold Time	t_{PF}	0		150	ns	
PROG Pulse Width	t_{PP}	1510			ns	
Port 2 I/O Data Setup	t_{PL}	400			ns	
Port 2 I/O Data Hold	t_{LP}	150			ns	

TIMING WAVEFORMS



INSTRUCTION FETCH FROM EXTERNAL MEMORY

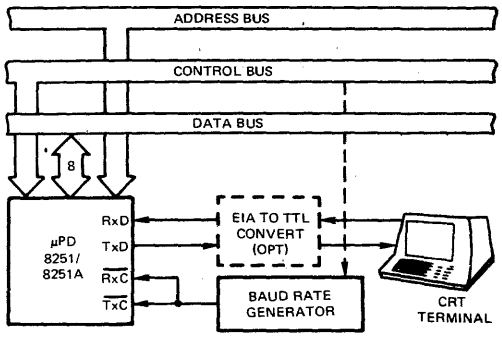
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PIN IDENTIFICATION

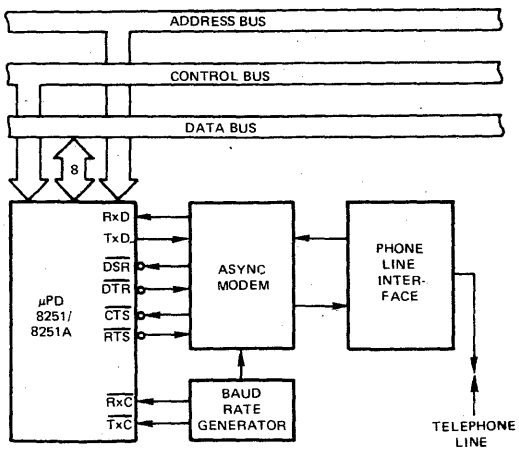
PIN NO.	PIN SYMBOL	PIN NAME	FUNCTION
1, 2, 27, 28 5 – 8	$D_7 - D_0$	Data Bus Buffer	An 8-bit, 3-state bi-directional buffer used to interface the μPD8251 and μPD8251A to the processor data bus. Data is transmitted or received by the buffer in response to input/output or Read/Write instructions from the processor. The Data Bus Buffer also transfers Control words, Command words, and Status.
26	V_{CC}	V_{CC} Supply Voltage	+5 volt supply
4	GND	Ground	Ground
Read/Write Control Logic			This logic block accepts inputs from the processor Control Bus and generates control signals for overall USART operation. The Mode Instruction and Command Instruction registers that store the control formats for device functional definition are located in the Read/Write Control Logic.
21	RESET	Reset	A "one" on this input forces the USART into the "Idle" mode where it will remain until reinitialized with a new set of control words. Minimum RESET pulse width is t_{CY}.
20	CLK	Clock Pulse	The CLK input provides for internal device timing and is usually connected to the Phase 2 (TTL) output of the μPB8224 Clock Generator. External inputs and outputs are not referenced to CLK, but the CLK frequency must be 30 times the Receiver or Transmitter clocks in the synchronous mode and 4.5 times for the asynchronous mode.
10	$\overline{WR}$	Write Data	A "zero" on this input instructs the μPD8251 and μPD8251A to accept the data or control word which the processor is writing out to the USART via the data bus.
13	$\overline{RD}$	Read Data	A "zero" on this input instructs the μPD8251 and μPD8251A to place the data or status information onto the Data Bus for the processor to read.
12	C/$\overline{D}$	Control/Data	The Control/Data input, in conjunction with the $\overline{WR}$ and $\overline{RD}$ inputs, informs USART to accept or provide either a data character, control word or status information via the Data Bus. 0 = Data; 1 = Control.
11	$\overline{CS}$	Chip Select	A "zero" on this input enables the USART for reading and writing to the processor.
Modem Control			The μPD8251 and μPD8251A have a set of control inputs and outputs which may be used to simplify the interface to a Modem.
22	$\overline{DSR}$	Data Set Ready	The Data Set Ready input can be tested by the processor via Status information. The $\overline{DSR}$ input is normally used to test Modem Data Set Ready condition.
24	$\overline{DTR}$	Data Terminal Ready	The Data Terminal Ready output can be controlled via the Command word. The $\overline{DTR}$ output is normally used to drive Modem Data Terminal Ready or Rate Select lines.
23	$\overline{RTS}$	Request to Send	The Request to Send output can be controlled via the Command word. The $\overline{RTS}$ output is normally used to drive the Modem Request to Send line.
17	$\overline{CTS}$	Clear to Send	A "zero" on the Clear to Send input enables the USART to transmit serial data if the TxEN bit in the Command Instruction register is enabled (one).

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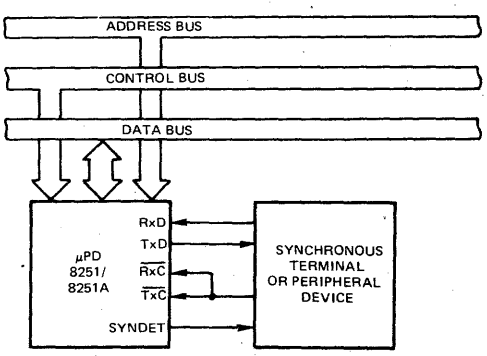
APPLICATION OF THE μPD8251 AND μPD8251A



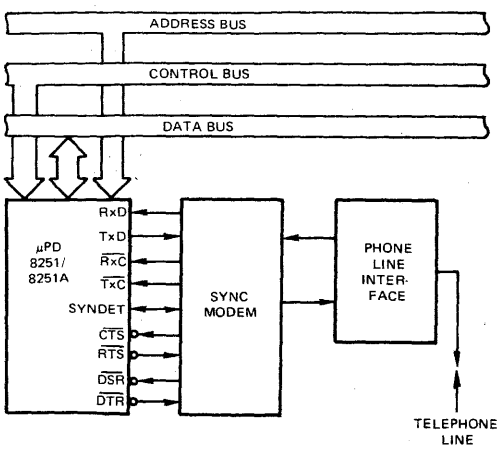
ASYNCHRONOUS SERIAL INTERFACE TO CRT TERMINAL, DC to 9600 BAUD



ASYNCHRONOUS INTERFACE TO TELEPHONE LINES



SYNCHRONOUS INTERFACE TO TERMINAL OR PERIPHERAL DEVICE

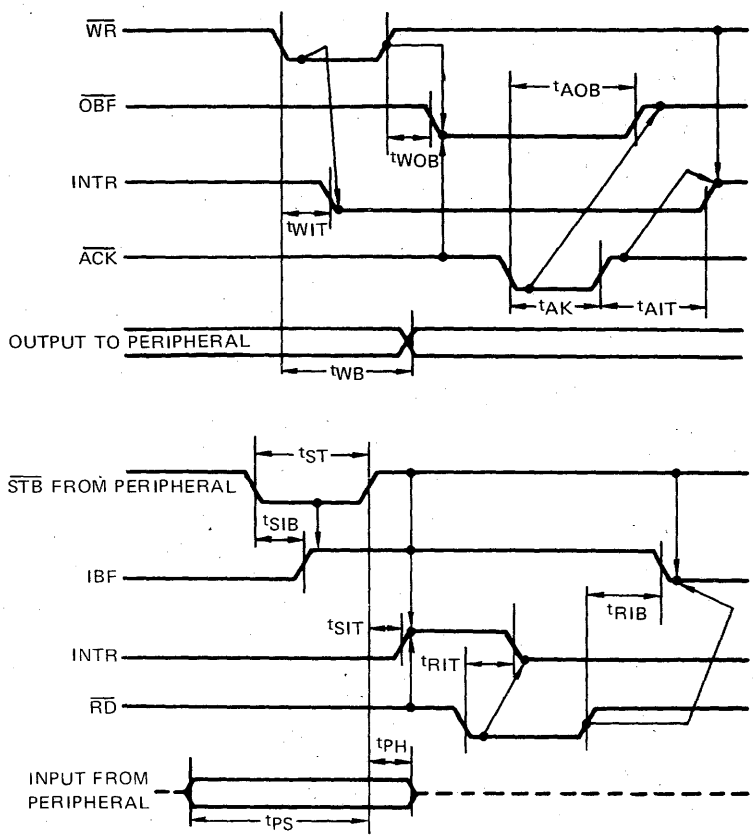


SYNCHRONOUS INTERFACE TO TELEPHONE LINES

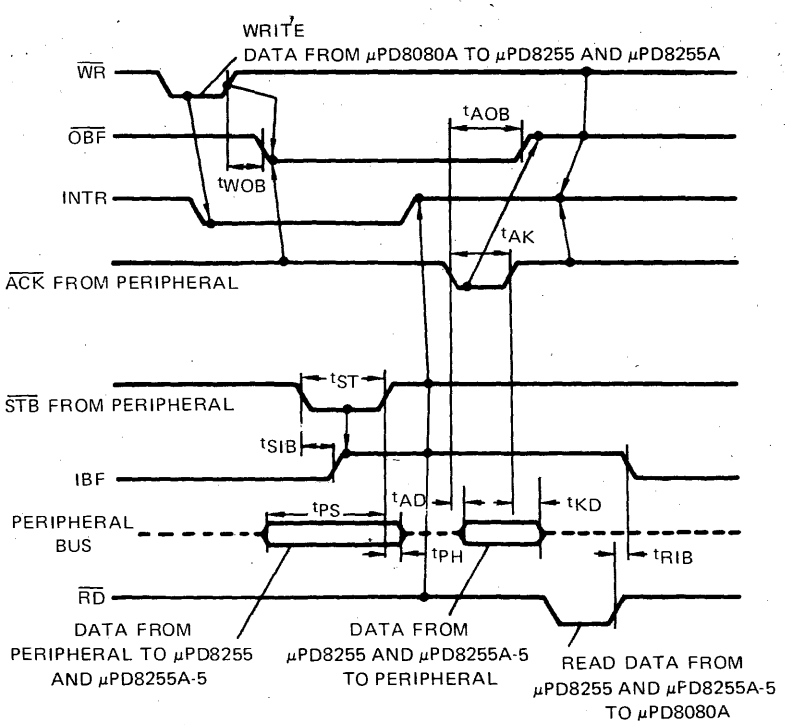
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TIMING WAVEFORMS (CONT.)

MODE 1



MODE 2

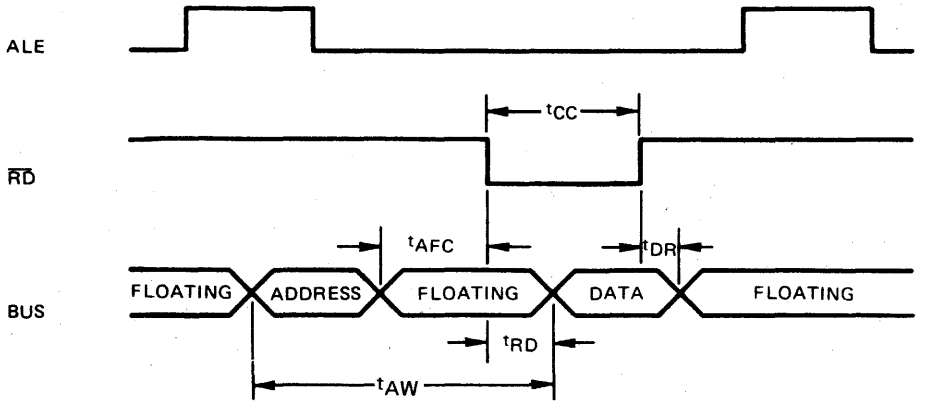


Note: ① Any sequence where $\overline{WR}$ occurs before $\overline{ACK}$ and $\overline{STB}$ occurs before $\overline{RD}$ is permissible.
(INTR = IBF · $\overline{MASK}$ · $\overline{STB}$ · $\overline{RD}$ + $\overline{OBF}$ · $\overline{MASK}$ · $\overline{ACK}$ · $\overline{WR}$)

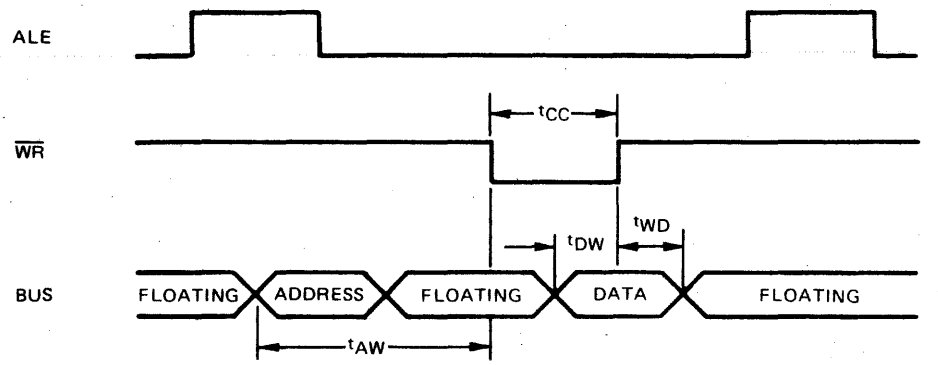
② When the μPD8255A-5 is set to Mode 1 or 2, $\overline{OBF}$ is reset to be high (logic 1).

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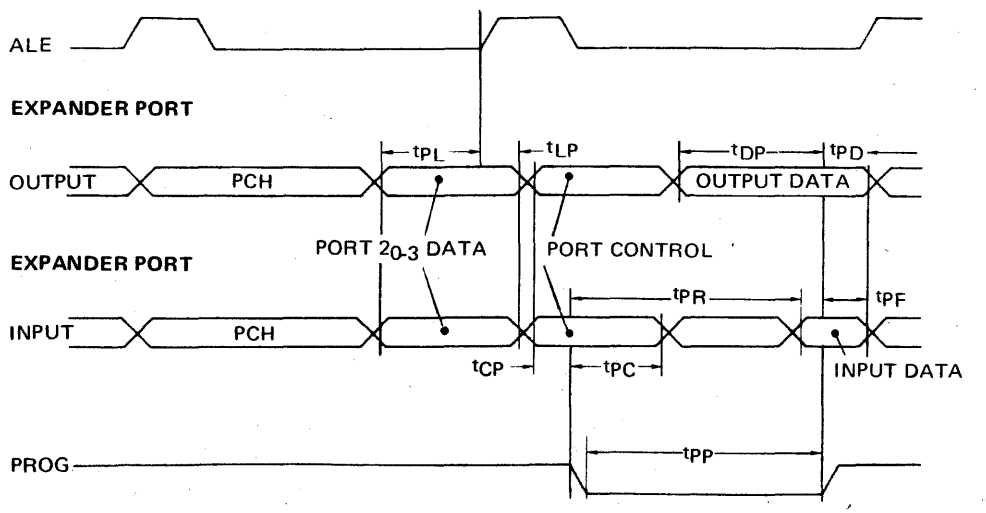
TIMING WAVEFORMS (CONT.)



READ FROM EXTERNAL DATA MEMORY



WRITE TO EXTERNAL MEMORY



PORT 2 TIMING

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MNEMONIC	FUNCTION	DESCRIPTION	INSTRUCTION CODE D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	CYCLES	BYTES	FLAGS C	AC	F0	F1
ACCUMULATOR																
ADD A, = data	(A) ← (A) + data	Add Immediate the specified Data to the Accumulator.	0 d_7	0 d_6	0 d_5	0 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2	•			
ADD A, Rr	(A) ← (A) + (Rr) for r = 0 – 7	Add contents of designated register to the Accumulator.	0	1	1	0	1	r	r	r	1	1	•			
ADD A, @ Rr	(A) ← (A) + ((Rr)) for r = 0 1	Add Indirect the contents the data memory location to the Accumulator.	0	1	1	0	0	0	0	r	1	1	•			
ADDC A, = data	(A) ← (A) + (C) + data	Add Immediate with carry the specified data to the Accumulator.	0 d_7	0 d_6	0 d_5	1 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2	•			
ADDC A, Rr	(A) ← (A) + (C) + (Rr) for r = 0 7	Add with carry the contents of the designated register to the Accumulator.	0	1	1	1	1	r	r	r	1	1	•			
ADDC A, @ Rr	(A) ← (A) + (C) + ((Rr)) for r = 0 1	Add Indirect with carry the contents of data memory location to the Accumulator.	0	1	1	1	0	0	0	r	1	1	•			
ANL A, = data	(A) ← (A) AND data	Logical and specified Immediate Data with Accumulator.	0 d_7	1 d_6	0 d_5	1 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2				
ANL A, Rr	(A) ← (A) AND (Rr) for r = 0 – 7	Logical and contents of designated register with Accumulator.	0	1	0	1	1	r	r	r	1	1				
ANL A, @ Rr	(A) ← (A) AND ((Rr)) for r = 0 1	Logical and Indirect the contents of data memory with Accumulator.	0	1	0	1	0	0	0	r	1	1				
CPL A	(A) ← NOT (A)	Complement the contents of the Accumulator.	0	0	1	1	0	1	1	1	1	1				
CLR A	(A) ← 0	CLEAR the contents of the Accumulator.	0	0	1	0	0	1	1	1	1	1				
DA A		DECIMAL ADJUST the contents of the Accumulator.	0	1	0	1	0	1	1	1	1	1	•			
DEC A	(A) ← (A) 1	DECREMENT by 1 the accumulator's contents.	0	0	0	0	0	1	1	1	1	1				
INC A	(A) ← (A) + 1	Increment by 1 the accumulator's contents.	0	0	0	1	0	1	1	1	1	1				
ORL A, = data	(A) ← (A) OR data	Logical OR specified immediate data with Accumulator	0 d_7	1 d_6	0 d_5	0 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2				
ORL A, Rr	(A) ← (A) OR (Rr) for r = 0 – 7	Logical OR contents of designated register with Accumulator.	0	1	0	0	1	r	r	r	1	1				
ORL A, @ Rr	(A) ← (A) OR ((Rr)) for r = 0 – 1	Logical OR Indirect the contents of data memory location with Accumulator.	0	1	0	0	0	0	0	r	1	1				
RL A	(AN + 1) ← (AN) (A_0) ← (A_7) for N = 0 – 6	Rotate Accumulator left by 1-bit without carry.	1	1	1	0	0	1	1	1	1	1				
RLC A	(AN + 1) ← (AN); N = 0 – 6 (A_0) ← (C) (C) ← (A_7)	Rotate Accumulator left by 1-bit through carry.	1	1	1	1	0	1	1	1	1	1	•			
RR A	(AN) ← (AN + 1); N = 0 – 6 (A_7) ← (A_0)	Rotate Accumulator right by 1-bit without carry.	0	1	1	1	0	1	1	1	1	1				
RRC A	(AN) ← (AN + 1); N = 0 – 6 (A_7) ← (C) (C) ← (A_0)	Rotate Accumulator right by 1-bit through carry.	0	1	1	0	0	1	1	1	1	1	•			
SWAP A	(A_{4-7}) ← (A_0 – 3)	Swap the 2 4-bit nibbles in the Accumulator.	0	1	0	0	0	1	1	1	1	1				
XRL A, = data	(A) ← (A) XOR data	Logical XOR specified immediate data with Accumulator.	1 d_7	1 d_6	0 d_5	1 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2				
XRL A, Rr	(A) ← (A) XOR (Rr) for r = 0 – 7	Logical XOR contents of designated register with Accumulator.	1	1	0	1	1	r	r	r	1	1				
XRL A, @ Rr	(A) ← (A) XOR ((Rr)) for r = 0 – 1	Logical XOR Indirect the contents of data memory location with Accumulator.	1	1	0	1	0	0	0	r	1	1				
BRANCH																
DJNZ Rr, addr	(Rr) ← (Rr) – 1; r = 0 – 7 If (Rr) ≠ 0: (PC 0 – 7) ← addr	Decrement the specified register and test contents.	1 a_7	1 a_6	1 a_5	0 a_4	1 a_3	r a_2	r a_1	r a_0	2	2				
JBb addr	(PC 0 – 7) ← addr if Bb = 1 (PC) ← (PC) + 2 if Bb = 0	Jump to specified address if Accumulator bit is set.	b_2 a_7	b_1 a_6	b_0 a_5	1 a_4	0 a_3	0 a_2	1 a_1	0 a_0	2	2				
JC addr	(PC 0 – 7) ← addr if C = 1 (PC) ← (PC) + 2 if C = 0	Jump to specified address if carry flag is set.	1 a_7	1 a_6	1 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				
JF0 addr	(PC 0 – 7) ← addr if FO = 1 (PC) ←)(PC) + 2 if FO = 0	Jump to specified address if Flag F0 is set.	1 a_7	0 a_6	1 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				
JF1 addr	(PC 0 - 7) ← addr if F1 = 1 (PC) ← (PC) + 2 if F1 = 0	Jump to specified address if Flag F1 is set.	0 a_7	1 a_6	1 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				
JMP addr	(PC 8 10) ← addr 8 10 (PC 0 - 7) ← addr 0 – 7 (PC 11) ← DBF	Direct Jump to specified address within the 2K address block.	a_{10} a_7	a_9 a_6	a_8 a_5	0 a_4	0 a_3	1 a_2	0 a_1	0 a_0	2	2				
JMPP @ A	(PC 0 7) ← ((A))	Jump indirect to specified address with with address page.	1	0	1	1	0	0	1	1	2	1				
JNC addr	(PC 0 7) ← addr if C = 0 (PC) ← (PC) + 2 if C = 1	Jump to specified address if carry flag is low.	1 a_7	1 a_6	1 a_5	0 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				
JNI addr	(PC 0 7) ← addr if I = 0 (PC) ← (PC) + 2 if I = 1	Jump to specified address if interrupt is low.	1 a_7	0 a_6	0 a_5	0 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				

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INSTRUCTION SET (CONT.)

MNEMONIC	FUNCTION	DESCRIPTION	INSTRUCTION CODE D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	CYCLES	BYTES	FLAGS C	AC	F0	F1
BRANCH (CONT.)																
JNT0 addr	(PC 0 – 7) ← addr if T0 = 0 (PC) ← (PC) + 2 if T0 = 1	Jump to specified address if Test 0 is low.	0 a_7	0 a_6	1 a_5	0 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				
JNT1 addr	(PC 0 – 7) ← addr if T1 = 0 (PC) ← (PC) + 2 if T1 = 1	Jump to specified address if Test 1 is low.	0 a_7	1 a_6	0 a_5	0 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				
JNZ addr	(PC 0 – 7) ← addr if A ≠ 0 (PC) ← (PC) + 2 if A = 0	Jump to specified address if accumulator is non-zero.	1 a_7	0 a_6	0 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				
JTF addr	(PC 0 – 7) ← addr if TF = 1 (PC) ← (PC) + 2 if TF = 0	Jump to specified address if Timer Flag is set to 1.	0 a_7	0 a_6	0 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				
JT0 addr	(PC 0 – 7) ← addr if T0 = 1 (PC) ← (PC) + 2 if T0 = 0	Jump to specified address if Test 0 is a	0 a_7	0 a_6	1 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				
JT1 addr	(PC 0 – 7) ← addr if T1 = 1 (PC) ← (PC) + 2 if T1 = 0	Jump to specified address if Test 1 is a 1.	0 a_7	1 a_6	0 a_5	1 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				
JZ addr	(PC 0 – 7) ← addr if A = 0 (PC) ← (PC) + 2 if A ≠ 0	Jump to specified address if Accumulator is 0.	1 a_7	1 a_6	0 a_5	0 a_4	0 a_3	1 a_2	1 a_1	0 a_0	2	2				
CONTROL																
EN I		Enable the External Interrupt input.	0	0	0	0	0	1	0	1	1	1				
DIS I		Disable the External Interrupt input.	0	0	0	1	0	1	0	1	1	1				
ENT0 CLK		Enable the Clock Output pin T0.	0	1	1	1	0	1	0	1	1	1				
SEL MB0	(DBF) ← 0	Select Bank 0 (locations 0 – 2047) of Program Memory.	1	1	1	0	0	1	0	1	1	1				
SEL MB1	(DBF) ← 1	Select Bank 1 (locations 2048 – 4095) of Program Memory.	1	1	1	1	0	1	0	1	1	1				
SEL RB0	(BS) ← 0	Select Bank 0 (locations 0 – 7) of Data Memory.	1	1	0	0	0	1	0	1	1	1				
SEL RB1	(BS) ← 1	Select Bank 1 (locations 24 – 31) of Data Memory.	1	1	0	1	0	1	0	1	1	1				
DATA MOVES																
MOV A, = data	(A) ← data	Move Immediate the specified data into the Accumulator.	0 d_7	0 d_6	1 d_5	0 d_4	0 d_3	0 d_2	1 d_1	1 d_0	2	2				
MOV A, Rr	(A) ← (Rr); r = 0 – 7	Move the contents of the designated registers into the Accumulator.	1	1	1	1	1	r	r	r	1	1				
MOV A, @ Rr	(A) ← ((Rr)); r = 0 – 1	Move Indirect the contents of data memory location into the Accumulator.	1	1	1	1	0	0	0	r	1	1				
MOV A, PSW	(A) ← (PSW)	Move contents of the Program Status Word into the Accumulator.	1	1	0	0	0	1	1	1	1	1				
MOV Rr, = data	(Rr) ← data; r = 0 – 7	Move Immediate the specified data into the designated register.	1 d_7	0 d_6	1 d_5	1 d_4	1 d_3	r d_2	r d_1	r d_0	2	2				
MOV Rr, A	(Rr) ← (A); r = 0 – 7	Move Accumulator Contents into the designated register.	1	0	1	0	1	r	r	r	1	1				
MOV @ Rr, A	((Rr)) ← (A); r = 0 – 1	Move Indirect Accumulator Contents into data memory location	1	0	1	0	0	0	0	r	1	1				
MOV @ Rr, = data	((Rr)) ← data; r = 0 – 1	Move Immediate the specified data into data memory.	1 d_7	0 d_6	1 d_5	1 d_4	0 d_3	0 d_2	0 d_1	r d_0	2	2				
MOV PSW, A	(PSW) ← (A)	Move contents of Accumulator into the program status word.	1	1	0	1	0	1	1	1	1	1				
MOVP A, @ A	(PC 0 – 7) ← (A) (A) ← ((PC))	Move data in the current page into the Accumulator.	1	0	1	0	0	0	1	1	2	1				
MOVP3 A, @ A	(PC 0 – 7) ← (A) (PC 8 – 10) ← 011 (A) ← ((PC))	Move Program data in Page 3 into the Accumulator.	1	1	1	0	0	0	1	1	2	1				
MOVX A, @ R	(A) ← ((Rr)); r = 0 – 1	Move Indirect the contents of external data memory into the Accumulator.	1	0	0	0	0	0	0	r	2	1				
MOVX @ R, A	((Rr)) ← (A); r = 0 – 1	Move Indirect the contents of the Accumulator into external data memory.	1	0	0	1	0	0	0	r	2	1				
XCH A, Rr	(A) ⇄ (Rr); r = 0 – 7	Exchange the Accumulator and designated register's contents.	0	0	1	0	1	r	r	r	1	1				
XCH A, @ Rr	(A) ⇄ ((Rr)); r = 0 – 1	Exchange Indirect contents of Accumulator and location in data memory.	0	0	1	0	0	0	0	r	1	1				
XCHD A, @ Rr	(A 0 – 3) ⇆ ((Rr)) 0 – 3)); r = 0 – 1	Exchange Indirect 4-bit contents of Accumulator and data memory.	0	0	1	1	0	0	0	r	1	1				
FLAGS																
CPL C	(C) ← NOT (C)	Complement Content of carry bit.	1	0	1	0	0	1	1	1	1	1	•			
CPL F0	(F0) ← NOT (F0)	Complement Content of Flag F0.	1	0	0	1	0	1	0	1	1	1			•	
CPL F1	(F1) ← NOT (F1)	Complement Content of Flag F1	1	0	1	1	0	1	0	1	1	1				•
CLR C	(C) ← 0	Clear content of carry bit to 0.	1	0	0	1	0	1	1	1	1	1	•			
CLR F0	(F0) ← 0	Clear content of Flag 0 to 0.	1	0	0	0	0	1	0	1	1	1			•	
CLR F1	(F1) ← 0	Clear content of Flag 1 to 0.	1	0	1	0	0	1	0	1	1	1				•

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MNEMONIC	FUNCTION	DESCRIPTION	INSTRUCTION CODE D7	D6	D5	D4	D3	D2	D1	D0	CYCLES	BYTES	FLAGS C	AC	F0	F1
INPUT/OUTPUT																
ANL BUS, #data	(BUS) ← (BUS) AND data	Logical and Immediate-specified data with contents of BUS.	1	0	0	1	1	0	0	0	2	2				
			d_7	d_6	d_5	d_4	d_3	d_2	d_1	d_0						
ANL Pp, #data	(Pp) ← (Pp) AND data p = 1 – 2	Logical and Immediate specified data with designated port (1 or 2)	1	0	0	1	1	0	p	p	2	2				
			d_7	d_6	d_5	d_4	d_3	d_2	d_1	d_0						
ANLD Pp, A	(Pp) ← (Pp) AND (A 0 – 3) p = 4 – 7	Logical and contents of Accumulator with designated port (4 – 7).	1	0	0	1	1	1	p	p	2	1				
IN A, Pp	(A) ← (Pp); p = 1 – 2	Input data from designated port (1 – 2) into Accumulator.	0	0	0	0	1	0	p	p	2	1				
INS A, BUS	(A) ← (BUS)	Input strobed BUS data into Accumulator.	0	0	0	0	1	0	0	0	2	1				
MOVD A, Pp	(A 0 – 3) ← (Pp); p = 4 – 7 (A 4 – 7) ← 0	Move contents of designated port (4 – 7) into Accumulator.	0	0	0	0	1	1	p	p	2	1				
MOVD Pp, A	(Pp) ← A 0 – 3; p = 4 – 7	Move contents of Accumulator to designated port (4 – 7).	0	0	1	1	1	1	p	p	1	1				
ORL BUS, #data	(BUS) ← (BUS) OR data	Logical or Immediate specified data with contents of BUS.	1	0	0	0	1	0	0	0	2	2				
			d_7	d_6	d_5	d_4	d_3	d_2	d_1	d_0						
ORLD Pp, A	(Pp) ← (Pp) OR (A 0 – 3) p = 4 – 7	Logical or contents of Accumulator with designated port (4 – 7).	1	0	0	0	1	1	p	p	1	1				
ORL Pp, #data	(Pp) ← (Pp) OR data p = 1 – 2	Logical or Immediate specified data with designated port (1 – 2)	1	0	0	0	1	0	p	p	2	2				
			d_7	d_6	d_5	d_4	d_3	d_2	d_1	d_0						
OUTL BUS, A	(BUS) ← (A)	Output contents of Accumulator onto BUS.	0	0	0	0	0	0	1	0	1	1				
OUTL Pp, A	(Pp) ← (A); p = 1 – 2	Output contents of Accumulator to designated port (1 – 2).	0	0	1	1	1	0	p	p	1	1				
REGISTERS																
DEC Rr (Rr)	(Rr) ← (Rr) – 1; r = 0 – 7	Decrement by 1 contents of designated register.	1	1	0	0	1	r	r	r	1	1				
INC Rr	(Rr) ← (Rr) +1; r = 0 – 7	Increment by 1 contents of designated register.	0	0	0	1	1	r	r	r	1	1				
INC @ Rr	((Rr)) ← ((Rr)) + 1; r = 0 – 1	Increment Indirect by 1 the contents of data memory location.	0	0	0	1	0	0	0	r	1	1				
SUBROUTINE																
CALL addr	((SP)) ← (PC), (PSW 4 – 7) (SP) ← (SP) + 1 (PC 8 – 10) ← addr 8 – 10 (PC 0 – 7) ← addr 0 – 7 (PC 11) ← DBF	Call designated Subroutine.	a_{10}	a_9	a_8	1	0	1	0	0	2	2				
			a_7	a_6	a_5	a_4	a_3	a_2	a_1	a_0						
RET	(SP) ← (SP) – 1 (PC) ← ((SP))	Return from Subroutine without restoring Program Status Word.	1	0	0	0	0	0	1	1	2	1				
RETR	(SP) ← (SP) – 1 (PC) ← ((SP)) (PSW 4 – 7) ← ((SP))	Return from Subroutine restoring Program Status Word.	1	0	0	1	0	0	1	1	2	1				
TIMER/COUNTER																
EN TCNTI		Enable Internal interrupt Flag for Timer/Counter output.	0	0	1	0	0	1	0	1	1	1				
DIS TCNTI		Disable Internal interrupt Flag for Timer/Counter output.	0	0	1	1	0	1	0	1	1	1				
MOV A, T	(A) ← (T)	Move contents of Timer/Counter into Accumulator.	0	1	0	0	0	0	1	0	1	1				
MOV T, A	(T) ← (A)	Move contents of Accumulator into Timer/Counter.	0	1	1	0	0	0	1	0	1	1				
STOP TCNT		Stop Count for Event Counter.	0	1	1	0	0	1	0	1	1	1				
STRT CNT		Start Count for Event Counter.	0	1	0	0	0	1	0	1	1	1				
STRT T		Start Count for Timer.	0	1	0	1	0	1	0	1	1	1				
MISCELLANEOUS																
NOP		No Operation performed.	0	0	0	0	0	0	0	0	1	1				

Notes: ① Instruction Code Designations r and p form the binary representation of the Registers and Ports involved.

② The dot under the appropriate flag bit indicates that its content is subject to change by the instruction it appears in.

③ References to the address and data are specified in bytes 2 and/or 1 of the instruction.

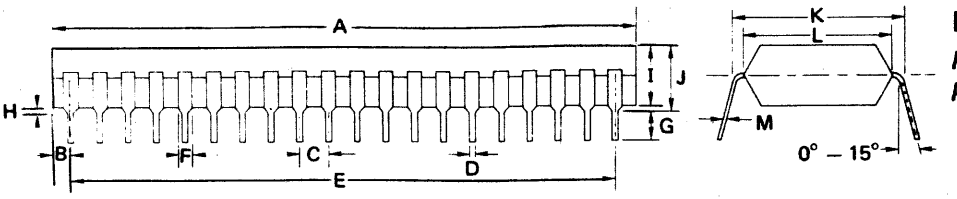
④ Numerical Subscripts appearing in the FUNCTION column reference the specific bits affected.

Symbol Definitions:

SYMBOL	DESCRIPTION
A	The Accumulator
AC	The Auxiliary Carry Flag
addr	Program Memory Address (12 bits)
Bb	Bit Designator (b = 0 – 7)
BS	The Bank Switch
BUS	The BUS Port
C	Carry Flag
CLK	Clock Signal
CNT	Event Counter
D	Nibble Designator (4 bits)
data	Number or Expression (8 bits)
DBF	Memory Bank Flip-Flop
F_0, F_1	Flags 0, 1
I	Interrupt
P	"In-Page" Operation Designator

SYMBOL	DESCRIPTION
P_p	Port Designator (p = 1, 2 or 4 – 7)
PSW	Program Status Word
Rr	Register Designator (r = 0, 1 or 0 – 7)
SP	Stack Pointer
T	Timer
TF	Timer Flag
T_0, T_1	Testable Flags 0, 1
X	External RAM
#	Prefix for Immediate Data
@	Prefix for Indirect Address
$	Program Counter's Current Value
(x)	Contents of External RAM Location
((x))	Contents of Memory Location Addressed by the Contents of External RAM Location.
←	Replaced By

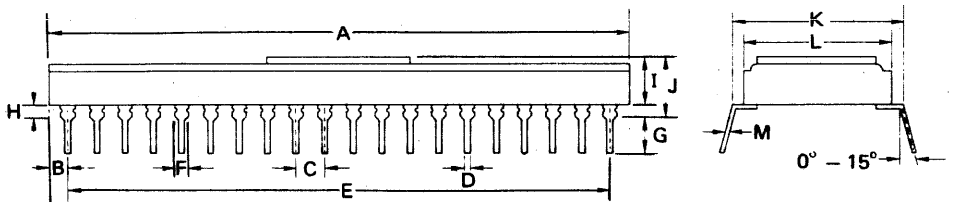
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PACKAGE OUTLINES
μPD8049C/D
μPD8039C/D

Plastic

ITEM	MILLIMETERS	INCHES
A	51.5 MAX	2.028 MAX
B	1.62	0.064
C	2.54 ± 0.1	0.10 ± 0.004
D	0.5 ± 0.1	0.019 ± 0.004
E	48.26	1.9
F	1.2 MIN	0.047 MIN
G	2.54 MIN	0.10 MIN
H	0.5 MIN	0.019 MIN
I	5.22 MAX	0.206 MAX
J	5.72 MAX	0.225 MAX
K	15.24	0.600
L	13.2	0.520
M	$0.25^{+0.1}_{-0.05}$	$0.010^{+0.004}_{-0.002}$



Ceramic

ITEM	MILLIMETERS	INCHES
A	51.5 MAX	2.028 MAX
B	1.62	0.064
C	2.54 ± 0.1	0.100 ± 0.004
D	0.50 ± 0.1	0.0197 ± 0.004
E	48.26 ± 0.2	1.900 ± 0.008
F	1.27	0.050
G	3.2 MIN	0.126 MIN
H	1.0 MIN	0.04 MIN
I	4.2 MAX	0.17 MAX
J	5.2 MAX	0.205 MAX
K	15.24 ± 0.1	0.6 ± 0.004
L	$13.5^{+0.2}_{-0.25}$	$0.531^{+0.008}_{-0.010}$
M	0.30 ± 0.1	0.012 ± 0.004

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μPD8080AF 8-BIT N-CHANNEL MIROPROCESSOR FAMILY

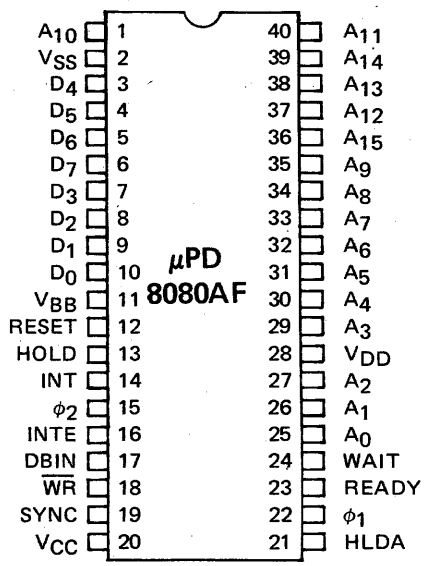
DESCRIPTION

The μPD8080AF is a complete 8-bit parallel processor for use in general purpose digital computer systems. It is fabricated on a single LSI chip using N-channel silicon gate MOS process, which offers much higher performance than conventional microprocessors (1.28 μs minimum instruction cycle). A complete microcomputer system is formed when the μPD8080AF is interfaced with I/O ports (up to 256 input and 256 output ports) and any type or speed of semiconductor memory. It is available in a 40 pin ceramic or plastic package.

FEATURES

- 78 Powerful Instructions
- Three Devices — Three Clock Frequencies
  μPD8080AF — 2.0 MHz
  μPD8080AF-2 — 2.5 MHz
  μPD8080AF-1 — 3.0 MHz
- Direct Access to 64K Bytes of Memory with 16-Bit Program Counter
- 256 8-Bit Input Ports and 256 8-Bit Output Ports
- Double Length Operations Including Addition
- Automatic Stack Memory Operation with 16-Bit Stack Pointer
- TTL Compatible (Except Clocks)
- Multi-byte Interrupt Capability
- **Fully** Compatible with Industry Standard 8080A
- Available in either Plastic or Ceramic Package

PIN CONFIGURATION



Rev/1

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FUNCTIONAL DESCRIPTION

The μPD8080AF contains six 8-bit data registers, an 8-bit accumulator, four testable flag bits, and an 8-bit parallel binary arithmetic unit. The μPD8080AF also provides decimal arithmetic capability and it includes 16-bit arithmetic and immediate operators which greatly simplify memory address calculations, and high speed arithmetic operations.

The μPD8080AF utilizes a 16-bit address bus to directly address 64K bytes of memory, is fully TTL compatible (1.9 mA), and utilizes the following addressing modes: Direct; Register; Register Indirect; and Immediate.

The μPD8080AF has a stack architecture wherein any portion of the external memory can be used as a last in/first out (LIFO) stack to store/retrieve the contents of the accumulator, the flags, or any of the data registers.

The μPD8080AF also contains a 16-bit stack pointer to control the addressing of this external stack. One of the major advantages of the stack is that multiple level interrupts can easily be handled since complete system status can be saved when an interrupt occurs and then restored after the interrupt is complete. Another major advantage is that almost unlimited subroutine nesting is possible.

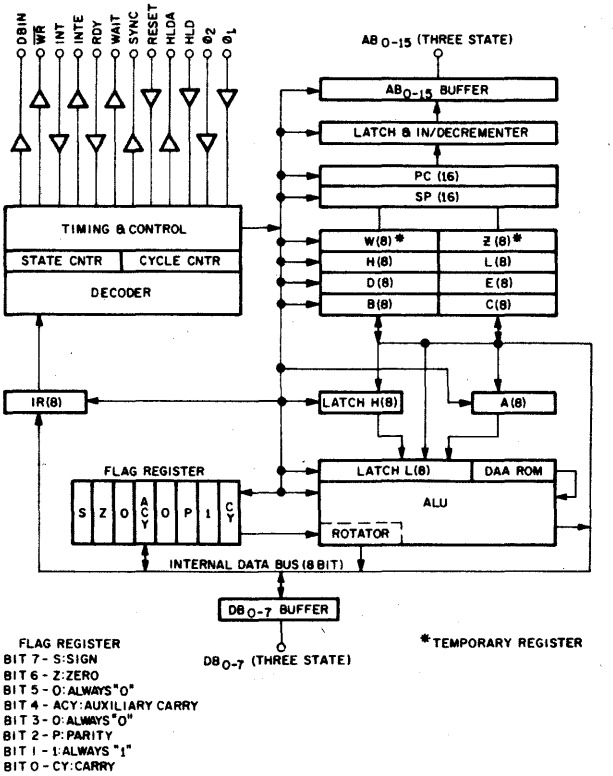
This processor is designed to greatly simplify system design. Separate 16-line address and 8-line bidirectional data busses are employed to allow direct interface to memories and I/O ports. Control signals, requiring no decoding, are provided directly by the processor. All busses, including the control bus, are TTL compatible.

Communication on both the address lines and the data lines can be interlocked by using the HOLD input. When the Hold Acknowledge (HLDA) signal is issued by the processor, its operation is suspended and the address and data lines are forced to be in the FLOATING state. This permits other devices, such as direct memory access channels (DMA), to be connected to the address and data busses.

The μPD8080AF has the capability to accept a multiple byte instruction upon an interrupt. This means that a CALL instruction can be inserted so that any address in the memory can be the starting location for an interrupt program. This allows the assignment of a separate location for each interrupt operation, and as a result no polling is required to determine which operation is to be performed.

NEC offers three versions of the μPD8080AF. These processors have all the features of the μPD8080AF except the clock frequency ranges from 2.0 MHz to 3.0 MHz. These units meet the performance requirements of a variety of systems while maintaining software and hardware compatibility with other 8080A devices.

BLOCK DIAGRAM



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PIN IDENTIFICATION

PIN NO.	PIN SYMBOL	PIN NAME	FUNCTION
1, 25-27, 29-40	$A_{15} - A_0$	Address Bus (output three-state)	The address bus is used to address memory (up to 64K 8-bit words) or specify the I/O device number (up to 256 input and 256 output devices). A_0 is the least significant bit.
2	V_{SS}	Ground (input)	Ground
3-10	$D_7 - D_0$	Data Bus (input/ output three-state)	The bidirectional data bus communicates between the processor, memory, and I/O devices for instructions and data transfers. During each sync time, the data bus contains a status word that describes the current machine cycle. D_0 is the least significant bit.
11	V_{BB}	V_{BB} Supply Voltage (input)	-5V ± 5%
12	RESET	Reset (input)	If the RESET signal is activated, the program counter is cleared. After RESET, the program starts at location 0 in memory. The INTE and HLDA flip-flops are also reset. The flags, accumulator, stack pointer, and registers are not cleared. (Note: External synchronization is not required for the RESET input signal which must be active for a minimum of 3 clock periods.)
13	HOLD	Hold (input)	HOLD requests the processor to enter the HOLD state. The HOLD state allows an external device to gain control of the μPD8080AF address and data buses as soon as the μPD8080AF has completed its use of these buses for the current machine cycle. It is recognized under the following conditions: • The processor is in the HALT state. • The processor is in the T_2 or T_W stage and the READY signal is active. As a result of entering the HOLD state, the ADDRESS BUS ($A_{15} - A_0$) and DATA BUS ($D_7 - D_0$) are in their high impedance state. The processor indicates its state on the HOLD ACKNOWLEDGE (HLDA) pin.
14	INT	Interrupt Request (input)	The μPD8080AF recognizes an interrupt request on this line at the end of the current instruction or while halted. If the μPD8080AF is in the HOLD state, or if the Interrupt Enable flip-flop is reset, it will not honor the request.
15	ϕ_2	Phase Two (input)	Phase two of processor clock.
16	INTE ①	Interrupt Enable (output)	INTE indicates the content of the internal interrupt enable flip-flop. This flip-flop is set by the Enable (EI) or reset by the Disable (DI) interrupt instructions and inhibits interrupts from being accepted by the processor when it is reset. INTE is automatically reset (disabling further interrupts) during T_1 of the instruction fetch cycle (M_1) when an interrupt is accepted and is also reset by the RESET signal.
17	DBIN	Data Bus In (output)	DBIN indicates that the data bus is in the input mode. This signal is used to enable the gating of data onto the μPD8080AF data bus from memory or input ports.
18	$\overline{WR}$	Write (output)	$\overline{WR}$ is used for memory WRITE or I/O output control. The data on the data bus is valid while the $\overline{WR}$ signal is active ($\overline{WR}$ = 0).
19	SYNC	Synchronizing Signal (output)	The SYNC signal indicates the beginning of each machine cycle.
20	V_{CC}	V_{CC} Supply Voltage (input)	+5V ± 5%
21	HLDA	Hold Acknowledge (output)	HLDA is in response to the HOLD signal and indicates that the data and address bus will go to the high impedance state. The HLDA signal begins at: • T_3 for READ memory or input operations. • The clock period following T_3 for WRITE memory or OUTPUT operations. In either case, the HLDA appears after the rising edge of ϕ_1 and high impedance occurs after the rising edge of ϕ_2.
22	ϕ_1	Phase One (input)	Phase one of processor clock.
23	READY	Ready (input)	The READY signal indicates to the μPD8080AF that valid memory or input data is available on the μPD8080AF data bus. READY is used to synchronize the processor with slower memory or I/O devices. If after sending an address out, the μPD8080AF does not receive a high on the READY pin, the μPD8080AF enters a WAIT state for as long as the READY pin is low. (READY can also be used to single step the processor.)
24	WAIT	Wait (output)	The WAIT signal indicates that the processor is in a WAIT state.
28	V_{DD}	V_{DD} Supply Voltage (input)	+12V ± 5%

Note: ① After the EI instruction, the μPD8080AF accepts interrupts on the second instruction following the EI. This allows proper execution of the RET instruction if an interrupt operation is pending after the service routine.

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μPD8080AF

ABSOLUTE MAXIMUM RATINGS*

Operating Temperature . . . . . 0°C to +70°C
Storage Temperature (Ceramic Package) . . . . . -65°C to +150°C
Storage Temperature (Plastic Package) . . . . . -40°C to +125°C
All Output Voltages ① . . . . . -0.3 to +20 Volts
All Input Voltages ① . . . . . -0.3 to +20 Volts
Supply Voltages V_{CC}, V_{DD} and V_{SS} ① . . . . . -0.3 to +20 Volts
Power Dissipation 1.5W
Note: ① Relative to V_{BB}.

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

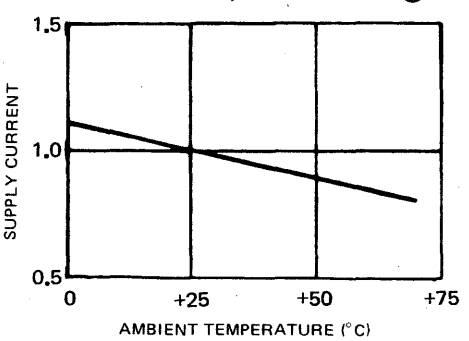
*T_a = 25°C

DC CHARACTERISTICS

T_a = 0°C to +70°C, V_{DD} = +12V ± 5%, V_{CC} = +5V ± 5%, V_{BB} = −5V ± 5%, V_{SS} = 0V, unless otherwise specified.

PARAMETER	SYMBOL	LIMITS MIN	TYP	MAX	UNIT	TEST CONDITIONS
Clock Input Low Voltage	V_{ILC}	V_{SS} - 1		V_{SS} + 0.8	V	
Clock Input High Voltage	V_{IHC}	9.0		V_{DD} + 1	V	
Input Low Voltage	V_{IL}	V_{SS} - 1		V_{SS} + 0.8	V	
Input High Voltage	V_{IH}	3.3		V_{CC} + 1	V	
Output Low Voltage	V_{OL}			0.45	V	I_{OL} = 1.9 mA on all outputs
Output High Voltage	V_{OH}	3.7			V	I_{OH} = −150 μA ②
Avg. Power Supply Current (V_{DD})	$I_{DD(AV)}$		40	70	mA	t_{CY} min
Avg. Power Supply Current (V_{CC})	$I_{CC(AV)}$		60	80	mA	
Avg. Power Supply Current (V_{BB})	$I_{BB(AV)}$		0.01	1	mA	
Input Leakage	I_{IL}			±10 ②	μA	$V_{SS} \leq V_{IN} \leq V_{CC}$
Clock Leakage	I_{CL}			±10 ②	μA	$V_{SS} \leq V_{CLOCK} \leq V_{DD}$
Data Bus Leakage in Input Mode	I_{DL} ①			−100 ②	μA	$V_{SS} \leq V_{IN} \leq V_{SS}$ + 0.8V
				−2 ②	mA	V_{SS} + 0.8V $\leq V_{IN} \leq V_{CC}$
Address and Data Bus Leakage During HOLD	I_{FL}			+10 ②	μA	$V_{ADDR/DATA} = V_{CC}$
				−100 ②		$V_{ADDR/DATA} = V_{SS}$ + 0.45V

TYPICAL SUPPLY CURRENT VS. TEMPERATURE, NORMALIZED ③



Notes: ① When DBIN is high and $V_{IN} > V_{IH}$ internal active pull-up resistors will be switched onto the data bus.
② Minus (−) designates current flow out of the device.
③ ΔI supply/ΔT_a = −0.45%/°C.

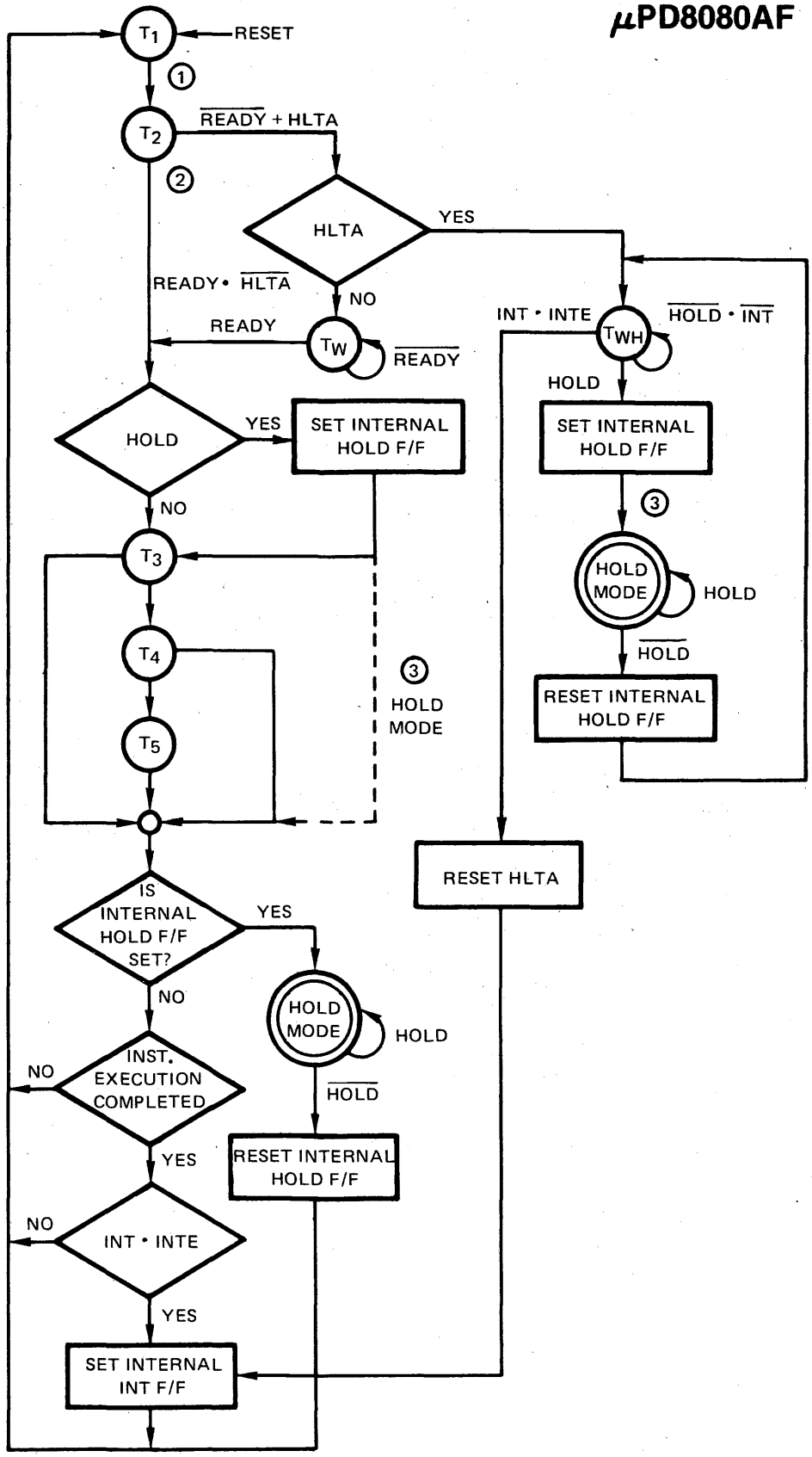
CAPACITANCE

T_a = 25°C, V_{CC} = V_{DD} = V_{SS} = 0V, V_{BB} = −5V.

PARAMETER	SYMBOL	LIMITS MIN	TYP	MAX	UNIT	TEST CONDITIONS
Clock Capacitance	C_ϕ		17	25	pF	f_c = 1 MHz
Input Capacitance	C_{IN}		6	10	pF	Unmeasured Pins
Output Capacitance	C_{OUT}		10	20	pF	Returned to V_{SS}

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PROCESSOR STATE TRANSITION DIAGRAM



Notes:
1. INTE F/F IS RESET IF INTERNAL INT F/F IS SET.
2. INTERNAL INT F/F IS RESET IF INTE F/F IS RESET.
3. IF REQUIRED, T_4 AND T_5 ARE COMPLETED SIMULTANEOUSLY WITH ENTERING HOLD STATE.

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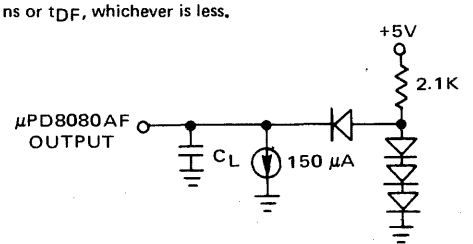
AC CHARACTERISTICS
μPD8080AF

T_a = 0°C to +70°C, V_{DD} = +12V ± 5%, V_{CC} = +5V ± 5%, V_{BB} = −5V ± 5%, V_{SS} = 0V, unless otherwise specified.

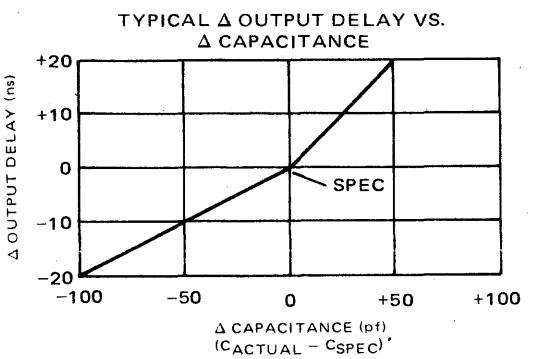
PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Clock Period	t_{CY} ③	0.48		2.0	μsec	
Clock Rise and Fall Time	t_r, t_f	0		50	nsec	
φ1 Pulse Width	$t_{\phi1}$	60			nsec	
φ2 Pulse Width	$t_{\phi2}$	220			nsec	
Delay φ1 to φ2	t_{D1}	0			nsec	
Delay φ2 to φ1	t_{D2}	70			nsec	
Delay φ1 to φ2 Leading Edges	t_{D3}	80			nsec	
Address Output Delay From φ2	t_{DA} ②			200	nsec	C_L = 100 pF
Data Output Delay From φ2	t_{DD} ②			220	nsec	
Signal Output Delay From φ1, or φ2 (SYNC, $\overline{WR}$, WAIT, HLDA)	t_{DC} ②			120	nsec	C_L = 50 pF
DBIN Delay From φ2	t_{DF} ②	25		140	nsec	
Delay for Input Bus to Enter Input Mode	t_{DI} ①			t_{DF}	nsec	
Data Setup Time During φ1 and DBIN	t_{DS1}	30			nsec	
Data Setup Time to φ2 During DBIN	t_{DS2}	150			nsec	
Data Hold Time From φ2 During DBIN	t_{DH} ①	①			nsec	
INTE Output Delay From φ2	t_{IE} ②			200	nsec	C_L = 50 pF
READY Setup Time During φ2	t_{RS}	120			nsec	
HOLD Setup Time to φ2	t_{HS}	140			nsec	
INT Setup Time During φ2 (During φ1 in Halt Mode)	t_{IS}	120			nsec	
Hold Time from φ2 (READY, INT, HOLD)	t_H	0			nsec	
Delay to Float During Hold (Address and Data Bus)	t_{FD}			120	nsec	
Address Stable Prior to $\overline{WR}$	t_{AW} ②	⑤			nsec	C_L = 100 pF: Address, Data C_L = 50 pF: $\overline{WR}$, HLDA, DBIN
Output Data Stable Prior to $\overline{WR}$	t_{DW} ②	⑥			nsec	
Output Data Stable From $\overline{WR}$	t_{WD} ②	⑦			nsec	
Address Stable from $\overline{WR}$	t_{WA} ②	⑦			nsec	
HLDA to Float Delay	t_{HF} ②	⑧			nsec	
$\overline{WR}$ to Float Delay	t_{WF} ②	⑨			nsec	
Address Hold Time after DBIN during HLDA	t_{AH} ②	−20			nsec	

Notes: ① Data input should be enabled with DBIN status. No bus conflict can then occur and data hold time is assured. t_{DH} = 50 ns or t_{DF}, whichever is less.

② Load Circuit.



③ Actual $t_{CY} = t_{D3} + t_{r\phi2} + t_{\phi2} + t_{f\phi2} + t_{D2} + t_{r\phi1} > t_{CY}$ Min.



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AC CHARACTERISTICS
μPD8080AF-2

T_a = 0°C to +70°C, V_{DD} = +12V ± 5%, V_{CC} = +5V ± 5%, V_{BB} = −5V ± 5%, V_{SS} = 0V, unless otherwise specified.

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Clock Period	t_{CY} ③	0.38		2.0	μsec	
Clock Rise and Fall Time	t_r, t_f	0		50	nsec	
φ1 Pulse Width	$t_{\phi1}$	60			nsec	
φ2 Pulse Width	$t_{\phi2}$	175			nsec	
Delay φ1 to φ2	t_{D1}	0			nsec	
Delay φ2 to φ1	t_{D2}	70			nsec	
Delay φ1 to φ2 Leading Edges	t_{D3}	70			nsec	
Address Output Delay From φ2	t_{DA} ②			175	nsec	C_L = 100 pF
Data Output Delay From φ2	t_{DD} ②			200	nsec	
Signal Output Delay From φ1, or φ2 (SYNC, $\overline{WR}$, WAIT, HLDA)	t_{DC} ②			120	nsec	C_L = 50 pF
DBIN Delay From φ2	t_{DF} ②	25		140	nsec	
Delay for Input Bus to Enter Input Mode	t_{DI} ①			t_{DF}	nsec	
Data Setup Time During φ1 and DBIN	t_{DS1}	20			nsec	
Data Setup Time to φ2 During DBIN	t_{DS2}	130			nsec	
Data Hold Time From φ2 During DBIN	t_{DH} ①	①			nsec	
INTE Output Delay From φ2	t_{IE} ②			200	nsec	C_L = 50 pF
READY Setup Time During φ2	t_{RS}	90			nsec	
HOLD Setup Time to φ2	t_{HS}	120			nsec	
INT Setup Time During φ2 (for all modes)	t_{IS}	100			nsec	
Hold Time from φ2 (READY, INT, HOLD)	t_H	0			nsec	
Delay to Float During Hold (Address and Data Bus)	t_{FD}			120	nsec	
Address Stable Prior to $\overline{WR}$	t_{AW} ②	⑤			nsec	C_L = 100 pF: Address, Data C_L = 50 pF: $\overline{WR}$, HLDA, DBIN
Output Data Stable Prior to $\overline{WR}$	t_{DW} ②	⑥			nsec	
Output Data Stable From $\overline{WR}$	t_{WD} ②	⑦			nsec	
Address Stable from $\overline{WR}$	t_{WA} ②	⑦			nsec	
HLDA to Float Delay	t_{HF} ②	⑧			nsec	
$\overline{WR}$ to Float Delay	t_{WF} ②	⑨			nsec	
Address Hold Time after DBIN during HLDA	t_{AH} ②	−20			nsec	

Notes Continued:

④ The following are relevant when interfacing the μPD8080AF to devices having V_{IH} = 3.3V.

a. Maximum output rise time from 0.8V to 3.3V = 100 ns at C_L = SPEC.

b. Output delay when measured to 3.0V = SPEC +60 ns at C_L = SPEC.

c. If $C_L \neq$ SPEC, add 0.6 ns/pF if $C_L > C_{SPEC}$, subtract 0.3 ns/pF (from modified delay) if $C_L < C_{SPEC}$.

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AC CHARACTERISTICS
μPD8080AF-1

T_a = 0°C to +70°C, V_{DD} = +12V ± 5%, V_{CC} = +5V ± 5%, V_{BB} = −5V ± 5%, V_{SS} = 0V, unless otherwise specified.

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Clock Period	t_{CY} ③	0.32		2.0	μsec	
Clock Rise and Fall Time	t_r, t_f	0		25	nsec	
φ1 Pulse Width	$t_{\phi1}$	50			nsec	
φ2 Pulse Width	$t_{\phi2}$	145			nsec	
Delay φ1 to φ2	t_{D1}	0			nsec	
Delay φ2 to φ1	t_{D2}	60			nsec	
Delay φ1 to φ2 Leading Edges	t_{D3}	60			nsec	
Address Output Delay From φ2	t_{DA} ②			150	nsec	C_L = 50 pF
Data Output Delay From φ2	t_{DD} ②			180	nsec	
Signal Output Delay From φ1, or φ2 (SYNC, $\overline{WR}$, WAIT, HLDA)	t_{DC} ②			110	nsec	C_L = 50 pF
DBIN Delay From φ2	t_{DF} ②	25		130	nsec	
Delay for Input Bus to Enter Input Mode	t_{DI} ①			t_{DF}	nsec	
Data Setup Time During φ1 and DBIN	t_{DS1}	10			nsec	
Data Setup Time to φ2 During DBIN	t_{DS2}	120			nsec	
Data Hold Time From φ2 During DBIN	t_{DH} ①	①			nsec	
INTE Output Delay From φ2	t_{IE} ②			200	nsec	C_L = 50 pF
READY Setup Time During φ2	t_{RS}	90			nsec	
HOLD Setup Time to φ2	t_{HS}	120			nsec	
INT Setup Time During φ2 (for all modes)	t_{IS}	100			nsec	
Hold Time from φ2 (READY, INT, HOLD)	t_H	0			nsec	
Delay to Float During Hold (Address and Data Bus)	t_{FD}			120	nsec	
Address Stable Prior to $\overline{WR}$	t_{AW} ②	⑤			nsec	C_L = 50 pF: Address, Data C_L = 50 pF: $\overline{WR}$, HLDA, DBIN
Output Data Stable Prior to $\overline{WR}$	t_{DW} ②	⑥			nsec	
Output Data Stable From $\overline{WR}$	t_{WD} ②	⑦			nsec	
Address Stable from $\overline{WR}$	t_{WA} ②	⑦			nsec	
HLDA to Float Delay	t_{HF} ②	⑧			nsec	
$\overline{WR}$ to Float Delay	t_{WF} ②	⑨			nsec	
Address Hold Time after DBIN during HLDA	t_{AH} ②	−20			nsec	

Notes Continued: ⑤

Device	t_{AW}
μPD8080AF	$2\,t_{CY} - t_{D3} - t_{r\phi2} - 140$
μPD8080AF-2	$2\,t_{CY} - t_{D3} - t_{r\phi2} - 130$
μPD8080AF-1	$2\,t_{CY} - t_{D3} - t_{r\phi2} - 110$

⑥

Device	t_{DW}
μPD8080AF	$t_{CY} - t_{D3} - t_{r\phi2} - 170$
μPD8080AF-2	$t_{CY} - t_{D3} - t_{r\phi2} - 170$
μPD8080AF-1	$t_{CY} - t_{D3} - t_{r\phi2} - 150$

⑦ If not HLDA, $t_{WD} = t_{WA} = t_{D3} + t_{r\phi2} + 10$ ns. If HLDA, $t_{WD} = t_{WA} = t_{WF}$.

⑧ $t_{HF} = t_{D3} + t_{r\phi2} - 50$ ns.

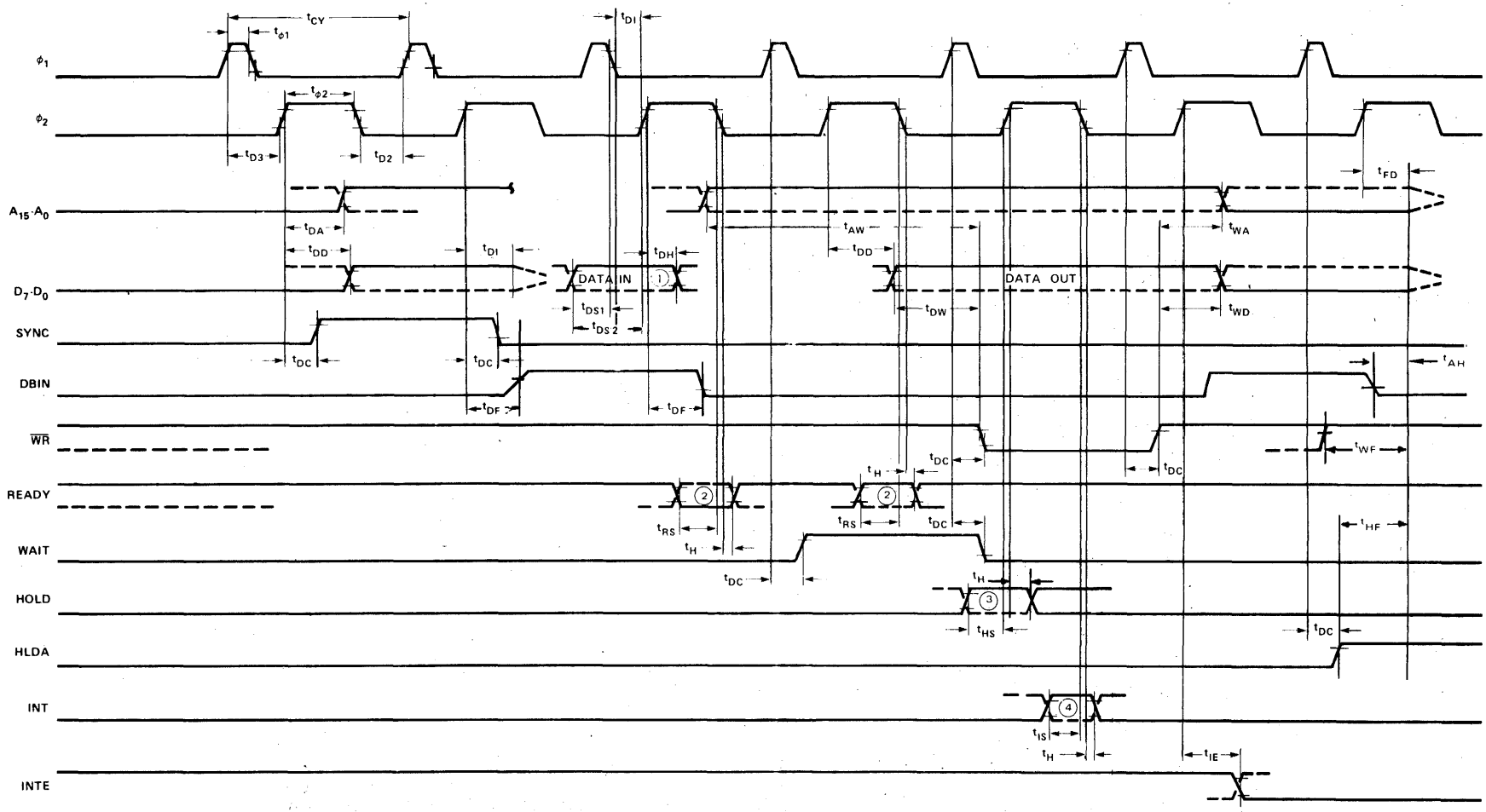
⑨ $t_{WF} = t_{D3} + t_{r\phi2} - 10$ ns.

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TIMING WAVEFORMS (5)

(Note: Timing measurements are made at the following reference voltages: CLOCK "1" = 8.0V, "0" = 1.0V; INPUTS "1" = 3.3V, "0" = 0.8V; OUTPUTS "1" = 2.0V, "0" = 0.8V.)



Notes:
(1) Data in must be stable for this period during DBIN • T_3. Both t_{DS1} and t_{DS2} must be satisfied.
(2) Ready signal must be stable for this period during T_2 or T_W. (Must be externally synchronized.)
(3) Hold signal must be stable for this period during T_2 or T_W when entering hold mode, and during T_3, T_4, T_5 and T_{WH} when in hold mode. (External synchronization is not required.)
(4) Interrupt signal must be stable during this period of the last clock cycle of any instruction in order to be recognized in the following instruction. (External synchronization is not required.)
(5) This timing diagram shows timing relationships only; it does not represent any specific machine cycle.
(6) Timing measurements are made at the following reference voltages: CLOCK "1" = 8.0V, "0" = 1.0V; INPUTS "1" = 3.3V; "0" = 0.8V; OUTPUTS "1" = 2.0V, "0" = 0.8V.

INSTRUCTION SET

The instruction set includes arithmetic and logical operators with direct, register, indirect, and immediate addressing modes.

Move, load, and store instruction groups provide the ability to move either 8 or 16 bits of data between memory, the six working registers and the accumulator using direct, register, indirect, and immediate addressing modes.

The ability to branch to different portions of the program is provided with direct, conditional, or computed jumps. Also the ability to call and return from subroutines is provided both conditionally and unconditionally. The RESTART (or single byte call instruction) is useful for interrupt vector operation.

Conditional jumps, calls and returns execute based on the state of the four testable flags (Sign, Zero, Parity and Carry). The state of each flag is determined by the result of the last instruction executed that affected flags. (See Instruction Set Table.)

The Sign flag is set (High) if bit 7 of the result is a "1"; otherwise it is reset (Low). The Zero flag is set if the result is "0"; otherwise it is reset. The Parity flag is set if the modulo 2 sum of the bits of the result is "0" (Even Parity); otherwise (Odd Parity) it is reset. The Carry flag is set if the last instruction resulted in a carry or a borrow out of the most significant bit (bit 7) of the result; otherwise it is reset.

In addition to the four testable flags, the μPD8080AF has another flag (ACY) that is not directly testable. It is used for multiple precision arithmetic operations with the DAA instruction. The Auxiliary Carry flag is set if the last instruction resulted in a carry or a borrow from bit 3 into bit 4; otherwise it is reset.

Double precision operators such as stack manipulation and double add instructions extend both the arithmetic and interrupt handling capability of the μPD8080AF. The ability to increment and decrement memory, the six general registers and the accumulator are provided as well as extended increment and decrement instructions to operate on the register pairs and stack pointer. Further capability is provided by the ability to rotate the accumulator left or right through or around the carry bit.

Input and output may be accomplished using memory addresses as I/O ports or the directly addressed I/O provided for in the μPD8080AF instruction set.

The special instruction group completes the μPD8080AF instruction set: NOP, HALT stop processor execution; DAA provides decimal arithmetic capability; STC sets the carry flag; CMC complements it; CMA complements the contents of the accumulator; and XCHG exchanges the contents of two 16-bit register pairs directly.

DATA AND INSTRUCTION FORMATS

Data in the μPD8080AF is stored as 8-bit binary integers. All data/instruction transfers to the system data bus are in the following format:

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0

MSB DATA WORD LSB

Instructions are one, two, or three bytes long. Multiple byte instructions must be stored in successive locations of program memory. The address of the first byte is used as the address of the instruction.

									TYPICAL INSTRUCTIONS
One Byte Instructions									
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	OP CODE	Register to register, memory reference, arithmetic or logical, rotate, return, push, pop, enable, or disable interrupt instructions
Two Byte Instructions									
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	OP CODE	Immediate mode or I/O instructions
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	OPERAND	
Three Byte Instructions									
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	OP CODE	Jump, call or direct load and store instructions
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	LOW ADDRESS OR OPERAND 1	
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	HIGH ADDRESS OR OPERAND 2	

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MNEMONIC[1]	DESCRIPTION	INSTRUCTION CODE[2] D7	D6	D5	D4	D3	D2	D1	D0	Clock Cycles[3]	FLAGS[4] SIGN	ZERO	PARITY	CARRY
MOVE														
MOV d,s	Move register to register	0	1	d	d	d	s	s	s	5				
MOV M,s	Move register to memory	0	1	1	1	0	s	s	s	7				
MOV d,M	Move memory to register	0	1	d	d	d	1	1	0	7				
MVI d,D8	Move immediate to register	0	0	d	d	d	1	1	0	7				
MVI M,D8	Move immediate to memory	0	0	1	1	0	1	1	0	10				
INCREMENT/DECREMENT														
INR d	Increment register	0	0	d	d	d	1	0	0	5	•	•	•	
DCR d	Decrement register	0	0	d	d	d	1	0	1	5	•	•	•	
INR M	Increment memory	0	0	1	1	0	1	0	0	10	•	•	•	
DCR M	Decrement memory	0	0	1	1	0	1	0	1	10	•	•	•	
ALU – REGISTER TO ACCUMULATOR														
ADD s	Add register to A	1	0	0	0	0	s	s	s	4	•	•	•	•
ADC s	Add register to A with carry	1	0	0	0	1	s	s	s	4	•	•	•	•
SUB s	Subtract register from A	1	0	0	1	0	s	s	s	4	•	•	•	•
SBB s	Subtract register from A with borrow	1	0	0	1	1	s	s	s	4	•	•	•	•
ANA s	AND register with A	1	0	1	0	0	s	s	s	4	•	•	•	0
XRA s	Exclusive OR Register with A	1	0	1	0	1	s	s	s	4	•	•	•	0
ORA s	OR register with A	1	0	1	1	0	s	s	s	4	•	•	•	0
CMP s	Compare register with A	1	0	1	1	1	s	s	s	4	•	•	•	•
ALU – MEMORY TO ACCUMULATOR														
ADD M	Add memory to A	1	0	0	0	0	1	1	0	7	•	•	•	•
ADC M	Add memory to A with carry	1	0	0	0	1	1	1	0	7	•	•	•	•
SUB M	Subtract memory from A	1	0	0	1	0	1	1	0	7	•	•	•	•
SBB M	Subtract memory from A with borrow	1	0	0	1	1	1	1	0	7	•	•	•	•
ANA M	AND memory with A	1	0	1	0	0	1	1	0	7	•	•	•	0
XRA M	Exclusive OR memory with A	1	0	1	0	1	1	1	0	7	•	•	•	0
ORA M	OR memory with A	1	0	1	1	0	1	1	0	7	•	•	•	0
CMP M	Compare memory with A	1	0	1	1	1	1	1	0	7	•	•	•	•
ALU – IMMEDIATE TO ACCUMULATOR														
ADI D8	Add immediate to A	1	1	0	0	0	1	1	0	7	•	•	•	•
ACI D8	Add immediate to A with carry	1	1	0	0	1	1	1	0	7	•	•	•	•
SUI D8	Subtract immediate from A	1	1	0	1	0	1	1	0	7	•	•	•	•
SBI D8	Subtract immediate from A with borrow	1	1	0	1	1	1	1	0	7	•	•	•	•
ANI D8	AND immediate with A	1	1	1	0	0	1	1	0	7	•	•	•	0
XRI D8	Exclusive OR immediate with A	1	1	1	0	1	1	1	0	7	•	•	•	0
ORI D8	OR immediate with A	1	1	1	1	0	1	1	0	7	•	•	•	0
CPI D8	Compare immediate with A	1	1	1	1	1	1	1	0	7	•	•	•	•
ALU – ROTATE														
RLC	Rotate A left, MSB to carry (8-bit)	0	0	0	0	0	1	1	1	4				•
RRC	Rotate A right, LSB to carry (8-bit)	0	0	0	0	1	1	1	1	4				•
RAL	Rotate A left through carry (9-bit)	0	0	0	1	0	1	1	1	4				•
RAR	Rotate A right through carry (9-bit)	0	0	0	1	1	1	1	1	4				•
JUMP														
JMP ADDR	Jump unconditional	1	1	0	0	0	0	1	1	10				
JNZ ADDR	Jump on not zero	1	1	0	0	0	0	1	0	10				
JZ ADDR	Jump on zero	1	1	0	0	1	0	1	0	10				
JNC ADDR	Jump on no carry	1	1	0	1	0	0	1	0	10				
JC ADDR	Jump on carry	1	1	0	1	1	0	1	0	10				
JPO ADDR	Jump on parity odd	1	1	1	0	0	0	1	0	10				
JPE ADDR	Jump on parity even	1	1	1	0	1	0	1	0	10				
JP ADDR	Jump on positive	1	1	1	1	0	0	1	0	10				
JM ADDR	Jump on minus	1	1	1	1	1	0	1	0	10				
CALL														
CALL ADDR	Call unconditional	1	1	0	0	1	1	0	1	17				
CNZ ADDR	Call on not zero	1	1	0	0	0	1	0	0	11/17				
CZ ADDR	Call on zero	1	1	0	0	1	1	0	0	11/17				
CNC ADDR	Call on no carry	1	1	0	1	0	1	0	0	11/17				
CC ADDR	Call on carry	1	1	0	1	1	1	0	0	11/17				
CPO ADDR	Call on parity odd	1	1	1	0	0	1	0	0	11/17				
CPE ADDR	Call on parity even	1	1	1	0	1	1	0	0	11/17				
CP ADDR	Call on positive	1	1	1	1	0	1	0	0	11/17				
CM ADDR	Call on minus	1	1	1	1	1	1	0	0	11/17				
RETURN														
RET	Return	1	1	0	0	1	0	0	1	10				
RNZ	Return on not zero	1	1	0	0	0	0	0	0	5/11				
RZ	Return on zero	1	1	0	0	1	0	0	0	5/11				
RNC	Return on no carry	1	1	0	1	0	0	0	0	5/11				
RC	Return on carry	1	1	0	1	1	0	0	0	5/11				
RPO	Return on parity odd	1	1	1	0	0	0	0	0	5/11				
RPE	Return on parity even	1	1	1	0	1	0	0	0	5/11				
RP	Return on positive	1	1	1	1	0	0	0	0	5/11				
RM	Return on minus	1	1	1	1	1	0	0	0	5/11				

MNEMONIC[1]	DESCRIPTION	INSTRUCTION CODE[2] D7	D6	D5	D4	D3	D2	D1	D0	Clock Cycles[3]	FLAGS[4] SIGN	ZERO	PARITY	CARRY
LOAD REGISTER PAIR														
LXI B,D16	Load immediate register pair BC	0	0	0	0	0	0	0	1	10				
LXI D,D16	Load immediate register pair DE	0	0	0	1	0	0	0	1	10				
LXI H,D16	Load immediate register pair HL	0	0	1	0	0	0	0	1	10				
LXI SP,D16	Load immediate Stack Pointer	0	0	1	1	0	0	0	1	10				
PUSH														
PUSH B	Push register pair BC on stack	1	1	0	0	0	1	0	1	11				
PUSH D	Push register pair DE on stack	1	1	0	1	0	1	0	1	11				
PUSH H	Push register pair HL on stack	1	1	1	0	0	1	0	1	11				
PUSH PSW	Push A and flags on stack	1	1	1	1	0	1	0	1	11				
POP														
POP B	Pop register pair BC off stack	1	1	0	0	0	0	0	1	10				
POP D	Pop register pair DE off stack	1	1	0	1	0	0	0	1	10				
POP H	Pop register pair HL off stack	1	1	1	0	0	0	0	1	10				
POP PSW	Pop A and flags off stack	1	1	1	1	0	0	0	1	10	•	•	•	•
DOUBLE ADD														
DAD B	Add BC to HL	0	0	0	0	1	0	0	1	10				•
DAD D	Add DE to HL	0	0	0	1	1	0	0	1	10				•
DAD H	Add HL to HL	0	0	1	0	1	0	0	1	10				•
DAD SP	Add Stack Pointer to HL	0	0	1	1	1	0	0	1	10				•
INCREMENT REGISTER PAIR														
INX B	Increment BC	0	0	0	0	0	0	1	1	5				
INX D	Increment DE	0	0	0	1	0	0	1	1	5				
INX H	Increment HL	0	0	1	0	0	0	1	1	5				
INX SP	Increment Stack Pointer	0	0	1	1	0	0	1	1	5				
DECREMENT REGISTER PAIR														
DCX B	Decrement BC	0	0	0	0	1	0	1	1	5				
DCX D	Decrement DE	0	0	0	1	1	0	1	1	5				
DCX H	Decrement HL	0	0	1	0	1	0	1	1	5				
DCX SP	Decrement Stack Pointer	0	0	1	1	1	0	1	1	5				
REGISTER INDIRECT														
STAX B	Store A at ADDR in BC	0	0	0	0	0	0	1	0	7				
STAX D	Store A at ADDR in DE	0	0	0	1	0	0	1	0	7				
LDAX B	Load A at ADDR in BC	0	0	0	0	1	0	1	0	7				
LDAX D	Load A at ADDR in DE	0	0	0	1	1	0	1	0	7				
DIRECT														
STA ADDR	Store A direct	0	0	1	1	0	0	1	0	13				
LDA ADDR	Load A direct	0	0	1	1	1	0	1	0	13				
SHLD ADDR	Store HL direct	0	0	1	0	0	0	1	0	16				
LHLD ADDR	Load HL direct	0	0	1	0	1	0	1	0	16				
MOVE REGISTER PAIR														
XCHG	Exchange DE and HL register pairs	1	1	1	0	1	0	1	1	4				
XTHL	Exchange top of stack and HL	1	1	1	0	0	0	1	1	18				
SPHL	HL to Stack Pointer	1	1	1	1	1	0	0	1	5				
PCHL	HL to Program Counter	1	1	1	0	1	0	0	1	5				
INPUT/OUTPUT														
IN A	Input	1	1	0	1	1	0	1	1	10				
OUT A	Output	1	1	0	1	0	0	1	1	10				
EI	Enable interrupts	1	1	1	1	1	0	1	1	4				
DI	Disable interrupts	1	1	1	1	0	0	1	1	4				
RST A	Restart	1	1	A	A	A	1	1	1	11				
MISCELLANEOUS														
CMA	Complement A	0	0	1	0	1	1	1	1	4				
STC	Set carry	0	0	1	1	0	1	1	1	4				1 Cy
CMC	Complement carry	0	0	1	1	1	1	1	1	4				
DAA	Decimal adjust A	0	0	1	0	0	1	1	1	4	•	•	•	•
NOP	No operation	0	0	0	0	0	0	0	0	4				
HLT	Halt	0	1	1	1	0	1	1	0	7				

Notes:

[1]Operand Symbols used
A = 8-bit address or expression
s = source register
d = destination register
PSW = Processor Status Word
SP = Stack Pointer
D8 = 8-bit data quantity, expression, or constant, always B_2 of instruction
D16 = 16-bit data quantity, expression, or constant, always B_3B_2 of instruction
ADDR = 16-bit Memory address expression

[2]ddd or sss – 000 B – 001 C – 010 D – 011 E – 100 H – 101 L – 110 Memory – 111 A.

[3]Two possible cycle times (5/11) indicate instruction cycles dependent on condition flags.

[4]• = flag affected
= flag not affected
0 = flag reset
1 = flag set

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INSTRUCTION CYCLE TIMES

One to five machine cycles ($M_1 - M_5$) are required to execute an instruction. Each machine cycle involves the transfer of an instruction or data byte into the processor or a transfer of a data byte out of the processor (the sole exception being the double add instruction). The first one, two or three machine cycles obtain the instruction from the memory or an interrupting I/O controller. The remaining cycles are used to execute the instruction. Each machine cycle requires from three to five clock times ($T_1 - T_5$). During $\phi_1 \cdot$ SYNC of each machine cycle, a status word that identifies the type of machine cycle is available on the data bus.

Execution times and machine cycles used for each type of instruction are shown below.

INSTRUCTION	MACHINE CYCLES EXECUTED	CLOCK TIMES (MIN/MAX)
RST X and PUSH RP	PCR5 ① SPW3 ⑤ SPW3 ⑤	11
All CALL Instructions	PCR5 ① PCR3 ② PCR3 ② SPW3 ⑤ SPW3 ⑤	11/17
Conditional TURN Instructions	PCR5 ① SPR3 ④ SPR3 ④	5/11
RET Instruction	PCR4 ① SPR3 ④ SPR3 ④	10
XTHL	PCR4 ① SPR3 ④ SPR3 ④ SPW3 ⑤ SPW5 ⑤	18
DAD RP	PCR4 ① PCX3 Ⓧ PCX3 Ⓧ	10
INR R; INX RP, DCR R; DCX RP; PCHL; MOV R, R; SPHL	PCR5 ①	5
All JUMP Instructions and LXI RP	PCR4 ① PCR3 ② PCR3 ②	10
POP RP	PCR4 ① SPR3 ④ SPR3 ④	10
LDA	PCR4 ① PCR3 ② PCR3 ② BBR3 ②	13
STA	PCR4 ① PCR3 ② PCR3 ② BBW3 ③	13
LHLD	PCR4 ① PCR3 ② PCR3 ② BBR3 ② BBR3 ②	16
SHLD	PCR4 ① PCR3 ② PCR3 ② BBW3 ③ BBW3 ③	16
STAX B	PCR4 ① BCW3 ③	7
STAX D	PCR4 ① DEW3 ③	7
LDAX B	PCR4 ① BCR3 ②	7
LDAX D	PCR4 ① DER3 ②	7
MOV R, M; ADD M; ADC M; SUB M; SB B M; ANA M; XRA M; ORA M; CMP M	PCR4 ① HLR3 ②	7
INR M and DCR M	PCR4 ① HLR3 ② HLW3 ③	10
MVI M	PCR4 ① PCR3 ② HLW3 ③	10
MVI R; ADI; ACI; SUI; SBI; ANI; XRI; ORI; CPI	PCR4 ① PCR3 ②	7
MOV M, R	PCR4 ① HLW3 ③	7
EI; DI ADD R; ADC R; SUB R; SBB R; ANA R; XRA R; ORA R; CMP R; RLC; RRC; RAL; RAR; DAA; CMA; STC; CMC; NOP; XCHG	PCR4 ①	4
OUT	PCR4 ① PCR3 ② ABW3 ⑦	10
IN	PCR4 ① PCR3 ② ABR3 ⑥	10
HLT	PCR4 ① PCX3 ⑨	7

Machine Cycle Symbol Definition

XX Y Z (N)
- XXYZ: Status word defining type of machine cycle (See Status Word Chart)
- Y: Number of clocks for this machine cycle
- Z: R = Read cycle – data into processor; W = Write cycle – data out of processor; X = No data transfer; PC = Program Counter used as address
- (N): Underlined (XXYZ(N)) indicates machine cycle is executed if condition is True.

XX:
- HL = Registers H and L used as address
- BC = Registers B and C used as address
- DE = Registers D and E used as address
- SP = Stack Pointer used as address
- BB = Byte 2 and 3 used as address
- AB = Byte 2 used as address

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STATUS INFORMATION DEFINITION

SYMBOLS	DATA BUS BIT	DEFINITION
INTA ①	D_0	Acknowledge signal for INTERRUPT request. Signal should be used to gate a restart or CALL instruction onto the data bus when DBIN is active.
$\overline{WO}$	D_1	Indicates that the operation in the current machine cycle will be a WRITE memory or OUTPUT function ($\overline{WO}$ = 0). Otherwise, a READ memory or INPUT operation will be executed.
STACK	D_2	Indicates that the address bus holds the pushdown stack address from the Stack Pointer.
HLTA	D_3	Acknowledge signal for HALT instruction.
OUT	D_4	Indicates that the address bus contains the address of an output device and the data bus will contain the output data when $\overline{WR}$ is active.
M_1	D_5	Provides a signal to indicate that the CPU is in the fetch cycle for the first byte of an instruction.
INP ①	D_6	Indicates that the address bus contains the address of an input device and the input data should be placed on the data bus when DBIN is active.
MEMR ①	D_7	Designates that the data bus will be used for memory read data.

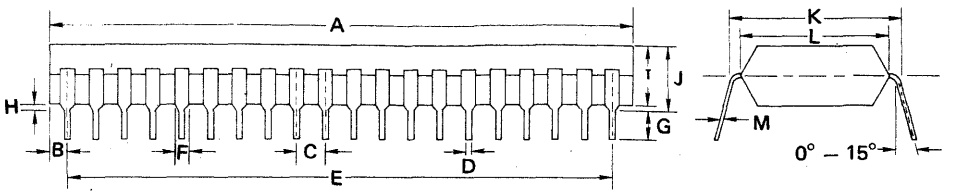
Note: ① These three status bits can be used to control the flow of data onto the μPD8080AF data bus.

STATUS WORD CHART

TYPE OF MACHINE CYCLE

DATA BUS BIT	STATUS INFORMATION	① INSTRUCTION FETCH	② MEMORY READ	③ MEMORY WRITE	④ STACK READ	⑤ STACK WRITE	⑥ INPUT READ	⑦ OUTPUT WRITE	⑧ INTERRUPT ACKNOWLEDGE	⑨ HALT ACKNOWLEDGE	⑩ INT. ACK. WHILE HALT
											← (N) STATUS WORD
D_0	INTA	0	0	0	0	0	0	0	1	0	1
D_1	$\overline{WO}$	1	1	0	1	0	1	0	1	1	1
D_2	STACK	0	0	0	1	1	0	0	0	0	0
D_3	HLTA	0	0	0	0	0	0	0	0	1	1
D_4	OUT	0	0	0	0	0	0	1	0	0	0
D_5	M_1	1	0	0	0	0	0	0	1	0	1
D_6	INP	0	0	0	0	0	1	0	0	0	0
D_7	MEMR	1	1	0	1	0	0	0	0	1	0

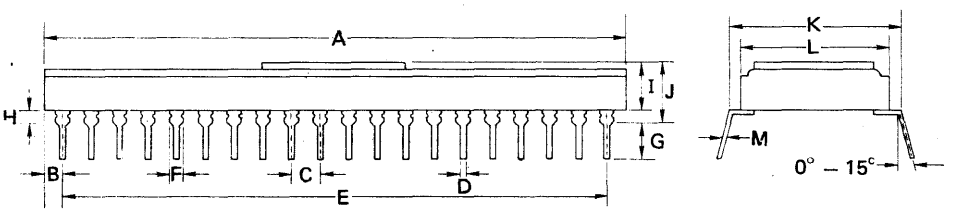
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PACKAGE OUTLINE
μPD8080AFC/D

μPD8080AFC
(Plastic)

ITEM	MILLIMETERS	INCHES
A	51.5 MAX	2.028 MAX
B	1.62	0.064
C	2.54	0.10
D	0.5 ± 0.1	0.019 ± 0.004
E	48.26	1.9
F	1.2 MIN	0.047 MIN
G	2.54 MIN	0.10 MIN
H	0.5 MIN	0.019 MIN
I	5.22 MAX	0.206 MAX
J	5.72 MAX	0.225 MAX
K	15.24	0.600
L	13.2	0.520
M	$0.25^{+0.1}_{-0.05}$	$0.010^{+0.004}_{-0.002}$



μPD8080AFD
(Ceramic)

ITEM	MILLIMETERS	INCHES
A	51.5 MAX	2.028 MAX
B	1.62	0.064
C	2.54	0.100
D	0.50 ± 0.1	0.0197 ± 0.004
E	48.26 ± 0.2	1.900 ± 0.008
F	1.27	0.050
G	3.2 MIN	0.126 MIN
H	1.0 MIN	0.04 MIN
I	4.2 MAX	0.17 MAX
J	5.2 MAX	0.205 MAX
K	15.24	0.6
L	13.5	0.531
M	0.30 ± 0.1	0.012 ± 0.004

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μPD8085A SINGLE CHIP 8-BIT N-CHANNEL MICROPROCESSOR

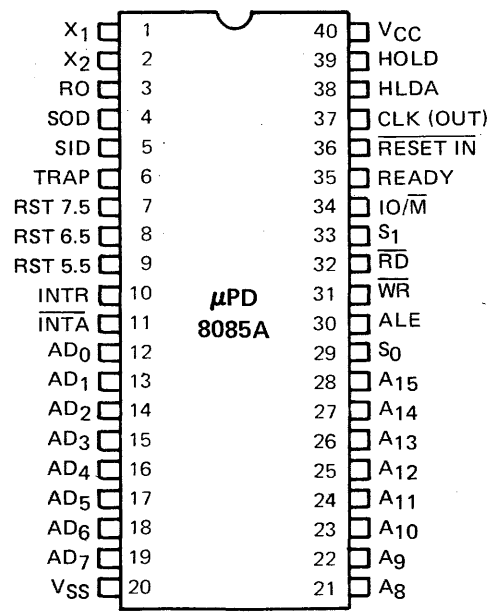
DESCRIPTION

The μPD8085A is a single chip 8-bit microprocessor which is 100 percent software compatible with the industry standard 8080A. It has the ability of increasing system performance of the standard 8080A by operating at a higher speed. Using the μPD8085A in conjunction with its family of ICs allows the designer complete flexibility with minimum chip count.

FEATURES

- Single Power Supply: +5 Volt
- Internal Clock Generation and System Control
- Internal Serial In/Out Port.
- Fully TTL Compatible
- Internal 4-Level Interrupt Structure
- Multiplexed Address/Data Bus for Increased System Performance
- Complete Family of Components for Design Flexibility
- Software Compatible with Standard 8080A
- Available in Either Plastic or Ceramic Package

PIN CONFIGURATION



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FUNCTIONAL DESCRIPTION

The μPD8085A contains six 8-bit data registers, an 8-bit accumulator, four testable flag bits, and an 8-bit parallel binary arithmetic unit. The μPD8085A also provides decimal arithmetic capability and it includes 16-bit arithmetic and immediate operators which greatly simplify memory address calculations, and high speed arithmetic operations.

The μPD8085A has a stack architecture wherein any portion of the external memory can be used as a last in/first out (LIFO) stack to store/retrieve the contents of the accumulator, the flags, or any of the data registers.

The μPD8085A also contains a 16-bit stack pointer to control the addressing of this external stack. One of the major advantages of the stack is that multiple level interrupts can easily be handled since complete system status can be saved when an interrupt occurs and then restored after the interrupt is complete. Another major advantage is that almost unlimited subroutine nesting is possible.

The μPD8085A was designed with speed and simplicity of the overall system in mind. The multiplexed address/data bus increases available pins for advanced functions in the processor and peripheral chips while providing increased system speed and less critical timing functions. All signals to and from the μPD8085A are fully TTL compatible.

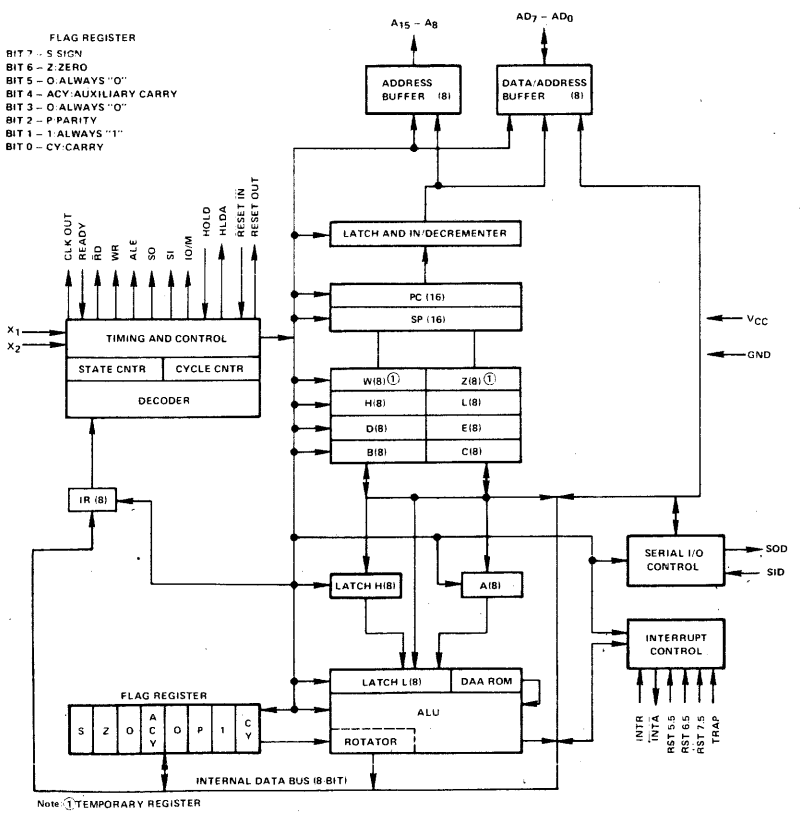
The internal interrupt structure of the μPD8085A features 4 levels of prioritized interrupt with three levels internally maskable.

Communication on both the address lines and the data lines can be interlocked by using the HOLD input. When the Hold Acknowledge (HLDA) signal is issued by the processor, its operation is suspended and the address, data and control lines are forced to be in the FLOATING state. This permits other devices, such as direct memory access channels (DMA), to be connected to the address and data busses.

The μPD8085A features internal clock generation with status outputs available for advanced read/write timing and memory/IO instruction indications. The clock may be crystal controlled, RC controlled, or driven by an external signal.

On chip serial in/out port is available and controlled by the newly added RIM and SIM instructions.

BLOCK DIAGRAM



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PIN IDENTIFICATION

PIN NO.	PIN SYMBOL	PIN NAME	FUNCTION
1, 2	X_1, X_2	Crystal In	Crystal, RC, or external clock input
3	RO	Reset Out	Acknowledge that the processor is being reset to be used as a system reset
4	SOD	Serial Out Data	1-bit data out by the SIM instruction
5	SID	Serial In Data	1-bit data into ACC bit 7 by the RIM instruction
6	Trap	Trap Interrupt Input	Highest priority nonmaskable restart interrupt
7 8 9	RST 7.5 RST 6.5 RST 5.5	Restart Interrupts	Priority restart interrupt inputs, of which 7.5 is the highest and 5.5 the lowest priority
10	INTR	Interrupt Request In	A general interrupt input which stops the PC from incrementing, generates $\overline{INTA}$, and samples the data bus for a restart or call instruction
11	$\overline{INTA}$	Interrupt Acknowledge	An output which indicates that the processor has responded to INTR
12-19	$AD_0 - AD_7$	Low Address/Data Bus	Multiplexed low address and data bus
20	V_{SS}	Ground	Ground Reference
21-28	$A_8 - A_{15}$	High Address Bus	Nonmultiplexed high 8-bits of the address bus
29, 33	S_0, S_1	Status Outputs	Outputs which indicate data bus status: Halt, Write, Read, Fetch
30	ALE	Address Latch Enable Out	A signal which indicates that the lower 8-bits of address are valid on the AD lines
31, 32	$\overline{WR}$, $\overline{RD}$	Write/Read Strobes Out	Signals out which are used as write and read strobes for memory and I/O devices
34	IO/$\overline{M}$	I/O or Memory Indicator	A signal out which indicates whether $\overline{RD}$ or $\overline{WR}$ strobes are for I/O or memory devices
35	Ready	Ready Input	An input which is used to increase the data and address bus access times (can be used for slow memory)
36	$\overline{Reset\ In}$	Reset Input	An input which is used to start the processor activity at address 0, resetting IE and HLDA flip-flops
37	CLK	Clock Out	System Clock Output
38, 39	HLDA, HOLD	Hold Acknowledge Out and Hold Input Request	Used to request and indicate that the processor should relinquish the bus for DMA activity. When hold is acknowledged, $\overline{RD}$, $\overline{WR}$, IO/$\overline{M}$, Address and Data busses are all 3-stated.
40	V_{CC}	5V Supply	Power Supply Input

ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	0°C to +70°C
Storage Temperature (Ceramic Package)	−65°C to +150°C
(Plastic Package)	−40°C to +125°C
All Output Voltages	−0.3 to +7 Volts
All Input Voltages	−0.3 to +7 Volts
Supply Voltage V_{CC}	−0.3 to +7 Volts
Power Dissipation	1.5W

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

DC CHARACTERISTICS

T_a = 0°C to +70°C, V_{CC} = +5V ± 5%, V_{SS} = GND, unless otherwise specified

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input Low Voltage	V_{IL}	V_{SS} − 0.5		V_{SS} + 0.8	V	
Input High Voltage	V_{IH}	2.0		V_{CC} + 0.5	V	
Output Low Voltage	V_{OL}			0.45	V	I_{OL} = 2 mA on all outputs
Output High Voltage	V_{OH}	2.4			V	I_{OH} = −400 μs ①
Power Supply Current (V_{CC})	I_{CC} (AV)			170	mA	t_{CY} min
Input Leakage	I_{IL}			±10 ①	μA	$V_{IN} = V_{CC}$
Output Leakage	I_{LO}			±10 ①	μA	$0.45V \leq V_{OUT} \leq V_{CC}$
Input Low Level, Reset	V_{ILR}	−0.5		+0.8	V	
Input High Level, Reset	V_{IHR}	2.4		V_{CC} + 0.5	V	
Hysteresis, Reset	V_{HY}	0.25			V	

Note: ① Minus (−) designates current flow out of the device.

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AC CHARACTERISTICS

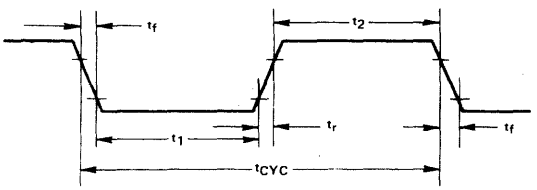
T_a = 0°C to +70°C; V_{CC} = 5V ± 5%; V_{SS} = 0V

PARAMETER	SYMBOL	LIMITS MIN	TYP	MAX	UNIT	TEST CONDITIONS
CLK Cycle Period	T_{CYC}	320		2000	ns	
CLK Low Time	t_1	80			ns	
CLK High Time	t_2	120			ns	
CLK Rise and Fall Time	t_r, t_f			30	ns	T_{CYC} = 320 ns
Address Valid Before Trailing Edge of ALE	t_{AL}	110			ns	C_L = 150 pF
Address Hold Time After ALE	t_{LA}	100			ns	
ALE Width	t_{LL}	140			ns	
ALE Low During CLK High	t_{LCK}	100			ns	Output Voltages:
Trailing Edge of ALE to Leading Edge of Control	t_{LC}	130			ns	V_L = 0.8 Volts
Address Float After Leading Edge of $\overline{READ}$ ($\overline{INTA}$)	t_{AFR}			0	ns	V_H = 2.0 Volts
Valid Address to Valid Data In	t_{AD}			575	ns	Input Voltages:
$\overline{READ}$ (or $\overline{INTA}$) to Valid Data	t_{RD}			300	ns	V_L = 0.8 Volts
Data Hold Time After $\overline{READ}$ ($\overline{INTA}$)	t_{RDH}	0			ns	V_H = 1.5 Volts at 20 ns rise and fall times
Trailing Edge of $\overline{READ}$ to Re-Enabling of Address	t_{RAE}	150			ns	
Address (A_8-A_{15}) Valid After Control ①	t_{CA}	120			ns	For outputs where C_L ≠ 150 pf, correct as follows:
Data Valid to Trailing Edge of $\overline{WRITE}$	t_{DW}	420			ns	
Data Valid After Trailing Edge of $\overline{WRITE}$	t_{WD}	100			ns	25 pf ≤ CL < 150 pf -0.10 ns/pf
Width of Control Low ($\overline{RD}$, $\overline{WR}$, $\overline{INTA}$)	t_{CC}	400			ns	
Trailing Edge of Control to Leading Edge of ALE	t_{CL}	50			ns	
READY Valid from Address Valid	t_{ARY}			220	ns	150 pf < CL ≤ 300 pf + 0.30 ns/pf
READY Setup Time to Leading Edge of CLK	t_{RYS}	110			ns	
READY Hold Time	t_{RYH}	0			ns	
HLDA Valid to Trailing Edge of CLK	t_{HACK}	110			ns	Outputs measured with only capacitive load
Bus Float After HLDA	t_{HABF}			210	ns	
HLDA to Bus Enable	t_{HABE}			210	ns	
ALE to Valid Data In	t_{LDR}			460	ns	
Control Trailing Edge to Leading Edge of Next Control	t_{RV}	400			ns	
Address Valid to Leading Edge of Control	t_{AC}	270			ns	
HOLD Setup Time to Trailing Edge of CLK	t_{HDS}	170			ns	
HOLD Hold Time	t_{HDH}	0			ns	
INTR Setup Time to Leading Edge of CLK (M1, T1 only). Also RST and TRAP	t_{INS}	160			ns	
INTR Hold Time	t_{INH}	0			ns	

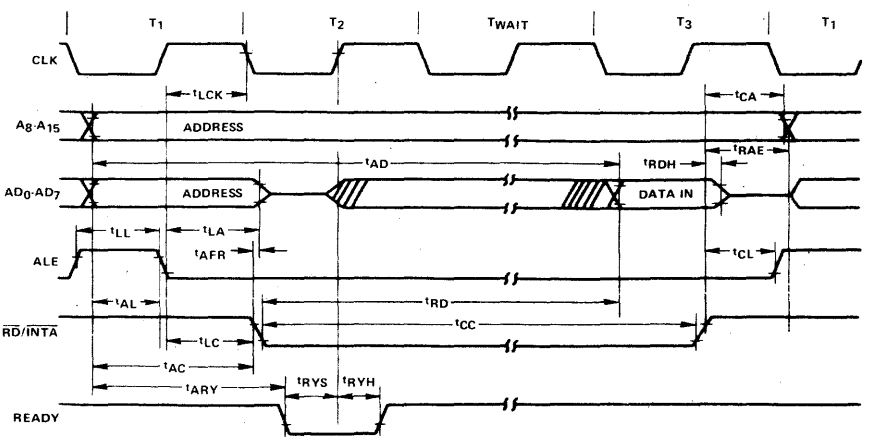
Note: ① IO/$\overline{M}$, SO, SI

TIMING WAVEFORMS

CLOCK TIMING



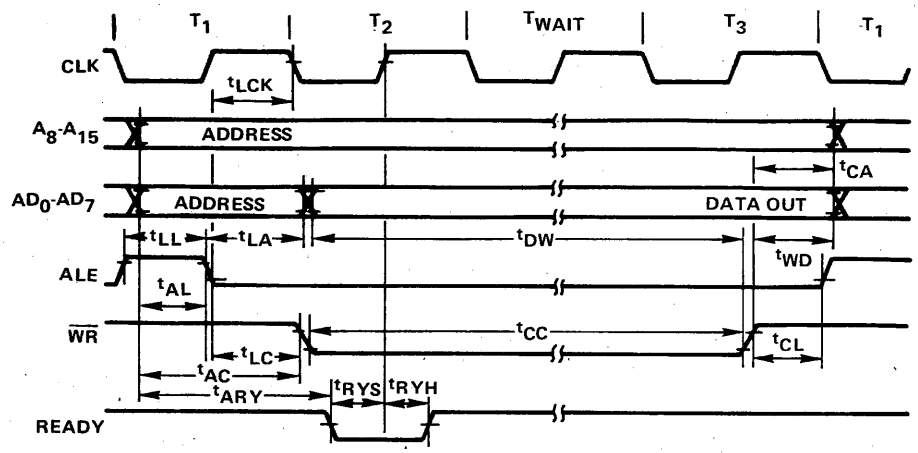
READ OPERATION



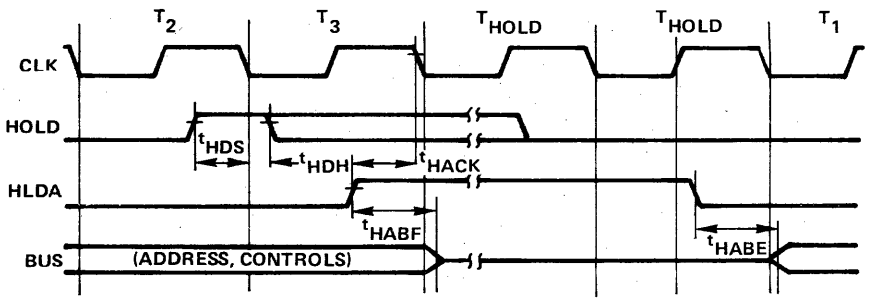
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TIMING WAVEFORMS (CONT.)

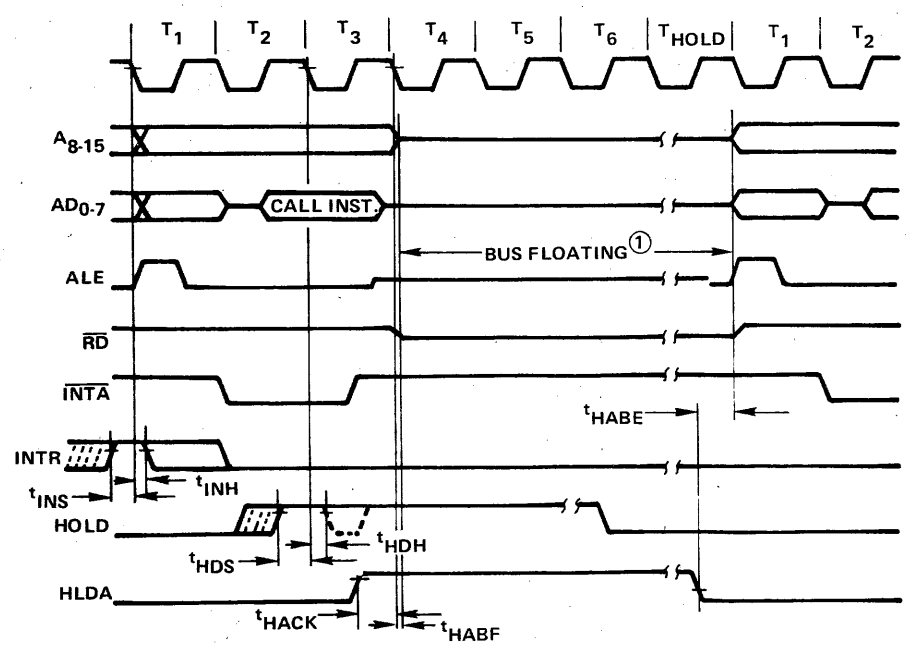
WRITE OPERATION



HOLD OPERATION



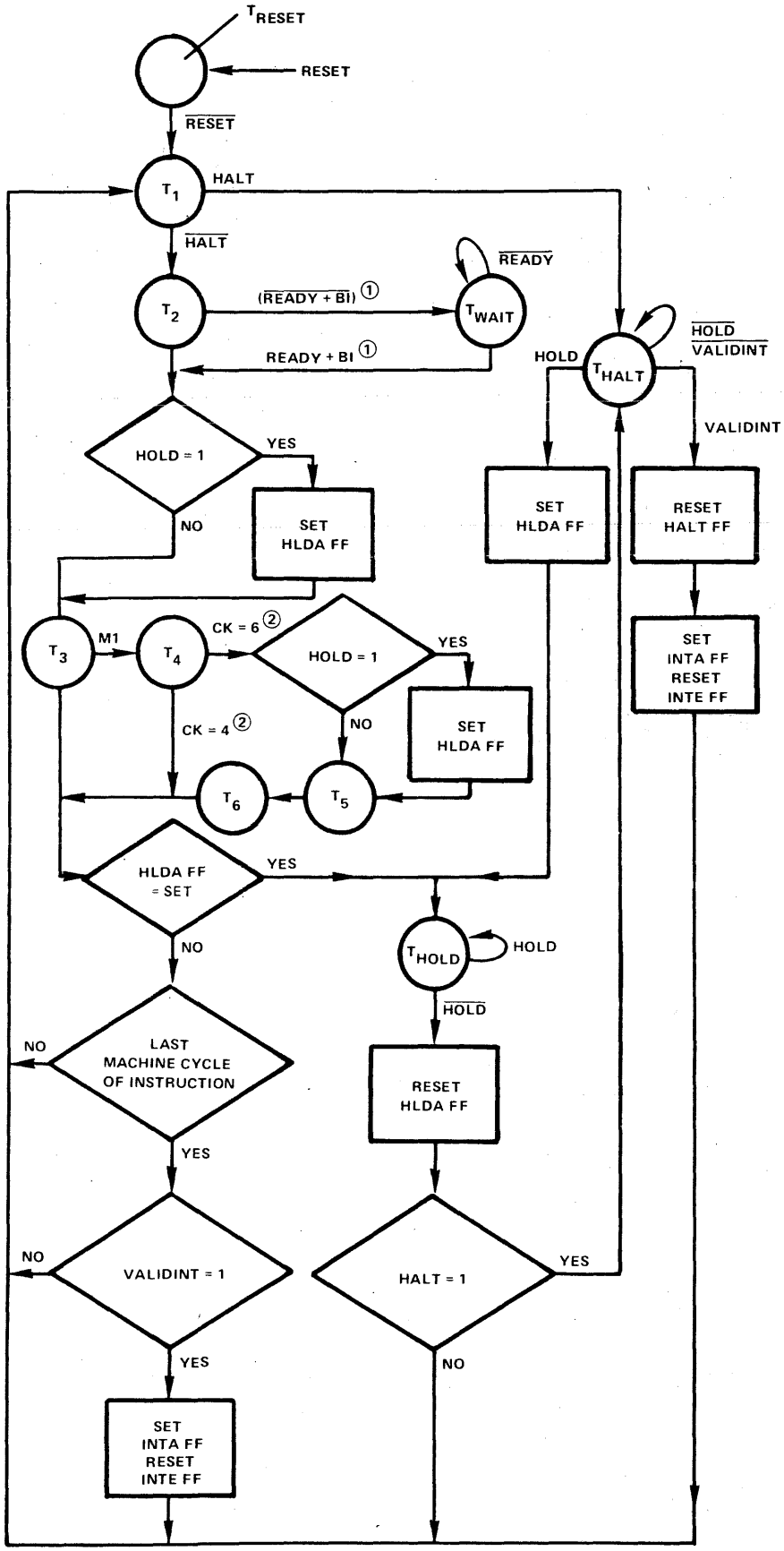
INTERRUPT TIMING



Note: ① IO/$\overline{M}$ is also floating during this time.

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PROCESSOR STATE TRANSITION DIAGRAM



Notes: ① BI indicates that the bus is idle during this machine cycle.

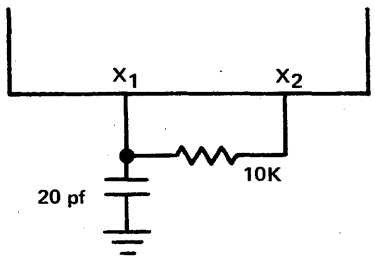
② CK indicates the number of clock cycles in this machine cycle.

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CLOCK INPUTS ①

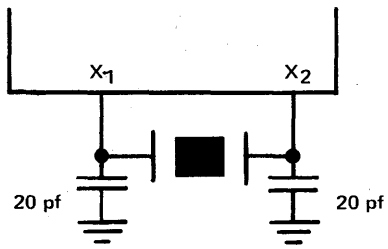
As stated, the timing for the μPD8085A may be generated in one of three ways; crystal, RC, or external clock. Recommendations for these methods are shown below.

RC



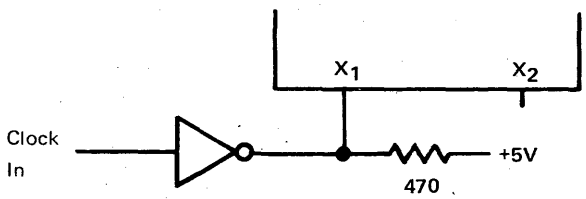
≈3 MHz Input Frequency
RC Resonance

CRYSTAL

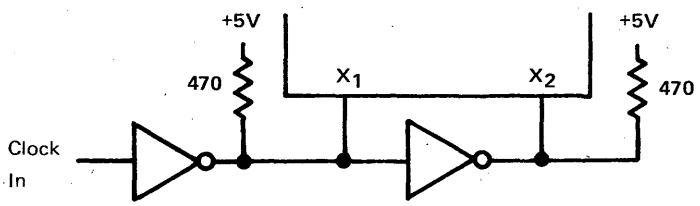


1-6 MHz Input Frequency
Parallel Resonant Crystal

EXTERNAL



1-6 MHz 25-50% DC
X_2 not used



1-6 MHz > 50% DC

Note: ① Input frequency must be twice the internal operating frequency.

STATUS OUTPUTS

The Status Outputs are valid during ALE time and have the following meaning:

	S1	S0
Halt	0	0
Write	0	1
Read	1	0
Fetch	1	1

These pins may be decoded to portray the processor's data bus status.

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INTERRUPTS

The μPD8085A has five interrupt pins available to the user. INTR is operationally the same as the 8080 interrupt request, three (3) internally maskable restart interrupts: RESTART 5.5, 6.5 and 7.5, and TRAP, a nonmaskable restart.

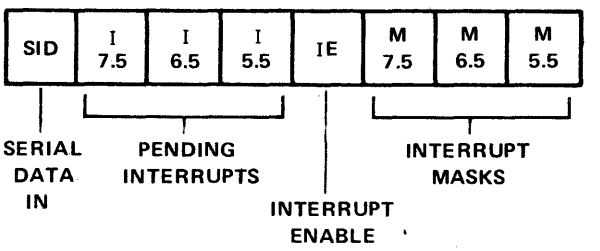
PRIORITY	INTERRUPT	RESTART ADDRESS
Highest	TRAP	24_{16}
|	RST 5.5	$2C_{16}$
|	RST 6.5	34_{16}
|	RST 7.5	$3C_{16}$
Lowest	INTR	

INTR, RST 5.5 and RST 6.5 are all level sensing inputs while RST 7.5 is set on a rising edge. TRAP, the highest priority interrupt, is nonmaskable and is set on the rising edge or positive level. It must make a low to high transition and remain high to be seen, but it will not be generated again until it makes another low to high transition.

SERIAL I/O

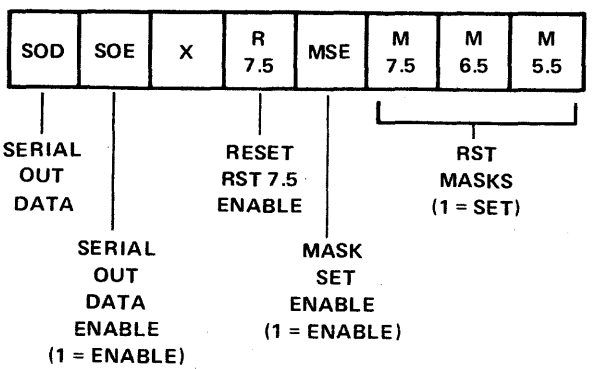
Serial input and output is accomplished with two new instructions not included in the 8080: RIM and SIM. These instructions serve several purposes: serial I/O, and reading or setting the interrupt mask.

The RIM (Read Interrupt Mask) instruction is used for reading the interrupt mask and for reading serial data. After execution of the RIM instruction the ACC content is as follows:



Note: After the TRAP interrupt, the RIM instruction must be executed to preserve the status of IE.

The SIM (Set Interrupt Mask) instruction is used to program the interrupt mask and to output serial data. Presetting the ACC for the SIM instruction has the following meaning:



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INSTRUCTION SET

The instruction set includes arithmetic and logical operators with direct, register, indirect, and immediate addressing modes.

Move, load, and store instruction groups provide the ability to move either 8 or 16 bits of data between memory, the six working registers and the accumulator using direct, register, indirect, and immediate addressing modes.

The ability to branch to different portions of the program is provided with direct, conditional, or computed jumps. Also, the ability to call and return from subroutines is provided both conditionally and unconditionally. The RESTART (or single byte call instruction) is useful for interrupt vector operation.

Conditional jumps, calls and returns execute based on the state of the four testable flags (Sign, Zero, Parity and Carry). The state of each flag is determined by the result of the last instruction executed that affected flags. (See Instruction Set Table.)

The Sign flag is set (High) if bit 7 of the result is a "1"; otherwise it is reset (Low). The Zero flag is set if the result is "0"; otherwise it is reset. The Parity flag is set if the modulo 2 sum of the bits of the result is "0" (Even Parity); otherwise (Odd Parity) it is reset. The Carry flag is set if the last instruction resulted in a carry or a borrow out of the most significant bit (bit 7) of the result; otherwise it is reset.

In addition to the four testable flags, the μPD8085A has another flag (ACY) that is not directly testable. It is used for multiple precision arithmetic operations with the DAA instruction. The Auxiliary Carry flag is set if the last instruction resulted in a carry or a borrow from bit 3 into bit 4; otherwise it is reset.

Double precision operators such as stack manipulation and double add instructions extend both the arithmetic and interrupt handling capability of the μPD8085A. The ability to increment and decrement memory, the six general registers and the accumulator are provided as well as extended increment and decrement instructions to operate on the register pairs and stack pointer. Further capability is provided by the ability to rotate the accumulator left or right through or around the carry bit.

Input and output may be accomplished using memory addresses as I/O ports or the directly addressed I/O provided for in the μPD8085A instruction set.

Two instructions, RIM and SIM, are used for reading and setting the internal interrupt mask as well as input and output to the serial I/O port.

The special instruction group completes the μPD8085A instruction set: NOP, HALT stop processor execution; DAA provides decimal arithmetic capability; STC sets the carry flag; CMC complements it; CMA complements the contents of the accumulator; and XCHG exchanges the contents of two 16-bit register pairs directly.

DATA AND INSTRUCTION FORMATS

Data in the μPD8085A is stored as 8-bit binary integers. All data/instruction transfers to the system data bus are in the following format:

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0

MSB DATA WORD LSB

Instructions are one, two, or three bytes long. Multiple byte instructions must be stored in successive locations of program memory. The address of the first byte is used as the address of the instruction.

									TYPICAL INSTRUCTIONS
One Byte Instructions									
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	OP CODE	Register to register, memory reference, arithmetic or logical, rotate, return, push, pop, enable, or disable interrupt instructions
Two Byte Instructions									
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	OP CODE	Immediate mode or I/O instructions
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	OPERAND	
Three Byte Instructions									
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	OP CODE	Jump, call or direct load and store instructions
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	LOW ADDRESS OR OPERAND 1	
D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	HIGH ADDRESS OR OPERAND 2	

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INSTRUCTION SET TABLE

MNEMONIC[1]	DESCRIPTION	INSTRUCTION CODE[2] D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Clock Cycles[3]	FLAGS[4] SIGN	ZERO	PARITY	CARRY
MOVE														
MOV d,s	Move register to register	0	1	d	d	d	s	s	s	4				
MOV M,s	Move register to memory	0	1	1	1	0	s	s	s	7				
MOV d,M	Move memory to register	0	1	d	d	d	1	1	0	7				
MVI d,D8	Move immediate to register	0	0	d	d	d	1	1	0	7				
MVI M,D8	Move immediate to memory	0	0	1	1	0	1	1	0	10				
INCREMENT/DECREMENT														
INR d	Increment register	0	0	d	d	d	1	0	0	4	•	•	•	
DCR d	Decrement register	0	0	d	d	d	1	0	1	4	•	•	•	
INR M	Increment memory	0	0	1	1	0	1	0	0	10	•	•	•	
DCR M	Decrement memory	0	0	1	1	0	1	0	1	10	•	•	•	
ALU – REGISTER TO ACCUMULATOR														
ADD s	Add register to A	1	0	0	0	0	s	s	s	4	•	•	•	•
ADC s	Add register to A with carry	1	0	0	0	1	s	s	s	4	•	•	•	•
SUB s	Subtract register from A	1	0	0	1	0	s	s	s	4	•	•	•	•
SBB s	Subtract register from A with borrow	1	0	0	1	1	s	s	s	4	•	•	•	•
ANA s	AND register with A	1	0	1	0	0	s	s	s	4	•	•	•	0
XRA s	Exclusive OR Register with A	1	0	1	0	1	s	s	s	4	•	•	•	0
ORA s	OR register with A	1	0	1	1	0	s	s	s	4	•	•	•	0
CMP s	Compare register with A	1	0	1	1	1	s	s	s	4	•	•	•	•
ALU – MEMORY TO ACCUMULATOR														
ADD M	Add memory to A	1	0	0	0	0	1	1	0	7	•	•	•	•
ADC M	Add memory to A with carry	1	0	0	0	1	1	1	0	7	•	•	•	•
SUB M	Subtract memory from A	1	0	0	1	0	1	1	0	7	•	•	•	•
SBB M	Subtract memory from A with borrow	1	0	0	1	1	1	1	0	7	•	•	•	•
ANA M	AND memory with A	1	0	1	0	0	1	1	0	7	•	•	•	0
XRA M	Exclusive OR memory with A	1	0	1	0	1	1	1	0	7	•	•	•	0
ORA M	OR memory with A	1	0	1	1	0	1	1	0	7	•	•	•	0
CMP M	Compare memory with A	1	0	1	1	1	1	1	0	7	•	•	•	•
ALU – IMMEDIATE TO ACCUMULATOR														
ADI D8	Add immediate to A	1	1	0	0	0	1	1	0	7	•	•	•	•
ACI D8	Add immediate to A with carry	1	1	0	0	1	1	1	0	7	•	•	•	•
SUI D8	Subtract immediate from A	1	1	0	1	0	1	1	0	7	•	•	•	•
SBI D8	Subtract immediate from A with borrow	1	1	0	1	1	1	1	0	7	•	•	•	•
ANI D8	AND immediate with A	1	1	1	0	0	1	1	0	7	•	•	•	0
XRI D8	Exclusive OR immediate with A	1	1	1	0	1	1	1	0	7	•	•	•	0
ORI D8	OR immediate with A	1	1	1	1	0	1	1	0	7	•	•	•	0
CPI D8	Compare immediate with A	1	1	1	1	1	1	1	0	7	•	•	•	•
ALU – ROTATE														
RLC	Rotate A left, MSB to carry (8-bit)	0	0	0	0	0	1	1	1	4				•
RRC	Rotate A right, LSB to carry (8-bit)	0	0	0	0	1	1	1	1	4				•
RAL	Rotate A left through carry (9-bit)	0	0	0	1	0	1	1	1	4				•
RAR	Rotate A right through carry (9-bit)	0	0	0	1	1	1	1	1	4				•
JUMP														
JMP ADDR	Jump unconditional	1	1	0	0	0	0	1	1	10				
JNZ ADDR	Jump on not zero	1	1	0	0	0	0	1	0	7/10				
JZ ADDR	Jump on zero	1	1	0	0	1	0	1	0	7/10				
JNC ADDR	Jump on no carry	1	1	0	1	0	0	1	0	7/10				
JC ADDR	Jump on carry	1	1	0	1	1	0	1	0	7/10				
JPO ADDR	Jump on parity odd	1	1	1	0	0	0	1	0	7/10				
JPE ADDR	Jump on parity even	1	1	1	0	1	0	1	0	7/10				
JP ADDR	Jump on positive	1	1	1	1	0	0	1	0	7/10				
JM ADDR	Jump on minus	1	1	1	1	1	0	1	0	7/10				
CALL														
CALL ADDR	Call unconditional	1	1	0	0	1	1	0	1	18				
CNZ ADDR	Call on not zero	1	1	0	0	0	1	0	0	9/18				
CZ ADDR	Call on zero	1	1	0	0	1	1	0	0	9/18				
CNC ADDR	Call on no carry	1	1	0	1	0	1	0	0	9/18				
CC ADDR	Call on carry	1	1	0	1	1	1	0	0	9/18				
CPO ADDR	Call on parity odd	1	1	1	0	0	1	0	0	9/18				
CPE ADDR	Call on parity even	1	1	1	0	1	1	0	0	9/18				
CP ADDR	Call on positive	1	1	1	1	0	1	0	0	9/18				
CM ADDR	Call on minus	1	1	1	1	1	1	0	0	9/18				
RETURN														
RET	Return	1	1	0	0	1	0	0	1	10				
RNZ	Return on not zero	1	1	0	0	0	0	0	0	6/12				
RZ	Return on zero	1	1	0	0	1	0	0	0	6/12				
RNC	Return on no carry	1	1	0	1	0	0	0	0	6/12				
RC	Return on carry	1	1	0	1	1	0	0	0	6/12				
RPO	Return on parity odd	1	1	1	0	0	0	0	0	6/12				
RPE	Return on parity even	1	1	1	0	1	0	0	0	6/12				
RP	Return on positive	1	1	1	1	0	0	0	0	6/12				
RM	Return on minus	1	1	1	1	1	0	0	0	6/12				

MNEMONIC[1]	DESCRIPTION	INSTRUCTION CODE[2] D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Clock Cycles[3]	FLAGS[4] SIGN	ZERO	PARITY	CARRY
LOAD REGISTER PAIR														
LXI B,D16	Load immediate register pair BC	0	0	0	0	0	0	0	1	10				
LXI D,D16	Load immediate register pair DE	0	0	0	1	0	0	0	1	10				
LXI H,D16	Load immediate register pair HL	0	0	1	0	0	0	0	1	10				
LXI SP,D16	Load immediate Stack Pointer	0	0	1	1	0	0	0	1	10				
PUSH														
PUSH B	Push register pair BC on stack	1	1	0	0	0	1	0	1	12				
PUSH D	Push register pair DE on stack	1	1	0	1	0	1	0	1	12				
PUSH H	Push register pair HL on stack	1	1	1	0	0	1	0	1	12				
PUSH PSW	Push A and flags on stack	1	1	1	1	0	1	0	1	12				
POP														
POP B	Pop register pair BC off stack	1	1	0	0	0	0	0	1	10				
POP D	Pop register pair DE off stack	1	1	0	1	0	0	0	1	10				
POP H	Pop register pair HL off stack	1	1	1	0	0	0	0	1	10				
POP PSW	Pop A and flags off stack	1	1	1	1	0	0	0	1	10	•	•	•	•
DOUBLE ADD														
DAD B	Add BC to HL	0	0	0	0	1	0	0	1	10				•
DAD D	Add DE to HL	0	0	0	1	1	0	0	1	10				•
DAD H	Add HL to HL	0	0	1	0	1	0	0	1	10				•
DAD SP	Add Stack Pointer to HL	0	0	1	1	1	0	0	1	10				•
INCREMENT REGISTER PAIR														
INX B	Increment BC	0	0	0	0	0	0	1	1	6				
INX D	Increment DE	0	0	0	1	0	0	1	1	6				
INX H	Increment HL	0	0	1	0	0	0	1	1	6				
INX SP	Increment Stack Pointer	0	0	1	1	0	0	1	1	6				
DECREMENT REGISTER PAIR														
DCX B	Decrement BC	0	0	0	0	1	0	1	1	6				
DCX D	Decrement DE	0	0	0	1	1	0	1	1	6				
DCX H	Decrement HL	0	0	1	0	1	0	1	1	6				
DCX SP	Decrement Stack Pointer	0	0	1	1	1	0	1	1	6				
REGISTER INDIRECT														
STAX B	Store A at ADDR in BC	0	0	0	0	0	0	1	0	7				
STAX D	Store A at ADDR in DE	0	0	0	1	0	0	1	0	7				
LDAX B	Load A at ADDR in BC	0	0	0	0	1	0	1	0	7				
LDAX D	Load A at ADDR in DE	0	0	0	1	1	0	1	0	7				
DIRECT														
STA ADDR	Store A direct	0	0	1	1	0	0	1	0	13				
LDA ADDR	Load A direct	0	0	1	1	1	0	1	0	13				
SHLD ADDR	Store HL direct	0	0	1	0	0	0	1	0	16				
LHLD ADDR	Load HL direct	0	0	1	0	1	0	1	0	16				
MOVE REGISTER PAIR														
XCHG	Exchange DE and HL register pairs	1	1	1	0	1	0	1	1	4				
XTHL	Exchange top of stack and HL	1	1	1	0	0	0	1	1	16				
SPHL	HL to Stack Pointer	1	1	1	1	1	0	0	1	6				
PCHL	HL to Program Counter	1	1	1	0	1	0	0	1	6				
INPUT/OUTPUT														
IN A	Input	1	1	0	1	1	0	1	1	10				
OUT A	Output	1	1	0	1	0	0	1	1	10				
EI	Enable interrupts	1	1	1	1	1	0	1	1	4				
DI	Disable interrupts	1	1	1	1	0	0	1	1	4				
RIM	Read Interrupt Mask	0	0	1	0	0	0	0	0	4				
SIM	Set Interrupt Mask	0	0	1	1	0	0	0	0	4				
RST A	Restart	1	1	A	A	A	1	1	1	12				
MISCELLANEOUS														
CMA	Complement A	0	0	1	0	1	1	1	1	4				
STC	Set carry	0	0	1	1	0	1	1	1	4				1
CMC	Complement carry	0	0	1	1	1	1	1	1	4				Cy
DAA	Decimal adjust A	0	0	1	0	0	1	1	1	4	•	•	•	•
NOP	No operation	0	0	0	0	0	0	0	0	4				
HLT	Halt	0	1	1	1	0	1	1	0	5				

Notes:

[1] Operand Symbols used
- A = 8-bit address or expression
- s = source register
- d = destination register
- PSW = Processor Status Word
- SP = Stack Pointer
- D8 = 8-bit data quantity, expression, or constant, always B_2 of instruction
- D16 = 16-bit data quantity, expression, or constant, always B_3B_2 of instruction
- ADDR = 16-bit Memory address expression

[2] ddd or sss – 000 B – 001 C – 010 D – 011 E – 100 H – 101 L – 110 Memory – 111 A.

[3] Two possible cycle times (7/10) indicate instruction cycles dependent on condition flags.

[4] • = flag affected
- flag not affected
0 = flag reset
1 = flag set

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INSTRUCTION CYCLE TIMES

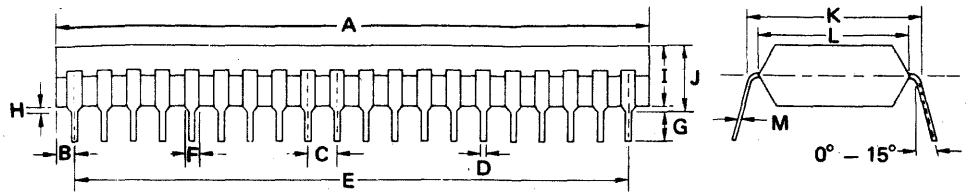
One to five machine cycles ($M_1 - M_5$) are required to execute an instruction. Each machine cycle involves the transfer of an instruction or data byte into the processor or a transfer of a data byte out of the processor (the sole exception being the double add instruction). The first one, two or three machine cycles obtain the instruction from the memory or an interrupting I/O controller. The remaining cycles are used to execute the instruction. Each machine cycle requires from three to five clock times ($T_1 - T_5$).

Machine cycles and clock states used for each type of instruction are shown below.

INSTRUCTION TYPE	MACHINE CYCLES EXECUTED MIN/MAX	CLOCK STATUS MIN/MAX
ALU R	1	4
CMC	1	4
CMA	1	4
DAA	1	4
DCR R	1	4
DI	1	4
EI	1	4
INR R	1	4
MOV R, R	1	4
NOP	1	4
ROTATE	1	4
RIM	1	4
SIM	1	4
STC	1	4
XCHG	1	4
HLT	1	5
DCX	1	6
INX	1	6
PCHL	1	6
RET COND.	1/3	6/12
SPHL	1	6
ALU I	2	7
ALU M	2	7
JNC	2/3	7/10
LDAX	2	7
MVI	2	7
MOV M, R	2	7
MOV R, M	2	7
STAX	2	7
CALL COND.	2/5	9/18
DAD	3	10
DCR M	3	10
IN	3	10
INR M	3	10
JMP	3	10
LOAD PAIR	3	10
MVI M	3	10
OUT	3	10
POP	3	10
RET	3	10
PUSH	3	12
RST	3	12
LDA	4	13
STA	4	13
LHLD	5	16
SHLD	5	16
XTHL	5	16
CALL	5	18

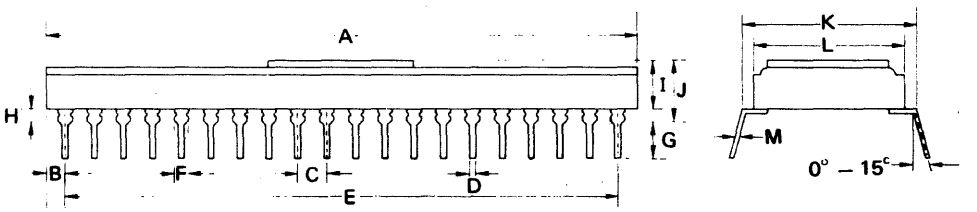
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PACKAGE OUTLINE
μPD8085AC/D



Plastic

ITEM	MILLIMETERS	INCHES
A	51.5 MAX	2.028 MAX
B	1.62	0.064
C	2.54 ± 0.1	0.10 ± 0.004
D	0.5 ± 0.1	0.019 ± 0.004
E	48.26	1.9
F	1.2 MIN	0.047 MIN
G	2.54 MIN	0.10 MIN
H	0.5 MIN	0.019 MIN
I	5.22 MAX	0.206 MAX
J	5.72 MAX	0.225 MAX
K	15.24	0.600
L	13.2	0.520
M	$0.25^{+0.1}_{-0.05}$	$0.010^{+0.004}_{-0.002}$



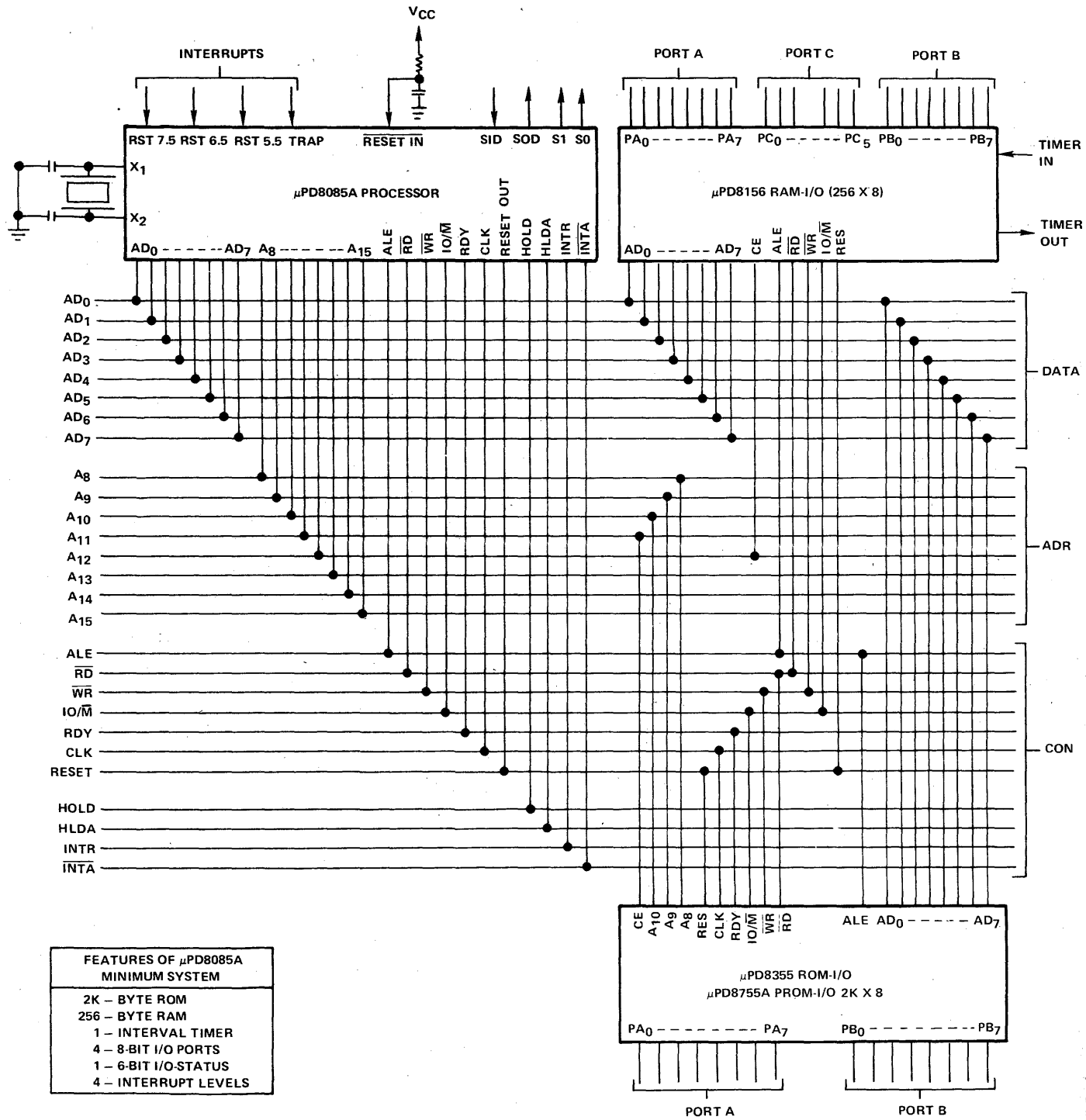
Ceramic

ITEM	MILLIMETERS	INCHES
A	51.5 MAX	2.028 MAX
B	1.62	0.064
C	2.54 ± 0.1	0.100 ± 0.004
D	0.50 ± 0.1	0.0197 ± 0.004
E	48.26 ± 0.2	1.900 ± 0.008
F	1.27	0.050
G	3.2 MIN	0.126 MIN
H	1.0 MIN	0.04 MIN
I	4.2 MAX	0.17 MAX
J	5.2 MAX	0.205 MAX
K	15.24 ± 0.1	0.6 ± 0.004
L	$13.5^{+0.2}_{-0.25}$	$0.531^{+0.008}_{-0.010}$
M	0.30 ± 0.1	0.012 ± 0.004

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μPD8085A FAMILY MINIMUM SYSTEM CONFIGURATION

A minimum computer system consisting of a processor, ROM, RAM, and I/O can be built with only 3-40 pin packs. This system is shown below with its address, data, control busses and I/O ports.



FEATURES OF μPD8085A MINIMUM SYSTEM
2K – BYTE ROM
256 – BYTE RAM
1 – INTERVAL TIMER
4 – 8-BIT I/O PORTS
1 – 6-BIT I/O-STATUS
4 – INTERRUPT LEVELS

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SINGLE/DOUBLE DENSITY FLOPPY DISK CONTROLLER

DESCRIPTION

The μPD765 is a LSI Floppy Disk Controller (FDC) Chip, which contains the circuitry and control functions for interfacing a processor to 4 Floppy Disk Drives. It is capable of supporting either IBM 3740 single density format (FM), or IBM System 34 Double Density format (MFM) including double sided recording. The μPD765 provides control signals which simplify the design of an external phase locked loop, and write precompensation circuitry. The FDC simplifies and handles most of the burdens associated with implementing a Floppy Disk Interface.

Hand-shaking signals are provided in the μPD765 which make DMA operation easy to incorporate with the aid of an external DMA Controller chip, such as the μPD8257. The FDC will operate in either DMA or Non-DMA mode. In the Non-DMA mode, the FDC generates interrupts to the processor every time a data byte is available. In the DMA mode, the processor need only load the command into the FDC and all data transfers occur under control of the μPD765 and DMA controller.

There are 15 separate commands which the μPD765 will execute. Each of these commands require multiple 8-bit bytes to fully specify the operation which the processor wishes the FDC to perform. The following commands are available:

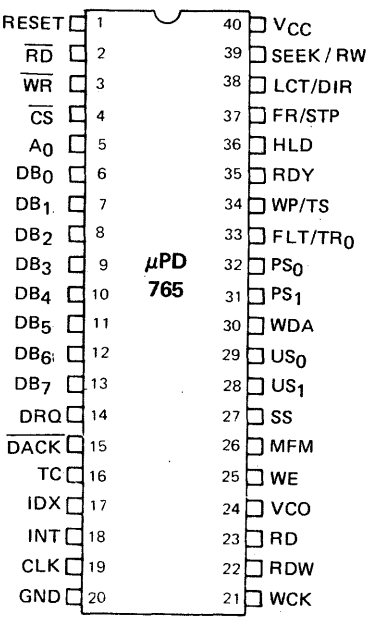
Read Data	Scan High or Equal	Write Deleted Data
Read ID	Scan Low or Equal	Seek
Read Deleted Data	Specify	Recalibrate (Restore to Track 0)
Read a Track	Write Data	Sense Interrupt Status
Scan Equal	Format a Track	Sense Drive Status

FEATURES

Address mark detection circuitry is internal to the FDC which simplifies the phase locked loop and read electronics. The track stepping rate, head load time, and head unload time may be programmed by the user. The μPD765 offers many additional features such as multiple sector transfers in both read and write with a single command, and full IBM compatibility in both single and double density modes.

- IBM Compatible in Both Single and Double Density Recording Formats
- Programmable Data Record Lengths: 128, 256, 512, or 1024 Bytes/Sector
- Multi-Sector and Multi-Track Transfer Capability
- Drive Up to 4 Floppy Disks
- Data Scan Capability – Will Scan a Single Sector or an Entire Cylinder's Worth of Data Fields, Comparing on a Byte by Byte Basis, Data in the Processor's Memory with Data Read from the Diskette
- Data Transfers in DMA or Non-DMA Mode
- Parallel Seek Operations on Up to Four Drives
- Compatible with Most Microprocessors Including 8080A, 8085A, μPD780 (Z80™)
- Single Phase 8 MHz Clock
- Single +5 Volt Power Supply
- Available in 40 Pin Plastic Dual-in-Line Package

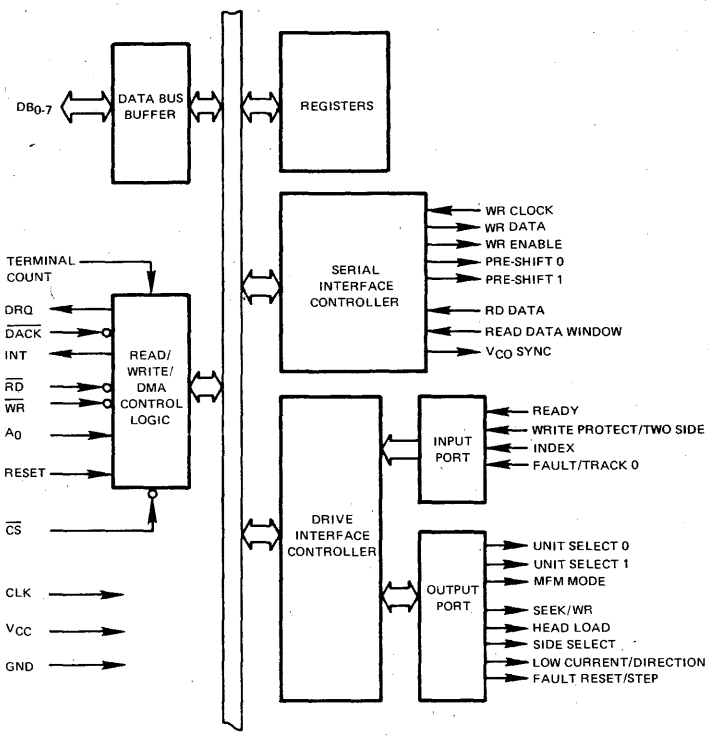
PIN CONFIGURATION



TM: Z80 is a registered trademark of Zilog

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BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	0°C to +70°C
Storage Temperature	-40°C to +125°C
All Output Voltages	-0.5 to +7 Volts
All Input Voltages	-0.5 to +7 Volts
Supply Voltage V_{CC}	-0.5 to +7 Volts
Power Dissipation	1 Watt

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

DC CHARACTERISTICS

T_a = 0°C to +70°C; V_{CC} = +5V ± 5% unless otherwise specified.

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP ①	LIMITS MAX	UNIT	TEST CONDITIONS
Input Low Voltage	V_{IL}	-0.5		0.8	V	
Input High Voltage	V_{IH}	2.5		V_{CC} + 0.5	V	
Output Low Voltage	V_{OL}			0.45	V	I_{OL} = 1.6 mA
Output High Voltage	V_{OH}	2.4		V_{CC}	V	I_{OH} = -150 μA for Data Bus I_{OH} = -80 μA for other outputs
Input Low Voltage (CLK + WR Clock)	$V_{IL(\Phi)}$	-0.5		0.8	V	
Input High Voltage (CLK + WR Clock)	$V_{IH(\Phi)}$	V_{CC} - 0.75		V_{CC} + 0.5	V	
V_{CC} Supply Current	I_{CC}		85	130	mA	
Input Load Current (All Input Pins)	I_{LI}			10	μA	V_{IN} = V_{CC}
				-10	μA	V_{IN} = 0V
High Level Output Leakage Current	I_{LOH}			10	μA	V_{OUT} = V_{CC}
Low Level Output Leakage Current	I_{LOL}			-10	μA	V_{OUT} = 0V

Note: ① Typical values for T_a = 25°C and nominal supply voltage.

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PIN IDENTIFICATION

PIN NO.	PIN SYMBOL	PIN NAME	INPUT/ OUTPUT	CONNECTION TO	FUNCTION
1	RST	Reset	Input	Processor	Places FDC in idle state. Resets output lines to FDD to "0" (low).
2	$\overline{RD}$	Read	Input①	Processor	Control signal for transfer of data from FDC to Data Bus, when "0" (low).
3	$\overline{WR}$	Write	Input①	Processor	Control signal for transfer of data to FDC via Data Bus, when "0" (low).
4	$\overline{CS}$	Chip Select	Input	Processor	IC selected when "0" (low), allowing $\overline{RD}$ and $\overline{WR}$ to be enabled.
5	A_0	Data/Status Reg Select	Input①	Processor	Selects Data Reg (A_0=1) or Status Reg (A_0=0) contents of the FDC to be sent to Data Bus.
6-13	DB_0-DB_7	Data Bus	Input/① Output	Processor	Bi-Directional 8-bit Data Bus.
14	DRQ	Data DMA Request	Output	DMA	DMA Request is being made by FDC when DRQ="1".
15	$\overline{DACK}$	DMA Acknowledge	Input	DMA	DMA cycle is active when "0" (low) and Controller is performing DMA transfer.
16	TC	Terminal Count	Input	DMA	Indicates the termination of a DMA transfer when "1" (high).
17	IDX	Index	Input	FDD	Indicates the beginning of a disk track.
18	INT	Interrupt	Output	Processor	Interrupt Request Generated by FDC.
19	CLK	Clock	Input		Single Phase 8 MHz Squarewave Clock.
20	GND	Ground			D.C. Power Return.
21	WCK	Write Clock	Input		Write data rate to FDD. FM = 500 kHz, MFM = 1 MHz, with a pulse width of 250 ns for both FM and MFM.
22	RDW	Read Data Window	Input	Phase Lock Loop	Generated by PLL, and used to sample data from FDD.
23	RDD	Read Data	Input	FDD	Read data from FDD, containing clock and data bits.
24	VCO	VCO Sync	Output	Phase Lock Loop	Inhibits VCO in PLL when "0" (low), enables VCO when "1".
25	WE	Write Enable	Output	FDD	Enables write data into FDD.
26	MFM	MFM Mode	Output	Phase Lock Loop	MFM mode when "1", FM mode when "0".
27	SS	Side Select	Output	FDD	Head 1 selected when "1" (high), Head 0 selected when "0" (low).
28, 29	US_1, US_0	Unit Select	Output	FDD	FDD Unit Selected.
30	WDA	Write Data	Output	FDD	Serial clock and data bits to FDD.
31, 32	PS_1, PS_0	Precompensation	Output	FDD	Write precompensation status during MFM mode. Determines early, late, and normal times.
33	FLT/TR_0	Fault/Track 0	Input	FDD	Senses FDD fault condition, in Read/ Write mode; and Track 0 condition in Seek mode.
34	WP/TS	Write Protect/ Two-Side	Input	FDD	Senses Write Protect status in Read/ Write mode; and Two Side Media in Seek mode.
35	RDY	Ready	Input	FDD	Indicates FDD is ready to send or receive data.
36	HLD	Head Load	Output	FDD	Command which causes read/write head in FDD to contact diskette.
37	FR/STP	Flt Reset/Step	Output	FDD	Resets fault F.F. in FDD in Read/Write mode, contains step pulses to move head to another cylinder in Seek mode.
38	LCT/DIR	Low Current/ Direction	Output	FDD	Lowers Write current on inner tracks in Read/Write mode, determines direction head will step in Seek mode.
39	SEEK/RW	SEEK/Read Write	Output	FDD	When "1" (high) Seek mode selected and when "0" (low) Read/Write mode selected.
40	V_{CC}	+5V			D.C. Power

Note: ① Disabled when $\overline{CS}$ = 1.

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AC CHARACTERISTICS

T_a = −10°C to +70°C; V_{CC} = +5V ± 5% unless otherwise specified.

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP 1	LIMITS MAX	UNIT	TEST CONDITIONS
Clock Period	ΦCY	1.0	8.0	9.0	MHz	
Clock Active (High)	Φ_0	35			ns	
Clock Rise Time	Φ_r			20	ns	
Clock Fall Time	Φ_f			20	ns	
A_0, $\overline{CS}$, $\overline{DACK}$ Set Up Time to $\overline{RD}$ ↓	T_{AR}	30			ns	
A_0, $\overline{CS}$, $\overline{DACK}$ Hold Time from $\overline{RD}$ ↑	T_{RA}	5.0			ns	
$\overline{RD}$ Width	T_{RR}	300			ns	
Data Access Time from $\overline{RD}$ ↓	T_{RD}			200	ns	
DB to Float Delay Time from $\overline{RD}$ ↑	T_{DF}	20		100	ns	
A_0, $\overline{CS}$, $\overline{DACK}$ Set Up Time to $\overline{WR}$ ↓	T_{AW}	50			ns	
A_0, $\overline{CS}$, $\overline{DACK}$ Hold Time to $\overline{WR}$ ↑	T_{WA}	30			ns	
$\overline{WR}$ Width	T_{WW}	300			ns	
Data Set Up Time to $\overline{WR}$ ↑	T_{DW}	250			ns	
Data Hold Time from $\overline{WR}$ ↑	T_{WD}	30			ns	
INT Delay Time from $\overline{RD}$ ↑	T_{RI}			500	ns	
INT Delay Time from $\overline{WR}$ ↑	T_{WI}			500	ns	
DRQ Cycle Time	T_{MCY}	13			μs	
DRQ Delay Time from $\overline{DACK}$ ↑	T_{AM}			1.0	μs	
$\overline{WR}$ or $\overline{RD}$ Response Time from DRQ ↑	T_{RWM}	1.0			μs	
TC Width	T_{TC}	300			ns	
Rest Width	T_{RST}	3.0			μs	
WCK Cycle Time	T_{CY}		2 or 4 1 or 2		μs	MFM = 0 MFM = 1
WCK Active Time (High)	T_0	150	250	350	ns	
WCK Rise Time	T_r			30	ns	
WCK Fall Time	T_f			30	ns	
Pre-Shift Delay Time from WCK ↑	T_{CP}	20		150	ns	
WDA Delay Time from WCK ↑	T_{CD}	20		150	ns	
RDD Active Time (High)	T_{RDD}	100			ns	
Window Cycle Time	T_{WCY}		2.0 1.0		μs	MFM = 0 MFM = 1
Window Hold Time to/from RDD	T_{RDW} T_{WRD}	100			ns	
$US_{0,1}$ Hold Time to SEEK/RW ↑	T_{US}	12			μs	8 MHz Clock Period
SEEK/RW Hold Time to LOW CURRENT/DIRECTION ↑	T_{SD}	7			μs	
LOW CURRENT/DIRECTION Hold Time to FAULT RESET/STEP ↑	T_{DST}	1.0			μs	
$US_{0,1}$ Hold Time from FAULT RESET/STEP ↑	T_{STU}	1.0			μs	
STEP Active Time (High)	T_{STP}		5.0		μs	
LOW CURRENT/DIRECTION Hold Time from FAULT RESET/STEP ↓	T_{STD}	5.0			μs	
STEP Cycle Time	T_{SC}	③		③	ms	
FAULT RESET Active Time (High)	T_{FR}	8.0		10	μs	8 MHz Clock Period

Notes: ① Typical values for T_a = 25°C and nominal supply voltage.
② The former value of 2 and 1 are applied to Standard Floppy, and the latter value of 4 and 2 are applied to Mini-floppy.
③ Under Software Control. The range is from 1 ms to 16 ms at 8 MHz Clock Period, and 2 to 32 ms at 4 MHz Clock Period.

CAPACITANCE

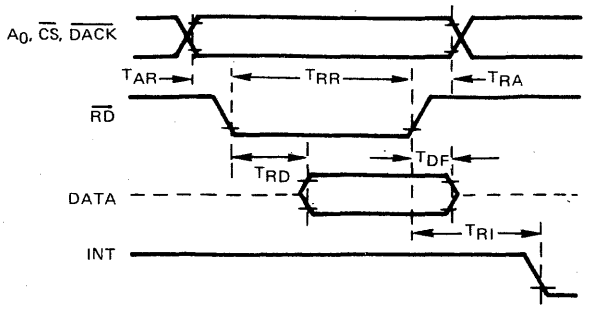
T_a = 25°C; f = 1 MHz

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Clock Input Capacitance	$C_{IN(\Phi)}$			35	pF	All Pins Except Pin Under Test Tied to AC Ground
Input Capacitance	C_{IN}			10	pF	
Output Capacitance	C_{OUT}			20	pF	

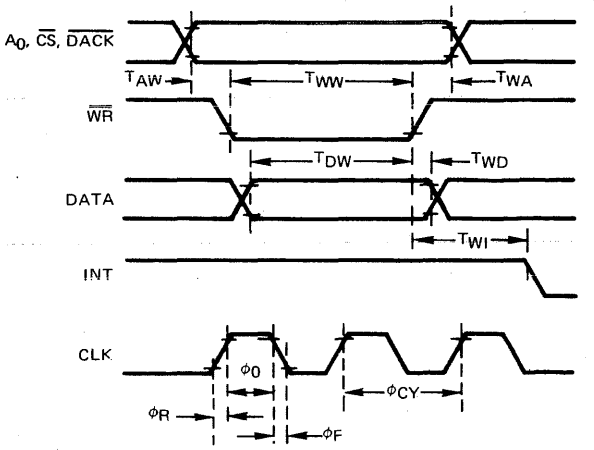
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TIMING WAVEFORMS

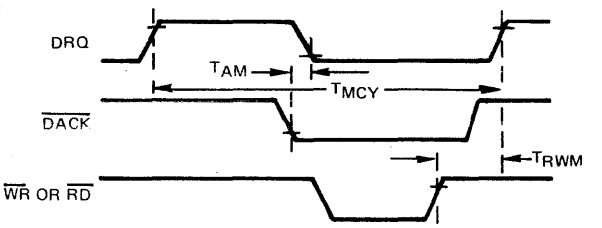
PROCESSOR READ OPERATION



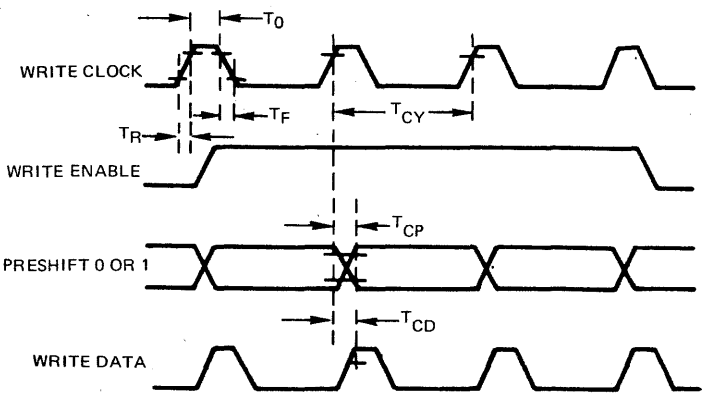
PROCESSOR WRITE OPERATION



DMA OPERATION



FDD READ OPERATION

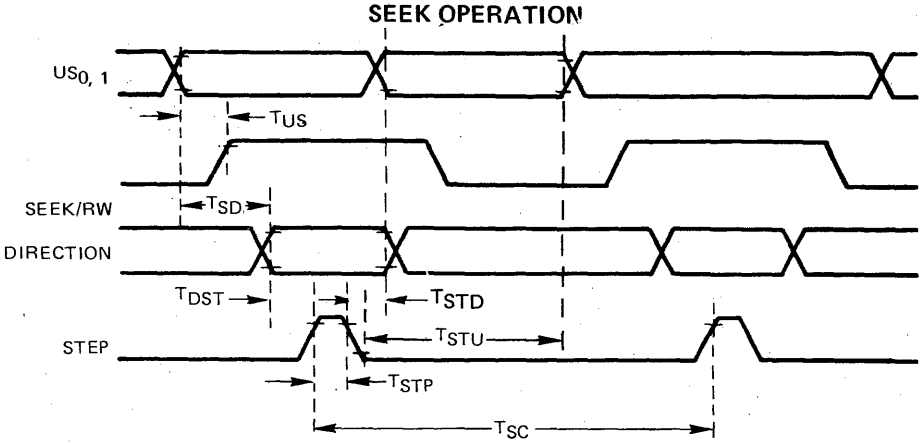


	PRESHIFT 0	PRESHIFT 1
NORMAL	0	0
LATE	0	1
EARLY	1	0
INVALID	1	1

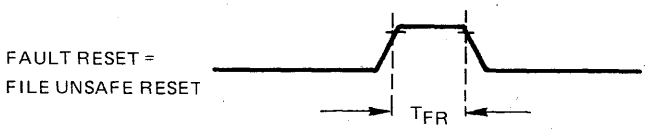
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TIMING WAVEFORMS (CONT.)

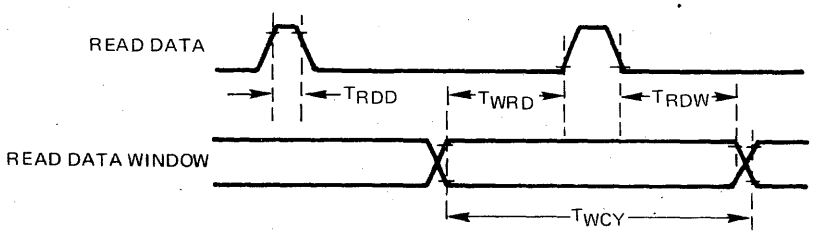
SEEK OPERATION



FLT RESET



FDD READ OPERATION

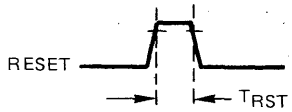


Note: Either polarity data window is valid.

TERMINAL COUNT



RESET



INTERNAL REGISTERS

The μPD765 contains two registers which may be accessed by the main system processor; a Status Register and a Data Register. The 8-bit Status Register contains the status information of the FDC, and may be accessed at any time. The 8-bit Data Register (actually consists of several registers in a stack with only one register presented to the data bus at a time), which stores data, commands, parameters, and FDD status information. Data bytes are read out of, or written into, the Data Register in order to program or obtain the results after a particular command. The Status Register may only be read and is used to facilitate the transfer of data between the processor and μPD765.

The relationship between the Status/Data registers and the signals $\overline{RD}$, $\overline{WR}$, and A_0 is shown below.

A_0	$\overline{RD}$	$\overline{WR}$	FUNCTION
0	0	1	Read Status Register
0	1	0	Illegal
0	0	0	Illegal
1	0	0	Illegal
1	0	1	Read from Data Register
1	1	0	Write into Data Register

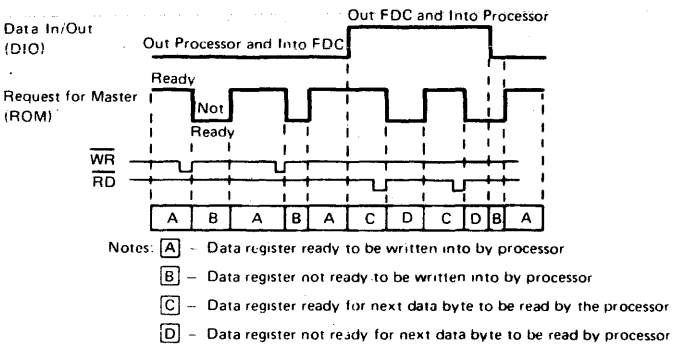
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INTERNAL REGISTERS (CONT.)

The bits in the Status Register are defined as follows:

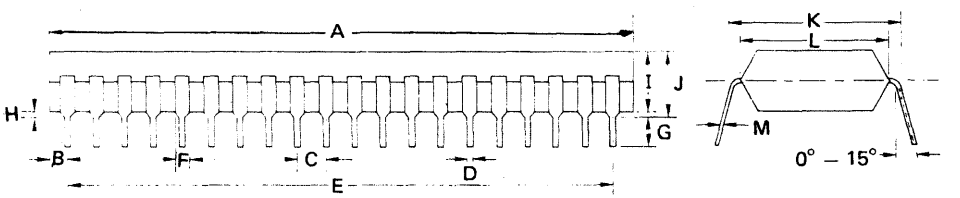
BIT NUMBER	NAME	SYMBOL	DESCRIPTION
DB_0	FDD 0 Busy	D_0B	FDD number 0 is in the Seek mode.
DB_1	FDD 1 Busy	D_1B	FDD number 1 is in the Seek mode.
DB_2	FDD 2 Busy	D_2B	FDD number 2 is in the Seek mode.
DB_3	FDD 3 Busy	D_3B	FDD number 3 is in the Seek mode.
DB_4	FDC Busy	CB	A read or write command is in process.
DB_5	Non-DMA mode	NDM	The FDC is in the non-DMA mode.
DB_6	Data Input/Output	DIO	Indicates direction of data transfer between FDC and Data Register. If DIO = "1" then transfer is from Data Register to the Processor. If DIO = "0", then transfer is from the Processor to Data Register.
DB_7	Request for Master	RQM	Indicates Data Register is ready to send or receive data to or from the Processor. Both bits DIO and RQM should be used to perform the handshaking functions of "ready" and "direction" to the processor.

The DIO and RQM bits in the Status Register indicate when Data is ready and in which direction data will be transferred on the Data Bus.



Notes: A – Data register ready to be written into by processor
B – Data register not ready to be written into by processor
C – Data register ready for next data byte to be read by the processor
D – Data register not ready for next data byte to be read by processor

PACKAGE OUTLINE μPD765C



ITEM	MILLIMETERS	INCHES
A	51.5 MAX	2.028 MAX
B	1.62	0.064
C	2.54 ± 0.1	0.10 ± 0.004
D	0.5 ± 0.1	0.019 ± 0.004
E	48.26	1.9
F	1.2 MIN	0.047 MIN
G	2.54 MIN	0.10 MIN
H	0.5 MIN	0.019 MIN
I	5.22 MAX	0.206 MAX
J	5.72 MAX	0.225 MAX
K	15.24	0.600
L	13.2	0.520
M	$0.25^{+0.1}_{-0.05}$	$0.010^{+0.004}_{-0.002}$

COMMAND SEQUENCE

The μPD765 is capable of performing 15 different commands. Each command is initiated by a multi-byte transfer from the processor, and the result after execution of the command may also be a multi-byte transfer back to the processor. Because of this multi-byte interchange of information between the μPD765 and the processor, it is convenient to consider each command as consisting of three phases:

Command Phase: The FDC receives all information required to perform a particular operation from the processor.

Execution Phase: The FDC performs the operation it was instructed to do.

Result Phase: After completion of the operation, status and other housekeeping information are made available to the processor.

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PHASE	R/W	DATA BUS D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	REMARKS
READ DATA										
Command	W	MT	MF	SK	0	0	1	1	0	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
	W	C								Sector ID information prior to Command execution
	W	H								
	W	R								
	W	N								
	W	EOT								
	W	GPL								
	W	DTL								
Execution										Data-transfer between the FDD and main-system
Result	R	ST 0								Status information after Command execution
	R	ST 1								
	R	ST 2								
	R	C								Sector ID information after Command execution
	R	H								
	R	R								
	R	N								
READ DELETED DATA										
Command	W	MT	MF	SK	0	1	1	0	0	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
	W	C								Sector ID information prior to Command execution
	W	H								
	W	R								
	W	N								
	W	EOT								
	W	GPL								
	W	DTL								
Execution										Data-transfer between the FDD and main-system
Result	R	ST 0								Status information after Command execution
	R	ST 1								
	R	ST 2								
	R	C								Sector ID information after Command execution
	R	H								
	R	R								
	R	N								
WRITE DATA										
Command	W	MT	MF	0	0	0	1	0	1	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
	W	C								Sector ID information prior to Command execution
	W	H								
	W	R								
	W	N								
	W	EOT								
	W	GPL								
	W	DTL								
Execution										Data-transfer between the main-system and FDD
Result	R	ST 0								Status information after Command execution
	R	ST 1								
	R	ST 2								
	R	C								Sector ID information after Command execution
	R	H								
	R	R								
	R	N								
WRITE DELETED DATA										
Command	W	MT	MF	0	0	1	0	0	1	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
	W	C								Sector ID information prior to Command execution
	W	H								
	W	R								
	W	N								
	W	EOT								
	W	GPL								
	W	DTL								
Execution										Data-transfer between the FDD and main-system
Result	R	ST 0								Status information after Command execution
	R	ST 1								
	R	ST 2								
	R	C								Sector ID information after Command execution
	R	H								
	R	R								
	R	N								

PHASE	R/W	DATA BUS D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	REMARKS
READ A TRACK										
Command	W	0	MF	SK	0	0	0	1	0	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
	W	C								Sector ID information prior to Command execution
	W	H								
	W	R								
	W	N								
	W	EOT								
	W	GPL								
	W	DTL								
Execution										Data-transfer between the FDD and main-system. FDC reads all of cylinders contents from index hole to EOT.
Result	R	ST 0								Status information after Command execution
	R	ST 1								
	R	ST 2								
	R	C								Sector ID information after Command execution
	R	H								
	R	R								
	R	N								
READ ID										
Command	W	0	MF	0	0	1	0	1	0	Commands
	W	X	X	X	X	X	HD	US1	US0	
Execution										The first correct ID information on the Cylinder is stored in Data Register
Result	R	ST 0								Status information after Command execution
	R	ST 1								
	R	ST 2								
	R	C								Sector ID information during Execution Phase
	R	H								
	R	R								
	R	N								
FORMAT A TRACK										
Command	W	0	MF	0	0	1	1	0	1	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
	W	N								Bytes/Sector
	W	SC								Sectors/Track
	W	GPL								Gap 3
	W	D								Filler Byte
Execution										FDC formats an entire cylinder
Result	R	ST 0								Status information after Command execution
	R	ST 1								
	R	ST 2								
	R	C								In this case, the ID information has no meaning
	R	H								
	R	R								
	R	N								
SCAN EQUAL										
Command	W	MT	MF	SK	1	0	0	0	1	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
	W	C								Sector ID information prior to Command execution
	W	H								
	W	R								
	W	N								
	W	EOT								
	W	GPL								
	W	STP								
Execution										Data-compared between the FDD and main-system
Result	R	ST 0								Status information after Command execution
	R	ST 1								
	R	ST 2								
	R	C								Sector ID information after Command execution
	R	H								
	R	R								
	R	N								

Note: ① Symbols used in this table are described at the end of this section.

② A_0 should equal binary 1 for all operations.

③ X = Don't care, usually made to equal binary 0.

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PHASE	R/W	DATA BUS D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	REMARKS
SCAN LOW OR EQUAL										
Command	W	MT	MF	SK	1	1	0	0	1	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
	W	C								Sector ID information prior
	W	H								Command execution
	W	R								
	W	N								
	W	EOT								
	W	GPL								
	W	STP								
Execution										Data-compared between the FDD and main-system
Result	R	ST 0								Status information after
	R	ST 1								Command execution
	R	ST 2								
	R	C								Sector ID information after
	R	H								Command execution
	R	R								
	R	N								
SCAN HIGH OR EQUAL										
Command	W	MT	MF	SK	1	1	1	0	1	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
	W	C								Sector ID information prior
	W	H								Command execution
	W	R								
	W	N								
	W	EOT								
	W	GPL								
	W	STP								
Execution										Data-compared between the FDD and main-system
Result	R	ST 0								Status information after
	R	ST 1								Command execution
	R	ST 2								
	R	C								Sector ID information after
	R	H								Command execution
	R	R								
	R	N								

PHASE	R/W	DATA BUS D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	REMARKS
RECALIBRATE										
Command	W	0	0	0	0	0	1	1	1	Command Codes
	W	X	X	X	X	X	0	US1	US0	
Execution										Head retracted to Track 0
SENSE INTERRUPT STATUS										
Command	W	0	0	0	0	1	0	0	0	Command Codes
Result	R	STO								Status information at the end
	R	PCN								of seek-operation about the FDC
SPECIFY										
Command	W	0	0	0	0	0	0	1	1	Command Codes
	W	SRT						HUT		
	W	HLT						ND		
SENSE DRIVE STATUS										
Command	W	0	0	0	0	0	1	0	0	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
Result	R	ST 3								Status information about FDD
SEEK										
Command	W	0	0	0	0	1	1	1	1	Command Codes
	W	X	X	X	X	X	HD	US1	US0	
	W	NCN								
Execution										Head is positioned over proper Cylinder on Diskette
INVALID										
Command	W	Invalid Codes								Invalid Command Codes (NoOp – FDC goes into Standby State)
Result	R	ST 0								ST 0 = 80 (16)

COMMAND SYMBOL DESCRIPTION

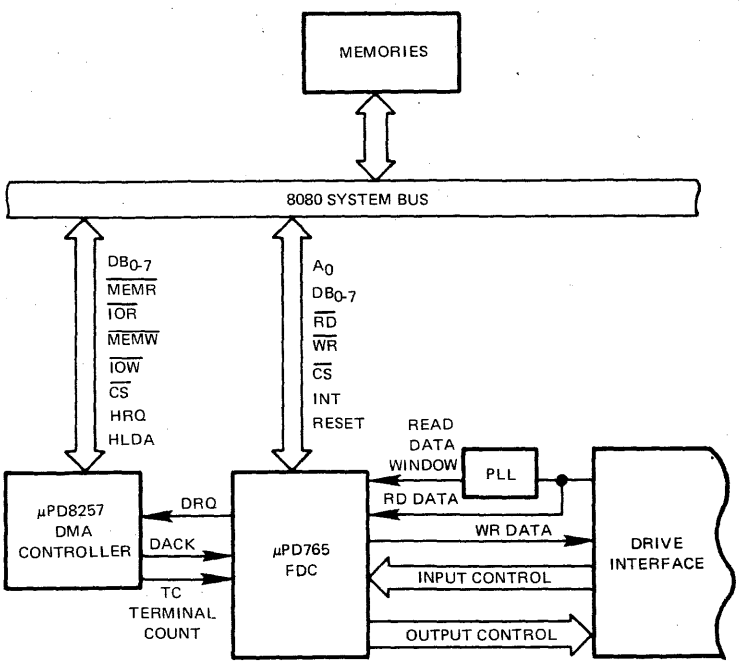
SYMBOL	NAME	DESCRIPTION
A_0		A_0 stands for control signal A_0 (pin 5)
C	Cylinder Number	C stands for the current/selected Cylinder (track) number 0 through 76 of the medium.
D	Data	D stands for the data pattern which is going to be written into a Sector.
D_7-D_0	Data Bus	8-bit Data Bus, where D_7 stands for a most significant bit, and D_0 stands for a least significant bit.
DTL	Data Length	When N is defined as 00, DTL stands for the data length which users are going to read out or write into the Sector.
EOT	End of Track	EOT stands for the final Sector number on a Cylinder.
GPL	Gap Length	GPL stands for the length of Gap 3 (excluding VCO Sync. Field).
H	Head Address	H stands for head number 0 or 1, as specified in ID field.
HD	Head	HD stands for a selected head number 0 or 1.
HLT	Head Load Time	HLT stands for the head load time in the FDD (2 to 256 ms in 2 ms increments).
HUT	Head Unload Time	HUT stands for the head unload time after a read or write operation has occurred (0 to 240 ms in 16 ms increments).
MF	FM or MFM Mode	If MF is low, FM mode is selected, and if it is high, MFM mode is selected.
MT	Multi-Track	If MT is high, a multi-track operation is to be performed. (A cylinder under both HD0 and HD1 will be read or written.)

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COMMAND SYMBOL DESCRIPTION (CONT.)

SYMBOL	NAME	DESCRIPTION
N	Number	N stands for the number of data bytes written in a Sector.
NCN	New Cylinder Number	NCN stands for a new Cylinder number, which is going to be reached as a result of the Seek operation. Desired position of Head.
ND	Non-DMA Mode	ND stands for operation in the Non-DMA Mode.
PCN	Present Cylinder Number	PCN stands for the Cylinder number at the completion of SENSE INTERRUPT STATUS Command. Position of Head at present time.
R	Record	R stands for the Sector number, which will be read or written.
R/W	Read/Write	R/W stands for either Read (R) or Write (W) signal.
SC	Sector	SC indicates the number of Sectors per Cylinder.
SK	Skip	SK stands for Skip Deleted Data Address Mark.
SRT	Step Rate Time	SRT stands for the Stepping Rate for the FDD. (1 to 16 ms in 1 ms increments.) Must be defined for each of the four drives.
ST 0 ST 1 ST 2 ST 3	Status 0 Status 1 Status 2 Status 3	ST 0-3 stand for one of four registers which store the status information after a command has been executed. This information is available during the result phase after command execution. These registers should not be confused with the main status register (selected by $A_0 = 0$). ST 0-3 may be read only after a command has been executed and contain information relevant to that particular command.
STP		During a Scan operation, if STP = 1, the data in contiguous sectors is compared byte by byte with data sent from the processor (or DMA); and if STP = 2, then alternate sectors are read and compared.
US	Unit Select	US stands for a selected drive number 0 or 1.

SYSTEM CONFIGURATION



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PROCESSOR INTERFACE

During Command or Result Phases the Main Status Register (described earlier) must be read by the processor before each byte of information is written into or read from the Data Register. Bits D6 and D7 in the Main Status Register must be in a 0 and 1 state, respectively, before each byte of the command word may be written into the μPD765. Many of the commands require multiple bytes, and as a result the Main Status Register must be read prior to each byte transfer to the μPD765. Also, bits 6 and 7 in the Status Register must appear as D6 = 0 and D7 = 1 before the byte transfer is executed. During the Result Phase, D6 and D7 in the Main Status Register must both be 1's (D6 = 1 and D7 = 1) before reading each byte from the Data Register. Note, this reading of the Main Status Register before each byte transfer to the μPD765 is required in only the Command and Result Phases, and NOT during the Execution Phase.

During the Execution Phase, the Main Status Register need not be read. If the μPD765 is in the NON-DMA Mode, then the receipt of each data byte (if μPD765 is reading data from FDD) is indicated by an Interrupt signal on pin 18 (INT = 1). The generation of a Read signal ($\overline{RD}$ = 0) will reset the Interrupt as well as output the Data onto the Data Bus. If the processor cannot handle interrupts fast enough (every 13 μs) then it may poll the Main Status Register and then bit D7 (ROM) functions just like the Interrupt signal. If a Write Command is in process then the $\overline{WR}$ signal performs the reset to the Interrupt signal.

If the μPD765 is in the DMA Mode, no Interrupts are generated during the Execution Phase. The μPD765 generates DRQ's (DMA Requests) when each byte of data is available. The DMA Controller responds to this request with both a $\overline{DACK}$ = 0 (DMA Acknowledge) and a $\overline{RD}$ = 0 (Read signal). When the DMA Acknowledge signal goes low ($\overline{DACK}$ = 0) then the DMA Request is reset (DRQ = 0). If a Write Command has been programmed then a $\overline{WR}$ signal will appear instead of $\overline{RD}$. After the Execution Phase has been completed (Terminal Count has occurred) then an Interrupt will occur (INT = 1). This signifies the beginning of the Result Phase. When the first byte of data is read during the Result Phase, the Interrupt is automatically reset (INT = 0).

It is important to note that during the Result Phase all bytes shown in the Command Table must be read. The Read Data Command, for example has seven bytes of data in the Result Phase. All seven bytes must be read in order to successfully complete the Read Data Command. The μPD765 will not accept a new command until all seven bytes have been read. Other commands may require fewer bytes to be read during the Result Phase.

The μPD765 contains five Status Registers. The Main Status Register mentioned above may be read by the processor at any time. The other four Status Registers (ST0, ST1, ST2, and ST3) are only available during the Result Phase, and may be read only after successfully completing a command. The particular command which has been executed determines how many of the Status Registers will be read.

The bytes of data which are sent to the μPD765 to form the Command Phase, and are read out of the μPD765 in the Result Phase, must occur in the order shown in the Command Table. That is, the Command Code must be sent first and the other bytes sent in the prescribed sequence. No foreshortening of the Command or Result Phases are allowed. After the last byte of data in the Command Phase is sent to the μPD765, the Execution Phase automatically starts. In a similar fashion, when the last byte of data is read out in the Result Phase, the command is automatically ended and the μPD765 is ready for a new command. A command may be truncated (prematurely ended) by simply sending a Terminal Count signal to pin 16 (TC = 1). This is a convenient means of ensuring that the processor may always get the μPD765's attention even if the disk system hangs up in an abnormal manner.

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READ DATA

A set of nine (9) byte words are required to place the FDC into the Read Data Mode. After the Read Data command has been issued the FDC loads the head (if it is in the unloaded state), waits the specified head settling time (defined in the Specify Command), and begins reading ID Address Marks and ID fields. When the current sector number ("R") stored in the ID Register (IDR) compares with the sector number read off the diskette, then the FDC outputs data (from the data field) byte-to-byte to the main system via the data bus.

After completion of the read operation from the current sector, the Sector Number is incremented by one, and the data from the next sector is read and output on the data bus. This continuous read function is called a "Multi-Sector Read Operation." The Read Data Command may be terminated by the receipt of a Terminal Count signal. Upon receipt of this signal, the FDC stops outputting data to the processor, but will continue to read data from the current sector, check CRC (Cyclic Redundancy Count) bytes, and then at the end of the sector terminate the Read Data Command.

The amount of data which can be handled with a single command to the FDC depends upon MT (multi-track), MF (MFM/FM), and N (Number of Bytes/Sector). Table 1 below shows the Transfer Capacity.

Multi-Track MT	MFM/FM MF	Bytes/Sector N	Maximum Transfer Capacity (Bytes/Sector) (Number of Sectors)	Final Sector Read from Diskette
0	0	00	(128) (26) = 3,328	26 at Side 0
0	1	01	(256) (26) = 6,656	26 at Side 1
1	0	00	(128) (52) = 6,656	26 at Side 1
1	1	01	(256) (52) = 13,312	
0	0	01	(256) (15) = 3,840	15 at Side 0
0	1	02	(512) (15) = 7,680	15 at Side 1
1	0	01	(256) (30) = 7,680	15 at Side 1
1	1	02	(512) (30) = 15,360	
0	0	02	(512) (8) = 4,096	8 at Side 0
0	1	03	(1024) (8) = 8,192	8 at Side 1
1	0	02	(512) (16) = 8,192	8 at Side 1
1	1	03	(1024) (16) = 16,384	

Table 1. Transfer Capacity

The "multi-track" function (MT) allows the FDC to read data from both sides of the diskette. For a particular cylinder, data will be transferred starting at Sector 0, Side 0 and completing at Sector L, Side 1 (Sector L = last sector on the side). Note, this function pertains to only one cylinder (the same track) on each side of the diskette.

When N = 0, then DTL defines the data length which the FDC must treat as a sector. If DTL is smaller than the actual data length in a Sector, the data beyond DTL in the Sector, is not sent to the Data Bus. The FDC reads (internally) the complete Sector performing the CRC check, and depending upon the manner of command termination, may perform a Multi-Sector Read Operation. When N is non-zero, then DTL has no meaning.

At the completion of the Read Data Command, the head is not unloaded until after Head Unload Time Interval (specified in the Specify Command) has elapsed. If the processor issues another command before the head unloads then the head settling time may be saved between subsequent reads. This time out is particularly valuable when a diskette is copied from one drive to another.

If the FDC reads all the data in the final sector of a cylinder and the read operation is not terminated by the processor, then the FDC sets the EN (End of Cylinder) flag in Status Register 1 to a 1 (high), and terminates the Read Data Command.

If the FDC detects the Index Hole twice without finding the right sector, (indicated in "R"), then the FDC sets the ND (No Data) flag in Status Register 1 to a 1 (high), and terminates the Read Data Command.

After reading the ID and Data Fields in each sector, the FDC checks the CRC bytes. If a read error is detected (incorrect CRC in ID field), the FDC sets the DE (Data Error) flag in Status Register 1 to a 1 (high), and if a CRC error occurs in the Data Field the FDC also sets the DD (Data Error in Data Field) flag in Status Register 2 to a 1 (high), and terminates the Read Data Command.

If the FDC reads a Deleted Data Address Mark off the diskette, and the SK bit (bit D5 in the first Command Word) is not set (SK = 0), then the FDC sets the DM (Control Mark) flag in Status Register 2 to a 1 (high), and terminates the Read Data Command, after reading all the data in the Sector. If SK = 1, the FDC skips the sector with the Deleted Data Address Mark and reads the next sector.

During disk data transfers between the FDC and the processor, via the data bus, the FDC must be serviced by the processor every 27 μs in the FM Mode, and every 13 μs in the MFM Mode, or the FDC sets the OR (Over Run) flag in Status Register 1 to a 1 (high), and terminates the Read Data Command.

If the processor terminates a read (or write) operation in the FDC, then the ID Information in the Result Phase is dependent upon the state of the MT bit and EOT byte. Table 2 shows the values for C, H, R, and N, when the processor terminates the Command.

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FUNCTIONAL DESCRIPTION OF COMMANDS (CONT.)

MT	EOT	Final Sector Transferred to Processor	ID Information at Result Phase			
			C	N	R	N
0	1A	Sector 1 to 25 at Side 0	NC	NC	R + 1	NC
	0F	Sector 1 to 14 at Side 0				
	08	Sector 1 to 7 at Side 0				
	1A	Sector 26 at Side 0	C + 1	NC	R = 01	NC
	0F	Sector 15 at Side 0				
	08	Sector 8 at Side 0				
	1A	Sector 1 to 25 at Side 1	NC	NC	R + 1	NC
	0F	Sector 1 to 14 at Side 1				
	08	Sector 1 to 7 at Side 1				
	1A	Sector 26 at Side 1	C + 1	NC	R = 01	NC
	0F	Sector 15 at Side 1				
	08	Sector 8 at Side 1				
1	1A	Sector 1 to 25 at Side 0	NC	NC	R + 1	NC
	0F	Sector 1 to 14 at Side 0				
	08	Sector 1 to 7 at Side 0				
	1A	Sector 26 at Side 0	NC	$\overline{LSB}$	R = 01	NC
	0F	Sector 15 at Side 0				
	08	Sector 8 at Side 0				
	1A	Sector 1 to 25 at Side 1	NC	NC	R + 1	NC
	0F	Sector 1 to 14 at Side 1				
	08	Sector 1 to 7 at Side 1				
	1A	Sector 26 at Side 1	C + 1	$\overline{LSB}$	R = 01	NC
	0F	Sector 15 at Side 1				
	08	Sector 8 at Side 1				

Notes: ① NC (No Change): The same value as the one at the beginning of command execution.

② LSB (Least Significant Bit): The least significant bit of H is complemented.

Table 2: ID Information When Processor Terminates Command

WRITE DATA

A set of nine (9) bytes are required to set the FDC into the Write Data mode. After the Write Data command has been issued the FDC loads the head (if it is in the unloaded state), waits the specified heat settling time (defined in the Specify Command), and begins reading ID Fields. When the current sector number ("R"), stored in the ID Register (IDR) compares with the sector number read off the diskette, then the FDC takes data from the processor byte-by-byte via the data bus, and outputs it to the FDD.

After writing data into the current sector, the Sector Number stored in "R" is incremented by one, and the next data field is written into. The FDC continues this "Multi-Sector Write Operation" until the issuance of a Terminal Count signal. If a Terminal Count signal is sent to the FDC it continues writing into the current sector to complete the data field. If the Terminal Count signal is received while a data field is being written then the remainder of the data field is filled with 00 (zeros).

The FDC reads the ID field of each sector and checks the CRC bytes. If the FDC detects a read error (incorrect CRC) in one of the ID Fields, it sets the DE (Data Error) flag of Status Register 1 to a 1 (high), and terminates the Write Data Command. (Status Register 0 also has bits 7 and 6 set to 0 and 1 respectively.)

The Write Command operates in much the same manner as the Read Command. The following items are the same, and one should refer to the Read Data Command for details:

- Transfer Capacity
- EN (End of Cylinder) Flag
- ND (No Data) Flag
- Head Unload Time Interval
- ID Information when the processor terminates command (see Table 2)
- Definition of DTL when N = 0 and when N ≠ 0

In the Write Data mode, data transfers between the processor and FDC, via the Data Bus, must occur every 31 μs in the FM mode, and every 15 μs in the MFM mode. If the time interval between data transfers is longer than this then the FDC sets the OR (Over Run) flag in Status Register 1 to a 1 (high), and terminates the Write Data Command. (Status Register 0 also has bit 7 and 6 set to 0 and 1 respectively.)

WRITE DELETED DATA

This command is the same as the Write Data Command except a Deleted Data Address Mark is written at the beginning of the Data Field instead of the normal Data Address Mark.

READ DELETED DATA

This command is the same as the Read Data Command except that when the FDC detects a Data Address Mark at the beginning of a Data Field (and SK = 0 (low), it will read all the data in the sector and set the DM flag in Status Register 2 to a 1 (high), and then terminate the command. If SK = 1, then the FDC skips the sector with the Data Address Mark and reads the next sector.

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READ A TRACK

This command is similar to READ DATA Command except that this is a continuous READ operation where the entire contents of the track are read. Immediately after encountering the INDEX HOLE, the FDC starts reading all data on the track, Gap bytes, Address Marks and Data are all read as a continuous data stream. If the FDC finds an error in the ID or DATA CRC check bytes, it continues to read data from the track. The FDC compares the ID information read from each sector with the value stored in the IDR, and sets the ND flag of Status Register 1 to a 1 (high) if there is no comparison. Multi-track or skip operations are not allowed with this command.

This command terminates when EOT number of sectors have been read ($EOT_{max} = FF_{hex} = 255_{dec}$). If the FDC does not find an ID Address Mark on the diskette after it encounters the INDEX HOLE for the second time, then it sets the MA (missing address mask) flag in Status Register 1 to a 1 (high), and terminates the command.

READ ID

The READ ID Command is used to give the present position of the recording head. The FDC stores the values from the first ID Field it is able to read. If no proper ID Address Mark is found on the diskette, before the INDEX HOLE is encountered for the second time then the MA (Missing Address Mark) flag in Status Register 1 is set to a 1 (high), and if no data is found then the ND (No Data) flag is also set in Status Register 1 to a 1 (high). The command is then terminated with Bits 7 and 6 in Status Register 0 set to 0 and 1 respectively.

FORMAT A TRACK

The Format Command allows an entire track to be formatted. After the INDEX HOLE is detected, Data is written on the Diskette; Gaps, Address Marks, ID Fields and Data Fields, all per the IBM System 34 (Double Density) or System 3740 (Single Density) Format are recorded. The particular format which will be written is controlled by the values programmed into N (number of bytes/sector), SC (sectors-cylinder), GPL (Gap Length), and D (Data Pattern) which are supplied by the processor during the Command Phase. The Data Field is filled with the Byte of data stored in D. The ID Field for each sector is supplied by the processor; that is, four data requests per sector are made by the FDC for C (Cylinder Number), H (Head Number), R (Sector Number) and N (Number of Bytes/Sector). This allows the diskette to be formatted with non-sequential sector numbers, if desired.

After formatting each sector, the processor must send new values for C, H, R, and N to the μPD765 for each sector on the track. The contents of the R register is incremented by one after each sector is formatted, thus, the R register contains a value of R + 1 when it is read during the Result Phase. This incrementing and formatting continues for the whole cylinder until the FDC encounters the INDEX HOLE for the second time, whereupon it terminates the command.

If a FAULT signal is received from the FDD at the end of a write operation, then the FDC sets the EC flag of Status Register 0 to a 1 (high), and terminates the command after setting bits 7 and 6 of Status Register 0 to 0 and 1 respectively. Also the loss of a READY signal at the beginning of a command execution phase causes bits 7 and 6 of Status Register 0 to be set to 0 and 1 respecitvely.

Table 3 shows the relationship between N, SC, and GPL for various sector sizes:

FORMAT	SECTOR SIZE	N	SC	GPL ①	GPL ②	REMARKS
FM Mode	128 bytes/Sector	00	$1A_{(16)}$	.07	$1B_{(16)}$	IBM Diskette 1
	256	01	$0F_{(16)}$	$OE_{(16)}$	$2A_{(16)}$	IBM Diskette 2
	512	02	08	$1B_{(16)}$	$3A_{(16)}$	
FM Mode	1024 bytes/Sector	03	04	–	–	
	2048	04	02	–	–	
	4096	05	01	–	–	
MFM Mode	256	01	$1A_{(16)}$	$OE_{(16)}$	$36_{(16)}$	IBM Diskette 2D
	512	02	$0F_{(16)}$	$1B_{(16)}$	$54_{(16)}$	
	1024	03	08	$35_{(16)}$	$74_{(16)}$	IBM Diskette 2D
	2048	04	04	–	–	
	4096	05	02	–	–	
	8192	06	01	–	–	

Table 3

Note: ① Suggested values of GPL in Read or Write Commands to avoid splice point between data field and ID field of contiguous sections.

② Suggested values of GPL in format command.

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FUNCTIONAL DESCRIPTION OF COMMANDS (CONT.)

SCAN COMMANDS

The SCAN Commands allow data which is being read from the diskette to be compared against data which is being supplied from the main system (Processor in NON-DMA mode, and DMA Controller in DMA mode). The FDC compares the data on a byte-by-byte basis, and looks for a sector of data which meets the conditions of $D_{FDD} = D_{Processor}$, $D_{FDD} \leq D_{Processor}$, or $D_{FDD} \geq D_{Processor}$. Ones complement arithmetic is used for comparison (FF = largest number, 00 = smallest number). After a whole sector of data is compared, if the conditions are not met, the sector number is incremented (R + STP → R), and the scan operation is continued. The scan operation continues until one of the following conditions occur; the conditions for scan are met (equal, low, or high), the last sector on the track is reached (EOT), or the terminal count signal is received.

If the conditions for scan are met then the FDC sets the SH (Scan Hit) flag of Status Register 2 to a 1 (high), and terminates the Scan Command. If the conditions for scan are not met between the starting sector (as specified by R) and the last sector on the cylinder (EOT), then the FDC sets the SN (Scan Not Satisfied) flag of Status Register 2 to a 1 (high), and terminates the Scan Command. The receipt of a TERMINAL COUNT signal from the Processor or DMA Controller during the scan operation will cause the FDC to complete the comparison of the particular byte which is in process, and then to terminate the command. Table 4 shows the status of bits SH and SN under various conditions of SCAN.

COMMAND	STATUS REGISTER 2		COMMENTS
	BIT 2 = SN	BIT 3 = SH	
Scan Equal	0	1	$D_{FDD} = D_{Processor}$
	1	0	$D_{FDD} \neq D_{Processor}$
Scan Low or Equal	0	1	$D_{FDD} = D_{Processor}$
	0	0	$D_{FDD} < D_{Processor}$
	1	0	$D_{FDD} \not< D_{Processor}$
Scan High or Equal	0	1	$D_{FDD} = D_{Processor}$
	0	0	$D_{FDD} < D_{Processor}$
	1	0	$D_{FDD} \not> D_{Processor}$

Table 4

If the FDC encounters a Deleted Data Address Mark on one of the sectors (and SK = 0), then it regards the sector as the last sector on the cylinder, sets CM (Control Mark) flag of Status Register 2 to a 1 (high) and terminates the command. If SK = 1, the FDC skips the sector with the Deleted Address Mark, and reads the next sector. In the second case (SK = 1), the FDC sets the CM (Control Mark) flag of Status Register 2 to a 1 (high) in order to show that a Deleted Sector had been encountered.

When either the STP (contiguous sectors = 01, or alternate sectors = 02 sectors are read) or the MT (Multi-Track) are programmed, it is necessary to remember that the last sector on the track must be read. For example, if STP = 02, MT = 0, the sectors are numbered sequentially 1 through 26, and we start the Scan Command at sector 21; the following will happen. Sectors 21, 23, and 25 will be read, then the next sector (26) will be skipped and the Index Hole will be encountered before the EOT value of 26 can be read. This will result in an abnormal termination of the command. If the EOT had been set at 25 or the scanning started at sector 20, then the Scan Command would be completed in a normal manner.

During the Scan Command data is supplied by either the processor or DMA Controller for comparison against the data read from the diskette. In order to avoid having the OR (Over Run) flag set in Status Register 1, it is necessary to have the data available in less than 27 μs (FM Mode) or 13 μs (MFM Mode). If an Overrun occurs the FDC ends the command with bits 7 and 6 of Status Register 0 set to 0 and 1, respectively.

SEEK

The read/write head within the FDD is moved from track to track under control of the Seek Command. The FDC compares the PCN (Present Cylinder Number) which is the current head position with the NCN (New Cylinder Number), and if there is a difference performs the following operation:

PCN < NCN: Direction signal to FDD set to a 1 (high), and Step Pulses are issued.
PCN > NCN: Direction signal to FDD set to a 0 (low), and Step Pulses are issued.

The rate at which Step Pulses are issued is controlled by SRT (Stepping Rate Time) in the SPECIFY Command. After each Step Pulse is issued NCN is compared against PCN, and when NCN = PCN, then the SE (Seek End) flag is set in Status Register 0 to a 1 (high), and the command is terminated.

During the Command Phase of the Seek operation the FDC is in the FDC BUSY state, but during the Execution Phase it is in the NON BUSY state. While the FDC is in the NON BUSY state, another Seek Command may be issued, and in this manner parallel seek operations may be done on up to 4 Drives at once.

If a FDD is in a NOT READY state at the beginning of the command execution phase or during the seek operation, then the NR (NOT READY) flag is set in Status Register 0 to a 1 (high), and the command is terminated after bits 7 and 6 of Status Register 0 are set to 0 and 1 respectively.

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RECALIBRATE

The function of this command is to retract the read/write head within the FDD to the Track 0 position. The FDC clears the contents of the PCN counter, and checks the status of the Track 0 signed signal from the FDD. As long as the Track 0 signal is low, the Direction signal remains 1 (high) and Step Pulses are issued. When the Track 0 signal goes high, the SE (SEEK END) flag in Status Register 0 is set to a 1 (high) and the command is terminated. If the Track 0 signal is still low after 77 Step Pulse have been issued, the FDC sets the SE (SEEK END) and EC (EQUIPMENT CHECK) flags of Status Register 0 to both 1s (highs), and terminates the command after bits 7 and 6 of Status Register 0 is set to 0 and 1 respectively.

The ability to do overlap RECALIBRATE Commands to multiple FDDs and the loss of the READY signal, as described in the SEEK Command, also applies to the RECALIBRATE Command.

SENSE INTERRUPT STATUS

An Interrupt signal is generated by the FDC for one of the following reasons:

1. Upon entering the Result Phase of:
   a. Read Data Command
   b. Read a Cylinder Command
   c. Read ID Command
   d. Read Deleted Data Command
   e. Write Data Command
   f. Format a Cylinder Command
   g. Write Deleted Data Command
   h. Scan Commands
2. Ready Line of FDD changes state
3. End of Seek or Recalibrate Command
4. During Execution Phase in the NON-DMA Mode

Interrupts caused by reasons 1 and 4 above occur during normal command operations and are easily discernible by the processor. However, interrupts caused by reasons 2 and 3 above may be uniquely identified with the aid of the Sense Interrupt Status Command. This command when issued resets the interrupt signal and via bits 5, 6, and 7 of Status Register 0 identifies the cause of the interrupt.

SEEK END BIT 5	INTERRUPT CODE		CAUSE
	BIT 6	BIT 7	
0	1	1	Ready Line changed state, either polarity
1	0	0	Normal Termination of Seek or Recalibrate Command
1	1	0	Abnormal Termination of Seek or Recalibrate Command

Table 5

Neither the Seek or Recalibrate Command have a Result Phase. As a result it is mandatory to use the Sense Interrupt Status Command after these commands to effectively terminate them and to provide verification of where the head is positioned (PCN).

SPECIFY

The Specify Command sets the initial values for each of the three internal timers. The HUT (Head Unload Time) defines the time from the end of the Execution Phase of one of the Read/Write Commands to the head unload state. This timer is programmable from 0 to 240 ms in increments of 16 ms (00 = 0 ms, 01 = 16 ms, 02 = 32 ms, etc.). The SRT (Step Rate Time) defines the time interval between adjacent step pulses. This timer is programmable from 1 to 16 ms in increments of 1 ms (01 = 1 ms, 02 = 2 ms, 03 = 3 ms, etc.). The HLT (Head Load Time) defines the time between when the Head Load signal goes high and when the Read/Write operation starts. This timer is programmable from 2 to 256 ms in increments of 2 ms (00 = 2 ms, 01 = 4 ms, 02 = 6 ms, etc.).

The time intervals mentioned above are a direct function of the clock (CLK on pin 19). Times indicated above are for an 8 MHz clock, if the clock was reduced to 4 MHz (mini-floppy application) then all time intervals are increased by a factor of 2.

The choice of DMA or NON-DMA operation is made by the ND (NON-DMA) bit. When this bit is high (ND = 1) the NON-DMA mode is selected, and when ND = 0 the DMA mode is selected.

SENSE DRIVE STATUS

This command may be used by the processor whenever it wishes to obtain the status of the FDDs.

INVALID

If an invalid command is sent to the FDC (a command not defined above), then the FDC will terminate the command after bits 7 and 6 of Status Register 0 are set to 1 and 0 respectively. **A Sense Interrupt Status Command must be sent after Seek or Recalibrate Commands, otherwise the FDC will consider the next command to be an Invalid Command.**

In some applications the user may wish to use this command as a No-Op command, to place the FDC in a standby or no operation state.

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STATUS REGISTER IDENTIFICATION

BIT NO.	BIT NAME	BIT SYMBOL	DESCRIPTION
STATUS REGISTER 0			
D_7	Interrupt Code	IC	$D_7 = 0$ and $D_6 = 0$ Normal Termination of Command, (NT). Command was completed and properly executed.
D_6			$D_7 = 0$ and $D_6 = 1$ Abnormal Termination of Command, (AT). Execution of Command was started, but was not successfully completed.
			$D_7 = 1$ and $D_6 = 0$ Invalid Command issue, (IC). Command which was issued was never started.
			$D_7 = 1$ and $D_6 = 1$ Abnormal Termination because during command execution the ready signal from FDD changed state.
D_5	Seek End	SE	When the FDC completes the SEEK Command, this flag is set to 1 (high).
D_4	Equipment Check	EC	If a fault Signal is received from the FDD, or if the Track 0 Signal fails to occur after 77 Step Pulses (Recalibrate Command) then this flag is set.
D_3	Not Ready	NR	When the FDD is in the not-ready state and a read or write command is issued, this flag is set. If a read or write command is issued to Side 1 of a single sided drive, then this flag is set.
D_2	Head Address	HD	This flag is used to indicate the state of the head at Interrupt.
D_1	Unit Select 0	US 0	These flags are used to indicate a Drive Unit Number at Interrupt
D_0	Unit Select 1	US 1	
STATUS REGISTER 1			
D_7	End of Cylinder	EN	When the FDC tries to access a Sector beyond the final Sector of a Cylinder, this flag is set.
D_6			Not used. This bit is always 0 (low).
D_5	Data Error	DE	When the FDC detects a CRC error in either the ID field or the data field, this flag is set.
D_4	Over Run	OR	If the FDC is not serviced by the main-systems during data transfers, within a certain time interval, this flag is set.
D_3			Not used. This bit always 0 (low).
D_2	No Data	ND	During execution of READ DATA, WRITE DELETED DATA or SCAN Command, if the FDC cannot find the Sector specified in the IDR Register, this flag is set.
			During executing the READ ID Command, if the FDC cannot read the ID field without an error, then this flag is set.
			During the execution of the READ A Cylinder Command, if the starting sector cannot be found, then this flag is set.

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STATUS REGISTER IDENTIFICATION (CONT.)

BIT NO.	BIT NAME	BIT SYMBOL	DESCRIPTION
STATUS REGISTER 1 (CONT.)			
D_1	Not Writable	NW	During execution of WRITE DATA, WRITE DELETED DATA or Format A Cylinder Command, if the FDC detects a write protect signal from the FDD, then this flag is set.
D_0	Missing Address Mark	MA	If the FDC cannot detect the ID Address Mark after encountering the index hold twice, then this flag is set.
			If the FDC cannot detect the Data Address Mark or Deleted Data Address Mark, this flag is set. Also at the same time, the MD (Missing Address Mark in Data Field) of Status Register 2 is set.
STATUS REGISTER 2			
D_7			Not used. This bit is always 0 (low).
D_6	Control Mark	CM	During executing the READ DATA or SCAN Command, if the FDC encounters a Sector which contains a Deleted Data Address Mark, this flag is set.
D_5	Data Error in Data Field	DD	If the FDC detects a CRC error in the data field then this flag is set.
D_4	Wrong Cylinder	WC	This bit is related with the ND bit, and when the contents of C on the medium is different from that stored in the IDR, this flag is set.
D_3	Scan Equal Hit	SH	During execution, the SCAN Command, if the condition of "equal" is satisfied, this flag is set.
D_2	Scan Not Satisfied	SN	During executing the SCAN Command, if the FDC cannot find a Sector on the cylinder which meets the condition, then this flag is set.
D_1	Bad Cylinder	BC	This bit is related with the ND bit, and when the content of C on the medium is different from that stored in the IDR and the content of C is FF, then this flag is set.
D_0	Missing Address Mark in Data Field	MD	When data is read from the medium, if the FDC cannot find a Data Address Mark or Deleted Data Address Mark, then this flag is set.
STATUS REGISTER 3			
D_7	Fault	FT	This bit is used to indicate the status of the Fault signal from the FDD.
D_6	Write Protected	WP	This bit is used to indicate the status of the Write Protected signal from the FDD.
D_5	Ready	RY	This bit is used to indicate the status of the Ready signal from the FDD.
D_4	Track 0	T0	This bit is used to indicate the status of the Track 0 signal from the FDD.
D_3	Two Side	TS	This bit is used to indicate the status of the Two Side signal from the FDD.
D_2	Head Address	HD	This bit is used to indicate the status of Side Select signal to the FDD.
D_1	Unit Select 1	US 1	This bit is used to indicate the status of the Unit Select 1 signal to the FDD.
D_0	Unit Select 0	US 0	This bit is used to indicate the status of the Unit Select 0 signal to the FDD.

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NEC
μPD8155
μPD8156

2048 BIT STATIC MOS RAM WITH I/O PORTS AND TIMER

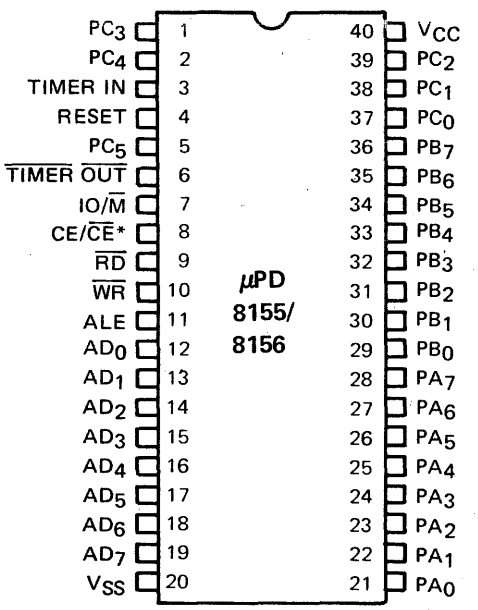
DESCRIPTION

The μPD8155 and μPD8156 are μPD8085A family components having 256 X 8 Static RAM, 3 programmable I/O ports and a programmable timer. They directly interface to the multiplexed μPD8085A bus with no external logic. The μPD8155 has an active low chip enable while the μPD8156 is active high.

FEATURES

- 256 X 8-Bit Static RAM
- Two Programmable 8-Bit I/O Ports
- One Programmable 6-Bit I/O Port
- Single Power Supplies: +5 Volt
- Directly Interfaces to the μPD8085A
- Available in 40 Pin Plastic Packages

PIN CONFIGURATION



*μPD8155: $\overline{CE}$
μPD8156: CE

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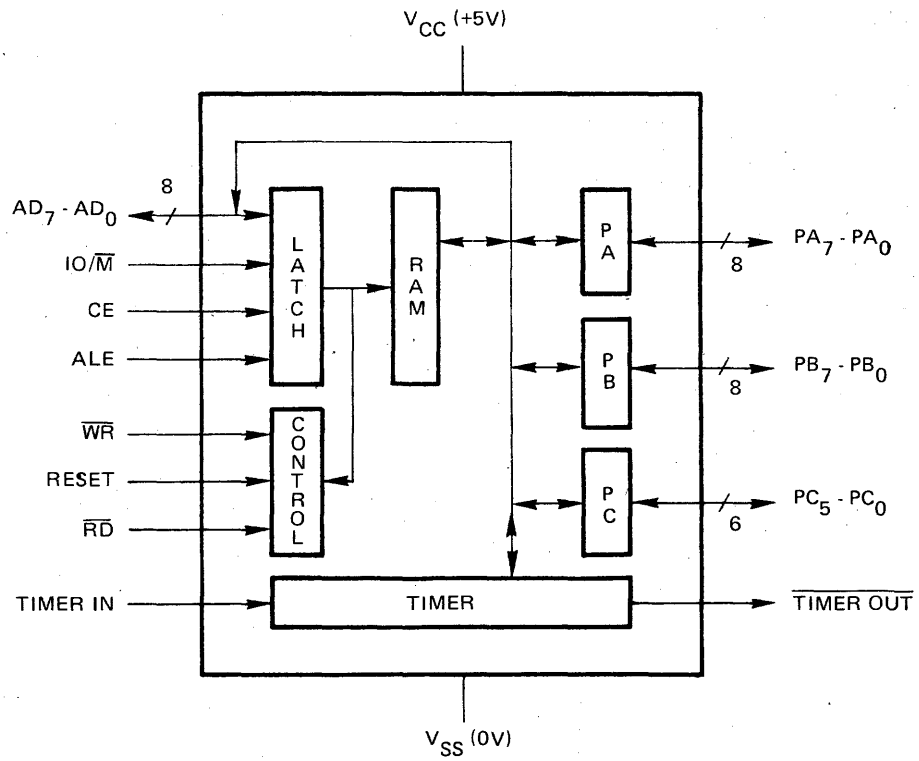
FUNCTIONAL DESCRIPTION

The μPD8155 and μPD8156 contain 2048 bits of Static RAM organized as 256 X 8. The 256 word memory location may be selected anywhere within the 64K memory space by using combinations of the upper 8 bits of address from the μPD8085A as a chip select.

The two general purpose 8-bit ports (PA and PB) may be programmed for input or output either in interrupt or status mode. The single 6-bit port (PC) may be used as control for PA and PB or general purpose input or output port. The μPD8155 and μPD8156 are programmed for their system personalities by writing into their Command/Status Registers (C/S) upon system initialization.

The timer is a single 14-bit down counter which is programmable for 4 modes of operation; see Timer Section.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	0°C to +70°C
Storage Temperature (Plastic Package)	-40°C to +125°C
Voltage on Any Pin	-0.3 to +7 Volts①
Power Dissipation	1.5 W

Note: ① With Respect to Ground.

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

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PIN IDENTIFICATION

PIN NO.	PIN SYMBOL	PIN NAME	FUNCTION
1, 2, 5 39, 38, 37	PC_3, PC_4, PC_5 PC_2, PC_1, PC_0	Port C	Used as control for PA and PB or as a 6-bit general purpose port
3	TIMER IN	Timer Clock In	Clock input to the 14-bit binary down counter
4	RESET	Reset In	From μPD8085A system reset to set PA, PB, PC to the input mode
6	$\overline{TIMER\ OUT}$	Timer Counter Output	The output of the timer function
7	IO/$\overline{M}$	I/O or Memory Indicator	Selects whether operation to and from the chip is directed to the internal RAM or to I/O ports
8	CE/$\overline{CE}$	Chip Enable	Chip Enable Input. Active low for μPD8155 and active high for μPD8156
9	$\overline{RD}$	Read Strobe	Causes Data Read
10	$\overline{WR}$	Write Strobe	Causes Data Write
11	ALE	Address Low Enable	Latches low order address in when valid
12-19	$AD_0 - AD_7$	Low Address/Data	3-State address/data bus to interface directly to μPD8085A
20	V_{SS}	Ground	Ground Reference
21-28	$PA_0 - PA_7$	Port A	General Purpose I/O Port
29-36	$PB_0 - PB_7$	Port B	General Purpose I/O Port
40	V_{CC}	5 Volt Input	Power Supply

DC CHARACTERISTICS

$T_a = 0°C$ to $+70°C$; $V_{CC} = 5V \pm 5\%$

PARAMETER		SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input Low Voltage		V_{IL}	-0.5		0.8	V	
Input High Voltage		V_{IH}	2.0		V_{CC}+0.5	V	
Output Low Voltage		V_{OL}			0.45	V	I_{OL} = 2 mA
Output High Voltage		V_{OH}	2.4			V	I_{OH} = 400 μA
Input Leakage		I_{IL}			±10	μA	$V_{IN} = V_{CC}$ to 0V
Output Leakage Current		I_{LO}			±10	μA	0.45V ≤ V_{OUT} ≤ V_{CC}
V_{CC} Supply Current		I_{CC}			180	mA	
Chip Enable Leakage	μPD8155	I_{IL} (CE)			+100	μA	$V_{IN} = V_{CC}$ to 0V
	μPD8156	I_{IL}(CE)			-100	μA	

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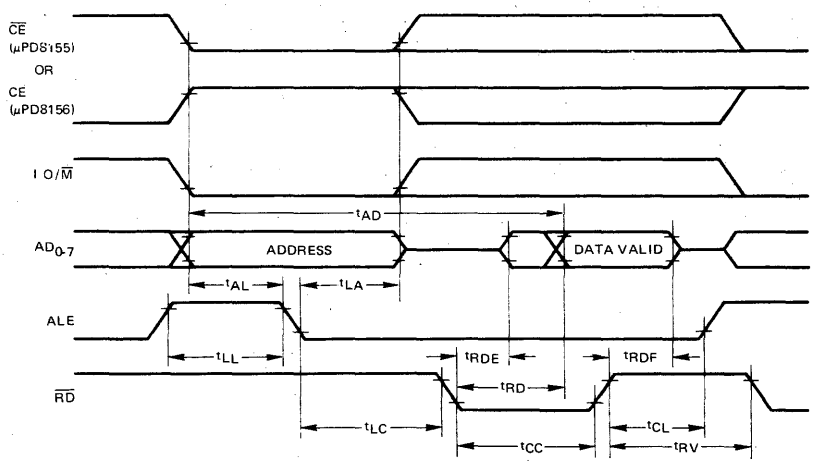
AC CHARACTERISTICS

T_a = 0°C to +70°C; V_{CC} = 5V ± 5%

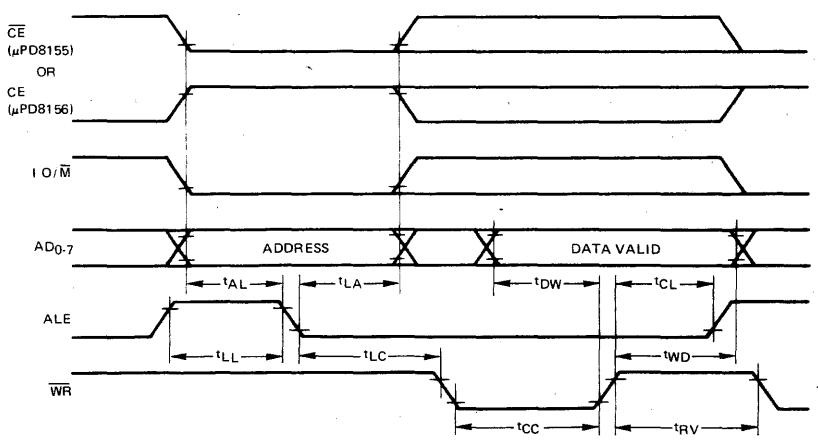
PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Address to Latch Set Up Time	t_{AL}	50			ns	150 pF Load
Address Hold Time after Latch	t_{LA}	80			ns	
Latch to READ/WRITE Control	t_{LC}	100			ns	
Valid Data Out Delay from READ Control	t_{RD}			170	ns	
Address Stable to Data Out Valid	t_{AD}			400	ns	
Latch Enable Width	t_{LL}	100			ns	
Data Bus Float After READ	t_{RDF}	0		100	ns	
READ/WRITE Control to Latch Enable	t_{CL}	20			ns	
READ/WRITE Control Width	t_{CC}	250			ns	
Data In to WRITE Set Up Time	t_{DW}	150			ns	
Data In Hold Time After WRITE	t_{WD}	0			ns	
Recovery Time Between Controls	t_{RV}	300			ns	
WRITE to Port Output	t_{WP}			400	ns	
Port Input Setup Time	t_{PR}	70			ns	
Port Input Hold Time	t_{RP}	50			ns	
Strobe to Buffer Full	t_{SBF}			400	ns	
Strobe Width	t_{SS}	200			ns	
READ to Buffer Empty	t_{RBE}			400	ns	
Strobe to INTR On	t_{SI}			400	ns	
READ to INTR Off	t_{RDI}			400	ns	
Port Setup Time to Strobe Strobe	t_{PSS}	50			ns	
Port Hold Time After Strobe	t_{PHS}	120			ns	
Strobe to Buffer Empty	t_{SBE}			400	ns	
WRITE to Buffer Full	t_{WBF}			400	ns	
WRITE to INTR Off	t_{WI}			400	ns	
TIMER-IN to $\overline{\text{TIMER-OUT}}$ Low	t_{TL}			400	ns	
TIMER-IN to $\overline{\text{TIMER-OUT}}$ High	t_{TH}			400	ns	
Data Bus Enable from READ Control	t_{RDE}	10			ns	

TIMING WAVEFORMS

READ CYCLE



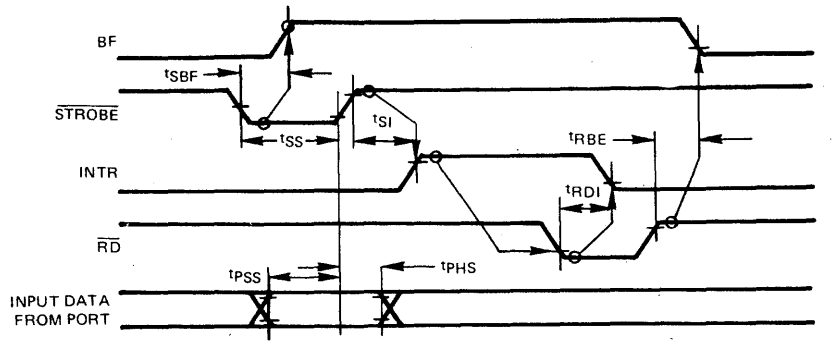
WRITE CYCLE



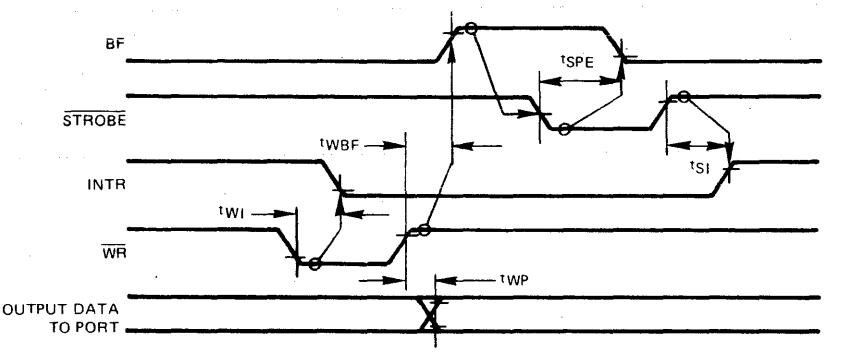
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TIMING WAVEFORMS (CONT.)

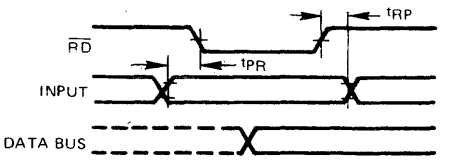
STROBED INPUT MODE



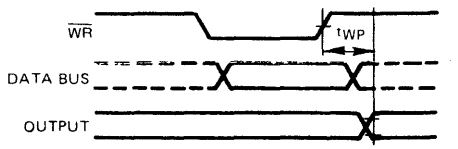
STROBED OUTPUT MODE



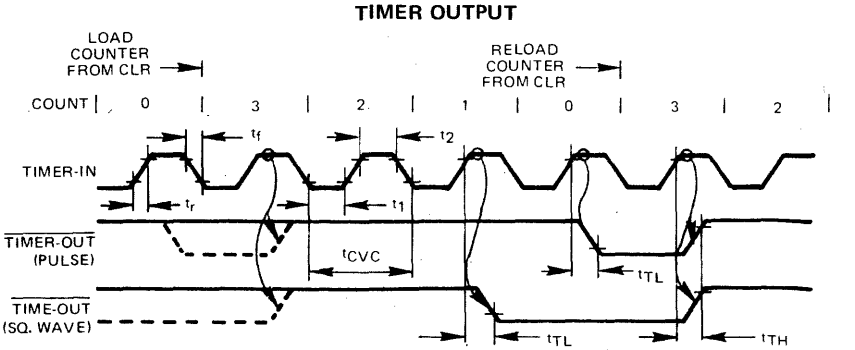
BASIC INPUT MODE



BASIC OUTPUT MODE



TIMER OUTPUT



COUNTDOWN FROM 3 TO 0

t_{CYC}	320 ns MIN.
t_{RISE} & t_{FALL}	30 ns MAX.
t_1	80 ns MIN.
t_2	120 ns MIN.
t_{TL}	TIMER-IN TO $\overline{\text{TIMER-OUT}}$ LOW (TO BE DEFINED).
t_{TH}	TIMER-IN TO $\overline{\text{TIMER-OUT}}$ HIGH (TO BE DEFINED).

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COMMAND STATUS REGISTER

The Command Status Register is an 8-bit register which must be programmed before the μPD8155/8156 may perform any useful functions. Its purpose is to define the mode of operation for the three ports and the timer. Programming of the device may be accomplished by writing to I/O address XXXXX000 (X denotes don't care) with a specific bit pattern. Reading of the Command Status Register can be accomplished by performing an I/O read operation at address XXXXX000. The pattern returned will be a 7-bit status report of PA, PB and the Timer. The bit patterns for the Command Status Register are defined as follows:

COMMAND STATUS WRITE

TM2	TM1	IEB	IEA	PC_2	PC_1	PB	PA

where:

TM2-TM1	Define Timer Mode
IEB	Enable Port B Interrupt
IEA	Enable Port A Interrupt
PC_2-PC_1	Define Port C Mode
PB/PA	Define Port B/A as In or Out ①

The Timer mode of operation is programmed as follows during command status write:

TM2	TM1	TIMER MODE
0	0	Don't Affect Timer Operation
0	1	Stop Timer Counting
1	0	Stop Counting after TC
1	1	Start Timer Operation

Interrupt enable status is programmed as follows:

IEB/IEA	INTERRUPT ENABLE PORT B/A
0	No
1	Yes

Port C may be placed in four possible modes of operation as outlined below. The modes are selected during command status write as follows:

PC_2	PC_1	PORT C MODE
0	0	ALT 1
0	1	ALT 3
1	0	ALT 4
1	1	ALT 2

The function of each pin of port C in the four possible modes is outlined as follows:

PIN	ALT 1	ALT 2	ALT 3 ②	ALT 4 ②
PC0	IN	OUT	A INTR	A INTR
PC1	IN	OUT	A BF	A BF
PC2	IN	OUT	A $\overline{STB}$	A $\overline{STB}$
PC3	IN	OUT	OUT	B INTR
PC4	IN	OUT	OUT	B BF
PC5	IN	OUT	OUT	B $\overline{STB}$

Notes: ① PB/PA Sets Port B/A Mode: 0 = Input; 1 = Output

② In ALT 3 and ALT 4 mode the control signals are initialized as follows:

CONTROL	INPUT	OUTPUT
$\overline{STB}$ (Input Strobe)	Input Control	Input Control
INTR (Interrupt Request)	Low	High
BF (Buffer Full)	Low	Low

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COMMAND STATUS REGISTER (CONT.)

COMMAND STATUS READ

	TI	INTE B	B BF	INTR B	INTE A	A BF	INTR A

Where the function of each bit is as follows:

TI	Defines a Timer Interrupt. Latched high at TC and reset after reading the CS register or starting a new count.
INTE B/A	Defines If Port B/A Interrupt is Enabled. High = enabled.
B/A BF	Defines If Port B/A Buffer is Full-Input Mode or Empty-Output Mode. High = active.
INTR B/A	Port B/A Interrupt Request. High = active.

The programming address summary for the status, ports, and timer are as follows:

I/O Address	Number of Bits	Function
XXXXX000	8	Command Status
XXXXX001	8	PA
XXXXX010	8	PB
XXXXX011	6	PC
XXXXX100	8	Timer-Low
XXXXX101	8	Timer-High

TIMER

The Internal Timer is a 14-bit binary down counter capable of operating in 4 modes. Its desired mode of operation is programmable at any time during operation. Any TTL clock meeting timer in requirements (See AC Characteristics) may be used as a time base and fed to the timer input. The timer output may be looped around and cause an interrupt or used as I/O control. The operational modes are defined as follows and programmed along with the 6 high bits of timer data.

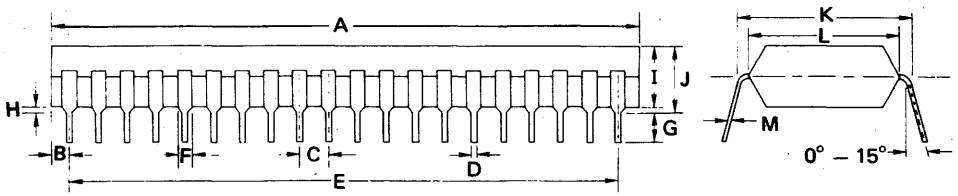
M2	M1	Operation
0	0	High at Start, Low During Second Half of Count
0	1	Square Wave (Period = Count Length, Auto Reload at TC)
1	0	Single Pulse at TC
1	1	Single Pulse at TC with Auto Reload

Programming the timer requires two words to be written to the μPD8155/8156 at I/O address XXXXX100 and XXXXX101 for the low and high order bytes respectively. Valid count length must be between 2_H and $3FFF_H$. The bit assignments for the high and low programming words are as follows:

Word	Bit Pattern								I/O Address
High Byte	M_2	M_1	T13	T12	T11	T10	T9	T8	XXXXX101
Low Byte	T7	T6	T5	T4	T3	T2	T1	T0	XXXXX100

The control of the timer is performed by TM2 and TM1 of the Command Status Word.

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PACKAGE OUTLINE
μPD8155C
μPD8156C

Plastic

ITEM	MILLIMETERS	INCHES
A	51.5 MAX	2.028 MAX
B	1.62	0.064
C	2.54 ± 0.1	0.10 ± 0.004
D	0.5 ± 0.1	0.019 ± 0.004
E	48.26	1.9
F	1.2 MIN	0.047 MIN
G	2.54 MIN	0.10 MIN
H	0.5 MIN	0.019 MIN
I	5.22 MAX	0.206 MAX
J	5.72 MAX	0.225 MAX
K	15.24	0.600
L	13.2	0.520
M	$0.25^{+0.1}_{-0.05}$	$0.010^{+0.004}_{-0.002}$

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EIGHT-BIT INPUT/OUTPUT PORT

DESCRIPTION

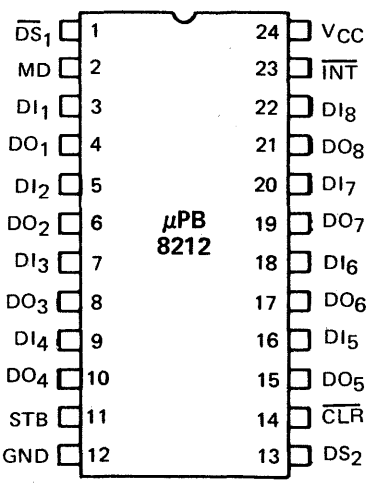
The μPB8212 input/output port consists of an 8-bit latch with three-state output buffers along with control and device selection logic. Also included is a service request flip-flop for the control and generation of interrupts to the microprocessor.

The device is multimode in nature and can be used to implement latches, gated buffers or multiplexers. Thus, all of the principal peripheral and input/output functions of a microcomputer system can be implemented with this device.

FEATURES

- Fully Parallel 8-Bit Data Register and Buffer
- Service Request Flip-Flop for Interrupt Generation
- Low Input Load Current – 0.25 mA Max.
- Three State Outputs
- Outputs Sink 15 mA
- 3.65V Output High Voltage for Direct Interface to 8080A Processor
- Asynchronous Register Clear
- Replaces Buffers, Latches and Multiplexers in Microcomputer Systems
- Reduces System Package Count
- Available in 24-pin Plastic and Cerdip Packages

PIN CONFIGURATION



PIN NAMES

$DI_1 - DI_8$	Data In
$DO_1 - DO_8$	Data Out
$\overline{DS_1}, DS_2$	Device Select
MD	Mode
STB	Strobe
$\overline{INT}$	Interrupt (Active Low)
$\overline{CLR}$	Clear (Active Low)

Rev/1

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FUNCTIONAL DESCRIPTION

Data Latch

The 8 flip-flops that compose the data latch are of a "D" type design. The output (Q) of the flip-flop follows the data input (D) while the clock input (C) is high. Latching occurs when the clock (C) returns low.

The data latch is cleared by an asynchronous reset input ($\overline{CLR}$).
(Note: Clock (C) Overrides Reset ($\overline{CLR}$).)

Output Buffer

The output of the data latch (Q) are connected to three-state, non-inverting output buffers. These buffers have a common control line (EN); enabling the buffer to transmit the data from the outputs of the data latch (Q) or disabling the buffer, forcing the output into a high impedance state (three-state).

This high-impedance state allows the designer to connect the μPB8212 directly to the microprocessor bi-directional data bus.

Control Logic

The μPB8212 has four control inputs: $\overline{DS}_1$, DS_2, MD and STB. These inputs are employed to control device selection, data latching, output buffer state and the service request flip-flop.

$\overline{DS}_1$, DS_2 (Device Select)

These two inputs are employed for device selection. When $\overline{DS}_1$ is low and DS_2 is high ($\overline{DS}_1 \cdot DS_2$) the device is selected. In the selected state the output buffer is enabled and the service request flip-flop (SR) is asynchronously set.

Service Request Flip-Flop (SR)

The (SR) flip-flop is employed to generate and control interrupts in microcomputer systems. It is asynchronously set by the $\overline{CLR}$ input (active low). When the (SR) flip-flop is set it is in the non-interrupting state.

The output (Q) of the (SR) flip-flop is connected to an inverting input of a "NOR" gate. The other input of the "NOR" gate is non-inverting and is connected to the device selection logic ($\overline{DS}_1 \cdot DS_2$). The output of the "NOR" gate ($\overline{INT}$) is active low (interrupting state) for connection to active low input priority generating circuits.

MD (Mode)

This input is employed to control the state of the output buffer and to determine the source of the clock input (C) to the data latch.

When MD is in the output mode (high) the output buffers are enabled and the source of clock (C) to the data latch is from the device selection logic ($\overline{DS}_1 \cdot DS_2$).

When MD is in the input mode (low) the output buffer state is determined by the device selection logic ($\overline{DS}_1 \cdot DS_2$) and the source of clock (C) to the data latch is the STB (Strobe) input.

STB (Strobe)

STB is employed as the clock (C) to the data latch for the input mode (MD = 0) and to synchronously reset the service request flip-flop (SR).

Note that the SR flip-flop triggers on the negative edge of STB which overrides $\overline{CLR}$.

ABSOLUTE MAXIMUM RATINGS*

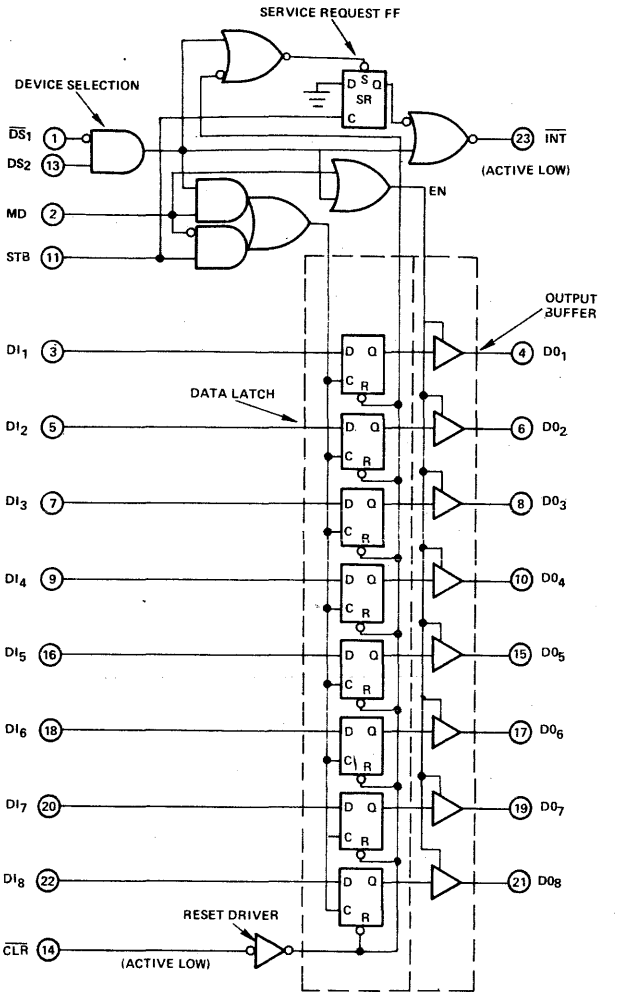
Operating Temperature	0°C to +70°C
Storage Temperature	−65°C to +150°C
All Output or Supply Voltages	−0.5 to +7 Volts
All Input Voltages	−1.0 to +5.5 Volts
Output Currents	125 mA

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

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BLOCK DIAGRAM



STB	MD	$(\overline{DS_1} \cdot DS_2)$	DATA OUT EQUALS
0	0	0	Three-State
1	0	0	Three-State
0	1	0	Data Latch
1	1	0	Data Latch
0	0	1	Data Latch
1	0	1	Data In
0	1	1	Data In
1	1	1	Data In

$\overline{CLR}$	$(\overline{DS_1} \cdot DS_2)$	STB	SR ②	$\overline{INT}$
0	0	0	1	1
0	1	0	1	0
1	0	0	③	③
1	↘	0	1	1
1	0	↘	0	0
1	1	0	1	0
1	1	↘	0	0

Notes: ① $\overline{CLR}$ resets data latch sets SR flip-flop. (No effect on output buffer)
② Internal SR flip-flop
③ Previous data remains

DC CHARACTERISTICS

$T_a = 0°C$ to $70°C$; $V_{CC} = +5V \pm 5\%$

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input Load Current ACK, DS_2, CR, $DI_1 - DI_8$ Inputs	I_F		−0.14	−0.25	mA	$V_F = 0.45V$
Input Load Current MD Input	I_F		−0.25	−0.75	mA	$V_F = 0.45V$
Input Load Current $\overline{DS_1}$ Input	I_F		−0.26	−1.0	mA	$V_F = 0.45V$
Input Leakage Current ACK, DS, CR, $DI_1 - DI_8$ Inputs	I_R			10	μA	$V_R = 5.25V$
Input Leakage Current MD Input	I_R			30	μA	$V_R = 5.25V$
Input Leakage Current $\overline{DS_1}$ Input	I_R			40	μA	$V_R = 5.25V$
Input Forward Voltage Clamp	V_C		−0.85	−1.3	V	$I_C = -5$ mA
Input "Low" Voltage	V_{IL}			0.85	V	
Input "High" Voltage	V_{IH}	2.0			V	
Output "Low" Voltage	V_{OL}		0.26	0.45	V	$I_{OL} = 15$ mA
Output "High" Voltage	V_{OH}	3.65	4.0		V	$I_{OH} = -1$ mA
Short Circuit Output Current	I_{SC}	−15	−38	−75	mA	$V_O = 0V$
Output Leakage Current High Impedance State	I_O			20	μA	$V_O = 0.45V/5.25V$
Power Supply Current	I_{CC}		103	130	mA	

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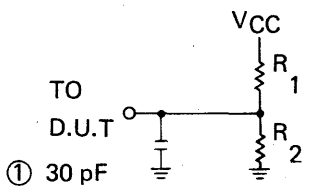
AC CHARACTERISTICS

T_a = 0°C to +70°C; V_{CC} = +5V ± 5%

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Pulse Width	t_{pw}	30			ns	Input Pulse Amplitude = 2.5V
Data To Output Delay	t_{pd}		20	30	ns	
Write Enable To Output Delay	t_{we}			40	ns	Input Rise and Fall Times = 5 ns
Data Setup Time	t_{set}	15			ns	
Data Hold Time	t_h	20			ns	Between 1V and 2V
Reset to Output Delay	t_r			40	ns	Measurement made at 1.5V with 15 mA and 30 pF Test Load
Set To Output Delay	t_s			30	ns	
Output Enable/Disable Time	t_e/t_d			45	ns	①
Clear To Output Delay	t_c			55	ns	②

Notes: ① R_1 = 300Ω/10KΩ; R_2 = 600Ω/1KΩ

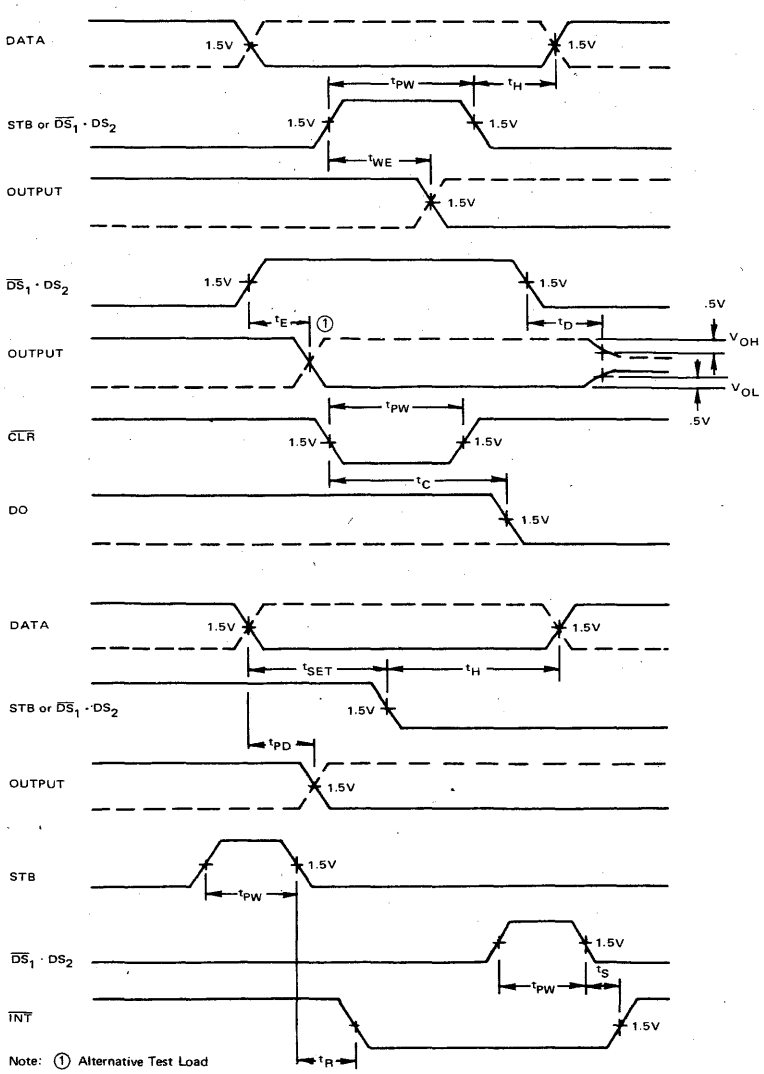
② R_1 = 300Ω; R_2 = 600Ω



TEST CIRCUIT

Note: ① Including Jig and Probe Capacitance

TIMING WAVEFORMS



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CAPACITANCE ①

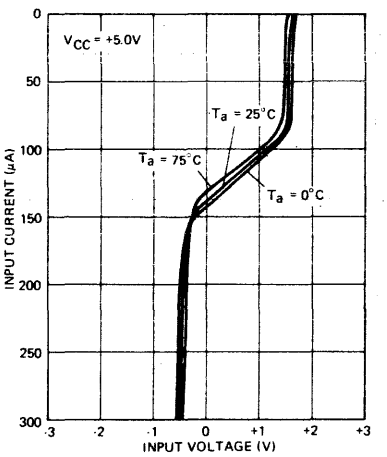
$T_a = 25°C$; $V_{CC} = +5V$; $V_{BIAS} = 2.5V$; f = 1 MHz

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input Capacitance	C_{IN}		7	12	pF	$\overline{DS}_1$, MD
Input Capacitance	C_{IN}		4	9	pF	DS_2, CLR, STB, $DI_1 - DI_8$
Output Capacitance	C_{OUT}		6	12	pF	$DO_1 - DO_8$

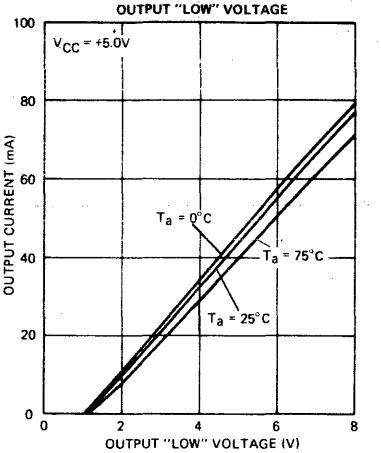
Note: ① This parameter is periodically sampled and not 100% tested

TYPICAL CHARACTERISTICS

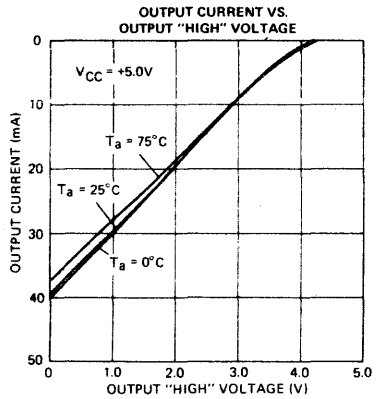
INPUT CURRENT VS. INPUT VOLTAGE



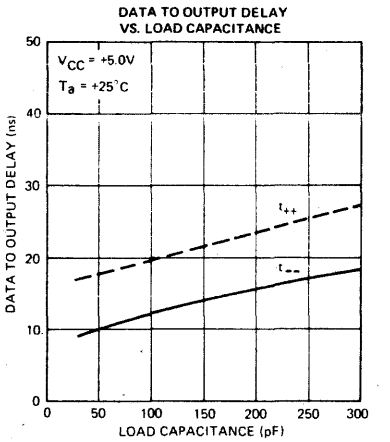
OUTPUT CURRENT VS. OUTPUT "LOW" VOLTAGE



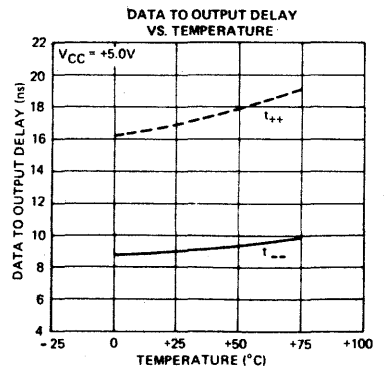
OUTPUT CURRENT VS. OUTPUT "HIGH" VOLTAGE



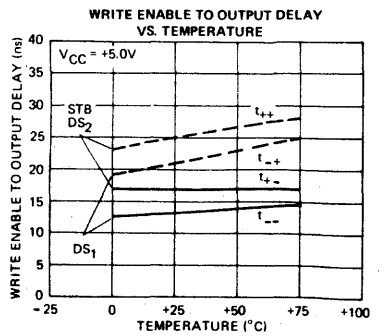
DATA TO OUTPUT DELAY VS. LOAD CAPACITANCE



DATA TO OUTPUT DELAY VS. TEMPERATURE

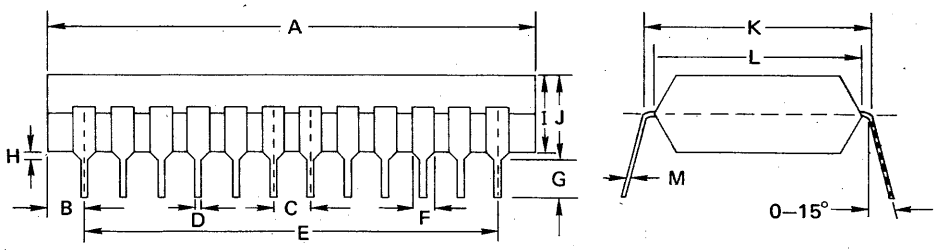


WRITE ENABLE TO OUTPUT DELAY VS. TEMPERATURE



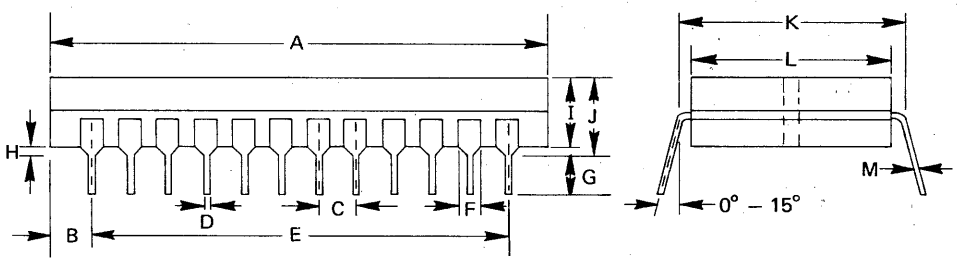
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PACKAGE OUTLINE
μPB8212C/D



μPB8212C (Plastic)

ITEM	MILLIMETERS	INCHES
A	33 MAX	1.3 MAX
B	2.53	0.1
C	2.54	0.1
D	0.5 ± 0.1	0.02 ± 0.004
E	27.94	1.1
F	1.5	0.059
G	2.54 MIN	0.1 MIN
H	0.5 MIN	0.02 MIN
I	5.22 MAX	0.205 MAX
J	5.72 MAX	0.225 MAX
K	15.24	0.6
L	13.2	0.52
M	$0.25^{+0.10}_{-0.05}$	$0.01^{+0.004}_{-0.0019}$



μPB8212D (Cerdip)

ITEM	MILLIMETERS	INCHES
A	33.5 MAX.	1.32 MAX.
B	2.78	0.11
C	2.54	0.1
D	0.46	0.018
E	27.94	1.1
F	1.5	0.059
G	2.54 MIN.	0.1 MIN.
H	0.5 MIN.	0.019 MIN.
I	4.58 MAX.	0.181 MAX.
J	5.08 MAX.	0.2 MAX.
K	15.24	0.6
L	13.5	0.53
M	$0.25^{+0.10}_{-0.05}$	$0.01^{+0.004}_{-0.002}$

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PRIORITY INTERRUPT CONTROLLER

DESCRIPTION

The μPB8214 is an eight-level priority interrupt controller. Designed to simplify interrupt driven microcomputer systems, the μPB8214 requires a single +5V power supply and is packaged in a 24 pin plastic Dual-in-line package.

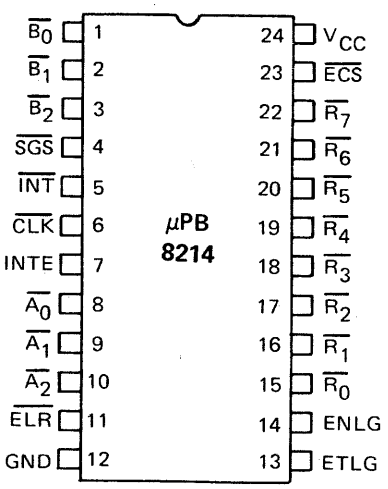
The μPB8214 accepts up to eight interrupts, determines which has the highest priority and then compares that priority with a software created current status register. If the incoming requires is of a higher priority than the interrupt currently being serviced, an interrupt request to the processor is generated. Vector information that identifies the interrupting device is also generated.

The interrupt structure of the microcomputer system can be expanded beyond eight interrupt levels by cascading μPB8214s. The μPB8214's interrupt and vector information outputs are open collector and control signals are provided to simplify expansion of the interrupt structure.

FEATURES

- Eight Priority Levels
- Current Status Register and Priority Comparator
- Easily Expanded Interrupt Structure
- Single +5 Volt Supply

PIN CONFIGURATION

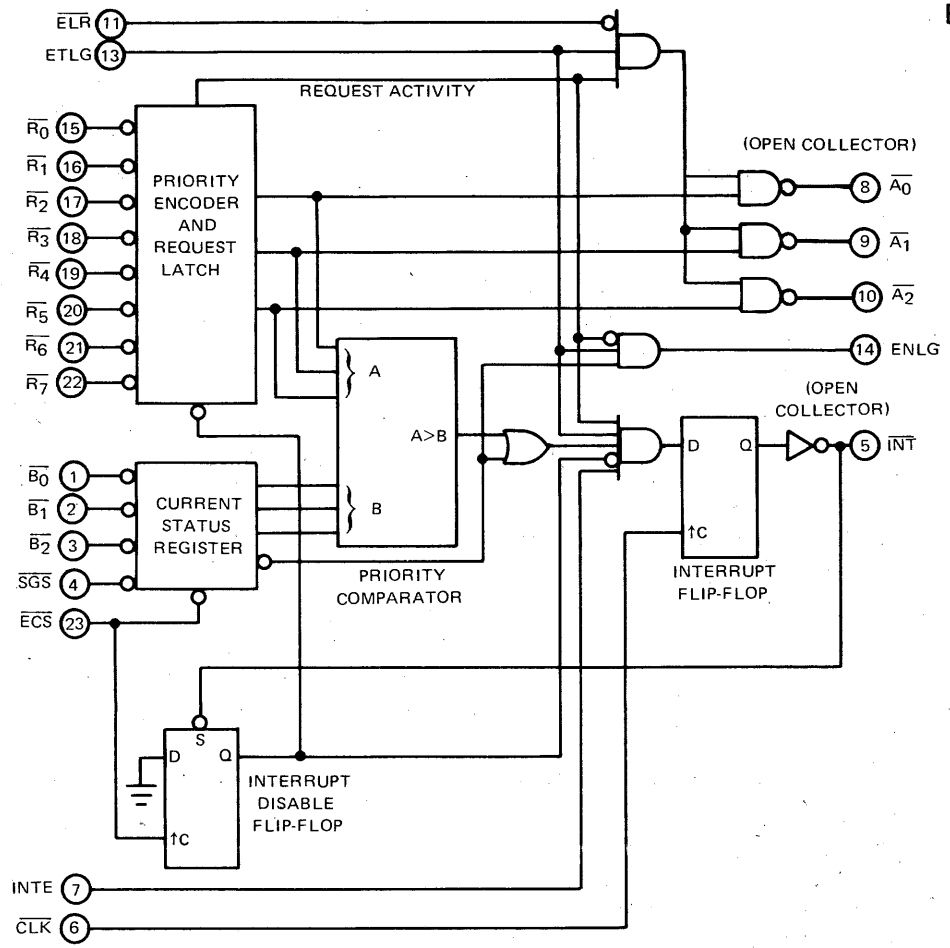


PIN NAMES

Inputs:		
$\overline{R_0}$–$\overline{R_7}$	Request Levels ($\overline{R_7}$ Highest Priority)	
$\overline{B_0}$–$\overline{B_2}$	Current Status	
$\overline{SGS}$	Status Group Select	
$\overline{ECS}$	Enable Current Status	
INTE	Interrupt Enable	
$\overline{CLK}$	Clock (INT F-F)	
$\overline{ELR}$	Enable Level Read	
ETLG	Enable This Level Group	
Outputs:		
$\overline{A_0}$–$\overline{A_2}$	Request Levels	Open
$\overline{INT}$	Interrupt (Act. Low)	Collector
ENLG	Enable Next Level Group	

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BLOCK DIAGRAM



FUNCTIONAL DESCRIPTION

General

The μPB8214 is an LSI device designed to simplify the circuitry required to implement an interrupt driven microcomputer system. Up to eight interrupting devices can be connected to a μPB8214, which will assign priority to incoming interrupt requests and accept the highest. It will also compare the priority of the highest incoming request with the priority of the interrupt being serviced. If the serviced interrupt has a higher priority, the incoming request will not be accepted.

A system with more than eight interrupting devices can be implemented by interconnecting additional μPB8214s. In order to facilitate this expansion, control signals are provided for cascading the controllers so that there is a priority established among the controllers. In addition, the interrupt and vector information outputs are open collector.

Priority Encoder and Request Latch

The priority encoder portion of the μPB8214 accepts up to eight active low interrupt requests ($\overline{R_0}$–$\overline{R_7}$). The circuit assigns priority to the incoming requests, with $\overline{R_7}$ having the highest priority and $\overline{R_0}$ the lowest. If two or more requests occur simultaneously, the μPB8214 accepts the one having the highest priority. Once an incoming interrupt request is accepted, it is stored by the request latch and a three-bit code is output. As shown in the following table, the outputs, ($\overline{A_0}$–$\overline{A_2}$) are the complement of the request level (modulo 8) and directly correspond to the bit pattern required to generate the one byte RESTART (RST) instructions recognized by an 8080A. Simultaneously with the $\overline{A_0}$–$\overline{A_2}$ outputs, a system interrupt request ($\overline{INT}$) is output by the μPB8214. It should be noted that incoming interrupt requests that are *not* accepted are not latched and must remain as an input to the μPB8214 in order to be serviced.

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FUNCTIONAL DESCRIPTION (CONT.)

RESTART GENERATION TABLE

PRIORITY REQUEST		RST	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
			1	1	$\overline{A_2}$	$\overline{A_1}$	$\overline{A_0}$	1	1	1
LOWEST	$\overline{R_0}$	7	1	1	1	1	1	1	1	1
	$\overline{R_1}$	6	1	1	1	1	0	1	1	1
	$\overline{R_2}$	5	1	1	1	0	1	1	1	1
	$\overline{R_3}$	4	1	1	1	0	0	1	1	1
	$\overline{R_4}$	3	1	1	0	1	1	1	1	1
	$\overline{R_5}$	2	1	1	0	1	0	1	1	1
	$\overline{R_6}$	1	1	1	0	0	1	1	1	1
HIGHEST	$\overline{R_7}$	0*	1	1	0	0	0	1	1	1

*CAUTION: RST 0 will vector the program counter to location 0 (zero) and invoke the same routine as the "RESET" input to 8080A.

Current Status Register

The current status register is designed to prevent an incoming interrupt request from overriding the servicing of an interrupt with higher priority. Via software, the priority level of the interrupt being serviced by the microprocessor is written into the current status register on $\overline{B_0}$–$\overline{B_2}$. The bit pattern written should be the complement of the interrupt level.

The interrupt level currently being serviced is written into the current status register by driving $\overline{ECS}$ (Enable Current Status) low. The μPB8214 will only accept interrupts with a higher priority than the value contained by the current status register. Note that the programmer is free to use the current status register for other than as above. Other levels may be written into it. The comparison may be completely disabled by driving $\overline{SGS}$ (Status Group Select) low when $\overline{ECS}$ is driven low. This will cause the μPB8214 to accept incoming interrupts only on the basis of their priority to each other.

Priority Comparator

The priority comparator circuitry compares the level of the interrupt accepted by the priority encoder and request latch with the contents of the current status register. If the incoming request has a priority level higher than that of the current status register, the $\overline{INT}$ output is enabled. Note that this comparison can be disabled by loading the current status register with $\overline{SGS}$=0.

Expansion Control Signals

A microcomputer design may often require more than eight different interrupts. The μPB8214 is designed so that interrupt system expansion is easily performed via the use of three signals: ETLG (Enable This Level Group); ENLG (Enable Next Level Group); and $\overline{ELR}$ (Enable Level Read). A high input to ETLG indicates that the μPB8214 may accept an interrupt. In a typical system, the ENLG output from one μPB8214 is connected to the ETLG input of another μPB8214, etc. The ETLG of the μPB8214 with the highest priority is tied high. This configuration sets up priority among the cascaded μPB8214's. The ENLG output will be high for any device that does not have an interrupt pending, thereby allowing a device with lower priority to accept interrupts. The $\overline{ELR}$ input is basically a chip enable and allows hardware or software to selectively disable/enable individual μPB8214's. A low on the $\overline{ELR}$ input enables the device.

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FUNCTIONAL DESCRIPTION (CONT.)

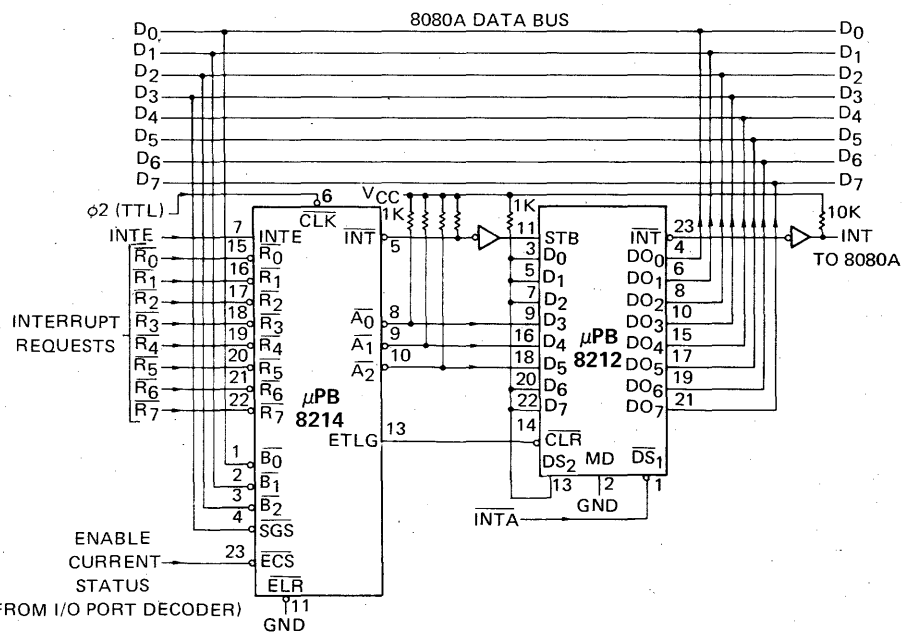
Interrupt Control Circuitry

The μPB8214 contains two flip-flops and several gates which determine whether an accepted interrupt request to the μPB8214 will generate a system interrupt to the 8080A. A condition gate drives the D input of the interrupt flip-flop whenever an interrupt request has been completely accepted. This requires that: the ETLG (Enable This Level Group) and INTE (Interrupt Enable) inputs to the μPB8214 are high; the $\overline{ELR}$ input is low; the incoming request must be of a higher priority than the contents of the current status register; and the μPB8214 must have been enabled to accept interrupt requests by the clearing of the interrupt disable flip-flop.

Once the condition gate drives the D input of the interrupt flip-flop high, a system interrupt ($\overline{INT}$) to the 8080A is generated on the next rising edge of the $\overline{CLK}$ input to the μPB8214. This $\overline{CLK}$ input is typically connected to the $\phi 2$ (TTL) output of an 8224 so that 8080A set-up time specifications are met. When $\overline{INT}$ is generated, it sets the interrupt disable flip-flop so that no additional system interrupts will be generated until it is reset. It is reset by driving $\overline{ECS}$ (Enable Current Status) low, thereby writing into the current status register.

It should be noted that the open collector $\overline{INT}$ output from the μPB8214 is active for only one clock period and thus must be externally latched for inputting to the 8080A. Also, because the $\overline{INT}$ output is open collector, when μPB8214's are cascaded, an $\overline{INT}$ output from any one will set all of the interrupt disable flip-flops in the array. Each μPB8214's interrupt disable flip-flop must then be cleared individually in order to generate subsequent system interrupts.

TYPICAL μPB8214 CIRCUITRY



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	0°C to +70°C
Storage Temperature	−65°C to +125°C
All Output and Supply Voltages	−0.5 to +7 Volts
All Input Voltages	−1.0 to +5.5 Volts
Output Currents	100 mA

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

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DC CHARACTERISTICS $T_a = 0°C$ to $+70°C$, $V_{CC} = 5V \pm 5\%$

PARAMETER	SYMBOL	LIMITS MIN.	LIMITS TYP.①	LIMITS MAX.	UNIT	TEST CONDITIONS
Input Clamp Voltage (all inputs)	V_C			-1.0	V	I_C=-5mA
Input Forward Current: ETLG input	I_F		-.15	-0.5	mA	V_F=0.45V
all other inputs			-.08	-0.25	mA	
Input Reverse Current: ETLG input	I_R			80	μA	V_R=5.25V
all other inputs				40	μA	
Input LOW Voltage: all inputs	V_{IL}			0.8	V	V_{CC}=5.0V
Input HIGH Voltage: all inputs	V_{IH}	2.0			V	V_{CC}=5.0V
Power Supply Current	I_{CC}		90	130	mA	②
Output LOW Voltage: all outputs	V_{OL}		.3	.45	V	I_{OL}=10mA
Output HIGH Voltage: ENLG output	V_{OH}	2.4	3.0		V	I_{OH}=-1mA
Short Circuit Output Current: ENLG output	I_{OS}	-20	-35	-55	mA	V_{OS}=0V, V_{CC}=5.0V
Output Leakage Current: $\overline{INT}$ and $\overline{A_0}$–$\overline{A_2}$	I_{CEX}			100	μA	V_{CEX}=5.25V

CAPACITANCE ③ $T_a = 25°C$

PARAMETER	SYMBOL	LIMITS MIN.	LIMITS TYP.①	LIMITS MAX.	UNIT	TEST CONDITIONS
Input Capacitance	C_{IN}		5	10	pF	V_{BIAS}=2.5V
Output Capacitance	C_{OUT}		7	12	pF	V_{CC}=5V f=1mHz

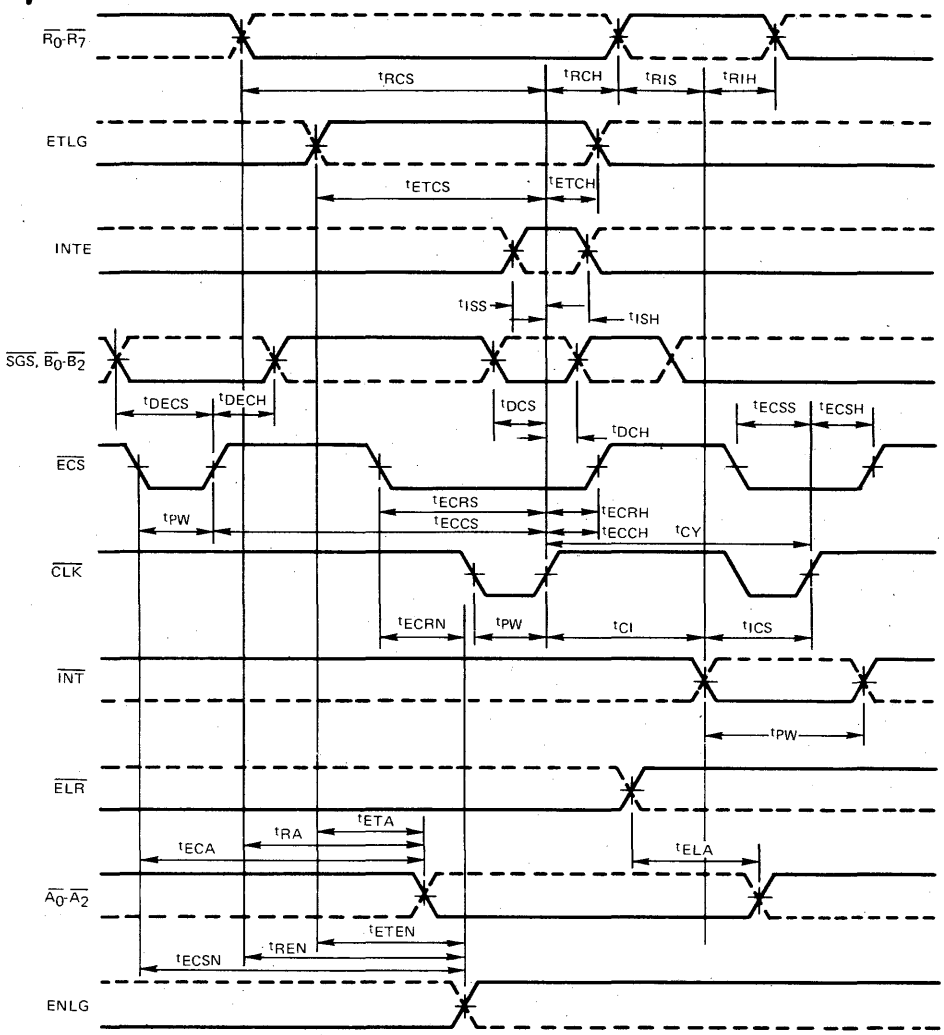
AC CHARACTERISTICS $T_a = 0°C$ to $+70°C$, $V_{CC} = +5V \pm 5\%$

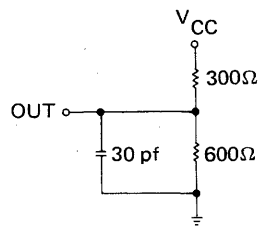
PARAMETER	SYMBOL	LIMITS MIN.	LIMITS TYP.①	LIMITS MAX.	UNIT	TEST CONDITIONS
$\overline{CLK}$ Cycle Time	t_{CY}	80	50		ns	Input pulse
$\overline{CLK}$, $\overline{ECS}$, $\overline{INT}$ Pulse Width	t_{PW}	25	15		ns	amplitude: 2.5 Volts
INTE Setup Time to $\overline{CLK}$	t_{ISS}	16	12		ns	
INTE Hold Time after $\overline{CLK}$	t_{ISH}	20	10		ns	
ETLG Setup Time to $\overline{CLK}$	t_{ETCS}④	25	12		ns	Input rise and fall
ETLG Hold Time After $\overline{CLK}$	t_{ETCH}④	20	10		ns	times: 5 ns between
$\overline{ECS}$ Setup Time to $\overline{CLK}$	t_{ECCS}④	80	50		ns	1 and 2 Volts
$\overline{ECS}$ Hold Time After $\overline{CLK}$	t_{ECCH}⑤	0			ns	
$\overline{ECS}$ Setup Time to $\overline{CLK}$	t_{ECRS}⑤	110	70		ns	
$\overline{ECS}$ Hold Time After $\overline{CLK}$	t_{ECRH}⑤	0				Output loading of
$\overline{ECS}$ Setup Time to $\overline{CLK}$	t_{ECSS}④	75	70		ns	15 mA and 30 pF.
$\overline{ECS}$ Hold Time After $\overline{CLK}$	t_{ECSH}④	0			ns	
$\overline{SGS}$ and $\overline{B_0}$–$\overline{B_2}$ Setup Time to $\overline{CLK}$	t_{DCS}④	70	50		ns	
$\overline{SGS}$ and $\overline{B_0}$–$\overline{B_2}$ Hold Time After $\overline{CLK}$	t_{DCH}④	0			ns	Speed measurements
$\overline{R_0}$–$\overline{R_7}$ Setup Time to $\overline{CLK}$	t_{RCS}⑤	90	55		ns	taken at the 1.5 Volts
$\overline{R_0}$–$\overline{R_7}$ Hold Time After $\overline{CLK}$	t_{RCH}⑤	0			ns	levels.
$\overline{INT}$ Setup Time to $\overline{CLK}$	t_{ICS}	55	35		ns	
$\overline{CLK}$ to $\overline{INT}$ Propagation Delay	t_{CI}		15	25	ns	
$\overline{R_0}$–$\overline{R_7}$ Setup Time to $\overline{INT}$	t_{RIS}⑥	10	0		ns	
$\overline{R_0}$–$\overline{R_7}$ Hold Time After $\overline{INT}$	t_{RIH}⑥	35	20		ns	
$\overline{R_0}$–$\overline{R_7}$ to $\overline{A_0}$–$\overline{A_2}$ Propagation Delay	t_{RA}		80	100	ns	
$\overline{ELR}$ to $\overline{A_0}$–$\overline{A_2}$ Propagation Delay	t_{ELA}		40	55	ns	
$\overline{ECS}$ to $\overline{A_0}$–$\overline{A_2}$ Propagation Delay	t_{ECA}		100	120	ns	
ETLG to $\overline{A_0}$–$\overline{A_2}$ Propagation Delay	t_{ETA}		35	70	ns	
$\overline{SGS}$ and $\overline{B_0}$–$\overline{B_2}$ Setup Time to $\overline{ECS}$	t_{DECS}⑥	15	10		ns	
$\overline{SGS}$ and $\overline{B_0}$–$\overline{B_2}$ Hold Time After $\overline{ECS}$	t_{DECH}⑥	15	10		ns	
$\overline{R_0}$–$\overline{R_7}$ to ENLG Propagation Delay	t_{REN}		45	70	ns	
ELTG to ENLG Propagation Delay	t_{ETEN}		20	25	ns	
$\overline{ECS}$ to ENLG Propagation Delay	t_{ECRN}		85	90	ns	
$\overline{ECS}$ to ENLG Propagation Delay	t_{ECSN}		35	55	ns	

Notes:
① Typical values are for T_a=25°C, V_{CC}=5.0V
② $\overline{B_0}$–$\overline{B_2}$, $\overline{SGS}$, $\overline{CLK}$, $\overline{R_0}$–$\overline{R_4}$ grounded, all other inputs and all outputs open.
③ This parameter is periodically sampled and not 100% tested.
④ Required for proper operation if INTE is enabled during next clock pulse.
⑤ These times are not required for proper operation but for desired change in interrupt flip-flop.
⑥ Required for new request or status to be properly loaded.

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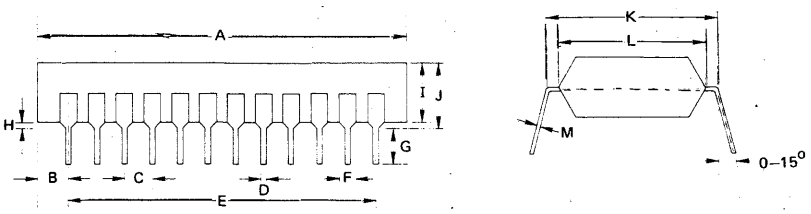
TIMING WAVEFORMS





TEST CIRCUIT

PACKAGE OUTLINE μPB8214C



ITEM	MILLIMETERS	INCHES
A	33 MAX.	1.28
B	2.53	0.1
C	2.54	0.1
D	0.5 ± 0.1	0.02 ± 0.004
E	27.94	1.1
F	1.5	0.059
G	3.2 MIN.	0.125 MIN.
H	0.5 MIN.	0.02 MIN.
I	5.22 MAX.	0.205 MAX.
J	5.72 MAX.	0.225 MAX.
K	15.24	0.6
L	13.2	0.52
M	0.25 ± 0.1	0.01 ± 0.004

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4 BIT PARALLEL BIDIRECTIONAL BUS DRIVER

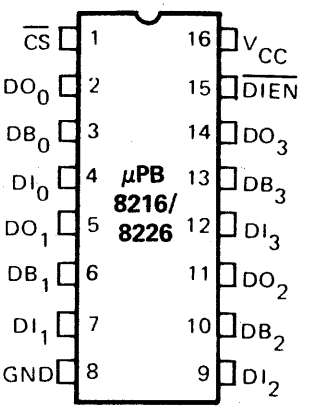
DESCRIPTION

All inputs are low power TTL compatible. For driving MOS, the DO outputs provide a high 3.65V (V_{OH}), and for high capacitance terminated bus structures, the DB outputs provide a high 55 mA (I_{OL}) capability.

FEATURES

- Data Bus Buffer Driver for μCOM-8 Microprocessor Family
- Low Input Load Current – 0.25 mA Maximum
- High Output Drive Capability for Driving System Data Bus
- 3.65V Output High Voltage for Direct Interface to μCOM-8 Microprocessor Family
- Three State Outputs
- Reduces System Package Count
- Available in 16 pin packages: Cerdip and Plastic

PIN CONFIGURATION



PIN NAMES

$DB_0 - DB_3$	Data Bus Bi-Directional
$DI_0 - DI_3$	Data Input
$DO_0 - DO_3$	Data Output
$\overline{DIEN}$	Data in Enable Direction Control
$\overline{CS}$	Chip Select

Rev/2

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μPB8216/8226

FUNCTIONAL DESCRIPTION

Microprocessors like the μPD8080A are MOS devices and are generally capable of driving a single TTL load. This also applies to MOS memory devices. This type of drive is sufficient for small systems with a few components, but often it is necessary to buffer the microprocessor and memories when adding components or expanding to a multi-board system.

The μPD8216/8226 is a four bit bi-directional bus driver specifically designed to buffer microcomputer system components.

Bi-Directional Driver

Each buffered line of the four bit driver consists of two separate buffers. They are three state in nature to achieve direct bus interface and bi-directional capability. On one side of the driver the output of one buffer and the input of another are tied together (DB), this is used to interface to the system side components such as memories, I/O, etc. Its interface is directly TTL compatible and it has high drive (55 mA). For maximum flexibility on the other side of the driver the inputs and outputs are separate. They can be tied together so that the driver can be used to buffer a true bi-directional bus such as the 8080A Data Bus. The DO outputs on this side of the driver have a special high voltage output drive capability (3.65V) so that direct interface to the 8080A processor is achieved with an adequate amount of noise immunity (650 mV worst case).

Control Gating $\overline{CS}$, $\overline{DIEN}$

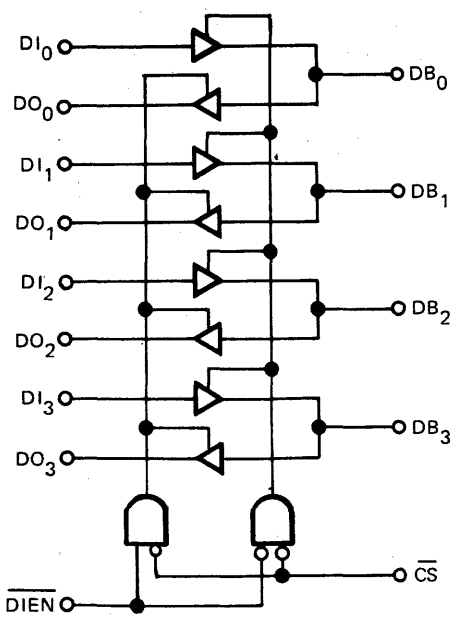
The $\overline{CS}$ input is used for device selection. When $\overline{CS}$ is "high" the output drivers are all forced to their high-impedance state. When it is "low" the device is selected (enabled) and the data flow direction is determined by the $\overline{DIEN}$ input.

The $\overline{DIEN}$ input controls the data flow direction (see Block Diagrams for complete truth table). This directional control is accomplished by forcing one of the pair of buffers to its high impedance state. This allows the other to transmit its data. This is accomplished by a simple two gate circuit.

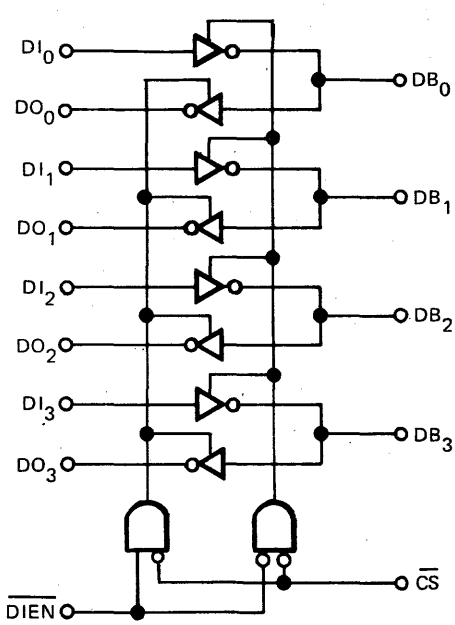
The μPB8216/8226 is a device that will reduce component count in microcomputer systems and at the same time enhance noise immunity to assure reliable, high performance operation.

BLOCK DIAGRAMS

8216



8226



$\overline{DIEN}$	$\overline{CS}$	RESULT
0	0	DI → DB
1	0	DB → DO
0	1	High Impedance
1	1	

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ABSOLUTE MAXIMUM RATINGS*

Operating Temperature . . . . . 0°C to 70°C
Storage Temperature (Cerdip) . . . . . −65°C to +150°C
(Plastic) . . . . . −65°C to +125°C
All Output and Supply Voltages . . . . . −0.5 to +7 Volts
All Input Voltages . . . . . −1.3 to +5.5 Volts
Output Currents . . . . . 125 mA

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

DC CHARACTERISTICS

T_a = 0°C to +70°C, V_{CC} = +5V±5%

PARAMETER		SYMBOL	LIMITS MIN	LIMITS TYP ①	LIMITS MAX	UNIT	TEST CONDITIONS
Input Load Current $\overline{DIEN}$, $\overline{CS}$		I_{F1}			−0.5	mA	V_F = 0.45
Input Load Current All Other Inputs		I_{F2}			−0.25*	mA	V_F = 0.45
Input Leakage Current $\overline{DIEN}$, $\overline{CS}$		I_{R1}			20	μA	V_R = 5.25V
Input Leakage Current DI Inputs		I_{R2}			10	μA	V_R = 5.25V
Input Forward Voltage Clamp		V_C			−1.0	V	I_C = −5 mA
Input "Low" Voltage		V_{IL}			0.95	V	
Input "High" Voltage		V_{IH}	2.0			V	
Output Leakage Current (3-State)	DO	I_O			20	μA	V_O = 0.45/5.25V
	DB	I_O			100		
Power Supply Current	8216	I_{CC}			130	mA	
	8226	I_{CC}			120	mA	
Output "Low" Voltage		V_{OL1}			0.48	V	DO Outputs I_{OL} = 15 mA DB Outputs I_{OL} = 25 mA
Output "Low" Voltage	8216	V_{OL2}			0.7	V	DB Outputs I_{OL} = 55 mA
	8226	V_{OL2}			0.7	V	DB Outputs I_{OH} = 50 mA
Output "High" Voltage		V_{OH1}	3.65			V	DO Outputs I_{OH} = −1 mA
Output "High" Voltage		V_{OH2}	2.4			V	DB Outputs I_{OH} = −10 mA
Output Short Circuit Current		I_{OS}	−15		−65	mA	DO Outputs V_O = 0V
		I_{OS}	−30		−120	mA	DB Outputs V_{CC} = 5.0V

Note: ① Typical values are for T_a = 25°C, V_{CC} = 5.0V.

CAPACITANCE ①

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input Capacitance	C_{IN}			8	pF	V_{BIAS} = 2.5V V_{CC} = 5V T_a = 25°C f = 1 MHz
Output Capacitance	C_{OUT1}			10 ②	pF	
Output Capacitance	C_{OUT2}			18 ③	pF	

Notes: ① This parameter is periodically sampled and not 100% tested.
② DO Output.
③ DB Output.

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AC CHARACTERISTICS

T_a = 0°C to +70°C; V_{CC} = +5V±5%

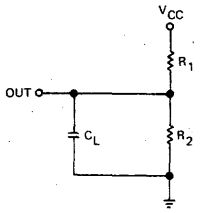
PARAMETER		SYMBOL	LIMITS MIN	LIMITS TYP ①	LIMITS MAX	UNIT	TEST CONDITIONS
Input to Output Delay DO Outputs		t_{PD1}			25	ns	C_L = 30 pF, R_1 = 300Ω, R_2 = 600Ω ④
Input to Output Delay	8216	t_{PD2}			30	ns	C_L = 300 pF, R_1 = 90Ω,
DB Outputs	8226	t_{PD2}			25	ns	R_2 = 180Ω 4
Output Enable Time	8216	t_E			65	ns	② ④
	8226	t_E			54	ns	
Output Disable Time		t_D			35	ns	③ ④

Notes: ① Typical values are for T_a = 25°C, V_{CC} = 5.0V

② DO Outputs, C_L = 30 pF, R_1 = 300/10 KΩ, R_2 = 600/1 KΩ,
DB Outputs, C_L = 300 pF, R_1 = 90/10 KΩ, R_2 = 180/1 KΩ.

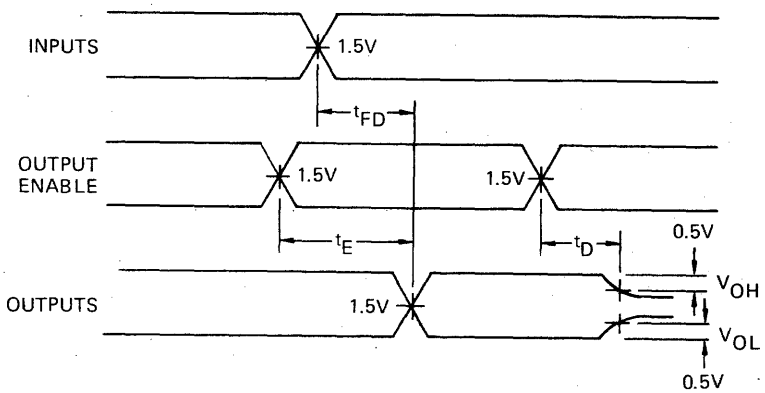
③ DO Outputs, C_L = 5 pF, R_1 = 300/10 KΩ, R_2 = 600/1 KΩ,
DB Outputs, C_L = 5 pF, R_1 = 90/10 KΩ, R_2 = 180/1 KΩ.

④ Input pulse amplitude: 2.5V
Input rise and fall times of 5 ns between 1 and 2 volts.
Output loading is 5 mA and 10 pF.
Speed measurements are made at 1.5 volt levels.

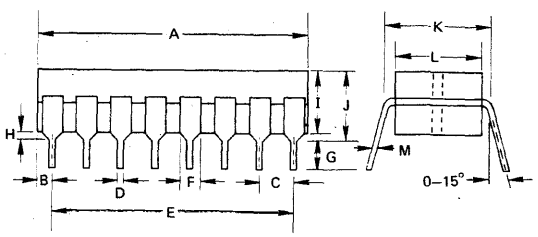


TEST CIRCUIT

TIMING WAVEFORMS

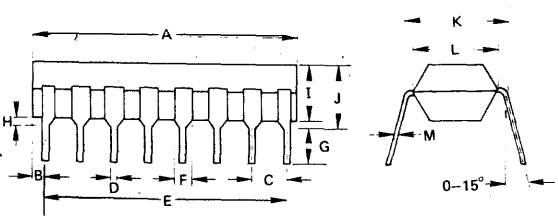


PACKAGE OUTLINE μPB8216C/D μPB8226C/D



Cerdip

ITEM	MILLIMETERS	INCHES
A	19.9 MAX.	0.784 MAX.
B	1.06	0.042
C	2.54	0.10
D	0.46 ± 0.10	0.018 ± 0.004
E	17.78	0.70
F	1.5	0.059
G	2.54 MIN.	0.10 MIN.
H	0.5 MIN.	0.019 MIN.
I	4.58 MAX.	0.181 MAX.
J	5.08 MAX.	0.20 MAX.
K	7.62	0.30
L	6.4	0.25
M	$0.25^{+0.10}_{0.05}$	$0.0098^{+0.0039}_{0.0019}$



Plastic

ITEM	MILLIMETERS	INCHES
A	19.4 MAX.	0.76 MAX.
B	0.81	0.03
C	2.54	0.10
D	0.5	0.02
E	17.78	0.70
F	1.3	0.051
G	2.54 MIN.	0.10 MIN.
H	0.5 MIN.	0.02 MIN.
I	4.05 MAX.	0.16 MAX.
J	4.55 MAX.	0.18 MAX.
K	7.62	0.30
L	6.4	0.25
M	$0.25^{+0.10}_{0.05}$	0.01

SP8216/8226-8-77-GN-CAT

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CLOCK GENERATOR AND DRIVER FOR 8080A PROCESSORS

DESCRIPTION

The μPB8224 is a single chip clock generator and driver for 8080A processors. The clock frequency is determined by a user specified crystal and is capable of meeting the timing requirements of the entire 8080A family of processors. MOS and TTL level clock outputs are generated.

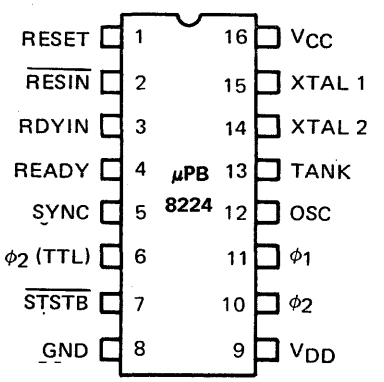
Additional logic circuitry of the μPB8224 provides signals for power-up reset, an advance status strobe and properly synchronizes the ready signal to the processor. This greatly reduces the number of chips needed for 8080A systems.

The μPB8224 is fabricated using NEC's Schottky bipolar process.

FEATURES

- Crystal Controlled Clocks
- Oscillator Output for External Timing
- MOS Level Clocks for 8080A Processor
- TTL Level Clock for DMA Activities
- Power-up Reset for 8080A Processor
- Ready Synchronization
- Advanced Status Strobe
- Reduces System Package Count
- Available in 16-pin Cerdip and Plastic Packages

PIN CONFIGURATION



PIN NAMES

$\overline{\text{RESIN}}$	Reset Input
RESET	Reset Output
RDYIN	Ready Input
READY	Ready Output
SYNC	Sync Input
$\overline{\text{STSTB}}$	Status STB Output
ϕ_1	Processor Clocks
ϕ_2	
XTAL 1	Crystal Connections
XTAL 2	
TANK	Used With Overtone Crystal
OSC	Oscillator Output
ϕ_2 (TTL)	ϕ_2 CLK (TTL Level)
V_{CC}	+5V
V_{DD}	+12V
GND	0V

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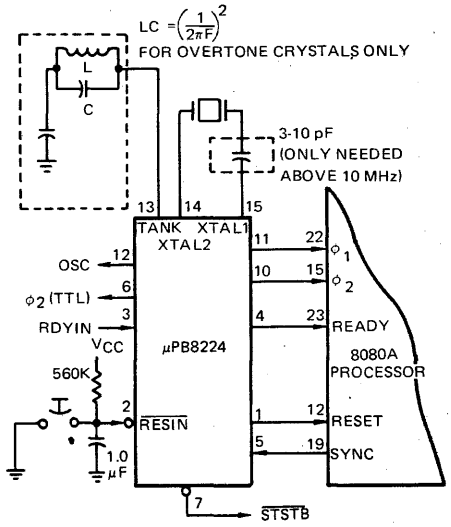
Clock Generator

The clock generator circuitry consists of a crystal controlled oscillator and a divide-by-nine counter. The crystal frequency is a function of the 8080A processor speed and is basically nine times the processor frequency, i.e.:

$$\text{Crystal frequency} = \frac{9}{t_{CY}}$$

where t_{CY} is the 8080A processor clock period.

A series resonant fundamental mode crystal is normally used and is connected across input pins XTAL1 and XTAL2. If an overtone mode crystal is used, an additional LC network, AC coupled to ground, must be connected to the TANK input of the μPB8224 as shown in the following figure.



The formula for the LC network is:

$$LC = \left(\frac{1}{2\pi F}\right)^2$$

where F is the desired frequency of oscillation.

The output of the oscillator is input to the divide-by-nine counter. It is also buffered and brought out on the OSC pin, allowing this stable, crystal controlled source to be used for derivation of other system timing signals. The divide-by-nine counter generates the two non-overlapping processor clocks, ϕ_1 and ϕ_2, which are buffered and at MOS levels, a TTL level ϕ_2 and internal timing signals.

The ϕ_1 and ϕ_2 high level outputs are generated in a 2-5-2 digital pattern, with ϕ_1 being high for two oscillator periods, ϕ_2 being high for five oscillator periods, and then neither being high for two oscillator periods. The TTL level ϕ_2,ϕ_2 (TTL), is normally used for DMA activities by gating the external device onto the 8080A bus once a Hold Acknowledge (HLDA) has been issued.

Additional Logic

In addition to the clock generator circuitry, the μPB8224 contains additional logic to aid the system designer in the proper timing of several interface signals.

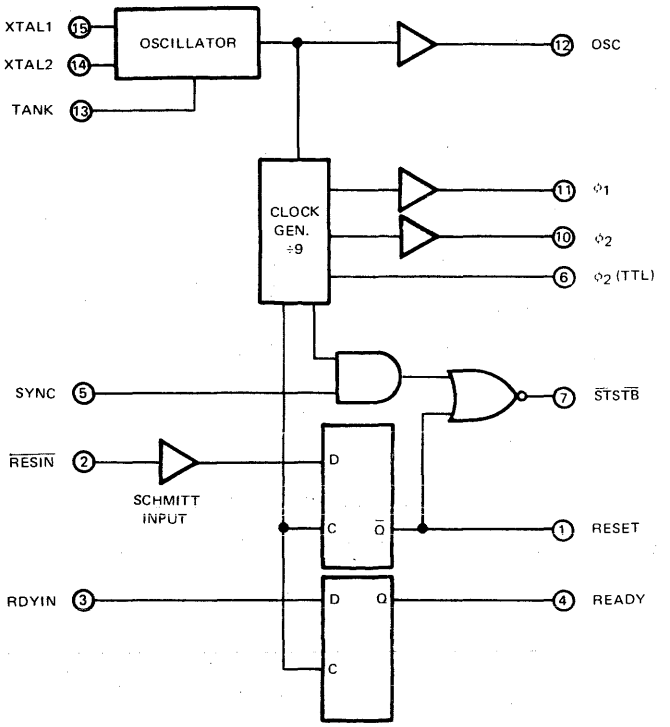
The $\overline{\text{STSTB}}$ signal indicates, at the earliest possible moment, when the status signals output from the 8080A processor are stable on the data bus. $\overline{\text{STSTB}}$ is designed to connect directly to the μPB8228 System Controller and automatically resets the μPB8228 during power-on Reset.

The $\overline{\text{RESIN}}$ input to the μPB8224 is used to automatically generate a RESET signal to the 8080A during power initialization. The slow rise of the power supply voltage in an external RC network is sensed by an internal Schmitt Trigger. The output of the Schmitt Trigger is gated to generate an 8080A compatible RESET. An active low manual switch may also be attached to the RC circuit for manual system reset.

The RDYIN input to the μPB8224 accepts an asynchronous "wait request" and generates a READY output to the 8080A that is fully synchronized to meet the 8080A timing requirements.

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BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	0°C to +70°C
Storage Temperature	−65°C to +150°C
All Output Voltages (TTL)	−0.5 to +7 Volts
All Output Voltages (MOS)	−1.0 to +13.5 Volts
All Input Voltages	−1.5 to +7 Volts
Supply Voltage V_{CC}	−0.5 to +7 Volts
Supply Voltage V_{DD}	−0.5 to +13.5 Volts
Output Currents	100 mA

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

DC CHARACTERISTICS

T_a = 0°C to +70°C; V_{CC} = +5V ±5%; V_{DD} = +12V ±5%

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input Current Loading	I_F			-0.25	mA	V_F = 0.45V
Input Leakage Current	I_R			10	μA	V_R = 5.25V
Input Forward Clamp Voltage	V_C			−1.0	V	I_C = −5 mA
Input "Low" Voltage	V_{IL}			0.8	V	V_{CC} = 5.0V
Input "High" Voltage	V_{IH}	2.6			V	Reset Input
		2.0				All Other Inputs
RESIN Input Hysteresis	V_{IH}-V_{IL}	0.25			V	V_{CC} = 5.0V
Output "Low" Voltage	V_{OL}			0.45	V	(ϕ_1, ϕ_2), Ready, Reset, STSTB
						I_{OL} = 2.5 mA
				0.45	V	All Other Inputs
						I_{OL} = 15 mA
Output "High" Voltage	V_{OH}					
ϕ_1, ϕ_2		9.4			V	I_{OH} = −100 μA
READY, RESET		3.6			V	I_{OH} = −100 μA
All Other Outputs		2.4			V	I_{OH} = −1 mA
Output Short Circuit Current (All Low Voltage Outputs Only)	I_{SC} ①	−10		−60	mA	V_O = 0V, V_{CC} = 5.0V
Power Supply Current	I_{CC}			115	mA	
Power Supply Current	I_{DD}			15	mA	

Note: ① Caution, ϕ_1 and ϕ_2 output drivers do not have short circuit protection

CAPACITANCE①

T_a = 25°C; f = 1 MHz; V_{CC} = 5V; V_{DD} = 12V; V_{BIAS} = 2.5V

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input Capacitance	C_{IN}			8	pF	

Note: ① This parameter is periodically sampled and not 100% tested.

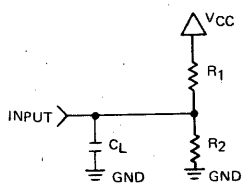
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AC CHARACTERISTICS

T_a = 0°C to +70°C; V_{CC} = +5V ±5%; V_{DD} = +12V ±5%

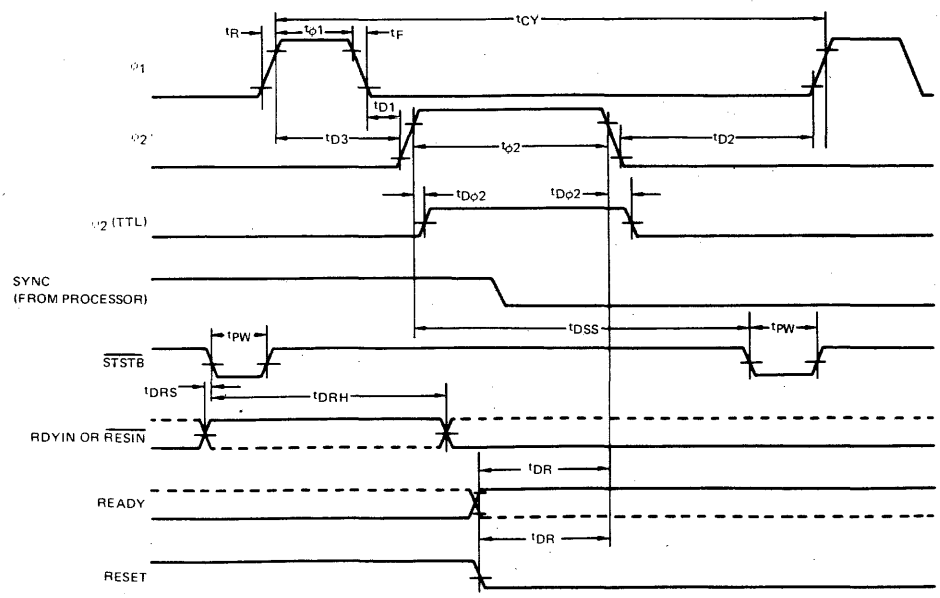
PARAMETER	SYMBOL	LIMITS ① MIN	LIMITS ① TYP	LIMITS ① MAX	UNIT	TEST CONDITIONS
ϕ_1 Pulse Width	$t_{\phi 1}$	$\frac{2t_{CY}}{9}$ −20 ns			ns	C_L = 20 pF to 50 pF
ϕ_2 Pulse Width	$t_{\phi 2}$	$\frac{5t_{CY}}{9}$ −35 ns				
ϕ_1 to ϕ_2 Delay	t_{D1}	0				
ϕ_2 to ϕ_1 Delay	t_{D2}	$\frac{2t_{CY}}{9}$ −14 ns				
ϕ_1 to ϕ_2 Delay	t_{D3}	$\frac{2t_{CY}}{9}$		$\frac{2t_{CY}}{9}$ +20 ns		
ϕ_1 and ϕ_2 Rise Time	t_R			20		
ϕ_1 and ϕ_2 Fall Time	t_F			20		
ϕ_2 to ϕ_2 (TTL) Delay	$t_{D\phi 2}$	−5		+15	ns	ϕ_2 TTL, CL = 30 pF R_1 = 300Ω R_2 = 600Ω
ϕ_2 to $\overline{STSTB}$ Delay	t_{DSS}	$\frac{6t_{CY}}{9}$ −30 ns		$\frac{6t_{CY}}{9}$	ns	$\overline{STSTB}$, CL = 15 pF R_1 = 2K R_2 = 4K
$\overline{STSTB}$ Pulse Width	t_{PW}	$\frac{t_{CY}}{9}$ −15 ns			ns	
RDYIN Setup Time to $\overline{STSTB}$	t_{DRS}	50 ns − $\frac{4t_{CY}}{9}$				
RDYIN Hold Time After $\overline{STSB}$	t_{DRH}	$\frac{4t_{CY}}{9}$				
READY or RESET to ϕ_2 Delay	t_{DR}	$\frac{4t_{CY}}{9}$ −25 ns			ns	Ready and Reset CL = 10 pF R_1 = 2K R_2 = 4K
Crystal Frequency	f_{CLK}		$\frac{9}{t_{CY}}$		MHz	
Maximum Oscillating Frequency	f_{MAX}			27	MHz	

Note: ① t_{CY} represents the processor clock period



TEST CIRCUIT

TIMING WAVEFORMS



Voltage Measurement Points: ϕ_1, ϕ_2 Logic "0" = 1.0V, Logic "1" = 8.0V.
All other signals measured at 1.5V.

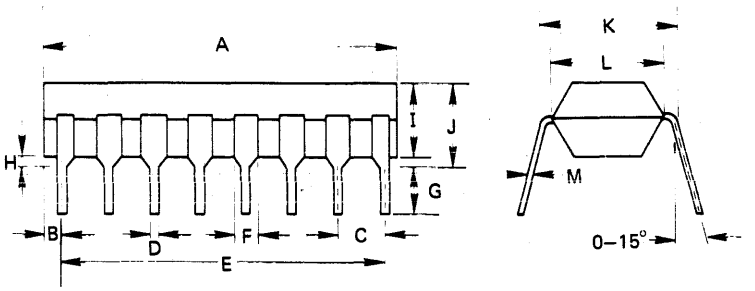
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CRYSTAL REQUIREMENTS

Tolerance	0.005% at 0°C–70°C
Resonance	Series (Fundamental) ①
Load Capacitance	20-35 pF
Equivalent Resistance	75-20 ohms
Power Dissipation (Min)	4 mW

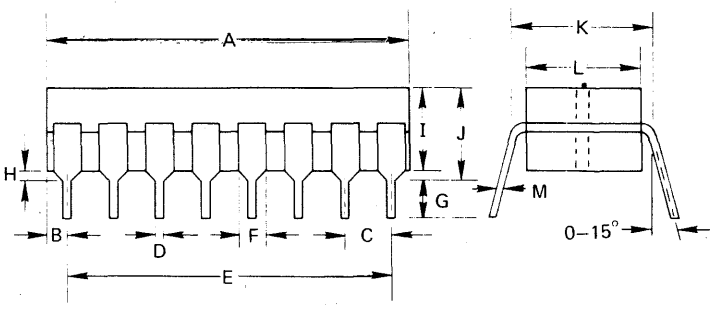
Note: ① With tank circuit use 3rd overtone mode.

PACKAGE OUTLINE μPB8224C/D



μPB8224C (Plastic)

ITEM	MILLIMETERS	INCHES
A	19.4 MAX.	0.76 MAX.
B	0.81	0.03
C	2.54	0.10
D	0.5	0.02
E	17.78	0.70
F	1.3	0.051
G	2.54 MIN.	0.10 MIN.
H	0.5 MIN.	0.02 MIN.
I	4.05 MAX.	0.16 MAX.
J	4.55 MAX.	0.18 MAX.
K	7.62	0.30
L	6.4	0.25
M	$0.25^{+0.10}_{-0.05}$	0.01



μPB8224D (Cerdip)

ITEM	MILLIMETERS	INCHES
A	19.9 MAX	0.784 MAX
B	1.06	0.042
C	2.54	0.10
D	0.46 ± 0.10	0.018 ± 0.004
E	17.78	0.70
F	1.5	0.059
G	2.54 MIN	0.10 MIN
H	0.5 MIN	0.019 MIN
I	4.58 MAX	0.181 MAX
J	5.08 MAX	0.20 MAX
K	7.62	0.30
L	6.8	0.27
M	$0.25^{+0.10}_{-0.05}$	$0.0098^{+0.0039}_{-0.0019}$

SP8224-8-77-GN-CAT

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8080A SYSTEM CONTROLLER AND BUS DRIVER

DESCRIPTION

The μPB8228/8238 is a single chip controller and bus driver for 8080A based systems. All the required interface signals necessary to connect RAM, ROM and I/O components to a μPD8080A are generated.

The μPB8228/8238 provides a bi-directional three-state bus driver for high TTL fan-out and isolation of the processor data bus from the system data bus for increased noise immunity.

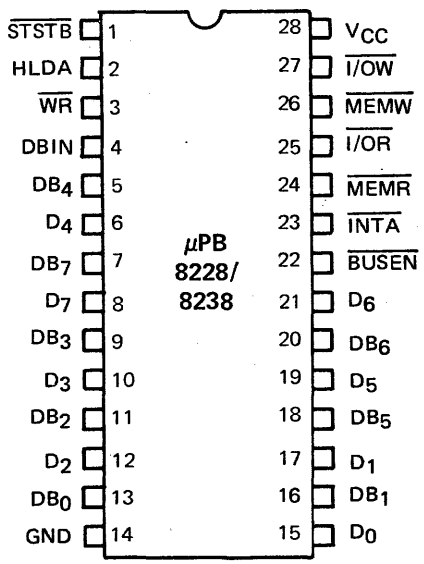
The system controller portion of the μPB8228/8238 consists of a status latch for definition of processor machine cycles and a gating array to decode this information for direct interface to system components. The controller can enable gating of a multi-byte interrupt onto the data bus or can automatically insert a RESTART 7 onto the data bus without any additional components.

Two devices are provided. The μPB8228 for small systems without tight write timing constraints and the μPB8238 for larger systems.

FEATURES

- System Controller for 8080A Systems
- Bi-Directional Data Bus for Processor Isolation
- 3.60V Output High Voltage for Direct Interface to 8080A Processor
- Three State Outputs on System Data Bus
- Enables Use of Multi-Byte Interrupt Instructions
- Generates RST 7 Interrupt Instruction
- μPB8228 for Small Memory Systems
- μPB8238 for Large Memory Systems
- Reduces System Package Count
- Schottky Bipolar Technology

PIN CONFIGURATION



NC: No Connection

PIN NAMES

$D_7 - D_0$	Data Bus (Processor Side)
$DB_7 - DB_0$	Data Bus (System Side)
$\overline{I/OR}$	I/O Read
$\overline{I/OW}$	I/O Write
$\overline{MEMR}$	Memory Read
$\overline{MEMW}$	Memory Write
DBIN	DBIN (From Processor)
$\overline{INTA}$	Interrupt Acknowledge
HLDA	HLDA (From Processor)
$\overline{WR}$	WR (From Processor)
$\overline{BUSEN}$	Bus Enable Input
$\overline{STSTB}$	Status Strobe (From μPB8224)
V_{CC}	+5V
GND	0 Volts

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FUNCTIONAL DESCRIPTION

Bi-Directional Bus Driver

The eight bit, bi-directional bus driver provides buffering between the processor data bus and the system data bus. On the processor side, the μPB8228/8238 exceeds the minimum input voltage requirements (3.0V) of the μPD8080A. On the system side, the driver is capable of adequate drive current (10 mA) for connection of a large number of memory and I/O devices to the bus. Signal flow in the bus driver is controlled by the gating array and its outputs can be forced into a high impedance state by use of the $\overline{\text{BUSEN}}$ input.

Status Latch

The Status Latch in the μPB8228/8238 stores the status information placed on the data bus by the 8080A at the beginning of each machine cycle. The information is latched when $\overline{\text{STSTB}}$ goes low and is then decoded by the gating array for the generation of control signals.

Gating Array

The Gating Array generates "active low" control signals for direct interfacing to system components by gating the contents of the status latch with control signals from the 8080A.

$\overline{\text{MEM/R}}$, $\overline{\text{I/OR}}$ and $\overline{\text{INTA}}$ are generated by gating the DBIN signal from the processor with the contents of the status latch. $\overline{\text{I/OR}}$ is used to enable an I/O input onto the system data bus. $\overline{\text{MEM/R}}$ is used to enable a memory input.

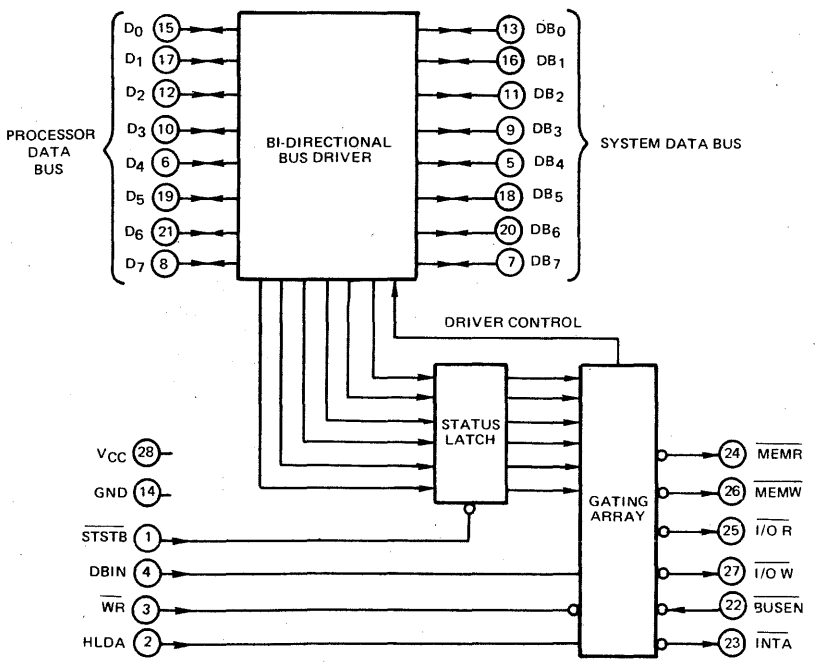
$\overline{\text{INTA}}$ is normally used to gate an interrupt instruction onto the system data bus. When used with the μPD8080A processor, the μPB8228/8238 will decode an interrupt acknowledge status word during all three machine cycles for a multi-byte interrupt instruction. For 8080A type processors that do not generate an interrupt acknowledge status word during the second and third machine cycles of a multi-byte interrupt instruction, the μPB8228/8238 will internally generate an $\overline{\text{INTA}}$ pulse for those machine cycles.

The μPB8228/8238 also provides the designer the ability to place a single interrupt instruction onto the bus without adding additional components. By connecting the +12 volt supply to the $\overline{\text{INTA}}$ output (pin 23) of the μPB8228/8238 through a 1 K ohm series resistor, RESTART 7 will be gated onto the processor data bus when DBIN is active during an interrupt acknowledge machine cycle.

$\overline{\text{MEM/W}}$ and $\overline{\text{I/OW}}$ are generated by gating the $\overline{\text{WR}}$ signal from the processor with the contents of the status latch. $\overline{\text{I/OW}}$ indicates that an output port write is about to occur. $\overline{\text{MEM/W}}$ indicates that a memory write will occur.

The data bus output buffers and control signal buffers can be asynchronously forced into a high impedance state by placing a high on the $\overline{\text{BUSEN}}$ pin of the μPB8228/8238. Normal operation is performed with $\overline{\text{BUSEN}}$ low.

BLOCK DIAGRAM



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ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	0°C to +70°C
Storage Temperature	−65°C to +150°C
All Output or Supply Voltages	−0.5 to +7 Volts
All Input Voltages	−1.5 to 5.5 Volts
Output Currents	100 mA

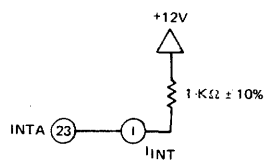
COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

DC CHARACTERISTICS

T_a = 0°C to 70°C, V_{CC} = 5V ± 5%

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input Clamp Voltage, All Inputs	V_C			−1.0	V	V_{CC} = 4.75V; I_{CC} = −5 mA
Input Load Current, $\overline{STSTB}$	I_F			500	μA	V_{CC} = 5.25V V_F = 0.45V
D_2 and D_6				750	μA	
D_0, D_1, D_4, D_5, and D_7				250	μA	
All Other Inputs				250	μA	
Input Leakage Current, $\overline{STSTB}$	I_R			100	μA	V_{CC} = 5.25V V_R = 5.0V
DB_0 through DB_7				20 *	μA	
All Other Inputs				100	μA	
Input Threshold Voltage, All Inputs	V_{TH}	0.8		2.0	V	V_{CC} = 5V
Power Supply Current	I_{CC}			190	mA	V_{CC} = 5.25V
Output Low Voltage, D_0 through D_7	V_{OL}			0.45	V	V_{CC} = 4.75V; I_{OL} = 2 mA
All Other Outputs				0.48	V	I_{OL} = 10 mA
Output High Voltage, D_0 through D_7	V_{OH}	3.6			V	V_{CC} = 4.75V; I_{OH} = −10 μA
All Other Outputs		2.4			V	I_{OH} = −1 mA
Short Circuit Current, All Outputs	I_{OS}	15		90	mA	V_{CC} = 5V
Off State Output Current, All Control Outputs	$I_{O(off)}$			100	μA	V_{CC} = 5.25V; V_O = 5.0V
				−100	μA	V_O = 0.45V
INTA Current	I_{INT}			5	mA	(See Figure below)



INTA TEST CIRCUIT

CAPACITANCE

T_a = 25°C

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input Capacitance	C_{IN}			12	pF	V_{BIAS} = 2.5V, V_{CC} = 5.0V, f = 1 MHz
Output Capacitance Control Signals	C_{OUT}			15	pF	
I/O Capacitance (D or DB)	$C_{I/O}$			15	pF	

NOTE: This parameter is periodically sampled and not 100% tested.

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STATUS WORD CHART

DATA BUS BIT	STATUS INFORMATION	INSTRUCTION FETCH	MEMORY READ	MEMORY WRITE	STACK READ	STACK WRITE	INPUT READ	OUTPUT WRITE	INTERRUPT ACKNOWLEDGE (M_1)	INT. ACK. (M_2, M_3)	HALT ACKNOWLEDGE	
		①	②	③	④	⑤	⑥	⑦	⑧	⑨	⑩	
D_0	INTA	0	0	0	0	0	0	0	1	0	1	μPD8080A OUTPUT
D_1	$\overline{WO}$	1	1	0	1	0	1	0	1	1	1	
D_2	STACK	0	0	0	1	1	0	0	0	0	0	
D_3	HLTA	0	0	0	0	0	0	0	0	1	1	
D_4	OUT	0	0	0	0	0	0	1	0	0	0	
D_5	M_1	1	0	0	0	0	0	0	1	0	1	
D_6	INP	0	0	0	0	0	1	0	0	0	0	
D_7	MEMR	1	1	0	1	0	0	0	0	1	0	
24	$\overline{MEMR}$	0	0	1	0	1	1	1	1	1	1	μPB8228/8238 OUTPUT
26	$\overline{MEMW}$	1	1	0	1	0	1	1	1	1	1	
25	$\overline{I/OR}$	1	1	1	1	1	0	1	1	1	1	
27	$\overline{I/OW}$	1	1	1	1	1	1	0	1	1	1	
23	$\overline{INTA}$	1	1	1	1	1	1	1	0	0	1	
PIN NO.		SIGNAL STATUS										
		μPB8228/8238 CONTROL SIGNALS										

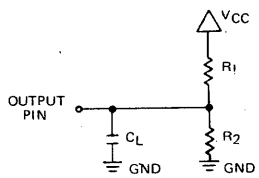
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AC CHARACTERISTICS

T_a = 0°C to 70°C, V_{CC} = 5V ± 5%

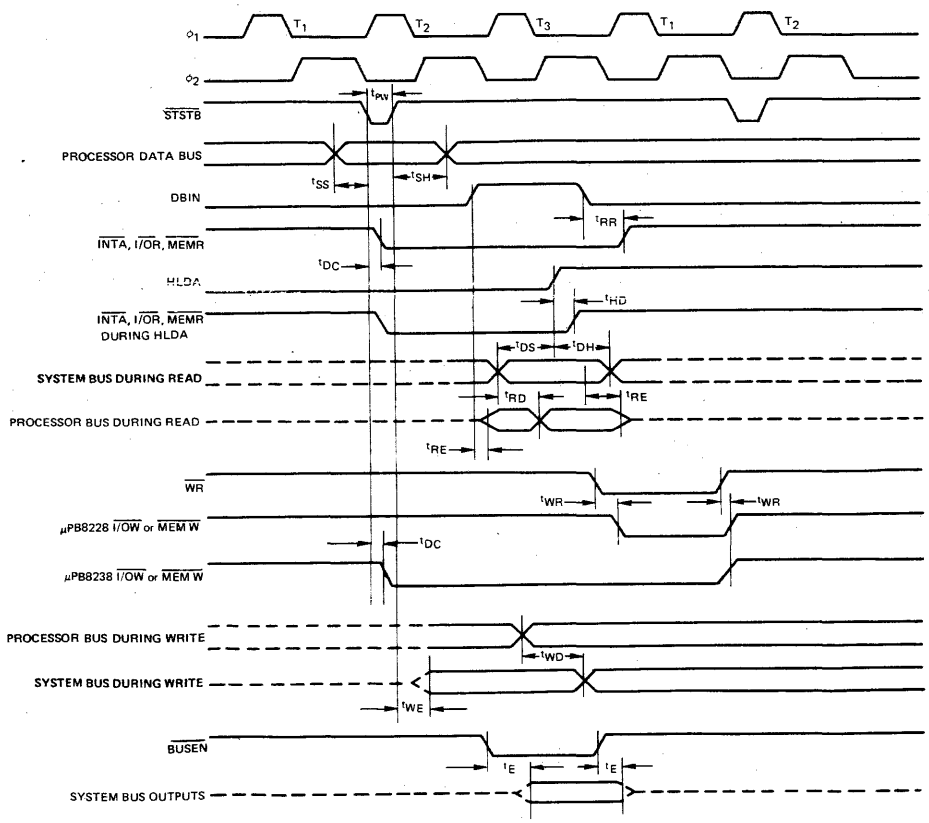
PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Width of Status Strobe	t_{PW}	22			ns	
Setup Time, Status Inputs D_0-D_7	t_{SS}	8			ns	
Hold Time, Status Inputs D_0-D_7	t_{SH}	5			ns	
Delay from $\overline{STSTB}$ to any Control Signal	t_{DC}	20		60	ns	C_L = 100 pF
Delay from DBIN to Control Outputs	t_{RR}			30	ns	C_L = 100 pF
Delay from DBIN to Enable/ Disable 8080A Bus	t_{RE}			45	ns	C_L = 25 pF
Delay from System Bus to 8080A Bus during Read	t_{RD}			30	ns	C_L = 25 pF
Delay from $\overline{WR}$ to Control Outputs	t_{WR}	5		45	ns	C_L = 100 pF
Delay to Enable System Bus DB_0-DB_7 after $\overline{STSTB}$	t_{WE}			30	ns	C_L = 100 pF
Delay from 8080A Bus D_0-D_7 to System Bus DB_0-DB_7 during Write	t_{WD}	5		40	ns	C_L = 100 pF
Delay from $\overline{System\ Bus\ Enable}$ to System Bus DB_0-DB_7	t_E			30	ns	C_L = 100 pF
HLDA to Read Status Outputs	t_{HD}			25	ns	
Setup Time, System Bus Inputs to HLDA	t_{DS}	10			ns	
Hold Time, System Bus Inputs to HLDA	t_{DH}	20			ns	C_L = 100 pF

For D_0-D_7: R_1 = 4 KΩ, R_2 = ∞Ω, C_L = 25 pF. For all other outputs: R_1 = 500Ω, R_2 = 1 KΩ, C_L = 100 pF.



TEST CIRCUIT

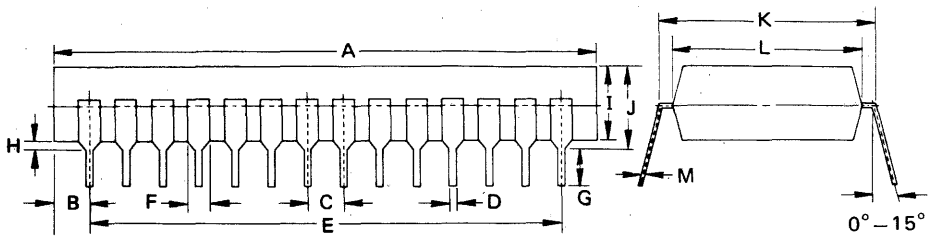
TIMING WAVEFORMS



VOLTAGE MEASUREMENT POINTS: D_0-D_7 (when outputs) Logic "0" = 0.8V, Logic "1" = 3.0V. All other signals measured at 1.5V.

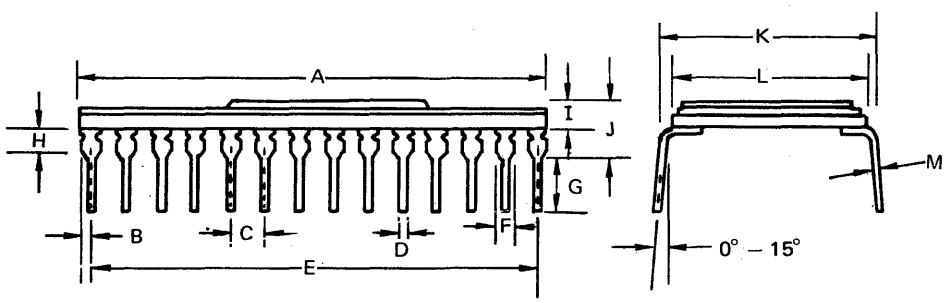
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PACKAGE OUTLINE
μPB8228/8238C/D



μPB8228/8238C
(Plastic)

ITEM	MILLIMETERS	INCHES
A	38.0 MAX.	1.496 MAX.
B	2.49	0.098
C	2.54	0.10
D	0.5 ± 0.1	0.02 ± 0.004
E	33.02	1.3
F	1.5	0.059
G	2.54 MIN.	0.10 MIN.
H	0.5 MIN.	0.02 MIN.
I	5.22 MAX.	0.205 MAX.
J	5.72 MAX.	0.225 MAX.
K	15.24	0.6
L	13.2	0.52
M	$0.25^{+0.10}_{-0.05}$	$0.01^{+0.004}_{-0.002}$



μPB8228/8238D
(Ceramic)

ITEM	MILLIMETERS	INCHES
A	36.0 MAX.	1.41 MAX.
B	1.5 MAX.	0.059 MAX
C	2.54	0.1
D	0.50 ± 0.1	0.02 ± 0.004
E	33.0	1.299
F	1.27	0.05
G	3.2 MIN.	0.126 MIN
H	1.0 MIN	0.04 MIN
I	3.3 MAX.	0.13 MAX.
J	5.2 MAX.	0.20 MAX.
K	15.3	0.60
L	13.9	0.55
M	0.30 ± 0.1	0.012 ± 0.004

SP8228/38-9-77-GN-CAT

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INPUT/OUTPUT EXPANDER FOR μPD8048/8748/8035

DESCRIPTION

The μPD8243 input/output expander is directly compatible with the μPD8048 family of single-chip microcomputers. Using NMOS technology the μPD8243 provides high drive capabilities while requiring only a single +5V supply voltage.

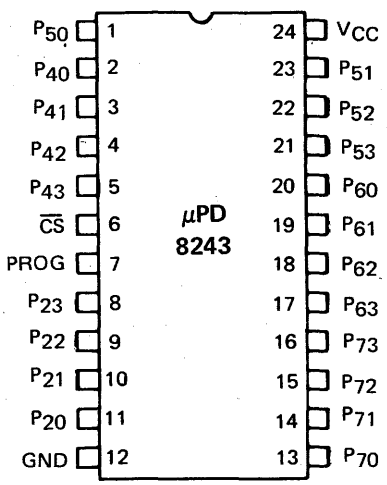
The μPD8243 interfaces to the μPD8048 family through a 4-bit I/O port and offers four 4-bit bi-directional static I/O ports. The ease of expansion allows for multiple μPD8243's to be added using the bus port.

The bi-directional I/O ports of the μPD8243 act as an extension of the I/O capabilities of the μPD8048 microcomputer family. They are accessible with their own ANL, MOV, and ORL instructions.

FEATURES

- Four 4-Bit I/O Ports
- Fully Compatible with μPD8048 Microcomputer Family
- High Output Drive
- NMOS Technology
- Single +5V Supply
- Direct Extension of Resident μPD8048 I/O Ports
- Logical AND and OR Directly to Ports
- Compatible with Industry Standard 8243
- Available in 24-Pin Plastic and Ceramic Packages

PIN CONFIGURATION



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FUNCTIONAL DESCRIPTION

General Operation

The I/O capabilities of the μPD8048/8748/8035 can be enhanced in four 4-bit I/O port increments using one or more μPD8243's. These additional I/O lines are addressed as ports 4-7. The following lists the operations which can be performed on ports 4-7.

- Logical AND Accumulator to Port.
- Logical OR Accumulator to Port.
- Transfer Port to Accumulator.
- Transfer Accumulator to Port.

Port 2 (P_{20}-P_{23}) forms the 4-bit bus through which the μPD8243 communicates with the host processor. The PROG output from the μPD8048/8748/8035 provides the necessary timing to the μPD8243. There are two 4-bit nibbles involved in each data transfer. The first nibble contains the op-code and port address followed by the second nibble containing the 4-bit data. Multiple μPD8243's can be used for additional I/O. The output lines from the μPD8048/8748/8035 can be used to form the chip selects for the additional μPD8243's.

Power On Initialization

Applying power to the μPD8243 sets ports 4-7 to the tri-state mode and port 2 to the input mode. The state of the PROG pin at power on may be either high or low. The PROG pin must make a high-to-low transition in order to exit from the power on mode. The power on sequence is initiated any time V_{CC} drops below 1V. The table below shows how the 4-bit nibbles on Port 2 correspond to the μPD8243 operations.

Port Address			Op-Code		
P_{21}	P_{20}	Address Code	P_{23}	P_{22}	Instruction Code
0	0	Port 4	0	0	Read
0	1	Port 5	0	1	Write
1	0	Port 6	1	0	ORLD
1	1	Port 7	1	1	ANLD

For example an 0010 appearing on P_{20}-P_{23}, respectively, would result in a Write to Port 4.

Read Mode

There is one Read mode in the μPD8243. A falling edge on the PROG pin latches the op-code and port address from input Port 2. The port address and Read operation are then decoded causing the appropriate outputs to be tri-stated and the input buffers switched on. The rising edge of PROG terminates the Read operation. The Port (4,5,6, or 7) that was selected by the Port address (P_{21}-P_{20}) is returned to the tri-state mode, and Port 2 is switched to the input mode.

Generally, in the read mode, a port will be an input and in the write mode it will be an output. If during program operation, the μPD8243's modes are changed, the first read pulse immediately following a write should be ignored. The subsequent read signals are valid. Reading a port will then force that port to a high impedance state.

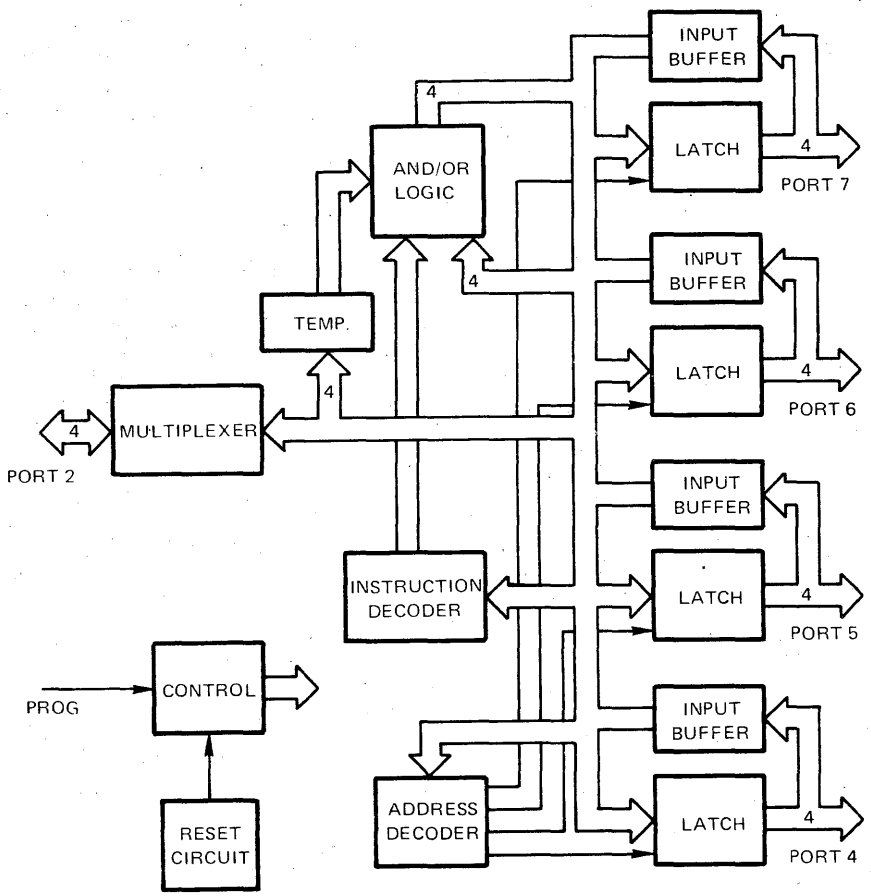
Write Modes

There are three write modes in the μPD8243. The MOVD P_p,A instruction from the μPD8048/8748/8035 writes the new data directly to the specified port (4,5,6, or 7). The old data previously latched at that port is lost. The ORLD Pp,A instruction performs a logical OR between the new data and the data currently latched at the selected port. The result is then latched at that port. The final write mode uses the ANLD Pp,A instruction. It performs a logical AND between the new data and the data currently latched at the specified port. The result is latched at that port.

The data remains latched at the selected port following the logical manipulation until new data is written to that port.

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BLOCK DIAGRAM



PIN IDENTIFICATION

PIN NO.	PIN SYMBOL	FUNCTION
2-5 1, 21-23 17-20 13-16	P_{40}-P_{43} P_{50}-P_{53} P_{60}-P_{63} P_{70}-P_{73}	The four 4-bit static bi-directional I/O ports. They are programmable into the following modes: input mode (during a Read operation); low impedance latched output mode (after a Write operation); and the tri-state mode (following a Read operation). Data appearing on I/O lines P_{20}-P_{23} can be written directly. That data can also be logically ANDed or ORed with the previous data on those lines.
6	$\overline{CS}$	Chip Select input (active-low). When the μPD8343 is deselected ($\overline{CS}$ = 1), output or internal status changes are inhibited.
7	PROG	Clock input pin. The control and address information are present on port lines P_{20}-P_{23} when PROG makes a high-to-low transition. Data is present on port lines P_{20}-P_{23} when PROG makes a low-to-high transition.
8-11	P_{20}-P_{23}	P_{20}-P_{23} form a 4-bit bi-directional port. Refer to PROG function for contents of P_{20}-P_{23} at the rising and falling edges of PROG. Data from a selected port is present on P_{20}-P_{23} prior to the rising edge of PROG if during a Read operation.
12	GND	The μPD8041/8741 ground potential.
24	V_{CC}	+5 volt supply.

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ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	0°C to +70°C
Storage Temperature (Ceramic Package)	−65°C to +150°C
Storage Temperature (Plastic Package)	−65°C to +125°C
Voltage on Any Pin	− 0.5 to +7 Volts ①
Power Dissipation	1 W

Note: ① With respect to ground.

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

DC CHARACTERISTICS

T_a = 0°C to +70°C; V_{CC} = +5V ± 5%

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input Low Voltage	V_{IL}	-0.5		0.8	V	
Input High Voltage	V_{IH}	2.0		V_{CC} + 0.5	V	
Output Low Voltage (Ports 4-7)	V_{OL1}			0.45	V	I_{OL} = 5 mA ①
Output Low Voltage (Port 7)	V_{OL2}			1	V	I_{OL} = 20 mA
Output Low Voltage (Port 2)	V_{OL3}			0.45	V	I_{OL} = 0.6 mA
Output High Voltage (Ports 4-7)	V_{OH1}	2.4			V	I_{OH} = 240 μA
Output High Voltage (Port 2)	V_{OH2}	2.4			V	I_{OH} = 100 μA
Sum of All I_{OL} From 16 Outputs	I_{OL}			100	mA	5 mA Each Pin
Input Leakage Current (Ports 4-7)	I_{IL1}	-10		20	μA	V_{IN} = V_{CC} to 0V
Input Leakage Current (Port 2, $\overline{CS}$, PROG)	I_{IL2}	-10		10	μA	V_{IN} = V_{CC} to 0V
V_{CC} Supply Current	I_{CC}		10	20	mA	

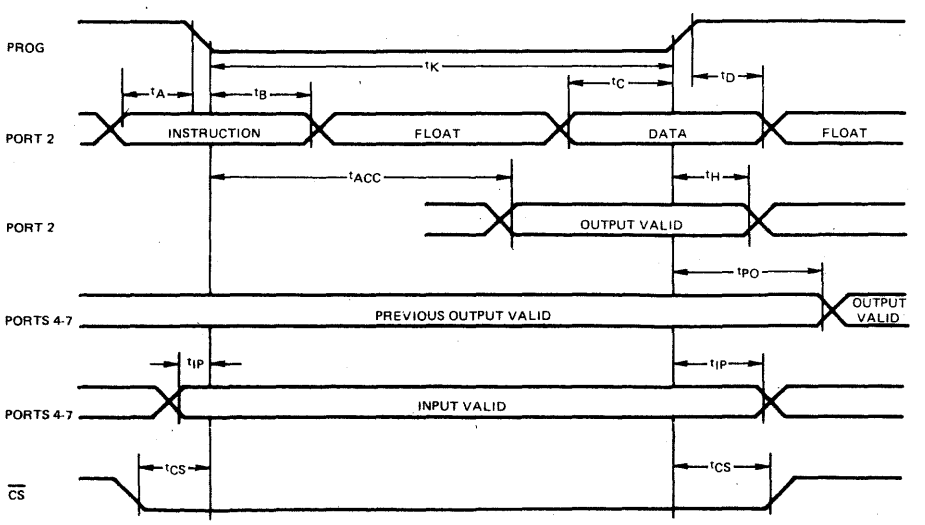
Note: ① Refer to graph of additional sink current drive.

AC CHARACTERISTICS

T_a = 0°C to +70°C; V_{CC} = +5V ± 5%

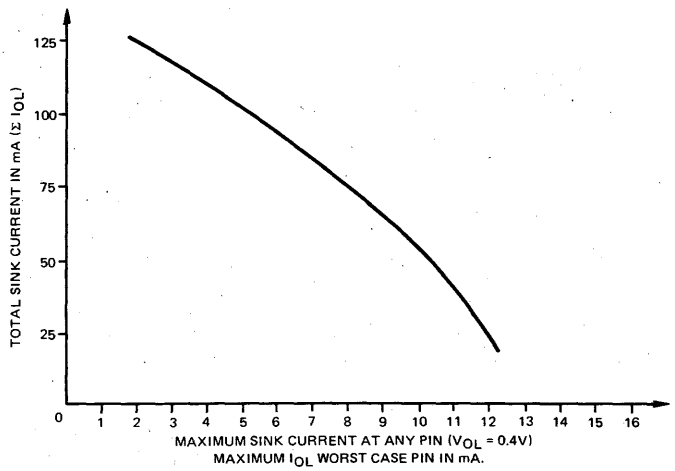
PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS	TEST CONDITIONS
Code Valid Before PROG	t_A	100			ns	80 pF Load
Code Valid After PROG	t_B	60			ns	20 pF Load
Data Valid Before PROG	t_C	200			ns	80 pF Load
Data Valid After PROG	t_D	20			ns	20 pF Load
Port 2 Floating After PROG	t_H	0		150	ns	20 pF Load
PROG Negative Pulse Width	t_K	900			ns	
Ports 4-7 Valid After PROG	t_{PO}			700	ns	100 pF Load
Ports 4-7 Valid Before/After PROG	t_{LP1}	100			ns	
Port 2 Valid After PROG	t_{ACC}			750	ns	80 pF Load
$\overline{CS}$ Valid Before/After PROG	$t_{\overline{CS}}$	50			ns	

TIMING WAVEFORMS



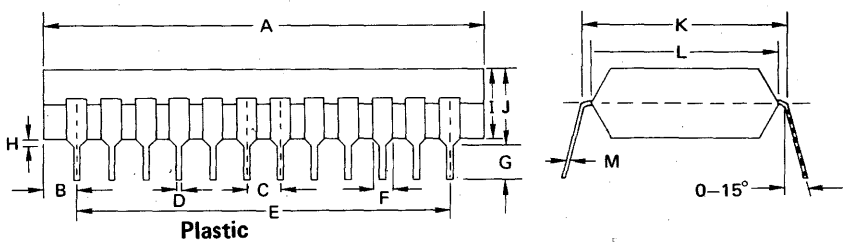
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CURRENT SINKING CAPABILITY ①



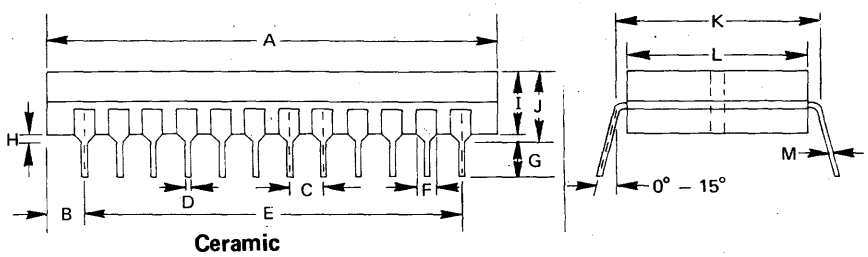
Note: ① This curve plots the guaranteed worst case current sinking capability of any I/O port line versus the total sink current of all pins. The μPD8243 is capable of sinking 5 mA (for V_{OL} = 0.4V) through each of the 16 I/O lines simultaneously. The current sinking curve shows how the individual I/O line drive increases if all the I/O lines are not fully loaded.

PACKAGE OUTLINES μPD8243C/D



Plastic

ITEM	MILLIMETERS	INCHES
A	33 MAX	1.3 MAX
B	2.53	0.1
C	2.54	0.1
D	0.5 ± 0.1	0.02 ± 0.004
E	27.94	1.1
F	1.5	0.059
G	2.54 MIN	0.1 MIN
H	0.5 MIN	0.02 MIN
I	5.22 MAX	0.205 MAX
J	5.72 MAX	0.225 MAX
K	15.24	0.6
L	13.2	0.52
M	$0.25^{+0.10}_{-0.05}$	$0.01^{+0.004}_{-0.0019}$



Ceramic

ITEM	MILLIMETERS	INCHES
A	33.5 MAX.	1.32 MAX.
B	2.78	0.11
C	2.54	0.1
D	0.46	0.018
E	27.94	1.1
F	1.5	0.059
G	2.54 MIN.	0.1 MIN.
H	0.5 MIN.	0.019 MIN.
I	4.58 MAX.	0.181 MAX.
J	5.08 MAX.	0.2 MAX.
K	15.24	0.6
L	13.5	0.53
M	$0.25^{+0.10}_{-0.05}$	$0.01^{+0.004}_{-0.002}$

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PROGRAMMABLE COMMUNICATION INTERFACES

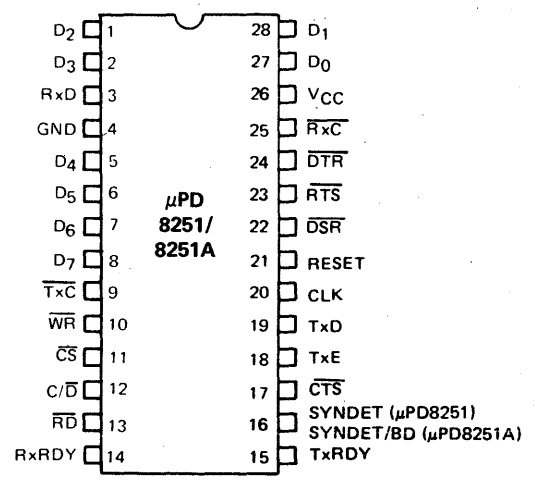
DESCRIPTION

The μPD8251 and μPD8251A Universal Synchronous/Asynchronous Receiver/Transmitters (USARTs) are designed for microcomputer systems data communications. The USART is used as a peripheral and is programmed by the μPD8080 or other processor to communicate in commonly used serial data transmission techniques including IBM Bi-Sync. The USART receives serial data streams and converts them into parallel data characters for the processor. While receiving serial data, the USART will also accept data characters from the processor in parallel format, convert them to serial format and transmit. The USART will signal the processor when it has completely received or transmitted a character and requires service. Complete USART status including data format errors and control signals such as TxE and SYNDET, is available to the processor at any time.

FEATURES

- Asynchronous or Synchronous Operation
  - Asynchronous:
    - 5-8 Bit Characters
    - Clock Rate – 1, 16 or 64 x Baud Rate
    - Break Character Generation
    - Select 1, 1-1/2, or 2 Stop Bits
    - False Start Bit Detector
    - Automatic Break Detect and Handling (μPD8251A)
  - Synchronous:
    - 5-8 Bit Characters
    - Internal or External Character Synchronization
    - Automatic Sync Insertion
    - Single or Double Sync Characters
- Baud Rate – Synchronous – DC to 56K Baud (μPD8251)
  – DC to 64K Baud (μPD8251A)
  – Asynchronous – DC to 9.6K Baud
- Full Duplex, Double Buffered Transmitter and Receiver
- Parity, Overrun and Framing Flags
- Fully Compatible with 8080/8085/μPD780 (Z80™)
- All Inputs and Outputs are TTL Compatible
- Single +5 Volt Supply
- Separate Device, Receive and Transmit TTL Clocks
- 28 Pin Plastic DIP Package
- N-Channel MOS Technology

PIN CONFIGURATION



PIN NAMES

D_7-D_0	Data Bus (8 bits)
C/D	Control or Data is to be Written or Read
RD	Read Data Command
WR	Write Data or Control Command
CS	Chip Enable
CLK	Clock Pulse (TTL)
RESET	Reset
TxC	Transmitter Clock (TTL)
TxD	Transmitter Data
RxC	Receiver Clock (TTL)
RxD	Receiver Data
RxRDY	Receiver Ready (has character for 8080)
TxRDY	Transmitter Ready (ready for char. from 8080)
DSR	Data Set Ready
DTR	Data Terminal Ready
SYNDET	Sync Detect
SYNDET/BD	Sync Detect/Break Detect
RTS	Request to Send Data
CTS	Clear to Send Data
TxE	Transmitter Empty
VCC	+5 Volt Supply
GND	Ground

*All data pertaining to the μPD8251A is preliminary

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Rev/2

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μPD8251/8251A

FUNCTIONAL DESCRIPTION

The μPD8251 and μPD8251A Universal Synchronous/Asynchronous Receiver/Transmitters are designed specifically for 8080 microcomputer systems but work with most 8-bit processors. Operation of the μPD8251 and μPD8251A, like other I/O devices in the 8080 family, are programmed by system software for maximum flexibility.

In the receive mode, the μPD8251 or μPD8251A converts incoming serial format data into parallel data and makes certain format checks. In the transmit mode, it formats parallel data into serial form. The device also supplies or removes characters or bits that are unique to the communication format in use. By performing conversion and formatting services automatically, the USART appears to the processor as a simple or "transparent" input or output of byte-oriented parallel data.

μPD8251A FEATURES AND ENHANCEMENTS

The μPD8251A is an advanced design of the industry standard 8251 USART. It operates with a wide range of microprocessors, including the 8080, 8085, and μPD780 (Z80™). The additional features and enhancements of the μPD8251A over the μPD8251 are listed below.

1. The data paths are double-buffered with separate I/O registers for control, status, Data In and Data Out. This feature simplifies control programming and minimizes processor overhead.
2. The Receiver detects and handles "break" automatically in asynchronous operations, which relieves the processor of this task.
3. The Receiver is prevented from starting when in "break" state by a refined Rx initialization. This also prevents a disconnected USART from causing unwanted interrupts.
4. When a transmission is concluded the TxD line will always return to the marking state unless SBRK is programmed.
5. The Tx Disable command is prevented from halting transmission by the Tx Enable Logic enhancement, until all data previously written has been transmitted. The same logic also prevents the transmitter from turning off in the middle of a word.
6. Internal Sync Detect is disabled when External Sync Detect is programmed. An External Sync Detect Status is provided through a flip-flop which clears itself upon a status read.
7. The possibility of a false sync detect is minimized by:
   - ensuring that if a double sync character is programmed, the characters be contiguously detected.
   - clearing the Rx register to all Logic 1s (V_{OH}) whenever the Enter Hunt command is issued in Sync mode.
8. The $\overline{RD}$ and $\overline{WR}$ do not affect the internal operation of the device as long as the μPD8251A is not selected.
9. The μPD8251A Status can be read at any time, however, the status update will be inhibited during status read.
10. The μPD8251A has enhanced AC and DC characteristics and is free from extraneous glitches, providing higher speed and improved operating margins.
11. Baud rate from DC to 64K.

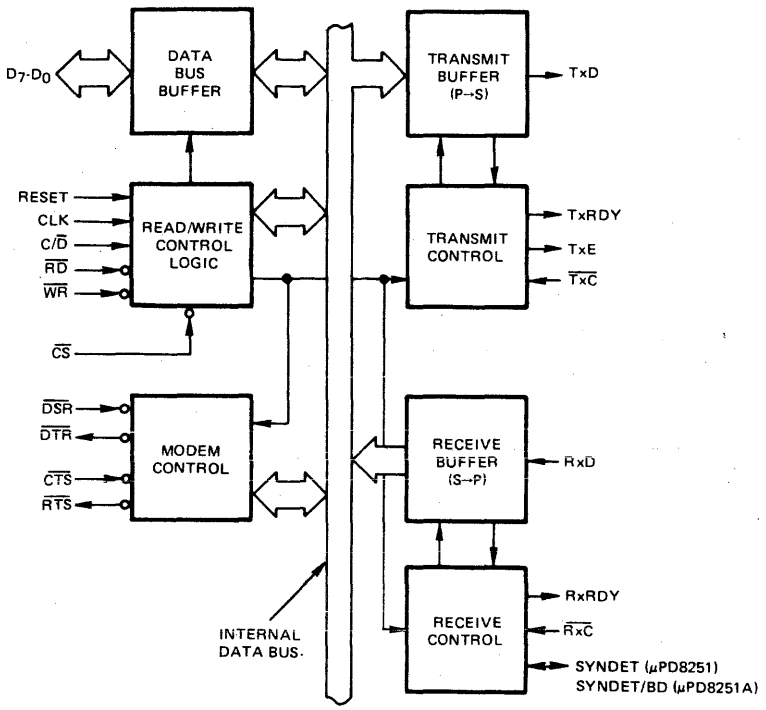
BASIC OPERATION

$C/\overline{D}$	$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	
0	0	1	0	μPD8251/μPD8251A → Data Bus
0	1	0	0	Data Bus → μPD8251/μPD8251A
1	0	1	0	Status → Data Bus
1	1	0	0	Data Bus → Control
X	X	X	1	Data Bus → 3-State
X	1	1	0	

TM: Z80 is a registered trademark of Zilog.

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BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	−0°C to +70°C
Storage Temperature	−65°C to +125°C
All Output Voltages	−0.5 to +7 Volts
All Input Voltages	−0.5 to +7 Volts
Supply Voltages	−0.5 to +7 Volts

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

DC CHARACTERISTICS

T_a = 0°C to 70°C; V_{CC} = 5.0V ± 5%; GND = 0V

PARAMETER	SYMBOL	LIMITS μPD8251 MIN	TYP	MAX	LIMITS μPD8251A MIN	MAX	UNIT	TEST CONDITIONS
Input Low Voltage	V_{IL}	−0.5		0.8	−0.5	0.8	V	
Input High Voltage	V_{IH}	2.0		V_{CC}	2.0	V_{CC}	V	
Output Low Voltage	V_{OL}			0.45		0.45	V	μPD8251: I_{OL} = 1.7 mA μPD8251A: I_{OL} = 2.2 mA
Output High Voltage	V_{OH}	2.4			2.4		V	μPD8251: I_{OH} = −100 μA μPD8251A: I_{OH} = −400 μA
Data Bus Leakage	I_{DL}			−50		−10	μA	V_{OUT} = 0.45V
				10		10		V_{OUT} = V_{CC}
Input Load Current	I_{IL}			10		10	μA	At 5.5V
Power Supply Current	I_{CC}		45	80		100	mA	μPD8251A: All Outputs = Logic 1

CAPACITANCE

T_a = 25°C; V_{CC} = GND = 0V

PARAMETER	SYMBOL	LIMITS MIN	TYP	MAX	UNIT	TEST CONDITIONS
Input Capacitance	C_{IN}			10	pF	fc = 1 MHz
I/O Capacitance	$C_{I/O}$			20	pF	Unmeasured pins returned to GND

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AC CHARACTERISTICS

T_a = 0°C to 70°C; V_{CC} = 5.0V ± 5%; GND = 0V.

PARAMETER	SYMBOL	LIMITS μPD8251 MIN	LIMITS μPD8251 MAX	LIMITS μPD8215A MIN	LIMITS μPD8215A MAX	UNIT	TEST CONDITIONS
READ							
Address Stable before $\overline{READ}$, ($\overline{CS}$, C/$\overline{D}$)	t_{AR}	50		0		ns	
Address Hold Time for $\overline{READ}$, ($\overline{CS}$, $\overline{CD}$)	t_{RA}	5		0		ns	
$\overline{READ}$ Pulse Width	t_{RR}	430		250		ns	
Data Delay from $\overline{READ}$	t_{RD}		350		200	ns	μPD8251: C_L = 100 pF μPD8251A: C_L = 150 pF
$\overline{READ}$ to Data Floating	t_{DF}	25	200	10	100	ns	μPD8251 C_L = 100 pF C_L = 15 pF
WRITE							
Address Stable before $\overline{WRITE}$	t_{AW}	20		0		ns	
Address Hold Time for $\overline{WRITE}$	t_{WA}	20		0		ns	
$\overline{WRITE}$ Pulse Width	t_{WW}	400		250		ns	
Data Set-Up Time for $\overline{WRITE}$	t_{DW}	200		150		ns	
Data Hold Time for $\overline{WRITE}$	t_{WD}	40		0		ns	
Recovery Time Between WRITES ②	t_{RV}	6		6		t_{CY}	
OTHER TIMING							
Clock Period ③	t_{CY}	0.420	1.35	0.32	1.35	μs	
Clock Pulse Width High	$t_{\phi W}$	220	0.7t_{CY}	120	t_{CY}-90	ns	
Clock Pulse Width Low	$t_{\overline{\phi}W}$			90		ns	
Clock Rise and Fall Time	$t_{R,tF}$	0	50	5	20	ns	
TxD Delay from Falling Edge of $\overline{TxC}$	t_{DTx}		1		1	μs	
Rx Data Set-Up Time to Sampling Pulse	t_{SRx}	2		2		μs	μPD8251: C_L = 100 pF
Rx Data Hold Time to Sampling Pulse	t_{HRx}	2		2		μs	
Transmitter Input Clock Frequency 1X Baud Rate 16X Baud Rate 64X Baud Rate	f_{Tx}	 DC DC DC	 56 520 520		 64 310 615	 kHz kHz kHz	
Transmitter Input Clock Pulse Width 1X Baud Rate 16X and 64X Baud Rate	t_{TPW}	 12 1		 12 1		 t_{CY} t_{CY}	
Transmitter Input Clock Pulse Delay 1X Baud Rate 16X and 64X Baud Rate	t_{TPD}	 15 3		 15 3		 t_{CY} t_{CY}	
Receiver Input Clock Frequency 1X Baud Rate 16X Baud Rate 64X Baud Rate	f_{Rx}	 DC DC DC	 56 520 520		 64 310 615	 kHz kHz kHz	
Receiver Input Clock Pulse Width 1X Baud Rate 16X and 64X Baud Rate	t_{RPW}	 12 1		 12 1		 t_{CY} t_{CY}	
Receiver Input Clock Pulse Delay 1X Baud Rate 16X and 64X Baud Rate	t_{RPD}	 15 3		 15 3		 t_{CY} t_{CY}	
TxRDY Delay from Center of Data Bit	t_{Tx}		16		8	t_{CY}	μPD8251: C_L = 50 pF
RxRDY Delay from Center of Data Bit	t_{RX}		20		24	t_{CY}	
Internal SYNDET Delay from Center of Data Bit	t_{IS}		25		24	t_{CY}	
External SYNDET Set-Up Time before Falling Edge of $\overline{RxC}$	t_{ES}	16	16		16	t_{CY}	
TxEMPTY Delay from Center of Data Bit	t_{TxE}		16		20	t_{CY}	μPD8251: C_L = 50 pF
Control Delay from Rising Edge of WRITE (TxE, $\overline{DTR}$, $\overline{RTS}$)	t_{WC}				8	t_{CY}	
Control to READ Set-Up Time ($\overline{DSR}$, $\overline{CTS}$)	t_{CR}	16			20	t_{CY}	

Notes: ① AC timings measured at V_{OH} = 2.0, V_{OL} = 0.8, and with load circuit of Figure 1.

② This recovery time is for initialization only, when MODE, SYNC1, SYNC2, COMMAND and first DATA BYTES are written into the USART. Subsequent writing of both COMMAND and DATA are only allowed when TxRDY = 1.

③ The TxC and RxC frequencies have the following limitations with respect to CLK.
- For 1X Baud Rate, f_{Tx} or $f_{Rx} \leq 1/(30\ t_{CY})$
- For 16X and 64X Baud Rate, f_{TX} or $f_{Rx} \leq 1/(4.5\ t_{CY})$

④ Reset Pulse Width = 6 t_{CY} minimum.

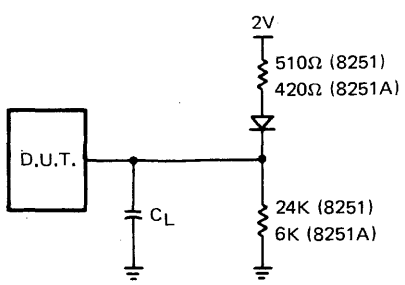
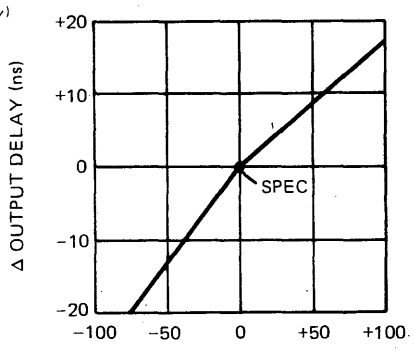


Figure 1.



Typical Δ Output Delay Versus Δ Capacitance (pF)

TEST LOAD CIRCUIT

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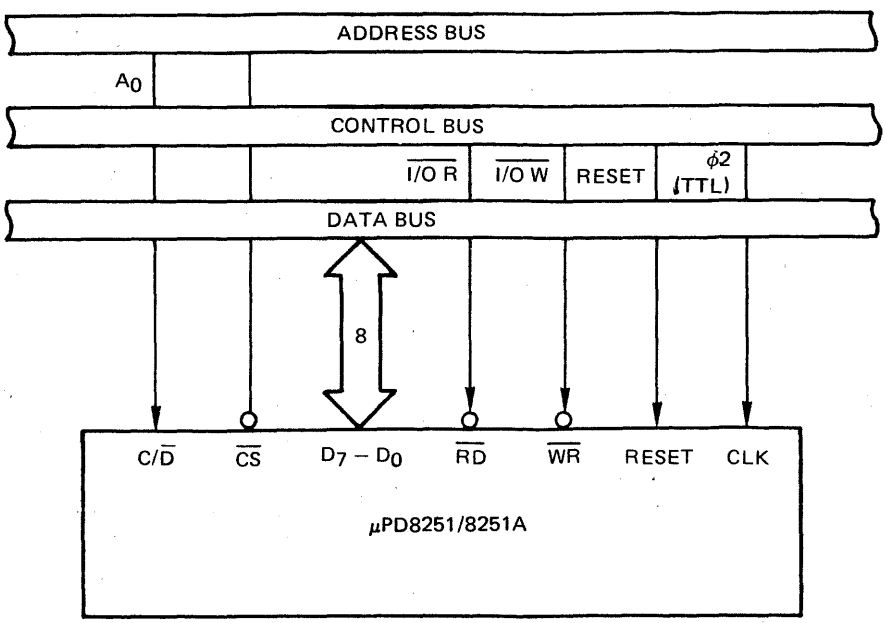
TRANSMIT BUFFER/ CONVERTER

The Transmit Buffer/Converter receives parallel data from the Data Bus Buffer via the internal data bus, converts parallel to serial data, inserts the necessary characters or bits needed for the programmed communication format and outputs composite serial data on the TxD output.

PIN IDENTIFICATION (CONT.)

PIN NO.	PIN SYMBOL	PIN NAME	FUNCTION
Transmit Control Logic			The Transmit Control Logic accepts and outputs all external and internal signals necessary for serial data transmission.
15	TxRDY	Transmitter Ready	Transmitter Ready signals the processor that the transmitter is ready to accept a data character. TxRDY can be used as an interrupt or may be tested through the Status information for Polled operation. Loading a character from the processor automatically resets TxRDY.
18	TxE	Transmitter Empty	The Transmitter Empty output signals the processor that the USART has no further characters to transmit. TxE is automatically reset upon receiving a data character from the processor. In half-duplex, TxE can be used to signal end of a transmission and request the processor to "turn the line around." The TxEn bit in the command instruction does not effect TxE. In the Synchronous mode, a "one" on this output indicates that a Sync character or characters are about to be automatically transmitted as "fillers" because the next data character has not been loaded.
9	$\overline{TxC}$	Transmitter Clock	The Transmitter Clock controls the serial character transmission rate. In the Asynchronous mode, the $\overline{TxC}$ frequency is a multiple of the actual Baud Rate. Two bits of the Mode Instruction select the multiple to be 1x, 16x, or 64x the Baud Rate. In the Synchronous mode, the $\overline{TxC}$ frequency is automatically selected to equal the actual Baud Rate. Note that for both Synchronous and Asynchronous modes, serial data is shifted out of the USART by the falling edge of $\overline{TxC}$.
19	TxD	Transmitter Data	The Transmit Control Logic outputs the composite serial data stream on this pin.

μPD8251 AND μPD8251A INTERFACE TO 8080 STANDARD SYSTEM BUS



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RECEIVER BUFFER

The Receiver Buffer accepts serial data input at the $\overline{RxD}$ pin and converts the data from serial to parallel format. Bits or characters required for the specific communication technique in use are checked and then an eight-bit "assembled" character is readied for the processor. For communication techniques which require less than eight bits, the μPD8251 and μPD8251A sets the extra bits to "zero."

PIN IDENTIFICATION (CONT.)

PIN NO.	PIN SYMBOL	PIN NAME	FUNCTION
Receiver Control Logic			This block manages all activities related to incoming data.
14	RxRDY	Receiver Ready	The Receiver Ready output indicates that the Receiver Buffer is ready with an "assembled" character for input to the processor. For Polled operation, the processor can check RxRDY using a Status Read or RxRDY can be connected to the processor interrupt structure. Note that reading the character to the processor automatically resets RxRDY.
25	$\overline{RxC}$	Receiver Clock	The Receiver Clock is the rate at which the incoming character is received. In the Asynchronous mode, the $\overline{RxC}$ frequency may be 1,16 or 64 times the actual Baud Rate but in the Synchronous mode the $\overline{RxC}$ frequency must equal the Baud Rate. Two bits in the mode instruction select Asynchronous at 1x, 16x or 64x or Synchronous operation at 1x the Baud Rate. Unlike $\overline{TxC}$, data is sampled by the μPD8251 and μPD8251A on the rising edge of $\overline{RxC}$. ①
3	RxD	Receiver Data	A composite serial data stream is received by the Receiver Control Logic on this pin.
16	SYNDET (μPD8251)	Sync Detect	The SYNC Detect pin is only used in the Synchronous mode. The μPD8251 may be programmed through the Mode Instruction to operate in either the internal or external Sync mode and SYNDET then functions as an output or input respectively. In the internal Sync mode, the SYNDET output will go to a "one" when the μPD8251 has located the SYNC character in the Receive mode. If double SYNC character (bi-sync) operation has been programmed, SYNDET will go to "one" in the middle of the last bit of the second SYNC character. SYNDET is automatically reset to "zero" upon a Status Read or RESET. In the external SYNC mode, a "zero" to "one" transition on the SYNDET input will cause the μPD8251 to start assembling data character on the next falling edge of $\overline{RxC}$. The length of the SYNDET input should be at least one $\overline{RxC}$ period, but may be removed once the μPD8251 is in SYNC.
16	SYNDET/BD (μPD8251A)	Sync Detect/ Break Detect	The SYNDET/BD pin is used in both Synchronous and Asynchronous modes. When in SYNC mode the features for the SYNDET pin described above apply. When in Asynchronous mode, the Break Detect output will go high when an all zero word of the programmed length is received. This word consists of: start bit, data bit, parity bit and one stop bit. Reset only occurs when Rx data returns to a logic one state or upon chip reset. The state of Break Detect can be read as a status bit.

Note: ① Since the μPD8251 and μPD8251A will frequently be handling both the reception and transmission for a given link, the Receive and Transmit Baud Rates will be same. $\overline{RxC}$ and $\overline{TxC}$ then require the same frequency and may be tied together and connected to a single clock source or Baud Rate Generator.

Examples:

If the Baud Rate equals 110 (Async):
- $\overline{RxC}$ or $\overline{TxC}$ equals 110 Hz (1x)
- $\overline{RxC}$ or $\overline{TxC}$ equals 1.76 KHz (16x)
- $\overline{RxC}$ or $\overline{TxC}$ equals 7.04 KHz (64x)

If the Baud Rate equals 300:
- $\overline{RxC}$ or $\overline{TxC}$ equals 300 Hz (1x) A or S
- $\overline{RxC}$ or $\overline{TxC}$ equals 4800 Hz (16x) A only
- $\overline{RxC}$ or $\overline{TxC}$ equals 19.2 KHz (64x) A only

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OPERATIONAL DESCRIPTION

A set of control words must be sent to the μPD8251 and μPD8251A to define the desired mode and communications format. The control words will specify the BAUD RATE FACTOR (1x, 16x, 64x), CHARACTER LENGTH (5 to 8), NUMBER OF STOP BITS (1, 1-1/2, 2) ASYNCHRONOUS or SYNCHRONOUS MODE, SYNDET (IN or OUT), PARITY, etc.

After receiving the control words, the μPD8251 and μPD8251A are ready to communicate. TxRDY is raised to signal the processor that the USART is ready to receive a character for transmission. When the processor writes a character to the USART, TxRDY is automatically reset.

Concurrently, the μPD8251 and μPD8251A may receive serial data; and after receiving an entire character, the RxRDY output is raised to indicate a completed character is ready for the processor. The processor fetch will automatically reset RxRDY.

Note: The μPD8251 and μPD8251A may provide faulty RxRDY for the first read after power-on or for the first read after receive is re-enabled by a command instruction (RxE). A dummy read is recommended to clear faulty RxRDY. But this is not the case for the first read after hardware or software reset after the device operation has once been established.

The μPD8251 and μPD8251A cannot transmit until the TxEN (Transmitter Enable) bit has been set by a Command Instruction and until the $\overline{CTS}$ (Clear to Send) input is a "zero". TxD is held in the "marking" state after Reset awaiting new Command Words.

μPD8251 PROGRAMMING

The USART must be loaded with a group of two to four control words provided by the processor before data reception and transmission can begin. A Reset (internal or external) must immediately proceed the control words which are used to program the complete operational description of the communications interface. If an external RESET is not available, three successive 00 Hex or two successive 80 Hex command instructions ($C/\overline{D}$ = 1) followed by a software reset command instruction (40 Hex) can be used to initialize the μPD8251 and μPD8251A.

There are two control word formats:

1. Mode Instruction
2. Command Instruction

MODE INSTRUCTION

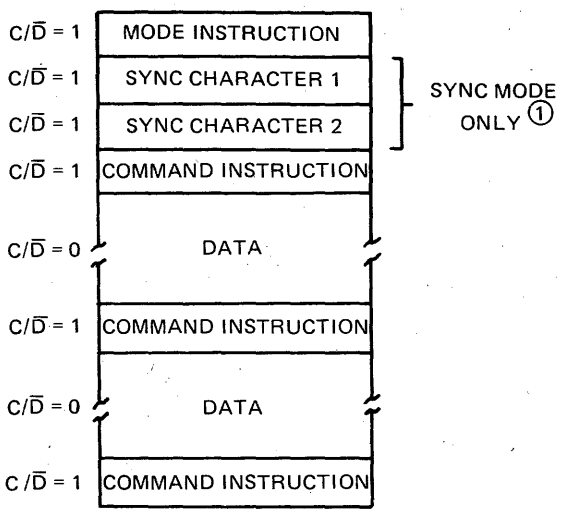
This control word specifies the general characteristics of the interface regarding the SYNCHRONOUS or ASYNCHRONOUS MODE, BAUD RATE FACTOR, CHARACTER LENGTH, PARITY, and NUMBER OF STOP BITS. Once the Mode Instruction has been received, SYNC characters or Command Instructions may be inserted depending on the Mode Instruction content.

COMMAND INSTRUCTION

This control word will be interpreted as a SYNC character definition if immediately preceded by a Mode Instruction which specified a Synchronous format. After the SYNC character(s) are specified or after an Asynchronous Mode Instruction, all subsequent control words will be interpreted as an update to the Command Instruction. Command Instruction updates may occur at any time during the data block. To modify the Mode Instruction, a bit may be set in the Command Instruction which causes an internal Reset which allows a new Mode Instruction to be accepted.

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TYPICAL DATA BLOCK



NOTE (1) The second SYNC character is skipped if MODE instruction has programmed the μPD8251 and μPD8251A to single character Internal SYNC Mode. Both SYNC characters are skipped if MODE instruction has programmed the μPD8251 and μPD8251A to ASYNC mode.

MODE INSTRUCTION DEFINITION

The μPD8251 and μPD8251A can operate in either Asynchronous or Synchronous communication modes. Understanding how the Mode Instruction controls the functional operation of the USART is easiest when the device is considered to be two separate components, one asynchronous and the other synchronous, which share the same support circuits and package. Although the format definition can be changed at will or "on the fly", the two modes will be explained separately for clarity.

ASYNCHRONOUS TRANSMISSION

When a data character is written into the μPD8251 and μPD8251A, the USART automatically adds a START bit (low level or "space") and the number of STOP bits (high level or "mark") specified by the Mode Instruction. If Parity has been enabled, an odd or even Parity bit is inserted just before the STOP bit(s), as specified by the Mode Instruction. Then, depending on $\overline{CTS}$ and TxEN, the character may be transmitted as a serial data stream at the TxD output. Data is shifted out by the falling edge of $\overline{TxC}$ at $\overline{TxC}$, $\overline{TxC}$/16 or $\overline{TxC}$/64, as defined by the Mode Instruction.

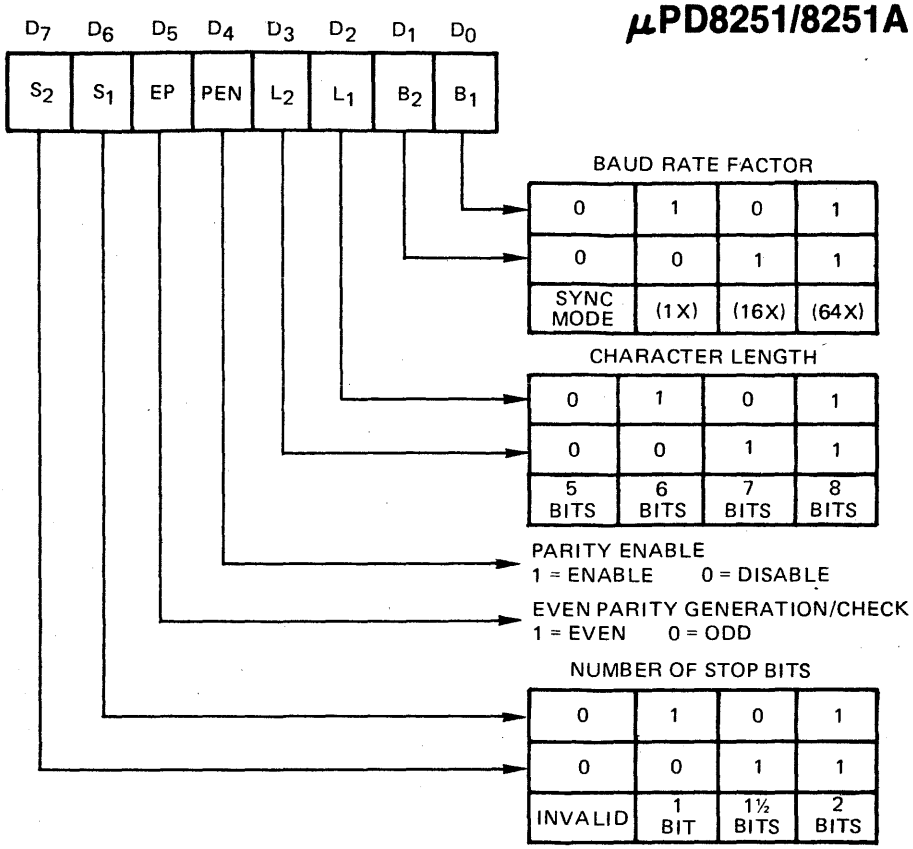
If no data characters have been loaded into the μPD8251 and μPD8251A, or if all available characters have been transmitted, the TxD output remains "high" (marking) in preparation for sending the START bit of the next character provided by the processor. TxD may be forced to send a BREAK (continuously low) by setting the correct bit in the Command Instruction.

ASYNCHRONOUS RECEIVE

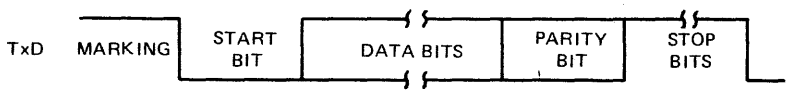
The RxD input line is normally held "high" (marking) by the transmitting device. A falling edge at RxD signals the possible beginning of a START bit and a new character. The START bit is checked by testing for a "low" at its nominal center as specified by the BAUD RATE. If a "low" is detected again, it is considered valid, and the bit assembling counter starts counting. The bit counter locates the approximate center of the date, parity (if specified), and STOP bits. The parity error flag (PE) is set, if a parity error occurs. Input bits are sampled at the RxD pin with the rising edge of $\overline{RxC}$. If a high is not detected for the STOP bit, which normally signals the end of an input character, a framing error (FE) will be set. After a valid STOP bit, the input character is loaded into the parallel Data Bus Buffer of the μPD8251 and μPD8251A and the RxRDY signal is raised to indicate to the processor that a character is ready to be fetched. If the processor has failed to fetch the previous character, the new character replaces the old and the overrun flag (OE) is set. All the error flags can be reset by setting a bit in the Command Instruction. Error flag conditions will not stop subsequent USART operation.

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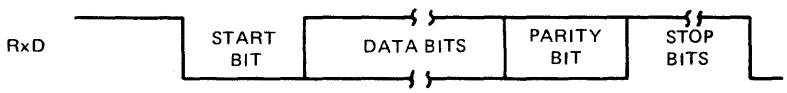
MODE INSTRUCTION FORMAT ASYNCHRONOUS MODE



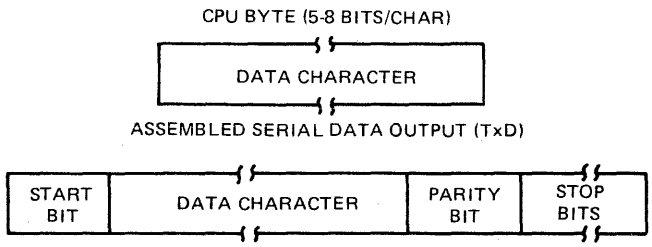
TRANSMIT/RECEIVE FORMAT ASYNCHRONOUS MODE



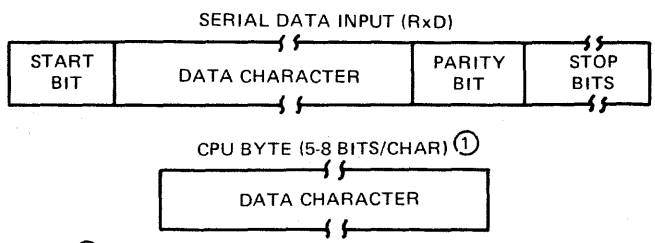
TRANSMITTER OUTPUT



RECEIVER INPUT



TRANSMISSION FORMAT



NOTE ①: IF CHARACTER LENGTH IS DEFINED AS 5, 6, OR 7 BITS; THE UNUSED BITS ARE SET TO "ZERO."

RECEIVE FORMAT

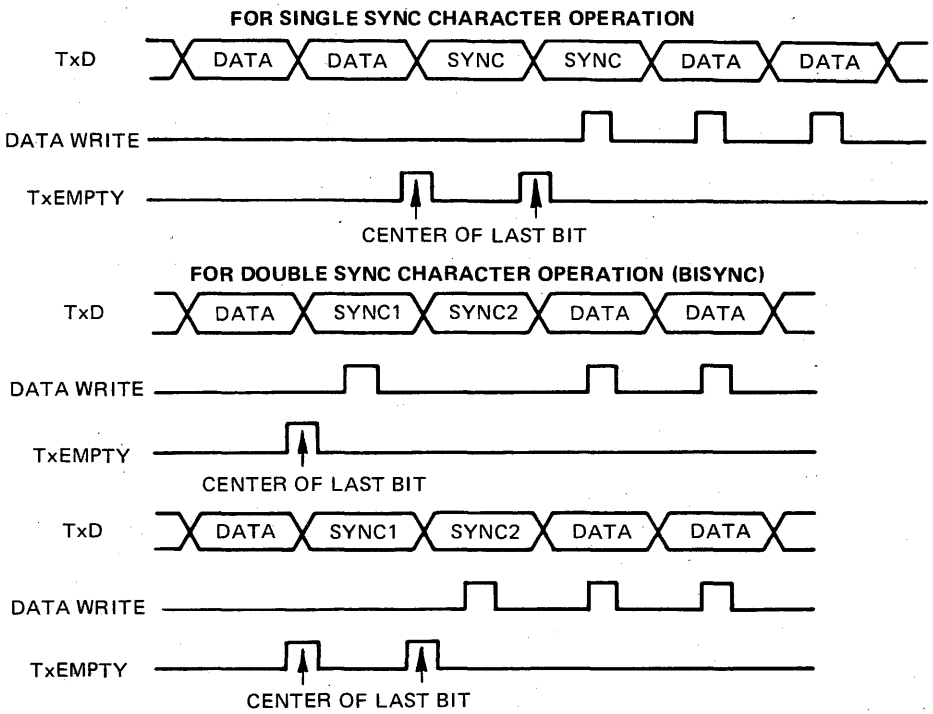
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SYNCHRONOUS TRANSMISSION

As in Asynchronous transmission, the TxD output remains "high" (marking) until the μPD8251 and μPD8251A receive the first character from the processor which is usually a SYNC character. After a Command Instruction has set TxEN and after Clear to Send ($\overline{CTS}$) goes low, the first character is serially transmitted. Data is shifted out on the falling edge of $\overline{TxC}$ and the same rate as $\overline{TxC}$.

Once transmission has started, Synchronous Mode format requires that the serial data stream at TxD continue at the $\overline{TxC}$ rate or SYNC will be lost. If a data character is not provided by the processor before the μPD8251 and μPD8251A Transmitter Buffer becomes empty, the SYNC character(s) loaded directly following the Mode Instruction will be automatically inserted in the TxD data stream. The SYNC character(s) are inserted to fill the line and maintain synchronization until new data characters are available for transmission. If the μPD8251 and μPD8251A become empty, and must send the SYNC character(s), the TxEMPTY output is raised to signal the processor that the Transmitter Buffer is empty and SYNC characters are being transmitted. TxEMPTY is automatically reset by the next character from the processor.

TxEMPTY go high at the middle of the last data bit when the Transmit Register is EMPTY. TxEMPTY goes low again as sync characters are transmitted. See figure below.



SYNCHRONOUS RECEIVE

In Synchronous Receive, character synchronization can be either external or internal. If the internal SYNC mode has been selected, and the Enter HUNT (EH) bit has been set by a Command Instruction, the receiver goes into the HUNT mode.

Incoming data on the RxD input is sampled on the rising edge of $\overline{RxC}$, and the Receiver Buffer is compared with the first SYNC character after each bit has been loaded until a match is found. If two SYNC characters have been programmed, the next received character is also compared. When the SYNC character(s) programmed have been detected, the μPD8251 and μPD8251A leave the HUNT mode and are in character synchronization. At this time, the SYNDET (output) is set high. SYNDET is automatically reset by a STATUS READ.

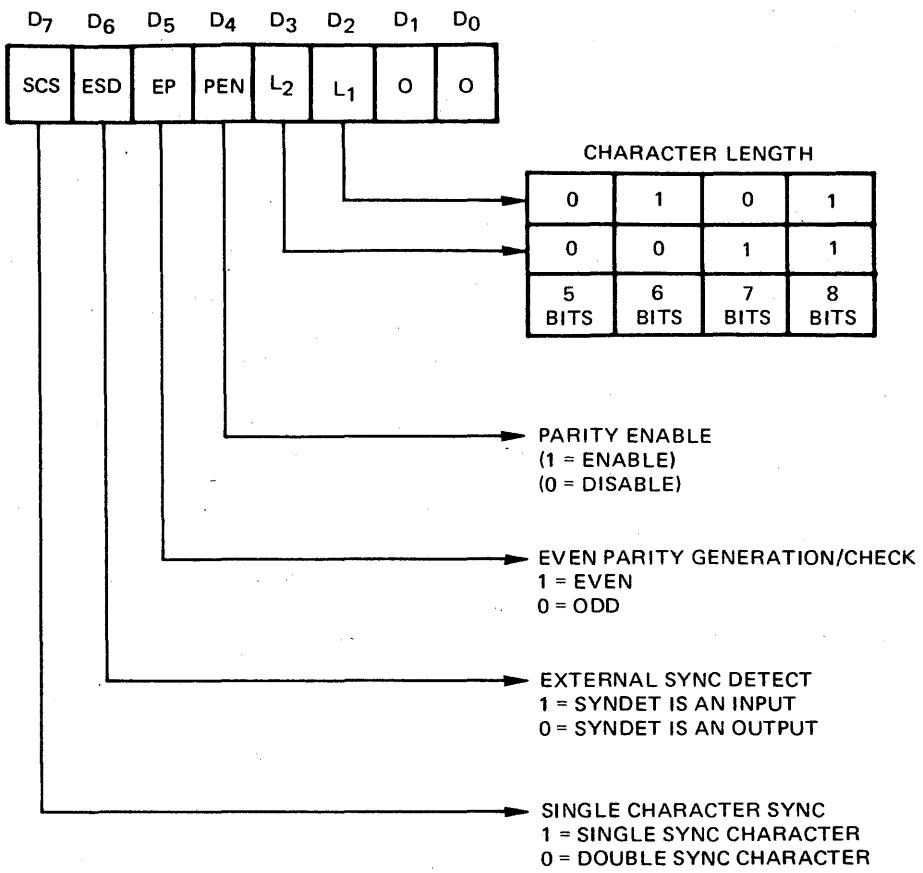
If external SYNC has been specified in the Mode Instruction, a "one" applied to the SYNDET (input) for at least one $\overline{RxC}$ cycle will synchronize the USART.

Parity and Overrun Errors are treated the same in the Synchronous as in the Asynchronous Mode. Framing errors do not apply in the Synchronous format.

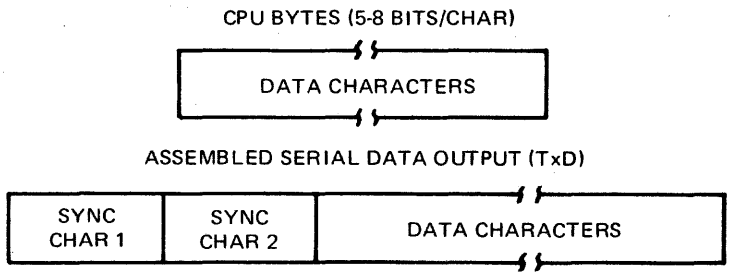
The processor may command the receiver to enter the HUNT mode with a Command Instruction which sets Enter HUNT (EH) if synchronization is lost.

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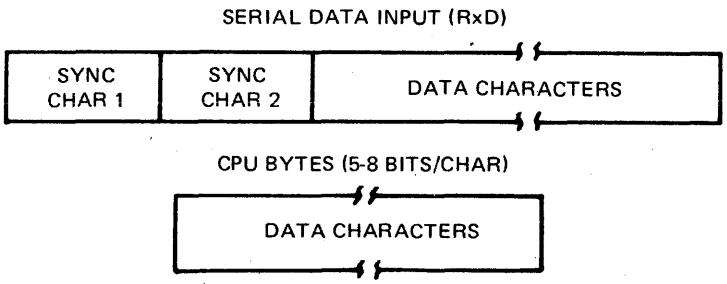
MODE INSTRUCTION FORMAT SYNCHRONOUS MODE



TRANSMIT/RECEIVE FORMAT SYNCHRONOUS MODE



TRANSMIT FORMAT



RECEIVE FORMAT

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COMMAND INSTRUCTION FORMAT

After the functional definition of the μPD8251 and μPD8251A has been specified by the Mode Instruction and the SYNC character(s) have been entered, if in SYNC mode, the USART is ready to receive Command Instructions and begin communication. A Command Instruction is used to control the specific operation of the format selected by the Mode Instruction. Enable Transmit, Enable Receive, Error Reset and Modem Controls are controlled by the Command Instruction.

After the Mode Instruction and the SYNC character(s), as needed, are loaded, all subsequent "control writes" ($C/\overline{D} = 1$) will load or overwrite the Command Instruction register. A Reset operation (internal via CMD IR or external via the RESET input) will cause the μPD8251 and μPD8251A to interpret the next "control write", which must immediately follow the reset, as a Mode Instruction.

STATUS READ FORMAT

It is frequently necessary for the processor to examine the "status" of an active interface device to determine if errors have occurred or to notice other conditions which require a response from the processor. The μPD8251 and μPD8251A have features which allow the processor to "read" the device status at any time. A data fetch is issued by the processor while holding the $C/\overline{D}$ input "high" to obtain device Status Information. Many of the bits in the status register are copies of external pins. This dual status arrangement allows the μPD8251 and μPD8251A to be used in both Polled and interrupt driven environments. Status update can have a maximum delay of a 16 clock period.

PARITY ERROR

When a parity error is detected, the PE flag is set, and is cleared by setting the ER bit in a subsequent Command Instruction. PE being set does not inhibit USART operation.

OVERRUN ERROR

If the processor fails to read a data character before the one following is available, the OE flag is set, and is cleared by setting the ER bit in a subsequent Command Instruction. Although OE being set does not inhibit USART operation, the previously received character is overwritten and lost.

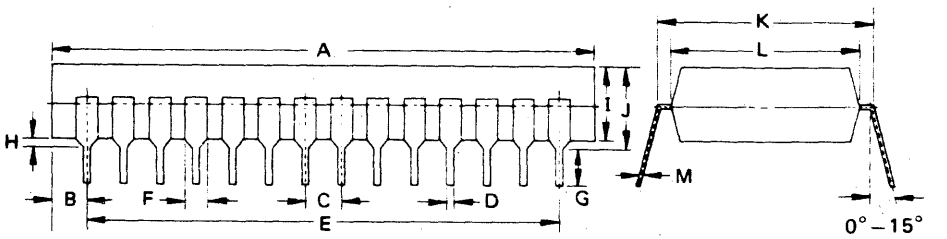
FRAMING ERROR①

If a valid STOP bit is not detected at the end of a character, the FE flag is set, and is cleared by setting the ER bit in a subsequent Command Instruction. FE being set does not inhibit USART operation.

Note: ① ASYNC mode only.

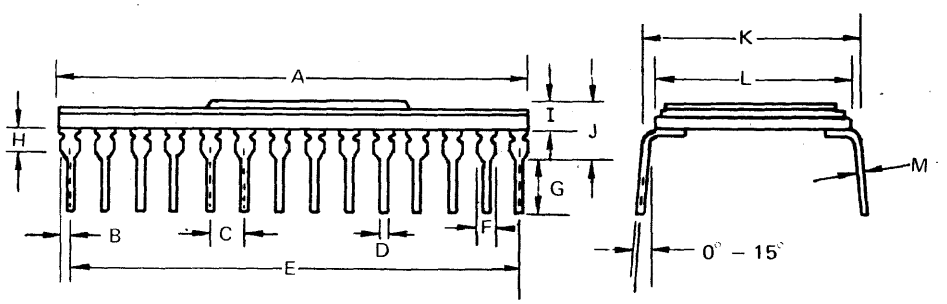
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PACKAGE OUTLINES
μPD8251C/D
μPD8251AC/D



Plastic

ITEM	MILLIMETERS	INCHES
A	38.0 MAX.	1.496 MAX.
B	2.49	0.098
C	2.54	0.10
D	0.5 ± 0.1	0.02 ± 0.004
E	33.02	1.3
F	1.5	0.059
G	2.54 MIN.	0.10 MIN.
H	0.5 MIN.	0.02 MIN.
I	5.22 MAX.	0.205 MAX.
J	5.72 MAX.	0.225 MAX.
K	15.24	0.6
L	13.2	0.52
M	$0.25^{+0.10}_{0.05}$	$0.01^{+0.004}_{0.002}$



Ceramic

ITEM	MILLIMETERS	INCHES
A	36.0 MAX.	1.41 MAX.
B	1.5 MAX.	0.059 MAX
C	2.54	0.1
D	0.50 ± 0.1	0.02 ± 0.004
E	33.0	1.299
F	1.27	0.05
G	3.2 MIN.	0.126 MIN
H	1.0 MIN	0.04 MIN
I	3.3 MAX.	0.13 MAX.
J	5.2 MAX.	0.20 MAX.
K	15.3	0.60
L	13.9	0.55
M	0.30 ± 0.1	0.012 ± 0.004

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PROGRAMMABLE INTERVAL TIMER

DESCRIPTION

The NEC μPD8253 contains three independent, programmable, multi-modal 16-bit counter/timers. It is designed as a general purpose device, fully compatible with the 8080 family. The μPD8253 interfaces directly to the busses of the processor as an array of I/O ports.

The μPD8253 can generate accurate time delays under the control of system software. The three independent 16-bit counters can be clocked at rates from DC to 2 MHz. The system software controls the loading and starting of the counters to provide accurate multiple time delays. The counter output flags the processor at the completion of the time-out cycles.

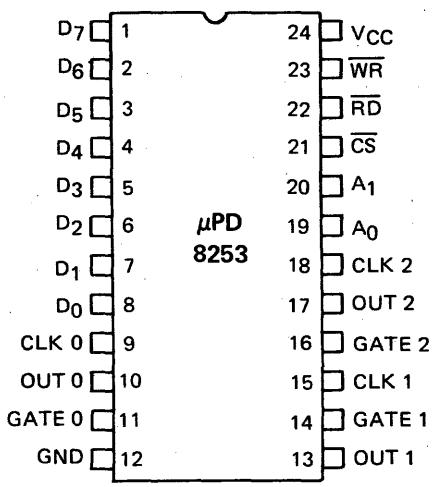
System overhead is greatly improved by relieving the software from the maintenance of timing loops. Some other common uses for the μPD8253 in microprocessor based systems are:

- Programmable Baud Rate Generator
- Event Counter
- Binary Rate Multiplier
- Real Time Clock
- Digital One-Shot
- Complex Motor Controller

FEATURES

- Three Indpendent 16-Bit Counters
- Clock Rate: DC to 3 MHz
- Programmable Counter Modes
- Count Binary or BCD
- Single +5 Volt Supply
- 24 Pin Dual-In-Line Plastic Package

PIN CONFIGURATION



PIN NAMES

D_7-D_0	Data Bus (8-Bit)
CLK N	Counter Clock Inputs
GATE N	Counter Gate Inputs
OUT N	Counter Outputs
$\overline{RD}$	Read Counter
$\overline{WR}$	Write Command or Data
$\overline{CS}$	Chip Select
A_0, A_1	Counter Select
V_{CC}	+5 Volts
GND	Ground

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FUNCTIONAL DESCRIPTION

Data Bus Buffer

The 3-state, 8-bit, bi-directional Data Bus Buffer interfaces the μPD8253 to the 8080A microprocessor system. It will transmit or receive data in accordance with the INput or OUTput instructions executed by the processor. There are three basic functions of the Data Bus Buffer.

1. Program the modes of the μPD8253
2. Load the count registers.
3. Read the count values.

Read/Write Logic

The Read/Write Logic controls the overall operation of the μPD8253 and is governed by inputs received from the processor system bus.

Control Word Register

Two bits from the address bus of the processor, A_0 and A_1, select the Control Word Register when both are at a logic "1" (active-high logic). When selected, the Control Word Register stores data from the Data Bus Buffer in a register. This data is then used to control:

1. The operational MODE of the counters.
2. The selection of BCD or Binary counting.
3. The loading of the count registers.

$\overline{RD}$ (Read)

This active-low signal instructs the μPD8253 to transmit the selected counter value to the processor.

$\overline{WR}$ (Write)

This active-low signal instructs the μPD8253 to receive MODE information or counter input data from the processor.

A_1, A_0

The A_1 and A_0 inputs are normally connected to the address bus of the processor. They control the one-of-three counter selection and address the control word register to select one of the six operational MODES.

$\overline{CS}$ (Chip Select)

The μPD8253 is enabled when an active-low signal is applied to this input. Reading or writing from this device is inhibited when the chip is disabled. The counter operation, however, is not affected.

Counters #0, #1, #2

The three identical, 16-bit down counters are functionally independent allowing for separate MODE configuration and counting operation. They function as Binary or BCD counters with their gate, input and output line configuration determined by the operational MODE data stored in the Control Word Register. The system software overhead time can be reduced by allowing the control word to govern the loading of the count data.

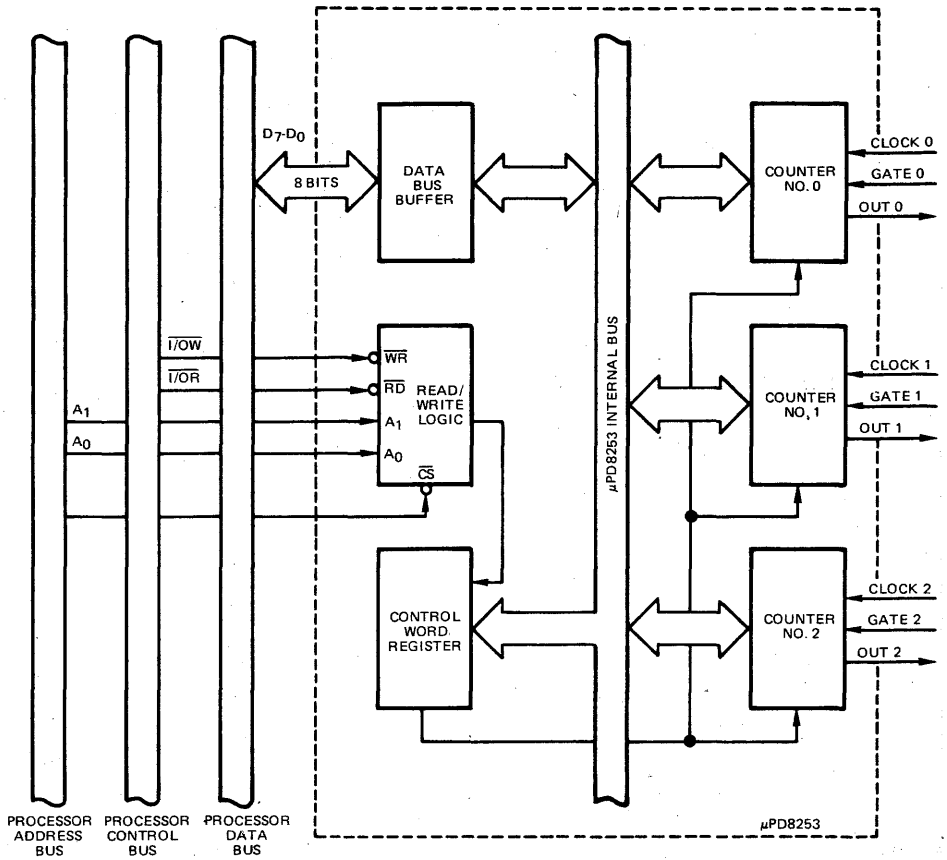
The programmer, with READ operations, has access to each counter's contents. The μPD8253 contains the commands and logic to read each counter's contents while still counting without disturbing its operation.

The following is a table showing how the counters are manipulated by the input signals to the Read/Write Logic.

$\overline{CS}$	$\overline{RD}$	$\overline{WR}$	A_1	A_0	FUNCTION
0	1	0	0	0	Load Counter No. 0
0	1	0	0	1	Load Counter No. 1
0	1	0	1	0	Load Counter No. 2
0	1	0	1	1	Write Mode Word
0	0	1	0	0	Read Counter No. 0
0	0	1	0	1	Read Counter No. 1
0	0	1	1	0	Read Counter No. 2
0	0	1	1	1	No-Operation, 3-State
1	X	X	X	X	Disable, 3-State
0	1	1	X	X	No-Operation, 3-State

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BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	0°C to +70°C
Storage Temperature	−65°C to +125°C
Voltage on Any Pin	−0.5 to +7 Volts (1)

Note: (1) With respect to ground.

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device realiability.

*T_a = 25°C

DC CHARACTERISTICS

T_a = 0°C to +70°C; V_{CC} = +5V ±5%

PARAMETER	SYMBOL	LIMITS MIN	TYP	MAX	UNIT	TEST CONDITIONS
Input Low Voltage	V_{IL}	−0.5		0.8	V	
Input High Voltage	V_{IH}	2.0		V_{CC}+0.5	V	
Output Low Voltage	V_{OL}			0.45	V	I_{OL} = 2.2 mA
Output High Voltage	V_{OH}	2.4			V	I_{OH} = −400 μA
Input Load Current	I_{IL}			±10	μA	V_{IN} = V_{CC} to 0 V
Output Float Leakage Current	I_{OFL}			±10	μA	V_{OUT} = V_{CC} to 0 V
V_{CC} Supply Current	I_{CC}			95	mA	

CAPACITANCE

T_a = 25°C; V_{CC} = GND = 0V

PARAMETER	SYMBOL	LIMITS MIN	TYP	MAX	UNIT	TEST CONDITIONS
Input Capacitance	C_{IN}			10	pF	f_c = 1 MHz
Input/Output Capacitance	$C_{I/O}$			20	pF	Unmeasured pins returned to V_{SS}

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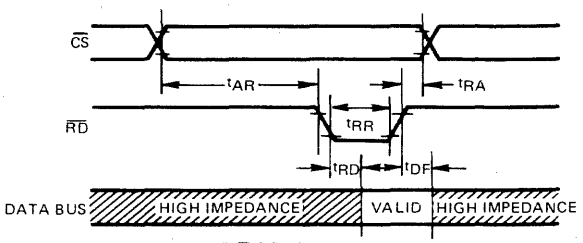
AC CHARACTERISTICS ①

T_a = 0°C to +70°C; V_{CC} = +5 V ± 5%; GND = 0 V

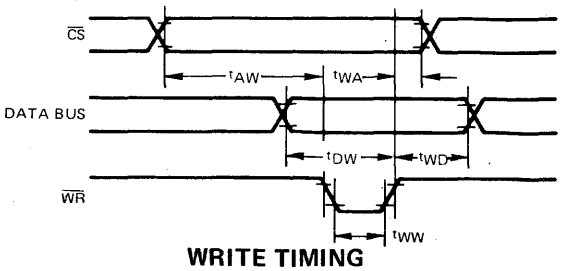
PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
READ						
Address Stable Before $\overline{READ}$	t_{AR}	50			ns	
Address Hold Time for $\overline{READ}$	t_{RA}	5			ns	
$\overline{READ}$ Pulse Width	t_{RR}	400			ns	
Data Delay from $\overline{READ}$	t_{RD}			300	ns	CL = 100 pF
$\overline{READ}$ to Data Floating	t_{DF}	25		125	ns	CL = 100 pF
WRITE						
Address Stable Before $\overline{WRITE}$	t_{AW}	20			ns	
Address Hold Time for $\overline{WRITE}$	t_{WA}	20			ns	
$\overline{WRITE}$ Pulse Width	t_{WW}	400			ns	
Data Set Up Time for $\overline{WRITE}$	t_{DW}	200			ns	
Data Hold Time for $\overline{WRITE}$	t_{WD}	40			ns	
Recovery Time Between $\overline{WRITES}$	t_{RV}	1			μs	
CLOCK AND GATE TIMING						
Clock Period	t_{CLK}	300		DC	ns	
High Pulse Width	t_{PWH}	200			ns	
Low Pulse Width	t_{PWL}	100			ns	
Gate Pulse Width High	t_{GW}	150			ns	
Gate Set Up Time to Clock ↑	t_{GS}	100			ns	
Gate Hold Time After Clock ↑	t_{GH}	50			ns	
Low Gate Width	t_{GL}	100			ns	
Output Delay from Clock ↓	t_{OD}			300	ns	CL = 100 pF
Output Delay from Gate	t_{ODG}			300	ns	CL = 100 pF

Note: ① AC Timing Measured at V_{OH} = 2.2 V; V_{OL} = 0.8 V.

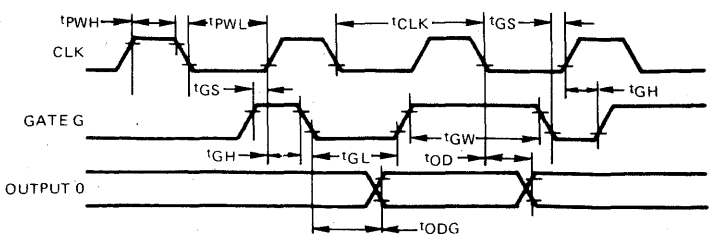
TIMING WAVEFORMS



READ TIMING



WRITE TIMING



CLOCK AND GATE TIMING

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PROGRAMMING THE μPD8253

The programmer can select any of the six operational MODES for the counters using system software. Individual counter programming is accomplished by loading the CONTROL WORD REGISTER with the appropriate control word data (A_0, A_1 = 11).

CONTROL WORD FORMAT

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
SC1	SC0	RL1	RL0	M2	M1	M0	BCD

SC – Select Counter

SC1	SC0	
0	0	Select Counter 0
0	1	Select Counter 1
1	0	Select Counter 2
1	1	Invalid

RL – Read/Load

RL1	RL0	
0	0	Counter Latching Operation
1	0	Read/Load Most Significant Byte Only
0	1	Read/Load Least Significant Byte Only
1	1	Read/Load Least Significant Byte First, Then Most Significant Byte

BCD

0	Binary Counter, 16-Bits
1	BCD Counter, 4-Decades

M-Mode

M2	M1	M0	
0	0	0	Mode 0
0	0	1	Mode 1
X	1	0	Mode 2
X	1	1	Mode 3
1	0	0	Mode 4
1	0	1	Mode 5

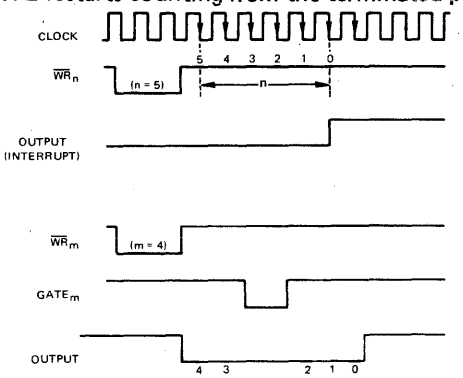
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OPERATIONAL MODES ①

Each of the three counters can be individually programmed with different operating MODES by appropriately formatted Control Words. The following is a summary of the MODE operations.

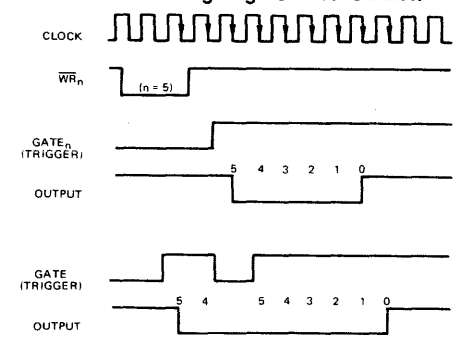
Mode 0: Interrupt on Terminal Count

The initial MODE set operation forces the OUTPUT low. When the specified counter is loaded with the count value, it will begin counting. The OUTPUT will remain low until the terminal count sets it high. It will remain in the high state until the trailing edge of the second $\overline{WR}$ pulse loads in COUNT data. If data is loaded during the counting process, the first $\overline{WR}$ stops the count. Counting starts with the new count data triggered by the falling clock edge after the second $\overline{WR}$. If a GATE pulse is asserted while counting, the count is terminated for the duration of GATE. The falling edge of CLK following the removal of GATE restarts counting from the terminated point.



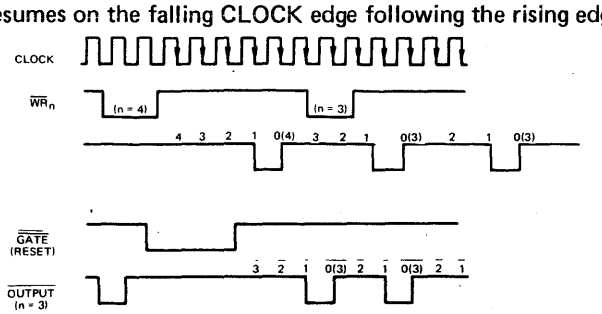
Mode 1: Programmable One-Shot

The OUTPUT is set low by the falling edge of CLOCK following the trailing edge of GATE. The OUTPUT is set high again at the terminal count. The output pulse is not affected if new count data is loaded while the OUTPUT is low. The new data will be loaded on the rising edge of the next trigger pulse. The assertion of a trigger pulse while OUTPUT is low, resets and retriggers the One-Shot. The OUTPUT will remain low for the full count value after the rising edge of TRIGGER.



Mode 2: Rate Generator

The RATE GENERATOR is a variable modulus counter. The OUTPUT goes low for one full CLOCK period as shown in following timing diagram. The count data sets the time between OUTPUT pulses. If the count register is reloaded between output pulses the present period will not be affected. The subsequent period will reflect the new value. The OUTPUT will remain high for the duration of the asserted GATE input. Normal operation resumes on the falling CLOCK edge following the rising edge of GATE.



Note: ① All internal counter events occur at the falling edge of the associated clock in all modes of operation.

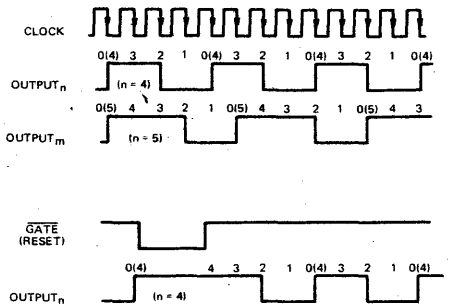
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OPERATIONAL MODES (Cont.) ①

Mode 3: Square Wave Generator

MODE 3 resembles MODE 2 except the OUTPUT will be high for half of the count and low for the other half (for even values of data). For odd values of count data the OUTPUT will be high one clock cycle longer than when it is low (High Period → $\frac{N+1}{2}$ clock cycles; Low Period → $\frac{N-1}{2}$ clock periods, where N is the decimal value of count data). If the count register is reloaded with a new value during counting, the new value will be reflected immediately after the output transition of the current count.

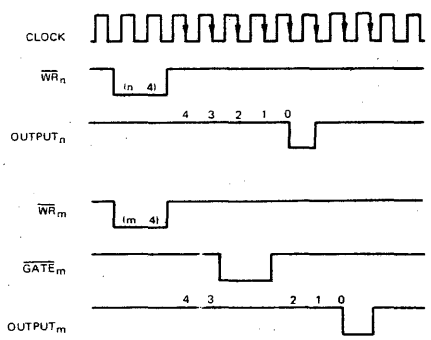
The OUTPUT will be held in the high state while GATE is asserted. Counting will start from the full count data after the GATE has been removed.



Mode 4: Software Triggered Strobe

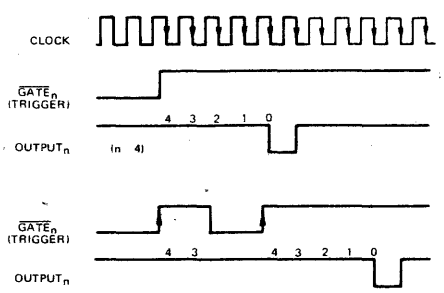
The OUTPUT goes high when MODE 4 is set, and counting begins after the second byte of data has been loaded. When the terminal count is reached, the OUTPUT will pulse low for one clock period. Changes in count data are reflected in the OUTPUT as soon as the new data has been loaded into the count registers. During the loading of new data, the OUTPUT is held high and counting is inhibited.

The OUTPUT is held high for the duration of GATE. The counters are reset and counting begins from the full data value after GATE is removed.



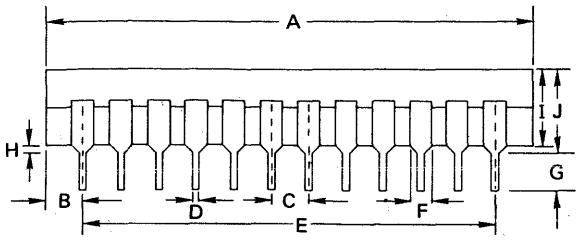
Mode 5: Hardware Triggered Strobe

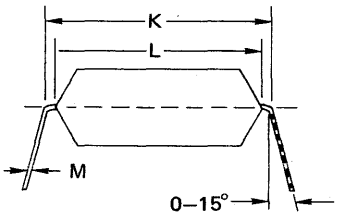
Loading MODE 5 sets OUTPUT high. Counting begins when count data is loaded and GATE goes high. After terminal count is reached, the OUTPUT will pulse low for one clock period. Subsequent trigger pulses will restart the counting sequence with the OUTPUT pulsing low on terminal count following the last rising edge of the trigger input (Reference bottom half of timing diagram).



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PACKAGE OUTLINE μPD8253C





ITEM	MILLIMETERS	INCHES
A	33 MAX	1.3 MAX
B	2.53	0.1
C	2.54	0.1
D	0.5 ± 0.1	0.02 ± 0.004
E	27.94	1.1
F	1.5	0.059
G	2.54 MIN	0.1 MIN
H	0.5 MIN	0.02 MIN
I	5.22 MAX	0.205 MAX
J	5.72 MAX	0.225 MAX
K	15.24	0.6
L	13.2	0.52
M	$0.25^{+0.10}_{-0.05}$	$0.01^{+0.004}_{-0.0019}$

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NEC

μPD8255
μPD8255A-5*

PROGRAMMABLE PERIPHERAL INTERFACES

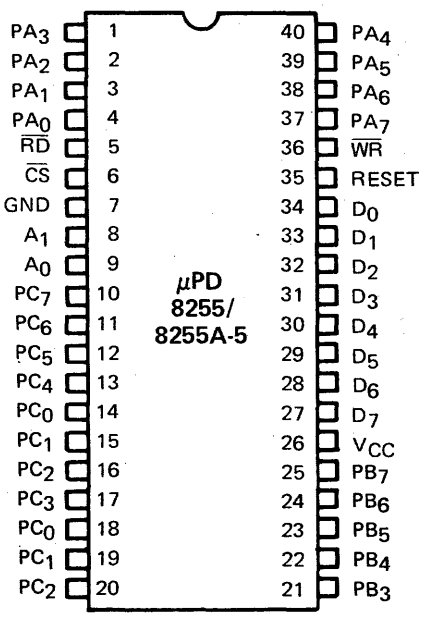
DESCRIPTION

The μPD8255 and μPD8255A-5 are general purpose programmable INPUT/OUTPUT devices designed for use with the 8080A/8085A microprocessors. Twenty-four (24) I/O lines may be programmed in two groups of twelve (group I and group II) and used in three modes of operation. In the Basic mode, (MODE 0), each group of twelve I/O pins may be programmed in sets of 4 to be input or output. In the Strobed mode, (MODE 1), each group may be programmed to have 8 lines of input or output. Three of the remaining four pins in each group are used for handshaking strobes and interrupt control signals. The Bidirectional Bus mode, (MODE 2), uses the 8 lines of Port A for a bidirectional bus, and five lines from Port C for bus control signals. The μPD8255 and μPD8255A-5 are packaged in 40 pin plastic dual-in-line packages.

FEATURES

- Fully Compatible with the 8080A/8085 Microprocessor Families
- All Inputs and Outputs TTL Compatible
- 24 Programmable I/O Pins
- Direct Bit SET/RESET Eases Control Application Interfaces
- 8 – 2 mA Darlington Drive Outputs for Printers and Displays (μPD8255)
- 8 – 4 mA Darlington Drive Outputs for Printers and Displays (μPD8255A-5)
- LSI Drastically Reduces System Package Count
- Standard 40 Pin Dual-In-Line Plastic Package

PIN CONFIGURATION



PIN NAMES

D_7-D_0	Data Bus (Bi-Directional)
RESET	Reset Input
$\overline{CS}$	Chip Select
$\overline{RD}$	Read Input
$\overline{WR}$	Write Input
A_0, A_1	Port Address
PA_7-PA_0	Port A (Bit)
PB_7-PB_0	Port B (Bit)
PC_7-PC_0	Port C (Bit)
V_{CC}	+5 Volts
GND	0 Volts

*All data pertaining to the μPD8255A-5 is preliminary.

Rev/2

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FUNCTIONAL DESCRIPTION

General

The μPD8255 and μPD8255A-5 Programmable Peripheral Interfaces (PPI) are designed for use in 8080A/8085A microprocessor systems. Peripheral equipment can be effectively and efficiently interfaced to the 8080A/8085A data and control busses with the μPD8255 and μPD8255A-5. The μPD8255 and μPD8255A-5 are functionally configured to be programmed by system software to avoid external logic for peripheral interfaces.

Data Bus Buffer

The 3-state, bidirectional, eight bit Data Bus Buffer (D_0-D_7) of the μPD8255 and μPD8255A-5 can be directly interfaced to the processor's system Data Bus (D_0-D_7). The Data Bus Buffer is controlled by execution of IN and OUT instructions by the processor. Control Words and Status information are also transmitted via the Data Bus Buffer.

Read/Write and Control Logic

This block manages all of the internal and external transfers of Data, Control and Status. Through this block, the processor Address and Control busses can control the peripheral interfaces.

Chip Select, $\overline{CS}$, pin 6

A Logic Low, V_{IL}, on this input enables the μPD8255 and μPD8255A-5 for communication with the 8080A/8085A.

Read, $\overline{RD}$, pin 5

A Logic Low, V_{IL}, on this input enables the μPD8255 and μPD8255A-5 to send Data or Status to the processor via the Data Bus Buffer.

Write, $\overline{WR}$, pin 36

A Logic Low, V_{IL}, on this input enables the Data Bus Buffer to receive Data or Control Words from the processor.

Port Select 0, A_0, pin 9

Port Select 1, A_1, pin 8

These two inputs are used in conjunction with $\overline{CS}$, $\overline{RD}$, and $\overline{WR}$ to control the selection of one of three ports on the Control Word Register. A_0 and A_1 are usually connected to A_0 and A_1 of the processor Address Bus.

Reset, pin 35

A Logic High, V_{IH}, on this input clears the Control Register and sets ports A, B, and C to the input mode. The input latches in ports A, B, and C are not cleared.

Group I and Group II Controls

Through an OUT instruction in System Software from the processor, a control word is transmitted to the μPD8255 and μPD8255A-5. Information such as "MODE," "Bit SET," and "Bit RESET" is used to initialize the functional configuration of each I/O port.

Each group (I and II) accepts "commands" from the Read/Write Control Logic and "control words" from the internal data bus and in turn controls its associated I/O ports.

Group I — Port A and upper Port C (PC_7-PC_4)
Group II — Port B and lower Port C (PC_3-PC_0)

While the Control Word Register can be written into, the contents cannot be read back to the processor.

Ports A, B, and C

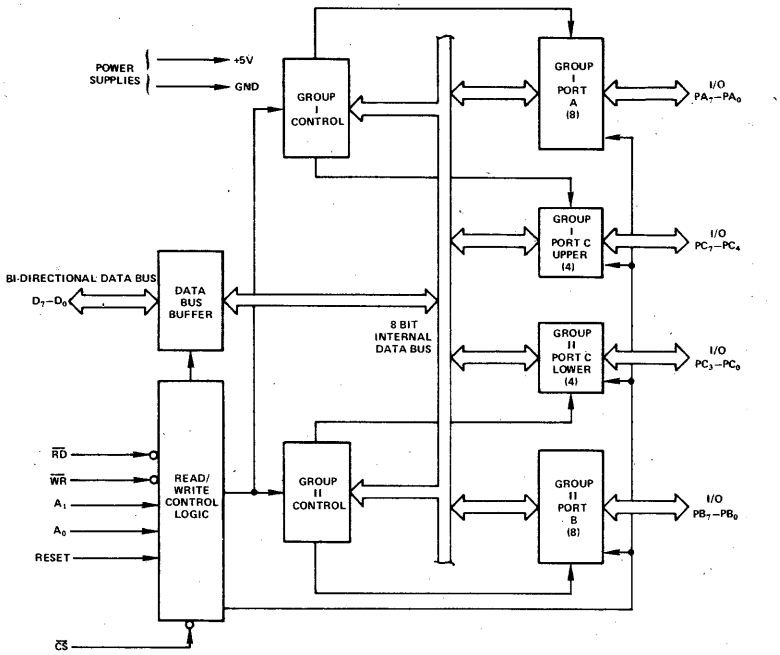
The three 8-bit I/O ports (A, B, and C) in the μPD8255 and μPD8255A-5 can all be configured to meet a wide variety of functional requirements through system software. The effectiveness and flexibility of the μPD8255 and μPD8255A-5 is further enhanced by special features unique to each of the ports.

Port A = An 8-bit data output latch/buffer and data input latch.
Port B = An 8-bit data input/output latch/buffer and an 8-bit data input buffer.
Port C = An 8-bit output latch/buffer and a data input buffer (input not latched).

Port C may be divided into two independent 4-bit control and status ports for use with Ports A and B.

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BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	0°C to +70°C
Storage Temperature	-65°C to +125°C
All Output Voltages ①	-0.5 to +7 Volts
All Input Voltages ①	-0.5 to +7 Volts
Supply Voltages ①	-0.5 to +7 Volts

Note: ① With respect to V_{SS}

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

DC CHARACTERISTICS

T_a = 0°C to +70°C, V_{CC} = +5V ± 5%; V_{SS} = 0V.

PARAMETER	SYMBOL	LIMITS μPD8255 MIN	μPD8255 TYP	μPD8255 MAX	LIMITS μPD8255A MIN	μPD8255A TYP	μPD8255A MAX	UNIT	TEST CONDITIONS
Input Low Voltage	V_{IL}	V_{SS}-0.5		0.8	-0.5		0.8	V	
Input High Voltage	V_{IH}	2		V_{CC}	2		V_{CC}	V	
Output Low Voltage	V_{OL}			0.4			0.45	V	②
Output High Voltage	V_{OH}	2.4			2.4			V	③
Darlington Drive Current	I_{OH} ①	1	2	4	-1	-2	-4	mA	V_{OH} = 1.5V, R_{EXT} = 750Ω
Power Supply Current	I_{CC}		40	120		40	120	mA	V_{CC} = +5V, Output Open
Input Leakage Current	I_{LIH}			10			10	μA	V_{IN} = V_{CC}
Input Leakage Current	I_{LIL}			-10			-10	μA	V_{IN} = 0.4V
Output Leakage Current	I_{LOH}			10			10	μA	V_{OUT} = V_{CC}; $\overline{CS}$ = 2.0V
Output Leakage Current	I_{LOL}			-10			-10	μA	V_{OUT} = 0.4V, $\overline{CS}$ = 2.0V

Notes: ① Any set of eight (8) outputs from either Port A, B, or C can source 2 mA into 1.5V for μPD8255, or 4 mA into 1.5V for μPD8255A.

② For μPD8255: I_{OL} = 1.7 mA
For μPD8255A: I_{OL} = 2.5 mA for DB Port; 1.7 mA for Peripheral Ports.

③ For μPD8255: I_{OH} = -100 μs for DB Port; 50 μs for Peripheral Ports.
For μPD8255A: I_{OH} = -400 μs for DB Port; -200 μs for Peripheral Ports.

CAPACITANCE

T_a = 25°C; V_{CC} = V_{SS} = 0V

PARAMETER	SYMBOL	LIMITS MIN	TYP	MAX	UNIT	TEST CONDITIONS
Input Capacitance	C_{IN}			10	pF	f_c = 1 MHz
I/O Capacitance	$C_{I/O}$			20	pF	Unmeasured pins returned to V_{SS}

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μPD8255/8255A-5

MODES

The μPD8255 and μPD8255A-5 can be operated in modes (0, 1 or 2) which are selected by appropriate control words and are detailed below.

MODE 0

- MODE 0 provides for basic Input and Output operations through each of the ports A, B, and C. Output data is latched and input data follows the peripheral. No "handshaking" strobes are needed.

  16 different configurations in MODE 0

  Two 8-bit ports and two 4-bit ports

  Inputs are not latched

  Outputs are latched

MODE 1

MODE 1 provides for Strobed Input and Output operations with data transferred through Port A or B and handshaking through Port C.

Two I/O Groups (I and II)

Both groups contain an 8-bit data port and a 4-bit control/data port

Both 8-bit data ports can be either Latched Input or Latched Output

MODE 2

MODE 2 provides for Strobed bidirectional operation using PA_{0-7} as the bidirectional latched data bus. PC_{3-7} is used for interrupts and "handshaking" bus flow controls similar to Mode 1. Note that PB_{0-7} and PC_{0-2} may be defined as Mode 0 or 1, input or output in conjunction with Port A in Mode 2.

An 8-bit latched bidirectional bus port (PA_{0-7}) and a 5-bit control port (PC_{3-7})

Both inputs and outputs are latched

An additional 8-bit input or output port with a 3-bit control port

BASIC OPERATION

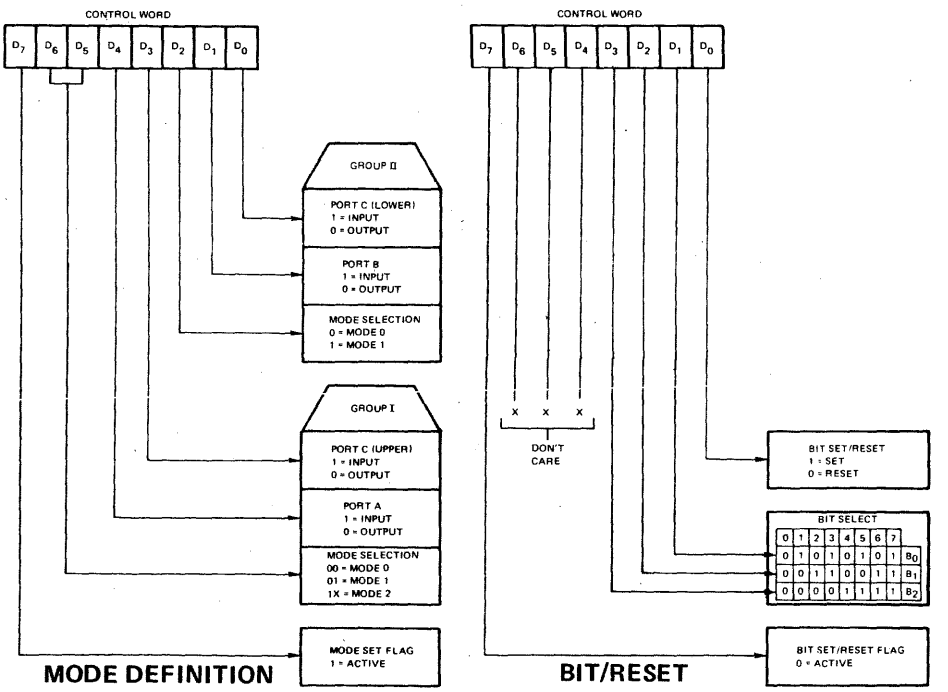
INPUT OPERATION (READ)					
A_1	A_0	$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	
0	0	0	1	0	PORT A → DATA BUS
0	1	0	1	0	PORT B → DATA BUS
1	0	0	1	0	PORT C → DATA BUS

OUTPUT OPERATION (WRITE)					
A_1	A_0	$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	
0	0	1	0	0	DATA BUS → PORT A
0	1	1	0	0	DATA BUS → PORT B
1	0	1	0	0	DATA BUS → PORT C
1	1	1	0	0	DATA BUS → CONTROL

DISABLE FUNCTION					
A_1	A_0	$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	
X	X	X	X	1	DATA BUS → HIGH Z STATE
X	X	1	1	0	DATA BUS → HIGH Z STATE

NOTES: ① X means "DO NOT CARE."
② All conditions not listed are illegal and should be avoided.

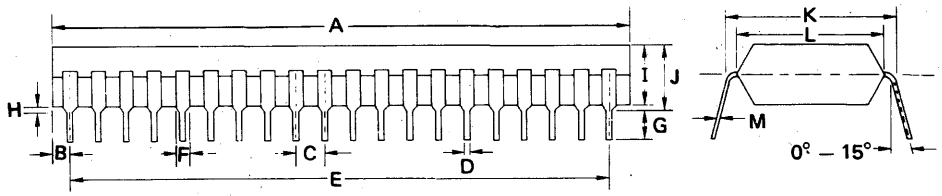
FORMATS



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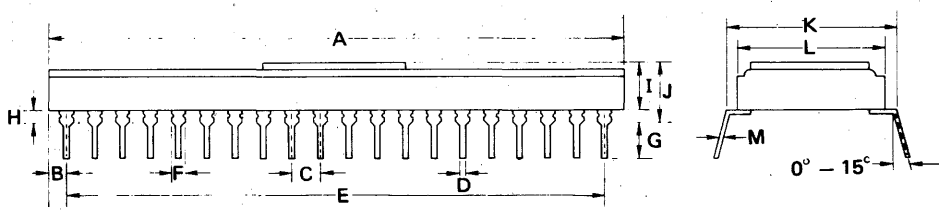
PACKAGE OUTLINE μPD8255C/D μPD8255AC/D-5

Members of the μPD8085 Family are housed in both plastic and ceramic 40 pin packages. The drawings and tables below apply to all five of the NEC Microcomputer parts covered in this data sheet.



Plastic

ITEM	MILLIMETERS	INCHES
A	51.5 MAX	2.028 MAX
B	1.62	0.064
C	2.54 ± 0.1	0.10 ± 0.004
D	0.5 ± 0.1	0.019 ± 0.004
E	48.26	1.9
F	1.2 MIN	0.047 MIN
G	2.54 MIN	0.10 MIN
H	0.5 MIN	0.019 MIN
I	5.22 MAX	0.206 MAX
J	5.72 MAX	0.225 MAX
K	15.24	0.600
L	13.2	0.520
M	$0.25^{+0.1}_{-0.05}$	$0.010^{+0.004}_{-0.002}$



Ceramic

ITEM	MILLIMETERS	INCHES
A	51.5 MAX	2.028 MAX
B	1.62	0.064
C	2.54 ± 0.1	0.100 ± 0.004
D	0.50 ± 0.1	0.0197 ± 0.004
E	48.26 ± 0.2	1.900 ± 0.008
F	1.27	0.050
G	3.2 MIN	0.126 MIN
H	1.0 MIN	0.04 MIN
I	4.2 MAX	0.17 MAX
J	5.2 MAX	0.205 MAX
K	15.24 ± 0.1	0.6 ± 0.004
L	$13.5^{+0.2}_{-0.25}$	$0.531^{+0.008}_{-0.010}$
M	0.30 ± 0.1	0.012 ± 0.004

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PROGRAMMABLE DMA CONTROLLER

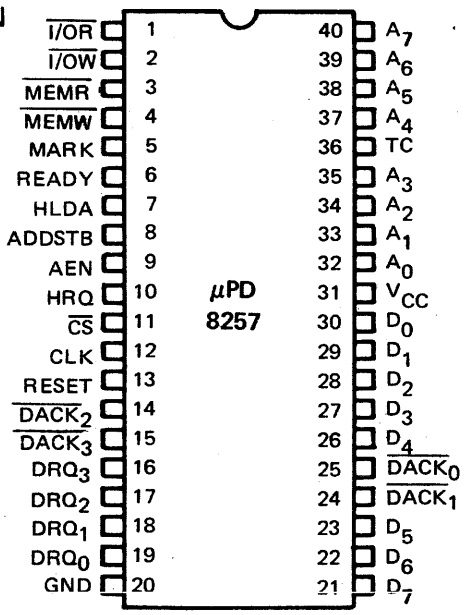
DESCRIPTION

The μPD8257 is a programmable four-channel Direct Memory Access (DMA) controller. It is designed to simplify high speed transfers between peripheral devices and memories. Upon a peripheral request, the 8257 generates a sequential memory address, thus allowing the peripheral to read or write data directly to or from memory. Peripheral requests are prioritized within the 8257 so that the system bus may be acquired by the generation of a single HOLD command to the 8080. DMA cycle counts are maintained for each of the four channels, and a control signal notifies the peripheral when the preprogrammed member of DMA cycles has occurred. Output control signals are also provided which allow simplified sectored data transfers and expansion to other 8257 devices for systems requiring more than four DMA channels.

FEATURES

- Four Channel DMA Controller
- Priority DMA Request Logic
- Channel Inhibit Logic
- Terminal Count and Modulo 128 Outputs
- Automatic Load Mode
- Single TTL Clock
- Single +5V Supply
- Expandable
- 40 Pin Plastic Dual-In-Line Package

PIN CONFIGURATION



PIN NAMES

D_7-D_0	Data Bus
A_7-A_0	Address Bus
$\overline{I/OR}$	I/O Read
$\overline{I/OW}$	I/O Write
$\overline{MEMR}$	Memory Read
$\overline{MEMW}$	Memory Write
CLK	Clock Input
RESET	Reset Input
READY	Ready
HRQ	Hold Request (to 8080A)
HLDA	Hold Acknowledge (from 8080A)
AEN	Address Enable
ADSTB	Address Strobe
TC	Terminal Count
MARK	Modulo 128 Mark
DRQ_3-DRQ_0	DMA Request Input
$\overline{DACK_3}$-$\overline{DACK_0}$	DMA Acknowledge Out
$\overline{CS}$	Chip Select
V_{CC}	+5 Volts
GND	Ground

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μPD8257

FUNCTIONAL DESCRIPTION

The 8257 is a programmable, Direct Memory Access (DMA) device and when used with an 8212 I/O port device, it provides a complete four-channel DMA controller for use in 8080 based systems. Once initialized by an 8080 CPU, the 8257 will block transfer up to 16,364 bytes of data between memory and a peripheral device without any attention from the CPU, and it will do this on all 4-DMA channels. After receiving a DMA transfer request from a peripheral, the following sequence of events occur within the 8257.

- It acquires control of the system bus (placing 8080 in hold mode).
- Resolves priority conflicts if multiple DMA requests are made.
- A 16 bit memory address word is generated with the aid of an 8212 in the following manner:

  The 8257 outputs the least significant eight bits (A_0-A_7) which go directly onto the address bus.

  The 8257 outputs the most significant eight bits (A_8-A_{15}) onto the data bus where they are latched into an 8212 and then sent to the high order bits on the address bus.
- The appropriate memory and I/O read/write control signals are generated allowing the peripheral to receive or deposit a data byte directly from or to the appropriate memory location.

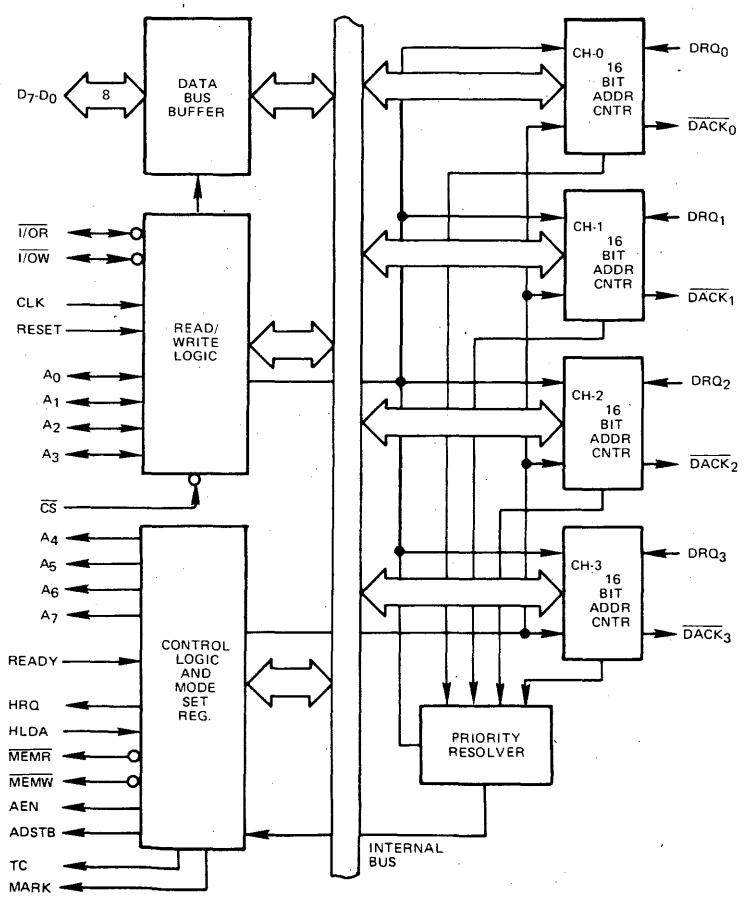
Block transfer of data (e.g., a sector of data on a floppy disk) either to or from a peripheral may be accomplished as long as the peripheral maintains its DMA Request (DRQ_n). The 8257 retains control of the system bus as long as DRQ_n remains high or until the Terminal Count (TC) is reached. When the Terminal Count occurs, TC goes high, informing the CPU that the operation is complete.

There are three different modes of operation:

- DMA read; which causes data to be transferred from memory to a peripheral;
- DMA write; which causes data to be transferred from a peripheral to memory; and
- DMA verify; which does not actually involve the transfer of data.

The DMA read and write modes are the normal operating conditions for the 8257. The DMA verify mode responds in the same manner as read/write except no memory or I/O read/write control signals are generated, thus preventing the transfer of data. The peripheral gains control of the system bus and obtains DMA Acknowledgements for its requests, thus allowing it to access each byte of a data block for check purposes or accumulation of a CRC (Cyclic Redundancy Code) checkword. In some applications it is necessary for a block of DMA read or write cycles to be followed by a block of DMA verify cycles to allow the peripheral to verify its newly acquired data.

BLOCK DIAGRAM



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Manufacturer Device	Replacement Source	Device	IC Master Page
NCR Corp., Microelectronics Div.			
NCR1105	Nitron	NC1105	
NCR1400	Nitron	NC1400	
NCR1711	Nitron	NC1711	
NCR1721	Nitron	NC1721	
NCR1731	Nitron	NC1731	
NCR2051	Nitron	NC2051	
NCR2055	Nitron	NC2055	
NCR2401	Nitron	NC2401	
NCR2450	Nitron	NC2450	
NCR2805	Nitron	NC2805	
NCR2810	Nitron	NC2810	
NEC America			
μPB10100	Fairchild	F10100	
	Motorola	MC10100	
	Signetics	10100	
μPB10101	Fairchild	F10101	
	Hitachi	HD10101	
	Motorola	MC10101	
	Signetics	10101	
μPB10102	Fairchild	F10102	
	Hitachi	HD10102	
	Motorola	MC10102	
	Signetics	10102	
μPB10103	Fairchild	F10103	
	Motorola	MC10103	
	Signetics	10103	
μPB10105	Fairchild	F10105	
	Hitachi	HD10105	
	Motorola	MC10105	
	National	DM10105	
	Signetics	10105	
μPB10106	Fairchild	F10106	
	Hitachi	HD10106	
	Motorola	MC10106	
	National	DM10106	
	Signetics	10106	
μPB10107	Fairchild	F10107	
	Hitachi	HD10107	
	Motorola	MC10107	
	Signetics	10107	
μPB10109	Fairchild	F10109	
	Hitachi	HD10109	
	Motorola	MC10109	
	National	DM10109	
	Signetics	10109	
μPB10110	Fairchild	F10110	
	Hitachi	HD10110	
	Motorola	MC10110	
	Signetics	10110	
μPB10111	Fairchild	F10111	
	Hitachi	HD10111	
	Motorola	MC10111	
	National	DM10111	
	Signetics	10111	
μPB10115	Fairchild	F10115	
	Motorola	MC10115	
	National	DM10115	
	Signetics	10115	
μPB10117	Fairchild	F10117	
	Hitachi	HD10117	
	Motorola	MC10117	
	National	DM10117	
	Signetics	10117	
μPB10118	Fairchild	F10118	
	Hitachi	HD10118	
	Motorola	MC10118	
	National	DM10118	
	Signetics	10118	
μPB10124	Fairchild	F10124	
	Hitachi	HD10124	
	Motorola	MC10124	
	National	DM10124	
	Signetics	10124	
μPB10131	Fairchild	F10131	
	Hitachi	HD10131	
	Motorola	MC10131	
	Signetics	10131	
μPB10133	Fairchild	F10133	
	Hitachi	HD10133	
μPB10133	Motorola	MC10133	
	Signetics	10133	
μPB10142	TI	SN10102	
μPB10144	Motorola	MC10144	
	Raytheon	RC10144	
	Signetics	10144	
	TI	SN10144	
μPB10148	Hitachi	HD10148	
	Signetics	10148	
	TI	SN10148	
μPB10158	Fairchild	F10158	
	Motorola	MC10158	
	Signetics	10158	
μPB10161	Fairchild	F10161	
	Hitachi	HD10161	
	Motorola	MC10161	
	Signetics	10161	
μPB10162	Fairchild	F10162	
	Hitachi	HD10162	
	Motorola	MC10162	
	Signetics	10162	
μPB10164	Fairchild	F10164	
	Hitachi	HD10164	
	Motorola	MC10164	
	Signetics	10164	
	TI	SN10164	
μPB10174	Fairchild	F10174	
	Hitachi	HD10174	
	Motorola	MC10174	
	Signetics	10174	
	TI	SN10174	
μPB10180	Fairchild	F10180	
	Hitachi	HD10180	
	Motorola	MC10180	
	Signetics	10180	
μPB10181	Fairchild	F10181	
	Hitachi	HD10181	
	Motorola	MC10181	
	Signetics	10181	
μPB74H00	Fairchild	74H00	
	National	DM74H00	
	Raytheon	74H00	
	Signetics	74H00	
	TI	SN74H00	
μPB74H01	Fairchild	74H01	
	National	DM74H01	
	Raytheon	74H01	
	Signetics	74H01	
	TI	SN74H01	
μPB74H04	Fairchild	74H04	
	National	DM74H04	
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	Raytheon	74H20	
	Signetics	74H20	
	TI	SN74H20	
μPB74H30	Fairchild	74H30	
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	Signetics	74H30	
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μPB74H40	Fairchild	74H40	
	National	DM74H40	
	Raytheon	74H40	
	Signetics	74H40	
	TI	SN74H40	
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	National	DM74H51	
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	TI	SN74H51	
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	Motorola	SN74LS00	
	National	DM74LS00	
	Raytheon	74LS00	
	Signetics	74LS00	
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	National	DM74LS02	
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	Hitachi	HD74LS03	
	Motorola	SN74LS03	
	National	DM74LS03	
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	Signetics	74LS03	
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	Signetics	74LS10	
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	TI	SN74LS11	
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	Signetics	74LS138	
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	National	DM74LS164	
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	Fairchild	74LS175	
	Hitachi	HD74LS175	
	Motorola	SN74LS175	
	National	DM74LS175	
	Raytheon	74LS175	
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	Fairchild	74LS194	
	Hitachi	HD74LS194A	
	Motorola	SN74LS194A	
	Raytheon	74LS194A	
	Signetics	74LS194A	
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	TI	SN74LS195A	
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	Motorola	SN74LS20	
	National	DM74LS20	
	Raytheon	74LS20	
	Signetics	74LS20	
	TI	SN74LS20	
μPB74LS21	Fairchild	74LS21	
	Hitachi	HD74LS21	

♦ Discontinued

The manufacturers report their devices can be used as direct replacements.
Performance details often differ, so compare the specifications considering your requirements.

AC CHARACTERISTICS PERIPHERAL (SLAVE) MODE

BUS PARAMETERS

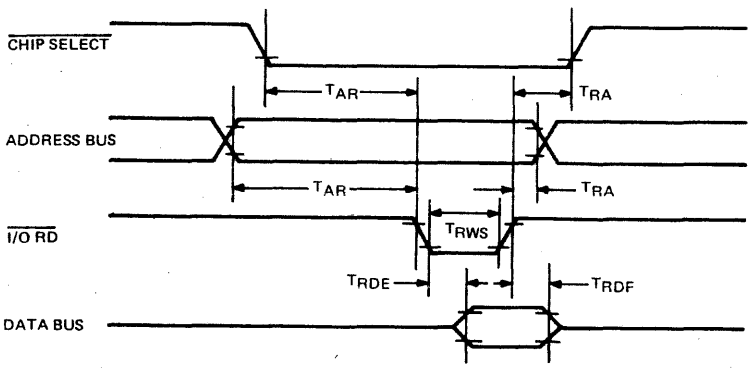
T_a = 0°C to 70°C; V_{CC} = 5V ± 5%; GND = 0V ①

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
READ						
Adr or $\overline{CS}$↓ Setup to $\overline{Rd}$↓	T_{AR}	50			ns	
Adr or $\overline{CS}$↑ Hold from $\overline{Rd}$↑	T_{RA}	0			ns	
Data Access from $\overline{Rd}$↓	T_{RDE}	0		300	ns	C_L = 100pF
DB→Float Delay from $\overline{Rd}$↑	T_{RDF}			150	ns	C_L = 100pF
		20			ns	C_L = 15pF
$\overline{Rd}$ Width	T_{RW}	300			ns	
WRITE						
$\overline{CS}$↓ Setup to $\overline{Wr}$↓	T_{CW}	300			ns	
$\overline{CS}$↑ Hold from $\overline{Wr}$↑	T_{WC}	20			ns	
Adr Setup to $\overline{Wr}$↓	T_{AW}	20			ns	
Adr Hold from $\overline{Wr}$↑	T_{WA}	20			ns	
Data Setup to $\overline{Wr}$↓	T_{DW}	200			ns	
Data Hold from $\overline{Wr}$↑	T_{WD}	35			ns	
Wr Width	T_{WWS}	200			ns	
OTHER TIMING						
Reset Pulse Width	T_{RSTW}	300			ns	
Power Supply↑(V_{CC}) Setup to Reset↓	T_{RSTD}	500			μs	
Signal Rise Time	T_r			20	ns	
Signal Fall Time	T_f			20	ns	
Reset to First $\overline{IOWR}$	T_{RSTS}	2			t_{CY}	

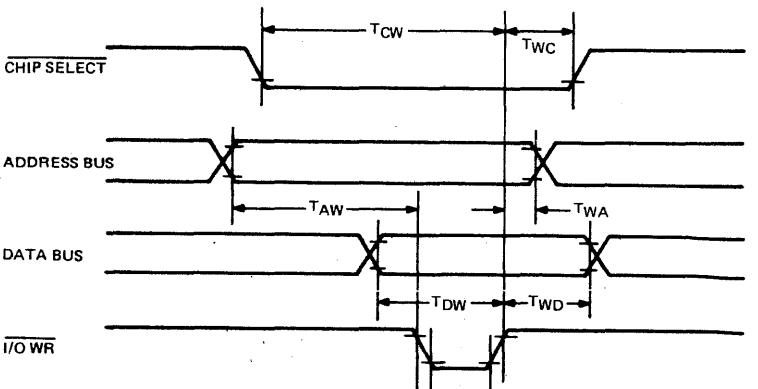
Note: ① All timing measurements are made at the following reference voltages unless specified otherwise: Input "1" at 2.0V, "0" at 0.8V, Output "1" at 2.0V, "0" at 0.8V.

TIMING WAVEFORMS PERIPHERAL (SLAVE) MODE

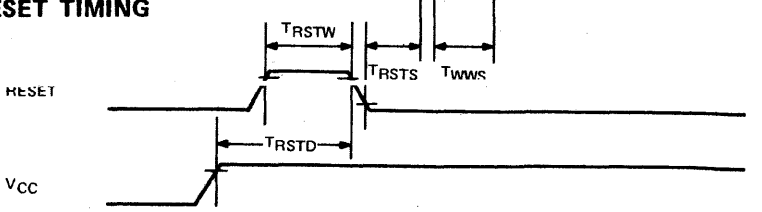
READ TIMING



WRITE TIMING



RESET TIMING



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AC CHARACTERISTICS DMA (MASTER) MODE

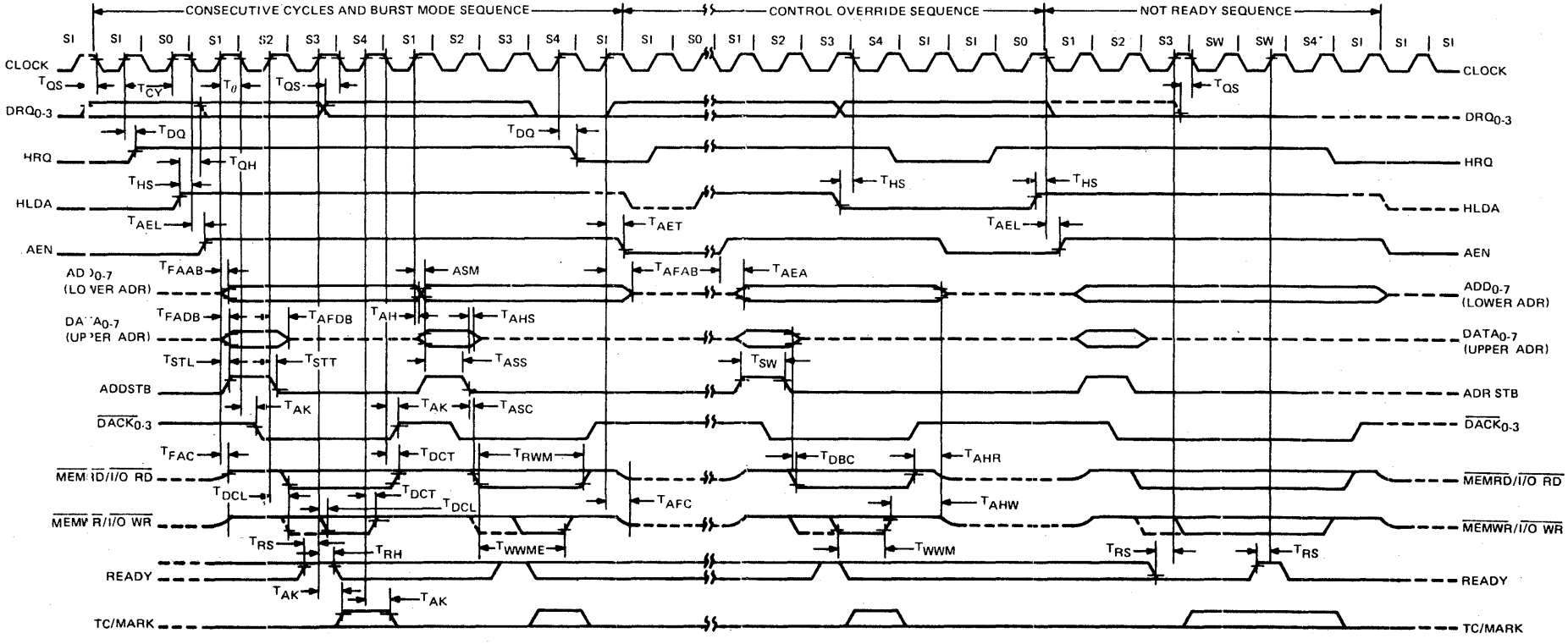
T_a = 0°C to 70°C; V_{CC} = +5V ±5%; GND = 0V

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN	TYP	MAX		
Cycle Time (Period)	T_{CY}	0.330		4	μs	
Clock Active (High)	T_θ	150		.8T_{CY}	ns	
DRQ↑ Setup to θ↓ (SI, S4)	T_{QS}	120				
DRQ↓ Hold from HLDA↑	T_{QH}	0				④
HRQ↑ or ↓Delay from θ↑ (SI, S4) (measured at 2.0V)	T_{DQ}			160	ns	①
HRQ↑ or ↓Delay from θ↑ (SI, S4) (measured at 3.3V)	T_{DQ1}			250	ns	③
HLDA↑ or ↓Setup to θ↓ (SI, S4)	T_{HS}	100			ns	
AEN↑ Delay from θ↓ (S1)	T_{AEL}			300	ns	①
AEN↓ Delay from θ↑ (SI)	T_{AET}			200	ns	①
Adr (AB) (Active) Delay from AEN↑ (S1)	T_{AEA}	20			ns	④
Adr (AB) (Active) Delay from θ↑ (S1)	T_{FAAB}			250	ns	②
Adr (AB) (Float) Delay from θ↑ (SI)	T_{AFAB}			150	ns	②
Adr (AB) (Stable) Delay from θ↑ (S1)	T_{ASM}			250	ns	②
Adr (AB) (Stable) Hold from θ↑ (S1)	T_{AH}	T_{ASM}–50				②
Adr (AB) (Valid) Hold from $\overline{Rd}$↑ (S1,SI)	T_{AHR}	60			ns	④
Adr (AB) (Valid) Hold from $\overline{Wr}$↑ (S1, SI)	T_{AHW}	300			ns	④
Adr (DB) (Active) Delay from θ↑ (S1)	T_{FADB}			300	ns	②
Adr (DB) (Float) Delay from θ↑ (S2)	T_{AFDB}	T_{STT}+20		250	ns	②
Adr (DB) Setup to Adr Stb↓ (S1-S2)	T_{ASS}	100			ns	④
Adr (DB) (Valid) Hold from Adr Stb↓ (S2)	T_{AHS}	50			ns	④
Adr Stb↑ Delay from θ↑ (S1)	T_{STL}			200	ns	①
Adr Stb↓ Delay from θ↑ (S2)	T_{STT}			140	ns	①
Adr Stb Width (S1-S2)	T_{SW}	T_{CY}–100			ns	④
$\overline{Rd}$↓ or $\overline{Wr}$ (Ext)↓ Delay from Adr Stb↓ (S2)	T_{ASC}	70			ns	④
$\overline{Rd}$↓ or $\overline{Wr}$ (Ext)↓ Delay from Adr (DB) (Float) (S2)	T_{DBC}	20			ns	④
DACK↑ or ↓Delay from θ↓ (S2, S1) and TC/Mark↑ Delay from θ↑ (S3) and TC/Mark↓ Delay from θ↑ (S4)	T_{AK}			250	ns	①⑤
$\overline{Rd}$↓ or $\overline{Wr}$ (Ext)↓ Delay from θ↑ (S2) and $\overline{Wr}$↓ Delay from θ↑ (S3)	T_{DCL}			200	ns	②⑥
$\overline{Rd}$↑ Delay from θ↓ (S1, SI) and $\overline{Wr}$↑ Delay from θ↑ (S4)	T_{DCT}			200	ns	②⑦
$\overline{Rd}$ or $\overline{Wr}$ (Active) from θ↑ (S1)	T_{FAC}			300	ns	②
$\overline{Rd}$ or $\overline{Wr}$ (Float) from θ↑ (SI)	T_{AFC}			150	ns	②
$\overline{Rd}$ Width (S2-S1 or SI)	T_{RWM}	$2T_{CY}$ + T_θ–50			ns	④
$\overline{Wr}$ Width (S3-S4)	T_{WWM}	T_{CY}–50			ns	④
$\overline{Wr}$ (Ext) Width (S2-S4)	T_{WWME}	$2T_{CY}$–50			ns	④
READY Set Up Time to θ↑ (S3, Sw)	T_{RS}	30			ns	
READY Hold Time from θ↑ (S3, Sw)	T_{RH}	20			ns	

Notes:
① Load = 1 TTL
② Load = 1 TTL + 50pF
③ Load = 1 TTL + (R_L = 3.3K), V_{OH} = 3.3V
④ Tracking Specification
⑤ $\Delta T_{AK} < 50$ ns
⑥ $\Delta T_{DCL} < 50$ ns
⑦ $\Delta T_{DCT} < 50$ ns

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TIMING WAVEFORMS
DMA (MASTER) MODE



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DMA OPERATION

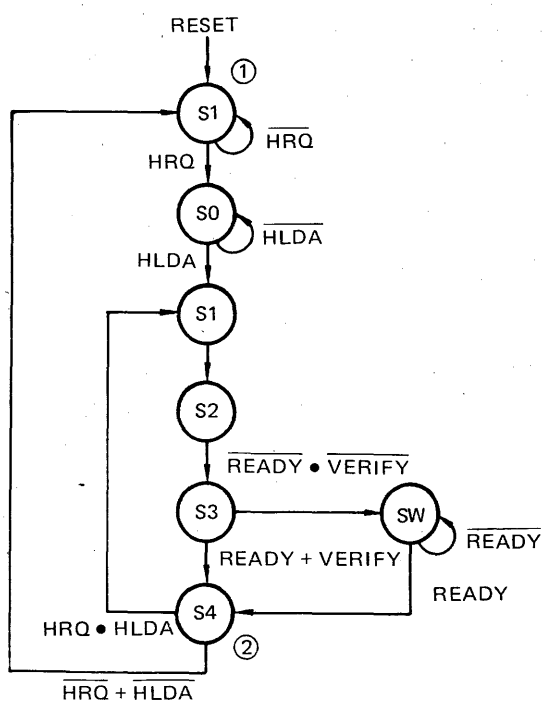
Internally the 8257 contains six different states (S0, S1, S2, S3, S4 and SW), the duration of each state is determined by the input clock. In the idle state, (S1), no DMA operation is being executed. A DMA cycle is started upon receipt of one or more DMA Requests (DRQ_n), then the 8257 enters the S0 state. During state S0 a Hold Request (HRQ) is sent to the 8080 and the 8257 waits in S0 until the 8080 issues a Hold Acknowledge (HLDA) back. During S0, DMA Requests are sampled and DMA priority is resolved (based upon either the fixed or priority scheme). After receipt of HLDA, the DMA Acknowledge line ($\overline{DACK_n}$) with the highest priority is driven low selecting that particular peripheral for the DMA cycle. The DMA Request line (DRQ_n) must remain high until either a DMA Acknowledge ($\overline{DACK_n}$) or both $\overline{DACK_n}$ and TC (Terminal Count) occur, indicating the end of a block or sector transfer (burst mode).

The DMA cycle consists of four internal states; S1, S2, S3 and S4. If the access time of the memory or I/O device is not fast enough to return a Ready command to the 8257 after it reaches state S3, then a Wait state is initiated (SW). One or more than one Wait state occurs until a Ready signal is received, and the 8257 is allowed to go into state S4. Either the extended write option or the DMA Verify mode may eliminate any Wait state.

If the 8257 should lose control of the system bus (i.e., HLDA goes low) then the current DMA cycle is completed, the device goes into the S1 state, and no more DMA cycles occur until the bus is reacquired. Ready setup time (t_{RS}), write setup time (t_{DW}), read data access time (t_{RD}) and HLDA setup time (t_{QS}) should all be carefully observed during the handshaking mode between the 8257 and the 8080.

During DMA write cycles, the I/O Read ($\overline{I/O\ R}$) output is generated at the beginning of state S2 and the Memory Write ($\overline{MEMW}$) output is generated at the beginning of S3. During DMA read cycles, the Memory Read ($\overline{MEMR}$) output is generated at the beginning of state S2 and the I/O Write ($\overline{I/O\ W}$) goes low at the beginning of state S3. No Read or Write control signals are generated during DMA verify cycles.

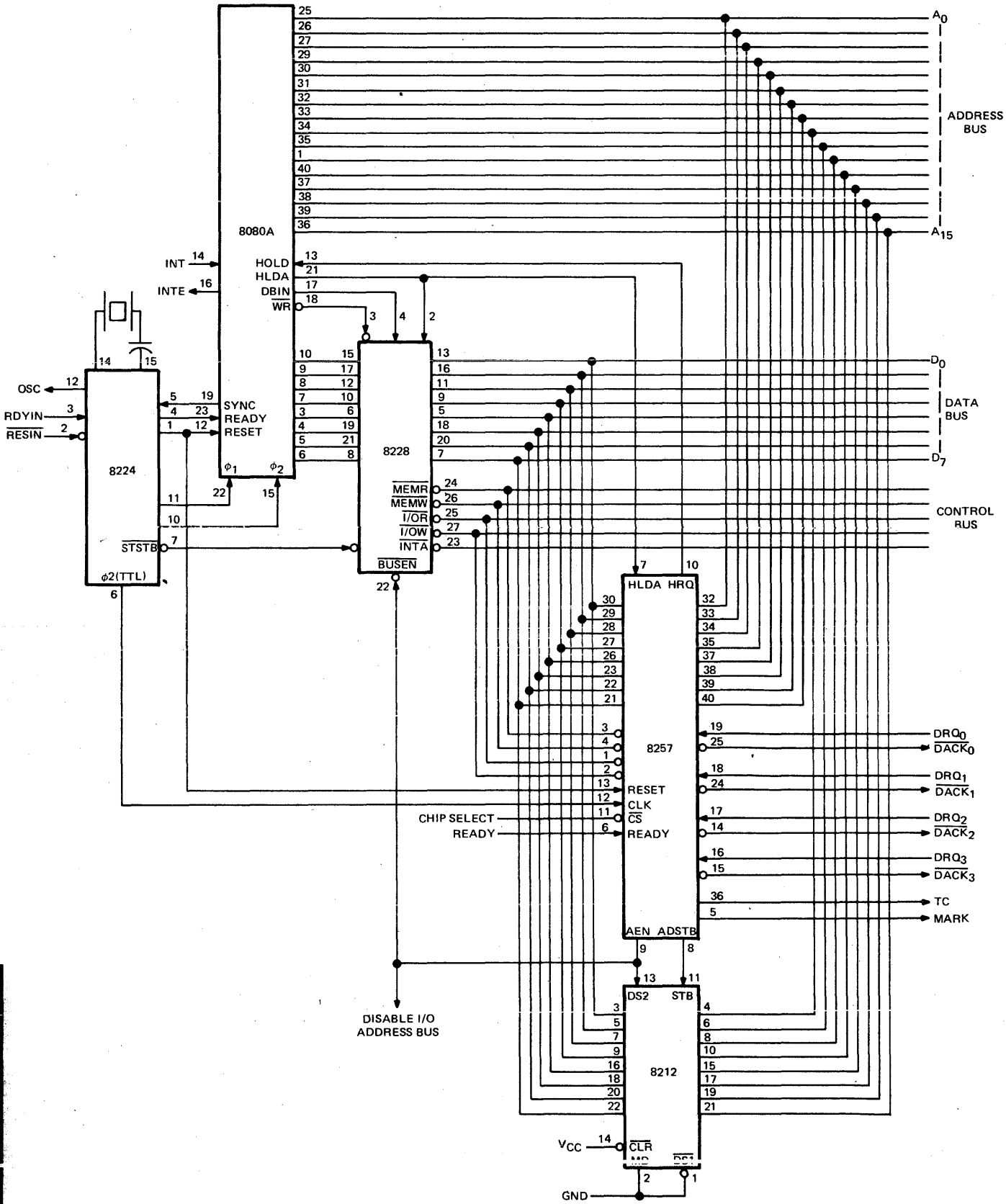
DMA OPERATION STATE DIAGRAM



Notes: ① HRQ is set if DRQ_n is active.
② HRQ is reset if DRQ_n is not active.

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TYPICAL 8257
SYSTEM INTERFACE SCHEMATIC



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ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	0°C to +70°C
Storage Temperature	-65°C to +150°C
Voltage on Any Pin	-0.5 to +7 Volts ①
Power Dissipation	1 Watt

Note: ① With Respect to Ground

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

DC CHARACTERISTICS

T_a = 0°C to +70°C; V_{CC} = +5V ± 5%; GND = 0V

PARAMETER	SYMBOL	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNIT	TEST CONDITIONS
Input Low Voltage	V_{IL}	-0.5		0.8	Volts	
Input High Voltage	V_{IH}	2.0		V_{CC} + 0.5	Volts	
Output Low Voltage	V_{OL}			0.45	Volts	I_{OL} = 1.6 mA
Output High Voltage	V_{OH}	2.4		V_{CC}	Volts	I_{OH} = -150 μA for AB, DB and AEN I_{OH} = -80 μA for others
HRQ Output High Voltage	V_{HH}	3.3		V_{CC}	Volts	I_{OH} = -80 μA
V_{CC} Current Drain	I_{CC}			120	mA	
Input Leakage	I_{IL}			10	μA	V_{IN} = V_{CC}
Output Leakage During Float	I_{OFL}			10	μA	V_{OUT} ①

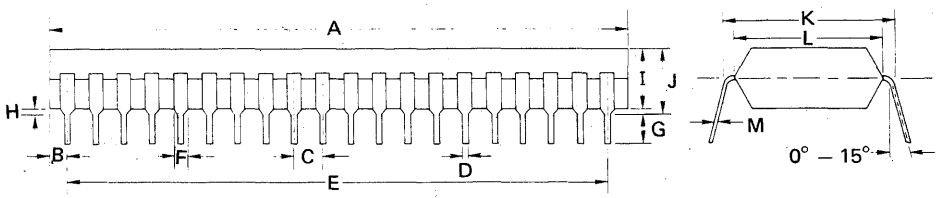
Note: ① $V_{CC} > V_{OUT} >$ GND + 0.45V

CAPACITANCE

T_a = 25°C; V_{CC} = GND = 0V

PARAMETER	SYMBOL	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNIT	TEST CONDITIONS
Input Capacitance	C_{IN}			10	pF	f_c = 1 MHz
I/O Capacitance	$C_{I/O}$			20	pF	Unmeasured pins returned to GND

PACKAGE OUTLINE



ITEM	MILLIMETERS	INCHES
A	51.5 MAX	2.028 MAX
B	1.62	0.064
C	2.54 ± 0.1	0.10 ± 0.004
D	0.5 ± 0.1	0.019 ± 0.004
E	48.26	1.9
F	1.2 MIN	0.047 MIN
G	2.54 MIN	0.10 MIN
H	0.5 MIN	0.019 MIN
I	5.22 MAX	0.206 MAX
J	5.72 MAX	0.225 MAX
K	15.24	0.600
L	13.2	0.520
M	$0.25^{+0.1}_{-0.05}$	$0.010^{+0.004}_{-0.002}$

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PROGRAMMABLE INTERRUPT CONTROLLER

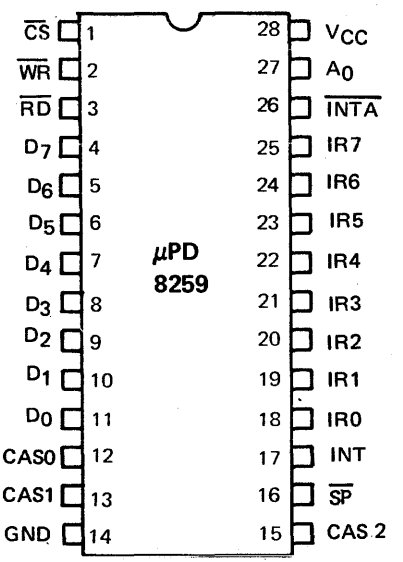
DESCRIPTION

The NEC μPD8259 is a programmable interrupt controller directly compatible with the 8080A/8085A/μPD780(Z80™). It can service eight levels of interrupts and contains on-chip logic to expand interrupt capabilities up to sixty-four levels with the addition of other μPD8259's. The user is offered a selection of priority algorithms to tailor the priority processing to meet his systems requirements. These algorithms can be dynamically modified during operation, expanding the versatility of the microprocessor system.

FEATURES

- Eight Level Priority Controller
- Programmable Base Vector Address
- Expandable to 64 Levels
- Programmable Interrupt Modes (Algorithms)
- Individual Request Mask Capability
- Single +5V Supply (No Clocks)
- Full Compatibility with 8080A/μPD780(Z80™)
- μPD8259-5 Compatible with 8085A Speeds
- Available in 28 Pin Plastic and Ceramic Packages

PIN CONFIGURATION



PIN NAMES

$D_7 - D_0$	Data Bus (Bi-Directional)
$\overline{RD}$	Read Input
$\overline{WR}$	Write Input
A_0	Command Select Address
CAS2 – CAS0	Cascade Lines
$\overline{SP}$	Slave Program Input
INT	Interrupt Output
$\overline{INTA}$	Interrupt Acknowledge Input
IR0 – iR7	Interrupt Request Inputs
$\overline{CS}$	Chip Select

*All data pertaining to the μPD8259-5 is preliminary.

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INTERRUPT REQUEST REGISTER (IRR) AND IN-SERVICE REGISTER (ISR)

The interrupt request register and in-service register store the in-coming interrupt request signals appearing on the IR0-7 lines (refer to functional block diagram). The inputs requesting service are stored in the IRR while the interrupts actually being serviced are stored in the ISR.

A positive transition on an IR input sets the corresponding bit in the Interrupt Request Register, and at the same time the INT output of the μPD8259 is set high. The IR input line must remain high until the first $\overline{\text{INTA}}$ input has been received. Multiple, non-masked interrupts occurring simultaneously can be stored in the IRR. The incoming $\overline{\text{INTA}}$ sets the appropriate ISR bit (determined by the programmed interrupt algorithm) and resets the corresponding IRR bit. The ISR bit stays high-active during the interrupt service subroutine until it is reset by the programmed End-of-Interrupt (EOI) command.

PRIORITY RESOLVER

The priority resolver decides the priority of the interrupt levels in the IRR. When the highest priority interrupt is determined it is loaded into the appropriate bit of the In-Service register by the first $\overline{\text{INTA}}$ pulse.

DATA BUS BUFFER

The 3-state, 8-bit, bi-directional data bus buffer interfaces the μPD8259 to the processor's system bus. It buffers the Control Word and Status Data transfers between the μPD8259 and the processor bus.

READ/WRITE LOGIC

The read/write logic accepts processor data and stores it in its Initialization Command Word (ICW) and Operation Command Word (OCW) registers. It also controls the transfer of the Status Data to the processor's data bus.

CHIP SELECT ($\overline{\text{CS}}$)

The μPD8259 is enabled when an active-low signal is received at this input. Reading or writing of the μPD8259 is inhibited when it is not selected.

WRITE ($\overline{\text{WR}}$)

This active-low signal instructs the μPD8259 to receive Command Data from the processor.

READ ($\overline{\text{RD}}$)

When an active-low signal is received on the $\overline{\text{RD}}$ input, the status of the Interrupt Request Register, In-Service Register, Interrupt Mask Register or binary code of the Interrupt Level is placed on the data bus.

INTERRUPT (INT)

The interrupt output from the μPD8259 is directly connected to the processor's INT input. The voltage levels of this output are compatible with the 8080's input voltage and timing requirements.

INTERRUPT MASK REGISTER (IMR)

The interrupt mask register stores the bits for the individual interrupt bits to be masked. The IMR masks the data in the ISR. Lower priority lines are not affected by masking a higher priority line.

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FUNCTIONAL DESCRIPTION (CONT.)

INTERRUPT ACKNOWLEDGE ($\overline{INTA}$)

The interrupt acknowledge signal is usually received from the 8228 (system controller for the 8080A). The system controller generates three $\overline{INTA}$ pulses to signal the 8259 to issue a 3-byte CALL instruction onto the data bus.

A_0

A_0 is usually connected to the processor's address bus. Together with $\overline{WR}$ and $\overline{RD}$ signals it directs the loading of data into the command register or the reading of status data. The following table illustrates the basic operations performed. Note that it is divided into three functions: Input, Output and Bus Disable distinguished by the $\overline{RD}$, $\overline{WR}$, and $\overline{CS}$ inputs.

μPD8259 BASIC OPERATION						
A_0	D_4	D_3	$\overline{RD}$	$\overline{WR}$	$\overline{CS}$	PROCESSOR INPUT OPERATION (READ)
0			0	1	0	IRR, ISR or IR → Data Bus ①
1			0	1	0	IMR → Data Bus
						PROCESSOR OUTPUT OPERATION (WRITE)
0	0	0	1	0	0	Data Bus → OCW2
0	0	1	1	0	0	Data Bus → OCW3
0	1	X	1	0	0	Data Bus → ICW1
1	X	X	1	0	0	Data Bus → OCW1, ICW2, ICW3 ②
						DISABLE FUNCTION
X	X	X	1	1	0	Data Bus → 3-State
X	X	X	X	X	1	Data Bus → 3-State

Notes: ① The contents of OCW2 written prior to the READ operation governs the selection of the IRR, ISR or Interrupt Level.

② The sequencer logic on the μPD8259 aligns these commands in the proper order.

CASCADE BUFFER/COMPARATOR. (For Use in Multiple μPD8259 Array.)

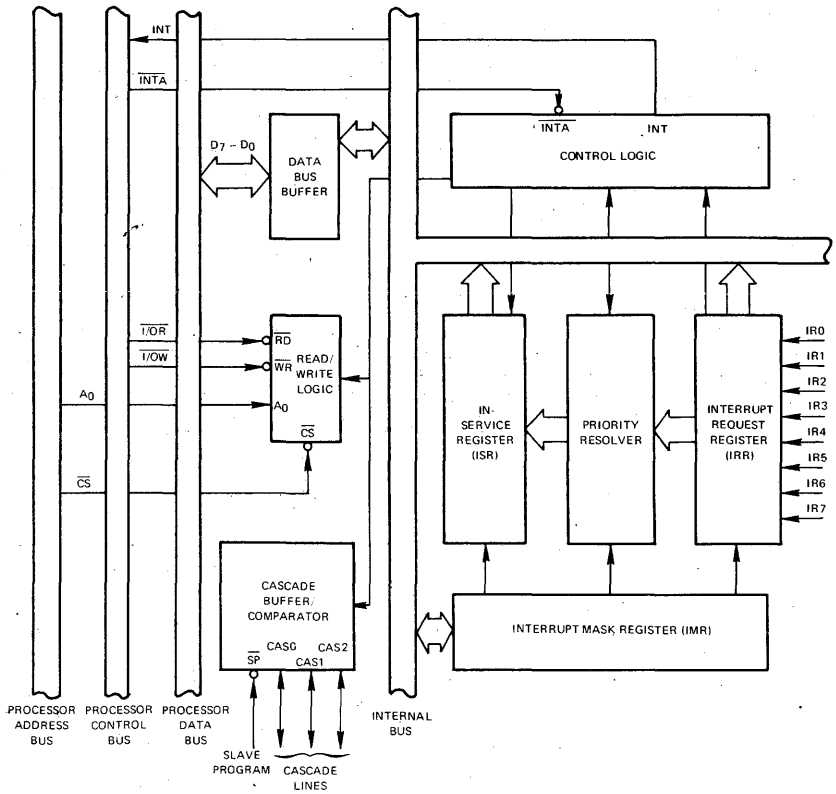
The ID's of all μPD8259's are buffered and compared in the cascade buffer/ comparator. The master μPD8259 will send the ID of the interrupting slave device along the CAS0, 1, 2 lines to all slave devices. The cascade buffer/comparator compares its preprogrammed ID to the CAS0, 1, 2 lines. The next two $\overline{INTA}$ pulses strobe the preprogrammed, 2 byte CALL routine address onto the data bus from the slave whose ID matches the code on the CAS0, 1, 2 lines.

SLAVE PROGRAM ($\overline{SP}$). (For Use in Multiple μPD8259 Array.)

The interrupt capability can be expanded to 64 levels by cascading multiple μPD8259's in a master-plus-slaves array. The master controls the slaves through the $\overline{CAS0}$, 1, 2 lines. The $\overline{SP}$ input to the device selects the CAS0-2 lines as either outputs ($\overline{SP}$=1) for the master or as inputs ($\overline{SP}$=0) for the slaves. For one device only the $\overline{SP}$ must be set to a logic "1" since it is functioning as a master.

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BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	0°C to +70°C
Storage Temperature	−65°C to +125°C
Voltage on Any Pin	−0.5 to +7 Volts (1)
Power Dissipation	1W

Note: (1) With respect to ground.

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

CAPACITANCE

T_a = 25°C; V_{CC} = GND = 0V

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input Capacitance	C_{IN}			10	pF	f_c = 1 MHz
I/O Capacitance	$C_{I/O}$			20	pF	Unmeasured Pins Returned to V_{SS}

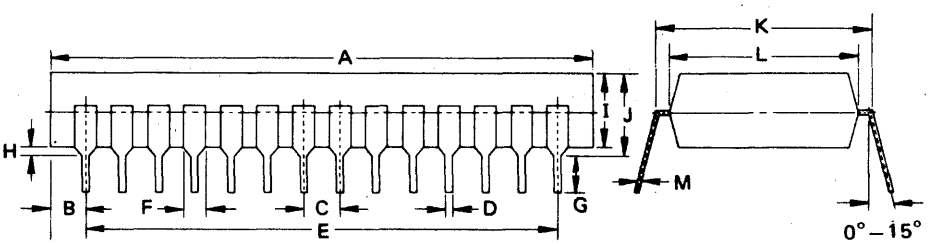
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DC CHARACTERISTICS

T_a = 0°C to +70°C; V_{CC} = +5V ± 5%

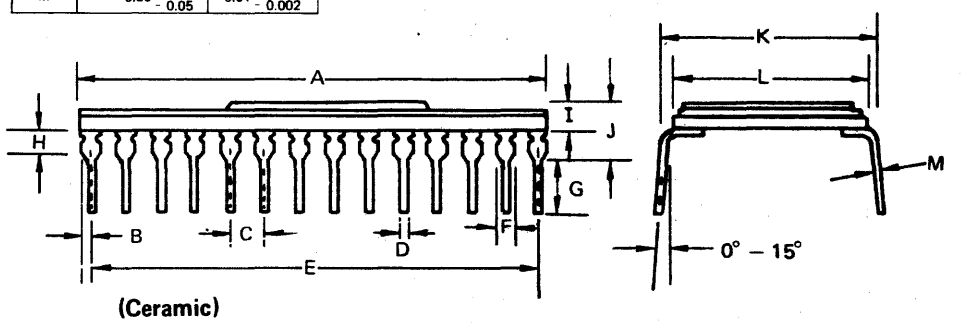
PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input Low Voltage	V_{IL}	-0.5		0.8	V	
Input High Voltage	V_{IH}	2.0		V_{CC} + 0.5V	V	
Output Low Voltage	V_{OL}			0.45	V	I_{OL} = 2 mA
Output High Voltage	V_{OH}	2.4			V	I_{OH} = -400 μA
Interrupt Output-High Voltage	V_{OH-INT}	2.4			V	I_{OH} = -400 μA
		3.5			V	I_{OH} = -50 μA
Input Leakage Current for IR_{0-7}	I_{IL} (IR_{0-7})			-300	μA	V_{IN} = 0V
				10	μA	V_{IN} = V_{CC}
Input Leakage Current for other inputs	I_{IL}			10	μA	V_{IN} = V_{CC} to 0V
Output Leakage Current	I_{LOL}			- 10	μA	V_{OUT} = 0.45 V
Output Leakage Current	I_{LOH}			10	μA	V_{OUT} = V_{CC}
V_{CC} Supply Current	I_{CC}			100	mA	

PACKAGE OUTLINE μPD8259C/D



(Plastic)

ITEM	MILLIMETERS	INCHES
A	38.0 MAX.	1.496 MAX.
B	2.49	0.098
C	2.54	0.10
D	0.5 ± 0.1	0.02 ± 0.004
E	33.02	1.3
F	1.5	0.059
G	2.54 MIN.	0.10 MIN.
H	0.5 MIN.	0.02 MIN.
I	5.22 MAX.	0.205 MAX.
J	5.72 MAX.	0.225 MAX.
K	15.24	0.6
L	13.2	0.52
M	$0.25^{+0.10}_{-0.05}$	$0.01^{+0.004}_{-0.002}$



(Ceramic)

ITEM	MILLIMETERS	INCHES
A	36.0 MAX.	1.41 MAX.
B	1.5 MAX.	0.059 MAX
C	2.54	0.1
D	0.50 · 0.1	0.02 · 0.004
E	33.0	1.299
F	1.27	0.05
G	3.2 MIN.	0.126 MIN
H	1.0 MIN	0.04 MIN
I	3.3 MAX.	0.13 MAX.
J	5.2 MAX.	0.20 MAX.
K	15.3	0.60
L	13.9	0.55
M	0.30 · 0.1	0.012 · 0.004

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AC CHARACTERISTICS

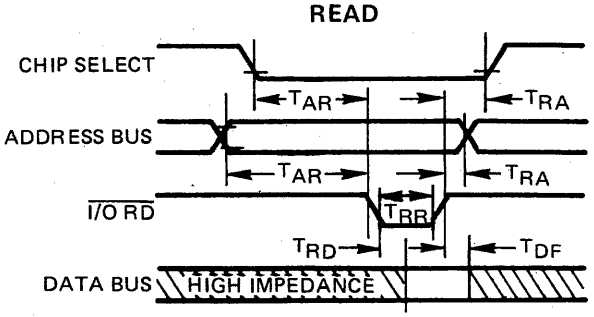
T_a = 0°C to +70°C; V_{CC} = +5V ± 5%; GND = 0V

PARAMETER	SYMBOL	LIMITS 8259 MIN	LIMITS 8259 MAX	LIMITS 8259-5 MIN	LIMITS 8259-5 MAX	UNIT	TEST CONDITIONS
READ							
$\overline{CS}/A_0$ Stable Before $\overline{RD}$ or $\overline{INTA}$	t_{AR}	50		50		ns	
$\overline{CS}/A_0$ Stable After $\overline{RD}$ or $\overline{INTA}$	t_{RA}	50		30		ns	
$\overline{RD}$ Pulse Width	t_{RR}	420		300		ns	
Data Valid From $\overline{RD}/\overline{INTA}$	t_{RD}		300		200	ns	①
Data Float After $\overline{RD}/\overline{INTA}$	t_{DF}	20	200	20	100	ns	①
WRITE							
A_0 Stable Before $\overline{WR}$	t_{AW}	50		50		ns	
A_0 Stable After $\overline{WR}$	t_{WA}	20		30		ns	
$\overline{CS}$ Stable Before $\overline{WR}$	t_{CW}	50				ns	
$\overline{CS}$ Stable After $\overline{WR}$	t_{WC}	20				ns	
$\overline{WR}$ Pulse Width	t_{WW}	400		300		ns	
Data Valid to $\overline{WR}$ (T.E.)	t_{DW}	300		250		ns	
Data Valid After $\overline{WR}$	t_{WD}	40		30		ns	
OTHER							
Width of Interrupt Request Pulse	t_{IW}	100		100		ns	
INT ↑ After IR ↑	t_{INT}	400		350		ns	
Cascade Line Stable After $\overline{INTA}$ ↑	t_{IC}	400		400		ns	

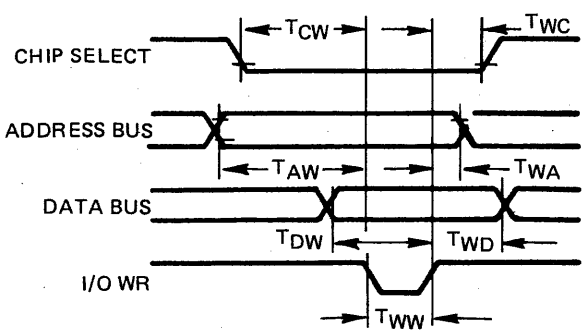
Note: ① For μPD8259: C_L = 100 pf; for μPD8259-5: C_L = 150 pf

TIMING WAVEFORMS

READ



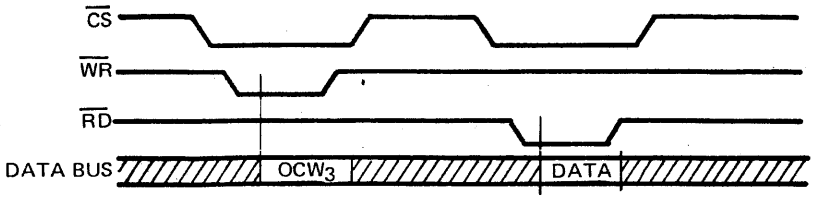
WRITE



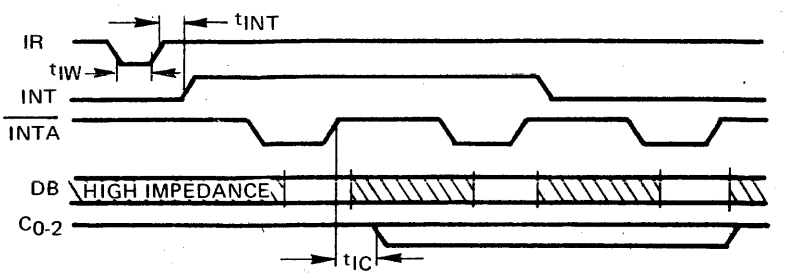
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TIMING WAVEFORMS (CONT.)

READ STATUS/POLL MODE

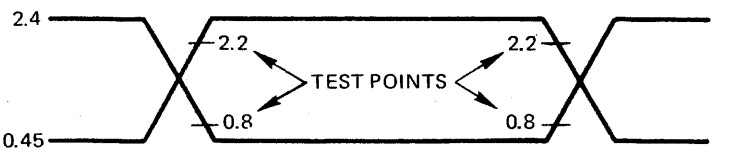


OTHER

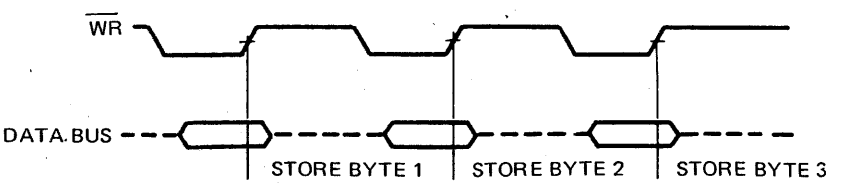


Note: IR must stay "high" at least until the leading edge of 1st $\overline{INTA}$.

INPUT WAVEFORMS FOR AC TESTS



INITIALIZATION SEQUENCE



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DETAILED OPERATIONAL DESCRIPTION

The μPD8259 derives its versatility from its programmable interrupt modes and its ability to jump to any memory address through programmable CALL instructions. The following sequence demonstrates how the μPD8259 interacts with the processor.

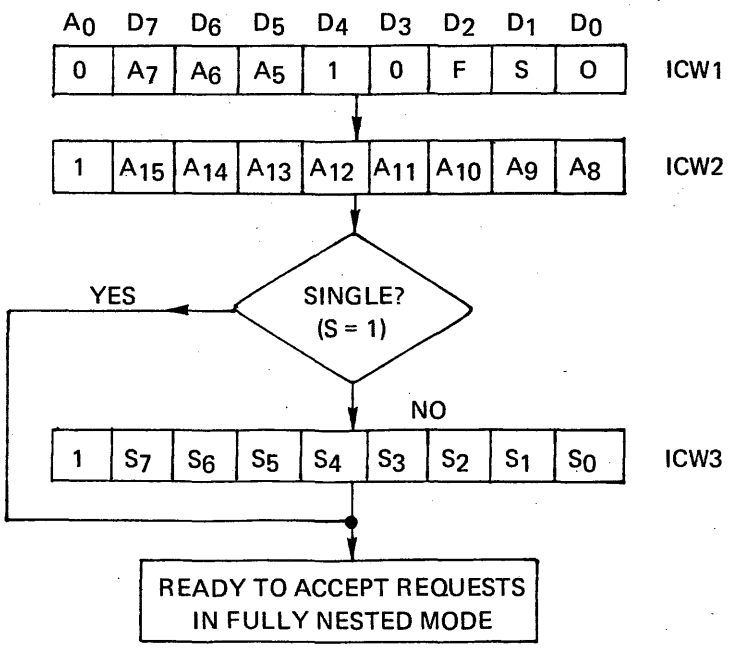
1. An interrupt or interrupts appearing on IR_{0-7} sets the corresponding IR bit(s) high. This in turn sets the corresponding IRR bit(s) high.
2. Once the IRR bit(s) has been set, the μPD8259 will resolve the priorities according to the preprogrammed interrupt algorithm. It then issues an INT signal to the processor.
3. The processor group issues an $\overline{INTA}$ to the μPD8259 when it receives the INT.
4. The $\overline{INTA}$ input to the μPD8259 from the processor group sets the highest priority ISR bit and resets the corresponding IRR bit. The $\overline{INTA}$ also signals the μPD8259 to issue an 8-bit CALL instruction op-code (11001101) onto its Data bus lines.
5. The CALL instruction code instructs the processor group to issue two more $\overline{INTA}$ pulses to the μPD8259.
6. The two $\overline{INTA}$ pulses signal the μPD8259 to place its preprogrammed interrupt vector address onto the Data bus. The first $\overline{INTA}$ releases the low-order 8-bits of the address and the second $\overline{INTA}$ releases the high-order 8-bits.
7. The μPD8259's CALL instruction sequence is complete. A preprogrammed EOI (End-of-Interrupt) command is issued to the μPD8259 at the end of an interrupt service routine to reset the ISR bit and allow the μPD8259 to service the next interrupt.

PROGRAMMING THE μPD8259

Two types of command words are required from the processor to fully define the operating modes of the μPD8259.

1. **Initialization Command Words (ICWs)**

   Each μPD8259 in the interrupt array must be initialized prior to normal operation. The initialization is performed by a 2 or 3-byte sequence clocked by $\overline{WR}$ pulses. Figure 1 shows this sequence. (Refer to Figure 2 for bit definitions.)



INITIALIZATION SEQUENCE – FIGURE 1.

PROGRAMMING THE μPD8259 (CONT.)

2. Operation Command Words (OCWs)

The operation command words are used to program the various interrupt algorithms listed below:

- Fully Nested Mode
- Rotating Priority Mode
- Special Mask Mode
- Polled Mode

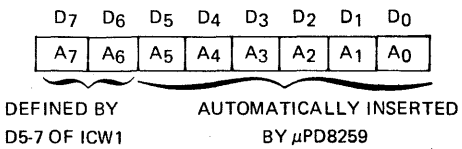
Once the μPD8259 has been initialized, OCWs can be written at any time.

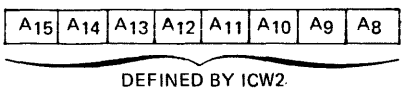
INITIALIZATION COMMAND WORDS 1 and 2 (ICW1 and ICW2)

When $A_0 = 0$ and $D_4 = 1$ in a command to the μPD8259, together with $\overline{CS} = 0$, it is recognized as Initialization Command Word 1. This is the start of the initialization sequence and causes the following to occur:

- The Interrupt Request edge-sense circuitry is reset so that an input must make a low-to-high transition to generate its interrupt.
- The initialization sequence clears Interrupt Mask Register to all unmasked and resets the Special Mask Mode and Status Read Flip-Flops.
- IR_7 input is set to priority 7.

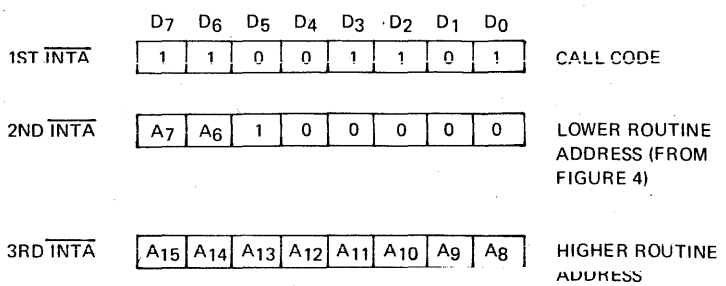
There are eight equally-spaced base vector addresses in memory for the eight interrupt inputs. The interval between the base vector addresses can be programmed to be either four or eight requiring 32 or 64 bytes in memory, respectively. The following shows how the address format is mapped onto the Data bus.





The μPD8259 automatically defines A_{0-4} with a separate address for each interrupt input. The base vector addresses A_{15-6} are programmed by ICW1 and ICW2. A_5 is either defined by the μPD8259 if the address interval is eight or must be user-defined if the interval is 4. The 8-byte CALL interval is consistent with 8080A processor RESTART instruction software. The 4-byte CALL interval can be used for a compact jump table. Refer to Figure 4 for a table of address formats.

The following is an example of an interrupt acknowledge sequence. The μPD8259 has been programmed for a CALL address (base vector address) interval of eight (F = 0) and there is an interrupt appearing on IR_4. The 3-byte sequence is strobed out to the Data bus by three $\overline{INTA}$ pulses.



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INITIALIZATION COMMAND WORD 3 (ICW3) ①

It is only necessary to program ICW3 when there are multiple μPD8259s in the interrupt array, i.e., S = 0. There are two types of ICW3s. The first is for programming the master μPD8259. The second is for the slaves.

1. ICW3-Master μPD8259. A "1" is set in S_{0-7} for each corresponding slave in the interrupt array. The S_{0-7} bits, together with $\overline{SP}$ = 1, instructs the cascade buffer/comparator to send the ID of the interrupting slave on the CAS0,1,2 lines.
2. ICW3-SLAVE μPD8259(s). Bits D_7-D_3 are "don't care" bits and have no effect on ICW3. The ID of each slave is programmed by bits D_{0-2} ($ID_{0,1,2}$). Once the master μPD8259 has sent out the first byte of the CALL sequence, the slave device(s) with their $\overline{SP}$ inputs set to Logic 0, compare their IDs appearing on the CAS0,1,2 lines through the cascade buffer/comparator. The slave whose ID matches the CAS0,1,2 code then issues bytes 2 and 3 of the CALL sequence.

OPERATIONAL COMMAND WORDS (OCWs) ②

Once the μPD8259 has been programmed with Initialization Command Words, it can now be programmed for the appropriate interrupt algorithm by the Operation Command Words. Interrupt algorithms in the μPD8259 can be changed at any time during program operation by issuing another set of Operation Command Words. The following sections describe the various algorithms available and their associated OCWs.

INTERRUPT MASKS

The individual Interrupt Request input lines are maskable by setting the corresponding bits in the Interrupt Mask Register to a logic "1" through OCW1. The actual masking is performed upon the contents of the In-Service Register (e.g., if Interrupt Request line 3 is to be masked, then only bit 3 of the IMR is set to logic "1." The IMR in turn acts upon the contents of the ISR to mask bit 3). Once the μPD8259 has acknowledged an interrupt, i.e., the μPD8259 has sent an INT signal to the processor and the system controller has sent it an $\overline{INTA}$ signal, the interrupt input, although it is masked, will inhibit lower priority requests from being acknowledged. There are two means of enabling these lower priority interrupt lines. The first is by issuing an End-of-Interrupt (EOI) through Operation Command Word 2 (OCW2), thereby resetting the appropriate ISR bit. The second approach is to select the Special Mask Mode through OCW3. The Special Mask Mode (SMM) and End-of-Interrupt (EOI) will be described in more detail further on.

FULLY NESTED MODE

The fully nested mode is the μPD8259's basic operating mode. It will operate in this mode after the initialization sequence, requiring no Operation Command Words for formatting. Priorities are set IR_0 through IR_7 with IR_0 the highest priority. After the interrupt has been acknowledged by the processor and system controller, only higher priorities will be serviced. Upon receiving an $\overline{INTA}$, the priority resolver determines the priority of the interrupt, the corresponding ISR bit is set, and the vector address is output to the Data bus. The EOI command resets the corresponding ISR bit at the end of its service routine.

Notes: ① Reference Figure 2
② Reference Figure 3

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OPERATIONAL COMMAND WORDS (CONT.)

ROTATING PRIORITY MODE COMMANDS

The two variations of Rotating Priorities are the Auto Rotate and Specific Rotate modes. These two modes are typically used to service interrupting devices of equivalent priorities.

1. Auto Rotate Mode

   Programming the Auto Rotate Mode through OCW2 assigns priorities 0-7 to the interrupt request input lines. Interrupt line IR_0 is set to the highest priority and IR_7 to the lowest. Once an interrupt has been serviced it is automatically assigned the lowest priority. That same input must then wait for the devices ahead of it to be serviced before it can be acknowledged again. The Auto Rotate Mode is selected by programming OCW2 in the following way (refer to Figure 3): set Rotate Priority bit "R" to a logic "1"; program EOI to a logic "1" and SEOI to a logic "0." The EOI and SEOI commands are discussed further on. The following is an example of the Auto Rotate Mode with devices requesting interrupts on lines IR_2 and IR_5.

   Before Interrupts are Serviced:

	IS_7	IS_6	IS_5	IS_4	IS_3	IS_2	IS_1	IS_0
In-Service Register	0	0	1	0	0	1	0	0
						→		Highest Priority
Priority Status Register	IR_7	IR_6	IR_5	IR_4	IR_3	IR_2	IR_1	IR_0

   According to the Priority Status Register, IR_2 has a higher priority than IR_5 and will be serviced first.

   After Servicing:

	IS_7	IS_6	IS_5	IS_4	IS_3	IS_2	IS_1	IS_0
In-Service Register	0	0	1	0	0	0	0	0
						→		Highest Priority
Priority Status Register	IR_2	IR_1	IR_0	IR_7	IR_6	IR_5	IR_4	IR_3

   At the completion of IR_2's service routine the corresponding In-Service Register bit, IS_2 is reset to "0" by the preprogrammed EOI command. IR_2 is then assigned the lowest priority level in the Priority Status Register. The μPD8259 is now ready to service the next highest interrupt, which in this case, is IR_5.

2. Specific Rotate Mode

   The priorities are set by programming the lowest level through OCW2. The μPD8259 then automatically assigns the highest priority. If, for example, IR_3 is set to the lowest priority (bits L_2, L_1, L_0 form the binary code of the bottom priority level), then IR_4 will be set to the highest priority. The Specific Rotate Mode is selected by programming OCW2 in the following manner: set Rotate Priority bit "R" to a logic "1," program EOI to a logic "0," SEOI to a logic "1" and L_2, L_1, L_0 to the lowest priority level. If EOI is set to a logic "1," the ISR bit defined by L_2, L_1, L_0 is reset.

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END-OF-INTERRUPT (EOI) AND SPECIFIC END-OF-INTERRUPT (SEOI)

The End-of-Interrupt or Specific End-of-Interrupt command must be issued to reset the appropriate In-Service Register bit before the completion of a service routine. Once the ISR bit has been reset to logic "0," the μPD8259 is ready to service the next interrupt.

Two types of EOIs are available to clear the appropriate ISR bit depending on the μPD8259's operating mode.

1. Non-Specific End-of-Interrupt (EOI)

   When operating in interrupt modes where the priority order of the interrupt inputs is preserved (e.g., fully nested mode), the particular ISR bit to be reset at the completion of the service routine can be determined. A non-specific EOI command will automatically reset the highest priority ISR bit of those set. The highest priority ISR bit must necessarily be the interrupt being serviced and must necessarily be the service subroutine returned from.

2. Specific End-of-Interrupt (SEOI)

   When operating in interrupt modes where the priority order of the interrupt inputs is not preserved (e.g., rotating priority mode) the last serviced interrupt level may not be known. In these modes a Specific End-of-Interrupt must be issued to clear the ISR bit at the completion of the interrupt service routine. The SEOI is programmed by setting the appropriate bits in OCW3 (Figure 2) to logic "1"s. Both the EOI and SEOI bits of OCW3 must be set to a logic "1" with L_2, L_1, L_0 forming the binary code of the ISR bit to be reset.

SPECIAL MASK MODE

Setting up an interrupt mask through the Interrupt Mask Register (refer to Interrupt Mask Register section) by setting the appropriate bits in OCW1 to a logic "1" will inhibit lower priority interrupts from being acknowledged. In applications requiring that the lower priorities be enabled while the IMR is set, the Special Mask Mode can be used. The SMM is programmed in OCW3 by setting the appropriate bits to a logic "1." Once the SMM is set, the μPD8259 remains in this mode until it is reset. The Special Mask Mode does not affect the higher priority interrupts.

POLLED MODE

In the Poll Mode the processor must be instructed to disable its interrupt input (INT). Interrupt service is initiated through software by a Poll Command. The Poll Mode is programmed by setting the Poll Mode bit in OCW3 (P = 1), during a $\overline{WR}$ pulse. The following $\overline{RD}$ pulse is then considered as an interrupt acknowledge. If an interrupt input is present, that $\overline{RD}$ pulse sets the appropriate ISR bit and reads the interrupt priority level. The Poll Mode is a one-time operation and must be programmed through OCW3 before every read. The word strobed onto the Data bus during Poll Mode is of the form:

D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
I	X	X	X	X	W_2	W_1	W_0

where: I = 1 if there is an interrupt requesting service
= 0 if there are no interrupts

$W_{2\text{-}0}$ forms the binary code of the highest priority level of the interrupts requesting service

The Poll Mode can be used when an interrupt service routine is common to several interrupt inputs. The $\overline{INTA}$ sequence is no longer required offering a saving in ROM space. The Poll Mode can also be used to expand the number of interrupts beyond 64.

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READING μPD8259 STATUS

The following major registers' status is available to the processor by appropriately formatting OCW3 and issuing a $\overline{RD}$ command.

INTERRUPT REQUEST REGISTER (8-BITS)

The Interrupt Request Register stores the interrupt levels awaiting acknowledgement. Once it has been acknowledged, the highest priority in-service bit is reset. (Note that the Interrupt Mask Register has no effect on the IRR.) A $\overline{WR}$ command must be issued with OCW3 prior to issuing the $\overline{RD}$ command. The bits which determine whether the IRR and ISR are being read from are RIS and ERIS. To read contents of the IRR, ERIS must be logic "1" and RIS a logic "0."

IN-SERVICE REGISTER (8-BITS)

The In-Service Register stores the priorities of the interrupt levels being serviced. Assertion of an End-of-Interrupt (EOI) updates the ISR to the next priority level. A $\overline{WR}$ command must be issued with OCW3 prior to issuing the $\overline{RD}$ command. Both ERIS and RIS should be set to a logic "1."

INTERRUPT MASK REGISTER (8-BITS)

The Interrupt Mask Register holds mask data modifying interrupt levels. To read the IMR status a $\overline{WR}$ pulse preceding the $\overline{RD}$ is not necessary. The IMR data is available to the data bus when $\overline{RD}$ is asserted with A_0 at a logic "1."

A single OCW3 is sufficient to enable successive status reads providing it is of the same register. A status read is over-ridden by the Poll Mode where bits P and ERIS of OCW3 are set to a logic "1."

CASCADING MULTIPLE μPD8259s

If more than eight interrupt levels are required, multiple μPD8259s can be cascaded with one master and up to eight slaves, to accommodate up to 64 levels of interrupt.

As shown in Figure 5, the master device directs the appropriate slave to release its CALL address through its three cascade lines (CAS0,1,2).

The INT output of the slave devices go to the IR inputs of the master device. The master μPD8259's INT output is connected to the processor's control bus. When the slave device signals the master that it has acknowledged an interrupt, the master issues an 8080A CALL Op-code at the first $\overline{INTA}$ pulse. The master then signals that slave device (via CAS0,1,2) to issue the appropriate CALL address during the second and third $\overline{INTA}$ pulses.

The slave address code is present on cascade lines 0,1,2 (active-high logic) from the trailing edge of the first $\overline{INTA}$ to the trailing edge of the third $\overline{INTA}$. Each device in the μPD8259 array must be individually initialized and can be programmed in different operating modes. Two End-of-Interrupt commands must be issued for the master and its corresponding slave. An address decoder is used to drive the Chip Select inputs for each μPD8259 in the array. The Slave Program ($\overline{SP}$) input must be held at a logic "0" level for each slave device and held at logic "1" level for the master. The $\overline{SP}$ input selects the Cascade lines as either inputs ($\overline{SP}$ = 0) or outputs ($\overline{SP}$ = 1).

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INITIALIZATION COMMAND WORD FORMAT

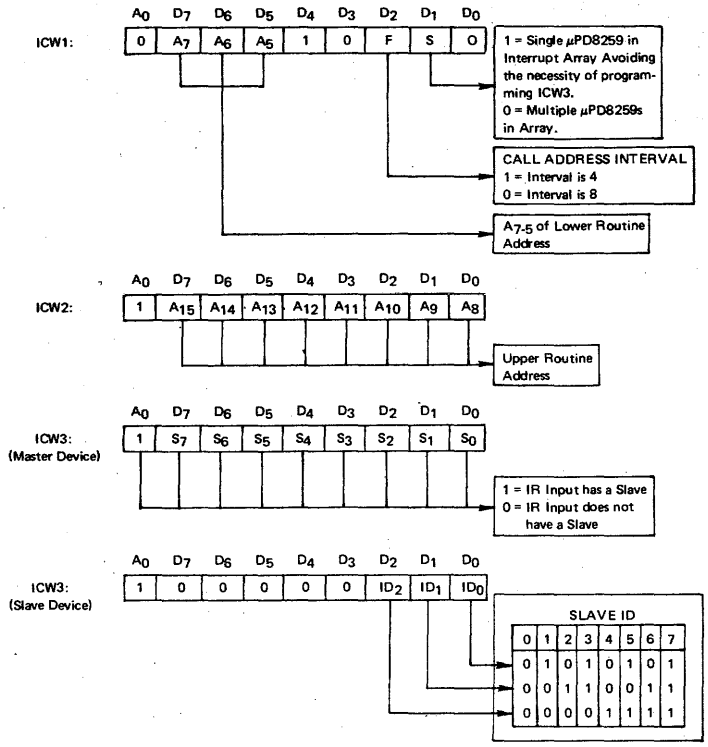


FIGURE 2

OPERATION COMMAND WORD FORMAT

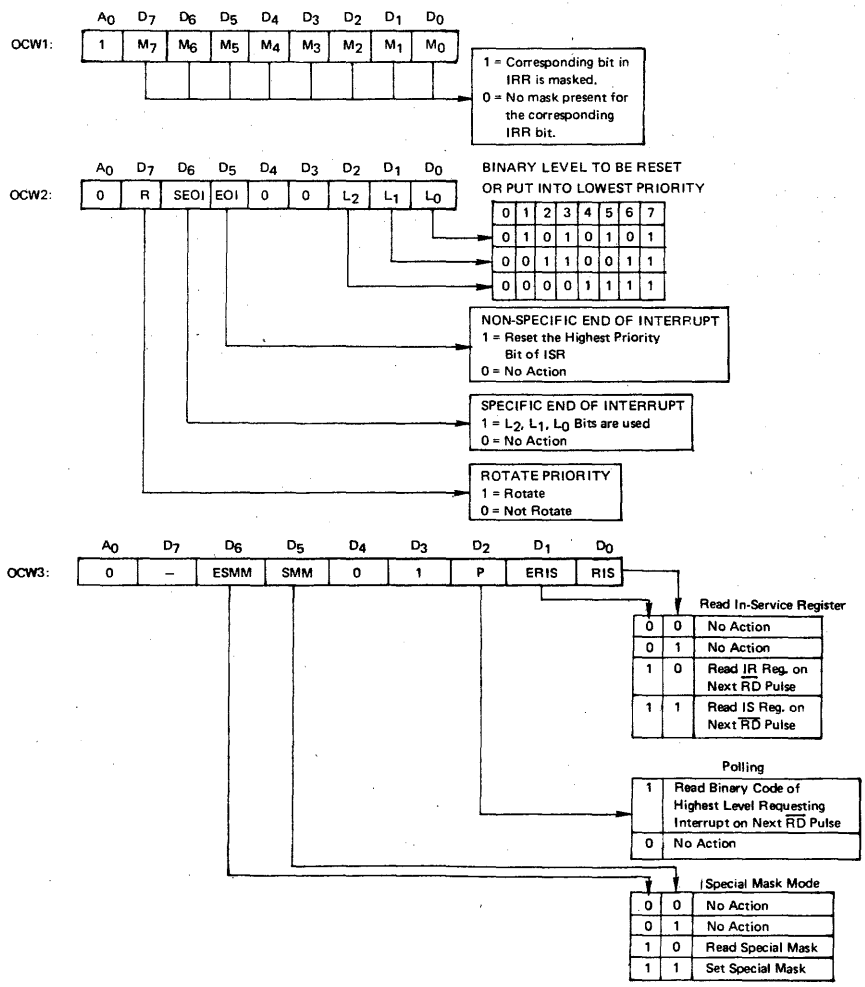


FIGURE 3

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SUMMARY OF OPERATION COMMAND WORD PROGRAMMING

	A_0	D_4	D_3				
OCW1	1	X	X	M_7-M_0			IMR (Interrupt Mask Register) $\overline{WR}$ loads IMR data while $\overline{RD}$ reads status
OCW2	0	0	0	R	SEOI	EOI	
				0	0	0	No Action
				0	0	1	Non-Specific End-of-Interrupt
				0	1	0	No Action
				0	1	1	Specific-End-of-Interrupt L_2, L_1, L_0 forms binary representation of level to be reset.
				1	0	0	No Action
				1	0	1	Rotate Priority at End-of-Interrupt (Auto Mode)
				1	1	0	Rotate Priority, L_2, L_1, L_0 specifies bottom priority without End-of-Interrupt
				1	1	1	Rotate Priority at End-of-Interrupt (Specific Mode). L_2, L_1, L_0 specifies bottom priority, and its In-Service Register bit is reset.
OCW3	0	0	1	ESMM	SMM		
				0	0		Special Mask not affected
				0	1		
				1	0		Reset Special Mask
				1	1		Set Special Mask
				ERIS	RIS		
				0	0		No Action
				0	1		
				1	0		Read IR Register Status
				1	1		Read IS Register Status

LOWER MEMORY INTERRUPT VECTOR ADDRESS

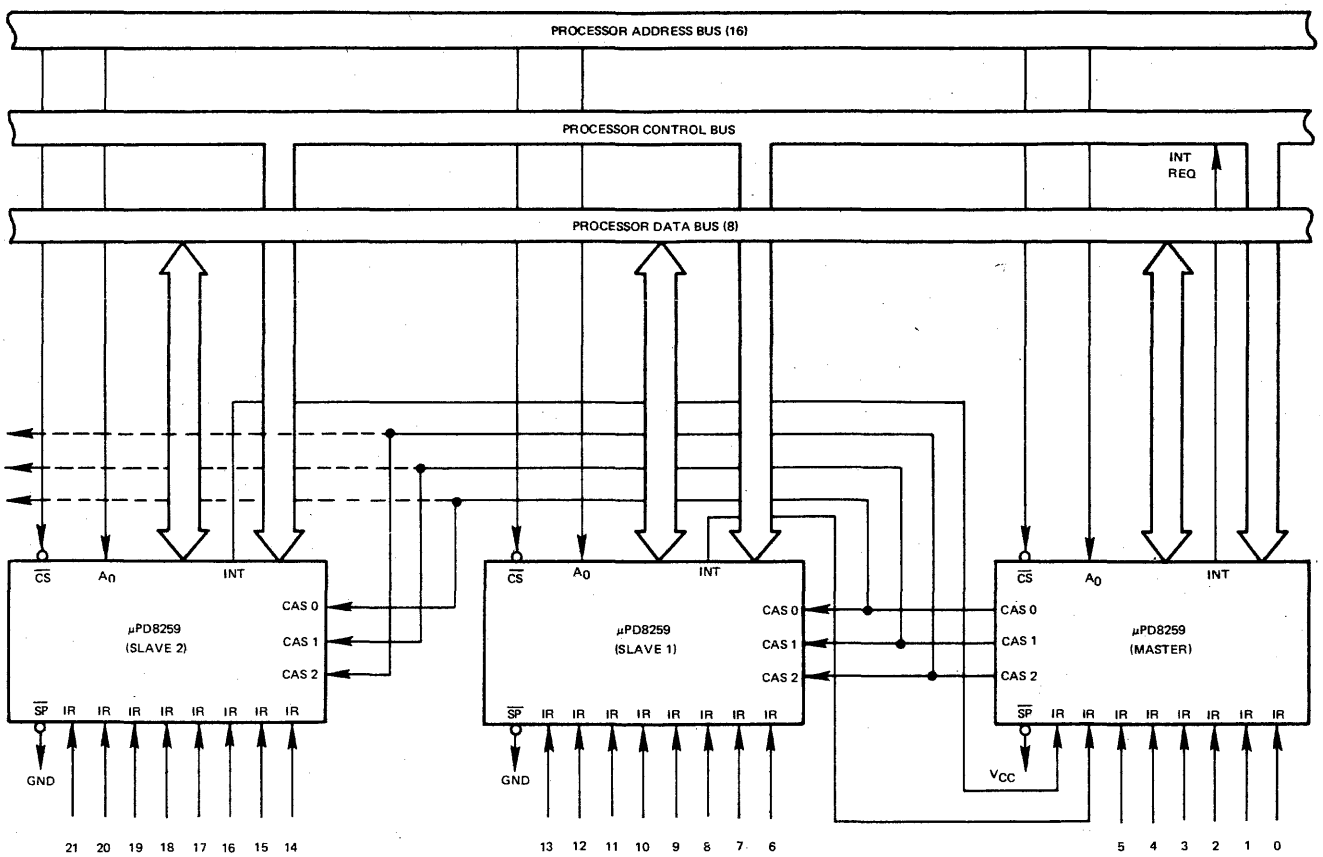
	INTERVAL = 4								INTERVAL = 8							
	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
IR_7	A_7	A_6	A_5	1	1	1	0	0	A_7	A_6	1	1	1	0	0	0
IR_6	A_7	A_6	A_5	1	1	0	0	0	A_7	A_6	1	1	0	0	0	0
IR_5	A_7	A_6	A_5	1	0	1	0	0	A_7	A_6	1	0	1	0	0	0
IR_4	A_7	A_6	A_5	1	0	0	0	0	A_7	A_6	1	0	0	0	0	0
IR_3	A_7	A_6	A_5	0	1	1	0	0	A_7	A_6	0	1	1	0	0	0
IR_2	A_7	A_6	A_5	0	1	0	0	0	A_7	A_6	0	1	0	0	0	0
IR_1	A_7	A_6	A_5	0	0	1	0	0	A_7	A_6	0	0	1	0	0	0
IR_0	A_7	A_6	A_5	0	0	0	0	0	A_7	A_6	0	0	0	0	0	0

FIGURE 4

Note: Insure that the processor's interrupt input is disabled during the execution of any control command and initialization sequence for all μPD8259s.

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CASCADING THE μPD8259



INSTRUCTION SET

Instruction Number	Mnemonic	A_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	Operation Description
1	ICW1 A	0	A_7	A_6	A_5	1	0	1	1	0	Byte 1 Initialization, Format = 4, Single
2	ICW1 B	0	A_7	A_6	A_5	1	0	1	0	0	Byte 1 Initialization, Format = 4, Not Single
3	ICW1 C	0	A_7	A_6	A_5	1	0	0	1	0	Byte 1 Initialization, Format = 8, Single
4	ICW1 D	0	A_7	A_6	A_5	1	0	0	0	0	Byte 1 Initialization, Format = 8, Not Single
5	ICW2	1	A_{15}	A_{14}	A_{13}	A_{12}	A_{11}	A_{10}	A_9	A_8	Byte 2 Initialization (Address No. 2)
6	ICW3 M	1	S_7	S_6	S_5	S_4	S_3	S_2	S_1	S_0	Byte 2 Initialization — MASTER
7	ICW3 S	1	0	0	0	0	0	S_2	S_1	S_0	Byte 3 Initialization — SLAVE
8	OCW1	1	M_7	M_6	M_5	M_4	M_3	M_2	M_1	M_0	Load Mask Register, Read Mask Register
9	OCW2 E	0	0	0	1	0	0	0	0	0	Non-Specific EOI
10	OCW2 SE	0	0	1	1	0	0	L_2	L_1	L_0	Specific EOI, L_2, L_1, L_0 Code of IS to be Reset
11	OCW2 RE	0	1	0	1	0	0	0	0	0	Rotate at EOI (Auto Mode)
12	OCW2 RSE	0	1	1	1	0	0	L_2	L_1	L_0	Rotate at EOI (Specific Mode). L_2, L_1, L_0 Code of Line to be Reset and Selected as Bottom Priority.
13	OCW2 RS	0	1	1	0	0	0	L_2	L_1	L_0	L_2, L_1, L_0 — Code of Bottom Priority Line.
14	OCW3 P	0	—	0	0	0	1	1	0	0	Poll Mode
15	OCW3 RIS	0	—	0	0	0	1	0	1	1	Read IS Register
16	OCW3 RR	0	—	0	0	0	1	0	1	0	Read Requests Register
17	OCW3 SM	0	—	1	1	0	1	0	0	0	Set Special Mask Mode
18	OCW3 RSM	0	—	1	0	0	1	0	0	0	Reset Special Mask Mode

Note: Insure that the processor's interrupt input is disabled during the execution of any control command and initialization sequence for all μPD8259s.

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PROGRAMMABLE KEYBOARD/DISPLAY INTERFACE

DESCRIPTION

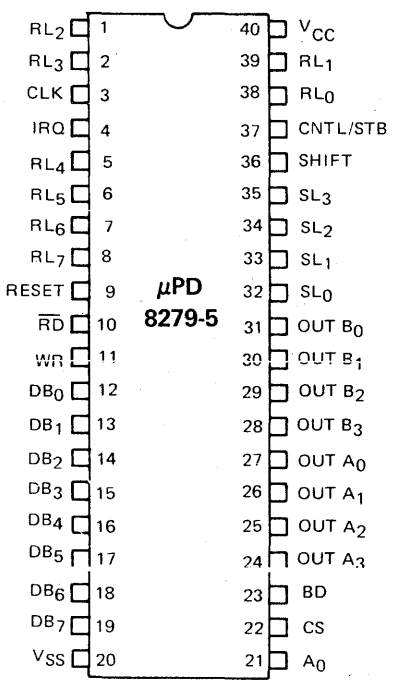
The μPD8279-5 is a programmable keyboard and display Input/Output device. It provides the user with the ability to display data on alphanumeric segment displays or simple indicators. The display RAM can be programmed as 16 x 8 or a dual 16 x 4 and loaded or read by the host processor. The display can be loaded with right or left entry with an auto-increment of the display RAM address.

The keyboard interface provides a scanned signal to a 64 contact key matrix expandable to 128. General sensors or strobed keys may also be used. Keystrokes are stored in an 8 character FIFO and can be either 2 key lockout or N key rollover. Keyboard entries generate an interrupt to the processor.

FEATURES

- Programmable by Processor
- 32 HEX or 16 Alphanumeric Displays
- 64 Expandable to 128 Keyboard
- Simultaneous Keyboard and Display
- 8 Character Keyboard – FIFO
- 2 Key Lockout or N Key Rollover
- Contact Debounce
- Programmable Scan Timer
- Interrupt on Key Entry
- Single +5 Volt Supply
- Fully Compatible with 8080A, 8085A, μPD780 (Z80™)
- Available in 40 Pin Plastic Package

PIN CONFIGURATION



PIN NAMES

DB_{0-7}	Data Bus (Bi-directional)
CLK	Clock Input
RESET	Reset Input
$\overline{CS}$	Chip Select
$\overline{RD}$	Read Input
$\overline{WR}$	Write Input
A_0	Buffer Address
IRQ	Interrupt Request Output
SL_{0-3}	Scan Lines
RL_{0-7}	Return Lines
SHIFT	Shift Input
CNTL/STB	Control/Strobe Input
$OUT\ A_{0-3}$	Display (A) Outputs
$OUT\ B_{0-3}$	Display (B) Outputs
$\overline{BD}$	Bland Display Output

TM: Z80 is a registered trademark of Zilog.

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μPD8279-5

FUNCTIONAL DESCRIPTION

The μPD8279-5 has two basic functions: 1) to control displays to output and 2) to control a keyboard for input. Its specific purpose is to unburden the host processor from monitoring keys and refreshing displays. The μPD8279-5 is designed to directly interface the microprocessor bus. The microprocessor must program the operating mode to the μPD8279-5, these modes are as follows:

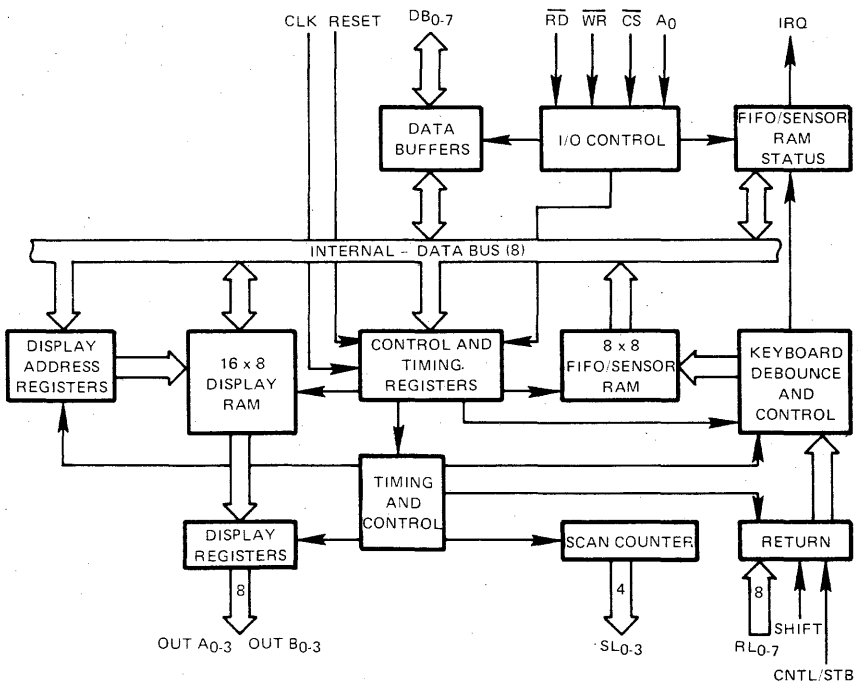
Output Modes

- 8 or 16 Character Display
- Right or Left Entry

Input Modes

- Scanned Keyboard with Encoded 8 x 8 x 4 Key Format or Decoded 4 x 8 x 8 Scan Lines.
- Scanned Sensor Matrix with Encoded 8 x 8 or Decoded 4 x 8 Scan Lines.
- Strobed Input.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	0°C to +70°C
Storage Temperature	-65°C to +125°C
All Output Voltages	-0.5 to +7 Volts①
All Input Voltages	-0.5 to +7 Volts①
Supply Voltages	-0.5 to +7 Volts①
Power Dissipation	1W

Note: ① With respect to V_{SS}

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

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PIN IDENTIFICATION

PIN			DESCRIPTION
NO.	SYMBOL	NAME	
1, 2, 5, 6, 7, 8, 38, 39	RL_{0-7}	Return Lines	Return line inputs which are connected to the scan lines through the keys or sensor switches. They have active internal pullups to keep them high until a switch closure pulls one low. They also serve as an 8-bit input in the Strobed Input mode.
3	CLK	Clock	Clock from system used to generate internal timing.
4	IRQ	Interrupt Request	Interrupt Request. In a keyboard mode, the interrupt line is high when there is data in the FIFO/Sensor RAM. The interrupt line goes low with each FIFO/Sensor RAM read and returns high if there is still information in the RAM. In a sensor mode, the interrupt line goes high whenever a change in a sensor is detected.
9	Reset	Reset Input	A high signal on this pin resets the μPD8279-5.
10	$\overline{RD}$	Read Input	Input/Output read and write. These signals enable the data buffers to either send data to the external bus or receive it from the external bus.
11	$\overline{WR}$	Write Input	
12-19	DB_{0-7}	Data Bus	Bi-Directional data bus. All data and commands between the processor and the μPD8279-5 are transmitted on these lines.
20	V_{SS}	Ground Reference	Power Supply Ground
21	A_0	Buffer Address	Buffer Address. A high on this line indicates the signals in or out are interpreted as a command or status. A low indicates that they are data.
22	$\overline{CS}$	Chip Select	Chip Select. A low on this pin enables the interface functions to receive or transmit.
23	$\overline{BD}$	Blank Display Output	Blank Display. This output is used to blank the display during digit switching or by a display blanking command.
24-27	$OUT\ A_{0-3}$	Display A Outputs	These two ports are the outputs for the 16 x 4 display refresh registers. The data from these outputs is synchronized to the scan lines (SL_0-SL_3) for multiplexed digit displays. The two 4-bit ports may be blanked independently. These two ports may also be considered as one 8-bit port.
28-31	$OUT\ B_{0-3}$	Display B Outputs	
32-35	SL_{0-3}	Scan Lines	Scan Lines which are used to scan the key switch or sensor matrix and the display digits. These lines can be either encoded (1 of 16) or decoded (1 of 4).
36	Shift	Shift Input	The shift input status is stored along with the key position on key closure in the Scanned Keyboard modes. It has an active internal pullup to keep it high until a switch closure pulls it low.
37	CNTL/STB	Control/ Strobe Input	For keyboard modes this line is used as a control input and stored like status on a key closure. The line is also the strobe line that enters the data into the FIFO in Strobed input mode (Rising Edge). It has an active internal pullup to keep it high until a switch closure pulls it low.
40	V_{CC}	+5V Input	Power Supply Input

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DC CHARACTERISTICS

T_a = 0°C to +70°C; V_{CC} = +5V ± 10%; V_{SS} = 0V.

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN	TYP	MAX		
Input Low Voltage for Shift, Control and Return Lines	V_{IL1}	-0.5		1.4	V	
Input Low Voltage (Others)	V_{IL2}	-0.5		0.8	V	
Input High Voltage for Shift, Control and Return Lines	V_{IH1}	2.2			V	
Input High Voltage (Others)	V_{IH2}	2.0			V	
Output Low Voltage	V_{OL}			0.45	V	I_{OL} = 2.2 mA
Output High Voltage on Interrupt Line	V_{OH}	3.5			V	I_{OH} = -400 μA
Input Current on Shift, Control and Return Lines	I_{IL1}			+10	μA	$V_{IN} = V_{CC}$
				-100	μA	V_{IN} = 0V
Input Leakage Current (Others)	I_{IL2}			±10	μA	$V_{IN} = V_{CC}$ to 0V
Output Float Leakage	I_{OFL}			±10	μA	$V_{OUT} = V_{CC}$ to 0V
Power Supply Current	I_{CC}			120	mA	

CAPACITANCE

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN	TYP	MAX		
Input Capacitance	C_{IN}	5		10	pF	$V_{IN} = V_{CC}$
Output Capacitance	C_{OUT}	10		20	pF	$V_{OUT} = V_{CC}$

AC CHARACTERISTICS

T_a = 0°C to +70°C; V_{CC} = +5V ± 10%; V_{SS} = 0V

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITIONS
		MIN	TYP	MAX		
READ						
Address Stable Before $\overline{READ}$	t_{AR}	0			ns	
Address Hold Time for $\overline{READ}$	t_{RA}	0			ns	
$\overline{READ}$ Pulse Width	t_{RR}	250			ns	
Data Delay from $\overline{READ}$	t_{RD}			150	ns	C_L = 150 pF
Address to Data Valid	t_{AD}			250	ns	C_L = 150 pF
$\overline{READ}$ to Data Floating	t_{DF}	10		100	ns	
Read Cycle Time	t_{RCY}	1			μs	
WRITE						
Address Stable Before $\overline{WRITE}$	t_{AW}	0			ns	
Address Hold Time for $\overline{WRITE}$	t_{WA}	0			ns	
$\overline{WRITE}$ Pulse Width	t_{WW}	250			ns	
Data Set Up Time for $\overline{WRITE}$	t_{DW}	150			ns	
Data Hold Time for $\overline{WRITE}$	t_{WD}	0			ns	
OTHER						
Clock Pulse Width	$t_{\phi W}$	120			ns	
Clock Period	t_{CY}	320			ns	

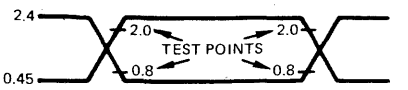
GENERAL TIMING

Keyboard Scan Time:	5.1 ms	Digit-on Time:	480 μs
Keyboard Debounce Time:	10.3 ms	Blanking Time:	160 μs
Key Scan Time:	80 μs	Internal Clock Cycle:	10 μs
Display Scan Time:	10.3 ms		

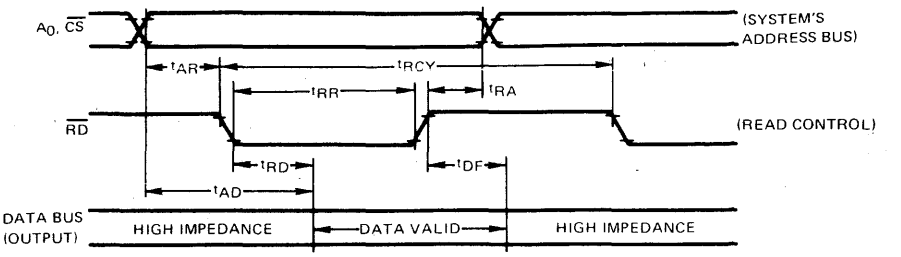
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TIMING WAVEFORMS

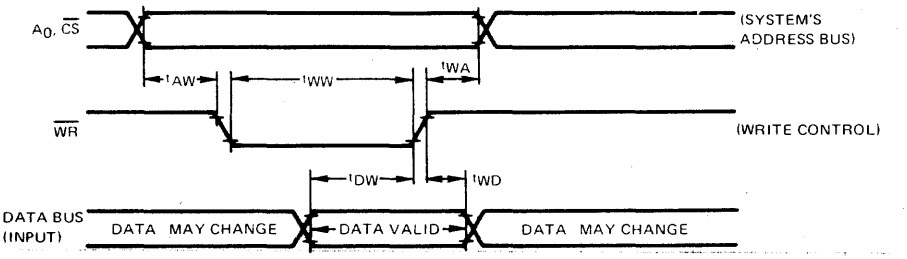
INPUT FOR AC TESTS



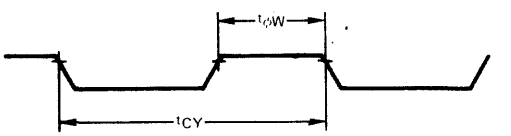
READ



WRITE



CLOCK INPUT



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OPERATIONAL DESCRIPTION

The following is a description of each section of the μPD8279-5. See the block diagram for functional reference.

I/O Control and Data Buffers

Communication to and from the μPD8279-5 is performed by selecting $\overline{CS}$, A_0, $\overline{RD}$ and $\overline{WR}$. The type of information written or read by the processor is selected by A_0. A logic 0 states that information is data while a 1 selects command or status. $\overline{RD}$ and $\overline{WR}$ select the direction by which the transfer occurs through the Data Buffers. When the chip is deselected ($\overline{CS}$ = 1) the bi-directional Data Buffers are in a high impedance state thus enabling the μPD8279-5 to be tied directly to the processor data bus.

Timing Registers and Timing Control

The Timing Registers store the display and keyboard modes and other conditions programmed by the processor. The timing control contains the timing counter chain. One counter is a divide by N scaler which may be programmed to match the processor cycle time. The scaler must take a value between 2 and 31 in binary. A value which scales the internal frequency to 100 KHz gives a 5.1 ms scan time and 10.3 ms switch debounce. The other counters divide down to make key, row matrix and display scans.

Scan Counter

The scan counter can operate in either the encoded or decoded mode. In the encoded mode, the counter provides a count which must be decoded to provide the scan lines. In the decoded mode, the counter provides a 1 out of 4 decoded scan. In the encoded mode the scan lines are active high and in the decoded mode they are active low.

Return Buffers, Keyboard Debounce and Control

The eight return lines are buffered and latched by the return buffers. In the keyboard mode these lines are scanned sampling for key closures in each row. If the debounce circuit senses a closure, about 10 ms are timed out and a check is performed again. If the switch is still pressed, the address of the switch matrix plus the status of shift and control are written into the FIFO. In the scanned sensor mode, the contents of return lines are sent directly to the sensor RAM (FIFO) each key scan. In the strobed mode, the transfer takes place on the rising edge of CNTL/STB.

FIFO/Sensor RAM and Status

This section is a dual purpose 8 x 8 RAM. In strobe or keyboard mode it is a FIFO. Each entry is pushed into the FIFO and read in order. Status keeps track of the number of entries in the FIFO. Too many reads or writes to the FIFO will be treated as an error condition. The status logic generates an IRQ whenever the FIFO has an entry. In the sensor mode the memory is a sensor RAM which detects changes in the status of a sensor. If a change occurs, the IRQ is generated until the change is acknowledged.

Display Address Registers and Display RAM

The Display Address Register contains the address of the word being read or written by the processor, as well as the word being displayed. This address may be programmed to auto-increment after each read or write. The display RAM may be read by the processor any time after the mode and address is set. Data entry to the display RAM may be set to either right or left entry.

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COMMAND OPERATION

The commands programmable to the μPD8279-5 via the data bus with $\overline{CS}$ active (0) and A_0 high are as follows:

Keyboard/Display Mode Set

0	0	0	D	D	K	K	K

MSB LSB

Display Mode:

DD

0	0	8-8-bit character display – Left entry
0	1 ①	16-8 bit character display – Left entry
1	0	8-8 bit character display – Right entry
1	1	16-8 bit character display – Right entry

Note: ① Power on default condition

Keyboard Mode:

KKK

0	0	0	Encoded Scan – 2 Key Lockout
0	0	1	Decoded Scan – 2 Key Lockout
0	1	0	Encoded Scan – N Key Rollover
0	1	1	Decoded Scan – N Key Rollover
1	0	0	Encoded Scan-Sensor Matrix
1	0	1	Decoded Scan-Sensor Matrix
1	1	0	Strobed Input, Encoded Display Scan
1	1	1	Strobed Input, Decoded Display Scan

Program Clock

0	0	1	P	P	P	P	P

Where PPPPP is the prescaler value between 2 and 31 this prescaler divides the external clock by PPPPP to develop its internal frequency. After reset, a default value of 31 is generated.

Read FIFO/Sensor RAM

0	1	0	A1	X	A	A	A

$A_0 = 0$

A_I is the auto-increment flag. AAA is the row to be read by the processor. The read command is accomplished with ($\overline{CS} \cdot RD \cdot \overline{A0}$) by the processor. If A_I is 1, the row select counter will be incremented after each read. Note that auto-incrementing has no effect on the display.

Read Display RAM

0	1	1	A1	A	A	A	A

$A_0 = 0$

Where A_I is the auto-increment flag and AAAA is the character which the processor is about to read.

Write Display RAM

1	0	0	A1	A	A	A	A

where AAAA is the character the processor is about to write.

Display Write Inhibit Blanking

1	0	1	X	IW A	IW B	BL A	BL B

Where IWA and IWB are Inhibit Writing nibble A and B respectively, and BLA, BLB are blanking. When using the display as a dual 4-bit, it is necessary to mask one of the 4-bit halves to eliminate interaction between the two halves. This is accomplished with the IW flags. The BL flags allow the programmer to blank either half of the display independently. To blank a display formatted as a single 8-bit, it is necessary to set both BLA and BLB. Default after a reset is all zeros. All signals are active high (1).

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Clear

1	1	0	C_D	C_D	C_D	C_F	C_A

C_D	C_D	C_D	
1	0	X	All zeros
1	1	0	AB = 20_{16}
1	1	1	All ones
0	X	X	Disable clear display

This command is used to clear the display RAM, the FIFO, or both. The C_D options allow the user the ability to clear the display RAM to either all zeros or all ones.

C_F clears the FIFO.
C_A clears all.

Clearing the display takes one complete display scan. During this time the processor can't write to the display RAM.

C_F will set the FIFO empty flag and reset IRQ. The sensor matrix mode RAM pointer will then be set to row 0.

C_A is equivalent to C_F and C_D. The display is cleared using the display clear code specified and resets the internal timing logic to synchronize it.

End Interrupt/Error Mode Set

1	1	1	E	X	X	X	X

In the sensor matrix mode, this instruction clears IRQ and allows writing into RAM.

In N key rollover, setting the E bit to 1 allows for operating in the special Error mode. See Description of FIFO status.

FIFO Status

D_U	S/E	O	U	F	N	N	N

Where: D_U = Display Unavailable because a clear display or clear all command is in progress.
S/E = Sensor Error flag due to multiple closure of switch matrix.
O = FIFO Overrun since an attempt was made to push too many characters into the FIFO.
U = FIFO Underrun. An indication that the processor tried to read an empty FIFO.
F = FIFO Full Flag.
NNN = The Number of characters presently in the FIFO.

The FIFO Status is Read with A_0 high and $\overline{CS}$, $\overline{RD}$ active low.

The Display not available is an indication that the C_D or C_A command has not completed its clearing. The S/E flags are used to show an error in multiple closures has occurred. The O or U, overrun or underrun, flags occur when too many characters are written into the FIFO or the processor tries to read an empty FIFO. F is an indication that the FIFO is full and NNN is the number of characters in the FIFO.

Data Read

Data can be read during A_0 = 0 and when $\overline{CS}$, $\overline{RD}$ are active low. The source of the data is determined by the Read Display or Read FIFO commands.

Data Write

Data is written to the chip when A_0, $\overline{CS}$, and $\overline{WR}$ are active low. Data will be written into the display RAM with its address selected by the latest Read or Write Display command.

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COMMAND OPERATION (CONT.)

Data Format

CNTL	SH	SCAN	RET

In the Scanned Key mode, the characters in the FIFO correspond to the above format where CNTL and SH are the most significant bits and the SCAN and return lines are the scan and column counters.

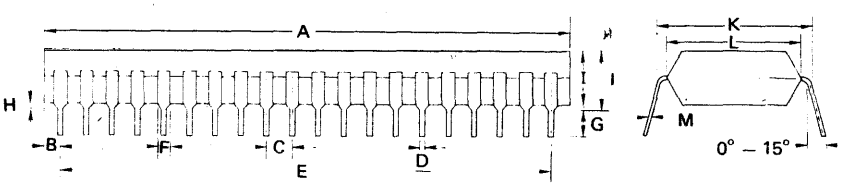
RL_7	RL_6	RL_5	RL_4	RL_3	RL_2	RL_1	RL_0

In the Sensor Matrix mode, the data corresponds directly to the row of the sensor RAM being scanned. Shift and control (SH, CNTL) are not used in this mode.

Control Address Summary

A_0	MSB			DATA				LSB	
1	0	0	0	D	D	K	K	K	Keyboard Display Mode Set
1	0	0	1	P	P	P	P	P	Load Program Clock
0	0	1	0	A_1	X	A	A	A	Read FIFO/Sensor RAM
0	0	1	1	A_1	A	A	A	A	Read Display RAM
1	1	0	0	A_1	A	A	A	A	Write Display RAM
1	1	0	1	X	IWA	IWB	BLA	BLB	Display Write Inhibit/Blanking
1	1	1	0	C_D	C_D	C_D	C_F	C_A	Clear
1	1	1	1	E	X	X	X	X	End Interrupt/Error Mode Set
1	D_U	S/E	0	U	F	N	N	N	FIFO Status

PACKAGE OUTLINE μPD8279C-5



(Plastic)

ITEM	MILLIMETERS	INCHES
A	51.5 MAX	2.028 MAX
B	1.62	0.064
C	2.54 ± 0.1	0.10 ± 0.004
D	0.5 ± 0.1	0.019 ± 0.004
E	48.26	1.9
F	1.2 MIN	0.047 MIN
G	2.54 MIN	0.10 MIN
H	0.5 MIN	0.019 MIN
I	5.22 MAX	0.206 MAX
J	5.72 MAX	0.225 MAX
K	15.24	0.600
L	13.2	0.520
M	$0.25^{+0.1}_{-0.05}$	$0.010^{+0.004}_{-0.002}$

SP8279-9-78-GN-CAT

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NEC
μPD8355
μPD8755A*

16,384 BIT ROM WITH I/O PORTS
16,384 BIT EPROM WITH I/O PORTS*

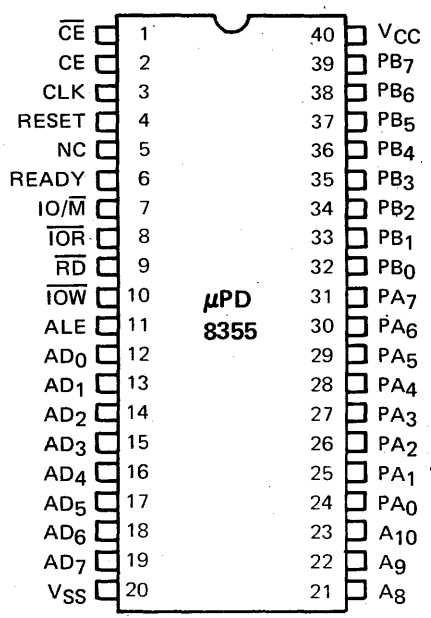
DESCRIPTION

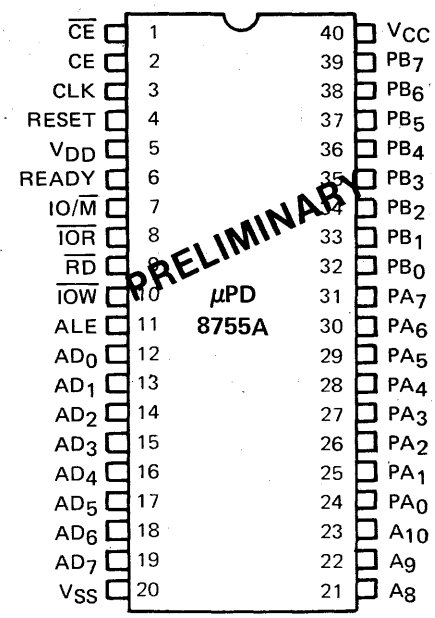
The μPD8355 and the μPD8755A are μPD8085A Family components with the μPD8355 containing 2048 X 8 bits of mask ROM and the μPD8755A containing 2048 X 8 bits of mask EPROM for program development. Both components also contain two general purpose 8-bit I/O ports. They are housed in 40 pin packages, are designed to directly interface to the μPD8085A and are pin for pin compatible to each other.

FEATURES

- 2048 X 8 Bits Mask ROM (μPD8355)
- 2048 X 8 Bits Mask EPROM (μPD8755A)
- 2 Programmable I/O Ports
- Single Power Supplies: +5V
- Directly Interfaces to the μPD8085A
- Pin for Pin Compatible
- μPD8755A: UV Eraseable and Electrically Programmable
- μPD8355 available in Plastic Package
- μPD8755A Available in Ceramic Package

PIN CONFIGURATIONS





NC: Not Connected

*All data pertaining to the μPD8755A is preliminary.

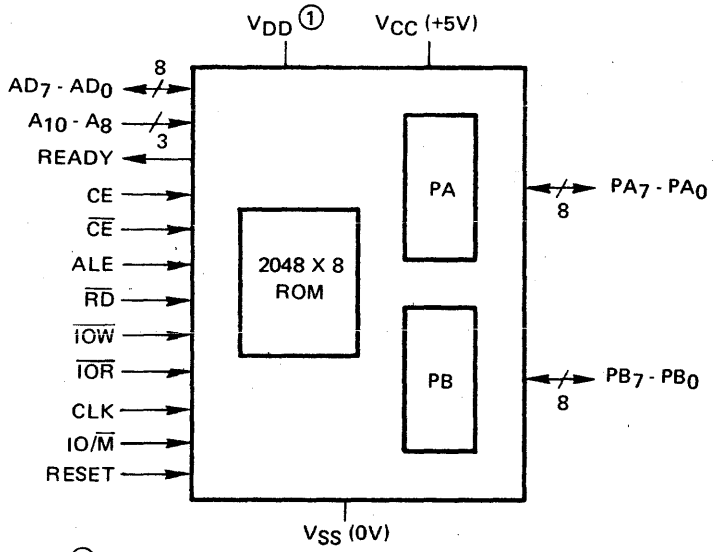
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FUNCTIONAL DESCRIPTION

The μPD8355 and μPD8755A contain 16,384 bits of mask ROM and EPROM respectively, organized as 2048 X 8. The 2048 word memory location may be selected anywhere within the 64K memory space by using the upper 5-bits of address from the μPD8085A as a chip select.

The two general purpose I/O ports may be programmed input or output at any time. Upon power up, they will be reset to the input mode.

BLOCK DIAGRAM



Note: ① V_{DD} applies to μPD8755A only.

ABSOLUTE MAXIMUM RATINGS*

Operating Temperature (μPD8355)	0°C to +70°C
(μPD8755A)	-10°C to +70°C
Storage Temperature (Ceramic Package)	-65°C to +150°C
(Plastic Package)	-40°C to +125°C
Voltage on Any Pin (μPD8355)	-0.3 to +7 Volts ①
(μPD8755A)	-0.5 to +7 Volts ①
Power Dissipation	1.5W

Note: ① With Respect to Ground

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

DC CHARACTERISTICS

T_a = 0°C to +70°C; V_{CC} = 5V ± 5%

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Input Low Voltage	V_{IL}	-0.5		0.8	V	V_{CC} = 5.0V ①
Input High Voltage	V_{IH}	2.0		V_{CC}+0.5	V	V_{CC} = 5.0V ①
Output Low Voltage	V_{OL}			0.45	V	I_{OL} = 2 mA
Output High Voltage	V_{OH}	2.4			V	I_{OH} = -400 μA
Input Leakage	I_{IL}			10	μA	V_{IN} = V_{CC} to 0V
Output Leakage Current	I_{LO}			±10	μA	0.45V ≤ V_{OUT} ≤ V_{CC}
V_{CC} Supply Current	I_{CC}			180	mA	

Note: ① These conditions apply to μPD8355 only.

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PIN IDENTIFICATION

PIN			FUNCTION
NO.	SYMBOL	NAME	
1,2	$\overline{CE}$, CE	Chip Enables	Enable Chip activity for memory or I/O
3	CLK	Clock Input	Used to Synchronize Ready
4	Reset	Reset Input	Resets PA and PB to all inputs
5 ①	NC	Not Connected	
5 ②	V_{DD}	Programming Voltage	Used as a programming voltage, tied to +5V normally
6	Ready	Ready Output	A tri-state output which is active during data direction register loading
7	IO/$\overline{M}$	I/O or Memory Indicator	An input signal which is used to indicate I/O or memory activity
8	IOR	I/O Read	I/O Read Strobe In
9	$\overline{RD}$	Memory Read	Memory Read Strobe In
10	$\overline{IOW}$	I/O Write	I/O Write Strobe In
11	ALE	Address Low Enable	Indicates information on Address/Data lines is valid
12-19	AD_0-AD_7	Low Address/Data Bus	Multiplexed Low Address and Data Bus
20	V_{SS}	Ground	Ground Reference
21-23	A_8-A_{10}	High Address	High Address inputs for ROM reading
24-31	PA_0-PA_7	Port A	General Purpose I/O Port
32-39	PB_0-PB_7	Port B	General Purpose I/O Port
40	V_{CC}	5V Input	Power Supply

Notes: ① μPD8355
② μPD8755A

I/O PORTS

I/O Port activity is controlled by performing I/O reads and writes to selected I/O port numbers. Any activity to and from the μPD8355 requires the chip enables to be active. This can be accomplished with no external decoding for multiple devices by utilizing the upper address lines for chip selects. ① Port activity is controlled by the following I/O addresses:

AD_1	AD_0	PORT SELECTED	FUNCTION
0	0	A	Read or Write PA
0	1	B	Read or Write PB
1	0	A	Write PA Data Direction
1	1	B	Write PB Data Direction

Since the data direction registers for PA and PB are each 8-bits, any pin on PA or PB may be programmed as input or output (0 = in, 1 = out).

Note: ① During ALE time the data/address lines are duplicated on A_{15}-A_8.

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AC CHARACTERISTICS

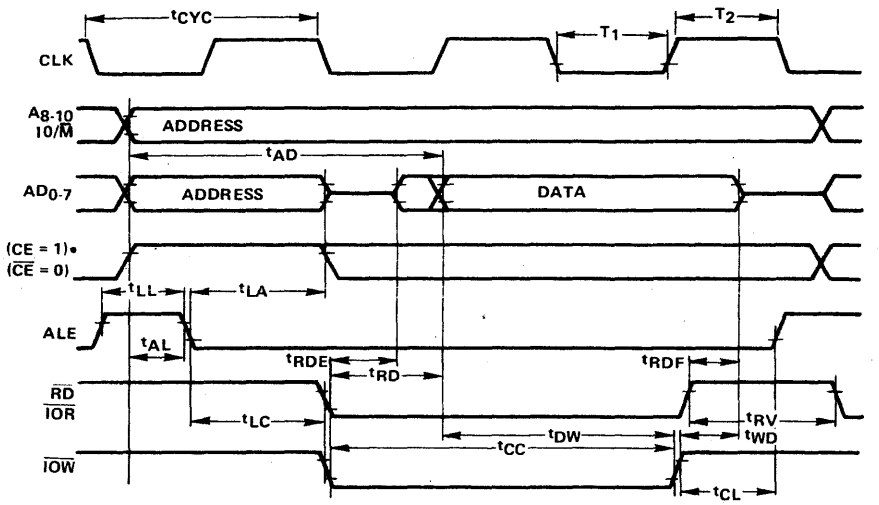
T_a = 0°C to +70°C; V_{CC} = 5V ± 5%

PARAMETER	SYMBOL	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNIT	TEST CONDITIONS
Clock Cycle Time	t_{CYC}	320			ns	
CLK Pulse Width	T_1	80			ns	C_{LOAD} = 150 pF
CLK Pulse Width	T_2	120			ns	
CLK Rise and Fall Time	t_f, t_r			30	ns	
Address to Latch Set Up Time	t_{AL}	50			ns	
Address Hold Time After Latch	t_{LA}	80			ns	
Latch to READ/WRITE Control	t_{LC}	100			ns	
Valid Data Out Delay from READ Control	t_{RD}			170 ① / 150 ②	ns	
Address Stable to Data Out Valid	t_{AD}			400	ns	150 pF Load
Latch Enable Width	t_{LL}	100			ns	
Data Bus Float After READ	t_{RDF}	0		100	ns	
READ/WRITE Control to Latch Enable	t_{CL}	20			ns	
READ/WRITE Control Width	t_{CC}	250			ns	
Data In to WRITE Set Up Time	t_{DW}	150			ns	
Data In Hold Time After WRITE	t_{WD}	10			ns	
WRITE to Port Output	t_{WP}			400	ns	
Port Input Set Up Time	t_{PR}	50			ns	
Port Input Hold Time	t_{RP}	50			ns	
READY HOLD TIME	t_{RYH}	0		160 ① / 120 ②	ns	
ADDRESS (CE) to READY	t_{ARY}			160	ns	
Recovery Time Between Controls	t_{RV}	300			ns	
Data Out Delay from READ Control	t_{RDE}	10			ns	

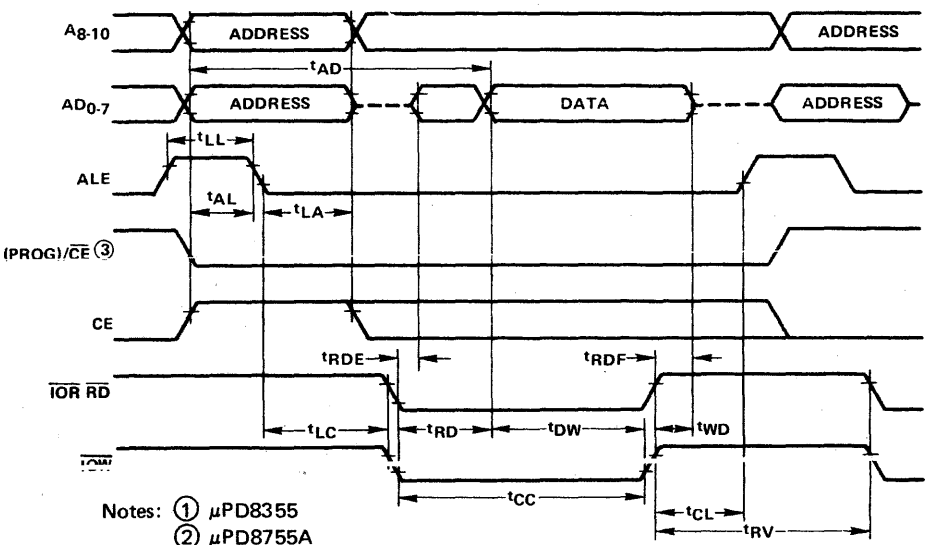
Notes: ① μPD8355
② μPD8755A

TIMING WAVEFORMS

ROM READ, I/O READ AND WRITE ①



PROM READ, I/O READ AND WRITE ②

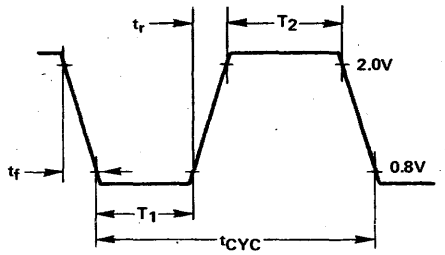


Notes: ① μPD8355
② μPD8755A
③ CE must remain low for the entire cycle

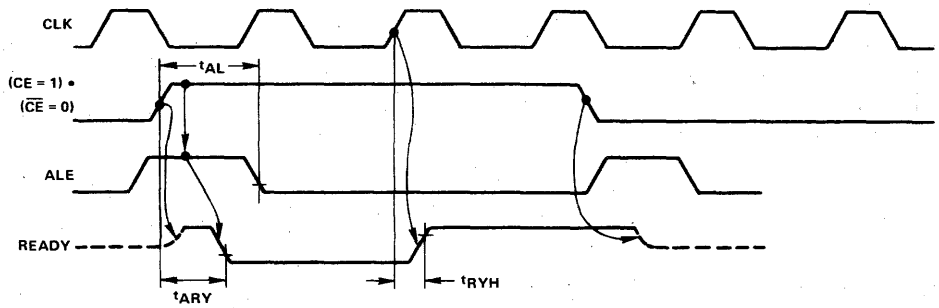
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TIMING WAVEFORMS (CONT.)

CLOCK

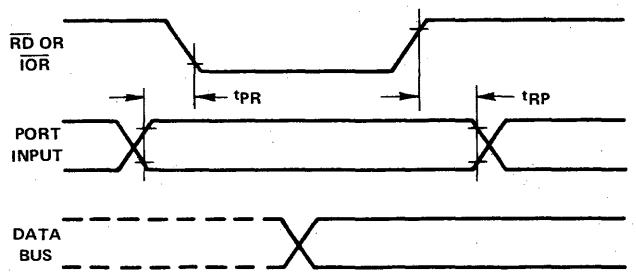


WAIT STATE TIMING (READY = 0)

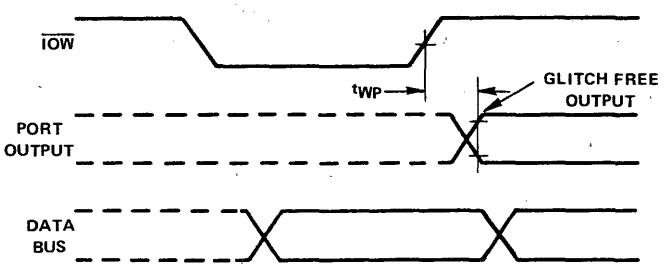


I/O PORT

INPUT MODE:



OUTPUT MODE:

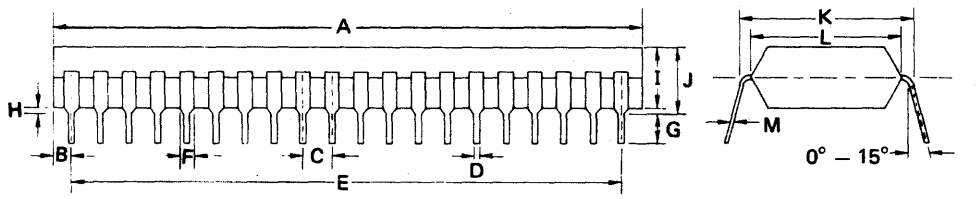


EPROM PROGRAMMING μPD8755A

Erasure of the μPD8755A occurs when exposed to ultraviolet light sources of wavelengths less than 4000 Å. It is recommended, if the device is exposed to room fluorescent lighting or direct sunlight, that opaque labels be placed over the window to prevent exposure. To erase, expose the device to ultraviolet light at 2537 Å at a minimum of 15 W-sec/cm^2 (intensity X expose time). After erasure, all bits are in the logic 1 state. Logic 0's must be selectively programmed into the desired locations. It is recommended that NEC's prom programmer be used for this application.

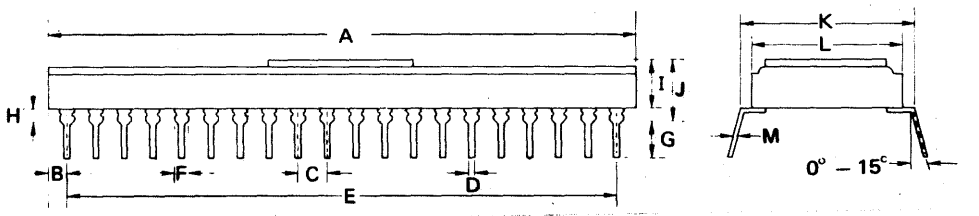
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PACKAGE OUTLINE
μPD8355C
μPD8755AD



Plastic

ITEM	MILLIMETERS	INCHES
A	51.5 MAX	2.028 MAX
B	1.62	0.064
C	2.54 ± 0.1	0.10 ± 0.004
D	0.5 ± 0.1	0.019 ± 0.004
E	48.26	1.9
F	1.2 MIN	0.047 MIN
G	2.54 MIN	0.10 MIN
H	0.5 MIN	0.019 MIN
I	5.22 MAX	0.206 MAX
J	5.72 MAX	0.225 MAX
K	15.24	0.600
L	13.2	0.520
M	$0.25^{+0.1}_{-0.05}$	$0.010^{+0.004}_{-0.002}$

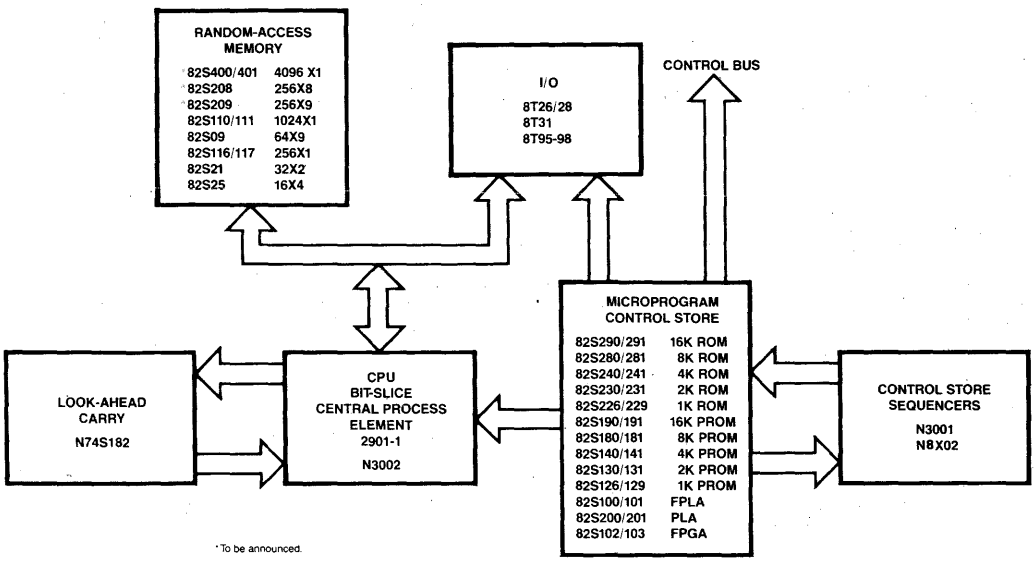


Ceramic

ITEM	MILLIMETERS	INCHES
A	51.5 MAX	2.028 MAX
B	1.62	0.064
C	2.54 ± 0.1	0.100 ± 0.004
D	0.50 ± 0.1	0.0197 ± 0.004
E	48.26 ± 0.2	1.900 ± 0.008
F	1.27	0.050
G	3.2 MIN	0.126 MIN
H	1.0 MIN	0.04 MIN
I	4.2 MAX	0.17 MAX
J	5.2 MAX	0.205 MAX
K	15.24 ± 0.1	0.6 ± 0.004
L	$13.5^{+0.2}_{-0.25}$	$0.531^{+0.008}_{-0.010}$
M	0.30 ± 0.1	0.012 ± 0.004

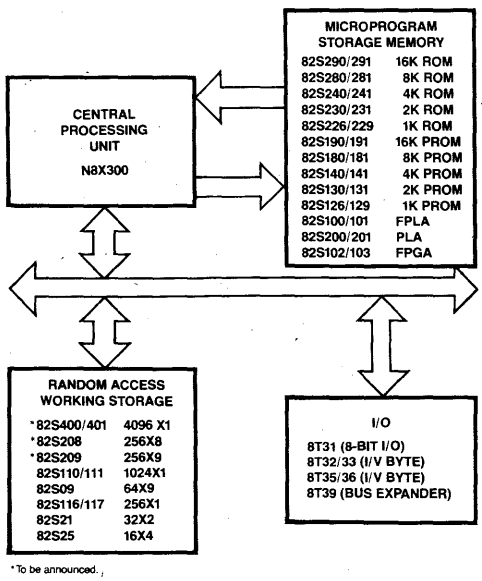
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BIT-SLICE BIPOLAR MICROPROCESSOR



Bit slice microprocessors are most often used for design of Mini and Micro CPU s where a significant amount of arithmetic processing capability is desired or where highly parallel data processing is desired, such as signal processing.

FIXED-INSTRUCTION BIPOLAR MICROPROCESSOR



Fixed instruction processors, designed for specific problem solving, are most cost effective in this use. For example, Signetics 8X300 is specifically designed to efficiently implement high speed control oriented operations. For these applications, such as double density floppy disc controllers, CRT controllers, data communications controllers, and industrial controllers, the 8X300 is more cost effective than bit slice and, in some cases, MOS controllers.

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BIT SLICE MICROPROCESSORS

Bit slice components are generally used as building blocks for the central processing unit (CPU). Bit slices are used when high speed arithmetic processing is a prime requirement.

PART #	PACKAGE	PINS	DESCRIPTION
2901-1	Ceramic, I	40	4-Bit Bipolar Microslice Control Processing Element
3002	Ceramic, I Plastic, N	28	2-Bit Bipolar Microslice Control Processing Element

CONTROL STORE MICROSEQUENCERS

Control store microsequencers are used to decide the order of command execution for a bit slice microprocessor. Also they can be used as stand-alone "single" sequencers for control functions requiring rapid decision making.

PART	PACKAGE	PINS	DESCRIPTION
8X02	Ceramic, I Plastic, N	28	10-Bit Address Control Store Microsequencer
3001	Ceramic, I	40	9-Bit Microprogram Control Unit

8X300 FIXED INSTRUCTION MICROCONTROLLER

The 8X300 control oriented instruction set provides very high performance for moving and interpreting data. This coupled with it's 250ns cycle time makes the 8X300 ideal for switching, controlling, and editing; in fact, any application in which a fast microprocessor is needed in the data path.

PART	PACKAGE	PINS	DESCRIPTION
8X300	Ceramic, I	50	8-Bit Fixed Instruction Microprocessor

INTERFACE VECTOR (IV) BYTES

An IV byte is a latched bi-directional 8-bit I/O port with a programmable address.

PART	PACKAGE	PINS	DESCRIPTION
8T32	Plastic, N Ceramic, F	24	Synchronous 3-State
8T33	Plastic, N Ceramic, F	24	Synchronous open collector
8T35	Plastic, N Ceramic, F	24	Asynchronous 3-State
8T36	Plastic, N Ceramic, F	24	Asynchronous open collector

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DESCRIPTION

The Signetics Micro Assembler is a complete software package used to design and program with Signetics bipolar bit-slice microprocessors. It contains advanced features to ease microprogramming and documentation.

The Micro Assembly language can be tailored to the configuration of the microprogram. It is designed especially for the Signetics bipolar microprocessors such as the 8X02 microprogram control sequencer, the 2900 microporcessor family, and the 3000 series. This flexibility enables it to handle virtually all microprogramming applications and microprocessor circuits.

The Micro Assembler consists of two interrelated programs. (See Figure 1)

The *Micro Assembly Program* reads the program system configurations and format descriptions to produce a listing of the source program and the resulting machine (binary) language. This listing contains source program error diagnostics and a cross-reference of microprogramming symbols.

The *Micro Format Program* translates the object program for direct use in programming PROMs. It reads the object program produced by the Micro Assembly Program and divides the object program into bits to be written into PROM modules, with separate output for each PROM.

FEATURES

- **High-level syntax—easy to use**
- **Cross reference listing**
- **Number of bits: Up to 4095 bits wide (default = 128)**
- **Number of instructions: Up to 65K words**
- **Mnemonic names and size of each control field**
- **Mnemonic names for control field values**
- **Organization of Micro Control Store as physical prom modules**
- **Formatting of object module for output**
- **Free-form input: Multiple statements per line**
- **Detection of overlapping fields for extensive error checking**
- **Multiple microinstruction formats: Variable microinstruction widths**
  - **Definition of sub-fields**
  - **Definition of more than one microinstruction thru multiple microinstruction Def. Sections**
- **Logical and relational expression operators**
- **Generation of non-microinstruction Proms (Look-up tables, mask generation, field expansion)**
- **Microp defaults under user definition**
- **Microp arguments**
- **Conditional (IF, THEN, ELSE) clause for field assignment and reference of microps**
- **Constants—Numeric and ASCII characters**
- **Nested microps**
- **Shift operators**

MICRO ASSEMBLY LANGUAGE

The Micro Assembly Language input into the assembler is divided into two sections:

The *definition* section defines instruction formats and device configurations of the user system. The name and length of each field is specified and symbolic opcodes are defined. Microinstructions may be any length, and multiple formats may be defined.

The *microprogram* section is the sequence of symbolic microinstructions that make up the operational program.

The Micro Assembly language also contains standard assembler directives and arithmetic, binary shift and logical operators.

Values used with the language may be decimal, hexadecimal, octal binary or ASCII character constants or symbolic values.

PROM FORMATTING

The format command file of the Micro Format Program translates the object program for PROM programming. Each bit of microinstruction, complemented or uncomplemented is identified with a PROM. The Microprogram addressing space may also be divided into bits and stored in PROM. There are provisions for inverted addresses. In a typical application, for example, microprogram may be distributed among ten 512x8 PROMs.

Among the output formats are: SMS, various BNPF formats, and 2650 absolute object code.

A full description is contained in the Signetics Micro Assembler Reference Manual.

AVAILABILITY

The Micro Assembler is written in ANSI FORTRAN IV. The source form is available on magnetic tape from Signetics in two formats:

- EBCDIC 9-track magnetic tape, unblocked 80-character records, 800 bpi density. Order part number 8X00MA1000SS.
- ASCII 9-track magnetic tape, unblocked 80-character records, 1600 bpi density. Order part number 8X00MA2000SS.

The Micro Assembler is also available on the more popular timesharing services.

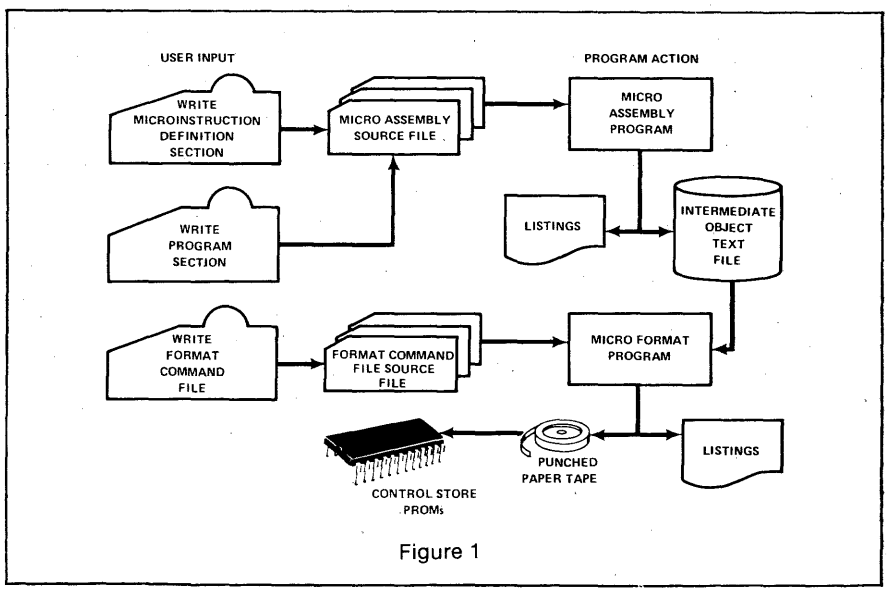


Figure 1

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DESCRIPTION

The 8X300 Assembler is a program which accepts source code written in the 8X300 assembly language and which produces both a listing of the symbolic program and an object module in one of four formats: MCSIM, ROM simulator, BPNF, or hexadecimal.

The assembler program is written in ANSI standard FORTRAN and is approximately 3000 card images in length. It requires some rewindable I/O medium such as disk or tape for temporary storage, an input device to read source code, and two output devices, one to output the assembler listing and one to output the object module. If desired, the assembler may be compiled and linked to execute in overlays.

The assembler consists of two passes which build a symbol table, issue helpful error messages, produce an easily readable program listing, and output a computer readable object module.

FEATURES

- **Macro nested to three levels**
- **Conditional assembly**
- **Address arithmetic**
- **Automatic procedure/subroutine handling**
- **Reserved symbols for registers**
- **Multiple entry to procedures**
- **Symbolic machine operation codes**
- **Symbolic assignment address references**
- **Symbolic data creation statements (I/O port reference)**
- **Free format source code**
- **Syntax error checking**
- **Self-defining constants**
- **Assembly listing control statements**
- **ASCII character code**
- **Comment statements and comment areas**
- **Forward referencing**
- **Cross-reference of the symbol table**
- **Instructions up to 32-bits wide**
- **Versatile object file format specification**

MCCAP LANGUAGE

The assembler recognizes three types of statements: Comment statements, machine instructions, and pseudo-ops (directives).

Comment statements are used to document a listing. They must contain an asterisk in column 1 and may contain any legal character in the other 79 columns.

Machine instruction statements are those statements that generate instruction(s) to be executed by the 8X300 processor. Machine instruction statements include:

MOVE	Move byte from one location to another.
ADD	Add the byte in one location to the byte in the auxiliary register and store the result in another location
AND	AND the byte in one location with the byte in the auxiliary register and store the result in another location.
XOR	Exclusive OR the byte in one location with the byte in the auxiliary register and store the result in another location.
XEC	Execute the instruction at the specified address.
XMIT	Transmit the literal (immediate data) contained in this instruction to the specified location.
NZT	Jump to the specified address if the value in the specified location is not zero.
JMP	Jump to the specified address.
CALL	Transfer control to a procedure or an entry point.
RTN	Returns control from a procedure or an entry point.
SEL	Places the address of an IV Byte variable into the IVL or the IVR register.
HALT	Halts by jump to current address.
NOP	Generates a no-op.

Pseudo-Ops (or Directives) are commands to the assembler, but have no meaning to the 8X300 processor.

EQU	Assigns a value to the symbol in the label field.
SET	Identical to EQU, except that the symbol may be redefined by another SET statement.
LIV	Assigns a symbolic name to the address, position and precision of the "left bank" Interface Vector Byte variable.
RIV	Identical to LIV, except that the assignment is made to the "right bank" I/O Field.
PROG	Introduces and names the main program.
PROC	Introduces and names a procedure.
ENTRY	Specifies an additional entry point to a procedure.
END	Terminates a procedure, a program or a MACRO.
ORG	Changes the value of the location counter.
OBJ	Specifies the format of the object module.
IF	Introduces source statements subject to conditional assembly.
ENDIF	Terminates the source statements subject to conditional assembly.



LIST	Specifies the list and punch options.
NLIST	Negates the list and punch options.
EJCT	Advances listing to next page.
SPAC	Advances listing to next line.
MACRO	Defines the source statements generated a macro call.
PROM	Specifies the size of the object module.
DEF	Defines extended instruction fields.

The assembler produces object code for the 8X300 and for extended instructions. Extended instructions are bit patterns that are selected at the same time as the standard 8X300 instructions and are used for hardware selection of I/O ports or working storage, thereby reducing program length and increasing throughput.

A full description of MCCAP is contained in the Signetics Microcontroller Cross-Assembly Program Manual.

AVAILABILITY

The assembler is available on the more popular timesharing services. It is also available from Signetics on 9-track magnetic tape in the following formats.

- EBCDIC unblocked 80-character records, 800 bpi density. Order part number 8X300AS100SS.
- ASCII blocked 80-character records, 1600 bpi density. Order part number 8X300AS200SS.

Signetics

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N2901A

DESCRIPTION

The 4-bit bipolar microprocessor slice is designed as a high-speed cascadable element intended for use in CPUs, peripheral controllers, programmable microprocessors and numerous other applications. The microinstruction flexibility of the 2901A will allow efficient emulation of almost any digital computing machine.

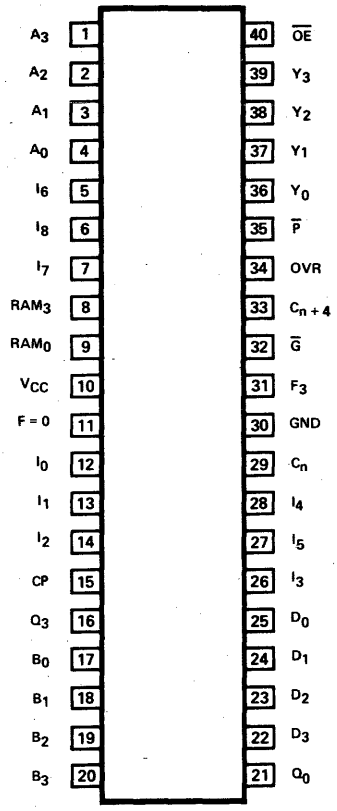
The device, as shown in the block diagram below, consists of a 16-word by 4-bit 2-port RAM, a high-speed ALU, and the associated shifting, decoding and multiplexing circuitry. The 9-bit microinstruction word is organized into 3 groups of 3 bits each and selects the ALU source operands, the ALU function, and the ALU destination register. The microprocessor is cascadable with full look-ahead or with ripple carry, has three-state outputs, and provides various status flag outputs from the ALU. Advanced low-power Schottky processing is used to fabricate this 40-lead LSI chip.

FEATURES

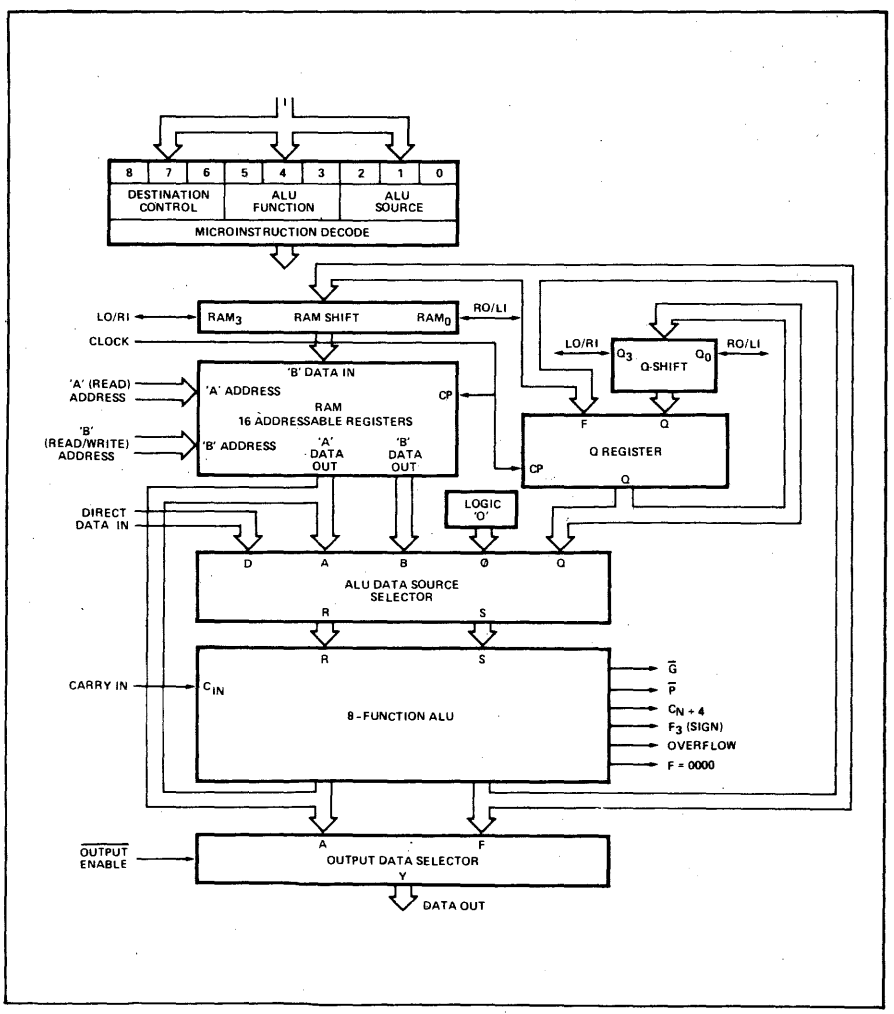
- **80ns cycle time**
- **2-address architecture**
  Independent simultaneous access to 2 working registers saves machine cycles
- **8-function ALU**
  Performs addition, 2 subtraction operations, and 5 logic functions on 2 source operands
- **Flexible data source selection**
  ALU data is selected from 5 source ports for a total of 203 source operand pairs for every ALU function
- **Left/right shift independent of ALU**
  Add and shift operations take only 1 cycle
- **4 status flags**
  Carry, overflow, zero, and negative
- **Expandable**
  Connect any number of 2901A's together for longer word lengths.
- **Microprogrammable**
  3 groups of 3 bits each for source operand, ALU function, and destination control

PIN CONFIGURATION

IW PACKAGE



BLOCK DIAGRAM



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8X02-I,XL

DESCRIPTION

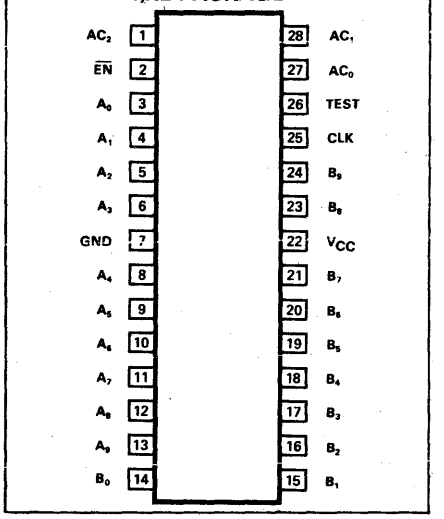
The Signetics 8X02 is a low power Schottky LSI device intended for use in high performance microprogrammed systems to control the fetch sequence of microinstructions. When combined with standard ROM or PROM, the 8X02 forms a powerful microprogrammed control section for computers, controllers, or sequential logic.

FEATURES

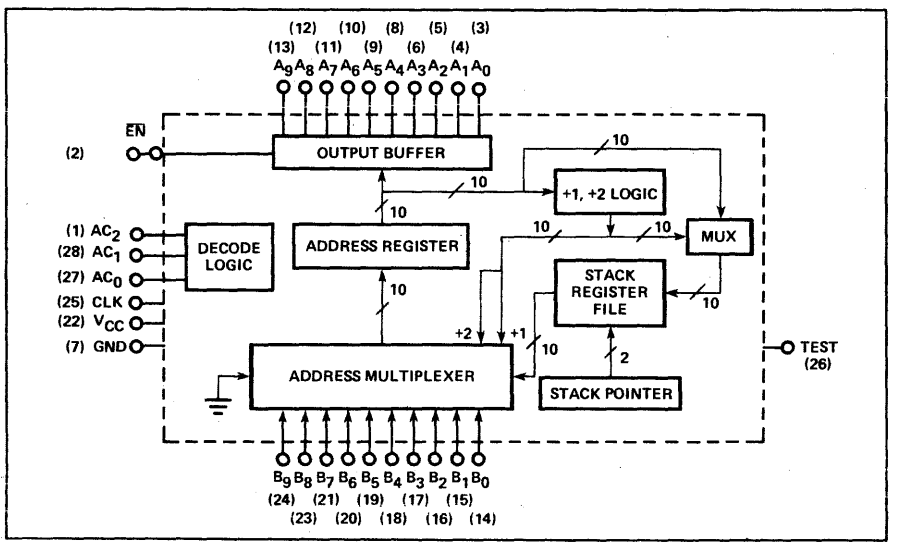
- **Low power Schottky process**
- **1024 microinstruction addressability**
- **N-way branch**
- **4-level stack register file (LIFO type)**
- **Automatic push/pop stack operation**
- **"Test and skip" operation on test input line**
- **3-bit command code**
- **Tri-state buffered outputs**
- **Auto-reset to address 0 during power-up**
- **Conditional branching, pop stack, and push stack**

PIN CONFIGURATION

I,XL PACKAGE



BLOCK DIAGRAM



PIN DESIGNATION

PIN	SYMBOL	NAME AND FUNCTION	TYPE
3-6 8-13	A_0-A_9	Microprogram Address outputs	Three-state Active high
27, 28, 1	AC_0-AC_2	Next Address Control Function inputs All addressing control functions are selected by these command lines.	Active high
14-21 23-24	B_0-B_9	Branch Address inputs Determines the next address of an N-way branch when used with the BRANCH TO SUBROUTINE (BSR) or BRANCH ON TEST (BRT) command.	Active high
2	$\overline{EN}$	Enable input When in the low state, the Microprogram Address outputs are enabled.	Active low
25	CLK	Clock Input—High to Low transition for stack operations, Low to High transition for address modification.	⊓
26	TEST	Test input Used in conjunction with four NEXT ADDRESS CONTROL FUNCTION commands to effect conditional skips, branches, and stack operations.	Active high
7	GND	Ground	
22	V_{CC}	+5 Volt supply	

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FUNCTIONAL DESCRIPTION

The Signetics 8X02 Control Store Sequencer is an LSI device using low power Schottky technology and is intended for use in high performance microprogrammed applications. When used alone, the 8X02 is capable of addressing up to 1K words of microprogram. This may be expanded to any microprogram size by conventional paging techniques.

The Address Register consists of 10 D-type, edge-triggered flip-flops with a common clock. A new address is entered into the Address Register on the low-to-high transition of the clock. The next address to be entered into the Address Register is supplied via the Address Multiplexer.

The Address Multiplexer is a 5-input device that is used to select either the branch input, +1 adder, +2 adder, stack register file, or ground (all zeros) as the source of the next microinstruction address. The proper multiplexer channel is automatically selected via the Decode Logic according to the Address Control Function Input and Test Input line.

The +1, +2 logic is used to increment the present contents of the Address Register by 1 or 2, depending on the function input command. Thus, the next address to the Control Store ROM/PROM may be either the current address plus 1 (N+1) or the current address plus 2 (N+2). If the same Microprogram Address is to be used on successive occasions, the clock to the 8X02 must simply be disabled; therefore, no new address is loaded into the Address Register.

The Stack File Register is used to provide a return address linkage whenever a subroutine or loop is executed. The 4X10 stack operates in a last-in, first-out (LIFO) mode, with the stack pointer always pointing to the next address to be read. Operation of the stack pointer is automatically controlled by the Address Control Function Inputs. Since the stack is 4 words deep, up to 4 loops and/or subroutines may be nested.

The stack pointer operates as an up/down counter. The stack pointer is incremented by one during the PUSH operation. The new data is written into the new location pointed to by the stack pointer. A POP operation will read data from the location pointed to by the stack pointer in the previous cycle, and the stack pointer will be decremented by one at the end of the current cycle. When the stack pointer is pointing at the first level of the stack, a POP operation will cause the stack pointer to wrap around to the fourth level of the stack. Similarly, a PUSH operation will cause the stack pointer, when pointing at the fourth level of the stack to wrap around to the first level of the stack.

The branch input is a 10-bit field of direct inputs to the multiplexer which can be selected as the next control store address. Using the appropriate branch command, an N-way branch is possible where N is the address of any microinstruction within the 1024 word microcode page. Likewise, the RESET command is a special case of an N-way branch in which the multiplexer selects an all zeros input, forcing the next microinstruction address to be zero.

The Test Input line is used in conjunction with the conditional execution of 4 Address Control Function commands. When the Test Input is false (low), the sequencer simply increments to the next address (N+1). When it is true (high), the sequencer executes a branch as defined by the input command, thereby transferring control to another portion of the microprogram.

All Address Output lines of the 8X02 are three-state buffered outputs with a common enable line ($\overline{EN}$). When the Enable line is high, all outputs are placed in a high-impedance state, and external access to the control store ROM/PROM is possible. This allows a preprogrammed set of microinstructions to be executed from external or built-in test equipment (BITE), vectored interrupts, and Writable Control Store if implemented.

NEXT ADDRESS CONTROL FUNCTION TABLE

MNEMONIC	DESCRIPTION	FUNCTION AC_2 1 0	TEST	NEXT ADDRESS	STACK	STACK POINTER
TSK	Test and skip	0 0 0	False	Current + 1	N.C.	N.C.
			True	Current + 2	N.C.	N.C.
INC	Increment	0 0 1	X	Current + 1	N.C.	N.C.
BLT	Branch to loop if test input true	0 1 0	False	Current + 1	X	Decr
			True	Stack reg file	POP (read)	Decr
POP	POP stack	0 1 1	X	Stack reg file	POP (read)	Decr
BSR	Branch to subroutine if test input true	1 0 0	False	Current + 1	N.C.	N.C.
			True	Branch address	PUSH (Curr + 1)	Incr
PLP	Push for looping	1 0 1	X	Current + 1	PUSH (Curr Addr)	Incr
BRT	Branch if test input true	1 1 0	False	Current + 1	N.C.	N.C.
			True	Branch address	N.C.	N.C.
RST	Set microprogram address output to zero	1 1 1	X	All O's	N.C.	N.C.

X = Don't care
N.C. = No change

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DESCRIPTION

The Signetics 8X300 Microcontroller is a monolithic, high-speed microprocessor implemented with bipolar Schottky technology. As the central processing unit, CPU, it allows 16-bit instructions to be fetched, decoded and executed in 250ns. A 250ns instruction cycle requires maximum memory access of 65ns, and maximum I/O device access of 35ns.

Microcontroller instructions operate on 8-bit, parallel data. Logic is distributed along the data path within the Microcontroller. Input data can be rotated and masked before being subject to an arithmetic or logical operation; and output data can be shifted and merged with the input data, before being output to external logic. This allows 1- to 8-bit I/O and data memory fields to be accessed and processed in a single instruction cycle.

PROGRAM STORAGE INTERFACE

Program Storage is typically connected to the A0-A12 (A12 is least significant bit) and I0-I15 signal lines. An address output on A0-A12 identifies one 16-bit instruction word in program storage. The instruction word is subsequently input on I0-I15 and defines the Microcontroller operations which are to follow.

The Signetics 82S115 PROM, or any TTL compatible memory, may be used for program storage.

I/O DEVICES INTERFACE

An 8-bit I/O bus, called the Interface Vector (IV) data bus, is used by the Microcontroller to communicate with 2 fields of I/O devices. The complementary $\overline{LB}$ and $\overline{RB}$ signals identify which field of the I/O devices is selected.

Both I/O data and I/O address information can be output on the IV bus. The SC and WC signals are typically used to distinguish between I/O data and I/O address information as follows:

SC	WC	
1	0	I/O address is being output on IV bus
0	1	I/O data is being output on IV bus
0	0	I/O data is expected on the IV, bus, as input to the Microcontroller
1	1	Not generated by the Microcontroller

The Signetics 82SXXX series RAM, and the 8T32/33 may be attached to the IV bus.

FEATURES

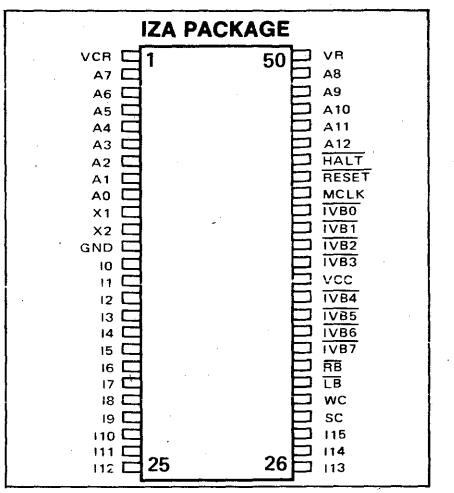
- **185ns instruction decode and execute delay (with Signetics 8T32/33 I/O port)**
- **Eight 8-bit working registers**
- **Single instruction access to 1-bit, 2-bit, 3-bit or 8-bit field on I/O bus**
- **Separate instruction address, instruction, and I/O data buses**
- **On-chip oscillator**
- **Bipolar Schottky technology**
- **TTL inputs and outputs**
- **Tri-state output on I/O data bus**
- **+5 volt operation from 0° to 70°C**

MILITARY

Also available in Military version as S8X300-1 or S8X300-2

PIN CONFIGURATION

IZA PACKAGE



PIN DESIGNATION

PIN	SYMBOL	NAME AND FUNCTION	TYPE
2-9, 45-49	A0-A12:	Instruction address lines. A high level equals "1." These outputs directly address up to 8192 words of program storage. A12 is least significant bit.	Active high
13-28	I0-I15:	Instruction lines. A high level equals "1." Receives instructions from Program Storage. I_{15} is least significant bit.	Active high
33-36, 38-41	$\overline{IVB0}$-$\overline{IVB7}$	Interface Vector (IV) Bus. A low level equals "1." Bidirectional tri-state lines to communicate with I/O devices. $\overline{IVB7}$ is least significant bit.	Three-state Active low
42	MCLK:	Master Clock. Output to clock I/O devices, and/or provide synchronization for external logic	Active high
30	WC:	Write Command. High level output indicates data is being output on the IV Bus.	Active high
29	SC:	Select Command. High level output indicates that an address is being output on the IV Bus.	Active high
31	$\overline{LB}$:	Left Bank. Low level output to enable one of two sets of I/O devices ($\overline{LB}$ is the complement of RB).	Active low
32	$\overline{RB}$:	Right Bank. Low level output to enable one of two sets of I/O devices ($\overline{RB}$ is the complement of $\overline{LB}$).	Active low
44	$\overline{HALT}$:	Low level is input to stop the Microcontroller.	Active low
43	$\overline{RESET}$:	Low level is input to initialize the Microcontroller.	Active low
10-11	X1, X2:	Inputs for an external frequency determining crystal. May also be interfaced to logic or test equipment.	
50	VR	Reference voltage to pass transistor.	
1	VCR	Regulated output voltage from pass transistor.	
37	V_{CC}:	5V power connection.	
12	GND:	Ground.	

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MICROCONTROLLER ARCHITECTURE

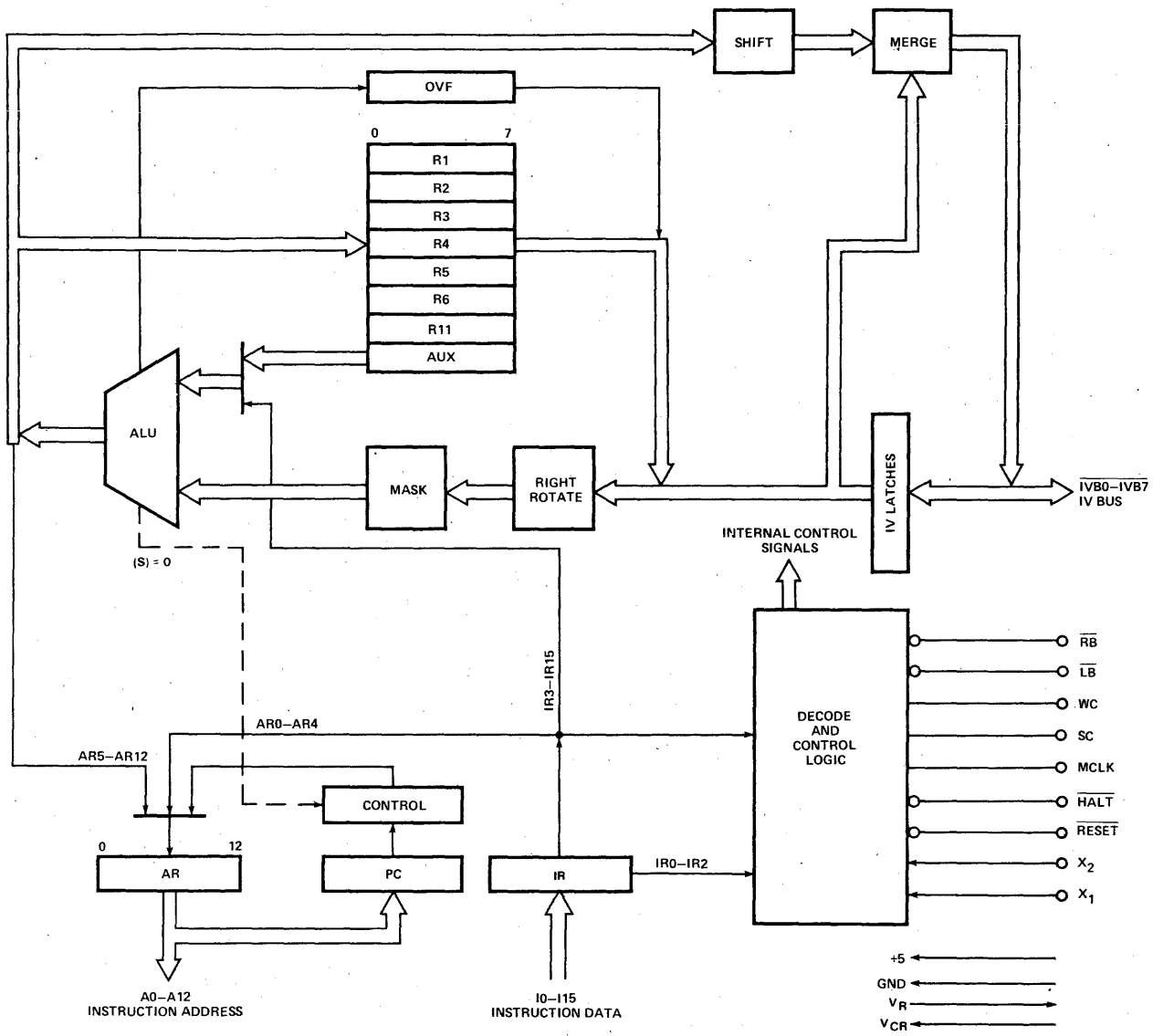


Figure 1

R1 — General working register
R2 — General working register
R3 — General working register
R4 — General working register
R5 — General working register
R6 — General working register
R11 — General working register
AUX — General working register. Contains second term for arithmetic or logical operations.

OVF — The least-significant bit of this register is used to reflect overflow status resulting from the most recent ADD operation (see Instruction Set Summary).

Instruction Register (IR)
— Holds the 16-bit instruction word currently being executed.

Program Counter (PC)
— Normally contains the address of the current instruction and is incremented to obtain the next instruction address.

Address Register (AR)
— A 13-bit register containing the address of the current instruction.

Table 1 INTERNAL REGISTERS

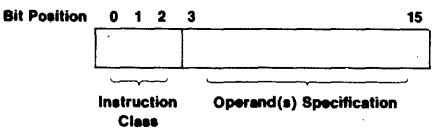
INSTRUCTION CYCLE

Each Microcontroller operation is executed in 1 instruction cycle, which may be as short as 250ns. The Microcontroller generates MCLK to synchronize external logic to the instruction cycle. Instruction cycles are subdivided into quarter cycles. MCLK is an output during the last quarter cycle.

During the third quarter cycle of an instruction, an address is output on A0-A12, identifying the location in program storage of the next instruction word. This instruction word defines the next instruction, which must be input on I0-I15 during the first quarter cycle of the next instruction cycle (see Table 2).

Instruction Set Summary

The 16-bit instruction word input on I0-I15 is decoded by the instruction decode logic to implement events that are to occur during the remainder of the instruction cycle. Generally the 16-bit instruction word is decoded as follows:



A detailed usage of the 13 "operand(s) specification" bits is given in following sections.

Three operation code bits allow for 8 instruction classes. The 8 instruction classes are summarized in Table 3. Each entry is referred to as an "instruction class" because the unique architecture of the Interpreter allows a number of powerful variations to be specified by the 13 operand(s) specification bits. A complete description of instruction formats and some instruction examples are provided in the Microprocessor Applications manual.

Data Processing

The Microcontroller architecture includes eight 8-bit working registers, an arithmetic logic unit (ALU), an overflow register, and the 8-bit IV Bus. Internal 8-bit data paths connect the registers and IV Bus to the ALU inputs, and the ALU output to the registers and IV Bus. Data processing logic is distributed along these internal 8-bit data paths. Rotate and mask logic precedes the ALU on the data entry path. Shift and merge logic follows the ALU on the data output path. All 4 sets of logic can operate on 8 data bits in a single instruction cycle (See Figure 1).

When less than 8 bits of data are specified for output to the IV bus by the ALU, the data field (shifted if necessary) is inserted into the prior contents of the IV bus latches. The IV bus latches contain data input at the start of an instruction. This data in the IV bus latches will be specified in the instruction as a) IV bus source data or b) data from an automatic read when the IV bus is specified as a destination. Therefore, IV bus bit positions outside an inserted bit field are unmodified.

Data Addressing

Sources and destinations of data are specified using a 5-bit octal number. The source and/or destination of data to be operated upon is specified in a single instruction word.

Referring to Figure 1, the Auxiliary register (address 00) is the implied source of the second argument for ADD, AND or XOR operations.

IVL and IVR are write-only registers used only as a destination. They have addresses and are treated as registers, but in reality they do not exist. When IVL is specified as a destination or the D field = $20\text{-}27_8$, then LB = 'low', RB = 'high' are generated; when IVR is specified as a destination or the D field = $30\text{-}37_8$, then RB = low, LB = 'high' are generated.

When IVL or IVR is specified as the destination in an instruction, SC is also activated and data is placed on the IV bus. If IVL or IVR is specified as a source of data, the source data is all zeroes.

TYPICAL SYSTEM CONFIGURATION

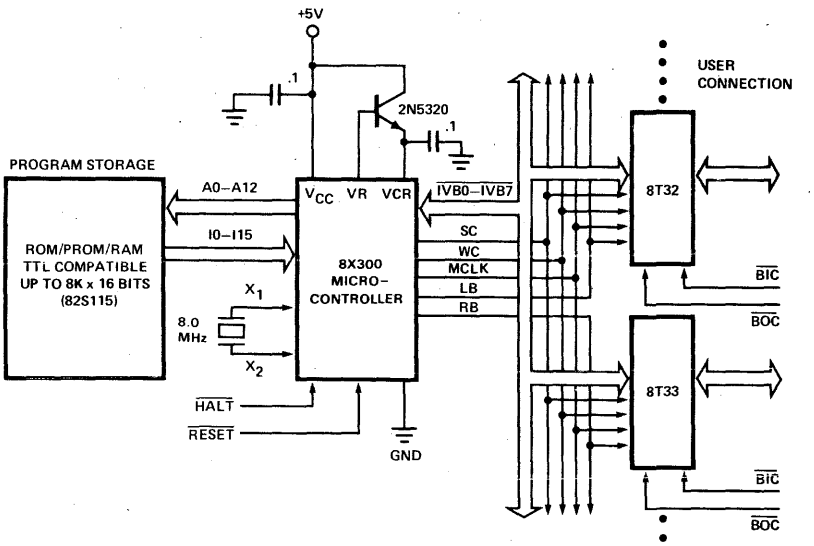


Figure 2

INSTRUCTION AND IV BUS DATA INPUT	DATA PROCESSING	ADDRESS AND IV BUS CHANGING	ADDRESS AND IV BUS DATA VALID MCLK=HIGH
← ¼ cycle →	← ¼ cycle →	← ¼ cycle →	← ¼ cycle →

Table 2 INSTRUCTION CYCLE

INSTRUCTION SEQUENCE CONTROL

The Address Register and Program Counter are used to generate addresses for accessing an instruction. The Address Register is used to form the instruction address, and in all but 3 instructions (XEC, NZT, and JMP) the address is copied into the Program Counter. The instruction address is formed in 1 of 3 ways:

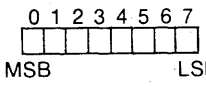
1. For all instructions but the JMP, XEC, and a satisfied NZT, the Program Counter is incremented by 1 and placed in the Address Register.
2. For the JMP instruction, the full 13-bit address field from the JMP instruction is placed into the Address Register and copied into the Program Counter.
3. For the XEC and NZT instructions, the high order 5- or 8-bits of the Program Counter are combined with 8- or 5-lower-order bits of ALU output (XEC or NZT) and placed in the Address Register. For the NZT instruction, it is also copied into the Program Counter.

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INSTRUCTION SET

The 8X300 Microcontroller has a repertoire of 8 instruction classes which allow the user to test input status lines, set or reset output control lines, and perform high speed input/output data transfers. All instructions are 16 bits in length and each is fetched, decoded and executed in 250ns.

Data is respresented as an 8-bit byte; bit positions are numbered from left to right, with the least significant bit in position 7.



Within the 8X300, all operations are performed on 8-bit bytes. Arithmetic operations use 8-bit, unsigned 2's complement arithmetic.

INSTRUCTION FORMATS

The general 8X300 instruction format is:

0 1 2	3 4 5 6 7 8 9 10 11 12 13 14 15
Op Code	Operand(s)

All instructions are specified by a 3-bit Operation (Op Code) field. The operand may consist of the following fields: Source (S) field, Destination (D) field, Rotate/Length (R/L) field, Immediate (I) field, or (Program Storage) Address (A) field.

The instructions are divided into 5 format types, based on the Op Code and the Operand(s), as shown in Figure 3.

OPERATION	FORMAT	RESULT	NOTES
MOVE	I,II	Content of data field specified by {S, R/L} replaces data in field specified by {D, R/L.}	If S and D both are registers, then R/L specifies a right rotate of the register specified by S.
ADD	I,II	Sum of AUX and data specified by {S, R/L} replaces data in field specified by {D, R/L}.	
AND	I,II	Logical AND of AUX and data specified by {S, R/L} replaces data in field specified by {D, R/L.}	
XOR	I,II	Logical exclusive OR of AUX and data specified by {S, R/L} replaces data in field specified by {D, R/L.}	
XMIT	III,IV	The literal value I replaces the data in the field specified by {S,L.}	If S is an I/O address then I is limited to range 00-37. Otherwise I is limited to range 000-377.
NZT	III,IV	If the data in the field specified by {S, L} equals zero, perform the next instruction in sequence. If the data specified by {S,L} is not equal to zero, execute the instruction at address determined by using the literal I as an offset to the Program Counter.	If S is an I/O address then I is limited to range 00-37. Otherwise I is limited to range 000-377.
XEC	III,IV	Perform the instruction at address determined by applying the sum of the literal I and the data specified by {S, L} as an offset to the Program Counter. If that instruction does not transfer control, the program sequence will continue from the XEC instruction location.	The offset operation is performed by reducing the value of PC to the nearest multiple of 32 (if I = 00-37) or 256 (if I = 000-377) and adding the offset.
JMP	V	The address value A replaces contents of the Program Counter.	A limited to the range 0-17777$_8$.

Table 3 8X300 INSTRUCTION SUMMARY

INSTRUCTION FORMATS

OPERATIONS
(REGISTER TO REGISTER)
MOVE AND
ADD XOR

0 1 2	3 4 5 6 7	8 9 10	11 12 13 14 15
OP CODE	S	R (ROTATE)	D

Type I

OPERATIONS
(REGISTER TO I/O, I/O TO REGISTER, I/O TO I/O)
MOVE ADD
AND XOR

0 1 2	3 4 5 6 7	8 9 10	11 12 13 14 15
OP CODE	S	L (LENGTH)	D

Type II

OPERATIONS

XEC XMIT*
NZT

0 1 2	3 4 5 6 7	8 9 10 11 12 13 14 15
OP CODE	S	I

Type III

OPERATIONS

XEC XMIT*
NZT

0 1 2	3 4 5 6 7	8 9 10	11 12 13 14 15
OP CODE	S	L (LENGTH)	I

Type IV

OPERATIONS

JMP

0 1 2	3 4 5 6 7 8 9 10 11 12 13 14 15
OP CODE	A

Type V

*NOTE
If XMIT, S actually represents the destination.

Figure 3

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SYSTEM DESIGN USING THE 8X300 MICROCONTROLLER

Designing hardware around the 8X300 Interpreter reduces to selecting a program storage devicer (ROM, PROM, etc.), selecting I/O devices (IV byte, multiplexers, RAM, etc.), selecting clock mode (system driven or crystal controlled) and interfacing the Microcontroller to these components.

A specific example of a control system using the 8X300 Microcontroller is shown in Figure 12. Only 8 components—four 8T32 I/O Ports, one 8X350 RAM, two 82S215 ROMs, and an 8X300 are required to build this system which contains 512 words of program storage, 32 TTL I/O connection points, 256 bytes of working storage, and operates at a 250ns instruction cycle time.

Halt, Reset Signals

$\overline{\text{HALT}}$:
A low level at the $\overline{\text{HALT}}$ input stops internal operation of the Microcontroller at the start of the next instruction after $\overline{\text{HALT}}$ is applied (quarter cycle after MCLK). Since $\overline{\text{HALT}}$ is sampled at the start of each instruction cycle it is possible to prevent a cycle by applying $\overline{\text{HALT}}$ early in that cycle. $\overline{\text{HALT}}$ does not inhibit MCLK or affect any internal registers. Normal operation begins with the next complete cycle after the $\overline{\text{HALT}}$ input goes high.

$\overline{\text{RESET}}$:
A low level at the $\overline{\text{RESET}}$ input sets the program counter and address register to zero. While $\overline{\text{RESET}}$ is low MCLK is inhibited. If $\overline{\text{RESET}}$ is applied during the last 2 quarter cycles, the MCLK during that cycle may be shortened. $\overline{\text{RESET}}$ should be applied for 1 full instruction cycle time to assure proper operation. When $\overline{\text{RESET}}$ input goes high an MCLK occurs prior to the resumption of normal processing. $\overline{\text{RESET}}$ does not affect the other internal registers.

SYSTEM TIMING

In systems with fast instruction cycle times, most Microcontroller delays are strictly determined by internal gate propagation delays.

EXAMPLE OF CONTROL SYSTEM

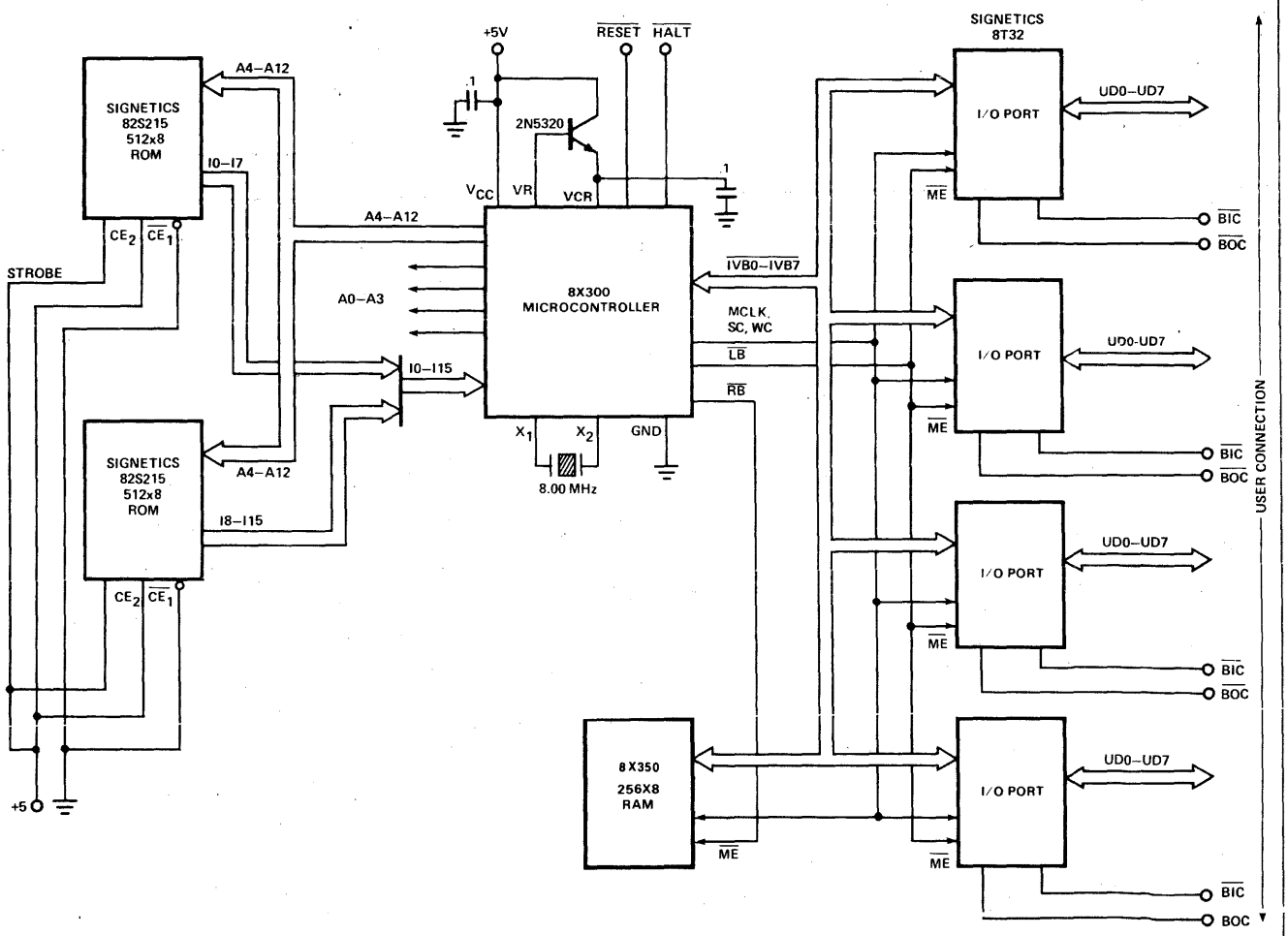


Figure 12

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Since some events are constrained to occur in certain quarter cycles, as system cycle times become slower, the delays will appear to increase due to gating with internal clocks. In the table of AC Electrical Characteristics, 2 columns are used: 1 to denote times which occur due to internal clock intervention and 1 to denote minimum delays for fast cycle times.

When using Signetics 8T32 I/O Ports, selection of instruction cycle time involves calculating the maximum program storage access time. Assuming the instruction is available when MCLK falls, the I/O control lines are stable 35ns later. Signetics 8T32's require another 35ns to disable a previously selected port and enable the desired port (assumes a change in bank signals). A 10ns margin has been added to the 8T32 enable for this evaluation to reflect the fact that most systems will have more capacitive loading than the 50pF test condition in the 8T32 specification and to allow for line delays.

The system instruction cycle time for normal systems such as shown in Figure 12 is determined by Microcontroller propagation delays, program storage access time, and port output enable times. Instruction cycle time is normally constrained by one or more of the following conditions:

1. Instruction to LB/RB (input phase) + I/O Port output enable: $T_{OE} \leq$ ½cycle - 55ns (Figure 13).
2. Program storage access time + instruction to LB/RB (input phase) + I/O Port output enable and IV data (input phase) to address ≤ instruction cycle time (Figure 14).
3. Program storage access time + instruction to address ≤ instruction cycle time (Figure 15).

The first constraint can be used to determine the minimum cycle time. Using the inequality 35ns + 35ns ≤ ½ cycle - 55ns implies ½ cycle ≥ 125ns or an instruction time of 250ns.

Program storage access time for a 250ns instruction cycle can be calculated from the second constraint. Noting that the specification for IV data (input phase) to address is 115ns: Program storage access time + 35ns + 35ns + 115ns ≤ 250ns implies program storage access time ≤ 65ns.

The third constraint can be used to verify the maximum program storage access time. Noting that the specification for instruction to address is 185ns: Program storage access time + 185ns ≤ 250ns confirms that program storage access time 65ns is satisfactory.

SYSTEM INSTRUCTION CYCLE TIME–INSTRUCTION TO IV DATA TIMES

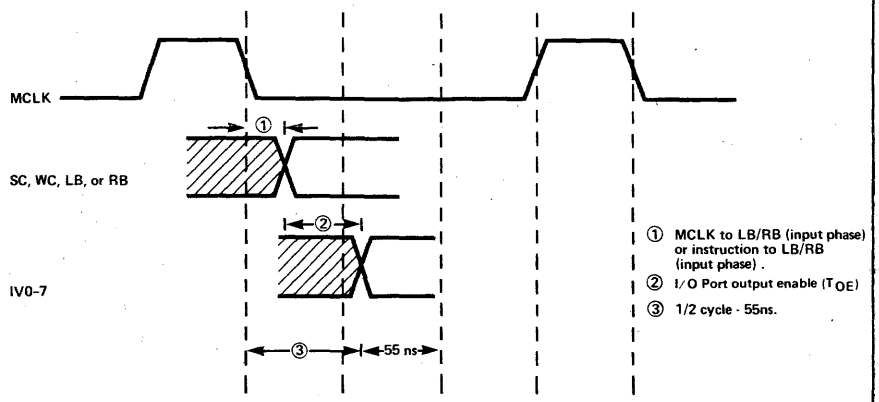


Figure 13

INSTRUCTION CYCLE TIME

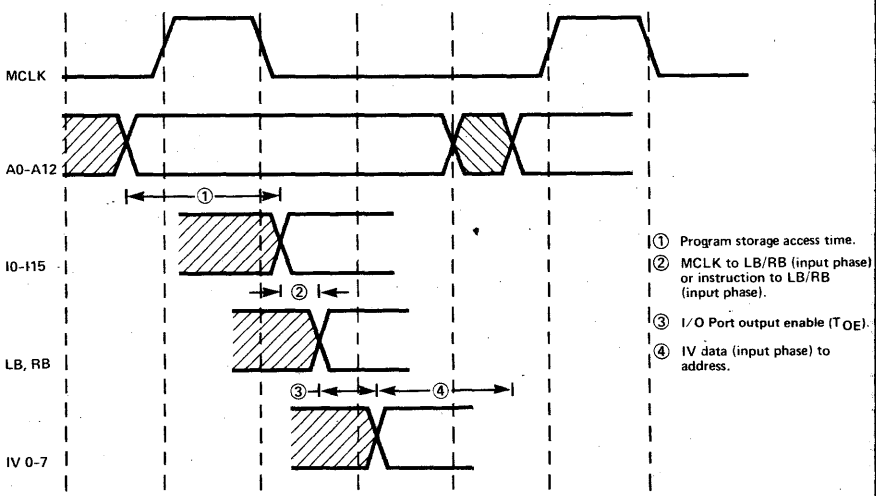


Figure 14

PROGRAM STORAGE ACCESS TIME

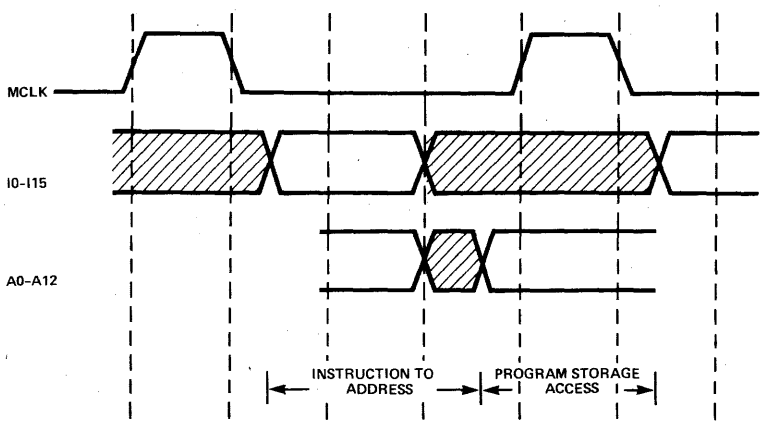


Figure 15

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System Clock

The Micrcontroller has an integrated oscillator which generates all necessary clock signals. The oscillator is designed to connect directly to a series resonant quartz crystal via pins X1 and X2. The crystal resonant frequency, f, is related to the desired cycle time, T, by the relationship f = 2/T. For a 250ns system, f = 8.00MHz.

Type:	Fundamental mode, series resonant
Impedance at Fundamental:	35 ohms maximum
Impedance at harmonics and spurs:	50 ohms minimum

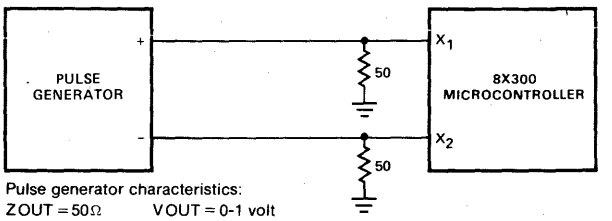
Table 7 CRYSTAL CHARACTERISTICS

In lower speed applications where the cycle time need not be precisely controlled, a capacitor may be connected between X1 and X2 to drive the oscillator. Approximate capacitor values are given in Table 8. If cycle time is to be varied, X1 and X2 should be driven from complementary outputs of a pulse generator. Figure 16 shows a typical configuration. For systems where the Interpreter is to be driven from a master clock the X1 and X2 lines may be interfaced to TTL logic as shown in Figure 17.

Cx,pF	CYCLE TIME
100	300ns
200	500ns
500	1.1μs
1000	2.0μs

Table 8 CLOCK CAPACITOR VALVES

CLOCKING WITH A PULSE GENERATOR

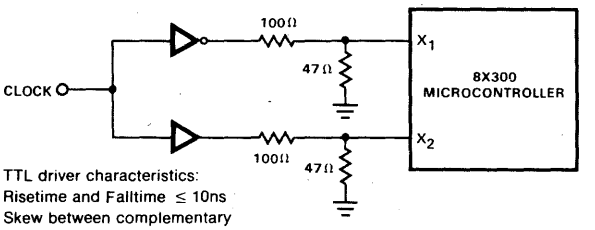


Pulse generator characteristics:
ZOUT = 50Ω VOUT = 0-1 volt
Risetime ≤ 10ns ≤ Skew ≤ 10ns
Complementary outputs

NOTE: All resistors values are typical and in ohms.

Figure 16

CLOCKING WITH TTL



TTL driver characteristics:
Risetime and Falltime ≤ 10ns
Skew between complementary outputs ≤ 10ns

Figure 17

AC ELECTRICAL CHARACTERISTICS V_{CC} = 5V ± 5% and 0°C ≤ T_A < 70°C

DELAY DESCRIPTION	PROPAGATION DELAY TIME	CYCLE TIME LIMIT
X1 falling edge to MCLK (driven from external pulse generator)	75ns	
MCLK to SC/WC falling edge (input phase)	25ns	
MCLK to SC/WC rising edge (output phase)		½ cycle + 25ns
MCLK to $\overline{LB}/\overline{RB}$ (input phase)	35ns	
Instruction to $\overline{LB}/\overline{RB}$ output (input phase)	35ns	
MCLK to $\overline{LB}/\overline{RB}$ (output phase)		½ cycle + 35ns
MCLK to IV data (output phase)	185ns	½ cycle + 60ns
IV data (input phase) to IV data (output phase)	115ns	
Instruction to Address	185ns	½ cycle + 40ns
MCLK to Address	185ns	½ cycle + 40ns
IV data (input phase) to Address	115ns	
MCLK to IV data (input phase)		½ cycle - 55ns
MCLK to Halt falling edge to prevent current cycle		¼ cycle - 40ns
Reset rising edge to first MCLK		0 to 1 cycle

NOTE
1. Reference to MCLK is to the falling edge when loaded with 300pF.
2. Loading on Address lines is 150pF.

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DC ELECTRICAL CHARACTERISTICS

Limits apply for $V_{CC} = 5V \pm 5\%$ and $0°C < T_A < 70°C$ unless specified otherwise.

PARAMETER		TEST CONDITIONS	LIMITS			UNIT
			Min	Typ	Max	
V_{IH}	High level input voltage					
	X1,X2		.6			V
	All others		2			V
V_{IL}	Low level input voltage					
	X1,X2				.4	V
	All others				.8	V
V_{IC}	Input clamp voltage (Note 1)	$V_{CC} = 4.75V$, $I_I = -10mA$			-1.5	V
I_{IH}	High level input current					
	X1,X2	$V_{CC} = 5.25V$, $V_{IH} = .6V$		2700		μA
	All others	$V_{CC} = 5.25V$, $V_{IH} = 4.5V$		<1	50	μA
I_{IL}	Low level input current					
	X1,X2	$V_{CC} = 5.25V$, $V_{IL} = .4V$		-2500		μA
	$\overline{IVBO}$-7			-140	-200	μA
	IO-I15	$V_{CC} = 5.25V$, $V_{IL} = .4V$		-880	-1600	μA
	$\overline{HALT}$, $\overline{RESET}$	$V_{CC} = 5.25V$, $V_{IL} = .4V$		-230	-400	μA
V_{OL}	Low level output voltage					
	A0-A12	$V_{CC} = 4.75V$, $I_{OL} = 4.25mA$		.35	.55	V
	All others	$V_{CC} = 4.75V$, $I_{OL} = 16mA$		.35	.55	V
V_{OH}	High level output voltage	$V_{CC} = 4.75V$, $I_{OH} = 3mA$	2.4			V
I_{OS}	Short circuit output current (Note 2)	$V_{CC} = 5.25V$	-30		-140	mA
V_{CC}	Supply voltage		4.75	5	5.25	V
I_{CC}	Supply current	$V_{CC} = 5.25V$			1.60	mA
I_{REG}	Regulator control	$V_{CC} = 5.0V$	-14		-21	mA
I_{CR}	Regulator current (Note 3)				290	mA
V_{CR}	Regulator voltage (Note 3)		2.2		3.2	V

NOTES
1. Crystal inputs X1 and X2 do not have clamp diodes.
2. Only one output may be grounded at a time.
3. $V_{CC} = 5.25V$, HALT = RESET = ADDRESS = IVX = 0.0V, all other pins open.

ABSOLUTE MAXIMUM RATINGS

PARAMETER	RATING	UNIT
V_{CC} Supply voltage	7	V
X1,X2 Crystal input voltage	2	V
Others Logic input voltage	5.5	V

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8T31-N,F

DESCRIPTION

The I/O Port is an 8-bit bidirectional data register designed to function as an I/O interface element in microprocessor systems. It contains 8 clocked data latches accessible from either a microprocessor port or a user port. Separate I/O control is provided for each port. The 2 ports operate independently, except when both are attempting to input data into the I/O Port. In this case, the user port has priority.

A master enable (ME) is provided that enables or disables the μP bus regardless of the state of the other inputs, but has no effect on the user bus.

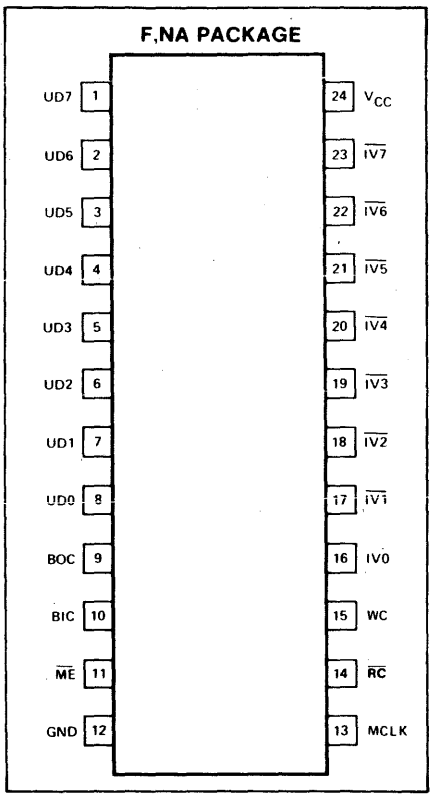
A unique feature of this family is its ability to start up in a predetermined state. If the clock is maintained at a voltage less than .8V until the power supply reaches 3.5V, the user port will always be all logic 1 levels, while the microprocessor port will be all logic 0 levels.

FEATURES

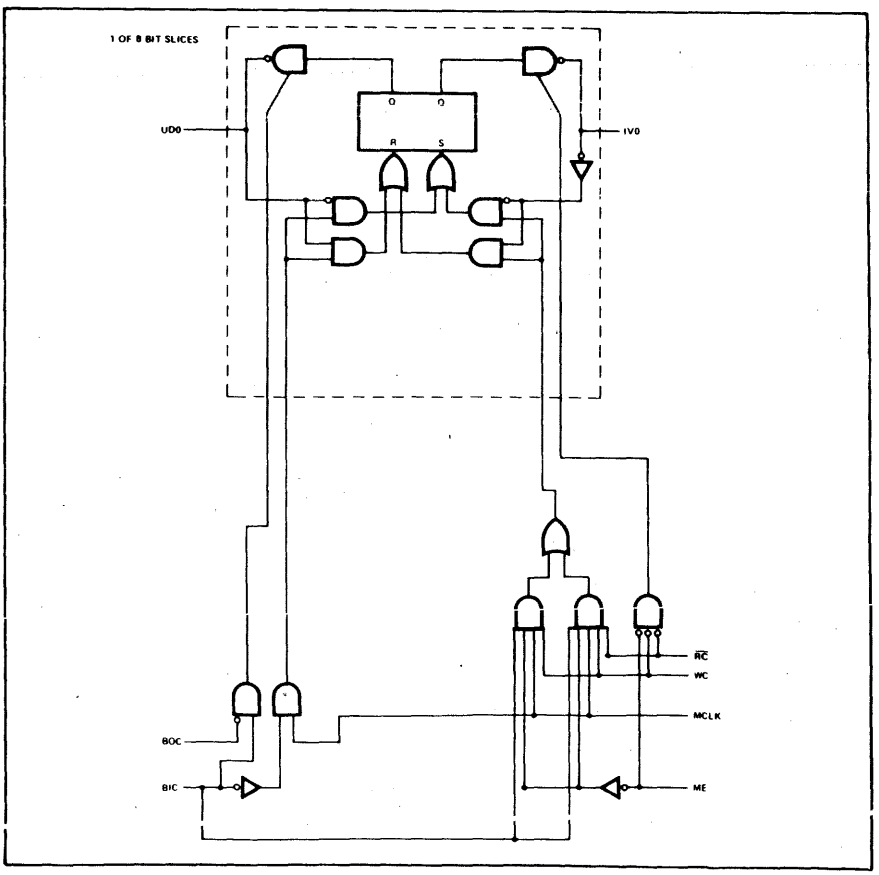
- **Each device has 2 ports, one to the user, the other to a microprocessor. I/O Ports are completely bidirectional**
- **Ports are independent, with the user port having priority for data entry**
- **User data input synchronous**
- **The user data bus is available with tri-state (8T32, 8T36) or open collector (8T33, 8T35) outputs**
- **At power up, the user port outputs are high**
- **Tri-state TTL outputs for high drive capability**
- **Directly compatible with the 8X300 Microcontroller**
- **Operates from a single 5V power supply over a temperature range of 0°C to +70°C**

PIN CONFIGURATION

F,NA PACKAGE



BLOCK DIAGRAM



signetics

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8T32/8T33/8T35/8T36-F,NA

TYPES

8T32 Tri-State, Synchronous User Port
8T33 Open Collector, Synchronous User Port
8T35 Open Collector, Asynchronous User Port
8T36 Tri-State, Asynchronous User Port

DESCRIPTION

The Addressable I/O Port is an 8-bit bidirectional data register designed to function as an I/O interface element in microprocessor systems. It contains 8 data latches accessible from either a microprocessor port or a user port. Separate I/O control is provided for each port. The 2 ports operate independently, except when both are attempting to input data into the I/O Port. In this case, the user port has priority.

A unique feature of the I/O Port is the way in which it is addressed. Each device has an 8-bit, field programmable address, which is used to enable the microprocessor port. When the SC control signal is high, data at the microprocessor port is treated as an address. If the address matches the I/O Port's internally programmed address, the microprocessor port is enabled, allowing data transfer through it.

The port remains enabled until an address which does not match is presented, at which time the port is disabled (data transfer is inhibited). A Master Enable input (ME) can serve as a ninth address bit, allowing 512 I/O Ports to be individually selected on a bus, without decoding. The user port is accessible at all times, independent of whether or not the microprocessor port is selected.

A unique feature of this family is their ability to start up in a predetermined state. If the clock is maintained at a voltage less than .8V until the power supply reaches 3.5V, the user port will always be all logic 1 levels, while the port will be all logic 0 levels.

ORDERING

The 8T32/33/35/36 may be ordered in preaddressed form. To order a preaddressed device use the following part number format:

N8TYY-XXX P

- P = F Ceramic package, NA Plastic package
- XXX = Any address from 000 through 255 (decimal) - 256 available addresses
- YY = I/O Port version (32, 33, 35, 36)

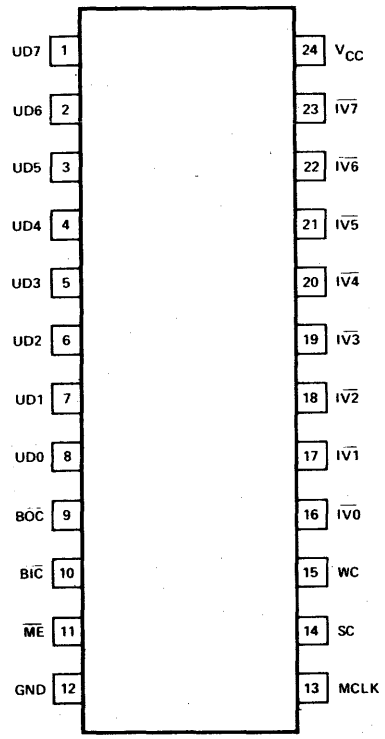
A stock of 8T32s and 8T36s with addresses 1 through 10 will be maintained. A small quantity of addresses 11 through 50 will also be available with a longer lead time.

FEATURES

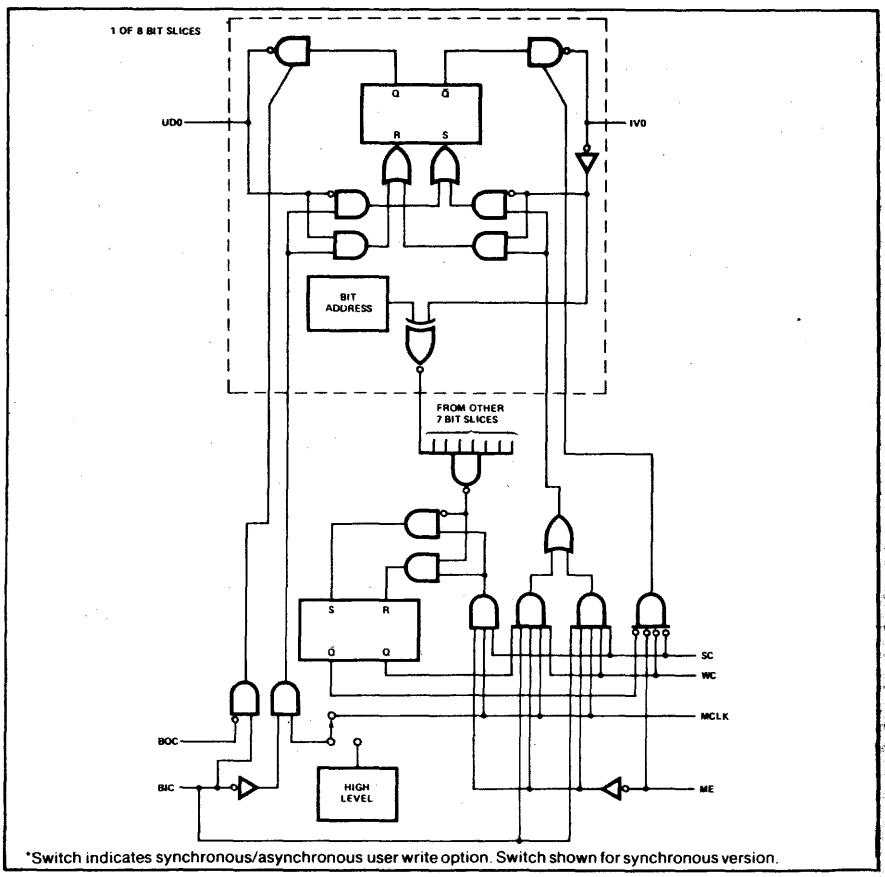
- **A field-programmable address allows 1 of 512 I/O Ports on a bus to be selected, without decoders.**
- **Each device has 2 ports, one to the user, the other to a microprocessor.**
- **Completely bidirectional.**
- **Ports are independent, with the user port having priority for data entry.**
- **A selected I/O Port de-selects itself when another I/O Port address is sensed.**
- **User data input available as synchronous (8T32, 8T33) or as asynchronous (8T35, 8T36) function.**
- **The user data bus is available with tri-state (8T32, 8T36) or open collector (8T33, 8T35) outputs.**
- **At power up, the I/O Port is not selected and the user port outputs are high.**
- **Tri-state TTL outputs for high drive capability.**
- **Directly compatible with the 8X300 Microcontroller.**
- **Operates from a single 5V power supply over a temperature range of 0° C to 70° C.**

PIN CONFIGURATION

F,NA PACKAGE



BLOCK DIAGRAM



*Switch indicates synchronous/asynchronous user write option. Switch shown for synchronous version.

signetics

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PRELIMINARY SPECIFICATION 8T39-I,XL

DESCRIPTION

The Bus Expander is specifically designed to increase the I/O capability of 8X300 systems previously limited by fanout considerations. The bus expander serves as a buffer between the 8X300 and blocks of I/O devices. Each bus expander can buffer a block of 16 I/O ports while only adding a single load to the 8X300.

FEATURES

- **15ns max propagation delay**
- **Bidirectional**
- **Three-state outputs on both ports**
- **Pre-programmed address range**

APPLICATIONS

The 8T39 Bus Expander is designed to be used with the 8X300 microprocessor to allow increased I/O capability in those systems previously limited by fanout considerations. Figure 1 shows a typical arrangement of the bus expander in an 8X300 system. Each expander services I/O ports whose address is within the range of the expander. Other I/O ports or working storage may be directly connected to the bus as shown.

The bus expander is not limited to use with the 8X300, but may be applied in any system which uses a combined address/data bus.

8T39 ADDRESSING

During normal operation of the 8X300 when an I/O port address is being sent on the IV Bus (SC is high), the I/O port will examine all eight bits of the microprocessor bus for an address compare. Since the 8T39 is used to buffer blocks of I/O ports, only the four most significant bits are examined by the 8T39 for an address compare.

Note that redundant addresses are not programmed into separate devices. Rather, a discrete device (such as the 8T39-03) may be wired for any address requiring two 1 bits and two 0 bits in the address. The various address ranges for this same device are obtained by permuting the high order (DI0 and DO0 are MSB) data lines accordingly. Both input and output lines must be redefined in order to maintain data and address integrity on the extended bus. Table 1 summarizes the 8T39 addressing.

Address functions are specified with the convention that bit 0 is the MSB and bit 7 is the LSB. The DI microprocessor bus address decoding is active low.

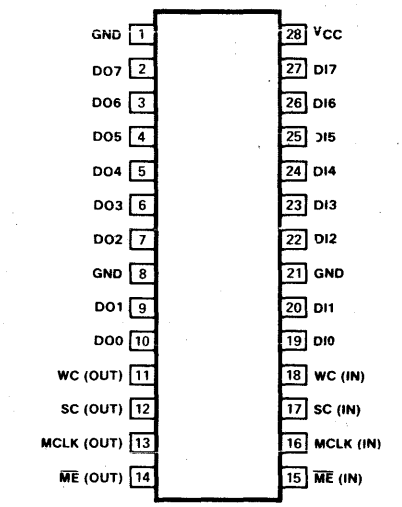
FUNCTIONAL DESCRIPTION

The Bus Expander contains eight sets of non-inverting bidirectional tri-state drivers for the bus data bits, four non-inverting unidirectional drivers for I/O port control, and necessary control logic. The control logic is required to maintain the proper directional transfer of bus data as dictated by the states of the I/O port control signals and the currently enabled I/O port. Each bus expander is programmed during manufacturing to respond to a specific block of I/O port addresses. Only I/O ports with addresses in the range of a given bus expander may be connected to that expander. A bus expander may be used on either left bank or right bank. Multiple expanders on the same bank must have different address ranges; however, expanders with the same address range can be connected if they are on different banks. Systems may be configured with I/O ports connected directly to the 8X300, as well as I/O ports connected through a bus expander; however, no unbuffered I/O port may have an address within the span of a bus expander on the same bank.

Addition of bus expanders may impact system cycle time due to the added delay in the data path. For the purposes of calculating allowable cycle time as described in the 8X300 data sheet, the bus expander delays may be considered additive to the I/O port delays so that a buffered I/O port simply appears as a slower I/O port.

PIN CONFIGURATION

I,XL PACKAGE



PIN DESIGNATION

PIN NO.	SYMBOL	NAME AND FUNCTION	TYPE
2-7,9,10	DO0-DO7	I/O port data bus	Active low, three-state
11	WC(OUT)	Write command output	Active high
12	SC(OUT)	Select command output	Active high
13	MCLK(OUT)	Master clock output	Acitve high
14	$\overline{ME}$(OUT)	Master enable output	Active low
15	$\overline{ME}$(IN)	Master enable input	Active low
16	MCLK(IN)	Master clock input	Active high
17	SC(IN)	Select command output	Active high
18	WC(IN)	Write command output	Active high
19,20,22-27	DI0-DI7	Microprocessor data bus	Active low, three-state
1,8,21	GND	Ground	
28	V_{CC}	+5 volt supply	

PART TYPE	ADDRESS PATTERN MSB(0) LSB(7)	ADDRESS BLOCKS Octal
8T39-00	0000XXXX	0-17
8T39-01	0001XXXX	20-37, 40-57, 100-117, 200-217
8T39-03	0011XXXX	60-77, 120-137, 220-237, 140-157, 240-257, 300-317
8T39-07	0111XXXX	160-177, 260-277, 320-337, 340-357
8T39-17	1111XXXX	360-377

Table 1 8T39 ADDRESSING SUMMARY

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PRELIMINARY SPECIFICATION 8T40/29540 I,N

DESCRIPTION

The Pipelined I/O Port is designed as a high speed multiple input/multiple output latched bus transceiver. The unique two-latch/or multiple-bus organization is well suited for any application in which several data buses are interconnected.

The organization of the part allows data from four sources (BUS X, INPUT A, INPUT B, INPUT C) to be routed to the INPUT LATCH. The INPUT LATCH drives bus Y via a three state 20mA driver. Bus Y can be driven by the INPUT LATCH via the three state Y bus driver, latched into the INPUT LATCH, or both. The OUTPUT LATCH is then able to drive Bus X via the Bus X three state 40mA driver, or Bus X can be latched into the input latch, or both. Use of the circuit is simplified by separate control lines to the INPUT MULTIPLEXER, INPUT LATCH, OUTPUT LATCH, and the three state drivers. Advanced low power Schottky processing is used to fabricate this 28 lead dual-in-line device.

FEATURES

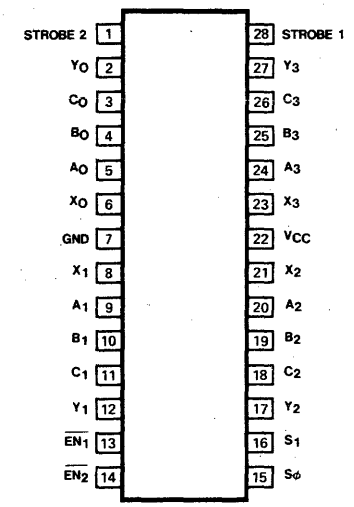
- **4 Bit organization on all data paths**
- **2 Output buses with high current, three-state drivers**
- **2 Internal storage latches**
- **Organized for efficient interconnection to multiple buses**
- **4 Data paths to the input latch**
- **Separate input latch and output latch strobes**
- **Simple control, easy to use**
- **Low power Schottky technology**
- **28 Pin dual-in-line package**

APPLICATIONS

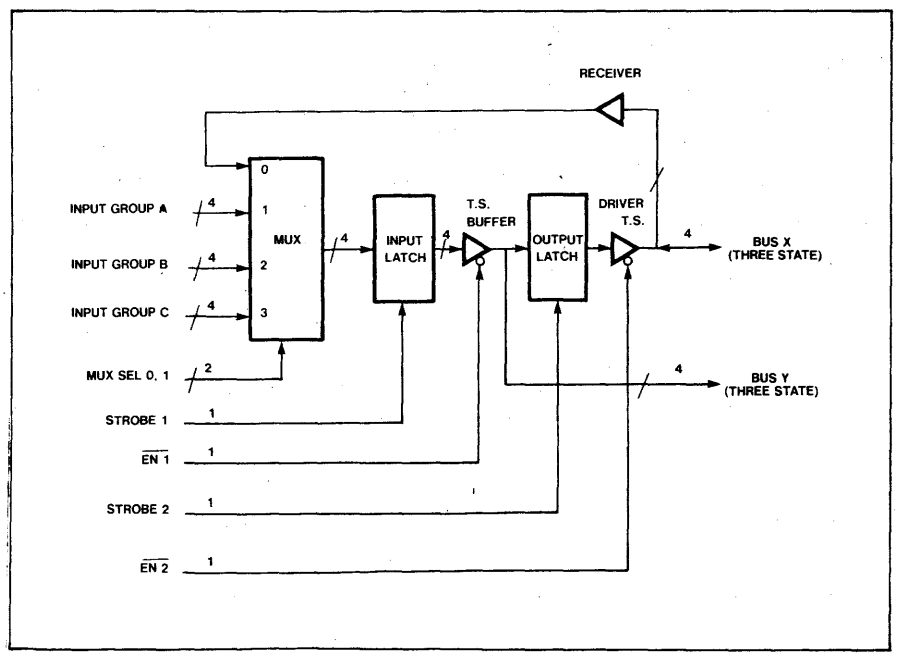
- **Data routing between floating point processor, CPU & Memory; or other sources**
- **Multiport memory data and address handling**
- **Data path element for CPU, I/O & memory**
- **Byte swap, character swap, without CPU intervention**
- **Ideal for the following system environments:**
  - **Bipolar Microcomputer Systems**
  - **Bipolar Minicomputer Systems**
  - **Data Communications**
  - **Smart Peripheral Controllers**
  - **Multiprocessing Systems**

PIN CONFIGURATION

IW, NQ PACKAGE



BLOCK DIAGRAM



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8T58-I,XL

DESCRIPTION

The Bus Expander is specifically designed to increase the I/O capability of 8X300 systems previously limited by fanout considerations. The bus expander serves as a buffer between the 8X300 and blocks of I/O devices. Each bus expander can buffer a block of 16 I/O ports while only adding a single load to the 8X300.

FEATURES

- **15ns max propagation delay**
- **Bidirectional**
- **Three-state outputs on both ports**

FUNCTIONAL DESCRIPTION

The Bus Expander contains eight sets of non-inverting bidirectional tri-state drivers for the bus data bits, four non-inverting undirectional drivers for I/O port control, and necessary control logic. The control logic is required to maintain the proper directional transfer of bus data as dictated by the states of the I/O port control signals. A bus expander may be used on either left bank or right bank. Systems may be configured with I/O ports connected directly to the 8X300, as well as I/O ports connected through a bus expander.

Addition of bus expanders may impact system cycle time due to the added delay in the data path. For the purposes of calculating allowable cycle time as described in the 8X300 data sheet, the bus expander delays may be considered additive to the I/O port delays so that a buffered I/O port simply appears as a slower I/O port.

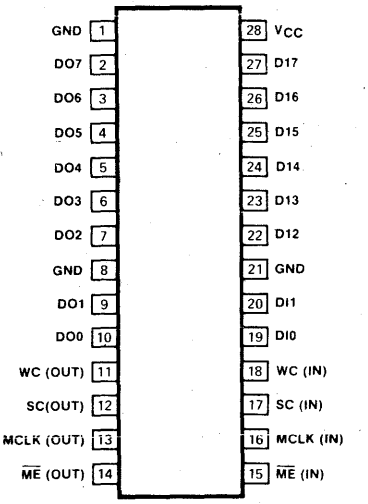
APPLICATIONS

The 8T39 Bus Expander is designed to be used with the 8X300 microprocessor to allow increased I/O capability in those systems previously limited by fanout considerations. Figure 1 shows a typical arrangement of the bus expander in an 8X300 system. Other I/O ports or working storage may be directly connected to the bus as shown.

The bus expander is not limited to use with the 8X300, but may be applied in any system which uses a combined address/data bus.

PIN CONFIGURATION

I,XL PACKAGE



μP Side

TRUTH TABLE

$\overline{ME}$	SC	WC	DATA TRANSFER DIRECTION	ADDRESS COMPARISON
L	L	L	DI Bus ← DO Bus	No
L	L	H	DI Bus → DO Bus	No
L	H	X	DI Bus → DO Bus	No
H	X	X	DI Bus → DO Bus	No

PIN DESIGNATION

PIN NO.	SYMBOL	NAME & FUNCTION	TYPE
2-7,9,10	DO0-DO7	I/O port data bus	Active low, three-state
11	WC(OUT)	Write command output	Active high
12	SC(OUT)	Select command output	Active high
13	MCLK(OUT)	Master clock input	Active high
14	$\overline{ME}$(OUT)	Master enable output	Active low
15	$\overline{ME}$(IN)	Master enable input	Active low
16	MCLK(IN)	Master clock input	Active high
17	SC(IN)	Select command output	Active high
18	WC(IN)	Write command output	Active high
19,20,22-27	DI0-DI7	Microprocessor data bus	Active low, three-state
1,8,21	GND	Ground	
28	VCC	+5 volt supply	

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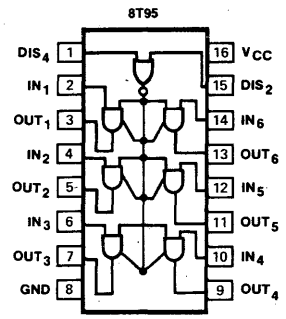
8T95-N,F • 8T96-N,F • 8T97-N,F • 8T98-N,F

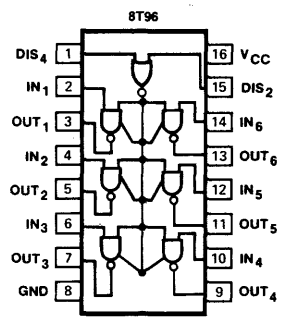
DESCRIPTION

Each of the 3-State Bus Interface Elements described herein has low current PNP inputs and is designed with Schottky TTL technology for ultra high speed. The devices are used to convert TTL/DTL or MOS/CMOS to 3-state TTL Bus levels. For maximum systems flexibility the 8T95 and 8T97 do so without logic inversion, whereas, the 8T96 and 8T98 provide the logical complement of the input. The 8T95 and 8T96 feature a common control line for all six devices, whereas, the 8T97 and 8T98 have control lines for four devices from one input and two from another input.

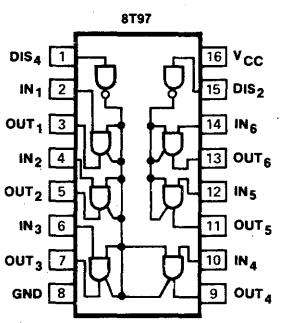
PIN CONFIGURATIONS

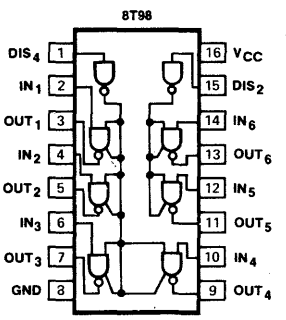
N,F PACKAGE





N,F PACKAGE





TRUTH TABLE

DEVICE	DISABLE DIS_1	DISABLE DIS_4	INPUT DIS_2	INPUT	OUTPUT
8T95	0	—	0	0	0
	0	—	0	1	1
	0	—		x	H-z
	1	—	0	x	H-z
	1	—	1	x	H-z
8T96	0	—	0	0	1
	0	—	0	1	0
	0	—	1	x	H-z
	1	—	0	x	H-z
	1	—	1	x	H-z
8T97	—	0	0	0	0
	—	0	0	1	1
	—	x	1	x	H-z*
	—	1	x	x	H-z**
8T98	—	0	0	0	1
	—	0	0	1	0
	—	x	1	x	H-z*
	—	1	x	x	H-z**

*Output 5-6 only **Output 1-4 only x = irrelevant

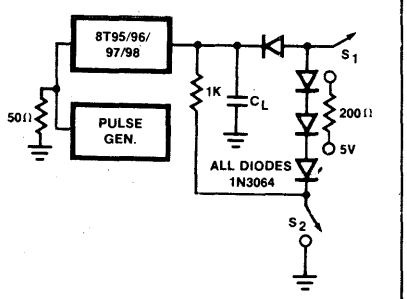
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8T95-N,F • 8T96-N,F • 8T97-N,F • 8T98-N,F

DC ELECTRICAL CHARACTERISTICS

PARAMETER		TEST CONDITIONS	LIMITS Min	Typ	Max	UNIT
	Input voltage					
V_{IL}	Low				0.8	V
V_{IH}	High		2.0			V
V_{IC}	Clamp	V_{CC} = MIN, I_{IN} = -12mA				
	Input				-1.5	V
	Output to ground				-1.5	V
	Output voltage	V_{CC}= MIN				
V_{OL}		I_{OL} = 48mA			0.5	V
V_{OH}		I_{OH} = 5.2mA	2.4			V
	Input current	V_{CC} = MAX, V_{IN} = 0.5V				
I_{IL}	Low	D_{IS} = 0.5V			-400	μA
		D_{IS} = 2.0V (third state)			-40	μA
I_{IH}	High	V_{IN} = 2.4V			40	μA
I_{OS}	Short circuit output current	V_{CC} = MAX, V_{IN} = 0V, V_{OUT} = 0V	-40	-80	-115	μA

AC TEST CIRCUIT

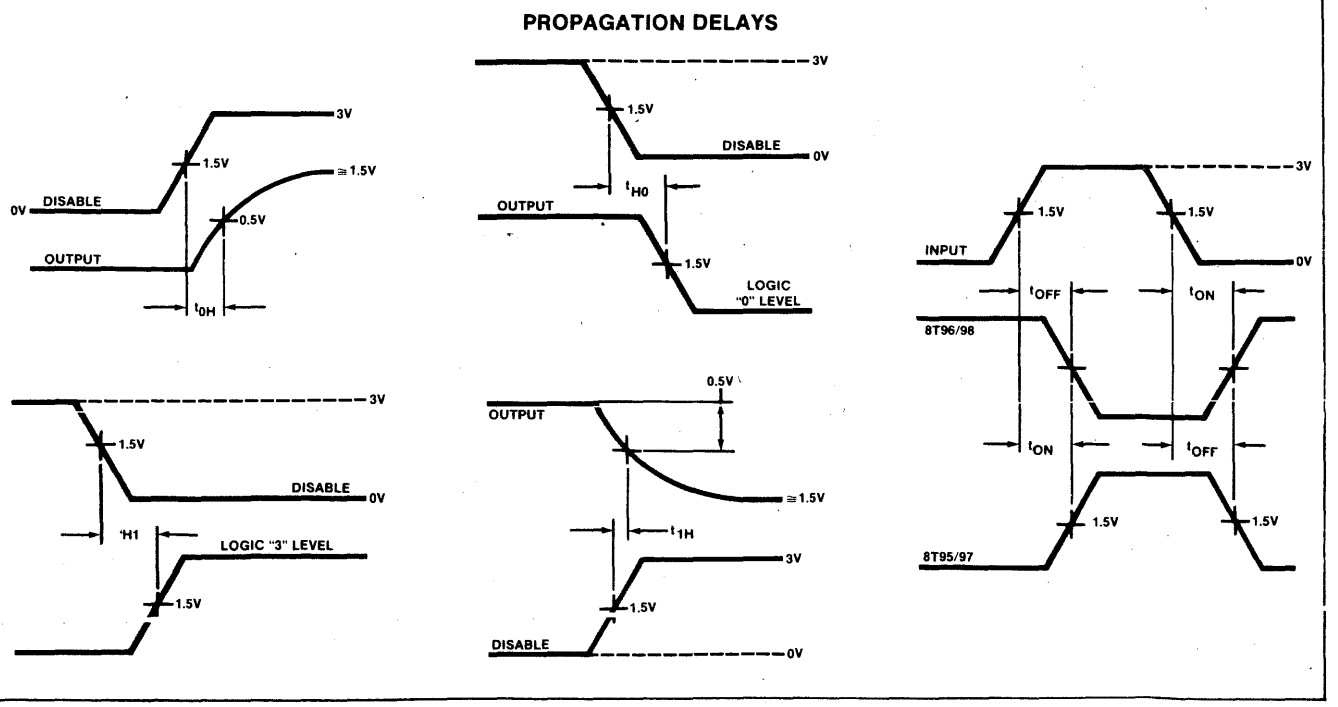


Input Characteristics
PA = 3V, f = 1MHz $t_R = t_F \leq$ 10ns (10% to 90%)
C_L includes probe and jig capacitance.

AC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V

PARAMETER	TO	FROM	TEST CONDITIONS	8T95/97 Min	Typ	Max	8T96/98 Min	Typ	Max	UNIT
Propagation delay										
t_{ON}	Outputs	Inputs		3	9	13	3	6	10	ns
t_{OFF}	Outputs	Inputs		3	7	12	4	7	11	ns
Disable to Outputs										
t_{POH}	High Z	Low	S_1, S_2 are closed, C_L = 5pF	3	6	12	5	10	16	ns
t_{PLH}	High Z	High	S_1, S_2 are closed, C_L = 5pF	3	5	10	3	6	10	ns
t_{PHO}	Low	High Z	S_1 is closed, S_2 is open; C_L = 50pF	12	14	25	11	18	24	ns
t_{PHL}	High	High Z	S_1 is open, S_2 is closed; C_L = 50pF	8	19	25	7	15	22	ns

PARAMETER MEASUREMENT INFORMATION



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DESCRIPTION

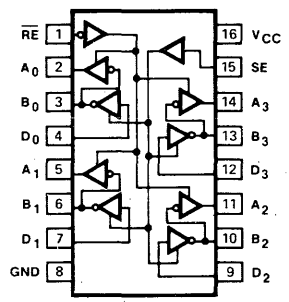
The 8T126 thru 8T129 are quad transceivers designed to handle many bus interface applications. The devices feature 3-state outputs on both send and receive buffers, and pnp transistors on all inputs to reduced input LOW loading requirements.

The 8T126 and 8T128 feature a 3.4V minimum V_{OH} level on the receiver for MOS interface applications. The send and receive buffers have separate enable inputs for independent control.

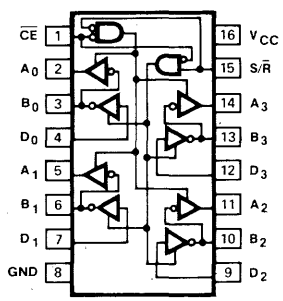
The 8T127 and 8T129 feature full 24mA drive in both send and receive buffers. These devices have a common Chip Enable input for easy cascading, and a Send/Receive input for direction control.

PIN CONFIGURATIONS

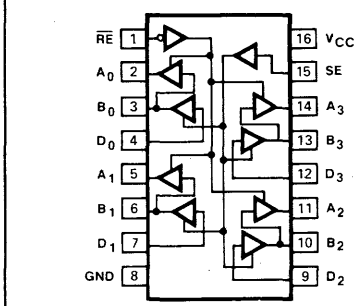
8T126



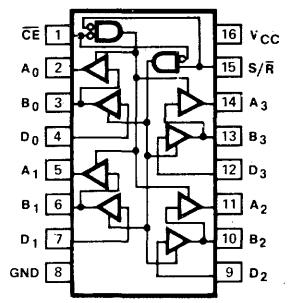
8T127



8T128



8T129



ORDERING CODE (See Section 9 for further Package and Ordering Information)

PACKAGES	COMMERCIAL RANGES V_{CC}=5V±5%; T_A=0°C to +70°C	MILITARY RANGES V_{CC}=5V±10%; T_A=−55°C to +125°C
Plastic DIP	N8T126N • N8T127N N8T128N • N8T129N	
Ceramic DIP	N8T126F • N8T127F N8T128F • N8T129F	S8T126F • S8T127F S8T128F • S8T129F
Flatpak		S8T126W • S8T127W S8T128W • S8T129W

INPUT AND OUTPUT LOADING AND FAN-OUT TABLE[a]

PINS	DESCRIPTION		8T126	8T127	8T128	8T129
$\overline{RE}$	Receive Enable (active LOW) input	I_{IH} (μA) I_{IL} (mA)	20 −0.1		20 −0.1	
SE	Send Enable (active HIGH) input	I_{IH} (μA) I_{IL} (mA)	20 −0.1		20 −0.1	
$\overline{CE}$	Chip Enable (active LOW) input	I_{IH} (μA) I_{IL} (mA)		20 −0.2		20 −0.2
S/$\overline{R}$	Send/Receive control input	I_{IH} (μA) I_{IL} (mA)		20 −0.2		20 −0.2
D_0-D_3	Data inputs	I_{IH} (μA) I_{IL} (mA)	20 −0.1	20 −0.2	20 −0.1	20 −0.2
B_0-B_3	Bus inputs	I_{IH} (μA) I_{IL} (mA)	20 −0.1	20 −0.2	20 −0.1	20 −0.2
B_0-B_3	3-State bus outputs	I_{OH} (mA) I_{OL} (mA)	−2/−5.2(a) 12/24(a)	−2/−5.2(a) 12/24(a)	−2/−5.2(a) 12/24(a)	−2/−5.2(a) 12/24(a)
A_0-A_3	3-State receiver outputs	I_{OH} (mA) I_{OL} (mA)	−1/−2.6(a) 6/12(a)	−2/−5.2(a) 12/24(a)	−1/−5/2(a) 6/12(a)	−2/−5.2(a) 12/24(a)

NOTE

a. The slashed numbers indicate different parametric values for Military Commercial temperature ranges respectively.

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FUNCTION TABLE (8T126)

INPUTS			RECVR. OUT	BUS I/O
SE	$\overline{RE}$	D_n	A_n	B_n
L	L	X	A = $\overline{B}$	INPUTS
L	H	X	(Z)	(Z)
H	H	L	(Z)	H
H	H	H	(Z)	L
H	L	L	L	H
H	L	H	H	L

H = HIGH voltage level
L = LOW voltage level
X = Don't care
(Z) = High impedance "off" stage

FUNCTION TABLE (8T128)

INPUTS			RECVR. OUT	BUS I/O
SE	$\overline{RE}$	D_n	A_n	B_n
L	L	X	A = B	INPUTS
L	H	X	(Z)	(Z)
H	H	L	(Z)	L
H	H	H	(Z)	H
H	L	L	L	L
H	L	H	H	H

H = HIGH voltage level
L = LOW voltage level
X = Don't care
(Z) = High impedance "off" stage

FUNCTION TABLE (8T127)

INPUTS			RECVR. OUT	BUS I/O
$\overline{CE}$	S/$\overline{R}$	D_n	A_n	B_n
L	L	X	A = $\overline{B}$	INPUTS
L	H	L	(Z)	H
L	H	H	(Z)	L
H	X	X	(Z)	(Z)

H = HIGH voltage level
L = LOW voltage level
X = Don't care
(Z) = High impedance "off" stage

FUNCTION TABLE (8T129)

INPUTS			RECVR. OUT	BUS I/O
$\overline{CE}$	S/$\overline{R}$	D_n	A_n	B_n
L	L	X	A = B	INPUTS
L	H	L	(Z)	L
L	H	H	(Z)	H
H	X	X	(Z)	(Z)

H = HIGH voltage level
L = LOW voltage level
X = Don't care
(Z) = High impedance "off" stage

AC CHARACTERISTICS: T_A = 25°C (See Section 4 for Waveforms and Conditions)

PARAMETER		TEST CONDITIONS	8T126/8T128		8T127/8T129		UNIT
			Min	Max	Min	Max	
t_{PLH} t_{PHL}	Propagation delay Data to bus output	Waveforms 1 & 2 C_L = 100pF, R_L = 667Ω		20 30		20 30	ns ns
t_{PLH} t_{PHL}	Propagation delay bus to receiver output	Waveforms 1 & 2 C_L = 50pF, R_L = 667Ω		20 30		20 25	ns ns
t_{PZH}	Enable to HIGH for bus output	Waveform 6 C_L = 100pF, R_L = 667Ω		30		35	ns
t_{PZH}	Enable to HIGH for receiver output	Waveform 6 C_L = 50pF, R_L = 667Ω		25		30	ns
t_{PZL}	Enable to LOW for bus output	Waveform 7 C_L = 100pF, R_L = 667Ω		35		35	ns
t_{PZL}	Enable to LOW for receiver output	Waveform 7 C_L = 50pF, R_L = 667Ω		30		30	ns
t_{PHZ}	Disable from HIGH	Waveform 6, C_L = 5pF, R_L = 667Ω		25		25	ns
t_{PLZ}	Disable from LOW	Waveform 7, C_L = 5pF, R_L = 667Ω		25		25	ns

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DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE

PARAMETER		TEST CONDITIONS		8T126/8T128		8T127/8T129		UNIT
				Min	Max	Min	Max	
V_{IH}	Input HIGH voltage	Guaranteed input HIGH threshold voltage		2.0		2.0		V
V_{IL}	Input LOW voltage	Guaranteed input LOW threshold voltage	Mil		0.7		0.7	V
			Com		0.8		0.8	V
V_{CD}	Input clamp diode voltage	V_{CC} = Min, I_{IN} = −18mA			−1.5		−1.5	V
V_{OH}	Output HIGH voltage for Bus outputs	V_{CC} = Min,	I_{OH} = −2.0mA Mil	2.4		2.4		V
			I_{OH} = −5.2mA Com	2.4		2.4		V
V_{OH}	Output HIGH voltage Receiver outputs	V_{CC} = Min, V_{IN} = V_{IL} or V_{IH} per Truth Table	I_{OH} = −100μA Mil	3.1				V
			I_{OH} = −100μA Com	3.4				V
			I_{OH} = −1.0mA Mil	2.4				V
			I_{OH} = −2.0mA Mil			2.4		V
			I_{OH} = −2.6mA Com	2.4				V
			I_{OH} = −5.2mA Com			2.4		V
V_{OL}	Output LOW voltage for Bus outputs	V_{CC} = Min,	I_{OL} = 12mA Mil & Com		0.4		0.4	V
			I_{OL} = 24mA Com		0.5		0.5	V
V_{OL}	Output LOW voltage for Receiver outputs	V_{CC} = Min,	I_{OL} = 6mA Mil & Com		0.4			V
			I_{OL} = 12mA Mil & Com				0.4	V
			I_{OL} = 12mA Com		0.5			V
			I_{OL} = 24mA Com				0.5	V
I_{OZH}	Output "off" current HIGH	V_{CC} = Max, V_{OUT} = 2.4V			20		20	μA
I_{OZL}	Receiver "off" current LOW	V_{CC} = Max, V_{OUT} = 0.4V			−20		−20	μA
I_{OZL}	Bus "off" current LOW	V_{CC} = Max, V_{OUT} = 0.4V			−100		−200	μA
I_{IH}	Input HIGH current	V_{CC} = Max, V_{IN} = 2.7V			20		20	μA
I_I	Input breakdown current	V_{CC} = Max,	Bus inputs V_{IN} = 5.5V		100		100	μA
			others V_{IN} = 10V		100		100	μA
I_{IL}	Input LOW current	V_{CC} = Max, V_{IN} = 0.4V			−100		−200	μA
I_{OS}	Output short circuit current	V_{CC} = Max, V_{OUT} = 0V		−40	−120	−40	−120	mA
I_{CCH}	Supply current HIGH	V_{CC} = Max, outputs HIGH			26		36	mA
I_{CCL}	Supply current LOW	V_{CC} = Max, outputs LOW			30		42	mA
I_{CCZ}	Supply current "off"	V_{CC} = Max, outputs "off"			36		44	mA

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PRELIMINARY SPECIFICATION

DESCRIPTION

The Signetics 2621 Universal Sync Generator (USG) provides the timing and control signals necessary for generating and displaying TV video information in the PAL format.

The USG accepts a single 3.55MHz input clock and generates various timing outputs including vertical, horizontal and composite blanking, composite sync and color burst flag. Several auxiliary clock outputs are also provided.

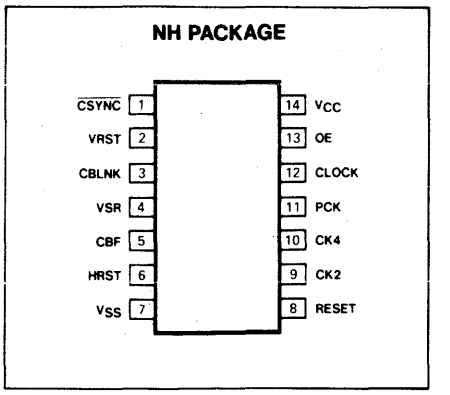
The USG is primarily intended for use in microprocessor-controlled video games. A typical game configuration consists of a 2621 USG, a 2650A microprocessor, a 2636 Programmable Video Interface, a 2616 16K ROM, and digital video summer circuitry.

The 2621 is constructed using Signetics silicon gate N-channel depletion load technology and operates from a single +5 volt power supply.

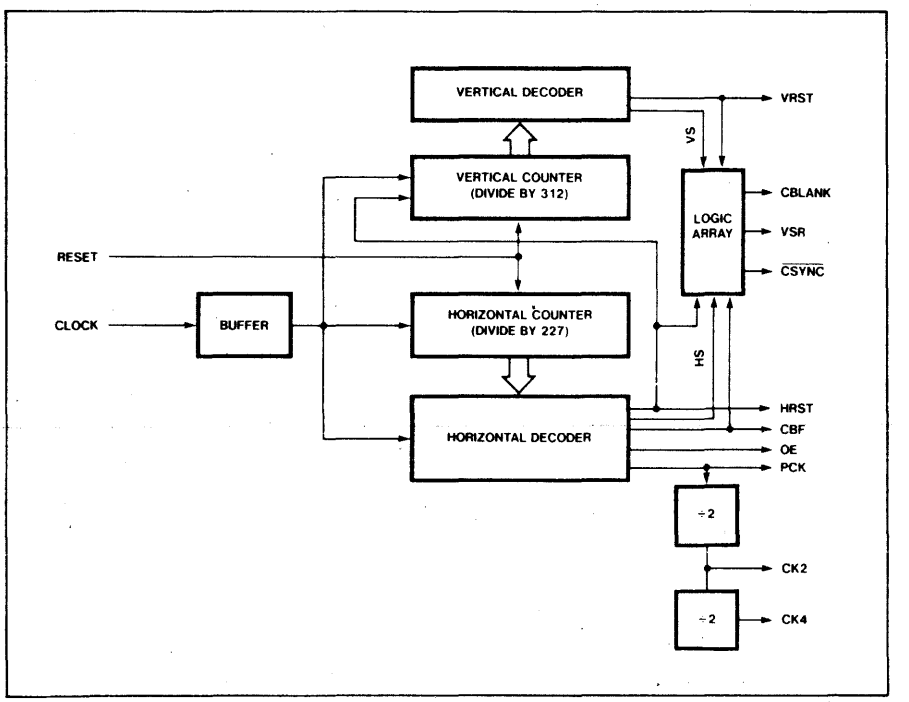
The Signetics 2622 Universal Sync Generator (USG) provides the timing and control signals necessary for generating and displaying TV video information in the NTSC format.

The USG accepts a single 3.5795MHz input clock and generates various timing outputs including vertical, horizontal, and composite blanking, composite sync and color burst flag. Several auxiliary clock outputs are also provided. The USG is primarily intended for use in microprocessor-controlled video games. A typical game configuration consists of a 2622 USG, a 2650A microprocessor, a 2636 Programmable Video Interface, a 2616 16K ROM, and an NE549 Digital Video Summer. The 2622 is constructed using Signetics silicon gate N-channel depletion load technology and operates from a single +5 volt power supply.

PIN CONFIGURATION



BLOCK DIAGRAM



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PRELIMINARY SPECIFICATION 2636I

DESCRIPTION

The Signetics 2636 Programmable Video Interface (PVI) is intended for use in microprocessor-controlled game systems, and provides all of the common game circuits on a single chip. Circuits are provided for player inputs, background, moving objects, scoring, and audio signals.

A typical system configuration consists of five LSI circuits: a PVI, a 2616 16K ROM, an NE549 Digital Video Summer (DVS) a Universal Sync Generator (USG), and a 2650A microprocessor.

Additional PVIs as well as random logic can easily be interfaced to enhance game complexity. Since the system is microprocessor based, the actual game itself need not be "hardwired" into the system. Game definition is completely contained in the ROM. To change games, one simply replaces one ROM with another. Each ROM can contain several games, depending on game complexity and similarity between games.

The 2636 PVI is constructed using Signetics' silicon gate N-Channel depletion load technology and operates from a single +5 volt power supply.

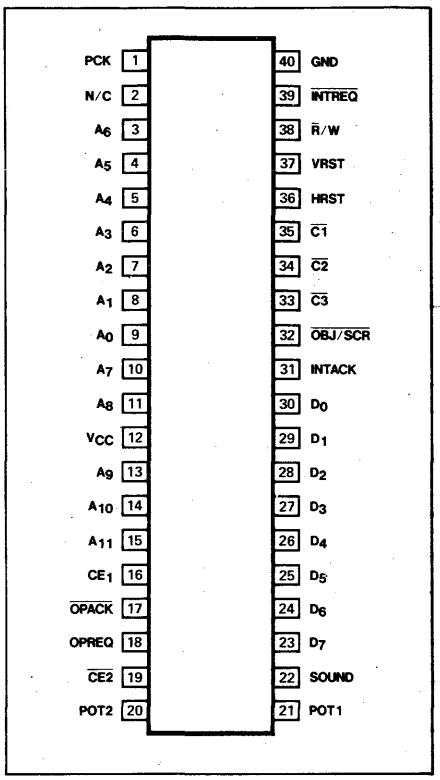
FEATURES

- **Four general-purpose, RAM-resident object modules**
- **Object duplication permitting generation of up to 80 object images on the screen**
- **280ns object resolution**
- **Object size and position under program control**
- **Programmable score**
- **Programmable sound**
- **Programmable background**
- **Eight programmable colors with multiple brightness levels**
- **37-byte scratch pad memory**
- **Chip Enable outputs for system ROMs and PROMs**
- **I/O facilities for switch scanning and potentiometer inputs**
- **Wire-OR expansion capability to multiple PVIs**
- **Forty-pin dual-in-line package**

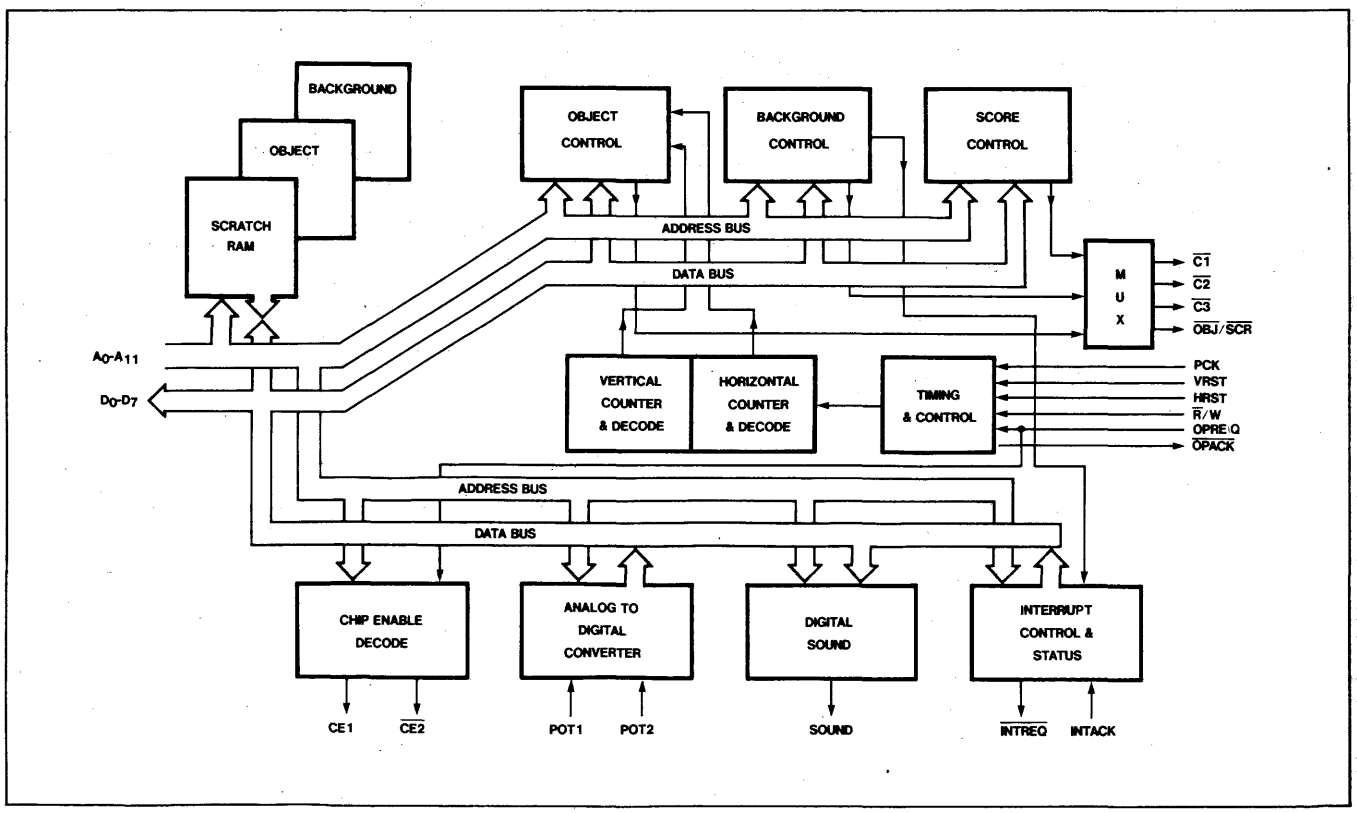
APPLICATIONS

- **Consumer programmable video games**
- **Arcade games**
- **Simulators**
- **Special purpose graphic displays**
- **Home computer center**

PIN CONFIGURATION



PVI BLOCK DIAGRAM



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PRELIMINARY SPECIFICATION

DESCRIPTION

The 2650A and -1 are additional members of the Signetics family of 8 bit, NMOS microprocessors.

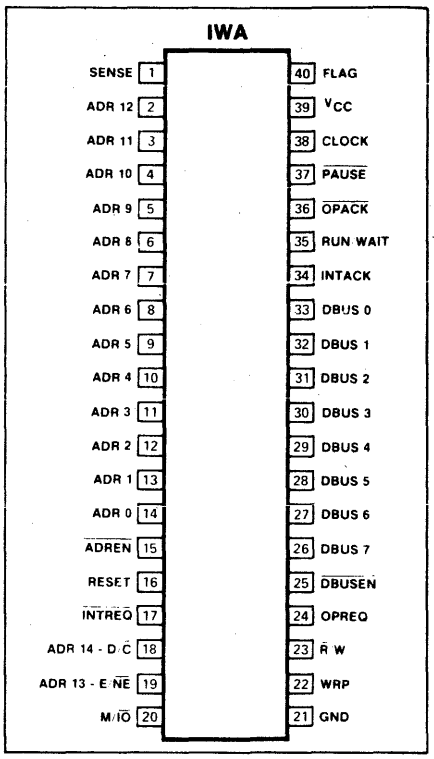
The 2650A is a functional equivalent of the 2650 with a new mask design which provides improved device operating margins.

The 2650A-1 is a high speed version of the 2650A.

FEATURES

- **Static 8 bit parallel NMOS microprocessor**
- **Single power supply of +5 volts**
- **TTL level single phase clock**
- **Standard 40 pin dual in-line package**
- **TTL compatible inputs and outputs**
- **75 variable length instructions of 1, 2 or 3 bytes**
- **32k byte address range**
- **Coding efficiency with multiple addressing modes**
- **Synchronous or asynchronous memory and I/O interface**
- **Interfaces directly with industry standard memories**
- **Single bit serial I/O path**
- **Seven 8 bit addressable general purpose registers**
- **Vectored interrupt**
- **Subroutine return address stack**
- **2.4μs machine cycle time (2650A)**
- **1.5μs machine cycle time (2650A-1)**

PIN CONFIGURATION



MICROPROCESSOR BLOCK DIAGRAM

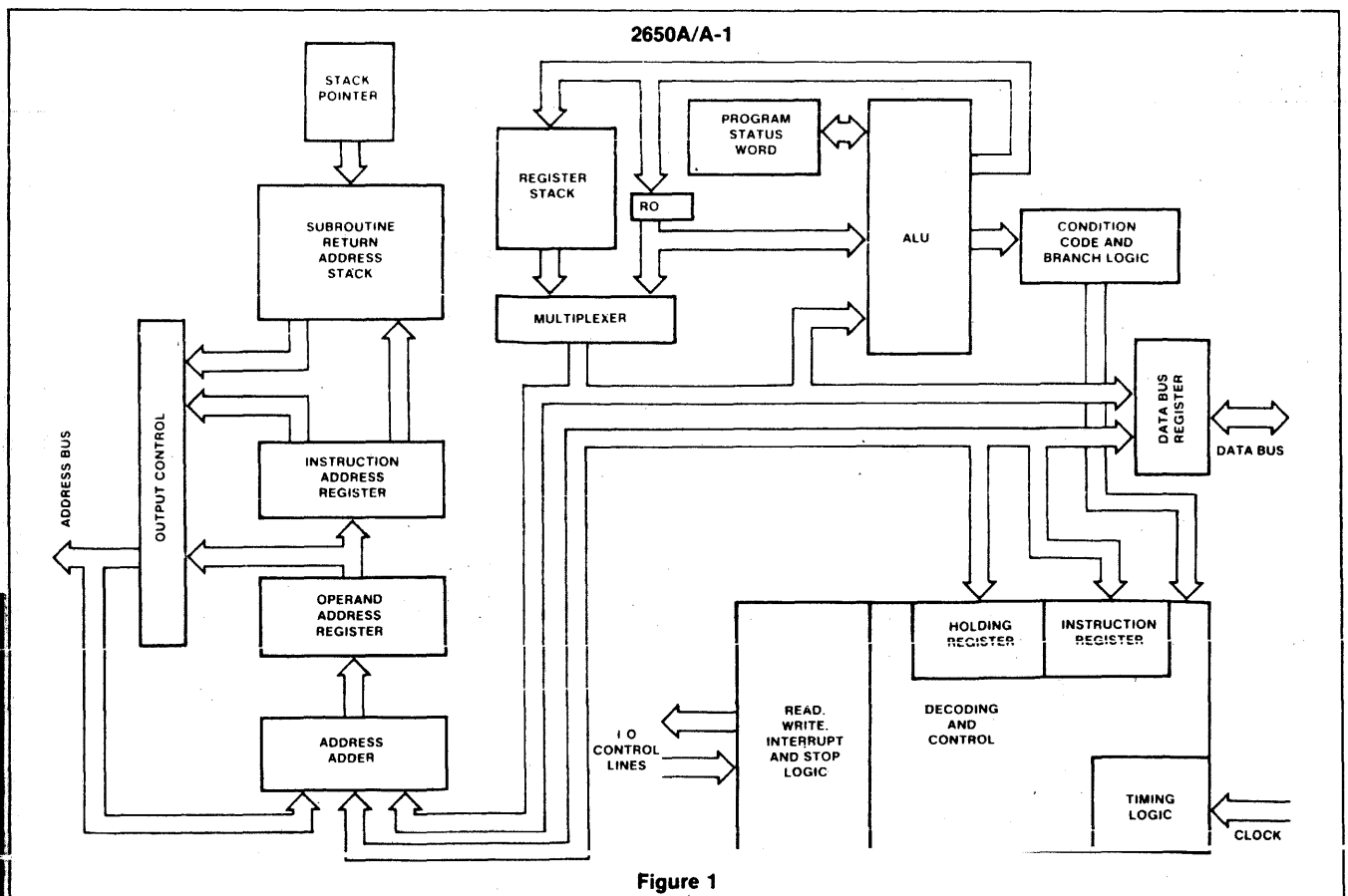


Figure 1

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PRELIMINARY SPECIFICATION

FUNCTIONAL DESCRIPTION

The 2650 series processors are general purpose, single chip, fixed instruction set, parallel 8-bit binary processors. A general purpose processor can perform any data manipulations through execution of a stored sequence of machine instructions. The processor has been designed to closely resemble conventional binary computers, but executes variable length instructions of one to three bytes in length.

The 2650 series contains a total of seven general purpose registers, each eight bits long. They may be used as source or destination for arithmetic operations, as index registers, and for I/O transfers.

The processor can address up to 32,768 bytes of memory in four pages of 8,192 bytes each. The processor instructions are one, two, or three bytes long, depending on the instruction. Variable length instructions tend to conserve memory space since a one-or-two byte instruction may often be used rather than a three byte instruction. The first byte of each instruction always specifies the operation to be performed and the addressing mode to be used. Most instructions use six of the first eight bits for this purpose, with the remaining two bits forming the register field. Some instructions use the full eight bits as an operation code.

The Data Bus and Address signals are tristate to provide convenience in system design. Memory and I/O interface signals are asynchronous so that Direct Memory Access (DMA) and multiprocessor operations are easy to implement.

The block diagram for the 2650 series (Figure 1) shows the major internal components and the data paths that interconnect them. In order for the processor to execute an instruction, it performs the following general steps:

1. The Instruction Address Register provides an address for memory.
2. The first byte of an instruction is fetched from memory and stored in the Instruction Register.
3. The Instruction Register is decoded to determine the type of instruction and the addressing mode.
4. If an operand from memory is required, the operand address is resolved and loaded into the Operand Address Register.
5. The operand is fetched from memory and the operation is executed.
6. The first byte of the next instruction is fetched.

The Instruction Register (IR) holds the first byte of each instruction and directs the subsequent operations required to execute each instruction. The IR contents are decoded and used in conjunction with the timing information to control the activation and sequencing of all the other elements on the chip. The Holding Register is used in some multiple-byte instructions to contain further instruction information and partial absolute addresses.

The Arithmetic Logic Unit (ALU) is used to perform all of the data manipulation operations, including Load, Store, Add, Subtract, And, Inclusive Or, Exclusive Or, Compare, Rotate, Increment and Decrement. It contains and controls the Carry bit, the Overflow bit, the Interdigit Carry and the Condition Code Register.

The Register Stack contains six registers that are organized into two banks of three registers each. The Register Select bit picks one of the two banks to be accessed by instructions. In order to accommodate the register-to register instructions, register zero (R0) is outside the array. Thus, register zero is always available along with one set of three registers.

The Address Adder is used to increment the instruction address and to calculate relative and indexed addresses.

The Instruction Address Register holds the address of the next instruction byte to be accessed. The Operand Address Register stores operand addresses and sometimes contains intermediate results during effective address calculations.

The Return Address Stack (RAS) is a Last In, First Out (LIFO) storage which receives the return address whenever a Branch-to-Subroutine instruction is executed. When a Return instruction is executed, the RAS provides the last return address for the processor's IAR. The stack contains eight levels of storage so that subroutines may be nested up to eight levels deep. The Stack Pointer is a three bit wraparound counter that indicates the next available level in the stack. It always points to the current address.

PROGRAM STATUS WORD

The Program Status Word (PSW) is a major feature of the 2650 which greatly increases its flexibility and processing power. The PSW is a special purpose register within the processor that contains status and control bits.

It is divided into two bytes called the Program Status Upper (PSU) and Program Status Lower (PSL). The PSW bits may be tested, loaded, stored, preset, or cleared using the instructions which affect the PSW. The bits are utilized as shown in Table 1.

PSU0,1,2	SP	Pointer for the Return Address Stack.
PSU3,4		Not used. These bits are always zero.
PSU5	II	Used to inhibit recognition of additional Interrupts.
PSU6	F	Flag is a latch directly driving the flag output.
PSU7	S	Sense equals the state of the sense input.
PSL0	C	Carry stores any carry from the high-order bit of ALU.
PSL1	COM	Compare determines if a logical or arithmetic comparison is to be made.
PSL2	OVF	Overflow is set if a two's complement overflow occurs.
PSL3	WC	With Carry determines if the carry is used in arithmetic and rotate instructions.
PSL4	RS	Register Select identifies which bank of 3 GP registers is being used.
PSL5	IDC	Inter Digit Carry stores the bit-3 to-bit-4 carry in arithmetic operations.
PSL6,7	CC	Condition Code is affected by compare, test and arithmetic instructions.

PSU

7	6	5	4	3	2	1	0
S	F	II			SP2	SP1	SP0

S	Sense
F	Flag
II	Interrupt Inhibit
SP2	Stack Pointer Two
SP1	Stack Pointer One
SP0	Stack Pointer Zero

PSL

7	6	5	4	3	2	1	0
CC1	CC0	IDC	RS	WC	OVF	COM	C

CC1	Condition Code One
CC0	Condition Code Zero
IDC	Interdigit Carry
RS	Register Bank Select
WC	With/Without Carry
OVF	Overflow
COM	Logical/Arithmetic Compare
C	Carry/Borrow

Table 1 PROGRAM STATUS WORD

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2651-I

DESCRIPTION

The Signetics 2651 PCI is a universal synchronous/asychronous data communications controller chip designed for microcomputer systems. It interfaces directly to the Signetics 2650 microprocessor and may be used in a polled or interrupt driven system environment. The 2651 accepts programmed instructions from the microprocessor and supports many serial data communication disciplines, synchronous and asynchronous, in the full or half-duplex mode.

The PCI serializes parallel data characters received from the microprocessor for transmission. Simultaneously, it can receive serial data and convert it into parallel data characters for input to the microcomputer.

The 2651 contains a baud rate generator which can be programmed to either accept an external clock or to generate internal transmit or receive clocks. Sixteen different baud rates can be selected under program control when operating in the internal clock mode.

The PCI is constructed using Signetics n-channel silicon gate depletion load technology and is packaged in a 28-pin DIP.

FEATURES

- **Synchronous operation**
  - **5 to 8-bit characters**
  - **Single or double SYN operation**
  - **Internal character synchronization**
  - **Transparent or non-transparent mode**
  - **Automatic SYN or DLE-SYN insertion**
  - **SYN or DLE stripping**
  - **Odd, even, or no parity**
  - **Local or remote maintenance loop back mode**
  - **Baud rate: dc to 1M bps (1X clock)**
- **Asynchronous operation**
  - **5 to 8-bit characters**
  - **1, 1 1/2 or 2 stop bits**
  - **Odd, even, or no parity**
  - **Parity, overrun and framing error detection**
  - **Line break detection and generation**
  - **False start bit detection**
  - **Automatic serial echo mode**
  - **Local or remote maintenance loop back mode**
  - **Baud rate: dc to 1M bps (1X clock)**
    - **dc to 62.5K bps (16X clock)**
    - **dc to 15.625K bps (64X clock)**

OTHER FEATURES

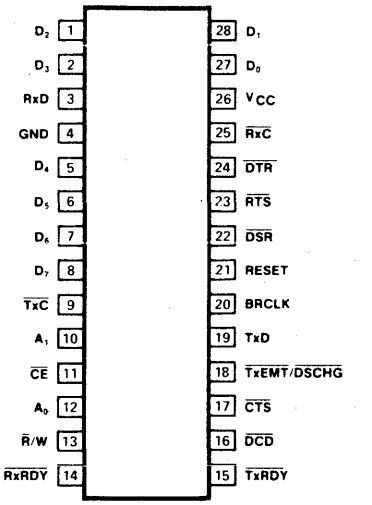
- **Internal or external baud rate clock**
- **16 internal rates-50 to 19,200 baud**
- **Double buffered transmitter and receiver**
- **Full or half duplex operation**
- **Fully compatible with 2650 CPU**
- **TTL compatible inputs and outputs**
- **Single 5V power supply**
- **No system clock required**
- **28-pin dual in-line package**

APPLICATIONS

- **Intelligent terminals**
- **Network processors**
- **Front end processors**
- **Remote data concentrators**
- **Computer to computer links**
- **Serial peripherals**

PIN CONFIGURATION

IQA PACKAGE



PIN DESIGNATION

PIN NO.	SYMBOL	NAME AND FUNCTION	TYPE
27,28,1,2, 5-8	D_0-D_7	8-bit data bus	I/O
21	RESET	Reset	I
12,10	A_0-A_1	Internal register select lines	I
13	$\overline{R}/W$	Read or write command	I
11	$\overline{CE}$	Chip enable input	I
22	$\overline{DSR}$	Data set ready	I
24	$\overline{DTR}$	Data terminal ready	O
23	$\overline{RTS}$	Request to send	O
17	$\overline{CTS}$	Clear to send	I
16	$\overline{DCD}$	Data carrier detected	I
18	$\overline{TxEMT/DSCHG}$	Transmitter empty or data set change	O
9	$\overline{TxC}$	Transmitter clock	I/O
25	$\overline{RxC}$	Receiver clock	I/O
19	TxD	Transmitter data	O
3	RxD	Receiver data	I
15	$\overline{TxRDY}$	Transmitter ready	O
14	$\overline{RxRDY}$	Receiver ready	O
20	BRCLK	Baud rate generator clock	I
26	V_{CC}	+5V supply	I
4	GND	Ground	I

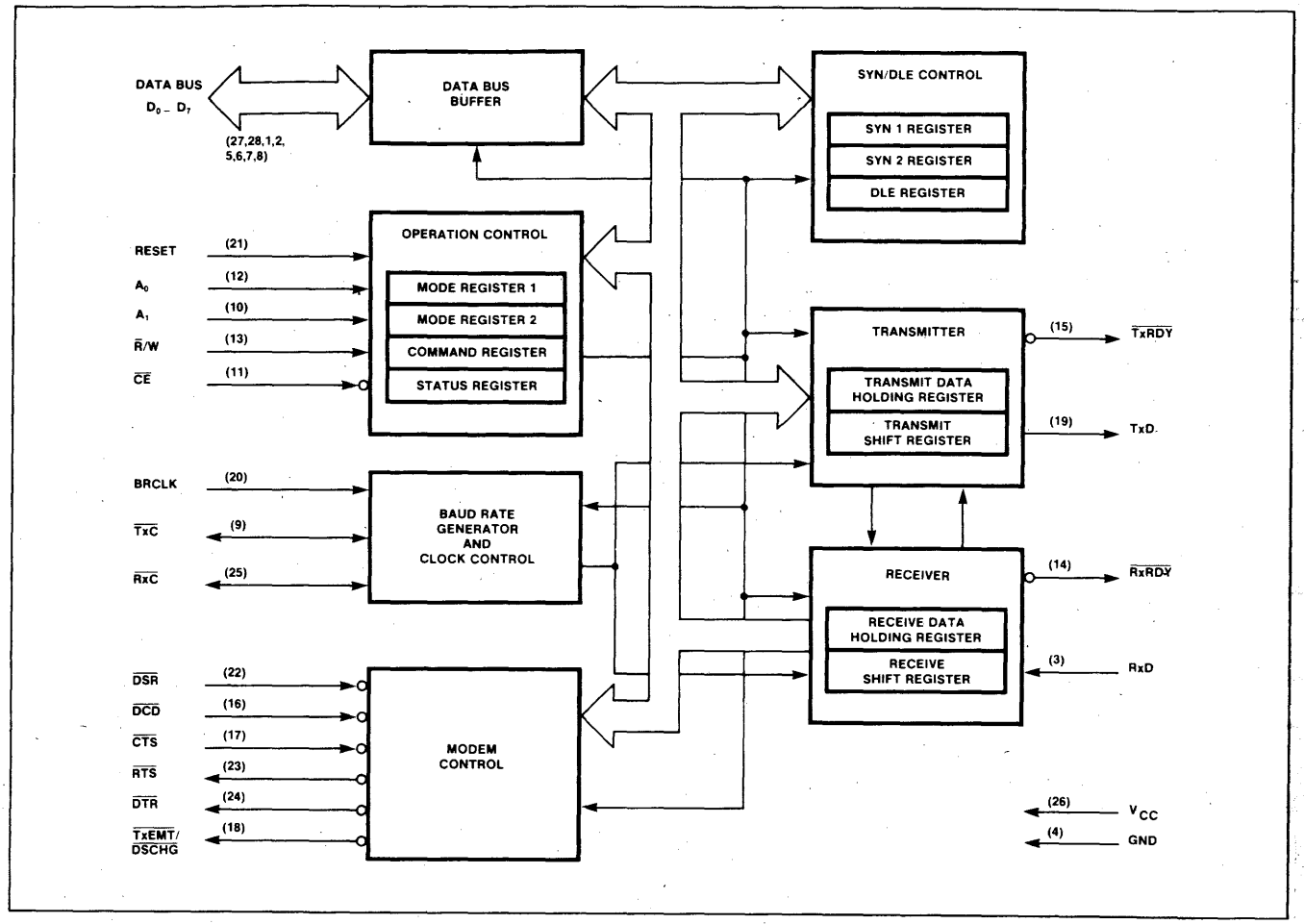
ABSOLUTE MAXIMUM RATINGS[1]

PARAMETER	RATING	UNIT
Operating ambient temperature[2]	0 to +70	°C
Storage temperature	-65 to +150	°C
All voltages with respect to ground[3]	-0.5 to +6.0	V

NOTES: 1, 2, 3—SEE PAGE 11

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BLOCK DIAGRAM



BLOCK DIAGRAM

The PCI consists of six major sections. These are the transmitter, receiver, timing, operation control, modem control and SYN/DLE control. These sections communicate with each other via an internal data bus and an internal control bus. The internal data bus interfaces to the microprocessor data bus via a data bus buffer.

Operation Control

This functional block stores configuration and operation commands from the CPU and generates appropriate signals to various internal sections to control the overall device operation. It contains read and write circuits to permit communications with the microprocessor via the data bus and contains Mode Registers 1 and 2, the Command Register, and the Status Register. Details of register addressing and protocol are presented in the PCI Programming section of this data sheet.

Timing

The PCI contains a Baud Rate Generator (BRG) which is programmable to accept external transmit or receive clocks or to divide an external clock to perform data communications. The unit can generate 16 commonly used baud rates, any one of which can be selected for full duplex operation. See Table 1.

Receiver

The Receiver accepts serial data on the RxD pin, converts this serial input to parallel format, checks for bits or characters that are unique to the communication technique and sends an "assembled" character to the CPU.

Transmitter

The Transmitter accepts parallel data from the CPU, converts it to a serial bit stream, inserts the appropriate characters or bits (based on the communication technique) and outputs a composite serial stream of data on the TxD output pin.

Modem Control

The modem control section provides interfacing for three input signals and three output signals used for "handshaking" and status indication between the CPU and a modem.

SYN/DLE Control

This section contains control circuitry and three 8-bit registers storing the SYN1, SYN2, and DLE characters provided by the CPU. These registers are used in the synchronous mode of operation to provide the characters required for synchronization, idle fill and data transparency.

DESCRIPTION

The 2652 Multi-Protocol Communications Controller (MPCC) is a monolithic n-channel MOS LSI circuit that formats, transmits and receives synchronous serial data while supporting bit-oriented or byte control protocols. The chip is TTL compatible, operates from a single +5V supply, and can interface to a processor with an 8 or 16-bit bidirectional data bus.

FEATURES

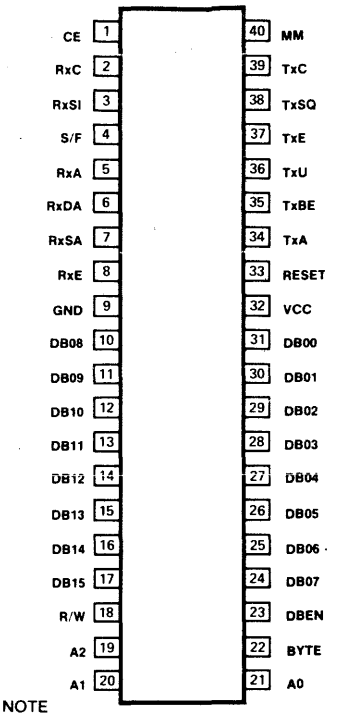
- DC to 1Mbps data rate, 2652-1 to 2Mbps
- Protocol management
  Bit-oriented protocols (BOP): SDLC, ADCCP, HDLC
  Byte-control protocols (BCP): BI-SYNC, DDCMP, limited BISYNC
- Programmable operation
  8 or 16-bit tri-state data bus
  Protocol selection—BOP or BCP
  Error control—CRC or VRC or no error check
  Character length—1 to 8 bits for BOP or 5 to 8 bits for BCP
  SYNC or secondary station address comparison for BCP-BOP
  Idle transmission of SYNC/FLAG or MARK for BCP-BOP
- Automatic detection and generation of special BOP control sequences, i.e., FLAG, ABORT, GA
- Zero insertion and deletion for BOP
- Short character detection for last BOP data character (will not overrun)
- SYNC generation, detection, and stripping for BCP
- Maintenance Mode for self-testing
- Common parameter control registers
- Independent status and data registers for receive and transmit
- Status indicator signals can be used as CPU interrupts
- TTL compatible
- 40-pin package
- Single +5V supply

APPLICATIONS

- Intelligent terminals
- Line controllers
- Network processors
- Front end communications
- Remote data concentrators
- Communication test equipment
- Computer to computer links

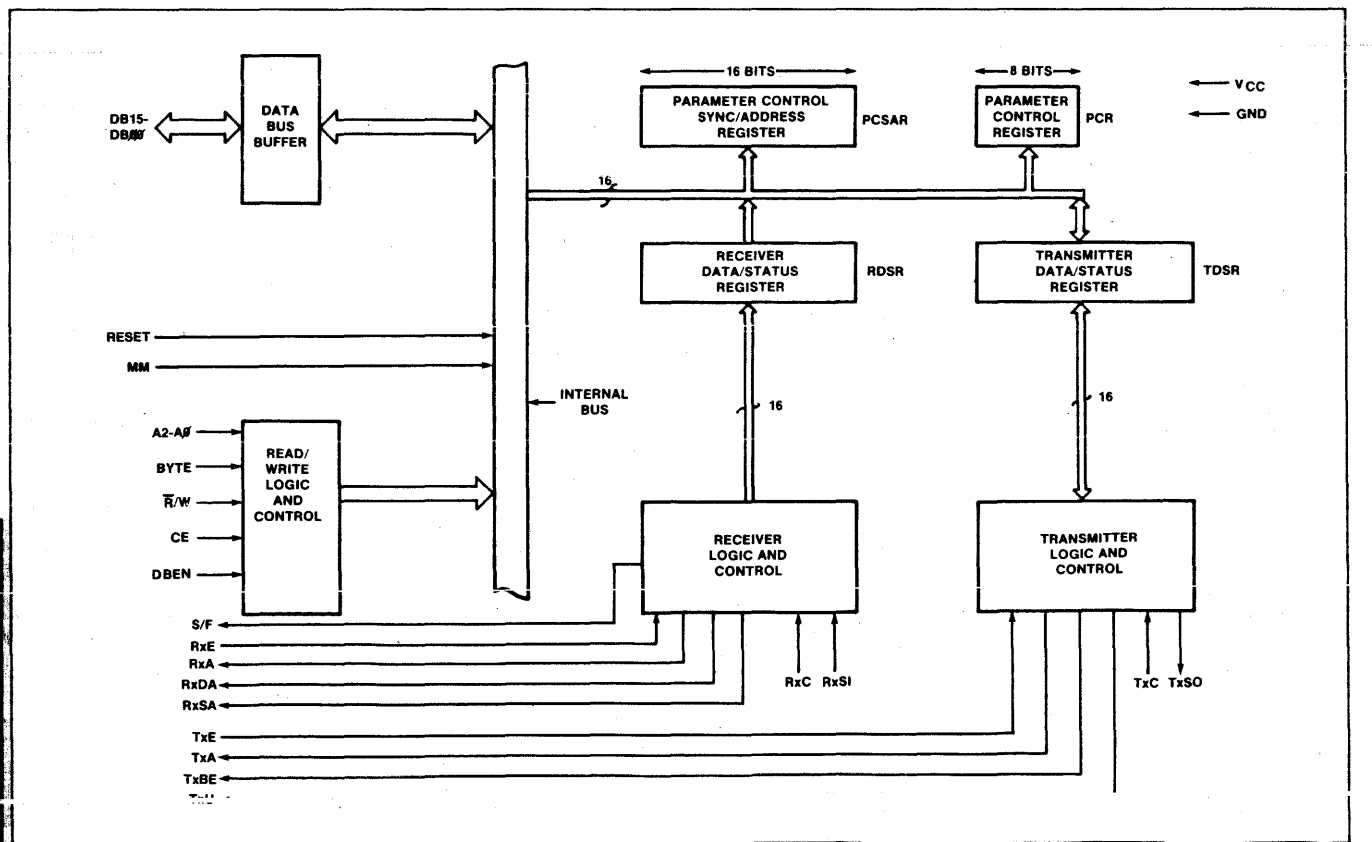
PIN CONFIGURATION

IWA PACKAGE



NOTE
00 is least significant bit, highest number (that is, DB15, A2) is most significant bit.

BLOCK DIAGRAM



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PIN DESIGNATION

MNEMONIC	PIN NO.	TYPE	NAME AND FUNCTION
DB15-DB00	17-10 24-31	I/O	**Data Bus:** DB07-DB00 contain bidirectional data while DB15-DB08 contain control and status information to or from the processor. Corresponding bits of the high and low order bytes can be WIRE OR'ed onto an 8-bit data bus.
A2-A0	19-21	I	**Address Bus:** A2-A0 select internal registers. The four 16-bit registers can be addressed on a word or byte basis. See Register Address section.
BYTE	22	I	**Byte:** Single byte (8 bit) data bus transfers are specified when this input is high. A low level specifies 16 bit data bus transfers.
CE	1	I	**Chip Enable:** A high input permits a data bus operation when DBEN is activated.
$\overline{R}$/W	18	I	**Read/Write:** $\overline{R}$/W controls the direction of data bus transfer. When high, the data is to be loaded into the addressed register. A low input causes the contents of the addressed register to be presented on the data bus.
DBEN	23	I	**Data Bus Enable:** After A2-A0, CE, BYTE and $\overline{R}$/W are set up, DBEN may be strobed. During a read, the tri-state data bus (DB) is enabled with information for the processor. During a write, the stable data is loaded into the addressed register and TxBE will be reset if TDSR was addressed.
RESET	33	I	**Reset:** A high level initializes all internal registers (to zero) and timing.
MM	40	I	**Maintenance Mode:** MM internally gates TxSO back to RxSI and $\overline{TxC}$ to RxC for off line diagnostic purposes. The RxC input is disabled when MM is asserted.
RxE	8	I	**Receiver Enable:** A high level input permits the processing of RxSI data. A low level disables the receiver logic and initializes all receiver registers and timing.
RxA	5	O	**Receiver Active:** RxA is asserted when the first data character of a message is ready for the processor. In the BOP mode this character is the address. The received address must match the secondary station address if the MPCC is a secondary station. In BCP mode, if strip-SYNC ($PCSAR_{13}$) is set, the first non-SYNC character is the first data character; if strip-SYNC is zero, the character following the second SYNC is the first data character. In the BOP mode, the closing FLAG resets RxA. In the BCP mode, RxA is reset by a low level at RxE.
RxDA*	6	O	**Receiver Data Available:** RxDA is asserted when an assembled character is in $RDSR_L$ and is ready to be presented to the processor. This output is reset when $RDSR_L$ is read.
RxC	2	I	**Receiver Clock:** RxC(1X) provides timing for the receiver logic. The positive going edge shifts serial data into the RxSR from RxSI.
S/F	4	O	**SYNC/FLAG:** S/F is asserted for one RxC clock time when a SYNC or FLAG character is detected.
RxSA*	7	O	**Receiver Status Available:** RxSA is asserted when there is a zero to one transition of any bit in $RDSR_H$ except for RSOM. It is cleared when $RDSR_H$ is read.
RxSI	3	I	**Receiver Serial Input:** RxSI is the received serial data. Mark = '1', space = '0'.
TxE	37	I	**Transmitter Enable:** A high level input enables the transmitter data path between $TDSR_L$ and TxSO. At the end of a message, a low level input causes TxSO = 1 (mark) and TxA = 0 after the closing FLAG (BOP) or last character (BCP) is output on TxSO.
TxA	34	O	**Transmitter Active:** TxA is asserted when TxE is high and TSOM ($TDSR_8$) is set. This output will reset when TxE is low and the closing FLAG (BOP) or last character (BCP) has been output on TxSO.
TxBE*	35	O	**Transmitter Buffer Empty:** TxBE is asserted when the TDSR is ready to be loaded with new control information or data. The processor should respond by loading the TDSR which resets TxBE.
TxU*	36	O	**Transmitter Underrun:** TxU is asserted during a transmit sequence when the service of TxBE has been delayed for one character time. This indicates the processor is not keeping up with the transmitter. Line fill depends on $PCSAR_{11}$. TxU is reset by RESET or setting of TSOM ($TDSR_8$). ($TDSR_8$).
TxC	39	I	**Transmitter Clock:** TxC (1X) provides timing for the transmitter logic. The positive going edge shifts data out of the TxSR to TxSO.
TxSO	38	O	**Transmitter Serial Output.** TxSO is the transmitted serial data. Mark = '1', space = '0'.
V_{CC}	32	I	**+5V:** Power supply.
GND	9	I	**Ground:** 0V reference ground.

*Indicates possible interrupt signal.

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DESCRIPTION

The 2655 Programmable Peripheral Interface (PPI) is a general purpose I/O component designed for microcomputer systems. It consists of three ports (24 I/O pins) which can be individually programmed to function as input, output or bidirectional ports. Interface with a microprocessor is via an 8-bit bidirectional data bus. Although designed primarily for use in 2650-based microcomputer systems, the 2655 can be easily interfaced to other microprocessors.

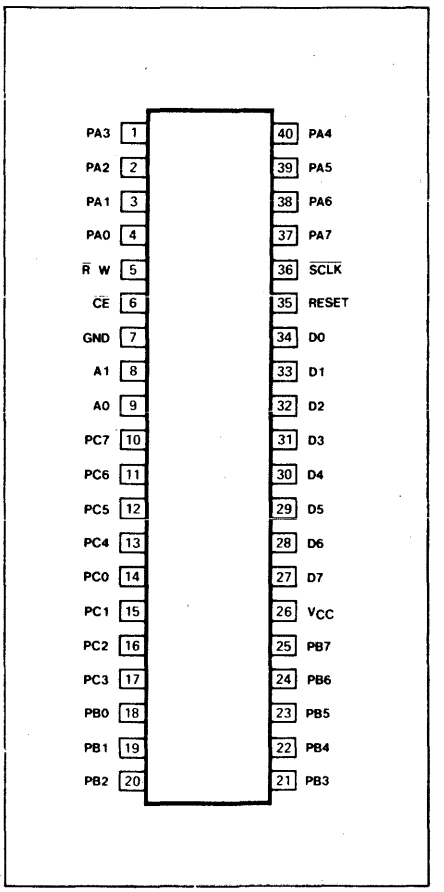
The PPI ports can be programmed to operate in one or more of seven operational modes: Static I/O, Strobed Input, Strobed Output, Strobed Bidirectional, Serial Input, Serial Output and Timer. The 2655 is fabricated using N-channel silicon gate technology and is packaged in a 40-pin DIP.

PIN DESIGNATION

PIN NO.	MNEMONIC	TYPE	NAME & FUNCTION
27-34	D7-D0	I/O	**Data Bus:** 8-bit 3-state, bidirectional data bus used for all data and command transfers.
35	RESET	I	**RESET:** When high, clears all internal registers. Clears Port A, B and C latches to zero and sets operating mode to Static I/O mode. An automatic power-on reset circuit is also provided.
8,9	A1,A0	I	**Address Bus:** A1, A0 select internal PPI registers. Select control or data words to be placed on the data bus. Used in conjunction with $\overline{R}$/W line.
5	$\overline{R}$/W	I	**Read/Write:** When low, gates the selected register to the data bus. When high, gates the contents of the data bus into the selected register. An address line may be used for this function if the CPU used does not provide a $\overline{R}$/W output.
6	$\overline{CE}$	I	**Chip Enable:** When low, indicates that control and data lines to the PPI are valid. Used as the timing signal for read/write operations.
36	$\overline{SCLK}$	I	**Serial Clock:** Provides a clock for the parallel to serial or serial to parallel conversion modes.
37-40 1-4	PA7-PA0	I/O	**Port A:** An 8-bit 3-stateable omni-port.*
25-18	PB7-PB0	I/O	**Port B:** An 8-bit omni-port which has serial I/O capability. Serial data is double buffered. Port B also contains a 16-bit binary timer, which can operate simultaneously with the serial I/O capability.
10-13 17-14	PC7-PC0	I/O	**Port C:** An 8-bit omni-port. Port C bits are also used as control and status signals for Ports A and B.
26	V_{CC}	I	**Power Supply:** +5V
7	GND	I	**Ground:**

*NOTE
See Omni-Port description is static I/O mode description.

PIN CONFIGURATION



FEATURES

- **Seven selectable operating modes**
- **Three ports with 24 programmable I/O pins**
- **Completely TTL compatible**
- **Three MHz programmable timer or event counter**
- **Direct bit set reset capability**
- **300 ns port read/write access time**

FUNCTIONAL DESCRIPTION

The block diagram illustrates the major internal components of the PPI.

Data Bus Buffer

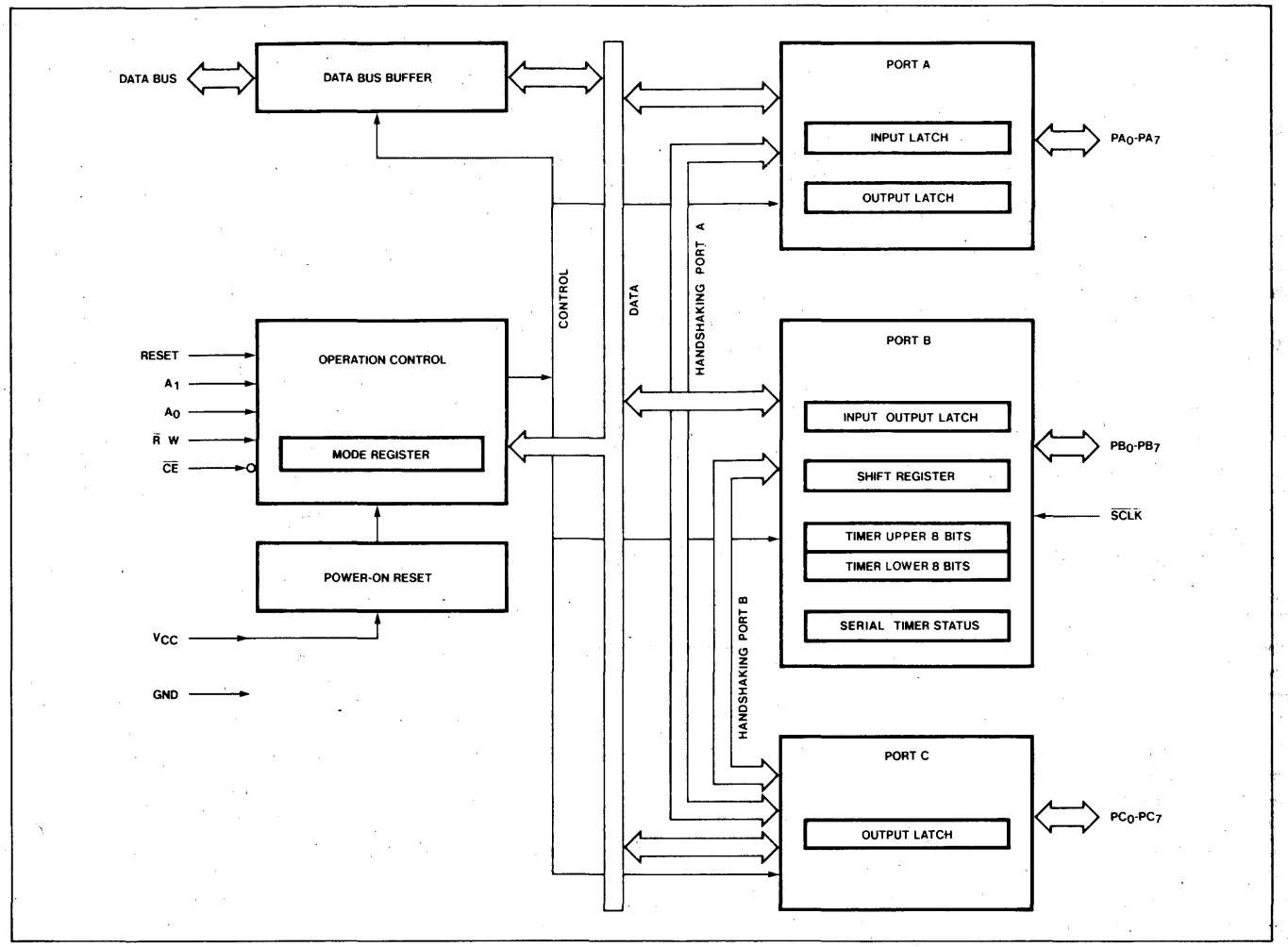
Three-state, bidirectional 8-bit buffer. All command and data transfers between the PPI and the CPU are accomplished via this buffer.

Operation Control

Access to the PPI is controlled by chip enable ($\overline{CE}$) and access to the various ports and registers is selected by address lines A0 and A1. The read/write ($\overline{R}$/W) signal selects the direction of the data flow between the PPI and the CPU. Table 1 specifies the inputs required to access the various internal registers.

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BLOCK DIAGRAM



The modes of operation of the PPI ports are selected by a control byte stored in the mode register. See the Mode Selection section of this specification.

Ports A, B and C

The 2655 contains three 8-bit ports, each of which may be configured to operate in a variety of data transfer modes by the system software.

PORT A: contains one 8-bit data output latch and one 8-bit data input latch. The port operates in either static I/O, strobed input, strobed output, or bidirectional I/O Mode.

PORT B: contains one 8-bit data input/output latch, one 8-bit shift register, one 16-bit binary counter (timer upper and lower 8 bits) and a serial/timer status register. The port operates in either static I/O, strobed input, strobed output, serial input, serial output, or timer mode. The timer mode may operate in conjunction with one of the serial modes.

PORT C: contains one 8-bit data output latch. The port operates in static I/O mode only. Port C bits are also used as control and status bits for ports A and B in certain modes of operation. A data selector selects the appropriate internal data path for the purpose of providing handshaking signals to and from Port C pins when used as control or status bits.

$\overline{CE}$	A1	A0	$\overline{R}/W$	FUNCTION
0	0	0	0	Read port A register
0	0	0	1	Write port A register
0	0	1	0	Read port B register
0	0	1	1	Write port B register
0	1	0	0	Read port C register
0	1	0	1	Write port C register
0	1	1	0	Read serial/timer status
0	1	1	1	Write mode register or bit set/reset
1	X	X	X	Data bus 3-state

Table 1 PPI REGISTER ADDRESSING

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PRELIMINARY SPECIFICATION

8048 8-BIT MICROCOMPUTER With Mask Programmable ROM
8748 8-BIT MICROCOMPUTER With Field Programmable Erasable EPROM
8035L 8-BIT MICROCOMPUTER With External ROM or PROM

DESCRIPTION

The 8048 family of single chip 8-bit microcomputers are fabricated using the Signetics NMOS silicon gate process.

To reduce development and production costs and yet provide maximum flexibility, three interchangeable (pin compatible) versions of this single chip microcomputer are available:

- The 8748 with user-programmable and erasable EPROM, for prototype and pre-production systems.
- The 8048 with factory-programmable mask ROM for low-cost, high-volume production.
- The 8035L without program memory for use with external EPROM/ROM.

The 8048 family processors are designed to be efficient control processors as well as arithmetic processors. They provide an instruction set which allows the user to directly set and reset individual lines within its I/O ports as well as test individual bits within the accumulator. A large variety of branch and table look-up instructions make these processors very efficient in implementing standard logic functions. Also, special attention has been given to code efficiency. Over 70% of the instructions are a single byte long and all others are only two bytes long. This means many functions requiring 1.5K to 2.0K bytes in other computers may very well be compressed into the 1K words resident in the 8048.

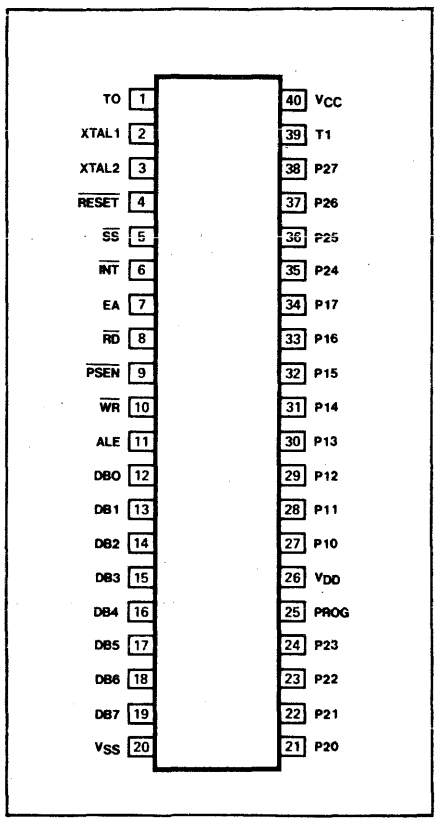
An on-chip 8-bit counter is provided, which can, under program control, count either internal clock pulses (÷32) or external events. The counter can be programmed to cause an interrupt to be applied to the microcomputer.

Program and data memories can be expanded using low-cost, readily available, standard devices. Input/output capabilities can be expanded using standard devices or the 8243 I/O Expander of the 8048 family.

FEATURES

- **8-bit CPU, ROM, RAM, I/O in single package**
- **Interchangeable ROM/EPROM versions**
- **1Kx8 ROM/EPROM, 64x8 RAM, 27 I/O lines**
- **Internal counter/timer**
- **Internal oscillator, clock driver**
- **Single level interrupt: External or counter/timer**
- **17 internal registers: accumulator plus 16 addressable registers**
- **Over 90 instructions: 70% single byte**
- **All instructions: 1 or 2 cycles 2.5/5.0μs per cycle**
- **Easily exandable memory and I/O**
- **TTL compatible inputs and outputs**
- **Single 5V supply**
- **For low cost 28-Pin version see 8021 data sheet**

PIN CONFIGURATION



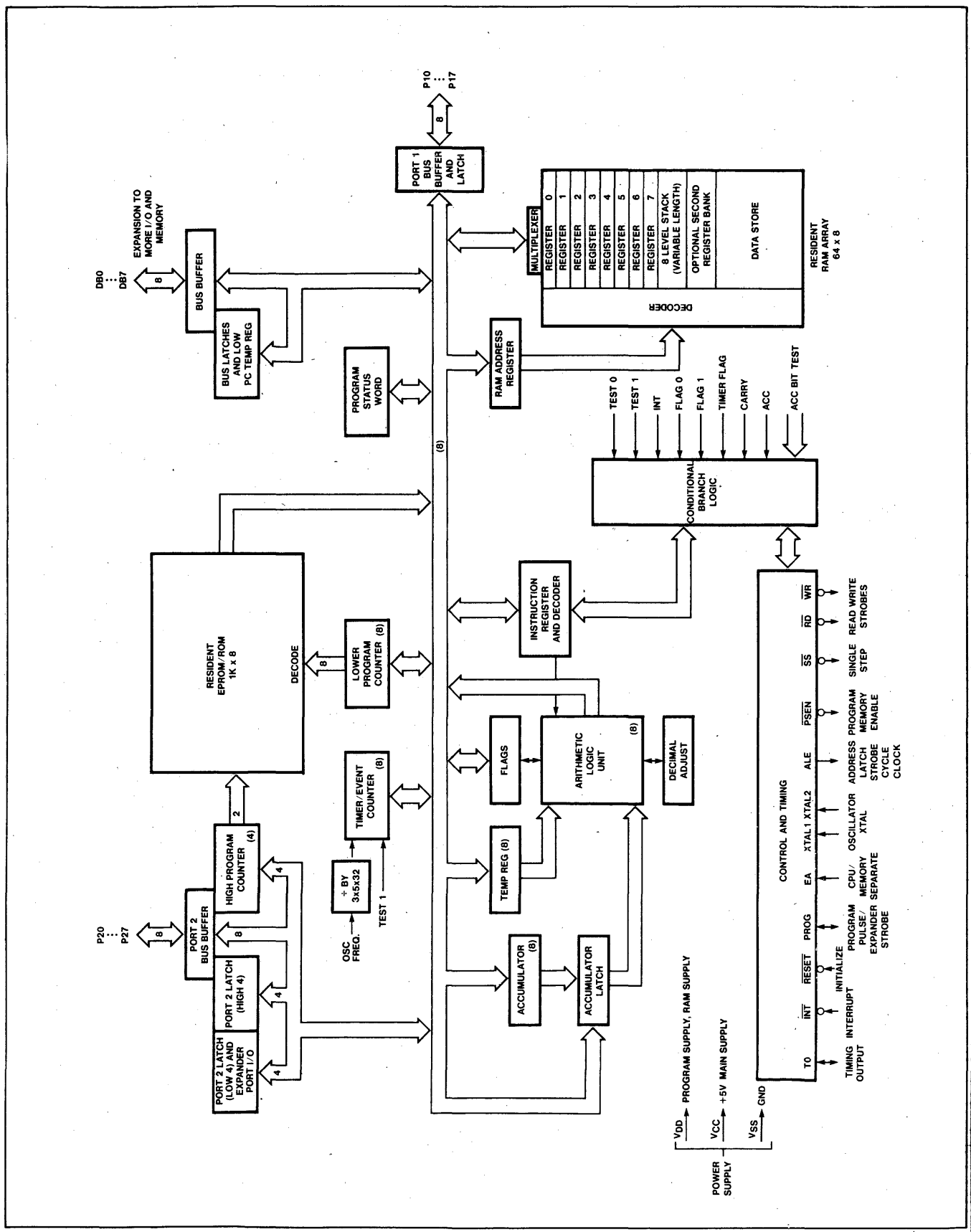
ORDERING CODE (All Device Types Operate over 0°C to 70°C Temperature Range)

	MASK PROGRAM ROM		FIELD PROGRAM EPROM		EXTERNAL ROM	
PACKAGES	2.5μs Cycle	5.0μs Cycle	2.5μs Cycle	5.0μs Cycle	2.5μs Cycle	5.0μs Cycle
Ceramic DIP	8048I	8048-8I	8748I	8748-8I	8035LI	8035L-8I
Plastic DIP	8048N	8048-8N			8035LN	8035-8N

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PRELIMINARY SPECIFICATION

MICROCOMPUTER BLOCK DIAGRAM



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MP8080A-I

DESCRIPTION

The MP8080A is an 8-bit microprocessor housed in a standard, 40-pin dual-in-line package. The chip, which is fabricated using N-channel silicon gate MOS technology, functions as the central processing unit (CPU) in Signetics' 8080 microcomputer family.

The MP8080A has a 16-bit address bus that is capable of addressing up to 65k bytes of memory and up to 256 input and 256 output devices. Data is routed to and from the MP8080A on a separate bidirectional 8-bit bus. This data bus is also Tri-State, making direct memory addressing (DMA) and multiprocessing applications possible. The MP8080A directly provides signals to control the interface to memory and I/O ports. All buses, including control, are TTL compatible.

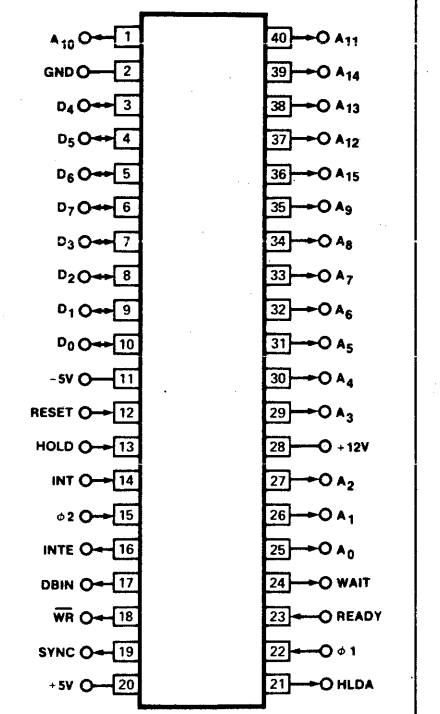
An asynchronous interrupt capability is included in the MP8080A to allow external signals to change the instruction sequence. The interrupting device may vector the program to a particular service routine location (or some other direct function) by specifying an interrupt instruction to be executed.

FEATURES

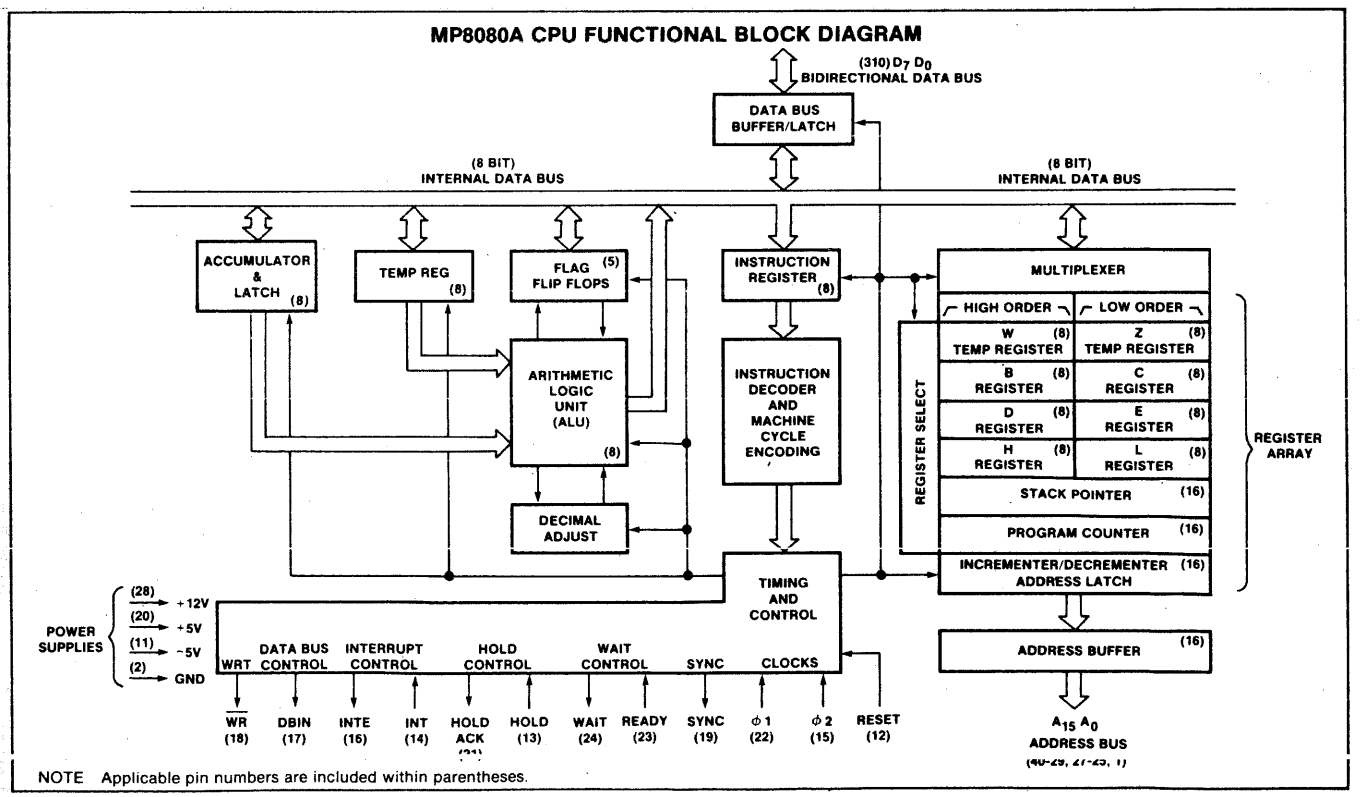
- **2μs instruction cycle**
- **Variable length instructions**
- **General purpose registers—six plus an accumulator**
- **Direct addressing up to 65k bytes**
- **Variable length stack accessed by 16-bit stack pointer**
- **Addresses 256 input and 256 output ports**
- **Provisions for vectored interrupts**
- **Tri-state bus for DMA and multiprocessing capability**
- **Tri-state TTL drive capabilities for address and data buses**
- **Decimal arithmetic capability**
- **Multiple addressing modes**
  - **Direct**
  - **Register**
  - **Register indirect**
  - **Immediate**
- **Direct plug-in replacement for Intel MP8080A**

PIN CONFIGURATION

IWA PACKAGE



FUNCTIONAL BLOCK DIAGRAM



NOTE Applicable pin numbers are included within parentheses.

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PRELIMINARY SPECIFICATION

DESCRIPTION

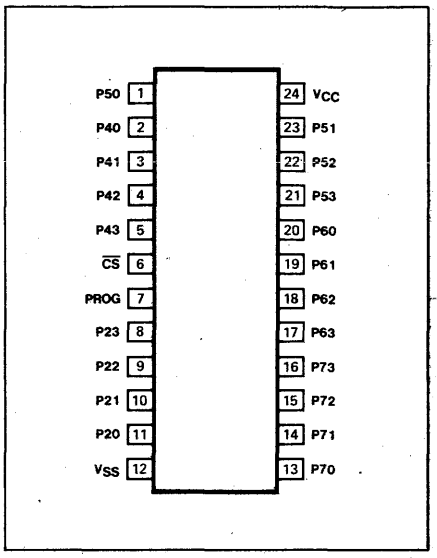
The 8243 is an input/output expander that provides an easy, low cost method of adding four 4-bit bidirectional, latched ports to 8048 and 8021 microcomputer based systems. Fabricated using the Signetics NMOS process, it features versatility, operation from a single 5 volt supply, and high current drive capability.

The data interface between the 8243 and the microcomputer is via the lower four bits of Port 2. Control is provided automatically by the PROG line when the MOVD P,A, MOVD A,P, ANLD P,A, or ORLD P,A instructions are executed.

FEATURES

- **Low cost**
- **Single 5V supply**
- **High output current drive**
- **Direct interface to 8048 and 8021 family of microcomputers**
- **Four 4-bit I/O ports**
- **Chip Select input for easy expansion**

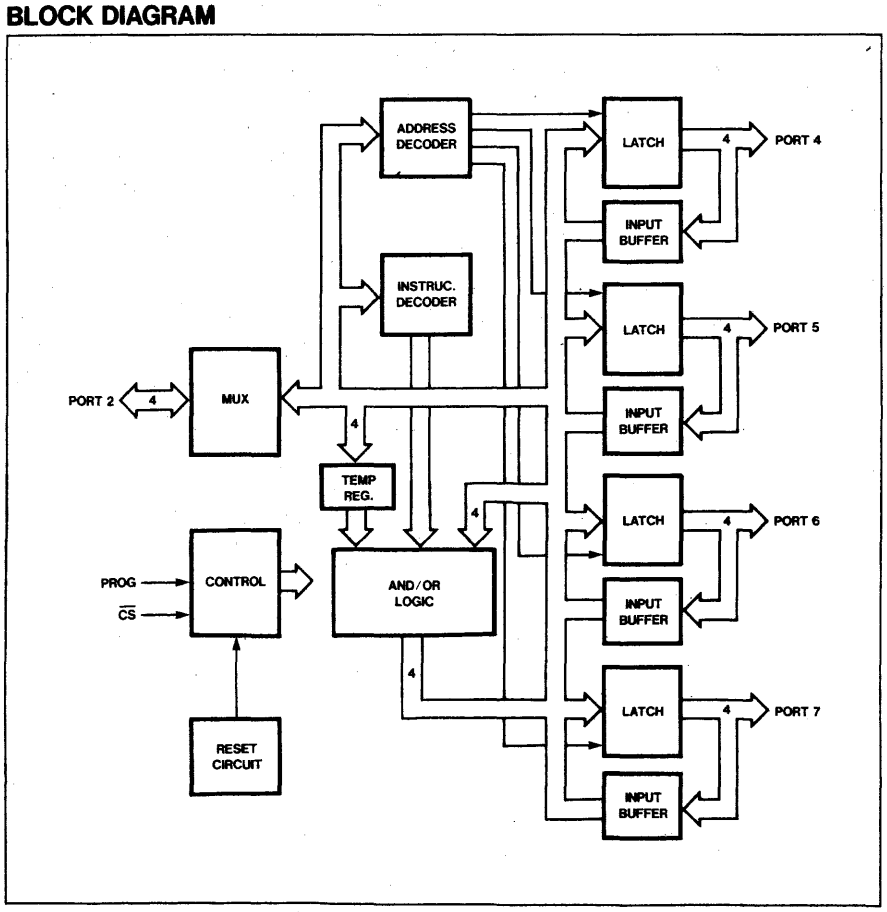
PIN CONFIGURATION



ORDERING CODE

PACKAGES	COMMERCIAL RANGES V_{CC} = 5V ± 10%, T_A = 0°C to 70°C
Ceramic DIP	MP8243I
Plastic DIP	MP8243N

BLOCK DIAGRAM



PIN DESIGNATION

SYMBOL & PIN NO.	NAME AND FUNCTION
PROG (7)	**Clock Input:** A high-to-low transition on PROG signifies that address and control are available on P20-P23, and a low-to-high transition signifies that data is available on P20-P23.
$\overline{CS}$ (6)	**Chip Select:** (active low) Input. A HIGH on $\overline{CS}$ inhibits any change of output or internal status.
P20-P23 (11-8)	**4-bit Bidirectional Port:** Contains the address and control bits on a high-to-low transition of PROG. During a low-to-high transition contains the data for a selected output port if a write operation, or the data from a selected port if a read operation.
P40-P43 (2-5) P50-P53 (23-21) P60-P63 (20-17) P70-P73 (13-16)	**Four 4-bit bidirectional I/O ports:** May be programmed to be input (during read), low impedance latched output (after write) or high impedance (after read). Data on pins P20-P23 may be directly written, ANDed or ORed with previous data.
V_{CC} (24)	**Power Supply:** +5 volts.
V_{SS} (12)	**Circuit ground.**

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ISP-8A/600-I

DESCRIPTION

SC/MP (Simple Cost-effective MicroProcessor) is a single-chip 8-bit microprocessor packaged in a standard, 40-pin, dual-in-line package.

N-channel, silicon gate, depletion mode standard-process technology ensures high performance, high reliability, and high producibility.

SC/MP is intended for use in general-purpose applications where cost per function is a most significant criterion. But cost efficiency is only a part of SC/MP's story. It goes on to include a variety of useful functions that are not even provided by some of the expensive microprocessors, like self-contained timing circuitry, 16-bit (65K) addressing capability, serial or parallel data-transfer capability and common memory/peripheral instructions. The built-in features in conjunction with the low initial cost describe what SC/MP really is—a microprocessor specifically designed to provide the simplest and most efficient solution to many application requirements.

APPLICATIONS

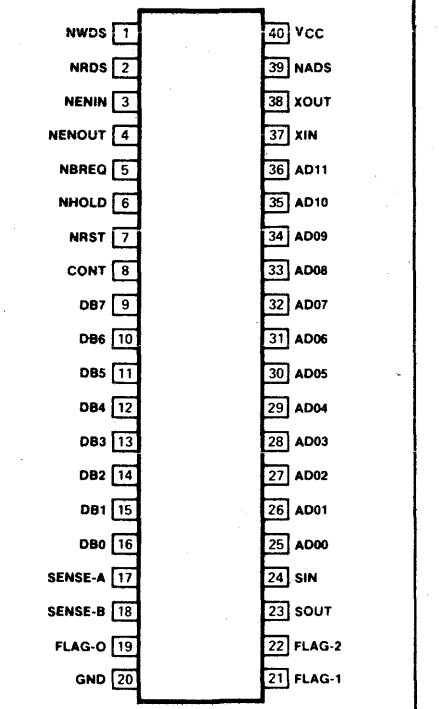
- **Test systems and instrumentation**
- **Machine tool control**
- **Small business machines**
- **Word processing systems**
- **Educational systems**
- **Multiprocessor systems**
- **Process controllers**
- **Terminals**
- **Traffic controls**
- **Laboratory controllers**
- **Sophisticated games**
- **Automotive**

FEATURES

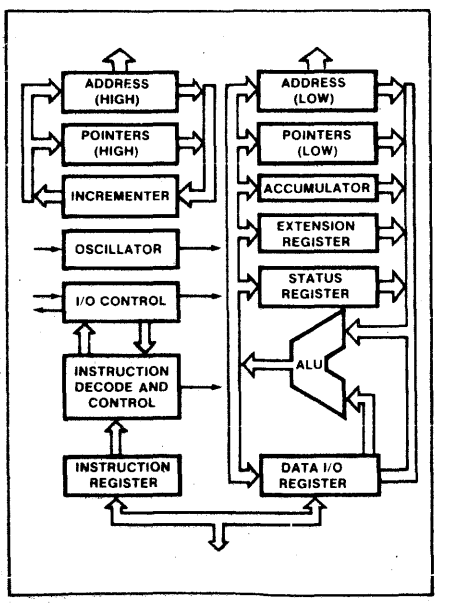
- **Simpler interfacing**
  - **Bidirectional Tri-state 8-bit data bus**
  - **TTL-compatible input/output interface**
- **Si-gate N-channel ion-implant process**
- **Direct Memory Access (DMA) and multiprocessor capabilities**
  - **Handshake bus-access control on chip**
- **Simplified programming**
  - **Multiple addressing modes—program-counter-relative, immediate data, indexed, auto-indexed, and implied**
- **Direct control output**
  - **Three user-accessible control-flag outputs**
- **Simpler I/O hardware**
  - **Separate serial-data input and output ports**
  - **Two sense inputs**
  - **Direct interfacing to standard memory parts**
- **Simplified timing hardware**
  - **On-chip clock generator**
- **Interface flexibility**
  - **Capability to interface with memories or peripherals of any speed**
- **Large system capability**
  - **Address capability to 65K bytes of memory**
- **Simplified power requirements**
  - **Single 5-volt supply**
  - **Low power**

PIN CONFIGURATION

IWA PACKAGE



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

	PARAMETER	RATING	UNIT
	Voltage at any pin	-0.5 to +7.0	V
T_A	Operating temperature range	0 to +70	°C
T_{STG}	Storage temperature range	-65 to +150	°C
	Lead temperature (solder, 10 sec)	+300	°C

*NOTE

Maximum ratings indicate limits beyond which damage may occur. Continuous operation at these limits is not intended and should be limited to those conditions specified under electrical characteristics.

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DESCRIPTION

The TWIN (TestWare Instrument) system, shown in the block diagram of Figure 1, consists of interdependent subsystems, each contributing to the total task of implementing user microprocessor applications from initial concept to actual hardware operation. The system closely resembles a general-purpose minicomputer during the initial stages of product development, and allows source programs to be entered, edited and assembled into object programs. Object programs may be executed simply as programs, or as part of a user's product emulation. When programs have been run and debugged to the user's satisfaction, the TWIN system is capable of programming PROM devices for inclusion in the user's prototype hardware.

The program development computer is configured using plug-in modules, each dedicated to a specific task within the system. Each module interacts with the others by use of a common bus structure. The major buses include a data bus, an address bus, and a control bus. The program development computer acts as the controller for the entire system, and performs the necessary functions of transferring data to and from system peripherals.

To facilitate system operation, a dual-drive floppy disk subsystem is provided in all TWIN configurations. This subsystem, with integral controller, stores user program "files" and allows retrieval of these files for operations by the editor and assembler. The Signetics Disk Operating System (SDOS) software is loaded from the disk system into the development computer. SDOS provides complete control over all portions of the TWIN system.

A CRT console is the standard device for entering user programs. It is equipped with a full ASCII keyboard for data entry and a CRT display to allow the operator to view the results of his program manipulations during editing, assembly, and debug operations. The display and keyboard can be separated for user convenience. An interface is provided for an ASR-33 teletypewriter, which can be used in place of the CRT console. An optional line printer provides hard copy output.

Other system I/O devices can be added to the system to enhance its capabilities. Physical interface to the system bus is accomplished by use of the optional General-Purpose I/O card. Addition of a peripheral device requires addition of its software driver to the TWIN operating system.

TWICE (TestWare In-Circuit Emulation) denotes hardware/software elements of the TWIN system that support the integration and check-out of the user's prototype product. A number of different TWICE operation modes support product development, integration, and production.

THE TWIN SYSTEM

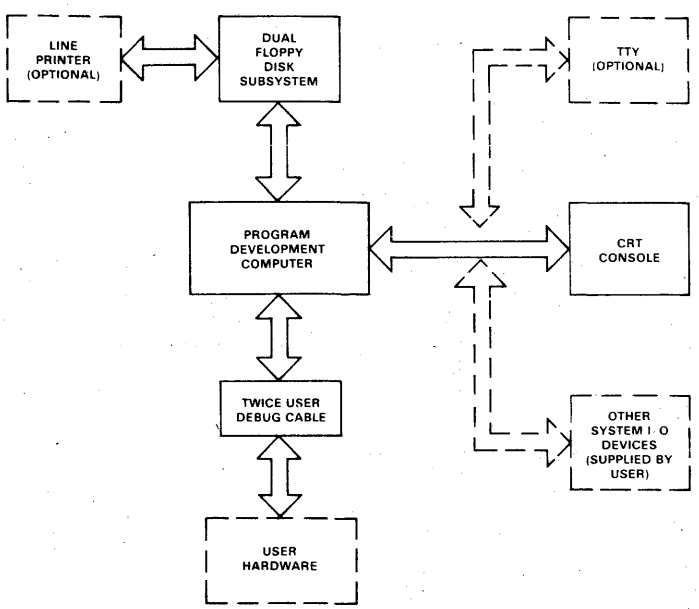


Figure 1

TWIN HARDWARE

The TWIN system is available in two configurations: the BASIC TWIN and the SUPER TWIN.

Basic TWIN Configuration

Program Development Computer consisting of:
- Master CPU—16K Master Memory
- Slave CPU—16K Slave Memory
- Debug Logic Card

TWICE Cable
Dual-Drive Floppy Disk Subsystem

Super TWIN Configuration

Basic TWIN configuration plus:
- 1702A PROM Program card
- 82S115 PROM Program card
- General-Purpose I/O Card

CRT Console
Line Printer

Program Development Computer

The Program Development Computer (PDC) is the principal subsystem of the TWIN. The PDC employs dual-processor architecture operating on a common bus structure.

The Master/Slave architectural concept provides the following features:

1. Protected operating system memory and I/O.
2. Complete user access to slave memory address space and I/O address space.
3. Operating system and Debug software are independent of user programs.
4. Use of future Slave processors by adding boards and supplying additional software only.
5. Multiple Slave CPUs of different types can be accommodated.
6. Debug and TWICE hardware.

The PDC can be divided into four distinct areas as shown in Figure 2.

1. The master CPU provides access to all support peripherals (Floppy Disk, Line Printer and CRT console). By way of the common bus, the slave side of the system can make requests of these system peripherals. In addition, via the General Purpose I/O Board, the user has the option of adding system peripherals on the master side.
2. The master CPU controls PROM programming by transferring data from the slave memory to the PROM sockets. Both erasable (1702A) and nonerasable (82S113) PROMs can be programmed through sockets controlled by the operating system.

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THE TWIN SYSTEM

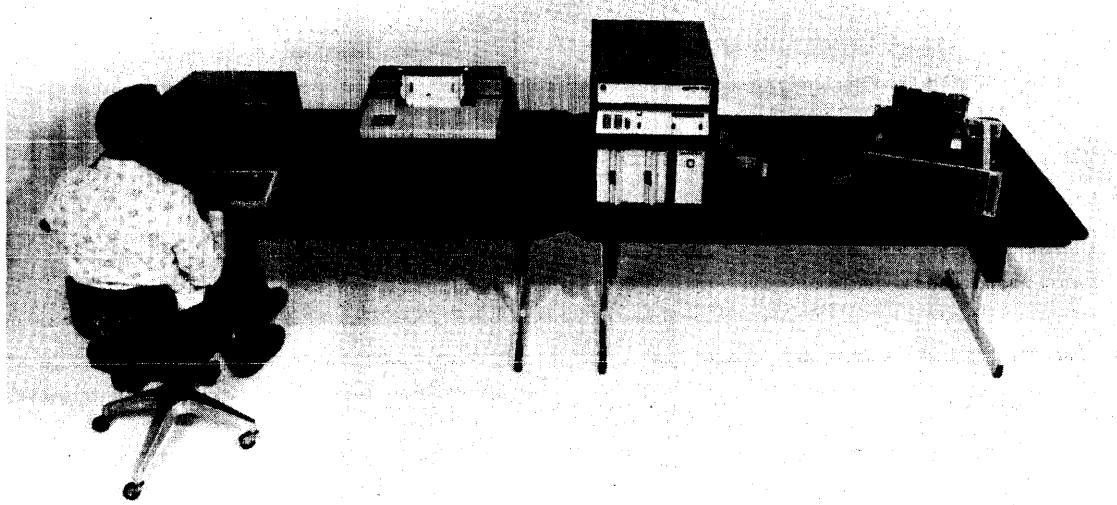


Figure 4

Text Editor

The Text Editor is a comprehensive software package that allows the user to enter and modify text files. The Text Editor is line oriented and accepts inputs from the terminal or a diskette file, performs modifications in a work space, and outputs the revised text to diskette file.

Assembler

The Prototype Development System Resident Assembler translates symbolic assembly language instructions into appropriate machine language code.

The Assembler is written in the Signetics Higher-Level Language (PLμS) and generates absolute object code. This code is in hexadecimal format and may be loaded into the system for direct execution or may be converted by an SDOS command to SMS format for PROM or ROM programming.

Debug

The debug system is a software program which provides the user with real-time program debug capabilities within both a software and hardware environment. It uses special hardware features built into the program development system to control the execution of the user's program. User programs operating under the debug system have dynamic program trace, breakpoint capabilities, and memory modification capabilities. Status reporting on the memory, the program, and the processor is also provided.

PHYSICAL AND ENVIRONMENTAL SPECIFICATIONS

	VOLTAGE	VOLT AMPERES	LINE FREQUENCY (HERTZ)	WEIGHT (POUNDS)	DIMENSIONS (INCHES)
Development Computer	115 ± 10%	230	47 — 63	65	8 x 17 x 22
Dual-Drive Floppy Disk	115 ± 10%	400	59.5 — 60.5	85	10 x 17 x 22
CRT Console	115 ± 10%	130	47 — 63	52	14 x 17 x 22
Printer	115 ± 10%	375	59.5 — 60.5	66	12 x 23 x 19

NOTE

Export version will operate from other line voltages and frequencies.

Table 1 SUBSYSTEM CHARACTERISTICS

Total System Characteristics

Operating Temperature Range: 15° — 37°C

Operating Humidity Range: 50% — 80% NC

Basic system shipping weight: 180 pounds

Card Cage—Mother Board Assembly

7 x 11 cards/20 slots in PDC

Common Bus Structure

External +5V ground bus (spare with rear panel terminals)

Front Panel Switches and Indicators

Key-operated primary power On/Off switch

PROM power switch

Reset switch that initializes system and sets both CPUs to location zero, enables master, and pauses slave.

Diagnostic interrupt switch

Power indicator

Run indicator

Master indicator

Slave indicator

PROM power indicator

signetics

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DESCRIPTION

The Signetics Adaptable Board Computer, ABC 1500, is a modular microcomputer containing a CPU, memory, I/O ports and support circuitry. It is designed to cover a broad range of applications from software development to system hardware prototyping. Cost performance trade offs have been carefully considered to achieve maximum flexibility and allow the card to be tailored to a variety of individual requirements.

The basic configuration consists of the 2650 8-bit microprocessor, 512 bytes of read/write memory (four 2112 static RAM's), 1k bytes of 2608 ROM with PIPBUG*, two 8T31 I/O ports and buffering on data, address and control lines. A single +5 volt supply will be required to power the card and communicate with a serial 20mA current loop terminal.

Modifications to the basic system can be easily made to allow for various memory configurations and operating modes. Unused plated through holes are provided for the PROM memory chips (82S115's). Other options are jumper selectable.

The ABC 1500 is sold either as a completely assembled and tested card (2650PC1500) or in kit form (2650KT9500).

*PIPBUG is a loader, editor, and debug program. See Table 1.

FEATURES

- Expandable printed circuit card: Unused area on card filled with plated through holes on .300 in. centers for wirewrap sockets
- 1k bytes of PIPBUG* ROM (in socket)
- 512 bytes of RAM
- Two latched I/O ports —four non-extended I/O read/write user strobes
- Tri-state buffers on data, address and control lines
- Serial input/output port
- Single +5 volt supply requirement (1.7A max) for card and 20mA current loop interface (±12 volt supply for RS232 interface)
- Interrupt and single step capability
- Simple clock configured from dual monostable multivibrator
- 24k memory expansion capability
- Directly compatible with 4k RAM card (2650PC2000) and power supply demonstration base (2650DS2000)
- Card dimensions: 8 in. by 6.875 in. with a 100 pin connector along the 8 in. dimension

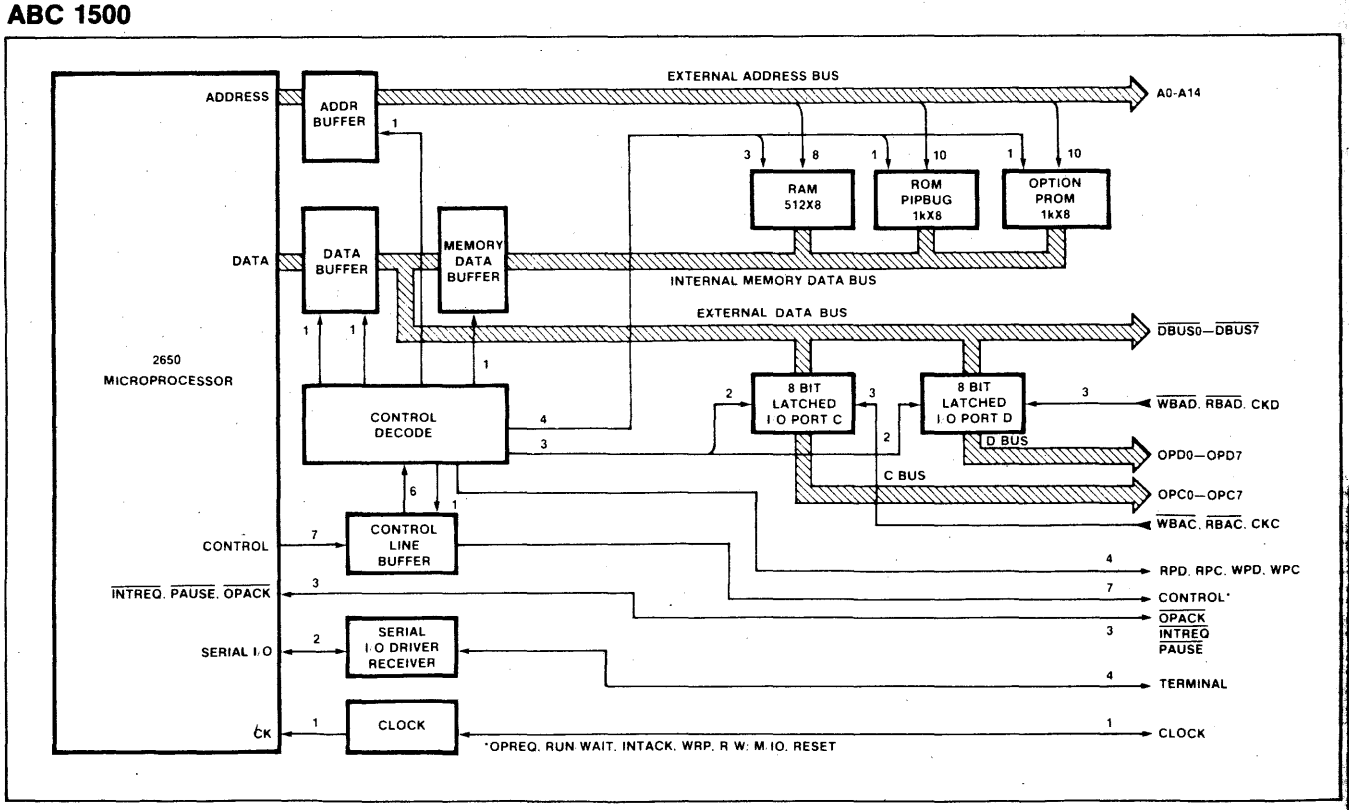
OPTIONS

- 1k bytes of PROM in place of ROM
- 512 bytes of PROM or ROM in place of RAM
- Asynchronous operation capability
- External clock input
- Interrupt vector from Port C

INTERFACE

- Terminal interface jumper selectable
  A. W4 to W5 and W6 to W7 jumpers select the 20mA current loop mode
  B. W3 to W4 and W7 to W8 jumpers select the RS232 mode
- Normally high input lines (10k pull up resistor on each): $\overline{\text{INTREQ}}$, $\overline{\text{PAUSE}}$, $\overline{\text{RESET}}$, $\overline{\text{WBAC}}$, $\overline{\text{WBAD}}$, CKC, CKD
- Plated through holes are available at each connector pin to allow for insertion of wirewrap pins.
- Edge connector supplied with card
- To allow for external clock input, remove jumper W9-W10
- Asynchronous operation by removing jumper W1 to W2 and driving $\overline{\text{OPACK}}$
- During vectored interrupts, it is possible to allow port C to place the interrupt address on the data bus by removing jumper W21-W22 and jumpering W22-W23

ABC 1500



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DESCRIPTION

Signetics offers one of the broadest choices of microprocessors . . . that translates to a broad understanding of microprocessors. This knowledge has gone into the development of the Instructor 50[tm]. Learning about the operational aspects of a microprocessor and how to program one is no easy task. Listening to long-winded lectures and sharing hands-on experience with ten other people during the last twenty minutes of a session are no way to learn about microprocessors, particularly when it comes to programming one.

That's precisely why we've developed the Instructor 50[tm] — to teach you about microprocessors and microprocessor programming the easy way, and "right in your own back yard." With the Instructor 50[tm] package, you have a complete microcomputer system right at your fingertips.

Instructor 50[tm] is a practical, low-cost microprocessor training tool. Its primary function is to teach you microprocessor operation, programming and applications. Even if you've never used a computer of any kind, you'll find that Instructor 50[tm] can help you learn and apply computer concepts very quickly.

FEATURES

- **Ready-to-run desktop unit with integral power supply.**
- **16-key hexadecimal keyboard for entering data values.**
- **12-key command function keyboard for issuing commands and selecting operating modes.**
- **Eight-digit LED display lets you instantly see results of your processing.**
- **Audio tape cassette interface allows you to create program library.**
- **S-100 interface bus permits system expansion.**
- **USE monitor program supervises operation of the system.**
- **Debugging aids, including breakpoint and single-step modes.**
- **Parallel and serial I/O.**
- **512 bytes of on-board user RAM.**
- **Crystal-controlled system clock.**
- **Comprehensive User's Guide and Introductory Manual.**
- **Port data input switches.**
- **Port data indicators.**
- **Direct/indirect interrupt switch.**
- **Port address select switch.**
- **FLAG and RUN indicators.**
- **Use of the powerful 2650 8-bit, N-channel microprocessor, with fixed command set of 75 instructions and eight different addressing modes.**

Each Instructor 50[tm] comes with a Warranty card, which offers parts replacement and related labor at no charge for 90 days after purchase. For repairs, simply ship the compact, lightweight unit to Signetics headquarters in Sunnyvale, California.

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Who Needs Instructor 50™? Research engineers, scientists, design engineers, engineering managers, instrumentation specialists, computer professionals, educators, students and hobbyists, to name a few. In fact, anyone desiring in-depth knowledge of how a microprocessor functions will benefit from Instructor 50™.

Instructor 50™ effectively supports college and university curricula by illustrating basic computing concepts. Educators who previously taught these fundamentals only through textbooks, lectures, and paper exercises now have a means by which their students can apply classroom instruction. Using the Instructor 50™, the student can write, enter and test his own programs, and observe the sequence of events associated with instruction execution.

Whether used in the classroom, office or home — the Instructor 50™ reinforces basic concepts, and provides the important "hands-on" experience to illustrate microcomputer functions.

No Experience Required. Plug in the Instructor 50™ — and the first message you'll read on the prompting display is "Hello." This friendly, interactive display combines with an exceptional ease of program entry to make the Instructor 50™ an ideal system for the novice.

There's absolutely no previous microprocessor experience required to use the Instructor 50™. This complete learning package comes with a User's Guide — plus a special introductory manual written just for the beginner. Also included is an audio cassette recording with helpful hints to assist you. On this cassette, you'll find interesting programs (e.g., clock, stopwatch and crap game) that you can run and enjoy right from the start.

While the Instructor 50™ "shakes hands" with the novice, its broad hardware/software capabilities can also challenge the pro. Accordingly, the Instructor 50™ is ready to handle more sophisticated applications when you are.

Fully Operational Microcomputer In One Package. Instructor 50™ minimizes the time and expense involved in learning the operation and programming of a microprocessor. A complete, ready-to-run unit with its own integral power supply, it features separate command and hexadecimal keyboards and an LED prompting display. The system includes everything you need to write, run and debug machine-language programs — housed in one compact package.

Build a Library of Program Tapes. You can save your programs on any ordinary cassette recorder tape. Simply depress the WCAS (write to cassette) key , and the Instructor 50™ will record your program onto a tape cassette. Later, you can rewind the tape, depress the RCAS (read from cassette) key, and reload computer memory. By saving your programs on tape, you can easily create your own library of programs.

Monitor Firmware Makes It Easy. The USE (User System Executive) Monitor firmware makes the Instructor 50™ the best system of its kind. Most systems require start-up procedures before a program can be loaded or executed. The Instructor 50™ does not. Its USE Monitor program runs automatically as soon as the system is turned on. And an LED display provides helpful prompting and error messages.

While in the monitor mode, you may:

- **enter and alter a program.**
- **read in a previously saved program from audio cassette tape.**
- **display and alter the contents of the microcomputer's general purpose working registers and/or Program Status Word.**
- **examine and alter the contents of the Program Counter and memory locations.**
- **specify and examine a program breakpoint.**
- **step through a program one instruction at a time.**
- **save a program on cassette tape.**
- **begin execution of a program you have written.**

Space for Expansion.* Equipped with an S-100 type expansion interface, the Instructor 50™ can be converted from a learning device to a small system computer — limited only by the number and type of peripheral boards used. Moreover, the powerful program/data entry and debug facilities of the basic Instructor 50™ can be extended to any device connected to the S-100 bus interface.

Heart of the System. The Instructor 50™ uses the Signetics 2650 microprocessor as the central processing element. Recognized as the microprocessor "most like a minicomputer," the 2650 reads instructions from program storage and, by executing these instructions, performs all the arithmetic and logical operations required. The 2650 also provides the system program with the physical means to access and control the system's input and output functions.

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FUNCTIONAL DESCRIPTION

- **Eight-Digit Display Panel.** This versatile display helps you learn by visually reinforcing the data the moment you enter it into the Instructor 50™. With it, you may examine and alter internal data, set up program parameters, observe the effects of your program one step at a time, and even write a program to display your own messages. Presenting some alphabetic, as well as numeric characters, it prompts you to enter necessary parameters and even tells you when you've made an error!

- **Cassette Connectors.** Virtually any audio cassette recorder can be hooked up here — and we supply the cords with the Instructor 50™. Use this connection to read a program into the microprocessor or take the program you've written through the keyboard and save it on an audio cassette tape.

- **Hexadecimal Keyboard.** Most professional programmers use the hexadecimal (base 16) numbering system. If you're not already familiar with this system, you'll learn about it in the Introductory Manual. And after a few turns at this keyboard, you'll understand why the hexadecimal system is preferred and how you can successfully use it for "machine language" programming.

- **Functional Control Keyboard.** Each of these 12 buttons commands the Instructor 50™ to perform a pre-defined operation as described in the Users' Guide. And three of the most used functions are color coded to make the keyboard even faster and easier to use.

- **Direct/Indirect Interrupt Switch.** This switch lets you learn and understand an important programming concept, direct and indirect "interrupt vectoring." The Instructor 50™'s 2650 microprocessor is one of the few to offer this sophisticated feature.

- **Port Address Select Switch.** This 3-position switch is used in conjunction with the Port Data Indicators and Port Data Input Switches. By providing three different ways to connect this "input/output" port to your microprocessor, it illustrates important tradeoffs that system designers must make.

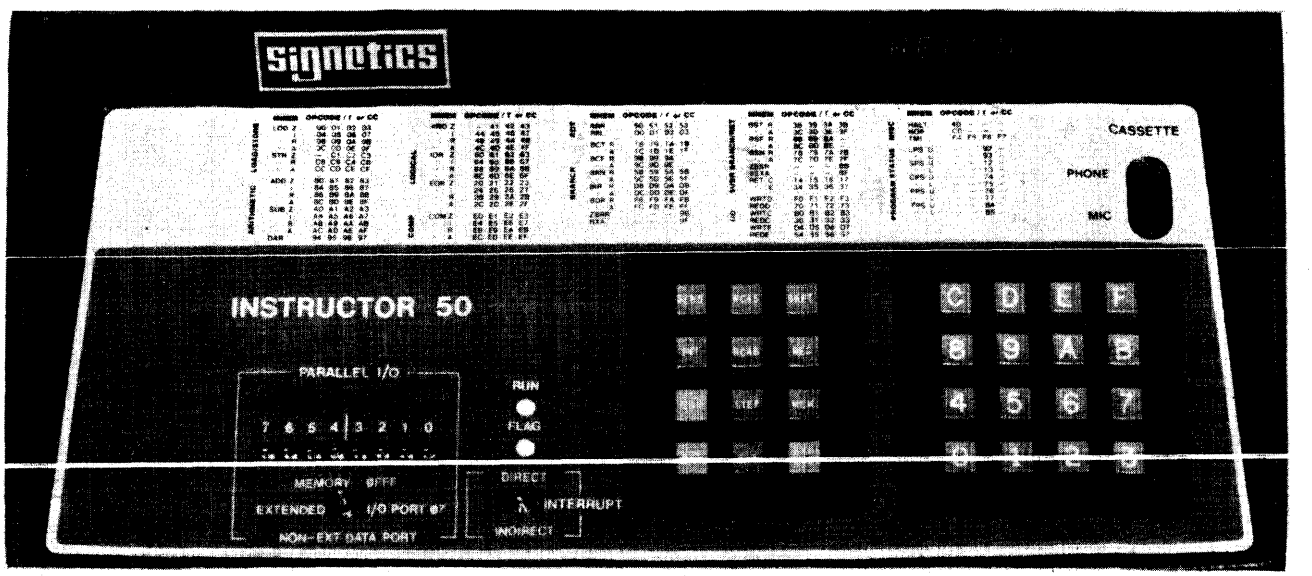
- **Port Data Input Switches.** Connected to an "input port," these eight rugged, numbered switches let you select up to 256 input combinations! You're limited only by your desire to learn with these simple switches at your command. Similar to the control switches found on large computers, they allow you to control the program flow of the microprocessor. Tell it what program to run. Or even use one or more of the combinations to play blackjack or a similar game.

- **Port Data Indicators.** These eight LEDs connected to an "output port" are your direct line to data within the 2650 microprocessor — the heart of the Instructor 50™. As they blink they're showing you the actual "ones" and "zeroes" being outputted from your unit. As your experience with the Instructor 50™ increases, you will gain a clear understanding of the internal operations of your learning tool.

- **Flag Indicator.** This LED signals the "Flag" condition, a special feature of the Instructor 50's 2650 microprocessor. This visual monitor lets you know when you've reached a limiting condition such as calculator overflow, or when you've reached a certain point in your program. It also can be used to illustrate "serial communications" concepts.

- **Run Indicator.** Another special monitor. This LED keeps a constant watch on the "run" signal of the 2650 microprocessor. And it's a straightforward way to verify that the 2650 is running a program — not in a paused or halted mode.

- **Instruction Reference Chart.** Before you know it, operating the Instructor 50™ will become second nature to you. But to make it even easier, we've printed a chart with basic instructions right on top of the unit. So in most cases, you won't need to refer to the comprehensive User's Guide or Introductory Manual that also come with your unit.



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ALTERNATE SOURCE DIRECTORY

The Alternate Source Directory is an industry-wide cross reference of those devices which manufacturers claim are pin-for-pin and functional equivalents to IC's made by other firms. It is a compilation of many individual references and shows literally thousands of alternates that aren't implied by their model numbers, especially in the linear and memory areas. Unlike the usual alternate source guides, this directory leads you to many alternate sources for any particular device, not just one. It is the most comprehensive alternate source directory ever published and contains over 44,000 cross references.

how to use the alternate source directory

The second column of this Alternate Source Directory shows devices which are replacements for those in the first column. Devices listed in **BOLD FACE** type have technical data in the Master Selection Guide. This information begins on the page listed to the right of the **BOLD FACE** part numbers. Products preceded by a ♦ have been discontinued by the manufacturer. This section does include devices not listed in the Master Selection Guide; e.g., discontinued items, DTL and 54L devices.

This list is compiled from manufacturers' recommendations. Since there is a tendency for every company to show only itself as an alternate to the prominent manufacturers, and for the larger ones to ignore the smaller ones, not every device is referenced both ways to every other one. Therefore, if you are looking for alternates to a lesser known company's device, take the replacements you find, especially if they are made by prominent companies and look them up to see if you can find any other sources.

In order to maintain this list within some reasonable bounds, the A and B suffixes indicating improved versions generally have been dropped. If this weren't done, for example, every higher speed selection conjured up by a memory manufacturer would result in a device that could replace many equal or slower competitors and this directory would become highly involved in slight performance variations. Moreover, improved performance is only important if your circuits take advantage of it.

One of the difficulties with any cross reference is that devices meant to be alternates do not necessarily perform the same in all circuits. Thus, it will be necessary for you to check specifications, or even to check circuit performance before deciding which alternates are right for you. A major benefit of this list is that it gives you more alternatives to study. But if you don't find what you need here, it may be possible to find additional alternates by locating the device in the Master Selection Guide. Particularly for digital circuits, the other products grouped with it will normally offer similar or identical performance.

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Advanced Micro Devices

Manufacturer Device	Replacement Source	Device	IC Master Page
♦AM2071	Signetics	82S07	
AM25LS07	Motorola	SN74LS378	
	TI	SN54LS378	
		SN74LS378	
AM25LS08	Motorola	SN74LS379	
	TI	SN54LS379	
		SN74LS379	
AM25LS09	Motorola	SN74LS399	
	TI	SN54LS399	
		SN74LS399	
AM25LS138	National	DM54LS138	
		DM74LS138	
	Raytheon	25LS138	
AM25LS139	National	DM54LS139	
		DM74LS139	
	Raytheon	25LS139	
AM25LS14	Motorola	SN74LS384	
	Raytheon	25LS14	
AM25LS15	Motorola	SN74LS385	
	Raytheon	25LS15	
AM25LS151	National	DM54LS151	
		DM74LS151	
	Raytheon	25LS151	
AM25LS153	National	DM54LS153	
		DM74LS153	
	Raytheon	25LS153	
AM25LS157	National	DM54LS157	
		DM74LS157	
	Raytheon	25LS157	
AM25LS158	National	DM54LS158	
		DM74LS158	
	Raytheon	25LS158	
AM25LS160	National	DM54LS160	
		DM74LS160	
	Raytheon	25LS160	
AM25LS161	National	DM54LS161	
		DM74LS161	
	Raytheon	25LS161	
AM25LS162	National	DM54LS162	
		DM74LS162	
	Raytheon	25LS162	
AM25LS163	National	DM54LS163	
		DM74LS163	
	Raytheon	25LS163	
AM25LS164	National	DM54LS164	
		DM74LS164	
♦AM25LS170	Raytheon	25LS170	
AM25LS174	National	DM54LS174	
		DM74LS174	
	Raytheon	25LS174	
AM25LS175	National	DM54LS175	
		DM74LS175	
	Raytheon	25LS175	
AM25LS181	National	DM54181	
		DM74181	
	Raytheon	25LS181	
AM25LS190	National	DM54LS190	
		DM74LS190	
	Raytheon	25LS190	
AM25LS191	National	DM54LS191	
		DM74LS191	
AM25LS192	Raytheon	25LS192	
AM25LS193	National	DM54LS193	
		DM74LS193	
	Raytheon	25LS193	
AM25LS194A	Raytheon	25LS194A	
AM25LS195	Raytheon	25LS195	
AM25LS22	Motorola	SN74LS322	
	Raytheon	25LS22	
	TI	SN54LS322	
		SN74LS322	
AM25LS23	Motorola	SN74LS323	
	Raytheon	25LS23	
	TI	SN54LS323	
		SN74LS323	
AM25LS241	Raytheon	25LS241	
AM25LS242	Raytheon	25LS242	
AM25LS243	Raytheon	25LS243	
AM25LS244	Raytheon	25LS244	
AM25LS251	Raytheon	25LS251	
AM25LS2518	Motorola	SN74LS368W	
AM25LS253	Raytheon	25LS253	
AM25LS257	National	DM54LS257	
AM25LS257	National	DM74LS257	
AM25LS258	National	DM54LS258	
		DM74LS258	
	Raytheon	25LS258	
AM25LS273	Raytheon	25LS273	
AM25LS299	Raytheon	25LS299	
AM25LS322	Raytheon	25LS322	
AM25LS323	Raytheon	25LS323	
AM25LS374	Raytheon	25LS374	
AM25LS377	Raytheon	25LS377	
AM25LS384	Raytheon	25LS384	
AM25LS385	Raytheon	25LS385	
♦AM25LS670	Raytheon	25LS670	
AM25L02	**National**	**DM2502**	**1073**
AM25L03	**National**	**DM2503**	**1073**
AM25L04	**National**	**DM2504**	**1073**
AM25S10	**Signetics**	**74S350**	**561**
AM2502	Intersil	2502	
	National	**DM2502**	**1073**
AM2503	Intersil	2503	
	National	**DM2503**	**1073**
AM2504	Intersil	2504	
	National	**DM2504**	**1073**
AM2505	Raytheon	RC2505	
		RM2505	
AM26LS31	National	DS26LS31	
	TI	AM26LS31	
AM26LS32	National	DS26LS32	
	TI	AM26LS22	
AM26LS33	National	DS26LS33	
	TI	AM26LS33	
AM26L02	National	DM8602	
		DM9602	
AM26L123	National	DM54L123	
		DM74L123	
AM26S02	National	DM8602	
		DM9602	
AM26S10	Fairchild	9640	
	Motorola	MC26S10	
	National	DS26S10	
	Raytheon	26S10	
	TI	AM26S10	
AM26S11	Fairchild	9641	
	Motorola	MC26S11	
	National	DS26S11	
	Raytheon	26S11	
	TI	AM26S11	
AM2602	National	DM8602	
		DM9602	
AM26123	National	DM54123	
		DM74123	
	TI	SN54123	
		SN74123	
AM27LS00	**Fairchild**	**93421**	**1252**
	National	DM54S200	
		DM74S200	
	TI	SN74LS200	
AM27LS01	Fairchild	93411	
	National	DM54S206	
		DM74S206	
AM27LS02	MMI	27LS02	
AM27LS03	MMI	27LS03	
AM27LS08	**MMI**	**53LS080**	**1458**
		63LS080	**1458**
AM27LS09	**MMI**	**53LS081**	**1458**
		63LS081	**1458**
AM27LS10	Fairchild	93416	
	Harris	HPROM1024	
	NEC Micro	μPB403	
AM27S02	MMI	27S02	
		5560	
		6560	
	National	DM54S289	
		DM74S289	
	NEC Micro	μPB2089	
	TI	SN54S289	
		SN74S289	
AM27S03	Fairchild	93405	
	MMI	27S03	
		5561	
		6561	
	National	DM54S189	
		DM74S189	
		DM7599	
		DM8599	
	TI	SN54S189	
AM27S03	TI	SN74S189	
AM27S08	**Harris**	**HM7602**	**1284**
	MMI	**5330-1**	**1449**
	National	DM7577	
		DM8577	
	TI	**SN54S188**	**1708**
		SN74S188	**1708**
AM27S09	**Harris**	**HM7603**	**1284**
	MMI	**5331-1**	**1449**
		6331-1	**1449**
	National	DM7578	
		DM8578	
	Signetics	**N82S123**	**1680**
		S82S123	**1680**
		82S123	
	TI	**SN54S288**	**1708**
		SN74S288	**1708**
AM27S10	**Harris**	**HM7610**	
			1284,1292
		HM7610A	
	MMI	**5300-1**	**1449**
		6300-1	**1449**
	National	DM54S387	
		DM74S387	
	NEC Micro	μPB403	
	TI	**SN54S387**	**1708**
		SN74S387	**1708**
AM27S11	**Harris**	**HM7611**	
			1284,1292
		HM7611A	
	Intel	M3621	
		3621	
	MMI	**5301-1**	**1449**
		6301-1	**1449**
	National	DM54S287	
		DM74S287	
	TI	**SN54S287**	**1708**
		SN74S287	**1708**
AM27S12	**MMI**	**5305-1**	**1449**
		6305-1	**1449**
	Raytheon	**29610**	**1654**
	Signetics	**N82S130**	**1680**
		S82S130	**1680**
AM27S13	**MMI**	**5306-1**	**1449**
		6306-1	**1449**
	Raytheon	**29611**	**1654**
	Signetics	**N82S131**	**1680**
		S82S131	**1680**
AM27S18	**MMI**	**53S080**	**1453**
		63S080	**1453**
AM27S19	**MMI**	**53S081**	**1453**
		63S081	**1453**
AM27S20	**MMI**	**53S140**	**1453**
		53S240	**1453**
		63S140	**1453**
		63S240	**1453**
	Raytheon	**29660**	**1664**
	Signetics	**N82S140**	**1680**
		S82S140	**1680**
AM27S21	**MMI**	**53S141**	**1453**
		53S241	**1453**
		63S141	**1453**
		63S241	**1453**
	Raytheon	**29661**	**1664**
AM27S28	**MMI**	**53S480**	**1453**
		63S480	**1453**
AM27S29	**MMI**	**53S481**	**1453**
		63S481	**1453**
AM27S30	**MMI**	**53S482**	**1453**
		63S482	**1453**
AM27S31	**MMI**	**53S483**	**1453**
		63S483	**1453**
AM27S32	**MMI**	**53S440**	**1453**
		63S440	**1453**
	Signetics	**N82S136**	**1680**
		S82S136	**1680**
AM27S33	**MMI**	**53S441**	**1453**
		63S441	**1453**
	Signetics	**N82S137**	**1680**
		S82S137	**1680**
AM2700	MMI	6531	
	Signetics	**N82S16**	**1678**
	TI	SN54S201	
		SN74S200A	
		SN74S201	
AM2701	Fairchild	93411	
AM2701	MMI	6530	
	Signetics	82S17	
	TI	SN54S301	
		SN74S300	
		SN74S301	
AM2802	Synertek	SY2802	
AM2803	Synertek	SY2803	
AM2804	Synertek	SY2804	
AM2809	TI	TMS3128	
AM2812	Plessey	MP3812	
AM2814	TI	TMS3114	
AM2825	Synertek	SY2825	
AM2826	Synertek	SY2826	
AM2827	Synertek	SY2827	
AM2833	Synertek	SY2833	
AM2847	TI	TMS3120	
AM2901	Motorola	MC2901	
	Raytheon	AM2901	
AM2901A	Fairchild	F2901A	
	MMI	2901A	
	Motorola	MC2901A	
	National	**IDM2901A**	**286**
	NEC Micro	μPB2901A	
	Raytheon	AM2901A	
	Signetics	**N2901A**	**2279**
AM2902	Motorola	MC2902	
	NEC Micro	μPB2902A	
	Raytheon	AM2902	
AM2903	Fairchild	F2903	
	Motorola	MC2903	
AM2905	MMI	2905	
	Motorola	MC2905	
	NEC Micro	μPB2905A	
	Raytheon	AM2905	
AM2906	MMI	2906	
	Motorola	MC2906	
	NEC Micro	μPB2906A	
	Raytheon	AM2906	
AM2907	MMI	2907	
	Motorola	MC2907	
	NEC Micro	μPB2907A	
	Raytheon	AM2907	
AM2909	MMI	2909	
	Motorola	MC2909	
	NEC Micro	μPB2909A	
	Raytheon	AM2909	
AM2910	Fairchild	F2910	
	Motorola	MC2910	
AM2911	MMI	2911	
	Motorola	MC2911	
	NEC Micro	μPB2911A	
	Raytheon	AM2911	
AM2914	Fairchild	F2914	
AM2915A	MMI	2915A	
	Motorola	MC2915A	
	NEC Micro	μPB2915A	
	Raytheon	AM2915A	
AM2916A	MMI	2916A	
	Motorola	MC2916A	
	NEC Micro	μPB2916A	
	Raytheon	AM2916A	
AM2917A	MMI	2917A	
	Motorola	MC2917A	
	NEC Micro	μPB2917A	
	Raytheon	AM2917A	
AM2918	MMI	2918	
	Motorola	MC2918	
	NEC Micro	μPB2918A	
	Raytheon	AM2918	
AM2919	MMI	2919	
AM29701	MMI	29701	
AM29702	MMI	29702	
	National	IDM29702	
AM29703	MMI	29703	
	National	IDM29703	
AM29750	**MMI**	**5330-1**	**1449**
		6330-1	**1449**
	National	IDM29750	
AM29751	**MMI**	**5331-1**	**1449**
		6331-1	**1449**
	National	IDM29751	
AM29760	**MMI**	**5300-1**	**1449**
		6300-1	**1449**
	National	IDM29760	
AM29761	**MMI**	**5301-1**	**1449**
		6301-1	**1449**

♦ Discontinued

Bold face device numbers indicate manufacturers data is provided in the IC Master on the pages noted.

Advanced Micro Devices (cont'd)

Manufacturer Device	Replacement Source	Device	IC Master Page
AM29761	National	IDM29761	
AM29770	**MMI**	**5305-1**	**1449**
		6305-1	**1449**
AM29771	**MMI**	**5306-1**	**1449**
		6306-1	**1449**
AM29772	**MMI**	**53S480**	**1453**
		63S480	**1453**
AM29773	**MMI**	**53S481**	**1453**
		63S481	**1453**
AM54LS170	TI	SN54LS170	
AM6070	PMI	DAC-76	
AM6072	PMI	DAC-86	
AM6073	PMI	DAC-87	
DAC-08	**Datel**	**DAC-08B**	**670**
	PMI	DAC-08	
	Signetics	DAC-08	
DM7820	Signetics	DS7820	
DM7820A	Signetics	DS7820A	
	TI	SN55182	
DM7830	Signetics	DS7830	
	TI	SN55183	
DM7831	TI	DS7831	
DM7832	TI	DS7832	
DM8820A	TI	SN75182	
DM8830	Signetics	DS8830	
	TI	SN75183	
DM8831	TI	DS7831	
DM8832	TI	DS7832	
DP8303	National	DP8303	
DP8304	National	DP8304	
LF155	Fairchild	μAF155	
	Intersil	LF155	
	Motorola	LF155	
	National	**LF155**	**1035**
	PMI	PM155	
	Raytheon	LF155	
	Signetics	LF155	
	TI	LF155	
LF156	Fairchild	μAF156	
	Intersil	LF156	
	Motorola	LF156	
	National	**LF156**	**1035**
	PMI	PM156	
	Raytheon	LF156	
	Signetics	LF156	
	TI	LF156	
LF157	Fairchild	μAF157	
	Intersil	LF157	
	Motorola	LF157	
	National	**LF157**	**1035**
	PMI	PM157	
	Raytheon	LF157	
	Signetics	LF157	
	TI	LF157	
LF255	Fairchild	μAF255	
	Intersil	LF255	
	Motorola	LF255	
	National	LF255	
	PMI	PM255	
	Raytheon	LF255	
	Signetics	LF255	
	TI	LF255	
LF256	Fairchild	μAF256	
	Intersil	LF256	
	Motorola	LF256	
	National	LF256	
	PMI	PM256	
	Raytheon	LF256	
	Signetics	LF256	
	TI	LF256	
LF257	Fairchild	μAF257	
	Intersil	LF257	
	Motorola	LF257	
	National	LF257	
	PMI	PM257	
	Raytheon	LF257	
	Signetics	LF257	
	TI	LF257	
LF298	PMI	SMP-11	
LF355	Fairchild	μAF355	
	Intersil	LF355	
	Motorola	LF355	
LF355	National	LF355	
	PMI	PM355	
	Raytheon	LF355	
	Signetics	LF355	
	TI	LF355	
LF356	Fairchild	μAF356	
	Intersil	LF356	
	Motorola	LF356	
	National	**LF356**	**1035,1073**
	PMI	PM356	
	Raytheon	LF356	
	Signetics	LF356	
	TI	LF356	
LF357	Fairchild	μAF357	
	Intersil	LF357	
	Motorola	LF357	
	National	LF357	
	PMI	PM357	
	Raytheon	LF357	
	Signetics	LF357	
	TI	LF357	
LF398	PMI	SMP-11	
LM101	AD	AD101	
	Fairchild	μA101	
	Intersil	LM101	
	Motorola	LM101	
	National	**LM101**	**1035**
	RCA	CA101	
	Signetics	LM101	
	Silicon G	SG101	
LM102	Fairchild	μA102	
	Silicon G	SG102	
LM105	**Fairchild**	**μA105**	**934**
	Intersil	LM105	
	Motorola	LM105	
	National	LM105	
	Raytheon	LM105	
	Silicon G	SG105	
LM107	Fairchild	μA107	
	Intersil	LM107	
	Motorola	LM107	
	National	LM107	
	Raytheon	LM107	
	RCA	CA107	
	Silicon G	SG107	
LM108	AD	AD108	
	Fairchild	μA108	
	Intersil	LM108	
	Motorola	LM108	
	National	**LM108**	**1035**
	Raytheon	LM108	
	RCA	CA108	
	Signetics	LM108	
	Silicon G	SG108	
LM110	Fairchild	μA110	
	Intersil	LM110	
	Motorola	LM110	
	National	LM110	
	PMI	BUE-01	
		BUF-02	
	Silicon G	SG110	
LM111	Fairchild	μA111	
	Intersil	LM111	
	Motorola	LM111	
	National	LM111	
	Raytheon	LM111	
	RCA	CA111	
	Signetics	LM111	
	Silicon G	SG111	
LM118	AD	AD518	
	National	**LM118**	**1035**
	Raytheon	LM118	
LM139	Fairchild	μA139	
LM139A	PMI	CMP-04	
		PM139A	
LM148	Exar	XR4741	
	Raytheon	LM148	
LM201	AD	AD201	
	Fairchild	μA201	
	Intersil	LM201	
	Motorola	LM201	
	National	LM201	
	RCA	CA201	
	Signetics	LM201	
	Silicon G	SG201	
LM202	Motorola	LM210	
LM202	Silicon G	SG202	
LM205	Intersil	LM205	
	Motorola	LM205	
	Raytheon	LM205	
	Silicon G	SG205	
LM207	Fairchild	μA207	
	Intersil	LM207	
	Motorola	LM207	
	Raytheon	LM207	
	RCA	CA207	
	Silicon G	SG207	
LM208	AD	AD208	
	Fairchild	μA208	
	Intersil	LM208	
	Motorola	LM208	
	Raytheon	LM208	
	RCA	CA208	
	Silicon G	SG208	
LM210	Intersil	LM210	
	Motorola	LM210	
	PMI	BUF-01	
		BUF-02	
	Silicon G	SG210	
LM211	Intersil	LM211	
	Motorola	LM211	
	Raytheon	LM211	
	RCA	CA211	
	Signetics	LM211	
	Silicon G	SG211	
LM218	AD	AD518	
	Raytheon	LM218	
LM239A	PMI	CMP-04	
		PM239A	
LM248	Exar	XR4741	
	Raytheon	LM248	
LM301	AD	AD301	
	Fairchild	μA301	
	Intersil	LM301	
	Motorola	LM301	
	Raytheon	LM301	
	RCA	CA301	
	Signetics	LM301	
	Silicon G	SG301	
LM302	Fairchild	μA302	
	Silicon G	SG302	
LM305	**Fairchild**	**μA305**	**934**
	Intersil	LM305	
	Motorola	LM305	
	Raytheon	LM305	
	Silicon G	SG305	
LM307	Fairchild	μA307	
	Intersil	LM307	
	Motorola	LM307	
	Raytheon	LM307	
	RCA	CA307	
	Signetics	LM307	
	Silicon G	SG307	
LM308	AD	AD308	
	Fairchild	μA308	
	Intersil	LM308	
	Motorola	LM308	
	Raytheon	LM308	
	RCA	CA308	
	Signetics	LM308	
	Silicon G	SG308	
LM310	Fairchild	μA310	
	Intersil	LM310	
	Motorola	LM310	
	PMI	BUF-01	
		BUF-02	
	Silicon G	SG310	
LM311	Fairchild	μA311	
	Intersil	LM311	
	Motorola	LM311	
	Raytheon	LM311	
	RCA	CA311	
	Signetics	LM311	
	Silicon G	SG311	
LM318	AD	AD518	
	Raytheon	LM318	
LM339	Fairchild	μA339	
	Silicon G	SG339	
LM339A	PMI	CMP-04	
		PM339A	
LM348	Exar	XR4741	
	Raytheon	LM348	
NE555	Cherry	CS555	
	Exar	XR555	
		XR555M	
	Fairchild	μA555	
	Motorola	MC1455	
	National	LM555	
	Silicon G	SG555	
NE556	Exar	XR556	
	Fairchild	μA556	
	Silicon G	SG556	
SE555	Exar	XR555	
	Silicon G	SG555	
SE556	Exar	XR556M	
	Silicon G	SG556	
SN54LS123	National	DM54LS123	
	Raytheon	54LS123	
	TI	SN54LS123	
SN54LS138	Fairchild	54LS138	
	Motorola	SN54LS138	
	Raytheon	54LS138	
SN54LS139	Fairchild	54LS139	
	Motorola	SN54LS139	
	National	DM54LS139	
	Raytheon	54LS139	
	Signetics	74LS139	
	TI	SN54LS139	
SN54LS148	TI	SN54LS148	
SN54LS151	Fairchild	54LS151	
	Motorola	SN54LS151	
	National	DM54LS151	
	Raytheon	54LS151	
	Signetics	54LS151	
	TI	SN54LS151	
SN54LS153	Fairchild	54LS153	
	Motorola	SN54LS153	
	National	DM54LS153	
	Raytheon	54LS153	
	Signetics	54LS153	
	TI	SN54LS153	
SN54LS157	Fairchild	54LS157	
	Motorola	SN54LS157	
	National	DM54LS157	
	Raytheon	54LS157	
	Signetics	54LS157	
	TI	SN54LS157	
SN54LS158	Fairchild	54LS158	
	Motorola	SN54LS158	
	Raytheon	54LS158	
SN54LS160	Fairchild	54LS160	
	Motorola	SN54LS160A	
	National	DM54LS160	
	Raytheon	54LS160	
	TI	SN54LS160A	
SN54LS161	Fairchild	54LS161	
	Motorola	SN54LS161A	
	National	DM54LS161	
	Raytheon	54LS161	
	Signetics	54LS161	
	TI	SN54LS161A	
SN54LS162	Fairchild	54LS162	
	Motorola	SN54LS162	
	National	DM54LS162	
	Raytheon	54LS162	
	TI	SN54LS162A	
SN54LS163	Fairchild	54LS163	
	Motorola	SN54LS163A	
	National	DM54LS163	
	Raytheon	54LS163	
	Signetics	54LS163	
	TI	SN54LS163A	
SN54LS164	Fairchild	54LS164	
	Motorola	SN54LS164A	
	National	DM54LS164	
	Raytheon	54LS164	
	Signetics	54LS164	
	TI	SN54LS164A	
SN54LS168	Fairchild	54LS168	
	National	DM54LS168	
	TI	SN54LS168	
SN54LS169	Fairchild	54LS169	
	National	DM54LS169	
	TI	SN54LS169	
SN54LS170	Fairchild	54LS170	
	Motorola	SN54LS170	
	National	DM54LS170	
	Raytheon	54LS170	

♦ Discontinued

The manufacturers report their devices can be used as direct replacements.
Performance details often differ, so compare the specifications considering your requirements.

Advanced Micro Devices (cont'd)

Manufacturer Device	Replacement Source	Device	IC Master Page
SN54LS170	Signetics	54LS170	
SN54LS174	Fairchild	54LS174	
	Motorola	SN54LS174	
	National	DM54LS174	
	Raytheon	54LS174	
	Signetics	54LS174	
	TI	SN54LS174	
SN54LS175	Fairchild	54LS175	
	Motorola	SN54LS175	
	National	DM54LS175	
	Raytheon	54LS175	
	Signetics	54LS175	
	TI	SN54LS175	
SN54LS181	Fairchild	54LS181	
	Motorola	SN54LS181	
	Raytheon	54LS181	
	Signetics	54LS181	
	TI	SN54LS181	
SN54LS190	Fairchild	54LS190	
	Motorola	SN54LS190	
	National	DM54LS190	
	Raytheon	54LS190	
	Signetics	54LS190	
	TI	SN54LS190	
SN54LS191	Fairchild	54LS191	
	Motorola	SN54LS191	
	National	DM54LS191	
	Raytheon	54LS191	
	Signetics	54LS191	
	TI	SN54LS191	
SN54LS192	Fairchild	54LS192	
	Motorola	SN54LS192	
	National	DM54LS192	
	Raytheon	54LS192	
	Signetics	54LS192	
	TI	SN54LS192	
SN54LS193	Fairchild	54LS193	
	Motorola	SN54LS193	
	National	DM54LS193	
	Raytheon	54LS193	
	Signetics	54LS193	
	TI	SN54LS193	
SN54LS194A	Fairchild	54LS194	
	Raytheon	54LS194A	
	TI	SN54LS194A	
SN54LS195A	Fairchild	54LS195	
	Raytheon	54LS195A	
	Signetics	54LS195A	
	TI	SN54LS195A	
SN54LS240	Fairchild	54LS240	
	MMI	**54LS240**	**768**
	TI	SN54LS240	
SN54LS241	Fairchild	54LS241	
	MMI	**54LS241**	**768**
	TI	SN54LS241	
SN54LS242	Fairchild	54LS242	
	Raytheon	**54LS242**	**528**
	TI	SN54LS242	
SN54LS243	Fairchild	54LS243	
	Raytheon	**54LS243**	**528**
	TI	SN54LS243	
SN54LS245	Motorola	SN54LS245	
SN54LS251	Fairchild	54LS251	
	Motorola	SN54LS251	
	Raytheon	54LS251	
	Signetics	54LS251	
	TI	SN54LS251	
SN54LS253	Fairchild	54LS253	
	Motorola	SN54LS253	
	National	DM54LS253	
	Raytheon	54LS253	
	Signetics	54LS253	
	TI	SN54LS253	
SN54LS257	Motorola	SN54LS257A	
	Raytheon	54LS257	
SN54LS258	Fairchild	54LS258A	
	Motorola	SN54LS258	
	Raytheon	54LS258	
	TI	SN54LS258	
[illegible]	[illegible]	[illegible]	
	TI	SN54LS273	
SN54LS299	Fairchild	54LS299	
SN54LS299	Motorola	SN54LS299	
	Raytheon	**54LS299**	**533**
	TI	SN54LS299	
SN54LS322	Motorola	SN54LS322	
	TI	SN54LS322	
SN54LS323	Motorola	SN54LS323	
	TI	SN54LS323	
SN54LS373	Motorola	SN54LS373	
SN54LS374	**MMI**	**54LS374**	**505**
	Motorola	SN54LS374	
	TI	SN54LS374	
SN54LS377	Motorola	SN54LS377	
	TI	SN54LS377	
SN54LS378	Fairchild	54LS378	
	TI	SN54LS378	
SN54LS379	Motorola	SN54LS379	
	TI	SN54LS379	
SN54LS381	TI	SN54LS381	
SN54LS384	Motorola	SN54LS384	
	TI	SN54LS384	
SN54LS385	Motorola	SN54LS385	
	TI	SN54LS385	
SN54LS399	Motorola	SN54LS399	
	TI	SN54LS399	
SN54LS424	TI	SN54LS424	
SN54LS568	Motorola	SN54LS568	
SN54LS569	Motorola	SN54LS569	
SN54LS670	Fairchild	54LS670	
	Motorola	SN54LS670	
	National	DM54LS670	
	Raytheon	54LS670	
	Signetics	54LS670	
	TI	SN54LS670	
SN54S138	Fairchild	54S138	
	TI	SN54S138	
SN54S139	Fairchild	54S139	
	Signetics	54S139	
	TI	SN54S139	
SN54S140	Fairchild	54S140	
	Signetics	54S140	
	TI	SN54S140	
SN54S151	Fairchild	54S151	
	Signetics	54S151	
	TI	SN54S151	
SN54S153	Fairchild	54S153	
	Signetics	54S153	
	TI	SN54S153	
SN54S157	Fairchild	54S157	
	Signetics	54S157	
	TI	SN54S157	
SN54S158	Fairchild	54S158	
	Signetics	54S158	
	TI	SN54S158	
SN54S174	Fairchild	54S174	
	TI	SN54S174	
SN54S175	Fairchild	93S411	
	TI	SN54S175	
SN54S181	Fairchild	54S181	
		93S41	
	Signetics	54S181	
	TI	SN54S181	
SN54S189	TI	SN54S189	
SN54S194	Fairchild	54S194	
	TI	SN54S194	
SN54S195	Fairchild	93S00	
	TI	SN54S195	
SN54S240	**MMI**	**54S240**	**768**
	TI	SN54S240	
SN54S241	**MMI**	**54S241**	**768**
	Raytheon	54S241	
	TI	SN54S241	
SN54S244	**MMI**	**54S244**	**768**
	Raytheon	54S244	
SN54S251	Fairchild	54S251	
	Signetics	54S251	
	TI	SN54S251	
SN54S253	Fairchild	54S253	
	Signetics	54S253	
SN54S257	Fairchild	54S257	
	Signetics	54S257	
	TI	SN74S257	
SN54S258	Fairchild	54S258	
	Signetics	54S258	
	TI	[illegible]	
SN54123	Fairchild	54123	
	Motorola	MC54123	
SN54123	National	DM54123	
	Signetics	54123	
	TI	SN54123	
SN54154	Fairchild	54154	
	Motorola	MC54154	
	National	DM54154	
	Signetics	54154	
	TI	SN54154	
SN54157	Fairchild	54157	
	Motorola	MC54157	
	National	DM54157	
	Signetics	54157	
	TI	SN54157	
SN54160	Fairchild	54160	
	Motorola	MC54160	
	National	DM54160	
	Signetics	54160	
	TI	SN54160	
SN54161	Fairchild	54161	
	Motorola	MC54161	
	National	DM54161	
	Signetics	54161	
	TI	SN54161	
SN54162	Fairchild	54162	
	Motorola	MC54162	
	National	DM54162	
	Signetics	54162	
	TI	SN54162	
SN54163	Fairchild	54163	
	Motorola	MC54163	
	National	DM54163	
	Signetics	54163	
	TI	SN54163	
SN54164	Fairchild	54164	
	National	DM54164	
	Signetics	54164	
	TI	SN54164	
SN54175	Fairchild	54175	
	Motorola	MC54175	
	National	DM54175	
	Signetics	54175	
	TI	SN54175	
SN54181	Fairchild	54181	
		9341	
	Motorola	MC54181	
	National	DM54181	
	Signetics	54181	
	TI	SN54181	
		SN74181	
SN54182	Fairchild	54182	
		9342	
	Motorola	MC54182	
	National	DM54182	
	Signetics	54182	
	TI	SN54182	
		SN74182	
SN54192	Fairchild	54192	
	Motorola	MC54192	
	National	DM54192	
	Signetics	54192	
	TI	SN54192	
SN54193	Fairchild	54193	
	Motorola	MC54193	
	National	DM54193	
	Signetics	54193	
	TI	SN54193	
SN54194	Fairchild	54194	
	Motorola	MC54194	
	National	DM54194	
	Signetics	54194	
	TI	SN54194	
SN54195	Fairchild	54195	
	Motorola	MC54195	
	National	DM54195	
	Signetics	54195	
	TI	SN54195	
SN54259	TI	SN54259	
SN5489	MMI	5560	
SN55107	Fairchild	55107	
	TI	SN55107	
SN55108	Fairchild	55108	
	TI	SN55108	
SN55109	Fairchild	55109	
	TI	[illegible]	
SN55110	Fairchild	55110	
	TI	SN55110	
SN5520	Fairchild	5520	
SN5521	Fairchild	5521	
SN55234	Fairchild	55234	
	TI	SN55234	
SN55235	Fairchild	55235	
	TI	SN55235	
SN55238	Fairchild	55238	
	TI	SN55238	
SN55239	Fairchild	55239	
	TI	SN55239	
SN5524	Fairchild	5524	
SN5525	Fairchild	5525	
SN55325	Fairchild	55325	
	TI	SN55325	
SN74LS123	Hitachi	HD74LS123	
	National	DM74LS123	
	Raytheon	74LS123	
	TI	SN74LS123	
SN74LS138	Fairchild	74LS138	
	Hitachi	HD74LS138	
	Motorola	SN74LS138	
	National	DM74LS138	
	NEC America	μPB74LS138	
	Raytheon	74LS138	
	Signetics	74LS138	
	TI	SN74LS138	
SN74LS139	Fairchild	74LS139	
	Hitachi	HD74LS139	
	Motorola	SN74LS139	
	National	DM74LS139	
	NEC America	μPB74LS139	
	Raytheon	74LS139	
	Signetics	74LS139	
	TI	SN74LS139	
SN74LS148	TI	SN74LS148	
SN74LS151	Fairchild	74LS151	
	Hitachi	HD74LS151A	
	Motorola	SN74LS151	
	National	DM74LS151	
	NEC America	μPB74LS151	
	Raytheon	74LS151	
	Signetics	74LS151	
	TI	SN74LS151	
SN74LS153	Fairchild	74LS153	
	Hitachi	HD74LS153	
	Motorola	SN74LS153	
	National	DM74LS153	
	NEC America	μPB74LS153	
	Raytheon	74LS153	
	Signetics	74LS153	
	TI	SN74LS153	
SN74LS157	Fairchild	74LS157	
	Motorola	SN74LS157	
	National	DM74LS157	
	NEC America	μPB74LS157	
	Raytheon	74LS157	
	Signetics	74LS157	
	TI	SN74LS157	
SN74LS158	Fairchild	74LS158	
	Motorola	SN74LS158	
	National	DM74LS158	
	Raytheon	74LS158	
	Signetics	74LS158	
	TI	SN74LS158	
SN74LS160	Fairchild	74LS160	
	Hitachi	HD74LS160A	
	Motorola	SN74LS160A	
	National	DM74LS160	
	Raytheon	74LS160	
	Signetics	74LS160A	
	TI	SN74LS160A	
SN74LS161	Fairchild	74LS161	
	Hitachi	HD74LS161A	
	Motorola	SN74LS161A	
	National	DM74LS161	
	NEC America	μPB74LS161	
	Raytheon	74LS161	
	Signetics	74LS161A	
	TI	SN74LS161A	
SN74LS162	Fairchild	74LS162	
	Hitachi	HD74LS162A	
	Motorola	SN74LS162A	
	National	DM74LS162	
	Raytheon	[illegible]	
	Signetics	74LS162A	
	TI	SN74LS162A	

♦ Discontinued

Bold face device numbers indicate manufacturers data is provided in the IC Master on the pages noted.

Advanced Micro Devices (cont'd)

Manufacturer Device	Replacement Source	Device	IC Master Page
SN74LS163	Fairchild	74LS163	
	Hitachi	HD74LS163A	
	Motorola	SN74LS163A	
	National	DM74LS163	
	Raytheon	74LS163	
	Signetics	74LS163	
	TI	SN74LS163A	
SN74LS164	Fairchild	74LS164	
	Hitachi	HD74LS164	
	Motorola	SN74LS164	
	National	DM74LS164	
	NEC America	μPB74LS164	
	Raytheon	74LS164	
	Signetics	74LS164	
	TI	SN74LS164	
SN74LS168	Fairchild	74LS168	
	National	DM74LS168	
	TI	SN74LS168	
SN74LS169	Fairchild	74LS169	
	National	DM74LS169	
	TI	SN74LS169	
♦SN74LS170	Fairchild	74LS170	
	Motorola	SN74LS170	
	National	DM74LS170	
	Raytheon	74LS170	
	Signetics	74LS170	
	TI	SN74LS170	
SN74LS174	Fairchild	74LS174	
	Hitachi	HD74LS174	
	Motorola	SN74LS174	
	National	DM74LS174	
	Raytheon	74LS174	
	Signetics	74LS174	
	TI	SN74LS174	
SN74LS175	Fairchild	74LS175	
	Hitachi	HD74LS175	
	Motorola	SN74LS175	
	National	DM74LS175	
	NEC America	μPB74LS175	
	Raytheon	74LS175	
	Signetics	74LS175	
	TI	SN74LS175	
SN74LS181	Fairchild	93S41	
	Motorola	SN74LS181	
	Raytheon	74LS181	
	Signetics	74LS181	
	TI	SN74LS181	
SN74LS190	Fairchild	74LS190	
	Motorola	SN74LS190	
	National	DM74LS190	
	Raytheon	74LS190	
	Signetics	74LS190	
	TI	SN74LS190	
SN74LS191	Fairchild	74LS191	
	Motorola	SN74LS191	
	National	DM74LS191	
	Raytheon	74LS191	
	Signetics	74LS191	
	TI	SN74LS191	
SN74LS192	Fairchild	74LS192	
	Motorola	SN74LS192	
	National	DM74LS192	
	NEC America	μPB74LS192	
	Raytheon	74LS192	
	Signetics	74LS192	
	TI	SN74LS192	
SN74LS193	Fairchild	74LS193	
	Motorola	SN74LS193	
	National	DM74LS193	
	NEC America	μPB74LS193	
	Raytheon	74LS193	
	Signetics	74LS193	
	TI	SN74LS193	
SN74LS194A	Fairchild	74LS194	
	Hitachi	HD74LS194A	
	Motorola	SN74LS194A	
	NEC America	μPB74LS194	
	Raytheon	74LS194A	
	Signetics	74LS194A	
	TI	SN74LS194A	
SN74LS195A	Fairchild	74LS195	
	Hitachi	HD74LS195A	
SN74LS195A	Motorola	SN74LS195A	
	NEC America	μPB74LS195	
	Raytheon	74LS195A	
	Signetics	74LS195A	
	TI	SN74LS195A	
SN74LS240	Fairchild	74LS240	
	MMI	**74LS240**	**768**
	Motorola	SN74LS240	
	Raytheon	**74LS240**	**522**
	Signetics	74LS240	
	TI	SN74LS240	
SN74LS241	Fairchild	74LS241	
	MMI	**74LS241**	**768**
	Motorola	SN74LS241	
	Raytheon	**74LS241**	**525**
	Signetics	74LS241	
	TI	SN74LS241	
SN74LS242	Fairchild	74LS242	
	Motorola	SN74LS242	
	Raytheon	**74LS242**	**528**
	Signetics	74LS242	
	TI	SN74LS242	
SN74LS243	Fairchild	74LS243	
	Motorola	SN74LS243	
	Raytheon	**74LS243**	**528**
	Signetics	74LS243	
	TI	SN74LS243	
SN74LS244	Fairchild	74LS244	
	MMI	**74LS244**	**768**
	Motorola	SN74LS244	
	Raytheon	**74LS244**	**525**
	Signetics	74LS244	
	TI	SN74LS244	
SN74LS245	Motorola	SN74LS245	
SN74LS251	Fairchild	74LS251	
	Hitachi	HD74LS251	
	Motorola	SN74LS251	
	National	DM74LS251	
	NEC America	μPB74LS251	
	Raytheon	74LS251	
	Signetics	74LS251	
	TI	SN74LS251	
SN74LS253	Fairchild	74LS253	
	Hitachi	HD74LS253	
	Motorola	SN74LS253	
	National	DM74LS253	
	NEC America	μPB74LS253	
	Raytheon	74LS253	
	Signetics	74LS253	
	TI	SN74LS253	
SN74LS257	Fairchild	74LS257	
	Motorola	SN74LS257A	
	National	DM74LS257	
	NEC America	μPB74LS257	
	Raytheon	74LS257	
	Signetics	74LS257	
	TI	SN74LS257A	
SN74LS258	Fairchild	74LS258	
	Motorola	SN74LS258A	
	National	DM74LS258	
	NEC America	μPB74LS258	
	Raytheon	74LS258	
	Signetics	74LS258	
	TI	SN74LS258A	
SN74LS273	Fairchild	74LS273	
	Motorola	SN74LS273	
	Signetics	74LS273	
	TI	SN74LS273	
SN74LS299	Fairchild	74LS299	
	Motorola	SN74LS299	
	Raytheon	**74LS299**	**533**
	TI	SN74LS299	
SN74LS322	Fairchild	74LS322	
	Motorola	SN74LS322	
	TI	SN74LS322	
SN74LS323	Fairchild	74LS323	
	Motorola	SN74LS323	
	Raytheon	**74LS323**	**540**
	TI	SN74LS323	
SN74LS373	Fairchild	74LS373	
	MMI	**74LS373**	**505**
	Motorola	SN74LS373	
	Raytheon	**74LS373**	**543**
	Signetics	74LS373	
	TI	SN74LS373	
SN74LS374	Fairchild	74LS374	
	MMI	**74LS374**	**505**
	Motorola	SN74LS374	
	Raytheon	**74LS374**	**543**
	TI	SN74LS374	
SN74LS377	Fairchild	74LS377	
	Motorola	SN74LS377	
	Raytheon	**74LS377**	**549**
	Signetics	74LS377	
	TI	SN74LS377	
SN74LS378	Fairchild	74LS378	
	Signetics	SN74LS378	
	TI	SN74LS378	
SN74LS379	Fairchild	74LS379	
	Motorola	SN74LS379	
	TI	SN74LS379	
SN74LS381	TI	SN74LS381	
SN74LS384	Fairchild	74LS384	
	Motorola	SN74LS384	
	TI	SN74LS384	
SN74LS385	Motorola	SN74LS385	
	TI	SN74LS385	
SN74LS399	Motorola	SN74LS399	
	TI	SN74LS399	
SN74LS424	TI	SN74LS424	
SN74LS568	Motorola	SN74LS568	
SN74LS569	Motorola	SN74LS569	
♦SN74LS670	Fairchild	74LS670	
	Motorola	SN74LS670	
	National	DM74LS670	
	Raytheon	74LS670	
	Signetics	74LS670	
	TI	SN74LS670	
SN74S138	Fairchild	74S138	
	Mitsubishi	M5S138	
	National	DM74S138	
	Signetics	74S138	
	TI	SN74S138	
SN74S139	Fairchild	74S139	
	National	DM74S139	
	Signetics	74S139	
	TI	SN74S139	
SN74S151	Fairchild	74S151	
	Hitachi	HD74S151	
	Mitsubishi	M5S151	
	National	DM74S151	
	Signetics	74S151	
	TI	SN74S151	
SN74S153	Fairchild	74S153	
	Mitsubishi	M5S153	
	National	DM74S153	
	Signetics	74S153	
	TI	SN74S153	
SN74S157	Fairchild	74S157	
	Mitsubishi	M5S157	
	National	DM74S157	
	Signetics	74S157	
	TI	SN74S157	
SN74S158	Fairchild	74S158	
	Mitsubishi	M5S158	
	National	DM74S158	
	Signetics	74S158	
	TI	SN74S158	
SN74S160	Fairchild	93S10	
SN74S161	Fairchild	93S16	
SN74S174	Fairchild	74S174	
	Hitachi	HD74S174	
	Mitsubishi	M5S174	
	National	DM74S174	
	Signetics	74S174	
	TI	SN74S174	
SN74S175	Fairchild	74S175	
	Hitachi	HD74S175	
	Mitsubishi	M5S175	
	National	DM74S175	
	Signetics	74S175	
	TI	SN74S175	
SN74S181	Fairchild	74S181	
		93S41	
	Hitachi	HD74S181	
	Mitsubishi	M5S181	
	Signetics	74S181	
	TI	SN74S181	
SN74S194	Fairchild	74S194	
	Signetics	74S194	
	TI	SN74S194	
SN74S195	Fairchild	93S00	
SN74S195	National	DM74S195	
	Signetics	74S195	
	TI	SN74S195	
SN74S240	Fairchild	74S240	
	MMI	**74S240**	**768**
	Raytheon	74S240	
	TI	SN74S240	
SN74S241	Fairchild	74S241	
	MMI	**74S241**	**768**
	Raytheon	74S241	
	TI	SN74S241	
SN74S244	**MMI**	**74S244**	**768**
	Raytheon	74S244	
SN74S251	Fairchild	74S251	
	Hitachi	HD74S251	
	Mitsubishi	M5S251	
	National	DM74S251	
	Signetics	74S251	
	TI	SN74S251	
SN74S253	Fairchild	74S253	
	National	DM74S253	
	Signetics	74S253	
SN74S257	Fairchild	74S257	
	Mitsubishi	M5S257	
	National	DM74S257	
	Signetics	74S257	
	TI	SN74S257	
SN74S258	Fairchild	74S258	
	Mitsubishi	M5S258	
	Signetics	74S258	
	TI	SN74S258	
SN74S289	Fairchild	74S289	
	NEC Micro	μPB2289	
SN74123	Fairchild	74123	
	Mitsubishi	M53323	
	Motorola	MC74123	
	National	DM74123	
	NEC America	μPB74123	
	Signetics	74123	
	TI	SN74123	
	TRW	74123	
SN74154	Fairchild	74154	
	Mitsubishi	M53354	
	Motorola	MC74154	
	National	DM74154	
	NEC America	μPB74154	
	Signetics	74154	
	TI	SN74154	
	TRW	74154	
SN74157	Fairchild	74157	
	Hitachi	HD74157	
	Mitsubishi	M53357	
	Motorola	MC74157	
	National	DM74157	
	NEC America	μPB74157	
	Signetics	74157	
	TI	SN74157	
SN74160	Fairchild	74160	
	Hitachi	HD74160	
	Mitsubishi	M53360	
	Motorola	MC74160	
	National	DM74160	
	Signetics	74160	
	TI	SN74160	
	TRW	74160	
SN74161	Fairchild	74161	
	Hitachi	HD74161	
	Mitsubishi	M53361	
	Motorola	MC74161	
	National	DM74161	
	NEC America	μPB74161	
	Signetics	74161	
	TI	SN74161	
	TRW	74161	
SN74162	Fairchild	74162	
	Hitachi	HD74162	
	Mitsubishi	M53362	
	Motorola	MC74162	
	National	DM74162	
	Signetics	74162	
	TI	SN74162	
	TRW	74162	
SN74163	Fairchild	74163	
	Hitachi	HD74163	
	Mitsubishi	M53363	
	Motorola	MC74163	

♦ Discontinued

The manufacturers report their devices can be used as direct replacements.
Performance details often differ, so compare the specifications considering your requirements.

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Manufacturer Device	Replacement Source	Device	IC Master Page
SN74163	National	DM74163	
	Signetics	74163	
	TI	SN74163	
	TRW	74163	
SN74174	Fairchild	54174	
		74174	
	Hitachi	HD74174	
	Mitsubishi	M53374	
	Motorola	MC54174	
		MC74174	
	National	DM54174	
		DM74174	
	Signetics	54174	
		74174	
	TI	SN54174	
		SN74174	
SN74175	Fairchild	74175	
	Hitachi	HD74175	
	Mitsubishi	M53375	
	Motorola	MC74175	
	National	DM74175	
	NEC America	μPB74175	
	Signetics	74175	
	TI	SN74175	
SN74181	Fairchild	74181	
	Mitsubishi	M53381	
	Motorola	MC74181	
	National	DM74181	
	NEC America	μPB74181	
	Signetics	74181	
	TI	SN74181	
SN74182	Fairchild	74182	
	Mitsubishi	M53382	
	Motorola	MC74182	
	National	DM74182	
	NEC America	μPB74182	
	Signetics	74182	
	TI	SN74182	
SN74192	Fairchild	74192	
	Mitsubishi	M53392	
	Motorola	MC74192	
	National	DM74192	
	NEC America	μPB74192	
	Signetics	74192	
	TI	SN74192	
SN74193	Fairchild	74193	
	Mitsubishi	M53393	
	Motorola	MC74193	
	National	DM74193	
	NEC America	μPB74193	
	Signetics	74193	
	TI	SN74193	
SN74194	Fairchild	74194	
	Hitachi	HD74194	
	Motorola	MC74194	
	National	DM74194	
	Signetics	74194	
	TI	SN74194	
SN74195	Fairchild	74195	
	Motorola	MC74195	
	National	DM74195	
	NEC America	μPB74195	
	Signetics	74195	
	TI	SN74195	
SN74259	TI	SN74259	
SN7489	Fairchild	7489	
	Mitsubishi	M53289	
	National	DM7489	
	TI	SN7489	
	TRW	7489	
SN75107	Fairchild	75107	
	TI	SN75107	
SN75108	Fairchild	75108	
	TI	SN75108	
SN75109	Fairchild	75109	
	TI	SN75109	
SN75110	Fairchild	75110	
	TI	SN75110	
SN7520	Fairchild	75S20	
SN75207	Fairchild	75207	
	TI	SN75207	
SN75208	Fairchild	75208	
SN75208	TI	SN75208	
SN7521	Fairchild	75S20	
SN75234	Fairchild	75S234	
	TI	SN75234	
SN75235	TI	SN75235	
SN75238	Fairchild	75238	
	TI	SN75238	
SN7524	Fairchild	75S24	
SN75325	Fairchild	75325	
	TI	SN75325	
SSS1408	AD	AD1408	
	Datel	**DAC-IC8BC**	**671**
	PMI	SSS1408	
SSS1508	**Datel**	**DAC-IC8BM**	**671**
	PMI	SSS1508	
SSS725	PMI	SSS725	
SSS741	PMI	OP-02	
		SSS741	
SSS747	PMI	OP-04	
		SSS747	
TMS2812	Plessey	MP2812	
0026	TI	SN75369	
1002	Mostek	MK1002	
1101	Mostek	MK4007	
1402	National	MM1402	
	Nortec	1402	
	Synertek	SY1402	
1403	National	MM1403	
	Nortec	1403	
	Synertek	SY1403	
1404	National	MM1404	
	Nortec	1404	
	Synertek	SY1404	
1408	**Datel**	**DAC-IC8BC**	**671**
	PMI	SSS1408	
1458	Exar	XR1458	
	Fairchild	μA1458	
1488	Exar	XR1488	
	Motorola	MC1488	
	National	DS1488	
	Raytheon	RC1488	
	Signetics	MC1488	
	Silicon G	SG1488	
	TI	SN75188	
1489	Exar	XR1489	
	National	DS1489	
	Raytheon	RC1489	
	Signetics	MC1489	
	Silicon G	SG1489	
	TI	SN75189	
1489A	TI	SN75189A	
1508	**Datel**	**DAC-IC8BM**	**671**
	PMI	SSS1508	
1558	Exar	XR1558	
	Fairchild	μA1558	
1702	Intel	1702A	
2101	EA	EA2101	
	Fairchild	3538	
	Intel	2101	
	Intersil	7101	
	National	MM2101	
	NEC Micro	**μPD2101**	**1586**
	Signetics	2101	
	Synertek	SY2101	
2102	**Fairchild**	**2102**	**1275**
	National	MM2102	
	NEC Micro	**μPD2102**	**1591**
	Signetics	2102	
2111	EA	EA2111	
	Intel	2111	
	National	MM2111	
	Signetics	2111	
	Synertek	SY2111	
2112	EA	EA2112	
	Intel	2112	
	Intersil	7112	
	National	MM2112	
	Signetics	2112	
	Synertek	SY2112	
2401	Synertek	SY2401	
25LS240	Raytheon	25LS240	
25LS373	Raytheon	25LS373	
2702	Synertek	SY2102	
2708	EA	EA2708	
	Fairchild	**2708**	**1282**
	Fujitsu	MB8518	
2708	Intel	2708	
	Motorola	MCM2708	
	National	MM2708	
	TI	TMS2708	
2841	Fairchild	3341A	
2847	Fairchild	3347	
29700	MMI	29700	
31L01	MMI	L5560	
		L6560	
	Signetics	**N82S25**	**1678**
31L0101	Signetics	N8225	
3101	NEC America	μPB2089	
	Signetics	82S25	
	TI	SN7489	
3101A	NEC America	μPB2289	
	Signetics	3101A	
	TI	SN54S289	
		SN74S289	
3114	TI	TMS3114	
3341	Fairchild	3341	
5889	Fairchild	5489	
	National	DM5489	
	TI	SN5489	
715	Fairchild	μA715	
723	**Fairchild**	**μA723**	**934**
	Intersil	723	
	Motorola	MC1723	
	Raytheon	RC723	
		RM723	
	RCA	CA723	
	Signetics	μA723	
	Silicon G	SG723	
725	Fairchild	μA725	
	PMI	SSS725	
733	Fairchild	μA733	
	Motorola	MC1733	
	Silicon G	SG733	
741	Fairchild	μA741	
	Intersil	741	
	Motorola	MC1741	
	PMI	OP-02	
		SSS741	
	Raytheon	RC741	
		RM741	
	RCA	CA741	
	Silicon G	SG741	
74164	Fairchild	74164	
	Hitachi	HD74164	
	Mitsubishi	M53364	
	National	DM74164	
	NEC America	μPB74164	
	Signetics	74164	
	TI	SN74164	
747	Fairchild	μA747	
	Motorola	MC1747	
	PMI	OP-04	
		SSS747	
	Raytheon	RC747	
		RM747	
	RCA	CA747	
	Silicon G	SG747	
748	Fairchild	μA748	
	Intersil	748	
	Motorola	MC1748	
	Raytheon	RC748	
		RM748	
	RCA	CA748	
	Silicon G	SG748	
8048	**NEC Micro**	**μPD8048**	**2098**
8085A	**NEC Micro**	**μPD8085A**	**2133**
8155	**NEC Micro**	**μPD8155**	**2164**
8212	**NEC Micro**	**μPB8212**	**2172**
		μPB88212	
8214	**NEC Micro**	**μPB8214**	**2178**
8216	**NEC Micro**	**μPB8216**	**2184**
8224	NEC Micro	μPB224	
		μPB8224	**2188**
8226	**NEC Micro**	**μPB8226**	**2184**
8228	**NEC Micro**	**μPB8228**	**2193**
8238	**NEC Micro**	**μPB8238**	**2193**
8251	**NEC Micro**	**μPD8251**	**2204**
8255	**NEC Micro**	**μPD8255**	**2229**
8257	**NEC Micro**	**μPD8257**	**2236**
8304	Intel	8226	1946
8355	**NEC Micro**	**μPD8355**	**2269**
9LS298	Fairchild	9LS298	
9LS298	Raytheon	9LS298	
9050	TI	TMS4050	
9060	Fujitsu	MB8107	
	NEC Micro	**μPD411**	**1547**
	TI	TMS4060	
9080A	Intel	8080A	
	National	DP8080A	
	NEC Micro	**μPD8080A**	**2119**
	TI	TMS8080A	
91L01	**NEC Micro**	**μPD2101**	**1586**
91L02	**Fairchild**	**21L02**	**1275**
	National	MM2102	
	NEC Micro	**μPD2102**	**1591**
	Signetics	2102	
91L11	**NEC Micro**	**μPD2111**	**1595**
9101	Intersil	7101	
	National	MM2101	
	NEC Micro	**μPD2101AL**	**1586**
9102	**Fairchild**	**2102**	**1275**
	National	MM2102	
	NEC Micro	**μPD2102**	**1591**
	Signetics	2102	
	Synertek	SY2102	
9107	**NEC Micro**	**μPD411**	**1547**
9111	Intersil	7111	
	National	MM2111	
	NEC Micro	**μPD2111**	**1595**
9112	Intersil	7112	
	National	MM2112	
9114	**AMI**	**S2114**	**1196**
	Fujitsu	MB8114	
9124	**AMI**	**S2114**	**1196**
♦9145	**Harris**	**HM6504**	**1363**
♦9151	TI	TMS4051	
9208	Fairchild	3508	
	Mostek	MK30000	
9214	Mostek	MK2600	
9216	Fairchild	3516E	
	NEC Micro	**μPD2316E**	**1633**
9217	**AMI**	**S6831A**	
			1215,1806
9218	**AMI**	**S4216B**	**1209**
		S6831B	
			1215,1806
93L00	Fairchild	93L00	
93L01	Fairchild	93L01	
93L08	Fairchild	93L08	
93L09	Fairchild	93L09	
93L10	Fairchild	93L10	
93L11	Fairchild	93L11	
93L12	Fairchild	93L12	
93L14	Fairchild	93L14	
93L16	Fairchild	93L16	
93L18	Fairchild	93L18	
93L21	Fairchild	93L21	
93L22	Fairchild	93L22	
93L24	Fairchild	93L24	
93L28	Fairchild	93L28	
93L34	Fairchild	93L34	
93L38	Fairchild	93L38	
93L41	Fairchild	93L41	
93L60	National	DM75L60	
		DM85L60	
93L66	National	DM75L63	
		DM85L63	
9300	Fairchild	9300	
	Raytheon	RM9300	
	TI	SN54195	
		SN74195	
9301	Fairchild	9301	
	TI	SN29301	
		SN39301	
9304	Fairchild	9304	
	Raytheon	RM9304	
9308	Fairchild	9308	
	Raytheon	RM9308	
	TI	SN29308	
		SN39308	
9309	Fairchild	9309	
	TI	SN29309	
		SN39309	
9310	Fairchild	9310	
	Raytheon	RM9310	
	TI	SN54160	
		SN74160	
9311	Fairchild	9311	

♦ Discontinued

Bold face device numbers indicate manufacturers data is provided in the IC Master on the pages noted.

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Manufacturer Device	Replacement Source	Device	IC Master Page
9311	Raytheon	RM9311	
	TI	SN54154	
		SN74154	
9312	Fairchild	9312	
	Raytheon	RM9312	
	TI	SN29312	
		SN39312	
9314	Fairchild	9314	
9316	Fairchild	9316	
	Raytheon	RM9316	
	TI	SN54161	
		SN74161	
9318	Fairchild	9318	
	TI	SN54148	
		SN74148	
9321	Fairchild	9321	
9322	Fairchild	9322	
	Raytheon	RM9322	
	TI	SN54157	
		SN74157	
9324	Fairchild	9324	
9328	Fairchild	9328	
9334	Fairchild	9334	
	TI	SN54259	
		SN74259	
9338	Fairchild	9338	
9340	Fairchild	9340	
9341	Fairchild	9341	
	Raytheon	RM9341	
	TI	SN54181	
		SN74181	
93415	Fujitsu	MBM93415	
	Intel	**2115**	**1416**
	NEC America	MBM93415	
	NEC Micro	μPB2205	
	TI	SN54S314	
		SN74S314	
9342	Fairchild	9342	
	Raytheon	RM9342	
	TI	SN54182	
		SN74182	
9360	Raytheon	RM9360	
9366	Raytheon	RM9366	
9401	Synertek	SY2401	
96L02	Fairchild	96L02	
9600	Fairchild	9600	
9601	Fairchild	9601	
	Raytheon	RF9601	
	TI	SN29601	
9602	Fairchild	9602	
	Raytheon	RF9602	
9614	Fairchild	9614	
	TI	SN55114	
		SN75114	
9615	Fairchild	9615	
	TI	SN55115	
		SN75115	
9616	Fairchild	9616	
9617	Fairchild	9617	
9620	Fairchild	9620	
9621	Fairchild	9621	
	Raytheon	RM9621	

American Microsystems, Inc.

S1103A	Intel	1103A
	Synertek	1103A
S1413	SSS	SCL5430
S1424A	SSS	SCL5403
S146	Intel	1103-146
♦S1670	Motorola	MC1160
S1757	GI	AY3-1014A
		AY3-1015
		AY5-1013A
	SMC	COM2502
	Western	TR1402
S1883	SMC	COM2017
	TI	TMS6011
	Western	TR1602
♦S2102	Motorola	MCM6605
S2181	Mostek	MK1002
S2181	Mostek	MK4116
S2181A	TI	TMS3113
S2182	Fairchild	3347
	SMC	SR5015
S2183	SMC	SR5015
S2185	SMC	SR5015
S2222	Nortec	2222
	Signetics	N2222
		S2222
	SSS	SCM5522
S2350	SMC	COM2601
S2470	GI	AY1-1006
S2555	Nitron	NC1183
S2556	Nitron	NC1184
S2559	Mostek	MK5085
♦S2566	Motorola	MC1182
S3102	SGS	M330
S3514	Fairchild	3515
	Mostek	MK2600
♦S4006	Mostek	MK4006
♦S4008	Mostek	MK4008
S4016	AMD	9114
		9124
	Fairchild	**2114** **1281**
	Rockwell	R2114
S4021	TI	TMS4060
♦S4096	EA	EA4096
	EMM/Semi	RO3-4096
	Fairchild	4096
	Mostek	MK4096
S4264	Mostek	MK36000
S5101	Harris	HM5101
		HM6501 **1356**
	Motorola	**MCM145101** **1536**
	RCA	CDP1822S
	SSS	SCM5101
S5232	Mostek	MK2500
		MK2600
	National	MM5232
S6508	**Harris**	**HM6508** **1366**
S6518	**Harris**	**HM6518** **1379**
S68A00	**Motorola**	**MC68A00** **2002**
S68A10	Motorola	MC68A10
S68A21	**Motorola**	**MC68A21** **1991**
S68B00	**Motorola**	**MC68B00** **2002**
S68B10	Motorola	MC68B10
S68B21	**Motorola**	**MC68B21** **1991**
S6800	**Fairchild**	**F6800** **1886,1888**
	Motorola	M6800
S6810	**Fairchild**	**F6810** **1887,1888**
	Motorola	MCM6810
S6820	**Fairchild**	**F6820** **1887**
	Motorola	MC6820
S6830	Fairchild	F6380
♦S6830	Motorola	MCM6830
S6831A	Mostek	MK31000
S6831B	Mostek	MK34000
S6850	**Fairchild**	**F6850** **1887,1891**
	Motorola	**MC6850** **1977**
S8499	SMC	CG4100
S8564	Fairchild	3260
S8772	Fairchild	3515
S8865	GI	RO5-8192
S8996	EMM/Semi	RO3-16384
	GI	RO3-16384
	Nortec	8996
S9900	TI	TMS9900
S9901	TI	TMS9901
S9902	TI	TMS9902
S9903	TI	TMS9903
S9940	TI	TMS9940
S9980	TI	TMS9980

Analog Devices

ADC0816	TI	ADC0816
AD101	AMD	LM101
	Fairchild	μA101
	Motorola	LM101
	National	**LM101** **1035**
	RCA	CA101
	Signetics	LM101
	Silicon G	SG101
AD108	AMD	LM108
	Fairchild	μA108
AD108	Motorola	LM108
	National	**LM108** **1035**
	Raytheon	LM108
	RCA	CA108
	Signetics	LM108
	Silicon G	SG108
AD111	Motorola	LM111
	National	LM111
	Raytheon	LM111
	RCA	CA111
	Signetics	LM111
	Silicon G	SG111
AD201	AMD	LM201
	Fairchild	μA201
	Motorola	LM201
	National	LM201
	RCA	CA201
	Signetics	LM201
	Silicon G	SG201
AD208	AMD	LM208
	Fairchild	μA208
	National	LM208
	Raytheon	LM208
	RCA	CA208
	Silicon G	SG208
AD211	National	LM211
	Raytheon	LM211
	RCA	CA211
	Signetics	LM211
	Silicon G	SG211
AD2700	Hybrid Sys.	R675-4
		R675-7
AD2701	Hybrid Sys.	R675-5
		R675-8
AD2702	Hybrid Sys.	R675-3
		R675-6
AD301	AMD	LM301
	Fairchild	μA301
	Motorola	LM301
	National	LM301
	Raytheon	LM301
	RCA	CA301
	Signetics	LM301
	Silicon G	SG301
AD308	AMD	LM308
	Fairchild	μA308
	Motorola	LM308
	National	LM308
	Raytheon	LM308
	RCA	CA308
	Signetics	LM308
	Silicon G	SG308
AD311	Motorola	LM311
	National	LM311
	Raytheon	LM311
	RCA	CA311
	Signetics	LM311
	Silicon G	SG311
AD503	National	LH0042
AD506	National	LH0022
AD507	**Datel**	**AM-462-2** **687**
	Harris	**HA-2620** **980**
AD509	**Datel**	**AM-452-2** **687**
	Harris	**HA-2520** **972**
AD510	PMI	OP-07
♦AD513	National	LH0042
AD515	**Burr-Brown**	**3528** **920**
♦AD516	National	LH0022
AD532	**Burr-Brown**	**4214** **921**
AD559	**Datel**	**DAC-IC8BC** **671**
	Motorola	MC1408
		MC1508
AD562	Burr-Brown	DAC862
	Harris	HI562
	PMI	SSS562
AD562A/BCD	Analogic	MN562-AD-BCD
AD562A/BIN	Analogic	MN562-AD-BIN
AD562I/BCD	Analogic	MN562-ID-BCD
AD562I/BIN	Analogic	MN562-ID-BIN
AD562K/BCD	Analogic	MN562-KD-BCD
AD562K/BIN	Analogic	MN562-ID-BIN
AD562S/BCD	Analogic	MN562-SD-BCD
AD562S/BIN	Analogic	MN562-SD-BIN
AD563	Burr-Brown	DAC863
AD563J/BCD	Analogic	MN563-JD-BCD
AD563J/BIN	Analogic	MN563-JD-BIN
AD563K/BIN	Analogic	MN563-KD-BIN
AD563S/BCD	Analogic	MN563-SD-BCD
AD563S/BIN	Analogic	MN563-SD-BIN
AD563T/BCD	Analogic	MN563-TD-BCD
AD563T/BIN	Analogic	MN563-TD-BIN
AD583	**Datel**	**SHM-IC-1** **685**
	Harris	**HA-2425** **1020**
AD741	AMD	741
	Fairchild	μA741
	Motorola	MC1741
	National	**LM741** **1035**
	PMI	SSS741
	Raytheon	RM741
	RCA	CA741
	Signetics	μA741
AD7501	Micro Power	MP7501
AD7502	Micro Power	MP7502
	RCA	CD4052
AD7503	Micro Power	MP7503
AD7505	Siliconix	DG507
AD7506	Harris	HI506
	Micro Power	MP7506
	RCA	CD4067
	Siliconix	DG506
AD7507	Harris	HI507
	Micro Power	MP7507
	RCA	CD4097
AD7510	Micro Power	MP7510
	PMI	SSS7510
AD7511	Micro Power	MP7511
	PMI	SSS7511
AD7512	Micro Power	MP7512
AD7513	Micro Power	MP7513
	Siliconix	DG200
AD7516	Fairchild	F4016
	Micro Power	MP7516
	Mitel	SIL4016
	Motorola	MC14016
	National	**CD4016** **1076**
	RCA	CD4016
	Solitron	CM4016
	SSS	SCL4016
	TI	TP4016
AD7519	Micro Power	MP7519
AD7520	**Datel**	**DAC-HA10B** **675**
	Hybrid Sys.	DAC331-10
		DAC331-8
	Intersil	AD7520
	Micro Power	MP7520
AD7521	**Datel**	**DAC-HA12B** **675**
	Hybrid Sys.	DAC331-10
		DAC331-8
	Intersil	AD7521
	Micro Power	MP7521
AD7522	Micro Power	MP7522
AD7523	Hybrid Sys.	DAC331-8
	Micro Power	MP7523
AD7530	**Datel**	**DAC-HA10B** **675**
	Hybrid Sys.	DAC331-10
		DAC331-8
	Intersil	AD7530
AD7531	**Datel**	**DAC-HA12B** **675**
	Hybrid Sys.	DAC331-10
		DAC331-8
	Intersil	AD7531
AD7533	Hybrid Sys.	DAC331-10
		DAC331-8
AD7541	Hybrid Sys.	DAC331-12
	Intersil	ICL7541
	Micro Power	MP7621
AD7550	Micro Power	MP7550
AD7570	Micro Power	MP7570
DAC80	Hybrid Sys.	DAC335

Beckman Instruments, Helipot Division

7521	Hybrid Sys.	DAC331-12
7580	Datel	DAC-HZ12B
	Hybrid Sys.	DAC335
877-80	Micro Net	DAC85
877-85	Datel	DAC-HZ12B
	Hybrid Sys.	DAC335
	Micro Net	DAC85

♦ Discontinued

The manufacturers report their devices can be used as direct replacements.
Performance details often differ, so compare the specifications considering your requirements.

Burr-Brown Research

Manufacturer Device	Replacement Source	Device	IC Master Page
ADC80	Micro Net	ADC80	
ADC82	Hybrid Sys.	ADC542	
ADC84	**Datel**	**ADC-HZ12BGC**	**669**
	Hybrid Sys.	ADC581	
	Micro Net	MNADC84	
		MN5240	
ADC85	Datel	ADC-HZ12BGZ	
	Hybrid Sys.	ADC581	
	Micro Net	ADC85	
		MNADC85	
		MN5240	
DAC120	AD	DAC120	
DAC80	AD	DAC80	
	Beckman	7580	
	Datel	DAC-HZ12B	
	Hybrid Sys.	DAC335	
	Micro Net	DAC80	
	National	**DAC1280**	**1073,1074**
DAC85	AD	DAC80	
	Beckman	877-85	
	Datel	DAC-HZ12B	
	Hybrid Sys.	DAC335	
	Micro Net	DAC85	
	National	**DAC1285**	**1073,1074**
DAC85/CCD	**National**	**DAC1287**	**1074**
MPC16S	**Datel**	**MX-1606**	**683**
	Harris	HI506A	
MPC4D	**Datel**	**MXD-409**	**683**
	Harris	HI509A	
MPC8D	**Datel**	**MXD-807**	**683**
	Harris	HI507A	
MPC8S	**Datel**	**MX-808**	**683**
	Harris	HI508A	
SHC23	**National**	**LH0023**	**1073**
SHC298AM	**Datel**	**SHM-LM-2**	**685**
3503	AD	AD540	
3505	**Datel**	**AM-450-2**	**687**
	Harris	**HA-2505**	**966**
3506	**Datel**	**AM-460-2**	**687**
	Harris	**HA-2605**	**976**
3507	AD	AD509	
	Datel	**AM-452-2**	**687**
	Harris	**HA-2525**	**972**
3508	AD	AD507	
	Datel	**AM-462-2**	**687**
	Harris	**HA-2625**	**980**
3528	AD	AD515	
3542	AD	AD3542	
4201	AD	AD530	
4205	AD	AD532	
4213	AD	AD532	

Cherry Semiconductor

CS555	Exar	XR555

Data Devices Corporation

ADH-030	HyComp	DA4000

Datel Systems

ADC-EK10B	Teledyne S	8701	
ADC-EK12B	Teledyne S	8702	
ADC-EK12D	Teledyne S	8750	
ADC-EK8B	Teledyne S	8700	
ADC-ET10B	Teledyne S	8704	
ADC-ET12B	Teledyne S	8705	
ADC-ET8B	Teledyne S	8703	
ADC-HX12B	Hybrid Sys.	ADC581	
	Micro Net	MNADC84	
		MNADC85	
ADC-HZ12	Micro Net	MN5240	
ADC-HZ12B	**Burr-Brown**	**ADC85**	**658**
	Hybrid Sys.	ADC581	
	Micro Net	MNADC84	
		MNADC85	
AM-405-2	**Harris**	**HA-2055**	**960**
AM-406-2	**Harris**	**HA-2065**	**962**
AM-450-2	Burr-Brown	3505	
	Harris	**HA-2505**	**966**
AM-452-2	AD	AD509	
	Burr-Brown	3507	
	Harris	**HA-2525**	**972**
	Teledyne P	TP1322	
AM-460-2	Burr-Brown	3506	
	Harris	**HA-2605**	**976**
AM-462-2	AD	AD507	
	Burr-Brown	3508	
	Harris	**HA-2625**	**980**
	Teledyne P	TP1321	
AM-464-2	**Harris**	**HA-2645**	**984**
AM-490-2	**Harris**	**HA-2905**	**996**
AM-500	Teledyne P	TP1430	
DAC-HA10B	Hybrid Sys.	DAC331-10	
DAC-HA12B	Hybrid Sys.	DAC331-12	
DAC-HZ12B	Beckman	7380	
	Burr-Brown	**DAC80**	**658**
	Hybrid Sys.	DAC335	
	Micro Net	DAC80	
		DAC85	
DAC-HZ12BM	Beckman	877-85	
	Burr-Brown	**DAC85**	**658**
	Micro Net	DAC85	
DAC-IC10	Motorola	MC3410	
MX-1606	Harris	HI506A	
MX-808	Harris	HI508A	
MXD-409	Harris	HI509A	
MXD-807	Harris	HI507A	
SHM-IC-1	AD	AD583	
	Harris	**HA-2425**	**1020**
	Teledyne P	TP4856	
VFQ-1	Teledyne S	9400	

Dionics Inc.

DI250	Cherry	CS250
DI260	Cherry	CS260
DI502	Sprague	UDN-6144
DI507	Sprague	UDN-6164
DI512	Sprague	UDN-6184

Electronic Arrays

EA2101	Fairchild	3538	
EA2107	Fujitsu	MB8107	
EA2308	TI	TMS4700	
EA2316A	**AMI**	**S6831A**	**1215,1806**
EA2316E	**AMI**	**S4216B**	**1209**
		S6831B	**1215,1806**
EA2708	AMD	2708	
	Fairchild	**2708**	**1282**
	Fujitsu	MB8518	
	Intel	2708	
	Motorola	MCM2708	
	National	MM2708	
	TI	TMS2708	
♦EA3000	AMI	S8773	
♦EA3001	AMI	S8773	
♦EA3100	AMI	S8773	
♦EA3101	AMI	S8773	
♦EA3132	AMI	S8773	
♦EA3300	AMI	S8772	
♦EA3307	AMI	S8772	
EA3800	AMI	S8773	
EA4000	AMI	S8771	
	GI	RO3-5120	
EA4004	AMI	S8771	
EA4015	AMI	S8771	
EA4016	AMI	S8771	
EA4060	TI	TMS4060	
EA4096	EMM/Semi	RO3-4096	
	Mostek	MK4096	
EA4122	Fujitsu	MB8107	
EA4600	AMI	S6831C	
	Synertek	SY4600	
EA4900	Mostek	MK28000	
EA5316	AMI	S1998	
2102	**Fairchild**	**2102**	**1275**
2316	Rockwell	R2316	
8316	Fairchild	3516E	

EMM Semi., Div. of Electronic Memories & Magnetics

♦1217	GI	RA3-1217	
♦1218	GI	RA3-1218	
2114	**AMI**	**S2114**	**1196**
	Fairchild	**2114**	**1281**
	Intel	2114	
	Rockwell	R2114	
3539	Fairchild	3539	
4200	**NEC Micro**	**μPD410**	**1600**
4202	**NEC Micro**	**μPD410**	**1600**

Exar Integrated Systems

XR1310	Motorola	MC1310	
	National	LM1310	
XR1458	Fairchild	μA1458	
	Motorola	MC1458	
	National	LM1458	
	Signetics	MC1458	
	Silicon G	SG1458	
	TI	MC1458	
XR146	**National**	**LM146**	**1035**
XR1488	Fairchild	μA1488	
	Motorola	MC1488	
	Signetics	MC1488	
	Silicon G	SG1488	
XR1489A	Fairchild	μA1489A	
	Motorola	MC1489A	
	National	DS1489A	
	Signetics	MC1489A	
	Silicon G	SG1489	
XR1524	**Silicon G**	**SG1524**	**1128**
	TI	SG1524	
XR1558	Fairchild	μA1558	
	Motorola	MC1558	
	National	LM1558	
	Signetics	MC1558	
	Silicon G	SG1558	
	TI	MC1558	
XR1800	National	LM1800	
XR2003	Signetics	NE5503	
		ULN2003	
	Silicon G	SG2003	
XR2201	Fairchild	9665	
	SGS	L201	
	Signetics	NE5501	
		ULN2001	
	Silicon G	SG2001	
	Sprague	ULN-2001	
		ULS-2201	
	TI	ULN2001	
XR2202	Fairchild	9666	
	Motorola	ULN2002	
	SGS	L202	
	Signetics	NE5502	
		ULN2002	
	Silicon G	SG2002	
	Sprague	ULN-2002	
		ULS-2002	
	TI	ULN2002	
XR2203	Fairchild	9667	
	Motorola	ULN2003	
	SGS	L203	
	Silicon G	SG2003	
	Sprague	ULN-2003	
		ULS-2003	
	TI	ULN2003	
XR2204	Fairchild	9668	
	Motorola	ULN2004	
	Signetics	NE5504	
		ULN2004	
	Sprague	ULN-2004	
		ULS-2004	
	TI	ULN2004	
XR2207	Raytheon	XR2207	
XR2211	Raytheon	XR2211	
XR2240	Fairchild	μA7240	
		7240	
	Intersil	8240	
XR246	National	LM246	
XR2524	TI	SG2524	
XR2567	Raytheon	XR2567	
XR3403	Fairchild	μA3403	
	Motorola	MC3403	
	Raytheon	RC3403	
XR346	National	LM346	
XR3503	Motorola	MC3503	
	Raytheon	RM3503	
	Silicon G	**SG3503**	**1128**
XR3524	**Silicon G**	**SG3524**	**1128**
	TI	SG3524	
XR4136	Fairchild	μA4136	
	PMI	PM4136	
	Raytheon	RC4136	
	Silicon G	SG4136	
	TI	RC4136	
XR4151	**Raytheon**	**RC4151**	**1094**
		RM4151	
		RV4151	
XR4152	Raytheon	RM4152	
		RV4152	
		SL758	
XR4156	**Raytheon**	**RC4156**	**1110**
		RM4156	
		RV4156	
XR4157	**Raytheon**	**RC4151**	**1094**
XR4194	Raytheon	RC4194	
	Silicon G	SG4194	
XR4195	Raytheon	RC4195	
XR4212	Harris	HA-4741	
	Motorola	MC4741	
XR4558	Fairchild	μA4558	
	Motorola	MC4558	
		RC4558	
	Raytheon	RC4558	
	TI	RC4558	
XR4734	Raytheon	RC4739	
XR4741	Harris	HA-4741	
	Motorola	MC4741	
	Raytheon	HA4741	
XR555	Cherry	CS555	
	Fairchild	μA555	
	Motorola	MC1455	
	National	LM555	
	Signetics	NE555	
	Silicon G	SG555	
	TI	NE555	
XR556	Fairchild	μA556	
	Motorola	MC3456	
	National	LM556	
	Raytheon	RC556	
	Silicon G	SG556	
XR567	National	LM567	
	Signetics	NE567	
XR742	Fairchild	μA742	
XR8038	Intersil	8038	

Fairchild

μAF155	AMD	LF155	
	Intersil	LF155	
	Motorola	LF155	
	National	**LF155**	**1035**
	PMI	PM155	
	Raytheon	LF155	
	Signetics	LF155	
	TI	LF155	
μAF156	AMD	LF156	
	Intersil	LF156	
	Motorola	LF156	
	National	**LF156**	**1035**
	PMI	PM156	
	Raytheon	LF156	
	Signetics	LF156	
	TI	LF156	
μAF157	AMD	LF157	
	Intersil	LF157	
	Motorola	LF157	
	National	**LF157**	**1035**
	PMI	PM157	
	Raytheon	LF157	
	Signetics	LF157	
	TI	LF157	
μAF255	AMD	LF255	

♦ Discontinued

Bold face device numbers indicate manufacturers data is provided in the IC Master on the pages noted.

Fairchild (cont'd)

Manufacturer Device	Replacement Source	Device	IC Master Page
µAF255	Intersil	LF255	
	Motorola	LF255	
	National	LF255	
	PMI	PM255	
	Raytheon	LF255	
	Signetics	LF255	
	TI	LF255	
µAF256	AMD	LF256	
	Intersil	LF256	
	Motorola	LF256	
	National	LF256	
	PMI	PM256	
	Raytheon	LF256	
	Signetics	LF256	
	TI	LF256	
µAF257	AMD	LF257	
	Intersil	LF257	
	Motorola	LF257	
	National	LF257	
	PMI	PM257	
	Raytheon	LF257	
	Signetics	LF257	
	TI	LF257	
µAF355	AMD	LF355	
	Intersil	LF355	
	Motorola	LF355	
	National	LF355	
	PMI	PM355	
	Raytheon	LF355	
	Signetics	LF355	
	TI	LF355	
µAF356	AMD	LF356	
	Intersil	LF356	
	Motorola	LF356	
	National	**LF356**	**1035,1073**
	PMI	PM356	
	Raytheon	LF356	
	Signetics	LF356	
	TI	LF356	
µAF357	AMD	LF357	
	Intersil	LF357	
	Motorola	LF357	
	National	LF357	
	PMI	PM357	
	Raytheon	LF357	
	Signetics	LF357	
	TI	LF357	
µA0801	**Datel**	**DAC-08B**	**670**
µA0802	AD	AD1408	
	Datel	**DAC-IC8B**	**671**
	Motorola	MC1408	
		MC1508	
	PMI	DAC-08	
		SSS1408	
		SSS1508	
µA101	AMD	LM101	
	Intersil	LM101	
	Motorola	LM101	
	National	**LM101**	**1035**
	RCA	CA101	
	Signetics	LM101	
	Silicon G	SG101	
	TI	LM101	
µA102	AMD	LM102	
	Intersil	LM102	
	Motorola	LM110	
	National	LM102	
	Silicon G	SG102	
µA104	Motorola	LM104	
	National	LM104	
	Raytheon	LM104	
	Silicon G	SG104	
	TI	LM104	
µA105	AMD	LM105	
	Intersil	LM105	
	Motorola	LM105	
	National	LM105	
	Raytheon	LM105	
	Silicon G	SG105	
	TI	LM105	
µA107	AMD	LM107	
	Intersil	LM107	
	Motorola	LM107	
µA107	RCA	CA107	
	Silicon G	SG107	
	TI	LM107	
µA108	AMD	LM108	
	Intersil	LM108	
	Motorola	LM108	
	National	**LM108**	**1035**
	PMI	PM108	
	Raytheon	LM108	
	RCA	CA108	
	Signetics	LM108	
	Silicon G	SG108	
µA109	Motorola	LM109	
	National	LM109	
	Raytheon	LM109	
	Signetics	LM109	
	Silicon G	SG109	
	TI	LM109	
µA110	AMD	LM110	
	Intersil	LM110	
	Motorola	LM110	
	National	LM110	
	PMI	BUF-01	
		BUF-02	
	Silicon G	SG110	
µA111	AMD	LM111	
	Intersil	LM111	
	Raytheon	LM111	
	RCA	CA111	
	Signetics	LM111	
	Silicon G	SG111	
	TI	LM111	
µA1312	Motorola	MC1312	
µA139	AMD	LM139	
	RCA	CA139	
	Silicon G	SG139	
	TI	LM139	
µA1391	Motorola	MC1391	
	RCA	CA1391	
µA1394	Motorola	MC1394	
	RCA	CA1394	
µA1458	AMD	1458	
	Exar	XR1458	
	Harris	**HA-2655**	**986**
	Motorola	MC1458	
	National	LM1458	
	NEC America	µPC1458	
	Raytheon	RC1458	
	RCA	CA1458	
	Signetics	MC1458	
	Silicon G	SG1458	
	TI	MC1458	
µA1488	Exar	XR1488	
	Signetics	MC1488	
	Silicon G	SG1488	
	TI	SN75188	
µA1489	Signetics	MC1489	
	Silicon G	SG1489	
	TI	SN85189	
µA1489A	Exar	XR1489A	
	Signetics	MC1489A	
	Silicon G	SG1489A	
	TI	SN75189A	
µA155	Motorola	LF155	
µA1558	AMD	1558	
	Exar	XR1558	
	Harris	**HA-2650**	**986**
	Motorola	MC1558	
	National	LM1558	
	Raytheon	RM1558	
	RCA	CA1558	
	Signetics	MC1558	
	Silicon G	SG1558	
	TI	MC1558	
µA156	Motorola	LF156	
µA157	Motorola	LF157	
µA201	AMD	LM201	
	Intersil	LM201	
	Motorola	LM201	
	National	LM201	
	RCA	CA201	
	Signetics	LM201	
	Silicon G	SG201	
	TI	LM201	
µA202	Intersil	LM202	
	Motorola	LM210	
µA202	Silicon G	SG202	
µA204	Motorola	LM204	
	Silicon G	SG204	
	TI	LM204	
µA205	Intersil	LM205	
	Motorola	LM205	
	National	LM205	
	Raytheon	LM205	
	Silicon G	SG205	
	TI	LM205	
µA207	AMD	LM207	
	Intersil	LM207	
	Motorola	LM207	
	National	LM207	
	Raytheon	LM207	
	RCA	CA207	
	Signetics	LM207	
	Silicon G	SG207	
	TI	LM207	
µA208	AMD	LM208	
	Intersil	LM208	
	Motorola	LM208	
	National	LM208	
	PMI	PM208	
	Raytheon	LM208	
	RCA	CA208	
	Signetics	LM208	
	Silicon G	SG208	
µA209	Motorola	LM209	
	National	LM209	
	Raytheon	LM209	
	Signetics	LM209	
	Silicon G	SG209	
	TI	LM209	
µA210	Intersil	LM210	
	Motorola	MLM210	
	Silicon G	SG210	
µA211	Intersil	LM211	
	National	LM211	
	Raytheon	LM211	
	RCA	CA211	
	Signetics	LM211	
	Silicon G	SG211	
	TI	LM211	
µA2136	Motorola	MC1352	
µA2240	Exar	XR2240	
	TI	µA2240	
µA301	AMD	LM301	
	Intersil	LM301	
	Motorola	LM301	
	National	LM301	
	Raytheon	LM301	
	RCA	CA301	
	Signetics	LM301	
	Silicon G	SG301	
	TI	LM301	
µA301A	NEC America	µPC157	
		µPC301A	
µA3018	RCA	CA3018	
µA3019	RCA	CA3019	
µA302	AMD	LM302	
	Intersil	LM302	
	Motorola	LM310	
	Silicon G	SG302	
µA3026	RCA	CA3026	
µA3036	RCA	CA3036	
µA3039	RCA	CA3039	
µA304	Motorola	LM304	
	National	LM304	
	NEC America	µPC142	
	Raytheon	LM304	
	Silicon G	SG304	
	TI	LM304	
µA3045	RCA	CA3045	
	Silicon G	SG3045	
	Sprague	ULS-2045	
µA3046	Motorola	MC3346	
	RCA	CA3046	
	Silicon G	SG3046	
	Sprague	ULN-2046	
µA305	AMD	LM305	
	Intersil	LM305	
	Motorola	LM305	
	National	LM305	
	NEC America	µPC141	
	Raytheon	LM305	
µA305	Silicon G	SG305	
	TI	LM305	
µA3054	Motorola	CA3054	
	RCA	CA3054	
	Silicon G	SG3054	
	Sprague	ULN-2054	
µA306	National	LM306	
	Raytheon	LM306	
µA3064	Motorola	MC1364	
	National	LM3064	
	RCA	CA3064	
	Sprague	ULN-2264	
µA3065	Motorola	MC1358	
	National	LM3065	
	RCA	CA3065	
	Sanyo	LA1365	
	Sprague	ULN-2165	
♦µA3066	RCA	CA3066	
♦µA3067	RCA	CA3067	
µA307	AMD	LM307	
	Intersil	LM307	
	Motorola	LM307	
	National	LM307	
	Raytheon	LM307	
	RCA	CA307	
	Signetics	LM307	
	Silicon G	SG307	
	TI	LM307	
µA3075	Motorola	MC1375	
	RCA	CA3075	
	Sprague	ULN-2129	
µA3076	RCA	CA3076	
µA308	AMD	LM308	
	Intersil	LM308	
	Motorola	LM308	
	National	LM308	
	NEC America	µPC156A	
	PMI	PM308	
	Raytheon	LM308	
	RCA	CA308	
	Signetics	LM308	
	Silicon G	SG308	
µA3081	RCA	CA3018	
	Silicon G	SG3081	
µA3086	Motorola	MC3386	
	RCA	CA3086	
	Silicon G	SG3886	
	Sprague	SLN-2086	
µA3089	RCA	CA3089	
	Siliconix	CA3089	
	Sprague	ULN-2289	
µA309	Motorola	LM309	
	Signetics	LM309	
	Silicon G	SG309	
	TI	LM309	
µA310	AMD	LM310	
	Intersil	LM310	
	Motorola	LM310	
	PMI	BUF-01	
		BUF-02	
	Silicon G	SG310	
µA311	AMD	LM311	
	Intersil	LM311	
	Motorola	LM311	
	NEC America	µPC311	
	Raytheon	LM311	
	RCA	CA311	
	Signetics	LM311	
	Silicon G	SG311	
	TI	LM311	
µA318	NEC America	µPC159A	
µA3301	Motorola	MC3301	
µA3302	Motorola	MC3302	
	Silicon G	SG3302	
µA3303	Motorola	MC3303	
µA339	AMD	LM339	
	RCA	CA339	
	Silicon G	SG339	
µA3401	Motorola	MC3401	
	RCA	CA3401	
µA3403	Exar	XR3403	
	Motorola	MC3403	
	NEC America	µPC324	
	Raytheon	RC3403	
µA3503	Exar	XR3503	
	Motorola	MC3503	

♦ Discontinued

The manufacturers report their devices can be used as direct replacements.
Performance details often differ, so compare the specifications considering your requirements.

Manufacturer Device	Replacement Source	Device	IC Master Page
Fairchild (cont'd)			
µA3503	Raytheon	RM3503	
	Silicon G	**SG3503**	**1128**
µA376	TI	LM376	
µA376T	NEC America	µPC305	
µA4136	Exar	XR4136	
	Raytheon	RC4136	
	Silicon G	SG4136	
	TI	RC4136	
µA4151	**Raytheon**	**RC4151**	**1094**
µA4558	Exar	XR4558	
	Motorola	MC4558	
	NEC America	µPC4558	
	Raytheon	RC4558	
µA555	AMD	NE555	
	Exar	XR555	
	Motorola	MC1455	
	Raytheon	RC555	
	Signetics	NE555	
	Silicon G	SG555	
	TI	NE555	
µA555T	NEC America	µPC1555	
µA556	AMD	NE556	
	Exar	XR556	
	Motorola	MC3456	
	Raytheon	RC556	
	Signetics	NE556	
	Silicon G	SG556	
	TI	NE556	
µA702	Motorola	MC1712	
	NEC America	µPC51	
		µPC51A	
	Raytheon	RC702	
		RM702	
	TI	µA702	
µA703	National	LM703	
µA705	Sprague	ULN-2278	
µA706	SGS	TBA641	
µA709	Motorola	MC1709	
	National	**LM709**	**1035**
	NEC America	µPC55A	
	Raytheon	RC709	
		RM709	
	Signetics	µA709	
	TI	µA709	
	Toshiba	TA7502	
µA710	Motorola	MC1710	
	National	LM710	
	NEC America	µPC71	
	Raytheon	RC710	
		RM710	
	Signetics	µA710	
	Silicon G	SG710	
	TI	µA710	
µA711	Motorola	MC1711	
	National	LM711	
	Raytheon	RC711	
		RM711	
	Signetics	µA711	
	Silicon G	SG711	
	TI	µA711	
µA714	AD	AD517	
µA715	AMD	715	
µA720	RCA	CA3123	
	Sprague	ULN-2137	
µA723	AMD	723	
	Hitachi	HA17723	
	Intersil	723	
	Motorola	MC1723	
	National	LM723	
	Raytheon	RC723	
		RM723	
	RCA	CA723	
	SGS	L123	
	Signetics	µA723	
	Silicon G	SG723	
	TI	µA723	
µA7240	Exar	XR2240	
µA725	AMD	725	
	NEC America	µPC154	
		µPC154A	
	PMI	PM725	
		SSS725	
	Raytheon	RC725	
µA725	Raytheon	RM725	
µA732	National	LM1305	
µA733	AMD	733	
	Hitachi	HA17733	
	Intersil	µA733	
	Motorola	MC1733	
	National	LM733	
	Raytheon	RC733	
		RM733	
	Signetics	µA733	
	Silicon G	SG733	
	TI	µA733	
µA739	Exar	XR4739	
	Raytheon	RC4739	
	SGS	TBA231	
µA740	Intersil	µA740	
		LH0042	
	Signetics	µA740	
µA741	AMD	741	
	Hitachi	HA17741	
	Intersil	741	
	Motorola	MC1741	
	National	**LM741**	**1035**
	NEC America	µPC151	
		µPC741	
	PMI	OP-02	
		PM741	
		SSS741	
	Raytheon	RC741	
		RM741	
	RCA	CA741	
	Signetics	µA741	
	Silicon G	SG741	
	Sprague	ULN-2151	
	TI	µA741	
	Toshiba	TA7504	
µA742	Exar	XR742	
µA746	National	LM746	
	RCA	CA3072	
	Sprague	ULN-2114	
		ULN-2228	
µA747	AMD	747	
	Hitachi	HA17747	
	Motorola	MC1747	
	National	LM747	
	NEC America	µPC251	
	PMI	OP-04	
		PM747	
		SSS747	
	Raytheon	RC747	
		RM747	
	RCA	CA747	
	Signetics	µA747	
	Silicon G	SG747	
	TI	µA747	
µA748	AMD	748	
	Intersil	748	
	Motorola	MC1748	
	National	**LM101**	**1035**
		LM201	
		LM748	
	Plessey	SL748	
	Raytheon	RC748	
		RM748	
	RCA	CA748	
	Signetics	µA748	
	Silicon G	SG748	
	TI	µA748	
µA749	Exar	XR4739	
µA751	Hitachi	HA17715	
µA753	Sprague	ULN-2209	
µA758	Exar	XR1800	
	Plessey	µA758	
	RCA	CA758	
	Signetics	µA758	
	Sprague	ULN-2244	
µA760	National	LM160	
µA763	National	LM1496	
µA772	PMI	OP-25	
µA775	Motorola	LM139	
	NEC America	µPC339	
	Raytheon	LM339	
µA776	Harris	HA-2720	990
	Motorola	MC1776	
µA777	Intersil	777	
	Silicon G	SG777	
µA777	TI	µA777	
µA78G	Signetics	µA78G	
µA78L02	Motorola	MC78L02	
µA78L05	Motorola	MC78L05	
	National	**LM78L05**	**1060**
	NEC America	µPC78L05	
	Signetics	µA78L05	
	Silicon G	SG7805	
	TI	µA78L05	
µA78L06	Motorola	MC78L06	
	National	LM78L06	
	Silicon G	SG7806	
	TI	µA78L06	
µA78L08	Motorola	MC78L08	
	NEC America	µPC78L08	
	Silicon G	SG7808	
	TI	µA78L08	
µA78L09	TI	µA78L09	
µA78L10	TI	µA78L10	
µA78L12	Motorola	MC78L12	
	National	LM78L12	
	NEC America	µPC78L12	
	Signetics	µA78L12	
	Silicon G	SG7812	
	TI	µA78L12	
µA78L15	Motorola	MC78L15	
	National	LM78L15	
	NEC America	µPC78L15	
	Signetics	µA78L15	
	Silicon G	SG7815	
	TI	µA78L15	
µA78L18	Silicon G	SG7818	
µA78L20	TI	µA78L20	
µA78L24	Signetics	µA78L24	
	Silicon G	SG7824	
µA78L26	Motorola	MC78L02	
		MC7802	
	Signetics	µA78L26	
	TI	µA78L02	
µA78L62	Signetics	µA78L06	
	TI	µA78L06	
µA78MG	Signetics	µA78MG	
µA78M05	Motorola	MC78M05	
	National	**LM78M05**	**1060**
	NEC America	µPC78M05	
	Signetics	µA78M05	
	Silicon G	SG7805	
	TI	µA78M05	
µA78M06	Motorola	MC78M06	
	National	**LM78M06**	**1060**
	Signetics	µA78M06	
	Silicon G	SG7806	
	TI	µA78M06	
µA78M08	Motorola	MC78M08	
	National	**LM78M08**	**1060**
	NEC America	µPC78M08	
	Signetics	µA78M08	
	Silicon G	SG7808	
	TI	µA78M08	
µA78M12	Motorola	MC78M12	
	National	**LM78M12**	**1060**
	NEC America	µPC78M12	
	Signetics	µA78M12	
	Silicon G	SG7812	
	TI	µA78M12	
µA78M15	Motorola	MC78M15	
	National	**LM78M15**	**1060**
	NEC America	µPC78M15	
	Signetics	µA78M15	
	Silicon G	SG7815	
	TI	µA78M15	
µA78M18	Motorola	MC78M18	
	National	LM78M18	
		LM78M18	**1060**
	Silicon G	SG7818	
µA78M20	Motorola	MC78M20	
	Plessey	SL78M20	
	TI	µA78M20	
µA78M24	Motorola	MC78M24	
	National	**LM78M24**	**1060**
	Signetics	µA78M24	
	Silicon G	SG7824	
	TI	µA78M24	
µA780	RCA	CA3070	
	Sprague	ULN-2124	
µA7805	**National**	**LM340-5**	**1060**
µA7805	**National**	**LM7805**	**1060**
	NEC America	µPC14305	
	Plessey	SL7805	
	Signetics	µA7805	
	Silicon G	SG7805	
	TI	µA7805	
	Toshiba	TA78005	
µA7806	Motorola	MC7806	
	National	**LM340-6**	**1060**
		LM7806	**1060**
	Signetics	µA7806	
	Silicon G	SG7806	
	TI	µA7806	
µA7808	Motorola	MC7808	
	National	**LM340-8**	**1060**
		LM7808	**1060**
	NEC America	µPC14308	
	Signetics	µA7808	
	Silicon G	SG7808	
	TI	µA7808	
µA781	RCA	CA3071	
	Sprague	ULN-2127	
µA7810	TI	µA7810	
µA7812	Motorola	MC7812	
	National	**LM340-12**	**1060**
		LM7812	**1060**
	NEC America	µPC14312	
	Signetics	µA7812	
	Silicon G	SG7812	
	TI	µA7812	
	Toshiba	TA78012	
µA7815	Motorola	MC7815	
	National	**LM340-15**	**1060**
		LM7815	**1060**
	NEC America	µPC14315	
	Signetics	µA7815	
	Silicon G	SG7815	
	TI	µA7815	
	Toshiba	TA78015	
µA7818	Motorola	MC7818	
	National	**LM340-18**	**1060**
		LM7818	**1060**
	NEC America	µPC14318	
	Signetics	µA7818	
	Silicon G	SG7818	
	TI	µA7818	
µA7822	TI	µA7822	
µA7824	Motorola	MC7824	
	National	**LM340-24**	**1060**
		LM7824	**1060**
	NEC America	µPC14324	
	Signetics	µA7824	
	Silicon G	SG7824	
	TI	µA7824	
♦µA786	SGS	TAA630	
µA787	RCA	CA3126	
µA7885	TI	µA7885	
µA79G	Signetics	µA79G	
µA79MG	Signetics	µA79MG	
µA79M05	**National**	**LM79M05**	**1061**
	Signetics	µA79M05	
	Silicon G	SG7905	
	TI	µA79M05	
µA79M06	**National**	**LM79M06**	**1061**
	Signetics	µA79M06	
	TI	µA79M06	
µA79M08	**National**	**LM79M08**	**1061**
	Signetics	µA79M08	
	Silicon G	SG7908	
	TI	µA79M08	
µA79M12	**National**	**LM79M12**	**1061**
	Signetics	µA79M12	
	Silicon G	SG7912	
	TI	µA79M12	
µA79M15	**National**	**LM79M15**	**1061**
	Signetics	µA79M15	
	Silicon G	SG7915	
	TI	µA79M15	
µA79M18	**National**	**LM79M18**	**1061**
µA79M20	TI	µA79M20	
µA79M24	**National**	**LM79M24**	**1061**
	Signetics	µA79M24	
	TI	µA79M24	
µA7902	Motorola	MC7902	
µA7905	Motorola	MC7905	
	National	**LM7905**	**1061**

♦ Discontinued

Bold face device numbers indicate manufacturers data is provided in the IC Master on the pages noted.

Fairchild (cont'd)

Manufacturer Device	Replacement Source	Device	IC Master Page
µA7905	Signetics	µA7905	
	Silicon G	SG120-5	
	TI	µA7905	
µA7906	Motorola	MC7906	
	National	**LM7906**	**1061**
	Signetics	µA7906	
	TI	µA7906	
µA7908	Motorola	MC7908	
	National	**LM7908**	**1061**
	Signetics	µA7908	
	Silicon G	SG7908	
	TI	µA7908	
µA7912	Motorola	MC7912	
	National	**LM7912**	**1061**
	Signetics	µA7912	
	Silicon G	SG120-12	
	TI	µA7912	
µA7915	Motorola	MC7915	
	National	**LM7915**	**1061**
	Signetics	µA7915	
	Silicon G	SG120-15	
	TI	µA7915	
µA7918	Motorola	MC7918	
	National	**LM7918**	**1061**
	Signetics	µA7918	
	TI	µA7918	
µA7924	Motorola	MC7924	
	National	**LM7924**	**1061**
	Signetics	µA7924	
	TI	µA7924	
♦µA795	Motorola	MC1495	
		MC1595	
µA7952	TI	µA7952	
µA796	Motorola	MC1496	
		MC1596	
	Signetics	MC1496	
	Silicon G	SG1496	
		SG1596	
µA798	Motorola	MC3458	
		MC3558	
µA8T13	TI	SN55121	
		SN75121	
µA8T14	TI	SN55122	
		SN75122	
µA8T23	TI	SN75123	
µA8T24	TI	SN75124	
9H55	TI	SN74H55	
FQ3724	RCA	CA3724	
FQ3725	RCA	CA3725	
F10100	Motorola	MC10100	
	NEC America	µPB10100	
	Signetics	10100	
F10101	Hitachi	HD10101	
	Motorola	MC10101	
	NEC America	µPB10101	
	Signetics	10101	
F10102	Hitachi	HD10102	
	Motorola	MC10102	
	NEC America	µPB10102	
	Signetics	10102	
F10103	Motorola	MC10103	
	NEC America	µPB10103	
	Signetics	10103	
F10104	Hitachi	HD10104	
	Motorola	MC10104	
	Signetics	10104	
F10105	Hitachi	HD10105	
	Motorola	MC10105	
	National	DM10105	
	NEC America	µPB10105	
	Signetics	10105	
F10106	Hitachi	HD10106	
	Motorola	MC10106	
	National	DM10106	
	NEC America	µPB10106	
	Signetics	10106	
F10107	Hitachi	HD10107	
	Motorola	MC10107	
	NEC America	µPB10107	
	Signetics	10107	
F10109	Hitachi	HD10109	
	Motorola	MC10109	
	National	DM10109	
F10109	NEC America	µPB10109	
	Signetics	10109	
F10110	Hitachi	HD10110	
	Motorola	MC10110	
	NEC America	µPB10110	
	Signetics	10110	
F10111	Hitachi	HD10111	
	Motorola	MC10111	
	National	DM10111	
	NEC America	µPB10111	
	Signetics	10111	
F10113	Motorola	MC10113	
	Signetics	10113	
F10114	Motorola	MC10114	
	Signetics	10114	
F10115	Motorola	MC10115	
	National	DM10115	
	NEC America	µPB10115	
	Signetics	10115	
F10116	Hitachi	HD10116	
	Motorola	MC10116	
	National	DM10116	
	Signetics	10116	
F10117	Hitachi	HD10117	
	Motorola	MC10117	
	National	DM10117	
	NEC America	µPB10117	
	Signetics	10117	
F10118	Hitachi	HD10118	
	Motorola	MC10118	
	National	DM10118	
	NEC America	µPB10118	
	Signetics	10118	
F10119	Hitachi	HD10119	
	Motorola	MC10119	
	National	DM10119	
	Signetics	10119	
F10121	Hitachi	HD10121	
	Motorola	MC10121	
	National	DM10121	
	Signetics	10121	
F10123	Motorola	MC10123	
	Signetics	10123	
F10124	Hitachi	HD10124	
	Motorola	MC10124	
	National	DM10124	
	NEC America	µPB10124	
	Signetics	10124	
F10125	Hitachi	HD10125	
	Motorola	MC10125	
	Signetics	10125	
F10130	Hitachi	HD10130	
	Motorola	MC10130	
	Signetics	1010130	
F10131	Hitachi	HD10131	
	Motorola	MC10131	
	NEC America	µPB10131	
	Signetics	10131	
F10132	Hitachi	HD10132	
	Motorola	MC10132	
	Signetics	10132	
F10133	Hitachi	HD10133	
	Motorola	MC10133	
	NEC America	µPB10133	
	Signetics	10133	
F10134	Hitachi	HD10134	
	Motorola	MC10134	
	Signetics	10134	
F10135	Motorola	MC10135	
	Signetics	10135	
F10136	Hitachi	HD10136	
	Motorola	MC10136	
	Signetics	10136	
F10137	Motorola	MC10137	
	Signetics	10137	
F10141	Motorola	MC10141	
	Signetics	10141	
F10144	Signetics	10144	
F10145	Hitachi	HD10145	
	Motorola	MC10145	
	Signetics	10145	
F10153	Motorola	MC10153	
F10158	Motorola	MC10158	
	NEC America	µPB10158	
	Signetics	10158	
F10159	Motorola	MC10159	
F10159	Signetics	10159	
F10160	Hitachi	HD10160	
	Motorola	MC10160	
	Signetics	10160	
F10161	Hitachi	HD10161	
	Motorola	MC10161	
	NEC America	µPB10161	
	Signetics	10161	
F10162	Hitachi	HD10162	
	Motorola	MC10162	
	NEC America	µPB10162	
	Signetics	10162	
F10164	Hitachi	HD10164	
	Motorola	MC10164	
	NEC America	µPB10164	
	Signetics	10164	
	TI	SN10164	
F10165	Hitachi	HD10165	
	Motorola	MC10165	
	Signetics	10165	
F10166	Motorola	MC10166	
F10168	Motorola	MC10168	
F10170	Motorola	MC10170	
	Signetics	10170	
F10171	Motorola	MC10171	
	Signetics	10171	
F10172	Motorola	MC10172	
	Signetics	10172	
F10173	Motorola	MC10173	
	Signetics	10173	
F10174	Hitachi	HD10174	
	Motorola	MC10174	
	NEC America	µPB10174	
	Signetics	10174	
	TI	SN10174	
F10175	Hitachi	HD10175	
	Motorola	MC10175	
	Signetics	10175	
F10176	Motorola	MC10176	
	Signetics	10176	
F10177	Motorola	MC10177	
F10179	Hitachi	HD10179	
	Motorola	MC10179	
	Signetics	10179	
F10180	Hitachi	HD10180	
	Motorola	MC10180	
	NEC America	µPB10180	
	Signetics	10180	
F10181	Hitachi	HD10181	
	Motorola	MC10181	
	NEC America	µPB10181	
	Signetics	10181	
F10186	Motorola	MC10186	
F10192	Signetics	10192	
F10212	Motorola	MC10212	
F10405	Fujitsu	MB7047	
	TI	SN10147	
F10410	Fujitsu	MBM10410	
	Hitachi	HM2105	
		HM2106	
	TI	SN10144	
F10414	Fujitsu	MB7042	
F10415	Fujitsu	MBM10415	
	Hitachi	HM2110	
	Signetics	10146	
F10470	Fujitsu	MB7078	
F16K	AMD	9016	
	Fujitsu	MB8116	
	Intel	2116	
	Intersil	7116	
	Mostek	MK4116	
	Motorola	**MCM4116**	**1505**
	NEC Micro	**µPD416**	**1562**
	Signetics	**2690**	**1676**
	TI	TMS4116	
	Zilog	Z6116	
F4001	Mitel	SIL4001	
	Motorola	MC14001	
	National	CD4001	
	NEC America	µPD4001	
	RCA	CD4001	
	SGS	HBF4001	
	Solitron	CM4001	
	SSS	SCL4001	
	TI	TP4001	
	Toshiba	TC4001	
F4002	Mitel	SIL4002	
	Motorola	MC14002	
	National	CD4002	
	NEC America	µPD4002	
	RCA	CD4002	
	SGS	HBF4002	
	Solitron	CM4002	
	SSS	SCL4002	
	TI	TP4002	
	Toshiba	TC4002	
F4006	Motorola	MC14006	
	National	CD4006	
	NEC America	µPD4006	
	RCA	CD4006	
	Solitron	CM4006	
	SSS	SCL4006	
F4007	Mitel	SIL4007	
	Motorola	MC14007	
	National	CD4007	
	RCA	CD4007	
	SGS	HBF4007	
	Solitron	CM4007	
	SSS	SCL4007	
	TI	TP4007	
	Toshiba	TC4007	
F4008	Motorola	MC14008	
	National	CD4008	
	RCA	CD4008	
	SGS	HBF4008	
	Solitron	CM4008	
	SSS	SCL4008	
	TI	TP4008	
	Toshiba	TC4008	
F40083	RCA	CD4008	
F40085	Harris	HD74C85	
	National	MM74C85	
	RCA	CD4063	
F40089	National	MM74C89	
F40097	Harris	HD80C97	
	National	MM80C97	
F40098	National	MM80C98	
F4011	Mitel	SIL4011	
	Motorola	MC14011	
	National	CD4011	
	NEC America	µPD4011	
	RCA	CD4011	
	SGS	HBF4011	
	Solitron	CM4011	
	SSS	SCL4011	
	TI	TP4011	
	Toshiba	TC4011	
F4012	Mitel	SIL4012	
	Motorola	MC14012	
	National	CD4012	
	NEC America	µPD4012	
	RCA	CD4012	
	SGS	HBF4012	
	Solitron	CM4012	
	SSS	SCL4012	
	TI	TP4012	
	Toshiba	TC4012	
F4013	Mitel	SIL4013	
	Motorola	MC14013	
	National	CD4013	
	NEC America	µPD4013	
	RCA	CD4013	
	SGS	HBF4013	
	Solitron	CM4013	
	SSS	SCL4013	
	TI	TP4013	
	Toshiba	TC4013	
F4014	Mitel	SIL4014	
	Motorola	MC14014	
	National	CD4014	
	NEC America	µPD4014	
	RCA	CD4014	
	SGS	HBF4014	
	Solitron	CM4014	
	SSS	SCL4014	
	TI	TP4014	
	Toshiba	TC4014	
F4015	Mitel	SIL4015	
	Motorola	MC14015	
	National	CD4015	
	NEC America	µPD4015	
	RCA	CD4015	

♦ Discontinued

The manufacturers report their devices can be used as direct replacements.
Performance details often differ, so compare the specifications considering your requirements.

Fairchild (cont'd)

Manufacturer Device	Replacement Source	Device	IC Master Page
F4015	SGS	HBF4015	
	Solitron	CM4015	
	SSS	SCL4015	
	TI	TP4015	
	Toshiba	TC4015	
F4016	AD	AD7516	
	Micro Power	MP7516	
	Mitel	SIL4016	
	Motorola	MC14016	
	National	**CD4016**	**1076**
	RCA	CD4016	
	Solitron	CM4016	
	SSS	SCL4016	
	TI	TP4016	
F40160	Harris	HD54C160	
		HD74C160	
	National	CD40160	
		MM54C160	
		MM74C160	
	RCA	CD40160	
	SSS	SCL4160	
	TI	TP4360	
F40161	Harris	HD54C161	
		HD74C161	
	National	CD40161	
		MM54C161	
		MM74C161	
	RCA	CD40161	
	SSS	SCL4161	
	TI	TP4361	
F40162	Harris	HD54C162	
		HD74C162	
	National	CD40162	
		MM54C162	
		MM74C162	
	RCA	CD40162	
	SSS	SCL4162	
	TI	TP4362	
F40163	Harris	HD54C163	
		HD74C163	
	National	CD40163	
		MM54C163	
		MM74C163	
	RCA	CD40163	
	SSS	SCL4163	
	TI	TP4363	
F4017	Mitel	SIL4017	
	Motorola	MC14017	
	National	CD4017	
	NEC America	μPD4017	
	RCA	CD4017	
	SGS	HBF4017	
	Solitron	CM4017	
	SSS	SCL4017	
	TI	TP4017	
	Toshiba	TC4017	
F40174	Harris	HD54C174	
		HD74C174	
	National	CD40174	
		MM54C174	
		MM74C174	
	RCA	CD40174	
F40175	Harris	HD54C175	
		HD74C175	
	National	MM54C175	
		MM74C175	
F4018	Mitel	SIL4018	
	National	CD4018	
	RCA	CD4018	
	SGS	HBF4018	
	Solitron	CM4018	
	SSS	SCL4018	
	TI	TP4018	
	Toshiba	TC4018	
F4019	Mitel	SIL4019	
	National	CD4019	
	NEC America	μPD4019	
	RCA	CD4019	
	SGS	HBF4019	
	Solitron	CM4019	
	SSS	SCL4019	
	TI	TP4019	
	Toshiba	TC4019	
F40192	Harris	HD54C192	
		HD74C192	
	National	CD40192	
		MM54C192	
		MM74C192	
	RCA	CD40192	
F40193	Harris	HD54C193	
		HD74C193	
	National	CD40193	
		MM54C193	
		MM74C193	
	RCA	CD40193	
F40194	NEC America	μPD4194	
	RCA	CD40194	
F40195	National	MM74C195	
F4020	Mitel	SIL4020	
	Motorola	MC14020	
	National	CD4020	
	NEC America	μPD4020	
	RCA	CD4020	
	SGS	HBF4020	
	Solitron	CM4020	
	SSS	SCL4020	
	TI	TP4020	
	Toshiba	TC4020	
F4021	Mitel	SIL4021	
	Motorola	MC14021	
	National	CD4021	
	NEC America	μPD4021	
	RCA	CD4021	
	Solitron	CM4021	
	SSS	SCL4021	
	TI	TP4021	
	Toshiba	TC4021	
F4022	Mitel	SIL4022	
	Motorola	MC14022	
	National	CD4022	
	RCA	CD4022	
	SGS	HBF4022	
	Solitron	CM4022	
	SSS	SCL4022	
	TI	TP4022	
	Toshiba	TC4022	
F4023	Mitel	SIL4023	
	Motorola	MC14023	
	National	CD4023	
	NEC America	μPD4023	
	RCA	CD4023	
	SGS	HBF4023	
	Solitron	CM4023	
	SSS	SCL4023	
	TI	TP4023	
	Toshiba	TC4023	
F4024	Mitel	SIL4024	
	Motorola	MC14024	
	National	CD4024	
	NEC America	μPD4024	
	RCA	CD4024	
	SGS	HBF4024	
	Solitron	CM4024	
	SSS	SCL4024	
	TI	TP4024	
	Toshiba	TC4024	
F4025	Mitel	SIL4025	
	Motorola	MC14025	
	National	CD4025	
	NEC America	μPD4025	
	RCA	CD4025	
	SGS	HBF4025	
	Solitron	CM4025	
	SSS	SCL4025	
	TI	TP4025	
	Toshiba	TC4025	
F4027	Mitel	SIL4027	
	Motorola	MC14027	
	National	CD4027	
	NEC America	μPD4027	
	RCA	CD4027	
	SGS	HBF4027	
	Solitron	CM4027	
	SSS	SCL4027	
	TI	TP4027	
	Toshiba	TC4027	
F4028	Mitel	SIL4028	
	Motorola	MC14028	
	National	CD4028	
F4028	NEC America	μPD4028	
	RCA	CD4028	
	SGS	HBF4028	
	Solitron	CM4028	
	SSS	SCL4028	
	TI	TP4028	
	Toshiba	TC4028	
F4029	Mitel	SIL4029	
	National	CD4029	
	NEC America	μPD4029	
	RCA	CD4029	
	SGS	HBF4029	
	Solitron	CM4029	
	SSS	SCL4029	
	TI	TP4029	
	Toshiba	TC4029	
F4030	Mitel	SIL4030	
	National	CD4030	
	NEC America	μPD4030	
	RCA	CD4030	
		CD4070	
	SGS	HBF4030	
	Solitron	CM4030	
	SSS	SCL4030	
	TI	TP4030	
	Toshiba	TC4030	
F4031	National	CD4031	
	RCA	CD4031	
F4034	Motorola	MC14034	
	National	CD4034	
	RCA	CD4034	
	Solitron	CM4034	
	SSS	SCL4034	
	Toshiba	TC4034	
F4035	Mitel	SIL4035	
	Motorola	MC14035	
	National	CD4035	
	NEC America	μPD4035	
	RCA	CD4035	
	SGS	HBF4035	
	Solitron	CM4035	
	SSS	SCL4035	
	TI	TP4035	
	Toshiba	TC4035	
F4040	Mitel	SIL4040	
	National	CD4040	
	NEC America	μPD4040	
	RCA	CD4040	
	Solitron	CM4040	
	SSS	SCL4040	
	TI	TP4040	
	Toshiba	TC4040	
F4041	National	CD4041	
	RCA	CD4041	
	Solitron	CM4041	
	SSS	CL4041	
		SCL4041	
F4042	Mitel	SIL4042	
	Motorola	MC14042	
	National	CD4042	
	NEC America	μPD4042	
	RCA	CD4042	
	SGS	HBF4042	
	Solitron	CM4042	
	SSS	SCL4042	
	TI	TP4042	
	Toshiba	TC4042	
F4043	Mitel	SIL4043	
	Motorola	MC14043	
	National	CD4043	
	NEC America	μPD4043	
	RCA	CD4043	
	Solitron	CM4043	
	SSS	SCL4043	
	TI	TP4043	
	Toshiba	TC4043	
F4044	Mitel	SIL4044	
	Motorola	MC14044	
	National	CD4044	
	NEC America	μPD4044	
	RCA	CD4044	
	Solitron	CM4044	
	SSS	SCL4044	
	TI	TP4044	
	Toshiba	TC4044	
F4046	Mitel	SIL4046	
F4046	Motorola	MC14046	
	National	CD4046	
	RCA	CD4046	
	Solitron	CM4046	
	SSS	SCL4046	
F4047	RCA	CD4047	
	Solitron	CM4047	
	TI	TP4047	
	Toshiba	TC4047	
F4049	Mitel	SIL4049	
	Motorola	MC14049	
	National	CD4049	
	NEC America	μPD4049	
	RCA	CD4049	
	SGS	HBF4049	
	Solitron	CM4049	
	SSS	SCL4049	
	TI	TP4049	
	Toshiba	TC4049	
F4050	Mitel	SIL4050	
	Motorola	MC14050	
	National	CD4050	
	NEC America	μPD4050	
	RCA	CD4050	
	SGS	HBF4050	
	Solitron	CM4050	
	SSS	SCL4050	
	TI	TP4050	
	Toshiba	TC4050	
F4051	Mitel	SIL4051	
	Motorola	MC14051	
	National	CD4051	
	NEC America	μPD4051	
	RCA	CD4051	
	Solitron	CM4051	
	SSS	SCL4051	
	TI	TP4051	
	Toshiba	TC4051	
F4052	Mitel	SIL4052	
	Motorola	MC14052	
	National	CD4052	
	NEC America	μPD4052	
	RCA	CD4052	
	Solitron	CM4052	
	SSS	SCL4052	
	TI	TP4052	
	Toshiba	TC4052	
F4053	Mitel	SIL4053	
	Motorola	MC14053	
	National	CD4053	
	NEC America	μPD4053	
	RCA	CD4053	
	Solitron	CM4053	
	SSS	SCL4053	
	Toshiba	TC4053	
F4066	Mitel	SIL4066	
	Motorola	MC14066	
	National	**CD4066**	**1076**
	NEC America	μPD4066	
	RCA	CD4066	
	SGS	HBF4066	
	Signetics	N4066	
	Solitron	CM4066	
	SSS	SCL4066	
	Toshiba	TC4066	
F4067	RCA	CD4067	
F4068	Mitel	SIL4068	
	Motorola	MC14068	
	NEC America	μPD4068	
	RCA	CD4068	
	Solitron	CM4068	
	SSS	SCL4068	
	TI	TP4068	
	Toshiba	TC4068	
F4069	Harris	HD74C04	
	Mitel	SIL4069	
	Motorola	MC14069	
	National	CD4069	
		MM74C04	
	NEC America	μPD4069	
	RCA	CD4069	
	Solitron	CM4069	
	SSS	SCL4069	
	TI	TP4069	
	Toshiba	TC4069	
F4070	Mitel	SIL4070	

♦ Discontinued

Bold face device numbers indicate manufacturers data is provided in the IC Master on the pages noted.

Fairchild (cont'd)

Manufacturer Device	Replacement Source	Device	IC Master Page
F4070	National	CD4070	
		MM74C86	
	RCA	CD4070	
	Solitron	CM4070	
	SSS	SCL4070	
F4071	Mitel	SIL4071	
	Motorola	MC14071	
	National	CD4071	
	NEC America	µPD4071	
	RCA	CD4071	
	Solitron	CM4071	
	SSS	SCL4071	
	TI	TP4071	
	Toshiba	TC4071	
F4072	Mitel	SIL4072	
	Motorola	MC14072	
	RCA	CD4072	
	SSS	SCL4072	
	TI	TP4072	
	Toshiba	TC4072	
F4073	Mitel	SIL4073	
	Motorola	MC14073	
	National	CD4073	
	NEC America	µPD4073	
	RCA	CD4073	
	Solitron	CM4073	
	SSS	SCL4073	
	TI	TP4073	
	Toshiba	TC4073	
F4075	Mitel	SIL4075	
	Motorola	MC14075	
	National	CD4075	
	NEC America	µPD4075	
	RCA	CD4075	
	SSS	SCL4075	
	TI	TP4075	
	Toshiba	TC4075	
F4076	Harris	HD74C173	
	Mitel	SIL4076	
	Motorola	MC14076	
	National	CD4076	
		MM74C173	
	RCA	CD4076	
	Solitron	CM4076	
	SSS	SCL4076	
F4077	Mitel	SIL4077	
	Motorola	MC14077	
	RCA	CD4077	
	Solitron	CM4077	
	SSS	SCL4077	
F4078	Mitel	SIL4078	
	Motorola	MC14078	
	NEC America	µPD4078	
	RCA	CD4078	
	Solitron	CM4078	
	SSS	SCL4078	
	Toshiba	TC4078	
F4081	Mitel	SIL4081	
	Motorola	MC14081	
	National	CD4081	
	NEC America	µPD4081	
	RCA	CD4081	
	Solitron	CM4081	
	SSS	SCL4081	
	TI	TP4081	
	Toshiba	TC4081	
F4082	Mitel	SIL4082	
	Motorola	MC14082	
	NEC America	µPD4082	
	RCA	CD4082	
	SSS	SCL4082	
	TI	TP4082	
	Toshiba	TC4082	
F4085	RCA	CD4085	
F4086	RCA	CD4086	
F4093	Motorola	MC14093	
	National	CD4093	
	NEC America	µPD4093	
	RCA	CD4093	
F4097	RCA	CD4097	
F4099	National	CD4099	
	NEC America	µPD4099	
	RCA	CD4099	
F4104	RCA	CD40104	
F4510	Mitel	SIL4510	
	Motorola	MC14510	
	National	CD4510	
	NEC America	µPD4510	
	RCA	CD40192	
		CD4510	
	SSS	SCL4510	
	Toshiba	TC4510	
F4511	Mitel	SIL4511	
	Motorola	MC14511	
	National	CD4511	
	NEC America	µPD4511	
	RCA	CD4511	
	Solitron	CM4511	
	SSS	SCL4511	
	TI	TP4511	
F4512	Mitel	SIL4512	
	Motorola	MC14512	
	National	CD4512	
	NEC America	µPD4512	
	SSS	SCL4512	
	TI	TP4512	
	Toshiba	TC4512	
F4514	Mitel	SIL4514	
	Motorola	MC14514	
	National	CD4514	
	NEC America	µPD4514	
	RCA	CD4514	
	Solitron	CM4514	
	SSS	SCL4514	
	Toshiba	TC4514	
F4515	Mitel	SIL4515	
	Motorola	MC14515	
	National	CD4515	
	NEC America	µPD4515	
	RCA	CD4515	
	SSS	SCL4515	
	Toshiba	TC4515	
F4516	Mitel	SIL4516	
	Motorola	MC14516	
	National	CD4516	
	NEC America	µPD4516	
	RCA	CD40193	
		CD4516	
	SSS	SCL4516	
	Toshiba	TC4516	
F4518	Mitel	SIL4518	
	Motorola	MC14518	
	National	CD4518	
	NEC America	µPD4518	
	RCA	CD4518	
	Solitron	CM4518	
	SSS	SCL4518	
	TI	TP4518	
	Toshiba	TC4518	
F4519	Motorola	MC14519	
	National	CD4519	
	NEC America	µPD4519	
	RCA	CD4019	
	TI	TP4519	
F4520	Mitel	SIL4520	
	Motorola	MC14520	
	National	CD4520	
	NEC America	µPD4520	
	RCA	CD4520	
	Solitron	CM4520	
	SSS	SCL4520	
	TI	TP4520	
	Toshiba	TC4520	
F4522	Motorola	MC14522	
	National	CD4522	
	RCA	CD4018	
	SSS	SCL4522	
	TI	TP4522	
F4526	Motorola	MC14526	
	SSS	SCL4526	
	TI	TP4526	
F4527	RCA	CD4527	
	SSS	SCL4527	
F4528	Motorola	MC14528	
	National	CD4528	
	NEC America	µPD4528	
	RCA	CD4098	
		CD4528	
	SSS	SCL4528	
F4528	Toshiba	TC4528	
F4531	Motorola	MC14531	
	RCA	CD40101	
	SSS	SCL4531	
	TI	TP4531	
F4532	Motorola	MC14532	
	RCA	CD4532	
	Toshiba	TC4532	
F4539	Motorola	MC14539	
	NEC America	µPD4539	
	Toshiba	TC4539	
F4553	Motorola	MC14553	
F4555	Motorola	MC14555	
	NEC America	µPD4555	
	RCA	CD4555	
	SSS	SCL4555	
F4556	Motorola	MC14556	
	NEC America	µPD4556	
	RCA	CD4556	
	SSS	SCL4556	
F4557	Motorola	MC14557	
	RCA	CD4031	
F4581	RCA	CD40181	
	SSS	SCL4581	
F4582	Motorola	MC14582	
	RCA	CD40182	
	SSS	SCL4582	
	TI	TP4582	
F4583	Motorola	MC14583	
	RCA	CD40100	
	Toshiba	TC4583	
F4585	RCA	CD4063	
	SSS	SCL4585	
F4702	Harris	HD4702	
F4703	RCA	CD40105	
F4710	RCA	CD4036	
		CD4039	
F4720	RCA	CD40061	
		CD4061	
F4731	RCA	CD4031	
F6800	**AMI**	**S6800**	**1776,1780**
	Motorola	**MC6800**	**2002**
F6802	**AMI**	**S6802**	**1785**
F6810	**AMI**	**S6810**	**1790**
F6820	**AMI**	**S6820**	**1802**
	Motorola	MC6820	
F6821	**AMI**	**S6821**	**1798,1802**
F6840	**AMI**	**S6840**	**1813**
F6846	**AMI**	**S6846**	**1817**
F6850	**AMI**	**S6850**	**1818**
F6852	**AMI**	**S6852**	**1822**
LM301	Toshiba	TA7506	
MC1412	Silicon G	SG2002	
MC1413	Silicon G	SG2003	
MC5524	Silicon G	SG5524	
MC5525	Silicon G	SG5525	
MC5528	Silicon G	SG5528	
MC5529	Silicon G	SG5529	
MC55325	Silicon G	SG55325	
MC5534	Silicon G	SG5534	
MC7905.2	Silicon G	SG7905.2	
MC7908	Silicon G	SG7908	
M4027	Fujitsu	MB8227	
	Intersil	MK4027	
	Mostek	MK4027	
	Motorola	**MCM4027**	**1522**
	Signetics	**4027**	**1677**
	TI	TMS4027	
SH3002	Siliconix	SI3002	
SN54LS126	Raytheon	54LS126	
	Signetics	54LS126	
	TI	SN54LS126	
TBA810	RCA	CA810	
♦102	Motorola	MC54H102	
11C05	Plessey	SP8610	
11C90	Plessey	SP8660	
1103	AMI	S1103A	
1800	TI	SN151800	
		SN151900	
1802	TI	SN151802	
		SN151902	
1805	TI	SN151805	
		SN151905	
1806	TI	SN151806	
		SN151906	
1807	TI	SN151807	
1807	TI	SN151907	
1808	TI	SN151808	
		SN151908	
1810	TI	SN151810	
		SN151910	
1812	TI	SN151812	
		SN151912	
2102	**NEC Micro**	**µPD2102**	**1591**
	Signetics	2102	
	TI	TMS4035	
2114	**AMI**	**S2114**	**1196**
	Fujitsu	MB8114	
	Rockwell	R2114	
2136	Motorola	MC1356	
	Sprague	ULN-2136	
2708	Fujitsu	MB8518	
2716	Intel	2716	
3257	GI	RO5-2240S	
	Mostek	MK2302	
3260	AMI	S8564	
3341	AMD	3341	
3342	TI	TMS3121	
		TMS3417	
3347	TI	TMS3120	
3348	TI	TMS3112	
3355	Synertek	SY2833	
3357	TI	TMS3404	
34XXX	Fairchild	F4XXX	
3501	National	MM3501	
3507	AMI	S8773	
3512	AMI	S8773	
3513	AMI	S8773	
3514	AMI	S3514	
		S8772	
	Fairchild	3515	
	Mostek	MK2600	
		MK2601	
	National	MM4233	
		MM5233	
3538	**NEC Micro**	**µPD2101**	**1586**
3539	**EMM/Semi**	**3539**	**1226**
3580	AMI	S8773	
3705	Siliconix	SI3705	
3730	GI	AY5-1013A	
3731	AMI	S1757	
3817	AMI	S1998	
3850	Mostek	MK3850	
3851	Mostek	MK3851	
3852	Mostek	MK3852	
3854	Mostek	MK3854	
3861	Mostek	MK3861	
3870	Mostek	MK3870	
4096	EA	EA4096	
	EMM/Semi	RO3-4096	
	Fujitsu	MB8227	
	Intersil	7005	
	Mostek	MK4096	
	NEC Micro	µPD414	
	Rockwell	1604	
	TI	TMS4027	
4721B	**AMI**	**S5101**	**1206**
4736B	**AMI**	**S6508**	**1207**
54H00	Motorola	MC54H00	
	National	DM54H00	
	Raytheon	54H00	
	Signetics	54H00	
	TI	SN54H00	
54H01	Motorola	MC54H01	
	National	DM54H01	
	Raytheon	54H01	
	Signetics	54H01	
	TI	SN54H01	
54H04	Motorola	MC54H04	
	National	DM54H04	
	Raytheon	54H04	
	Signetics	54H04	
	TI	SN54H04	
54H05	Motorola	MC54H05	
	National	DM54H05	
	Raytheon	54H05	
	Signetics	54H05	
	TI	SN54H05	
54H08	Motorola	MC54H08	
	National	DM54H08	
	Signetics	54H08	
54H10	Motorola	MC54H10	

♦ Discontinued

The manufacturers report their devices can be used as direct replacements.
Performance details often differ, so compare the specifications considering your requirements.

Fairchild (cont'd)

Manufacturer Device	Replacement Source	Device	IC Master Page
54H10	National	DM54H10	
	Raytheon	54H10	
	Signetics	54H10	
	TI	SN54H10	
54H101	Motorola	MC54H101	
	Signetics	54H101	
	TI	SN54H101	
54H102	Motorola	MC54H102	
	Signetics	54H102	
	TI	SN54H102	
54H103	National	DM54H103	
	Signetics	54H103	
	TI	SN54H103	
54H106	National	DM54H106	
	Signetics	54H106	
	TI	SN54H106	
54H108	Motorola	MC54H108	
	National	DM54H108	
	Signetics	54H108	
	TI	SN54H108	
54H11	Motorola	MC54H11	
	National	DM54H11	
	Raytheon	54H11	
	Signetics	54H11	
	TI	SN54H11	
54H15	Raytheon	54H15	
	TI	SN54H15	
54H183	TI	SN54H183	
54H20	Motorola	MC54H20	
	National	DM54H20	
	Raytheon	54H20	
	Signetics	54H20	
	TI	SN54H20	
54H21	Motorola	MC54H21	
	National	DM54H21	
	Signetics	54H21	
	TI	SN54H21	
54H22	Motorola	MC54H22	
	National	DM54H22	
	Raytheon	54H22	
	Signetics	54H22	
	TI	SN54H22	
54H30	Motorola	MC54H30	
	National	DM54H30	
	Signetics	54H30	
	TI	SN54H30	
54H40	Motorola	MC54H40	
	National	DM54H40	
	Raytheon	54H40	
	Signetics	54H40	
	TI	SN54H40	
54H50	Motorola	MC54H50	
	National	DM54H50	
	Signetics	54H50	
	TI	SN54H50	
54H51	Motorola	MC54H51	
	National	DM54H51	
	Signetics	54H51	
	TI	SN54H51	
54H52	Motorola	MC54H52	
	National	DM54H52	
	Signetics	54H52	
	TI	SN54H52	
54H53	Motorola	MC54H53	
	National	DM54H53	
	Signetics	54H53	
	TI	SN54H53	
54H54	Motorola	MC54H54	
	National	DM54H54	
	Signetics	54H54	
	TI	SN54H54	
54H55	Motorola	MC54H55	
	National	DM54H55	
	Signetics	54H55	
	TI	SN54H55	
54H60	Motorola	MC54H60	
	National	DM54H60	
	Signetics	54H60	
	TI	SN54H60	
54H61	Motorola	MC54H61	
	National	DM54H61	
	Signetics	54H61	
	TI	SN54H61	
54H62	Motorola	MC54H62	
	National	DM54H62	
	Signetics	54H62	
	TI	SN54H62	
54H71	Motorola	MC54H71	
	National	DM54H71	
	Signetics	54H71	
	TI	SN54H71	
54H72	Fairchild	54H73	
	Motorola	MC54H72	
	National	DM54H72	
	Signetics	54H72	
	TI	SN54H72	
54H73	Fairchild	54H72	
	Motorola	MC54H73	
	National	DM54H72	
		DM54H73	
	Signetics	54H72	
		54H73	
	TI	SN54H72	
		SN54H73	
54H74	Motorola	MC54H74	
	National	DM54H74	
	Raytheon	54H74	
	Signetics	54H74	
	TI	SN54H74	
54H76	National	DM54H76	
	Signetics	54H76	
	TI	SN54H76	
54H78	National	DM54H78	
	TI	SN54H78	
54LS00	Motorola	SN54LS00	
	National	DM54LS00	
	Raytheon	54LS00	
	Signetics	54LS00	
	TI	SN54LS00	
54LS01	National	DM54LS01	
	Raytheon	54LS01	
	Signetics	54LS01	
	TI	SN54LS01	
54LS02	Motorola	SN54LS02	
	National	DM54LS02	
	Raytheon	54LS02	
	Signetics	54LS02	
	TI	SN54LS02	
54LS03	Motorola	SN54LS03	
	National	DM54LS03	
	Raytheon	54LS03	
	Signetics	54LS03	
	TI	SN54LS03	
54LS04	Motorola	SN54LS04	
	National	DM54LS04	
	Raytheon	54LS04	
	Signetics	54LS04	
	TI	SN54LS04	
54LS05	Motorola	SN54LS05	
	National	DM54LS05	
	Raytheon	54LS05	
	Signetics	54LS05	
	TI	SN54LS05	
54LS08	Motorola	SN54LS08	
	National	DM54LS08	
	Raytheon	54LS08	
	Signetics	54LS08	
	TI	SN54LS08	
54LS09	Motorola	SN54LS09	
	National	DM54LS09	
	Raytheon	54LS09	
	Signetics	54LS09	
	TI	SN54LS09	
54LS10	Motorola	SN54LS10	
	National	DM54LS10	
	Raytheon	54LS10	
	Signetics	54LS10	
	TI	SN54LS10	
54LS107	Motorola	SN54LS107A	
	National	DM54LS107	
	Raytheon	54LS107	
	Signetics	54LS107	
	TI	SN54LS107A	
54LS109	Motorola	SN54LS109A	
	National	DM54LS109	
	Raytheon	54LS109	
	Signetics	54LS109	
	TI	SN54LS109A	
54LS11	Motorola	SN54LS11	
	National	DM54LS11	
	Raytheon	54LS11	
	Signetics	54LS11	
	TI	SN54LS11	
54LS112	Motorola	SN54LS112A	
	National	DM54LS112	
	Raytheon	54LS112	
	Signetics	54LS112	
	TI	SN54LS112	
54LS113	Motorola	SN54LS113A	
	National	DM54LS113	
	Raytheon	54LS113	
	Signetics	54LS113	
	TI	SN54LS113	
54LS114	Motorola	SN54LS114A	
	National	DM54LS114	
	Raytheon	54LS114	
	Signetics	54LS114	
	TI	SN54LS114A	
54LS12	Motorola	SN54LS12	
	National	DM54LS12	
	Raytheon	54LS12	
	Signetics	54LS12	
	TI	SN54LS12	
54LS125	National	DM54LS125	
	Raytheon	54LS125	
	Signetics	54LS125	
	TI	SN54LS125	
54LS126	Motorola	SN54LS126	
	National	DM54LS126	
54LS132	Motorola	SN54LS132	
	National	DM54LS132	
	Raytheon	54LS132	
	Signetics	54LS132	
	TI	SN54LS132	
54LS133	Motorola	SN54LS133	
54LS136	Motorola	SN54LS136	
	Raytheon	54LS136	
	Signetics	54LS136	
	TI	SN54LS136	
54LS138	Motorola	SN54LS138	
	National	DM54LS138	
	Raytheon	54LS138	
	Signetics	54LS138	
	TI	SN54LS138	
54LS139	AMD	SN54LS139	
	Motorola	SN54LS139	
	National	DM54LS139	
	Raytheon	54LS139	
	Signetics	74LS139	
	TI	SN54LS139	
54LS14	Motorola	SN54LS14	
	National	DM54LS14	
	Raytheon	54LS14	
	Signetics	54LS14	
	TI	SN54LS14	
54LS145	TI	SN54LS145	
54LS15	Motorola	SN54LS15	
	National	DM54LS15	
	Raytheon	54LS15	
	Signetics	54LS15	
	TI	SN54LS15	
54LS151	AMD	SN54LS151	
	Motorola	SN54LS151	
	National	DM54LS151	
	Raytheon	54LS151	
	Signetics	54LS151	
	TI	SN54LS151	
54LS152	Motorola	SN54LS152	
	Raytheon	54LS152	
	TI	SN54LS152	
54LS153	AMD	SN54LS153	
	Motorola	SN54LS153	
	National	DM54LS153	
	Raytheon	54LS153	
	Signetics	54LS153	
	TI	SN54LS153	
54LS155	Motorola	SN54LS155	
	National	DM54LS155	
	Raytheon	54LS155	
		74LS155	
	TI	SN54LS155	
54LS156	Motorola	SN54LS156	
	National	DM54LS156	
	Raytheon	54LS156	
	TI	SN54LS156	
54LS157	AMD	SN54LS157	
	Motorola	SN54LS157	
	National	DM54LS157	
	Raytheon	54LS157	
	Signetics	54LS157	
	TI	SN54LS157	
54LS158	Motorola	SN54LS158	
	National	DM54LS158	
	Raytheon	54LS158	
	Signetics	54LS158	
	TI	SN54LS158	
54LS160	AMD	SN54LS160	
	Motorola	SN54LS160A	
	National	DM54LS160	
	Raytheon	54LS160	
	TI	SN54LS160A	
54LS161	AMD	SN54LS161	
	Motorola	SN54LS161	
	National	DM54LS161	
	Raytheon	54LS161	
	Signetics	54LS161A	
	TI	SN54LS161A	
54LS162	AMD	SN54LS162	
	Motorola	SN54LS162A	
	National	DM54LS162	
	Raytheon	54LS162	
	TI	SN54LS162A	
54LS163	AMD	SN54LS163	
	Motorola	SN54LS163A	
	National	DM54LS163	
	Raytheon	54LS163	
	Signetics	54LS163A	
	TI	SN54LS163A	
54LS164	AMD	SN54LS164	
	Motorola	SN54LS164A	
	National	DM54LS164	
	Raytheon	54LS164	
	Signetics	54LS164	
	TI	SN54LS164A	
54LS165	TI	SN54LS165	
54LS168	AMD	SN54LS168	
	National	DM54LS168	
	TI	SN54LS168	
54LS169	AMD	SN54LS169	
	National	DM54LS169	
	TI	SN54LS169	
54LS170	AMD	AM54LS170	
	Motorola	SN54LS170	
	National	DM54LS170	
	Raytheon	54LS170	
	Signetics	54LS170	
	TI	SN54LS170	
54LS173	National	DM54LS173	
	Signetics	54LS173	
	TI	SN54LS173	
54LS174	AMD	SN54LS174	
	National	DM54LS174	
	Raytheon	54LS174	
	Signetics	54LS174	
	TI	SN54LS174	
54LS175	AMD	SN54LS175	
	Motorola	SN54LS175	
	National	DM54LS175	
	Raytheon	54LS175	
	Signetics	54LS175	
	TI	SN54LS175	
54LS181	AMD	SN54LS181	
	Motorola	SN54LS181	
	Raytheon	54LS181	
	Signetics	54LS181	
	TI	SN54LS181	
54LS190	AMD	SN54LS190	
	Motorola	SN54LS190	
	National	DM54LS190	
	Raytheon	54LS190	
	Signetics	54LS190	
	TI	SN54LS190	
54LS191	AMD	SN54LS191	
	Motorola	SN54LS191	
	National	DM54LS191	
	Raytheon	54LS191	
	Signetics	54LS191	
	TI	SN54LS191	
54LS192	AMD	SN54LS192	
	Motorola	SN54LS192	
	National	DM54LS192	

♦ Discontinued

Bold face device numbers indicate manufacturers data is provided in the IC Master on the pages noted.

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Manufacturer Device	Replacement Source	Device	IC Master Page
54LS192	Raytheon	54LS192	
	Signetics	54LS192	
	TI	SN54LS192	
54LS193	AMD	SN54LS193	
	Motorola	SN54LS193	
	National	DM54LS193	
	Raytheon	54LS193	
	Signetics	54LS193	
	TI	SN54LS193	
54LS194	AMD	SN54LS194A	
	Motorola	SN54LS194A	
	Raytheon	54LS194A	
	TI	SN54LS194A	
54LS195	AMD	SN54LS195A	
	Motorola	SN54LS195A	
	Raytheon	54LS195A	
	Signetics	54LS195A	
	TI	SN54LS195A	
54LS196	Motorola	SN54LS196	
	National	DM54LS196	
	Raytheon	54LS196	
	TI	SN54LS196	
54LS197	Motorola	SN54LS197	
	National	DM54LS197	
	Raytheon	54LS197	
	TI	SN54LS197	
54LS20	Motorola	SN54LS20	
	National	DM54LS20	
	Raytheon	54LS20	
	Signetics	54LS20	
	TI	SN54LS20	
54LS21	Motorola	SN54LS21	
	National	DM54LS21	
	Raytheon	54LS21	
	Signetics	54LS21	
	TI	SN54LS21	
54LS22	Motorola	SN54LS22	
	National	DM54LS22	
	Raytheon	54LS22	
	Signetics	54LS22	
	TI	SN54LS22	
54LS240	AMD	SN54LS240	
	MMI	**54LS240**	**768**
	TI	SN54LS240	
54LS241	AMD	SN54LS241	
	MMI	**54LS241**	**768**
	TI	SN54LS241	
54LS245	Motorola	SN54LS245	
54LS247	Motorola	SN54LS247	
54LS248	Motorola	SN54LS248	
54LS249	Motorola	SN54LS249	
54LS251	AMD	SN54LS251	
	Motorola	SN54LS251	
	Raytheon	54LS251	
	Signetics	54LS251	
	TI	SN54LS251	
54LS253	AMD	SN54LS253	
	Motorola	SN54LS253	
	National	DM54LS253	
	Raytheon	54LS253	
	Signetics	54LS253	
	TI	SN54LS253	
54LS255	Raytheon	54LS255	
54LS256	Motorola	SN54LS256	
54LS257	Motorola	SN54LS257A	
	National	DM54LS257	
	Raytheon	54LS257	
	Signetics	54LS257	
	TI	SN54LS257A	
54LS258	AMD	SN54LS258	
	Motorola	SN54LS258A	
	Raytheon	54LS258	
	TI	SN54LS258A	
54LS259	Motorola	SN54LS259	
	TI	SN54LS259	
54LS26	Motorola	SN54LS26	
	National	DM54LS26	
	Raytheon	54LS26	
	Signetics	54LS26	
	TI	SN54LS26	
54LS260	Motorola	SN54LS260	
54LS266	Motorola	SN54LS266	
	Raytheon	54LS266	
54LS266	Signetics	54LS266	
	TI	SN54LS266	
54LS27	Motorola	SN54LS27	
	National	DM54LS27	
	Raytheon	54LS27	
	Signetics	54LS27	
	TI	SN54LS27	
54LS279	Motorola	SN54LS279	
	National	DM54LS279	
	Raytheon	54LS279	
		74LS279	
	Signetics	54LS279	
	TI	SN54LS279	
54LS280	TI	SN54LS280	
54LS283	Motorola	SN54LS283	
	National	DM54LS283	
	Raytheon	54LS283	
	TI	SN54LS283	
54LS290	Motorola	SN54LS290	
	Signetics	54LS290	
	TI	SN54LS290	
54LS293	Motorola	SN54LS293	
	Signetics	54LS293	
	TI	SN54LS293	
54LS295	Raytheon	54LS295A	
	TI	SN54LS295B	
54LS298	Motorola	SN54LS298	
	Raytheon	54LS298	
	TI	SN54LS298	
54LS299	AMD	SN54LS299	
	Raytheon	**54LS299**	**533**
	TI	SN54LS299	
54LS30	Motorola	SN54LS30	
	National	DM54LS30	
	Raytheon	54LS30	
	Signetics	54LS30	
	TI	SN54LS30	
54LS32	Motorola	SN54LS32	
	National	DM54LS32	
	Raytheon	54LS32	
	Signetics	54LS32	
	TI	SN54LS32	
54LS322	Motorola	SN54LS322	
54LS323	Motorola	SN54LS323	
		SN74LS323	
54LS33	Raytheon	54LS33	
	Signetics	54LS33	
	TI	SN54LS33	
54LS352	Motorola	SN54LS352	
	National	DM54LS352	
	TI	SN54LS352	
54LS353	Motorola	SN54LS353	
	National	DM54LS353	
	TI	SN54LS353	
54LS365	Motorola	SN54LS365A	
	Raytheon	54LS365	
	Signetics	54LS365A	
	TI	SN54LS365A	
54LS366	Motorola	SN54LS366A	
	Raytheon	54LS366	
	Signetics	54LS366A	
	TI	SN54LS366A	
54LS367	Motorola	SN54LS367A	
	Raytheon	54LS367	
	Signetics	54LS367A	
	TI	SN54LS367A	
54LS368	Motorola	SN54LS368A	
	Raytheon	54LS368	
	Signetics	54LS368A	
	TI	SN54LS368A	
54LS37	Motorola	SN54LS37	
	National	DM54LS37	
	Raytheon	54LS37	
	Signetics	54LS37	
	TI	SN54LS37	
54LS373	Motorola	SN54LS373	
54LS375	Motorola	SN54LS375	
54LS379	Motorola	SN54LS379	
54LS38	Motorola	SN54LS38	
	National	DM54LS38	
	Raytheon	54LS38	
	Signetics	54LS38	
	TI	SN54LS38	
54LS390	TI	SN54LS390	
54LS393	TI	SN54LS393	
54LS395	National	DM54LS395	
54LS395	Raytheon	54LS395	
	Signetics	54LS395	
	TI	SN54LS395	
54LS40	Motorola	SN54LS40	
	National	DM54LS40	
	Raytheon	54LS40	
	Signetics	54LS40	
	TI	SN54LS40	
54LS42	Motorola	SN54LS42	
	National	DM54LS42	
	Raytheon	54LS42	
	Signetics	54LS42	
	TI	SN54LS42	
54LS47	Motorola	SN54LS47	
54LS49	Motorola	SN54LS49	
54LS490	TI	SN54LS490	
54LS502	Motorola	SN54LS502	
54LS503	Motorola	SN54LS503	
54LS504	Motorola	SN54LS504	
54LS51	Motorola	SN54LS51	
	National	DM54LS51	
	Raytheon	54LS51	
	Signetics	54LS51	
	TI	SN54LS51	
54LS54	Motorola	SN54LS54	
	National	DM54LS54	
	Raytheon	54LS54	
	Signetics	54LS54	
	TI	SN54LS54	
54LS540	Motorola	SN54LS540	
54LS541	Motorola	SN54LS541	
54LS55	Motorola	SN54LS55	
	National	DM54LS55	
	Raytheon	54LS55	
	Signetics	54LS55	
	TI	SN54LS55	
54LS573	Motorola	SN54LS573	
54LS574	Motorola	SN54LS574	
54LS670	Motorola	SN54LS670	
	National	DM54LS670	
	Raytheon	54LS670	
	Signetics	54LS670	
	TI	SN54LS670	
54LS73	Motorola	SN54LS73A	
	National	DM54LS73	
	Raytheon	54LS73	
	Signetics	54LS73	
	TI	SN54LS73A	
54LS74	Motorola	SN54LS74A	
	National	DM54LS74	
	Raytheon	54LS74	
	Signetics	54LS74	
	TI	SN54LS74A	
54LS75	Motorola	SN54LS75	
	National	DM54LS75	
	Raytheon	54LS75	
	Signetics	54LS75	
	TI	SN54LS75	
54LS76	Motorola	SN54LS76A	
54LS77	Motorola	SN74LS77	
	Raytheon	54LS77	
	TI	SN54LS77	
54LS78	Motorola	SN54LS78A	
54LS83	Motorola	SN54LS83	
	National	DM54LS83	
	Raytheon	54LS83A	
	TI	SN54LS83A	
54LS85	Motorola	SN54LS85	
	National	DM54LS85	
	Raytheon	54LS85	
	Signetics	54LS85	
	TI	SN54LS85	
54LS86	Motorola	SN54LS86	
	Raytheon	54LS86	
	Signetics	54LS86	
	TI	SN54LS86	
54LS90	Motorola	SN54LS90	
	National	DM54LS90	
	Raytheon	54LS90	
	Signetics	54LS90	
	TI	SN54LS90	
54LS92	Raytheon	54LS92	
54LS93	Motorola	SN54LS93	
	Raytheon	54LS93	
	Signetics	54LS93	
	TI	SN54LS93	
54LS95B	Motorola	SN54LS95B	
	National	DM54LS95B	
	Raytheon	54LS95B	
	TI	SN54LS95B	
54S00	TI	SN54S00	
54S02	Signetics	54S02	
	TI	SN54S02	
54S03	TI	SN54S03	
54S04	Signetics	54S04	
	TI	SN54S04	
54S05	Signetics	54S05	
	TI	SN54S05	
54S08	Signetics	54S08	
	TI	SN54S08	
54S09	Signetics	54S09	
	TI	SN54S09	
54S10	TI	SN54S10	
54S11	Signetics	54S11	
	TI	SN54S11	
54S112	Motorola	SN54S112	
	TI	SN54S112	
54S113	Motorola	SN54S113	
	TI	SN54S113	
54S114	TI	SN54S114	
54S132	TI	SN54S132	
54S133	TI	SN54S133	
54S134	TI	SN54S134	
54S135	TI	SN54S135	
54S138	AMD	SN54S138	
	TI	SN54S138	
54S139	AMD	SN54S139	
	Signetics	54S139	
	TI	SN54S139	
54S15	Signetics	54S15	
	TI	SN54S15	
54S151	AMD	SN54S151	
	Signetics	54S151	
	TI	SN54S151	
54S153	AMD	SN54S153	
	Signetics	54S153	
	TI	SN54S153	
54S157	AMD	SN54S157	
	Signetics	54S157	
	TI	SN54S157	
54S158	AMD	SN54S158	
	Signetics	54S158	
	TI	SN54S158	
54S174	AMD	SN54S174	
	TI	SN54S174	
54S175	AMD	SN54S175	
	TI	SN54S175	
54S181	AMD	SN54S181	
	Signetics	54S181	
	TI	SN54S181	
54S182	TI	SN54S182	
54S194	AMD	SN54S194	
	TI	SN54S194	
54S195	AMD	SN54S195	
	TI	SN54S195	
54S20	TI	SN54S20	
54S22	National	DM54S22	
	Signetics	54S22	
	TI	SN54S22	
54S251	AMD	SN54S251	
	Signetics	54S251	
	TI	SN54S251	
54S253	AMD	SN54S253	
	Signetics	54S253	
54S257	AMD	SN54S257	
	Signetics	54S257	
	TI	SN74S257	
54S258	AMD	SN54S258	
	Signetics	54S258	
	TI	SN54S258	
54S30	TI	SN54S30	
54S32	Signetics	54S32	
	TI	SN54S32	
54S40	TI	SN54S40	
54S51	TI	SN54S51	
54S64	TI	SN54S64	
54S65	TI	SN54S65	
54S74	TI	SN54S74	
54S86	Signetics	54S86	
	TI	SN54S86	
6400	Motorola	MC5400	
	National	DM5400	

♦ Discontinued

The manufacturers report their devices can be used as direct replacements.
Performance details often differ, so compare the specifications considering your requirements.

Fairchild (cont'd)

Manufacturer Device	Replacement Source	Device	IC Master Page
5400	Signetics	5400	
	TI	SN5400	
5401	Motorola	MC5401	
	National	DM5401	
	Signetics	5401	
	TI	SN5401	
5402	Motorola	MC5402	
	National	DM5402	
	Signetics	5402	
	TI	SN5402	
5403	Motorola	MC5403	
	National	DM5403	
	Signetics	5403	
	TI	SN5403	
5404	Motorola	MC5404	
	National	DM5404	
	Signetics	5404	
	TI	SN5404	
5405	Motorola	MC5405	
	National	DM5405	
	Signetics	5405	
	TI	SN5405	
5406	Motorola	MC5406	
	National	DM5406	
	Signetics	5406	
	TI	SN5406	
5407	Motorola	MC5407	
	National	DM5407	
	Signetics	5407	
	TI	SN5407	
5408	Motorola	MC5408	
	National	DM5408	
	Signetics	5408	
	TI	SN5408	
5409	Motorola	MC5409	
	National	DM5409	
	Signetics	5409	
	TI	SN5409	
5410	Motorola	MC5410	
	National	DM5410	
	Signetics	5410	
	TI	SN5410	
54107	AMD	SN54107	
	Motorola	MC54107	
	National	DM54107	
	Signetics	54107	
	TI	SN54107	
5411	National	DM5411	
	Signetics	5411	
	TI	SN5411	
54116	Signetics	54116	
	TI	SN54116	
5412	Motorola	MC5412	
	Signetics	5412	
	TI	SN5412	
54121	Motorola	MC54121	
		MC9603	
	National	DM54121	
	Signetics	54121	
	TI	SN54121	
54122	Motorola	MC54122	
	TI	SN54122	
54123	AMD	SN54123	
	Motorola	MC54123	
	National	DM54123	
	Signetics	54123	
	TI	SN54123	
54125	National	DM54125	
	Signetics	54125	
	TI	SN54125	
54126	National	DM54126	
	Signetics	54126	
	TI	SN54126	
5413	Motorola	MC5413	
	National	DM5413	
	Signetics	5413	
	TI	SN5413	
54132	Motorola	MC54132	
	National	DM54132	
	Signetics	54132	
	TI	SN54132	
54136	TI	SN54136	
5414	Motorola	MC5414	
5414	National	DM5414	
	Signetics	5414	
	TI	SN5414	
54145	Motorola	MC54145	
		MC93145	
	National	DM54145	
	Raytheon	54145	
	Signetics	54145	
	TI	SN54145	
54150	Motorola	MC54150	
		MC93150	
	National	DM54150	
	Raytheon	54150	
	Signetics	54150	
	TI	SN54150	
54151	Motorola	MC54151	
		MC93151	
	National	DM54151	
	Raytheon	54151	
	Signetics	54151	
	TI	SN54151	
		SN54151A	
54152	Motorola	MC54152	
		MC93152	
	Raytheon	54152	
	Signetics	54152	
	TI	SN54152A	
54153	AMD	SN54153	
	Motorola	MC54153	
		MC93153	
	National	DM54153	
	Signetics	54153	
	TI	SN54153	
54154	AMD	SN54154	
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		MC9311	
	National	DM54154	
	Signetics	54154	
	TI	SN54154	
54155	Motorola	MC54155	
	National	DM54155	
	Signetics	54155	
	TI	SN54155	
54156	Motorola	MC54156	
	National	DM54156	
	Signetics	54156	
	TI	SN54156	
54157	AMD	SN54157	
	Motorola	MC54157	
		MC9322	
	National	DM54157	
	Signetics	54157	
	TI	SN54157	
54159	TI	SN54159	
5416	Motorola	MC5416	
	National	DM5416	
	Signetics	5416	
	TI	SN5416	
54160	AMD	SN54160	
	Motorola	MC54160	
		MC9310	
	National	DM54160	
	Signetics	54160	
	TI	SN54160	
54161	AMD	SN54161	
	Motorola	MC54161	
		MC9316	
	National	DM54161	
	Signetics	54161	
	TI	SN54161	
54162	AMD	SN54162	
	Motorola	MC54162	
	National	DM54162	
	Signetics	54162	
	TI	SN54162	
54163	AMD	SN54163	
	Motorola	MC54163	
	National	DM54163	
	Signetics	54163	
	TI	SN54163	
54164	AMD	SN54164	
	National	DM54164	
	Signetics	54164	
	TI	SN54164	
54165	Motorola	MC54165	
	National	DM54165	
54165	Signetics	54165	
	TI	SN54165	
54166	National	DM54166	
	Signetics	54166	
	TI	SN54166	
5417	Motorola	MC5417	
		MC9417	
	National	DM5417	
	Signetics	5417	
	TI	SN5417	
54170	National	DM54170	
	Signetics	54170	
	TI	SN54170	
54173	National	DM54173	
	TI	SN54173	
54174	AMD	SN74174	
	Motorola	MC54174	
	National	DM54174	
	Signetics	54174	
	TI	SN54174	
54175	AMD	SN54175	
	Motorola	MC54175	
	National	DM54175	
	Signetics	54175	
	TI	SN54175	
54176	Motorola	MC54176	
		MC93176	
	National	DM54176	
	Signetics	54176	
	TI	SN54176	
54177	Motorola	MC54177	
		MC93177	
	National	DM54177	
	Signetics	54177	
	TI	SN54177	
54178	Motorola	MC93178	
	TI	SN54178	
54179	Motorola	MC93179	
	TI	SN54179	
54180	Motorola	MC54180	
		MC93180	
	National	DM54180	
	Signetics	54180	
	TI	SN54180	
54181	AMD	SN54181	
	Motorola	MC54181	
		MC9341	
	National	DM54181	
	Signetics	54181	
	TI	SN54181	
54182	AMD	SN54182	
	Motorola	MC54182	
		MC9342	
	National	DM54182	
	Signetics	54182	
	TI	SN54182	
54190	Motorola	MC54190	
	National	DM54190	
	Signetics	54190	
	TI	SN54190	
54191	Motorola	MC54191	
	National	DM54191	
	Signetics	54191	
	TI	SN54191	
54192	AMD	SN54192	
	Motorola	MC54192	
		MC9360	
	National	DM54192	
	Signetics	54192	
	TI	SN54192	
54193	AMD	SN54193	
	Motorola	MC54193	
		MC9366	
	National	DM54193	
	Signetics	54193	
	TI	SN54193	
54194	AMD	SN54194	
	Motorola	MC54194	
	National	DM54194	
	Signetics	54194	
	TI	SN54194	
54195	AMD	SN54195	
	Motorola	MC54195	
	National	DM54195	
	Signetics	54195	
	TI	SN54195	
54196	Motorola	MC54196	
	National	DM54196	
	Signetics	54196	
	TI	SN54196	
54197	Motorola	MC54197	
	National	DM54197	
	Signetics	54197	
	TI	SN54197	
54198	National	DM54198	
	Signetics	54198	
	TI	SN54198	
54199	National	DM54199	
	Signetics	54199	
	TI	SN54199	
5420	Motorola	MC5420	
	National	DM5420	
	Signetics	5420	
	TI	SN5420	
5421	Signetics	5421	
5422	Raytheon	5422	
	TI	SN5422	
5423	Motorola	MC5423	
	National	DM5423	
	TI	SN5423	
5425	Motorola	MC5425	
	National	DM5425	
	TI	SN5425	
5426	Motorola	MC5426	
	National	DM5426	
	Signetics	5426	
	TI	SN5426	
5427	Motorola	MC5427	
	National	DM5427	
	TI	SN5427	
54279	Signetics	54279	
	TI	SN54279	
54283	TI	SN54283	
54298	Motorola	MC54298	
	Signetics	54298	
	TI	SN54298	
5430	Motorola	MC5430	
	National	DM5430	
	Signetics	5430	
	TI	SN5430	
5432	National	DM5432	
	Signetics	5432	
	TI	SN5432	
5437	Motorola	MC5437	
	National	DM5437	
	Signetics	5437	
	TI	SN5437	
5438	Motorola	MC5438	
	National	DM5438	
	Signetics	5438	
	TI	SN5438	
5440	Motorola	MC5440	
	National	DM5440	
	Signetics	5440	
	TI	SN5440	
5441	National	DM5441	
5442	Motorola	MC5442	
		MC9352	
	National	DM5442	
	Signetics	5442	
	TI	SN5442	
5443	Motorola	MC5443	
		MC9353	
	Raytheon	5443	
	Signetics	5443	
	TI	SN5443	
5444	Motorola	MC5444	
		MC9354	
	Signetics	5444	
	TI	SN5444	
		SN5444A	
5445	Motorola	MC5445	
		MC9345	
	National	DM5445	
	Signetics	5445	
	TI	SN5445	
		SN5445A	
5446	Motorola	MC5446	
		MC9357A	
	National	DM5446	
	Signetics	5446	
	TI	SN5446	

♦ Discontinued

Bold face device numbers indicate manufacturers data is provided in the IC Master on the pages noted.

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Manufacturer Device	Replacement Source	Device	IC Master Page
5446	TI	SN5446A	
5447	Motorola	MC5447	
		MC9357B	
	National	DM5447	
	Signetics	5447	
	TI	SN5447	
		SN5447A	
5448	Motorola	MC5448	
		MC9358	
	National	DM5448	
	Signetics	5448	
	TI	SN5448	
5449	Motorola	MC5449	
		MC9359	
	TI	SN5449	
5450	Motorola	MC5450	
	National	DM5450	
	Signetics	5450	
	TI	SN5450	
5451	Motorola	MC5451	
	National	DM5451	
	Signetics	5451	
	TI	SN5451	
5453	Motorola	MC5453	
	National	DM5453	
	Signetics	5453	
	TI	SN5453	
5454	Motorola	MC5454	
	National	DM5454	
	Signetics	5454	
	TI	SN5454	
5460	Motorola	MC5460	
	National	DM5460	
	Signetics	5460	
	TI	SN5460	
5470	Motorola	MC5470	
	National	DM5470	
	Signetics	5470	
	TI	SN5470	
5472	Motorola	MC5472	
	National	DM5472	
	Signetics	5472	
	TI	SN5472	
5473	Motorola	MC5473	
	National	DM5473	
	Signetics	5473	
	TI	SN5473	
5474	Motorola	MC5474	
	National	DM5474	
	Signetics	5474	
	TI	SN5474	
5475	Motorola	MC5475	
		MC9375	
	National	DM5475	
	Signetics	5475	
	TI	SN5475	
5476	Motorola	MC5476	
	National	DM5476	
	Signetics	5476	
	TI	SN5476	
5477	Motorola	MC5477	
		MC9377	
	Signetics	5477	
	TI	SN5477	
5480	Motorola	MC5480	
		MC9380	
	Signetics	5480	
	TI	SN5480	
5481	Motorola	MC4304	
	TI	SN5481A	
5482	Motorola	MC5482	
		MC9382	
	TI	SN5482	
5483	Motorola	MC9383	
	Signetics	5483A	
	TI	SN5483A	
5485	Motorola	MC5485	
	National	DM5485	
	Signetics	5485	
	TI	SN5485	
5486	Motorola	MC5486	
	National	DM5486	
	Raytheon	5486	
5486	Signetics	5486	
	TI	SN5486	
5488	Motorola	MCM4002	
	TI	SN5488A	
5489	AMD	SN5489	
		5889	
	Motorola	MC4064	
	National	DM5489	
	TI	SN5489	
5490	Motorola	MC5490	
		MC9390	
	National	DM5490	
	Signetics	5490	
	TI	SN5490	
		SN5490A	
5491	Motorola	MC5491	
		MC9391	
	National	DM5491	
	Signetics	5491	
	TI	SN5491	
		SN5491A	
5492	Motorola	MC5492	
		MC9392	
	National	DM5492	
	Signetics	5492	
	TI	SN5492	
		SN5492A	
5493	Motorola	MC5493	
		MC9393	
	National	DM5493	
	Signetics	5493	
	TI	SN5493	
		SN5493A	
5494	Motorola	MC5494	
		MC9394	
	Signetics	5494	
	TI	SN5494	
		SN5494A	
5495	Motorola	MC5495	
		MC9395	
	National	DM5495	
	Signetics	5495	
	TI	SN5495	
		SN5495A	
5496	Motorola	MC5496	
		MC9396	
	National	DM5496	
	Signetics	5496	
	TI	SN5496	
5497	Motorola	MC5497	
	TI	SN5497	
55107	AMD	SN55107B	
	Motorola	MC55107	
	National	DS55107	
	Raytheon	RM55107	
	TI	SN55107	
55108	AMD	SN55108	
	Motorola	MC55108	
	National	DS55108	
	Raytheon	RM55108	
	TI	SN55108	
55109	AMD	SN55109	
	Raytheon	RM55109	
	TI	SN55109	
55110	AMD	SN55110	
	Raytheon	RM55110	
	TI	SN55110	
55121	TI	SN55121	
55122	TI	SN55122	
5520	AMD	SN5520	
	Silicon G	SG5520	
5521	AMD	SN5521	
	Silicon G	SG5521	
55232	TI	SN55232	
55233	TI	SN55232	
55234	AMD	SN55234	
	TI	SN55234	
55235	AMD	SN55235	
	Motorola	MC55325	
	TI	SN55234	
55238	AMD	SN55238	
	TI	SN55238	
55239	AMD	SN55239	
	TI	SN55239	
5524	AMD	SN5524	
	Motorola	SN5524	
5524	National	DS5524	
	Silicon G	SG5524	
	TI	SN5524	
5525	AMD	SN5525	
	Motorola	SN5525	
	Silicon G	SG5525	
	TI	SN5524	
5528	Motorola	MC5528	
	Silicon G	SG5528	
	TI	SN5528	
5529	Motorola	MC5529	
	Silicon G	SG5529	
	TI	SN5528	
55325	AMD	SN55325	
	Silicon G	SG55325	
	TI	SN55325	
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55327	TI	SN55327	
5534	Motorola	MC5534	
	Silicon G	SG5534	
5535	Motorola	MC5535	
	Silicon G	SG5535	
5538	Motorola	MC5538	
	Silicon G	SG5538	
5539	Motorola	MC5539	
	Silicon G	SG5539	
55450	Silicon G	SG55450	
	TI	SN55450	
55451	Silicon G	SG55451	
	TI	SN55451	
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	TI	SN55453	
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	TI	SN55454	
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	TI	SN55460	
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	TI	SN55461	
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55470	Silicon G	SG55470	
	TI	SN55470	
55471	Silicon G	SG55471	
	TI	SN55471	
55472	Silicon G	SG55472	
	TI	SN55472	
55473	Silicon G	SG55473	
	TI	SN55473	
55474	Silicon G	SG55474	
	TI	SN55474	
6105	SSS	SCL5430	
68316	**AMI**	**S4216B**	**1209**
68316E	**AMI**	**S6831B**	**1215,1806**
74H00	Motorola	MC74H00	
	National	DM74H00	
	NEC America	μPB74H00	
	Raytheon	74H00	
	Signetics	74H00	
	TI	SN74H00	
74H01	Motorola	MC74H01	
	National	DM74H01	
	NEC America	μPB74H01	
	Raytheon	74H01	
	Signetics	74H01	
	TI	SN74H01	
74H04	Motorola	MC74H04	
	National	DM74H04	
	NEC America	μPB74H04	
	Raytheon	74H04	
	Signetics	74H04	
	TI	SN74H04	
74H05	Motorola	MC74H05	
	National	DM74H05	
	Raytheon	74H05	
	Signetics	74H05	
	TI	SN74H05	
74H08	Motorola	MC74H08	
	National	DM74H08	
	Signetics	74H08	
74H10	Motorola	MC74H10	
	National	DM74H10	
	NEC America	μPB74H10	
	Raytheon	74H10	
	Signetics	74H10	
	TI	SN74H10	
74H101	Motorola	MC74H101	
	TI	SN74H101	
74H102	Motorola	MC74H102	
	Signetics	74H102	
	TI	SN74H102	
74H103	National	DM74H103	
	Signetics	74H103	
	TI	SN74H103	
74H105	Motorola	MC9001	
74H106	National	DM74H106	
	Signetics	74H106	
	TI	SN74H106	
74H108	Motorola	MC74H108	
	National	DM74H108	
	Signetics	74H108	
	TI	SN74H108	
74H11	Motorola	MC74H11	
	National	DM74H11	
	Raytheon	74H11	
	Signetics	74H11	
	TI	SN74H11	
74H15	Raytheon	74H15	
	TI	SN74H15	
74H183	Hitachi	HD74H183	
	TI	SN74H183	
74H20	Motorola	MC74H20	
	National	DM74H20	
	NEC America	μPB74H20	
	Raytheon	74H20	
	Signetics	74H20	
	TI	SN74H20	
74H21	Motorola	MC74H21	
	National	DM74H21	
	Signetics	74H21	
	TI	SN74H21	
74H22	Motorola	MC74H22	
	National	DM74H22	
	Raytheon	74H22	
	Signetics	74H22	
	TI	SN74H22	
74H30	Motorola	MC74H30	
	National	DM74H30	
	NEC America	μPB74H30	
	Signetics	74H30	
	TI	SN74H30	
74H40	Motorola	MC74H40	
	National	DM74H40	
	NEC America	μPB74H40	
	Raytheon	74H40	
	Signetics	74H40	
	TI	SN74H40	
74H50	Motorola	MC74H50	
	National	DM74H50	
	Signetics	74H50	
	TI	SN74H50	
74H51	Motorola	MC74H51	
	National	DM74H51	
	NEC America	μPB74H51	
	Signetics	74H51	
	TI	SN74H51	
74H52	Motorola	MC74H52	
	National	DM74H52	
	Signetics	74H52	
	TI	SN74H52	
74H53	Motorola	MC74H53	
	National	DM74H53	
	Signetics	74H53	
	TI	SN74H53	
74H54	Motorola	MC74H54	
	National	DM74H54	
	Signetics	74H54	
	TI	SN74H54	
74H55	Motorola	MC74H55	
	National	DM74H55	
	Signetics	74H55	
	TI	SN74H55	
74H60	Motorola	MC74H60	
	National	DM74H60	
	Signetics	74H60	
	TI	SN74H60	

♦ Discontinued

The manufacturers report their devices can be used as direct replacements.
Performance details often differ, so compare the specifications considering your requirements.

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Manufacturer Device	Replacement Source	Device	IC Master Page
74H61	Motorola	MC74H61	
	Signetics	74H61	
	TI	SN74H61	
74H62	Motorola	MC74H62	
	National	DM74H62	
	Signetics	74H62	
	TI	SN74H62	
74H71	Motorola	MC74H71	
	National	DM74H71	
	Signetics	74H71	
	TI	SN74H71	
74H72	Motorola	MC74H72	
	National	DM74H72	
	Signetics	74H72	
	TI	SN74H72	
74H73	Motorola	MC74H73	
	National	DM74H73	
	Signetics	74H73	
	TI	SN74H73	
74H74	Motorola	MC74H74	
	National	DM74H74	
	Raytheon	74H74	
	Signetics	74H74	
	TI	SN74H74	
74H76	National	DM74H76	
	Signetics	74H76	
	TI	SN74H76	
74H78	National	DM74H78	
	TI	SN74H78	
74H87	Motorola	MC74H87	
	TI	SN74H87	
74LS00	Hitachi	HD74LS00	
	Motorola	SN74LS00	
	National	DM74LS00	
	NEC America	μPB74LS00	
	Raytheon	74LS00	
	Signetics	74LS00	
	TI	SN74LS00	
74LS01	Hitachi	HD74LS01	
	National	DM74LS01	
	Raytheon	74LS01	
	Signetics	74LS01	
	TI	SN74LS01	
74LS02	Hitachi	HD74LS02	
	Motorola	SN74LS02	
	National	DM74LS02	
	NEC America	μPB74LS02	
	Raytheon	74LS02	
	Signetics	74LS02	
	TI	SN74LS02	
74LS03	Hitachi	HD74LS03	
	Motorola	SN74LS03	
	National	DM74LS03	
	NEC America	μPB74LS03	
	Raytheon	74LS03	
	Signetics	74LS03	
	TI	SN74LS03	
74LS04	Hitachi	HD74LS04	
	Motorola	SN74LS04	
	National	DM74LS04	
	NEC America	μPB74LS04	
	Raytheon	74LS04	
	Signetics	74LS04	
	TI	SN74LS04	
74LS05	Hitachi	HD74LS05	
	Motorola	SN74LS05	
	National	DM74LS05	
	NEC America	μPB74LS05	
	Raytheon	74LS05	
	Signetics	74LS05	
	TI	SN74LS05	
74LS08	Hitachi	HD74LS08	
	Motorola	SN74LS08	
	National	DM74LS08	
	NEC America	μPB74LS08	
	Raytheon	74LS08	
	Signetics	74LS08	
	TI	SN74LS08	
74LS09	Hitachi	HD74LS09	
	Motorola	SN74LS09	
	National	DM74LS09	
	Raytheon	74LS09	
	Signetics	74LS09	
74LS09	TI	SN74LS09	
74LS10	Hitachi	HD74LS10	
	Motorola	SN74LS10	
	National	DM74LS10	
	NEC America	μPB74LS10	
	Raytheon	74LS10	
	Signetics	74LS10	
	TI	SN74LS10	
74LS107	Hitachi	HD74LS107	
	Motorola	SN74LS107A	
	National	DM74LS107	
	Raytheon	74LS107	
	Signetics	74LS107	
	TI	SN74LS107	
74LS109	Motorola	SN74LS109A	
	National	DM74LS109	
	NEC America	μPB74LS109	
	Raytheon	74LS109	
	Signetics	74LS109	
	TI	SN74LS109A	
74LS11	Hitachi	HD74LS11	
	Motorola	SN74LS11	
	National	DM74LS11	
	NEC America	μPB74LS11	
	Raytheon	74LS11	
	Signetics	74LS11	
	TI	SN74LS11	
74LS112	Hitachi	HD74LS112	
	Motorola	SN74LS112A	
	National	DM74LS112	
	NEC America	μPB74LS112	
	Raytheon	74LS112	
	Signetics	74LS112	
	TI	SN74LS112	
74LS113	Hitachi	74LS113	
	Motorola	SN74LS113A	
	National	DM74LS113	
	NEC America	μPB74LS113	
	Raytheon	74LS113	
	Signetics	74LS113	
	TI	SN74LS113	
74LS114	Hitachi	HD74LS114	
	Motorola	SN74LS114A	
	National	DM74LS114	
	Raytheon	74LS114	
	Signetics	74LS114	
	TI	SN74LS114A	
74LS12	Hitachi	HD74LS12	
	Motorola	SN74LS12	
	National	DM74LS12	
	Raytheon	74LS12	
	Signetics	74LS12	
	TI	SN74LS12	
74LS125	National	DM74LS125	
	Raytheon	74LS125	
	Signetics	74LS125	
	TI	SN74LS125	
		SN74LS125A	
74LS126	Motorola	SN74LS126	
	National	DM74LS126	
	Raytheon	74LS126	
	Signetics	74LS126	
	TI	SN74LS126	
		SN74LS126A	
74LS13	Hitachi	HD74LS13	
	Motorola	SN74LS13	
	National	DM74LS13	
	Raytheon	74LS13	
	Signetics	74LS13	
	TI	SN74LS13	
74LS132	Hitachi	HD74LS132	
	Motorola	SN74LS132	
	National	DM74LS132	
	Raytheon	74LS132	
	Signetics	74LS132	
	TI	SN74LS132	
74LS133	Motorola	SN74LS133	
74LS136	Hitachi	HD74LS136	
	Motorola	SN74LS136	
	National	DM74LS136	
	Raytheon	74LS136	
	Signetics	74LS136	
	TI	SN74LS136	
74LS138	AMD	SN74LS138	
	Hitachi	HD74LS138	
	Motorola	SN74LS138	
74LS138	National	DM74LS138	
	NEC America	μPB74LS138	
	Raytheon	74LS138	
	Signetics	74LS138	
	TI	SN74LS138	
74LS139	AMD	SN74LS139	
	Hitachi	HD74LS139	
	Motorola	SN74LS139	
	National	DM74LS139	
	NEC America	μPB74LS139	
	Raytheon	74LS139	
	Signetics	74LS139	
	TI	SN74LS139	
74LS14	Hitachi	HD74LS14	
	Motorola	SN74LS14	
	National	DM74LS14	
	Raytheon	74LS14	
	Signetics	74LS14	
	TI	SN74LS14	
74LS145	Signetics	74LS145	
	TI	SN74LS145	
74LS15	Hitachi	HD74LS15	
	Motorola	SN74LS15	
	National	DM74LS15	
	Raytheon	74LS15	
	Signetics	74LS15	
	TI	SN74LS15	
74LS151	AMD	SN74LS151	
	Hitachi	HD74LS151A	
	Motorola	SN74LS151	
	National	DM74LS151	
	NEC America	μPB74LS151	
	Raytheon	74LS151	
	Signetics	74LS151	
	TI	SN74LS151	
74LS152	Hitachi	HD74LS152	
	Motorola	SN74LS152	
	Raytheon	74LS152	
74LS153	AMD	SN74LS153	
	Hitachi	HD74LS153	
	Motorola	SN74LS153	
	National	DM74LS153	
	NEC America	μPB74LS153	
	Raytheon	74LS153	
	Signetics	74LS153	
	TI	SN74LS153	
74LS155	Hitachi	HD74LS155	
	Motorola	SN74LS155	
	National	DM74LS155	
	NEC America	μPB74LS155	
	Raytheon	74LS155	
	Signetics	74LS155	
	TI	SN74LS155	
74LS156	Hitachi	HD74LS156	
	Motorola	SN74LS156	
	National	DM74LS156	
	Raytheon	74LS156	
	Signetics	74LS156	
	TI	SN74LS156	
74LS157	AMD	SN74LS157	
	Motorola	SN74LS157	
	National	DM74LS157	
	NEC America	μPB74LS157	
	Raytheon	74LS157	
	Signetics	74LS157	
	TI	SN74LS157	
74LS158	AMD	SN74LS158	
	Hitachi	HD74LS158	
	Motorola	SN74LS158	
	National	DM74LS158	
	Raytheon	74LS158	
	Signetics	74LS158	
	TI	SN74LS158	
74LS160	AMD	SN74LS160	
	Hitachi	HD74LS160A	
	Motorola	SN74LS160A	
	National	DM74LS160	
	Raytheon	74LS160	
	Signetics	74LS160A	
	TI	SN74LS160A	
74LS161	AMD	SN74LS161	
	Hitachi	HD74LS161A	
	Motorola	SN74LS161A	
	National	DM74LS161	
	NEC America	μPB74LS161	
	Raytheon	74LS161	
74LS161	Signetics	74LS161A	
	TI	SN74LS161A	
74LS162	AMD	SN74LS162	
	Hitachi	HD74LS162A	
	Motorola	SN74LS162A	
	National	DM74LS162	
	Raytheon	74LS162	
	Signetics	74LS162A	
	TI	SN74LS162A	
74LS163	AMD	SN74LS163	
	Hitachi	HD74LS163A	
	Motorola	SN74LS163A	
	National	DM74LS163	
	Raytheon	74LS163	
	Signetics	74LS163A	
	TI	SN74LS163A	
74LS164	AMD	SN74LS164	
	Hitachi	HD74LS164	
	Motorola	SN74LS164A	
	National	DM74LS164	
	NEC America	μPB74LS164	
	Raytheon	74LS164	
	Signetics	74LS164	
	TI	SN74LS164A	
74LS165	TI	SN74LS165	
74LS168	AMD	SN74LS168	
	National	DM74LS168	
	TI	SN74LS168	
74LS169	AMD	SN74LS169	
	National	DM74LS169	
	TI	SN74LS169	
74LS170	AMD	SN74LS170	
	Motorola	SN74LS170	
	National	DM74LS170	
	Raytheon	74LS170	
	Signetics	74LS170	
	TI	SN74LS170	
74LS173	National	DM74LS173	
	Signetics	74LS173	
	TI	SN74LS173	
74LS174	AMD	SN74LS174	
	Hitachi	HD74LS174	
	Motorola	SN74LS174	
	National	DM74LS174	
	Raytheon	74LS174	
	Signetics	74LS174	
	TI	SN74LS174	
74LS175	AMD	SN74LS175	
	Hitachi	HD74LS175	
	Motorola	SN74LS175	
	National	DM74LS175	
	NEC America	μPB74LS175	
	Raytheon	74LS175	
	Signetics	74LS175	
	TI	SN74LS175	
74LS181	AMD	SN74LS181	
	Motorola	SN74LS181	
	Raytheon	74LS181	
	Signetics	74LS181	
	TI	SN74LS181	
74LS190	AMD	SN74LS190	
	Motorola	SN74LS190	
	National	DM74LS190	
	Raytheon	74LS190	
	Signetics	74LS190	
	TI	SN74LS190	
74LS191	AMD	SN74LS191	
	Motorola	SN74LS191	
	National	DM74LS191	
	Raytheon	74LS191	
	Signetics	74LS191	
	TI	SN74LS191	
74LS192	AMD	SN74LS192	
	Motorola	SN74LS192	
	National	DM74LS192	
	NEC America	μPB74LS192	
	Raytheon	74LS192	
	Signetics	74LS192	
	TI	SN74LS192	
74LS193	AMD	SN74LS193	
	Motorola	SN74LS193	
	National	DM74LS193	
	NEC America	μPB74LS193	
	Raytheon	74LS193	
	Signetics	74LS193	
	TI	SN74LS193	

◆ Discontinued

Bold face device numbers indicate manufacturers data is provided in the IC Master on the pages noted.

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Manufacturer Device	Replacement Source	Device	IC Master Page
74LS194	AMD	SN74LS194A	
	Motorola	SN74LS194A	
	NEC America	μPB74LS194	
	Raytheon	74LS194A	
	Signetics	74LS194A	
	TI	SN74LS194A	
74LS194A	Hitachi	HD74LS194A	
74LS195	AMD	SN74LS195A	
	Hitachi	HD74LS195A	
	Motorola	SN74LS1954	
	NEC America	μPB74LS195	
	Raytheon	74LS195A	
	Signetics	74LS195A	
	TI	SN74LS195A	
74LS196	Motorola	SN74LS196	
	National	DM74LS196	
	Raytheon	74LS196	
	Signetics	74LS196	
	TI	SN74LS196	
74LS197	Motorola	SN74LS197	
	National	DM74LS197	
	Raytheon	74LS197	
	Signetics	74LS197	
	TI	SN74LS197	
74LS20	Hitachi	HD74LS20	
	Motorola	SN74LS20	
	National	DM74LS20	
	NEC America	μPB74LS20	
	Raytheon	74LS20	
	Signetics	74LS20	
	TI	SN74LS20	
74LS21	Hitachi	HD74LS21	
	Motorola	SN74LS21	
	National	DM74LS21	
	NEC America	μPB74LS21	
	Raytheon	74LS21	
	Signetics	74LS21	
	TI	SN74LS21	
74LS22	Hitachi	HD74LS22	
	Motorola	SN74LS22	
	National	DM74LS22	
	Raytheon	74LS22	
	Signetics	74LS22	
	TI	SN74LS22	
74LS221	Motorola	SN74LS221	
	National	DM74LS221	
	Raytheon	74LS221	
	Signetics	74LS221	
	TI	SN74LS221	
74LS240	AMD	SN74LS240	
	MMI	**74LS240**	**768**
	Motorola	SN74LS240	
	Raytheon	**74LS240**	**522**
	Signetics	74LS240	
	TI	SN74LS240	
74LS241	AMD	SN74LS241	
	MMI	**74LS241**	**768**
	Motorola	SN74LS241	
	Raytheon	**74LS241**	**525**
	Signetics	74LS241	
	TI	SN74LS241	
74LS242	AMD	SN74LS242	
	Motorola	SN74LS242	
	Raytheon	**74LS242**	**528**
	Signetics	74LS242	
	TI	SN74LS242	
74LS243	AMD	SN74LS243	
	Motorola	SN74LS243	
	Raytheon	**74LS243**	**528**
	Signetics	74LS243	
	TI	SN74LS243	
74LS244	AMD	SN74LS244	
	MMI	**74LS244**	**768**
	Motorola	SN74LS244	
	Raytheon	**74LS244**	**525**
	Signetics	74LS244	
	TI	SN74LS244	
74LS245	Motorola	SN74LS245	
74LS247	Hitachi	HD74LS247	
	Motorola	SN74LS247	
	National	DM74LS247	
	TI	SN74LS247	
74LS248	Hitachi	HD74LS248	
74LS248	Motorola	SN74LS248	
	National	DM74LS248	
	TI	SN74LS248	
74LS249	Hitachi	HD74LS249	
	Motorola	SN74LS249	
	National	DM74LS249	
	TI	SN74LS249	
74LS251	AMD	SN74LS251	
	Hitachi	HD74LS251	
	Motorola	SN74LS251	
	National	DM74LS251	
	NEC America	μPB74LS251	
	Raytheon	74LS251	
	Signetics	74LS251	
	TI	SN74LS251	
74LS253	AMD	SN74LS253	
	Hitachi	HD74LS253	
	Motorola	SN74LS253	
	National	DM74LS253	
	NEC America	μPB74LS253	
	Raytheon	74LS253	
	Signetics	74LS253	
	TI	SN74LS253	
74LS255	Raytheon	74LS255	
74LS256	Motorola	SN74LS256	
	Signetics	74LS256	
74LS257	AMD	SN74LS257	
	Hitachi	HD74LS257	
	Motorola	SN74LS257A	
	National	DM74LS257	
	NEC America	μPB74LS257	
	Raytheon	74LS257	
	Signetics	74LS257	
	TI	SN74LS257A	
74LS258	AMD	SN74LS258	
	Motorola	SN74LS258A	
	National	DM74LS258	
	NEC America	μPB74LS258	
	Raytheon	74LS258	
	Signetics	74LS258	
	TI	SN74LS258A	
74LS259	Motorola	SN74LS259	
	Signetics	74LS259	
	TI	SN74LS259	
74LS26	Hitachi	HD74LS26	
	Motorola	SN74LS26	
	National	DM74LS26	
	Raytheon	74LS26	
	Signetics	74LS26	
	TI	SN74LS26	
74LS260	Motorola	SN74LS260	
	Signetics	74LS260	
74LS266	Fairchild	74LS266	
	Motorola	SN74LS266	
	Raytheon	74LS266	
	Signetics	74LS266	
	TI	SN74LS266	
74LS27	Hitachi	HD74LS27	
	Motorola	SN74LS27	
	National	DM74LS27	
	NEC America	μPB74LS27	
	Raytheon	74LS27	
	Signetics	74LS27	
	TI	SN74LS27	
74LS273	AMD	SN74LS273	
	Signetics	74LS273	
	TI	SN74LS273	
74LS279	Motorola	SN74LS279	
	National	DM74LS279	
	NEC America	μPB74LS279	
	Raytheon	74LS279	
	Signetics	74LS279	
	TI	SN74LS279	
74LS28	Raytheon	74LS28	
	Signetics	74LS28	
	TI	SN74LS28	
74LS280	TI	SN74LS280	
74LS283	Hitachi	SN74LS283	
	Motorola	SN74LS283	
	National	DM74LS283	
	Raytheon	74LS283	
	Signetics	74LS283	
	TI	SN74LS283	
74LS290	Motorola	SN74LS290	
	National	DM74LS290	
	Signetics	74LS290	
74LS290	TI	SN74LS290	
74LS293	Motorola	SN74LS293	
	National	DM74LS293	
	Signetics	74LS293	
	TI	SN74LS293	
74LS295	Motorola	SN74LS295	
	NEC America	μPB74LS295	
	Raytheon	74LS295A	
	Signetics	74LS295	
	TI	SN74LS295B	
74LS298	Hitachi	HD74LS298	
	Motorola	SN74LS298	
	Raytheon	74LS298	
	Signetics	74LS298	
	TI	SN74LS298	
74LS299	AMD	SN74LS299	
	Raytheon	**74LS299**	**533**
	TI	SN74LS299	
74LS30	Hitachi	HD74LS30	
	Motorola	SN74LS30	
	National	DM74LS30	
	NEC America	μPB74LS30	
	Raytheon	74LS30	
	Signetics	74LS30	
	TI	SN74LS30	
74LS32	Hitachi	HD74LS32	
	Motorola	SN74LS32	
	National	DM74LS32	
	NEC America	μPB74LS32	
	Raytheon	74LS32	
	Signetics	74LS32	
	TI	SN74LS32	
74LS322	Motorola	SN74LS322	
74LS352	Motorola	SN74LS352	
	National	DM74LS352	
	TI	SN74LS352	
74LS353	Motorola	74LS353	
	National	DM74LS353	
	TI	SN74LS353	
74LS365	Motorola	SN74LS365A	
	National	DM74LS365	
	NEC America	μPB74LS365	
	Raytheon	74LS365	
	Signetics	74LS365A	
	TI	SN74LS365A	
74LS366	Motorola	SN74LS366A	
	National	DM74LS366	
	NEC America	μPB74LS366	
	Raytheon	74LS366	
	Signetics	74LS366A	
	TI	SN74LS366A	
74LS367	Hitachi	HD74LS367	
	Motorola	SN74LS367A	
	National	DM74LS367	
	NEC America	μPB74LS367	
	Raytheon	74LS367	
	Signetics	74LS367A	
	TI	SN74LS367A	
74LS368	Hitachi	HD74LS368	
	Motorola	SN74LS368A	
	National	DM74LS368	
	NEC America	μPB74LS368	
	Raytheon	74LS368	
	Signetics	74LS368A	
	TI	SN74LS368A	
74LS37	Hitachi	HD74LS37	
	Motorola	SN74LS37	
	National	DM74LS37	
	NEC America	μPB74LS37	
	Raytheon	74LS37	
	Signetics	74LS37	
	TI	SN74LS37	
74LS373	AMD	SN74LS373	
	MMI	**74LS373**	**505**
	Motorola	SN74LS373	
	Raytheon	**74LS373**	**543**
	Signetics	74LS373	
	TI	SN74LS373	
74LS374	AMD	SN74LS374	
	MMI	**74LS374**	**505**
	Raytheon	**74LS374**	**543**
	TI	SN74LS374	
74LS375	Motorola	SN74LS375	
74LS377	AMD	SN74LS377	
	Raytheon	**74LS377**	**549**
	Signetics	74LS377	
74LS377	TI	SN74LS377	
74LS378	AMD	SN74LS378	
	Signetics	SN74LS378	
	TI	SN74LS378	
74LS379	Motorola	SN74LS379	
74LS38	Hitachi	HD74LS38	
	Motorola	SN74LS38	
	National	DM74LS38	
	NEC America	μPB74LS38	
	Raytheon	74LS38	
	Signetics	74LS38	
	TI	SN74LS38	
74LS386	Motorola	SN74LS386	
	National	DM74LS386	
	Raytheon	74LS386	
	Signetics	74LS386	
	TI	SN74LS386	
74LS390	TI	SN74LS390	
74LS393	TI	SN74LS393	
74LS395	National	DM74LS395	
	Raytheon	74LS395	
	Signetics	74LS395	
	TI	SN74LS395	
74LS40	Hitachi	HD74LS40	
	Motorola	SN74LS40	
	National	DM74LS40	
	NEC America	μPB74LS40	
	Raytheon	74LS40	
	Signetics	74LS40	
	TI	SN74LS40	
74LS42	Hitachi	HD74LS42	
	Motorola	SN74LS42	
	National	DM74LS42	
	NEC America	μPB74LS42	
	Raytheon	74LS42	
	Signetics	74LS42	
	TI	SN74LS42	
74LS47	Hitachi	HD74LS47	
	Motorola	SN74LS47	
74LS48	Hitachi	HD74LS48	
	Motorola	SN74LS48	
74LS49	Hitachi	HD74LS49	
	Motorola	SN74LS49	
74LS490	TI	SN74LS490	
74LS502	Motorola	SN74LS502	
74LS503	Motorola	SN74LS503	
74LS504	Motorola	SN74LS504	
74LS51	Hitachi	HD74LS51	
	Motorola	SN74LS51	
	National	DM74LS51	
	NEC America	μPB74LS51	
	Raytheon	74LS51	
	Signetics	74LS51	
	TI	SN74LS51	
74LS54	Hitachi	HD74LS54	
	Motorola	SN74LS54	
	National	DM74LS54	
	NEC America	μPB74LS54	
	Raytheon	74LS54	
	Signetics	74LS54	
	TI	SN74LS54	
74LS540	Motorola	SN74LS540	
74LS541	Motorola	SN74LS541	
74LS55	Hitachi	HD74LS55	
	Motorola	SN74LS55	
	National	DM74LS55	
	NEC America	μPB74LS55	
	Raytheon	74LS55	
	Signetics	74LS55	
	TI	SN74LS55	
74LS573	Motorola	SN74LS573	
74LS574	Motorola	SN74LS574	
74LS670	Motorola	SN74LS670	
	National	DM74LS670	
	Raytheon	74LS670	
	Signetics	74LS670	
	TI	SN74LS670	
74LS73	Hitachi	HD74LS73	
	Motorola	SN74LS73A	
	National	DM74LS73	
	Raytheon	74LS73	
	Signetics	74LS73	
	TI	SN74LS73A	
74LS74	Hitachi	HD74LS74A	
	Motorola	SN74LS74A	
	National	DM74LS74	

♦ Discontinued

The manufacturers report their devices can be used as direct replacements.
Performance details often differ, so compare the specifications considering your requirements.

Fairchild (cont'd)

Manufacturer Device	Replacement Source	Device	IC Master Page
74LS74	NEC America	μPB74LS74	
	Raytheon	74LS74	
	Signetics	74LS74	
	TI	SN74LS74A	
74LS75	Motorola	SN74LS75	
	National	DM74LS75	
	Raytheon	74LS75	
	Signetics	74LS75	
	TI	SN74LS75	
74LS76	Hitachi	HD74LS76	
	Motorola	SN74LS76A	
74LS77	National	DM74LS77	
	Raytheon	54LS77	
74LS78	Hitachi	HD74LS78	
	Motorola	SN74LS78A	
74LS83	Hitachi	HD74LS183A	
	Motorola	SN74LS83A	
	National	DM74LS83	
		DM74LS83A	
	Raytheon	74LS83A	
	Signetics	74LS83	
	TI	SN74LS83A	
74LS85	Motorola	SN74LS85	
	National	DM74LS85	
	Raytheon	74LS85	
	Signetics	74LS85	
	TI	SN74LS85	
74LS86	Hitachi	HD74LS86	
	Motorola	SN74LS86	
	NEC America	μPB74LS86	
	Raytheon	74LS86	
	Signetics	74LS86	
	TI	SN74LS86	
74LS90	Motorola	SN74LS90	
	Raytheon	74LS90	
	Signetics	74LS90	
	TI	SN74LS90	
74LS92	Hitachi	HD74LS92	
	Motorola	SN74LS92	
	Raytheon	74LS92	
	Signetics	74LS92	
	TI	SN74LS92	
74LS93	Motorola	SN74LS93	
	Raytheon	74LS93	
	Signetics	74LS93	
	TI	SN74LS93	
74LS95	Motorola	SN74LS95	
	Raytheon	74LS95B	
	Signetics	74LS95B	
	TI	SN74LS95B	
74LS95B	Hitachi	HD74LS95B	
74S00	Hitachi	HD74S00	
	Mitsubishi	M5S000	
	National	DM74S00	
	Signetics	74S00	
	TI	SN74S00	
74S02	National	DM74S02	
	Signetics	74S02	
	TI	SN74S32	
74S03	Hitachi	HD74S03	
	Mitsubishi	M5S003	
	National	DM74S03	
	Signetics	74S03	
	TI	SN74S03	
74S04	Hitachi	HD74S04	
	Mitsubishi	M5S004	
	National	DM74S04	
	Signetics	74S04	
	TI	SN74S04	
74S05	Hitachi	HD74S05	
	Mitsubishi	M5S005	
	National	DM74S05	
	Signetics	74S05	
	TI	SN74S05	
74S08	Signetics	74S08	
	TI	SN74S08	
74S09	Signetics	74S09	
	TI	SN74S09	
74S10	Hitachi	HD74S10	
	Mitsubishi	M5S010	
	National	DM74S10	
	Signetics	74S10	
	TI	SN74S10	
74S11	Hitachi	HD74S11	
	Mitsubishi	M5S011	
	National	DM74S11	
	Signetics	74S11	
	TI	SN74S11	
74S112	Hitachi	HD74S112	
	Mitsubishi	M5S112	
	Motorola	SN74S112	
	National	DM74S112	
	Signetics	74S112	
	TI	SN74S112	
74S113	Hitachi	HD74S113	
	Mitsubishi	M5S113	
	Motorola	SN74S113	
	National	DM74S113	
	Signetics	74S113	
	TI	SN74S113	
74S114	Hitachi	HD74S114	
	Mitsubishi	M5S114	
	National	DM74S114	
	Signetics	74S114	
	TI	SN74S114	
74S132	TI	SN74S132	
74S133	Hitachi	HD74S133	
	Mitsubishi	M5S133	
	National	DM74S133	
	Signetics	74S133	
	TI	SN74S133	
74S134	Hitachi	HD74S134	
	National	DM74S134	
	Signetics	74S134	
	TI	SN74S134	
74S135	Hitachi	HD74S135	
	National	DM74S135	
	Signetics	74S135	
	TI	SN74S135	
74S138	AMD	SN74S138	
	Mitsubishi	M5S138	
	National	DM74S138	
	Signetics	74S138	
	TI	SN74S138	
74S139	AMD	SN74S139	
	National	DM74S139	
	Signetics	74S139	
	TI	SN74S139	
74S140	Hitachi	HD74S140	
	National	DM74S140	
	Signetics	74S140	
	TI	SN74S140	
74S15	Hitachi	HD74S15	
	Mitsubishi	M5S015	
	National	DM74S15	
	Signetics	74S15	
	TI	SN74S15	
74S151	AMD	SN74S151	
	Hitachi	HD74S151	
	Mitsubishi	M5S151	
	National	DM74S151	
	Signetics	74S151	
	TI	SN74S151	
74S153	AMD	SN74S153	
	Mitsubishi	M5S153	
	National	DM74S153	
	Signetics	74S153	
	TI	SN74S153	
74S157	AMD	SN74S157	
	Mitsubishi	M5S157	
	National	DM74S157	
	Signetics	74S157	
	TI	SN74S157	
74S158	AMD	SN74S158	
	Mitsubishi	M5S158	
	National	DM74S158	
	Signetics	74S158	
	TI	SN74S158	
74S174	AMD	SN74S174	
	Hitachi	HD74S174	
	Mitsubishi	M5S174	
	National	DM74S174	
	Signetics	74S174	
	TI	SN74S174	
74S175	AMD	SN74S175	
	Hitachi	HD74S175	
	Mitsubishi	M5S175	
	National	DM74S175	
	Signetics	74S175	
74S175	TI	SN74S175	
74S181	AMD	SN74S181	
	Hitachi	HD74S181	
	Mitsubishi	M5S181	
	Signetics	74S181	
	TI	SN74S181	
74S182	Mitsubishi	M5S182	
	National	DM74S182	
	Signetics	74S182	
	TI	SN74S182	
74S194	AMD	SN74S194	
	Signetics	74S194	
	TI	SN74S194	
74S195	AMD	SN74S195	
	National	DM74S195	
	Signetics	74S195	
	TI	SN74S195	
74S20	Hitachi	HD74S20	
	Mitsubishi	M5S020	
	National	DM74S20	
	Signetics	74S20	
	TI	SN74S20	
74S22	Hitachi	HD74S22	
	Mitsubishi	M5S22	
	National	DM74S22	
	Signetics	74S22	
	TI	SN74S22	
74S251	AMD	SN74S251	
	Hitachi	HD74S251	
	Mitsubishi	M5S251	
	National	DM74S251	
	Signetics	74S251	
	TI	SN74S251	
74S253	AMD	SN74S253	
	National	DM74S253	
	Signetics	74S253	
74S257	AMD	SN74S257	
	Mitsubishi	M5S257	
	National	DM74S257	
	Signetics	74S257	
	TI	SN74S257	
74S258	AMD	SN74S258	
	Mitsubishi	M5S258	
	Signetics	74S258	
	TI	SN74S258	
74S30	Mitsubishi	M5S030	
	National	DM74S30	
	TI	SN74S30	
74S32	Signetics	74S32	
74S40	Hitachi	HD74S40	
	Mitsubishi	M5S040	
	National	DM74S40	
	Signetics	74S40	
	TI	SN74S40	
74S51	Mitsubishi	M5S051	
	National	DM74S51	
	Signetics	74S51	
	TI	SN74S51	
74S64	Hitachi	HD74S64	
	National	DM74S64	
	Signetics	74S64	
	TI	SN74S64	
74S65	Hitachi	HD74S65	
	National	DM74S65	
	Signetics	74S65	
	TI	SN74S65	
74S74	Hitachi	HD74S74	
	Mitsubishi	M5S074	
	TI	SN74S74	
74S86	Hitachi	HD74S86	
	National	DM74S86	
	Signetics	74S86	
	TI	SN74S86	
7400	Hitachi	HD7400	
	Mitsubishi	M53200	
	Motorola	MC7400	
	National	DM7400	
	NEC America	μPB7400	
	Signetics	7400	
	TI	SN7400	
	Toshiba	TC7400	
	TRW	7400	
7401	Hitachi	HD7401	
	Mitsubishi	M53201	
	Motorola	MC7401	
	National	DM7401	
7401	Signetics	7401	
	TI	SN7401	
	TRW	7401	
7402	Hitachi	HD7402	
	Mitsubishi	M53202	
	Motorola	MC7402	
	National	DM7402	
	NEC America	μPB7402	
	Signetics	7402	
	TI	SN7402	
	TRW	7402	
7403	Hitachi	HD7403	
	Mitsubishi	M53203	
	Motorola	MC7403	
	National	DM7403	
	Signetics	7403	
	TI	SN7403	
	TRW	7403	
7404	Hitachi	HD7404	
	Mitsubishi	M53204	
	Motorola	MC7404	
	National	DM7404	
	NEC America	μPB7404	
	Signetics	7404	
	TI	SN7404	
	Toshiba	TC7404	
	TRW	7404	
7405	Hitachi	HD7405	
	Mitsubishi	M53205	
	Motorola	MC7405	
	National	DM7405	
	NEC America	μPB7405	
	Signetics	7405	
	TI	SN7405	
	TRW	7405	
7406	Hitachi	HD7406	
	Mitsubishi	M53206	
	Motorola	MC7406	
	National	DM7406	
	Signetics	7406	
	TI	SN7406	
	TRW	7406	
7407	Hitachi	HD7407	
	Mitsubishi	M53207	
	Motorola	MC7407	
	National	DM7407	
	Signetics	7407	
	TI	SN7407	
	TRW	7407	
7408	Hitachi	HD7408	
	Mitsubishi	M53208	
	Motorola	MC7408	
	National	DM7408	
	Signetics	7408	
	TI	SN7408	
	Toshiba	TC7408	
	TRW	7408	
7409	Hitachi	HD7409	
	Mitsubishi	M53209	
	Motorola	MC7409	
	National	DM7409	
	Signetics	7409	
	TI	SN7409	
	TRW	7409	
7410	Hitachi	HD7410	
	Mitsubishi	M53210	
	Motorola	MC7410	
	National	DM7410	
	NEC America	μPB7410	
	Signetics	7410	
	TI	SN7410	
		SN7427	
	Toshiba	TC7410	
	TRW	7410	
74105	NEC America	μPB74105	
74107	AMD	SN74107	
	Hitachi	HD74107	
	Mitsubishi	M53307	
	Motorola	MC74H107	
		MC74107	
	National	DM74107	
	NEC America	μPB74107	
	Signetics	74107	
	TI	SN74107	
74109	National	DM74109	
	Signetics	74109	

♦ Discontinued

Bold face device numbers indicate manufacturers data is provided in the IC Master on the pages noted.

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Manufacturer Device	Replacement Source	Device	IC Master Page
74109	TI	SN74109	
7411	Hitachi	HD7411	
	National	DM7411	
	Signetics	7411	
74116	Signetics	74116	
	TI	SN74116	
7412	Hitachi	HD7412	
	Signetics	7412	
	TI	SN7412	
	TRW	7412	
74121	Hitachi	HD74121	
	Mitsubishi	M53321	
	Motorola	MC74121	
		MC8603	
	National	DM74121	
	Signetics	74121	
	TI	SN74121	
	TRW	74121	
74122	Mitsubishi	M53322	
	Motorola	MC74122	
	Signetics	74122	
	TI	SN74122	
74123	AMD	SN74123	
	Mitsubishi	M53323	
	Motorola	MC74123	
	National	DM74123	
	NEC America	μPB74123	
	Signetics	74123	
	TI	SN74123	
	TRW	74123	
74125	Hitachi	HD74125	
	Mitsubishi	M53325	
	National	DM74125	
	Signetics	74125	
	TI	SN74125	
74126	Hitachi	HD74126	
	Mitsubishi	M53326	
	National	DM74126	
	Signetics	74126	
	TI	SN74126	
7413	Mitsubishi	M53213	
	Motorola	MC7413	
	National	DM7413	
	NEC America	μPB7413	
	Signetics	7413	
	TI	SN7413	
	TRW	7413	
74132	Hitachi	HD74132	
	Mitsubishi	M53332	
	Motorola	MC74132	
	National	DM74132	
	Signetics	74132	
	TI	SN74132	
74136	Raytheon	74136	
	TI	SN74136	
7414	Hitachi	HD7414	
	Mitsubishi	M53214	
	Motorola	MC7414	
	National	DM7414	
	Signetics	7414	
	TI	SN7414	
74141	Motorola	MC74141	
	National	DM74141	
	NEC America	μPB74141	
	Signetics	74141	
	TI	SN74141	
74145	Mitsubishi	M53345	
	Motorola	MC74145	
		MC83145	
	National	DM74145	
	Raytheon	74145	
	Signetics	74145	
	TI	SN74145	
	TRW	74145	
74150	Hitachi	HD74150	
	Mitsubishi	M53350	
	Motorola	MC74150	
		MC83150	
	National	DM74150	
	NEC America	μPB74150	
	Signetics	74150	
	TI	SN74150	
	TRW	74150	
74151	Hitachi	HD74151	
	Mitsubishi	M53351	
	Motorola	MC74151	
		MC83151	
	National	DM74151	
	NEC America	μPB74151	
	Signetics	74151	
	TI	SN74151	
		SN74151A	
	TRW	74151	
74152	Motorola	MC74152	
		MC83152	
	TI	SN74152	
	TRW	74152	
74153	AMD	SN74153	
	Mitsubishi	M53353	
	Motorola	MC74153	
		MC83153	
	National	DM74153	
	NEC America	μPB74153	
	Signetics	74153	
	TI	SN74153	
	TRW	74153	
74154	AMD	SN74154	
	Mitsubishi	M53354	
	Motorola	MC74154	
		MC8311	
	National	DM74154	
	NEC America	μPB74154	
	Signetics	74154	
	TI	SN74154	
	TRW	74154	
74155	Mitsubishi	M53355	
	Motorola	MC74155	
	National	DM74155	
	NEC America	μPB74155	
	Signetics	74155	
	TI	SN74155	
	TRW	74155	
74156	Hitachi	HD74156	
	Mitsubishi	M53356	
	Motorola	MC74156	
	National	DM74156	
	NEC America	μPB74156	
	Signetics	74156	
	TI	SN74156	
	TRW	74156	
74157	AMD	SN74157	
	Hitachi	HD74157	
	Mitsubishi	M53357	
	Motorola	MC74157	
		MC8322	
	National	DM74157	
	NEC America	μPB74157	
	Signetics	74157	
	TI	SN74157	
74159	TI	SN74159	
7416	Hitachi	HD7416	
	Mitsubishi	M53216	
	Motorola	MC7416	
	National	DM7416	
	Signetics	7416	
	TI	SN7416	
	TRW	7416	
74160	AMD	SN74160	
	Hitachi	HD74160	
	Mitsubishi	M53360	
	Motorola	MC74160	
		MC8310	
		MC8316	
	National	DM74160	
	Raytheon	74160	
	Signetics	74160	
	TI	SN74160	
	TRW	74160	
74161	AMD	SN74161	
	Hitachi	HD74161	
	Mitsubishi	M53361	
	Motorola	MC74161	
	National	DM74161	
	NEC America	μPB74161	
	Signetics	74161	
	TI	SN74161	
	TRW	74161	
74162	AMD	SN74162	
	Hitachi	HD74162	
74162	Mitsubishi	M53362	
	Motorola	MC74162	
	National	DM74162	
	Signetics	74162	
	TI	SN74162	
	TRW	74162	
74163	AMD	SN74163	
	Hitachi	HD74163	
	Mitsubishi	M53363	
	Motorola	MC74163	
	National	DM74163	
	Signetics	74163	
	TI	SN74163	
	TRW	74163	
74164	AMD	SN74164	
		74164	
	Hitachi	HD74164	
	Mitsubishi	M53364	
	Motorola	MC83164	
	National	DM74164	
	NEC America	μPB74164	
	Raytheon	74164	
	Signetics	74164	
	TI	SN74164	
74165	Mitsubishi	M53365	
	Motorola	MC74165	
		MC83165	
	National	DM74165	
	Signetics	74165	
	TI	SN74165	
74166	Hitachi	HD74166	
	Mitsubishi	M53366	
	National	DM74166	
	Signetics	74166	
	TI	SN74166	
7417	Hitachi	HD7417	
	Mitsubishi	M53217	
	Motorola	MC7417	
	National	DM7417	
	Signetics	7417	
	TI	SN7417	
	TRW	7417	
74170	Mitsubishi	M53370	
	National	DM74170	
	NEC America	μPB74170	
	Signetics	74170	
	TI	SN74170	
74173	National	DM74173	
	TI	SN74173	
74174	AMD	SN74174	
	Hitachi	HD74174	
	Mitsubishi	M53374	
	Motorola	MC74174	
	National	DM74174	
	Signetics	74174	
	TI	SN74174	
74175	AMD	SN74175	
	Hitachi	HD74175	
	Mitsubishi	M53375	
	Motorola	MC74175	
	National	DM74175	
	NEC America	μPB74175	
	Signetics	74175	
	TI	SN74175	
74176	Mitsubishi	M53376	
	Motorola	MC74176	
		MC83176	
	National	DM74176	
	Signetics	74176	
	TI	SN74176	
74177	Mitsubishi	M53377	
	Motorola	MC74177	
		MC83177	
	National	DM74177	
	Signetics	74177	
	TI	SN74177	
74178	Motorola	MC83178	
	TI	SN74178	
74179	Motorola	MC83179	
	TI	SN74179	
74180	Hitachi	HD74180	
	Mitsubishi	M53380	
	Motorola	MC74180	
		MC83180	
	National	DM74180	
	NEC America	μPB74180	
74180	Signetics	74180	
	TI	SN74180	
	TRW	74180	
74181	AMD	SN74181	
	Mitsubishi	M53381	
	Motorola	MC74181	
		MC8341	
	National	DM74181	
	NEC America	μPB74181	
	Signetics	74181	
	TI	SN74181	
74182	AMD	SN74182	
	Mitsubishi	M53382	
	Motorola	MC74182	
		MC8342	
	National	DM74182	
	NEC America	μPB74182	
	Signetics	74182	
	TI	SN74182	
74190	Hitachi	HD74190	
	Mitsubishi	M53390	
	Motorola	MC74190	
	National	DM74190	
	Signetics	74190	
	TI	SN74190	
74191	Hitachi	HD74191	
	Mitsubishi	M53391	
	Motorola	MC74191	
	National	DM74191	
	Signetics	74191	
	TI	SN74191	
74192	AMD	SN74192	
	Mitsubishi	M53392	
	Motorola	MC74192	
		MC8360	
	National	DM74192	
	NEC America	μPB74192	
	Signetics	74192	
	TI	SN74192	
74193	AMD	SN74193	
	Mitsubishi	M53393	
	Motorola	MC74193	
		MC8366	
	National	DM74193	
	NEC America	μPB74193	
	Signetics	74193	
	TI	SN74193	
74194	AMD	SN74194	
	Hitachi	HD74194	
	Motorola	MC74194	
	National	DM74194	
	Signetics	74194	
	TI	SN74194	
74195	AMD	SN74195	
	Motorola	MC74195	
	National	DM74195	
	NEC America	μPB74195	
	Signetics	74195	
		7447	
	TI	SN74195	
		SN7447A	
74196	Motorola	MC74196	
	National	DM74196	
	Signetics	74196	
	TI	SN74196	
74197	Motorola	MC74197	
	National	DM74197	
	Signetics	74197	
	TI	SN74197	
74198	Hitachi	HD74198	
	Mitsubishi	M53398	
	National	DM74198	
	NEC America	μPB74198	
	Signetics	74198	
	TI	SN74198	
74199	Mitsubishi	M53399	
	National	DM74199	
	Signetics	74199	
	TI	SN74199	
7420	Hitachi	HD7420	
	Mitsubishi	M53220	
	Motorola	MC7420	
	National	DM7420	
	NEC America	μPB7420	
	Signetics	7420	
	TI	SN7420	

♦ Discontinued

The manufacturers report their devices can be used as direct replacements.
Performance details often differ, so compare the specifications considering your requirements.

Fairchild (cont'd)

Manufacturer Device	Replacement Source	Device	IC Master Page
7420	Toshiba	TC7420	
	TRW	7420	
7421	Signetics	7421	
7422	Hitachi	HD7422	
	TI	SN7422	
7423	Motorola	MC7423	
	National	DM7423	
	TI	SN7423	
7425	Mitsubishi	M53225	
	Motorola	MC7425	
	National	DM7425	
	TI	SN7425	
7426	Hitachi	HD7426	
	Motorola	MC7426	
	National	DM7426	
	Signetics	7426	
	TI	SN7426	
	TRW	7426♦	
7427	Hitachi	HD7427	
	Mitsubishi	M53227	
	Motorola	MC7427	
	National	DM7427	
	Signetics	7427	
	TI	SN7427	
74279	Signetics	74279	
	TI	SN74279	
74283	Mitsubishi	M53483	
	NEC America	μPB74283	
	TI	SN74283	
74290	Mitsubishi	M53490	
	Motorola	MC74290	
	TI	SN74290	
	TRW	74290	
74293	Mitsubishi	M53493	
	Motorola	MC74293	
	TI	SN74293	
	TRW	74293	
74298	Motorola	MC74298	
	Signetics	74298	
	TI	SN74298	
7430	Hitachi	HD7430	
	Mitsubishi	M53230	
	Motorola	MC7430	
	National	DM7430	
	NEC America	μPB7430	
	Signetics	7430	
	TI	SN7430	
	TRW	7430	
7432	Hitachi	HD7432	
	National	DM7432	
	Signetics	7432	
	TI	SN7432	
7437	Mitsubishi	M53237	
	Motorola	MC7437	
	National	DM7437	
	NEC America	μPB7437	
	Signetics	7437	
	TI	SN7437	
	TRW	7437	
7438	Mitsubishi	M53238	
	Motorola	MC7438	
	National	DM7438	
	NEC America	μPB7438	
	Signetics	7438	
	TI	SN7438	
	TRW	7438	
7439	Signetics	7439	
7440	Hitachi	HD7440	
	Mitsubishi	M53240	
	Motorola	MC7440	
	National	DM7440	
	NEC America	μPB7440	
	Signetics	7440	
	TI	SN7440	
	TRW	7440	
7441	Mitsubishi	M53241	
	Motorola	MC8315	
	National	DM7441	
	Signetics	7441	
	TI	SN74141	
7442	Hitachi	HD7442	
	Mitsubishi	M53242	
	Motorola	MC7442	
	Motorola	MC8352	
	National	DM7442	
	NEC America	μPB7442	
	Signetics	7442	
	TI	SN7442	
		SN7442A	
7443	Hitachi	HD7443	
	Mitsubishi	M53243	
	Motorola	MC7443	
		MC8353	
	Signetics	7443	
	TI	SN7443	
		SN7443A	
7444	Hitachi	HD7444	
	Mitsubishi	M53244	
	Motorola	MC7444	
		MC8354	
	Signetics	7444	
	TI	SN7444A	
7445	Mitsubishi	M53245	
	Motorola	MC7445	
		MC8345	
	National	DM7445	
	NEC America	μPB7445	
	Signetics	7445	
	TI	SN7445	
	TRW	7445	
7446	Motorola	MC7446	
		MC8357	
	National	DM7446	
	Signetics	7446	
	TI	SN7446A	
7447	Mitsubishi	M53247	
	Motorola	MC7447	
		MC8357	
	National	DM7447	
	NEC America	μPB7447	
	Signetics	7447	
	TI	SN7447	
7448	Mitsubishi	M53248	
	Motorola	MC7448	
		MC8358	
	National	DM7448	
	Signetics	7448	
	TI	SN7448	
7449	Motorola	MC7449	
		MC8359	
	TI	SN7449	
7450	Hitachi	HD7450	
	Mitsubishi	M53250	
	Motorola	MC7450	
	National	DM7450	
	NEC America	μPB7450	
	Signetics	7450	
	TI	SN7450	
	TRW	7450	
7451	Hitachi	HD7451	
	Motorola	MC7451	
	National	DM7451	
	NEC America	μPB7451	
	Signetics	7451	
	TI	SN7451	
	TRW	7451	
7453	Hitachi	HD7453	
	Mitsubishi	M53253	
	Motorola	MC7453	
	National	DM7453	
	NEC America	μPB7453	
	Signetics	7453	
	TI	SN7453	
	TRW	7453	
7454	Hitachi	HD7454	
	Motorola	MC7454	
	National	DM7454	
	NEC America	μPB7454	
	Signetics	7454	
	TI	SN7454	
	TRW	7454	
7460	Hitachi	HD7460	
	Mitsubishi	M53260	
	Motorola	MC7460	
	National	DM7460	
	NEC America	μPB7460	
	Signetics	7460	
	TI	SN7460	
	TRW	7460	
7470	Hitachi	HD7470	
	Mitsubishi	M53270	
	Motorola	MC7470	
	National	DM7470	
	Signetics	7470	
	TI	SN7470	
7472	Hitachi	HD7472	
	Mitsubishi	M53272	
	Motorola	MC7472	
	National	DM7472	
	Signetics	7472	
	TI	SN7472	
	TRW	7472	
7473	Hitachi	HD7473	
	Mitsubishi	M53273	
	Motorola	MC7473	
	National	DM7473	
	NEC America	μPB7473	
	Signetics	7473	
	TI	SN7473	
7474	Hitachi	HD7474	
	Mitsubishi	M53274	
	Motorola	MC7474	
	National	DM7474	
	NEC America	μPB7474	
	Signetics	7474	
	TI	SN7474	
	TRW	7474	
7475	Hitachi	HD7475	
	Mitsubishi	M53275	
	Motorola	MC7475	
		MC8375	
	National	DM7475	
	Signetics	7475	
	TI	SN7475	
	TRW	7475	
7476	Hitachi	HD7476	
	Mitsubishi	M53276	
	Motorola	MC7476	
	National	DM7476	
	NEC America	μPB7476	
	Signetics	7476	
	TI	SN7476	
	TRW	7476	
7477	Motorola	MC7477	
		MC8377	
	Signetics	7477	
7480	Mitsubishi	M53280	
	Motorola	MC7480	
	NEC America	μPB7480	
	Signetics	7480	
	TI	SN7480	
7481	Motorola	MC4004	
	TI	SN7481A	
7482	Hitachi	HD7482	
	Motorola	MC7482	
		MC8382	
	TI	SN7482	
7483	Mitsubishi	M53283	
	Motorola	MC7483	
		MC8383	
	National	DM7483	
	Signetics	7483	
	TI	SN7483	
		SN7483A	
7485	Hitachi	HD7485	
	Mitsubishi	M53285	
	Motorola	MC7485	
	National	DM7485	
	NEC America	μPB7485	
	Signetics	7485	
	TI	SN7485	
	TRW	7485	
7486	Hitachi	HD7486	
	Mitsubishi	M53286	
	Motorola	MC7486	
	National	DM7486	
	NEC America	μPB7486	
	Signetics	7486	
	TI	SN7486	
	TRW	7486	
7488	Motorola	MC4002	
	TI	SN7488A	
7489	AMD	SN7489	
	Mitsubishi	M53289	
	Motorola	MC4064	
	National	DM7489	
	TI	SN7489	
	TRW	7489	
7490	Hitachi	HD7490	
	Mitsubishi	M53290	
	Motorola	MC7490	
		MC8390	
	National	DM7490	
	Signetics	7490	
	TI	SN7490A	
	TRW	7490	
7491	Hitachi	HD7491	
	Mitsubishi	M53291	
	Motorola	MC7491	
		MC8391	
	National	DM7491	
	NEC America	μPB7491	
	Signetics	7491	
	TI	SN7491A	
7492	Hitachi	HD7492	
	Mitsubishi	M53292	
	Motorola	MC7492	
		MC8392	
	National	DM7492	
	Signetics	7492	
	TI	SN7492	
		SN7492A	
	TRW	7492	
7493	Hitachi	HD7493	
	Mitsubishi	M53293	
	Motorola	MC7493	
		MC8393	
	National	DM7493	
	Signetics	7493	
	TI	SN7493A	
	TRW	7493	
7494	Motorola	MC7494	
		MC8394	
	Signetics	7494	
	TI	SN7494	
7495	Hitachi	HD7495	
	Mitsubishi	M53295	
	Motorola	MC7495	
		MC8395	
	National	DM7495	
	Signetics	7495	
	TI	SN7495	
		SN7495A	
7496	Hitachi	HD7496	
	Mitsubishi	M53296	
	Motorola	MC7496	
		MC8396	
	National	DM7496	
	Signetics	7496	
	TI	SN7496	
	TRW	7496	
7497	Motorola	MC7497	
	TI	SN7497	
75107	AMD	SN75107	
	Motorola	MC75107	
	National	DS75107	
	Raytheon	RC75107	
	TI	SN75107	
75108	AMD	SN75108	
	Motorola	MC75108	
	National	DS75108	
	Raytheon	RC75108	
	TI	SN75108	
75109	AMD	SN75109	
	Raytheon	RC75109	
	TI	SN75109	
75110	AMD	SN75110	
	Motorola	MC75110	
	Raytheon	RC75110	
	TI	SN75110	
75112	TI	SN75112	
75121	Motorola	MC8T13	
	TI	SN75121	
75122	Motorola	MC8T14	
	TI	SN75122	
75123	Motorola	MC8T23	
	TI	SN75123	
75124	Motorola	MC8T24	
	TI	SN75124	
75150	TI	SN75150	
75154	TI	SN75154	

♦ Discontinued

Bold face device numbers indicate manufacturers data is provided in the IC Master on the pages noted.

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Manufacturer Device	Replacement Source	Device	IC Master Page
7520	Silicon G	SG7520	
75207	TI	SN75207	
75208	AMD	SN75208	
	TI	SN75208	
7521	Silicon G	SG7521	
75234	AMD	SN75234	
	TI	SN75234	
75238	AMD	SN75238	
	TI	SN75238	
7524	Motorola	MC7524	
	National	DS7524	
	Signetics	7524	
	Silicon G	SG7524	
	TI	SN7524	
7525	Silicon G	SG7525	
7528	Motorola	MC7528	
	Silicon G	SG7528	
	TI	SN7528	
7529	Silicon G	SG7529	
75325	AMD	SN75325	
	Motorola	MC75325	
	National	DS75325	
	Signetics	75325	
	Silicon G	SG75325	
	TI	SN75325	
75326	TI	SN75326	
75327	TI	SN75327	
7535	Silicon G	SG7535	
7538	Silicon G	SG7538	
7539	Silicon G	SG7539	
75430	TI	SN75430	
75450	Motorola	MC75450	
	National	DS75450	
	Signetics	75450	
	Silicon G	SG75450	
	TI	SN75450	
75451	Motorola	MC75451	
	National	DS75451	
	Signetics	75451	
	Silicon G	SG75451	
	TI	SN75451	
75452	Motorola	MC75452	
	National	DS75452	
	Signetics	75452	
	Silicon G	SG75452	
	TI	SN75452	
75453	Motorola	MC75453	
	National	DS75453	
	Signetics	75453	
	Silicon G	SG75453	
	TI	SN75453	
75454	Motorola	MC75454	
	National	DS75454	
	Signetics	75454	
	Silicon G	SG75454	
	TI	SN75454	
75460	National	DS75460	
	Silicon G	SG75460	
	TI	SN75460	
75461	Motorola	MC75461	
	National	DS75461	
	Silicon G	SG75461	
	TI	SN75461	
75462	Motorola	MC75462	
	National	DS75462	
	Silicon G	SG75462	
	TI	SN75462	
75463	Motorola	MC75463	
	National	DS75463	
	Silicon G	SG75463	
	TI	SN75463	
75464	Motorola	MC75464	
	National	DS75464	
	Silicon G	SG75464	
	TI	SN75464	
75470	Silicon G	SG75470	
	TI	SN75470	
75471	Silicon G	SG75471	
	TI	SN75471	
75472	Silicon G	SG75472	
	TI	SN75472	
75473	Silicon G	SG75473	
	TI	SN75473	
75474	Silicon G	SG75474	
	TI	SN75474	
75491	Motorola	MC75491	
	National	DS75491	
	TI	SN75491	
75492	Motorola	MC75492	
	National	DS75492	
	TI	SN75492	
8T13	Motorola	MC8T13	
	National	DS55121	
	TI	SN55121	
8T14	Motorola	MC8T14	
	National	DS55122	
	TI	SN55122	
8T23	Motorola	MC8T23	
	National	DS75123	
	TI	SN75123	
8T24	Motorola	MC8T24	
	National	DS75124	
	TI	SN75124	
♦9H00	Motorola	MC54H00	
		MC74H00	
	National	DM54H00	
		DM74H00	
	Signetics	54H00	
		74H00	
	TI	SN54H00	
		SN74H00	
♦9H01	Motorola	MC54H01	
		MC74H01	
	National	DM54H01	
	TI	SN54H01	
		SN74H01	
♦9H04	Motorola	MC54H04	
		MC74H04	
	National	DM54H04	
		DM74H04	
	Signetics	54H04	
		74H04	
	TI	SN54H04	
		SN74H04	
♦9H05	Motorola	MC54H05	
		MC74H05	
	National	DM54H05	
		DM74H05	
	Signetics	54H05	
		74H05	
	TI	SN54H05	
		SN74H05	
♦9H08	Motorola	MC54H08	
		MC74H08	
	National	DM54H08	
		DM74H08	
	Signetics	54H08	
		74H08	
♦9H10	Motorola	MC54H10	
		MC74H10	
	National	DM54H10	
		DM74H10	
	Signetics	54H10	
		74H10	
	TI	SN54H10	
		SN74H10	
♦9H101	Motorola	MC54H101	
		MC74H101	
	Signetics	54H101	
		74H101	
	TI	SN54H101	
		SN74H101	
♦9H102	Motorola	MC74H102	
	Signetics	54H102	
		74H102	
	TI	SN54H102	
		SN74H102	
♦9H103	National	DM54H103	
		DM74H103	
	TI	SN54H103	
		SN74H103	
♦9H106	National	DM54H106	
		DM74H106	
	Signetics	54H106	
		74H106	
	TI	SN54H106	
		SN54H107	
		SN74H106	
		SN74H107	
♦9H108	Motorola	MC54H108	
		MC74H108	
	National	DM54H108	
		DM74H108	
	Signetics	54H108	
		74H108	
	TI	SN54H108	
		SN74H108	
♦9H11	Motorola	MC54H11	
		MC74H11	
	National	DM54H11	
		DM74H11	
	Signetics	54H11	
		74H11	
	TI	SN54H11	
		SN74H11	
♦9H20	Motorola	MC54H20	
		MC74H20	
	National	DM54H20	
		DM74H20	
	Signetics	54H20	
		74H20	
	TI	SN54H20	
		SN74H20	
♦9H21	Motorola	MC54H21	
		MC74H21	
	National	DM54H21	
		DM74H21	
	TI	SN54H21	
		SN74H21	
♦9H22	Motorola	MC54H22	
		MC74H22	
	National	DM54H22	
		DM74H22	
	Signetics	54H22	
		74H22	
	TI	SN54H22	
		SN74H22	
♦9H30	Motorola	MC54H30	
		MC74H30	
	National	DM54H30	
		DM74H30	
	Signetics	54H30	
		74H30	
	TI	SN54H30	
		SN74H30	
♦9H40	Motorola	MC54H40	
		MC74H40	
	National	DM54H40	
		DM74H40	
	Signetics	54H40	
		74H40	
	TI	SN54H40	
		SN74H40	
♦9H50	Motorola	MC74H50	
	National	DM54H50	
		DM74H50	
	Signetics	54H50	
		74H50	
	TI	SN54H50	
		SN74H50	
♦9H51	Motorola	MC54H51	
		MC74H51	
	National	DM54H51	
		DM74H51	
	Signetics	54H51	
		74H51	
	TI	SN54H51	
		SN74H51	
♦9H52	Motorola	MC54H52	
		MC74H52	
	National	DM54H52	
		DM74H52	
	TI	SN54H52	
		SN74H52	
♦9H53	Motorola	MC54H53	
		MC74H53	
	National	DM54H53	
		DM74H53	
	TI	SN54H53	
		SN74H53	
♦9H54	Motorola	MC54H54	
		MC74H54	
	National	DM54H54	
		DM74H54	
	TI	SN54H54	
♦9H54	TI	SN74H54	
♦9H55	Motorola	MC54H55	
		MC74H55	
	National	DM54H55	
		DM74H55	
	TI	SN54H55	
♦9H60	Motorola	MC54H60	
		MC74H60	
	National	DM54H60	
		DM74H60	
	TI	SN54H60	
		SN74H60	
♦9H61	Motorola	MC54H61	
		MC74H61	
	National	DM54H61	
		DM74H61	
	Signetics	54H61	
		74H61	
	TI	SN54H61	
		SN74H61	
♦9H62	Motorola	MC54H62	
		MC74H62	
	National	DM54H62	
		DM74H62	
	Signetics	54H62	
		74H62	
	TI	SN54H62	
		SN74H62	
♦9H71	Motorola	MC54H71	
		MC74H71	
	National	DM54H71	
		DM74H71	
	Signetics	54H71	
		74H71	
	TI	SN54H71	
		SN74H71	
♦9H72	Motorola	MC54H72	
	National	DM54H72	
		DM74H72	
	Signetics	54H72	
		74H72	
	TI	SN54H72	
		SN74H72	
♦9H73	Motorola	MC54H73	
	National	DM54H73	
		DM74H73	
	Signetics	54H73	
		74H73	
	TI	SN54H73	
		SN74H73	
♦9H74	Motorola	MC54H74	
		MC74H74	
	National	DM54H74	
		DM74H74	
	Signetics	54H74	
		74H74	
	TI	SN54H74	
		SN74H74	
♦9H76	National	DM54H76	
		DM74H76	
	Signetics	54H76	
		74H76	
	TI	SN54H76	
		SN74H76	
♦9H78	National	DM54H78	
		DM74H78	
	TI	SN54H78	
		SN74H78	
9LS00	National	DM54LS00	
		DM74LS00	
	Raytheon	9LS00	
9LS02	National	DM54LS02	
		DM74LS02	
	Raytheon	9LS02	
9LS03	National	DM54LS03	
		DM74LS03	
	Raytheon	9LS03	
9LS04	National	DM54LS04	
		DM74LS04	
	Raytheon	9LS04	
9LS05	National	DM54LS05	
		DM74LS05	
	Raytheon	9LS05	
9LS08	National	DM54LS08	
		DM74LS08	
	Raytheon	9LS08	

♦ Discontinued

The manufacturers report their devices can be used as direct replacements.
Performance details often differ, so compare the specifications considering your requirements.

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Manufacturer Device	Replacement Source	Replacement Device	IC Master Page
9LS09	National	DM54LS09	
		DM74LS09	
	Raytheon	9LS09	
9LS10	National	DM54LS10	
		DM74LS10	
	Raytheon	9LS10	
9LS109	National	DM54LS109	
		DM74LS109	
	Raytheon	9LS109	
9LS11	National	DM54LS11	
		DM74LS11	
	Raytheon	9LS11	
9LS112	National	DM54LS112	
		DM74LS112	
	Raytheon	9LS112	
9LS113	National	DM54LS113	
		DM74LS113	
	Raytheon	9LS113	
9LS114	National	DM54LS114	
		DM74LS114	
	Raytheon	9LS114	
9LS125	National	DM54LS125	
		DM74LS125	
9LS126	National	DM54LS126	
		DM74LS126	
9LS132	National	DM54LS132	
		DM74LS132	
	Raytheon	9LS132	
9LS133	National	DM74S133	
9LS136	National	DM54LS136	
		DM74LS136	
	Raytheon	9LS136	
9LS138	National	DM54LS138	
		DM74LS138	
	Raytheon	9LS138	
9LS139	National	DM54LS139	
		DM74LS139	
	Raytheon	9LS139	
9LS14	National	DM54LS14	
		DM74LS14	
	Raytheon	9LS14	
9LS15	National	DM54LS15	
		DM74LS15	
	Raytheon	9LS15	
9LS151	National	DM54LS151	
		DM74LS151	
	Raytheon	9LS151	
9LS152	Raytheon	9LS152	
9LS153	National	DM54LS153	
		DM74LS153	
	Raytheon	9LS153	
9LS155	National	DM54LS155	
		DM74LS155	
	Raytheon	9LS155	
9LS156	National	DM54LS156	
		DM74LS156	
	Raytheon	9LS156	
9LS157	National	DM54LS157	
		DM74LS157	
	Raytheon	9LS157	
9LS158	National	DM54LS158	
		DM74LS158	
	Raytheon	9LS158	
9LS160	National	DM54LS160	
		DM74LS160	
	Raytheon	9LS160	
9LS161	National	DM54LS161	
		DM74LS161	
	Raytheon	9LS161	
9LS162	National	DM54LS162	
		DM74LS162	
	Raytheon	9LS162	
9LS163	National	DM54LS163	
		DM74LS163	
	Raytheon	9LS163	
9LS164	National	DM54LS164	
		DM74LS164	
9LS170	National	DM54LS170	
		DM74LS170	
	Raytheon	9LS170	
9LS173	Raytheon	9LS173	
9LS174	National	DM54LS174	
		DM74LS174	
9LS174	Raytheon	9LS174	
9LS175	National	DM54LS175	
		DM74LS175	
	Raytheon	9LS175	
9LS181	National	DM54181	
		DM74181	
	Raytheon	9LS181	
9LS190	National	DM54LS190	
		DM74LS190	
	Raytheon	9LS190	
9LS191	National	DM54LS191	
		DM74LS191	
	Raytheon	9LS191	
9LS192	National	DM54LS192	
		DM74LS192	
	Raytheon	9LS192	
9LS193	National	DM54LS193	
		DM74LS193	
	Raytheon	9LS193	
9LS194	Raytheon	9LS194A	
9LS195	Raytheon	9LS195A	
9LS196	National	DM54LS196	
		DM74LS196	
	Raytheon	9LS196	
9LS197	National	DM54LS197	
		DM74LS197	
	Raytheon	9LS197	
9LS20	National	DM54LS20	
		DM74LS20	
	Raytheon	9LS20	
9LS21	National	DM54LS21	
		DM74LS21	
	Raytheon	9LS21	
9LS22	National	DM54LS22	
		DM74LS22	
	Raytheon	9LS22	
9LS251	Raytheon	9LS251	
9LS253	National	DM54LS253	
		DM74LS253	
	Raytheon	9LS253	
9LS257	National	DM54LS257	
		DM74LS257	
	Raytheon	9LS257	
9LS258	National	DM54LS258	
		DM74LS258	
	Raytheon	9LS258	
9LS259	National	DM8334	
		DM9334	
9LS266	National	DM54LS266	
		DM74LS266	
	Raytheon	9LS266	
9LS27	National	DM54LS27	
		DM74LS27	
	Raytheon	9LS27	
9LS279	National	DM54LS279	
		DM74LS279	
	Raytheon	9LS279	
9LS283	National	DM54LS283	
		DM74LS283	
	Raytheon	9LS283	
9LS295	Raytheon	9LS295A	
9LS298	AMD	9LS298	
	Raytheon	9LS298	
9LS30	National	DM54LS30	
		DM74LS30	
	Raytheon	9LS30	
9LS32	National	DM54LS32	
		DM74LS32	
	Raytheon	9LS32	
9LS365	National	DM54LS365	
		DM74LS365	
9LS366	National	DM54LS366	
		DM74LS366	
9LS367	National	DM54LS367	
		DM74LS367	
9LS368	National	DM54LS368	
		DM74LS368	
9LS37	National	DM54LS37	
		DM74LS37	
	Raytheon	9LS37	
9LS38	National	DM54LS38	
		DM74LS38	
	Raytheon	9LS38	
9LS40	National	DM54LS40	
		DM74LS40	
	Raytheon	9LS40	
9LS42	National	DM54LS42	
		DM74LS42	
	Raytheon	9LS42	
9LS51	National	DM54LS51	
		DM74LS51	
	Raytheon	9LS51	
9LS54	National	DM54LS54	
		DM74LS54	
	Raytheon	9LS54	
9LS55	National	DM54LS55	
		DM74LS55	
	Raytheon	9LS55	
9LS670	National	DM54LS670	
		DM74LS670	
	Raytheon	9LS670	
9LS73	National	DM54LS73	
		DM74LS73	
9LS74	National	DM54LS74	
		DM74LS74	
	Raytheon	9LS74	
9LS83	National	DM54LS83	
		DM74LS83	
	Raytheon	9LS83A	
9LS86	National	DM54LS86	
		DM74LS86	
	Raytheon	9LS86	
9LS90	Raytheon	9LS90	
9LS93	Raytheon	9LS93	
9LS95	Raytheon	9LS95B	
9L00	National	DM54L00	
		DM74L00	
	TI	SN54LS00	
		SN74LS00	
9L04	National	DM54L04	
		DM74L04	
	TI	SN54LS04	
		SN74LS04	
9L24	National	DM8024	
		DM9024	
	TI	SN54LS109	
		SN74LS109	
9L54	National	DM54L54	
		DM74L54	
	TI	SN54LS54	
		SN74LS54	
9L86	National	DM5486	
		DM7486	
	TI	SN54LS86	
		SN74LS86	
♦9NXX	Fairchild	54XX	
		74XX	
♦9SXX	Fairchild	54SXX	
		74SXX	
♦9S04	National	DM74S04	
	Signetics	74S04	
	TI	SN54S04	
		SN74S04	
♦9S05	National	DM74S05	
	Signetics	74S05	
	TI	SN54S05	
		SN74S05	
9000	TI	SN29000	
9001	Motorola	MC3052	
		MC9001	
	TI	SN29001	
9002	Motorola	MC7400	
	National	DM9002C	
	TI	SN29002	
		SN5400	
		SN7400	
9003	Motorola	MC7410	
	National	DM9003C	
	TI	SN29003	
		SN5410	
		SN7410	
9004	Motorola	MC7420	
	National	DM9004C	
	TI	SN29004	
		SN5420	
		SN7420	
9005	Motorola	MC7450	
	National	DM9005C	
	TI	SN29005	
		SN5450	
		SN7450	
9006	Motorola	MC7460	
9006	National	DM9006C	
	TI	SN5460	
		SN7460	
9007	TI	SN29007	
9008	National	DM9008C	
	TI	SN29008	
9009	Motorola	MC7440	
	National	DM9009C	
	TI	SN29009	
		SN5440	
9012	National	DM9012C	
	TI	SN29012	
		SN5403	
		SN7403	
9016	Motorola	MC7404	
	National	DM9016C	
	TI	SN29016	
		SN5404	
		SN7404	
9017	TI	SN5405	
		SN7405	
9024	National	DM74109	
		DM8024	
		DM9024	
	Signetics	74109	
	TI	SN29024	
		SN54109	
		SN74109	
9031	Signetics	N8252	
9034	Motorola	MCM4002	
	Signetics	8224	
	TI	SN5488A	
		SN7488A	
9093	Hitachi	HD2211	
	National	DM9093	
	Raytheon	RM993	
	TI	SN158093	
		SN159093	
9094	National	DM9094	
	Raytheon	RM994	
	TI	SN158094	
		SN159094	
9097	National	DM9097	
	Raytheon	RM997	
	TI	SN158097	
		SN159097	
9099	Hitachi	HD2210	
	National	DM9099	
	Raytheon	RM999	
	TI	SN158099	
		SN159099	
9135	National	DM935	
9157	National	DM957	
9158	National	DM958	
93H00	TI	SN54S195	
		SN74S195	
93L00	AMD	93L00	
	National	DM74L00	
	TI	SN54LS195	
		SN74LS195	
93L01	AMD	93L01	
	National	DM8301	
		DM9301	
93L08	AMD	93L08	
93L09	National	DM8309	
		DM9309	
93L10	AMD	93L10	
	National	DM76L75	
		DM86L75	
93L11	AMD	93L11	
	National	DM54L154A	
		DM74L154A	
93L12	AMD	93L12	
	National	DM8312	
		DM9312	
93L14	AMD	93L14	
93L16	AMD	93L16	
	National	DM76L76	
		DM86L76	
93L18	AMD	93L18	
	National	DM8318	
		DM9318	
93L21	AMD	93L21	
	TI	SN54LS139	
		SN74LS139	
93L22	AMD	93L22	

♦ Discontinued

Bold face device numbers indicate manufacturers data is provided in the IC Master on the pages noted.

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Manufacturer Device	Replacement Source	Device	IC Master Page
93L22	National	DM54L157A	
		DM74L157A	
93L24	AMD	93L24	
93L28	AMD	93L28	
93L34	AMD	93L34	
	National	DM8334	
		DM9334	
93L38	AMD	93L38	
♦93L40	AMD	93L40	
93L41	AMD	93L41	
	National	DM54181	
		DM74181	
♦93L60	AMD	93L60	
♦93L66	AMD	93L66	
93S00	National	DM74S195	
	TI	SN54S195	
		SN74S195	
93S10	AMD	93S10	
	National	DM54LS160	
		DM74LS160	
93S12	AMD	93S12	
	National	DM8312	
		DM9312	
♦93S138	National	DM74S138	
	TI	SN54S138	
		SN74S138	
♦93S139	National	DM74S139	
	TI	SN54S139	
		SN74S139	
♦93S151	National	DM74S151	
	TI	SN54S151	
		SN74S151	
♦93S153	National	DM74S153	
	TI	SN54S153	
		SN74S153	
♦93S157	National	DM74S157	
	TI	SN54S157	
		SN74S157	
♦93S158	National	DM74S158	
	TI	SN54S158	
		SN74S158	
93S16	AMD	93S16	
	National	DM54LS161	
		DM74LS161	
♦93S174	National	DM74S174	
	TI	SN54S174	
		SN74S174	
♦93S175	National	DM74S175	
	TI	SN54S175	
		SN74S175	
♦93S194	National	DM74S194	
	TI	SN54S194	
		SN74S194	
♦93S21	AMD	93S21	
	National	DM74S139	
93S22	AMD	93S22	
	National	DM74S157	
		DM74S22	
	TI	SN54S157	
		SN74S157	
♦93S251	National	DM74S251	
	TI	SN54S251	
		SN74S251	
93S253	National	DM74S253	
93S257	National	DM74S257	
	TI	SN54S257	
		SN74S257	
♦93S258	National	DM74S258	
	TI	SN54S258	
		SN74S258	
93S41	National	DM54181	
		DM74181	
	TI	SN54S181	
		SN74S181	
93S42	National	DM74S182	
	TI	SN54S182	
		SN74S182	
93S46	National	DM7160	
		DM8160	
93S47	National	DM7160	
		DM74S47	
		DM8160	
♦93S48	AMD	93S48	
930	National	DM930	
9300	AMD	9300	
	Motorola	MC9300	
	National	DM8300	
		DM9300	
	Raytheon	RC9300	
		RM9300	
	TI	SN54195	
		SN74195	
9301	AMD	9301	
	Motorola	MC9301	
	National	DM8301	
		DM9301	
	TI	SN29301	
		SN39301	
9304	AMD	9304	
	Mitsubishi	M54304	
	Motorola	MC9304	
	Raytheon	RC9304	
		RM9304	
♦9306	AMD	9306	
	Motorola	MC9306	
9307	Motorola	MC9307	
	National	DM5448	
		DM7448	
	TI	SN5448A	
		SN7448A	
9308	AMD	9308	
	Motorola	MC9308	
	Raytheon	RC9308	
		RM9308	
	TI	SN29308	
		SN39308	
		SN54116	
		SN74116	
9309	AMD	9309	
	Motorola	MC9309	
	National	DM8309	
		DM9309	
	TI	SN29309	
		SN39309	
9310	AMD	9310	
	Motorola	MC8310	
		MC9310	
	National	DM74160	
		DM8310	
		DM9310	
	Raytheon	RC9310	
		RM9310	
	TI	SN29310	
		SN39310	
		SN54160	
		SN74160	
9311	AMD	9311	
	Motorola	MC8311	
		MC9311	
	National	DM8311	
		DM9311	
	Raytheon	RC9311	
		RM9311	
	TI	SN29311	
		SN39311	
		SN54154	
		SN74154	
9312	AMD	9312	
	Motorola	MC9312	
	National	DM8312	
		DM9312	
	Raytheon	RC9312	
		RM9312	
	Signetics	8230	
	TI	SN29312	
		SN39312	
9314	AMD	9314	
	Motorola	MC9314	
♦93141	National	DM54141	
		DM74141	
	TI	SN74141	
♦93145	Motorola	MC83145	
		MC93145	
	National	DM54145	
		DM74145	
	Raytheon	54145	
		74145	
	TI	SN54145	
		SN74145	
9315	Motorola	MC8315	
		MC9315	
	National	DM5441	
		DM7441A	
	Signetics	7441	
	TI	SN54141	
♦93150	Motorola	MC83150	
		MC93150	
	National	DM54150	
		DM74150	
	Raytheon	54150	
	TI	SN54150	
		SN74150	
♦93151	Motorola	MC83151	
		MC93151	
	National	DM54151	
		DM74151	
	Raytheon	54151	
	TI	SN54151A	
		SN74151A	
♦93152	Motorola	MC83152	
		MC93152	
	Raytheon	54152	
	TI	SN54152A	
		SN74152	
♦93153	Motorola	MC83153	
		MC93153	
	National	DM54153	
		DM74153	
	Raytheon	54153	
	TI	SN54153	
		SN74153	
♦93155	National	DM54155	
		DM74155	
	TI	SN54155	
		SN74155	
♦93156	National	DM54156	
		DM74156	
	TI	SN54156	
		SN74156	
♦93157	National	DM54157	
		DM74157	
	TI	SN54157	
		SN74157	
9316	AMD	9316	
	Motorola	MC8316	
		MC9316	
	National	DM8316	
		DM9316	
	Raytheon	RC9316	
		RM9316	
	TI	SN29316	
		SN39316	
		SN54161	
		SN74161	
♦93160	National	DM54160	
		DM74160	
	TI	SN54160	
		SN74160	
♦93161	National	DM54161	
		DM74161	
	TI	SN54161	
		SN74161	
♦93162	National	DM54162	
		DM74162	
	TI	SN54162	
		SN74162	
♦93163	National	DM54163	
		DM74163	
	TI	SN54163	
		SN74163	
♦93164	AMD	SN74164	
	Motorola	MC83164	
		MC93164	
	National	DM54164	
		DM74164	
	TI	SN54164	
		SN74164	
♦93165	Motorola	MC83165	
	National	DM54165	
		DM74165	
	TI	SN54165	
		SN74165	
♦93166	National	DM54166	
		DM74166	
	TI	SN54166	
♦93166	TI	SN74166	
9317B	National	DM5447	
		DM7447	
	TI	SN5446A	
		SN7446A	
9317C	National	DM5446	
		DM7446	
	TI	SN29318	
		SN39318	
		SN5446A	
		SN7446A	
♦93170	National	DM74170	
	TI	SN54170	
		SN74170	
♦93174	AMD	SN74174	
	National	DM54174	
		DM74174	
	TI	SN54174	
		SN74174	
♦93175	AMD	SN74175	
	National	DM54175	
		DM74175	
	TI	SN54175	
		SN74175	
♦93176	Motorola	MC93176	
	National	DM54176	
		DM74176	
	TI	SN54176	
		SN74176	
♦93177	Motorola	MC83177	
		MC93177	
	National	DM54177	
		DM74177	
	TI	SN54177	
		SN74177	
♦93178	Motorola	MC83178	
		MC93178	
	TI	SN54178	
		SN74178	
♦93179	Motorola	MC83179	
		MC93179	
	TI	SN54179	
		SN74179	
9318	AMD	9318	
	Motorola	MC9318	
	National	DM8318	
		DM9318	
	TI	SN54148	
		SN74148	
♦93180	Motorola	MC83180	
		MC93180	
	National	DM54180	
		DM74180	
	TI	SN54180	
		SN74180	
♦93190	National	DM54190	
		DM74190	
	TI	SN54190	
		SN74190	
♦93191	National	DM54191	
		DM74191	
	TI	SN54191	
		SN74191	
♦93194	AMD	SN74194	
	National	DM54194	
		DM74194	
	TI	SN54194	
		SN74194	
♦93195	National	DM54195	
		DM74195	
	TI	SN54195	
		SN74195	
♦93196	Motorola	MC7280	
	National	DM54196	
		DM74196	
	TI	SN54196	
		SN74196	
♦93197	Motorola	MC8280	
	National	DM54197	
		DM74197	
	TI	SN54197	
		SN74197	
♦93198	Motorola	MC8316	
	National	DM54198	
		DM74198	
	Signetics	54198	

♦ Discontinued

The manufacturers report their devices can be used as direct replacements.
Performance details often differ, so compare the specifications considering your requirements.

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Manufacturer Device	Replacement Source	Device	IC Master Page
♦93198	Signetics	74198	
	TI	SN54198	
		SN74198	
♦93199	National	DM54199	
		DM74199	
	TI	SN54199	
		SN74199	
932	National	DM932	
9321	AMD	9321	
	National	DM54LS139	
		DM74LS139	
	TI	SN54S139	
		SN74S139	
9322	AMD	9322	
	Motorola	MC8322	
		MC9322	
	National	DM74157	
		DM8322	
		DM9322	
	Raytheon	RC9322	
		RM9322	
	TI	SN29322	
		SN39322	
		SN54157	
		SN74157	
9324	AMD	9324	
	Motorola	MC9324	
♦9325	National	DM54141	
		DM74141	
	Signetics	54141	
		74141	
	TI	SN74141	
9328	AMD	9328	
	Motorola	MC9328	
	Signetics	N8277	
933	National	DM933	
9334	AMD	9334	
	Motorola	MC9334	
	National	DM9334	
	TI	SN54259	
		SN74259	
9338	AMD	9338	
9340	AMD	9340	
♦93400	Motorola	MCM4012	
♦93403	AMD	93403	
	Fairchild	7489	
	MMI	27S02	
		6560	
	Motorola	MCM4064	
		MC4064	
	National	DM7489	
	Signetics	**N82S25**	**1678**
	TI	SN54S289	
		SN74S289	
		SN7489	
♦93404	Signetics	82S25	
♦93406	Intersil	IM5603	
	MMI	**6200-1**	**1466**
	Motorola	MCM4006	
	Signetics	N82S226	
	TI	SN54187	
		SN74187	
93407	Motorola	MC4004	
		MC4304	
	TI	SN5481A	
		SN7481A	
9341	AMD	9341	
	Motorola	MC8341	
		MC9341	
	National	DM54181	
		DM74181	
	Raytheon	RC9341	
		RM9341	
	Signetics	54181	
		74181	
	TI	SN54181	
		SN74181	
93410	Motorola	MCM4056	
♦93410	**Signetics**	**54S301**	**1678**
		74S301	**1678**
	TI	SN54S300	
		SN54S301	
		SN74S300	
♦93410	TI	SN74S301	
93411	Hitachi	HM2504	
	MMI	5530	
		6530	
		6531	
	National	DM54S206	
		DM74S206	
	Raytheon	RC5330	
		RM5330	
	Signetics	82S17	
	TI	SN54S200A	
		SN54S201	
		SN74S200A	
		SN74S201	
93412	Intersil	IM5600	
	Motorola	MCM93412	
	TI	SN54S214	
		SN74S214	
93415	**AMI**	**S4015**	**1203**
	Fujitsu	MBM93415	
	Hitachi	HM2510	
	Intel	**2115**	**1416**
	Motorola	MCM93415	
	Raytheon	RC5500	
		RM5500	
	RCA	MWS5001	
		MWS5501	
	Signetics	**N82S10**	**1678**
		N82S110	**1678**
		S82S110	
		93415	
	TI	SN54S314	
		SN74S314	
93415A	TI	SN74S314	
93416	Harris	HPROM1024A	
	Intersil	IM5603	
	MMI	**6300-1**	**1449**
	NEC Micro	μPD403	
	Signetics	**N82S126**	**1680**
	TI	**SN54S387**	**1708**
		SN74S387	**1708**
93417	AMD	AM27S20	
	Harris	**HM7610**	**1284,1292**
		HM7610A	
	MMI	**53S140**	**1453**
		5300-1	**1449**
		63S140	**1453**
		6300-1	**1449**
	National	DM54S387	
		DM74S387	
	NEC Micro	μPB403	
	Raytheon	**29660**	**1664**
	TI	**SN54S387**	**1708**
		SN74S387	**1708**
934183	TI	SN54H183	
		SN74H183	
9342	AMD	9342	
	Motorola	MC8342	
		MC9342	
	National	DM54182	
		DM74182	
	Raytheon	RM9342	
	Signetics	54182	
		74182	
	TI	SN54182	
		SN74182	
93421	MMI	5531	
		6531	
	National	DM54S200	
		DM74S200	
	NEC America	μPB2200	
	Raytheon	RC5340	
		RM5340	
	Signetics	**N82S16**	**1678**
	TI	SN54S200A	
		SN54S201	
		SN74S200A	
		SN74S201	
93422	Motorola	MCM93422	
93425	**AMI**	**S4025**	**1203**
	Hitachi	HM2511	
	Intel	**2125**	**1416**
	Motorola	MCM93425	
	RCA	MWS5001	
		MWS5501	
93425	**Signetics**	**N82S111**	**1678**
		S82S111	
		93425	
	TI	SN54S214	
		SN74S214	
93426	Harris	HPROM1024	
	Intersil	IM5623	
	MMI	**6301-1**	**1449**
	Signetics	**N82S129**	**1680**
	TI	**SN54S287**	**1708**
		SN74S287	**1708**
93427	AMD	AM27S21	
	Harris	**HM7611**	**1284,1292**
		HM7611A	
	MMI	**53S141**	**1453**
		5301-1	**1449**
		63S141	**1453**
		6301-1	**1449**
	National	DM54S287	
		DM74S287	
	Raytheon	**29661**	**1664**
	TI	**SN54S287**	**1708**
		SN74S287	**1708**
93433	Hitachi	HM2501	
	Motorola	MC4004	
	TI	SN83433	
		SN93433	
♦93434	Intersil	IM5600	
	MMI	**5230-1**	**1466**
		6230-1	**1466**
	Motorola	MCM4002	
	National	DM5487	
		DM7488	
	Signetics	8223	
	TI	SN5488A	
		SN7488A	
93435	MMI	5560	
		6560	
	Motorola	MC4064	
	TI	SN7489	
93436	AMD	AM27S12	
	Harris	**HM7621**	**1284,1298**
	Intel	3602	
	Intersil	IM5604	
	MMI	**53S240**	**1453**
		5305-1	**1449**
		63S240	**1453**
		6305-1	**1449**
	National	DM54S570	
		DM74S570	
	Raytheon	**29610**	**1654**
	Signetics	82S130	
	TI	SN54S270	
		SN74S270	
93438	**Harris**	**HM7640**	**1284,1304**
		HM7640A	
	MMI	**53S482**	**1453**
		5340-1	**1449**
		63S482	**1453**
		6340-1	**1449**
	National	DM77S295	
		DM87S295	
	NEC Micro	**μPB405**	**1621**
	Raytheon	**29624**	**1658**
	TI	**SN54S475**	**1708**
		SN74S475	**1708**
93446	AMD	AM27S13	
	Harris	**HM7621**	**1284,1298**
	Intel	3622	
	MMI	**53S241**	**1453**
		5306-1	**1449**
		63S241	**1453**
		6306-1	**1449**
	National	DM54S571	
		DM74S571	
	Raytheon	**29611**	**1654**
	Signetics	82S131	
93448	**Harris**	**HM7641**	**1284,1304**
		HM7641A	
	MMI	**53S483**	**1453**
		5341-1	**1449**
93448	**MMI**	**63S483**	**1453**
		6341-1	**1449**
	National	DM77S296	
		DM87S296	
	NEC Micro	**μPB425**	**1621**
	Raytheon	**29625**	**1658**
	TI	**SN54S474**	**1708**
		SN74S474	**1708**
♦9345	Motorola	MC9345	
	National	DM5445	
		DM7445	
	Signetics	5445	
		7445	
	TI	SN5445A	
		SN7445A	
93450	**MMI**	**5380-1**	**1449**
		6380-1	**1449**
93451	**MMI**	**5381-1**	**1449**
		6381-1	**1449**
93452	**MMI**	**5352-1**	**1449**
		6352-1	**1449**
	National	DM54S572	
		DM74S572	
	NEC Micro	**μPB406**	**1625**
	Raytheon	29640	
	Signetics	**N82S136**	**1680**
		S82S136	**1680**
93453	**MMI**	**5353-1**	**1449**
		6353-1	**1449**
	National	DM54S573	
		DM74S573	
	NEC Micro	**μPB426**	**1625**
	Raytheon	29641	
93474	**AMI**	**S2114**	**1196**
93487	TI	SN54H87	
♦93487	TI	SN74H87	
♦9349	Signetics	54180	
		74180	
	TI	SN54180	
		SN74180	
♦935	National	DM935	
♦9350	TI	SN54290	
		SN74290	
♦9352	Motorola	MC8352	
		MC9352	
	National	DM5442	
		DM7442	
	Signetics	5442	
		7442	
	TI	SN5442	
		SN7442	
♦9353	Motorola	MC8353	
		MC9353	
	Signetics	5443	
		7443	
	TI	SN5443	
		SN7443	
♦9354	Motorola	MC8354	
		MC9354	
	Signetics	5444	
		7444	
	TI	SN5444A	
		SN7444A	
♦9355	Motorola	MC8355	
♦9356	TI	SN54293	
		SN74293	
♦9357	Motorola	MC8357	
		MC9357	
♦9357A	Motorola	MC9357A	
	National	DM5446A	
		DM7446A	
	Signetics	7446	
	TI	SN5446A	
		SN7446A	
♦9357B	Motorola	MC9357B	
	National	DM5447A	
		DM7447A	
	Signetics	7447	
	TI	SN5447A	
		SN7447A	
♦9358	Motorola	MC8358	
		MC9358	
	National	DM5448	
		DM7448	
	Signetics	7448	
	TI	SN5448	

♦ Discontinued

Bold face device numbers indicate manufacturers data is provided in the IC Master on the pages noted.

Fairchild (cont'd)

Manufacturer Device	Replacement Source	Device	IC Master Page
♦9358	TI	SN7448	
♦9359	Motorola	MC8359	
		MC9359	
	TI	SN54293	
936	National	DM936	
9360	AMD	9360	
	Motorola	MC8360	
		MC9360	
	National	DM54192	
		DM74192	
	Raytheon	RC9360	
		RM9360	
	TI	SN54192	
		SN74192	
♦9366	AMD	9366	
	Motorola	MC8366	
		MC9366	
	National	DM54193	
		DM74193	
	Raytheon	RM9366	
	TI	SN54193	
		SN74193	
9368	Mitel	MD4368	
937	National	DM937	
9375	Motorola	MC9375	
	National	DM5475	
		DM7475	
	Signetics	5475	
		7475	
♦9375	TI	SN5475	
		SN7475	
♦9377	Motorola	MC8377	
		MC9377	
	National	DM54LS77	
		DM74LS77	
	TI	SN5477	
		SN7477	
♦9380	Motorola	MC8380	
		MC9380	
	Signetics	5480	
		7480	
	TI	SN5480	
		SN7480	
♦9382	Motorola	MC8382	
		MC9382	
	National	DM7482	
	TI	SN5482	
		SN7482	
♦9383	Motorola	MC8383	
		MC9383	
	National	DM5483	
		DM7483	
	Signetics	5483	
		7483	
	TI	SN5483A	
		SN7483A	
♦9385	National	DM5485	
		DM7485	
9386	TI	SN54LS266	
		SN74LS266	
939	National	DM939	
♦9390	Motorola	MC8390	
		MC9390	
	National	DM5490	
		DM7490	
	Signetics	5490	
		7490	
	TI	SN5490A	
		SN7490A	
♦9391	Motorola	MC8391	
		MC9391	
	National	DM5491	
		DM7491	
	Signetics	5491	
		7491	
	TI	SN5491A	
		SN7491A	
♦9392	Motorola	MC8392	
		MC9392	
	National	DM5492	
		DM7492	
	Signetics	9392	
	TI	SN5492A	
♦9392	TI	SN7492A	
♦9393	Motorola	MC8393	
		MC9393	
	National	DM5493	
		DM7493	
	Signetics	5493	
		7493	
	TI	SN5493	
		SN7493	
♦9394	Motorola	MC8394	
		MC9394	
	Signetics	5494	
		7494	
	TI	SN5494	
		SN7494	
♦9395	Motorola	MC8395	
		MC9395	
	National	DM5495	
		DM7495	
	Signetics	5495	
		7495	
	TI	SN5495A	
		SN7495A	
♦9396	Motorola	MC8396	
		MC9396	
	National	DM5496	
		DM7496	
	Signetics	5496	
		7496	
	TI	SN5496	
		SN7496	
944	National	DM944	
945	National	DM945	
946	National	DM946	
948	National	DM948	
949	National	DM949	
95H90	Plessey	SP8641	
96L02	AMD	96L02	
	National	DM9602	
96S02	National	DM8602	
		DM9602	
9600	AMD	9600	
9601	AMD	9601	
	Motorola	MC9601	
	National	DM8601	
		DM9601	
	Raytheon	RF8601	
		RF9601	
	TI	SN29601	
9602	AMD	9602	
	Motorola	MC9602	
	National	DM8602	
		DM9602	
	Raytheon	RF8602	
		RF9602	
9603	Motorola	MC8603	
		MC9603	
	National	DM54121	
		DM74121	
	Signetics	54121	
		74121	
	TI	SN54121	
		SN74121	
961	National	DM961	
9614	AMD	9614	
	TI	SN55114	
		SN75114	
9615	AMD	9615	
	TI	SN55115	
		SN75115	
9616	AMD	9616	
9617	AMD	9617	
96176	Motorola	MC83176	
962	National	DM962	
9620	AMD	9620	
9621	AMD	9621	
	Raytheon	RC9621	
		RM9621	
9622	Raytheon	RC9622	
		RM9622	
963	National	DM963	
9636	Motorola	MC3488	
9640	AMD	AM26S10	
	Motorola	MC3440	
		MC3443	
	TI	AM26S10	
9641	AMD	AM26S11	
	TI	AM26S11	
9664	Signetics	7524	
	TI	SN75492	
9665	**Exar**	**XR2201**	**931**
	Motorola	MC1411	
	SGS	L201	
	Signetics	NE5501	
		ULN2001	
		7525	
	Silicon G	SG2001	
	Sprague	ULN-2001	
	TI	ULN2001	
9666	**Exar**	**XR2202**	**931**
	Motorola	MC1412	
	SGS	L202	
	Signetics	NE5502	
		ULN2002	
	Silicon G	SG2002	
	Sprague	ULN-2002	
	TI	ULN2002	
9667	**Exar**	**XR2203**	**931**
	Motorola	MC1413	
	SGS	L203	
	Signetics	NE5503	
		ULN2003	
	Silicon G	SG2003	
	Sprague	ULN-2003	
	TI	ULN2003	
9668	**Exar**	**XR2204**	**931**
	Motorola	MC1416	
	Signetics	NE5504	
		ULN2004	
	Sprague	ULN-2004	
	TI	ULN2004	
9930	Hitachi	HD2204	
	Raytheon	RM930	
	TI	SN15830	
		SN15930	
9932	Hitachi	HD2201	
	Raytheon	RM932	
	TI	SN15832	
		SN15932	
9933	Hitachi	HD2202	
	Raytheon	RM933	
	TI	SN15833	
		SN15933	
9935	Hitachi	HD2208	
	Raytheon	RM935	
	TI	SN15835	
		SN15935	
9936	Hitachi	HD2206	
	Raytheon	RM936	
	TI	SN15836	
		SN15936	
9937	Raytheon	RM937	
	TI	SN15837	
		SN15937	
9941	Raytheon	RM941	
	TI	SN15841	
		SN15941	
9944	Hitachi	HD2209	
	Raytheon	RM944	
	TI	SN15844	
		SN15944	
9945	Hitachi	HD2205	
	Raytheon	RM945	
	TI	SN15845	
		SN15945	
9946	Hitachi	HD2203	
	Raytheon	RM946	
	TI	SN15846	
		SN15946	
9948	Raytheon	RM948	
	TI	SN15848	
		SN15948	
9949	TI	SN15849	
		SN15949	
9950	Raytheon	RM950	
	TI	SN15850	
		SN15950	
9951	Raytheon	RM951	
	TI	SN15851	
		SN15951	
9961	Raytheon	RM961	
	TI	SN15861	
9961	TI	SN15961	
9962	Hitachi	HD2207	
	Raytheon	RM962	
	TI	SN15862	
		SN15962	
9963	Raytheon	RM963	
	TI	SN15863	
		SN15963	

Ferranti Electric

ZN425	**Datel**	**ADC-MC8B**	**664**

Fujitsu

MBL6800	**Fairchild**	**F6800**	**1886,1888**
MBL6802	**Fairchild**	**F6802**	**1887,1888**
MBL6850	**Fairchild**	**F6850**	**1887,1891**
MBM4044	TI	TMS4044	
MB2114	**NEC Micro**	**μPD2114**	**1604**
MB7054	**Fairchild**	**93453**	**1264**
	NEC Micro	**μPB426**	**1625**
MB7055	**Signetics**	**N82S2708**	**1702**
MB7057	NEC Micro	μPB403	
MB7059	**Fairchild**	**93452**	**1264**
	NEC Micro	**μPB406**	**1625**
MB8101	**NEC Micro**	**μPD2101AL**	**1586**
MB8107	**NEC Micro**	**μPD411**	**1547**
	TI	TMS4060	
MB8111	**NEC Micro**	**μPD2111AL**	**1595**
MB8114	**Fairchild**	**2114**	**1281**
	Rockwell	R2114	
MB8116	AMD	9016	
	NEC Micro	**μPD416**	**1562**
	TI	TMS4116	
MB8224	NEC Micro	μPD414	
MB8227	Fairchild	M4027	
	NEC Micro	μPD414A	
	TI	TMS4027	
MB8308	TI	TMS4700	
MB8508	TI	TMS2708	
MB8515	AMD	2708	
	EA	EA2708	
	Intel	2708	
	Motorola	MCM2708	
	National	MM2708	
	TI	TMS2708	

General Instrument

AY1-0212	AMI	S50242	
AY1-2006	AMI	S10131	
AY3-1014A	RCA	CDP1854	
	SMC	COM2017	
	TI	TMS6011	
AY5-1012	SMC	COM2502	
♦AY5-1012	TI	TMS6011	
AY5-1013A	**AMI**	**S1883**	**629**
	SMC	COM2502H	
	Western	TR1402	
		TR1602	
AY5-2376	SMC	KR2376	
AY5-3507	Plessey	μP3202	
AY5-3600	SMC	KR3600	
AY5-3600-PRO	SMC	KR3600-PRO	
ER1400	Nitron	NC1400	
ER1711	Nitron	NC1711	
ER2051	Nitron	NC2051	
ER2055	Nitron	NC2055	
ER2401	Nitron	NC2401	
ER2805	Nitron	NC2805	
RA9-1101	Mostek	MK4007	
♦RA9-1103	Signetics	1103	
♦RO1-2048	AMI	S8773	
RO3-16384	AMI	S8996	
RO3-8316	**AMI**	**S6831A**	
			1215,1806
	Fairchild	3516E	
	Mostek	MK31000	
	Rockwell	R2316	
RO3-9316	**AMI**	**S4216B**	**1209**
		S6831B	
			1215,1806

♦ Discontinued

The manufacturers report their devices can be used as direct replacements.
Performance details often differ, so compare the specifications considering your requirements.

General Instrument (cont'd)

Manufacturer Device	Replacement Source	Device	IC Master Page
RO3-9316	Mostek	MK34000	
RO3-9332	**AMI**	**S68332**	**1216**
RO5-2240	Fairchild	3257	
	Mostek	MK2302	
	SMC	CG4100	
RO5-8192	AMI	S8865	
♦RO6-1024	AMI	S8773	
♦RO6-2048	AMI	S8773	
R03-9332C	TI	TMS4732	

Harris Semiconductor

HA-2050	**Datel**	**AM-405-2M**	**687**
HA-2055	**Datel**	**AM-405-2**	**687**
HA-2060	**Datel**	**AM-406-2M**	**687**
HA-2065	**Datel**	**AM-406-2**	**687**
HA-2420	**Datel**	**SHM-IC-1M**	**685**
HA-2425	AD	AD583	
	Datel	**SHM-IC-1**	**685**
HA-2500	Intersil	HA2500	
HA-2502	**Datel**	**AM-450-2M**	**687**
	Intersil	HA2502	
HA-2505	**Datel**	**AM-450-2**	**687**
	Intersil	HA2505	
HA-2520	AD	AD509	
	Intersil	HA2520	
HA-2522	**Datel**	**AM-452-2M**	**687**
	Intersil	HA2522	
HA-2525	AD	AD509	
	Datel	**AM-452-2**	**687**
	Intersil	HA2525	
HA-2600	Intersil	HA2600	
HA-2602	**Datel**	**AM-460-2M**	**687**
	Intersil	HA2602	
HA-2605	**Datel**	**AM-460-2**	**687**
HA-2620	Intersil	HA2620	
HA-2622	**Datel**	**AM-462-2M**	**687**
	Intersil	HA2622	
HA-2625	AD	AD507	
	Datel	**AM-462-2**	**687**
HA-2640	**Datel**	**AM-464-2M**	**687**
	National	LM143	
HA-2645	**Datel**	**AM-464-2**	**687**
	National	LM343	
HA-2650	Exar	XR1558	
HA-2665	Exar	XR1458	
HA-2700	Datel	AM-470-2M	
HA-2705	Datel	AM-470-2C	
HA-2720	Fairchild	μA776	
	Intersil	8021	
HA-2900	**Datel**	**AM-490-2M**	**690**
HA-2905	**Datel**	**AM-490-2A**	**690**
	TI	TL089	
HA-4741	Exar	XR4741	
	Raytheon	HA4741	
HA1488	Signetics	MC1488	
♦HD14518	RCA	CD4518	
	SSS	SCL4518	
♦HD14520	RCA	CD4520	
	SSS	SCL4520	
♦HD14529	RCA	CD4052	
HD1489	Signetics	MC1489	
HD1489A	Signetics	MC1489A	
♦HD4000	Motorola	MC14000	
	RCA	CD4000	
	SSS	SCL4000	
♦HD4001	Motorola	MC14001	
	National	CD4001	
	RCA	CD4001	
	SSS	SCL4001	
♦HD4002	Motorola	MC14002	
	National	CD4002	
	RCA	CD4002	
	SSS	SCL4002	
♦HD4006	RCA	CD4006	
	SSS	SCL4006	
♦HD4007	Motorola	MC14007	
	National	CD4007	
	RCA	CD4007	
	SSS	SCL4007	
♦HD4008	RCA	CD4008	
♦HD4011	National	CD4011	
♦HD4011	RCA	CD4011	
	SSS	SCL4011	
♦HD4012	Motorola	MC14012	
	National	CD4012	
	RCA	CD4012	
	SSS	SCL4012	
♦HD4013	Motorola	MC14013	
	National	CD4013	
	RCA	CD4013	
	SSS	SCL4013	
♦HD4014	National	CD4014	
	RCA	CD4014	
	SSS	SCL4014	
♦HD4015	National	CD4015	
	RCA	CD4015	
	SSS	SCL4015	
♦HD4017	National	CD4017	
	RCA	CD4017	
	SSS	SCL4017	
♦HD4018	National	CD4018	
	RCA	CD4018	
	SSS	SCL4018	
♦HD4019	National	CD4019	
	RCA	CD4019	
	SSS	SCL4019	
♦HD4020	National	CD4020	
	RCA	CD4020	
	SSS	SCL4020	
♦HD4021	National	CD4021	
	RCA	CD4021	
	SSS	SCL4021	
♦HD4022	National	CD4022	
	RCA	CD4022	
	SSS	SCL4022	
♦HD4023	Motorola	MC14023	
	National	CD4023	
	RCA	CD4023	
	SSS	SCL4023	
♦HD4024	National	CD4024	
	RCA	CD4024	
	SSS	SCL4024	
♦HD4025	Motorola	MC14025	
	National	CD4025	
	RCA	CD4025	
	SSS	SCL4025	
♦HD4027	National	CD4027	
	RCA	CD4027	
	SSS	SCL4027	
♦HD4028	National	CD4028	
	RCA	CD4028	
	SSS	SCL4028	
♦HD4029	National	CD4029	
	RCA	CD4029	
	SSS	SCL4029	
♦HD4030	National	CD4030	
	RCA	CD4030	
		CD4070	
	SSS	SCL4030	
♦HD4035	National	CD4035	
	RCA	CD4035	
	SSS	SCL4035	
♦HD4040	National	CD4040	
	RCA	CD4040	
	SSS	SCL4040	
♦HD4042	National	CD4042	
	SSS	SCL4042	
♦HD4049	National	CD4049	
	RCA	CD4049	
	SSS	SCL4049	
♦HD4050	National	CD4050	
	RCA	CD4050	
	SSS	SCL4050	
♦HD4066	**National**	**CD4066**	**1076**
	RCA	CD4066	
	SSS	SCL4066	
HD4702	Fairchild	F4702	
♦HD54CXX	National	MM54CXX	
HD6101	Intersil	IM6101	
HD6101A	Intersil	IM6101A	
HD6101C	Intersil	IM6101C	
HD6402	Intersil	IM6402	
	SMC	COM2017	
		COM2502	
HD6402A	Intersil	IM6402A	
HD6402C	Intersil	IM6402C	
HD6403	Intersil	IM6403	
HD6403	SMC	COM2017	
		COM2502	
HD6403A	Intersil	IM6403A	
HD6403C	Intersil	IM6403C	
HD6600	MMI	HD6600	
HD6605	MMI	HD6605	
HD70C95	National	MM70C95	
HD70C97	National	MM70C97	
♦HD74CXX	National	MM74CXX	
HD80C95	National	MM70C95	
HD80C97	Fairchild	F40097	
	National	MM70C97	
		MM80C97	
HI1818	RCA	CD4051	
HI1818A	**Datel**	**MV-808**	**683**
HI1828	RCA	CD4052	
HI1828A	**Datel**	**MVD-409**	**683**
HI5040	Intersil	IH5040	
HI5041	Intersil	IH5041	
HI5042	Intersil	IH5042	
HI5044	Intersil	IH5044	
HI5045	Intersil	IH5045	
HI5046	Intersil	IH5046	
HI5047	Intersil	IH5047	
HI5048	Intersil	IH5048	
HI5049	Intersil	IH5049	
HI5050	Intersil	IH5050	
HI5051	Intersil	IH5051	
HI506	**Datel**	**MV-1606**	**683**
	Intersil	IH5060	
	RCA	CD4067	
	Siliconix	DG506	
HI506A	**Datel**	**MX-1606**	**683**
	Teledyne P	4552	
HI507	**Datel**	**MVD-807**	**683**
	RCA	CD4097	
	Siliconix	DG507	
HI507A	**Datel**	**MXD-807**	**683**
	Teledyne P	4551	
HI508	RCA	CD4051	
HI508A	**Datel**	**MX-808**	**683**
HI509	RCA	CD4052	
HI509A	**Datel**	**MXD-409**	**683**
HI562-2	**Datel**	**DAC-681M**	**674**
HI562-5	**Datel**	**DAC-681C**	**674**
HM5101	**AMI**	**S5101**	**1206**
HM6100	Intersil	IM6100	
HM6100A	Intersil	IM6100A	
HM6100C	Intersil	IM6100C	
HM6402	SMC	COM6402	
HM6501	**AMI**	**S5101**	**1206**
	Fairchild	3538	
	Intel	2101	
		5101	
	NEC Micro	**μPD5101**	**1562**
	RCA	CPD1822	
		MWS5040	
	SSS	SCM5101	
HM6504	AMD	9145	
	Fujitsu	MBM6504	
	Mostek	MK4104	
	Toshiba	TC5504	
HM6508	**AMI**	**S6508**	**1207**
	Intel	**2125**	**1416**
	Intersil	IM6508	
	National	MM74C929	
	NEC Micro	**μPD6508**	**1562**
	Toshiba	TC5508	
HM6514	**Fairchild**	**2114**	**1281**
	Fujitsu	MBM6514	
	Intel	2114	
	Rockwell	R2114	
HM6518	**AMI**	**S6518**	**1208**
	Intersil	IM6518	
	National	MM74C930	
HM6551	Intersil	IM6551	
	National	MM74C920	
HM6561	Intersil	IM6561	
HM7161	**MMI**	**53S1681**	**1453**
		63S1681	**1453**
HM7602	AMD	AM27S18	
	MMI	**5330-1**	**1449**
		5331-1	**1449**
		6330-1	**1449**
		6331-1	**1449**
	National	DM7577	
HM7602	National	DM8577	
	Signetics	**N82S23**	**1680**
	TI	**SN54S188**	**1708**
		SN74S188	**1708**
HM7603	AMD	AM27S19	
	MMI	**5331-1**	**1449**
		6331-1	**1449**
	Signetics	**N82S123**	**1680**
	TI	**SN54S288**	**1708**
		SN74S288	**1708**
HM7608	**Raytheon**	**29635**	**1662**
HM7610	AMD	AM27S20	
	Fairchild	**93417**	**1258**
	Intel	3601-1	
	Intersil	IM5603	
	MMI	**53S1680**	**1453**
		5300-1	**1449**
		63S1680	**1453**
		6300-1	**1449**
	National	DM54S387	
		DM74S387	
	NEC Micro	μPB403	
	Raytheon	**29660**	**1664**
	Signetics	**N82S126**	**1680**
		S82S126	**1680**
	TI	**SN54S387**	**1708**
		SN74S387	**1708**
HM7610A	**MMI**	**53S140**	**1453**
		63S140	**1453**
HM7611	AMD	AM27S21	
	Fairchild	**93427**	**1258**
	Intersil	IM5623	
	MMI	**5301-1**	**1449**
		6301-1	**1449**
	National	DM7574	
	Raytheon	**29661**	**1664**
	Signetics	**N82S129**	**1680**
		S82S129	**1680**
	TI	**SN54S287**	**1708**
		SN74S287	**1708**
HM7611A	**MMI**	**53S141**	**1453**
		63S141	**1453**
HM7620	AMD	AM27S12	
	Fairchild	**93436**	**1260**
	Intel	3602	
	MMI	**5305-1**	**1449**
		6305-1	**1449**
	Motorola	MCM7620	
	National	DM54S570	
		DM74S570	
	Raytheon	**29610**	**1654**
	Signetics	**N82S130**	**1680**
		S82S130	**1680**
	TI	SN54S270	
		SN74S270	
HM7620A	**MMI**	**53S240**	**1453**
		63S240	**1453**
HM7621	AMD	AM27S13	
	Fairchild	**93446**	**1260**
	Intel	3622	
	MMI	**5306-1**	**1449**
		6306-1	**1449**
	Motorola	MCM7621	
	National	DM54S571	
		DM74S571	
	Raytheon	**29611**	**1654**
	Signetics	**N82S131**	**1680**
		S82S131	**1680**
	TI	SN54S370	
		SN74S370	
HM7621A	**MMI**	**53S241**	**1453**
		63S241	**1453**
HM7640	**Fairchild**	**93438**	**1262**
	Intel	3604	
	MMI	**5340-1**	**1449**
		6340-1	**1449**
	Motorola	MCM7640	
	National	DM77S295	
		DM87S295	
	NEC Micro	**μPB405**	**1621**
	Raytheon	**29621**	**1656**
		29624	**1658**
	RCA	CD40032	
	TI	SN54S475	1708
		SN74S475	**1708**
HM7640A	**MMI**	**53S482**	**1453**

♦ Discontinued

Bold face device numbers indicate manufacturers data is provided in the IC Master on the pages noted.

Harris Semiconductor (cont'd)

Manufacturer Device	Replacement Source	Device	IC Master Page
HM7640A	**MMI**	**63S482**	**1453**
HM7641	Intel	3624	
	MMI	**53S483**	**1453**
		5341-1	**1449**
		63S483	**1453**
		6341-1	**1449**
	Motorola	MCM7641	
	National	DM77S296	
		DM87S296	
	NEC Micro	**μPB425**	**1621**
	Raytheon	**29625**	**1658**
	TI	**SN54S474**	**1708**
		SN74S474	**1708**
HM7642	**Fairchild**	**93452**	**1264**
	Intel	3605	
	MMI	**5352-1**	**1449**
		6352-1	**1449**
	Motorola	MCM7642	
	National	DM54S572	
		DM74S572	
	NEC Micro	**μPB406**	**1625**
	Raytheon	29640	
	Signetics	**N82S136**	**1680**
		S82S136	**1680**
HM7643	**Fairchild**	**93453**	**1264**
	Intel	3625	
	MMI	**5353-1**	**1449**
		6353-1	**1449**
	Motorola	MCM7643	
	National	DM54S573	
		DM74S573	
	NEC Micro	**μPB426**	**1625**
	Raytheon	29641	
	Signetics	**N82S137**	**1680**
		S82S137	**1680**
HM7647R	AMD	AM27S15	
HM7648	**MMI**	**5348-1**	**1449**
		6348-1	**1449**
	Raytheon	**29620**	**1656**
HM7649	**MMI**	**5349-1**	**1449**
		6349-1	**1449**
HM7680	**Fairchild**	**93450**	**1266**
	MMI	**5380-1**	**1449**
		6380-1	**1449**
	Motorola	MCM7680	
	Raytheon	**29630**	**1660**
HM7680P	MMI	53PS880	
		63PS880	
HM7681	**Fairchild**	**93451**	**1266**
	MMI	**5381-1**	**1449**
		6381-1	**1449**
	Motorola	MCM7681	
	Raytheon	**29631**	**1660**
HM7681P	MMI	53PS881	
		63PS881	
HM7684	**MMI**	**53S840**	**1453**
		63S840	**1453**
	Raytheon	29650	
HM7684P	MMI	53PS840	
		63PS840	
HM7685	**MMI**	**53S841**	**1453**
		63S841	**1453**
	Motorola	MCM7685	
	Raytheon	29651	
HM7685P	MMI	53PS841	
		63PS841	
HM7686	Motorola	MCM7686	
HM7687	Motorola	MCM7687	
HN7684	Motorola	MCM7684	
HPROM-1024A	NEC Micro	μPB403	
HPROM0512	TI	SN54186	
		SN74186	
HPROM1024	**MMI**	**5301-1**	**1449**
		6301-1	**1449**
	Signetics	**N82S129**	**1680**
	TI	**SN54S287**	**1708**
		SN74S287	**1708**
HPROM1024A	Fairchild	93416	
	Intersil	IM5603	
	MMI	**5300-1**	**1449**
		6300-1	**1449**
	Signetics	**N82S126**	**1680**
	TI	**SN54S387**	**1708**
HPROM1024A	**TI**	**SN74S387**	**1708**
♦HPROM2048	**Fairchild**	**93446**	**1260**
	Intersil	IM5624	
	Signetics	**N82S131**	**1680**
HPROM2048A	**Fairchild**	**93436**	**1260**
	Signetics	**N82S130**	**1680**
HPROM8256	Intersil	IM5600	
	MMI	**5330-1**	**1449**
		6330-1	**1449**
	National	DM7577	
		DM8577	
	Signetics	**N82S23**	**1680**
	TI	**SN54S188**	**1708**
		SN54188	
		SN74S188	**1708**
		SN74188	
HROM1024	TI	SN54187	
		SN74187	

Hitachi America, Ltd.

HA1137	Sanyo	LA7230	
HA1197	Sanyo	LA1240	
HA1199	Sprague	ULN-2249	
HA1303	Toshiba	TA7502	
HA17741	Toshiba	TA7504	
HD10101	Fairchild	F10101	
	Motorola	MC10101	
	NEC America	μPB10101	
	Signetics	10101	
HD10102	Fairchild	F10102	
	Motorola	MC10102	
	NEC America	μPB10102	
	Signetics	10102	
HD10104	Fairchild	F10104	
	Motorola	MC10104	
	Signetics	10104	
HD10105	Fairchild	F10105	
	Motorola	MC10105	
	National	DM10105	
	NEC America	μPB10105	
	Signetics	10105	
HD10106	Fairchild	F10106	
	Motorola	MC10106	
	National	DM10106	
	NEC America	μPB10106	
	Signetics	10106	
HD10107	Fairchild	F10107	
	Motorola	MC10107	
	NEC America	μPB10107	
	Signetics	10107	
HD10109	Fairchild	F10109	
	Motorola	MC10109	
	National	DM10109	
	NEC America	μPB10109	
	Signetics	10109	
HD10110	Fairchild	F10110	
	Motorola	MC10110	
	NEC America	μPB10110	
	Signetics	10110	
HD10111	Fairchild	F10111	
	Motorola	MC10111	
	National	DM10111	
	NEC America	μPB10111	
	Signetics	10111	
HD10116	Fairchild	F10116	
	Motorola	MC10116	
	National	DM10116	
	Signetics	10116	
HD10117	Fairchild	F10117	
	Motorola	MC10117	
	National	DM10117	
	NEC America	μPB10117	
	Signetics	10117	
HD10118	Fairchild	F10118	
	Motorola	MC10118	
	National	DM10118	
	NEC America	μPB10118	
	Signetics	10118	
HD10119	Fairchild	F10119	
	Motorola	MC10119	
	National	DM10119	
	Signetics	10119	
HD10121	Fairchild	F10121	
	Motorola	MC10121	
HD10121	National	DM10121	
	Signetics	10121	
HD10124	Fairchild	F10124	
	Motorola	MC10124	
	National	DM10124	
	NEC America	μPB10124	
	Signetics	10124	
HD10125	Fairchild	F10125	
	Motorola	MC10125	
	Signetics	10125	
HD10130	Fairchild	F10130	
	Motorola	MC10130	
	Signetics	1010130	
HD10131	Fairchild	F10131	
	Motorola	MC10131	
	NEC America	μPB10131	
	Signetics	10131	
HD10132	Fairchild	F10132	
	Motorola	MC10132	
	Signetics	10132	
HD10133	Fairchild	F10133	
	Motorola	MC10133	
	NEC America	μPB10133	
	Signetics	10133	
HD10134	Fairchild	F10134	
	Motorola	MC10134	
	Signetics	10134	
HD10136	Fairchild	F10136	
	Motorola	MC10136	
	Signetics	10136	
HD10145	Fairchild	F10145	
	Motorola	MC10145	
	Signetics	10145	
HD10148	Motorola	MCM10148	
	NEC America	μPB10148	
	Signetics	10148	
	TI	SN10148	
HD10160	Fairchild	F10160	
	Motorola	MC10160	
	Signetics	10160	
HD10161	Fairchild	F10161	
	Motorola	MC10161	
	NEC America	μPB10161	
	Signetics	10161	
HD10162	Fairchild	F10162	
	Motorola	MC10162	
	NEC America	μPB10162	
	Signetics	10162	
HD10164	Fairchild	F10164	
	Motorola	MC10164	
	NEC America	μPB10164	
	Signetics	10164	
	TI	SN10164	
HD10165	Fairchild	F10165	
	Motorola	MC10165	
	Signetics	10165	
HD10174	Fairchild	F10174	
	Motorola	MC10174	
	NEC America	μPB10174	
	Signetics	10174	
	TI	SN10174	
HD10175	Fairchild	F10175	
	Motorola	MC10175	
	Signetics	10175	
HD10179	Fairchild	F10179	
	Motorola	MC10179	
	Signetics	10179	
HD10180	Fairchild	F10180	
	Motorola	MC10180	
	NEC America	μPB10180	
	Signetics	10180	
HD10181	Fairchild	F10181	
	Motorola	MC10181	
	NEC America	μPB10181	
	Signetics	10181	
HD46800	**Fairchild**	**F6800**	**1886,1888**
HD46810	**Fairchild**	**F6810**	**1887,1888**
HD46820	**Fairchild**	**F6820**	**1887**
HD46852	**Fairchild**	**F6852**	**1887,1891**
HD74H183	Fairchild	74H183	
	TI	SN74H183	
HD74LS00	Fairchild	74LS00	
	Motorola	SN74LS00	
	National	DM74LS00	
	NEC America	μPB74LS00	
	Raytheon	74LS00	
HD74LS00	Signetics	74LS00	
	TI	SN74LS00	
HD74LS01	Fairchild	HD74LS01	
	Motorola	SN74LS01	
	National	DM74LS01	
	Raytheon	74LS01	
	Signetics	74LS01	
	TI	SN74LS01	
HD74LS02	Fairchild	74LS02	
	Motorola	SN74LS02	
	National	DM74LS02	
	NEC America	μPB74LS02	
	Raytheon	74LS02	
	Signetics	74LS02	
	TI	SN74LS02	
HD74LS03	Fairchild	74LS03	
	Motorola	SN74LS03	
	National	DM74LS03	
	NEC America	μPB74LS03	
	Raytheon	74LS03	
	Signetics	74LS03	
	TI	SN74LS03	
HD74LS04	Fairchild	74LS04	
	Motorola	SN74LS04	
	National	DM74LS04	
	NEC America	μPB74LS04	
	Raytheon	74LS04	
	Signetics	74LS04	
	TI	SN74LS04	
HD74LS05	Fairchild	74LS05	
	Motorola	SN74LS05	
	National	DM74LS05	
	NEC America	μPB74LS05	
	Raytheon	74LS05	
	Signetics	74LS05	
	TI	SN74LS05	
HD74LS08	Fairchild	74LS08	
	Motorola	SN74LS08	
	National	DM74LS08	
	NEC America	μPB74LS08	
	Raytheon	74LS08	
	Signetics	74LS08	
	TI	SN74LS08	
HD74LS09	Fairchild	74LS09	
	Motorola	SN74LS09	
	National	DM74LS09	
	Raytheon	74LS09	
	Signetics	74LS09	
	TI	SN74LS09	
HD74LS10	Fairchild	74LS10	
	Motorola	SN74LS10	
	National	DM74LS10	
	NEC America	μPB74LS10	
	Raytheon	74LS10	
	Signetics	74LS10	
	TI	SN74LS10	
HD74LS107	Fairchild	74LS107	
	Motorola	SN74LS107A	
	National	DM74LS107	
	Raytheon	74LS107	
	Signetics	74LS107	
	TI	SN74LS107A	
HD74LS11	Fairchild	74LS11	
	Motorola	SN74LS11	
	National	DM74LS11	
	NEC America	μPB74LS11	
	Raytheon	74LS11	
	Signetics	74LS11	
	TI	SN74LS11	
HD74LS112	Fairchild	74LS112	
	Motorola	SN74LS112A	
	National	DM74LS112	
	NEC America	μPB74LS112	
	Raytheon	74LS112	
	Signetics	74LS112	
	TI	SN74LS112A	
HD74LS113	Fairchild	74LS113	
	Motorola	SN74LS113A	
	National	DM74LS113	
	NEC America	μPB74LS113	
	Raytheon	74LS113	
	Signetics	74LS113	
	TI	SN74LS113A	
HD74LS114	Fairchild	74LS114	
	Motorola	74LS114A	
	National	DM74LS114	

♦ Discontinued

The manufacturers report their devices can be used as direct replacements.
Performance details often differ, so compare the specifications considering your requirements.

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Manufacturer Device	Replacement Source	Device	IC Master Page
HD74LS114	Raytheon	74LS114	
	Signetics	74LS114	
	TI	SN74LS114A	
HD74LS12	Fairchild	74LS12	
	Motorola	SN74LS12	
	National	DM74LS12	
	Raytheon	74LS12	
	Signetics	74LS12	
	TI	SN74LS12	
HD74LS123	AMD	SN74LS123	
	Motorola	SN74LS123	
	National	DM74LS123	
	Raytheon	74LS123	
	TI	SN74LS123	
HD74LS13	Fairchild	74LS13	
	Motorola	SN74LS13	
	National	DM74LS13	
	Raytheon	74LS13	
	Signetics	74LS13	
	TI	SN74LS13	
HD74LS132	Fairchild	74LS132	
	Motorola	SN74LS132	
	National	DM74LS132	
	Raytheon	74LS132	
	Signetics	74LS132	
	TI	SN74LS132	
HD74LS136	Fairchild	74LS136	
	Motorola	SN74LS136	
	National	DM74LS136	
	Raytheon	74LS136	
	Signetics	74LS136	
	TI	SN74LS136	
HD74LS138	AMD	SN74LS138	
	Fairchild	74LS138	
	Motorola	SN74LS138	
	National	DM74LS138	
	NEC America	μPB74LS138	
	Raytheon	74LS138	
	Signetics	74LS138	
	TI	SN74LS138	
HD74LS139	AMD	SN74LS139	
	Fairchild	74LS139	
	Motorola	SN74LS139	
	National	DM74LS139	
	NEC America	μPB74LS139	
	Raytheon	74LS139	
	Signetics	74LS139	
	TI	SN74LS139	
HD74LS14	Fairchild	74LS14	
	Motorola	SN74LS14	
	National	DM74LS14	
	Raytheon	74LS14	
	Signetics	74LS14	
	TI	SN74LS14	
HD74LS15	Fairchild	74LS15	
	Motorola	SN74LS15	
	National	DM74LS15	
HD74LS151A	AMD	SN74LS151	
	Fairchild	74LS151	
	Motorola	SN74LS151	
	National	DM74LS151	
	NEC America	μPB74LS151	
	Raytheon	74LS151	
	Signetics	74LS151	
	TI	SN74LS151	
HD74LS152	Fairchild	74LS152	
	Motorola	SN74LS152	
	Raytheon	74LS152	
	TI	SN74LS152	
HD74LS153	AMD	SN74LS153	
	Fairchild	74LS153	
	Motorola	SN74LS153	
	National	DM74LS153	
	NEC America	μPB74LS153	
	Raytheon	74LS153	
	Signetics	74LS153	
	TI	SN74LS153	
HD74LS155	Fairchild	74LS155	
	Motorola	74LS155	
	National	DM74LS155	
	NEC America	μPB74LS155	
	Raytheon	74LS155	
	Signetics	74LS155	
HD74LS155	TI	SN74LS155	
HD74LS156	Fairchild	74LS156	
	Motorola	SN74LS156	
	National	DM74LS156	
HD74LS158	Fairchild	74LS158	
	Motorola	SN74LS158	
	National	DM74LS158	
	Raytheon	74LS158	
	Signetics	74LS158	
	TI	SN74LS158	
HD74LS160A	AMD	SN74LS160	
	Fairchild	74LS160	
	Motorola	SN74LS160A	
	National	DM74LS160	
	Raytheon	74LS160	
	Signetics	74LS160A	
	TI	SN74LS160A	
HD74LS161A	AMD	SN74LS161	
	Fairchild	74LS161	
	Motorola	SN74LS161A	
	National	DM74LS161	
	NEC America	μPB74LS161	
	Raytheon	74LS161	
	Signetics	74LS161A	
	TI	SN74LS161A	
HD74LS162A	AMD	SN74LS162	
	Fairchild	74LS162	
	Motorola	SN74LS162A	
	National	DM74LS162	
	Raytheon	74LS162	
	Signetics	74LS162A	
	TI	SN74LS162A	
HD74LS163A	AMD	SN74LS163	
	Fairchild	74LS163	
	Motorola	SN74LS163A	
	National	DM74LS163	
	Raytheon	74LS163	
	Signetics	74LS163A	
	TI	SN74LS163A	
HD74LS164	AMD	SN74LS164	
	Fairchild	74LS164	
	Motorola	SN74LS164	
	National	DM74LS164	
	NEC America	μPB74LS164	
	Raytheon	74LS164	
	Signetics	74LS164	
	TI	SN74LS164	
HD74LS174	AMD	SN74LS174	
	Fairchild	74LS174	
	Motorola	SN74LS174	
	Raytheon	74LS174	
	Signetics	74LS174	
	TI	SN74LS174	
HD74LS175	AMD	SN74LS175	
	Fairchild	74LS175	
	Motorola	SN74LS175	
	National	DM74LS174	
		DM74LS175	
	NEC America	μPB74LS175	
	Raytheon	74LS175	
	Signetics	74LS175	
	TI	SN74LS175	
HD74LS183A	Fairchild	74LS83	
	Motorola	SN74LS83A	
	National	DM74LS83A	
	Raytheon	74LS83A	
	TI	SN74LS83A	
HD74LS194A	AMD	SN74LS194A	
	Fairchild	74LS194A	
	Motorola	SN74LS194A	
	NEC America	μPB74LS194	
	Raytheon	74LS194A	
	Signetics	74LS194A	
	TI	SN74LS194A	
HD74LS195A	AMD	SN74LS195A	
	Fairchild	74LS195	
	Motorola	SN74LS195A	
	NEC America	μPB74LS195	
	Raytheon	74LS195A	
	Signetics	74LS195A	
	TI	SN74LS195A	
HD74LS20	Fairchild	74LS20	
	Motorola	SN74LS20	
	National	DM74LS20	
	NEC America	μPB74LS20	
	Raytheon	74LS20	
HD74LS20	Signetics	74LS20	
	TI	SN74LS20	
HD74LS21	Fairchild	74LS21	
	Motorola	SN74LS21	
	National	DM74LS21	
	NEC America	μPB74LS21	
	Raytheon	74LS21	
	Signetics	74LS21	
	TI	SN74LS21	
HD74LS22	Fairchild	74LS22	
	Motorola	SN74LS22	
	National	DM74LS22	
	Raytheon	74LS22	
	Signetics	74LS22	
	TI	SN74LS22	
HD74LS247	Fairchild	74LS247	
	Motorola	SN74LS247	
	National	DM74LS247	
	TI	SN74LS247	
HD74LS248	Fairchild	74LS248	
	Motorola	SN74LS248	
	National	DM74LS248	
	TI	SN74LS248	
HD74LS249	Fairchild	74LS249	
	Motorola	SN74LS249	
	National	DM74LS249	
	TI	SN74LS249	
HD74LS251	AMD	SN74LS251	
	Fairchild	74LS251	
	Motorola	SN74LS251	
	NEC America	μPB74LS251	
	Raytheon	74LS251	
	Signetics	74LS251	
	TI	SN74LS251	
HD74LS253	AMD	SN74LS253	
	Fairchild	74LS253	
	Motorola	SN74LS253	
	National	DM74LS253	
	NEC America	μPB74LS253	
	Raytheon	74LS253	
	Signetics	74LS253	
	TI	SN74LS253	
HD74LS257	Fairchild	74LS257	
	Motorola	SN74LS257A	
	National	DM74LS257	
	NEC America	μPB74LS257	
	Raytheon	74LS257	
	Signetics	74LS257	
	TI	SN74LS257A	
HD74LS26	Fairchild	74LS26	
	Motorola	SN74LS26	
	National	DM74LS26	
	Raytheon	74LS26	
	Signetics	74LS26	
	TI	SN74LS26	
HD74LS27	Fairchild	74LS27	
	Motorola	SN74LS27	
	National	DM74LS27	
	NEC America	μPB74LS27	
	Raytheon	74LS27	
	Signetics	74LS27	
	TI	SN74LS27	
HD74LS298	Fairchild	74LS298	
	Motorola	SN74LS298	
	Raytheon	74LS298	
	Signetics	74LS298	
	TI	SN74LS298	
HD74LS30	Fairchild	74LS30	
	Motorola	SN74LS30	
	National	DM74LS30	
	NEC America	μPB74LS30	
	Raytheon	74LS30	
	Signetics	74LS30	
	TI	SN74LS30	
HD74LS32	Fairchild	74LS32	
	Motorola	SN74LS32	
	National	DM74LS32	
	NEC America	μPB74LS32	
	Raytheon	74LS32	
	Signetics	74LS32	
	TI	SN74LS32	
HD74LS367	Fairchild	74LS367	
	Motorola	SN74LS367	
	National	DM74LS367	
	NEC America	μPB74LS367	
	Raytheon	74LS367	
HD74LS367	Signetics	74LS367	
HD74LS368	Fairchild	74LS368	
	Motorola	SN74LS368A	
	National	DM74LS368	
	NEC America	μPB74LS368	
	Raytheon	74LS368	
	Signetics	74LS368	
	TI	SN74LS368	
HD74LS37	Fairchild	74LS37	
	Motorola	SN74LS37	
	National	DM74LS37	
	NEC America	μPB74LS37	
	Raytheon	74LS37	
	Signetics	74LS37	
	TI	SN74LS37	
HD74LS38	Fairchild	74LS38	
	Motorola	SN74LS38	
	National	DM74LS38	
	NEC America	μPB74LS38	
	Raytheon	74LS38	
	Signetics	74LS38	
	TI	SN74LS38	
HD74LS386	Motorola	SN74LS386	
	National	DM74LS386	
	Raytheon	74LS386	
	Signetics	74LS386	
	TI	SN74LS386	
HD74LS40	Fairchild	74LS40	
	Motorola	SN74LS40	
	National	DM74LS40	
	NEC America	μPB74LS40	
	Raytheon	74LS40	
	Signetics	74LS40	
	TI	SN74LS40	
HD74LS42	Fairchild	74LS42	
	Motorola	SN74LS42	
	National	DM74LS42	
	NEC America	μPB74LS42	
	Raytheon	74LS42	
	Signetics	74LS42	
	TI	SN74LS42	
HD74LS47	Fairchild	74LS47	
	Motorola	SN74LS47	
	National	DM74LS47	
	TI	SN74LS47	
HD74LS48	Fairchild	74LS48	
	Motorola	SN74LS48	
	National	DM74LS48	
	TI	SN74LS48	
HD74LS49	Fairchild	74LS49	
	Motorola	SN74LS49	
	National	DM74LS49	
	TI	SN74LS49	
HD74LS51	Fairchild	74LS51	
	Motorola	SN74LS51	
	National	DM74LS51	
	NEC America	μPB74LS51	
	Raytheon	74LS51	
	Signetics	74LS51	
	TI	SN74LS51	
HD74LS54	Fairchild	74LS54	
	Motorola	SN74LS54	
	National	DM74LS54	
	NEC America	μPB74LS54	
	Raytheon	74LS54	
	Signetics	74LS54	
	TI	SN74LS54	
HD74LS55	Fairchild	74LS55	
	Motorola	SN74LS55	
	National	DM74LS55	
	NEC America	μPB74LS55	
	Raytheon	74LS55	
	Signetics	74LS55	
	TI	SN74LS55	
HD74LS73	Fairchild	74LS73	
	Motorola	SN74LS73A	
	National	DM74LS73	
	Raytheon	74LS73	
	Signetics	74LS73	
	TI	SN74LS73A	
HD74LS74A	Fairchild	74LS74	
	Motorola	SN74LS74A	
	National	DM74LS74	
	NEC America	μPB74LS74	
	Raytheon	74LS74	
	Signetics	74LS74	

♦ Discontinued

Bold face device numbers indicate manufacturers data is provided in the IC Master on the pages noted.

Hitachi America, Ltd. (cont'd)

Manufacturer Device	Replacement Source	Device	IC Master Page
HD74LS74A	TI	SN74LS74A	
HD74LS76	Fairchild	74LS76	
	Motorola	SN74LS76A	
	National	DM74LS76	
	Raytheon	74LS76	
	Signetics	74LS76	
	TI	SN74LS76	
HD74LS78	Fairchild	74LS78	
	Motorola	SN74LS78A	
	National	DM74LS78	
	Raytheon	74LS78	
	Signetics	74LS78	
	TI	SN74LS78A	
HD74LS86	Fairchild	74LS86	
	Motorola	SN74LS86	
	National	DM74LS86	
	NEC America	μPB74LS86	
	Raytheon	74LS86	
	Signetics	74LS86	
	TI	SN74LS86	
HD74LS92	Fairchild	74LS92	
	Motorola	SN74LS92	
	National	DM74LS92	
	Raytheon	74LS92	
	Signetics	74LS92	
	TI	SN74LS92	
HD74LS95B	Fairchild	74LS95B	
	Motorola	SN74LS95B	
	Raytheon	74LS95B	
	Signetics	74LS95B	
	TI	SN74LS95B	
HD74S00	Fairchild	74S00	
	Hitachi	HD74S00	
	Mitsubishi	M5S000	
	National	DM74S00	
	Signetics	74S00	
	TI	SN74S00	
HD74S03	Fairchild	74S03	
	Mitsubishi	M5S003	
	National	DM74S03	
	Signetics	74S03	
	TI	SN74S03	
HD74S04	Fairchild	74S04	
	Mitsubishi	M5S004	
	National	DM74S04	
	Signetics	74S04	
	TI	SN74S04	
HD74S05	Fairchild	74S05	
	Mitsubishi	M5S005	
	National	DM74S05	
	Signetics	74S05	
	TI	SN74S05	
HD74S10	Fairchild	74S10	
	Mitsubishi	M5S010	
	National	DM74S10	
	Signetics	74S10	
	TI	SN74S10	
HD74S11	Fairchild	74S11	
	Mitsubishi	M5S011	
	National	DM74S11	
	Signetics	74S11	
	TI	SN74S11	
HD74S112	Fairchild	74S112	
	Mitsubishi	M5S112	
	Motorola	SN74S112	
	National	DM74S112	
	Signetics	74S112	
	TI	SN74S112	
HD74S113	Fairchild	74S113	
	Mitsubishi	M5S113	
	Motorola	SN74S113	
	National	DM74S113	
	Signetics	74S113	
	TI	SN74S113	
HD74S114	Fairchild	74S114	
	Mitsubishi	M5S114	
	National	DM74S114	
	Signetics	74S114	
	TI	SN74S114	
HD74S133	Fairchild	74S133	
	Mitsubishi	M5S133	
	National	DM74S133	
	Signetics	74S133	
HD74S133	TI	SN74S133	
HD74S134	Fairchild	74S134	
	National	DM74S134	
	Signetics	74S134	
	TI	SN74S134	
HD74S135	Fairchild	74S135	
	National	DM74S135	
	Signetics	74S135	
	TI	SN74S135	
HD74S140	Fairchild	74S140	
	National	DM74S140	
	Signetics	74S140	
	TI	SN74S140	
HD74S15	Fairchild	74S15	
	Mitsubishi	M5S015	
	National	DM74S15	
	Signetics	74S15	
	TI	SN74S15	
HD74S151	AMD	SN74S151	
	Fairchild	74S151	
	Mitsubishi	M5S151	
	National	DM74S151	
	Signetics	74S151	
	TI	SN74S151	
HD74S174	AMD	SN74S174	
	Fairchild	74S174	
	Mitsubishi	M5S174	
	National	DM74S174	
	Signetics	74S174	
	TI	SN74S174	
HD74S175	AMD	SN74S175	
	Fairchild	74S175	
	Mitsubishi	M5S175	
	National	DM74S175	
	Signetics	74S175	
	TI	SN74S175	
HD74S181	AMD	SN74S181	
	Fairchild	93S41	
	Mitsubishi	M5S181	
	Signetics	74S181	
	TI	SN74S181	
HD74S182	MMI	74S182	
	National	DM74S182	
	Signetics	74S182	
	TI	SN74S182	
HD74S20	Fairchild	74S20	
	Mitsubishi	M5S020	
	National	DM74S20	
	Signetics	74S20	
	TI	SN74S20	
HD74S22	Fairchild	74S22	
	Mitsubishi	M5S22	
	National	DM74S22	
	Signetics	74S22	
	TI	SN74S22	
HD74S251	AMD	SN74S251	
	Fairchild	74S251	
	Mitsubishi	M5S251	
	National	DM74S251	
	Signetics	74S251	
	TI	SN74S251	
HD74S40	Fairchild	74S40	
	Mitsubishi	M5S040	
	National	DM74S40	
	Signetics	74S40	
	TI	SN74S40	
HD74S64	Fairchild	74S64	
	National	DM74S64	
	Signetics	74S64	
	TI	SN74S64	
HD74S65	Fairchild	74S65	
	National	DM74S65	
	Signetics	74S65	
	TI	SN74S65	
HD74S74	Fairchild	74S74	
	Mitsubishi	M5S074	
	TI	SN74S74	
HD74S86	Fairchild	74S86	
	National	DM74S86	
	Signetics	74S86	
	TI	SN74S86	
HD7400	Fairchild	7400	
	Mitsubishi	M53200	
	Motorola	MC7400	
	National	DM7400	
	NEC America	μPB7400	
HD7400	Signetics	7400	
	TI	SN7400	
	Toshiba	TC7400	
	TRW	7400	
HD7402	Fairchild	7402	
	Mitsubishi	M53202	
	Motorola	MC7402	
	National	DM7402	
	NEC America	μPB7402	
	Signetics	7402	
	TI	SN7402	
	TRW	7402	
HD7403	Fairchild	7403	
	Mitsubishi	M53203	
	Motorola	MC7403	
	National	DM7403	
	Signetics	7403	
	TI	SN7403	
	TRW	7403	
HD7404	Fairchild	7404	
	Mitsubishi	M53204	
	Motorola	MC7404	
	National	DM7404	
	NEC America	μPB7404	
	Signetics	7404	
	TI	SN7404	
	Toshiba	TC7404	
	TRW	7404	
HD7405	Fairchild	7405	
	Mitsubishi	M53205	
	Motorola	MC7405	
	National	DM7405	
	NEC America	μPB7405	
	Signetics	7405	
	TI	SN7405	
	TRW	7405	
HD7406	Fairchild	7406	
	Mitsubishi	M53206	
	Motorola	MC7406	
	National	DM7406	
	Signetics	7406	
	TI	SN7406	
	TRW	7406	
HD7407	Fairchild	7407	
	Mitsubishi	M53207	
	Motorola	MC7407	
	National	DM7407	
	Signetics	7407	
	TI	SN7407	
	TRW	7407	
HD7409	Fairchild	7409	
	Mitsubishi	M53209	
	Motorola	MC7409	
	National	DM7409	
	Signetics	7409	
	TI	SN7409	
	TRW	7409	
HD7410	Fairchild	7410	
	Mitsubishi	M53210	
	Motorola	MC7410	
	National	DM7410	
	NEC America	μPB7410	
	Signetics	7410	
	TI	SN7410	
		SN7427	
	Toshiba	TC7410	
	TRW	7410	
HD74107	Fairchild	74107	
	Mitsubishi	M53307	
	Motorola	MC74107	
	National	DM74107	
	NEC America	μPB74107	
	Signetics	74107	
	TI	SN74107	
HD7411	Fairchild	7411	
	National	DM7411	
	Signetics	7411	
HD7412	Fairchild	7412	
	Signetics	7412	
	TI	SN7412	
	TRW	7412	
HD74121	Fairchild	74121	
	Mitsubishi	M53321	
	Motorola	MC74121	
	National	DM74121	
	Signetics	74121	
HD74121	TI	SN74121	
	TRW	74121	
HD74125	Fairchild	74125	
	Mitsubishi	M53325	
	National	DM74125	
	Signetics	74125	
	TI	SN74125	
HD74126	Fairchild	74126	
	Mitsubishi	M53326	
	National	DM74126	
	Signetics	74126	
	TI	SN74126	
HD74132	Fairchild	74132	
	Mitsubishi	M53332	
	Motorola	MC74132	
	National	DM74132	
	Signetics	74132	
	TI	SN74132	
HD74136	Motorola	MC74136	
	TI	SN74136	
	TRW	74136	
HD7414	Fairchild	7414	
	Mitsubishi	M53214	
	Motorola	MC7414	
	National	DM7414	
	Signetics	7414	
	TI	SN7414	
HD74147	Mitsubishi	M53347	
	National	DM74147	
	NEC America	μPB74147	
	Signetics	74147	
	TI	SN74147	
HD74148	Fairchild	9318	
	Mitsubishi	M53348	
	National	DM74148	
	NEC America	μPB74148	
	Signetics	74148	
	TI	SN74148	
HD74150	Fairchild	74150	
	Mitsubishi	M53350	
	Motorola	MC74150	
	National	DM74150	
	NEC America	μPB74150	
	Signetics	74150	
	TI	SN74150	
	TRW	74150	
HD74151	Fairchild	74151	
	Mitsubishi	M53351	
	Motorola	MC74151	
	National	DM74151	
	NEC America	μPB74151	
	Signetics	74151	
	TI	SN74151	
	TRW	74151	
HD74156	Fairchild	74156	
	Mitsubishi	M53356	
	Motorola	MC74156	
	National	DM74156	
	NEC America	μPB74156	
	Signetics	74156	
	TI	SN74156	
	TRW	74156	
HD74157	AMD	SN74157	
	Fairchild	74157	
	Mitsubishi	M53357	
	Motorola	MC74157	
	National	DM74157	
	NEC America	μPB74157	
	Signetics	74157	
	TI	SN74157	
HD7416	Fairchild	7416	
	Mitsubishi	M53216	
	Motorola	MC7416	
	National	DM7416	
	Signetics	7416	
	TI	SN7416	
	TRW	7416	
HD74160	AMD	SN74160	
	Fairchild	74160	
	Mitsubishi	M53360	
	Motorola	MC74160	
	National	DM74160	
	Signetics	74160	
	TI	SN74160	
	TRW	74160	
HD74161	AMD	SN74161	

♦ Discontinued

The manufacturers report their devices can be used as direct replacements.
Performance details often differ, so compare the specifications considering your requirements.

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Manufacturer Device	Replacement Source	Replacement Device	IC Master Page
HD74161	Fairchild	74161	
	Mitsubishi	M53361	
	Motorola	MC74161	
	National	DM74161	
	NEC America	μPB74161	
	Signetics	74161	
	TI	SN74161	
	TRW	74161	
HD74162	AMD	SN74162	
	Fairchild	74162	
	Mitsubishi	M53362	
	Motorola	MC74162	
	National	DM74162	
	Signetics	74162	
	TI	SN74162	
	TRW	74162	
HD74163	AMD	SN74163	
	Fairchild	74163	
	Mitsubishi	M53363	
	Motorola	MC74163	
	National	DM74163	
	Signetics	74163	
	TI	SN74163	
	TRW	74163	
HD74164	AMD	74164	
	Fairchild	74164	
	Mitsubishi	M53364	
	National	DM74164	
	NEC America	μPB74164	
	Signetics	74164	
	TI	SN74164	
HD74166	Fairchild	74166	
	Mitsubishi	M53366	
	National	DM74166	
	Signetics	74166	
	TI	SN74166	
HD7417	Fairchild	7417	
	Mitsubishi	M53217	
	Motorola	MC7417	
	National	DM7417	
	Signetics	7417	
	TI	SN7417	
	TRW	7417	
HD74174	AMD	SN74174	
	Fairchild	74174	
	Mitsubishi	M53374	
	Motorola	MC74174	
	National	DM74174	
	Signetics	74174	
	TI	SN74174	
HD74175	AMD	SN74175	
	Fairchild	74175	
	Mitsubishi	M53375	
	Motorola	MC74175	
	National	DM74175	
	NEC America	μPB74175	
	Signetics	74175	
	TI	SN74175	
HD74180	Fairchild	74180	
	Mitsubishi	M53380	
	Motorola	MC74180	
	National	DM74180	
	NEC America	μPB74180	
	Signetics	74180	
	TI	SN74180	
	TRW	74180	
HD74190	Fairchild	74190	
	Mitsubishi	M53390	
	Motorola	MC74190	
	National	DM74190	
	Signetics	74190	
	TI	SN74190	
HD74191	Fairchild	74191	
	Mitsubishi	M53391	
	Motorola	MC74191	
	National	DM74191	
	Signetics	74191	
	TI	SN74191	
HD74194	AMD	SN74194	
	Fairchild	74194	
	Motorola	MC74194	
	National	DM74194	
	Signetics	74194	
HD74194	TI	SN74194	
HD74198	Fairchild	74198	
	Mitsubishi	M53398	
	National	DM74198	
	NEC America	μPB74198	
	Signetics	74198	
	TI	SN74198	
HD7420	Fairchild	7420	
	Mitsubishi	M53220	
	Motorola	MC7420	
	National	DM7420	
	NEC America	μPB7420	
	Signetics	7420	
	TI	SN7420	
	Toshiba	TC7420	
	TRW	7420	
HD7422	Fairchild	7422	
	TI	SN7422	
HD7426	Fairchild	7426	
	Motorola	MC7426	
	National	DM7426	
	Signetics	7426	
	TI	SN7426	
	TRW	7426	
HD7427	Fairchild	7427	
	Mitsubishi	M53227	
	Motorola	MC7427	
	National	DM7427	
	Signetics	7427	
HD7430	Fairchild	7430	
	Mitsubishi	M53230	
	Motorola	MC7430	
	National	DM7430	
	NEC America	μPB7430	
	Signetics	7430	
	TI	SN7430	
	TRW	7430	
HD7432	Fairchild	7432	
	National	DM7432	
	Signetics	7432	
	TI	SN7432	
HD7440	Fairchild	7440	
	Mitsubishi	M53240	
	Motorola	MC7440	
	National	DM7440	
	NEC America	μPB7440	
	Signetics	7440	
	TI	SN7440	
	TRW	7440	
HD7442	Fairchild	7442	
	Mitsubishi	M53242	
	Motorola	MC7442	
	National	DM7442	
	NEC America	μPB7442	
	Signetics	7442	
	TI	SN7442	
HD7443	Fairchild	7443	
	Mitsubishi	M53243	
	Motorola	MC7443	
	Signetics	7443	
	TI	SN7443	
HD7444	Fairchild	7444	
	Mitsubishi	M53244	
	Motorola	MC7444	
	Signetics	7444	
	TI	SN7444	
HD7450	Fairchild	7450	
	Mitsubishi	M53250	
	Motorola	MC7450	
	National	DM7450	
	NEC America	μPB7450	
	Signetics	7450	
	TI	SN7450	
	TRW	7450	
HD7451	Fairchild	7451	
	Motorola	MC7451	
	National	DM7451	
	NEC America	μPB7451	
	Signetics	7451	
	TI	SN7451	
	TRW	7451	
HD7453	Fairchild	7453	
	Mitsubishi	M53253	
	Motorola	MC7453	
	National	DM7453	
	NEC America	μPB7453	
HD7453	Signetics	7453	
	TI	SN7453	
	TRW	7453	
HD7454	Fairchild	7454	
	Motorola	MC7454	
	National	DM7454	
	NEC America	μPB7454	
	Signetics	7454	
	TI	SN7454	
	TRW	7454	
HD7460	Fairchild	7460	
	Mitsubishi	M53260	
	Motorola	MC7460	
	National	DM7460	
	NEC America	μPB7460	
	Signetics	7460	
	TI	SN7460	
	TRW	7460	
HD7472	Fairchild	7472	
	Mitsubishi	M53272	
	Motorola	MC7472	
	National	DM7472	
	Signetics	7472	
	TI	SN7472	
	TRW	7472	
HD7474	Fairchild	7474	
	Mitsubishi	M53274	
	Motorola	MC7474	
	National	DM7474	
	NEC America	μPB7474	
	Signetics	7474	
	TI	SN7474	
	TRW	7474	
HD7475	Fairchild	7475	
	Mitsubishi	M53275	
	Motorola	MC7475	
	National	DM7475	
	Signetics	7475	
	TI	SN7475	
	TRW	7475	
HD7485	Fairchild	7485	
	Mitsubishi	M53285	
	Motorola	MC7485	
	National	DM7485	
	NEC America	μPB7485	
	Signetics	7485	
	TI	SN7485	
	TRW	7485	
HD7486	Fairchild	7486	
	Mitsubishi	M53286	
	Motorola	MC7486	
	National	DM7486	
	NEC America	μPB7486	
	Signetics	7486	
	TI	SN7486	
	TRW	7486	
HD7490	Fairchild	7490	
	Mitsubishi	M53290	
	Motorola	MC7490	
	National	DM7490	
	Signetics	7490	
	TI	SN7490	
	TRW	7490	
HD7492	Fairchild	7492	
	Mitsubishi	M53292	
	Motorola	MC7492	
	National	DM7492	
	Signetics	7492	
	TI	SN7492	
	TRW	7492	
HD7493	Fairchild	7493	
	Mitsubishi	M53293	
	Motorola	MC7493	
	National	DM7493	
	Signetics	7493	
	TI	SN7493	
	TRW	7493	
HD7496	Fairchild	7496	
	Mitsubishi	M53296	
	Motorola	MC7496	
	National	DM7496	
	Signetics	7496	
	TI	SN7496	
	TRW	7496	
HM2101	Fairchild	3538	
HM2105	Fujitsu	MBM10410	
HM2114	TI	TMS4045	
HM2510	Fujitsu	MBM93415	
HM4704	Fujitsu	MB8227	
HM4711	Fujitsu	MB8107	
HM4716	Fujitsu	MB8116	
SN74LS283	Fairchild	74LS283	
	Motorola	SN74LS283	
	National	DM74LS283	
	Raytheon	74LS283	
	TI	SN74LS283	
SN74LS367	TI	SN74LS367	
74LS15	Raytheon	74LS15	
	Signetics	74LS15	
	TI	SN74LS15	
74LS156	Raytheon	74LS156	
	Signetics	74LS156	
	TI	SN74LS156	

Hughes Aircraft, Solid State Products

HCMP159	SSS	SCP1859
HCMP1802	RCA	CDP1802
	SSS	SCP1802
HCMP1822	RCA	CDP1822
	SSS	SCP1822
HCMP1824	RCA	CDP1824
	SSS	SCP1824
HCMP1831	RCA	CDP1831
	SSS	SCP1831
HCMP1832	RCA	CDP1832
	SSS	SCP1832
HCMP1833	RCA	CDP1833
	SSS	SCP1833
HCMP1834	RCA	CDP1834
	SSS	SCP1834
HCMP1852	RCA	CDP1852
	SSS	SCP1852
HCMP1853	RCA	CDP1853
	SSS	SCP1853
HCMP1854	RCA	CDP1854
	SSS	SCP1854
HCMP1856	RCA	CDP1856
	SSS	SCP1856
HCMP1857	RCA	CDP1857
	SSS	SCP1857
HCMP1858	RCA	CDP1858
	SSS	SCP1858
HCMP1859	RCA	CDP1859
	SSS	SCP1859

Hybrid Systems

ADC-581	Micro Net	MNADC84
		MNADC85
ADC581	Micro Net	MNADC84
		MNADC85
ADC586-10	Teledyne S	8701
ADC586-12	Teledyne S	8702
ADC586-8	Teledyne S	8700

Intel

♦M3601	AMD	AM27S20
1101	AMD	1101
	Mostek	MK4007
	National	MM1101
1103	AMI	S146
	Fairchild	1103
	Hitachi	HM3503
	Nortec	1103
	Rockwell	1103
	Signetics	1103
	Synertek	SY1103
1103A	AMI	S1103
	Synertek	1103
♦1301	AMI	S8773
♦1302	GI	R05-1302
♦1402	AMD	1402
	Hitachi	HD3502
	National	MM1402
	Nortec	1402
	Synertek	SY1402

♦ Discontinued

Bold face device numbers indicate manufacturers data is provided in the IC Master on the pages noted.

Intel (cont'd)

Manufacturer Device	Replacement Source	Device	IC Master Page
♦1403	AMD	1403	
	Hitachi	HD3503	
	National	MM1403	
	Nortec	1403	
	Synertek	SY1403	
♦1404	AMD	1404	
	Hitachi	HD3504	
	National	MM1404	
	Nortec	1404	
	Synertek	SY1404	
♦1405	AMD	1405	
	Hitachi	HD3505	
♦1406	AMD	1406	
♦1407	AMD	1407	
♦1506	AMD	1506	
	Hitachi	HD3506	
♦1507	AMD	1507	
	Hitachi	HD3507	
♦1702	AMD	1702	
	Hitachi	HN351702	
	Mitsubishi	M5L1702	
	National	MM1702	
	Signetics	1702	
2101	AMD	2101	
	EA	EA2101	
	Fairchild	3538	
	Harris	**HM6501**	**1356**
	Hitachi	HM2101	
	Mitsubishi	M5L2101	
	National	MM2101	
	NEC Micro	**μPD2101**	**1586**
	RCA	CDP1822	
	Signetics	2101	
	Synertek	SY2101	
2102	AMD	2102	
		9102	
	EA	EA2102	
	Fairchild	**21L02**	**1275**
		2102	**1275**
		3542	
	Mitsubishi	M5L2102	
	National	MM2102	
	NEC Micro	**μPD2102**	**1591**
	RCA	CDP1821	
	SGS	M330	
	Signetics	2102	
	Synertek	SY2102	
	Toshiba	TMM313	
2104	Fairchild	M4027	
		4096	
	Mitsubishi	M5L2104	
	Mostek	MK4027	
		MK4096	
	Signetics	**4027**	**1677**
2104A	Fujitsu	MB8227	
	Intersil	IM7027	
		MK4027	
	TI	TMS4027	
2107	AMD	90L60	
	Fujitsu	MB8107	
	Hitachi	HM4711	
	Mitsubishi	M5L2107	
	National	**MM5280**	**270**
	NEC Micro	**μPD411**	**1547**
	TI	TMS4060	
2107B	TI	TMS4060	
2111	AMD	2111	
	EA	EA2111	
	Mitsubishi	M5L2111	
	National	MM2111	
	NEC Micro	**μPD2111**	**1595**
	Signetics	2111	
	Synertek	SY2111	
	Toshiba	TMM311	
2112	AMD	2112	
	EA	EA2112	
	Mitsubishi	M5L2112	
	National	MM2112	
	Signetics	2112	
	Synertek	SY2112	
	Toshiba	TMM312	
2114	AMD	9114	
		9124	
2114	**AMI**	**S2114**	**1196**
	EMM/Semi	**2114**	**1222**
	Fairchild	**2114**	**1281**
	Fujitsu	MB8114	
	Harris	**HM6514**	**1376**
	Hitachi	HM472114	
	Intersil	1M7114	
	Mitsubishi	**M5L2114L**	**1438**
	Motorola	**MCM2114**	**1528**
	NEC Micro	**μPD2114**	**1604**
	Rockwell	R2114	
	Signetics	**2614**	**1669**
	Synertek	SY2114	
	TI	TMS40L45	
		TMS4045	
	Toshiba	TMM314	
		TMM314A	
2115	**AMI**	**S4015**	**1203**
	NEC Micro	**μPD2114**	**1604**
2116	AMD	9016	
	Fairchild	**F16K**	**1272**
	Fujitsu	MBM8116	
	Intersil	MK4116	
	Mostek	MK4116	
	Motorola	**MCM4116**	**1505**
	NEC Micro	**μPD416**	**1562**
	TI	TMS4116	
	Toshiba	TM323	
2117	AMD	9016	
	Fujitsu	MBM8116	
		MB8116	
	Mostek	MK4116	
	NEC Micro	**μPD416**	**1562**
	Zilog	Z6116	
2125	**AMI**	**S4025**	**1203**
	Harris	**HM6508**	**1366**
	NEC Micro	μPD2125	
2141	AMD	4044	
	Fujitsu	MBM4044	
2146	AMI	S146	
2147	AMD	2147	
	AMI	**S2147**	**1200**
		S4017	**1204**
	Fujitsu	MBM2147	
	NEC Micro	**μPD2147**	**1609**
	Synertek	SY2147	
	Toshiba	TMM315	
2148	**AMI**	**S2114**	**1196**
♦2308	EA	EA2308	
	Fairchild	3508	
	Mostek	MK30000	
	NEC Micro	μPD2308	
	Signetics	2607	
	TI	TMS4700	
2316	EA	2316	
	Fairchild	3516E	
	GI	RO3-8316	
	Mostek	MK31000	
		MK34000	
	Motorola	MCM68316	
	NEC Micro	μPD2316	
	Rockwell	R2316	
2316A	**AMI**	**S6831A**	**1215,1806**
	NEC Micro	μPD2316A	
	Toshiba	TMM331	
2316E	**AMI**	**S4216B**	**1209**
		S6831B	**1215,1806**
	Toshiba	TMM334	
2401	Mitsubishi	M5G2401	
♦2401	Synertek	SY2401	
2416	Synertek	SY2416	
2704	RCA	CDP1832	
2708	AMD	2708	
	EA	EA2708	
	Fairchild	**2708**	**1282**
	Fujitsu	MB8518	
	Hitachi	HN462708	
	Mitsubishi	**M5L2708**	**1441**
	Motorola	MCM2708	
		MC27A08	
		MC2708	
	National	MM2708	
	TI	TMS2708	
	Toshiba	TMM322	
2716	**AMI**	**S4716**	**1220**
	Fujitsu	MBM2716	
	Hitachi	HN4716	
	NEC Micro	**μPD2716**	**1617**
	Synertek	SY2716	
	TI	TMS2516	
	Toshiba	TMM323	
3001	Signetics	N3001	
3002	Signetics	N3002	
3101	AMD	AM27S02	
		3101	
	MMI	27S02	
		5560	
		6560	
	National	MM54S289	
		MM74S289	
	Signetics	**N82S25**	**1678**
		3101	
	TI	SN54S289	
		SN74S289	
♦3106	**Fairchild**	**93421**	**1252**
	MMI	6531	
	National	MM74S200	
	Raytheon	RC5340	
		RM5340	
	Signetics	**N82S16**	**1678**
	TI	SN54S200A	
		SN54S201	
		SN74S200A	
		SN74S201	
♦3107	Fairchild	93411	
	MMI	5530	
		6530	
	National	MM74S206	
	Raytheon	RC5330	
		RM5330	
	Signetics	**N82S17**	**1678**
		74S01	
		82S17	
	TI	SN54S300	
		SN54S301	
		SN74S300	
		SN74S301	
♦3110	TI	SN74S214	
		SN74S314	
3207	NEC Micro	μPD246	
	Signetics	3207	
3212	AMD	3212	
	TI	SN54S412	
		SN74S412	
3216	AMD	3216	
3226	AMD	3226	
3232	Motorola	MC3232	
		MC3232A	
3242	Motorola	MC3242A	
3245	Motorola	MC3245	
	National	DS3245	
♦3301	AMD	SN74186	
	Intersil	IM5603	
	MMI	**5200-1**	**1466**
	TI	SN54187	
		SN74187	
♦3304	Signetics	8205	
♦3601	AMD	AM27S20	
	Fairchild	**93417**	**1258**
	Harris	**HM7610**	**1284,1292**
		HPROM1024A	
	Intersil	IM5603	
	MMI	**5300-1**	**1449**
		6300-1	**1449**
	National	DM54S387	
		DM74S387	
	NEC Micro	μPB403	
	Raytheon	**29660**	**1664**
	Signetics	**N82S126**	**1680**
	TI	**SN54S387**	**1708**
		SN74S387	**1708**
3602	AMD	AM27S12	
	Fairchild	**93436**	**1260**
	Harris	**HM7620**	**1284,1298**
	MMI	**5305-1**	**1449**
		6305-1	**1449**
	National	DM54S570	
		DM74S570	
3602	**Raytheon**	**29610**	**1654**
	Signetics	82S130	
	TI	**SN54S475**	**1708**
		SN74S475	**1708**
3602A	**MMI**	**5305-1**	**1449**
		5306-1	**1449**
		6305-1	**1449**
		6306-1	**1449**
3604	**Harris**	**HM7640**	**1284,1304**
	MMI	**5340-1**	**1449**
		6340-1	**1449**
	National	DM77S295	
		DM87S295	
		SN54S475	
		SN74S475	
	NEC Micro	**μPB405**	**1621**
	Raytheon	**29624**	**1658**
	Signetics	**N82S140**	**1680**
3604A	**Fairchild**	**93438**	**1262**
	MMI	**5340-1**	**1449**
		6340-1	**1449**
	NEC Micro	**μPB405**	**1621**
3605	**Harris**	**HM7642**	**1284,1308**
	MMI	**5352-1**	**1449**
		6352-1	**1449**
	National	DM54S572	
		DM74S572	
	NEC Micro	**μPB406**	**1625**
	Raytheon	29640	
3605A	**Fairchild**	**93452**	**1264**
	NEC Micro	**μPB406**	**1625**
3608	**Harris**	**HM7680**	**1322**
	MMI	**5380-1**	**1449**
		6380-1	**1449**
	Raytheon	**29630**	**1660**
3616	**MMI**	**53S1680**	**1453**
		63S1680	**1453**
3621	AMD	AM27S21	
	Fairchild	**93427**	**1258**
	Harris	**HM7611**	**1284,1292**
	MMI	**5301-1**	**1449**
		6301-1	**1449**
	National	DM54S287	
		DM74S287	
	Raytheon	**29661**	**1664**
	TI	**SN54S287**	**1708**
		SN74S287	**1708**
3622	AMD	AM27S13	
	Fairchild	**93446**	**1260**
	Harris	**HM7621**	**1284,1298**
	MMI	**5306-1**	**1449**
		6306-1	**1449**
	National	DM54S571	
		DM74S571	
	Raytheon	**29611**	**1654**
	Signetics	82S131	
3624	**Harris**	**HM7641**	**1284,1304**
	MMI	**5341-1**	**1449**
		6341-1	**1449**
	National	DM77S296	
		DM87S296	
		SN54S474	
		SN74S474	
	NEC Micro	**μPB425**	**1621**
	Raytheon	**29625**	**1658**
	Signetics	**N82S141**	**1680**
3624A	**Fairchild**	**93448**	**1262**
	MMI	**5341-1**	**1449**
		6341-1	**1449**
	NEC Micro	**μPB425**	**1621**
3625	**Harris**	**HM7643**	**1284,1308**
	MMI	**5353-1**	**1449**
		6353-1	**1449**
		6363-1	
	National	DM54S573	
		DM74S573	
	NEC Micro	**μPB426**	**1625**
	Raytheon	29641	
	Signetics	**N82S137**	**1680**
		S82S137	**1680**

♦ Discontinued

The manufacturers report their devices can be used as direct replacements.
Performance details often differ, so compare the specifications considering your requirements.

Intel (cont'd)

Manufacturer Device	Replacement Source	Device	IC Master Page
3625A	**Fairchild**	**93453**	**1264**
	NEC Micro	**μPB426**	**1625**
3628	**Harris**	**HM7681**	**1322**
	MMI	5381	
		6381	
		6381-1	**1449**
	National	DM77S228	
	Raytheon	**29631**	**1660**
	Signetics	**N82S181**	**1680**
3636	**MMI**	**53S1681**	**1453**
		63S1681	**1453**
4001	**Harris**	**HM7621**	**1284,1298**
	Hitachi	HN35600	
	National	INS4001	
4002	National	INS4002	
4003	National	INS4003	
4004	National	INS4004	
4008	National	INS4008	
4009	National	INS4009	
4201	National	DP4201	
4308	Hitachi	HN35800	
4702	AMD	4702	
5101	**AMI**	**S5101**	**1206**
		S6831B	**1215,1806**
	Harris	**HM6501**	**1356**
	Hitachi	HM435101	
	Motorola	**MCM145101**	**1536**
	NEC Micro	**μPD5101**	**1562**
	SSS	SCM5101	
	Synertek	SY5101	
	Toshiba	TC5501	
5201	SSS	SCL5424	
5801	SSS	SCL5437	
8021	**NEC Micro**	**μPD8021**	**2085**
	Signetics	8021	
8035	AMD	8035	
	NEC Micro	**μPD8035**	**2098**
8039	**NEC Micro**	**μPD8039**	**2104**
8041	AMD	8041	
	NEC Micro	**μPD8041**	**2090**
8048	AMD	8048	
	NEC Micro	**μPD8048**	**2098**
	Signetics	**8048**	**2310**
8049	**NEC Micro**	**μPD8049**	**2104**
8080A	AMD	9080	
	Mitsubishi	M5L8080A	
	National	**INS8080A**	**238**
	NEC Micro	**μPD8080A**	**2119**
		μPD8080AF	**2119**
	TI	TMS8080A	
8085A	AMD	8085A	
	Mitsubishi	M5L8085A	
	NEC Micro	**μPD8085A**	**2133**
8101	**NEC Micro**	**μPD2101**	**1586**
8101A	**NEC Micro**	**μPD2101**	**1586**
8102	**NEC Micro**	**μPD2102**	**1591**
8102A	**NEC Micro**	**μPD2102**	**1591**
8111	**NEC Micro**	**μPD2111**	**1595**
8155	AMD	8155	
	NEC Micro	**μPD8155**	**2164**
8156	AMD	8156	
	NEC Micro	**μPD8156**	**2164**
8212	AMD	8212	
	Mitsubishi	M5L8212	
	National	DP8212	
	NEC Micro	**μPB8212**	**2172**
		μPD8212	
	TI	SN54S412	
		SN74S412	
8214	**NEC Micro**	**μPB8214**	**2178**
8216	AMD	8216	
	Mitsubishi	M5L8216	
	NEC Micro	**μPB8216**	**2184**
8224	AMD	8224	
	Mitsubishi	M5L8224	
	National	DP8224	
	NEC Micro	**μPB8224**	**2188**
	TI	SN74LS424	
8226	AMD	8226	
	Mitsubishi	M5L8226	
	NEC Micro	**μPB8226**	**2184**
8228	AMD	8228	
	Mitsubishi	M5L8228	
	National	DP8228	
	NEC Micro	**μPB8228**	**2193**
	TI	SN74S428	
		TIM8228	
8238	AMD	8238	
	National	DP8238	
	NEC Micro	**μPB8238**	**2193**
		μPD8238	
	TI	SN74S438	
		TIM8238	
8243	AMD	8243	
	Signetics	**8243**	**2313**
8251	AMD	8251	
		9551	
	National	DP8251	
	NEC Micro	μPB8251	
		μPD8251	**2204**
	Western	TR1953	
8251A	**NEC Micro**	**μPD8251A**	**2204**
8253	AMD	8253	
	NEC Micro	**μPD8253**	**2221**
8253-5	AMD	8253-5	
8255	AMD	8255	
		9555	
	Mitsubishi	M5L8255	
	National	DP8255	
	NEC Micro	μPD8225	
		μPD8255	**2229**
8255A	AMD	8255A	
	NEC Micro	μPD8255A	
8255A-5	AMD	8255A-5	
8257	AMD	8257	
	NEC Micro	**μPD8257**	**2236**
8259	**NEC Micro**	**μPD8259**	**2244**
8279	AMD	8279	
	Mitsubishi	M5L8279	
	NEC Micro	**μPD8279**	**2260**
8279-5	AMD	8279-5	
8300	National	DP8300	
8302	National	DP8302	
8304	National	DP8304	
8308	AMD	9208	
	EA	EA8308	
	Mostek	MK30000	
	TI	TMS4700	
8316	**AMI**	**S6831**	**1215,1806**
	EA	EA8316	
	GI	RO3-8316	
	Mostek	MK31000	
		MK34000	
	NEC Micro	μPD2316	
	Supertex	**CM3200**	**1706**
	Synertek	SY2316	
8316A	AMD	8316A	
	AMI	**S6831A**	**1215,1806**
	EA	EA8316A	
	NEC Micro	μPB2316A	
	Synertek	SY2316A	
8316B	**AMI**	**S6831B**	**1215,1806**
	EA	EA8316B	
	NEC Micro	μPB2316B	
	Synertek	SY2316B	
8316E	**AMI**	**S4216B**	**1209**
		S6831B	**1215,1806**
8355	AMD	8355	
	NEC Micro	**μPD8355**	**2269**
8702	AMD	8702	
8741	**NEC Micro**	**μPD8741**	**2090**
8748	**NEC Micro**	**μPD8748**	**2098**
8755A	**NEC Micro**	**μPD8755A**	**2269**

Interdesign

MCA	Master Logic	MCA	
MCB	Master Logic	MCB	
MCC	Master Logic	MCC	
MCD	Master Logic	MCD	
MOE	Cherry	MOE	
MOF	Cherry	MOF	

International Microcircuits, Inc.

MASTER MOS Monosil		Master MOS

Intersil

DG111	Siliconix	DGM111	
DG116	Siliconix	DG116	
DG118	Siliconix	DG172	
DG123	Siliconix	DG123	
DG125	Siliconix	DG125	
DG126	Siliconix	DG126	
DG129	Siliconix	DG129	
DG133	Siliconix	DG133	
DG134	Siliconix	DG134	
DG139	Siliconix	DG139	
DG140	Siliconix	DG140	
DG141	Siliconix	DG141	
DG142	Siliconix	DG142	
DG143	Siliconix	DG143	
DG144	Siliconix	DG144	
DG145	Siliconix	DG145	
DG146	Siliconix	DG146	
DG151	Siliconix	DG151	
DG152	Siliconix	DG152	
DG153	Siliconix	DG153	
DG154	Siliconix	DG154	
DG161	Siliconix	DG161	
DG162	Siliconix	DG162	
DG163	Siliconix	DG163	
DG164	Siliconix	DG164	
DG182	Siliconix	DG182	
DG185	Siliconix	DG185	
DG188	Siliconix	DG188	
DG191	Siliconix	DG191	
DG426	Siliconix	DG126	
DG464	Siliconix	DG164	
D123	Siliconix	D123	
D125	Siliconix	D125	
G115	Siliconix	G115	
G116	Siliconix	G116	
G117	Siliconix	G117	
G118	Siliconix	G118	
G119	Siliconix	G119	
G123	Siliconix	G123	
G125	Siliconix	G125	
G126	Siliconix	G126	
G127	Siliconix	G127	
G128	Siliconix	G128	
G129	Siliconix	G129	
G130	Siliconix	G130	
G131	Siliconix	G131	
G132	Siliconix	G132	
HA2505	**Datel**	**AM-450-2**	**687**
HA2525	**Datel**	**AM-450-2**	**687**
ICL8007	AD	AD8007	
ICL8013	AD	AD530	
		AD533	
	Burr-Brown	4201	
ICL8021	**Harris**	**HA-2720**	**990**
ICL8038	Exar	XR8038	
♦ICL8101	RCA	CA748	
♦ICL8201	RCA	CA748	
IH5009	**National**	**AH5009**	**1073**
IH5010	National	AH5010	
IH5040	**Harris**	**HI5040**	**696**
IH5041	**Harris**	**HI5041**	**696**
IH5042	**Harris**	**HI5042**	**696**
	Siliconix	DG188	
IH5043	Siliconix	DG191	
IH5044	Harris	HI5044	696
IH5045	**Harris**	**HI5045**	**696**
	Siliconix	DG185	
IH5046	**Harris**	**HI5046**	**696**
IH5047	**Harris**	**HI5047**	**696**
IH5048	Siliconix	DG181	
IH5049	**Harris**	**HI5049**	**696**
	Siliconix	DG184	
IH5050	**Harris**	**HI5050**	**696**
	Siliconix	DG187	
IH5051	Harris	HI5051	696
	Siliconix	DG190	
IH5060	Harris	HI506	
IH5070	AD	AD7507	
	Harris	HI507	
	Siliconix	DG507	
IM55S08	Fujitsu	MBM93415	
♦IM55S08	TI	SN54S314	
		SN74S314	
♦IM55S18	TI	SN54S214	
		SN74S214	
		SN74S314	
♦IM5501	AMD	IM5501	
	MMI	5560	
		6560	
	Signetics	**N82S25**	**1678**
	TI	SN54S289	
		SN74S289	
♦IM5502	TI	SN54S81A	
		SN5481A	
♦IM5503	MMI	6531	
	Signetics	**N82S17**	**1678**
		74S301	**1678**
	TI	SN54S300	
		SN54S301	
		SN74S300	
		SN74S301	
♦IM5508	**Fairchild**	**93415**	**1240**
	TI	SN54S314	
		SN54214	
		SN74S314	
		SN7481A	
♦IM5512	TI	SN5481A	
♦IM5523	**Fairchild**	**93421**	**1252**
	MMI	5531	
		6531	
	National	MM74S200	
	Raytheon	RC5340	
		RC5540	
		RM5340	
	Signetics	**N82S16**	**1678**
		S82S16	**1678**
	TI	SN54S201	
		SN54200A	
		SN74S201	
		SN74200A	
♦IM5533	Fairchild	93411	
	MMI	5530	
		6530	
	National	MM74S206	
	Raytheon	RC5330	
		RM5330	
	Signetics	**N82S17**	**1678**
	TI	SN54S301	
		SN74S300	
		SN74S301	
♦IM5543	**Fairchild**	**93421**	**1252**
	TI	SN54S301	
		SN54S475	**1708**
		SN74S301	
		SN74S475	**1708**
♦IM5553	Fairchild	93411	
	TI	SN54S200	
		SN74S200	
IM56S03	AMD	AM27S20	
IM56S04	AMD	AM27C12	
		AM27S12	
IM56S06	**Fairchild**	**93452**	**1264**
	Raytheon	29640	
IM56S23	AMD	AM27S21	
IM56S24	AMD	AM27S13	
IM56S26	**Fairchild**	**93453**	**1264**
	Raytheon	29641	
IM5600	AMD	AM27S18	
♦IM5600	Harris	HPROM8256	
	MMI	**5330-1**	**1449**
		6330-1	**1449**
	National	DM7577	
		DM8577	
	Signetics	**N82S23**	**1680**
	TI	**SN54S188**	**1708**
		SN74S188	**1708**
♦IM5602	**TI**	**SN54S475**	**1708**
		SN74S475	**1708**
IM5603	AMD	AM27S20	
	Fairchild	93416	
		93417	**1258**
	Harris	HPROM1624	
	MMI	**5300-1**	**1449**

♦ Discontinued

Bold face device numbers indicate manufacturers data is provided in the IC Master on the pages noted.

Intersil (cont'd)

Manufacturer Device	Replacement Source	Device	IC Master Page
IM5603	**MMI**	**6300-1**	**1449**
	NEC Micro	μPB403	
	Raytheon	**29660**	**1664**
	Signetics	**N82S126**	**1680**
		S82S126	**1680**
		82S126	
	TI	**SN54S387**	**1708**
		SN74S387	**1708**
IM5604	AMD	AM27C12	
		AM27S12	
	Fairchild	**93436**	**1260**
	Harris	**HM7620**	
			1284,1298
	Intel	3602	
	MMI	**5305-1**	**1449**
		6305-1	**1449**
	National	DM54S570	
		DM74S570	
	Raytheon	**29610**	**1654**
	Signetics	**N82S130**	**1680**
	TI	SN54S270	
		SN74S270	
IM5605	**Harris**	**HM7640**	
			1284,1304
	Intel	3604	
	MMI	**5340-1**	**1449**
		6340-1	**1449**
	National	DM77S295	
		DM87S295	
	NEC Micro	**μPB405**	**1621**
	Raytheon	**29624**	**1658**
	TI	**SN54S475**	**1708**
		SN74S475	**1708**
IM5606	**Fairchild**	**93438**	**1262**
	MMI	**5352-1**	**1449**
		6352-1	**1449**
	National	DM54S572	
		DM74S572	
	NEC Micro	**μPB406**	**1625**
IM5608	**MMI**	**5380-1**	**1449**
		6380-1	**1449**
IM5610	AMD	AM27S19	
	Harris	**HM7603**	**1284**
	MMI	**5331-1**	**1449**
		6331-1	**1449**
	National	DM7578	
		DM8578	
	Signetics	**N82S123**	**1680**
	TI	**SN54S288**	**1708**
		SN74S288	**1708**
IM5618	**MMI**	**5381-1**	**1449**
		6381-1	**1449**
IM5623	AMD	AM27S21	
	Fairchild	93426	
	Harris	HPROM1024	
	Intel	3621	
	MMI	**5301-1**	**1449**
		6301-1	**1449**
	Raytheon	**29661**	**1664**
	Signetics	**N82S129**	**1680**
	TI	**SN54S287**	**1708**
		SN74S287	**1708**
IM5623A	**Fairchild**	**93427**	**1258**
IM5624	AMD	AM27S13	
	Fairchild	**93446**	**1260**
	Harris	**HM7621**	
			1284,1298
	Intel	3622	
	MMI	**5306-1**	**1449**
		6306-1	**1449**
	National	DM54S571	
		DM74S571	
	Raytheon	**29611**	**1654**
	Signetics	**N82S131**	**1680**
	TI	SN54S370	
		SN74S370	
IM5625	**Fairchild**	**93448**	**1262**
	Harris	**HM7641**	
			1284,1304
	Intel	3624	
	MMI	**5341-1**	**1449**
		6341-1	**1449**
	National	DM77S296	
IM5625	National	DM87S296	
	NEC Micro	**μPB425**	**1621**
	Raytheon	**29625**	**1658**
	TI	**SN54S474**	**1708**
		SN74S474	**1708**
IM5626	**MMI**	**5353-1**	**1449**
		6353-1	**1449**
	National	DM54S573	
		DM74S573	
IM6002	TI	TMS4062	
IM6100	**Harris**	**HM6100**	
			1918,1923
IM6100A	**Harris**	**HM6100A**	**1918**
IM6100C	**Harris**	**HM6100C**	**1918**
IM6101	Harris	HD6101	
IM6101A	Harris	HD6101A	
IM6101C	Harris	HD6101C	
IM6312	**Harris**	**HM6312**	**1348**
IM6402	Harris	HD6402	
	RCA	CDP1854	
IM6402A	Harris	HD6402A	
IM6402C	Harris	HD6402C	
IM6403A	Harris	HD6403A	
IM6508	**AMI**	**S6508**	**1207**
	Fairchild	F4736	
	Harris	**HM6508**	**1366**
	National	MM74C929	
	NEC Micro	**μPD6508**	**1562**
IM6508C	Harris	HM6508C	
IM6518	**AMI**	**S6518**	**1208**
	Harris	**HM6518**	**1379**
	National	MM74C930	
IM6523	National	MM74C200	
	RCA	CD4061	
IM6551	Fairchild	F4721	
	Harris	**HM6551**	**1389**
	National	MM74C920	
IM6561	**Harris**	**HM6561**	**1389**
IM6900	Harris	HM6900	
IM7001	RCA	MW7001	
IM7027	Fairchild	M4027	
	Mostek	MK4027	
	TI	TMS4027	
IM7051	AMD	1101	
IM7114	AMD	9114	
		9124	
	AMI	**S2114**	**1196**
	Fairchild	**2114**	**1281**
	Fujitsu	MB8114	
	Intel	2114	
	Motorola	**MCM2114**	**1528**
	National	MM2114	
	NEC Micro	**μPD2114**	**1604**
	Rockwell	R2114	
	Signetics	**2614**	**1669**
	TI	TMS4045	
IM7116	AMD	9016	
	Fujitsu	MBM8116	
		MB8116	
	Intel	2116	
	Mostek	MK4116	
	Motorola	**MCM4116**	**1505**
	NEC Micro	**μPD416**	**1562**
	TI	TMS4116	
	Zilog	Z6116	
IM7141	AMD	4044	
	Fujitsu	MBM4044	
	Intel	**2141**	**1418**
	National	MM5257	
	Signetics	**2613**	**1668**
	TI	TMS4044	
♦IM7210	AMI	S2733	
♦IM7270	National	MM5270	
♦IM7271	National	MM5271	
♦IM7280	National	MM7280	
	TI	TMS4060	
♦IM7501	Mostek	MK4007	
♦IM7511	Mostek	MK4007	
♦IM7512	Mostek	MK4007	
	Signetics	1101	
IM7552	**NEC Micro**	**μPD2102**	**1591**
	SGS	M330	
	Signetics	2102	
♦IM7702	Nortec	1402	
♦IM7703	Nortec	1403	
♦IM7704	Nortec	1404	
♦IM7708	Intel	2708	
	Signetics	2708	
	TI	TMS2708	
♦IM7712	AMD	AM2806	
	Nortec	2512	
♦IM7716	**Fairchild**	**F16K**	**1272**
♦IM7722	AMD	AM2808	
IM7780	Fairchild	3347	
♦IM7780	Mostek	MK1007	
	TI	TMS3409	
LD110	**Siliconix**	**LD110**	**829**
LD111	**Siliconix**	**LD111**	**829**
LF155	AMD	LF155	
	Fairchild	μAF155	
	Motorola	LF155	
	National	**LF155**	**1035**
	PMI	PM155	
	Raytheon	LF155	
	Signetics	LF155	
	TI	LF155	
LF156	AMD	LF156	
	Fairchild	μAF156	
	Motorola	LF156	
	National	**LF156**	**1035**
	PMI	PM156	
	Raytheon	LF156	
	Signetics	LF156	
	TI	LF156	
LF157	AMD	LF157	
	Fairchild	μAF157	
	Motorola	LF157	
	National	**LF157**	**1035**
	PMI	PM157	
	Raytheon	LF157	
	Signetics	LF157	
	TI	LF157	
LF255	AMD	LF255	
	Fairchild	μAF255	
	Motorola	LF255	
	National	LF255	
	PMI	PM255	
	Raytheon	LF255	
	Signetics	LF255	
	TI	LF255	
LF256	AMD	LF256	
	Fairchild	μAF256	
	Motorola	LF256	
	National	LF256	
	PMI	PM256	
	Raytheon	LF256	
	Signetics	LF256	
	TI	LF256	
LF257	AMD	LF257	
	Fairchild	μAF257	
	Motorola	LF257	
	National	LF257	
	PMI	PM257	
	Raytheon	LF257	
	Signetics	LF257	
	TI	LF257	
LF355	AMD	LF355	
	Fairchild	μAF355	
	Motorola	LF355	
	National	LF355	
	PMI	PM355	
	Raytheon	LF355	
	Signetics	LF355	
	TI	LF355	
LF356	AMD	LF356	
	Fairchild	μAF356	
	Motorola	LF356	
	National	**LF356**	**1035,1073**
	PMI	PM356	
	Raytheon	LF356	
	Signetics	LF356	
	TI	LF356	
LF357	AMD	LF357	
	Fairchild	μAF357	
	Motorola	LF357	
	National	LF357	
	PMI	PM357	
	Raytheon	LF357	
	Signetics	LF357	
	TI	LF357	
LH2108A	PMI	PM2108A	
LH2208A	PMI	PM2208A	
LH2308A	PMI	PM2308A	
LM139A	PMI	CMP-04	
		PM139A	
LM148	AMD	LM148	
	Exar	XR4741	
	Raytheon	LM148	
LM239A	PMI	CMP-04	
		PM239A	
LM248	AMD	LM248	
	Exar	XR4741	
	Raytheon	LM248	
LM339A	PMI	CMP-04	
		PM339A	
LM348	AMD	LM348	
	Raytheon	LM348	
MK4027	Fairchild	M4027	
	Pujitsu	MB8227	
MM452	Siliconix	SI452	
MM455	Siliconix	SI455	
MM552	Siliconix	SI552	
MM555	Siliconix	SI555	
NE555	Exar	XR555	
	RCA	CA555	
NE556	Exar	XR555	
SE555	Cherry	CS555	
	Exar	XR555M	
	RCA	CA555	
SE556	Exar	XR555M	
♦SSS1458	Exar	XR1458	
	RCA	CA1458	
	Silicon G	SG1458	
♦SSS1558	AD	AD101	
	Exar	XR1558	
	National	**LM101**	**1035**
	RCA	CA101	
		CA1558	
		CA748	
	Silicon G	SG1558	
♦101	Motorola	LM101	
	RCA	CA101	
	Silicon G	SG101	
♦105	Motorola	LM105	
	Silicon G	SG105	
♦107	Motorola	LM107	
	RCA	CA107	
	Silicon G	SG107	
♦108	AD	AD108	
	National	**LM108**	**1035**
	Raytheon	LM108	
	RCA	CA108	
	Silicon G	SG108	
♦111	Motorola	LM111	
	RCA	CA111	
	Silicon G	SG111	
♦201	AD	AD201	
	Motorola	LM201	
	National	LM201	
	RCA	CA201	
		CA748	
	Silicon G	SG201	
♦205	Motorola	LM205	
	Silicon G	SG205	
♦207	Motorola	LM207	
	RCA	CA207	
	Silicon G	SG207	
♦208	AD	AD208	
	Motorola	LM208	
	National	LM208	
	Raytheon	LM208	
	RCA	CA208	
	Silicon G	SG208	
♦211	Motorola	LM211	
	RCA	CA211	
	Silicon G	SG211	
2114	**AMI**	**S2114**	**1196**
	Fujitsu	MB8114	
	TI	TMS4045	
♦2650	Signetics	2650	
301	AD	AD301	
	Motorola	LM301	
	National	LM301	
	Raytheon	LM301	
	RCA	CA301	
	Silicon G	SG301	
305	Motorola	LM305	
	Silicon G	SG305	

♦ Discontinued

The manufacturers report their devices can be used as direct replacements.
Performance details often differ, so compare the specifications considering your requirements.

Intersil (cont'd)

Manufacturer Device	Replacement Source	Device	IC Master Page
307	RCA	CA307	
	Silicon G	SG307	
308	AD	AD308	
	Motorola	LM308	
	National	LM308	
	Raytheon	LM308	
	RCA	CA308	
	Silicon G	SG308	
310	PMI	BUF-01	
		BUF-02	
311	Motorola	LM311	
	RCA	CA311	
	Silicon G	SG311	
4250	National	LM4250	
	Silicon G	SG4250	
5101	**AMI**	**S5101**	**1206**
555	Motorola	MC1455	
	National	LM555	
	Raytheon	RC555	
		RM555	
	RCA	CA355	
	Silicon G	SG555	
723	Motorola	MC1723	
	National	LM723	
	Raytheon	RC723	
		RM723	
	RCA	CA723	
	Signetics	µA723	
	Silicon G	SG723	
741	AD	AD741	
	Fairchild	µA741	
	Motorola	MC1741	
	National	**LM741**	**1035**
	PMI	SSS741	
	Raytheon	RC741	
		RM741	
	RCA	CA741	
	Silicon G	SG741	
♦747	Motorola	MC1747	
	RCA	CA747	
	Silicon G	SG747	
748	Fairchild	µA748	
	Motorola	MC1748	
	National	LM748	
	Raytheon	RC748	
		RM748	
	RCA	CA748	
	Silicon G	SG748	
8240	Exar	XR2240	

Maruman Integrated Circuits

Manufacturer Device	Replacement Source	Device	IC Master Page
MIC2332	**AMI**	**S68332**	**1216**

Micro Networks

Manufacturer Device	Replacement Source	Device	IC Master Page
DAC80	AD	DAC80	
	Beckman	7580	
	Burr-Brown	**DAC80**	**658**
	Datel	DAC-HZ12B	
	Hybrid Sys.	DAC335	
DAC85	Beckman	877-85	
	Datel	DAC-HZ12B	
	Hybrid Sys.	DAC335	
MNADC84	**Datel**	**ADC-HZ12BGC**	**669**
MNAD84	Hybrid Sys.	ADC581	
MNAD85	Hybrid Sys.	ADC581	
MN3000	Hybrid Sys.	DAC337-0	
MN3001	Hybrid Sys.	DAC337-1	
MN3002	Hybrid Sys.	DAC337-2	
MN3003	Hybrid Sys.	DAC337-3	
MN3004	Hybrid Sys.	DAC337-4	
MN3005	Hybrid Sys.	DAC337-5	
MN3006	Hybrid Sys.	DAC337-6	
MN3007	Hybrid Sys.	DAC337-7	
MN3210	Hybrid Sys.	DAC346	
		DAC347	
MN3211	Hybrid Sys.	DAC346	
		DAC347	
		DAC356	
MN370	Hybrid Sys.	DAC346	
		DAC347	
		DAC356	
MN371	Hybrid Sys.	DAC346	
		DAC347	
MN410	HyComp	M/DA2005	
MN411	HyComp	M/DA2005-1	
MN5065	Motorola	MC1358	
MN5240	**Datel**	**ADC-HZ12BGC**	**669**

Micro Power Systems

Manufacturer Device	Replacement Source	Device	IC Master Page
MP7501	AD	AD7501	
MP7502	AD	AD7502	
MP7503	AD	AD7503	
MP7506	AD	AD7506	
MP7507	AD	AD7507	
MP7510	AD	AD7510	
	PMI	SSS7510	
MP7511	AD	AD7511	
	PMI	SSS7511	
MP7512	AD	AD7512	
MP7513	AD	AD7513	
MP7516	AD	AD7516	
	Fairchild	F4016	
	Mitel	SIL4016	
	Motorola	MC14016	
	National	**CD4016**	**1076**
	RCA	CD4016	
	Solitron	CM4016	
	SSS	SCL4016	
	TI	TP4016	
MP7519	AD	AD7519	
MP7520	AD	AD7520	
	Hybrid Sys.	DAC331-10	
		DAC331-8	
MP7521	AD	AD7521	
	Hybrid Sys.	DAC331-10	
		DAC331-8	
MP7522	AD	AD7522	
MP7523	AD	AD7523	
MP7550	AD	AD7550	
MP7570	AD	AD7570	
MP7621	AD	AD7541	

Mitel Semiconductor

Manufacturer Device	Replacement Source	Device	IC Master Page
SIL4000	Motorola	MC14000	
	National	CD4000	
	RCA	CD4000	
	Solitron	CM4000	
	SSS	SCL4000	
	TI	TP4000	
SIL4001	Fairchild	F4001	
	Motorola	MC14001	
	National	CD4001	
	NEC America	µPD4001	
	RCA	CD4001	
	SGS	HBF4001	
	Solitron	CM4001	
	SSS	SCL4001	
	TI	TP4001	
	Toshiba	TC4001	
SIL4002	Fairchild	F4002	
	Motorola	MC14002	
	National	CD4002	
	NEC America	µPD4002	
	RCA	CD4002	
	SGS	HBF4002	
	Solitron	CM4002	
	SSS	SCL4002	
	TI	TP4002	
	Toshiba	TC4002	
SIL4007	Fairchild	F4007	
	Motorola	MC14007	
	National	CD4007	
	RCA	CD4007	
	SGS	HBF4007	
	Solitron	CM4007	
	SSS	SCL4007	
	TI	TP4007	
	Toshiba	TC4007	
SIL4009	National	CD4009	
SIL4009	RCA	CD4009	
	SGS	HBF4009	
	Solitron	CM4009	
	SSS	SCL4009	
	TI	TP4009	
	Toshiba	TC4009	
SIL4010	National	CD4010	
	RCA	CD4010	
	SGS	HBF4010	
	Solitron	CM4010	
	SSS	SCL4010	
	TI	TP4010	
	Toshiba	TC4010	
SIL4011	Fairchild	F4011	
	Motorola	MC14011	
	National	CD4011	
	NEC America	µPD4011	
	RCA	CD4011	
	SGS	HBF4011	
	Solitron	CM4011	
	SSS	SCL4011	
	TI	TP4011	
	Toshiba	TC4011	
SIL4012	Fairchild	F4012	
	Motorola	MC14012	
	National	CD4012	
	NEC America	µPD4012	
	RCA	CD4012	
	SGS	HBF4012	
	Solitron	CM4012	
	SSS	SCL4012	
	TI	TP4012	
	Toshiba	TC4012	
SIL4013	Fairchild	F4013	
	Motorola	MC14013	
	National	CD4013	
	NEC America	µPD4013	
	RCA	CD4013	
	SGS	HBF4013	
	Solitron	CM4013	
	SSS	SCL4013	
	TI	TP4013	
	Toshiba	TC4013	
SIL4014	Fairchild	F4014	
	Motorola	MC14014	
	National	CD4014	
	NEC America	µPD4014	
	RCA	CD4014	
	SGS	HBF4014	
	Solitron	CM4014	
	SSS	SCL4014	
	TI	TP4014	
	Toshiba	TC4014	
SIL4015	Fairchild	F4015	
	Motorola	MC14015	
	National	CD4015	
	NEC America	µPD4015	
	RCA	CD4015	
	SGS	HBF4015	
	Solitron	CM4015	
	SSS	SCL4015	
	TI	TP4015	
	Toshiba	TC4015	
SIL4016	AD	AD7516	
	Fairchild	F4016	
	Micro Power	MP7516	
	Motorola	MC14016	
	National	**CD4016**	**1076**
	RCA	CD4016	
	Solitron	CM4016	
	SSS	SCL4016	
	TI	TP4016	
SIL4017	Fairchild	F4017	
	Motorola	MC14017	
	National	CD4017	
	NEC America	µPD4017	
	RCA	CD4017	
	SGS	HBF4017	
	Solitron	CM4017	
	SSS	SCL4017	
	TI	TP4017	
	Toshiba	TC4017	
SIL4018	Fairchild	F4018	
	National	CD4018	
	RCA	CD4018	
	SGS	HBF4018	
SIL4018	Solitron	CM4018	
	SSS	SCL4018	
	TI	TP4018	
	Toshiba	TC4018	
SIL4019	Fairchild	F4019	
	National	CD4019	
	RCA	CD4019	
	SGS	HBF4019	
	Solitron	CM4019	
	SSS	SCL4019	
	TI	TP4019	
	Toshiba	TC4019	
SIL4020	Fairchild	F4020	
	Motorola	MC14020	
	National	CD4020	
	NEC America	µPD4020	
	RCA	CD4020	
	SGS	HBF4020	
	Solitron	CM4020	
	SSS	SCL4020	
	TI	TP4020	
	Toshiba	TC4020	
SIL4021	Fairchild	F4021	
	Motorola	MC14021	
	National	CD4021	
	NEC America	µPD4021	
	RCA	CD4021	
	Solitron	CM4021	
	SSS	SCL4021	
	TI	TP4021	
	Toshiba	TC4021	
SIL4022	Fairchild	F4022	
	Motorola	MC14022	
	National	CD4022	
	RCA	CD4022	
	SGS	HBF4022	
	Solitron	CM4022	
	SSS	SCL4022	
	TI	TP4022	
	Toshiba	TC4022	
SIL4023	Fairchild	F4023	
	Motorola	MC14023	
	National	CD4023	
	NEC America	µPD4023	
	RCA	CD4023	
	SGS	HBF4023	
	Solitron	CM4023	
	SSS	SCL4023	
	TI	TP4023	
	Toshiba	TC4023	
SIL4024	Fairchild	F4024	
	Motorola	MC14024	
	National	CD4024	
	RCA	CD4024	
	SGS	HBF4024	
	Solitron	CM4024	
	SSS	SCL4024	
	TI	TP4024	
	Toshiba	TC4024	
SIL4025	Fairchild	F4025	
	Motorola	MC14025	
	National	CD4025	
	NEC America	µPD4025	
	RCA	CD4025	
	SGS	HBF4025	
	Solitron	CM4025	
	SSS	SCL4025	
	TI	TP4025	
	Toshiba	TC4025	
SIL4027	Fairchild	F4027	
	Motorola	MC14027	
	National	CD4027	
	NEC America	µPD4027	
	RCA	CD4027	
	SGS	HBF4027	
	Solitron	CM4027	
	SSS	SCL4027	
	TI	TP4027	
	Toshiba	TC4027	
SIL4028	Fairchild	F4028	
	Motorola	MC14028	
	National	CD4028	
	NEC America	µPD4028	
	RCA	CD4028	
	SGS	HBF4028	
	Solitron	CM4028	

♦ Discontinued

Bold face device numbers indicate manufacturers data is provided in the IC Master on the pages noted.

Mitel Semiconductor (cont'd)

Manufacturer Device	Replacement Source	Device	IC Master Page
SIL4028	SSS	SCL4028	
	TI	TP4028	
	Toshiba	TC4028	
SIL4029	Fairchild	F4029	
	National	CD4029	
	NEC America	μPD4029	
	RCA	CD4029	
	SGS	HBF4029	
	Solitron	CM4029	
	SSS	SCL4029	
	TI	TP4029	
	Toshiba	TC4029	
SIL4030	Fairchild	F4030	
	National	CD4030	
	NEC America	μPD4030	
	RCA	CD4030	
	SGS	HBF4030	
	Solitron	CM4030	
	SSS	SCL4030	
	TI	TP4030	
	Toshiba	TC4030	
SIL4035	Fairchild	F4035	
	Motorola	MC14035	
	National	CD4035	
	NEC America	μPD4035	
	RCA	CD4035	
	SGS	HBF4035	
	Solitron	CM4035	
	SSS	SCL4035	
	TI	TP4035	
	Toshiba	TC4035	
SIL4040	Fairchild	F4040	
	National	CD4040	
	NEC America	μPD4040	
	RCA	CD4040	
	Solitron	CM4040	
	SSS	SCL4040	
	TI	TP4040	
	Toshiba	TC4040	
SIL4042	Fairchild	F4042	
	Motorola	MC14042	
	National	CD4042	
	NEC America	μPD4042	
	RCA	CD4042	
	SGS	HBF4042	
	Solitron	CM4042	
	SSS	SCL4042	
	TI	TP4042	
	Toshiba	TC4042	
SIL4043	Fairchild	F4043	
	Motorola	MC14043	
	National	CD4043	
	NEC America	μPD4043	
	RCA	CD4043	
	Solitron	CM4043	
	SSS	SCL4043	
	TI	TP4043	
	Toshiba	TC4043	
SIL4044	Fairchild	F4044	
	Motorola	MC14044	
	National	CD4044	
	NEC America	μPD4044	
	RCA	CD4044	
	Solitron	CM4044	
	SSS	SCL4044	
	TI	TP4044	
	Toshiba	TC4044	
SIL4046	Fairchild	F4046	
	Motorola	MC14046	
	National	CD4046	
	RCA	CD4046	
	Solitron	CM4046	
	SSS	SCL4046	
SIL4049	Fairchild	F4049	
	Motorola	MC14049	
	National	CD4049	
	NEC America	μPD4049	
	RCA	CD4049	
	SGS	HBF4049	
	Solitron	CM4049	
	SSS	SCL4049	
	TI	TP4049	
	Toshiba	TC4049	
SIL4050	Fairchild	F4050	
	Motorola	MC14050	
	National	CD4050	
	NEC America	μPD4050	
	RCA	CD4050	
	SGS	HBF4050	
	Solitron	CM4050	
	SSS	SCL4050	
	TI	TP4050	
	Toshiba	TC4050	
SIL4051	Fairchild	F4051	
	Motorola	MC14051	
	National	CD4051	
	RCA	CD4051	
	Solitron	CM4051	
	SSS	SCL4051	
	TI	TP4051	
	Toshiba	TC4051	
SIL4052	Fairchild	F4052	
	Motorola	MC14052	
	National	CD4052	
	RCA	CD4052	
	Solitron	CM4052	
	SSS	SCL4052	
	TI	TP4052	
	Toshiba	TC4052	
SIL4053	Fairchild	F4053	
	Motorola	MC14053	
	National	CD4053	
	RCA	CD4053	
	Solitron	CM4053	
	SSS	SCL4053	
	Toshiba	TC4053	
SIL4055	RCA	CD4055	
SIL4056	RCA	CD4056	
SIL4060	National	CD4060	
	RCA	CD4060	
	SSS	SCL4060	
SIL4066	Fairchild	F4066	
	Motorola	MC14066	
	National	**CD4066**	**1076**
	NEC America	μPD4066	
	RCA	CD4066	
	SGS	HBF4066	
	Signetics	N4066	
	Solitron	CM4066	
	SSS	SCL4066	
	Toshiba	TC4066	
SIL4068	Fairchild	F4068	
	Motorola	MC14068	
	RCA	CD4068	
	Solitron	CM4068	
	SSS	SCL4068	
	TI	TP4068	
	Toshiba	TC4068	
SIL4069	Fairchild	F4069	
	Harris	HD74C04	
	Motorola	MC14069	
	National	CD4069	
		MM74C04	
	NEC America	μPD4069	
	RCA	CD4069	
	Solitron	CM4069	
	SSS	SCL4069	
	TI	TP4069	
	Toshiba	TC4069	
SIL4070	Fairchild	F4070	
	National	CD4070	
		MM74C86	
	RCA	CD4070	
	Solitron	CM4070	
	SSS	SCL4070	
SIL4071	Fairchild	F4071	
	Motorola	MC14071	
	National	CD4071	
	NEC America	μPD4071	
	RCA	CD4071	
	Solitron	CM4071	
	SSS	SCL4071	
	TI	TP4071	
	Toshiba	TC4071	
SIL4072	Fairchild	F4072	
	Motorola	MC14072	
	RCA	CD4072	
	SSS	SCL4072	
	TI	TP4072	
SIL4072	Toshiba	TC4072	
SIL4073	Fairchild	F4073	
	Motorola	MC14073	
	National	CD4073	
	RCA	CD4073	
	Solitron	CM4073	
	SSS	SCL4073	
	TI	TP4073	
	Toshiba	TC4073	
SIL4075	Fairchild	F4075	
	Motorola	MC14075	
	National	CD4075	
	RCA	CD4075	
	SSS	SCL4075	
	TI	TP4075	
	Toshiba	TC4075	
SIL4076	Fairchild	F4076	
	Harris	HD74C173	
	Motorola	MC14076	
	National	CD4076	
		MM74C173	
	RCA	CD4076	
	Solitron	CM4076	
	SSS	SCL4076	
SIL4077	Fairchild	F4077	
	Motorola	MC14077	
	RCA	CD4077	
	Solitron	CM4077	
	SSS	SCL4077	
SIL4078	Fairchild	F4078	
	Motorola	MC14078	
	RCA	CD4078	
	Solitron	CM4078	
	SSS	SCL4078	
	Toshiba	TC4078	
SIL4081	Fairchild	F4081	
	Motorola	MC14081	
	National	CD4081	
	NEC America	μPD4081	
	RCA	CD4081	
	Solitron	CM4081	
	SSS	SCL4081	
	TI	TP4081	
	Toshiba	TC4081	
SIL4082	Fairchild	F4082	
	Motorola	MC14082	
	RCA	CD4082	
	SSS	SCL4082	
	TI	TP4082	
	Toshiba	TC4082	
SIL4098	RCA	CD4098	
SIL4502	Motorola	MC14502	
	RCA	CD4502	
	SSS	SCL4502	
SIL4508	Motorola	MC14508	
	RCA	CD4508	
	SSS	SCL4508	
	Toshiba	TC4508	
SIL4510	Fairchild	F4510	
	Motorola	MC14510	
	National	CD4510	
	RCA	CD40192	
		CD4510	
	SSS	SCL4510	
	Toshiba	TC4510	
SIL4511	Fairchild	F4511	
	Motorola	MC14511	
	National	CD4511	
	RCA	CD4511	
	Solitron	CM4511	
	SSS	SCL4511	
	TI	TP4511	
SIL4512	Fairchild	F4512	
	Motorola	MC14512	
	National	CD4512	
	NEC America	μPD4512	
	SSS	SCL4512	
	TI	TP4512	
	Toshiba	TC4512	
SIL4514	Fairchild	F4514	
	Motorola	MC14514	
	National	CD4514	
	RCA	CD4514	
	Solitron	CM4514	
	SSS	SCL4514	
	Toshiba	TC4514	
SIL4515	Fairchild	F4515	
	Motorola	MC14515	
	National	CD4515	
	RCA	CD4515	
	Solitron	CM4515	
	SSS	SCL4515	
	Toshiba	TC4515	
SIL4516	Fairchild	F4516	
	Motorola	MC14516	
	National	CD4516	
	RCA	CD40193	
		CD4516	
	SSS	SCL4516	
	Toshiba	TC4516	
SIL4518	Fairchild	F4518	
	Motorola	MC14518	
	National	CD4518	
	RCA	CD4518	
	Solitron	CM4518	
	SSS	SCL4518	
	TI	TP4518	
	Toshiba	TC4518	
SIL4520	Fairchild	F4520	
	Motorola	MC14520	
	National	CD4520	
	NEC America	μPD4520	
	RCA	CD4520	
	Solitron	CM4520	
	SSS	SCL4520	
	TI	TP4520	
	Toshiba	TC4520	

Mitsubishi Electric Co.

Manufacturer Device	Replacement Source	Device	IC Master Page
M5L2104	Fujitsu	MB8116	
M5S000	Fairchild	74S00	
	Hitachi	HD74S00	
	National	DM74S00	
	Signetics	74S00	
	TI	SN74S00	
M5S003	Fairchild	74S03	
	Hitachi	HD74S03	
	National	DM74S03	
	Signetics	74S03	
	TI	SN74S03	
M5S004	Fairchild	74S04	
	Hitachi	HD74S04	
	National	DM74S04	
	Signetics	74S04	
	TI	SN74S04	
M5S005	Fairchild	74S05	
	Hitachi	HD74S05	
	National	DM74S05	
	Signetics	74S05	
	TI	SN74S05	
M5S010	Fairchild	74S10	
	Hitachi	HD74S10	
	National	DM74S10	
	Signetics	74S10	
	TI	SN74S10	
M5S011	Fairchild	74S11	
	Hitachi	HD74S11	
	National	DM74S11	
	Signetics	74S11	
	TI	SN74S11	
M5S015	Fairchild	74S15	
	Hitachi	HD74S15	
	National	DM74S15	
	Signetics	74S15	
	TI	SN74S15	
M5S020	Fairchild	74S20	
	Hitachi	HD74S20	
	National	DM74S20	
	Signetics	74S20	
	TI	SN74S20	
M5S030	Fairchild	74S30	
	National	DM74S30	
	TI	SN74S30	
M5S040	Fairchild	74S40	
	Hitachi	HD74S40	
	National	DM74S40	
	Signetics	74S40	
	TI	SN74S40	
M5S051	Fairchild	74S51	
	National	DM74S51	

♦ Discontinued

The manufacturers report their devices can be used as direct replacements.
Performance details often differ, so compare the specifications considering your requirements.

Mitsubishi Electric Co. (cont'd)

Manufacturer Device	Replacement Source	Device	IC Master Page
M5S051	Signetics	74S51	
	TI	SN74S51	
M5S074	Fairchild	74S74	
	Hitachi	HD74S74	
	TI	SN74S74	
M5S085	Signetics	74S85	
	TI	SN74S85	
M5S112	Fairchild	74S112	
	Hitachi	HD74S112	
	Motorola	SN74S112	
	National	DM74S112	
	Signetics	74S112	
	TI	SN74S112	
M5S113	Fairchild	74S113	
	Hitachi	HD74S113	
	Motorola	SN74S113	
	National	DM74S113	
	Signetics	74S113	
	TI	SN74S113	
M5S114	Fairchild	74S114	
	Hitachi	HD74S114	
	National	DM74S114	
	Signetics	74S114	
	TI	SN74S114	
M5S133	Fairchild	74S133	
	Hitachi	HD74S133	
	National	DM74S133	
	Signetics	74S133	
	TI	SN74S133	
M5S138	AMD	SN74S138	
	Fairchild	74S138	
	National	DM74S138	
	Signetics	74S138	
	TI	SN74S138	
M5S151	AMD	SN74S151	
	Fairchild	74S151	
	Hitachi	HD74S151	
	National	DM74S151	
	Signetics	74S151	
	TI	SN74S151	
M5S153	AMD	SN74S153	
	Fairchild	74S153	
	National	DM74S153	
	Signetics	74S153	
	TI	SN74S153	
M5S157	AMD	SN74S157	
	Fairchild	74S157	
	National	DM74S157	
	Signetics	74S157	
	TI	SN74S157	
M5S158	AMD	SN74S158	
	Fairchild	74S158	
	National	DM74S158	
	Signetics	74S158	
	TI	SN74S158	
M5S174	AMD	SN74S174	
	Fairchild	74S174	
	Hitachi	HD74S174	
	National	DM74S174	
	Signetics	74S174	
	TI	SN74S174	
M5S175	AMD	SN74S175	
	Fairchild	74S175	
	Hitachi	HD74S175	
	National	DM74S175	
	Signetics	74S175	
	TI	SN74S175	
M5S181	AMD	SN74S181	
	Fairchild	93S41	
	Hitachi	HD74S181	
	Signetics	74S181	
	TI	SN74S181	
M5S182	Fairchild	93S42	
	National	DM74S182	
	Signetics	74S182	
	TI	SN74S182	
M5S22	Fairchild	74S22	
	Hitachi	HD74S22	
	National	DM74S22	
	Signetics	74S22	
	TI	SN74S22	
M5S251	AMD	SN74S251	
M5S251	Fairchild	74S251	
	Hitachi	HD74S251	
	National	DM74S251	
	Signetics	74S251	
	TI	SN74S251	
M5S257	AMD	SN74S257	
	Fairchild	74S257	
	National	DM74S257	
	Signetics	74S257	
	TI	SN74S257	
M5S258	AMD	SN74S258	
	Fairchild	74S258	
	Signetics	74S258	
	TI	SN74S258	
M5141	Toshiba	TA7504	
M51709	Toshiba	TA7502	
M53200	Fairchild	7400	
	Hitachi	HD7400	
	Motorola	MC7400	
	National	DM7400	
	NEC America	μPB7400	
	Signetics	7400	
	TI	SN7400	
	Toshiba	TC7400	
	TRW	7400	
M53201	Fairchild	7401	
	Motorola	MC7401	
	National	DM7401	
	Signetics	7401	
	TI	SN7401	
	TRW	7401	
M53202	Fairchild	7402	
	Hitachi	HD7402	
	Motorola	MC7402	
	National	DM7402	
	NEC America	μPB7402	
	Signetics	7402	
	TI	SN7402	
	TRW	7402	
M53203	Fairchild	7403	
	Hitachi	HD7403	
	Motorola	MC7403	
	National	DM7403	
	Signetics	7403	
	TI	SN7403	
	TRW	7403	
M53204	Fairchild	7404	
	Hitachi	HD7404	
	Motorola	MC7404	
	National	DM7404	
	NEC America	μPB7404	
	Signetics	7404	
	TI	SN7404	
	Toshiba	TC7404	
	TRW	7404	
M53205	Fairchild	7405	
	Hitachi	HD7405	
	Motorola	MC7405	
	National	DM7405	
	NEC America	μPB7405	
	Signetics	7405	
	TI	SN7405	
	TRW	7405	
M53206	Fairchild	7406	
	Hitachi	HD7406	
	Motorola	MC7406	
	National	DM7406	
	Signetics	7406	
	TI	SN7406	
	TRW	7406	
M53207	Fairchild	7407	
	Hitachi	HD7407	
	Motorola	MC7407	
	National	DM7407	
	Signetics	7407	
	TI	SN7407	
	TRW	7407	
M53208	Fairchild	7408	
	Motorola	MC7408	
	National	DM7408	
	Signetics	7408	
	TI	SN7408	
	Toshiba	TC7408	
	TRW	7408	
M53209	Fairchild	7409	
	Hitachi	HD7409	
M53209	Motorola	MC7409	
	National	DM7409	
	Signetics	7409	
	TI	SN7409	
	TRW	7409	
M53210	Fairchild	7410	
	Hitachi	HD7410	
	Motorola	MC7410	
	National	DM7410	
	NEC America	μPB7410	
	Signetics	7410	
	TI	SN7410	
		SN7427	
	Toshiba	TC7410	
	TRW	7410	
M53213	Fairchild	7413	
	Motorola	MC7413	
	National	DM7413	
	NEC America	μPB7413	
	Signetics	7413	
	TI	SN7413	
	TRW	7413	
M53214	Fairchild	7414	
	Hitachi	HD7414	
	Motorola	MC7414	
	National	DM7414	
	Signetics	7414	
	TI	SN7414	
M53216	Fairchild	7416	
	Hitachi	HD7416	
	Motorola	MC7416	
	National	DM7416	
	Signetics	7416	
	TI	SN7416	
	TRW	7416	
M53217	Fairchild	7417	
	Hitachi	HD7417	
	Motorola	MC7417	
	National	DM7417	
	Signetics	7417	
	TI	SN7417	
	TRW	7417	
M53220	Fairchild	7420	
	Hitachi	HD7420	
	Motorola	MC7420	
	National	DM7420	
	NEC America	μPB7420	
	Signetics	7420	
	TI	SN7420	
	Toshiba	TC7420	
	TRW	7420	
M53225	Fairchild	7425	
	Motorola	MC7425	
	National	DM7425	
	TI	SN7425	
M53227	Fairchild	7427	
	Hitachi	HD7427	
	Motorola	MC7427	
	National	DM7427	
	Signetics	7427	
M53230	Fairchild	7430	
	Hitachi	HD7430	
	Motorola	MC7430	
	National	DM7430	
	NEC America	μPB7430	
	Signetics	7430	
	TI	SN7430	
	TRW	7430	
M53237	Fairchild	7437	
	Motorola	MC7437	
	National	DM7437	
	NEC America	μPB7437	
	Signetics	7437	
	TI	SN7437	
	TRW	7437	
M53238	Fairchild	7438	
	Motorola	MC7438	
	National	DM7438	
	NEC America	μPB7438	
	Signetics	7438	
	TI	SN7438	
	TRW	7438	
M53240	Fairchild	7440	
	Hitachi	HD7440	
	Motorola	MC7440	
	National	DM7440	
M53240	NEC America	μPB7440	
	Signetics	7440	
	TI	SN7440	
	TRW	7440	
M53241	Fairchild	7441	
	National	DM7441	
M53242	Fairchild	7442	
	Hitachi	HD7442	
	Motorola	MC7442	
	National	DM7442	
	NEC America	μPB7442	
	Signetics	7442	
	TI	SN7442	
M53243	Fairchild	7443	
	Hitachi	HD7443	
	Motorola	MC7443	
	Signetics	7443	
	TI	SN7443	
M53244	Fairchild	7444	
	Hitachi	HD7444	
	Motorola	MC7444	
	Signetics	7444	
	TI	SN7444	
M53245	Fairchild	7445	
	Motorola	MC7445	
	National	DM7445	
	NEC America	μPB7445	
	Signetics	7445	
	TI	SN7445	
	TRW	7445	
M53247	Fairchild	7447	
	Motorola	MC7447	
	National	DM7447	
	NEC America	μPB7447	
	Signetics	7447	
	TI	SN7447	
M53248	Fairchild	7448	
	Motorola	MC7448	
	National	DM7448	
	Signetics	7448	
	TI	SN7448	
M53250	Fairchild	7450	
	Hitachi	HD7450	
	Motorola	MC7450	
	National	DM7450	
	NEC America	μPB7450	
	Signetics	7450	
	TI	SN7450	
	TRW	7450	
M53253	Fairchild	7453	
	Hitachi	HD7453	
	Motorola	MC7453	
	National	DM7453	
	NEC America	μPB7453	
	Signetics	7453	
	TI	SN7453	
	TRW	7453	
M53260	Fairchild	7460	
	Hitachi	HD7460	
	Motorola	MC7460	
	National	DM7460	
	NEC America	μPB7460	
	Signetics	7460	
	TI	SN7460	
	TRW	7460	
M53270	Fairchild	7470	
	Motorola	MC7470	
	National	DM7470	
	Signetics	7470	
	TI	SN7470	
M53272	Fairchild	7472	
	Hitachi	HD7472	
	Motorola	MC7472	
	National	DM7472	
	Signetics	7472	
	TI	SN7472	
	TRW	7472	
M53273	Fairchild	7473	
	Motorola	MC7473	
	National	DM7473	
	NEC America	μPB7473	
	Signetics	7473	
	TI	SN7473	
M53274	Fairchild	7474	
	Hitachi	HD7474	
	Motorola	MC7474	

♦ Discontinued

Bold face device numbers indicate manufacturers data is provided in the IC Master on the pages noted.

Mitsubishi Electric Co. (cont'd)

Manufacturer Device	Replacement Source	Device	IC Master Page
M53274	National	DM7474	
	NEC America	μPB7474	
	Signetics	7474	
	TI	SN7474	
	TRW	7474	
M53275	Fairchild	7475	
	Hitachi	HD7475	
	Motorola	MC7475	
	National	DM7475	
	Signetics	7475	
	TI	SN7475	
	TRW	7475	
M53276	Fairchild	7476	
	Motorola	MC7476	
	National	DM7476	
	NEC America	μPB7476	
	Signetics	7476	
	TI	SN7476	
	TRW	7476	
M53280	Fairchild	7480	
	Motorola	MC7480	
	NEC America	μPB7480	
	Signetics	7480	
	TI	SN7480	
M53283	Fairchild	7483	
	Motorola	MC7483	
	National	DM7483	
	Signetics	7483	
	TI	SN7483	
M53285	Fairchild	7485	
	Hitachi	HD7485	
	Motorola	MC7485	
	National	DM7485	
	NEC America	μPB7485	
	Signetics	7485	
	TI	SN7485	
	TRW	7485	
M53286	Fairchild	7486	
	Hitachi	HD7486	
	Motorola	MC7486	
	National	DM7486	
	NEC America	μPB7486	
	Signetics	7486	
	TI	SN7486	
	TRW	7486	
M53289	AMD	SN7489	
	Fairchild	7489	
	National	DM7489	
	TI	SN7489	
	TRW	7489	
M53290	Fairchild	7490	
	Hitachi	HD7490	
	Motorola	MC7490	
	National	DM7490	
	Signetics	7490	
	TI	SN7490	
	TRW	7490	
M53291	Fairchild	7491	
	Motorola	MC7491	
	National	DM7491	
	NEC America	μPB7491	
	Signetics	7491	
	TI	SN7491	
M53292	Fairchild	7492	
	Hitachi	HD7492	
	Motorola	MC7492	
	National	DM7492	
	Signetics	7492	
	TI	SN7492	
	TRW	7492	
M53293	Fairchild	7493	
	Hitachi	HD7493	
	Motorola	MC7493	
	National	DM7493	
	Signetics	7493	
	TI	SN7493	
	TRW	7493	
M53295	Fairchild	7495	
	Motorola	MC7495	
	National	DM7495	
	Signetics	7495	
	TI	SN7495	
M53296	Fairchild	7496	
	Hitachi	HD7496	
	Motorola	MC7496	
	National	DM7496	
	Signetics	7496	
	TI	SN7496	
	TRW	7496	
M53307	Fairchild	74107	
	Hitachi	HD74107	
	Motorola	MC74107	
	National	DM74107	
	NEC America	μPB74107	
	Signetics	74107	
	TI	SN74107	
M53321	Fairchild	74121	
	Hitachi	HD74121	
	Motorola	MC74121	
	National	DM74121	
	Signetics	74121	
	TI	SN74121	
	TRW	74121	
M53322	Fairchild	74122	
	Motorola	MC74122	
	Signetics	74122	
	TI	SN74122	
M53323	AMD	SN74123	
	Fairchild	74123	
	Motorola	MC74123	
	National	DM74123	
	NEC America	μPB74123	
	Signetics	74123	
	TI	SN74123	
	TRW	74123	
M53325	Fairchild	74125	
	Hitachi	HD74125	
	National	DM74125	
	Signetics	74125	
	TI	SN74125	
M53326	Fairchild	74126	
	Hitachi	HD74126	
	National	DM74126	
	Signetics	74126	
	TI	SN74126	
M53332	Fairchild	74132	
	Hitachi	HD74132	
	Motorola	MC74132	
	National	DM74132	
	Signetics	74132	
	TI	SN74132	
M53345	Fairchild	74145	
	Motorola	MC74145	
	National	DM74145	
	Signetics	74145	
	TI	SN74145	
	TRW	74145	
M53347	Hitachi	HD74147	
	National	DM74147	
	NEC America	μPB74147	
	Signetics	74147	
	TI	SN74147	
M53348	Hitachi	HD74148	
	National	DM74148	
	NEC America	μPB74148	
	Signetics	74148	
	TI	SN74148	
M53350	Fairchild	74150	
	Hitachi	HD74150	
	Motorola	MC74150	
	National	DM74150	
	NEC America	μPB74150	
	Signetics	74150	
	TI	SN74150	
	TRW	74150	
M53351	Fairchild	74151	
	Hitachi	HD74151	
	Motorola	MC74151	
	National	DM74151	
	NEC America	μPB74151	
	Signetics	74151	
	TI	SN74151	
	TRW	74151	
M53353	Fairchild	74153	
	Motorola	MC74153	
	National	DM74153	
	NEC America	μPB74153	
	Signetics	74153	
M53353	TI	SN74153	
	TRW	74153	
M53354	AMD	SN74154	
	Fairchild	74154	
	Motorola	MC74154	
	National	DM74154	
	NEC America	μPB74154	
	Signetics	74154	
	TI	SN74154	
	TRW	74154	
M53355	Fairchild	74155	
	Motorola	MC74155	
	National	DM74155	
	NEC America	μPB74155	
	Signetics	74155	
	TI	SN74155	
	TRW	74155	
M53356	Fairchild	74156	
	Hitachi	HD74156	
	Motorola	MC74156	
	National	DM74156	
	NEC America	μPB74156	
	Signetics	74156	
	TI	SN74156	
	TRW	74156	
M53357	AMD	SN74157	
	Fairchild	74157	
	Hitachi	HD74157	
	Motorola	MC74157	
	National	DM74157	
	NEC America	μPB74157	
	Signetics	74157	
	TI	SN74157	
M53358	Signetics	74158	
M53360	AMD	SN74160	
	Fairchild	74160	
	Hitachi	HD74160	
	Motorola	MC74160	
	National	DM74160	
	Signetics	74160	
	TI	SN74160	
	TRW	74160	
M53361	AMD	SN74161	
	Fairchild	74161	
	Hitachi	HD74161	
	Motorola	MC74161	
	National	DM74161	
	NEC America	μPB74161	
	Signetics	74161	
	TI	SN74161	
	TRW	74161	
M53362	AMD	SN74162	
	Fairchild	74162	
	Hitachi	HD74162	
	Motorola	MC74162	
	National	DM74162	
	Signetics	74162	
	TI	SN74162	
	TRW	74162	
M53363	AMD	SN74163	
	Fairchild	74163	
	Hitachi	HD74163	
	Motorola	MC74163	
	National	DM74163	
	Signetics	74163	
	TI	SN74163	
	TRW	74163	
M53364	AMD	74164	
	Fairchild	74164	
	Hitachi	HD74164	
	National	DM74164	
	NEC America	μPB74164	
	Signetics	74164	
	TI	SN74164	
M53365	Fairchild	74165	
	Motorola	MC74165	
	National	DM74165	
	Signetics	74165	
	TI	SN74165	
M53366	Fairchild	74166	
	Hitachi	HD74166	
	National	DM74166	
	Signetics	74166	
	TI	SN74166	
M53370	Fairchild	74170	
	National	DM74170	
M53370	NEC America	μPB74170	
	Signetics	74170	
	TI	SN74170	
M53374	AMD	SN74174	
	Fairchild	74174	
	Hitachi	HD74174	
	Motorola	MC74174	
	National	DM74174	
	Signetics	74174	
	TI	SN74174	
M53375	AMD	SN74175	
	Fairchild	74175	
	Hitachi	HD74175	
	Motorola	MC74175	
	National	DM74175	
	NEC America	μPB74175	
	Signetics	74175	
	TI	SN74175	
M53376	Fairchild	74176	
	Motorola	MC74176	
	National	DM74176	
	Signetics	74176	
	TI	SN74176	
M53377	Fairchild	74177	
	Motorola	MC74177	
	National	DM74177	
	Signetics	74177	
	TI	SN74177	
M53380	Fairchild	74180	
	Hitachi	HD74180	
	Motorola	MC74180	
	National	DM74180	
	NEC America	μPB74180	
	Signetics	74180	
	TI	SN74180	
	TRW	74180	
M53381	AMD	SN74181	
	Fairchild	74181	
	Motorola	MC74181	
	National	DM74181	
	NEC America	μPB74181	
	Signetics	74181	
	TI	SN74181	
M53382	AMD	SN74182	
	Fairchild	74182	
	Motorola	MC74182	
	National	DM74182	
	NEC America	μPB74182	
	Signetics	74182	
	TI	SN74182	
M53385	National	DM74185	
	TI	SN74185	
M53390	Fairchild	74190	
	Hitachi	HD74190	
	Motorola	MC74190	
	National	DM74190	
	Signetics	74190	
	TI	SN74190	
M53391	Fairchild	74191	
	Hitachi	HD74191	
	Motorola	MC74191	
	National	DM74191	
	Signetics	74191	
	TI	SN74191	
M53392	AMD	SN74192	
	Fairchild	74192	
	Motorola	MC74192	
	National	DM74192	
	NEC America	μPB74192	
	Signetics	74192	
	TI	SN74192	
M53393	AMD	SN74193	
	Fairchild	74193	
	Motorola	MC74193	
	National	DM74193	
	NEC America	μPB74193	
	Signetics	74193	
	TI	SN74193	
M53398	Fairchild	74198	
	Hitachi	HD74198	
	National	DM74198	
	NEC America	μPB74198	
	Signetics	74198	
	TI	SN74198	
M53399	Fairchild	74199	
	National	DM74199	

♦ Discontinued

The manufacturers report their devices can be used as direct replacements.
Performance details often differ, so compare the specifications considering your requirements.

Manufacturer Device	Replacement Source	Device	IC Master Page
Mitsubishi Electric Co. (cont'd)			
M53399	Signetics	74199	
	TI	SN74199	
M53478	TI	SN74278	
M53483	Fairchild	74283	
	NEC America	μPB74283	
	TI	SN74283	
M53490	Fairchild	74290	
	Motorola	MC74290	
	TI	SN74290	
	TRW	74290	
M53493	Fairchild	74293	
	Motorola	MC74293	
	TI	SN74293	
	TRW	74293	
M58755	Fujitsu	MB8107	
Monolithic Memories, Inc.			
♦A5280	AMD	AM27S80	
♦A5281	AMD	AM27S81	
♦A6280	AMD	AM27S80	
♦A6281	AMD	AM27S81	
♦H5201	**TI**	**SN54S287**	**1708**
♦H6201	**TI**	**SN74S287**	**1708**
♦L5560	AMD	31L01	
	National	DM54LS289	
		DM54L89	
		DM54L89A	
L5561	National	DM76L99	
L6550	AMD	AM27S02	
L6551	AMD	AM27S03	
L6560	AMD	AM31L01	
	National	DM74L89	
♦L6561	National	DM74S189	
		DM86L89	
PAL10H8	Raytheon	PAL10H8	
PAL10L8	Raytheon	PAL10L8	
PAL12H6	Raytheon	PAL12H6	
PAL12L6	Raytheon	PAL12L6	
PAL14H4	Raytheon	PAL14H4	
PAL14L4	Raytheon	PAL14L4	
PAL16A4	Raytheon	PAL16A4	
PAL16C1	Raytheon	PAL16C1	
PAL16H2	Raytheon	PAL16H2	
PAL16L2	Raytheon	PAL16L2	
PAL16L8	Raytheon	PAL16L8	
PAL16R4	Raytheon	PAL16R4	
PAL16R6	Raytheon	PAL16R6	
PAL16R8	Raytheon	PAL16R8	
PAL16X4	Raytheon	PAL16X4	
SN54S240	TI	SN54S240	
SN54S241	TI	SN54S241	
SN54S244	TI	SN54S244	
SN54S373	TI	SN54S373	
SN54S374	TI	SN54S374	
SN74S240	TI	SN74S240	
SN74S241	TI	SN74S241	
SN74S244	TI	SN74S244	
SN74S373	TI	SN74S373	
SN74S374	TI	SN74S374	
5200-1	Intersil	IM5603	
	National	DM54S189	
	TI	SN54187	
5201-1	Intersil	IM5623	
	National	DM75S97	
	Signetics	S82S299	
	TI	**SN54S387**	**1708**
5205-1	Intersil	IM5604	
	National	DM54S270	
	Signetics	S82S230	
	TI	SN54S270	
5206-1	Fairchild	93441	
	National	DM54S370	
	TI	SN54S370	
5230-1	Intersil	IM5600	
	National	DM5488	
	TI	SN5488A	
5231-1	Intersil	IM5610	
	National	DM7598	
	TI	SN54S188	1708
5240-1	National	DM77S95	
5241-1	Fairchild	93442	
	National	DM77S96	
5275-1	Signetics	82S291	
		87S290	
5280-1	National	DM87S29	
5281-1	National	DM87S29	
53PS140	**Raytheon**	**29662**	**1665**
53PS141	**Raytheon**	**29663**	**1665**
53PS240	**Raytheon**	**29612**	**1655**
53PS241	**Raytheon**	**29613**	**1655**
53PS480	**Raytheon**	**29622**	**1657**
53PS481	**Raytheon**	**29623**	**1657**
53PS482	**Raytheon**	**29626**	**1659**
53PS483	**Raytheon**	**29627**	**1659**
53PS840	Raytheon	29652	
53PS841	Raytheon	29653	
53PS880	**Raytheon**	**29632**	**1661**
53PS881	**Raytheon**	**29633**	**1661**
53S840	Raytheon	29650	
53S841	Raytheon	29651	
5300-1	AMD	AM27S20	
		AM29S10	
		AM29760	
	Fairchild	**93417**	**1258**
	Harris	**HM7610-2**	**1284**
		HPROM1024A	
	Intersil	IM5603	
	National	DM54S387	
	NEC Micro	μPD403	
	Raytheon	**29660**	**1664**
	Signetics	**S82S126**	**1680**
	TI	**SN54S387**	**1708**
5301-1	AMD	AM27S21	
		AM29S11	
		AM29761	
	Fairchild	**93427**	**1258**
	Harris	**HM7611-2**	**1284**
		HPROM1024	
	Intel	3621	
	Intersil	IM5623	
	National	DM54S287	
	Raytheon	**29661**	**1664**
	Signetics	**S82S129**	**1680**
	TI	**SN54S287**	**1708**
5305-1	AMD	AM27S12	
		AM29770	
	Fairchild	**93436**	**1260**
	Fujitsu	MB7058	
	Harris	**HM7620**	
			1284,1298
	Intel	3602	
	Intersil	IM5604	
	National	DM54S570	
		DM54S571	
	Raytheon	**29610**	**1654**
		29611	**1654**
	Signetics	**S82S130**	**1680**
	TI	SN54S270	
5306-1	AMD	AM27S13	
		AM29771	
	Fairchild	**93446**	**1260**
	Harris	**HM7621**	
			1284,1298
	Intel	3622	
	Intersil	IM5624	
	National	DM54S571	
	Raytheon	**29611**	**1654**
	Signetics	**S82S131**	**1680**
5308-1	National	DM54S470	
	Raytheon	**29600**	**1652**
	TI	**SN54S470**	**1708**
5309-1	National	DM54S471	
	Raytheon	**29601**	**1652**
	TI	**SN54S471**	**1708**
5330-1	AMD	AM27S18	
		AM29750	
	Harris	**HM7602-2**	**1284**
		HPROM8256	
	Intersil	IM5600	
	National	DM54S188	
		DM7577	
	Signetics	**S82S23**	**1680**
	TI	**SN54S188**	**1708**
5331-1	AMD	AM27S19	
		AM29750	
	Harris	**HM7603**	**1284**
5331-1	Intersil	IM5610	
	National	DM54S288	
		DM7578	
	Signetics	**S82S123**	**1680**
	TI	**SN54S288**	**1708**
5340-1	**Fairchild**	**93438**	**1262**
	Harris	**HM7640**	
			1284,1304
	Intel	M3604	
	Intersil	IM5605	
	National	DM77S295	
		DM77S296	
	Raytheon	**29624**	**1658**
	Signetics	**S82S140**	**1680**
	TI	**SN54S475**	**1708**
5341-1	**Harris**	**HM7641**	
			1284,1304
	Intel	M3624	
		3624	
	National	DM77S296	
	Raytheon	**29625**	**1658**
	TI	**SN54S474**	**1708**
5348-1	National	DM54S473	
	Raytheon	**29620**	**1656**
	TI	**SN54S473**	**1708**
5349-1	National	DM54S472	
	Raytheon	**29621**	**1656**
	TI	**SN54S472**	**1708**
5350-1	Raytheon	29640	
5351-1	Raytheon	29641	
5352-1	**Fairchild**	**93452**	**1264**
	Harris	**HM7642-2**	**1284**
	Intel	3605	
	National	DM54S572	
	Raytheon	29640	
	Signetics	**S82S136**	**1680**
	TI	**SN54S476**	**1713**
5353-1	**Fairchild**	**93453**	**1264**
	Harris	**HM7642**	
			1284,1308
		HM7643-2	**1284**
	Intel	3625	
	National	DM54S573	
	Raytheon	29641	
	Signetics	**S82S137**	**1680**
	TI	**SN54S477**	**1713**
5380-1	**Harris**	**HM7680**	**1322**
	Intel	3608	
	National	DM77S229	
	Raytheon	**29630**	**1660**
	Signetics	**S82S180**	**1680**
5381-1	**Harris**	**HM7681**	**1322**
	Intel	3628	
	National	DM77S228	
	Raytheon	**29631**	**1660**
	Signetics	**S82S181**	**1680**
5384-1	**Raytheon**	**29634**	**1662**
5385-1	**Raytheon**	**29635**	**1662**
	Signetics	**S82S2708**	**1702**
54LS240	AMD	SN54LS240	
	Fairchild	54LS240	
	TI	SN54LS240	
54LS241	AMD	SN54LS241	
	Fairchild	54LS241	
	TI	SN54LS241	
54LS244	TI	SN54LS244	
54LS245	Motorola	SN54LS245	
54LS322	Motorola	SN54LS322	
54LS323	Motorola	SN54LS323	
		SN74LS323	
54LS363	TI	SN54LS363	
54LS373	Motorola	SN54LS373	
	TI	SN54LS373	
54LS374	AMD	SN54LS374	
	TI	SN54LS374	
54S240	AMD	SN54S240	
	Raytheon	54S240	
	TI	SN54S240	
54S241	AMD	SN54S241	
	Raytheon	54S241	
	TI	SN54S241	
54S244	AMD	SN54S244	
	Raytheon	54S244	
54S373	TI	SN54S373	
54S374	TI	SN54S374	
5530	Fairchild	93411	
5530	National	DM54S206	
	Raytheon	RM5330	
	Signetics	**S82S17**	**1678**
	TI	SN54S206	
		SN54S301	
5531	**Fairchild**	**93421**	**1252**
	National	DM54S200	
	Raytheon	RM5340	
	Signetics	**S82S16**	**1678**
	TI	SN54S201	
5560	AMD	AM27S02	
	National	DM54S289	
		DM5489	
	TI	SN54S289	
5561	AMD	AM27S03	
	National	DM54S189	
	TI	SN54S189	
6200-1	Intersil	IM5603	
	National	DM74S187	
	TI	SN74187	
6201-1	Intersil	IM5623	
	National	DM85S97	
	TI	**SN74S387**	**1708**
6205-1	Intersil	IM5604	
	National	DM74S270	
	Signetics	N82S230	
	TI	SN74S270	
6206-1	National	DM74S370	
	TI	SN74S370	
6230-1	Intersil	IM5600	
	Motorola	MCM4002	
	National	DM7488	
	Signetics	8223	
	TI	SN7488A	
6231-1	National	DM8598	
6240-1	Fairchild	93432	
	National	DM87S95	
6241-1	Fairchild	93442	
	National	DM87S96	
6246-1	Signetics	N8204	
6247-1	Signetics	N8205	
6275-1	Signetics	N82S290	
6276-1	Signetics	N82S291	
6280-1	National	DM85S29	
6281-1	National	DM85S28	
63PS140	**Raytheon**	**29662**	**1665**
63PS141	**Raytheon**	**29663**	**1665**
63PS240	**Raytheon**	**29612**	**1655**
63PS241	**Raytheon**	**29613**	**1655**
63PS480	**Raytheon**	**29622**	**1657**
63PS481	**Raytheon**	**29623**	**1657**
63PS482	**Raytheon**	**29626**	**1659**
63PS483	**Raytheon**	**29627**	**1659**
63PS840	Raytheon	29652	
63PS841	Raytheon	29653	
63PS880	**Raytheon**	**29632**	**1661**
63PS881	**Raytheon**	**29633**	**1661**
63S840	Raytheon	29650	
63S841	Raytheon	29651	
6300-1	AMD	AM27S20	
		AM29760	
	Fairchild	**93417**	**1258**
	Harris	**HM7610**	
			1284,1292
		HPROM1024A	
	Intersil	IM5603	
	Mitsubishi	M54700	
	National	DM74S387	
	NEC Micro	μPD403	
	Raytheon	**29660**	**1664**
	Signetics	**N82S126**	**1680**
	TI	**SN74S387**	**1708**
6301-1	AMD	AM27S21	
		AM29761	
	Fairchild	**93427**	**1258**
	Harris	**HM7611**	
			1284,1292
		HPROM1024	
	Intel	3621	
	Intersil	IM5623	
	Mitsubishi	M54730	
	National	DM74S287	
	Raytheon	**29661**	**1664**
	Signetics	N82S623	
	TI	**SN74S287**	**1708**
6305-1	AMD	AM27S12	

♦ Discontinued

Bold face device numbers indicate manufacturers data is provided in the IC Master on the pages noted.

Monolithic Memories, Inc. (cont'd)

Manufacturer Device	Replacement Source	Device	IC Master Page
6305-1	AMD	AM29770	
	Fairchild	**93436**	**1260**
	Harris	**HM7620**	
		1284,1298	
	Intel	3602	
	Intersil	IM5604	
	National	DM74S570	
		DM74S571	
	Raytheon	**29610**	**1654**
	Signetics	**N82S130**	**1680**
	TI	SN74S270	
6306-1	AMD	AM27S13	
		AM29770	
	Fairchild	**93446**	**1260**
	Harris	**HM7621**	
		1284,1298	
	Intel	3622	
	Intersil	IM5624	
	National	DM74S571	
	Raytheon	**29611**	**1654**
	Signetics	**N82S131**	**1680**
	TI	SN74S370	
6308-1	National	DM74S470	
	Raytheon	**29600**	**1652**
	TI	**SN74S470**	**1708**
6309-1	National	DM74S471	
	Raytheon	**29601**	**1652**
	TI	**SN74S471**	**1708**
6330-1	AMD	AM27S18	
		AM29750	
	Harris	**HM7602**	**1284**
		HPROM8256	
	Intersil	IM5600	
	National	DM74S188	
		DM8577	
	Signetics	**N82S23**	**1680**
	TI	**SN74S188**	**1708**
6331-1	AMD	AM27S19	
		AM29751	
	Harris	**HM7603**	**1284**
	Intersil	IM5610	
	National	DM74S288	
		DM8578	
	Signetics	**N82S123**	**1680**
	TI	**SN74S288**	**1708**
6335-1	**Fairchild**	**93436**	**1260**
	Intel	3602	
6340-1	**Fairchild**	**93438**	**1262**
	Harris	**HM7640**	
		1284,1304	
	Intel	3604	
	Intersil	IM5605	
	National	DM87S295	
	NEC Micro	**μPB405**	**1621**
	Raytheon	**29624**	**1658**
	Signetics	**N82S140**	**1680**
	TI	**SN74S475**	**1708**
6341-1	**Fairchild**	**93448**	**1262**
	Harris	**HM7641**	
		1284,1304	
	Intel	3624	
	Intersil	IM5625	
	National	DM87S296	
	NEC Micro	**μPB425**	**1621**
	Raytheon	**29625**	**1658**
	Signetics	**N82S141**	**1680**
	TI	**SN74S474**	**1708**
6348-1	National	DM74S473	
	NEC Micro	**μPB405**	**1621**
	Raytheon	**29620**	**1656**
	TI	**SN74S473**	**1708**
6349-1	National	DM74S472	
	NEC Micro	**μPB425**	**1621**
	Raytheon	**29621**	**1656**
	TI	**SN74S472**	**1708**
6350-1	Raytheon	29640	
6351-1	Raytheon	29641	
6352-1	**Fairchild**	**93452**	**1264**
	Harris	**HM7642**	
		1284,1308	
	Intel	3605	
	National	DM74S572	
6352-1	**NEC Micro**	**μPB406**	**1625**
	Raytheon	29640	
	Signetics	**N82S136**	**1680**
	TI	**SN74S476**	**1713**
6353-1	**Fairchild**	**93453**	**1264**
	Harris	**HM7643**	
		1284,1308	
	Intel	3625	
	National	DM74S573	
	NEC Micro	**μPB426**	**1625**
	Raytheon	29641	
	Signetics	**N82S137**	**1680**
	TI	**SN74S477**	**1713**
6380-1	**Harris**	**HM7680**	**1322**
	Intel	3608	
	National	DM87S229	
	NEC Micro	μPB408	
	Raytheon	**29630**	**1660**
	Signetics	**N82S180**	**1680**
6381-1	**Harris**	**HM7681**	**1322**
	Intel	3628	
	National	DM87S228	
	NEC Micro	μPB428	
	Raytheon	**29631**	**1660**
	Signetics	**N82S181**	**1680**
6384-1	**Raytheon**	**29634**	**1662**
6385-1	**Raytheon**	**29635**	**1662**
	Signetics	82S2708	
6530	AMD	AM2701	
	Fairchild	93411	
	National	DM74S206	
	NEC Micro	μPB2206	
	Raytheon	RC5330	
	Signetics	**N82S17**	**1678**
	TI	SN74S206	
		SN74S301	
6531	AMD	AM27S02	
	Fairchild	**93421**	**1252**
	National	DM74S200	
	Signetics	**N82S16**	**1678**
	TI	SN74S200	
		SN74S201	
6560	AMD	AM27S02	
		AM2700	
		MM6560	
	National	DM74S289	
	Signetics	**N82S25**	**1678**
		3101A	
	TI	SN74S289	
6561	AMD	AM27S03	
		MM6561	
	National	DM74S189	
	TI	SN74S189	
67401	Raytheon	67401	
74LS240	AMD	SN74LS240	
	Fairchild	74LS240	
	Motorola	SN74LS240	
	Raytheon	**74LS240**	**522**
	Signetics	74LS240	
	TI	SN74LS240	
74LS241	AMD	SN74LS241	
	Fairchild	74LS241	
	Motorola	SN74LS241	
	Raytheon	**74LS241**	**525**
	Signetics	74LS241	
	TI	SN74LS241	
74LS244	AMD	SN74LS244	
	Fairchild	74LS244	
	Motorola	SN74LS244	
	Raytheon	**74LS244**	**525**
	Signetics	74LS244	
	TI	SN74LS244	
74LS245	Motorola	SN74LS245	
74LS322	Motorola	SN74LS322	
74LS373	AMD	SN74LS373	
	Fairchild	74LS373	
	Motorola	SN74LS373	
	Raytheon	**74LS373**	**543**
	Signetics	74LS373	
	TI	SN74LS373	
74LS374	AMD	SN74LS374	
	Fairchild	74LS374	
	National	DM74LS374	
	Raytheon	**74LS374**	**543**
	TI	SN74LS374	
74S182	Hitachi	HD74S182	
74S240	AMD	SN74S240	
	Raytheon	74S240	
	TI	SN74S240	
74S241	AMD	SN74S241	
	Raytheon	74S241	
	TI	SN74S241	
74S244	AMD	SN74S244	
	Raytheon	74S244	
74S373	TI	SN74S02	
		SN74S373	
74S374	TI	SN74S374	

MOS Technology

Manufacturer Device	Replacement Source	Device	IC Master Page
MCS1004	SMC	CG4100	
MCS2027	SMC	CG4100	
MCS6502	Rockwell	R6502	
	Synertek	SY6502	
MCS6503	Rockwell	R6503	
	Synertek	SY6503	
MCS6504	Rockwell	R6504	
	Synertek	SY6504	
MCS6505	Rockwell	R6505	
	Synertek	SY6505	
MCS6506	Rockwell	R6506	
MCS6507	Rockwell	R6507	
MCS6512	Rockwell	R6512	
	Synertek	SY6512	
MCS6513	Rockwell	R6513	
	Synertek	SY6513	
MCS6514	Rockwell	R6514	
	Synertek	SY6514	
MCS6515	Synertek	SY6515	
MCS6520	Rockwell	R6520	
	Synertek	SY6520	
MCS6522	Synertek	SY6522	
MCS6530	Rockwell	R6530	
	Synertek	SY6530	
MCS6532	Rockwell	R6532	
	Synertek	SY6532	
MK2002	SMC	G4100	
SY6515	Rockwell	R6515	

Mostek

Manufacturer Device	Replacement Source	Device	IC Master Page
MK1002	AMD	1002	
MK1007	TI	TMS3409	
MK2302	Fairchild	3257	
		3757	
	GI	RO5-2240S	
♦MK2400	AMI	S8773	
MK2500	AMI	S5232	
	Fairchild	3514	
		3515	
MK2600	AMI	S3514	
	Fairchild	3514	
		3515	
MK2708	AMD	2708	
	EA	EA2708	
	Fairchild	**2708**	**1282**
	Fujitsu	MB8518	
	Intel	2708	
	Motorola	MCM2708	
	National	MM2708	
	TI	TMS2708	
MK2716	Intel	2716	
	TI	TMS2516	
MK30000	NEC Micro	μPD2308	
	TI	TMS4700	
MK31000	**AMI**	**S6831A**	
		1215,1806	
	Fairchild	3516E	
	NEC Micro	μPD2316A	
	Rockwell	R2316	
MK32000	**NEC Micro**	**μPD2332**	**1637**
	Signetics	**2632**	**1672**
	Synertek	SY2332	
MK34000	**AMI**	**S4216B**	**1209**
		S6831B	
		1215,1806	
	NEC Micro	μPD2316	
	Rockwell	R2316	
MK3600	**Signetics**	**2664**	**1674**
MK36000	**AMI**	**S4264**	**1212**
MK36000	**Signetics**	**2664**	**1674**
	Synertek	SY2364	
MK3702	Intel	1702	
MK3820	**Fairchild**	**F6820**	**1887**
MK3850	**Fairchild**	**3850**	**1867,1871**
MK3851	**Fairchild**	**3851**	**1867,1871**
MK3852	**Fairchild**	**3852**	**1867,1871**
MK3853	**Fairchild**	**3853**	**1867,1871**
MK3854	**Fairchild**	**3854**	**1867,1873**
MK3856	**Fairchild**	**3856**	**1867,1871**
MK3857	**Fairchild**	**3857**	**1867,1873**
MK3870	**Fairchild**	**3870**	**1863,1867**
MK3871	**Fairchild**	**3871**	**1867,1874**
MK3880	Zilog	Z80-CPU	
MK3881	Zilog	Z80-PIO	
MK3882	Zilog	Z80-CTC	
MK3883	Zilog	Z80-DMA	
MK3884	Zilog	Z80-SIO	
MK4006	Motorola	MCM4006	
	TI	**SN74S387**	**1708**
MK4027	Fairchild	FM4027	
	Fujitsu	MB8227	
	Hitachi	HM4704	
	Intersil	IM7027	
		MK4027	
	Motorola	**MCM4027**	**1522**
	Signetics	**4027**	**1677**
	TI	TMS4027	
MK4096	EA	EA4096	
	Fairchild	4096	
	Motorola	MCM4096	
	TI	TMS4027	
MK4101	**Harris**	**HM6504**	**1363**
MK4102	**Fairchild**	**2102**	**1275**
	NEC Micro	**μPD2102**	**1591**
		μPD2102A	
	Signetics	2102	
MK4104	**NEC Micro**	**μPD4104**	**1610**
		μPD8104	
	TI	TMS4044	
	Zilog	Z6104	
MK4114	TI	TMS4045	
MK4116	AMD	9016	
	Fairchild	**F16K**	**1272**
	Fujitsu	MB8116	
	Hitachi	HM4716	
	Intel	2116	
	Intersil	7116	
	Mitsubishi	**M5K4116**	**1420**
	Motorola	**MCM4116**	**1505**
	NEC Micro	**μPD416**	**1562**
	Signetics	**2690**	**1676**
	TI	TMS4116	
	Toshiba	TMM4116	
		TMM416	
	Zilog	Z6116	
MK4414	Fujitsu	MB8114	
MK50240	AMI	S50240	
	GI	AY3-0215	
MK50241	AMI	S50241	
	GI	AY3-0216	
MK50242	AMI	S50242	
	GI	AY1-0212	
		AY3-0214	
MK5085	**AMI**	**S2559**	**638**
MK5086	**AMI**	**S2559**	**638**
MK5087	**AMI**	**S2559**	**638**

Motorola Semiconductor

Manufacturer Device	Replacement Source	Device	IC Master Page
LF155	AMD	LF155	
	Fairchild	μAF155	
	Intersil	LF155	
	National	**LF155**	**1035**
	PMI	PM155	
	Raytheon	LF155	
	Signetics	LF155	
	TI	LF155	
LF156	AMD	LF156	
	Fairchild	μAF156	
	Intersil	LF156	
	National	**LF156**	**1035**
	PMI	PM156	
	Raytheon	LF156	
	Signetics	LF156	

♦ Discontinued

The manufacturers report their devices can be used as direct replacements.
Performance details often differ, so compare the specifications considering your requirements.

Motorola Semiconductor (cont'd)

Manufacturer Device	Replacement Source	Device	IC Master Page
LF156	TI	LF156	
LF157	AMD	LF157	
	Fairchild	μAF157	
	Intersil	LF157	
	National	**LF157**	**1035**
	PMI	PM157	
	Raytheon	LF157	
	Signetics	LF157	
	TI	LF157	
LF255	AMD	LF255	
	Fairchild	μAF255	
	Intersil	LF255	
	National	LF255	
	PMI	PM255	
	Raytheon	LF255	
	Signetics	LF255	
	TI	LF255	
LF256	AMD	LF256	
	Fairchild	μAF256	
	Intersil	LF256	
	National	LF256	
	PMI	PM256	
	Raytheon	LF256	
	Signetics	LF256	
	TI	LF256	
LF257	AMD	LF257	
	Fairchild	μAF257	
	Intersil	LF257	
	National	LF257	
	PMI	PM257	
	Raytheon	LF257	
	Signetics	LF257	
	TI	LF257	
LF355	AMD	LF355	
	Fairchild	μAF355	
	Intersil	LF355	
	National	LF355	
	PMI	PM355	
	Raytheon	LF355	
	Signetics	LF355	
	TI	LF355	
LF356	AMD	LF356	
	Fairchild	μAF356	
	Intersil	LF356	
	National	**LF356**	**1035,1073**
	PMI	PM356	
	Raytheon	LF356	
	Signetics	LF356	
	TI	LF356	
LF357	AMD	LF357	
	Fairchild	μAF357	
	Intersil	LF357	
	National	LF357	
	PMI	PM357	
	Raytheon	LF357	
	Signetics	LF357	
	TI	LF357	
LM101	AMD	LM101	
	Fairchild	μA101	
	Intersil	LM101	
	National	**LM101**	**1035**
	RCA	CA101	
	Signetics	LM101	
	Silicon G	SG101	
	TI	LM101	
LM104	**Fairchild**	**μA104**	**934**
	National	LM104	
	Raytheon	LM104	
	Silicon G	SG104	
	TI	LM104	
LM105	AMD	LM105	
	Fairchild	**μA105**	**934**
	Intersil	LM105	
	National	LM105	
	Raytheon	LM105	
	Silicon G	SG105	
	TI	LM105	
LM107	AMD	LM107	
	Fairchild	μA107	
	Intersil	LM107	
	National	LM107	
	Raytheon	LM107	
LM107	RCA	CA107	
	Signetics	LM107	
	Silicon G	SG107	
	TI	LM107	
LM108	RCA	CA108	
	Silicon G	SG108	
		SG208	
LM109	**Fairchild**	**μA109**	**934**
	National	LM109	
	Raytheon	LM109	
	Signetics	LM109	
	Silicon G	SG109	
	TI	LM109	
LM110	AMD	LM110	
	Fairchild	μA110	
	Intersil	LM110	
	National	LM110	
	Silicon G	SG110	
LM111	AMD	LM111	
	National	LM111	
	Raytheon	LM111	
	RCA	CA111	
	Signetics	LM111	
	Silicon G	SG111	
	TI	LM111	
LM124	RCA	CA124	
	Silicon G	SG124	
LM139	RCA	CA139	
	Silicon G	SG139	
LM139A	PMI	CMP-04	
		PM139A	
LM158	National	LM158	
LM201	AMD	LM201	
	Fairchild	μA201	
	Intersil	LM201	
	National	LM201	
	RCA	CA201	
	Signetics	LM201	
	Silicon G	SG201	
	TI	LM201	
LM204	Fairchild	μA204	
	National	LM204	
	Raytheon	LM204	
	Silicon G	SG204	
	TI	LM204	
LM205	AMD	LM205	
	Intersil	LM205	
	National	LM205	
	Raytheon	LM205	
	Silicon G	SG205	
	TI	LM205	
LM207	AMD	LM207	
	Fairchild	μA207	
	Intersil	LM207	
	National	LM207	
	Raytheon	LM207	
	RCA	CA207	
	Signetics	LM207	
	Silicon G	SG207	
	TI	LM207	
LM208	RCA	CA208	
	Silicon G	SG208	
LM209	AMD	LM209	
	Fairchild	**μA209**	**934**
	National	LM209	
	Raytheon	LM209	
	Signetics	LM209	
	Silicon G	SG209	
	TI	LM209	
LM210	AMD	LM210	
	Fairchild	μA210	
	Intersil	LM210	
	National	LM210	
	Silicon G	SG210	
LM211	AMD	LM211	
	Intersil	LM211	
	National	LM211	
	Raytheon	LM211	
	RCA	CA211	
	Signetics	LM211	
	Silicon G	SG211	
	TI	LM211	
LM224	RCA	CA224	
	Silicon G	SG224	
LM239	RCA	CA239	
	Silicon G	SG239	
LM239A	PMI	CMP-04	
		PM239A	
LM258	National	LM258	
LM289	Silicon G	SG208	
LM2901	NEC America	μPC2901	
LM2902	NEC America	μPC2902	
LM301	AMD	LM301	
	Fairchild	μA301	
	Intersil	LM301	
	National	LM301	
	Raytheon	LM301	
	RCA	CA301	
	Signetics	LM301	
	Silicon G	SG301	
	TI	LM301	
	Toshiba	TA7506	
LM301A	NEC America	μPC157	
		μPC301A	
LM304	**Fairchild**	**μA304**	**934**
	National	LM304	
	NEC America	μPC142	
	Raytheon	LM304	
	Silicon G	SG304	
LM305	AMD	LM305	
	Fairchild	**μA305**	**934**
	Intersil	LM305	
	National	LM305	
	NEC America	μPC141	
	Raytheon	LM305	
	Silicon G	SG305	
	TI	LM305	
LM307	AMD	LM307	
	Fairchild	μA307	
	Intersil	LM307	
	National	LM307	
	Raytheon	LM307	
	RCA	CA307	
	Signetics	LM307	
	Silicon G	SG307	
	TI	LM307	
LM308	NEC America	μPC156A	
	RCA	CA308	
	Silicon G	SG308	
LM309	AMD	LM309	
	Fairchild	**μA309**	**934**
	National	LM309	
	Raytheon	LM309	
	Signetics	LM309	
	Silicon G	SG309	
	TI	LM309	
LM310	AMD	LM310	
	Fairchild	μA310	
	Intersil	LM310	
	National	LM310	
	PMI	BUF-02	
		BUR-01	
	Silicon G	SG310	
LM311	AMD	LM311	
	Fairchild	μA311	
	Intersil	LM311	
	National	LM311	
	NEC America	μPC311	
	Raytheon	LM311	
	RCA	CA311	
	Signetics	LM311	
	Silicon G	SG311	
	TI	LM311	
LM317	**National**	**LM317**	**1060**
LM323	**National**	**LM323**	**1060**
	Silicon G	SG323	
LM324	NEC America	μPC324	
	RCA	CA324	
	Silicon G	SG324	
LM339	NEC America	μPC339	
	RCA	CA339	
	Silicon G	SG339	
LM339A	PMI	CMP-04	
		PM339A	
LM358	National	LM358	
	NEC America	μPC358	
LM710	NEC America	μPC71	
LM741	NEC America	μPC151	
		μPC741	
♦MCM10140	Signetics	10140	
	TI	SN10140	
♦MCM10142	NEC America	μPB10142	
♦MCM10142	TI	SN10142	
MCM10144	Fairchild	F10410	
	Raytheon	RC10144	
	Signetics	10144	
	TI	SN10144	
MCM10145	Hitachi	MD10145	
	Signetics	10145	
	TI	SN10145	
MCM10147	Fairchild	F10405	
	Fujitsu	MB7047	
	TI	SN10147	
♦MCM10148	Signetics	10148	
	TI	SN10147	
		SN10148	
MCM10149	Signetics	10149	
MCM10152	Fujitsu	MB7042	
MCM1110	National	MM5231	
♦MCM1112	National	MM4230	
		MM5230	
MCM145101	SSS	SCM5101	
MCM14537	RCA	CD4061	
MCM2102	**NEC Micro**	**μPD2102**	**1591**
MCM2111	**NEC Micro**	**μPD2111**	**1595**
MCM2114	AMD	9114	
		9124	
	AMI	**S2114**	**1196**
	Fairchild	**2114**	**1281**
	Fujitsu	MB8114	
	Intel	2114	
	TI	TMS4045	
MCM2141	Fujitsu	MBM4044	
		MBM8044	
	TI	TMS4044	
MCM2147	**AMI**	**S2147**	**1200**
		S4017	**1204**
MCM2708	AMD	2708	
	EA	EA2708	
	Fairchild	**2708**	**1282**
	Fujitsu	MB8518	
	Intel	2708	
	National	MM2708	
	TI	TMS2708	
MCM2716	TI	TMS2716	
MCM4002	Intersil	IM5600	
	MMI	**6230-1**	**1466**
	National	DM5488	
		DM7488	
	TI	SN7488	
MCM4004	Fairchild	93407	
	Intersil	IM5603	
	MMI	**6200-1**	**1466**
	TI	SN7481A	
MCM4005	Fairchild	93407	
	TI	SN7481A	
MCM4006	**TI**	**SN74S387**	**1708**
MCM4027	Fairchild	M4027	
	Fujitsu	MB8227	
	Mostek	MK4027	
	NEC Micro	μPD414	
	TI	TMS4027	
♦MCM4065	Signetics	8225	
MCM4096	Fujitsu	MB8227	
	NEC Micro	μPD414	
MCM4116	AMD	9016	
	Fairchild	**F16K**	**1272**
	Fujitsu	MB8116	
	Intel	2116	
	Intersil	7116	
	Mostek	MK4116	
	NEC Micro	**μPD416**	**1562**
	Signetics	**2690**	**1676**
	TI	TMS4116	
	Zilog	Z6116	
MCM4227	Fujitsu	MB8227	
MCM5303	**Harris**	**HPROM0512**	**1346**
MCM6560	Nitron	NC6560	
MCM6561	Nitron	NC6561	
MCM6570	Nitron	NC6570	
MCM6571	Nitron	NC6571	
MCM6572	Nitron	NC6572	
MCM6573	Nitron	NC6573	
MCM6573A	Nitron	NC6573A	
MCM6574	Nitron	NC6574	
MCM6575	Nitron	NC6575	
MCM6576	Nitron	NC6576	

♦ Discontinued

Bold face device numbers indicate manufacturers data is provided in the IC Master on the pages noted.

Motorola Semiconductor (cont'd)

Manufacturer Device	Replacement Source	Device	IC Master Page
MCM6580	Nitron	NC6580	
MCM6581	Nitron	NC6581	
MCM6583	Nitron	NC6583	
MCM6590	Nitron	NC6590	
MCM6591	Nitron	NC6591	
MCM6604	Fujitsu	MB8227	
	Mostek	MK4096	
	NEC Micro	μPD414	
	TI	TMS4027	
MCM6605	Fujitsu	MB8107	
	Intersil	IM7505	
MCM6616	**NEC Micro**	**μPD416**	**1562**
	TI	TMS4116	
MCM68A10	Hitachi	HM468A10	
MCM68A364	Mostek	MK36000	
MCM6810	**AMI**	**S6810**	**1790**
	Hitachi	HM46810	
MCM68111	NEC Micro	μPD2111A	
MCM6830	Fairchild	F6830	
	Hitachi	HM46830	
	TI	TMS4700	
MCM68308	**Fairchild**	**F683081887,1889**	
	TI	TMS4700	
MCM68316	**Fairchild**	**F683161887,1889**	
		3516E	
	Mostek	MK34000	
	Signetics	**2616**	**1670**
MCM68316E	**AMI**	**S4216B**	**1209**
MCM68317	NEC Micro	μPD2316	
		μPD2316E	**1633**
MCM6832	Nitron	NCM6832	
MCM68332	**AMI**	**S68332**	**1216**
MCM68708	Fujitsu	MB8518	
	TI	TMS2708	
♦MCM7001	RCA	MW7001	
MCM7620	**MMI**	**5305-1**	**1449**
		6305-1	**1449**
MCM7621	**MMI**	**5306-1**	**1449**
		6306-1	**1449**
MCM7640	**MMI**	**5340-1**	**1449**
		6340-1	**1449**
	NEC Micro	**μPB405**	**1621**
		μPD405	
MCM7641	**MMI**	**5341-1**	**1449**
		6341-1	**1449**
	NEC Micro	**μPB425**	**1621**
MCM7642	Fujitsu	MB7059	
	MMI	**5352-1**	**1449**
		6352-1	**1449**
	NEC Micro	**μPB406**	**1625**
		μPD406	
MCM7643	Fujitsu	MB7054	
	MMI	**5353-1**	**1449**
		6353-1	**1449**
	NEC Micro	**μPB426**	**1625**
MCM7680	**MMI**	**5380-1**	**1449**
		6380-1	**1449**
MCM7681	**MMI**	**5381-1**	**1449**
		6381-1	**1449**
MCM93415	**AMI**	**S4015**	**1203**
	Fairchild	**93415**	**1240**
MCM93425	**AMI**	**S4025**	**1203**
	Fairchild	**93425**	**1240**
MCS403	TI	MC3403	
MC10100	Fairchild	F10100	
	NEC America	μPB10100	
	Signetics	10100	
MC10101	Fairchild	F10101	
	Hitachi	HD10101	
	NEC America	μPB10101	
	Plessey	SP10101	
	Signetics	10101	
MC10102	Fairchild	F10102	
	Hitachi	HD10102	
	NEC America	μPB10102	
	Signetics	10102	
MC10103	Fairchild	F10103	
	NEC America	μPB10103	
	Signetics	10103	
MC10104	Fairchild	F10104	
	Hitachi	HD10104	
	Signetics	10104	
MC10105	Fairchild	F10105	
	Hitachi	HD10105	
	National	DM10105	
	NEC America	μPB10105	
	Signetics	10105	
MC10106	Fairchild	F10106	
	Hitachi	HD10106	
	National	DM10106	
	NEC America	μPB10106	
	Signetics	10106	
MC10107	Fairchild	F10107	
	Hitachi	HD10107	
	NEC America	μPB10107	
	Signetics	10107	
MC10109	Fairchild	F10109	
	Hitachi	HD10109	
	National	DM10109	
	NEC America	μPB10109	
	Signetics	10109	
MC10110	Fairchild	F10110	
	Hitachi	HD10110	
	NEC America	μPB10110	
	Signetics	10110	
MC10111	Fairchild	F10111	
	Hitachi	HD10111	
	National	DM10111	
	NEC America	μPB10111	
	Signetics	10111	
MC10113	Fairchild	F10113	
	Signetics	10113	
MC10114	Fairchild	F10114	
	Signetics	10114	
MC10115	Fairchild	F10115	
	National	DM10115	
	NEC America	μPB10115	
	Signetics	10115	
MC10116	Fairchild	F10116	
	Hitachi	HD10116	
	National	DM10116	
	Signetics	10116	
MC10117	Fairchild	F10117	
	Hitachi	HD10117	
	National	DM10117	
	NEC America	μPB10117	
	Signetics	10117	
MC10118	Fairchild	F10118	
	Hitachi	HD10118	
	National	DM10118	
	NEC America	μPB10118	
	Signetics	10118	
MC10119	Fairchild	F10119	
	Hitachi	HD10119	
	National	DM10119	
	Signetics	10119	
MC10121	Fairchild	F10121	
	Hitachi	HD10121	
	National	DM10121	
	Signetics	10121	
MC10123	Fairchild	F10123	
	Signetics	10123	
MC10124	Fairchild	F10124	
	Hitachi	HD10124	
	National	DM10124	
	NEC America	μPB10124	
	Signetics	10124	
MC10125	Fairchild	F10125	
	Hitachi	HD10125	
	Signetics	10125	
MC10128	Signetics	10128	
MC10129	Signetics	10129	
MC10130	Fairchild	F10130	
	Hitachi	HD10130	
	Signetics	1010130	
		10130	
MC10131	Fairchild	F10131	
	Hitachi	HD10131	
	NEC America	μPB10131	
	Signetics	10131	
MC10132	Fairchild	F10132	
	Hitachi	HD10132	
	Signetics	10132	
MC10133	Fairchild	F10133	
	Hitachi	HD10133	
	NEC America	μPB10133	
	Signetics	10133	
MC10134	Fairchild	F10134	
	Hitachi	HD10134	
	Signetics	10134	
MC10135	Fairchild	F10135	
	Signetics	10135	
MC10136	Fairchild	F10136	
	Hitachi	HD10136	
	Signetics	10136	
MC10137	Fairchild	F10137	
	Signetics	10137	
MC10138	Signetics	10138	
MC10139	Intersil	IM5600	
	Signetics	10139	
MC10141	Fairchild	F10141	
	Signetics	10141	
MC10144	NEC America	μPB10144	
	Raytheon	RC10144	
	Signetics	10144	
	TI	SN10144	
MC10145	Fairchild	F10145	
	Hitachi	HD10145	
	Signetics	10145	
MC10149	Signetics	10149	
MC10153	Fairchild	F10153	
MC10158	Fairchild	F10158	
	NEC America	μPB10158	
	Signetics	10158	
MC10159	Fairchild	F10159	
	Signetics	10159	
MC10160	Fairchild	F10160	
	Hitachi	HD10160	
	Signetics	10160	
MC10161	Fairchild	F10161	
	Hitachi	HD10161	
	NEC America	μPB10161	
	Signetics	10161	
MC10162	Fairchild	F10162	
	Hitachi	HD10162	
	Signetics	10162	
MC10164	Fairchild	F10164	
	Hitachi	HD10164	
	NEC America	μPB10164	
	Signetics	10164	
	TI	SN10164	
MC10165	Fairchild	F10165	
	Hitachi	HD10165	
	Signetics	10165	
MC10166	Fairchild	F10166	
MC10168	Fairchild	F10168	
MC10170	Fairchild	F10170	
	Signetics	10170	
MC10171	Fairchild	F10171	
	Signetics	10171	
MC10172	Fairchild	F10172	
	Signetics	10172	
MC10173	Fairchild	F10173	
	Signetics	10173	
MC10174	Fairchild	F10174	
	Hitachi	HD10174	
	NEC America	μPB10174	
	Signetics	10174	
	TI	SN10174	
MC10175	Fairchild	F10175	
	Hitachi	HD10175	
	Signetics	10175	
MC10176	Fairchild	F10176	
	Signetics	10176	
MC10177	Fairchild	F10177	
MC10178	Fairchild	F10178	
	Signetics	10178	
MC10179	Fairchild	F10179	
	Hitachi	HD10179	
	Signetics	10179	
MC10180	Fairchild	F10180	
	Hitachi	HD10180	
	NEC America	μPB10180	
	Signetics	10180	
MC10181	Fairchild	F10181	
	Hitachi	HD10181	
	NEC America	μPB10181	
	Signetics	10181	
MC10186	Fairchild	F10186	
	Signetics	10186	
MC10190	Signetics	10190	
MC10191	Signetics	10191	
MC10192	Fairchild	F10192	
	Signetics	10192	
MC10195	Signetics	10195	
MC10211	Fairchild	F10211	
MC10212	Fairchild	F10212	
MC10216	Fairchild	F10216	
	Signetics	10216	
MC10231	Fairchild	F10231	
	Signetics	10231	
MC1132	SMC	CG4100	
♦MC1161	TI	TMS4062	
♦MC1181	AMI	S2567	
♦MC1182	AMI	S2566	
♦MC1183	Nitron	NC1183	
♦MC1184	Nitron	NC1184	
MC1303	Raytheon	RC4739	
♦MC1304	Fairchild	μA732	
	National	LM1304	
♦MC1305	National	LM1305	
♦MC1307	Fairchild	μA767	
	National	LM1307	
MC1310	Exar	XR1310	
	Plessey	SL1310	
	RCA	CA1310	
	Sprague	ULN-2110	
		ULN-2211	
♦MC1311	Exar	XR1800	
	Fairchild	μA758	
	RCA	CA758	
	Sprague	ULN-2244	
MC1312	Fairchild	μA1312	
MC1324	Sprague	ULN-2224	
MC1327	Sprague	ULN-2217	
♦MC1328	RCA	CA3072	
	Sprague	ULN-2114	
		ULN-2228	
MC1329	Sprague	ULN-2229	
MC1330	Mitsubishi	M5169	
♦MC1339	Signetics	PA239	
MC1350	NPC	ESM1350	
MC1351	National	LM1351	
MC1352	Mitsubishi	M5183	
	RCA	CA1352	
	Sanyo	LA1352	
MC1353	Mitsubishi	M5784	
	Sanyo	LA1353	
MC1356	Sprague	ULN-2136	
MC1357	Fairchild	μA2136	
	RCA	CA2111	
	Signetics	ULN2111	
	Sprague	ULN-2111	
		ULN-2113	
MC1358	Fairchild	μA3065	
	RCA	CA3065	
	Sprague	ULN-2165	
MC1364	Fairchild	μA3064	
	RCA	CA3064	
	Sprague	ULN-2264	
♦MC1370	Fairchild	μA780	
	RCA	CA3070	
	Sprague	ULN-2124	
♦MC1371	Fairchild	μA781	
	RCA	CA3071	
	Sprague	ULN-2127	
MC1375	RCA	CA3075	
MC1389	RCA	CA3089	
	Sprague	ULN-2289	
MC1391	Fairchild	μA1391	
	RCA	CA1391	
	Sprague	ULN-2291	
MC1394	Fairchild	μA1394	
	RCA	CA1394	
	Sprague	ULN-2294	
MC1398	Mitsubishi	M5190	
	RCA	CA1398	
	Sprague	ULN-2298	
MC1399	Signetics	MC1399	
	Sprague	ULN-2299	
MC14000	Mitel	SIL4000	
	National	CD4000	
	RCA	CD4000	
	Solitron	CM4000	
	SSS	SCL4000	
	TI	TP4000	
MC14001	Fairchild	F4001	
	Mitel	SIL4001	
	National	CD4001	
	NEC America	μPD4001	

♦ Discontinued

The manufacturers report their devices can be used as direct replacements.
Performance details often differ, so compare the specifications considering your requirements.

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Manufacturer Device	Replacement Source	Device	IC Master Page
MC14001	RCA	CD4001	
	SGS	HBF4001	
	Solitron	CM4001	
	SSS	SCL4001	
	TI	TP4001	
	Toshiba	TC4001	
MC14002	Fairchild	F4002	
	Hitachi	HD14002	
	Mitel	SIL4002	
	National	CD4002	
	NEC America	μPD4002	
	RCA	CD4002	
	SGS	HBF4002	
	Solitron	CM4002	
	SSS	SCL4002	
	TI	TP4002	
	Toshiba	TC4002	
MC14006	Fairchild	F4006	
	National	CD4006	
	NEC America	μPD4006	
	RCA	CD4006	
	Solitron	CM4006	
	SSS	SCL4006	
MC14007	Fairchild	F4007	
	Mitel	SIL4007	
	National	CD4007	
	RCA	CD4007	
	SGS	HBF4007	
	Solitron	CM4007	
	SSS	SCL4007	
	TI	TP4007	
	Toshiba	TC4007	
MC14008	Fairchild	F4008	
	Hitachi	HD14008	
	National	CD4008	
	RCA	CD4008	
	SGS	HBF4008	
	Solitron	CM4008	
	SSS	SCL4008	
	TI	TP4008	
	Toshiba	TC4008	
MC14009	National	CD4009	
	RCA	CD4009	
	SSS	SCL4009	
MC14010	National	CD4010	
	RCA	CD4010	
	SSS	SCL4010	
MC14011	Fairchild	F4011	
	Hitachi	HD14011	
	Mitel	SIL4011	
	National	CD4011	
	NEC America	μPD4011	
	RCA	CD4011	
	SGS	HBF4011	
	Solitron	CM4011	
	SSS	SCL4011	
	TI	TP4011	
	Toshiba	TC4011	
MC14012	Fairchild	F4012	
	Hitachi	HD14012	
	Mitel	SIL4012	
	National	CD4012	
	NEC America	μPD4012	
	RCA	CD4012	
	SGS	HBF4012	
	Solitron	CM4012	
	SSS	SCL4012	
	TI	TP4012	
	Toshiba	TC4012	
MC14013	Fairchild	F4013	
	Hitachi	HD14013	
	Mitel	SIL4013	
	National	CD4013	
	NEC America	μPD4013	
	RCA	CD4013	
	SGS	HBF4013	
	Solitron	CM4013	
	SSS	SCL4013	
	TI	TP4013	
	Toshiba	TC4013	
MC14014	Fairchild	F4014	
	Hitachi	HD14014	
MC14014	Mitel	SIL4014	
	National	CD4014	
	NEC America	μPD4014	
	RCA	CD4014	
	SGS	HBF4014	
	Solitron	CM4014	
	SSS	SCL4014	
	TI	TP4014	
	Toshiba	TC4014	
MC14015	Fairchild	F4015	
	Hitachi	HD14015	
	Mitel	SIL4015	
	National	CD4015	
	NEC America	μPD4015	
	RCA	CD4015	
	SGS	HBF4015	
	Solitron	CM4015	
	SSS	SCL4015	
	TI	TP4015	
	Toshiba	TC4015	
MC14016	AD	AD7516	
	Fairchild	F4016	
	Hitachi	HD14016	
	Micro Power	MPS7516	
	Mitel	SIL4016	
	National	**CD4016**	**1076**
	RCA	CD4016	
	Solitron	CM4016	
	SSS	SCL4016	
	TI	TP4016	
MC14017	Fairchild	F4017	
	Hitachi	HD14017	
	Mitel	SIL4017	
	National	CD4017	
	NEC America	μPD4017	
	RCA	CD4017	
	SGS	HBF4017	
	Solitron	CM4017	
	SSS	SCL4017	
	TI	TP4017	
	Toshiba	TC4017	
MC14018	TI	TP4018	
MC14020	Fairchild	F4020	
	Hitachi	HD14020	
	Mitel	SIL4020	
	National	CD4020	
	NEC America	μPD4020	
	RCA	CD4020	
	SGS	HBF4020	
	Solitron	CM4020	
	SSS	SCL4020	
	TI	TP4020	
	Toshiba	TC4020	
MC14021	Fairchild	F4021	
	Hitachi	HD14021	
	Mitel	SIL4021	
	National	CD4021	
	NEC America	μPD4021	
	RCA	CD4021	
	Solitron	CM4021	
	SSS	SCL4021	
	TI	TP4021	
	Toshiba	TC4021	
MC14022	Fairchild	F4022	
	Mitel	SIL4022	
	National	CD4022	
	RCA	CD4022	
	SGS	HBF4022	
	Solitron	CM4022	
	SSS	SCL4022	
	TI	TP4022	
	Toshiba	TC4022	
MC14023	Fairchild	F4023	
	Hitachi	HD14023	
	Mitel	SIL4023	
	National	CD4023	
	NEC America	μPD4023	
	RCA	CD4023	
	SGS	HBF4023	
	Solitron	CM4023	
	SSS	SCL4023	
	TI	TP4023	
	Toshiba	TC4023	
MC14024	Fairchild	F4024	
	Hitachi	HD14024	
	Mitel	SIL4024	
	National	CD4024	
MC14024	NEC America	μPD4024	
	RCA	CD4024	
	SGS	HBF4024	
	Solitron	CM4024	
	SSS	SCL4024	
	TI	TP4024	
	Toshiba	TC4024	
MC14025	Fairchild	F4025	
	Hitachi	HD14025	
	Mitel	SIL4025	
	National	CD4025	
	NEC America	μPD4025	
	RCA	CD4025	
	SGS	HBF4025	
	Solitron	CM4025	
	SSS	SCL4025	
	TI	TP4025	
	Toshiba	TC4025	
MC14027	Fairchild	F4027	
	Hitachi	HD14027	
	Mitel	SIL4027	
	National	CD4027	
	NEC America	μPD4027	
	RCA	CD4027	
	SGS	HBF4027	
	Solitron	CM4027	
	SSS	SCL4027	
	TI	TP4027	
	Toshiba	TC4027	
MC14028	Fairchild	F4028	
	Hitachi	HD14028	
	Mitel	SIL4028	
	National	CD4028	
	NEC America	μPD4028	
	RCA	CD4028	
	SGS	HBF4028	
	Solitron	CM4028	
	SSS	SCL4028	
	TI	TP4028	
	Toshiba	TC4028	
MC14032	RCA	CD4032	
	Solitron	CM4032	
	Toshiba	TC4032	
MC14034	Fairchild	F4034	
	Hitachi	HD14034	
	National	CD4034	
	NEC America	μPD4034	
	RCA	CD4034	
	Solitron	CM4034	
	SSS	SCL4034	
	Toshiba	TC4034	
MC14035	Fairchild	F4035	
	Hitachi	HD14035	
	Mitel	SIL4035	
	National	CD4035	
	NEC America	μPD4035	
	RCA	CD4035	
	SGS	HBF4035	
	Solitron	CM4035	
	SSS	SCL4035	
	TI	TP4035	
	Toshiba	TC4035	
MC14038	RCA	CD4038	
	Toshiba	TC4038	
MC14040	Fairchild	F4040	
	Hitachi	HD14040	
	National	CD4040	
	RCA	CD4040	
	SSS	SCL4040	
	TI	TP4040	
	Toshiba	TC4040	
MC14042	Fairchild	F4042	
	Hitachi	HD14042	
	Mitel	SIL4042	
	National	CD4042	
	NEC America	μPD4042	
	RCA	CD4042	
	SGS	HBF4042	
	Solitron	CM4042	
	SSS	SCL4042	
	TI	TP4042	
	Toshiba	TC4042	
MC14043	Fairchild	F4043	
	Hitachi	HD14043	
	Mitel	SIL4043	
	National	CD4043	
MC14043	NEC America	μPD4043	
	RCA	CD4043	
	Solitron	CM4043	
	SSS	SCL4043	
	TI	TP4043	
	Toshiba	TC4043	
MC14044	Fairchild	F4044	
	Hitachi	HD14044	
	Mitel	SIL4044	
	National	CD4044	
	NEC America	μPD4044	
	RCA	CD4044	
	Solitron	CM4044	
	SSS	SCL4044	
	TI	TP4044	
	Toshiba	TC4044	
MC14046	Fairchild	F4046	
	Mitel	SIL4046	
	National	CD4046	
	RCA	CD4046	
	Solitron	CM4046	
	SSS	SCL4046	
MC14049	Fairchild	F4049	
	Hitachi	HD14049	
	Mitel	SIL4049	
	National	CD4049	
	NEC America	μPD4049	
	RCA	CD4009	
		CD4049	
	SGS	HBF4049	
	Solitron	CM4049	
	SSS	SCL4049	
	TI	TP4049	
	Toshiba	TC4049	
MC14050	Fairchild	F4050	
	Hitachi	HD14050	
	Mitel	SIL4050	
	National	CD4050	
	NEC America	μPD4050	
	RCA	CD4010	
		CD4050	
	SGS	HBF4050	
	Solitron	CM4050	
	SSS	SCL4050	
	TI	TP4050	
	Toshiba	TC4050	
MC14051	Fairchild	F4051	
	Hitachi	HD14051	
	Mitel	SIL4051	
	National	CD4051	
	NEC America	μPD4051	
	RCA	CD4051	
	Solitron	CM4051	
	SSS	SCL4051	
	TI	TP4051	
	Toshiba	TC4051	
MC14052	Fairchild	F4052	
	Hitachi	HD14052	
	Mitel	SIL4052	
	National	CD4052	
	NEC America	μPD4052	
	RCA	CD4052	
	Solitron	CM4052	
	SSS	SCL4052	
	TI	TP4052	
	Toshiba	TC4052	
MC14053	Fairchild	F4053	
	Hitachi	HD14053	
	Mitel	SIL4053	
	National	CD4053	
	NEC America	μPD4053	
	RCA	CD4053	
	Solitron	CM4053	
	SSS	SCL4053	
	TI	TP4053	
	Toshiba	TC4053	
MC1406	Signetics	MC1406	
MC14066	Fairchild	F4066	
	Hitachi	HD14066	
	Mitel	SIL4066	
	National	**CD4066**	**1076**
	NEC America	μPD4066	
	RCA	CD4063	
		CD4066	
	SGS	HBF4066	
	Signetics	N4066	

◆ Discontinued

Bold face device numbers indicate manufacturers data is provided in the IC Master on the pages noted.

Motorola Semiconductor (cont'd)

Manufacturer Device	Replacement Source	Device	IC Master Page
MC14066	Solitron	CM4066	
	SSS	SCL4066	
	Toshiba	TC4066	
MC14068	Fairchild	F4068	
	Hitachi	HD14068	
	Mitel	SIL4068	
	NEC America	μPD4068	
	RCA	CD4068	
	Solitron	CM4068	
	SSS	SCL4068	
	TI	TP4068	
	Toshiba	TC4068	
MC14069	Fairchild	F4069	
	Harris	HD74C04	
	Hitachi	HD14069	
	Mitel	SIL4069	
	National	CD4069	
		MM74C04	
	NEC America	μPD4069	
	RCA	CD4069	
	Solitron	CM4069	
	SSS	SCL4069	
	TI	TP4069	
	Toshiba	TC4069	
MC14070	Hitachi	HD14070	
	RCA	CD4070	
	SSS	SCL4070	
MC14071	Fairchild	F4071	
	Hitachi	HD14071	
	Mitel	SIL4071	
	National	CD4071	
	NEC America	μPD4071	
	RCA	CD4071	
	Solitron	CM4071	
	SSS	SCL4071	
	TI	TP4071	
	Toshiba	TC4071	
MC14072	Fairchild	F4072	
	Hitachi	HD14072	
	Mitel	SIL4072	
	NEC America	μPD4072	
	RCA	CD4072	
	SSS	SCL4072	
	TI	TP4072	
	Toshiba	TC4072	
MC14073	Fairchild	F4073	
	Hitachi	HD14073	
	Mitel	SIL4073	
	National	CD4073	
	NEC America	μPD4073	
	RCA	CD4073	
	Solitron	CM4073	
	SSS	SCL4073	
	TI	TP4073	
	Toshiba	TC4073	
MC14075	Fairchild	F4075	
	Hitachi	HD14075	
	Mitel	SIL4075	
	National	CD4075	
	NEC America	μPD4075	
	RCA	CD4075	
	SSS	SCL4075	
	TI	TP4075	
	Toshiba	TC4075	
MC14076	Fairchild	F4076	
	Harris	HD74C173	
	Mitel	SIL4076	
	National	CD4076	
		MM74C173	
	RCA	CD4076	
	Solitron	CM4076	
	SSS	SCL4076	
MC14077	Fairchild	F4077	
	Hitachi	HD14077	
	Mitel	SIL4077	
	RCA	CD4077	
	Solitron	CM4077	
	SSS	SCL4077	
MC14078	Fairchild	F4078	
	Hitachi	HD14078	
	Mitel	SIL4078	
	NEC America	μPD4078	
MC14078	RCA	CD4078	
	Solitron	CM4078	
	SSS	SCL4078	
	TI	TP4078	
	Toshiba	TC4078	
MC1408	AD	AD1408	
		AD559	
	AMD	SSS1408	
	Datel	**DAC-IC8BC**	**671**
	Fairchild	μA0802C	
	PMI	SSS1408	
	Signetics	MC1408	
MC14081	Fairchild	F4081	
	Hitachi	HD14081	
	Mitel	SIL4081	
	National	CD4081	
	NEC America	μPD4081	
	RCA	CD4081	
	Solitron	CM4081	
	SSS	SCL4081	
	TI	TP4081	
	Toshiba	TC4081	
MC14082	Fairchild	F4082	
	Hitachi	HD14082	
	Mitel	SIL4082	
	NEC America	μPD4082	
	RCA	CD4082	
	SSS	SCL4082	
	TI	TP4082	
	Toshiba	TC4082	
MC14093	Fairchild	F4093	
	National	CD4093	
	NEC America	μPD4093	
	RCA	CD4093	
MC1411	Signetics	NE5501	
		ULN2001	
	Silicon G	SG2001	
	Sprague	ULN-2001	
	TI	ULN2001	
MC1412	Signetics	NE5502	
		ULN2002	
	Sprague	ULN-2002	
	TI	ULN2002	
MC1413	Signetics	NE5503	
		ULN2003	
	Sprague	ULN-2003	
	TI	ULN2003	
MC1414	National	LM1414	
	Raytheon	RC1414	
	TI	TL514	
MC1416	Signetics	NE5504	
		ULN2004	
	TI	ULN2004	
MC14160	Fairchild	F40160	
	SSS	SCL4160	
	TI	TP4360	
MC14161	Fairchild	F40161	
	SSS	SCL4161	
	TI	TP4361	
MC14162	Fairchild	F40162	
	SSS	SCL4162	
	TI	TP4362	
MC14163	Fairchild	F40163	
	SSS	SCL4163	
	TI	TP4363	
MC14174	Fairchild	F40174	
	Hitachi	HD14174	
MC14175	Hitachi	HD14175	
	NEC America	μPD4175	
	Toshiba	TC40175	
MC14194	Fairchild	F40194	
	Hitachi	HD14194	
	NEC America	μPD4194	
MC14308	RCA	CD4038	
	Solitron	CM4038	
	Toshiba	TC4038	
MC1436	**Harris**	**HA-2645**	**984**
	National	LM1436	
	Silicon G	SG1436	
MC1437	Raytheon	RC1437	
♦MC1441	RCA	CA1541	
MC14501	Hitachi	HD14501	
	NEC America	μPD4501	
	RCA	CD4068	
MC14502	Hitachi	HD14502	
	Mitel	SIL4502	
MC14502	RCA	CD4502	
	SSS	SCL4502	
MC14503	National	CD4503	
	NEC America	μPD4503	
MC14506	RCA	CD4085	
MC14507	National	CD4070	
		CD4507	
		MM74C86	
	RCA	CD4030	
		CD4070	
		CD4070A	
	SSS	SCL4030	
	TI	TP4507	
MC14508	Hitachi	HD14508	
	Mitel	SIL4508	
	NEC America	μPD4508	
	RCA	CD4508	
	Solitron	CM4508	
	SSS	SCL4508	
	Toshiba	TC4508	
MC14510	Fairchild	F4510	
	Mitel	SIL4510	
	National	CD4510	
	NEC America	μPD4510	
	RCA	CD40192	
		CD4510	
	SSS	SCL4510	
	Toshiba	TC4510	
MC14511	Fairchild	F4511	
	Hitachi	HD14511	
	Mitel	SIL4511	
	National	CD4511	
	NEC America	μPD4511	
	RCA	CD4511	
	Solitron	CM4511	
	SSS	SCL4511	
	TI	TP4511	
MC14512	Fairchild	F4512	
	Hitachi	HD14512	
	Mitel	SIL4512	
	National	CD4512	
	NEC America	μPD4512	
	SSS	SCL4512	
	TI	TP4512	
	Toshiba	TC4512	
MC14514	Fairchild	F4514	
	Mitel	SIL4514	
	National	CD4514	
	NEC America	μPD4514	
	RCA	CD4514	
	Solitron	CM4514	
	SSS	SCL4514	
	Toshiba	TC4514	
MC14515	Fairchild	F4515	
	Hitachi	HD14515	
	Mitel	SIL4515	
	National	CD4515	
	NEC America	μPD4515	
	RCA	CD4515	
	Solitron	CM4515	
	SSS	SCL4515	
	Toshiba	TC4515	
MC14516	Fairchild	F4516	
	Hitachi	HD14516	
	Mitel	SIL4516	
	National	CD4516	
	NEC America	μPD4516	
	RCA	CD40193	
		CD4516	
	SSS	SCL4516	
	Toshiba	TC4516	
MC14517	NEC America	μPD4517	
	SSS	SCL4517	
MC14518	Fairchild	F4518	
	Mitel	SIL4518	
	National	CD4518	
	NEC America	μPD4518	
	RCA	CD4518	
	Solitron	CM4518	
	SSS	SCL4518	
	TI	TP4518	
	Toshiba	TC4518	
MC14519	Fairchild	F4519	
	Hitachi	HD14519	
	National	CD4519	
	NEC America	μPD4519	
MC14519	RCA	CD4019	
	TI	TP4519	
MC14520	Fairchild	F4520	
	Hitachi	HD14520	
	Mitel	SIL4520	
	National	CD4520	
	NEC America	μPD4520	
	RCA	CD4520	
	Solitron	CM4520	
	SSS	SCL4520	
	TI	TP4520	
	Toshiba	TC4520	
MC14522	Fairchild	F4522	
	National	CD4522	
	NEC America	μPD4522	
	RCA	CD4018	
	SSS	SCL4522	
	TI	TP4522	
MC14526	Fairchild	F4526	
	NEC America	μPD4526	
	SSS	SCL4526	
	TI	TP4526	
MC14527	National	CD4527	
	RCA	CD4527	
	SSS	SCL4527	
MC14528	Fairchild	F4528	
	Hitachi	HD14528	
	National	CD4528	
	NEC America	μPD4528	
	RCA	CD4528	
	SSS	SCL4528	
	Toshiba	TC4528	
MC14529	National	CD4529	
	RCA	CD4067	
MC14530	NEC America	μPD4530	
MC14531	Fairchild	F4531	
	RCA	CD40101	
	SSS	SCL4531	
	TI	TP4531	
MC14532	Fairchild	F4532	
	Hitachi	HD14532	
	NEC America	μPD4532	
	RCA	CD4532	
	Toshiba	TC4532	
MC14538	OKI	MSM4538	
	SSS	SCL4538	
MC14539	Fairchild	F4539	
	NEC America	μPD4539	
	OKI	MSM4539	
	Toshiba	TC4539	
MC14543	National	CD4543	
	RCA	CD4056	
	SSS	SCL4543	
	Toshiba	TC4543	
MC1455	AMD	NE555	
	Cherry	CS555	
	Exar	XR555	
	Fairchild	μA555	
	Raytheon	RC555	
	RCA	CA555	
	Signetics	NE555	
	Silicon G	SG555	
	TI	NE555	
MC14553	Fairchild	F4553	
MC14555	Fairchild	F4555	
	Hitachi	HD14555	
	NEC America	μPD4555	
	RCA	CD4555	
	SSS	SCL4555	
MC14556	Fairchild	F4556	
	NEC America	μPD4556	
	RCA	CD4556	
	SSS	SCL4556	
MC14557	Fairchild	F4557	
	RCA	CD4031	
MC14558	RCA	CD4055	
MC1456	**Harris**	**HA-2605**	**976**
	Raytheon	RC1556	
	Signetics	MC1456	
	Silicon G	SG1456	
MC14560	Hitachi	HD14560	
	NEC America	μPD4560	
	Toshiba	TC4560	
MC14561	Hitachi	HD14561	
	NEC America	μPD4561	
	Toshiba	TC4561	

♦ Discontinued

The manufacturers report their devices can be used as direct replacements.
Performance details often differ, so compare the specifications considering your requirements.

Motorola Semiconductor (cont'd)

Manufacturer Device	Replacement Source	Device	IC Master Page
MC14562	RCA	CD4062	
MC14569	RCA	CD4059	
MC14572	Hitachi	HD14572	
MC1458	AMD	AM1458	
	Exar	XR1458	
	Fairchild	μA1458	
	Harris	**HA-2655**	**986**
	National	LM1458	
	NEC America	μPC1458	
	PMI	OP-17	
		SSS1458	
	Raytheon	RC1458	
		RC4558	
	RCA	CA1458	
	Signetics	MC1458	
	Silicon G	SG1458	
	TI	MC1458	
MC14580	RCA	CD40108	
MC14581	RCA	CD40181	
		CD4057	
	SSS	SCL4581	
	TI	TP4581	
MC14582	Fairchild	F4582	
	RCA	CD40182	
	SSS	SCL4582	
	TI	TP4582	
MC14583	Fairchild	F4583	
	Hitachi	HD14583	
	OKI	MSM4583	
	RCA	CD40100	
	Toshiba	TC4583	
MC14584	Hitachi	HD14584	
	National	CD40106	
		CD4584	
		MM74C14	**262**
	NEC America	μPD4584	
	OKI	MSM4584	
	RCA	CD40106	
		CD4016	
	SSS	SCL4584	
MC14585	Hitachi	HD14585	
	National	MM74C85	
	RCA	CD4063	
	SSS	HD14585	
		SCL4585	
	Toshiba	TC4585	
MC1461	Toshiba	TA7084	
MC1463	Toshiba	TA7085	
MC1468	Exar	XR1468	
	Raytheon	RC4195	
	Silicon G	SG1468	
MC1471	Sprague	UDN-5711	
MC1472	Sprague	UDN-5712	
MC1473	Sprague	UDN-5713	
MC1474	Sprague	UDN-5714	
MC1488	AMD	MC1488	
	Exar	XR1488	
	National	DS1488	
	Raytheon	RC1488	
		RM1488	
	Signetics	MC1488	
	Silicon G	SG1488	
	TI	MC1488	
		SN75188	
MC1489	AMD	MC1489	
	Exar	XR1489	
	National	DS1489	
	Raytheon	RC1489	
	Signetics	MC1489	
	Silicon G	SG1489	
	TI	MC1489	
		SN75189	
MC1489A	Exar	XR1489A	
MC1495	Intech/FMI	A8495	
		A8595	
	Plessey	SL1495	
	Silicon G	SG1495	
MC1496	Fairchild	μA796	
	Plessey	SL1496	
	Signetics	MC1496	
	Silicon G	SG1496	
MC1508	AD	AD1508	
	AD	AD559	
	AMD	SSS1508	
	Datel	**DAC-IC8BM**	**671**
	Fairchild	MA0802M	
	PMI	SSS1508	
	Signetics	MC1508	
MC1510	TI	SN75189	
MC1514	National	LM1514	
	Raytheon	RM1514	
	TI	TL514	
MC1536	**Harris**	**HA-2640**	**984**
	National	LM1536	
	Silicon G	SG1536	
MC1537	Raytheon	RM1537	
MC1539	Sprague	ULS-2139	
♦MC1541	RCA	CA1541	
MC1555	AMD	SE555	
	Cherry	CS555	
	Exar	XR555M	
	NEC America	μPC1555	
	Raytheon	RM555	
	RCA	CA555	
	Signetics	SE555	
	Silicon G	SG555	
	TI	NE555	
MC1556	**Harris**	**HA-2600**	**976**
	Raytheon	RM1556	
		RM1556A	
	Signetics	MC1556	
	Silicon G	SG1556	
MC1558	AMD	1558	
	Exar	XR1558	
	Fairchild	μA1558	
	Harris	**HA-2650**	**986**
	National	LM1558	
	PMI	PM1558	
		SSS1558	
	Raytheon	RM1558	
		RM4558	
	RCA	CA1558	
	Signetics	MC1558	
	Silicon G	SG1558	
	TI	MC1558	
MC1568	Exar	XR1568	
	Raytheon	RM4195	
	Silicon G	SG1568	
MC1595	Intech/FMI	A8495	
		A8595	
	Plessey	SL1595	
	Silicon G	SG1595	
MC1596	Fairchild	μA796	
	National	LM1596	
	Plessey	SL1596	
	Signetics	MC1596	
	Silicon G	SG1596	
MC1648	Plessey	SP1648	
MC1650	Plessey	SP1650	
MC1651	Plessey	SP1651	
MC1658	Fairchild	11C58	
	Plessey	SP1658	
MC1660	Plessey	SP1660	
MC1661	Plessey	SL1661	
MC1662	Plessey	SP1662	
MC1663	Plessey	SL1663	
MC1664	Plessey	SP1664	
MC1665	Plessey	SL1665	
MC1666	Plessey	SP1666	
MC1667	Plessey	SL1667	
MC1668	Plessey	SP1668	
MC1669	Plessey	SL1669	
MC1670	Fairchild	11C70	
	Plessey	SP1670	
MC1671	Plessey	SL1671	
MC1672	Plessey	SP1672	
MC1673	Plessey	SL1673	
MC1674	Plessey	SP1674	
MC1675	Plessey	SL1675	
MC1688	Fairchild	11C01	
MC1690	Fairchild	11C06C	
	Plessey	SP1690	
MC1692	Plessey	SP1692	
MC1709	Fairchild	μA709	
	National	LM1709	
		LM709	**1035**
	NEC America	μPC55A	
	Raytheon	RC709	
MC1709	Raytheon	RM709	
	Signetics	μA709	
	TI	μA709	
	Toshiba	TA7502	
MC1710	Fairchild	μA710	
	National	LM710	
	Raytheon	RC710	
		RM710	
	Silicon G	SG1710	
	TI	μA710	
MC1711	Fairchild	μA711	
	National	LM711	
	Raytheon	RC711	
		RM711	
	Signetics	μA711	
	Silicon G	SG711	
	TI	μA711	
MC1712	Fairchild	μA702	
	NEC America	μPC51	
		μPC51A	
	Raytheon	RC702	
		RM702	
	TI	μA702	
MC1723	AMD	723	
	Fairchild	**μA723**	**934**
	Intersil	723	
	National	LM723	
	Raytheon	RC723	
		RM723	
	RCA	CA723	
	Signetics	μA723	
	Silicon G	SG723	
	TI	μA723	
MC1732	RCA	CA723	
MC1733	AMD	733	
	National	LM733	
	Raytheon	RC733	
		RM733	
	Signetics	μA733	
	Silicon G	SG733	
	TI	μA733	
MC1741	AMD	741	
	Fairchild	μA741	
	Intersil	741	
	National	**LM741**	**1035**
	PMI	OP-02	
		PM741	
		SSS741	
	Raytheon	RC741	
		RM741	
	RCA	CA741	
	Signetics	μA741	
	Sprague	ULN-2151	
	TI	μA741	
	Toshiba	TA7504	
MC1747	AMD	747	
	Fairchild	μA747	
	NEC America	μPC251	
	PMI	PM747	
	Raytheon	RC747	
		RM747	
	RCA	CA747	
	Signetics	μA747	
	Silicon G	SG747	
	Teledyne S	747	
	TI	μA747	
MC1748	AMD	748	
	Fairchild	μA748	
	Intersil	748	
	National	LM748	
	Raytheon	RC748	
		RM748	
	RCA	CA748	
	Signetics	μA748	
	Silicon G	SG748	
	TI	μA748	
MC1776	Fairchild	μA776	
MC1800	National	DM1800	
	TI	SN151800	
MC1801	National	DM1801	
	TI	SN151801	
MC1802	TI	SN151802	
MC1803	TI	SN151803	
MC1804	TI	SN151804	
MC1805	TI	SN151805	
MC1806	TI	SN151806	
MC1807	TI	SN151807	
MC1808	TI	SN151808	
MC1809	TI	SN151809	
MC1810	TI	SN151810	
MC1811	TI	SN151811	
MC1812	TI	SN151812	
MC1900	TI	SN151900	
MC1901	TI	SN151901	
MC1902	TI	SN151902	
MC1903	TI	SN151903	
MC1904	TI	SN151904	
MC1905	TI	SN151905	
MC1906	TI	SN151906	
MC1907	TI	SN151907	
MC1908	TI	SN151908	
MC1909	TI	SN151909	
MC1910	TI	SN151910	
MC1911	TI	SN151911	
MC1912	TI	SN151912	
MC2114	Rockwell	R2114	
MC2257	Nitron	NC2257	
MC2259	Nitron	NC2259	
MC2260	Nitron	NC2260	
MC26S10	AMD	AM26S10	
MC2901	AMD	AM2901	
	NEC Micro	μPB2901A	
	Raytheon	AM2901	
MC2901A	NEC Micro	μPB2901A	
MC2902	AMD	AM2902	
	NEC Micro	μPB2902A	
	Raytheon	AM2902	
MC2905	AMD	AM2905	
	NEC Micro	μPB2905A	
	Raytheon	AM2905	
MC2906	AMD	AM2906	
	NEC Micro	μPB2906A	
	Raytheon	AM2906	
MC2907	AMD	AM2907	
	NEC Micro	μPB2907A	
	Raytheon	AM2907	
MC2909	AMD	AM2909	
	NEC Micro	μPB2909A	
	Raytheon	AM2909	
MC2911	AMD	AM2911	
	NEC Micro	μPB2911A	
	Raytheon	AM2911	
MC2915A	AMD	AM2915A	
	NEC Micro	μPB2915A	
MC2916A	AMD	AM2916A	
	NEC Micro	μPB2916A	
MC2917A	AMD	AM2917A	
	NEC Micro	μPB2917A	
	OEI	μPB2917A	
MC2918	AMD	AM2918	
	NEC Micro	μPB2918A	
	OEI	μPB2918A	
	Raytheon	AM2918	
MC3000	Fairchild	74H00	
	TI	SN74H00	
MC3001	Fairchild	74H08	
	TI	SN7408	
MC3003	TI	SN7432	
MC3004	Fairchild	74H01	
	TI	SN74H01	
MC3005	Fairchild	74H10	
	TI	SN74H10	
MC3006	Fairchild	74H11	
	TI	SN74H11	
MC3008	Fairchild	74H04	
	TI	SN74H04	
MC3009	Fairchild	74H05	
	TI	SN74H05	
MC3010	Fairchild	74H20	
	TI	SN74H20	
MC3011	Fairchild	74H21	
	TI	SN74H21	
MC3012	Fairchild	74H22	
	TI	SN74H22	
MC3015	TI	SN74H30	
MC3016	Fairchild	74H30	
	TI	SN74430	
MC3018	Fairchild	74H62	
	TI	SN74H62	
MC3019	Fairchild	74H61	
	TI	SN74H61	
MC3020	Fairchild	74H50	

♦ Discontinued

Bold face device numbers indicate manufacturers data is provided in the IC Master on the pages noted.

Motorola Semiconductor (cont'd)

Manufacturer Device	Replacement Source	Device	IC Master Page
MC3020	TI	SN74H50	
MC3021	TI	SN74S86	
MC3023	Fairchild	74H51	
	TI	SN74H51	
MC3024	Fairchild	74H40	
	TI	SN74H40	
MC3025	TI	SN74H40	
MC3030	Fairchild	74H60	
	TI	SN74H60	
MC3031	Fairchild	74H52	
	TI	SN74H52	
MC3032	Fairchild	74H53	
	TI	SN74H53	
MC3033	Fairchild	74H54	
	TI	SN74H54	
MC3034	Fairchild	74H55	
	TI	SN74H55	
MC3054	Fairchild	74H71	
	TI	SN74H71	
MC3055	Fairchild	74H72	
	TI	SN74H72	
MC3060	TI	SN74H74	
MC3061	Fairchild	74S114	
	TI	SN74S114	
MC3062	Fairchild	74S113	
	TI	SN74S113	
MC3063	Fairchild	74H73	
	TI	SN74H73	
MC3100	Fairchild	54H00	
	TI	SN54H00	
MC3101	Fairchild	5408	
	TI	SN5408	
MC3103	Fairchild	5432	
	TI	SN5432	
MC3104	Fairchild	54H01	
	TI	SN54H01	
MC3105	Fairchild	54H10	
	TI	SN54H10	
MC3106	TI	SN54H11	
MC3108	Fairchild	54H04	
	TI	SN54H04	
MC3109	Fairchild	54H05	
	TI	SN54H05	
MC3110	Fairchild	54H20	
	TI	SN54H20	
MC3111	Fairchild	54H27	
	TI	SN54H21	
MC3112	Fairchild	54H22	
	TI	SN54H22	
MC3116	Fairchild	54H30	
	TI	SN54H30	
MC3118	Fairchild	54H62	
	TI	SN54H62	
MC3119	Fairchild	54H61	
	TI	SN54H61	
MC3120	Fairchild	54H50	
	TI	SN54H50	
MC3121	TI	SN54H86	
MC3123	Fairchild	54H51	
	TI	SN54H51	
MC3124	Fairchild	54H40	
	TI	SN54H40	
MC3125	Fairchild	54H40	
	TI	SN54H40	
MC3130	Fairchild	54H60	
	TI	SN54H60	
MC3131	Fairchild	54H52	
	TI	SN54H52	
MC3132	Fairchild	54H53	
	TI	SN54H53	
MC3133	Fairchild	54H54	
	TI	SN54H54	
MC3134	Fairchild	54H55	
	TI	SN54H55	
MC3154	Fairchild	54H71	
	TI	SN54H71	
MC3155	Fairchild	54H72	
	TI	SN54H72	
MC3160	Fairchild	54H74	
	TI	SN54H74	
MC3161	Fairchild	54S114	
	TI	SN54S114	
MC3162	Fairchild	54S113	
	TI	SN54S113	
MC3163	Fairchild	54H73	
	TI	SN54H73	
MC3301	Fairchild	μA3301	
	Hitachi	HA17301	
	Raytheon	LM2900	
		RC3301	
MC3302	Fairchild	μA3302	
	NEC America	μPC177	
	Raytheon	RC3302	
	RCA	CA339	
	Silicon G	SG3302	
	TI	LM3302	
MC3346	RCA	CA3046	
		CA3086	
MC3401	Fairchild	μA3401	
	Raytheon	LM3900	
		RC3401	
	RCA	CA3401	
MC3403	Exar	XR3403	
	Fairchild	μA3403C	
	Raytheon	RC3403	
		RC4137	
MC3403C	TI	MC3403C	
MC3403M	TI	MC3403M	
MC3410C	Datel	DAC-IC10B	
MC3416	Raytheon	RC4444	
MC3423	TI	MC3423	
MC3437	National	DS8837	
MC3438	National	DS8838	
MC3441	National	DS3651	
MC3443	National	DS3653	
	TI	MC3443	
MC3446	TI	MC3446	
MC3450	National	DS3650	
MC3452	National	DS3652	
MC3456	AMD	NE556	
	Exar	XR556	
	Signetics	NE556	
MC3460	National	DS3674	
MC3461	Hitachi	HD103461	
MC3486	National	DS3486	
MC3487	National	DS3487	
MC3503	Exar	XR3503	
	Fairchild	μA3503	
	Raytheon	RM3503	
		RM4137	
MC3523	TI	MC3523	
MC3556	AMD	SE556	
	Exar	XR556M	
MC4004	TI	SN7481A	
MC4005	Fairchild	93407	
	TI	SN7481	
MC4015	Raytheon	RL4015	
MC4024	Fairchild	11C24C	
MC4044	Fairchild	11C44C	
MC4064	MMI	6560	
	Signetics	**N82S16**	**1678**
MC4304	TI	SN5481A	
MC4305	TI	SN5481A	
MC4324	Fairchild	11C24	
MC4344	Fairchild	11C44	
MC4558	Exar	XR4558	
	Raytheon	RC4558	
MC4558C	NEC America	μPC4558	
MC4741	Exar	XR4741	
	Harris	HA-4741	
	National	**LM148**	**1035**
	NEC America	μPC4741	
MC5003	TI	SN74186	
MC5005	**TI**	**SN74S387**	**1708**
MC5303	TI	SN54186	
MC5400	Fairchild	5400	
	National	DM5400	
	Signetics	5400	
	TI	SN5400	
MC5401	Fairchild	5401	
	National	DM5401	
	Signetics	5401	
	TI	SN5401	
MC5402	Fairchild	5402	
	National	DM5402	
	Signetics	5402	
	TI	SN5402	
MC5403	Fairchild	5403	
MC5403	National	DM5403	
	Signetics	5403	
	TI	SN5403	
MC5404	Fairchild	5404	
	National	DM5404	
	Raytheon	5404	
	Signetics	5404	
	TI	SN5404	
MC5405	Fairchild	5405	
	National	DM5405	
	Signetics	5405	
	TI	SN5405	
MC5406	Fairchild	5406	
	National	DM5406	
	Signetics	5406	
	TI	SN5406	
MC5407	Fairchild	5407	
	National	DM5407	
	Signetics	5407	
	TI	SN5407	
MC5408	Fairchild	5408	
	National	DM5408	
	Signetics	5408	
	TI	SN5408	
MC5409	Fairchild	5409	
	National	DM5409	
	Signetics	5409	
	TI	SN5409	
MC5410	Fairchild	5410	
	National	DM5410	
	Signetics	5410	
	TI	SN5410	
MC54100	Signetics	54100	
	TI	SN54100	
MC54107	Fairchild	54107	
	National	DM54107	
	Signetics	54107	
	TI	SN54107	
MC54120	TI	SN54120	
MC54121	Fairchild	54121	
	National	DM54121	
	Signetics	54121	
	TI	SN54121	
MC54122	Fairchild	54122	
	TI	SN54122	
MC54123	AMD	SN54123	
	Fairchild	54123	
	National	DM54123	
	Signetics	54123	
	TI	SN54123	
MC5413	Fairchild	5413	
	National	DM5413	
	Signetics	5413	
	TI	SN5413	
MC54132	Fairchild	54132	
	National	DM54132	
	Signetics	54132	
	TI	SN54132	
MC5414	Fairchild	5414	
	National	DM5414	
	Signetics	5414	
	TI	SN5414	
MC54141	National	DM54141	
	TI	SN54141	
MC54145	Fairchild	54145	
	National	DM54145	
	Signetics	54145	
	TI	SN54145	
MC54150	Fairchild	54150	
	National	DM54150	
	Signetics	54150	
	TI	SN54150	
MC54151	Fairchild	54151	
	National	DM54151	
	Signetics	54151	
	TI	SN54151	
MC54152	Fairchild	54152	
	Signetics	54152	
	TI	SN54152	
MC54153	Fairchild	54153	
	National	DM54153	
	Signetics	54153	
	TI	SN54153	
MC54154	AMD	SN54154	
	Fairchild	54154	
	National	DM54154	
MC54154	Signetics	54154	
	TI	SN54154	
MC54155	Fairchild	54155	
	National	DM54155	
	Signetics	54155	
	TI	SN54155	
MC54156	Fairchild	54156	
	National	DM54156	
	Signetics	54156	
	TI	SN54156	
MC54157	AMD	SN54157	
	Fairchild	54157	
	National	DM54157	
	Signetics	54157	
	TI	SN54157	
MC5416	Fairchild	5416	
	National	DM5416	
	Signetics	5416	
	TI	SN5416	
MC54160	AMD	SN54160	
	Fairchild	54160	
	National	DM54160	
	Signetics	54160	
	TI	SN54160	
MC54161	AMD	SN54161	
	Fairchild	54161	
	National	DM54161	
	Signetics	54161	
	TI	SN54161	
MC54162	AMD	SN54162	
	Fairchild	54162	
	National	DM54162	
	Signetics	54162	
	TI	SN54162	
MC54163	AMD	SN54163	
	Fairchild	54163	
	National	DM54163	
	Signetics	54163	
	TI	SN54163	
♦MC54164	Raytheon	54164	
MC54165	Fairchild	54165	
	National	DM54165	
	Raytheon	54165	
	Signetics	54165	
	TI	SN54165	
MC54167	TI	SN54167	
MC5417	Fairchild	5417	
	National	DM5417	
	Signetics	5417	
	TI	SN5417	
MC54170	Fairchild	54170	
MC54174	AMD	SN74174	
	Fairchild	54174	
	National	DM54174	
	Signetics	54174	
	TI	SN54174	
MC54175	AMD	SN54175	
	Fairchild	54175	
	National	DM54175	
	Signetics	54175	
	TI	SN54175	
MC54176	Fairchild	54176	
	National	DM54176	
	Signetics	54176	
	TI	SN54176	
MC54177	Fairchild	54177	
	National	DM54177	
	Signetics	54177	
	TI	SN54177	
MC54180	Fairchild	54180	
	National	DM54180	
	Signetics	54180	
	TI	SN54180	
MC54181	AMD	SN54181	
	Fairchild	54181	
	National	DM54181	
	Signetics	54181	
	TI	SN54181	
MC54182	AMD	SN54182	
	Fairchild	54182	
	National	DM54182	
	Signetics	54182	
	TI	SN54182	
MC54190	Fairchild	54190	
	National	DM54190	
	Signetics	54190	

♦ Discontinued

The manufacturers report their devices can be used as direct replacements.
Performance details often differ, so compare the specifications considering your requirements.

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Manufacturer Device	Replacement Source	Device	IC Master Page
MC54190	TI	SN54190	
MC54191	Fairchild	54191	
	National	DM54191	
	Signetics	54191	
	TI	SN54191	
MC54192	AMD	SN54192	
	Fairchild	54192	
	National	DM54192	
	Signetics	54192	
	TI	SN54192	
MC54193	AMD	SN54193	
	Fairchild	54193	
	National	DM54193	
	Signetics	54193	
	TI	SN54193	
MC54194	AMD	SN54194	
	Fairchild	54194	
	National	DM54194	
	Signetics	54194	
	TI	SN54194	
MC54195	AMD	SN54195	
	Fairchild	54195	
	National	DM54195	
	Signetics	54195	
	TI	SN54195	
MC54196	Fairchild	54196	
	National	DM54196	
	Signetics	54196	
	TI	SN54196	
MC54197	Fairchild	54197	
	National	DM54197	
	Signetics	54197	
	TI	SN54197	
MC54198	Fairchild	54198	
MC54199	Fairchild	54199	
MC5420	Fairchild	5420	
	National	DM5420	
	Signetics	5420	
	TI	SN5420	
MC5423	Fairchild	5423	
	National	DM5423	
	TI	SN5423	
MC5425	Fairchild	5425	
	National	DM5425	
	TI	SN5425	
MC5426	Fairchild	5426	
	National	DM5426	
	Signetics	5426	
	TI	SN5426	
MC5427	Fairchild	5427	
	National	DM5427	
	TI	SN5427	
MC54283	Fairchild	54283	
MC54290	Fairchild	54290	
	TI	SN54290	
MC54293	Fairchild	54293	
	TI	SN54293	
MC54298	Fairchild	54298	
	Signetics	54298	
	TI	SN54298	
MC5430	Fairchild	5430	
	National	DM5430	
	Signetics	5430	
	TI	SN5430	
MC5437	Fairchild	5437	
	National	DM5437	
	Signetics	5437	
	TI	SN5437	
MC5438	Fairchild	5438	
	National	DM5438	
	Signetics	5438	
	TI	SN5438	
MC5440	Fairchild	5440	
	National	DM5440	
	Signetics	5440	
	TI	SN5440	
MC5442	Fairchild	5442	
	National	DM5442	
	Signetics	5442	
	TI	SN5442	
MC5443	Fairchild	5443	
	Signetics	5443	
MC5443	TI	SN5443	
MC5444	Fairchild	5444	
	Signetics	5444	
	TI	SN5444	
MC5445	Fairchild	5445	
	National	DM5445	
	Signetics	5445	
	TI	SN5445	
MC5446	Fairchild	5446	
	National	DM5446	
	Signetics	5446	
	TI	SN5446	
MC5447	Fairchild	5447	
	National	DM5447	
	Signetics	5447	
	TI	SN5447	
MC5448	Fairchild	5448	
	National	DM5448	
	Signetics	5448	
	TI	SN5448	
MC5449	Fairchild	5449	
	TI	SN5449	
MC5450	Fairchild	5450	
	National	DM5450	
	Signetics	5450	
	TI	SN5450	
MC5451	Fairchild	5451	
	National	DM5451	
	Signetics	5451	
	TI	SN5451	
MC5453	Fairchild	5453	
	National	DM5453	
	Signetics	5453	
	TI	SN5453	
MC5454	Fairchild	5454	
	National	DM5454	
	Signetics	5454	
	TI	SN5454	
MC5460	Fairchild	5460	
	National	DM5460	
	Signetics	5460	
	TI	SN5460	
MC5470	Fairchild	5470	
	National	DM5470	
	TI	SN5470	
MC5472	Fairchild	5472	
	National	DM5472	
	Signetics	5472	
	TI	SN5472	
MC5473	Fairchild	5473	
	National	DM5473	
	Signetics	5473	
	TI	SN5473	
MC5474	Fairchild	5474	
	National	DM5474	
	Signetics	5474	
	TI	SN5474	
MC5475	Fairchild	5475	
	National	DM5475	
	Signetics	5475	
	TI	SN5475	
MC5476	Fairchild	5476	
	National	DM5476	
	Signetics	5476	
	TI	SN5476	
MC5477	Fairchild	5477	
	Signetics	5477	
	TI	SN5477	
MC5480	Fairchild	5480	
	Signetics	5480	
	TI	SN5480	
MC5482	Fairchild	5482	
	TI	SN5482	
MC5485	Fairchild	5485	
	National	DM5485	
	Signetics	5485	
	TI	SN5485	
MC5486	Fairchild	5486	
	National	DM5486	
	Signetics	5486	
	TI	SN5486	
MC5490	Fairchild	5490	
	National	DM5490	
	Signetics	5490	
	TI	SN5490	
MC5491	Fairchild	5491	
MC5491	National	DM5491	
	Signetics	5491	
	TI	SN5491	
MC5492	Fairchild	5492	
	National	DM5492	
	Signetics	5492	
	TI	SN5492	
MC5493	Fairchild	5493	
	National	DM5493	
	TI	SN5493	
MC5494	Fairchild	5494	
	TI	SN5494	
MC5495	Fairchild	5495	
	National	DM5495	
	Signetics	5495	
	TI	SN5495	
MC5496	Fairchild	5496	
	National	DM5496	
	Signetics	5496	
	TI	SN5496	
MC5497	Fairchild	5497	
	TI	SN5497	
MC55107	AMD	SN55107	
	Fairchild	55107	
	National	DS55107	
	Raytheon	RM55107	
	TI	SN55107	
MC55108	AMD	SN55108	
	Fairchild	55108	
	National	DS55108	
	Raytheon	RM55108	
	TI	SN55108	
♦MC55109	AMD	SN55109	
	Fairchild	55109	
	Raytheon	RM55109	
	TI	SN55109	
♦MC55110	AMD	SN55110	
	Fairchild	55110	
	Raytheon	RM55110	
	TI	SN55110	
♦MC5522	National	DS5522	
	TI	SN5522	
MC5523	TI	SN5522	
MC5524	AMD	SN5524	
	National	DS5524	
	TI	SN5524	
MC5525	AMD	SN5525	
	TI	SN5524	
MC5528	Fairchild	5528	
	TI	SN5528	
MC5529	Fairchild	5529	
	TI	SN5528	
MC55325	AMD	SN55325	
	Fairchild	55325	
	TI	SN55325	
MC5534	Fairchild	5534	
MC5535	Fairchild	5535	
MC574	Raytheon	5474	
MC6002	TI	TMS4062	
MC68A00	**AMI**	**S68A00**	**1780**
MC68A10	**AMI**	**S68A10**	**1794**
	Fujitsu	MBL6800E	
MC68A21	**AMI**	**S68A21**	**1798**
MC68A332	**Signetics**	**2632**	**1672**
MC68A50	**AMI**	**S68A50**	**1818**
	Fujitsu	MBL6850E	
MC68B00	**AMI**	**S68B00**	**1780**
MC68B10	**AMI**	**S68B10**	**1794**
MC68B21	**AMI**	**S68B21**	**1798**
MC68B50	**AMI**	**S68B50**	**1818**
MC6800	**AMI**	**S6800**	**1776,1780**
	Fairchild	**F6800**	**1886,1888**
		F6800A	
	Hitachi	HD46800	
MC6802	**AMI**	**S6802**	**1785**
	Fairchild	**F6802**	**1887,1888**
	Hitachi	HD46802	
MC6810	**AMI**	**S6810**	**1790**
	Fairchild	**F6810**	**1887,1888**
MC6820	**AMI**	**S6820**	**1802**
	Fairchild	F6820A	
	Hitachi	HD46820	
	Rockwell	R6520	
MC6821	AMI	S6821	1798,1802
	Fairchild	**F6821**	**1887,1889**
	Fujitsu	MBL6821	
MC6821	Hitachi	HD46821	
	Rockwell	R6520	
MC68316	Rockwell	R2316	
MC68332	Rockwell	R2332	
MC6840	**AMI**	**S6840**	**1813**
	Fairchild	**F6840**	**1887,1890**
	Fujitsu	MBL6840	
MC6843	Hitachi	HD46503	
MC6844	Hitachi	HD46504	
MC6845	Hitachi	HD46505	
	Rockwell	R6545	
MC6846	**AMI**	**S6846**	**1817**
	Fairchild	**F6846**	**1887,1890**
	Fujitsu	MBL6846	
	Hitachi	HD46846	
MC68488	**AMI**	**S68488**	**1834**
	Fairchild	**F68488**	**1887,1890**
	Fujitsu	MBL68488	
MC6850	**AMI**	**S6850**	**1818**
	Fairchild	**F6850**	**1887,1891**
	Hitachi	HD46850	
	Rockwell	R6551	
	SMC	COM2502	
MC6852	**AMI**	**S6852**	**1822**
	Fairchild	**F6852**	**1887,1891**
	Hitachi	HD46852	
MC6854	**AMI**	**S6854**	**1826**
	Fairchild	**F6854**	**1887**
	Fujitsu	MBL6854	
MC6860	Fairchild	F6860	
MC6862	Fairchild	F6862	
MC6885	Motorola	MC8T95	
MC6886	Motorola	MC8T96	
MC6887	Motorola	MC8T97	
MC6888	Motorola	MC8T98	
MC7241	Raytheon	RC8241	
	Signetics	N8241	
MC7242	Fairchild	9386	
	Raytheon	RC8242	
	Signetics	N8242	
MC7250	Raytheon	RC8250	
	Signetics	N8250	
MC7251	Raytheon	RC8251	
	Signetics	N8251	
MC7261	Raytheon	RC8261	
	Signetics	N8261	
MC73525	AMD	SN75325	
MC74H00	Raytheon	74H00	
MC74H01	Raytheon	74H01	
MC74H04	Raytheon	74H04	
MC74H05	Raytheon	74H05	
MC74H10	Raytheon	74H10	
MC74H11	Raytheon	74H11	
MC74H20	Raytheon	74H20	
MC74H22	Raytheon	74H22	
MC74H40	Raytheon	74H40	
MC74H74	Raytheon	74H74	
MC74H87	Fairchild	74H87	
	TI	SN74H87	
MC7400	Fairchild	7400	
	Hitachi	HD7400	
	Mitsubishi	M53200	
	National	DM7400	
	NEC America	μPB7400	
	Signetics	7400	
	TI	SN7400	
	Toshiba	TC7400	
	TRW	7400	
MC7401	Fairchild	7401	
	Hitachi	HD7401	
	Mitsubishi	M53201	
	National	DM7401	
	Raytheon	7401	
	Signetics	7401	
	TI	SN7401	
	TRW	7401	
MC7402	Fairchild	7402	
	Hitachi	HD7402	
	Mitsubishi	M53202	
	National	DM7402	
	NEC America	μPB7402	
	Signetics	7402	
	TI	SN7402	
	TRW	7402	
MC7403	Fairchild	7403	
	Hitachi	HD7403	

♦ Discontinued

Bold face device numbers indicate manufacturers data is provided in the IC Master on the pages noted.

Motorola Semiconductor (cont'd)

Manufacturer Device	Replacement Source	Device	IC Master Page
MC7403	Mitsubishi	M53203	
	National	DM7403	
	Signetics	7403	
	TI	SN7403	
	TRW	7403	
MC7404	Fairchild	7404	
	Hitachi	HD7404	
	Mitsubishi	M53204	
	National	DM7404	
	NEC America	μPB7404	
	Signetics	7404	
	TI	SN7404	
	Toshiba	TC7404	
	TRW	7404	
MC7405	Fairchild	7405	
	Hitachi	HD7405	
	Mitsubishi	M53205	
	National	DM7405	
	NEC America	μPB7405	
	Signetics	7405	
	TI	SN7405	
	TRW	7405	
MC7406	Fairchild	7406	
	Hitachi	HD7406	
	Mitsubishi	M53206	
	National	DM7406	
	Signetics	7406	
	TI	SN7406	
	TRW	7406	
MC7407	Fairchild	7407	
	Hitachi	HD7407	
	Mitsubishi	M53207	
	National	DM7407	
	Signetics	7407	
	TI	SN7407	
	TRW	7407	
MC7408	Fairchild	7408	
	Mitsubishi	M53208	
	National	DM7408	
	Signetics	7408	
	TI	SN7408	
	Toshiba	TC7408	
	TRW	7408	
MC7409	Fairchild	7409	
	Hitachi	HD7409	
	Mitsubishi	M53209	
	National	DM7409	
	Signetics	7409	
	TI	SN7409	
	TRW	7409	
MC7410	Fairchild	7410	
	Hitachi	HD7410	
	Mitsubishi	M53210	
	National	DM7410	
	NEC America	μPB7410	
	Signetics	7410	
	TI	SN7410	
		SN7427	
	Toshiba	TC7410	
	TRW	7410	
MC74100	Signetics	74100	
	TI	SN74100	
MC74107	Fairchild	74107	
	Hitachi	HD74107	
	Mitsubishi	M53307	
	National	DM74107	
	NEC America	μPB74107	
	Signetics	74107	
	TI	SN74107	
MC74120	TI	SN74120	
MC74121	Fairchild	74121	
	Hitachi	HD74121	
	Mitsubishi	M53321	
	National	DM74121	
	Signetics	74121	
	TI	SN74121	
	TRW	74121	
MC74122	Fairchild	74122	
	Mitsubishi	M53322	
	Signetics	74122	
	TI	SN74122	
MC74123	AMD	SN74123	
MC74123	Fairchild	74123	
	Mitsubishi	M53323	
	National	DM74123	
	NEC America	μPB74123	
	Signetics	74123	
	TI	SN74123	
	TRW	74123	
MC7413	Fairchild	7413	
	Mitsubishi	M53213	
	National	DM7413	
	NEC America	μPB7413	
	Signetics	7413	
	TI	SN7413	
	TRW	7413	
MC74132	Fairchild	74132	
	Hitachi	HD74132	
	Mitsubishi	M53332	
	National	DM74132	
	Signetics	74132	
	TI	SN74132	
MC74136	Hitachi	HD74136	
	TI	SN74136	
	TRW	74136	
MC7414	Fairchild	7414	
	Hitachi	HD7414	
	Mitsubishi	M53214	
	National	DM7414	
	Signetics	7414	
	TI	SN7414	
MC74141	Fairchild	74141	
	National	DM74141	
	NEC America	μPB74141	
	TI	SN74141	
MC74145	Fairchild	74145	
	Mitsubishi	M53345	
	National	DM74145	
	Signetics	74145	
	TI	SN74145	
	TRW	74145	
MC74150	Fairchild	74150	
	Hitachi	HD74150	
	Mitsubishi	M53350	
	National	DM74150	
	NEC America	μPB74150	
	Signetics	74150	
	TI	SN74150	
	TRW	74150	
MC74151	Fairchild	74151	
	Hitachi	HD74151	
	Mitsubishi	M53351	
	National	DM74151	
	NEC America	μPB74151	
	Signetics	74151	
	TI	SN74151	
		SN74151A	
	TRW	74151	
MC74152	Fairchild	74152	
	TRW	74152	
MC74153	Fairchild	74153	
	Mitsubishi	M53353	
	National	DM74153	
	NEC America	μPB74153	
	Signetics	74153	
	TI	SN74153	
	TRW	74153	
MC74154	AMD	SN74154	
	Fairchild	74154	
	Mitsubishi	M53354	
	National	DM74154	
	NEC America	μPB74154	
	Raytheon	74154	
	Signetics	74154	
	TI	SN74154	
	TRW	74154	
MC74155	Fairchild	74155	
	Mitsubishi	M53355	
	National	DM74155	
	NEC America	μPB74155	
	Signetics	74155	
	TI	SN74155	
	TRW	74155	
MC74156	Fairchild	74156	
	Hitachi	HD74156	
	Mitsubishi	M53356	
	National	DM74156	
	NEC America	μPB74156	
MC74156	Signetics	74156	
	TI	SN74156	
	TRW	74156	
MC74157	AMD	SN74157	
	Fairchild	74157	
	Hitachi	HD74157	
	Mitsubishi	M53357	
	National	DM74157	
	NEC America	μPB74157	
	Signetics	74157	
	TI	SN74157	
MC7416	Fairchild	7416	
	Hitachi	HD7416	
	Mitsubishi	M53216	
	National	DM7416	
	Signetics	7416	
	TI	SN7416	
	TRW	7416	
MC74160	AMD	SN74160	
	Fairchild	74160	
	Hitachi	HD74160	
	Mitsubishi	M53360	
	National	DM74160	
	Raytheon	74160	
	Signetics	74160	
	TI	SN74160	
	TRW	74160	
MC74161	AMD	SN74161	
	Fairchild	74161	
	Hitachi	HD74161	
	Mitsubishi	M53361	
	National	DM74161	
	NEC America	μPB74161	
	Signetics	74161	
	TI	SN74161	
	TRW	74161	
MC74162	AMD	SN74162	
	Fairchild	74162	
	Hitachi	HD74162	
	Mitsubishi	M53362	
	National	DM74162	
	Signetics	74162	
	TI	SN74162	
	TRW	74162	
MC74163	AMD	SN74163	
	Fairchild	74163	
	Hitachi	HD74163	
	Mitsubishi	M53363	
	National	DM74163	
	Signetics	74163	
	TI	SN74163	
	TRW	74163	
♦MC74164	Raytheon	74164	
MC74165	Fairchild	74165	
	Mitsubishi	M53365	
	National	DM74165	
	Signetics	74165	
	TI	SN74165	
MC74166	Fairchild	74166	
MC74167	Fairchild	74167	
	TI	SN74167	
MC7417	Fairchild	7417	
	Hitachi	HD7417	
	Mitsubishi	M53217	
	National	DM7417	
	Signetics	7417	
	TI	SN7417	
	TRW	7417	
MC74170	Fairchild	74170	
MC74174	AMD	SN74174	
	Hitachi	HD74174	
	Mitsubishi	M53374	
	National	DM74174	
	Signetics	74174	
	TI	SN74174	
MC74175	AMD	SN74175	
	Fairchild	74175	
	Hitachi	HD74175	
	Mitsubishi	M53375	
	National	DM74175	
	NEC America	μPB74175	
	Signetics	74175	
	TI	SN74175	
MC74176	Fairchild	74176	
	Mitsubishi	M53376	
	National	DM74176	
MC74176	Signetics	74176	
	TI	SN74176	
MC74177	Fairchild	74177	
	Mitsubishi	M53377	
	National	DM74177	
	Signetics	74177	
	TI	SN74177	
MC74180	Fairchild	74180	
	Hitachi	HD74180	
	Mitsubishi	M53380	
	National	DM74180	
	NEC America	μPB74180	
	Signetics	74180	
	TI	SN74180	
	TRW	74180	
MC74181	AMD	SN74181	
	Fairchild	74181	
	Mitsubishi	M53381	
	National	DM74181	
	NEC America	μPB74181	
	Signetics	74181	
	TI	SN74181	
MC74182	AMD	SN74182	
	Fairchild	74182	
	Mitsubishi	M53382	
	National	DM74182	
	NEC America	μPB74182	
	Signetics	74182	
	TI	SN74182	
MC74190	Fairchild	74190	
	Hitachi	HD74190	
	Mitsubishi	M53390	
	National	DM74190	
	Signetics	74190	
	TI	SN74190	
MC74191	Fairchild	74191	
	Hitachi	HD74191	
	Mitsubishi	M53391	
	National	DM74191	
	Signetics	74191	
	TI	SN74191	
MC74192	AMD	SN74192	
	Fairchild	74192	
	Mitsubishi	M53392	
	National	DM74192	
	NEC America	μPB74192	
	Signetics	74192	
	TI	SN74192	
MC74193	AMD	SN74193	
	Fairchild	74193	
	Mitsubishi	M53393	
	National	DM74193	
	NEC America	μPB74193	
	Signetics	74193	
	TI	SN74193	
MC74194	AMD	SN74194	
	Fairchild	74194	
	Hitachi	HD74194	
	National	DM74194	
	Signetics	74194	
	TI	SN74194	
MC74195	AMD	SN74195	
	Fairchild	74195	
	National	DM74195	
	NEC America	μPB74195	
	Signetics	74195	
	TI	SN74195	
MC74196	Fairchild	74196	
	National	DM74196	
	Signetics	74196	
	TI	SN74196	
MC74197	Fairchild	74197	
	National	DM74197	
	Signetics	74197	
	TI	SN74197	
MC74198	Fairchild	74198	
MC74199	Fairchild	74199	
MC7420	Fairchild	7420	
	Hitachi	HD7420	
	Mitsubishi	M53220	
	National	DM7420	
	NEC America	μPB7420	
	Signetics	7420	
	TI	SN7420	
	Toshiba	TC7420	
	TRW	7420	

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The manufacturers report their devices can be used as direct replacements.
Performance details often differ, so compare the specifications considering your requirements.

Motorola Semiconductor (cont'd)

Manufacturer Device	Replacement Source	Device	IC Master Page
MC7423	Fairchild	7423	
	National	DM7423	
	TI	SN7423	
MC7425	Fairchild	7425	
	Mitsubishi	M53225	
	National	DM7425	
	TI	SN7425	
MC7426	Fairchild	7426	
	Hitachi	HD7426	
	National	DM7426	
	Signetics	7426	
	TI	SN7426	
	TRW	7426	
MC7427	Fairchild	7427	
	Hitachi	HD7427	
	Mitsubishi	M53227	
	National	DM7427	
	Signetics	7427	
MC74283	Fairchild	74283	
MC74290	Fairchild	74290	
	Mitsubishi	M53490	
	TI	SN74290	
	TRW	74290	
MC74293	Fairchild	74293	
	Mitsubishi	M53493	
	TI	SN74293	
	TRW	74293	
MC74298	Fairchild	74298	
	Signetics	74298	
	TI	SN74298	
MC7430	Fairchild	7430	
	Hitachi	HD7430	
	Mitsubishi	M53230	
	National	DM7430	
	NEC America	μPB7430	
	Signetics	7430	
	TI	SN7430	
	TRW	7430	
MC7437	Fairchild	7437	
	Mitsubishi	M53237	
	National	DM7437	
	NEC America	μPB7437	
	Signetics	7437	
	TI	SN7437	
	TRW	7437	
MC7438	Fairchild	7438	
	Mitsubishi	M53238	
	National	DM7438	
	NEC America	μPB7438	
	Signetics	7438	
	TI	SN7438	
	TRW	7438	
MC7440	Fairchild	7440	
	Hitachi	HD7440	
	Mitsubishi	M53240	
	National	DM7440	
	NEC America	μPB7440	
	Signetics	7440	
	TI	SN7440	
	TRW	7440	
♦MC7441	Hitachi	HD7441	
	TI	SN74141	
MC7442	Fairchild	7442	
	Hitachi	HD7442	
	Mitsubishi	M53242	
	National	DM7442	
	NEC America	μPB7442	
	Signetics	7442	
	TI	SN7442	
MC7443	Fairchild	7443	
	Hitachi	HD7443	
	Mitsubishi	M53243	
	Signetics	7443	
	TI	SN7443	
MC7444	Fairchild	7444	
	Hitachi	HD7444	
	Mitsubishi	M53244	
	Signetics	7444	
	TI	SN7444	
MC7445	Fairchild	7445	
	Mitsubishi	M53245	
	National	DM7445	
MC7445	NEC America	μPB7445	
	Signetics	7445	
	TI	SN7445	
	TRW	7445	
MC7446	Fairchild	7446	
	National	DM7446	
	Signetics	7446	
	TI	SN7446	
MC7447	Fairchild	7447	
	Mitsubishi	M53247	
	National	DM7447	
	NEC America	μPB7447	
	Signetics	7447	
	TI	SN7447	
MC7448	Fairchild	7448	
	Mitsubishi	M53248	
	National	DM7448	
	Signetics	7448	
	TI	SN7448	
MC7449	Fairchild	7449	
	TI	SN7449	
MC7450	Fairchild	7450	
	Hitachi	HD7450	
	Mitsubishi	M53250	
	National	DM7450	
	NEC America	μPB7450	
	Signetics	7450	
	TI	SN7450	
	TRW	7450	
MC7451	Fairchild	7451	
	Hitachi	HD7451	
	National	DM7451	
	NEC America	μPB7451	
	Signetics	7451	
	TI	SN7451	
	TRW	7451	
MC7453	Fairchild	7453	
	Hitachi	HD7453	
	Mitsubishi	M53253	
	National	DM7453	
	NEC America	μPB7453	
	Signetics	7453	
	TI	SN7453	
	TRW	7453	
MC7454	Fairchild	7454	
	Hitachi	HD7454	
	National	DM7454	
	NEC America	μPB7454	
	Signetics	7454	
	TI	SN7454	
	TRW	7454	
MC7460	Fairchild	7460	
	Hitachi	HD7460	
	Mitsubishi	M53260	
	National	DM7460	
	NEC America	μPB7460	
	Signetics	7460	
	TI	SN7460	
	TRW	7460	
MC7470	Fairchild	7470	
	Mitsubishi	M53270	
	National	DM7470	
	Signetics	7470	
	TI	SN7470	
MC7472	Fairchild	7472	
	Hitachi	HD7472	
	Mitsubishi	M53272	
	National	DM7472	
	Signetics	7472	
	TI	SN7472	
	TRW	7472	
MC7473	Fairchild	7473	
	Hitachi	HD7473	
	Mitsubishi	M53273	
	National	DM7473	
	NEC America	μPB7473	
	Signetics	7473	
	TI	SN7473	
MC7474	Fairchild	7474	
	Hitachi	HD7474	
	Mitsubishi	M53274	
	National	DM7474	
	NEC America	μPB7474	
	Raytheon	MC7474	
	Signetics	7474	
	TI	SN7474	
MC7474	TRW	7474	
MC7475	Fairchild	7475	
	Hitachi	HD7475	
	Mitsubishi	M53275	
	National	DM7475	
	Signetics	7475	
	TI	SN7475	
	TRW	7475	
MC7476	Fairchild	7476	
	Hitachi	HD7476	
	Mitsubishi	M53276	
	National	DM7476	
	NEC America	μPB7476	
	Signetics	7476	
	TI	SN7476	
	TRW	7476	
MC7477	Fairchild	7477	
	Signetics	7477	
	TI	SN7477	
MC7480	Fairchild	7480	
	Mitsubishi	M53280	
	NEC America	μPB7480	
	Signetics	7480	
	TI	SN7480	
MC7482	Fairchild	7482	
	TI	SN7482	
MC7483	Fairchild	7483	
	Mitsubishi	M53283	
	National	DM7483	
	Signetics	7483	
	TI	SN7483	
MC7485	Fairchild	7485	
	Hitachi	HD7485	
	Mitsubishi	M53285	
	National	DM7485	
	NEC America	μPB7485	
	Signetics	7485	
	TI	SN7485	
	TRW	7485	
MC7486	Fairchild	7486	
	Hitachi	HD7486	
	Mitsubishi	M53286	
	National	DM7486	
	NEC America	μPB7486	
	Signetics	7486	
	TI	SN7486	
	TRW	7486	
MC7490	Fairchild	7490	
	Hitachi	HD7490	
	Mitsubishi	M53290	
	National	DM7490	
	Signetics	7490	
	TI	SN7490	
		SN7490A	
	TRW	7490	
MC7491	Fairchild	7491	
	Hitachi	HD7491	
	Mitsubishi	M53291	
	National	DM7491	
	NEC America	μPB7491	
	Signetics	7491	
	TI	SN7491	
		SN7491A	
MC7492	Fairchild	7492	
	Hitachi	HD7492	
	Mitsubishi	M53292	
	National	DM7492	
	Signetics	7492	
	TI	SN7492	
		SN7492A	
	TRW	7492	
MC7493	Fairchild	7493	
	Hitachi	HD7493	
	Mitsubishi	M53293	
	National	DM7493	
	Signetics	7493	
	TI	SN7493	
		SN7493A	
	TRW	7493	
MC7494	Fairchild	7494	
	TI	SN7494	
MC7495	Fairchild	7495	
	Hitachi	HD7495	
	Mitsubishi	M53295	
	National	DM7495	
	Signetics	7495	
MC7495	TI	SN7495	
		SN7495A	
MC7496	Fairchild	7496	
	Hitachi	HD7496	
	Mitsubishi	M53296	
	National	DM7496	
	Signetics	7496	
	TI	SN7496	
	TRW	7496	
MC7497	Fairchild	7497	
	TI	SN7497	
♦MC75107	AMD	SN75107	
	Fairchild	75107	
	National	DS75107	
	Raytheon	RC75107	
	TI	SN75107A	
♦MC75108	AMD	SN75108	
	Fairchild	75108	
	National	DS75108	
	Raytheon	RC75108	
	TI	SN75108A	
MC75109	AMD	SN75109	
	Fairchild	75109	
	Raytheon	RC75109	
	TI	SN75109	
MC75110	AMD	SN75110	
	Fairchild	75110	
	Raytheon	RC75110	
	TI	SN75110	
MC75140	TI	SN75140	
MC7520	National	DS7520	
	Signetics	7520	
	Silicon G	SG7520	
	TI	SN7520	
MC7521	Signetics	7521	
	Silicon G	SG7521	
♦MC7522	National	DS7522	
	Signetics	7522	
	Silicon G	SG7522	
	TI	SN7522	
♦MC7523	Signetics	7523	
	Silicon G	SG7523	
	TI	SN7522	
MC7524	AMD	SN7524	
	Fairchild	75S24	
	National	DS7524	
	Signetics	7524	
	Silicon G	SG7524	
	TI	SN7524	
MC7525	AMD	SN7525	
	Signetics	7525	
	Silicon G	SG7525	
	TI	SN7524	
MC7528	Fairchild	7528	
	National	DS7528	
	Silicon G	SG7528	
	TI	SN7528	
MC7529	Silicon G	SG7529	
	TI	SN7528	
MC75325	AMD	SN75325	
	Fairchild	75325	
	National	DS75325	
	Raytheon	RC75325	
	Silicon G	SG75325	
	TI	SN75325	
MC7534	National	DS7534	
	Silicon G	SG7534	
MC7535	Silicon G	SG7535	
MC75358	TI	SN75368	
MC75365	TI	SN75365	
MC75368	TI	SN75368	
MC7538	National	DS7538	
	Silicon G	SG7538	
MC7539	Silicon G	SG7539	
MC75450	Fairchild	75450	
	National	DS75450	
	Raytheon	RC75450	
	Silicon G	SG75450	
	TI	SN75450	
MC75451	Fairchild	75451	
	National	DS75451	
	Raytheon	RC75451	
	Silicon G	SG75451	
	TI	SN75451	
MC75452	Fairchild	75452	
	National	DS75452	

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Bold face device numbers indicate manufacturers data is provided in the IC Master on the pages noted.

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Manufacturer Device	Replacement Source	Device	IC Master Page
MC75452	Raytheon	RC75452	
	Silicon G	SG75452	
	TI	SN75452	
MC75453	Fairchild	75453	
	National	DS75453	
	Raytheon	RC75453	
	Silicon G	SG75453	
	TI	SN75453	
MC75454	Fairchild	75454	
	Silicon G	SG75454	
	TI	SN75454	
MC75460	TI	SN75460	
MC75461	TI	SN75461	
MC75462	TI	SN75462	
MC75463	TI	SN75463	
MC75464	TI	SN75464	
MC75491	Fairchild	75491	
	National	DS75491	
	TI	SN75491	
MC75492	Fairchild	75492	
	National	DS75492	
	TI	SN75492	
MC7705	Signetics	μA78M05	
MC7706	Signetics	μA78M06	
MC78L02	Signetics	μA78L02	
MC78L02.6	TI	μA78L02	
MC78L05	NEC America	μPC78L05	
	Signetics	μA78L05	
	TI	μA78L05	
MC78L06.2	TI	μA78L06	
MC78L08	NEC America	μPC78L08	
	Signetics	μA78L08	
	TI	μA78L08	
MC78L12	NEC America	μPC78L12	
	Signetics	μA78L12	
	TI	μA78L12	
MC78L15	NEC America	μPC78L15	
	Signetics	μA78L15	
	TI	μA78L15	
MC78L24	Signetics	μA78L24	
MC78M05	NEC America	μPC78M05	
	Signetics	μA78M05	
	TI	μA78M05	
MC78M06	Signetics	μA78M06	
	TI	μA78M06	
MC78M08	NEC America	μPC78M08	
	TI	μA78M08	
MC78M12	NEC America	μPC78M12	
	TI	μA78M12	
MC78M15	NEC America	μPC78M15	
	TI	μA78M15	
MC78M20	TI	μA78M20	
MC78M24	TI	μA78M24	
MC7805	Fairchild	μA7805	
	National	**LM340-5**	**1060**
	NEC America	μPC14305	
	Raytheon	RC7805	
	Signetics	μA7805	
	Silicon G	SG7805	
	TI	μA7805	
MC7806	Fairchild	μA7806	
	National	**LM340-6**	**1060**
	Raytheon	RC7806	
	Signetics	μA7806	
	Silicon G	SG7806	
	TI	μA7806	
MC7808	Fairchild	μA7808	
	National	**LM340-8**	**1060**
	NEC America	μPC14308	
	Raytheon	RC7808	
	Signetics	μA7808	
	Silicon G	SG7808	
	TI	μA7808	
MC7812	Fairchild	μA7812	
	National	**LM340-12**	**1060**
	NEC America	μPC14312	
	Raytheon	RC7812	
	Signetics	μA7812	
	Silicon G	SG7812	
	TI	μA7812	
MC7815	Fairchild	μA7815	
	National	**LM340-15**	**1060**
MC7815	NEC America	μPC14315	
	Raytheon	RC7815	
	Signetics	μA7815	
	Silicon G	SG7815	
	TI	μA7815	
MC7818	Fairchild	μA7818	
	National	**LM340-18**	**1060**
	NEC America	μPC14318	
	Raytheon	RC7818	
	Signetics	μA7818	
	Silicon G	SG7818	
	TI	μA7818	
MC7824	Fairchild	μA7824	
	National	**LM340-24**	**1060**
	NEC America	μPC14324	
	Raytheon	RC7824	
	Signetics	μA7824	
	Silicon G	SG7824	
	TI	μA7824	
MC7905	Fairchild	μA7905	
	National	**LM7905**	**1061**
	Signetics	μA7905	
	Silicon G	SG320-05	
	TI	μA7905	
MC7905.2	Signetics	μA7905.2	
MC7906	Fairchild	μA7906	
	National	**LM7906**	**1061**
	Signetics	μA7906	
	TI	μA7906	
MC7908	Fairchild	μA7908	
	National	**LM7908**	**1061**
	Signetics	μA7908	
	TI	μA7908	
MC7912	Fairchild	μA7912	
	National	**LM7912**	**1061**
	Signetics	μA7912	
	Silicon G	SG320-12	
	TI	μA7912	
MC7915	Fairchild	μA7915	
	National	**LM7915**	**1061**
	Signetics	μA7915	
	Silicon G	SG320-15	
	TI	μA7915	
MC7918	Fairchild	μA7918	
	National	**LM7918**	**1061**
	Signetics	μA7918	
	TI	μA7918	
MC7924	Fairchild	μA7924	
	National	**LM7924**	**1061**
	Signetics	μA7924	
	TI	μA7924	
MC7952	Silicon G	SG320-5.2	
MC8T13	Fairchild	8T13	
	TI	SN75121	
MC8T14	Fairchild	8T14	
	TI	SN75122	
MC8T23	Fairchild	8T23	
	TI	SN75123	
MC8T24	Fairchild	8T24	
	TI	SN75124	
MC8T26	AMD	N8T26	
	Hitachi	HD268T26	
	Signetics	N8T26	
MC8T28	Signetics	N8T28	
MC8T95	Motorola	MC6885	
MC8T96	Motorola	MC6886	
MC8T97	Motorola	MC6887	
MC8T98	Motorola	MC6888	
MC8241	Raytheon	RM8241	
	Signetics	S8241	
MC8242	Fairchild	9386	
	Raytheon	RM8242	
	Signetics	S8242	
MC8250	Raytheon	RM8250	
	Signetics	S8250	
MC8251	Raytheon	RM8251	
	Signetics	S8251	
MC8260	Raytheon	RM8260	
MC8261	Raytheon	RM8261	
	Signetics	S8261	
MC830	Fairchild	930	
	Hitachi	HD2204	
	National	DM930	
	TI	SN15930	
MC8300	AMD	9300	
	Fairchild	9300	
MC8300	Raytheon	RC9300	
	TI	SN74195	
MC8301	AMD	9301	
	Fairchild	9301	
	Signetics	N8252	
	TI	SN29301	
MC8304	AMD	9304	
	Fairchild	9304	
	Raytheon	RC9304	
MC8308	AMD	9308	
	Fairchild	9308	
	Raytheon	RC9308	
	TI	SN29308	
MC8309	AMD	9309	
	Fairchild	9309	
	TI	SN29309	
MC831	Fairchild	931	
	TI	SN15831	
MC8310	AMD	9310	
	Fairchild	9310	
	Raytheon	RC9310	
	TI	SN74160	
MC8311	AMD	9311	
	Fairchild	9311	
	Raytheon	RC9311	
	TI	SN74154	
MC8312	AMD	9312	
	Fairchild	9312	
	Raytheon	RC9312	
	Signetics	N8230	
	TI	SN29312	
MC8314	AMD	9314	
MC8316	AMD	9316	
	Fairchild	9316	
	Raytheon	RC9316	
	TI	SN74161	
MC8318	AMD	9318	
	TI	SN29318	
MC832	Fairchild	932	
	Hitachi	HD2201	
	National	DM932	
	TI	SN15832	
MC8328	AMD	9328	
	Fairchild	9328	
	Signetics	N8277	
MC833	Fairchild	933	
	Hitachi	HD2202	
	National	DM933	
	TI	SN15833	
MC834	TI	SN15834	
MC835	Fairchild	9135	
	TI	SN15838	
MC836	Fairchild	936	
	Hitachi	HD2206	
	National	DM936	
	TI	SN15836	
MC837	Fairchild	937	
	National	DM937	
	TI	SN15837	
MC840	Fairchild	935	
	National	DM935	
	TI	SN15835	
MC841	TI	SN15835	
MC844	Fairchild	944	
	Hitachi	HD2209	
	National	DM944	
MC845	Fairchild	945	
	Hitachi	HD2205	
	National	DM945	
	TI	SN15845	
MC846	Fairchild	946	
	Hitachi	HD2203	
	National	DM946	
	TI	SN15846	
MC848	Fairchild	948	
	National	DM948	
	TI	SN15848	
MC849	Fairchild	949	
	National	DM949	
	TI	SN15849	
MC850	Fairchild	950	
	TI	SN15850	
MC851	Fairchild	951	
	TI	SN15851	
MC852	Fairchild	951	
	National	DM9099	
MC852	TI	SN158099	
MC853	Fairchild	9093	
	National	DM9093	
	TI	SN158093	
MC855	Fairchild	9097	
	National	DM9097	
	TI	SN158097	
MC856	Fairchild	9094	
	National	DM9094	
	TI	SN158094	
MC857	Fairchild	9157	
	Hitachi	HD2213	
	National	DM957	
	TI	SN15857	
MC858	Fairchild	9158	
	Hitachi	HD2214	
	National	DM958	
	TI	SN15858	
MC8601	AMD	9601	
	Fairchild	9601	
	Raytheon	RF8601	
	Signetics	8T22	
	TI	SN29601	
MC8602	AMD	9602	
	Raytheon	RF8602	
MC861	Fairchild	961	
	National	DM961	
	TI	SN15861	
MC862	Fairchild	962	
	Hitachi	HD2207	
	National	DM962	
	TI	SN15862	
MC863	Fairchild	963	
	National	DM963	
	TI	SN15863	
MC930	Fairchild	930	
	Raytheon	RM930	
	TI	SN15930	
MC9300	AMD	9300	
	Fairchild	9300	
	Raytheon	RM9300	
	TI	SN54195	
MC9301	AMD	9301	
	Fairchild	9301	
	TI	SN39301	
MC9304	AMD	9304	
	Fairchild	9304	
	Raytheon	RM9304	
MC9308	AMD	9308	
	Fairchild	9308	
	Raytheon	RM9308	
	TI	SN39308	
MC931	Fairchild	931	
	TI	SN15931	
MC9310	AMD	9310	
	Fairchild	9310	
	Raytheon	RM9310	
	TI	SN54160	
MC9311	AMD	9311	
	Fairchild	9311	
	Raytheon	RM9311	
	TI	SN54154	
MC9312	AMD	9312	
	Fairchild	9312	
	Raytheon	RM9312	
	Signetics	S8230	
	TI	SN39312	
MC9314	AMD	9314	
	Fairchild	9314	
MC9316	AMD	9316	
	Fairchild	9316	
	Raytheon	RM9316	
	TI	SN54161	
MC9318	AMD	9318	
	Fairchild	9318	
	TI	SN39318	
MC932	Fairchild	932	
	Raytheon	RM932	
	TI	SN15939	
MC9328	AMD	9328	
	Fairchild	9328	
	Signetics	N8277	
MC933	Fairchild	933	
	TI	SN15933	
MC934	TI	SN15934	
MC935	Fairchild	9135	

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The manufacturers report their devices can be used as direct replacements.
Performance details often differ, so compare the specifications considering your requirements.

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Manufacturer Device	Replacement Source	Device	IC Master Page
MC935	Raytheon	RM935	
	TI	SN15938	
MC936	Fairchild	936	
	Raytheon	RM936	
	TI	SN15936	
MC937	Fairchild	937	
	Raytheon	RM937	
	TI	SN15937	
MC940	Fairchild	935	
	Raytheon	RM940	
	TI	SN15935	
MC943	Fairchild	SH2001	
MC944	Fairchild	944	
	Raytheon	RM944	
	TI	SN15944	
MC945	Fairchild	945	
	Raytheon	RM945	
	TI	SN15945	
MC946	Fairchild	946	
	Raytheon	RM946	
	TI	SN15946	
MC948	Fairchild	948	
	Raytheon	RM948	
	TI	SN15948	
MC949	Fairchild	949	
	Raytheon	RM949	
	TI	SN15949	
MC950	Fairchild	950	
	Raytheon	RM950	
	TI	SN15950	
MC951	Fairchild	951	
	Raytheon	RM951	
	TI	SN15951	
MC952	Fairchild	9099	
	Raytheon	RM952	
	TI	SN159099	
MC953	Fairchild	9093	
	TI	SN159093	
MC955	Fairchild	9097	
	TI	SN159097	
MC956	Fairchild	9094	
	TI	SN159094	
MC957	Fairchild	9157	
	Raytheon	RM957	
	TI	SN15957	
MC958	Fairchild	9158	
	Raytheon	RM958	
	TI	SN15958	
MC9601	AMD	9601	
	Raytheon	RF9601	
	Signetics	S8T22	
	TI	SN29601	
MC9602	AMD	9602	
	Fairchild	9602	
	Raytheon	RF9602	
MC961	Fairchild	961	
	Raytheon	RM961	
	TI	SN15961	
MC962	Fairchild	962	
	Raytheon	RM962	
	TI	SN15962	
MC963	Fairchild	963	
	Raytheon	RM963	
	TI	SN15963	
♦MFC4000	Motorola	MC3360	
♦MFC4010	Motorola	MC3310	
♦MFC6040	Motorola	MC3340	
♦MFC8030	Motorola	MC3330	
♦MFC8070	Motorola	MC3370	
MLM304	TI	LM304	
MMH0026	AMD	MMH0026	
	National	DS0026	
	TI	SN75369	
MM2316E	**AMI**	**S6831B**	**1215,1806**
MQ3724	RCA	CA3724	
MQ3725	RCA	CA3725	
NE592	AMD	NE592	
SE592	AMD	SE592	
SN54H54	Signetics	10170	
SN54LS00	Fairchild	54LS00	
	National	DM54LS00	
SN54LS00	Raytheon	54LS00	
	Signetics	54LS00	
	TI	SN54LS00	
SN54LS02	Fairchild	54LS02	
	National	DM54LS02	
	Raytheon	54LS02	
	Signetics	54LS02	
	TI	SN54LS02	
SN54LS03	Fairchild	54LS03	
	National	DM54LS03	
	Raytheon	54LS03	
	Signetics	54LS03	
	TI	SN54LS03	
SN54LS04	Fairchild	54LS04	
	National	DM54LS04	
	Raytheon	54LS04	
	Signetics	54LS04	
	TI	SN54LS04	
SN54LS05	Fairchild	54LS05	
	National	DM54LS05	
	Raytheon	54LS05	
	Signetics	54LS05	
	TI	SN54LS05	
SN54LS08	Fairchild	54LS08	
	National	DM54LS08	
	Raytheon	54LS08	
	Signetics	54LS08	
	TI	SN54LS08	
SN54LS09	Fairchild	54LS09	
	National	DM54LS09	
	Raytheon	54LS09	
	Signetics	54LS09	
	TI	SN54LS09	
SN54LS10	Fairchild	54LS10	
	National	DM54LS10	
	Raytheon	54LS10	
	Signetics	54LS10	
	TI	SN54LS10	
SN54LS107	Fairchild	54LS107	
	National	DM54LS107	
	Raytheon	54LS107	
	Signetics	54LS107	
	TI	SN54LS107	
SN54LS109	Fairchild	54LS109	
	National	DM54LS109	
	Raytheon	54LS109	
	Signetics	54LS109	
	TI	SN54LS109	
SN54LS11	Fairchild	54LS11	
	National	DM54LS11	
	Raytheon	54LS11	
	Signetics	54LS11	
	TI	SN54LS11	
SN54LS114	Fairchild	54LS114	
	National	DM54LS114	
	Raytheon	54LS114	
	Signetics	54LS114	
	TI	SN54LS114A	
SN54LS126	Fairchild	54LS126	
	National	DM54LS126	
	Raytheon	54LS126	
	Signetics	54LS126	
	TI	SN54LS126A	
SN54LS13	Fairchild	54LS13	
	National	DM54LS13	
	Raytheon	54LS13	
	Signetics	54LS13	
	TI	SN54LS13	
SN54LS132	Fairchild	54LS132	
	National	DM54LS132	
	Raytheon	54LS132	
	Signetics	54LS132	
	TI	SN54LS132	
SN54LS136	Fairchild	54LS136	
	Raytheon	54LS136	
	Signetics	54LS136	
	TI	SN54LS136	
SN54LS138	Fairchild	54LS138	
	National	DM54LS138	
	Raytheon	54LS138	
	Signetics	54LS138	
	TI	SN54LS138	
SN54LS139	AMD	SN54LS139	
	Fairchild	54LS139	
	National	DM54LS139	
	Raytheon	54LS139	
SN54LS139	Signetics	74LS139	
	TI	SN54LS139	
SN54LS14	Fairchild	54LS14	
	National	DM54LS14	
	Raytheon	54LS14	
	Signetics	54LS14	
	TI	SN54LS14	
SN54LS15	Fairchild	54LS15	
	National	DM54LS15	
	Raytheon	54LS15	
	Signetics	54LS15	
	TI	SN54LS15	
SN54LS151	AMD	SN54LS151	
	Fairchild	54LS151	
	National	DM54LS151	
	Raytheon	54LS151	
	Signetics	54LS151	
	TI	SN54LS151	
SN54LS152	Fairchild	54LS152	
	Raytheon	54LS152	
	TI	SN54LS152	
SN54LS153	AMD	SN54LS153	
	Fairchild	54LS153	
	National	DM54LS153	
	Raytheon	54LS153	
	Signetics	54LS153	
	TI	SN54LS153	
SN54LS155	Fairchild	54LS155	
	National	DM54LS155	
	Raytheon	74LS155	
	TI	SN54LS155	
SN54LS156	Fairchild	54LS156	
	National	DM54LS156	
	Raytheon	54LS156	
	TI	SN54LS156	
SN54LS157	AMD	SN54LS157	
	Fairchild	54LS157	
	National	DM54LS157	
	Raytheon	54LS157	
	Signetics	54LS157	
	TI	SN54LS157	
SN54LS158	Fairchild	54LS158	
	National	DM54LS158	
	Raytheon	54LS158	
	Signetics	54LS158	
	TI	SN54LS158	
SN54LS160A	AMD	SN54LS160	
	Fairchild	54LS160	
	National	DM54LS160	
	Raytheon	54LS160	
	TI	SN54LS160A	
SN54LS161A	AMD	SN54LS161	
	Fairchild	54LS161	
	National	DM54LS161	
	Raytheon	54LS161	
	Signetics	54LS161A	
	TI	SN54LS161A	
SN54LS162A	AMD	SN54LS162	
	Fairchild	54LS162	
	National	DM54LS162	
	Raytheon	54LS162	
	TI	SN54LS162A	
SN54LS163A	AMD	SN54LS163	
	Fairchild	54LS163	
	National	DM54LS163	
	Raytheon	54LS163	
	Signetics	54LS163A	
	TI	54LS163A	
SN54LS164A	AMD	SN54LS164	
	Fairchild	54LS164	
	National	DM54LS164	
	Raytheon	54LS164	
	Signetics	54LS164	
	TI	SN54LS164A	
SN54LS170	AMD	SN54LS170	
	Fairchild	54LS170	
	National	DM54LS170	
	Raytheon	54LS170	
	Signetics	54LS170	
	TI	SN54LS170	
SN54LS175	AMD	SN54LS175	
	Fairchild	54LS175	
	National	DM54LS175	
	Raytheon	54LS175	
	Signetics	54LS175	
	TI	SN54LS175	
SN54LS181	AMD	SN54LS181	
	Fairchild	54LS181	
	Raytheon	54LS181	
	Signetics	54LS181	
	TI	SN54LS181	
SN54LS190	AMD	SN54LS190	
	Fairchild	54LS190	
	National	DM54LS190	
	Raytheon	54LS190	
	Signetics	54LS190	
	TI	SN54LS190	
SN54LS191	AMD	SN54LS191	
	Fairchild	54LS191	
	National	DM54LS191	
	Raytheon	54LS191	
	Signetics	54LS191	
	TI	SN54LS191	
SN54LS192	AMD	SN54LS192	
	Fairchild	54LS192	
	National	DM54LS192	
	Raytheon	54LS192	
	Signetics	54LS192	
	TI	SN54LS192	
SN54LS193	AMD	SN54LS193	
	Fairchild	54LS193	
	National	DM54LS193	
	Raytheon	54LS193	
	Signetics	54LS193	
	TI	SN54LS193	
SN54LS194	AMD	SN54LS194A	
	Fairchild	54LS194	
	Raytheon	54LS194A	
	TI	SN54LS194A	
SN54LS195	AMD	SN54LS195A	
	Fairchild	54LS195	
	Raytheon	54LS195A	
	Signetics	54LS195A	
	TI	SN54LS195A	
SN54LS196	Fairchild	54LS196	
	National	DM54LS196	
	Raytheon	54LS196	
	TI	SN54LS196	
SN54LS197	Fairchild	54LS197	
	National	DM54LS197	
	Raytheon	54LS197	
	TI	SN54LS197	
SN54LS20	Fairchild	54LS20	
	National	DM54LS20	
	Raytheon	54LS20	
	Signetics	54LS20	
	TI	SN54LS20	
SN54LS21	Fairchild	54LS21	
	National	DM54LS21	
	Raytheon	54LS21	
	Signetics	54LS21	
	TI	SN54LS21	
SN54LS22	Fairchild	54LS22	
	National	DM54LS22	
	Raytheon	54LS22	
	Signetics	54LS22	
	TI	SN54LS22	
SN54LS251	AMD	SN54LS251	
	Fairchild	54LS251	
	Raytheon	54LS251	
	Signetics	54LS251	
	TI	SN54LS251	
SN54LS253	AMD	SN54LS253	
	Fairchild	54LS253	
	National	DM54LS253	
	Raytheon	54LS253	
	Signetics	54LS253	
	TI	SN54LS253	
SN54LS257	Fairchild	54LS257	
	National	DM54LS257	
	Raytheon	54LS257	
	Signetics	54LS257	
	TI	SN54LS257	
SN54LS258	AMD	SN54LS258	
	Fairchild	54LS258	
	Raytheon	54LS258	
	TI	SN54LS258	
SN54LS259	Fairchild	54LS259	
	TI	SN54LS259	
SN54LS266	Fairchild	54LS266	
	Raytheon	54LS266	
	Signetics	54LS266	

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Bold face device numbers indicate manufacturers data is provided in the IC Master on the pages noted.

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Manufacturer Device	Replacement Source	Device	IC Master Page
SN54LS266	TI	SN54LS266	
SN54LS27	Fairchild	54LS27	
	National	DM54LS27	
	Raytheon	54LS27	
	Signetics	54LS27	
	TI	SN54LS27	
SN54LS279	Fairchild	54LS279	
	National	DM54LS279	
	Raytheon	74LS279	
	Signetics	54LS279	
	TI	SN54LS279	
SN54LS283	Fairchild	54LS283	
	National	DM54LS283	
	Raytheon	54LS283	
	TI	SN54LS283	
SN54LS295	Fairchild	54LS295	
	Raytheon	54LS295A	
	TI	SN54LS295B	
SN54LS298	Fairchild	54LS298	
	Raytheon	54LS298	
	TI	SN54LS298	
SN54LS30	Fairchild	54LS30	
	National	DM54LS30	
	Raytheon	54LS30	
	Signetics	54LS30	
	TI	SN54LS30	
SN54LS32	Fairchild	54LS32	
	National	DM54LS32	
	Raytheon	54LS32	
	Signetics	54LS32	
	TI	SN54LS32	
SN54LS365A	Fairchild	54LS365	
	Raytheon	54LS365	
	Signetics	54LS365A	
	TI	SN54LS365A	
SN54LS366A	Fairchild	54LS366	
	Raytheon	54LS366	
	Signetics	54LS366A	
	TI	SN54LS366A	
SN54LS367A	Fairchild	54LS367	
	Raytheon	54LS367	
	Signetics	54LS367A	
	TI	SN54LS367A	
SN54LS368A	Fairchild	54LS368	
	Raytheon	54LS368	
	Signetics	54LS368A	
	TI	SN54LS368A	
SN54LS37	Fairchild	54LS37	
	National	DM54LS37	
	Raytheon	54LS37	
	Signetics	54LS37	
	TI	SN54LS37	
SN54LS38	Fairchild	54LS38	
	National	DM54LS38	
	Raytheon	54LS38	
	Signetics	54LS38	
	TI	SN54LS38	
SN54LS40	Fairchild	54LS40	
	National	DM54LS40	
	Raytheon	54LS40	
	Signetics	54LS40	
	TI	SN54LS40	
SN54LS42	Fairchild	54LS42	
	National	DM54LS42	
	Raytheon	54LS42	
	Signetics	54LS42	
	TI	SN54LS42	
SN54LS51	Fairchild	54LS51	
	National	DM54LS51	
	Raytheon	54LS51	
	Signetics	54LS51	
	TI	SN54LS51	
SN54LS54	Fairchild	54LS54	
	National	DM54LS54	
	Raytheon	54LS54	
	Signetics	54LS54	
	TI	SN54LS54	
SN54LS55	Fairchild	54LS55	
	National	DM54LS55	
	Raytheon	54LS55	
	Signetics	54LS55	
	TI	SN54LS55	
SN54LS670	Fairchild	54LS670	
	National	DM54LS670	
	Raytheon	54LS670	
	Signetics	54LS670	
	TI	SN54LS670	
SN54LS73	Fairchild	54LS73	
	National	DM54LS73	
	Raytheon	54LS73	
	Signetics	54LS73	
	TI	SN54LS73	
SN54LS74	Fairchild	54LS74	
	National	DM54LS74	
	Raytheon	54LS74	
	Signetics	54LS74	
	TI	SN54LS74	
SN54LS83	Fairchild	54LS83	
	National	DM54LS83	
	Raytheon	54LS83A	
	TI	SN54LS83A	
SN54LS86	Fairchild	54LS86	
	Raytheon	54LS86	
	Signetics	54LS86	
	TI	SN54LS86	
SN54LS90	Fairchild	54LS90	
	Raytheon	54LS90	
	Signetics	54LS90	
	TI	SN54LS90	
SN54LS92	Raytheon	54LS92	
	Signetics	54LS92	
	TI	SN54LS92	
SN54LS93	Fairchild	54LS93	
	Raytheon	54LS93	
	Signetics	54LS93	
	TI	SN54LS93	
SN54LS95B	Fairchild	54LS95B	
	Raytheon	54LS95B	
	TI	SN54LS95B	
SN54S112	Fairchild	54S112	
	TI	SN54S112	
SN54S113	Fairchild	54S113	
	TI	SN54S113	
SN73LS368A	Raytheon	74LS368	
SN74LS00	Fairchild	74LS00	
	Hitachi	HD74LS00	
	National	DM74LS00	
	NEC America	μPB74LS00	
	Raytheon	74LS00	
	Signetics	74LS00	
	TI	SN74LS00	
SN74LS01	Hitachi	HD74LS01	
SN74LS02	Fairchild	74LS02	
	Hitachi	HD74LS02	
	National	DM74LS02	
	NEC America	μPB74LS02	
	Raytheon	74LS02	
	Signetics	74LS02	
	TI	SN74LS02	
SN74LS03	Fairchild	74LS03	
	Hitachi	HD74LS03	
	National	DM74LS03	
	NEC America	μPB74LS03	
	Raytheon	74LS03	
	Signetics	74LS03	
	TI	SN74LS03	
SN74LS04	Fairchild	74LS04	
	Hitachi	HD74LS04	
	National	DM74LS04	
	NEC America	μPB74LS04	
	Raytheon	74LS04	
	Signetics	74LS04	
	TI	SN74LS04	
SN74LS05	Fairchild	74LS05	
	Hitachi	HD74LS05	
	National	DM74LS05	
	NEC America	μPB74LS05	
	Raytheon	74LS05	
	Signetics	74LS05	
	TI	SN74LS05	
SN74LS08	Fairchild	74LS08	
	Hitachi	HD74LS08	
	National	DM74LS08	
	NEC America	μPB74LS08	
	Raytheon	74LS08	
	Signetics	74LS08	
	TI	SN74LS08	
SN74LS09	Fairchild	74LS09	
SN74LS09	Hitachi	HD74LS09	
	National	DM74LS09	
	Raytheon	74LS09	
	Signetics	74LS09	
	TI	SN74LS09	
SN74LS10	Fairchild	74LS10	
	Hitachi	HD74LS10	
	National	DM74LS10	
	NEC America	μPB74LS10	
	Raytheon	74LS10	
	Signetics	74LS10	
	TI	SN74LS10	
SN74LS107A	Hitachi	HD74LS107	
SN74LS109	Fairchild	74LS109	
	National	DM74LS109	
	NEC America	μPB74LS109	
	Raytheon	74LS109	
	Signetics	74LS109	
	TI	SN74LS109	
SN74LS11	Fairchild	74LS11	
	Hitachi	HD74LS11	
	National	DM74LS11	
	NEC America	μPB74LS11	
	Raytheon	74LS11	
	Signetics	74LS11	
	TI	SN74LS11	
SN74LS112A	Hitachi	HD74LS112	
SN74LS113A	Hitachi	HD74LS113	
SN74LS114	Fairchild	74LS114	
	National	DM74LS114	
	Raytheon	74LS114	
	Signetics	74LS114	
	TI	SN74LS114	
SN74LS114A	Hitachi	HD74LS114	
SN74LS12	Hitachi	HD74LS12	
SN74LS123	Hitachi	HD74LS123	
SN74LS126	Fairchild	74LS126	
	National	DM74LS126	
	Raytheon	74LS126	
	Signetics	74LS126	
	TI	SN74LS126A	
SN74LS13	Fairchild	74LS13	
	Hitachi	HD74LS13	
	National	DM74LS13	
	Raytheon	74LS13	
	Signetics	74LS13	
	TI	SN74LS13	
SN74LS132	Fairchild	74LS132	
	Hitachi	HD74LS132	
	National	DM74LS132	
	Raytheon	74LS132	
	Signetics	74LS132	
	TI	SN74LS132	
SN74LS136	Fairchild	74LS136	
	Hitachi	HD74LS136	
	National	DM74LS136	
	Raytheon	74LS136	
	Signetics	74LS136	
	TI	SN74LS136	
SN74LS138	AMD	SN74LS138	
	Fairchild	74LS138	
	Hitachi	HD74LS138	
	National	DM74LS138	
	NEC America	μPB74LS138	
	Raytheon	74LS138	
	Signetics	74LS138	
	TI	SN74LS138	
SN74LS139	AMD	SN74LS139	
	Fairchild	74LS139	
	Hitachi	HD74LS139	
	National	DM74LS139	
	NEC America	μPB74LS139	
	Raytheon	74LS139	
	Signetics	74LS139	
	TI	SN74LS139	
SN74LS14	Fairchild	74LS14	
	Hitachi	HD74LS14	
	National	DM74LS14	
	Raytheon	74LS14	
	Signetics	74LS14	
	TI	SN74LS14	
SN74LS15	Fairchild	74LS15	
	Hitachi	HD74LS15	
	National	DM74LS15	
	Raytheon	74LS15	
	Signetics	74LS15	
SN74LS15	TI	SN74LS15	
SN74LS151	AMD	SN74LS151	
	Fairchild	74LS151	
	Hitachi	HD74LS151A	
	National	DM74LS151	
	NEC America	μPB74LS151	
	Raytheon	74LS151	
	Signetics	74LS151	
	TI	SN74LS151	
SN74LS152	Fairchild	74LS152	
	Hitachi	HD74LS152	
	Raytheon	74LS152	
SN74LS153	AMD	SN74LS153	
	Fairchild	74LS153	
	Hitachi	HD74LS153	
	National	DM74LS153	
	NEC America	μPB74LS153	
	Raytheon	74LS153	
	Signetics	74LS153	
	TI	SN74LS153	
SN74LS155	Fairchild	74LS155	
	Hitachi	HD74LS155	
	National	DM74LS155	
	NEC America	μPB74LS155	
	Raytheon	74LS155	
	Signetics	74LS155	
	TI	SN74LS155	
SN74LS156	Fairchild	74LS156	
	Hitachi	HD74LS156	
	National	DM74LS156	
	Raytheon	74LS156	
	Signetics	74LS156	
	TI	SN74LS156	
SN74LS157	AMD	SN74LS157	
	Fairchild	74LS157	
	National	DM74LS157	
	NEC America	μPB74LS157	
	Raytheon	74LS157	
	Signetics	74LS157	
	TI	SN74LS157	
SN74LS158	AMD	SN74LS158	
	Fairchild	74LS158	
	Hitachi	HD74LS158	
	National	DM74LS158	
	Raytheon	74LS158	
	Signetics	74LS158	
	TI	SN74LS158	
SN74LS160A	AMD	SN74LS160	
	Fairchild	74LS160	
	Hitachi	HD74LS160A	
	National	DM74LS160	
	Raytheon	74LS160	
	Signetics	74LS160A	
	TI	SN74LS160A	
SN74LS161A	AMD	SN74LS161	
	Fairchild	74LS161	
	Hitachi	HD74LS161A	
	National	DM74LS161	
	NEC America	μPB74LS161	
	Raytheon	74LS161	
	Signetics	74LS161A	
	TI	SN74LS161A	
SN74LS162A	AMD	SN74LS162	
	Fairchild	74LS162	
	Hitachi	HD74LS162A	
	National	DM74LS162	
	Raytheon	74LS162	
	Signetics	74LS162	
	TI	SN74LS162	
SN74LS163A	AMD	SN74LS163	
	Fairchild	74LS163	
	Hitachi	HD74LS163A	
	National	DM74LS163	
	Raytheon	74LS163	
	Signetics	74LS163	
	TI	SN74LS163	
SN74LS164	Hitachi	HD74LS164	
SN74LS164A	AMD	SN74LS164	
	Fairchild	74LS164	
	National	DM74LS164	
	NEC America	μPB74LS164	
	Raytheon	74LS164	
	Signetics	74LS164	
	TI	SN74LS164	
SN74LS170	AMD	SN74LS170	
	Fairchild	74LS170	

♦ Discontinued

The manufacturers report their devices can be used as direct replacements.
Performance details often differ, so compare the specifications considering your requirements.

Motorola Semiconductor (cont'd)

Manufacturer Device	Replacement Source	Device	IC Master Page
SN74LS170	National	DM74LS170	
	Raytheon	74LS170	
	Signetics	74LS170	
	TI	SN74LS170	
SN74LS174	AMD	SN74LS174	
	Fairchild	74LS174	
	Hitachi	HD74LS174	
	National	DM74LS174	
	Raytheon	74LS174	
	Signetics	74LS174	
	TI	SN74LS174	
SN74LS175	AMD	SN74LS175	
	Fairchild	74LS175	
	Hitachi	HD74LS175	
	National	DM74LS175	
	NEC America	μPB74LS175	
	Raytheon	74LS175	
	Signetics	74LS175	
	TI	SN74LS175	
SN74LS181	AMD	SN74LS181	
	Fairchild	74LS181	
	Raytheon	74LS181	
	Signetics	74LS181	
	TI	SN74LS181	
SN74LS190	AMD	SN74LS190	
	Fairchild	74LS190	
	National	DM74LS190	
	Raytheon	74LS190	
	Signetics	74LS190	
	TI	SN74LS190	
SN74LS191	AMD	SN74LS191	
	Fairchild	74LS191	
	National	DM74LS191	
	Raytheon	74LS191	
	Signetics	74LS191	
	TI	SN74LS191	
SN74LS192	AMD	SN74LS192	
	Fairchild	74LS192	
	National	DM74LS192	
	NEC America	μPB74LS192	
	Raytheon	74LS192	
	Signetics	74LS192	
	TI	SN74LS192	
SN74LS193	AMD	SN74LS193	
	Fairchild	74LS193	
	National	DM74LS193	
	NEC America	μPB74LS193	
	Raytheon	74LS193	
	Signetics	74LS193	
	TI	SN74LS193	
SN74LS194	AMD	SN74LS194A	
	Fairchild	74LS194	
	NEC America	μPB74LS194	
	Raytheon	74LS194A	
	Signetics	74LS194A	
	TI	SN74LS194A	
SN74LS194A	Hitachi	HD74LS194A	
SN74LS195	AMD	SN74LS195A	
	Fairchild	74LS195	
	NEC America	μPB74LS195	
	Raytheon	74LS195A	
	Signetics	74LS195A	
	TI	SN74LS195A	
SN74LS195A	Hitachi	HD74LS195A	
SN74LS196	Fairchild	74LS196	
	National	DM74LS196	
	Raytheon	74LS196	
	Signetics	74LS196	
	TI	SN74LS196	
SN74LS197	Fairchild	74LS197	
	National	DM74LS197	
	Raytheon	74LS197	
	Signetics	74LS197	
	TI	SN74LS197	
SN74LS20	Fairchild	74LS20	
	Hitachi	HD74LS20	
	National	DM74LS20	
	NEC America	μPB74LS20	
	Raytheon	74LS20	
	Signetics	74LS20	
	TI	SN74LS20	
SN74LS21	Fairchild	74LS21	
SN74LS21	Hitachi	HD74LS21	
	National	DM74LS21	
	NEC America	μPB74LS21	
	Raytheon	74LS21	
	Signetics	74LS21	
	TI	SN74LS21	
SN74LS22	Fairchild	74LS22	
	Hitachi	HD74LS22	
	National	DM74LS22	
	Raytheon	74LS22	
	Signetics	74LS22	
	TI	SN74LS22	
SN74LS221	National	DM74LS221	
	Raytheon	74LS221	
	Signetics	74LS221	
	TI	SN74LS221	
SN74LS240	AMD	SN74LS240	
	Fairchild	74LS240	
	MMI	**74LS240**	**768**
	Raytheon	**74LS240**	**522**
	Signetics	74LS240	
	TI	SN74LS240	
SN74LS241	AMD	SN74LS241	
	Fairchild	74LS241	
	MMI	**74LS241**	**768**
	Raytheon	**74LS241**	**525**
	Signetics	74LS241	
	TI	SN74LS241	
SN74LS242	AMD	SN74LS242	
	Fairchild	74LS242	
	Raytheon	**74LS242**	**528**
	Signetics	74LS242	
	TI	SN74LS242	
SN74LS243	AMD	SN74LS243	
	Fairchild	74LS243	
	Raytheon	**74LS243**	**528**
	Signetics	74LS243	
	TI	SN74LS243	
SN74LS244	AMD	SN74LS244	
	Fairchild	74LS244	
	MMI	**74LS244**	**768**
	Raytheon	**74LS244**	**525**
	Signetics	74LS244	
	TI	SN74LS244	
SN74LS247	Hitachi	HD74LS247	
SN74LS248	Hitachi	HD74LS248	
SN74LS249	Hitachi	HD74LS249	
SN74LS251	AMD	SN74LS251	
	Fairchild	74LS251	
	Hitachi	HD74LS251	
	National	DM74LS251	
	NEC America	μPB74LS251	
	Raytheon	74LS251	
	Signetics	74LS251	
	TI	SN74LS251	
SN74LS253	AMD	SN74LS253	
	Fairchild	74LS253	
	Hitachi	HD74LS253	
	National	DM74LS253	
	NEC America	μPB74LS253	
	Raytheon	74LS253	
	Signetics	74LS253	
	TI	SN74LS253	
SN74LS256	Signetics	74LS256	
SN74LS257	AMD	SN74LS257	
	Fairchild	74LS257	
	National	DM74LS257	
	NEC America	μPB74LS257	
	Raytheon	74LS257	
	Signetics	74LS257	
	TI	SN74LS257	
SN74LS257A	Hitachi	HD74LS257	
SN74LS258	AMD	SN74LS258	
	Fairchild	74LS258	
	National	DM74LS258	
	NEC America	μPB74LS258	
	Raytheon	74LS258	
	Signetics	74LS258	
	TI	SN74LS258	
SN74LS259	Fairchild	74LS259	
	Signetics	74LS259	
	TI	SN74LS259	
SN74LS26	Hitachi	HD74LS26	
SN74LS266	Fairchild	74LS266	
	Raytheon	74LS266	
	Signetics	74LS266	
SN74LS266	TI	SN74LS266	
SN74LS27	Fairchild	74LS27	
	Hitachi	HD74LS27	
	National	DM74LS27	
	NEC America	μPB74LS27	
	Raytheon	74LS27	
	Signetics	74LS27	
	TI	SN74LS27	
SN74LS279	Fairchild	74LS279	
	National	DM74LS279	
	NEC America	μPB74LS279	
	Raytheon	74LS279	
	Signetics	74LS279	
	TI	SN74LS279	
SN74LS283	Fairchild	74LS283	
	Hitachi	SN74LS283	
	National	DM74LS283	
	Raytheon	74LS283	
	Signetics	74LS283	
	TI	SN74LS283	
SN74LS290	Fairchild	74LS290	
	National	DM74LS290	
	Signetics	74LS290	
	TI	SN74LS290	
SN74LS293	Fairchild	74LS293	
	National	DM74LS293	
	Signetics	74LS293	
	TI	SN74LS293	
SN74LS295	Fairchild	74LS295	
	NEC America	μPB74LS295	
	Raytheon	74LS295A	
	Signetics	74LS295	
	TI	SN74LS295B	
SN74LS298	Fairchild	74LS298	
	Hitachi	HD74LS298	
	Raytheon	74LS298	
	Signetics	74LS298	
	TI	SN74LS298	
SN74LS30	Fairchild	74LS30	
	Hitachi	HD74LS30	
	National	DM74LS30	
	NEC America	μPB74LS30	
	Raytheon	74LS30	
	Signetics	74LS30	
	TI	SN74LS30	
SN74LS32	Fairchild	74LS32	
	Hitachi	HD74LS32	
	National	DM74LS32	
	NEC America	μPB74LS32	
	Raytheon	74LS32	
	Signetics	74LS32	
	TI	SN74LS32	
SN74LS365A	Fairchild	74LS365	
	National	DM74LS365	
	NEC America	μPB74LS365	
	Raytheon	74LS365	
	Signetics	74LS365A	
	TI	SN74LS365A	
SN74LS366A	Fairchild	74LS366	
	National	DM74LS366	
	NEC America	μPB74LS366	
	Raytheon	74LS366	
	Signetics	74LS366A	
	TI	SN74LS366A	
SN74LS367	Hitachi	HD74LS367	
SN74LS367A	Fairchild	74LS367	
	National	DM74LS367	
	NEC America	μPB74LS367	
	Raytheon	74LS367	
	Signetics	74LS367A	
	TI	SN74LS367A	
SN74LS368A	Fairchild	74LS368	
	Hitachi	HD74LS368	
	National	DM74LS368	
	NEC America	μPB74LS368	
	Signetics	74LS368A	
	TI	SN74LS368A	
SN74LS37	Fairchild	74LS37	
	Hitachi	HD74LS37	
	National	DM74LS37	
	NEC America	μPB74LS37	
	Raytheon	74LS37	
	Signetics	74LS37	
	TI	SN74LS37	
SN74LS375	Fairchild	74LS375	
	NEC America	μPB74LS375	
SN74LS375	Raytheon	74LS375	
	Signetics	74LS375	
	TI	SN74LS375	
SN74LS38	Fairchild	74LS38	
	Hitachi	HD74LS38	
	National	DM74LS38	
	NEC America	μPB74LS38	
	Raytheon	74LS38	
	Signetics	74LS38	
	TI	SN74LS38	
SN74LS386	Hitachi	HD74LS386	
	National	DM74LS386	
	Raytheon	74LS386	
	Signetics	74LS386	
	TI	SN74LS386	
SN74LS40	Fairchild	74LS40	
	Hitachi	HD74LS40	
	National	DM74LS40	
	NEC America	μPB74LS40	
	Raytheon	74LS40	
	Signetics	74LS40	
	TI	SN74LS40	
SN74LS42	Fairchild	74LS42	
	Hitachi	HD74LS42	
	National	DM74LS42	
	NEC America	μPB74LS42	
	Raytheon	74LS42	
	Signetics	74LS42	
	TI	SN74LS42	
SN74LS47	Hitachi	HD74LS47	
SN74LS48	Hitachi	HD74LS48	
SN74LS49	Hitachi	HD74LS49	
SN74LS51	Fairchild	74LS51	
	Hitachi	HD74LS51	
	National	DM74LS51	
	NEC America	μPB74LS51	
	Raytheon	74LS51	
	Signetics	74LS51	
	TI	SN74LS51	
SN74LS54	Fairchild	74LS54	
	Hitachi	HD74LS54	
	National	DM74LS54	
	NEC America	μPB74LS54	
	Raytheon	74LS54	
	Signetics	74LS54	
	TI	SN74LS54	
SN74LS55	Fairchild	74LS55	
	Hitachi	HD74LS55	
	National	DM74LS55	
	NEC America	μPB74LS55	
	Raytheon	74LS55	
	Signetics	74LS55	
	TI	SN74LS55	
SN74LS670	Fairchild	74LS670	
	National	DM74LS670	
	Raytheon	74LS670	
	Signetics	74LS670	
	TI	SN74LS670	
SN74LS73	Fairchild	74LS73	
	National	DM74LS73	
	Raytheon	74LS73	
	Signetics	74LS73	
	TI	SN74LS73	
SN74LS73A	Hitachi	HD74LS73	
SN74LS74	Fairchild	74LS74	
	National	DM74LS74	
	NEC America	μPB74LS74	
	Raytheon	74LS74	
	Signetics	74LS74	
	TI	SN74LS74	
SN74LS74A	Hitachi	HD74LS74A	
SN74LS76A	Hitachi	HD74LS76	
SN74LS78A	Hitachi	HD74LS78	
SN74LS83	Fairchild	74LS83	
	National	DM74LS83	
		DM74LS83A	
	Raytheon	74LS83A	
	Signetics	74LS83	
	TI	SN74LS83A	
SN74LS83A	Hitachi	HD74LS83A	
SN74LS85	Fairchild	74LS85	
	National	DM74LS85	
	Raytheon	74LS85	
	Signetics	74LS85	
	TI	SN74LS85	
SN74LS86	Fairchild	74LS86	

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Bold face device numbers indicate manufacturers data is provided in the IC Master on the pages noted.

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Manufacturer Device	Replacement Source	Device	IC Master Page
SN74LS86	Hitachi	HD74LS86	
	NEC America	μPB74LS86	
	Raytheon	74LS86	
	Signetics	74LS86	
	TI	SN74LS86	
SN74LS90	Fairchild	74LS90	
	Raytheon	74LS90	
	Signetics	74LS90	
	TI	SN74LS90	
SN74LS92	Fairchild	74LS92	
	Hitachi	HD74LS92	
	Raytheon	74LS92	
	Signetics	74LS92	
	TI	SN74LS92	
SN74LS93	Fairchild	74LS93	
	Raytheon	74LS93	
	Signetics	74LS93	
	TI	SN74LS93	
SN74LS95	Fairchild	74LS95	
	Raytheon	74LS95B	
	Signetics	74LS95B	
	TI	SN74LS95B	
SN74LS95B	Hitachi	HD74LS95B	
SN74S112	Fairchild	74S112	
	Hitachi	HD74S112	
	Mitsubishi	M5S112	
	National	DM74S112	
	Signetics	74S112	
	TI	SN74S112	
SN74S113	Fairchild	74S113	
	Hitachi	HD74S113	
	Mitsubishi	M5S113	
	National	DM74S113	
	Signetics	74S113	
	TI	SN74S113	
TBA395	Sprague	ULN-2218	
TBA396	Sprague	ULN-2219	
ULN2001	**Exar**	**XR2201**	**931**
ULN2002	**Exar**	**XR2202**	**931**
ULN2003	**Exar**	**XR2203**	**931**
ULN2004	**Exar**	**XR2204**	**931**
XR2201	Motorola	ULN2001	
3106	Fairchild	54H11	

National Semiconductor

Manufacturer Device	Replacement Source	Device	IC Master Page
ADC0816	TI	ADC0816	
AH0126	Siliconix	DG126	
AH0129	Siliconix	DG129	
AH0133	Siliconix	DG133	
AH0134	Siliconix	DG134	
AH0139	Siliconix	DG139	
AH0140	Siliconix	DG140	
AH0141	Siliconix	DG141	
AH0142	Siliconix	DG142	
AH0143	Siliconix	DG143	
AH0144	Siliconix	DG144	
AH0145	Siliconix	DG145	
AH0146	Siliconix	DG146	
AH0151	Siliconix	DG151	
AH0152	Siliconix	DG152	
AH0153	Siliconix	DG153	
AH0154	Siliconix	DG154	
AH0161	Siliconix	DG161	
AH0162	Siliconix	DG162	
AH0163	Siliconix	DG163	
AH0164	Siliconix	DG164	
CA3089	Signetics	CA3089	
CD4000	Mitel	SIL4000	
	Motorola	MC14000	
	RCA	CD4000	
	Solitron	CM4000	
	SSS	SCL4000	
	TI	TP4000	
CD4001	Fairchild	F4001	
	Mitel	SIL4001	
		SIL4901	
	Motorola	MC14001	
	NEC America	μPD4001	
	RCA	CD4001	
	SGS	HBF4001	
CD4001	Solitron	CM4001	
	SSS	SCL4001	
	TI	TP4001	
	Toshiba	TC4001	
CD4002	Fairchild	F4002	
	Mitel	SIL4002	
	Motorola	MC14002	
	NEC America	μPD4002	
	RCA	CD4002	
	SGS	HBF4002	
	Solitron	CM4002	
	SSS	SCL4002	
	TI	TP4002	
	Toshiba	TC4002	
CD4006	Fairchild	F4006	
	Motorola	MC14006	
	NEC America	μPD4006	
	RCA	CD4006	
	Solitron	CM4006	
	SSS	SCL4006	
CD4007	Fairchild	F4007	
	Mitel	SIL4007	
	Motorola	MC14007	
	RCA	CD4007	
	SGS	HBF4007	
	Solitron	CM4007	
	SSS	SCL4007	
	TI	TP4007	
	Toshiba	TC4007	
CD4008	Fairchild	F4008	
	Motorola	MC14008	
	RCA	CD4008	
	SGS	HBF4008	
	Solitron	CM4008	
	SSS	SCL4008	
	TI	TP4008	
	Toshiba	TC4008	
CD4009	Mitel	SIL4009	
	RCA	CD4009	
	SGS	HBF4009	
	Solitron	CM4009	
	SSS	SCL4009	
	TI	TP4009	
	Toshiba	TC4009	
CD4010	Mitel	SIL4010	
	RCA	CD4010	
	SGS	HBF4010	
	Solitron	CM4010	
	SSS	SCL4010	
	TI	TP4010	
	Toshiba	TC4010	
CD40106	Motorola	MC14584	
	National	**MM74C14**	**262**
	RCA	CD40106	
CD4011	Fairchild	F4011	
	Mitel	SIL4011	
		SIL4911	
	Motorola	MC14011	
	NEC America	μPD4011	
	RCA	CD4011	
	SGS	HBF4011	
	Solitron	CM4011	
	SSS	SCL4011	
	TI	TP4011	
	Toshiba	TC4011	
CD4012	Fairchild	F4012	
	Mitel	SIL4012	
		SIL4912	
	Motorola	MC14012	
	NEC America	μPD4012	
	RCA	CD4012	
	SGS	HBF4012	
	Solitron	CM4012	
	SSS	SCL4012	
	TI	TP4012	
	Toshiba	TC4012	
CD4013	Fairchild	F4013	
	Mitel	SIL4013	
	Motorola	MC14013	
	NEC America	μPD4013	
	RCA	CD4013	
	SGS	HBF4013	
	Solitron	CM4013	
	SSS	SCL4013	
	TI	TP4013	
	Toshiba	TC4013	
CD4014	Fairchild	F4014	
	Mitel	SIL4014	
	Motorola	MC14014	
	NEC America	μPD4014	
	RCA	CD4014	
	SGS	HBF4014	
	Solitron	CM4014	
	SSS	SCL4014	
	TI	TP4014	
	Toshiba	TC4014	
CD4015	Fairchild	F4015	
	Mitel	SIL4015	
	Motorola	MC14015	
	NEC America	μPD4015	
	RCA	CD4015	
	SGS	HBF4015	
	Solitron	CM4015	
	SSS	SCL4015	
	TI	TP4015	
	Toshiba	TC4015	
CD4016	AD	AD7516	
	Fairchild	F4016	
	Micro Power	MPS7516	
	Mitel	SIL4016	
	Motorola	MC14016	
	RCA	CD4016	
	Solitron	CM4016	
	SSS	SCL4016	
	TI	TP4016	
CD40160	Fairchild	F40160	
	RCA	CD40160	
CD40161	Fairchild	F40161	
	RCA	CD40161	
CD40162	Fairchild	F40162	
	RCA	CD40162	
CD40163	Fairchild	F40163	
	RCA	CD40163	
CD4017	Fairchild	F4017	
	Mitel	SIL4017	
	Motorola	MC14017	
	NEC America	μPD4017	
	RCA	CD4017	
	SGS	HBF4017	
	Solitron	CM4017	
	SSS	SCL4017	
	TI	TP4017	
	Toshiba	TC4017	
CD40174	Fairchild	F40174	
	RCA	CD40174	
CD4018	Fairchild	F4018	
	Mitel	SIL4018	
	RCA	CD4018	
	SGS	HBF4018	
	Solitron	CM4018	
	SSS	SCL4018	
	TI	TP4018	
	Toshiba	TC4018	
CD4019	Fairchild	F4019	
	Mitel	SIL4019	
	NEC America	μPD4019	
	RCA	CD4019	
	SGS	HBF4019	
	Solitron	CM4019	
	SSS	SCL4019	
	TI	TP4019	
	Toshiba	TC4019	
CD40192	Fairchild	F40192	
	National	MM74C192	
	RCA	CD40192	
CD40193	Fairchild	F40193	
	National	MM74C193	
	RCA	CD40193	
CD4020	Fairchild	F4020	
	Mitel	SIL4020	
	Motorola	MC14020	
	NEC America	μPD4020	
	RCA	CD4020	
	SGS	HBF4020	
	Solitron	CM4020	
	SSS	SCL4020	
	TI	TP4020	
	Toshiba	TC4020	
CD4021	Fairchild	F4021	
	Mitel	SIL4021	
	Motorola	MC14021	
	NEC America	μPD4021	
CD4021	RCA	CD4021	
	Solitron	CM4021	
	SSS	SCL4021	
	TI	TP4021	
	Toshiba	TC4021	
CD4022	Fairchild	F4022	
	Mitel	SIL4022	
	Motorola	MC14022	
	RCA	CD4022	
	SGS	HBF4022	
	Solitron	CM4022	
	SSS	SCL4022	
	TI	TP4022	
	Toshiba	TC4022	
CD4023	Fairchild	F4023	
	Mitel	SIL4023	
		SIL4923	
	Motorola	MC14023	
	NEC America	μPD4023	
	RCA	CD4023	
	SGS	HBF4023	
	Solitron	CM4023	
	SSS	SCL4023	
	TI	TP4023	
	Toshiba	TC4023	
CD4024	Fairchild	F4024	
	Mitel	SIL4024	
	Motorola	MC14024	
	NEC America	μPD4024	
	RCA	CD4024	
	SGS	HBF4024	
	Solitron	CM4024	
	SSS	SCL4024	
	TI	TP4024	
	Toshiba	TC4024	
CD4025	Fairchild	F4025	
	Mitel	SIL4025	
		SIL4925	
	Motorola	MC14025	
	NEC America	μPD4025	
	RCA	CD4025	
	SGS	HBF4025	
	Solitron	CM4025	
	SSS	SCL4025	
	TI	TP4025	
	Toshiba	TC4025	
CD4027	Fairchild	F4027	
	Mitel	SIL4027	
	Motorola	MC14027	
	NEC America	μPD4027	
	RCA	CD4027	
	SGS	HBF4027	
	Solitron	CM4027	
	SSS	SCL4027	
	TI	TP4027	
	Toshiba	TC4027	
CD4028	Fairchild	F4028	
	Mitel	SIL4028	
	Motorola	MC14028	
	NEC America	μPD4028	
	RCA	CD4028	
	SGS	HBF4028	
	Solitron	CM4028	
	SSS	SCL4028	
	TI	TP4028	
	Toshiba	TC4028	
CD4029	Fairchild	F4029	
	Mitel	SIL4029	
	NEC America	μPD4029	
	RCA	CD4029	
	SGS	HBF4029	
	Solitron	CM4029	
	SSS	SCL4029	
	TI	TP4029	
	Toshiba	TC4029	
CD4030	Fairchild	F4030	
	Mitel	SIL4030	
	NEC America	μPD4030	
	RCA	CD4030	
	SGS	HBF4030	
	Solitron	CM4030	
	SSS	SCL4030	
	TI	TP4030	
	Toshiba	TC4030	
CD4031	Fairchild	F4031	
	RCA	CD4031	

♦ Discontinued

The manufacturers report their devices can be used as direct replacements.
Performance details often differ, so compare the specifications considering your requirements.

National Semiconductor (cont'd)

Manufacturer Device	Replacement Source	Device	IC Master Page
CD4034	Fairchild	F4034	
	Motorola	MC14034	
	NEC America	μPD4034	
	RCA	CD4034	
	Solitron	CM4034	
	SSS	SCL4034	
	Toshiba	TC4034	
CD4035	Fairchild	F4035	
	Mitel	SIL4035	
	Motorola	MC14035	
	NEC America	μPD4035	
	RCA	CD4035	
	SGS	HBF4035	
	Solitron	CM4035	
	SSS	SCL4035	
	TI	TP4035	
	Toshiba	TC4035	
CD4040	Fairchild	F4040	
	Mitel	SIL4040	
	NEC America	μPD4040	
	RCA	CD4040	
	Solitron	CM4040	
	SSS	SCL4040	
	TI	TP4040	
	Toshiba	TC4040	
CD4041	Fairchild	F4041	
	RCA	CD4041	
	Solitron	CM4041	
	SSS	CL4041	
		SCL4041	
CD4042	Fairchild	F4042	
	Mitel	SIL4042	
	Motorola	MC14042	
	NEC America	μPD4042	
	RCA	CD4042	
	SGS	HBF4042	
	Solitron	CM4042	
	SSS	SCL4042	
	TI	TP4042	
	Toshiba	TC4042	
CD4043	Fairchild	F4043	
	Mitel	SIL4043	
	Motorola	MC14043	
	NEC America	μPD4043	
	RCA	CD4043	
	Solitron	CM4043	
	SSS	SCL4043	
	TI	TP4043	
	Toshiba	TC4043	
CD4044	Fairchild	F4044	
	Mitel	SIL4044	
	Motorola	MC14044	
	NEC America	μPD4044	
	RCA	CD4044	
	Solitron	CM4044	
	SSS	SCL4044	
	TI	TP4044	
	Toshiba	TC4044	
CD4046	Fairchild	F4046	
	Mitel	SIL4046	
	Motorola	MC14046	
	RCA	CD4046	
	Solitron	CM4046	
	SSS	SCL4046	
CD4048	RCA	CD4048	
CD4049	Fairchild	F4049	
	Mitel	SIL4049	
	Motorola	MC14049	
	NEC America	μPD4049	
	RCA	CD4049	
	SGS	HBF4049	
	Solitron	CM4049	
	SSS	SCL4049	
	TI	TP4049	
	Toshiba	TC4049	
CD4050	Fairchild	F4050	
	Mitel	SIL4050	
	Motorola	MC14050	
	NEC America	μPD4050	
	RCA	CD4050	
	SGS	HBF4050	
	Solitron	CM4050	
CD4050	SSS	SCL4050	
	TI	TP4050	
	Toshiba	TC4050	
CD4051	Fairchild	F4051	
	Mitel	SIL4051	
	Motorola	MC14051	
	NEC America	μPD4051	
	RCA	CD4051	
	Solitron	CM4051	
	SSS	SCL4051	
	TI	TP4051	
	Toshiba	TC4051	
CD4052	Fairchild	F4052	
	Mitel	SIL4052	
	Motorola	MC14052	
	NEC America	μPD4052	
	RCA	CD4052	
	Solitron	CM4052	
	SSS	SCL4052	
	TI	TP4052	
	Toshiba	TC4052	
CD4053	Fairchild	F4053	
	Mitel	SIL4053	
	Motorola	MC14053	
	NEC America	μPD4053	
	RCA	CD4053	
	Solitron	CM4053	
	SSS	SCL4053	
	Toshiba	TC4053	
CD4060	Mitel	SIL4060	
	RCA	CD4060	
	SSS	SCL4060	
CD4066	Fairchild	F4066	
	Mitel	SIL4066	
	Motorola	MC14066	
	NEC America	μPD4066	
	RCA	CD4066	
	SGS	HBF4066	
	Signetics	N4066	
	Solitron	CM4066	
	SSS	SCL4066	
	Toshiba	TC4066	
CD4069	Fairchild	F4069	
	Harris	HD74C04	
	Mitel	SIL4069	
	Motorola	MC14069	
	National	MM74C04	
	NEC America	μPD4069	
	RCA	CD4069	
	Solitron	CM4069	
	SSS	SCL4069	
	TI	TP4069	
	Toshiba	TC4069	
CD4070	Fairchild	F4070	
	Mitel	SIL4070	
	Motorola	MC14507	
	National	CD4507	
		MM74C86	
	RCA	CD4030	
		CD4070	
	Solitron	CM4070	
	SSS	SCL4030	
		SCL4070	
	TI	TP4507	
CD4071	Fairchild	F4071	
	Mitel	SIL4071	
	Motorola	MC14071	
	NEC America	μPD4071	
	RCA	CD4071	
	Solitron	CM4071	
	SSS	SCL4071	
	TI	TP4071	
	Toshiba	TC4071	
CD4073	Fairchild	F4073	
	Mitel	SIL4073	
	Motorola	MC14073	
	NEC America	μPD4073	
	RCA	CD4073	
	Solitron	CM4073	
	SSS	SCL4073	
	TI	TP4073	
	Toshiba	TC4073	
CD4075	Fairchild	F4075	
	Mitel	SIL4075	
	Motorola	MC14075	
	NEC America	μPD4075	
CD4075	RCA	CD4075	
	SSS	SCL4075	
	TI	TP4075	
	Toshiba	TC4075	
CD4076	Fairchild	F4076	
	Harris	HD74C173	
	Mitel	SIL4076	
	Motorola	MC14076	
	RCA	CD4076	
	Solitron	CM4076	
	SSS	SCL4076	
CD4081	Fairchild	F4081	
	Mitel	SIL4081	
	Motorola	MC14081	
	NEC America	μPD4081	
	RCA	CD4081	
	Solitron	CM4081	
	SSS	SCL4081	
	TI	TP4081	
	Toshiba	TC4081	
CD4089	RCA	CD4089	
CD4093	Fairchild	F4093	
	Motorola	MC14093	
	NEC America	μPD4093	
	RCA	CD4093	
CD4099	Fairchild	F4099	
	NEC America	μPD4099	
	RCA	CD4099	
CD4503	Motorola	MC14503	
	NEC America	μPD4503	
CD4507	Motorola	MC14507	
	National	CD4070	
		MM74C86	
	RCA	CD4030	
		CD4070	
	SSS	SCL4030	
	TI	TP4507	
CD4510	Fairchild	F4510	
	Mitel	SIL4510	
	Motorola	MC14510	
	NEC America	μPD4510	
	RCA	CD40192	
		CD4510	
	SSS	SCL4510	
	Toshiba	TC4510	
CD4511	Fairchild	F4511	
	Mitel	SIL4511	
	Motorola	MC14511	
	NEC America	μPD4511	
	RCA	CD4511	
	Solitron	CM4511	
	SSS	SCL4511	
	TI	TP4511	
CD4512	Fairchild	F4512	
	Mitel	SIL4512	
	Motorola	MC14512	
	NEC America	μPD4512	
	SSS	SCL4512	
	TI	TP4512	
	Toshiba	TC4512	
CD4514	Fairchild	F4514	
	Mitel	SIL4514	
	Motorola	MC14514	
	RCA	CD4514	
	SSS	SCL4514	
	Toshiba	TC4514	
CD4515	Fairchild	F4515	
	Mitel	SIL4515	
	Motorola	MC14515	
	RCA	CD4515	
	SSS	SCL4515	
	Toshiba	TC4515	
CD4516	Fairchild	F4516	
	Mitel	SIL4516	
	Motorola	MC14516	
	NEC America	μPD4516	
	RCA	CD40193	
		CD4516	
	SSS	SCL4516	
	Toshiba	TC4516	
CD4518	Fairchild	F4518	
	Mitel	SIL4518	
	Motorola	MC14518	
	NEC America	μPD4518	
	RCA	CD4518	
	Solitron	CM4518	
CD4518	SSS	SCL4518	
	TI	TP4518	
	Toshiba	TC4518	
CD4519	Fairchild	F4519	
	Motorola	MC14519	
	NEC America	μPD4519	
	RCA	CD4019	
	TI	TP4519	
CD4520	Fairchild	F4520	
	Mitel	SIL4520	
	Motorola	MC14520	
	NEC America	μPD4520	
	RCA	CD4520	
	Solitron	CM4520	
	SSS	SCL4520	
	TI	TP4520	
	Toshiba	TC4520	
CD4522	Fairchild	F4522	
	Motorola	MC14522	
	SSS	SCL4522	
	TI	TP4522	
CD4527	Motorola	MC14527	
	RCA	CD4527	
	SSS	SCL4527	
CD4528	Fairchild	F4528	
	Motorola	MC14528	
	NEC America	μPD4528	
	RCA	CD4528	
	SSS	SCL4528	
CD4529	Motorola	MC14529	
CD4543	Motorola	MC14543	
	SSS	SCL4543	
CD4584	Motorola	MC14584	
	National	**MM74C14**	**262**
	NEC America	μPD4584	
	RCA	CD4016	
	SSS	SCL4584	
DAC0800	**Datel**	**DAC-08B**	**670**
	PMI	DAC-08	
DAC0801	**Datel**	**DAC-08B**	**670**
	PMI	DAC-08	
DAC1285	Micro Net	DAC85	
♦DH3724	RCA	CA3724	
DH3725	RCA	CA3725	
DM10101	Fairchild	F10101	
	Motorola	MC10101	
DM10102	Fairchild	F10102	
	Motorola	MC10102	
DM10105	Fairchild	F10105	
	Hitachi	HD10105	
	Motorola	MC10105	
	NEC America	μPB10105	
	Signetics	10105	
DM10106	Fairchild	F10106	
	Hitachi	HD10106	
	Motorola	MC10106	
	NEC America	μPB10106	
	Signetics	10106	
♦DM10107	Motorola	MC10107	
DM10109	Fairchild	F10109	
	Hitachi	HD10109	
	Motorola	MC10109	
	NEC America	μPB10109	
	Signetics	10109	
♦DM10110	Motorola	MC10110	
DM10111	Fairchild	F10111	
	Hitachi	HD10111	
	Motorola	MC10111	
	NEC America	μPB10111	
	Signetics	10111	
DM10112	Signetics	10112	
DM10115	Fairchild	F10115	
	Motorola	MC10115	
	NEC America	μPB10115	
	Signetics	10115	
♦DM10116	Fairchild	F10116	
	Hitachi	HD10116	
	Motorola	MC10116	
	Signetics	10116	
DM10117	Fairchild	F10117	
	Hitachi	HD10117	
	Motorola	MC10117	
	NEC America	μPB10117	
	Signetics	10117	
DM10118	Fairchild	F10118	
	Hitachi	HD10118	

♦ Discontinued

Bold face device numbers indicate manufacturers data is provided in the IC Master on the pages noted.

National Semiconductor (cont'd)

Manufacturer Device	Replacement Source	Device	IC Master Page
DM10118	Motorola	MC10118	
	NEC America	μPB10118	
	Signetics	10118	
DM10119	Fairchild	F10119	
	Hitachi	HD10119	
	Motorola	MC10119	
	Signetics	10119	
DM10121	Fairchild	F10121	
	Hitachi	HD10121	
	Motorola	MC10121	
	Signetics	10121	
DM10124	Fairchild	F10124	
	Hitachi	HD10124	
	Motorola	MC10124	
	NEC America	μPB10124	
	Signetics	10124	
♦DM10130	Motorola	MC10130	
♦DM1800	Motorola	MC1800	
♦DM1801	Motorola	MC1801	
DM27LS08	**Harris**	**HM7608**	**1290**
	Raytheon	**29635**	**1662**
DM54H00	Fairchild	54H00	
	Raytheon	54H00	
	Signetics	54H00	
	TI	SN54H00	
DM54H01	Fairchild	54H01	
	Raytheon	54H01	
	Signetics	54H01	
	TI	SN54H01	
DM54H04	Fairchild	54H04	
	Raytheon	54H04	
	Signetics	54H04	
	TI	SN54H04	
DM54H05	Fairchild	54H05	
	Raytheon	54H05	
	Signetics	54H05	
	TI	SN54H05	
DM54H08	Fairchild	54H08	
	Signetics	54H08	
DM54H10	Fairchild	54H10	
	Raytheon	54H10	
	Signetics	54H10	
	TI	SN54H10	
DM54H103	Fairchild	54H103	
	Signetics	54H103	
	TI	SN54H103	
DM54H106	Fairchild	54H106	
	Signetics	54H106	
	TI	SN54H106	
DM54H108	Fairchild	54H108	
	Signetics	54H108	
	TI	SN54H108	
DM54H11	Fairchild	54H11	
	Raytheon	54H11	
	Signetics	54H11	
	TI	SN54H11	
DM54H20	Fairchild	54H20	
	Raytheon	54H20	
	Signetics	54H20	
	TI	SN54H20	
DM54H21	Fairchild	54H21	
	Signetics	54H21	
DM54H22	Fairchild	54H22	
	Raytheon	54H22	
	Signetics	54H22	
	TI	SN54H22	
DM54H30	Fairchild	54H30	
	Signetics	54H30	
	TI	SN54H30	
DM54H40	Fairchild	54H40	
	Raytheon	54H40	
	Signetics	54H40	
	TI	SN54H40	
DM54H50	Fairchild	54H50	
	Signetics	54H50	
	TI	SN54H50	
DM54H51	Fairchild	54H51	
	Signetics	54H51	
	TI	SN54H51	
DM54H52	Fairchild	54H52	
	Signetics	54H52	
	TI	SN54H52	
DM54H53	Fairchild	54H53	
	Signetics	54H53	
	TI	SN54H53	
DM54H54	Fairchild	54H54	
	Signetics	54H54	
	TI	SN54H54	
DM54H55	Fairchild	54H55	
	Signetics	54H55	
	TI	SN54H55	
DM54H60	Fairchild	54H60	
	Signetics	54H60	
	TI	SN54H60	
DM54H61	Fairchild	54H61	
	Signetics	54H61	
	TI	SN54H61	
DM54H62	Fairchild	54H62	
	Signetics	54H62	
	TI	SN54H62	
DM54H71	Fairchild	54H71	
	Signetics	54H71	
	TI	SN54H71	
DM54H72	Fairchild	54H72	
		54H73	
	Signetics	54H72	
	TI	SN54H72	
DM54H73	Fairchild	54H73	
	Signetics	54H73	
	TI	SN54H73	
DM54H74	Fairchild	54H74	
	Raytheon	54H74	
	Signetics	54H74	
	TI	SN54H74	
DM54H76	Fairchild	54H76	
	Signetics	54H76	
	TI	SN54H76	
DM54H78	Fairchild	54H78	
	TI	SN54H78	
DM54LS00	Fairchild	54LS00	
	Motorola	SN54LS00	
	Raytheon	54LS00	
	Signetics	54LS00	
	TI	SN54LS00	
DM54LS01	Raytheon	54LS01	
	Signetics	54LS01	
	TI	SN54LS01	
DM54LS02	Fairchild	54LS02	
	Motorola	SN54LS02	
	Raytheon	54LS02	
	Signetics	54LS02	
	TI	SN54LS02	
DM54LS03	Fairchild	54LS03	
	Motorola	SN54LS03	
	Raytheon	54LS03	
	Signetics	54LS03	
	TI	SN54LS03	
DM54LS04	Fairchild	54LS04	
	Motorola	SN54LS04	
	Raytheon	54LS04	
	Signetics	54LS04	
	TI	SN54LS04	
DM54LS05	Fairchild	54LS05	
	Motorola	SN54LS05	
	Raytheon	54LS05	
	Signetics	54LS05	
	TI	SN54LS05	
DM54LS08	Fairchild	54LS08	
	Motorola	SN54LS08	
	Raytheon	54LS08	
	Signetics	54LS08	
	TI	SN54LS08	
DM54LS09	Fairchild	54LS09	
	Motorola	SN54LS09	
	Raytheon	54LS09	
	Signetics	54LS09	
	TI	SN54LS09	
DM54LS10	Fairchild	54LS10	
	Motorola	SN54LS10	
	Raytheon	54LS10	
	Signetics	54LS10	
	TI	SN54LS10	
DM54LS107	Fairchild	54LS107	
	Raytheon	54LS107	
	Signetics	54LS107	
DM54LS107A	Motorola	SN54LS107	
	TI	SN54LS107	
DM54LS109	Fairchild	54LS109	
	Raytheon	54LS109	
	Signetics	54LS109	
DM54LS109A	Motorola	SN54LS109	
	TI	SN54LS109	
DM54LS11	Fairchild	54LS11	
	Motorola	SN54LS11	
	Raytheon	54LS11	
	Signetics	54LS11	
	TI	SN54LS11	
DM54LS112	Fairchild	54LS112	
	Motorola	SN54LS112A	
	Raytheon	54LS112	
	Signetics	54LS112	
	TI	SN54LS112	
DM54LS113	Fairchild	54LS113	
	Motorola	SN54LS113A	
	Raytheon	54LS113	
	Signetics	54LS113	
	TI	SN54LS113	
DM54LS114	Fairchild	54LS114	
	Raytheon	54LS114	
	Signetics	54LS114	
DM54LS114A	Motorola	SN54LS114	
	TI	SN54LS114	
DM54LS12	Motorola	SN54LS12	
	Raytheon	54LS12	
	Signetics	54LS12	
	TI	SN54LS12	
DM54LS122	Raytheon	54LS122	
	TI	SN54LS122	
DM54LS123	AMD	SN54LS123	
	Raytheon	54LS123	
	TI	SN54LS123	
DM54LS125	Fairchild	54LS125	
	Raytheon	54LS125	
	Signetics	54LS125	
	TI	SN54LS125A	
DM54LS126	Fairchild	54LS126	
	Motorola	SN54LS126	
	Raytheon	54LS126	
	Signetics	54LS126	
	TI	SN54LS126A	
DM54LS13	Fairchild	54LS13	
	Motorola	SN54LS13	
	Raytheon	54LS13	
	Signetics	54LS13	
	TI	SN54LS13	
DM54LS132	Fairchild	54LS132	
	Motorola	SN54LS132	
	Raytheon	54LS132	
		74LS132	
	Signetics	54LS132	
	TI	SN54LS132	
DM54LS138	Fairchild	54LS138	
	Motorola	SN54LS138	
	Raytheon	54LS138	
	Signetics	54LS138	
	TI	SN54LS138	
DM54LS139	AMD	SN54LS139	
	Fairchild	54LS139	
	Motorola	SN54LS139	
	Raytheon	54LS139	
	Signetics	74LS139	
	TI	SN54LS139	
DM54LS14	Fairchild	54LS14	
	Motorola	SN54LS14	
	Raytheon	54LS14	
	Signetics	54LS14	
	TI	SN54LS14	
DM54LS15	Fairchild	54LS15	
	Motorola	SN54LS15	
	Raytheon	54LS15	
	Signetics	54LS15	
	TI	SN54LS15	
DM54LS151	AMD	SN54LS151	
	Fairchild	54LS151	
	Motorola	SN54LS151	
	Raytheon	54LS151	
	Signetics	54LS151	
	TI	SN54LS151	
DM54LS153	AMD	SN54LS153	
	Fairchild	54LS153	
	Motorola	SN54LS153	
	Raytheon	54LS153	
	Signetics	54LS153	
	TI	SN54LS153	
DM54LS154	Signetics	54LS154	
DM54LS155	Fairchild	54LS155	
	Motorola	SN54LS155	
	Raytheon	74LS155	
	TI	SN54LS155	
DM54LS156	Fairchild	54LS156	
	Motorola	SN54LS156	
	Raytheon	54LS156	
	TI	SN54LS156	
DM54LS157	AMD	SN54LS157	
	Fairchild	54LS157	
	Motorola	SN54LS157	
	Raytheon	54LS157	
	Signetics	54LS157	
	TI	SN54LS157	
DM54LS158	Fairchild	54LS158	
	Motorola	SN54LS158	
	Raytheon	54LS158	
	Signetics	54LS158	
	TI	SN54LS158	
DM54LS160	AMD	SN54LS160	
	Fairchild	54LS160	
	Raytheon	54LS160	
DM54LS160A	Motorola	SN54LS160	
	TI	SN54LS160	
DM54LS161	AMD	SN54LS161	
	Fairchild	54LS161	
	Raytheon	54LS161	
DM54LS161A	Motorola	SN54LS161	
	Signetics	54LS161	
	TI	SN54LS161	
DM54LS162	AMD	SN54LS162	
	Fairchild	54LS162	
	Raytheon	54LS162	
DM54LS162A	Motorola	SN54LS162	
	TI	SN54LS162	
DM54LS163	AMD	SN54LS163	
	Fairchild	54LS163	
	Raytheon	54LS163	
DM54LS163A	Motorola	SN54LS163	
	Signetics	54LS163	
	TI	SN54LS163	
DM54LS164	AMD	SN54LS164	
	Fairchild	54LS164	
	Raytheon	54LS164	
	Signetics	54LS164	
DM54LS164A	Motorola	SN54LS164	
	TI	SN54LS164	
DM54LS168	AMD	SN54LS168	
	Fairchild	54LS168	
	TI	SN54LS168	
DM54LS169	AMD	SN54LS169	
	Fairchild	54LS169	
	TI	SN54LS169	
DM54LS170	AMD	SN54LS170	
	Fairchild	54LS170	
	Motorola	SN54LS170	
	Raytheon	54LS170	
	Signetics	54LS170	
	TI	SN54LS170	
DM54LS173	Fairchild	54LS173	
	Signetics	54LS173	
	TI	SN54LS173	
DM54LS174	AMD	SN54LS174	
	Fairchild	54LS174	
	Raytheon	54LS174	
	Signetics	54LS174	
	TI	SN54LS174	
DM54LS175	AMD	SN54LS175	
	Fairchild	54LS175	
	Motorola	SN54LS175	
	Raytheon	54LS175	
	Signetics	54LS175	
	TI	SN54LS175	
DM54LS190	AMD	SN54LS190	
	Fairchild	54LS190	
	Motorola	SN54LS190	
	Raytheon	54LS190	
	Signetics	54LS190	
	TI	SN54LS190	
DM54LS191	AMD	SN54LS191	
	Fairchild	54LS191	
	Motorola	SN54LS191	
	Raytheon	54LS191	
	Signetics	54LS191	
	TI	SN54LS191	

♦ Discontinued

The manufacturers report their devices can be used as direct replacements.
Performance details often differ, so compare the specifications considering your requirements.

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Manufacturer Device	Replacement Source	Device	IC Master Page
DM54LS192	AMD	SN54LS192	
	Fairchild	54LS192	
	Motorola	SN54LS192	
	Raytheon	54LS192	
	Signetics	54LS192	
	TI	SN54LS192	
DM54LS193	AMD	SN54LS193	
	Fairchild	54LS193	
	Motorola	SN54LS193	
	Raytheon	54LS193	
	Signetics	54LS193	
	TI	SN54LS193	
DM54LS196	Fairchild	54LS196	
	Motorola	SN54LS196	
	Raytheon	54LS196	
	TI	SN54LS196	
DM54LS197	Fairchild	54LS197	
	Motorola	SN54LS197	
	Raytheon	54LS197	
	TI	SN54LS197	
DM54LS20	Fairchild	54LS20	
	Motorola	SN54LS20	
	Raytheon	54LS20	
	Signetics	54LS20	
	TI	SN54LS20	
DM54LS21	Fairchild	54LS21	
	Motorola	SN54LS21	
	Raytheon	54LS21	
	Signetics	54LS21	
	TI	SN54LS21	
DM54LS22	Fairchild	54LS22	
	Motorola	SN54LS22	
	Raytheon	54LS22	
	Signetics	54LS22	
	TI	SN54LS22	
DM54LS221	Raytheon	54LS221	
	Signetics	54LS221	
	TI	SN54LS221	
DM54LS247	Fairchild	54LS247	
	Motorola	SN54LS247	
	TI	SN54LS247	
DM54LS248	Fairchild	54LS248	
	Motorola	SN54LS248	
	TI	SN54LS248	
DM54LS249	Fairchild	54LS249	
	Motorola	SN54LS249	
	TI	SN54LS249	
DM54LS253	AMD	SN54LS253	
	Fairchild	54LS253	
	Motorola	SN54LS253	
	Raytheon	54LS253	
	Signetics	54LS253	
	TI	SN54LS253	
DM54LS257	Fairchild	54LS257	
	Motorola	SN54LS257	
	Raytheon	54LS257	
	Signetics	54LS257	
	TI	SN54LS257	
DM54LS26	Fairchild	54LS26	
	Motorola	SN54LS26	
	Raytheon	54LS26	
	Signetics	54LS26	
	TI	SN54LS26	
DM54LS27	Fairchild	54LS27	
	Motorola	SN54LS27	
	Raytheon	54LS27	
	Signetics	54LS27	
	TI	SN54LS27	
DM54LS279	Fairchild	54LS279	
	Motorola	SN54LS279	
	Raytheon	74LS279	
	Signetics	54LS279	
	TI	SN54LS279	
DM54LS283	Fairchild	54LS283	
	Motorola	SN54LS283	
	Raytheon	54LS283	
	TI	SN54LS283	
DM54LS290	Motorola	SN54LS290	
DM54LS293	Motorola	SN54LS293	
DM54LS30	Fairchild	54LS30	
	Motorola	SN54LS30	
	Raytheon	54LS30	
DM54LS30	Signetics	54LS30	
	TI	SN54LS30	
DM54LS32	Fairchild	54LS32	
	Motorola	SN54LS32	
	Raytheon	54LS32	
	Signetics	54LS32	
	TI	SN54LS32	
DM54LS352	Fairchild	54LS352	
	Motorola	SN54LS352	
	TI	SN54LS352	
DM54LS353	Fairchild	54LS353	
	Motorola	SN54LS353	
	TI	SN54LS353	
DM54LS37	Fairchild	54LS37	
	Motorola	SN54LS37	
	Raytheon	54LS37	
	Signetics	54LS37	
	TI	SN54LS37	
DM54LS38	Fairchild	54LS38	
	Motorola	SN54LS38	
	Raytheon	54LS38	
	Signetics	54LS38	
	TI	SN54LS38	
DM54LS395	Fairchild	54LS395	
	Raytheon	54LS395	
	Signetics	54LS395	
	TI	SN54LS395	
DM54LS40	Fairchild	54LS40	
	Motorola	SN54LS40	
	Raytheon	54LS40	
	Signetics	54LS40	
	TI	SN54LS40	
DM54LS42	Fairchild	54LS42	
	Motorola	SN54LS42	
	Raytheon	54LS42	
	Signetics	54LS42	
	TI	SN54LS42	
DM54LS49	Motorola	SN54LS49	
DM54LS51	Fairchild	54LS51	
	Motorola	SN54LS51	
	Raytheon	54LS51	
	Signetics	54LS51	
	TI	SN54LS51	
DM54LS54	Fairchild	54LS54	
	Motorola	SN54LS54	
	Raytheon	54LS54	
	Signetics	54LS54	
	TI	SN54LS54	
DM54LS55	Fairchild	54LS55	
	Motorola	SN54LS55	
	Raytheon	54LS55	
	Signetics	54LS55	
	TI	SN54LS55	
DM54LS670	Fairchild	54LS670	
	Motorola	SN54LS670	
	Raytheon	54LS670	
	Signetics	54LS670	
	TI	SN54LS670	
DM54LS73	Fairchild	54LS73	
	Motorola	SN54LS73	
	Raytheon	54LS73	
	Signetics	54LS73	
DM54LS73A	TI	SN54LS73	
DM54LS74	Fairchild	54LS74	
	Raytheon	54LS74	
	Signetics	54LS74	
DM54LS74A	Motorola	SN54LS74	
	TI	SN54LS74	
DM54LS75	Motorola	SN54LS75	
	Raytheon	54LS75	
	Signetics	54LS75	
	TI	SN54LS75	
DM54LS76	Fairchild	74LS76	
	Motorola	SN54LS76A	
	Raytheon	54LS76	
	Signetics	54LS76	
	TI	SN54LS76	
DM54LS77	Motorola	SN74LS77	
DM54LS78	Fairchild	54LS78	
	Motorola	SN54LS78A	
	Raytheon	54LS78	
	Signetics	54LS78	
	TI	SN54LS78	
DM54LS83A	Fairchild	54LS83	
	Motorola	SN54LS83	
	Raytheon	54LS83A	
DM54LS83A	TI	SN54LS83A	
DM54LS85	Fairchild	54LS85	
	Motorola	SN54LS85	
	Raytheon	54LS85	
	Signetics	54LS85	
	TI	SN54LS85	
DM54LS93	Fairchild	54LS93	
	Motorola	SN54LS93	
	Raytheon	54LS93	
	Signetics	54LS93	
	TI	SN54LS93	
DM54L187	Intersil	IM5603	
DM54L89	MMI	L5560	
	TI	**SN54S287**	**1708**
DM54SL136	Motorola	SN54SL136	
DM54SL170	Motorola	SN54SL170	
DM54S188	AMD	AM27S18	
	MMI	**53S080**	**1453**
DM54S200	**Fairchild**	**93421**	**1252**
DM54S206	Fairchild	93411	
DM54S22	Fairchild	54S22	
	Signetics	54S22	
	TI	SN54S22	
DM54S287	AMD	AM27S21	
	Fairchild	**93427**	**1258**
	MMI	**53S141**	**1453**
	Raytheon	**29661**	**1664**
DM54S288	AMD	AM27S19	
	MMI	**53S081**	**1453**
DM54S387	AMD	AM27S20	
	Fairchild	**93417**	**1258**
	MMI	**53S140**	**1453**
		5300-1	**1449**
	Raytheon	**29660**	**1664**
	TI	**SN54S387**	**1708**
DM54S470	**MMI**	**5308-1**	**1449**
	Raytheon	**29600**	**1652**
DM54S471	**MMI**	**5309-1**	**1449**
	Raytheon	**29601**	**1652**
DM54S472	**MMI**	**5349-1**	**1449**
	Raytheon	**29621**	**1656**
DM54S473	**MMI**	**5348-1**	**1449**
	Raytheon	**29620**	**1656**
DM54S570	**Fairchild**	**93436**	**1260**
	MMI	**5305-1**	**1449**
	Raytheon	**29610**	**1654**
DM54S571	**Fairchild**	**93446**	**1260**
	MMI	**5306-1**	**1449**
	Raytheon	**29611**	**1654**
DM54S572	**Fairchild**	**93452**	**1264**
	MMI	**5352-1**	**1449**
	Raytheon	29640	
DM54S573	**Fairchild**	**93453**	**1264**
	MMI	**5353-1**	**1449**
	Raytheon	29641	
DM5400	Fairchild	5400	
	Motorola	MC5400	
	Signetics	5400	
	TI	SN5400	
DM5401	Fairchild	5401	
	Motorola	MC5401	
	Signetics	5401	
	TI	SN5401	
DM5402	Fairchild	5402	
	Motorola	MC5402	
	Signetics	5402	
	TI	SN5402	
DM5403	Fairchild	5403	
	Motorola	MC5403	
	Signetics	5403	
	TI	SN5403	
DM5404	Fairchild	5404	
	Motorola	MC5404	
	Signetics	5404	
	TI	SN5404	
DM5405	Fairchild	5405	
	Motorola	MC5405	
	Signetics	5405	
	TI	SN5405	
DM5406	Fairchild	5406	
	Motorola	MC5406	
	Signetics	5406	
	TI	SN5406	
DM5407	Fairchild	5407	
	Motorola	MC5407	
	Signetics	5407	
DM5407	TI	SN5407	
DM5408	Fairchild	5408	
	Motorola	MC5408	
	Signetics	5408	
	TI	SN5408	
DM5409	Fairchild	5409	
	Motorola	MC5409	
	Signetics	5409	
	TI	SN5409	
DM5410	Fairchild	5410	
	Motorola	MC5410	
	Signetics	5410	
	TI	SN5410	
DM54107	Fairchild	54107	
	Motorola	MC54107	
	Signetics	54107	
	TI	SN54107	
DM54109	Signetics	54109	
	TI	SN54109	
DM5411	Fairchild	5411	
	Signetics	5411	
	TI	SN5411	
DM54121	Fairchild	54121	
	Motorola	MC54121	
	Signetics	54121	
	TI	SN54121	
DM54123	AMD	SN54123	
	Fairchild	54123	
	Motorola	MC54123	
	Signetics	54123	
	TI	SN54123	
DM54125	Fairchild	54125	
	Signetics	54125	
	TI	SN54125	
DM54126	Fairchild	54126	
	Signetics	54126	
	TI	SN54126	
DM5413	Fairchild	5413	
	Motorola	MC5413	
	Signetics	5413	
	TI	SN5413	
DM54132	Fairchild	54132	
	Motorola	MC54132	
	Signetics	54132	
	TI	SN54132	
♦DM54136	Raytheon	54136	
DM5414	Fairchild	5414	
	Motorola	MC5414	
	Signetics	5414	
	TI	SN5414	
DM54141	Motorola	MC54141	
	TI	SN54141	
DM54145	Fairchild	54145	
	Motorola	MC54145	
	Signetics	54145	
	TI	SN54145	
DM54147	Signetics	54147	
	TI	SN54147	
DM54148	Fairchild	9318	
	Signetics	54148	
	TI	SN54148	
♦DM5415	Raytheon	5415	
DM54150	Fairchild	54150	
	Motorola	MC54150	
	Signetics	54150	
	TI	SN54150	
DM54151	Fairchild	54151	
	Motorola	MC54151	
	Signetics	54151	
	TI	SN54151	
♦DM54152	Raytheon	54152	
DM54153	AMD	SN54153	
	Fairchild	54153	
	Motorola	MC54153	
	Signetics	54153	
	TI	SN54153	
DM54154	AMD	SN54154	
	Fairchild	54154	
	Motorola	MC54154	
	Signetics	54154	
	TI	SN54154	
DM54155	Fairchild	54155	
	Motorola	MC54155	
	Signetics	54155	
	TI	SN54155	
DM54156	Fairchild	54156	

♦ Discontinued

Bold face device numbers indicate manufacturers data is provided in the IC Master on the pages noted.

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Manufacturer Device	Replacement Source	Device	IC Master Page
DM54156	Motorola	MC54156	
	Signetics	54156	
	TI	SN54156	
DM54157	AMD	SN54157	
	Fairchild	54157	
	Motorola	MC54157	
	Raytheon	54157	
	Signetics	54157	
	TI	SN54157	
DM5416	Fairchild	5416	
	Motorola	MC5416	
	Signetics	5416	
	TI	SN5416	
DM54160	AMD	SN54160	
	Fairchild	54160	
	Motorola	MC54160	
	Signetics	54160	
	TI	SN54160	
DM54161	AMD	SN54161	
	Fairchild	54161	
	Motorola	MC54161	
	Signetics	54161	
	TI	SN54161	
DM54162	AMD	SN54162	
	Fairchild	54162	
	Motorola	MC54162	
	Signetics	54162	
	TI	SN54162	
DM54163	AMD	SN54163	
	Fairchild	54163	
	Motorola	MC54163	
	Signetics	54163	
	TI	SN54163	
DM54164	AMD	SN54164	
	Fairchild	54164	
	Signetics	54164	
	TI	SN54164	
DM54165	Fairchild	54165	
	Motorola	MC54165	
	Signetics	54165	
	TI	SN54165	
DM54166	Fairchild	54166	
	Signetics	54166	
	TI	SN54166	
DM5417	Fairchild	5417	
	Motorola	MC5417	
	Signetics	5417	
	TI	SN5417	
♦DM54170	Fairchild	54170	
	Signetics	54170	
	TI	SN54170	
DM54173	Fairchild	54173	
	TI	SN54173	
DM54174	AMD	SN74174	
	Fairchild	54174	
	Motorola	MC54174	
	Signetics	54174	
	TI	SN54174	
DM54175	AMD	SN54175	
	Fairchild	54175	
	Motorola	MC54175	
	Signetics	54175	
	TI	SN54175	
DM54176	Fairchild	54176	
	Motorola	MC54176	
	Signetics	54176	
	TI	SN54176	
DM54177	Fairchild	54177	
	Motorola	MC54177	
	Signetics	54177	
	TI	SN54177	
DM54180	Fairchild	54180	
	Motorola	MC54180	
	Signetics	54180	
	TI	SN54180	
DM54181	AMD	SN54181	
	Fairchild	54181	
	Motorola	MC54181	
	Signetics	54181	
	TI	SN54181	
DM54182	AMD	SN54182	
	Fairchild	54182	
DM54182	Motorola	MC54182	
	Signetics	54182	
	TI	SN54182	
DM54184	TI	SN54184	
DM54185	TI	SN54185	
♦DM54187	Intersil	IM5603	
	MMI	**5200-1**	**1466**
	National	DM54S187	
	TI	SN54187	
DM54190	Fairchild	54190	
	Motorola	MC54190	
	Signetics	54190	
	TI	SN54190	
DM54191	Fairchild	54191	
	Motorola	MC54191	
	Signetics	54191	
	TI	SN54191	
DM54192	AMD	SN54192	
	Fairchild	54192	
	Motorola	MC54192	
	Signetics	54192	
	TI	SN54192	
DM54193	AMD	SN54193	
	Fairchild	54193	
	Motorola	MC54193	
	Signetics	54193	
	TI	SN54193	
DM54194	AMD	SN54194	
	Fairchild	54194	
	Motorola	MC54194	
	Signetics	54194	
	TI	SN54194	
DM54195	AMD	SN54195	
	Fairchild	54195	
	Motorola	MC54195	
	Signetics	54195	
	TI	SN54195	
DM54196	Fairchild	54196	
	Motorola	MC54196	
	Signetics	54196	
	TI	SN54196	
DM54197	Fairchild	54197	
	Motorola	MC54197	
	Signetics	54197	
	TI	SN54197	
DM54198	Fairchild	54198	
	Signetics	54198	
	TI	SN54198	
DM54199	Fairchild	54199	
	Signetics	54199	
	TI	SN54199	
DM5420	Fairchild	5420	
	Motorola	MC5420	
	Signetics	5420	
	TI	SN5420	
♦DM54200	MMI	5531	
	Raytheon	RM5340	
	TI	SN54S201	
DM5423	Fairchild	5423	
	Motorola	MC5423	
	TI	SN5423	
DM5425	Fairchild	5425	
	Motorola	MC5425	
	TI	SN5425	
DM5426	Fairchild	5426	
	Motorola	MC5426	
	Signetics	5426	
	TI	SN5426	
DM5427	Fairchild	5427	
	Motorola	MC5427	
	TI	SN5427	
DM5430	Fairchild	5430	
	Motorola	MC5430	
	Signetics	5430	
	TI	SN5430	
DM5432	Fairchild	5432	
	Signetics	5432	
	TI	SN5432	
DM5437	Fairchild	5437	
	Motorola	MC5437	
	Signetics	5437	
	TI	SN5437	
DM5438	Fairchild	5438	
	Motorola	MC5438	
	Signetics	5438	
	TI	SN5438	
DM5440	Fairchild	5440	
	Motorola	MC5440	
	Signetics	5440	
	TI	SN5440	
DM5441	Fairchild	5441	
DM5442	Fairchild	5442	
	Motorola	MC5442	
	Raytheon	5442	
	Signetics	5442	
	TI	SN5442	
DM5445	Fairchild	5445	
	Motorola	MC5445	
	Signetics	5445	
	TI	SN5445	
DM5446	Fairchild	5446	
	Motorola	MC5446	
	Signetics	5446	
	TI	SN5446	
DM5447	Fairchild	5447	
	Motorola	MC5447	
	Signetics	5447	
	TI	SN5447	
DM5448	Fairchild	5448	
	Motorola	MC5448	
	Signetics	5448	
	TI	SN5448	
DM5450	Fairchild	5450	
	Motorola	MC5450	
	Signetics	5450	
	TI	SN5450	
DM5451	Fairchild	5451	
	Motorola	MC5451	
	Signetics	5451	
	TI	SN5451	
DM5453	Fairchild	5453	
	Motorola	MC5453	
	Signetics	5453	
	TI	SN5453	
DM5454	Fairchild	5454	
	Motorola	MC5454	
	Signetics	5454	
	TI	SN5454	
DM5460	Fairchild	5460	
	Motorola	MC5460	
	Signetics	5460	
	TI	SN5460	
DM5470	Fairchild	5470	
	Motorola	MC5470	
	TI	SN5470	
DM5472	Fairchild	5472	
	Motorola	MC5472	
	Signetics	5472	
	TI	SN5472	
DM5473	Fairchild	5473	
	Motorola	MC5473	
	Signetics	5473	
	TI	SN5473	
DM5474	Fairchild	5474	
	Motorola	MC5474	
	Signetics	5474	
	TI	SN5474	
DM5475	Fairchild	5475	
	Motorola	MC5475	
	Signetics	5475	
	TI	SN5475	
DM5476	Fairchild	5476	
	Motorola	MC5476	
	Signetics	5476	
	TI	SN5476	
DM5485	Fairchild	5485	
	Motorola	MC5485	
	Signetics	5485	
	TI	SN5485	
DM5486	Fairchild	5486	
	Motorola	MC5486	
	Signetics	5486	
	TI	SN5486	
DM5488	Intersil	IM5600	
	MMI	**5230-1**	**1466**
	TI	SN5488	
		SN5488A	
DM5489	AMD	SN5489	
		31013	
		5889	
	Fairchild	5489	
	MMI	5560	
DM5489	TI	SN5489	
DM5490	Fairchild	5490	
	Motorola	MC5490	
	Signetics	5490	
	TI	SN5490	
		SN5490A	
DM5491	Fairchild	5491	
	Motorola	MC5491	
	Signetics	5491	
	TI	SN5491	
		SN5491A	
DM5492	Fairchild	5492	
	Motorola	MC5492	
	Signetics	5492	
	TI	SN5492	
		SN5492A	
DM5493	Fairchild	5493	
	Motorola	MC5493	
	Signetics	5493	
	TI	SN5493	
		SN5493A	
DM5495	Fairchild	5495	
	Motorola	MC5495	
	Signetics	5495	
	TI	SN5495	
DM5496	Fairchild	5496	
	Motorola	MC5496	
	Signetics	5496	
	TI	SN5496	
DM7093	TI	SN54125	
DM7094	TI	SN54126	
DM7095	TI	SN54365	
DM7096	TI	SN54366	
DM7097	TI	SN54367	
DM7098	TI	SN54368	
DM71LS95	AMD	DM71LS95	
DM71LS96	AMD	DM71LS96	
DM71LS97	AMD	DM71LS97	
DM71LS98	AMD	DM71LS98	
DM71L22	TI	SN54L157	
DM71S60	Fairchild	93S43	
DM7121	TI	SN54251	
DM7123	TI	SN54S257	
DM7213	TI	SN54154	
DM7214	TI	SN54LS253	
DM7280	TI	SN54176	
DM7281	TI	SN54177	
DM7283	TI	SN54836	
DM7290	TI	SN54196	
DM7291	TI	SN54197	
DM74H00	Fairchild	74H00	
	NEC America	μPB74H00	
	Raytheon	74H00	
	Signetics	74H00	
	TI	SN74H00	
DM74H01	Fairchild	74H01	
	NEC America	μPB74H01	
	Raytheon	74H01	
	Signetics	74H01	
	TI	SN74H01	
DM74H04	Fairchild	74H04	
	NEC America	μPB74H04	
	Raytheon	74H04	
	Signetics	74H04	
	TI	SN74H04	
DM74H05	Fairchild	74H05	
	Raytheon	74H05	
	Signetics	74H05	
	TI	SN74H05	
DM74H08	Fairchild	74H08	
	Signetics	74H08	
DM74H10	Fairchild	74H10	
	NEC America	μPB74H10	
	Raytheon	74H10	
	Signetics	74H10	
	TI	SN74H10	
DM74H103	Fairchild	74H103	
	Signetics	74H103	
	TI	SN74H103	
DM74H106	Fairchild	74H106	
	Signetics	74H106	
	TI	SN74H106	
DM74H108	Fairchild	74H108	
	Signetics	74H108	
	TI	SN74H108	
DM74H11	Fairchild	74H11	

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The manufacturers report their devices can be used as direct replacements.
Performance details often differ, so compare the specifications considering your requirements.

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Manufacturer Device	Replacement Source	Device	IC Master Page
DM74H11	Raytheon	74H11	
	Signetics	74H11	
	TI	SN74H11	
DM74H20	Fairchild	74H20	
	NEC America	μPB74H20	
	Raytheon	74H20	
	Signetics	74H20	
	TI	SN74H20	
DM74H21	Fairchild	74H21	
	Signetics	74H21	
	TI	SN74H21	
DM74H22	Fairchild	74H22	
	Raytheon	74H22	
	Signetics	74H22	
	TI	SN74H22	
DM74H30	Fairchild	74H30	
	NEC America	μPB74H30	
	Signetics	74H30	
	TI	SN74H30	
DM74H40	Fairchild	74H40	
	NEC America	μPB74H40	
	Raytheon	74H40	
	Signetics	74H40	
	TI	SN74H40	
DM74H50	Fairchild	74H50	
	Signetics	74H50	
	TI	SN74H50	
DM74H51	Fairchild	74H51	
	NEC America	μPB74H51	
	Signetics	74H51	
	TI	SN74H51	
DM74H52	Fairchild	74H52	
	Signetics	74H52	
	TI	SN74H52	
DM74H53	Fairchild	74H53	
	Signetics	74H53	
	TI	SN74H53	
DM74H54	Fairchild	74H54	
	Signetics	74H54	
	TI	SN74H54	
DM74H55	Fairchild	74H55	
	Signetics	74H55	
	TI	SN74H55	
DM74H60	Fairchild	74H60	
	Signetics	74H60	
	TI	SN74H60	
DM74H62	Fairchild	74H62	
	Signetics	74H62	
	TI	SN74H62	
DM74H71	Fairchild	74H71	
	Signetics	74H71	
	TI	SN74H71	
DM74H72	Fairchild	74H72	
	Signetics	74H72	
	TI	SN74H72	
DM74H73	Fairchild	74H73	
	Signetics	74H73	
	TI	SN74H73	
DM74H74	Fairchild	74H74	
	Raytheon	74H74	
	Signetics	74H74	
	TI	SN74H74	
DM74H76	Fairchild	74H76	
	Signetics	74H76	
	TI	SN74H76	
DM74H78	Fairchild	74H78	
	TI	SN74H78	
DM74LS00	Fairchild	74LS00	
	Hitachi	HD74LS00	
	Motorola	SN74LS00	
	NEC America	μPB74LS00	
	Raytheon	74LS00	
	Signetics	74LS00	
	TI	SN74LS00	
DM74LS01	Hitachi	HD74LS01	
	Raytheon	74LS01	
	Signetics	74LS01	
	TI	SN74LS01	
DM74LS02	Fairchild	74LS02	
	Hitachi	HD74LS02	
	Motorola	SN74LS02	
	NEC America	μPB74LS02	
DM74LS02	Raytheon	74LS02	
	Signetics	74LS02	
	TI	SN74LS02	
DM74LS03	Fairchild	74LS03	
	Hitachi	HD74LS03	
	Motorola	SN74LS03	
	NEC America	μPB74LS03	
	Raytheon	74LS03	
	Signetics	74LS03	
	TI	SN74LS03	
DM74LS04	Fairchild	74LS04	
	Hitachi	HD74LS04	
	Motorola	SN74LS04	
	NEC America	μPB74LS04	
	Raytheon	74LS04	
	Signetics	74LS04	
	TI	SN74LS04	
DM74LS05	Fairchild	74LS05	
	Hitachi	HD74LS05	
	Motorola	SN74LS05	
	NEC America	μPB74LS05	
	Raytheon	74LS05	
	Signetics	74LS05	
	TI	SN74LS05	
DM74LS08	Fairchild	74LS08	
	Hitachi	HD74LS08	
	Motorola	SN74LS08	
	NEC America	μPB74LS08	
	Raytheon	74LS08	
	Signetics	74LS08	
	TI	SN74LS08	
DM74LS09	Fairchild	74LS09	
	Hitachi	HD74LS09	
	Motorola	SN74LS09	
	Raytheon	74LS09	
	Signetics	74LS09	
	TI	SN74LS09	
DM74LS10	Fairchild	74LS10	
	Hitachi	HD74LS10	
	Motorola	SN74LS10	
	NEC America	μPB74LS10	
	Raytheon	74LS10	
	Signetics	74LS10	
	TI	SN74LS10	
DM74LS107	Fairchild	74LS107	
	Hitachi	HD74LS107	
	Motorola	SN74LS107A	
	Raytheon	74LS107	
	Signetics	74LS107	
	TI	SN74LS107	
DM74LS109	Fairchild	74LS109	
	Motorola	SN74LS109A	
	NEC America	μPB74LS109	
	Raytheon	74LS109	
	Signetics	74LS109	
	TI	SN74LS109A	
DM74LS11	Fairchild	74LS11	
	Hitachi	HD74LS11	
	Motorola	SN74LS11	
	NEC America	μPB74LS11	
	Raytheon	74LS11	
	Signetics	74LS11	
	TI	SN74LS11	
DM74LS112	Fairchild	74LS112	
	Hitachi	HD74LS112	
	Motorola	SN74LS112A	
	NEC America	μPB74LS112	
	Raytheon	74LS112	
	Signetics	74LS112	
	TI	SN74LS112	
DM74LS113	Fairchild	74LS113	
	Hitachi	HD74LS113	
	Motorola	SN74LS113A	
	NEC America	μPB74LS113	
	Raytheon	74LS113	
	Signetics	74LS113	
	TI	SN74LS113	
DM74LS114	Fairchild	74LS114	
	Hitachi	HD74LS114	
	Motorola	SN74LS114A	
	Raytheon	74LS114	
	Signetics	74LS114	
	TI	SN74LS114A	
DM74LS12	Hitachi	HD74LS12	
	Motorola	SN74LS12	
	Raytheon	74LS12	
DM74LS12	Signetics	74LS12	
	TI	SN74LS12	
DM74LS122	Raytheon	74LS122	
	TI	SN74LS122	
DM74LS123	AMD	SN74LS123	
	Hitachi	HD74LS123	
	Raytheon	74LS123	
	TI	SN74LS123	
DM74LS125	Fairchild	74LS125	
	Raytheon	74LS125	
	Signetics	74LS125	
	TI	SN74LS125A	
DM74LS126	Fairchild	74LS126	
	Motorola	SN74LS126	
	Raytheon	74LS126	
	Signetics	74LS126	
	TI	SN74LS126A	
DM74LS13	Fairchild	74LS13	
	Hitachi	HD74LS13	
	Motorola	SN74LS13	
	Raytheon	74LS13	
	Signetics	74LS13	
	TI	SN74LS13	
DM74LS132	Fairchild	74LS132	
	Hitachi	HD74LS132	
	Motorola	SN74LS132	
	Raytheon	74LS132	
	Signetics	74LS132	
	TI	SN74LS132	
DM74LS136	Fairchild	74LS136	
	Hitachi	HD74LS136	
	Motorola	SN74LS136	
	Raytheon	74LS136	
	Signetics	74LS136	
	TI	SN74LS136	
DM74LS138	AMD	SN74LS138	
	Fairchild	74LS138	
	Hitachi	HD74LS138	
	Motorola	SN74LS138	
	NEC America	μPB74LS138	
	Raytheon	74LS138	
	Signetics	74LS138	
	TI	SN74LS138	
DM74LS139	AMD	SN74LS139	
	Fairchild	74LS139	
	Hitachi	HD74LS139	
	Motorola	SN74LS139	
	NEC America	μPB74LS139	
	Raytheon	74LS139	
	Signetics	74LS139	
	TI	SN74LS139	
DM74LS14	Fairchild	74LS14	
	Hitachi	HD74LS14	
	Motorola	SN74LS14	
	Raytheon	74LS14	
	Signetics	74LS14	
	TI	SN74LS14	
DM74LS15	Fairchild	74LS15	
	Hitachi	HD74LS15	
	Motorola	SN74LS15	
	Raytheon	74LS15	
	Signetics	74LS15	
	TI	SN74LS15	
DM74LS151	AMD	SN74LS151	
	Fairchild	74LS151	
	Hitachi	HD74LS151A	
	Motorola	SN74LS151	
	NEC America	μPB74LS151	
	Raytheon	74LS151	
	Signetics	74LS151	
	TI	SN74LS151	
DM74LS153	AMD	SN74LS153	
	Fairchild	74LS153	
	Hitachi	HD74LS153	
	Motorola	SN74LS153	
	NEC America	μPB74LS153	
	Raytheon	74LS153	
	Signetics	74LS153	
	TI	SN74LS153	
DM74LS154	Signetics	74LS154	
DM74LS155	Fairchild	74LS155	
	Hitachi	HD74LS155	
	Motorola	SN74LS155	
	NEC America	μPB74LS155	
	Raytheon	74LS155	
	Signetics	74LS155	
DM74LS155	TI	SN74LS155	
DM74LS156	Fairchild	74LS156	
	Hitachi	HD74LS156	
	Motorola	SN74LS156	
	Raytheon	74LS156	
	Signetics	74LS156	
	TI	SN74LS156	
DM74LS157	AMD	SN74LS157	
	Fairchild	74LS157	
	Motorola	SN74LS157	
	NEC America	μPB74LS157	
	Raytheon	74LS157	
	Signetics	74LS157	
	TI	SN74LS157	
DM74LS158	AMD	SN74LS158	
	Fairchild	74LS158	
	Hitachi	HD74LS158	
	Motorola	SN74LS158	
	Raytheon	74LS158	
	Signetics	74LS158	
	TI	SN74LS158	
DM74LS160	AMD	SN74LS160	
	Fairchild	74LS160	
	Hitachi	HD74LS160A	
	Motorola	SN74LS160A	
	Raytheon	74LS160	
	Signetics	74LS160A	
	TI	SN74LS160A	
DM74LS161	AMD	SN74LS161	
	Fairchild	74LS161	
	Hitachi	HD74LS161A	
	Motorola	SN74LS161A	
	NEC America	μPB74LS161	
	Raytheon	74LS161	
	Signetics	74LS161A	
	TI	SN74LS161A	
DM74LS162	AMD	SN74LS162	
	Fairchild	74LS162	
	Hitachi	HD74LS162A	
	Motorola	SN74LS162A	
	Raytheon	74LS162	
	Signetics	74LS162A	
	TI	SN74LS162A	
DM74LS163	AMD	SN74LS163	
	Fairchild	74LS163	
	Hitachi	HD74LS163A	
	Motorola	SN74LS163A	
	Raytheon	74LS163	
	Signetics	74LS163A	
	TI	SN74LS163A	
DM74LS164	AMD	SN74LS164	
	Fairchild	74LS164	
	Hitachi	HD74LS164	
	Motorola	SN74LS164A	
	NEC America	μPB74LS164	
	Raytheon	74LS164	
	Signetics	74LS164	
	TI	SN74LS164A	
DM74LS168	AMD	SN74LS168	
	Fairchild	74LS168	
	TI	SN74LS168	
DM74LS169	AMD	SN74LS169	
	Fairchild	74LS169	
	TI	SN74LS169	
DM74LS170	AMD	SN74LS170	
	Fairchild	74LS170	
	Motorola	SN74LS170	
	Raytheon	74LS170	
	Signetics	74LS170	
	TI	SN74LS170	
DM74LS173	Fairchild	74LS173	
	Signetics	74LS173	
	TI	SN74LS173	
DM74LS174	AMD	SN74LS174	
	Fairchild	74LS174	
	Hitachi	HD74LS174	
	Motorola	SN74LS174	
	Raytheon	74LS174	
	Signetics	74LS174	
	TI	SN74LS174	
DM74LS175	AMD	SN74LS175	
	Fairchild	74LS175	
	Hitachi	HD74LS175	
	Motorola	SN74LS175	
	NEC America	μPB74LS175	
	Raytheon	74LS175	

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Bold face device numbers indicate manufacturers data is provided in the IC Master on the pages noted.

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Manufacturer Device	Replacement Source	Device	IC Master Page
DM74LS175	Signetics	74LS175	
	TI	SN74LS175	
DM74LS189	MMI	AM27S03A	
DM74LS190	AMD	SN74LS190	
	Fairchild	74LS190	
	Motorola	SN74LS190	
	Raytheon	74LS190	
	Signetics	74LS190	
	TI	SN74LS190	
DM74LS191	AMD	SN74LS191	
	Fairchild	74LS191	
	Motorola	SN74LS191	
	Raytheon	74LS191	
	Signetics	74LS191	
	TI	SN74LS191	
DM74LS192	AMD	SN74LS192	
	Fairchild	74LS192	
	Motorola	SN74LS192	
	NEC America	μPB74LS192	
	Raytheon	74LS192	
	Signetics	74LS192	
	TI	SN74LS192	
DM74LS193	AMD	SN74LS193	
	Fairchild	74LS193	
	Motorola	SN74LS193	
	NEC America	μPB74LS193	
	Raytheon	74LS193	
	Signetics	74LS193	
	TI	SN74LS193	
DM74LS196	Fairchild	74LS196	
	Motorola	SN74LS196	
	Raytheon	74LS196	
	Signetics	74LS196	
	TI	SN74LS196	
DM74LS197	Fairchild	74LS197	
	Motorola	SN74LS197	
	Raytheon	74LS197	
	Signetics	74LS197	
	TI	SN74LS197	
DM74LS20	Fairchild	74LS20	
	Hitachi	HD74LS20	
	Motorola	SN74LS20	
	NEC America	μPB74LS20	
	Raytheon	74LS20	
	Signetics	74LS20	
	TI	SN74LS20	
DM74LS21	Hitachi	HD74LS21	
	Motorola	SN74LS21	
	NEC America	μPB74LS21	
	Raytheon	74LS21	
	Signetics	74LS21	
	TI	SN74LS21	
DM74LS22	Fairchild	74LS22	
	Hitachi	HD74LS22	
	Motorola	SN74LS22	
	Raytheon	74LS22	
	Signetics	74LS22	
	TI	SN74LS22	
DM74LS221	Fairchild	74LS221	
	Motorola	SN74LS221	
	Raytheon	74LS221	
	Signetics	74LS221	
	TI	SN74LS221	
DM74LS247	Fairchild	74LS247	
	Hitachi	HD74LS247	
	Motorola	SN74LS247	
	TI	SN74LS247	
DM74LS248	Fairchild	74LS248	
	Hitachi	HD74LS248	
	Motorola	SN74LS248	
	TI	SN74LS248	
DM74LS249	Fairchild	74LS249	
	Hitachi	HD74LS249	
	Motorola	SN74LS249	
	TI	SN74LS249	
DM74LS251	AMD	SN74LS251	
	Fairchild	74LS251	
	Motorola	SN74LS251	
	NEC America	μPB74LS251	
	Raytheon	74LS251	
	Signetics	74LS251	
	TI	SN74LS251	
DM74LS253	AMD	SN74LS253	
	Fairchild	74LS253	
	Hitachi	HD74LS253	
	Motorola	SN74LS253	
	NEC America	μPB74LS253	
	Raytheon	74LS253	
	Signetics	74LS253	
	TI	SN74LS253	
DM74LS257	AMD	SN74LS257	
	Fairchild	74LS257	
	Hitachi	HD74LS257	
	Motorola	SN74LS257A	
	NEC America	μPB74LS257	
	Raytheon	74LS257	
	Signetics	74LS257	
	TI	SN74LS257A	
DM74LS258	AMD	SN74LS258	
	Fairchild	74LS258	
	Motorola	SN74LS258A	
	NEC America	μPB74LS258	
	Raytheon	74LS258	
	Signetics	74LS258	
	TI	SN74LS258A	
DM74LS26	Fairchild	74LS26	
	Hitachi	HD74LS26	
	Motorola	SN74LS26	
	Raytheon	74LS26	
	Signetics	74LS26	
	TI	SN74LS26	
DM74LS27	Fairchild	74LS27	
	Hitachi	HD74LS27	
	Motorola	SN74LS27	
	NEC America	μPB74LS27	
	Raytheon	74LS27	
	Signetics	74LS27	
	TI	SN74LS27	
DM74LS279	Fairchild	74LS279	
	Motorola	SN74LS279	
	NEC America	μPB74LS279	
	Raytheon	74LS279	
	Signetics	74LS279	
	TI	SN74LS279	
DM74LS283	Fairchild	74LS283	
	Hitachi	SN74LS283	
	Motorola	SN74LS283	
	Raytheon	74LS283	
	Signetics	74LS283	
	TI	SN74LS283	
DM74LS289	MMI	AM27S02A	
DM74LS290	Fairchild	74LS290	
	Motorola	SN74LS290	
	Signetics	74LS290	
	TI	SN74LS290	
DM74LS293	Fairchild	74LS293	
	Motorola	SN74LS293	
	Signetics	74LS293	
	TI	SN74LS293	
DM74LS30	Fairchild	74LS30	
	Hitachi	HD74LS30	
	Motorola	SN74LS30	
	NEC America	μPB74LS30	
	Raytheon	74LS30	
	Signetics	74LS30	
	TI	SN74LS30	
DM74LS32	Fairchild	74LS32	
	Hitachi	HD74LS32	
	Motorola	SN74LS32	
	NEC America	μPB74LS32	
	Raytheon	74LS32	
	Signetics	74LS32	
	TI	SN74LS32	
DM74LS352	Fairchild	74LS352	
	Motorola	SN74LS352	
	TI	SN74LS352	
DM74LS353	Fairchild	74LS353	
	Motorola	DM74LS353	
	TI	SN74LS353	
DM74LS365	Fairchild	74LS365	
	Motorola	SN74LS365A	
	NEC America	μPB74LS365	
	Raytheon	74LS365	
	Signetics	74LS365A	
	TI	SN74LS365A	
DM74LS366	Fairchild	74LS366	
	Motorola	SN74LS366A	
	NEC America	μPB74LS366	
DM74LS366	Raytheon	74LS366	
	Signetics	74LS366A	
	TI	SN74LS366A	
DM74LS367	Fairchild	74LS367	
	Hitachi	HD74LS367	
	Motorola	SN74LS367A	
	NEC America	μPB74LS367	
	Raytheon	74LS367	
	Signetics	74LS367A	
	TI	SN74LS367A	
DM74LS368	Fairchild	74LS368	
	Hitachi	HD74LS368	
	Motorola	SN74LS368A	
	NEC America	μPB74LS368	
	Raytheon	74LS368	
	Signetics	74LS368A	
	TI	SN74LS368A	
DM74LS37	Fairchild	74LS37	
	Hitachi	HD74LS37	
	Motorola	SN74LS37	
	NEC America	μPB74LS37	
	Raytheon	74LS37	
	Signetics	74LS37	
	TI	SN74LS37	
DM74LS38	Fairchild	74LS38	
	Hitachi	HD74LS38	
	Motorola	SN74LS38	
	NEC America	μPB74LS38	
	Raytheon	74LS38	
	Signetics	74LS38	
	TI	SN74LS38	
DM74LS386	Fairchild	74LS386	
	Hitachi	HD74LS386	
	Motorola	SN74LS386	
	Raytheon	74LS386	
	Signetics	74LS386	
	TI	SN74LS386	
DM74LS395	Fairchild	74LS395	
	Raytheon	74LS395	
	Signetics	74LS395	
	TI	SN74LS395	
DM74LS40	Fairchild	74LS40	
	Hitachi	HD74LS40	
	Motorola	SN74LS40	
	NEC America	μPB74LS40	
	Raytheon	74LS40	
	Signetics	74LS40	
	TI	SN74LS40	
DM74LS42	Fairchild	74LS42	
	Hitachi	HD74LS42	
	Motorola	SN74LS42	
	NEC America	μPB74LS42	
	Raytheon	74LS42	
	Signetics	74LS42	
	TI	SN74LS42	
DM74LS47	Hitachi	HD74LS47	
	Motorola	SN54LS47	
		SN74LS47	
DM74LS48	Hitachi	HD74LS48	
	Motorola	SN74LS48	
DM74LS49	Hitachi	HD74LS49	
	Motorola	SN74LS49	
DM74LS51	Fairchild	74LS51	
	Hitachi	HD74LS51	
	Motorola	SN74LS51	
	NEC America	μPB74LS51	
	Raytheon	74LS51	
	Signetics	74LS51	
	TI	SN74LS51	
DM74LS54	Fairchild	74LS54	
	Hitachi	HD74LS54	
	Motorola	SN74LS54	
	NEC America	μPB74LS54	
	Raytheon	74LS54	
	Signetics	74LS54	
	TI	SN74LS54	
DM74LS55	Fairchild	74LS55	
	Hitachi	HD74LS55	
	Motorola	SN74LS55	
	NEC America	μPB74LS55	
	Raytheon	74LS55	
	Signetics	74LS55	
	TI	SN74LS55	
DM74LS670	AMD	SN74LS670	
	Fairchild	74LS670	
	Motorola	SN74LS670	
DM74LS670	Raytheon	74LS670	
	Signetics	74LS670	
	TI	SN74LS670	
DM74LS73	Fairchild	74LS73	
	Hitachi	HD74LS73	
	Motorola	SN74LS73	
	Raytheon	74LS73	
	Signetics	74LS73	
	TI	SN74LS73	
DM74LS74	Fairchild	74LS74	
	Hitachi	HD74LS74A	
	Motorola	SN74LS74	
	NEC America	μPB74LS74	
	Raytheon	74LS74	
	Signetics	74LS74	
	TI	SN74LS74	
DM74LS75	Fairchild	74LS75	
	Motorola	SN74LS75	
	Raytheon	74LS75	
	Signetics	74LS75	
	TI	SN74LS75	
DM74LS76	Hitachi	HD74LS76	
	Motorola	SN74LS76A	
	Raytheon	74LS76	
	Signetics	74LS76	
	TI	SN74LS76	
DM74LS77	Fairchild	74LS77	
	Raytheon	54LS77	
DM74LS78	Fairchild	74LS78	
	Hitachi	HD74LS78	
	Motorola	SN74LS78A	
	Raytheon	74LS78	
	Signetics	74LS78	
	TI	SN74LS78	
DM74LS83A	Fairchild	74LS83	
	Hitachi	HD74LS83A	
	Motorola	SN74LS83	
	Raytheon	74LS83A	
	Signetics	74LS83	
	TI	SN74LS83A	
DM74LS85	Fairchild	74LS85	
	Motorola	SN74LS85	
	Raytheon	74LS85	
	Signetics	74LS85	
	TI	SN74LS85	
DM74LS86	Hitachi	HD74LS86	
DM74LS92	Hitachi	HD74LS92	
DM74LS93	Fairchild	74LS93	
	Motorola	SN74LS93	
	Raytheon	74LS93	
	Signetics	74LS93	
	TI	SN74LS93	
DM74L187	Intersil	IM5603	
DM74L63	TI	SN54L193	
DM74L89	MMI	L6560	
DM74S00	Fairchild	74S00	
	Hitachi	HD74S00	
	Mitsubishi	M5S000	
	Signetics	74S00	
	TI	SN74S00	
DM74S02	Fairchild	74S02	
	Signetics	74S02	
	TI	SN74S32	
DM74S03	Fairchild	74S03	
	Hitachi	HD74S03	
	Mitsubishi	M5S003	
	Signetics	74S03	
	TI	SN74S03	
DM74S04	Fairchild	74S04	
	Hitachi	HD74S04	
	Mitsubishi	M5S004	
	Signetics	74S04	
	TI	SN74S04	
DM74S05	Falrchild	74S05	
	Hitachi	HD74S05	
	Mitsubishi	M5S005	
	Signetics	74S05	
	TI	SN74S05	
DM74S10	Fairchild	74S10	
	Hitachi	HD74S10	
	Mitsubishi	M5S010	
	Signetics	74S10	
	TI	SN74S10	
DM74S11	Fairchild	74S11	
	Hitachi	HD74S11	
	Mitsubishi	M5S011	

♦ Discontinued

The manufacturers report their devices can be used as direct replacements.
Performance details often differ, so compare the specifications considering your requirements.

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Manufacturer Device	Replacement Source	Device	IC Master Page
DM74S11	Signetics	74S11	
	TI	SN74S11	
DM74S112	Fairchild	74S112	
	Hitachi	HD74S112	
	Mitsubishi	M5S112	
	Motorola	SN74S112	
	Signetics	74S112	
	TI	SN74S112	
DM74S113	Fairchild	74S113	
	Hitachi	HD74S113	
	Mitsubishi	M5S113	
	Motorola	SN74S113	
	Signetics	74S113	
	TI	SN74S113	
DM74S114	Fairchild	74S114	
	Hitachi	HD74S114	
	Mitsubishi	M5S114	
	Signetics	74S114	
	TI	SN74S114	
DM74S133	Fairchild	74S133	
	Hitachi	HD74S133	
	Mitsubishi	M5S133	
	Signetics	74S133	
	TI	SN74S133	
DM74S134	Fairchild	74S134	
	Hitachi	HD74S134	
	Signetics	74S134	
	TI	SN74S134	
DM74S135	Fairchild	74S135	
	Hitachi	HD74S135	
	Signetics	74S135	
	TI	SN74S135	
DM74S138	AMD	SN74S138	
	Fairchild	74S138	
	Mitsubishi	M5S138	
	Signetics	74S138	
	TI	SN74S138	
DM74S139	AMD	SN74S139	
	Fairchild	74S139	
	Signetics	74S139	
	TI	SN74S139	
DM74S140	Fairchild	74S140	
	Hitachi	HD74S140	
	Signetics	74S140	
	TI	SN74S140	
DM74S15	Fairchild	74S15	
	Hitachi	HD74S15	
	Mitsubishi	M5S015	
	Signetics	74S15	
	TI	SN74S15	
DM74S151	AMD	SN74S151	
	Fairchild	74S151	
	Hitachi	HD74S151	
	Mitsubishi	M5S151	
	Signetics	74S151	
	TI	SN74S151	
DM74S153	AMD	SN74S153	
	Fairchild	74S153	
	Mitsubishi	M5S153	
	Signetics	74S153	
	TI	SN74S153	
DM74S157	AMD	SN74S157	
	Fairchild	74S157	
	Mitsubishi	M5S157	
	Signetics	74S157	
	TI	SN74S157	
DM74S158	AMD	SN74S158	
	Fairchild	74S158	
	Mitsubishi	M5S158	
	Signetics	74S158	
	TI	SN74S158	
DM74S174	AMD	SN74S174	
	Fairchild	74S174	
	Hitachi	HD74S174	
	Mitsubishi	M5S174	
	Signetics	74S174	
	TI	SN74S174	
DM74S175	AMD	SN74S175	
	Fairchild	74S175	
	Hitachi	HD74S175	
	Mitsubishi	M5S175	
	Signetics	74S175	
DM74S175	TI	SN74S175	
DM74S182	Fairchild	93S42	
	Hitachi	HD74S182	
	Mitsubishi	M5S182	
	Signetics	74S182	
	TI	SN74S182	
DM74S188	AMD	AM27S18	
	MMI	**63S080**	**1453**
DM74S195	AMD	SN74S195	
	Fairchild	93S00	
	Signetics	74S195	
	TI	SN74S195	
DM74S20	Fairchild	74S20	
	Hitachi	HD74S20	
	Mitsubishi	M5S020	
	Signetics	74S20	
	TI	SN74S20	
DM74S200	**Fairchild**	**93421**	**1252**
	Signetics	**74S200**	**1678**
DM74S206	Fairchild	93411	
DM74S22	Fairchild	74S22	
	Hitachi	HD74S22	
	Mitsubishi	M5S22	
	Signetics	74S22	
	TI	SN74S22	
DM74S251	AMD	SN74S251	
	Fairchild	74S251	
	Hitachi	HD74S251	
	Mitsubishi	M5S251	
	Signetics	74S251	
	TI	SN74S251	
DM74S253	AMD	SN74S253	
	Fairchild	74S253	
	Signetics	74S253	
DM74S257	AMD	SN74S257	
	Fairchild	74S257	
	Mitsubishi	M5S257	
	Signetics	74S257	
	TI	SN74S257	
DM74S280	Fairchild	74S280	
	Signetics	74S280	
	TI	SN74S280	
DM74S281	TI	SN74S281	
DM74S287	AMD	AM27S21	
	Fairchild	**93427**	**1258**
	MMI	**63S141**	**1453**
	Raytheon	**29661**	**1664**
DM74S288	AMD	AM27S19	
	MMI	**63S081**	**1453**
DM74S30	Fairchild	74S30	
	Mitsubishi	M5S030	
	TI	SN74S30	
DM74S387	AMD	AM27S20	
	Fairchild	**93417**	**1258**
	Intel	3601-1	
	MMI	**63S140**	**1453**
		6300-1	**1449**
	NEC Micro	μPB403	
	Raytheon	**29660**	**1664**
	Signetics	**N82S126**	**1680**
	TI	**SN74S387**	**1708**
DM74S40	Fairchild	74S40	
	Hitachi	HD74S40	
	Mitsubishi	M5S040	
	Signetics	74S40	
	TI	SN74S40	
DM74S470	**MMI**	**6308-1**	**1449**
	Raytheon	**29600**	**1652**
DM74S471	**MMI**	**6309-1**	**1449**
	Raytheon	**29601**	**1652**
DM74S472	**MMI**	**6349-1**	**1449**
	Raytheon	**29621**	**1656**
DM74S473	**MMI**	**6348-1**	**1449**
	Raytheon	**29620**	**1656**
DM74S51	Fairchild	74S51	
	Mitsubishi	M5S051	
	Signetics	74S51	
	TI	SN74S51	
DM74S570	AMD	AM27S12	
	Fairchild	**93436**	**1260**
	MMI	**6305-1**	**1449**
	Raytheon	**29610**	**1654**
DM74S571	AMD	AM27S13	
	Fairchild	**93446**	**1260**
	MMI	**6306-1**	**1449**
	Raytheon	**29611**	**1654**
DM74S572	**Fairchild**	**93452**	**1264**
	Intel	3605A	
	MMI	**6352-1**	**1449**
	NEC Micro	**μPB406**	**1625**
	Raytheon	29640	
DM74S573	**Fairchild**	**93453**	**1264**
	Intel	3625A	
	MMI	**6353-1**	**1449**
	NEC Micro	**μPB426**	**1625**
DM74S64	Fairchild	74S64	
	Hitachi	HD74S64	
	Signetics	74S64	
	TI	SN74S64	
DM74S65	Fairchild	74S65	
	Hitachi	HD74S65	
	Signetics	74S65	
	TI	SN74S65	
DM74S86	Fairchild	74S86	
	Hitachi	HD74S86	
	Signetics	74S86	
	TI	SN74S86	
DM7400	Fairchild	7400	
	Hitachi	HD7400	
	Mitsubishi	M53200	
	Motorola	MC7400	
	NEC America	μPB7400	
	Signetics	7400	
	TI	SN7400	
	Toshiba	TC7400	
		TD3400	
	TRW	7400	
DM7401	Fairchild	7401	
	Hitachi	HD7401	
	Mitsubishi	M53201	
	Motorola	MC7401	
	Signetics	7401	
	TI	SN7401	
	Toshiba	TD3401	
	TRW	7401	
DM7402	Fairchild	7402	
	Hitachi	HD7402	
	Mitsubishi	M53202	
	Motorola	MC7402	
	NEC America	μPB7402	
	Signetics	7402	
	TI	SN7402	
	Toshiba	TD3402	
	TRW	7402	
DM7403	Fairchild	7403	
	Hitachi	HD7403	
	Mitsubishi	M53203	
	Motorola	MC7403	
	Signetics	7403	
	TI	SN7403	
	Toshiba	TD3403	
	TRW	7403	
DM7404	Fairchild	7404	
	Hitachi	HD7404	
	Mitsubishi	M53204	
	Motorola	MC7404	
	NEC America	μPB7404	
	Signetics	7404	
	TI	SN7404	
	Toshiba	TC7404	
		TD3404	
	TRW	7404	
DM7405	Fairchild	7405	
	Hitachi	HD7405	
	Mitsubishi	M53205	
	Motorola	MC7405	
	NEC America	μPB7405	
	Signetics	7405	
	TI	SN7405	
	Toshiba	TD3405	
	TRW	7405	
DM7406	Fairchild	7406	
	Hitachi	HD7406	
	Mitsubishi	M53206	
	Motorola	MC7406	
	Signetics	7406	
	TI	SN7406	
	Toshiba	TD3406	
	TRW	7406	
DM7407	Fairchild	7407	
	Hitachi	HD7407	
	Mitsubishi	M53207	
DM7407	Motorola	MC7407	
	Signetics	7407	
	TI	SN7407	
	Toshiba	TD3407	
	TRW	7407	
DM7408	Fairchild	7408	
	Hitachi	HD7408	
	Mitsubishi	M53208	
	Motorola	MC7408	
	Signetics	7408	
	TI	SN7408	
	Toshiba	TC7408	
		TD3408	
	TRW	7408	
DM7409	Fairchild	7409	
	Hitachi	HD7409	
	Mitsubishi	M53209	
	Motorola	MC7409	
	Signetics	7409	
	TI	SN7409	
	Toshiba	TD3409	
	TRW	7409	
DM7410	Fairchild	7410	
	Hitachi	HD7410	
	Mitsubishi	M53210	
	Motorola	MC7410	
	NEC America	μPB7410	
	Raytheon	7410	
	Signetics	7410	
	TI	SN7410	
		SN7427	
	Toshiba	TC7410	
		TD3410	
	TRW	7410	
DM74107	Fairchild	74107	
	Hitachi	HD74107	
	Mitsubishi	M53307	
	Motorola	MC74107	
	NEC America	μPB74107	
	Signetics	74107	
	TI	SN74107	
	Toshiba	TD34107	
DM74109	Fairchild	9024	
	Signetics	74109	
	TI	SN74109	
DM7411	Fairchild	7411	
	Hitachi	HD7411	
	Signetics	7411	
♦DM7412	Raytheon	7412	
DM74121	Fairchild	74121	
	Hitachi	HD74121	
	Mitsubishi	M53321	
	Motorola	MC74121	
	Signetics	74121	
	TI	SN74121	
	Toshiba	TD34121	
	TRW	74121	
DM74123	AMD	SN74123	
	Fairchild	74123	
	Mitsubishi	M53323	
	Motorola	MC74123	
	NEC America	μPB74123	
	Signetics	74123	
	TI	SN74123	
	TRW	74123	
DM74125	Fairchild	74125	
	Hitachi	HD74125	
	Mitsubishi	M53325	
	Signetics	74125	
	TI	SN74125	
		SN74425	
DM74126	Fairchild	74126	
	Hitachi	HD74126	
	Mitsubishi	M53326	
	Signetics	74126	
	TI	SN74126	
		SN74426	
DM7413	Fairchild	7413	
	Mitsubishi	M53213	
	Motorola	MC7413	
	NEC America	μPB7413	
	Signetics	7413	
	TI	SN7413	
	TRW	7413	
DM74132	Fairchild	74132	
	Hitachi	HD74132	

♦ Discontinued

Bold face device numbers indicate manufacturers data is provided in the IC Master on the pages noted.

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Manufacturer Device	Replacement Source	Device	IC Master Page
DM74132	Mitsubishi	M53332	
	Motorola	MC74132	
	Signetics	74132	
	TI	SN74132	
♦DM74136	Raytheon	74136	
DM7414	Fairchild	7414	
	Hitachi	HD7414	
	Mitsubishi	M53214	
	Motorola	MC7414	
	Signetics	7414	
	TI	SN7414	
DM74141	Fairchild	74141	
	Motorola	MC74141	
	NEC America	μPB74141	
	Signetics	74141	
	TI	SN74141	
DM74145	Fairchild	74145	
	Mitsubishi	M53345	
	Motorola	MC74145	
	Signetics	74145	
	TI	SN74145	
	TRW	74145	
DM74147	Hitachi	HD74147	
	Mitsubishi	M53347	
	NEC America	μPB74147	
	Signetics	74147	
	TI	SN74147	
DM74148	Fairchild	9318	
	Hitachi	HD74148	
	Mitsubishi	M53348	
	NEC America	μPB74148	
	Signetics	74148	
	TI	SN74148	
♦DM7415	Raytheon	7415	
DM74150	Fairchild	74150	
	Hitachi	HD74150	
	Mitsubishi	M53350	
	Motorola	MC74150	
	NEC America	μPB74150	
	Signetics	74150	
	TI	SN74150	
	TRW	74150	
DM74151	Fairchild	74151	
	Hitachi	HD74151	
	Mitsubishi	M53351	
	Motorola	MC74151	
	NEC America	μPB74151	
	Raytheon	74151	
	Signetics	74151	
	TI	SN74151	
		SN74151A	
	TRW	74151	
DM74153	AMD	SN74153	
	Fairchild	74153	
	Hitachi	HD74153	
	Mitsubishi	M53353	
	Motorola	MC74153	
	NEC America	μPB74153	
	Signetics	74153	
	TI	SN74153	
	TRW	74153	
DM74154	AMD	SN74154	
	Fairchild	74154	
	Hitachi	HD74154	
	Mitsubishi	M53354	
	Motorola	MC74154	
	NEC America	μPB74154	
	Raytheon	74154	
	Signetics	74154	
	TI	SN74154	
	TRW	74154	
DM74155	Fairchild	74155	
	Mitsubishi	M53355	
	Motorola	MC74155	
	NEC America	μPB74155	
	Signetics	74155	
	TI	SN74155	
	TRW	74155	
DM74156	Fairchild	74156	
	Hitachi	HD74156	
	Mitsubishi	M53356	
	Motorola	MC74156	
DM74156	NEC America	μPB74156	
	Signetics	74156	
	TI	SN74156	
	TRW	74156	
DM74157	AMD	SN74157	
	Fairchild	74157	
	Hitachi	HD74157	
	Mitsubishi	M53357	
	Motorola	MC74157	
	NEC America	μPB74157	
	Signetics	74157	
	TI	SN74157	
DM7416	Fairchild	7416	
	Hitachi	HD7416	
	Mitsubishi	M53216	
	Motorola	MC7416	
	Signetics	7416	
	TI	SN7416	
	Toshiba	TD3416	
	TRW	7416	
DM74160	AMD	SN74160	
	Fairchild	74160	
	Hitachi	HD74160	
	Mitsubishi	M53360	
	Motorola	MC74160	
	Signetics	74160	
	TI	SN74160	
	TRW	74160	
DM74161	AMD	SN74161	
	Fairchild	74161	
	Hitachi	HD74161	
	Mitsubishi	M53361	
	Motorola	MC74161	
	NEC America	μPB74161	
	Raytheon	74161	
	Signetics	74161	
	TI	SN74161	
	TRW	74161	
DM74162	AMD	SN74162	
	Fairchild	74162	
	Hitachi	HD74162	
	Mitsubishi	M53362	
	Motorola	MC74162	
	Signetics	74162	
	TI	SN74162	
	TRW	74162	
DM74163	AMD	SN74163	
	Fairchild	74163	
	Hitachi	HD74163	
	Mitsubishi	M53363	
	Motorola	MC74163	
	Signetics	74163	
	TI	SN74163	
	TRW	74163	
DM74164	AMD	SN74164	
		74164	
	Fairchild	74164	
	Hitachi	HD74164	
	Mitsubishi	M53364	
	NEC America	μPB74164	
	Signetics	74164	
	TI	SN74164	
DM74165	Fairchild	74165	
	Mitsubishi	M53365	
	Motorola	MC74165	
	Signetics	74165	
	TI	SN74165	
DM74166	Fairchild	74166	
	Hitachi	HD74166	
	Mitsubishi	M53366	
	Signetics	74166	
	TI	SN74166	
DM7417	Fairchild	7417	
	Hitachi	HD7417	
	Mitsubishi	M53217	
	Motorola	MC7417	
	Signetics	7417	
	TI	SN7417	
	Toshiba	TD3417	
	TRW	7417	
DM74170	Fairchild	74170	
	Hitachi	HD74170	
	Mitsubishi	M53370	
	NEC America	μPB74170	
	Signetics	74170	
	TI	SN74170	
DM74172	Signetics	74S172	
		74172	
	TI	SN74172	
DM74173	Fairchild	74173	
	TI	SN74173	
DM74174	AMD	SN74174	
	Fairchild	74174	
	Hitachi	HD74174	
	Mitsubishi	M53374	
	Motorola	MC74174	
	Raytheon	74174	
	Signetics	74174	
	TI	SN74174	
DM74175	AMD	SN74175	
	Fairchild	74175	
	Hitachi	HD74175	
	Mitsubishi	M53375	
	Motorola	MC74175	
	NEC America	μPB74175	
	Signetics	74175	
	TI	SN74175	
DM74176	Fairchild	74176	
	Mitsubishi	M53376	
	Motorola	MC74176	
	Signetics	74176	
	TI	SN74176	
DM74177	Fairchild	74177	
	Mitsubishi	M53377	
	Motorola	MC74177	
	Signetics	74177	
	TI	SN74177	
DM74180	Fairchild	74180	
	Hitachi	HD74180	
	Mitsubishi	M53380	
	Motorola	MC74180	
	NEC America	μPB74180	
	Signetics	74180	
	TI	SN74180	
	TRW	74180	
DM74181	AMD	SN74181	
	Fairchild	74181	
	Mitsubishi	M53381	
	Motorola	MC74181	
	NEC America	μPB74181	
	Raytheon	74181	
	Signetics	74181	
	TI	SN74181	
DM74182	AMD	SN74182	
	Fairchild	74182	
		9342	
	Mitsubishi	M53382	
	Motorola	MC74182	
	NEC America	μPB74182	
	Raytheon	74182	
	Signetics	74182	
	TI	SN74182	
DM74184	TI	SN74184	
DM74185	Mitsubishi	M53385	
	TI	SN74185	
♦DM74187	Intersil	IM5603	
	MMI	**6200-1**	**1466**
	National	DM74S187	
	Signetics	N82S226	
	TI	SN74187	
DM74190	Fairchild	74190	
	Hitachi	HD74190	
	Mitsubishi	M53390	
	Motorola	MC74190	
	Signetics	74190	
	TI	SN74190	
DM74191	Fairchild	74191	
	Hitachi	HD74191	
	Mitsubishi	M53391	
	Motorola	MC74191	
	Signetics	74191	
	TI	SN74191	
DM74192	AMD	SN74192	
	Fairchild	74192	
	Mitsubishi	M53392	
	Motorola	MC74192	
	NEC America	μPB74192	
	Signetics	74192	
	TI	SN74192	
	Toshiba	TD34192	
DM74193	AMD	SN74193	
	Fairchild	74193	
DM74193	Mitsubishi	M53393	
	Motorola	MC74193	
	NEC America	μPB74193	
	Signetics	74193	
	TI	SN74193	
	Toshiba	TD34193	
DM74194	AMD	SN74194	
	Fairchild	74194	
	Hitachi	HD74194	
	Motorola	MC74194	
	Signetics	74194	
	TI	SN74194	
DM74195	AMD	SN74195	
	Fairchild	74195	
	Motorola	MC74195	
	NEC America	μPB74195	
	Signetics	74195	
	TI	SN74195	
DM74196	Fairchild	74196	
	Motorola	MC74196	
	Signetics	74196	
	TI	SN74196	
DM74197	Fairchild	74197	
	Motorola	MC74197	
	Signetics	74197	
	TI	SN74197	
DM74198	Fairchild	74198	
	Hitachi	HD74198	
	Mitsubishi	M53398	
	NEC America	μPB74198	
	Signetics	74198	
	TI	SN74198	
DM74199	Fairchild	74199	
	Mitsubishi	M53399	
	Signetics	74199	
	TI	SN74199	
DM7420	Fairchild	7420	
	Hitachi	HD7420	
	Mitsubishi	M53220	
	Motorola	MC7420	
	NEC America	μPB7420	
	Signetics	7420	
	TI	SN7420	
	Toshiba	TC7420	
		TD3420	
	TRW	7420	
♦DM74200	**Fairchild**	**93421**	**1252**
	MMI	6531	
	TI	SN74S201	
DM7421	Toshiba	TD3421	
DM7423	Fairchild	7423	
	Motorola	MC7423	
	TI	SN7423	
DM7425	Fairchild	7425	
	Mitsubishi	M53225	
	Motorola	MC7425	
	TI	SN7425	
DM74251	TI	SN74251	
DM7426	Fairchild	7426	
	Hitachi	HD7426	
	Motorola	MC7426	
	Signetics	7426	
	TI	SN7426	
	Toshiba	TD3426	
	TRW	7426	
DM7427	Fairchild	7427	
	Hitachi	HD7427	
	Mitsubishi	M53227	
	Motorola	MC7427	
	Signetics	7427	
♦DM74283	Raytheon	74283	
DM7430	Fairchild	7430	
	Hitachi	HD7430	
	Mitsubishi	M53230	
	Motorola	MC7430	
	NEC America	μPB7430	
	Signetics	7430	
	TI	SN7430	
	Toshiba	TD3430	
	TRW	7430	
DM7432	Fairchild	7432	
	Hitachi	HD7432	
	Signetics	7432	
	TI	SN7432	
DM7437	Fairchild	7437	
	Mitsubishi	M53237	

♦ Discontinued

The manufacturers report their devices can be used as direct replacements.
Performance details often differ, so compare the specifications considering your requirements.

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Manufacturer Device	Replacement Source	Device	IC Master Page
DM7437	Motorola	MC7437	
	NEC America	μPB7437	
	Signetics	7437	
	TI	SN7437	
	Toshiba	TD3437	
	TRW	7437	
DM7438	Fairchild	7438	
	Mitsubishi	M53238	
	Motorola	MC7438	
	NEC America	μPB7438	
	Signetics	7438	
	TI	SN7438	
	Toshiba	TD3438	
	TRW	7438	
DM7440	Fairchild	7440	
	Hitachi	HD7440	
	Mitsubishi	M53240	
	Motorola	MC7440	
	NEC America	μPB7440	
	Signetics	7440	
	TI	SN7440	
	Toshiba	TD3440	
	TRW	7440	
DM7441	Fairchild	7441	
	Hitachi	HD7441	
	Mitsubishi	M53241	
	Signetics	7441	
	TI	SN74141	
	Toshiba	TD3441	
DM7442	Fairchild	7442	
	Hitachi	HD7442	
	Mitsubishi	M53242	
	Motorola	MC7442	
	NEC America	μPB7442	
	Signetics	7442	
	TI	SN7442	
		SN7442A	
	Toshiba	TD3442	
DM7445	Fairchild	7445	
	Mitsubishi	M53245	
	Motorola	MC7445	
	NEC America	μPB7445	
	Signetics	7445	
	TI	SN7445	
	TRW	7445	
DM7446	Fairchild	7446	
	Hitachi	HD7446	
	Motorola	MC7446	
	Signetics	7446	
	TI	SN7446	
		SN7446A	
DM7447	Fairchild	7447	
	Hitachi	HD7447	
	Mitsubishi	M53247	
	Motorola	MC7447	
	NEC America	μPB7447	
	Signetics	7447	
	TI	SN7447	
		SN7447A	
	Toshiba	TD3447	
DM7448	Fairchild	7448	
	Mitsubishi	M53248	
	Motorola	MC7448	
	Signetics	7448	
	TI	SN7448	
DM7450	Fairchild	7450	
	Hitachi	HD7450	
	Mitsubishi	M53250	
	Motorola	MC7450	
	NEC America	μPB7450	
	Signetics	7450	
	TI	SN7450	
	Toshiba	TD3450	
	TRW	7450	
DM7451	Fairchild	7451	
	Hitachi	HD7451	
	Motorola	MC7451	
	NEC America	μPB7451	
	Signetics	7451	
	TI	SN7451	
	Toshiba	TD3451	
	TRW	7451	
DM7453	Fairchild	7453	
	Hitachi	HD7453	
	Mitsubishi	M53253	
	Motorola	MC7453	
	NEC America	μPB7453	
	Signetics	7453	
	TI	SN7453	
	TRW	7453	
DM7454	Fairchild	7454	
	Hitachi	HD7454	
	Motorola	MC7454	
	NEC America	μPB7454	
	Signetics	7454	
	TI	SN7454	
	TRW	7454	
DM7460	Fairchild	7460	
	Hitachi	HD7460	
	Mitsubishi	M53260	
	Motorola	MC7460	
	NEC America	μPB7460	
	Signetics	7460	
	TI	SN7460	
	Toshiba	TD3460	
	TRW	7460	
DM7470	Fairchild	7470	
	Mitsubishi	M53270	
	Motorola	MC7470	
	Signetics	7470	
	TI	SN7470	
DM7472	Fairchild	7472	
	Hitachi	HD7472	
	Mitsubishi	M53272	
	Motorola	MC7472	
	Signetics	7472	
	TI	SN7472	
	Toshiba	TD3472	
	TRW	7472	
DM7473	Fairchild	7473	
	Hitachi	HD7473	
	Mitsubishi	M53273	
	Motorola	MC7473	
	NEC America	μPB7473	
	Signetics	7473	
	TI	SN7473	
	Toshiba	TD3473	
DM7474	Fairchild	7474	
	Hitachi	HD7474	
	Mitsubishi	M53274	
	Motorola	MC7474	
	NEC America	μPB7474	
	Signetics	7474	
	TI	SN7474	
	Toshiba	TD3474	
	TRW	7474	
DM7475	Fairchild	7475	
	Hitachi	HD7475	
	Mitsubishi	M53275	
	Motorola	MC7475	
	Signetics	7475	
	TI	SN7475	
	Toshiba	TD3475	
	TRW	7475	
DM7476	Fairchild	7476	
	Hitachi	HD7476	
	Mitsubishi	M53276	
	Motorola	MC7476	
	NEC America	μPB7476	
	Signetics	7476	
	TI	SN7476	
	Toshiba	TD3476	
	TRW	7476	
DM7483	Fairchild	7483	
	Hitachi	HD7483	
	Mitsubishi	M53283	
	Motorola	MC7483	
	Signetics	7483	
	TI	SN7483	
		SN7483A	
DM7485	Fairchild	7485	
	Hitachi	HD7485	
	Mitsubishi	M53285	
	Motorola	MC7485	
	NEC America	μPB7485	
	Signetics	7485	
	TI	SN7485	
	TRW	7485	
DM7486	Fairchild	7486	
	Hitachi	HD7486	
	Mitsubishi	M53286	
	Motorola	MC7486	
	NEC America	μPB7486	
	Signetics	7486	
	TI	SN7486	
	Toshiba	TD3486	
	TRW	7486	
DM7488	Intersil	IM5600	
	MMI	**6230-1**	**1466**
	TI	SN7488	
		SN7488A	
DM7489	AMD	C3101	
		SN7489	
	Fairchild	7489	
	Mitsubishi	M53289	
	MMI	6560	
	TI	SN7489	
	TRW	7489	
DM7490	Fairchild	7490	
	Hitachi	HD7490	
	Mitsubishi	M53290	
	Motorola	MC7490	
	Signetics	7490	
	TI	SN7490	
		SN7490A	
	Toshiba	TD3490	
	TRW	7490	
DM7491	Fairchild	7491	
	Mitsubishi	M53291	
	Motorola	MC7491	
	NEC America	μPB7491	
	Signetics	7491	
	TI	SN7491	
		SN7491A	
	Toshiba	TD3491	
DM7492	Fairchild	7492	
	Hitachi	HD7492	
	Mitsubishi	M53292	
	Motorola	MC7492	
	Signetics	7492	
	TI	SN7492	
		SN7492A	
	Toshiba	TD3492	
	TRW	7492	
DM7493	Fairchild	7493	
	Hitachi	HD7493	
	Mitsubishi	M53293	
	Motorola	MC7493	
	Signetics	7493	
	TI	SN7493	
		SN7493A	
	Toshiba	TD3492	
	TRW	7493	
DM7495	Fairchild	7495	
	Hitachi	HD7495	
	Mitsubishi	M53295	
	Motorola	MC7495	
	Signetics	7495	
	TI	SN7495	
		SN7495A	
	Toshiba	TD3495	
DM7496	Fairchild	7496	
	Hitachi	HD7496	
	Mitsubishi	M53296	
	Motorola	MC7496	
	Signetics	7496	
	TI	SN7496	
	TRW	7496	
DM75L60	TI	SN54L192	
DM75L63	TI	SN54L193	
DM75S228	**Raytheon**	**29631**	**1660**
DM75S229	**Raytheon**	**29630**	**1660**
DM7535	NEC Micro	μPB403	
DM75491	Motorola	MC75491	
	National	DS75491	
DM75492	Motorola	MC75492	
	National	DS75492	
DM7551	TI	SN54173	
DM7560	TI	SN54192	
DM7563	TI	SN54193	
DM7570	TI	SN54164	
◆DM7575	Harris	HPROM1024A	
	Intel	M3601	
	Intersil	IM5603	
◆DM7573	**MMI**	**5300-1**	**1449**
	TI	**SN54S387**	**1708**
◆DM7574	**Harris**	**HM7602**	**1284**
		HPROM1024	
	Intersil	IM5623	
	MMI	**5301-1**	**1449**
	National	DM54S287	
	NEC Micro	μPB403	
	TI	**SN54S287**	**1708**
DM7577	**Harris**	**HM7602**	**1284**
	TI	**SN54S188**	**1708**
DM7578	AMD	AM27S19	
	Harris	**HM7603**	**1284**
	TI	**SN54S288**	**1708**
◆DM7582	TI	SN54S301	
DM7588	**TI**	**SN54S188**	**1708**
DM7590	TI	SN54165	
DM7596	**TI**	**SN54S473**	**1708**
◆DM7597	Intersil	IM5623	
	MMI	**5201-1**	**1466**
	National	DM75S97	
	TI	**SN54S287**	**1708**
		SN54S370	
◆DM7598	Intersil	IM5610	
	MMI	**5231-1**	**1466**
	National	DM75598	
DM7599	AMD	AM27S03	
		DM7599	
	MMI	5561	
	TI	SN54S189	
DM76L70	TI	SN54L164	
DM76L97	Intersil	IM5623	
◆DM76L99	MMI	L5561	
	National	DM54S189	
◆DM7640	National	DS7640	
DM77S228	**MMI**	**5381-1**	**1449**
DM77S229	**MMI**	**5380-1**	**1449**
DM77S295	**MMI**	**5340-1**	**1449**
	NEC Micro	**μPB405**	**1621**
	Raytheon	**29624**	**1658**
DM77S296	**MMI**	**5341-1**	**1449**
	NEC Micro	**μPB425**	**1621**
	Raytheon	**29625**	**1658**
DM77S474	**Fairchild**	**93448**	**1262**
DM77S475	**Fairchild**	**93438**	**1262**
◆DM7795	National	DM77S95	
◆DM7796	**MMI**	**5241-1**	**1466**
	National	DM77S96	
DM7800	TI	SN55180	
DM7810	TI	SN5426	
DM7812	TI	SN5416	
◆DM7893	National	DS55493	
◆DM7894	National	DS55494	
DM8093	Fairchild	74125	
	TI	SN74125	
DM8094	Fairchild	74126	
	TI	SN74126	
DM8095	TI	SN74365	
DM8096	TI	SN74366	
DM8097	TI	SN74367	
DM8098	TI	SN74368	
DM81LS95	AMD	SN54LS240	
DM81LS96	AMD	SN54LS241	
DM81LS97	AMD	SN54LS240	
DM81LS98	AMD	SN54LS241	
◆DM81L22	TI	SN74L157	
◆DM81S60	Fairchild	93S47	
DM8121	TI	SN74251	
DM8123	Fairchild	74S257	
	TI	SN74S257	
DM8200	Signetics	N8269	
◆DM8213	Fairchild	9311	
	Motorola	MC8311	
	Raytheon	RC9311	
	Signetics	74154	
	TI	SN74154	
DM8214	TI	SN74LS253	
DM8220	Hitachi	HD8220	
DM8280	Fairchild	74176	
	Raytheon	RC8280	
	Signetics	N8280	
	TI	SN74176	
DM8281	Fairchild	74177	
	Raytheon	RC8281	
	Signetics	N8281	
	TI	SN74177	

◆ Discontinued

Bold face device numbers indicate manufacturers data is provided in the IC Master on the pages noted.

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Manufacturer Device	Replacement Source	Device	IC Master Page
DM8283	Fairchild	7483	
♦DM8283	Motorola	MC7483	
	Signetics	7483	
	TI	SN7483A	
DM8288	Signetics	N8288	
DM8290	Fairchild	74196	
	Raytheon	RC8290	
	TI	SN74196	
DM8291	Fairchild	74197	
	Raytheon	RC8291	
	TI	SN74197	
♦DM8296	TI	SN74196	
DM8300	AMD	9300	
	Fairchild	9300	
	Raytheon	RC9300	
	TI	SN29300	
DM8301	AMD	9301	
	Fairchild	9301	
	TI	SN29301	
DM8309	AMD	9309	
	Fairchild	9309	
	TI	SN29309	
DM8310	AMD	9310	
	Fairchild	9310	
	Raytheon	RC9310	
	TI	SN29310	
DM8311	AMD	9311	
	Fairchild	9311	
	Raytheon	RC9311	
	TI	SN29311	
DM8312	AMD	9312	
	Fairchild	9312	
	Raytheon	RC9312	
	TI	SN29312	
DM8316	AMD	9316	
	Fairchild	9316	
	Raytheon	RC9316	
	TI	SN29316	
DM8322	AMD	9322	
	Fairchild	9322	
	Raytheon	RC9322	
		74154	
		74157	
	TI	SN29322	
DM85L60	TI	SN74L192	
DM85L63	TI	SN74L193	
DM85S228	**Harris**	**HM7681**	**1322**
	Raytheon	**29631**	**1660**
DM85S229	**Harris**	**HM7680**	**1322**
	Raytheon	**29630**	**1660**
DM85S68	MMI	85S68	
♦DM85S99	AMD	SN74S189	
	Fairchild	74S189	
	TI	SN74S189	
♦DM8500	Signetics	7476	
	TI	SN7476	
♦DM8501	Signetics	7473	
	TI	SN7473	
♦DM8510	Signetics	7474	
	TI	SN7474	
DM8530	Fairchild	7490	
♦DM8530	Motorola	MC7490	
	Signetics	7490	
	TI	SN7490A	
DM8532	Fairchild	7492	
♦DM8532	Motorola	MC7492	
	Signetics	7492	
	TI	SN7492A	
DM8533	Fairchild	7493	
♦DM8533	Motorola	MC7493	
	Signetics	7493	
	TI	SN7493A	
DM8550	Fairchild	7475	
♦DM8550	Motorola	MC7475	
	Signetics	7475	
	TI	SN7475	
DM8551	TI	SN74173	
DM8560	Fairchild	74192	
	Hitachi	HD8560	
	Motorola	MC74192	
	Raytheon	74192	
	Signetics	74192	
DM8560	TI	SN74192	
DM8563	Fairchild	74193	
	Hitachi	HD8563	
	Motorola	MC74193	
	Raytheon	74193	
	Signetics	74193	
	TI	SN74193	
DM8570	Fairchild	74164	
	Motorola	MC74164	
	Raytheon	74164	
	TI	SN74164	
	Toshiba	TD3503	
♦DM8573	Fairchild	93416	
	Harris	HPROM1024A	
	Intersil	IM5603	
	MMI	**6300-1**	**1449**
	National	DM74S387	
	Signetics	**N82S126**	**1680**
	TI	**SN74S387**	**1708**
♦DM8574	Fairchild	93426	
	Harris	HPROM1024	
	Intersil	IM5603	
		IM5623	
	MMI	**6301-1**	**1449**
	National	DM74S287	
	TI	**SN74S287**	**1708**
DM8577	AMD	AM27S18	
	Harris	**HM7602**	**1284**
	TI	**SN74S188**	**1708**
DM8578	AMD	AM27S19	
	Harris	**HM7603**	**1284**
	MMI	**6331-1**	**1449**
	Signetics	**N82S123**	**1680**
	TI	**SN74S288**	**1708**
DM8579	TI	SN74164	
DM8580	Fairchild	7495	
♦DM8580	Motorola	MC7495	
	Signetics	7495	
	TI	SN7495A	
♦DM8582	MMI	6530	
	TI	SN74S301	
♦DM8588	Intersil	IM5600	
	TI	**SN74S188**	**1708**
DM8590	Fairchild	74165	
	Raytheon	74165	
	TI	SN74165	
♦DM8597	Intersil	IM5623	
	MMI	**6201-1**	**1466**
	National	DM85S97	
	TI	**SN74S287**	**1708**
		SN74S370	
DM8598	Intersil	IM5610	
	MMI	**6231-1**	**1466**
	TI	**SN74S288**	**1708**
DM8599	AMD	AM27S03	
		DM8599	
	Fairchild	74S189	
	MMI	6561	
	TI	SN74S189	
DM86L70	TI	SN74L164	
DM86L97	Intersil	IM5623	
♦DM86L99	Fairchild	IM5501	
	MMI	L6561	
	National	DM74LS189	
♦DM8600	Motorola	MC8300	
DM8601	AMD	9601	
	Fairchild	9601	
	Raytheon	RF8601	
	Signetics	N8T22	
	TI	SN29601	
DM8602	AMD	9602	
	Fairchild	9602	
	Raytheon	RF8602	
♦DM8640	National	DS8640	
	TI	SN74141	
DM87S228	**MMI**	**6381-1**	**1449**
DM87S229	**MMI**	**6380-1**	**1449**
DM87S295	**MMI**	**6340-1**	**1449**
	Raytheon	**29624**	**1658**
DM87S296	**MMI**	**6341-1**	**1449**
	Raytheon	**29625**	**1658**
DM87S474	**Fairchild**	**93448**	**1262**
DM87S475	**Fairchild**	**93438**	**1262**
DM8796	**MMI**	**6241-1**	**1466**
DM8810	TI	SN7426	
DM8842	Fairchild	7442	
DM8842	TI	SN7442A	
DM8846	Fairchild	7446	
	TI	SN7446A	
DM8847	Fairchild	7447	
	TI	SN7447A	
DM8848	Fairchild	7448	
	TI	SN7448	
♦DM8860	National	DS75491	
♦DM8862	National	DS75492	
DM8893	National	DS75493	
DM8894	National	DS75494	
DM9093	Fairchild	9093	
	Motorola	MC853	
	Raytheon	RM993	
	TI	SN158093	
DM9094	Fairchild	9094	
	Motorola	MC856	
	Raytheon	RM9094	
	TI	SN158094	
DM9097	Fairchild	9097	
	Motorola	MC855	
	TI	SN158097	
DM9099	Fairchild	9099	
	Motorola	MC852	
	Raytheon	RM999	
	TI	SN158099	
DM930	Fairchild	930	
	Motorola	MC830	
	Raytheon	RM930	
	TI	SN15830	
DM9300	AMD	9300	
	Fairchild	9300	
	Raytheon	RM9300	
	TI	SN29300	
DM9301	AMD	9301	
	Fairchild	9301	
	TI	SN29301	
DM9312	AMD	9312	
	Fairchild	9312	
	TI	SN29312	
DM932	Fairchild	932	
	Motorola	MC832	
	Raytheon	RM932	
	TI	SN15838	
DM9322	AMD	9322	
	Fairchild	9322	
	Raytheon	RM9322	
		54157	
	TI	SN29322	
DM933	Fairchild	933	
	Motorola	MC833	
	Raytheon	RM933	
	TI	SN15833	
DM93415	Fujitsu	MBM93415	
DM935	Fairchild	935	
	Motorola	MC840	
	Raytheon	RM935	
	TI	SN15835	
DM936	Fairchild	936	
	Motorola	MC836	
	Raytheon	RM936	
	TI	SN15836	
DM937	Fairchild	937	
	Motorola	MC837	
	Raytheon	RM937	
	TI	SN15837	
DM944	Fairchild	944	
	Motorola	MC844	
	Raytheon	RM944	
	TI	SN15844	
DM945	Fairchild	945	
	Motorola	MC845	
	Raytheon	RM945	
	TI	SN15845	
DM946	Fairchild	946	
	Motorola	MC846	
	Raytheon	RM946	
	TI	SN15846	
DM948	Fairchild	948	
	Motorola	MC848	
	Raytheon	RM948	
	TI	SN15848	
DM949	Fairchild	949	
	Motorola	MC849	
	Raytheon	RM949	
	TI	SN15849	
DM951	Fairchild	9157	
	Motorola	MC851	
	Raytheon	RM951	
	TI	SN15851	
DM9567	Motorola	MC857	
DM957	Raytheon	RM957	
	TI	SN15857	
DM958	Fairchild	9158	
	Motorola	MC858	
	Raytheon	RM958	
	TI	SN15858	
DM9601	AMD	9601	
	Fairchild	9601	
	Raytheon	RF9601	
	TI	SN29601	
DM9602	AMD	9602	
	Fairchild	9602	
	Raytheon	RF9602	
DM961	Fairchild	961	
	Motorola	MC861	
	Raytheon	RM961	
	TI	SN15861	
DM962	Fairchild	961	
	Motorola	MC862	
	Raytheon	RM962	
	TI	SN15862	
DM963	Fairchild	963	
	Motorola	MC863	
	Raytheon	RM963	
	TI	SN15863	
DP8212	**NEC Micro**	**μPB8212**	**2172**
DP8216	**NEC Micro**	**μPB8216**	**2184**
DP8224	**NEC Micro**	**μPB8224**	**2188**
DP8226	**NEC Micro**	**μPB8226**	**2184**
DP8228	**NEC Micro**	**μPB8228**	**2193**
DP8238	**NEC Micro**	**μPB8238**	**2193**
DP8304	**Intel**	**8286**	**1948**
DS0026	AMD	MH0026	
	Motorola	MMH0026	
	TI	SN75369	
DS0056	AMD	DS0056	
DS1488	AMD	MC1488	
	Exar	XR1488	
	Motorola	MC1488	
	Raytheon	RC1488	
	Signetics	MC1488	
	Silicon G	SG1488	
	TI	SN75188	
DS1489	AMD	MC1489	
	Exar	XR1489	
	Motorola	MC1489	
	Raytheon	RC1489	
	Signetics	MC1489	
	Silicon G	SG1489	
	TI	SN75189	
DS1489A	Exar	XR1489A	
	Signetics	MC1489A	
DS1603	AMD	DS1603	
DS1691	AMD	AM26LS30	
DS3486	Motorola	MC3486	
DS3487	Motorola	MC3487	
DS3603	AMD	DS3603	
DS3604	AMD	DS3604	
DS3611	Signetics	DS3611	
DS3612	Signetics	DS3612	
DS3613	Signetics	DS3613	
DS3614	Signetics	DS3614	
DS36147	Motorola	DS36147	
DS36177	Motorola	DS36177	
DS3650	Motorola	MC3450	
DS3651	Motorola	MC3430	
DS3652	Motorola	MC3452	
DS3653	Motorola	MC3432	
DS3674	Motorola	MC3460	
DS3687	Motorola	MC3487	
DS3691	AMD	AM26LS30	
DS55107	AMD	SN55107	
	Fairchild	55107	
	Motorola	MC55107	
	Raytheon	RM55107	
	TI	SN55107B	
DS55108	AMD	SN55108	
	Fairchild	55108	
	Motorola	MC55108	
	Raytheon	RM55108	
	TI	SN55108B	

♦ Discontinued

The manufacturers report their devices can be used as direct replacements.
Performance details often differ, so compare the specifications considering your requirements.

National Semiconductor (cont'd)

Manufacturer Device	Replacement Source	Device	IC Master Page
DS55109	AMD	SN55109	
	Fairchild	55109	
	Raytheon	RM55109	
	TI	SN55109A	
DS55110	AMD	SN55110	
	Fairchild	55110	
	TI	SN55110A	
DS55121	Fairchild	55121	
	TI	SN55121	
DS55122	Fairchild	55122	
	TI	SN55122	
DS5520	AMD	SN5520	
	TI	SN5520	
♦DS5521	AMD	SN5521	
	TI	SN5520	
DS5522	TI	SN5522	
♦DS5523	TI	SN5522	
DS5524	AMD	SN5524	
	Fairchild	5524	
	Motorola	MC5524	
	TI	SN5524	
♦DS5525	AMD	SN5525	
	Fairchild	5525	
	Motorola	SN5525	
	TI	SN5524	
DS5528	Fairchild	5528	
	Motorola	MC5528	
	TI	SN5528	
♦DS5529	Fairchild	5529	
	Motorola	MC5529	
	TI	SN5528	
DS55325	AMD	SN55325	
	Motorola	MC55325	
	Raytheon	RM55325	
	TI	SN55325	
DS5534	Fairchild	5534	
	Motorola	MC5534	
♦DS5535	Fairchild	5535	
	Motorola	MC5535	
DS5538	Motorola	MC5538	
♦DS5539	Motorola	MC5539	
DS55450	TI	SN55450	
DS55451	TI	SN55451	
DS55452	TI	SN55452	
DS55453	TI	SN55453	
DS55454	TI	SN55454	
DS55460	TI	SN55460	
DS55461	TI	SN55461	
DS55462	TI	SN55462	
DS55463	TI	SN55463	
DS55464	TI	SN55464	
DS75107	AMD	SN75107	
	Fairchild	75107	
	Motorola	MC75107	
	Raytheon	RC75107	
	TI	SN75107B	
DS75108	AMD	SN74108	
	Fairchild	75108	
	Motorola	MC75108	
	Raytheon	RC75108	
	TI	SN75108B	
DS75109	AMD	SN75109	
	Fairchild	75109	
	Motorola	MC75109	
	Raytheon	RC75109	
	TI	SN75109A	
DS75110	AMD	SN75110	
	Fairchild	75110	
	Motorola	MC75110	
	Raytheon	RC75110	
	TI	SN75110A	
DS75121	Fairchild	75121	
	Motorola	MC8T13	
	TI	SN75121	
DS75122	Fairchild	75122	
	Motorola	MC8T14	
	TI	SN75122	
DS75123	Fairchild	75123	
	Motorola	MC8T23	
	TI	SN75123	
DS75124	Fairchild	75124	
	Motorola	MC8T24	
DS75124	TI	SN75124	
DS75150	TI	SN75150	
DS75154	Fairchild	75154	
	TI	SN75154	
DS7520	AMD	SN7520	
	Motorola	MC7520	
	Signetics	7520	
	Silicon G	SG7520	
	TI	SN7520	
DS75207	AMD	SN75207	
	Fairchild	75207	
	TI	SN75207B	
DS75208	AMD	SN75208	
	Fairchild	75208	
	TI	SN75208B	
♦DS7521	AMD	SN7521	
	Signetics	7521	
	Silicon G	SG7521	
	TI	SN7520	
♦DS7522	Motorola	MC7522	
	Signetics	7522	
	Silicon G	SG7522	
	TI	SN7522	
♦DS7523	Motorola	MC7523	
	Signetics	7523	
	Silicon G	SG7523	
	TI	SN7522	
DS7524	AMD	SN7524	
	Fairchild	75S24	
	Motorola	MC7524	
	Signetics	7524	
	Silicon G	SG7524	
	TI	SN7524	
♦DS7525	AMD	SN7525	
	Motorola	MC7525	
	NPC	SFC2525	
	Signetics	7525	
	Silicon G	SG7525	
	TI	SN7524	
DS7528	Fairchild	7528	
	Motorola	MC7528	
	NPC	SFC2528	
	Silicon G	SG7528	
	TI	SN7528	
♦DS7529	Motorola	MC7529	
	Silicon G	SG7529	
	TI	SN7528	
DS75322	TI	SN75322	
DS75324	Raytheon	RC75324	
	TI	SN75324	
DS75325	AMD	SN75325	
	Fairchild	75325	
	Motorola	MC75325	
	Raytheon	RC75325	
	Silicon G	SG75325	
	TI	SN75325	
DS7534	Fairchild	75S34	
	Motorola	MC7534	
	Silicon G	SG7534	
♦DS7535	Motorola	MC7535	
DS75361	TI	SN75361A	
DS75364	TI	SN75364	
DS75365	Motorola	MC75365	
	TI	SN75365	
DS7538	Motorola	MC7538	
	Silicon G	SG7538	
♦DS7539	Motorola	MC7539	
	Silicon G	SG7539	
DS75450	Fairchild	75450	
	Motorola	MC75450	
	Raytheon	RC75450	
	Signetics	75450	
	Silicon G	SG75450	
	TI	SN75450	
DS75451	Fairchild	75451	
	Motorola	MC75451	
	Raytheon	RC75451	
	Signetics	75451	
	Silicon G	SG75451	
	TI	SN75451	
DS75452	Fairchild	75452	
	Motorola	MC75452	
	Raytheon	RC75452	
	Signetics	75452	
	Silicon G	SG75452	
	TI	SN75452	
DS75453	Fairchild	75453	
	Motorola	MC75453	
	Raytheon	RC75453	
	Signetics	75453	
	TI	SN75453	
DS75454	Fairchild	75454	
	Motorola	MC75454	
	Raytheon	RC75454	
	Signetics	75454	
	Silicon G	SG75454	
	TI	SN75454	
DS75460	TI	SN75460	
DS75461	Motorola	MC75401	
	TI	SN75461	
DS75462	Motorola	MC75402	
	TI	SN75462	
DS75463	Motorola	MC75403	
	TI	SN75463	
DS75464	Motorola	MC75404	
	TI	SN75464	
DS75491	Fairchild	75491	
	Motorola	MC75491	
	TI	SN75491	
DS75492	Fairchild	75492	
	Motorola	MC75492	
	TI	SN75492	
DS75493	TI	SN75493	
DS75494	TI	SN75494	
DS7800	TI	SN55180	
DS7820	AMD	DM7820	
	Signetics	DS7820	
	TI	SN55182	
DS7830	AMD	DM7830	
	Signetics	DS7830	
	TI	SN55183	
DS7831	AMD	DM7831	
	TI	DS7831	
DS7832	AMD	DM7832	
	TI	DS7832	
DS7838	AMD	DS7838	
DS8640	Signetics	SP380	
DS8641	Motorola	DS8641	
DS8800	TI	SN75180	
DS8820	AMD	DM8820	
	Signetics	DS8820	
	TI	DS8820	
		SN75182	
DS8830	AMD	DM8830	
	Signetics	DS8830	
	TI	SN75183	
DS8831	AMD	DM8831	
	TI	DS8831	
DS8832	AMD	DM8832	
	TI	DS8832	
DS8837	Motorola	MC3437	
DS8838	AMD	DS8838	
	Motorola	MC3438	
DS8880	Signetics	DS8880	
	TI	SN75480	
DS8889	Motorola	MC3491	
IDM2901A	NEC Micro	μPB2901A	
IDM2902	NEC Micro	μPB2902A	
IDM2909	NEC Micro	μPB2909A	
IDM2911	NEC Micro	μPB2911A	
INS1671	Western	UC1671	
INS1771	Western	FD1771	
INS2650	Signetics	2650	
INS2651	**Signetics**	**2651**	**2304**
INS2652	**Signetics**	**2652**	**2306**
INS2656	Signetics	2656	
INS4001	Intel	4001	
INS4002	Intel	4002	
INS4003	Intel	4003	
INS4004	Intel	4004	
INS4008	Intel	4008	
INS4009	Intel	4009	
INS8080A	**NEC Micro**	**μPD8080A**	**2119**
		μPD8080AF	**2119**
INS8212	**NEC Micro**	**μPB8212**	**2172**
INS8214	**NEC Micro**	**μPB8214**	**2178**
INS8216	**NEC Micro**	**μPB8216**	**2184**
INS8224	**NEC Micro**	**μPB8224**	**2188**
INS8226	**NEC Micro**	**μPB8226**	**2184**
INS8228	**NEC Micro**	**μPB8228**	**2188**
INS8238	**NEC Micro**	**μPB8238**	**2193**
INS8251	**NEC Micro**	**μPD8251**	**2204**
INS8255	**NEC Micro**	**μPD8255**	**2229**
ISP-8A/600	**Signetics**	**ISP-8A/600**	**2314**
LF111	AMD	LF111	
	Fairchild	μAF111	
LF11508	PMI	MUX-08	
		MUX-88	
LF12508	PMI	MUX-08	
		MUX-88	
LF13508	PMI	MUX-08	
		MUX-88	
LF152	**Datel**	**AM-435-1M**	**689**
	TI	LF152	
		LF252	
LF155	AMD	LF155	
	Fairchild	μAF155	
	Intersil	LF155	
	Motorola	LF155	
	PMI	OP-15	
		PM155	
	Raytheon	LF155	
	Signetics	LF155	
	TI	LF155	
LF156	AMD	LF156	
	Fairchild	μAF156	
	Intersil	LF156	
	Motorola	LF156	
	PMI	OP-16	
		PM156	
	Raytheon	LF156	
	Signetics	LF156	
	TI	LF156	
LF157	AMD	LF157	
	Fairchild	μAF157	
	Intersil	LF157	
	Motorola	LF157	
	PMI	OP-17	
		PM157	
	Raytheon	LF157	
	Signetics	LF157	
	TI	LF157	
LF198	AMD	LF198	
	Datel	**SHM-LM-2M**	**685**
LF211	AMD	LF211	
	Fairchild	μAF211	
LF252	TI	LF252	
LF255	AMD	LF255	
	Fairchild	μAF255	
	Intersil	LF255	
	Motorola	LF255	
	PMI	OP-15	
		PM255	
	Raytheon	LF255	
	TI	LF255	
LF256	AMD	LF256	
	Fairchild	μAF256	
	Intersil	LF256	
	Motorola	LF256	
	PMI	OP-16	
		PM256	
	Raytheon	LF256	
	TI	LF256	
LF257	AMD	LF257	
	Fairchild	μAF257	
	Intersil	LF257	
	Motorola	LF257	
	PMI	OP-17	
		PM257	
	Raytheon	LF257	
	TI	LF257	
LF298	AMD	LF298	
	PMI	SMP-11	
LF311	AMD	LF311	
LF352	**Datel**	**AM-435-1C**	**689**
	TI	LF352	
LF355	AMD	LF355	
	Fairchild	μAF355	
	Intersil	LF355	
	Motorola	LF355	
	PMI	OP-15	
		PM355	
	Raytheon	LF355	
	TI	LF355	
LF356	AMD	LF356	
	Fairchild	μAF356	
	Intersil	LF356	
	Motorola	LF356	

♦ Discontinued

Bold face device numbers indicate manufacturers data is provided in the IC Master on the pages noted.

National Semiconductor (cont'd)

Manufacturer Device	Replacement Source	Device	IC Master Page
LF356	PMI	OP-16	
		PM356	
	Raytheon	LF356	
	TI	LF356	
LF357	AMD	LF357	
	Fairchild	μAF357	
	Intersil	LF357	
	Motorola	LF357	
	PMI	OP-17	
		PM357	
	Raytheon	LF357	
	TI	LF357	
LF398	AMD	LF398	
	Datel	**SHM-LM-2**	**685**
	PMI	SMP-11	
LH0001	PMI	OP-20	
LH0021	Beckman	833-21	
LH0042	AD	AD0042	
	Intersil	LH0042	
LH0044	AD	AD517	
LH0062	AD	AD528	
LH0070	AD	AD581	
LH2101	AMD	LH2101	
	Intersil	LH2101	
	Raytheon	LH2101	
LH2108	Intersil	LH2108	
LH2108A	PMI	PM2108A	
LH2110	Intersil	LH2110	
LH2111	AMD	LH2111	
	Intersil	LH2111	
	Raytheon	LH2111	
LH2201	AMD	LH2201	
	Raytheon	LH2201	
LH2208	PMI	PM2208	
LH2208A	PMI	PM2208A	
LH2211	AMD	LH2211	
	Raytheon	LH2211	
LH2301	AMD	LH2301	
	Intersil	LH2301	
	Raytheon	LH2301	
LH2308	Intersil	LH2308	
	PMI	PM2308	
LH2308A	PMI	PM2308A	
LH2310	Intersil	LH2310	
LH2311	AMD	LH2311	
	Intersil	LH2311	
	Raytheon	LH2311	
LH740	Fairchild	μA740	
	Intersil	LH740	
	Signetics	μA740	
LM0052	AD	AD506	
LM100	Intersil	LM100	
	NPC	SFC2100	
	Silicon G	SG100	
LM101	AD	AD101	
	AMD	LM101	
	Fairchild	μA101	
	Intersil	LM101	
	Motorola	LM101	
	NPC	SFC2101	
	Raytheon	LM101	
	RCA	CA101	
		CA748	
	Signetics	LM101	
	Silicon G	SG101	
	TI	LM101	
LM102	AMD	LM102	
	Fairchild	μA102	
	Intersil	LM102	
	Motorola	LM110	
	Silicon G	SG102	
LM104	**Fairchild**	**μA104**	**934**
	Motorola	LM104	
	NPC	SFC2104	
	Raytheon	LM104	
	Silicon G	SG104	
	TI	LM104	
LM105	AMD	LM105	
	Fairchild	**μA105**	**934**
	Intersil	LM105	
	Motorola	LM105	
	NPC	SFC2105	
LM105	Raytheon	LM105	
	Silicon G	SG105	
	TI	LM105	
LM106	AMD	LM106	
	Raytheon	LM106	
	TI	LM106	
LM107	AD	AD741S	
	AMD	LM107	
	Fairchild	μA107	
	Intersil	LM107	
	Motorola	LM107	
	NPC	SFC2107	
	Raytheon	LM107	
	RCA	CA107	
	Signetics	LM107	
	Silicon G	SG107	
	TI	LM107	
LM108	AD	AD108	
	AMD	LM108	
	Fairchild	μA108	
	Intersil	LM108	
	Motorola	LM108	
	PMI	PM108	
	Raytheon	LM108	
	RCA	CA108	
	Signetics	LM108	
	Silicon G	SG108	
LM109	**Fairchild**	**μA109**	**934**
	Motorola	LM109	
	NPC	SFC2109	
	Raytheon	LM109	
	Signetics	LM109	
	Silicon G	SG109	
	TI	LM109	
LM110	AMD	LM110	
	Fairchild	μA110	
	Intersil	LM110	
	Motorola	LM110	
	PMI	BUF-01	
		BUF-02	
	Silicon G	SG110	
LM111	AMD	LM111	
	Fairchild	μA111	
	Intersil	LM111	
	Motorola	LM111	
	NPC	SFC2111	
	Raytheon	LM111	
	RCA	CA111	
	Signetics	LM111	
	Silicon G	SG111	
	TI	LM111	
LM112	AMD	LM112	
	Raytheon	LM112	
	Silicon G	SG1118	
LM114	PMI	MAT-01	
LM117	Motorola	LM117	
	Silicon G	SG117	
	TI	LM117	
LM118	AD	AD518	
	AMD	LM118	
	Raytheon	LM118	
	TI	LM118	
LM119	AMD	LM119	
LM120-12	Silicon G	SG120-12	
LM120-15	Silicon G	SG120-15	
LM120-5	Silicon G	SG120-5	
LM120-5.2	Silicon G	SG120-5.2	
LM120-8	Silicon G	SG120-8	
LM123	Motorola	LM123	
	Silicon G	SG123	
LM124	AMD	LM124	
	Fairchild	μA124	
	Intersil	LM124	
	Motorola	LM124	
	Raytheon	LM124	
	RCA	CA124	
	Signetics	LM124	
	Silicon G	SG124	
	TI	LM124	
LM129	Raytheon	LM129	
LM1303	Motorola	MC1303	
	Raytheon	RC4739	
LM1304	Fairchild	μA732	
LM1307	Fairchild	μA767	
	Motorola	MC1307	
		MC1317	
LM1310	Exar	XR1310	
	Motorola	MC1310	
	RCA	CA1310	
	Sprague	ULN-2110	
		ULN-2210	
LM1351	Motorola	MC1351	
LM1360◊	**Exar**	**XR13600**	**933**
LM137	Motorola	LM137	
	TI	LM137	
LM139	AMD	LM139	
	Fairchild	μA139	
	Motorola	LM139	
	Raytheon	LM139	
	RCA	CA139	
	Signetics	LM139	
	Silicon G	SG139	
	TI	LM139	
LM139A	Motorola	LM139A	
	PMI	CMP-04	
		PM139A	
LM1391	Motorola	MC1391	
	RCA	CA1391	
	Sprague	ULN-2291	
LM1394	Motorola	MC1394	
	RCA	CA1394	
	Sprague	ULN-2294	
LM140	**Exar**	**XR146**	**929**
LM140-05	Silicon G	SG140-05	
LM140-06	Silicon G	SG140-06	
LM140-08	Silicon G	SG140-08	
LM140-12	Silicon G	SG140-12	
LM140-15	Silicon G	SG140-15	
LM140-18	Silicon G	SG140-18	
LM140-24	Silicon G	SG140-24	
LM1408	**Datel**	**DAC-IC8BC**	**671**
LM1414	Motorola	MC1414	
	Raytheon	RC1414	
	TI	TL514	
LM143	**Harris**	**HA-2640**	**984**
LM1458	AMD	1458	
	Exar	XR1458	
	Fairchild	μA1458	
	Harris	**HA-2655**	**986**
	Hitachi	HA17458	
	Motorola	MC1458	
	NEC America	μPC1458	
	PMI	OP-14	
		SSS1458	
	Raytheon	RC1458	
		RC4558	
	RCA	CA1458	
	Signetics	MC1458	
	Silicon G	SG1458	
	TI	MC1458	
LM146	**Exar**	**XR146**	**929**
LM148	AMD	LM148	
	Exar	XR4741	
	Harris	HA-4741	
	Intersil	LM148	
	Motorola	LM148	
		MC4741	
	Raytheon	LM148	
	TI	LM148	
LM1488	Exar	XR1488	
	Motorola	MC1488	
	National	DS1488	
	Silicon G	SG1488	
LM1489	Motorola	MC1489	
	National	DS1489	
	Silicon G	SG1489	
LM149	AMD	LM149	
	Intersil	LM149	
	Raytheon	LM149	
LM1496	Fairchild	μA796	
	Motorola	MC1496	
	Signetics	MC1496	
	Silicon G	SG1496	
LM150	Motorola	LM150	
LM1508	**Datel**	**DAC-IC8BM**	**671**
LM1514	Motorola	MC1514	
	Raytheon	RM1514	
	TI	TL514	
LM1558	AMD	1558	
	Exar	XR1588	
	Fairchild	μA1558	
	Harris	**HA-2650**	**986**
LM1558	Motorola	MC1558	
	PMI	PM1558	
		SSS1558	
	Raytheon	RM1558	
	RCA	CA1558	
	Signetics	MC1558	
	Silicon G	SG1558	
	TI	MC1558	
LM158	Motorola	LM158	
	Raytheon	LM158	
		RM4139	
	Signetics	**SE532**	**1109**
	TI	LM158	
LM1596	Motorola	MC1596	
	Signetics	MC1596	
	Silicon G	SG1596	
LM160	Fairchild	μA760	
LM1611	National	DS1611	
LM1612	National	DS1612	
LM1613	National	DS1613	
LM1614	National	DS1614	
LM163	National	DS1603	
LM163A	National	DS1604	
LM1800	Exar	XR1800	
	Fairchild	μA758	
	RCA	CA758	
	Sprague	ULN-2244	
LM1820	Fairchild	μA720	
	Sprague	ULN-2137	
LM1828	Sprague	ULN-2228	
LM1829	Fairchild	μA787	
LM1841	Fairchild	μA2136	
	Motorola	MC1356	
	Sprague	ULN-2136	
LM1848	Sprague	ULN-2229	
LM1877	Sprague	ULN-2274	
LM1880	Signetics	LM1880	
LM1900	TI	LM1900	
LM193	Signetics	LM193	
	TI	LM193	
LM199	Raytheon	LM199	
LM200	Intersil	LM200	
	NPC	SFC2200	
	Silicon G	SG200	
LM201	AD	AD201	
	AMD	LM201	
	Fairchild	μA201	
	Intersil	LM201	
	Motorola	LM201	
	NPC	SFC2201	
	RCA	CA201	
		CA748	
	Signetics	LM201	
	Silicon G	SG201	
	TI	LM201	
LM202	AMD	LM202	
	Fairchild	μA202	
	Intersil	LM202	
	Motorola	LM210	
	Silicon G	SG202	
LM204	Fairchild	μA204	
	Motorola	LM204	
	NPC	SFC2204	
	Raytheon	LM204	
	Silicon G	SG204	
	TI	LM204	
LM205	AMD	LM205	
	Fairchild	μA205	
	Intersil	LM205	
	Motorola	LM205	
	NPC	SFC2205	
	Raytheon	LM205	
	Silicon G	SG205	
	TI	LM205	
LM206	AMD	LM206	
	TI	LM206	
LM207	AD	AD741J	
	AMD	LM207	
	Fairchild	μA207	
	Intersil	LM207	
	Motorola	LM207	
	NPC	SFC2207	
	Raytheon	LM207	
	RCA	CA207	
	Signetics	LM207	
	Silicon G	SG207	

◆ Discontinued

The manufacturers report their devices can be used as direct replacements.
Performance details often differ, so compare the specifications considering your requirements.

National Semiconductor (cont'd)

Manufacturer Device	Replacement Source	Device	IC Master Page
LM207	TI	LM207	
LM208	AD	AD208	
	AMD	LM208	
	Fairchild	µA208	
	Intersil	LM208	
	Motorola	LM208	
	PMI	PM208	
	Raytheon	LM208	
	RCA	CA208	
	Signetics	LM208	
	Silicon G	SG208	
LM209	**Fairchild**	**µA209**	**934**
	Motorola	LM209	
	NPC	SFC2209	
	Raytheon	LM209	
	Signetics	LM209	
	Silicon G	SG209	
	TI	LM209	
LM210	AMD	LM210	
	Fairchild	µA210	
	Intersil	LM210	
	Motorola	LM210	
	PMI	BUF-01	
		BUF-02	
	Silicon G	SG210	
LM211	AMD	LM211	
	Fairchild	µA211	
	Intersil	LM211	
	Motorola	LM211	
	NPC	SFC2211	
	Raytheon	LM211	
	RCA	CA211	
	Signetics	LM211	
	Silicon G	SG211	
	TI	LM211	
LM2111	Motorola	MC1357	
	RCA	CA2111	
	Signetics	ULN2111	
	Sprague	ULN-2111	
LM2113	Sprague	ULN-2113	
LM212	AMD	LM212	
	Raytheon	LM212	
	Silicon G	SG212	
LM216	AMD	LM216	
LM217	Motorola	LM217	
	Silicon G	SG217	
	TI	LM217	
LM218	AD	AD518	
	AMD	LM218	
	Raytheon	LM218	
	TI	LM218	
LM219	AMD	LM219	
	NEC America	µPC219	
LM220-05	Silicon G	SG220-05	
LM220-12	Silicon G	SG220-12	
LM220-15	Silicon G	SG220-15	
LM220-5.2	Silicon G	SG220-5.2	
LM220-8	Silicon G	SG220-8	
LM223	Motorola	LM223	
	Silicon G	SG223	
LM224	AMD	LM224	
	Intersil	LM224	
	Motorola	LM224	
	Raytheon	LM224	
	RCA	CA224	
	Signetics	LM224	
	Silicon G	SG224	
	TI	LM224	
LM237	Motorola	LM237	
	TI	LM237	
LM239	AMD	LM239	
	Motorola	LM239	
		MC3302	
	Raytheon	LM239	
	RCA	CA239	
	Signetics	LM239	
	Silicon G	SG239	
	TI	LM239	
LM239A	Motorola	LM239A	
	PMI	CMP-04	
		PM239A	
LM246	**Exar**	**XR246**	**929**
LM248	AMD	LM248	
	Exar	XR4741	
	Intersil	LM248	
	Motorola	LM248	
		MC4741	
	Raytheon	LM248	
	TI	LM248	
LM249	AMD	LM249	
	Intersil	LM249	
	Raytheon	LM249	
LM250	Motorola	LM250	
LM258	Motorola	LM258	
	Raytheon	LM258	
	Signetics	LM258	
	TI	LM258	
LM2900	Fairchild	µA2900	
	Motorola	LM2900	
	Raytheon	LM2900	
	TI	LM2900	
LM2901	Fairchild	µA2901	
	Hitachi	HA17901	
	Motorola	LM2901	
	NEC America	µPC2901	
	Raytheon	LM2901	
	RCA	CA339	
	TI	LM2901	
LM2902	Fairchild	µA2902	
	Hitachi	HA17902	
	Motorola	LM2902	
	NEC America	µPC2902	
	Raytheon	LM2902	
	TI	LM2902	
LM2903	TI	LM2903	
LM2904	Motorola	LM2904	
	TI	LM2904	
LM293	Signetics	LM293	
	TI	LM293	
LM298	Burr-Brown	SHC298	
LM299	Raytheon	LM299	
LM300	Intersil	LM300	
	NPC	SFC2300	
	Silicon G	SG300	
LM301	AD	AD301	
	AMD	LM301	
	Fairchild	µA301	
	Intersil	LM301	
	Motorola	LM301	
	NEC America	µPC301A	
	NPC	SFC2301	
	Raytheon	LM301	
	RCA	CA301	
	Signetics	LM301	
	Silicon G	SG301	
	TI	LM301	
	Toshiba	TA7505	
LM301A	NEC America	µPC157	
LM3011	RCA	CA3011	
LM3018	Fairchild	µA3018	
	RCA	CA3018	
LM3019	Fairchild	µA3019	
	RCA	CA3019	
LM302	AMD	LM302	
	Fairchild	µA302	
	Intersil	LM302	
	Motorola	LM310	
		MC7912	
	Silicon G	SG302	
LM3026	Fairchild	µA3026	
	RCA	CA3026	
LM3028	RCA	CA3028	
LM3039	RCA	CA3039	
LM304	**Fairchild**	**µA304**	**934**
	Motorola	LM304	
	NEC America	µPC142	
	NPC	SFC2304	
	Raytheon	LM304	
	Silicon G	SG304	
	TI	LM304	
LM3045	Fairchild	µA3045	
	RCA	CA3045	
	Silicon G	SG3045	
LM3046	Fairchild	µA3046	
	Motorola	MC3346	
	RCA	CA3046	
	Silicon G	SG3046	
LM305	AMD	LM305	
LM305	**Fairchild**	**µA305**	**934**
	Intersil	LM305	
	Motorola	LM305	
	NEC America	µPC141	
	NPC	SFC2305	
	Raytheon	LM305	
	Silicon G	SG305	
	TI	LM305	
LM3053	Fairchild	µA753	
	RCA	CA3053	
	Sprague	ULN-2209	
LM3054	Fairchild	µA3054	
	Motorola	CA3054	
	RCA	CA3054	
LM306	AMD	LM306	
	Raytheon	LM306	
	TI	LM306	
LM3064	Fairchild	µA3064	
	Motorola	MC1364	
	RCA	CA3064	
	Sprague	ULN-2264	
LM3065	Fairchild	µA3065	
	Motorola	MC1358	
	RCA	CA3065	
	Sprague	ULN-2165	
LM3066	RCA	CA3066	
LM3067	RCA	CA3067	
LM307	AD	AD741J	
	AMD	LM307	
	Fairchild	µA307	
	Intersil	LM307	
	Motorola	LM307	
	NPC	SFC2307	
	Raytheon	LM307	
	RCA	CA307	
	Signetics	LM307	
	Silicon G	SG307	
	TI	LM307	
LM3070	Fairchild	µA780	
	RCA	CA3070	
	Sprague	ULN-2124	
LM3071	RCA	CA3071	
	Sprague	ULN-2127	
LM3072	RCA	CA3072	
LM3075	Fairchild	µA3075	
	Motorola	MC1375	
	RCA	CA3075	
LM308	AD	AD308	
	AMD	LM308	
	Fairchild	µA308	
	Intersil	LM308	
	Motorola	LM308	
	NEC America	µPC156A	
	PMI	PM308	
	Raytheon	LM308	
	RCA	CA308	
	Signetics	LM308	
	Silicon G	SG308	
LM3086	Fairchild	µA3086	
	Motorola	MC3386	
	RCA	CA3086	
	Silicon G	SG3086	
LM3089	RCA	CA3089	
	Sprague	ULN-2289	
LM309	**Fairchild**	**µA309**	**934**
	Motorola	LM309	
	NPC	SFC2309	
	Raytheon	LM309	
	Signetics	LM309	
	Silicon G	SG309	
	TI	LM309	
LM310	AMD	LM310	
	Fairchild	µA310	
	Intersil	LM310	
	Motorola	LM310	
	PMI	BUF-01	
		BUF-02	
	Silicon G	SG310	
LM311	AMD	LM311	
	Fairchild	µA311	
	Intersil	LM311	
	Motorola	LM311	
	NEC America	µPC271	
		µPC311	
	NPC	SFC2311	
	Raytheon	LM311	
LM311	RCA	CA311	
	Signetics	LM311	
	Silicon G	SG311	
	TI	LM311	
LM312	AMD	LM312	
	Raytheon	LM312	
	Silicon G	SG3118	
LM3126	RCA	CA3126	
LM316	AMD	LM316	
LM317	Motorola	LM317	
	Silicon G	SG317	
	TI	LM317	
LM318	AD	AD518	
	AMD	LM318	
	NEC America	µPC159A	
	Raytheon	LM318	
	TI	LM318	
LM319	AMD	LM319	
	NEC America	µPC319	
		LM319	
LM320-05	Motorola	MC7905	
	Silicon G	SG320-05	
	TI	µA7905	
LM320-06	TI	µA7906	
LM320-08	Silicon G	SG320-08	
	TI	µA7908	
LM320-12	Motorola	MC7912	
	Silicon G	SG320-12	
	TI	µA7912	
LM320-15	Silicon G	SG320-15	
	TI	µA7915	
LM320-24	TI	µA7924	
LM320-5.2	Silicon G	SG320-5.2	
LM320-8	Silicon G	SG320-8	
LM320MP-12	Silicon G	SG320P-12	
LM320MP-15	Silicon G	SG320P-15	
LM320MP-5.0	Silicon G	SG320P-5.0	
LM320MP12	Signetics	µA79M12	
	TI	µA79M12	
LM320MP15	Signetics	µA79M15	
	TI	µA79M15	
LM320MP18	Signetics	µA79M18	
LM320MP24	Signetics	µA79M24	
	TI	µA79M24	
LM320MP5.0	Signetics	µA79M05	
	TI	µA79M05	
LM320MP6.0	Signetics	µA79M06	
	TI	µA79M06	
LM320MP8.0	Signetics	µA79M08	
	TI	µA79M08	
LM320T12	Signetics	µA7912	
	TI	µA7912	
LM320T15	Signetics	µA7915	
	TI	µA7915	
LM320T18	Signetics	µA7918	
LM320T24	Signetics	µA7924	
	TI	µA7924	
LM320T5.0	TI	µA7905	
LM320T6.0	Signetics	µA7906	
	TI	µA7906	
LM320T8.0	Signetics	µA7908	
	TI	µA7908	
LM323	Fairchild	SH0323	
	Motorola	LM323	
	Silicon G	SG323	
LM324	AMD	LM324	
	Fairchild	µA324	
	Motorola	LM324	
	NEC America	µPC324	
	Raytheon	LM324	
	RCA	CA324	
	Signetics	LM324	
	Silicon G	SG324	
	TI	LM324	
LM329	Raytheon	LM329	
LM3301	Motorola	MC3301	
LM3302	Motorola	MC3302	
	Silicon G	SG3302	
	TI	LM3302	
LM337	Motorola	LM337	
	TI	LM337	
LM339	AMD	LM339	
	Fairchild	µA339	
	Motorola	LM339	
		MC3302	
	NEC America	µPC339	

♦ Discontinued

Bold face device numbers indicate manufacturers data is provided in the IC Master on the pages noted.

National Semiconductor (cont'd)

Manufacturer Device	Replacement Source	Device	IC Master Page
LM339	Raytheon	LM339	
	RCA	CA339	
	Signetics	LM339	
	Silicon G	SG339	
	TI	LM339	
LM339A	Motorola	LM339A	
	PMI	CMP-04	
		PM339A	
LM340-10	TI	LM340-10	
LM340-12	Fairchild	µA7812	
	Motorola	MC7812	
	Raytheon	RC7812	
	Signetics	LM340-12	
	Silicon G	SG340-12	
	TI	µA7812	
		LM340-12	
LM340-15	Fairchild	µA7815	
	Motorola	MC7815	
	Signetics	µA7815	
		LM340-15	
	Silicon G	SG340-15	
	TI	µA7815	
		LM340-15	
LM340-18	Fairchild	µA7818	
	Motorola	MC7818	
	Raytheon	RC7818	
	Signetics	µA7818	
		LM340-18	
	Silicon G	SG340-18	
	TI	µA7818	
		LM340-18	
LM340-24	Fairchild	µA7824	
	Motorola	MC7824	
	Raytheon	RC7824	
	Signetics	µA7824	
		LM340-24	
	Silicon G	SG340-24	
	TI	µA7824	
		LM340-24	
LM340-5	Fairchild	µA7805	
	Motorola	MC7805	
	Raytheon	RC7805	
	Signetics	µA7805	
		LM340-5	
	Silicon G	SG340-05	
	TI	µA7805	
		LM340-5	
LM340-6	Fairchild	µA7806	
	Motorola	MC7806	
	Raytheon	RC7806	
	Signetics	µA7806	
		LM340-6	
	Silicon G	SG340-06	
	TI	LM340-6	
LM340-8	Fairchild	µA7808	
	Motorola	MC7808	
	Raytheon	RC7808	
	Signetics	µA7808	
		LM340-8	
	Silicon G	SG340-08	
	TI	µA7808	
		LM340-8	
LM340LA-12	TI	µA78L12	
LM340LA-15	TI	µA78L15	
LM340LA-5	TI	µA78L05	
LM340LA-6	TI	µA78L06	
LM340LA-8	TI	µA78L08	
LM340T-12	NEC America	µPC14312	
LM340T-15	NEC America	µPC14315	
LM340T-18	NEC America	µPC14318	
LM340T-24	NEC America	µPC14324	
LM340T-5	NEC America	µPC14305	
LM340T-8	NEC America	µPC14308	
LM3401	Motorola	MC3401	
LM341-12	Motorola	MC78M12	
	TI	µA78M12	
LM341-15	Motorola	MC78M15	
	TI	µA78M15	
LM341-24	Motorola	MC78M24	
	TI	µA78M24	
LM341-5	Motorola	MC78M05	
	TI	µA78M05	
LM341-6	Motorola	MC78M06	
	Signetics	µA78M06	
	TI	µA78M06	
LM341-8	Motorola	MC78M08	
	TI	µA78M08	
LM342-05	Motorola	MC78M05	
LM342-06	Motorola	MC78M06	
LM342-08	Motorola	MC78M08	
LM342-12	Motorola	MC78M12	
LM342-15	Motorola	MC78M15	
LM342-18	Motorola	MC78M18	
LM342-24	Motorola	MC78M24	
LM343	**Harris**	**HA-2645**	**984**
	Motorola	MC1439	
LM346	**Exar**	**XR346**	**929**
LM348	AMD	LM348	
	Exar	XR4741	
	Harris	HA-4741	
	Motorola	LM348	
		MC4741	
	Raytheon	LM348	
	TI	LM348	
LM349	AMD	LM349	
	Raytheon	LM349	
LM350	Motorola	LM350	
LM351	National	DS75453	
LM354	NPC	SFC2524	
		SFC2525	
♦LM358	Motorola	LM358	
	NEC America	µPC358	
	Raytheon	LM358	
		RC4139	
	Signetics	LM358	
	TI	LM358	
♦LM360	Fairchild	µA760	
LM3611	Sprague	UDN-3611	
		ULN-3611	
♦LM3612	National	DS3612	
	Sprague	UDN-3612	
		ULN-3612	
♦LM3613	National	DS3613	
	Sprague	UDN-3613	
		ULN-3613	
♦LM3614	National	DS3614	
	Sprague	UDN-3614	
		ULN-3614	
♦LM3625	National	DS3625	
♦LM363	National	DS3603	
♦LM363A	National	DS3604	
♦LM367	Silicon G	SG305	
♦LM376	**Fairchild**	**µA376**	**934**
	Motorola	LM305	
	NEC America	µPC305	
		LM376	
	NPC	SFC2376	
	TI	LM376	
LM377	Sprague	ULN-2278	
LM380	Sprague	ULN-2280	
LM381	Signetics	LM381	
LM382	Signetics	LM382	
LM383	Sprague	ULN-3701	
LM384	Sprague	ULN-2281	
LM387	Signetics	LM387	
LM3900	Fairchild	µA3900	
	Motorola	MC3401	
	Raytheon	RC3302	
	TI	LM3900	
♦LM3901	Motorola	MC3302	
	Raytheon	MC3302	
LM3909	Siliconix	LM3909	
LM3911	NEC America	µPC3911	
LM3911-05	NEC America	µPC616	
LM393	Signetics	LM393	
	TI	LM393	
LM399	AD	AD581	
	Raytheon	LM399	
LM4250	Fairchild	µA776	
	Harris	**HA-2720**	**990**
	Intersil	LM4250	
	Silicon G	SG4250	
	Solitron	UC4250	
LM55107A	Motorola	MC55107	
	National	DS55107	
LM55108A	Motorola	MC55108	
	National	DS55108	
LM5520	National	DS5520	
LM5520	Silicon G	SG5520	
LM5521	Silicon G	SG5521	
LM5522	National	DS5522	
	Silicon G	SG5522	
LM5523	Silicon G	SG5523	
LM5524	Motorola	MC5524	
	National	DS5524	
	Silicon G	SG5524	
LM5525	Motorola	MC5525	
	Silicon G	SG5525	
LM5528	Motorola	MC5528	
	National	DS5528	
	Silicon G	SG5528	
LM5529	Motorola	MC5529	
	Silicon G	SG5529	
LM55325	Motorola	MC55325	
	National	DS55325	
	Silicon G	SG55325	
LM5534	Motorola	MC5534	
	National	DS5534	
	Silicon G	SG5534	
LM5535	Motorola	MC5535	
	Silicon G	SG5535	
LM5538	Motorola	MC5538	
♦LM5538	National	DS5538	
	Silicon G	SG5538	
LM5539	Motorola	MC5539	
	Silicon G	SG5539	
LM55450	National	DS55450	
	Silicon G	SG55450	
LM55451	National	DS55451	
	Silicon G	SG55451	
LM55452	National	DS55452	
	Silicon G	SG55452	
LM55453	Silicon G	SG55453	
LM55454	National	DS55454	
	Silicon G	SG55454	
LM555	AMD	LM555	
	Cherry	CS555	
	Exar	XR555	
	Fairchild	µA555	
	Motorola	MC1455	
		MC1555	
	NEC America	µPC1555	
	Raytheon	RC555	
		RM555	
	RCA	CA555	
	Signetics	NE555	
	Silicon G	SG555	
	TI	NE555	
		SE555	
LM556	AMD	LM556	
	Exar	XR556	
	Fairchild	µA556	
	Motorola	MC3456	
		MC3556	
	Raytheon	RC556	
	Silicon G	SG556	
	TI	NE556	
		SE556	
LM565	Motorola	LM565	
	Signetics	NE565	
LM566	Signetics	NE566	
LM567	Exar	XR567	
	Signetics	NE567	
LM703	Fairchild	µA703	
LM709	Fairchild	µA709	
	Motorola	MC1709	
	NEC America	µPC55A	
	NPC	SFC2709	
	Raytheon	RC709	
		RM709	
	Signetics	µA709	
	TI	µA709	
	Toshiba	TA7502	
LM710	Fairchild	µA710	
	Motorola	MC1710	
	NEC America	µPC71	
	NPC	SFC2710	
	Raytheon	RC710	
		RM710	
	RCA	CA710	
	Signetics	µA710	
	Silicon G	SG710	
	TI	µA710	
LM711	Fairchild	µA711	
LM711	Motorola	MC1711	
	NPC	SFC2711	
	Raytheon	RC711	
		RM711	
	RCA	CA711	
	Signetics	µA711	
	Silicon G	SG711	
	TI	µA711	
LM723	AMD	723	
	Fairchild	**µA723**	**934**
	Intersil	723	
	Motorola	MC1723	
	NPC	SFC2723	
	Raytheon	RC723	
		RM723	
	RCA	CA723	
	SGS	L123	
	Signetics	µA723	
	Silicon G	SG723	
	TI	µA723	
LM725	AMD	725	
	Fairchild	µA725	
	NEC America	µPC154	
		µPC154A	
	PMI	PM725	
		SSS725	
	Raytheon	RC725	
		RM725	
LM733	AMD	733	
	Fairchild	µA733	
	Motorola	MC1733	
	Raytheon	RC733	
		RM733	
	Signetics	µA733	
	Silicon G	SG733	
	TI	µA733	
LM741	AD	AD741	
	AMD	741	
	Fairchild	µA741	
	Intersil	741	
	Motorola	MC1741	
	NEC America	µPC151	
		µPC741	
	NPC	SFC2741	
	PMI	OP-02	
		PM741	
		SSS741	
	Raytheon	RC741	
		RM741	
	RCA	CA741	
	Signetics	µA741	
	Silicon G	SG741	
	Sprague	ULN-2151	
	TI	µA741	
	Toshiba	TA7504	
LM746	Motorola	MC1328	
	Sprague	ULN-2114	
		ULN-2228	
LM747	AMD	747	
	Fairchild	µA747	
	Motorola	MC1747	
	NEC America	µPC251	
	PMI	OP-04	
		PM747	
		SSS747	
	Raytheon	RC747	
		RM747	
	RCA	CA747	
	Signetics	µA747	
	Silicon G	SG747	
	TI	µA747	
LM748	AMD	748	
	Fairchild	µA748	
	Intersil	748	
	Motorola	MC1748	
	NPC	SFC2748	
	Raytheon	RC748	
		RM748	
	RCA	CA748	
	Signetics	µA748	
	Silicon G	SG748	
	TI	µA748	
LM75107A	Motorola	MC75107	
	National	DS75107	
LM75108A	Motorola	MC75108	
	National	DS75108	

♦ Discontinued

The manufacturers report their devices can be used as direct replacements.
Performance details often differ, so compare the specifications considering your requirements.

NEC America (cont'd)

Manufacturer Device	Replacement Source	Device	IC Master Page
μPB74LS21	Motorola	SN74LS21	
	National	DM74LS21	
	Raytheon	74LS21	
	Signetics	74LS21	
	TI	SN74LS21	
μPB74LS251	AMD	SN74LS251	
	Fairchild	74LS251	
	Hitachi	HD74LS251	
	Motorola	SN74LS251	
	National	DM74LS251	
	Raytheon	74LS251	
	Signetics	74LS251	
	TI	SN74LS251	
μPB74LS253	AMD	SN74LS253	
	Fairchild	74LS253	
	Hitachi	HD74LS253	
	Motorola	SN74LS253	
	National	DM74LS253	
	Raytheon	74LS253	
	Signetics	74LS253	
	TI	SN74LS253	
μPB74LS257	AMD	SN74LS257	
	Fairchild	74LS257	
	Hitachi	HD74LS257	
	Motorola	SN74LS257A	
	National	DM74LS257	
	Raytheon	74LS257	
	Signetics	74LS257	
	TI	SN74LS257A	
μPB74LS258	AMD	SN74LS258	
	Fairchild	74LS258	
	Motorola	SN74LS258	
	National	DM74LS258	
	Raytheon	74LS258	
	Signetics	74LS258	
	TI	SN74LS258	
μPB74LS27	Fairchild	74LS27	
	Hitachi	HD74LS27	
	Motorola	SN74LS27	
	National	DM74LS27	
	Raytheon	74LS27	
	Signetics	74LS27	
	TI	SN74LS27	
μPB74LS279	Fairchild	74LS279	
	Motorola	SN74LS279	
	National	DM74LS279	
	Raytheon	74LS279	
	Signetics	74LS279	
	TI	SN74LS279	
μPB74LS295	Fairchild	74LS295	
	Motorola	SN74LS295	
	Raytheon	74LS295A	
	Signetics	74LS295	
	TI	SN74LS295B	
μPB74LS30	Fairchild	74LS30	
	Hitachi	HD74LS30	
	Motorola	SN74LS30	
	National	DM74LS30	
	Raytheon	74LS30	
	Signetics	74LS30	
	TI	SN74LS30	
μPB74LS32	Fairchild	74LS32	
	Hitachi	HD74LS32	
	Motorola	SN74LS32	
	National	DM74LS32	
	Raytheon	74LS32	
	Signetics	74LS32	
	TI	SN74LS32	
μPB74LS365	Fairchild	74LS365	
	Motorola	SN74LS365A	
	National	DM74LS365	
	Raytheon	74LS365	
	Signetics	74LS365A	
	TI	SN74LS365A	
μPB74LS366	Fairchild	74LS366	
	Motorola	SN74LS366A	
	National	DM74LS366	
	Raytheon	74LS366	
	Signetics	74LS366A	
	TI	SN74LS366A	
μPB74LS367	Fairchild	74LS367	
	Hitachi	HD74LS367	
	Motorola	SN74LS367A	
μPB74LS367	National	DM74LS367	
	Raytheon	74LS367	
	Signetics	74LS367A	
	TI	SN74LS367A	
μPB74LS368	Fairchild	74LS368	
	Hitachi	HD74LS368	
	Motorola	SN74LS368A	
	National	DM74LS368	
	Raytheon	74LS368	
	Signetics	74LS368A	
	TI	SN74LS368A	
μPB74LS37	Fairchild	74LS37	
	Hitachi	HD74LS37	
	Motorola	SN74LS37	
	National	DM74LS37	
	Raytheon	74LS37	
	Signetics	74LS37	
	TI	SN74LS37	
μPB74LS375	Fairchild	74LS375	
	Motorola	SN74LS375	
	Raytheon	74LS375	
	Signetics	74LS375	
	TI	SN74LS375	
μPB74LS38	Fairchild	74LS38	
	Hitachi	HD74LS38	
	Motorola	SN74LS38	
	National	DM74LS38	
	Raytheon	74LS38	
	Signetics	74LS38	
	TI	SN74LS38	
μPB74LS40	Fairchild	74LS40	
	Hitachi	HD74LS40	
	Motorola	SN74LS40	
	National	DM74LS40	
	Raytheon	74LS40	
	Signetics	74LS40	
	TI	SN74LS40	
μPB74LS42	Fairchild	74LS42	
	Hitachi	HD74LS42	
	Motorola	SN74LS42	
	National	DM74LS42	
	Raytheon	74LS42	
	Signetics	74LS42	
	TI	SN74LS42	
μPB74LS51	Fairchild	74LS51	
	Hitachi	HD74LS51	
	Motorola	SN74LS51	
	National	DM74LS51	
	Raytheon	74LS51	
	Signetics	74LS51	
	TI	SN74LS51	
μPB74LS54	Fairchild	74LS54	
	Hitachi	HD74LS54	
	Motorola	SN74LS54	
	National	DM74LS54	
	Raytheon	74LS54	
	Signetics	74LS54	
	TI	SN74LS54	
μPB74LS55	Fairchild	74LS55	
	Hitachi	HD74LS55	
	Motorola	SN74LS55	
	National	DM74LS55	
	Raytheon	74LS55	
	Signetics	74LS55	
	TI	SN74LS55	
μPB74LS74	Fairchild	74LS74	
	Hitachi	HD74LS74A	
	Motorola	SN74LS74A	
	National	DM74LS74	
	Raytheon	74LS74	
	Signetics	74LS74	
	TI	SN74LS74A	
μPB74LS86	Fairchild	74LS86	
	Hitachi	HD74LS86	
	Motorola	SN74LS86	
	Raytheon	74LS86	
	Signetics	74LS86	
	TI	SN74LS86	
μPB74S113	Motorola	SN74LS113A	
μPB7400	Fairchild	7400	
	Hitachi	HD7400	
	Mitsubishi	M53200	
	Motorola	MC7400	
	National	DM7400	
	Signetics	7400	
	TI	SN7400	
μPB7400	Toshiba	TC7400	
	TRW	7400	
μPB7402	Fairchild	7402	
	Hitachi	HD7402	
	Mitsubishi	M53202	
	Motorola	MC7402	
	National	DM7402	
	Signetics	7402	
	TI	SN7402	
	TRW	7402	
μPB7404	Fairchild	7404	
	Hitachi	HD7404	
	Mitsubishi	M53204	
	Motorola	MC7404	
	National	DM7404	
	Signetics	7404	
	TI	SN7404	
	Toshiba	TC7404	
	TRW	7404	
μPB7405	Fairchild	7405	
	Hitachi	HD7405	
	Mitsubishi	M53205	
	Motorola	MC7405	
	National	DM7405	
	Signetics	7405	
	TI	SN7405	
	TRW	7405	
μPB7410	Fairchild	7410	
	Hitachi	HD7410	
	Mitsubishi	M53210	
	Motorola	MC7410	
	National	DM7410	
	Signetics	7410	
	TI	SN7410	
		SN7427	
	Toshiba	TC7410	
	TRW	7410	
μPB74105	Fairchild	74105	
μPB74107	Fairchild	74107	
	Hitachi	HD74107	
	Mitsubishi	M53307	
	Motorola	MC74107	
	National	DM74107	
	Signetics	74107	
	TI	SN74107	
μPB74123	AMD	SN74123	
	Fairchild	74123	
	Mitsubishi	M53323	
	Motorola	MC74123	
	National	DM74123	
	Signetics	74123	
	TI	SN74123	
	TRW	74123	
μPB7413	Fairchild	7413	
	Mitsubishi	M53213	
	Motorola	MC7413	
	National	DM7413	
	Signetics	7413	
	TI	SN7413	
	TRW	7413	
μPB74141	Fairchild	74141	
	Motorola	MC74141	
	National	DM74141	
	TI	SN74141	
μPB74147	Hitachi	HD74147	
	Mitsubishi	M53347	
	National	DM74147	
	Signetics	74147	
	TI	SN74147	
μPB74148	Fairchild	9318	
	Hitachi	HD74148	
	Mitsubishi	M53348	
	National	DM74148	
	Signetics	74148	
	TI	SN74148	
μPB74150	Fairchild	74150	
	Hitachi	HD74150	
	Mitsubishi	M53350	
	Motorola	MC74150	
	National	DM74150	
	Signetics	74150	
	TI	SN74150	
	Toshiba	TC74	
	TRW	74150	
μPB74151	Fairchild	74151	
	Hitachi	HD74151	
μPB74151	Mitsubishi	M53351	
	Motorola	MC74151	
	National	DM74151	
	Signetics	74151	
	TI	SN74151	
	TRW	74151	
μPB74153	Fairchild	74153	
	Mitsubishi	M53353	
	Motorola	MC74153	
	National	DM74153	
	Signetics	74153	
	TI	SN74153	
	TRW	74153	
μPB74154	AMD	SN74154	
	Fairchild	74154	
	Mitsubishi	M53354	
	Motorola	MC74154	
	National	DM74154	
	Signetics	74154	
	TI	SN74154	
	TRW	74154	
μPB74155	Fairchild	74155	
	Mitsubishi	M53355	
	Motorola	MC74155	
	National	DM74155	
	Signetics	74155	
	TI	SN74155	
	TRW	74155	
μPB74156	Fairchild	74156	
	Hitachi	HD74156	
	Mitsubishi	M53356	
	Motorola	MC74156	
	National	DM74156	
	Signetics	74156	
	TI	SN74156	
	TRW	74156	
μPB74157	AMD	SN74157	
	Fairchild	74157	
	Hitachi	HD74157	
	Mitsubishi	M53357	
	Motorola	MC74157	
	National	DM74157	
	Signetics	74157	
	TI	SN74157	
μPB74161	AMD	SN74161	
	Fairchild	74161	
	Hitachi	HD74161	
	Mitsubishi	M53361	
	Motorola	MC74161	
	National	DM74161	
	Signetics	74161	
	TI	SN74161	
	TRW	74161	
μPB74164	AMD	74164	
	Fairchild	74164	
	Hitachi	HD74164	
	Mitsubishi	M53364	
	National	DM74164	
	Signetics	74164	
	TI	SN74164	
μPB74170	Fairchild	74170	
	Mitsubishi	M53370	
	National	DM74170	
	Signetics	74170	
	TI	SN74170	
μPB74175	AMD	SN74175	
	Fairchild	74175	
	Hitachi	HD74175	
	Mitsubishi	M53375	
	Motorola	MC74175	
	National	DM74175	
	Signetics	74175	
	TI	SN74175	
μPB74180	Fairchild	74180	
	Hitachi	HD74180	
	Mitsubishi	M53380	
	Motorola	MC74180	
	National	DM74180	
	Signetics	74180	
	TI	SN74180	
	TRW	74180	
μPB74181	AMD	SN74181	
	Fairchild	74181	
	Mitsubishi	M53381	
	Motorola	MC74181	
	National	DM74181	

♦ Discontinued

Bold face device numbers indicate manufacturers data is provided in the IC Master on the pages noted.

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Manufacturer Device	Replacement Source	Device	IC Master Page
μPB74181	Signetics	74181	
	TI	SN74181	
μPB74182	AMD	SN74182	
	Fairchild	74182	
	Mitsubishi	M53382	
	Motorola	MC74182	
	National	DM74182	
	Signetics	74182	
	TI	SN74182	
μPB74192	AMD	SN74192	
	Fairchild	74192	
	Mitsubishi	M53392	
	Motorola	MC74192	
	National	DM74192	
	Signetics	74192	
	TI	SN74192	
μPB74193	AMD	SN74193	
	Fairchild	74193	
	Mitsubishi	M53393	
	Motorola	MC74193	
	National	DM74193	
	Signetics	74193	
	TI	SN74193	
μPB74195	AMD	SN74195	
	Fairchild	74195	
	Motorola	MC74195	
	National	DM74195	
	Signetics	74195	
	TI	SN74195	
μPB74198	Fairchild	74198	
	Hitachi	HD74198	
	Mitsubishi	M53398	
	National	DM74198	
	Signetics	74198	
	TI	SN74198	
μPB7420	Fairchild	7420	
	Hitachi	HD7420	
	Mitsubishi	M53220	
	Motorola	MC7420	
	National	DM7420	
	Signetics	7420	
	TI	SN7420	
	Toshiba	TC7420	
	TRW	7420	
μPB74283	Fairchild	74283	
	Mitsubishi	M53483	
	TI	SN74283	
μPB7430	Fairchild	7430	
	Hitachi	HD7430	
	Mitsubishi	M53230	
	Motorola	MC7430	
	National	DM7430	
	Signetics	7430	
	TI	SN7430	
	TRW	7430	
μPB7437	Fairchild	7437	
	Mitsubishi	M53237	
	Motorola	MC7437	
	National	DM7437	
	Signetics	7437	
	TI	SN7437	
	TRW	7437	
μPB7438	Fairchild	7438	
	Mitsubishi	M53238	
	Motorola	MC7438	
	National	DM7438	
	Signetics	7438	
	TI	SN7438	
	TRW	7438	
μPB7440	Fairchild	7440	
	Hitachi	HD7440	
	Mitsubishi	M53240	
	Motorola	MC7440	
	National	DM7440	
	Signetics	7440	
	TI	SN7440	
	TRW	7440	
μPB7442	Fairchild	7442	
	Hitachi	HD7442	
	Mitsubishi	M53242	
	Motorola	MC7442	
	National	DM7442	
	Signetics	7442	
μPB7442	TI	SN7442	
μPB7445	Fairchild	7445	
	Mitsubishi	M53245	
	Motorola	MC7445	
	National	DM7445	
	Signetics	7445	
	TI	SN7445	
	TRW	7445	
μPB7447	Fairchild	7447	
	Mitsubishi	M53247	
	Motorola	MC7447	
	National	DM7447	
	Signetics	7447	
	TI	SN7447	
μPB7450	Fairchild	7450	
	Hitachi	HD7450	
	Mitsubishi	M53250	
	Motorola	MC7450	
	National	DM7450	
	Signetics	7450	
	TI	SN7450	
	TRW	7450	
μPB7451	Fairchild	7451	
	Hitachi	HD7451	
	Motorola	MC7451	
	National	DM7451	
	Signetics	7451	
	TI	SN7451	
	TRW	7451	
μPB7453	Fairchild	7453	
	Hitachi	HD7453	
	Mitsubishi	M53253	
	Motorola	MC7453	
	National	DM7453	
	Signetics	7453	
	TI	SN7453	
	TRW	7453	
μPB7454	Fairchild	7454	
	Hitachi	HD7454	
	Motorola	MC7454	
	National	DM7454	
	Signetics	7454	
	TI	SN7454	
	TRW	7454	
μPB7460	Fairchild	7460	
	Hitachi	HD7460	
	Mitsubishi	M53260	
	Motorola	MC7460	
	National	DM7460	
	Signetics	7460	
	TI	SN7460	
	TRW	7460	
μPB7473	Fairchild	7473	
	Mitsubishi	M53273	
	Motorola	MC7473	
	National	DM7473	
	Signetics	7473	
	TI	SN7473	
μPB7474	Fairchild	7474	
	Hitachi	HD7474	
	Mitsubishi	M53274	
	Motorola	MC7474	
	National	DM7474	
	Signetics	7474	
	TI	SN7474	
	TRW	7474	
μPB7476	Fairchild	7476	
	Mitsubishi	M53276	
	Motorola	MC7476	
	National	DM7476	
	Signetics	7476	
	TI	SN7476	
	TRW	7476	
μPB7480	Fairchild	7480	
	Mitsubishi	M53280	
	Motorola	MC7480	
	Signetics	7480	
	TI	SN7480	
μPB7485	Fairchild	7485	
	Hitachi	HD7485	
	Mitsubishi	M53285	
	Motorola	MC7485	
	National	DM7485	
	Signetics	7485	
	TI	SN7485	
	TRW	7485	
μPB7486	Fairchild	7486	
	Hitachi	HD7486	
	Mitsubishi	M53286	
	Motorola	MC7486	
	National	DM7486	
	Signetics	7486	
	TI	SN7486	
	TRW	7486	
μPB7491	Fairchild	7491	
	Mitsubishi	M53291	
	Motorola	MC7491	
	National	DM7491	
	Signetics	7491	
	TI	SN7491	
μPC151	Toshiba	TA7504	
μPC157	Toshiba	TA7506	
μPC255	Toshiba	TA7502	
μPD4001	Fairchild	F4001	
	Mitel	SIL4001	
	Motorola	MC14001	
	National	CD4001	
	RCA	CD4001	
	SGS	HBF4001	
	Solitron	CM4001	
	SSS	SCL4001	
	TI	TP4001	
	Toshiba	TC4001	
μPD4002	Fairchild	F4002	
	Mitel	SIL4002	
	Motorola	MC14002	
	National	CD4002	
	RCA	CD4002	
	SGS	HBF4002	
	Solitron	CM4002	
	SSS	SCL4002	
	TI	TP4002	
	Toshiba	TC4002	
μPD4011	Fairchild	F4011	
	Mitel	SIL4011	
	Motorola	MC14011	
	National	CD4011	
	RCA	CD4011	
	SGS	HBF4011	
	Solitron	CM4011	
	SSS	SCL4011	
	TI	TP4011	
	Toshiba	TC4011	
μPD4012	Fairchild	F4012	
	Mitel	SIL4012	
	Motorola	MC14012	
	National	CD4012	
	RCA	CD4012	
	SGS	HBF4012	
	Solitron	CM4012	
	SSS	SCL4012	
	TI	TP4012	
	Toshiba	TC4012	
μPD4013	Fairchild	F4013	
	Mitel	SIL4013	
	Motorola	MC14013	
	National	CD4013	
	RCA	CD4013	
	SGS	HBF4013	
	Solitron	CM4013	
	SSS	SCL4013	
	TI	TP4013	
	Toshiba	TC4013	
μPD4014	Fairchild	F4014	
	Mitel	SIL4014	
	Motorola	MC14014	
	National	CD4014	
	RCA	CD4014	
	SGS	HBF4014	
	Solitron	CM4014	
	SSS	SCL4014	
	TI	TP4014	
	Toshiba	TC4014	
μPD4015	Fairchild	F4015	
	Mitel	SIL4015	
	Motorola	MC14015	
	National	CD4015	
	RCA	CD4015	
	SGS	HBF4015	
	Solitron	CM4015	
	SSS	SCL4015	
	TI	TP4015	
μPD4015	Toshiba	TC4015	
μPD4017	Fairchild	F4017	
	Mitel	SIL4017	
	Motorola	MC14017	
	National	CD4017	
	RCA	CD4017	
	SGS	HBF4017	
	Solitron	CM4017	
	SSS	SCL4017	
	TI	TP4017	
	Toshiba	TC4017	
μPD4020	Fairchild	F4020	
	Mitel	SIL4020	
	Motorola	MC14020	
	National	CD4020	
	RCA	CD4020	
	SGS	HBF4020	
	Solitron	CM4020	
	SSS	SCL4020	
	TI	TP4020	
	Toshiba	TC4020	
μPD4021	Fairchild	F4021	
	Mitel	SIL4021	
	Motorola	MC14021	
	National	CD4021	
	RCA	CD4021	
	Solitron	CM4021	
	SSS	SCL4021	
	TI	TP4021	
	Toshiba	TC4021	
μPD4023	Fairchild	F4023	
	Mitel	SIL4023	
	Motorola	MC14023	
	National	CD4023	
	RCA	CD4023	
	SGS	HBF4023	
	Solitron	CM4023	
	SSS	SCL4023	
	TI	TP4023	
	Toshiba	TC4023	
μPD4025	Fairchild	F4025	
	Mitel	SIL4025	
	Motorola	MC14025	
	National	CD4025	
	RCA	CD4025	
	SGS	HBF4025	
	Solitron	CM4025	
	SSS	SCL4025	
	TI	TP4025	
	Toshiba	TC4025	
μPD4027	Fairchild	F4027	
	Mitel	SIL4027	
	Motorola	MC14027	
	National	CD4027	
	RCA	CD4027	
	SGS	HBF4027	
	Solitron	CM4027	
	SSS	SCL4027	
	TI	TP4027	
	Toshiba	TC4027	
μPD4028	Fairchild	F4028	
	Mitel	SIL4028	
	Motorola	MC14028	
	National	CD4028	
	RCA	CD4028	
	SGS	HBF4028	
	Solitron	CM4028	
	SSS	SCL4028	
	TI	TP4028	
	Toshiba	TC4028	
μPD4029	Fairchild	F4029	
	Mitel	SIL4029	
	National	CD4029	
	RCA	CD4029	
	SGS	HBF4029	
	Solitron	CM4029	
	SSS	SCL4029	
	TI	TP4029	
	Toshiba	TC4029	
μPD4030	Fairchild	F4030	
	Mitel	SIL4030	
	National	CD4030	
	RCA	CD4030	
	SGS	HBF4030	
	Solitron	CM4030	
	SSS	SCL4030	

› Discontinued

The manufacturers report their devices can be used as direct replacements.
Performance details often differ, so compare the specifications considering your requirements.

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Manufacturer Device	Replacement Source	Device	IC Master Page
μPD4030	TI	TP4030	
	Toshiba	TC4030	
μPD4035	Fairchild	F4035	
	Mitel	SIL4035	
	Motorola	MC14035	
	National	CD4035	
	RCA	CD4035	
	SGS	HBF4035	
	Solitron	CM4035	
	SSS	SCL4035	
	TI	TP4035	
	Toshiba	TC4035	
μPD4040	Fairchild	F4040	
	Mitel	SIL4040	
	National	CD4040	
	RCA	CD4040	
	Solitron	CM4040	
	SSS	SCL4040	
	TI	TP4040	
	Toshiba	TC4040	
μPD4042	Fairchild	F4042	
	Mitel	SIL4042	
	Motorola	MC14042	
	National	CD4042	
	RCA	CD4042	
	SGS	HBF4042	
	Solitron	CM4042	
	SSS	SCL4042	
	TI	TP4042	
	Toshiba	TC4042	
μPD4043	Fairchild	F4043	
	Mitel	SIL4043	
	Motorola	MC14043	
	National	CD4043	
	RCA	CD4043	
	Solitron	CM4043	
	SSS	SCL4043	
	TI	TP4043	
	Toshiba	TC4043	
μPD4044	Fairchild	F4044	
	Mitel	SIL4044	
	Motorola	MC14044	
	National	CD4044	
	RCA	CD4044	
	Solitron	CM4044	
	SSS	SCL4044	
	TI	TP4044	
	Toshiba	TC4044	
μPD4049	Fairchild	F4049	
	Mitel	SIL4049	
	Motorola	MC14049	
	National	CD4049	
	RCA	CD4049	
	SGS	HBF4049	
	Solitron	CM4049	
	SSS	SCL4049	
	TI	TP4049	
	Toshiba	TC4049	
μPD4050	Fairchild	F4050	
	Mitel	SIL4050	
	Motorola	MC14050	
	National	CD4050	
	RCA	CD4050	
	SGS	HBF4050	
	Solitron	CM4050	
	SSS	SCL4050	
	TI	TP4050	
	Toshiba	TC4050	
μPD4063	RCA	CD4063	
μPD4066	Fairchild	F4066	
	Mitel	SIL4066	
	Motorola	MC14066	
	National	**CD4066**	**1076**
	RCA	CD4066	
	SGS	HBF4066	
	Signetics	N4066	
	Solitron	CM4066	
	SSS	SCL4066	
	Toshiba	TC4066	
μPD4069	Fairchild	F4069	
	Harris	HD74C04	
	Mitel	SIL4069	
	Motorola	MC14069	
μPD4069	National	CD4069	
		MM74C04	
	RCA	CD4069	
	Solitron	CM4069	
	SSS	SCL4069	
	TI	TP4069	
	Toshiba	TC4069	
μPD4071	Fairchild	F4071	
	Mitel	SIL4071	
	Motorola	MC14071	
	National	CD4071	
	RCA	CD4071	
	Solitron	CM4071	
	SSS	SCL4071	
	TI	TP4071	
	Toshiba	TC4071	
μPD4081	Fairchild	F4081	
	Mitel	SIL4081	
	Motorola	MC14081	
	National	CD4081	
	RCA	CD4081	
	Solitron	CM4081	
	SSS	SCL4081	
	TI	TP4081	
	Toshiba	TC4081	
μPD4512	Fairchild	F4512	
	Mitel	SIL4512	
	Motorola	MC14512	
	National	CD4512	
	SSS	SCL4512	
	TI	TP4512	
	Toshiba	TC4512	
μPD4519	Fairchild	F4519	
	Motorola	MC14519	
	National	CD4519	
	RCA	CD4019	
	TI	TP4519	
μPD4520	Fairchild	F4520	
	Mitel	SIL4520	
	Motorola	MC14520	
	National	CD4520	
	RCA	CD4520	
	Solitron	CM4520	
	SSS	SCL4520	
	TI	TP4520	
	Toshiba	TC4520	
μPD4528	Fairchild	F4528	
	Motorola	MC14528	
	National	CD4528	
	RCA	CD4528	
	SSS	SCL4528	
	Toshiba	TC4528	
μPD4539	Fairchild	F4539	
	Motorola	MC14539	
	Toshiba	TC4539	
μPD4556	Fairchild	F4556	
	Motorola	MC14556	
	RCA	CD4556	
	SSS	SCL4556	

NEC Microcomputers

Manufacturer Device	Replacement Source	Device	IC Master Page
μPB10148	Motorola	MCM10148	
♦μPB2089	AMD	AM27S02	
		SN7489	
		3101	
	Fairchild	74S289	
		7489	
	National	DM7489	
		MM74S289	
	Signetics	**N3101A**	**1678**
		74S89	**1679**
	TI	SN74S289	
		SN7489	
♦μPB2200	AMD	AM27LS00	
	MMI	6531	
	Signetics	**N82S17**	**1678**
		74S200	**1678**
	TI	SN74S301	
♦μPB2202	**Signetics**	**74S201**	**1678**
	TI	SN74S201	
♦μPB2205	AMD	93415M	
	Fairchild	**93415**	**1240**
	National	DM93415	
	TI	SN74S314	
♦μPB2206	AMD	AM27LS01	
	Fairchild	93411	
	MMI	6530	
	Signetics	**N82S16**	**1678**
♦μPB2289	AMD	SN74S289	
μPB2902	Motorola	MC2902	
μPB2911	National	IDM2911	
	Raytheon	AM2911	
μPB403	**Fairchild**	**93417**	**1258**
	Harris	**HM7610**	
			1284,1292
		HPROM-1024A	
	Intersil	IM5603	
	MMI	**6300-1**	**1449**
	National	DM74S387	
		DM7535	
	Signetics	**N82S126**	**1680**
	TI	**SN74S387**	**1708**
μPB405	**Fairchild**	**93438**	**1262**
	Harris	**HM7640**	
			1284,1304
	Intel	3604A	
	Intersil	IM5605	
	MMI	**6340-1**	**1449**
		6348-1	**1449**
	National	DM77S295	
	Signetics	**N82S140**	**1680**
	TI	**SN74S475**	**1708**
μPB406	**Fairchild**	**93452**	**1264**
	Harris	**HM7642**	
			1284,1308
	Intel	3605A	
	MMI	**6352-1**	**1449**
	National	DM74S572	
	Signetics	**N82S136**	**1680**
♦μPB408	AMD	AM27S80	
	Intel	3608	
	MMI	**6380-1**	**1449**
μPB410	EMM/Semi	4200	
μPB425	**Fairchild**	**93448**	**1262**
	Harris	**HM7641**	
			1284,1304
	Intersil	IM5625	
	MMI	**6341-1**	**1449**
		6349-1	**1449**
	National	DM77S296	
	Signetics	**N82S141**	**1680**
	TI	SN74S44	
μPB426	**Fairchild**	**93453**	**1264**
	Harris	**HM7643**	
			1284,1308
	MMI	**6353-1**	**1449**
	National	DM74S573	
	Signetics	**N82S137**	**1680**
♦μPB428	AMD	AM27S81	
	Intel	3628	
	MMI	**6381-1**	**1449**
μPB8212	AMD	8212	
	Intel	8212	
	National	DP8212	
	TI	SN74S412	
μPB8214	AMD	8214	
	Intel	8214	
μPB8216	AMD	8216	
	Intel	8216	
	National	DP8216	
μPB8224	AMD	8224	
	Intel	8224	
	National	DP8224	
	TI	SN74LS424	
μPB8226	AMD	8226	
	Intel	8226	
	National	DP8226	
μPB8228	AMD	8228	
	Intel	8228	
	National	DP8228	
	TI	SN74S428	
μPB8238	AMD	8238	
	Intel	8238	
	National	DP8238	
	TI	SN74S438	
μPD2101	AMD	2101	
		9101	
	Fairchild	3538	
	Intel	2101	
		8101	
μPD2101	National	MM2101	
	Signetics	2101	
μPD2102	AMD	2102	
		9102	
	Fairchild	**2102**	**1275**
	Intel	2102	
		8102	
	National	MM2102A	
	Signetics	2102	
μPD2111	AMD	2111	
		9111	
	Intel	2111	
		8111	
	Motorola	MCM2111	
		MCM68111	
	National	MM2111	
	Signetics	2111	
μPD2114	AMD	9114	
		9124	
	AMI	**S2114**	**1196**
	Fairchild	**2114**	**1281**
	Fujitsu	MB8114	
	Intel	2114	
	Intersil	7114	
	Rockwell	R2114	
	TI	TMS4045	
♦μPD2308	AMD	9208	
	Fairchild	3508	
	Mostek	MK30000	
	TI	TMS4700	
♦μPD2316	Intel	2316	
		2616	
		8316	
	Mostek	MK34000	
	Rockwell	R2316	
	Signetics	2316	
μPD2316A	**AMI**	**S6831A**	
			1215,1806
♦μPD2316A	Intel	4316	
	Mostek	MK31000	
	National	MM2316A	
μPD2316E	AMD	9216	
	AMI	**S4216B**	**1209**
		S6831B	
			1215,1806
	Mostek	MK34000	
	Motorola	MCM68317	
μPD2332	Mostek	MK32000	
	TI	TMS4732	
μPD2716	Fujitsu	MBM2716	
μPD410	EMM/Semi	4200	
		4202	
μPD4104	Mostek	MK4104	
μPD411	AMD	9060	
		9107	
	Fujitsu	MB8107	
	Intel	2107	
	National	MM4280	
		MM5280A	
		MM5281	
	TI	TMS4060	
μPD414	Fairchild	M4027	
♦μPD414	Fairchild	M4027	
		4096	
	Fujitsu	MB8227	
	Intel	2104	
	Mostek	MK4027	
		MK4096	
	Motorola	**MCM4027**	**1522**
		MCM4096	
	TI	TMS4027	
μPD416	AMD	9016	
	Fairchild	**F16K**	**1272**
	Fujitsu	MB8116	
	Intel	2116	
	Intersil	7116	
	Mostek	MK4116	
	Motorola	μPD416	
		MCM4116	**1505**
	TI	TMS4116	
	Zilog	Z6116	
♦μPD418	AMD	9050	
	TI	TMS4050	
		TMS4051	
μPD5101	**AMI**	**S5101**	**1206**
	Harris	**HM6501**	**1356**

♦ Discontinued

Bold face device numbers indicate manufacturers data is provided in the IC Master on the pages noted.

NEC Microcomputers (cont'd)

Manufacturer Device	Replacement Source	Device	IC Master Page
µPD5101	Intel	5101	
	National	MM74C920	
µPD6508	**AMI**	**S6508**	**1207**
	Harris	**HM6508**	**1366**
	Intersil	IM6508	
µPD8035	**Intel**	**8035**	**1934**
µPD8048	**Intel**	**8048**	**1934**
µPD8080A	AMD	9080A	
	TI	TMS8080A	
µPD8080AF	Intel	8080A	
	National	**INS8080A**	**238**
µPD8085	Intel	8085	
µPD8085A	AMD	8085	
		8085A	
µPD8155	AMD	8155	
	Intel	**8155**	**1945**
µPD8156	AMD	8156	
µPD8251	AMD	8251	
	Intel	8251	
	National	INS8251	
µPD8253	Intel	8253	
µPD8255	AMD	8255	
	Intel	8255	
	National	INS8255	
µPD8255A	AMD	8255A	
µPD8257	AMD	8257	
	Intel	8257	
µPD8259	Intel	8259	
µPD8355	AMD	8355	
	Intel	**8355**	**1946**
µPD8748	**Intel**	**8748**	**1934**
µPD8755	Intel	8755	
5101	SSS	SCM5101	

Nitron

♦NC1181	AMI	S2567	
♦NC1182	AMI	S2566	
NC1183	National	MM5555	
NC1184	National	MM5556	
NC6560	Motorola	MCM6560	
NC6561	Motorola	MCM6561	
NC6570	Motorola	MCM6570	
NC6571	Motorola	MCM6571	
NC6572	Motorola	MCM6572	
NC6580	Motorola	MCM6580	
NC6581	Motorola	MCM6581	
NC6583	Motorola	MCM6583	
NC6590	Motorola	MCM6590	
♦NC6832	Motorola	MCM6832	

Nortec Electronics

2222	AMI	S2222	
6002	TI	TMS4062	
		TMS4732	
6003	TI	TMS4063	
7001	RCA	MW7001	

Panasonic

AN332	Mitsubishi	M5188	
MN1001	Fujitsu	MB8107	

Plessey Semiconductors

MP3409	TI	TMS3404	
MP3417	TI	TMS3417	
SL3045	RCA	CA3045	
	Sprague	ULS-2045	
SL3046	RCA	CA3046	
	Sprague	ULN-2046	
SL3054	Sprague	ULN-2054	
SL3081	Sprague	ULN-2081	
SL3082	Sprague	ULN-2082	
SL3083	Signetics	CA3083	
	Sprague	ULN-2083	
SL3086	RCA	CA3086	
	Sprague	ULN-2086	
SL3183	Signetics	CA3183	
SP1012	Motorola	MC1012	
SP1014	Motorola	MC1014	
SP1015	Motorola	MC1015	
SP1016	Motorola	MC1016	
SP1020	Motorola	MC1020	
SP1023	Motorola	MC1023	
SP1648	Motorola	MC1648	
SP1660	Motorola	MC1660	
SP1662	Motorola	MC1662	
SP1664	Motorola	MC1664	
SP1666	Motorola	MC1666	
SP1668	Motorola	MC1668	
SP1670	Fairchild	11C70	
	Motorola	MC1670	
SP1690	Motorola	MC1690	
SP1692	Motorola	MC1692	
SP8616	Fairchild	11C05C	
SP8640	Fairchild	95H90	
SP8641	Fairchild	95H90	
SP8685	Fairchild	11C90	

Precision Monolithics, Inc.

DAC-01	Micro Power	MP5520	
DAC-01C	NEC America	µPC603	
DAC-02CC	NEC America	µPC610	
DAC-08	AMD	DAC-08	
	Datel	DAC-08	
	Fairchild	µA0801	
	Motorola	DAC-08	
	NEC America	DAC-08	
		DAC08D	
	Raytheon	DAC-08	
	Signetics	DAC-08	
		NE5007	
		NE5008	
		NE5009	
		SE5008	
		SE5009	
DAC-08E	NEC America	DAC08C	
OP-01	Micro Power	MP5501	
		MP7621	
OP-07	AD	517	
	Fairchild	µA714	
PM1458	Exar	XR1458	
PM155	AMD	LF155	
	Fairchild	µAF155	
	Intersil	LF155	
	Motorola	LF155	
	National	**LF155**	**1035**
	Raytheon	LF155	
	Signetics	LF155	
	TI	LF155	
PM1558	Exar	XR1558	
PM156	AMD	LF156	
	Fairchild	µAF156	
	Intersil	LF156	
	Motorola	LF156	
	National	**LF156**	**1035**
	Raytheon	LF156	
	Signetics	LF156	
	TI	LF156	
PM157	AMD	LF157	
	Fairchild	µAF157	
	Intersil	LF157	
	Motorola	LF157	
	National	**LF157**	**1035**
	Raytheon	LF157	
	Signetics	LF157	
	TI	LF157	
PM255	AMD	LF255	
	Fairchild	µAF255	
	Intersil	LF255	
	Motorola	LF255	
	National	LF255	
	Raytheon	LF255	
	Signetics	LF255	
	TI	LF255	
PM256	AMD	LF256	
	Fairchild	µAF256	
	Intersil	LF256	
	Motorola	LF256	
	National	LF256	
	Raytheon	LF256	
PM256	Signetics	LF256	
	TI	LF256	
PM257	AMD	LF257	
	Fairchild	µAF257	
	Intersil	LF257	
	Motorola	LF257	
	National	LF257	
	Raytheon	LF257	
	Signetics	LF257	
	TI	LF257	
PM355	AMD	LF355	
	Fairchild	µAF355	
	Intersil	LF355	
	Motorola	LF355	
	National	LF355	
	Raytheon	LF355	
	Signetics	LF355	
	TI	LF355	
PM356	AMD	LF356	
	Fairchild	µAF356	
	Intersil	LF356	
	Motorola	LF356	
	National	**LF356**	**1035,1073**
	Raytheon	LF356	
	Signetics	LF356	
	TI	LF356	
PM357	AMD	LF357	
	Fairchild	µAF357	
	Intersil	LF357	
	Motorola	LF357	
	National	LF357	
	Raytheon	LF357	
	Signetics	LF357	
	TI	LF357	
PM4136	Exar	XR4136	
REF-01	AD	AD581	
♦SSS108	RCA	CA108	
SSS1408	AD	AD1408	
	AMD	AM1408	
		SSS1408	
	Datel	**DAC-IC8B**	**671**
	Motorola	MC1408	
SSS1408A	AMD	SSS1408A	
SSS1458	Exar	XR1458	
	Motorola	MC1458	
	RCA	SSS1458	
SSS1508	AMD	SSS1508	
	Motorola	MC1508	
SSS1558	Exar	XR1558	
	Motorola	MC1558	
	RCA	SSS1558	
♦SSS208	RCA	CA208	
♦SSS308	RCA	CA308	
SSS741	Motorola	MC1741	
	RCA	CA741	
SSS747	AMD	SSS747	
	Motorola	MC1747	
	RCA	CA747	
SS1508	**Datel**	**DAC-IC8BM**	**671**
0P-05CJ	NEC America	µPC254	
0P-07	AD	AD517	

Raytheon Semiconductor

AM2901	AMD	AM2901	
	Motorola	MC2901	
AM2901A	NEC Micro	µPB2901A	
	OEI	µPB2901A	
AM2902	AMD	AM2902	
	Motorola	MC2902	
	NEC Micro	µPB2902A	
AM2905	AMD	AM2905	
	Motorola	MC2905	
	NEC Micro	µPB2905A	
AM2906	AMD	AM2906	
	Motorola	MC2906	
	NEC Micro	µPB2906A	
AM2907	AMD	AM2907	
	Motorola	MC2907	
	NEC Micro	µPB2907A	
AM2909	AMD	AM2909	
	NEC Micro	µPB2909A	
AM2911	AMD	AM2911	
	Motorola	MC2911	
	NEC Micro	µPB2911A	
AM2918	AMD	AM2918	
	NEC Micro	µPB2918A	
HA4741	Harris	HA-4741	
LF155	AMD	LF155	
	Fairchild	µAF155	
	Intersil	LF155	
	Motorola	LF155	
	National	**LF155**	**1035**
	PMI	PM155	
	Signetics	LF155	
	TI	LF155	
LF156	AMD	LF156	
	Fairchild	µAF156	
	Intersil	LF156	
	Motorola	LF156	
	National	**LF156**	**1035**
	PMI	PM156	
	Signetics	LF156	
	TI	LF156	
LF157	AMD	LF157	
	Fairchild	µAF157	
	Intersil	LF157	
	Motorola	LF157	
	National	**LF157**	**1035**
	PMI	PM157	
	Signetics	LF157	
	TI	LF157	
LF255	AMD	LF255	
	Fairchild	µAF255	
	Intersil	LF255	
	Motorola	LF255	
	National	LF255	
	PMI	PM255	
	Signetics	LF255	
	TI	LF255	
LF256	AMD	LF256	
	Fairchild	µAF256	
	Intersil	LF256	
	Motorola	LF256	
	National	LF256	
	PMI	PM256	
	Signetics	LF256	
	TI	LF256	
LF257	AMD	LF257	
	Fairchild	µAF257	
	Intersil	LF257	
	Motorola	LF257	
	National	LF257	
	PMI	PM257	
	Signetics	LF257	
	TI	LF257	
LF355	AMD	LF355	
	Fairchild	µAF355	
	Intersil	LF355	
	Motorola	LF355	
	National	LF355	
	PMI	PM355	
	Signetics	LF355	
	TI	LF355	
LF356	AMD	LF356	
	Fairchild	µAF356	
	Intersil	LF356	
	Motorola	LF356	
	National	**LF356**	**1035,1073**
	PMI	PM356	
	Signetics	LF356	
	TI	LF356	
LF357	AMD	LF357	
	Fairchild	µAF357	
	Intersil	LF357	
	Motorola	LF357	
	National	LF357	
	PMI	PM357	
	Signetics	LF357	
	TI	LF357	
LM101	AMD	LM101	
	Intersil	LM101	
	Motorola	LM101	
	National	**LM101**	**1035**
	RCA	CA101	
	Signetics	LM101	
	Silicon G	SG101	
	TI	LM101	
LM104	Motorola	LM104	
	Silicon G	SG104	
	TI	LM104	

♦ Discontinued

The manufacturers report their devices can be used as direct replacements.
Performance details often differ, so compare the specifications considering your requirements.

Raytheon Semiconductor (cont'd)

Manufacturer Device	Replacement Source	Device	IC Master Page
LM105	AMD	LM105	
	Intersil	LM105	
	Motorola	LM105	
	National	LM105	
	Silicon G	SG105	
	TI	LM105	
LM106	AMD	LM106	
	TI	LM106	
LM107	AMD	LM107	
	Intersil	LM107	
	Motorola	LM107	
	National	LM107	
	RCA	CA107	
	Signetics	LM107	
	Silicon G	SG107	
	TI	LM107	
LM108	AMD	LM108	
	Intersil	LM108	
	Motorola	LM108	
	National	**LM108**	**1035**
	PMI	OP-08	
		PM108	
	RCA	CA108	
	Signetics	LM108	
	Silicon G	SG108	
LM109	Motorola	LM109	
	National	LM109	
	Signetics	LM109	
	Silicon G	SG109	
	TI	LM109	
LM111	AMD	LM111	
	Intersil	LM111	
	Motorola	LM111	
	National	LM111	
	RCA	CA111	
	Signetics	LM111	
	Silicon G	SG111	
	TI	LM111	
LM112	AMD	LM112	
LM118	AMD	LM118	
	TI	LM118	
LM124	Motorola	LM124	
	National	LM104	
	Silicon G	SG124	
	TI	LM124	
LM139	Motorola	LM139	
	Silicon G	SG139	
	TI	LM139	
LM148	AMD	LM148	
	Exar	XR4741	
LM201	AMD	LM201	
	Intersil	LM201	
	Motorola	LM201	
	National	LM201	
	RCA	CA201	
	Silicon G	SG201	
	TI	LM201	
LM204	Motorola	LM204	
	National	LM204	
	Silicon G	SG204	
	TI	LM204	
LM205	AMD	LM205	
	Intersil	LM205	
	Motorola	LM205	
	National	LM205	
	Silicon G	SG205	
	TI	LM205	
LM207	AMD	LM207	
	Intersil	LM207	
	Motorola	LM207	
	National	LM207	
	RCA	CA207	
	Silicon G	SG207	
	TI	LM207	
LM208	AMD	LM208	
	Intersil	LM208	
	Motorola	LM208	
	PMI	OP-08	
		PM208	
	RCA	CA208	
	Silicon G	SG208	
LM209	National	LM209	
LM209	Signetics	LM209	
	Silicon G	SG209	
LM211	AMD	LM211	
	Intersil	LM211	
	Motorola	LM211	
	National	LM211	
	RCA	CA211	
	Signetics	LM211	
	Silicon G	SG211	
	TI	LM211	
LM216	AMD	LM216	
LM224	Motorola	LM224	
	RCA	CA224	
	Silicon G	SG224	
	TI	LM224	
LM239	Motorola	LM239	
	Silicon G	SG239	
	TI	LM239	
LM248	AMD	LM248	
	Exar	XR4741	
LM2900	National	LM2900	
LM2902	Motorola	LM2902	
	National	LM2902	
	TI	LM2902	
LM301	AMD	LM301	
	Intersil	LM301	
	Motorola	LM301	
	National	LM301	
	RCA	CA301	
	Signetics	LM301	
	Silicon G	SG301	
	TI	LM301	
LM304	Motorola	LM304	
	National	LM304	
	Silicon G	SG304	
	TI	LM304	
LM305	AMD	LM305	
	Intersil	LM305	
	Motorola	LM305	
	National	LM305	
	Silicon G	SG305	
	TI	LM305	
LM306	AMD	LM306	
	TI	LM306	
LM307	AMD	LM307	
	Intersil	LM307	
	Motorola	LM307	
	National	LM307	
	RCA	CA307	
	Signetics	LM307	
	Silicon G	SG307	
	TI	LM307	
LM308	AMD	LM308	
	Intersil	LM308	
	Motorola	LM308	
	PMI	OP-08	
		PM308	
	RCA	CA308	
	Signetics	LM308	
	Silicon G	SG308	
LM309	Motorola	LM309	
	National	LM309	
	Signetics	LM309	
	Silicon G	SG309	
	TI	LM309	
LM311	AMD	LM311	
	Intersil	LM311	
	Motorola	LM311	
	National	LM311	
	RCA	CA311	
	Signetics	LM311	
	Silicon G	SG311	
	TI	LM311	
LM312	AMD	LM312	
LM316	AMD	LM316	
LM318	AMD	LM318	
	TI	LM318	
LM324	Motorola	LM324	
	RCA	CA324	
	Silicon G	SG324	
	TI	LM324	
LM339	Motorola	LM339	
	RCA	CA339	
	Silicon G	SG339	
LM348	AMD	LM348	
	Exar	XR4741	
RC10144	Fairchild	F10410	
	Fujitsu	MBM10410	
	Motorola	MC10144	
	NEC America	μPB10144	
	Signetics	10144	
	TI	SN10144	
RC1414	Motorola	MC1414	
	TI	TL514	
RC1437	Motorola	MC1437	
RC1458	Exar	XR1458	
	Harris	**HA-2655**	**986**
	Motorola	MC1458	
	PMI	OP-14	
		SSS1458	
	RCA	CA1458	
	Signetics	MC1458	
	Silicon G	SG1458	
	TI	MC1458	
RC1488	Exar	XR1488	
	Motorola	MC1488	
	Signetics	MC1488	
	Silicon G	SG1488	
	TI	SN75188	
RC1489	Exar	XR1489	
	Motorola	MC1489	
	Signetics	MC1489	
	Silicon G	SG1489	
	TI	SN75189	
RC1489A	Signetics	MC1489A	
	Silicon G	SG1489A	
RC1556	Motorola	MC1456	
	Signetics	MC1456	
	Silicon G	SG1456	
RC1558	Motorola	RC1558	
	Silicon G	SG1558	
RC2207	**Exar**	**XR2207**	**925**
RC2211	**Exar**	**XR2211**	**922**
RC2567	Exar	XR2567	
		XR2567C	
RC3302	Motorola	MC3302	
	Silicon G	SG3302	
	TI	LM3302	
RC3403	Exar	XR3403	
		XR3403C	
	Fairchild	μA3403	
	Motorola	MC3403	
RC4136	Exar	XR4136	
		XR4212	
	Fairchild	μA4136	
	PMI	OP-09	
		PM4136	
	Silicon G	SG4136	
	Sprague	ULN-4136	
	TI	RC4136	
RC414	TI	TL514	
RC4151	TI	XR4151	
RC4152	TI	XR4152	
RC4156	TI	XR4156	
RC4194	Exar	XR4194	
	Silicon G	SG4194	
RC4236	Sprague	ULN-4236	
RC4336	Sprague	ULN-4336	
RC4436	Sprague	ULN-4436	
RC4444	Motorola	MC3416	
RC4531	Signetics	NE531	
RC4558	Exar	XR4558	
	Fairchild	μA4558	
	Motorola	MC4558	
	TI	RC4558	
RC4739	Exar	XR4739	
RC5330	Fairchild	93411	
RC5500	TI	SN74S314	
RC555	Cherry	CS555	
	Exar	XR555	
	Fairchild	μA555	
	Intersil	NE555	
	Motorola	MC1455	
	RCA	CA555	
	Signetics	NE555	
	Silicon G	SG555	
	TI	NE555	
RC556	Exar	XR556	
	Fairchild	μA556	
	Motorola	MC3456	
	Signetics	NE556	
	Silicon G	SG556	
RC556	TI	NE556	
RC592	Motorola	NE592	
	Signetics	NE592	
RC702	Motorola	MC1712	
	TI	μA702	
RC709	Motorola	MC1709	
	Signetics	μA709	
	TI	μA709	
RC710	Motorola	MC1710	
	Signetics	μA710	
	Silicon G	SG710	
	TI	TL710	
RC711	Motorola	MC1711	
	Signetics	μA711	
	Silicon G	SG711	
	TI	μA711	
RC723	AMD	723	
	Intersil	723	
	Motorola	MC1723	
	National	LM723	
	RCA	CA723	
	Signetics	μA723	
	Silicon G	SG723	
	TI	μA723	
RC725	AMD	725	
	PMI	PM725	
		SSS725	
RC733	AMD	733	
	Fairchild	μA733	
	Motorola	MC1733	
	Signetics	μA733	
	Silicon G	SG733	
	TI	μA733	
RC741	AMD	741	
	Intersil	741	
	Motorola	MC1741	
	PMI	OP-02	
		SSS741	
	RCA	CA741	
	Signetics	μA741	
	Silicon G	SG741	
	Sprague	ULN-2151	
	TI	μA741	
RC747	AMD	747	
	Motorola	MC1747	
	PMI	OP-04	
		SSS747	
	RCA	CA747	
	Signetics	μA747	
	Silicon G	SG747	
	TI	μA747	
RC748	AMD	748	
	Intersil	748	
	Motorola	MC1748	
	RCA	CA748	
	Signetics	μA748	
	Silicon G	SG748	
	TI	μA748	
RC75107	Fairchild	75107	
	Motorola	MC75107	
	TI	SN75107	
RC75108	Fairchild	75108	
	Motorola	MC75108	
	TI	SN75108	
RC75109	Fairchild	75109	
	TI	SN75109	
RC75110	Fairchild	75110	
	Motorola	MC75110	
	TI	SN75110	
♦RC7520	Signetics	7520	
	Silicon G	SG7520	
	TI	SN7520	
♦RC7521	Signetics	7521	
	Silicon G	SG7521	
♦RC7522	Motorola	MC7522	
	Signetics	7522	
	Silicon G	SG7522	
	TI	SN7522	
RC7523	Motorola	MC7523	
	Signetics	7523	
	Silicon G	SG7523	
RC75235	TI	SN75235	
♦RC7524	Motorola	MC7524	
	Signetics	7524	
	Silicon G	SG7524	
	TI	SN7524	

♦ Discontinued

Bold face device numbers indicate manufacturers data is provided in the IC Master on the pages noted.

Manufacturer Device	Replacement Source	Device	IC Master Page
Raytheon Semiconductor (cont'd)			
♦RC7525	Motorola	MC7525	
	Signetics	7525	
	Silicon G	SG7525	
RC7528	Fairchild	7528	
	Silicon G	SG7528	
	TI	SN7528	
RC7529	Silicon G	SG7529	
RC75325	Fairchild	75325	
	Motorola	MC75325	
	Silicon G	SG75325	
RC8T09	Signetics	8T09	
RC8T10	Signetics	8T10	
RC8200	Signetics	N8200	
RC8201	Signetics	N8201	
RC8202	Signetics	N8202	
RC8203	Signetics	N8203	
RC8225	Fairchild	74S189	
	Signetics	N8225	
	TI	SN74S189	
		SN74S289	
RC8230	Signetics	N8230	
RC8231	Signetics	N8231	
RC8233	Signetics	N8233	
RC8234	Signetics	N8234	
RC8241	Signetics	N8241	
RC8242	Signetics	N8242	
RC8243	Signetics	N8243	
RC8250	Signetics	N8250	
RC8251	Signetics	N8251	
RC8252	Signetics	N8252	
RC8260	Signetics	N8260	
RC8261	Signetics	N8261	
RC8263	Signetics	N8263	
RC8264	Signetics	N8264	
RC8266	Signetics	N8266	
RC8267	Signetics	N8267	
RC8270	Fairchild	74178	
	Signetics	N8270	
	TI	SN74178	
RC8271	Fairchild	74179	
	Signetics	N8271	
	TI	SN74179	
RC8273	Signetics	N8273	
RC8274	Signetics	N8274	
RC8280	Fairchild	74176	
	Signetics	N8280	
	TI	SN74176	
RC8281	Signetics	N8281	
RC8290	Fairchild	74196	
	Signetics	N8290	
		8290	
	TI	SN74196	
RC8291	Fairchild	74197	
	Signetics	N8291	
	TI	SN74197	
RC930	Fairchild	930	
	Motorola	MC830	
	TI	SN15830	
RC932	Fairchild	932	
	Motorola	MC832	
	TI	SN15832	
RC933	Fairchild	933	
	Motorola	MC933	
	TI	SN15833	
RC934	Motorola	MC934	
	TI	SN15834	
RC935	Fairchild	935	
	Motorola	MC835	
	TI	SN15835	
RC936	Fairchild	936	
	Motorola	MC836	
RC937	Fairchild	937	
	Motorola	MC837	
	TI	SN15837	
RC940	Motorola	MC840	
RC941	Motorola	MC841	
RC944	Fairchild	944	
	Motorola	MC844	
	TI	SN15844	
RC945	Fairchild	945	
	Motorola	MC845	
	TI	SN15845	
RC946	Fairchild	946	
	Motorola	MC846	
	TI	SN15846	
RC948	Fairchild	948	
	Motorola	MC848	
	TI	SN15848	
RC949	Fairchild	949	
	Motorola	MC849	
	TI	SN15849	
RC950	Fairchild	950	
	Motorola	MC850	
	TI	SN15850	
RC951	Fairchild	951	
	Motorola	MC851	
	TI	SN15851	
RC957	Fairchild	9157	
	Motorola	MC857	
	TI	SN15857	
RC958	Fairchild	9158	
	Motorola	MC858	
	TI	SN15858	
RC961	Fairchild	961	
	Motorola	MC861	
	TI	SN15861	
RC962	Fairchild	962	
	Motorola	MC862	
	TI	SN15862	
RC9621	Fairchild	9621	
RC9622	Fairchild	9622	
RC963	Motorola	MC863	
	TI	SN15863	
RC993	Fairchild	9093	
	Motorola	MC853	
	TI	SN158093	
RC994	Fairchild	9094	
	Motorola	MC856	
	TI	SN158094	
RC997	Fairchild	9097	
	Motorola	MC855	
	TI	SN158097	
RC999	Motorola	MC852	
	TI	SN158092	
RM1514	Motorola	MC1514	
	TI	TL514	
RM1537	Motorola	MC1537	
RM1556	Motorola	MC1556	
	Signetics	MC1556	
	Silicon G	SG1556	
RM1558	Exar	XR1558	
	Harris	**HA-2650**	**986**
	Motorola	MC1558	
	PMI	PM1558	
		SSS1558	
	RCA	CA1558	
	Signetics	MC1558	
	Silicon G	SG1558	
	TI	MC1558	
RM2207	**Exar**	**XR2207**	**925**
RM2211	**Exar**	**XR2211**	**922**
RM2567	Exar	XR2567	
		XR2567M	
RM3403	Exar	XR3403M	
RM3503	Exar	XR3503	
	Fairchild	μA3503	
	Motorola	MC3503	
	Silicon G	**SG3503**	**1128**
RM4136	Exar	XR4136	
		XR4136M	
	Fairchild	μA4136	
	PMI	OP-09	
		PM4136M	
	Silicon G	SG4136	
	TI	RM4136	
RM4151	TI	XR4151	
RM4152	TI	XR4152	
RM4156	TI	XR4156	
RM4194	Exar	XR4194	
	Silicon G	SG4194	
RM4531	Signetics	SE531	
RM4558	Motorola	MC4558	
	RCA	CA1558	
	Silicon G	SG1558	
	TI	RM4558	
RM55107	Fairchild	55107	
	Motorola	MC55107	
	TI	SN55107	
RM55108	Fairchild	55108	
	TI	SN55108	
RM55109	Fairchild	55109	
	TI	SN55109	
RM55110	Fairchild	55110	
	TI	SN55110	
RM5524	Fairchild	5524	
	TI	SN5524	
RM5525	Fairchild	5525	
RM55325	Fairchild	55325	
	Motorola	MC55325	
	TI	SN55325	
RM555	AMD	SE555	
	Cherry	CS555	
	Exar	XR555M	
	Fairchild	μA555	
	Intersil	SE555	
	Motorola	MC1555	
	Signetics	SE555	
	Silicon G	SG555	
	TI	SE555	
RM556	Exar	XR556M	
	Fairchild	μA556	
	Motorola	MC3556	
	Silicon G	SG556	
	TI	SE556	
RM592	Motorola	SE592	
	Signetics	SE592	
RM702	Motorola	MC1712	
	TI	μA702	
RM709	Motorola	MC1709	
	Signetics	μA709	
	TI	μA709	
RM710	Motorola	MC1710	
	Signetics	μA710	
	Silicon G	SG710	
	TI	μA710	
RM711	Motorola	MC1711	
	Signetics	μA711	
	Silicon G	SG711	
	Teledyne S	711	
	TI	μA711	
RM723	AMD	723	
	Intersil	723	
	Motorola	MC1723	
	National	LM723	
	RCA	CA723	
	Signetics	μA723	
	Silicon G	SG723	
	TI	μA723	
RM725	AMD	725	
	PMI	PM725	
		SSS725	
RM733	AMD	733	
	Fairchild	μA733	
	Motorola	MC1733	
	Signetics	μA733	
	Silicon G	SG733	
	TI	μA733	
RM741	AMD	741	
	Intersil	741	
	Motorola	MC1741	
	PMI	PM741	
		SSS741	
	RCA	CA741	
	Signetics	μA741	
	Silicon G	SG741	
	Sprague	ULS-2151	
	TI	μA741	
RM747	AMD	747	
	Motorola	MC1747	
	PMI	PM747	
		SSS747	
	RCA	CA747	
	Signetics	μA747	
	Silicon G	SG747	
	TI	μA747	
RM748	AMD	748	
	Intersil	748	
	Motorola	MC1748	
	RCA	CA748	
	Signetics	μA748	
	Silicon G	SG748	
	TI	μA748	
RM930	Motorola	MC930	
	TI	SN15930	
RM932	Motorola	MC932	
	TI	SN15932	
RM933	Motorola	MC933	
	TI	SN15933	
RM934	Motorola	MC934	
	TI	SN15934	
RM935	Motorola	MC935	
	TI	SN15935	
RM936	Motorola	MC936	
	TI	SN15936	
RM937	Motorola	MC937	
	TI	SN15937	
RM940	Motorola	MC940	
RM941	Motorola	MC941	
RM944	Motorola	MC944	
	TI	SN15944	
RM945	Motorola	MC945	
	TI	SN15945	
RM946	Motorola	MC946	
	TI	SN15946	
RM947	TI	SN15947	
RM948	Motorola	MC948	
	TI	SN15948	
RM949	Motorola	MC949	
	TI	SN15949	
RM950	Motorola	MC950	
	TI	SN15950	
RM951	Motorola	MC951	
	TI	SN15951	
RM957	Motorola	MC957	
	TI	SN15957	
RM958	Motorola	MC958	
	TI	SN15958	
RM961	Motorola	MC961	
	TI	SN15961	
RM962	Motorola	MC962	
	TI	SN15962	
RM9621	Fairchild	9621	
RM9622	Fairchild	9622	
RM963	Motorola	MC963	
	TI	SN15963	
RM993	Motorola	MC953	
	TI	SN159093	
RM994	Motorola	MC956	
	TI	SN159094	
RM997	Motorola	MC955	
	TI	SN159097	
RM999	Motorola	MC952	
	TI	SN159099	
RV4151	TI	XR4151	
RV4152	TI	XR4152	
RV4156	TI	XR4156	
SP3724	RCA	CA3724	
SP3725	RCA	CA3725	
25LS138	AMD	AM25LS138	
25LS139	AMD	AM25LS138	
25LS14	AMD	AM25LS14	
25LS15	AMD	AM25LS15	
25LS151	AMD	AM25LS125	
25LS153	AMD	AM25LS153	
25LS157	AMD	AM25LS157	
25LS158	AMD	AM25LS158	
25LS160	AMD	AM25LS160	
25LS161	AMD	AM25LS161	
25LS162	AMD	AM25LS162	
25LS163	AMD	AM25LS163	
25LS164	AMD	AM25LS164	
25LS174	AMD	AM25LS174	
25LS175	AMD	AM25LS175	
25LS181	AMD	AM25LS181	
25LS190	AMD	AM25LS190	
25LS191	AMD	AM25LS191	
25LS192	AMD	AM25LS192	
25LS193	AMD	AM25LS193	
25LS194A	AMD	AM25LS194A	
25LS195	AMD	AM25LS195	
25LS22	AMD	AM25LS22	
25LS23	AMD	AM25LS23	
25LS240	AMD	25LS240	
25LS241	AMD	AM25LS241	
25LS251	AMD	AM25LS251	
25LS253	AMD	AM25LS253	
25LS258	AMD	AM25LS258	
25LS299	AMD	AM25LS299	
25LS373	AMD	25LS373	
26S10	AMD	AM26S10	

♦ Discontinued

The manufacturers report their devices can be used as direct replacements.
Performance details often differ, so compare the specifications considering your requirements.

Raytheon Semiconductor (cont'd)

Manufacturer Device	Replacement Source	Device	IC Master Page
26S11	AMD	AM26S11	
29600	**MMI**	**5308-1**	**1449**
		6308-1	**1449**
29601	**MMI**	**5309-1**	**1449**
		6309-1	**1449**
29610	**MMI**	**5305-1**	**1449**
		6305-1	**1449**
29611	**MMI**	**5306-1**	**1449**
		6306-1	**1449**
29612	MMI	53PS240	
		63PS240	
29613	MMI	53PS241	
		63PS241	
29620	**MMI**	**5348-1**	**1449**
		6348-1	**1449**
29621	**MMI**	**5349-1**	**1449**
		6349-1	**1449**
29622	MMI	53PS480	
		63PS480	
29623	MMI	53PS481	
		63PS481	
29624	**MMI**	**5340-1**	**1449**
		6340-1	**1449**
29625	**MMI**	**5341-1**	**1449**
		6341-1	**1449**
29626	MMI	53PS482	
		63PS482	
29627	MMI	53PS483	
		63PS483	
29630	**MMI**	**5380-1**	**1449**
		6380-1	**1449**
29631	**MMI**	**5381-1**	**1449**
		6381-1	**1449**
29632	MMI	53PS880	
		63PS880	
29633	MMI	53PS881	
		63PS881	
29650	**MMI**	**53S840**	**1453**
		63S840	**1453**
29651	**MMI**	**53S841**	**1453**
		63S841	**1453**
29652	MMI	53PS840	
		63PS840	
29653	MMI	53PS841	
		63PS841	
29660	**MMI**	**5300-1**	**1449**
		6300-1	**1449**
29661	**MMI**	**5301-1**	**1449**
		6301-1	**1449**
29662	MMI	53PS140	
		63PS140	
29663	MMI	53PS141	
		63PS141	
♦54HXX	Fairchild	54HXX	
	National	DM54HXX	
	Signetics	54HXX	
	TI	SN54HXX	
54LS00	Fairchild	54LS00	
	Motorola	SN54LS00	
	National	DM54LS00	
	Signetics	54LS00	
	TI	SN54LS00	
54LS01	National	DM54LS01	
	Signetics	54LS01	
	TI	SN54LS01	
54LS02	Fairchild	54LS02	
	Motorola	SN54LS02	
	National	DM54LS02	
	Signetics	54LS02	
	TI	SN54LS02	
54LS03	Fairchild	54LS03	
	Motorola	SN54LS03	
	National	DM54LS03	
	Signetics	54LS03	
	TI	SN54LS03	
54LS04	Fairchild	54LS04	
	Motorola	SN54LS04	
	National	DM54LS04	
	Signetics	54LS04	
	TI	SN54LS04	
54LS05	Fairchild	54LS05	
	Motorola	SN54LS05	
54LS05	National	DM54LS05	
	Signetics	54LS05	
	TI	SN54LS05	
54LS08	Fairchild	54LS08	
	Motorola	SN54LS08	
	National	DM54LS08	
	Signetics	54LS08	
	TI	SN54LS08	
54LS09	Fairchild	54LS09	
	Motorola	SN54LS09	
	National	DM54LS09	
	Signetics	54LS09	
	TI	SN54LS09	
54LS10	Fairchild	54LS10	
	Motorola	SN54LS10	
	National	DM54LS10	
	Signetics	54LS10	
	TI	SN54LS10	
54LS107	Fairchild	54LS107	
	Motorola	SN54LS107A	
	National	DM54LS107	
	Signetics	54LS107	
	TI	SN54LS107A	
54LS109	Fairchild	54LS109	
	Motorola	SN54LS109	
	National	DM54LS109	
	Signetics	54LS109	
	TI	SN54LS109	
54LS11	Fairchild	54LS11	
	Motorola	SN54LS11	
	National	DM54LS11	
	Signetics	54LS11	
	TI	SN54LS11	
54LS112	Fairchild	54LS112	
	Motorola	SN54LS112A	
	National	DM54LS112	
	Signetics	54LS112	
	TI	SN54LS112	
54LS113	Fairchild	54LS113	
	Motorola	SN54LS113A	
	National	DM54LS113	
	Signetics	54LS113	
	TI	SN54LS113	
54LS114	Fairchild	54LS114	
	Motorola	SN54LS114A	
	National	DM54LS114	
	Signetics	54LS114	
	TI	SN54LS114A	
54LS12	Fairchild	54LS12	
	Motorola	SN54LS12	
	National	DM54LS12	
	Signetics	54LS12	
	TI	SN54LS12	
54LS122	National	DM54LS122	
	TI	SN54LS122	
54LS123	AMD	SN54LS123	
	National	DM54LS123	
	TI	SN54LS123	
54LS125	Fairchild	54LS125	
	National	DM54LS125	
	Signetics	54LS125	
	TI	SN54LS125A	
54LS126	Fairchild	54LS126	
	Motorola	SN54LS126	
	National	DM54LS126	
	Signetics	54LS126	
	TI	SN54LS126A	
54LS13	Fairchild	54LS13	
	Motorola	SN54LS13	
	National	DM54LS13	
	Signetics	54LS13	
	TI	SN54LS13	
54LS132	Fairchild	54LS132	
	Motorola	SN54LS132	
	National	DM54LS132	
	Signetics	54LS132	
54LS136	Fairchild	54LS136	
	Motorola	SN54LS136	
	Signetics	54LS136	
	TI	SN54LS136	
54LS138	Fairchild	54LS138	
	Motorola	SN54LS138	
	National	DM54LS138	
	Signetics	54LS138	
	TI	SN54LS138	
54LS139	AMD	SN54LS139	
54LS139	Fairchild	54LS139	
	Motorola	SN54LS139	
	National	DM54LS139	
	Signetics	54LS139	
		74LS139	
	TI	SN54LS139	
54LS14	Fairchild	54LS14	
	Motorola	SN54LS14	
	National	DM54LS14	
	Signetics	54LS14	
	TI	SN54LS14	
54LS15	Fairchild	54LS15	
	Motorola	SN54LS15	
	National	DM54LS15	
	Signetics	54LS15	
	TI	SN54LS15	
54LS151	AMD	SN54LS151	
	Fairchild	54LS151	
	Motorola	SN54LS151	
	National	DM54LS151	
	Signetics	54LS151	
		54LS153	
	TI	SN54LS151	
54LS152	Fairchild	54LS152	
	Motorola	SN54LS152	
	TI	SN54LS152	
54LS153	AMD	SN54LS153	
	Fairchild	54LS153	
	Motorola	SN54LS153	
	National	DM54LS153	
	Signetics	54LS153	
	TI	SN54LS153	
54LS156	Fairchild	54LS156	
	Motorola	SN54LS156	
	National	DM54LS156	
	TI	SN54LS156	
54LS157	AMD	SN54LS157	
	Fairchild	54LS157	
	Motorola	SN54LS157	
	National	DM54LS157	
	Signetics	54LS157	
	TI	SN54LS157	
54LS158	Fairchild	54LS158	
	Motorola	SN54LS158	
	National	DM54LS158	
	Signetics	54LS158	
	TI	SN54LS158	
54LS160	AMD	SN54LS160	
	Fairchild	54LS160	
	Motorola	SN54LS160A	
	National	DM54LS160	
	Signetics	54LS160A	
	TI	SN54LS160A	
54LS161	AMD	SN54LS161	
	Fairchild	54LS161	
	Motorola	SN54LS161A	
	National	DM54LS161	
	Signetics	54LS161A	
	TI	SN54LS161A	
54LS162	AMD	SN54LS162	
	Fairchild	54LS162	
	Motorola	SN54LS162A	
	National	DM54LS162	
	Signetics	54LS162A	
	TI	SN54LS162A	
54LS163	AMD	SN54LS163	
	Fairchild	54LS163	
	Motorola	SN54LS163A	
	National	DM54LS163	
	Signetics	54LS163A	
	TI	SN54LS163A	
54LS164	AMD	SN54LS164	
	Fairchild	54LS164	
	Motorola	SN54LS164A	
	National	DM54LS164	
	Signetics	54LS164	
	TI	SN54LS164A	
54LS170	AMD	SN54LS170	
	Fairchild	54LS170	
	Motorola	SN54LS170	
	National	DM54LS170	
	Signetics	54LS170	
	TI	SN54LS170	
54LS174	AMD	SN54LS174	
	Fairchild	54LS174	
	National	DM54LS174	
54LS174	Signetics	54LS174	
	TI	SN54LS174	
54LS175	AMD	SN54LS175	
	Fairchild	54LS175	
	Motorola	SN54LS175	
	National	DM54LS175	
	Signetics	54LS175	
	TI	SN54LS175	
54LS181	AMD	SN54LS181	
	Fairchild	54LS181	
	Motorola	SN54LS181	
	Signetics	54LS181	
	TI	SN54LS181	
54LS190	AMD	SN54LS190	
	Fairchild	54LS190	
	Motorola	SN54LS190	
	National	DM54LS190	
	Signetics	54LS190	
	TI	SN54LS190	
54LS191	AMD	SN54LS191	
	Fairchild	54LS191	
	Motorola	SN54LS191	
	National	DM54LS191	
	Signetics	54LS191	
	TI	SN54LS191	
54LS192	AMD	SN54LS192	
	Fairchild	54LS192	
	Motorola	SN54LS192	
	National	DM54LS192	
	Signetics	54LS192	
	TI	SN54LS192	
54LS193	AMD	SN54LS193	
	Fairchild	54LS193	
	Motorola	SN54LS193	
	National	DM54LS193	
	Signetics	54LS193	
	TI	SN54LS193	
54LS194A	AMD	SN54LS194A	
	Fairchild	54LS194	
	Motorola	SN54LS194A	
	Signetics	54LS194A	
	TI	SN54LS194A	
54LS195A	AMD	SN54LS195A	
	Fairchild	54LS195	
	Motorola	SN54LS195A	
	Signetics	54LS195A	
	TI	SN54LS195A	
54LS196	Fairchild	54LS196	
	Motorola	SN54LS196	
	National	DM54LS196	
	Signetics	54LS196	
	TI	SN54LS196	
54LS197	Fairchild	54LS197	
	Motorola	SN54LS197	
	National	DM54LS197	
	Signetics	54LS197	
	TI	SN54LS197	
54LS20	Fairchild	54LS20	
	Motorola	SN54LS20	
	National	DM54LS20	
	Signetics	54LS20	
	TI	SN54LS20	
54LS21	Fairchild	54LS21	
	Motorola	SN54LS21	
	National	DM54LS21	
	Signetics	54LS21	
	TI	SN54LS21	
54LS22	Fairchild	54LS22	
	Motorola	SN54LS22	
	National	DM54LS22	
	Signetics	54LS22	
	TI	SN54LS22	
54LS221	National	DM54LS221	
	Signetics	54LS221	
	TI	SN54LS221	
54LS242	AMD	SN54LS242	
	Fairchild	54LS242	
	TI	SN54LS242	
54LS243	AMD	SN54LS243	
	Fairchild	54LS243	
	TI	SN54LS243	
54LS251	AMD	SN54LS251	
	Fairchild	54LS251	
	Motorola	SN54LS251	
	Signetics	54LS251	
	TI	SN54LS251	

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Bold face device numbers indicate manufacturers data is provided in the IC Master on the pages noted.

Raytheon Semiconductor (cont'd)

Manufacturer Device	Replacement Source	Device	IC Master Page
54LS253	AMD	SN54LS253	
	Fairchild	54LS253	
	Motorola	SN54LS253	
	National	DM54LS253	
	Signetics	54LS253	
	TI	SN54LS253	
54LS257	Fairchild	54LS257	
	Motorola	SN54LS257A	
	National	DM54LS257	
	Signetics	54LS257	
	TI	SN54LS257A	
54LS258	AMD	SN54LS258	
	Fairchild	54LS258	
	Motorola	SN54LS258	
	Signetics	54LS258	
	TI	SN54LS258	
54LS26	Fairchild	54LS26	
	Motorola	SN54LS26	
	National	DM54LS26	
	Signetics	54LS26	
	TI	SN54LS26	
54LS261	Signetics	54LS261	
	TI	SN54LS261	
54LS266	Fairchild	54LS266	
	Motorola	SN54LS266	
	Signetics	54LS266	
	TI	SN54LS266	
54LS27	Fairchild	54LS27	
	Motorola	SN54LS27	
	National	DM54LS27	
	Signetics	54LS27	
	TI	SN54LS27	
54LS28	Fairchild	54LS28	
	Signetics	54LS28	
	TI	SN54LS28	
54LS283	Fairchild	54LS283	
	Motorola	SN54LS283	
	National	DM54LS283	
	Signetics	54LS283	
	TI	SN54LS283	
54LS290	Motorola	SN54LS290	
54LS293	Motorola	SN54LS293	
54LS295A	Fairchild	54LS295	
	Motorola	SN54LS295	
	Signetics	54LS295A	
	TI	SN54LS295B	
54LS298	Fairchild	54LS298	
	Motorola	SN54LS298	
	TI	SN54LS298	
54LS299	AMD	SN54LS299	
	Fairchild	54LS299	
	TI	SN54LS299	
54LS30	Fairchild	54LS30	
	Motorola	SN54LS30	
	National	DM54LS30	
	Signetics	54LS30	
	TI	SN54LS30	
54LS32	Fairchild	54LS32	
	Motorola	SN54LS32	
	National	DM54LS32	
	Signetics	54LS32	
	TI	SN54LS32	
54LS322	Motorola	SN54LS322	
54LS323	Motorola	SN54LS323	
		SN74LS323	
54LS33	Fairchild	54LS33	
	Signetics	54LS33	
	TI	SN54LS33	
54LS365	Fairchild	54LS365	
	Motorola	SN54LS365A	
	Signetics	54LS365A	
	TI	SN54LS265A	
54LS366	Fairchild	54LS366	
	Motorola	SN54LS366A	
	Signetics	54LS366A	
	TI	SN54LS366A	
54LS367	Fairchild	54LS367	
	Motorola	SN54LS367A	
	Signetics	54LS367A	
	TI	SN54LS367A	
54LS368	Fairchild	54LS368	
	Motorola	SN54LS368A	
54LS368	Signetics	54LS368A	
	TI	SN54LS368A	
54LS37	Fairchild	54LS37	
	Motorola	SN54LS37	
	National	DM54LS37	
	Signetics	54LS37	
	TI	SN54LS37	
54LS373	Motorola	SN54LS373	
54LS375	Fairchild	54LS375	
	Signetics	54LS375	
	TI	SN54LS375	
54LS38	Fairchild	54LS38	
	Motorola	SN54LS38	
	National	DM54LS38	
	Signetics	54LS38	
	TI	SN54LS38	
54LS384	Motorola	SN54LS384	
54LS385	Motorola	SN54LS385	
54LS386	Signetics	54LS386	
	TI	54LS386	
54LS395	Fairchild	54LS395	
	National	DM54LS395	
	Signetics	54LS395	
	TI	SN54LS395	
54LS40	Fairchild	54LS40	
	Motorola	SN54LS40	
	National	DM54LS40	
	Signetics	54LS40	
	TI	SN54LS40	
54LS42	Fairchild	54LS42	
	Motorola	SN54LS42	
	National	DM54LS42	
	Signetics	54LS42	
	TI	SN54LS42	
54LS51	Fairchild	54LS51	
	Motorola	SN54LS51	
	National	DM54LS51	
	Signetics	54LS51	
	TI	SN54LS51	
54LS54	Fairchild	54LS54	
	Motorola	SN54LS54	
	National	DM54LS54	
	Signetics	54LS54	
	TI	SN54LS54	
54LS55	Fairchild	54LS55	
	Motorola	SN54LS55	
	National	DM54LS55	
	Signetics	54LS55	
	TI	SN54LS55	
54LS670	AMD	SN54LS670	
	Fairchild	54LS670	
	Motorola	SN54LS670	
	National	DM54LS670	
	Signetics	54LS670	
	TI	SN54LS670	
54LS73	Fairchild	54LS73	
	Motorola	SN54LS73A	
	National	DM54LS73	
	Signetics	54LS73	
	TI	SN54LS73A	
54LS74	Fairchild	54LS74	
	Motorola	SN54LS74A	
	National	DM54LS74	
	Signetics	54LS74	
	TI	SN54LS74A	
54LS75	Motorola	SN54LS75	
	National	DM54LS75	
	Signetics	54LS75	
	TI	SN54LS75	
54LS76	Fairchild	54LS76	
	Motorola	SN54LS76A	
	National	DM54LS76	
	Signetics	54LS76	
	TI	SN54LS76	
54LS77	Motorola	SN74LS77	
	National	DM74LS77	
	TI	SN54LS77	
54LS78	Fairchild	54LS78	
	Motorola	SN54LS78A	
	National	DM54LS78	
	Signetics	54LS78	
	TI	SN54LS78	
54LS83A	Fairchild	54LS83	
	Motorola	SN54LS83	
	National	DM54LS83	
	Signetics	54LS83A	
54LS83A	TI	SN54LS83A	
54LS85	Fairchild	54LS85	
	Motorola	SN54LS85	
	National	DM54LS85	
	Signetics	54LS85	
	TI	SN54LS85	
54LS86	Fairchild	54LS86	
	Motorola	SN54LS86	
	Signetics	54LS86	
	TI	SN54LS86	
54LS90	Fairchild	54LS90	
	Motorola	SN54LS90	
	Signetics	54LS90	
	TI	SN54LS90	
54LS91	TI	SN54LS91	
54LS92	Motorola	SN54LS92	
	Signetics	54LS92	
	TI	SN54LS92	
54LS93	Fairchild	54LS93	
	Motorola	SN54LS93	
	Signetics	54LS93	
	TI	SN54LS93	
54LS95B	Fairchild	54LS95B	
	Motorola	SN54LS95B	
	Signetics	54LS95B	
	TI	SN54LS95B	
54S240	Fairchild	54S240	
	MMI	**54S240**	**768**
	TI	SN54S240	
54S241	AMD	SN54S241	
	Fairchild	54S241	
	MMI	**54S241**	**768**
	TI	SN54S241	
54S244	AMD	SN54S244	
	MMI	**54S244**	**768**
♦5400 series	AMD	SN54XX	
	Fairchild	54XX	
	Ferranti	ZN54XX	
	Motorola	SN54XX	
	National	DM54XX	
	Signetics	54XX	
	TI	SN54XX	
♦74HXX	Fairchild	74HXX	
	National	DM74HXX	
	Signetics	74HXX	
	TI	SN74HXX	
74LS00	Fairchild	74LS00	
	Hitachi	HD74LS00	
	Motorola	SN74LS00	
	National	DM74LS00	
	NEC America	μPB74LS00	
	Signetics	74LS00	
	TI	SN74LS00	
74LS01	Hitachi	HD74LS01	
	National	DM74LS01	
	Signetics	74LS01	
	TI	SN74LS01	
74LS02	Fairchild	74LS02	
	Hitachi	HD74LS02	
	Motorola	SN74LS02	
	National	DM74LS02	
	NEC America	μPB74LS02	
	Signetics	74LS02	
	TI	SN74LS02	
74LS03	Fairchild	74LS03	
	Hitachi	HD74LS03	
	Motorola	SN74LS03	
	National	DM74LS03	
	NEC America	μPB74LS03	
	Signetics	74LS03	
	TI	SN74LS03	
74LS04	Fairchild	74LS04	
	Hitachi	HD74LS04	
	Motorola	SN74LS04	
	National	DM74LS04	
	NEC America	μPB74LS04	
	Signetics	74LS04	
	TI	SN74LS04	
74LS05	Fairchild	74LS05	
	Hitachi	HD74LS05	
	Motorola	SN74LS05	
	National	DM74LS05	
	NEC America	μPB74LS05	
	Signetics	74LS05	
	TI	SN74LS05	
74LS08	Fairchild	74LS08	
74LS08	Hitachi	HD74LS08	
	Motorola	SN74LS08	
	National	DM74LS08	
	NEC America	μPB74LS08	
	Signetics	74LS08	
	TI	SN74LS08	
74LS09	Fairchild	74LS09	
	Hitachi	HD74LS09	
	Motorola	SN74LS09	
	National	DM74LS09	
	Signetics	74LS09	
	TI	SN74LS09	
74LS10	Fairchild	74LS10	
	Hitachi	HD74LS10	
	Motorola	SN74LS10	
	National	DM74LS10	
	NEC America	μPB74LS10	
	Signetics	74LS10	
	TI	SN74LS10	
74LS107	Fairchild	74LS107	
	Hitachi	HD74LS107	
	Motorola	SN74LS107A	
	National	DM74LS107	
	Signetics	74LS107	
	TI	SN74LS107	
74LS109	Fairchild	74LS109	
	Motorola	SN74LS109A	
	National	DM74LS109	
	NEC America	μPB74LS109	
	Signetics	74LS109	
	TI	SN74LS109A	
74LS11	Fairchild	74LS11	
	Hitachi	HD74LS11	
	Motorola	SN74LS11	
	National	DM74LS11	
	NEC America	μPB74LS11	
	Signetics	74LS11	
	TI	SN74LS11	
74LS112	Fairchild	74LS112	
	Hitachi	HD74LS112	
	Motorola	SN74LS112A	
	National	DM74LS112	
	NEC America	μPB74LS112	
	Signetics	74LS112	
	TI	SN74LS112	
74LS113	Fairchild	74LS113	
	Hitachi	HD74LS113	
	Motorola	SN74LS113A	
	National	DM74LS113	
	NEC America	μPB74LS113	
	Signetics	74LS113	
	TI	SN74LS113	
74LS114	Fairchild	74LS114	
	Hitachi	HD74LS114	
	Motorola	SN74LS114A	
	National	DM74LS114	
	Signetics	74LS114	
	TI	SN74LS114A	
74LS12	Hitachi	HD74LS12	
	Motorola	SN74LS12	
	National	DM74LS12	
	Signetics	74LS12	
	TI	SN74LS12	
74LS122	National	DM74LS122	
	TI	SN74LS122	
74LS123	AMD	SN74LS123	
	Hitachi	HD74LS123	
	National	DM74LS123	
	TI	SN74LS123	
74LS125	Fairchild	74LS125	
	National	DM74LS125	
	Signetics	74LS125	
	TI	SN74LS125A	
74LS126	Fairchild	74LS126	
	Motorola	SN74LS126	
	National	DM74LS126	
	Signetics	74LS126	
	TI	SN74LS126A	
74LS13	Fairchild	74LS13	
	Hitachi	HD74LS13	
	Motorola	SN74LS13	
	National	DM74LS13	
	Signetics	74LS13	
	TI	SN74LS13	
74LS132	Fairchild	74LS132	
	Hitachi	HD74LS132	

♦ Discontinued

The manufacturers report their devices can be used as direct replacements.
Performance details often differ, so compare the specifications considering your requirements.

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Manufacturer Device	Replacement Source	Device	IC Master Page
74LS132	Motorola	SN74LS132	
	National	DM54LS132	
		DM74LS132	
	Signetics	74LS132	
	TI	SN74LS132	
74LS136	Fairchild	74LS136	
	Hitachi	HD74LS136	
	Motorola	SN74LS136	
	National	DM74LS136	
	Signetics	74LS136	
	TI	SN74LS136	
74LS138	AMD	SN74LS138	
	Fairchild	74LS138	
	Hitachi	HD74LS138	
	Motorola	SN74LS138	
	National	DM74LS138	
	NEC America	μPB74LS138	
	Signetics	74LS138	
	TI	SN74LS138	
74LS139	AMD	SN74LS139	
	Fairchild	74LS139	
	Hitachi	HD74LS139	
	Motorola	SN74LS139	
	National	DM74LS139	
	NEC America	μPB74LS139	
	Signetics	74LS139	
	TI	SN74LS139	
74LS14	Fairchild	74LS14	
	Hitachi	HD74LS14	
	Motorola	SN74LS14	
	National	DM74LS14	
	Signetics	74LS14	
	TI	SN74LS14	
74LS15	Fairchild	74LS15	
	Hitachi	HD74LS15	
	Motorola	SN74LS15	
	National	DM74LS15	
	Signetics	74LS15	
	TI	SN74LS15	
74LS151	AMD	SN74LS151	
	Fairchild	74LS151	
	Hitachi	HD74LS151A	
	Motorola	SN74LS151	
	National	DM74LS151	
	NEC America	μPB74LS151	
	Signetics	74LS151	
	TI	SN74LS151	
74LS152	Fairchild	74LS152	
	Hitachi	HD74LS152	
	Motorola	SN74LS152	
74LS153	AMD	SN74LS153	
	Fairchild	74LS153	
	Hitachi	HD74LS153	
	Motorola	SN74LS153	
	National	DM74LS153	
	NEC America	μPB74LS153	
	Signetics	74LS153	
	TI	SN74LS153	
74LS155	Fairchild	54LS155	
		74LS155	
	Hitachi	HD74LS155	
	Motorola	SN54LS155	
		SN74LS155	
	National	DM54LS155	
		DM74LS155	
	NEC America	μPB74LS155	
	Signetics	74LS155	
	TI	SN54LS155	
		SN74LS155	
74LS156	Fairchild	74LS156	
	Hitachi	HD74LS156	
	Motorola	SN74LS156	
	National	DM74LS156	
	Signetics	74LS156	
	TI	SN74LS156	
74LS157	AMD	SN74LS157	
	Fairchild	74LS157	
	Motorola	SN74LS157	
	National	DM74LS157	
	NEC America	μPB74LS157	
	Signetics	74LS157	
	TI	SN74LS157	
74LS158	AMD	SN74LS158	
	Fairchild	74LS158	
	Hitachi	HD74LS158	
	Motorola	SN74LS158	
	National	DM74LS158	
	Signetics	74LS158	
	TI	SN74LS158	
74LS160	AMD	SN74LS160	
	Fairchild	74LS160	
	Hitachi	HD74LS160A	
	Motorola	SN74LS160A	
	National	DM74LS160	
	Signetics	74LS160A	
	TI	SN74LS160A	
74LS161	AMD	SN74LS161	
	Fairchild	74LS161	
	Hitachi	HD74LS161A	
	Motorola	SN74LS161A	
	National	DM74LS161	
	NEC America	μPB74LS161	
	Signetics	74LS161A	
	TI	SN74LS161A	
74LS162	AMD	SN74LS162	
	Fairchild	74LS162	
	Hitachi	HD74LS162A	
	Motorola	SN74LS162A	
	National	DM74LS162	
	Signetics	74LS162A	
	TI	SN74LS162A	
74LS163	AMD	SN74LS163	
	Fairchild	74LS163	
	Hitachi	HD74LS163A	
	Motorola	SN74LS163A	
	National	DM74LS163	
	Signetics	74LS163A	
	TI	SN74LS163A	
74LS164	AMD	SN74LS164	
	Fairchild	74LS164	
	Hitachi	HD74LS164	
	Motorola	SN74LS164A	
	National	DM74LS164	
	NEC America	μPB74LS164	
	Signetics	74LS164	
	TI	SN74LS164A	
74LS170	AMD	SN74LS170	
	Fairchild	74LS170	
	Motorola	SN74LS170	
	National	DM74LS170	
	Signetics	74LS170	
	TI	SN74LS170	
74LS174	AMD	SN74LS174	
	Fairchild	74LS174	
	Hitachi	HD74LS174	
	Motorola	SN74LS174	
	National	DM74LS174	
	Signetics	74LS174	
	TI	SN74LS174	
74LS175	AMD	SN74LS175	
	Fairchild	74LS175	
	Hitachi	HD74LS175	
	Motorola	SN74LS175	
	National	DM74LS175	
	NEC America	μPB74LS175	
	Signetics	74LS175	
	TI	SN74LS175	
74LS181	AMD	SN74LS181	
	Fairchild	74LS181	
	Motorola	SN74LS181	
	Signetics	74LS181	
	TI	SN74LS181	
74LS190	AMD	SN74LS190	
	Fairchild	74LS190	
	Motorola	SN74LS190	
	National	DM74LS190	
	Signetics	74LS190	
	TI	SN74LS190	
74LS191	AMD	SN74LS191	
	Fairchild	74LS191	
	Motorola	SN74LS191	
	National	DM74LS191	
	Signetics	74LS191	
	TI	SN74LS191	
74LS192	AMD	SN74LS192	
	Fairchild	74LS192	
	Motorola	SN74LS192	
	National	DM74LS192	
74LS192	NEC America	μPB74LS192	
	Signetics	74LS192	
	TI	SN74LS192	
74LS193	AMD	SN74LS193	
	Fairchild	74LS193	
	Motorola	SN74LS193	
	National	DM74LS193	
	NEC America	μPB74LS193	
	Signetics	74LS193	
	TI	SN74LS193	
74LS194A	AMD	SN74LS194A	
	Fairchild	74LS194	
	Hitachi	HD74LS194A	
	Motorola	SN74LS194A	
	NEC America	μPB74LS194	
	Signetics	74LS194A	
	TI	SN74LS194A	
74LS195A	AMD	SN74LS195A	
	Fairchild	74LS195	
	Hitachi	HD74LS195A	
	Motorola	SN74LS195A	
	NEC America	μPB74LS195	
	Signetics	74LS195A	
	TI	SN74LS195A	
74LS196	Fairchild	74LS196	
	Motorola	SN74LS196	
	National	DM74LS196	
	Signetics	74LS196	
	TI	SN74LS196	
74LS197	Fairchild	74LS197	
	Motorola	SN74LS197	
	National	DM74LS197	
	Signetics	74LS197	
	TI	SN74LS197	
74LS20	Fairchild	74LS20	
	Hitachi	HD74LS20	
	Motorola	SN74LS20	
	National	DM74LS20	
	NEC America	μPB74LS20	
	Signetics	74LS20	
	TI	SN74LS20	
74LS21	Fairchild	74LS21	
	Hitachi	HD74LS21	
	Motorola	SN74LS21	
	National	DM74LS21	
	NEC America	μPB74LS21	
	Signetics	74LS21	
	TI	SN74LS21	
74LS22	Fairchild	74LS22	
	Hitachi	HD74LS22	
	Motorola	SN74LS22	
	National	DM74LS22	
	Signetics	74LS22	
	TI	SN74LS22	
74LS221	Motorola	SN74LS221	
	National	DM74LS221	
	Signetics	74LS221	
	TI	SN74LS221	
74LS240	AMD	SN74LS240	
	Fairchild	74LS240	
	MMI	**74LS240**	**768**
	Motorola	SN74LS240	
	Signetics	74LS240	
	TI	SN74LS240	
74LS241	AMD	SN74LS241	
	Fairchild	74LS241	
	MMI	**74LS241**	**768**
	Motorola	SN74LS241	
	Signetics	74LS241	
	TI	SN74LS241	
74LS242	AMD	SN74LS242	
	Fairchild	74LS242	
	Motorola	SN74LS242	
	Signetics	74LS242	
	TI	SN74LS242	
74LS243	AMD	SN74LS243	
	Fairchild	74LS243	
	Motorola	SN74LS243	
	Signetics	74LS243	
	TI	SN74LS243	
74LS244	AMD	SN74LS244	
	Fairchild	74LS244	
	MMI	**74LS244**	**768**
	Motorola	SN74LS244	
	Signetics	74LS244	
	TI	SN74LS244	
74LS251	AMD	SN74LS251	
	Fairchild	74LS251	
	Motorola	SN74LS251	
	National	DM74LS251	
	NEC America	μPB74LS251	
	Signetics	74LS251	
	TI	SN74LS251	
74LS253	AMD	SN74LS253	
	Fairchild	74LS253	
	Hitachi	HD74LS253	
	Motorola	SN74LS253	
	National	DM74LS253	
	NEC America	μPB74LS253	
	Signetics	74LS253	
	TI	SN74LS253	
74LS257	AMD	SN74LS257	
	Fairchild	74LS257	
	Hitachi	HD74LS257	
	Motorola	SN74LS257A	
	National	DM74LS257	
	NEC America	μPB74LS257	
	Signetics	74LS257A	
	TI	SN74LS257	
74LS258	AMD	SN74LS258	
	Fairchild	74LS258	
	Motorola	SN74LS258A	
	National	DM74LS258	
	NEC America	μPB74LS258	
	Signetics	74LS258	
	TI	SN74LS258A	
74LS26	Fairchild	74LS26	
	Hitachi	HD74LS26	
	Motorola	SN74LS26	
	National	DM74LS26	
	Signetics	74LS26	
	TI	SN74LS26	
74LS261	Signetics	74LS261	
	TI	SN74LS261	
74LS266	Fairchild	74LS266	
	Motorola	SN74LS266	
	Signetics	74LS266	
	TI	SN74LS266	
74LS27	Fairchild	74LS27	
	Hitachi	HD74LS27	
	Motorola	SN74LS27	
	National	DM74LS27	
	NEC America	μPB74LS27	
	Signetics	74LS27	
	TI	SN74LS27	
74LS279	Fairchild	54LS279	
		74LS279	
	Motorola	SN54LS279	
		SN74LS279	
	National	DM54LS279	
		DM74LS279	
	NEC America	μPB74LS279	
	Signetics	54LS279	
		74LS279	
	TI	SN54LS279	
		SN74LS279	
74LS28	Fairchild	74LS28	
	Signetics	74LS28	
	TI	SN74LS28	
74LS283	Fairchild	74LS283	
	Hitachi	SN74LS283	
	Motorola	SN74LS283	
	National	DM74LS283	
	Signetics	74LS283	
	TI	SN74LS283	
74LS290	Motorola	SN74LS290	
74LS295A	Fairchild	74LS295	
	Motorola	SN74LS295	
	NEC America	μPB74LS295	
	Signetics	74LS295	
	TI	SN74LS295B	
74LS298	Fairchild	74LS298	
	Hitachi	HD74LS298	
	Motorola	SN74LS298	
	Signetics	74LS298	
	TI	SN74LS298	
74LS299	AMD	SN74LS299	
	Fairchild	74LS299	
	TI	SN74LS299	
74LS30	Fairchild	74LS30	
	Hitachi	HD74LS30	
	Motorola	SN74LS30	

♦ Discontinued

Bold face device numbers indicate manufacturers data is provided in the IC Master on the pages noted.

Raytheon Semiconductor (cont'd)

Manufacturer Device	Replacement Source	Device	IC Master Page
74LS30	National	DM74LS30	
	NEC America	μPB74LS30	
	Signetics	74LS30	
	TI	SN74LS30	
74LS32	Fairchild	74LS32	
	Hitachi	HD74LS32	
	Motorola	SN74LS32	
	National	DM74LS32	
	NEC America	μPB74LS32	
	Signetics	74LS32	
	TI	SN74LS32	
74LS322	Motorola	SN74LS322	
74LS323	AMD	SN74LS323	
	Fairchild	74LS323	
	TI	SN74LS323	
74LS33	Fairchild	74LS33	
	Signetics	74LS33	
	TI	SN74LS33	
74LS365	Fairchild	74LS365	
	Motorola	SN74LS365A	
	National	DM74LS365	
	NEC America	μPB74LS365	
	Signetics	74LS365A	
	TI	SN74LS365A	
74LS366	Fairchild	74LS366	
	Motorola	SN74LS366A	
	National	DM74LS366	
	NEC America	μPB74LS366	
	Signetics	74LS366A	
	TI	SN74LS366A	
74LS367	Fairchild	74LS367	
	Hitachi	HD74LS367	
	Motorola	SN74LS367A	
	National	DM74LS367	
	NEC America	μPB74LS367	
	Signetics	74LS367A	
	TI	SN74LS367A	
74LS368	Fairchild	74LS368	
	Hitachi	HD74LS368	
	Motorola	SN74LS368A	
	National	DM74LS368	
	NEC America	μPB74LS368	
	Signetics	74LS368A	
	TI	SN74LS368A	
74LS37	Fairchild	74LS37	
	Hitachi	HD74LS37	
	Motorola	SN74LS37	
	National	DM74LS37	
	NEC America	μPB74LS37	
	Signetics	74LS37	
	TI	SN74LS37	
74LS373	AMD	SN74LS373	
	Fairchild	74LS373	
	MMI	**74LS373**	**505**
	Motorola	SN74LS373	
	Signetics	74LS373	
	TI	SN74LS373	
74LS374	AMD	SN74LS374	
	Fairchild	74LS374	
	MMI	**74LS374**	**505**
	TI	SN74LS374	
74LS375	Fairchild	74LS375	
	Motorola	SN74LS375	
	NEC America	μPB74LS375	
	Signetics	74LS375	
	TI	SN74LS375	
74LS377	AMD	SN74LS377	
	Fairchild	74LS377	
	Signetics	74LS377	
	TI	SN74LS377	
74LS38	Fairchild	74LS38	
	Hitachi	HD74LS38	
	Motorola	SN74LS38	
	National	DM74LS38	
	NEC America	μPB74LS38	
	Signetics	74LS38	
	TI	SN74LS38	
74LS384	Motorola	SN74LS384	
74LS385	Motorola	SN74LS385	
74LS386	Hitachi	HD74LS386	
	Motorola	SN74LS386	
	National	DM74LS386	
74LS386	Signetics	74LS386	
	TI	SN74LS386	
74LS395	Fairchild	74LS395	
	National	DM74LS395	
	Signetics	74LS395	
	TI	SN74LS395	
74LS40	Fairchild	74LS40	
	Hitachi	HD74LS40	
	Motorola	SN74LS40	
	National	DM74LS40	
	NEC America	μPB74LS40	
	Signetics	74LS40	
	TI	SN74LS40	
74LS42	Fairchild	74LS42	
	Hitachi	HD74LS42	
	Motorola	SN74LS42	
	National	DM74LS42	
	NEC America	μPB74LS42	
	Signetics	74LS42	
	TI	SN74LS42	
74LS51	Fairchild	74LS51	
	Hitachi	HD74LS51	
	Motorola	SN74LS51	
	National	DM74LS51	
	NEC America	μPB74LS51	
	Signetics	74LS51	
	TI	SN74LS51	
74LS54	Fairchild	74LS54	
	Hitachi	HD74LS54	
	Motorola	SN74LS54	
	National	DM74LS54	
	NEC America	μPB74LS54	
	Signetics	74LS54	
	TI	SN74LS54	
74LS55	Fairchild	74LS55	
	Hitachi	HD74LS55	
	Motorola	SN74LS55	
	National	DM74LS55	
	NEC America	μPB74LS55	
	Signetics	74LS55	
	TI	SN74LS55	
74LS670	Fairchild	74LS670	
	Motorola	SN74LS670	
	National	DM74LS670	
	Signetics	74LS670	
	TI	SN74LS670	
74LS73	Fairchild	74LS73	
	Hitachi	HD74LS73	
	Motorola	SN74LS73	
	National	DM74LS73	
	Signetics	74LS73	
	TI	SN74LS73A	
74LS74	Fairchild	74LS74	
	Hitachi	HD74LS74A	
	Motorola	SN74LS74A	
	National	DM74LS74	
	NEC America	μPB74LS74	
	Signetics	74LS74	
	TI	SN74LS74A	
74LS75	Motorola	SN74LS75	
	National	DM74LS75	
	Signetics	74LS75	
	TI	SN74LS75	
74LS76	Fairchild	74LS76	
	Hitachi	HD74LS76	
	Motorola	SN74LS76A	
	National	DM74LS76	
	Signetics	74LS76	
	TI	SN74LS76	
74LS78	Fairchild	74LS78	
	Hitachi	HD74LS78	
	Motorola	SN74LS78A	
	National	DM74LS78	
	Signetics	74LS78	
	TI	SN74LS78	
74LS83A	Fairchild	74LS83	
	Hitachi	HD74LS83A	
	Motorola	SN74LS83A	
	National	DM74LS83	
		DM74LS83A	
	Signetics	74LS83	
	TI	SN74LS83A	
74LS85	Fairchild	74LS85	
	Motorola	SN74LS85	
	National	DM74LS85	
	Signetics	74LS85	
74LS85	TI	SN74LS85	
74LS86	Fairchild	74LS86	
	Hitachi	HD74LS86	
	Motorola	SN74LS86	
	NEC America	μPB74LS86	
	Signetics	74LS86	
	TI	SN74LS86	
74LS90	Fairchild	74LS90	
	Motorola	SN74LS90	
	National	DM74LS90	
	Signetics	74LS90	
	TI	SN74LS90	
74LS91	TI	SN74LS91	
74LS92	Fairchild	74LS92	
	Hitachi	HD74LS92	
	Motorola	SN74LS92	
	National	DM74LS92	
	Signetics	74LS92	
	TI	SN74LS92	
74LS93	Fairchild	74LS93	
	Motorola	SN74LS93	
	National	DM74LS93	
	Signetics	74LS93	
	TI	SN74LS93	
74LS95B	Fairchild	74LS95	
	Hitachi	HD74LS95B	
	Motorola	SN74LS95	
	National	DM74LS95B	
	Signetics	74LS95B	
	TI	SN74LS95B	
74S240	AMD	SN74S240	
	Fairchild	74S240	
	MMI	**74S240**	**768**
	TI	SN74S240	
74S241	AMD	SN74S241	
	Fairchild	74S241	
	MMI	**74S241**	**768**
	TI	SN74S241	
74S244	AMD	SN74S244	
	MMI	**74S244**	**768**
♦7400 series	AMD	SN74XX	
	Fairchild	74XX	
	Ferranti	ZN74XX	
	Hitachi	HD74XX	
	Motorola	SN74XX	
	National	DM74XX	
	NEC America	μPB74XX	
	Signetics	74XX	
	TI	SN74XX	
9LS00	Fairchild	9LS00	
9LS02	Fairchild	9LS02	
9LS03	Fairchild	9LS03	
9LS04	Fairchild	9LS04	
9LS05	Fairchild	9LS05	
9LS08	Fairchild	9LS08	
9LS09	Fairchild	9LS09	
9LS10	Fairchild	9LS10	
9LS109	Fairchild	9LS109	
9LS11	Fairchild	9LS11	
9LS112	Fairchild	9LS112	
9LS113	Fairchild	9LS113	
9LS114	Fairchild	9LS114	
9LS132	Fairchild	9LS132	
9LS136	Fairchild	9LS136	
9LS138	Fairchild	9LS138	
9LS139	Fairchild	9LS139	
9LS14	Fairchild	9LS14	
9LS15	Fairchild	9LS15	
9LS151	Fairchild	9LS151	
9LS152	Fairchild	9LS159	
9LS153	Fairchild	9LS153	
9LS155	Fairchild	9LS155	
9LS156	Fairchild	9LS156	
9LS157	Fairchild	9LS157	
9LS158	Fairchild	9LS158	
9LS159	Fairchild	9LS159	
9LS160	Fairchild	9LS160	
9LS161	Fairchild	9LS161	
9LS162	Fairchild	9LS162	
9LS163	Fairchild	9LS163	
9LS164	Fairchild	9LS164	
9LS170	Fairchild	9LS170	
9LS173	Fairchild	9LS173	
9LS174	Fairchild	9LS174	
9LS175	Fairchild	9LS175	
9LS181	Fairchild	9LS181	
9LS190	Fairchild	9LS190	
9LS191	Fairchild	9LS191	
9LS192	Fairchild	9LS192	
9LS193	Fairchild	9LS193	
9LS194	Fairchild	9LS194	
9LS195	Fairchild	9LS195	
9LS196	Fairchild	9LS196	
9LS197	Fairchild	9LS197	
9LS20	Fairchild	9LS20	
9LS21	Fairchild	9LS21	
9LS22	Fairchild	9LS22	
9LS251	Fairchild	9LS251	
9LS253	Fairchild	9LS253	
9LS257	Fairchild	9LS257	
9LS258	Fairchild	9LS258	
9LS259	Fairchild	9LS259	
9LS266	Fairchild	9LS266	
9LS27	Fairchild	9LS27	
9LS279	Fairchild	9LS279	
9LS283	Fairchild	9LS283	
9LS295	Fairchild	9LS295	
9LS298	AMD	9LS298	
	Fairchild	9LS298	
9LS30	Fairchild	9LS30	
9LS32	Fairchild	9LS32	
9LS37	Fairchild	9LS37	
9LS38	Fairchild	9LS38	
9LS40	Fairchild	9LS40	
9LS42	Fairchild	9LS42	
9LS51	Fairchild	9LS51	
9LS54	Fairchild	9LS54	
9LS55	Fairchild	9LS55	
9LS670	Fairchild	9LS670	
9LS73	Fairchild	9LS73	
9LS74	Fairchild	9LS74	
9LS83	Fairchild	9LS83	
9LS86	Fairchild	9LS86	
9LS93	Fairchild	9LS93	
9LS95B	Fairchild	9LS95	
93415	Fujitsu	MBM93415	

RCA Solid State Division

Manufacturer Device	Replacement Source	Device	IC Master Page
Ca139A	PMI	CMP-04	
CA101	AD	AD101	
	AMD	LM101	
	Fairchild	μA101	
	Intersil	LM101	
	Motorola	LM101	
	National	**LM101**	**1035**
	NPC	SFC2121	
	Signetics	LM101	
	Silicon G	SG101	
	TI	LM101	
CA107	AMD	LM107	
	Intersil	LM107	
	Motorola	LM107	
	National	LM107	
	Raytheon	LM107	
	Signetics	LM107	
	Silicon G	SG107	
	TI	LM107	
CA108	AMD	LM108	
	Fairchild	μA108	
	Motorola	LM108	
	National	**LM108**	**1035**
	PMI	PM108	
	Raytheon	LM108	
	Signetics	LM108	
	Silicon G	SG108	
CA111	AMD	LM111	
	Intersil	LM111	
	Motorola	LM111	
	National	LM111	
	NPC	SFC2111	
	Raytheon	LM111	
	Signetics	LM111	
	Silicon G	SG111	
	TI	LM111	
CA1190	Sprague	ULN-2290	
CA1310	Motorola	MC1310	
	Sprague	ULN-2110	
		ULN-2210	
CA1352	Motorola	MC1352	
	Sanyo	LA1352	

♦ Discontinued

The manufacturers report their devices can be used as direct replacements.
Performance details often differ, so compare the specifications considering your requirements.

RCA Solid State Division (cont'd)

Manufacturer Device	Replacement Source	Device	IC Master Page
CA139	Motorola	LM139	
CA139A	PMI	PM139A	
CA1391	Motorola	MC1391	
	Sprague	ULN-2291	
CA1394	Motorola	MC1394	
	Sprague	ULN-2294	
CA1398	Motorola	MC1398	
	Sprague	ULN-2298	
CA1458	Exar	XR1458	
	Fairchild	μA1458	
	Harris	**HA-2655**	**986**
	Motorola	MC1458	
	National	LM1458	
	PMI	OP-14	
		SSS1458	
	Raytheon	RC1458	
	Signetics	MC1458	
	Silicon G	SG1458	
	TI	MC1458	
CA1541	Motorola	MC1441	
CA1558	Exar	XR1558	
	Fairchild	μA1558	
	Harris	**HA-2650**	**986**
	Motorola	MC1558	
	National	LM1558	
	PMI	PM1558	
		SSS1558	
	Raytheon	RM1558	
	Signetics	MC1558	
	Silicon G	SG1558	
	TI	MC1558	
CA2002	Sprague	ULN-3701	
CA201	AD	AD201	
	AMD	LM201	
	Fairchild	μA201	
	Intersil	LM201	
	Motorola	LM201	
	National	LM201	
	Signetics	LM201	
	Silicon G	SG201	
	TI	LM201	
CA207	AMD	LM207	
	Fairchild	μA207	
	Intersil	LM207	
	Motorola	LM207	
	National	LM207	
	Raytheon	LM207	
	Signetics	LM207	
	Silicon G	SG207	
	TI	LM207	
CA208	AD	AD208	
	AMD	LM208	
	Fairchild	μA208	
	Intersil	LM208	
	Motorola	LM208	
	National	LM208	
	NPC	SFC2208	
	PMI	PM208	
	Raytheon	LM208	
	Signetics	LM208	
	Silicon G	SG208	
CA211	AMD	LM211	
	Intersil	LM211	
	Motorola	LM211	
	National	LM211	
	NPC	SFC2211	
	Raytheon	LM211	
	Signetics	LM211	
	Silicon G	SG211	
	TI	LM211	
CA2111	Motorola	MC1357	
	Sprague	ULN-2111	
CA239	Motorola	LM239	
	Silicon G	SG239	
	TI	LM239	
CA239A	PMI	CMP-04	
		PM239A	
CA3001	Hitachi	HA1110	
	Silicon G	SG3001	
CA301	AD	AD301	
	Fairchild	μA301	
	Intersil	LM301	
CA301	Motorola	LM301	
	National	LM301	
	NPC	SFC2301	
	Raytheon	LM301	
	Signetics	LM301	
	Silicon G	SG301	
	TI	LM301	
CA3011	Motorola	MC1590	
CA3012	Motorola	MC1590	
CA3013	Motorola	MC1355	
CA3014	Motorola	MC1357	
CA3018	Fairchild	μA3018	
	NPC	SFC2018	
	Silicon G	SG3018	
CA3019	Fairchild	μA3019	
CA3026	Fairchild	μA3026	
	Silicon G	SG3822	
♦CA3032	Motorola	MC1712	
CA3036	Fairchild	μA3036	
	NPC	SFC2036	
CA3038	Motorola	MC1709	
CA3039	Fairchild	μA3039	
CA3044	Fairchild	μA3064	
	Mitsubishi	M5134	
CA3045	Fairchild	μA3045	
	Hitachi	HA1127	
	National	LM3045	
	Plessey	SL3045	
	Silicon G	SG3821	
	Sprague	ULS-2045	
CA3046	Fairchild	μA3046	
	Motorola	MC3346	
	National	LM3046	
	NPC	SFC2046	
	Plessey	SL3046	
	Silicon G	SG3821	
	Sprague	ULN-2046	
CA3054	Fairchild	μA3054	
	Motorola	CA3054	
	National	LM3054	
	NPC	SFC2054	
	Silicon G	SG3822	
	Sprague	ULN-2054	
CA3055	Silicon G	SG300	
CA3056	Motorola	MC1741	
	Silicon G	SG300	
CA3058	Silicon G	SG3058	
CA3059	Motorola	CA3059	
	Silicon G	SG3059	
CA3064	Fairchild	μA3064	
	Mitsubishi	M5135	
	Motorola	MC1364	
	Sprague	ULN-2264	
CA3065	Fairchild	μA3065	
	Motorola	MC1358	
		M5140	
	Sanyo	LA1365	
	Sprague	ULN-2165	
CA307	AMD	LM307	
	Fairchild	μA307	
	Intersil	LM307	
	Motorola	LM307	
	National	LM307	
	Raytheon	LM307	
	Signetics	LM307	
	Silicon G	SG307	
	TI	LM307	
CA3070	Fairchild	μA780	
	Sprague	ULN-2124	
CA3071	Fairchild	μA781	
	Sprague	ULN-2127	
CA3072	Fairchild	μA746	
	Sprague	ULN-2114	
		ULN-2228	
CA3075	Fairchild	μA3075	
	Motorola	MC1375	
CA3076	Fairchild	μA3076	
CA3078	Raytheon	RC3078	
CA3079	Silicon G	SG3079	
CA308	AD	AD308	
	AMD	LM308	
	Fairchild	μA308	
	Intersil	LM308	
	Motorola	LM308	
	National	LM308	
	NPC	SFC308	
CA308	PMI	PM308	
	Raytheon	LM308	
	Signetics	LM308	
	Silicon G	SG308	
CA3081	Plessey	SL3081	
	Silicon G	SG3081	
	Sprague	ULN-2081	
CA3082	Plessey	SL3082	
	Silicon G	SG3082	
	Sprague	ULN-2082	
CA3083	Plessey	SL3083	
	Signetics	CA3083	
	Silicon G	SG3083	
	Sprague	ULN-2083	
CA3086	Fairchild	μA3086	
	Motorola	MC3386	
	National	LM3086	
	Plessey	SL3086	
	Silicon G	SG3086	
	Sprague	ULN-2086	
CA3089	Fairchild	μA3089	
	SGS	TDA1200	
	Signetics	CA3089	
	Sprague	ULN-2289	
CA311	AMD	LM311	
	Fairchild	μA311	
	Intersil	LM311	
	Motorola	LM311	
	National	LM311	
	NPC	SFC3111	
	Raytheon	LM311	
	Signetics	LM311	
	Silicon G	SG311	
	TI	LM311	
CA3120	Sprague	ULN-2125	
CA3121	Sprague	ULN-2269	
CA3123	Sprague	ULN-2137	
CA3126	Fairchild	μA787	
CA3135	Sprague	ULN-2261	
CA3139	Motorola	CA3139	
CA3146	Plessey	SL3146	
	Silicon G	SG3146	
CA3162	AD	AD2020	
CA3170	Sprague	ULN-2268	
CA3172	Sprague	ULN-2229	
CA3183	Plessey	SL3183	
	Signetics	CA3183	
	Silicon G	SG3183	
CA324	Motorola	LM324	
	National	LM324	
	Signetics	LM324	
	Silicon G	SG324	
	TI	LM324	
CA3302	Motorola	MC3302	
	Silicon G	SG3302	
CA339	Motorola	LM339	
	National	LM339	
	Raytheon	LM339	
	Signetics	LM339	
	Silicon G	SG339	
	TI	LM339	
CA339A	PMI	CMP-04	
		PM339A	
CA3401	Motorola	MC3401	
CA3458	Exar	XR1458	
♦CA3458	RCA	CA1458	
CA3558	Exar	XR1558	
♦CA3558	RCA	CA1558	
♦CA3741	RCA	CA741	
♦CA3747	RCA	CA747	
♦CA3748	RCA	CA748	
CA555	AMD	NE555	
		SE555	
	Cherry	CS555	
	Exar	XR555	
	Intersil	NE555	
	Motorola	MC1455	
		MC1555	
	National	LM555	
	Raytheon	RC555	
		RM555	
	Signetics	NE555	
	Silicon G	SG555	
	TI	NE555	
		SE555	
CA723	AMD	723	
CA723	**Fairchild**	**μA723**	**934**
	Intersil	723	
	Motorola	MC1723	
	National	LM723	
	NPC	SFC2723	
	Raytheon	RC723	
	Signetics	μA723	
	Silicon G	SG723	
	TI	μA723	
CA741	AD	AD741	
	AMD	SSS741	
		741	
	Fairchild	μA741	
	Intersil	741	
	Motorola	MC1741	
	National	**LM741**	**1035**
	NPC	SFC2741	
	PMI	OP-02	
		PM741	
		SSS741	
	Raytheon	RC741	
		RM741	
	Signetics	μA741	
	Silicon G	SG741	
	TI	μA741	
CA747	AMD	SSS747	
		747	
	Fairchild	μA747	
	Motorola	MC1747	
	National	LM747	
	PMI	OP-04	
		PM747	
		SSS747	
	Raytheon	RC747	
		RM747	
	Signetics	μA747	
	Silicon G	SG747	
	TI	μA747	
CA748	AMD	748	
	Fairchild	μA748	
	Intersil	748	
	Motorola	MC1748	
	National	LM748	
	Raytheon	RC748	
		RM748	
	Signetics	μA748	
	Silicon G	SG748	
	TI	μA748	
CA758	Sprague	ULN-2244	
CA810	Motorola	MC1384	
	SGS	TBA810	
CDP1802	Hughes	HMPC1802	
	SSS	SCP1802	
CDP1821	SSS	SCP1821	
CDP1822	**AMI**	**S5101**	**1206**
	Fairchild	3538	
	Harris	**HM6501**	**1356**
	SSS	SCM5101	
		SCP1822	
CDP1824	Hughes	HCMP1824	
	SSS	SCP1824	
CDP1831	Hughes	HCMP1831	
	SSS	SCP1831	
CDP1832	Hughes	HCMP1832	
	SSS	SCP1832	
CDP1833	Hughes	HCMP1833	
	SSS	SCP1833	
CDP1834	Hughes	HCMP1834	
	SSS	SCP1834	
CDP1852	Hughes	HCMP1852	
	SSS	SCP1852	
CDP1853	Hughes	HCMP1853	
	SSS	SCP1853	
CDP1854	Hughes	HCMP1854	
	SSS	SCP1854	
CDP1856	Hughes	HCMP1856	
	SSS	SCP1856	
CDP1857	Hughes	HCMP1857	
	SSS	SCP1857	
CDP1858	Hughes	HCMP1858	
	SSS	SCP1858	
CDP1859	Hughes	HCMP1859	
	SSS	SCP1859	
CD4000	Motorola	MC14000	
	National	CD4000	

♦ Discontinued

Bold face device numbers indicate manufacturers data is provided in the IC Master on the pages noted.

RCA Solid State Division (cont'd)

Manufacturer Device	Replacement Source	Device	IC Master Page
CD4000	Solitron	CM4000	
	SSS	SCL4000	
	TI	TP4000	
CD4001	Fairchild	F4001	
	Hitachi	HD14001	
	Mitel	SIL4001	
		SIL4901	
	Motorola	MC14001	
	National	CD4001	
	NEC America	μPD4001	
	OKI	MSM4001	
	SGS	HBF4001	
	Solitron	CM4001	
	SSS	SCL4001	
	TI	TP4001	
	Toshiba	TC4001	
CD4002	Fairchild	F4002	
	Hitachi	HD14002	
	Mitel	SIL4002	
	Motorola	MC14002	
	National	CD4002	
	NEC America	μPD4002	
	OKI	MSM4002	
	SGS	HBF4002	
	Solitron	CM4002	
	SSS	SCL4002	
	TI	TP4002	
	Toshiba	TC4002	
CD4006	Fairchild	F4006	
	Motorola	MC14006	
	National	CD4006	
	NEC America	μPD4006	
	Solitron	CM4006	
	SSS	SCL4006	
	Toshiba	TC4006	
CD4007	Fairchild	F4007	
	Mitel	SIL4007	
	Motorola	MC14007	
	National	CD4007	
	OKI	MSM4007	
	SGS	HBF4007	
	Solitron	CM4007	
	SSS	SCL4007	
	TI	TP4007	
	Toshiba	TC4007	
CD4008	Fairchild	F4008	
	Hitachi	HD14008	
	Motorola	MC14008	
	National	CD4008	
	OKI	MSM4008	
	SGS	HBF4008	
	Solitron	CM4008	
	SSS	SCL4008	
	TI	TP4008	
	Toshiba	TC4008	
CD4009	Mitel	SIL4009	
	National	CD4009	
	SGS	HBF4009	
	Solitron	CM4009	
	SSS	SCL4009	
	TI	TP4009	
	Toshiba	TC4009	
CD4010	Mitel	SIL4010	
	National	CD4010	
	SGS	HBF4010	
	Solitron	CM4010	
	SSS	SCL4010	
	TI	TP4010	
	Toshiba	TC4010	
CD40100	Fairchild	F4583	
	Motorola	MC14583	
	Toshiba	TC4583	
CD40101	Fairchild	F4531	
	Motorola	MC14531	
	SSS	SCL4531	
	TI	TP4531	
CD40104	OKI	MSM40104	
CD40106	Motorola	MC14584	
	National	CD40106	
		MM74C14	**262**
CD40108	Motorola	MC14580	
CD4011	Fairchild	F4011	
CD4011	Hitachi	HD14011	
	Mitel	SIL4011	
		SIL4911	
	Motorola	MC14011	
	National	CD4011	
	NEC America	μPD4011	
	OKI	MSM4011	
		MSM4012	
	SGS	HBF4011	
	Solitron	CM4011	
	SSS	SCL4011	
	TI	TP4011	
	Toshiba	TC4011	
CD4012	Fairchild	F4012	
	Hitachi	HD14012	
	Mitel	SIL4012	
		SIL4912	
	Motorola	MC14012	
	National	CD4012	
	NEC America	μPD4012	
	SGS	HBF4012	
	Solitron	CM4012	
	SSS	SCL4012	
	TI	TP4012	
	Toshiba	TC4012	
CD4013	Fairchild	F4013	
	Hitachi	HD14013	
	Mitel	SIL4013	
	Motorola	MC14013	
	National	CD4013	
	NEC America	μPD4013	
	SGS	HBF4013	
	Solitron	CM4013	
	SSS	SCL4013	
	TI	TP4013	
	Toshiba	TC4013	
CD4014	Fairchild	F4014	
	Hitachi	HD14014	
	Mitel	SIL4014	
	Motorola	MC14014	
	National	CD4014	
	NEC America	μPD4014	
	OKI	MSM4014	
	SGS	HBF4014	
	Solitron	CM4014	
	SSS	SCL4014	
	TI	TP4014	
	Toshiba	TC4014	
CD4015	Fairchild	F4015	
	Hitachi	HD14015	
	Mitel	SIL4015	
	Motorola	MC14015	
	National	CD4015	
	NEC America	μPD4015	
	OKI	MSM4015	
	SGS	HBF4015	
	Solitron	CM4015	
	SSS	SCL4015	
	TI	TP4015	
	Toshiba	TC4015	
CD4016	AD	AD7516	
	Fairchild	F4016	
	Hitachi	HD14016	
	Micro Power	MP7516	
	Mitel	SIL4016	
	Motorola	MC14016	
		MC14584	
	National	**CD4016**	**1076**
		CD4584	
		MM74C14	**262**
	Solitron	CM4016	
	SSS	SCL4016	
		SCL4584	
	TI	TP4016	
CD40160	Fairchild	F40160	
	National	CD40160	
	Toshiba	TC40160	
CD40161	Fairchild	F40161	
	National	CD40161	
	Toshiba	TC40161	
CD40162	Fairchild	F40162	
	National	CD40162	
	Toshiba	TC40162	
CD40163	Fairchild	F40163	
	National	CD40163	
	Toshiba	TC40163	
CD4017	Fairchild	F4017	
	Hitachi	HD14017	
	Mitel	SIL4017	
	Motorola	MC14017	
	National	CD4017	
	NEC America	μPD4017	
	SGS	HBF4017	
	Solitron	CM4017	
	SSS	SCL4017	
	TI	TP4017	
	Toshiba	TC4017	
CD40174	Fairchild	F40174	
	National	CD40174	
CD4018	Fairchild	F4018	
		F4522	
	Mitel	SIL4018	
	Motorola	MC14018	
		MC14522	
	National	CD4018	
	SGS	HBF4018	
	Solitron	CM4018	
	SSS	SCL4018	
		SCL4522	
	TI	TP4018	
		TP4522	
	Toshiba	TC4018	
CD40181	Motorola	MC14581	
	SSS	SCL4581	
	TI	TP4581	
CD40182	Fairchild	F4582	
	Motorola	MC14582	
	SSS	SCL4582	
	TI	TP4582	
CD4019	Fairchild	F4019	
		F4519	
	Mitel	SIL4019	
	Motorola	MC14519	
	National	CD4019	
		CD4519	
	NEC America	μPD4019	
		μPD4519	
	OKI	MSM4019	
	SGS	HBF4019	
	Solitron	CM4019	
	SSS	SCL4019	
	TI	TP4019	
		TP4519	
	Toshiba	TC4019	
CD40192	Fairchild	F40192	
		F4510	
	Mitel	SIL4510	
	Motorola	MC14510	
	National	CD40192	
		CD4510	
		MM74C192	
	OKI	MSM40192	
	RCA	CD4510	
	SSS	SCL4510	
	Toshiba	TC4510	
CD40193	Fairchild	F40193	
		F4516	
	Mitel	SIL4516	
	Motorola	MC14516	
	National	CD40193	
		CD4516	
		MM74C193	
	RCA	CD4516	
	SSS	SCL4516	
	Toshiba	TC4516	
CD40194	Fairchild	F40194	
	Motorola	MC14194	
	OKI	MSM40194	
CD40196	Fairchild	F40196	
CD4020	Fairchild	F4020	
	Hitachi	HD14020	
	Mitel	SIL4020	
	Motorola	MC14020	
	National	CD4020	
	NEC America	μPD4020	
	OKI	MSM4020	
	SGS	HBF4020	
	Solitron	CM4020	
	SSS	SCL4020	
	TI	TP4020	
	Toshiba	TC4020	
CD4021	Fairchild	F4021	
CD4021	Hitachi	HD14021	
	Mitel	SIL4021	
	Motorola	MC14021	
	National	CD4021	
	NEC America	μPD4021	
	OKI	MSM4021	
	Solitron	CM4021	
	SSS	SCL4021	
	TI	TP4021	
	Toshiba	TC4021	
CD4022	Fairchild	F4022	
	Mitel	SIL4022	
	Motorola	MC14022	
	National	CD4022	
	OKI	MSM4022	
	SGS	HBF4022	
	Solitron	CM4022	
	SSS	SCL4022	
	TI	TP4022	
	Toshiba	TC4022	
CD4023	Fairchild	F4023	
	Hitachi	HD14023	
	Mitel	SIL4023	
		SIL4923	
	Motorola	MC14023	
	National	CD4023	
	NEC America	μPD4023	
	OKI	MSM4023	
	SGS	HBF4023	
	Solitron	CM4023	
	SSS	SCL4023	
	TI	TP4023	
	Toshiba	TC4023	
CD4024	Fairchild	F4024	
	Mitel	SIL4024	
	Motorola	MC14024	
	National	CD4024	
	NEC America	μPD4024	
	OKI	MSM4024	
	SGS	HBF4024	
	Solitron	CM4024	
	SSS	SCL4024	
	TI	TP4024	
	Toshiba	TC4024	
CD4025	Fairchild	F4025	
	Hitachi	HD14025	
	Mitel	SIL4025	
		SIL4925	
	Motorola	MC14025	
	National	CD4025	
	NEC America	μPD4025	
	OKI	MSM4025	
	SGS	HBF4025	
	Solitron	CM4025	
	SSS	SCL4025	
	TI	TP4025	
	Toshiba	TC4025	
CD4026	Solitron	CM4026	
	SSS	SCL4026	
CD4027	Fairchild	F4027	
	Hitachi	HD14027	
	Mitel	SIL4027	
	Motorola	MC14027	
	National	CD4027	
	NEC America	μPD4027	
	OKI	MSM4027	
	SGS	HBF4027	
	Solitron	CM4027	
	SSS	SCL4027	
	TI	TP4027	
	Toshiba	TC4027	
CD4028	Fairchild	F4028	
	Hitachi	HD14028	
	Mitel	SIL4028	
	Motorola	MC14028	
	National	CD4028	
	NEC America	μPD4028	
	OKI	MSM4028	
	SGS	HBF4028	
	Solitron	CM4028	
	SSS	SCL4028	
	TI	TP4028	
	Toshiba	TC4028	
CD4029	Fairchild	F4029	
	Mitel	SIL4029	
	Motorola	MC14510	

♦ Discontinued

The manufacturers report their devices can be used as direct replacements.
Performance details often differ, so compare the specifications considering your requirements.

RCA Solid State Division (cont'd)

Manufacturer Device	Replacement Source	Device	IC Master Page
CD4029	National	CD4029	
	NEC America	μPD4029	
	OKI	MSM4029	
	SGS	HBF4029	
	Solitron	CM4029	
	SSS	SCL4029	
	TI	TP4029	
	Toshiba	TC4029	
CD4030	Fairchild	F4030	
	Mitel	SIL4030	
	Motorola	MC14070	
		MC14507	
	National	CD4030	
		CD4070	
		CD4507	
		MM74C86	
	NEC America	μPD4030	
	OKI	MSM4030	
	RCA	CD4070	
	SGS	HBF4030	
	Solitron	CM4030	
	SSS	SCL4030	
	TI	TP4030	
		TP4507	
	Toshiba	TC4030	
CD4031	Fairchild	F4031	
		F4557	
	Motorola	MC14557	
	National	CD4031	
CD4032	Motorola	MC14032	
	OKI	MSM4032	
	Solitron	CM4032	
	Toshiba	TC4032	
CD4033	SGS	HBF4033	
	Solitron	CM4033	
	SSS	SCL4033	
CD4034	Fairchild	F4034	
	Hitachi	HD14034	
	Motorola	MC14034	
	National	CD4034	
	OKI	MSM4034	
	Solitron	CM4034	
	SSS	SCL4034	
	Toshiba	TC4034	
CD4035	Fairchild	F4035	
	Hitachi	HD14035	
	Mitel	SIL4035	
	Motorola	MC14035	
	National	CD4035	
	NEC America	μPD4035	
	OKI	MSM4035	
	SGS	HBF4035	
	Solitron	CM4035	
	SSS	SCL4035	
	TI	TP4035	
	Toshiba	TC4035	
CD4036	Toshiba	TC4036	
CD4038	Motorola	MC14038	
		MC14308	
	OKI	MSM4038	
	Solitron	CM4038	
	Toshiba	TC4038	
CD4039	Solitron	CM4039	
	Toshiba	TC4039	
CD4040	Fairchild	F4040	
	Hitachi	HD14040	
	Mitel	SIL4040	
	Motorola	MC14040	
	National	CD4040	
	NEC America	μPD4040	
	OKI	MSM4040	
	Solitron	CM4040	
	SSS	SCL4040	
	TI	TP4040	
	Toshiba	TC4040	
CD4041	Fairchild	F4041	
	National	CD4041	
	Solitron	CM4041	
	SSS	CL4041	
		SCL4041	
CD4042	Fairchild	F4042	
	Hitachi	HD14042	
CD4042	Mitel	SIL4042	
	Motorola	MC14042	
	National	CD4042	
	NEC America	μPD4042	
	OKI	MSM4042	
	SGS	HBF4042	
	Solitron	CM4042	
	SSS	SCL4042	
	TI	TP4042	
	Toshiba	TC4042	
CD4043	Fairchild	F4043	
	Hitachi	HD14043	
	Mitel	SIL4043	
	Motorola	MC14043	
	National	CD4043	
	NEC America	μPD4043	
	OKI	MSM4043	
	Solitron	CM4043	
	SSS	SCL4043	
	TI	TP4043	
	Toshiba	TC4043	
CD4044	Fairchild	F4044	
	Hitachi	HD14044	
	Mitel	SIL4044	
	Motorola	MC14044	
	National	CD4044	
	NEC America	μPD4044	
	OKI	MSM4044	
	Solitron	CM4044	
	SSS	SCL4044	
	TI	TP4044	
	Toshiba	TC4044	
CD4045	SGS	HBF4045	
	Solitron	CM4045	
	SSS	SCL4445	
CD4046	Fairchild	F4046	
	Mitel	SIL4046	
	Motorola	MC14046	
	National	CD4046	
	Solitron	CM4046	
	SSS	SCL4046	
CD4047	Fairchild	F4047	
	National	CD4047	
	Solitron	CM4047	
	SSS	SCL4047	
	Toshiba	TC4047	
CD4048	National	CD4048	
	Solitron	CM4048	
CD4049	Fairchild	F4049	
	Hitachi	HD14049	
	Mitel	SIL4049	
	Motorola	MC14049	
	National	CD4049	
	NEC America	μPD4049	
	OKI	MSM4049	
	SGS	HBF4049	
	Solitron	CM4049	
	SSS	SCL4049	
	TI	TP4049	
	Toshiba	TC4049	
CD4050	Fairchild	F4050	
	Hitachi	HD14050	
	Mitel	SIL4050	
	Motorola	MC14050	
	National	CD4050	
	NEC America	μPD4050	
	OKI	MSM4050	
	SGS	HBF4050	
	Solitron	CM4050	
	SSS	SCL4050	
	TI	TP4050	
	Toshiba	TC4050	
CD4051	Fairchild	F4051	
	Hitachi	HD14051	
	Mitel	SIL4051	
	Motorola	MC14051	
	National	CD4051	
	NEC America	μPD4051	
	Solitron	CM4051	
	SSS	SCL4051	
	TI	TP4051	
	Toshiba	TC4051	
CD4052	Fairchild	F4052	
	Hitachi	HD14052	
	Mitel	SIL4052	
	Motorola	MC14052	
CD4052	National	CD4052	
	NEC America	μPD4052	
	Solitron	CM4052	
	SSS	SCL4052	
	TI	TP4052	
	Toshiba	TC4052	
CD4053	Fairchild	F4053	
	Hitachi	HD14053	
	Mitel	SIL4053	
	Motorola	MC14053	
	National	CD4053	
	NEC America	μPD4053	
	Solitron	CM4053	
	SSS	SCL4053	
	TI	TP4053	
	Toshiba	TC4053	
CD4054	OKI	MSM4054	
	Toshiba	TC4054	
CD4055	Mitel	SIL4055	
	Motorola	MC14558	
	Toshiba	TC4055	
CD4056	Mitel	SIL4056	
	Motorola	MC14543	
	SSS	SCL4543	
	Toshiba	TC4056	
CD4059	OKI	MSM4059	
CD4060	Mitel	SIL4060	
	National	CD4060	
	SSS	SCL4060	
CD4061	OKI	MSM4061	
	Toshiba	TC4061	
CD4062	Motorola	MC14562	
CD4063	Motorola	MC14066	
		MC14585	
	National	MM74C85	
	NEC America	μPD4063	
	OKI	MSM4063	
	SGS	HBF4066	
	Signetics	N4066	
	Solitron	CM4066	
	SSS	SCL4066	
		SCL4585	
	Toshiba	TC4063	
		TC4066	
		TC4585	
CD4066	Fairchild	F4066	
	Hitachi	HD14066	
	Mitel	SIL4066	
	Motorola	MC14066	
	National	**CD4066**	**1076**
	NEC America	μPD4066	
	SGS	HBF4066	
	Signetics	N4066	
	Solitron	CM4066	
		CM4116	
	SSS	SCL4066	
	Toshiba	TC4066	
CD4067	Fairchild	F4067	
	Motorola	MC14529	
CD4068	Fairchild	F4068	
	Hitachi	HD14068	
	Mitel	SIL4068	
	Motorola	MC14068	
		MC14501	
	NEC America	μPD4068	
	OKI	MSM4068	
	Solitron	CM4068	
	SSS	SCL4068	
	TI	TP4068	
	Toshiba	TC4068	
CD4069	Fairchild	F4069	
	Harris	HD4069	
		HD54C04	
		HD74C04	
	Hitachi	HD14069	
	Mitel	SIL4069	
	Motorola	MC14069	
	National	CD4069	
		MM54C04	
		MM74C04	
	NEC America	μPD4069	
	OKI	MSM4069	
	Solitron	CM4069	
	SSS	SCL4069	
	TI	TP4069	
	Toshiba	TC4069	
CD4070	Fairchild	F4070	
	Hitachi	HD14070	
	Mitel	SIL4070	
	Motorola	MC14507	
	National	CD4070	
		CD4507	
		MM74C86	
	RCA	CD4030	
	Solitron	CM4030	
		CM4070	
	SSS	SCL4030	
		SCL4070	
	TI	TP4507	
CD4070A	Motorola	MC14070	
CD4071	Fairchild	F4071	
	Hitachi	HD14071	
	Mitel	SIL4071	
	Motorola	MC14071	
	National	CD4071	
	NEC America	μPD4071	
	OKI	MSM4071	
	Solitron	CM4071	
	SSS	SCL4071	
	TI	TP4071	
	Toshiba	TC4071	
CD4072	Fairchild	F4072	
	Hitachi	HD14072	
	Mitel	SIL4072	
	Motorola	MC14072	
	OKI	MSM4072	
	SSS	SCL4072	
	TI	TP4072	
	Toshiba	TC4072	
CD4073	Fairchild	F4073	
	Hitachi	HD14073	
	Mitel	SIL4073	
	Motorola	MC14073	
	National	CD4073	
	NEC America	μPD4073	
	OKI	MSM4073	
	Solitron	CM4073	
	SSS	SCL4073	
	TI	TP4073	
	Toshiba	TC4073	
CD4075	Fairchild	F4075	
	Hitachi	HD14075	
	Mitel	SIL4075	
	Motorola	MC14075	
	National	CD4075	
	NEC America	μPD4075	
	OKI	MSM4075	
	SSS	SCL4075	
	TI	TP4075	
	Toshiba	TC4075	
CD4076	Fairchild	F4076	
	Harris	HD54C173	
		HD74C173	
	Mitel	SIL4076	
	Motorola	MC14076	
	National	CD4076	
		MM54C173	
		MM74C173	
	Solitron	CM4076	
	SSS	SCL4076	
CD4077	Fairchild	F4077	
	Hitachi	HD14077	
	Mitel	SIL4077	
	Motorola	MC14077	
	Solitron	CM4077	
	SSS	SCL4077	
CD4078	Fairchild	F4078	
	Hitachi	HD14078	
	Mitel	SIL4078	
	Motorola	MC14078	
	NEC America	μPD4078	
	OKI	MSM4078	
	Solitron	CM4078	
	SSS	SCL4078	
	TI	TP4078	
	Toshiba	TC4078	
CD4081	Fairchild	F4081	
	Hitachi	HD14081	
	Mitel	SIL4081	
	Motorola	MC14081	
	National	CD4081	
	NEC America	μPD4081	

♦ Discontinued

Bold face device numbers indicate manufacturers data is provided in the IC Master on the pages noted.

RCA Solid State Division (cont'd)

Manufacturer Device	Replacement Source	Device	IC Master Page
CD4081	OKI	MSM4081	
	Solitron	CM4081	
	SSS	SCL4081	
	TI	TP4081	
	Toshiba	TC4081	
CD4082	Fairchild	F4082	
	Hitachi	HD14082	
	Mitel	SIL4082	
	Motorola	MC14082	
	NEC America	μPD4082	
	SSS	SCL4082	
	TI	TP4082	
	Toshiba	TC4082	
CD4085	Fairchild	F4085	
	Motorola	MC14506	
	OKI	MSM4085	
	Toshiba	TC4085	
CD4086	Fairchild	F4086	
	OKI	MSM4086	
	Toshiba	TC4086	
CD4089	National	CD4089	
CD4093	Fairchild	F4093	
	Motorola	MC14093	
	National	CD4093	
	NEC America	μPD4093	
	OKI	MSM4093	
	SSS	SCL4093	
	Toshiba	TC4093	
CD4094	NEC America	μPD4094	
	OKI	MSM4094	
	SSS	SCL4094	
CD4098	Mitel	SIL4098	
	Motorola	MC14528	
CD4099	Fairchild	F4099	
	Motorola	MC14099	
	National	CD4099	
	NEC America	μPD4099	
CD4174	Hitachi	HD14174	
CD4175	Hitachi	HD14175	
CD4194	Hitachi	HD14194	
	NEC America	μPD4194	
CD4501	Hitachi	HD14501	
CD4502	Hitachi	HD14502	
	Mitel	SIL4502	
	Motorola	MC14502	
	OKI	MSM4502	
	SSS	SCL4502	
CD4508	Hitachi	HD14508	
	Mitel	SIL4508	
	Motorola	MC14508	
	NEC America	μPD4508	
	OKI	MSM4508	
	Solitron	CM4508	
	SSS	SCL4508	
	Toshiba	TC4508	
CD4510	Fairchild	F4510	
	Mitel	SIL4510	
	Motorola	MC14510	
	National	CD4510	
	NEC America	μPD4510	
	OKI	MSM4510	
	RCA	CD40192	
	SSS	SCL4510	
	Toshiba	TC4510	
CD4511	Fairchild	F4511	
	Hitachi	HD14511	
	Mitel	SIL4511	
	Motorola	MC14511	
	National	CD4511	
	NEC America	μPD4511	
	OKI	MSM4511	
	Solitron	CM4511	
	SSS	SCL4511	
	TI	TP4511	
CD4512	Hitachi	HD14512	
	OKI	MSM4512	
CD4514	Fairchild	F4514	
	Mitel	SIL4514	
	Motorola	MC14514	
	National	CD4514	
	NEC America	μPD4514	
	OKI	MSM4514	
CD4514	Solitron	CM4514	
	SSS	SCL4514	
	Toshiba	TC4514	
CD4515	Fairchild	F4515	
	Hitachi	HD14515	
	Mitel	SIL4515	
	Motorola	MC14515	
	National	CD4515	
	NEC America	μPD4515	
	OKI	MSM4515	
	Solitron	CM4515	
	SSS	SCL4515	
	Toshiba	TC4515	
CD4516	Fairchild	F4516	
	Hitachi	HD14516	
	Mitel	SIL4516	
	Motorola	MC14516	
	National	CD4516	
	NEC America	μPD4516	
	OKI	MSM4516	
	RCA	CD40193	
	SSS	SCL4516	
	Toshiba	TC4516	
CD4518	Fairchild	F4518	
	Mitel	SIL4518	
	Motorola	MC14518	
	National	CD4518	
	NEC America	μPD4518	
	OKI	MSM4518	
	Solitron	CM4518	
	SSS	SCL4518	
	TI	TP4518	
	Toshiba	TC4518	
CD4519	Hitachi	HD14519	
CD4520	Fairchild	F4520	
	Hitachi	HD14520	
	Mitel	SIL4520	
	Motorola	MC14520	
	National	CD4520	
	NEC America	μPD4520	
	OKI	MSM4520	
	Solitron	CM4520	
	SSS	SCL4520	
	TI	TP4520	
	Toshiba	TC4520	
CD4527	Motorola	MC14527	
	National	CD4527	
	SSS	SCL4527	
	Toshiba	TR4527	
CD4528	Fairchild	F4528	
	Hitachi	HD14528	
	Motorola	MC14528	
	National	CD4528	
	NEC America	μPD4528	
	SSS	SCL4528	
	Toshiba	TC4528	
CD4532	Fairchild	F4532	
	Hitachi	HD15532	
	Motorola	MC14532	
	NEC America	μPD4532	
	OKI	MSM4532	
	SSS	SCL4532	
	Toshiba	TC4532	
CD4555	Fairchild	F4555	
	Hitachi	HD14555	
	Motorola	MC14555	
	NEC America	μPD4555	
	OKI	MSM4555	
	SSS	SCL4555	
	Toshiba	TC4555	
CD4556	Fairchild	F4556	
	Motorola	MC14556	
	NEC America	μPD4556	
	OKI	MSM4556	
	SSS	SCL4556	
	Toshiba	TC4556	
CD4560	Hitachi	HD14560	
CD4561	Hitachi	HD14561	
CD4572	Hitachi	HD14572	
CD4583	Hitachi	HD14583	
CD4584	Hitachi	HD14584	
CD4585	Hitachi	HD14585	
CPP1852	SSS	SCP1852	
MWS5040	**Harris**	**HM6501**	**1356**
MWS5101	SSS	SCM5101	

RIFA

Manufacturer Device	Replacement Source	Device	IC Master Page
PBD352301	Sprague	ULN-2001	
PBD352302	Sprague	ULN-2002	
PBD352303	Sprague	ULN-2003	

Rockwell, Microelectronic Devices

Manufacturer Device	Replacement Source	Device	IC Master Page
R2332	**AMI**	**S68332**	**1216**
R6502	MOS	MCS6502	
	Synertek	SY6502	
R6503	MOS	MCS6503	
	Synertek	SY6503	
R6504	MOS	MCS6504	
	Synertek	SY6504	
R6505	MOS	MCS6505	
	Synertek	SY6505	
R6512	MOS	MCS6512	
	Synertek	SY6512	
R6514	MOS	MCS6514	
	Synertek	SY6514	
R6515	MOS	SY6515	
	Synertek	SY6515	
R6520	MOS	MCS6520	
	Synertek	SY6520	
R6530	MOS	MCS6530	
	Synertek	SY6530	
R6532	MOS	MCS6532	
	Synertek	SY6532	
♦1103	AMI	S1103	
♦1103A	AMI	S1103	
	Intel	1103	
	Synertek	1103	
♦1604	EA	EA4096	

Sanyo

Manufacturer Device	Replacement Source	Device	IC Master Page
LA1230	Hitachi	HA1137	
LA1240	Hitachi	HA1197	
LA1352	Motorola	MC1352	
	RCA	CA1352	
LA1353	Motorola	MC1353	
LA1365	Fairchild	μA3065	
	RCA	CA3065	

SGS-ATES Semiconductor

Manufacturer Device	Replacement Source	Device	IC Master Page
HBF4001	Fairchild	F4001	
	Mitel	SIL4001	
	Motorola	MC14001	
	National	CD4001	
	NEC America	μPD4001	
	RCA	CD4001	
	Solitron	CM4001	
	SSS	SCL4001	
	TI	TP4001	
	Toshiba	TC4001	
HBF4002	Fairchild	F4002	
	Mitel	SIL4002	
	Motorola	MC14002	
	National	CD4002	
	NEC America	μPD4002	
	RCA	CD4002	
	Solitron	CM4002	
	SSS	SCL4002	
	TI	TP4002	
	Toshiba	TC4002	
HBF4007	Fairchild	F4007	
	Mitel	SIL4007	
	Motorola	MC14007	
	National	CD4007	
	RCA	CD4007	
	Solitron	CM4007	
	SSS	SCL4007	
	TI	TP4007	
	Toshiba	TC4007	
HBF4008	Fairchild	F4008	
	Motorola	MC14008	
	National	CD4008	
	RCA	CD4008	
	Solitron	CM4008	
HBF4008	SSS	SCL4008	
	TI	TP4008	
	Toshiba	TC4008	
HBF4009	Mitel	SIL4009	
	National	CD4009	
	RCA	CD4009	
	Solitron	CM4009	
	SSS	SCL4009	
	TI	TP4009	
	Toshiba	TC4009	
HBF4010	Mitel	SIL4010	
	National	CD4010	
	RCA	CD4010	
	Solitron	CM4010	
	SSS	SCL4010	
	TI	TP4010	
	Toshiba	TC4010	
HBF4011	Fairchild	F4011	
	Mitel	SIL4011	
	Motorola	MC14011	
	National	CD4011	
	NEC America	μPD4011	
	RCA	CD4011	
	Solitron	CM4011	
	SSS	SCL4011	
	TI	TP4011	
	Toshiba	TC4011	
HBF4012	Fairchild	F4012	
	Mitel	SIL4012	
	Motorola	MC14012	
	National	CD4012	
	NEC America	μPD4012	
	RCA	CD4012	
	Solitron	CM4012	
	SSS	SCL4012	
	TI	TP4012	
	Toshiba	TC4012	
HBF4013	Fairchild	F4013	
	Mitel	SIL4013	
	Motorola	MC14013	
	National	CD4013	
	NEC America	μPD4013	
	RCA	CD4013	
	Solitron	CM4013	
	SSS	SCL4013	
	TI	TP4013	
	Toshiba	TC4013	
HBF4014	Fairchild	F4014	
	Mitel	SIL4014	
	Motorola	MC14014	
	National	CD4014	
	NEC America	μPD4014	
	RCA	CD4014	
	Solitron	CM4014	
	SSS	SCL4014	
	TI	TP4014	
	Toshiba	TC4014	
HBF4015	Fairchild	F4015	
	Mitel	SIL4015	
	Motorola	MC14015	
	National	CD4015	
	NEC America	μPD4015	
	RCA	CD4015	
	Solitron	CM4015	
	SSS	SCL4015	
	TI	TP4015	
	Toshiba	TC4015	
HBF4016	RCA	CD4016	
		CD4066	
	SSS	SCL4016	
HBF4017	Fairchild	F4017	
	Mitel	SIL4017	
	Motorola	MC14017	
	National	CD4017	
	NEC America	μPD4017	
	RCA	CD4017	
	Solitron	CM4017	
	SSS	SCL4017	
	TI	TP4017	
	Toshiba	TC4017	
HBF4018	Fairchild	F4018	
	Mitel	SIL4018	
	National	CD4018	
	RCA	CD4018	
	Solitron	CM4018	
	SSS	SCL4018	

♦ Discontinued

The manufacturers report their devices can be used as direct replacements.
Performance details often differ, so compare the specifications considering your requirements.

SGS-ATES Semiconductor (cont'd)

Manufacturer Device	Replacement Source	Device	IC Master Page
HBF4018	TI	TP4018	
	Toshiba	TC4018	
HBF4019	Fairchild	F4019	
	Mitel	SIL4019	
	National	CD4019	
	RCA	CD4019	
	Solitron	CM4019	
	SSS	SCL4019	
	TI	TP4019	
	Toshiba	TC4019	
HBF4020	Fairchild	F4020	
	Mitel	SIL4020	
	Motorola	MC14020	
	National	CD4020	
	NEC America	μPD4020	
	RCA	CD4020	
	Solitron	CM4020	
	SSS	SCL4020	
	TI	TP4020	
	Toshiba	TC4020	
HBF4021	RCA	CD4021	
	SSS	SCL4021	
HBF4022	Fairchild	F4022	
	Mitel	SIL4022	
	Motorola	MC14022	
	National	CD4022	
	RCA	CD4022	
	Solitron	CM4022	
	SSS	SCL4022	
	TI	TP4022	
	Toshiba	TC4022	
HBF4023	Fairchild	F4023	
	Mitel	SIL4023	
	Motorola	MC14023	
	National	CD4023	
	NEC America	μPD4023	
	RCA	CD4023	
	Solitron	CM4023	
	SSS	SCL4023	
	TI	TP4023	
	Toshiba	TC4023	
HBF4024	Fairchild	F4024	
	Mitel	SIL4024	
	Motorola	MC14024	
	National	CD4024	
	RCA	CD4024	
	Solitron	CM4024	
	SSS	SCL4024	
	TI	TP4024	
	Toshiba	TC4024	
HBF4025	Fairchild	F4025	
	Mitel	SIL4025	
	Motorola	MC14025	
	National	CD4025	
	NEC America	μPD4025	
	RCA	CD4025	
	Solitron	CM4025	
	SSS	SCL4025	
	TI	TP4025	
	Toshiba	TC4025	
HBF4027	Fairchild	F4027	
	Mitel	SIL4027	
	Motorola	MC14027	
	National	CD4027	
	NEC America	μPD4027	
	RCA	CD4027	
	Solitron	CM4027	
	SSS	SCL4027	
	TI	TP4027	
	Toshiba	TC4027	
HBF4028	Fairchild	F4028	
	Mitel	SIL4028	
	Motorola	MC14028	
	National	CD4028	
	NEC America	μPD4028	
	RCA	CD4028	
	Solitron	CM4028	
	SSS	SCL4028	
	TI	TP4028	
	Toshiba	TC4028	
HBF4029	Fairchild	F4029	
	Mitel	SIL4029	
HBF4029	National	CD4029	
	NEC America	μPD4029	
	RCA	CD4029	
	Solitron	CM4029	
	SSS	SCL4029	
	TI	TP4029	
	Toshiba	TC4029	
HBF4030	Fairchild	F4030	
	Mitel	SIL4030	
	National	CD4030	
	NEC America	μPD4030	
	RCA	CD4030	
	Solitron	CM4030	
	SSS	SCL4030	
	TI	TP4030	
	Toshiba	TC4030	
HBF4033	RCA	CD4033	
	Solitron	CM4033	
	SSS	SCL4033	
HBF4035	Fairchild	F4035	
	Mitel	SIL4035	
	Motorola	MC14035	
	National	CD4035	
	NEC America	μPD4035	
	RCA	CD4035	
	Solitron	CM4035	
	SSS	SCL4035	
	TI	TP4035	
	Toshiba	TC4035	
HBF4040	RCA	CD4040	
	SSS	SCL4040	
HBF4042	Fairchild	F4042	
	Mitel	SIL4042	
	Motorola	MC14042	
	National	CD4042	
	NEC America	μPD4042	
	RCA	CD4042	
	Solitron	CM4042	
	SSS	SCL4042	
	TI	TP4042	
	Toshiba	TC4042	
HBF4045	RCA	CD4045	
	Solitron	CM4045	
	SSS	SCL4445	
HBF4049	Fairchild	F4049	
	Mitel	SIL4049	
	Motorola	MC14049	
	National	CD4049	
	NEC America	μPD4049	
	RCA	CD4049	
	Solitron	CM4049	
	SSS	SCL4049	
	TI	TP4049	
	Toshiba	TC4049	
HBF4050	Fairchild	F4050	
	Mitel	SIL4050	
	Motorola	MC14050	
	National	CD4050	
	NEC America	μPD4050	
	RCA	CD4050	
	Solitron	CM4050	
	SSS	SCL4050	
	TI	TP4050	
	Toshiba	TC4050	
HBF4066	Fairchild	F4066	
	Mitel	SIL4066	
	Motorola	MC14066	
	National	**CD4066**	**1076**
	NEC America	μPD4066	
	RCA	CD4063	
		CD4066	
	Signetics	N4066	
	Solitron	CM4066	
	SSS	SCL4066	
	Toshiba	TC4066	
L201	**Exar**	**XR2201**	**931**
	Fairchild	9665	
	Motorola	MC1411	
	Silicon G	SG2001	
	Sprague	ULN-2001	
	TI	ULN2001	
L202	**Exar**	**XR2202**	**931**
	Fairchild	9666	
	Motorola	MC1412	
	Silicon G	SG2002	
	Sprague	ULN-2002	
L202	TI	ULN2002	
L203	**Exar**	**XR2203**	**931**
	Fairchild	9667	
	Motorola	MC1413	
	Silicon G	SG2003	
	Sprague	ULN-2003	
	TI	ULN2003	
M142	TI	TMS3120	
M340	Fujitsu	MB8107	
TBA641	**Fairchild**	**μA706**	**937**
		TBA641	**937**
TBA800	**Fairchild**	**TBA800**	**937**
	NPC	TBA800	
	Plessey	TBA800	
TBA810	**Fairchild**	**TBA810**	**936**
	Motorola	MC1384	
	RCA	CA810	
	SGS	TBA810	
	Signetics	TBA810	
TCA3089	Sprague	ULN-2289	
TCA900	NPC	TCA900	
TDA1190	Sprague	ULN-2290	
TDA1190Z	Sprague	ULN-2290	
TDA1200	Sprague	ULN-2289	
TDA2002	Sprague	ULN-3701	
142	TI	TMS3404	

Siemens

GXB10147	Fujitsu	MB7047	
HYB4060	Fujitsu	MB8107	
TBA120	Plessey	TBA120	
TBA221	Sprague	ULN-2151	
TBA440	Plessey	TBA440	
TCA440	Signetics	TCA440	

Signetics

μA709	Fairchild	μA709	
	Motorola	MC1709	
	National	**LM709**	**1035**
	Raytheon	RC709	
		RM709	
	TI	μA709	
μA710	Fairchild	μA710	
	Motorola	MC1710	
	National	LM710	
	Raytheon	RC710	
		RM710	
	Silicon G	SG710	
	TI	μA710	
μA711	Fairchild	μA711	
	Motorola	MC1711	
	National	LM711	
	Raytheon	RC711	
		RM711	
	Silicon G	SG711	
	TI	μA711	
μA723	AMD	723	
	Fairchild	**μA723**	**934**
	Intersil	723	
	Motorola	MC1723	
	National	LM723	
	Raytheon	RC723	
		RM723	
	RCA	CA723	
	Silicon G	SG723	
	TI	μA723	
μA733	AMD	733	
	Motorola	MC1733	
	National	LM733	
	Raytheon	RC733	
		RM733	
	Silicon G	SG733	
	TI	μA733	
μA740	Fairchild	μA740	
	Intersil	740	
	National	LH740	
μA741	AD	AD741	
	AMD	741	
	Fairchild	μA741	
	Intersil	741	
	Motorola	MC1741	
	National	**LM741**	**1035**
μA741	PMI	SSS741	
	Raytheon	RC741	
		RM741	
	RCA	CA741	
	Silicon G	SG741	
	TI	μA741	
μA747	AMD	747	
	Fairchild	μA747	
	Motorola	MC1747	
	National	LM747	
	PMI	SSS747	
	Raytheon	RC747	
		RM747	
	RCA	CA747	
	Silicon G	SG747	
	TI	μA747	
μA748	AMD	748	
	Fairchild	μA748	
	Intersil	748	
	Motorola	MC1748	
	National	LM748	
	Raytheon	RC748	
		RM748	
	RCA	CA748	
	Silicon G	SG748	
	TI	μA748	
μA78G	**Fairchild**	**μA78G**	**934**
μA78L02	TI	μA78L02	
μA78L05	Fairchild	μA78L05	
	Silicon G	SG7805	
	TI	μA78L05	
μA78L06	Silicon G	SG7806	
	TI	μA78L06	
μA78L12	Fairchild	μA78L12	
	Silicon G	SG7812	
	TI	μA78L12	
μA78L15	Fairchild	μA78L15	
	Silicon G	SG7815	
	TI	μA78L15	
μA78L62	Fairchild	μA78L06	
μA78MG	**Fairchild**	**μA78MG**	**934**
μA78M05	Fairchild	μA78M05	
	Silicon G	SG7805	
	TI	μA78M05	
μA78M06	Fairchild	μA78M06	
	Silicon G	SG7806	
	TI	μA78M06	
μA78M08	Fairchild	μA78M08	
	TI	μA78M08	
μA78M12	Fairchild	μA78M12	
	TI	μA78M12	
μA78M15	Fairchild	μA78M15	
	TI	μA78M15	
μA78M20	Fairchild	μA78M20	
	TI	μA78M20	
μA78M24	Fairchild	μA78M24	
	Silicon G	SG7824	
	TI	μA78M24	
μA7805	Fairchild	μA7805	
	Silicon G	SG7805	
	TI	μA7805	
μA7806	Fairchild	μA7806	
	Silicon G	SG7806	
	TI	μA7806	
μA7808	Fairchild	μA7808	
	Silicon G	SG7808	
	TI	μA7808	
μA7809	TI	μA7805	
μA7812	Fairchild	μA7812	
	Silicon G	SG7812	
	TI	μA7812	
μA7815	Fairchild	μA7815	
	Silicon G	SG7815	
	TI	μA7815	
μA7818	Fairchild	μA7818	
	Silicon G	SG7818	
	TI	μA7818	
μA7824	Fairchild	μA7824	
	Silicon G	SG7824	
	TI	μA7824	
μA79G	**Fairchild**	**μA79G**	**934**
μA79L05	Motorola	MC79L05	
μA79L12	Motorola	MC79L12	
μA79L15	Motorola	MC79L15	
μA79MG	**Fairchild**	**μA79MG**	**934**
μ78M08	Silicon G	SG7808	

♦ Discontinued

Bold face device numbers indicate manufacturers data is provided in the IC Master on the pages noted.

Signetics (cont'd)

Manufacturer Device	Replacement Source	Device	IC Master Page
μ78M12	Silicon G	SG7812	
μ78M15	Silicon G	SG7815	
7521	AMD	SN7521	
DM7577	AMD	AM27S18	
DM7820	AMD	DM7820	
	TI	SN55182	
DM7830	AMD	DM7830	
	TI	SN55183	
DM8800	TI	SN5480	
DM8820	AMD	DM8820	
	TI	SN75182	
		SN75480	
DM8830	AMD	DM8830	
	TI	SN75183	
DM8880	National	DS8880	
DS3611	National	DS3611	
DS3612	National	DS3612	
DS3613	National	DS3613	
DS3614	National	DS3614	
INS2652	National	2652	
ISP-8A/600	National	ISP-8A/600	
LF155	**National**	**LF155**	**1035**
LF156	**National**	**LF156**	**1035**
LF157	**National**	**LF157**	**1035**
LF255	National	LF255	
LF256	National	LF256	
LF257	National	LF257	
LF355	National	LF355	
LF356	**National**	**LF356**	**1035,1073**
LF357	National	LF357	
LH2108	PMI	PM2108	
LH2108A	PMI	PM2108A	
LH2208	PMI	PM2208	
LH2208A	PMI	PM2208A	
LH2308A	PMI	PM2308A	
LM101	AMD	LM101	
	Fairchild	μA101	
	Intersil	LM101	
	Motorola	LM101	
	RCA	CA101	
	Silicon G	SG101	
	TI	LM101	
LM107	AMD	LM107	
	Fairchild	μA107	
	Intersil	LM107	
	Motorola	LM107	
	Raytheon	LM107	
	RCA	CA107	
	Silicon G	SG107	
	TI	LM107	
LM108	AMD	LM108	
	Fairchild	μA108	
	Motorola	LM108	
	Raytheon	LM108	
	RCA	CA108	
	Silicon G	SG108	
LM109	**Fairchild**	**μA109**	**934**
	Motorola	LM109	
	Silicon G	SG109	
	TI	LM109	
LM111	AMD	LM111	
	Motorola	LM111	
	Silicon G	SG111	
	TI	LM111	
LM119	AMD	LM119	
LM124	AMD	LM124	
	Motorola	LM124	
	Silicon G	SG124	
	TI	LM124	
LM139	AMD	LM139	
	Motorola	LM139	
	RCA	CA139	
	Silicon G	SG139	
	TI	LM139	
LM139A	PMI	CMP-04	
		PM139A	
LM193	National	LM193	
LM201	AMD	LM201	
	Fairchild	μA201	
	Intersil	LM201	
	Motorola	LM201	
	RCA	CA201	
	Silicon G	SG201	
LM201	Teledyne S	LM201	
	TI	LM201	
LM207	AMD	LM207	
	Fairchild	μA207	
	Intersil	LM207	
	Motorola	LM207	
	Raytheon	LM207	
	RCA	CA207	
	Silicon G	SG207	
	TI	LM207	
LM208	AMD	LM208	
	Motorola	LM208	
	RCA	CA208	
	Silicon G	SG208	
LM209	**Fairchild**	**μA209**	**934**
	Motorola	LM209	
	Raytheon	LM209	
	Silicon G	SG209	
	TI	LM209	
LM211	AMD	LM211	
	Motorola	LM211	
	Silicon G	SG211	
	TI	LM211	
LM219	AMD	LM219	
LM224	AMD	LM224	
	Motorola	LM224	
	RCA	CA224	
	Silicon G	SG224	
	TI	LM224	
LM239	AMD	LM239	
	Motorola	LM239	
	RCA	CA239	
	Silicon G	SG239	
	TI	LM239	
LM239A	PMI	CMP-04	
		PM239A	
LM293	National	LM293	
LM301	AMD	LM301	
	Fairchild	μA301	
	Intersil	LM301	
	Motorola	LM301	
	National	LM301	
	Raytheon	LM301	
	RCA	CA301	
	Silicon G	SG301	
	TI	LM301	
LM307	AMD	LM307	
	Fairchild	μA307	
	Intersil	LM307	
	Motorola	LM307	
	National	LM307	
	Raytheon	LM307	
	RCA	CA307	
	Silicon G	SG307	
	TI	LM307	
LM308	AMD	LM308	
	Fairchild	μA308	
	Motorola	LM308	
	National	LM308	
	Raytheon	LM308	
	RCA	CA308	
	Silicon G	SG308	
LM309	**Fairchild**	**μA309**	**934**
	Motorola	LM309	
	Raytheon	LM309	
	Silicon G	SG309	
	TI	LM309	
LM311	AMD	LM311	
	Motorola	LM311	
	Raytheon	LM311	
	RCA	CA311	
	Silicon G	SG311	
	TI	LM311	
LM319	AMD	LM319	
LM324	AMD	LM324	
	Motorola	LM324	
	RCA	CA324	
	Silicon G	SG324	
	TI	LM324	
LM329	TI	LM329	
LM339	AMD	LM339	
	Motorola	LM339	
	RCA	CA339	
	Silicon G	SG339	
	TI	LM339	
LM339A	PMI	CMP-04	
LM339A	PMI	PM339A	
LM393	National	LM393	
MC1399	Motorola	MC1399	
MC1408	AD	DA1408	
	Datel	**DAC-IC8BC**	**671**
	Motorola	MC1408	
MC1456	Motorola	MC1456	
	Raytheon	RC1556	
	Silicon G	SG1456	
MC1458	Exar	XR1458	
	Fairchild	MC1458	
	Motorola	MC1458	
	National	LM1458	
	Raytheon	RC1458	
	RCA	CA1458	
	Silicon G	SG1458	
	TI	MC1458	
MC1488	AMD	MC1488	
	Exar	XR1488	
	Silicon G	SG1488	
	TI	SN75188	
MC1489	AMD	MC1489	
	Silicon G	SG1489	
	TI	SN75189	
MC1489A	Exar	XR1489A	
	Silicon G	SG1489A	
MC1496	Motorola	MC1496	
	National	LM1496	
	Silicon G	SG1496	
MC1508	**Datel**	**DAC-IC8BM**	**671**
MC1556	Motorola	MC1556	
	Raytheon	RM1556	
	Silicon G	SG1556	
MC1558	Exar	XR1558	
	Motorola	MC1558	
	Raytheon	RM1558	
	RCA	CA1558	
	Silicon G	SG1558	
	TI	MC1558	
MC1596	Motorola	MC1596	
	Silicon G	SG1596	
MC3302	Motorola	MC3302	
	Silicon G	SG3302	
NE5008	PMI	DAC-08	
NE529	National	LM361	
NE531	Raytheon	RC4531	
NE532	TI	LM358	
NE535	Motorola	MC1741S	
NE536	Fairchild	μA740	
NE546	RCA	CA3123	
NE5532	**Exar**	**XR5532**	**929**
NE5532A	Exar	XR5532A	
NE5533	**Exar**	**XR5533**	**929**
NE5533A	Exar	XR5533A	
NE5534	Datel	AM-453C	
	Exar	**XR5534**	**929**
	TI	NE5534	
NE5534A	Exar	XR5534A	
	TI	NE5534A	
NE555	AMD	NE555	
	Cherry	CS555	
	Exar	XR555	
	Fairchild	μA555	
	Hitachi	HA17555	
	Intersil	NE555	
	Motorola	MC1455	
	Raytheon	RC555	
	RCA	CA555	
	Silicon G	SG555	
	TI	NE555	
NE5556	Raytheon	RC1556	
NE5558	Raytheon	RC1458	
NE556	AMD	NE556	
	Exar	XR556	
	Fairchild	μA556	
	Motorola	MC3456	
	Raytheon	RC556	
	Silicon G	SG556	
	TI	NE556	
NE565	Motorola	LM565	
NE567	Exar	XR567	
	Raytheon	XR2567	
NE592	AMD	AM592	
	Motorola	MC1733	
		NE592	
♦N1004	Motorola	MC1004	
♦N1006	Motorola	MC1006	
♦N1010	Motorola	MC1010	
♦N1011	Motorola	MC1011	
♦N1012	Motorola	MC1012	
♦N1013	Motorola	MC1013	
♦N1014	Motorola	MC1014	
♦N1015	Motorola	MC1015	
♦N1016	Motorola	MC1016	
♦N1017	Motorola	MC1017	
♦N1024	Motorola	MC1024	
♦N1025	Motorola	MC1025	
♦N1027	Motorola	MC1027	
♦N1033	Motorola	MC1033	
♦N1039	Motorola	MC1039	
♦N2010	Motorola	MC1160/236	
N2211	Sprague	ULN-2211	
N2212	Sprague	ULN-2212	
N3002	Intel	3002	
N3101	Intel	3101	
N4066	Fairchild	F4066	
	Mitel	SIL4066	
	Motorola	MC14066	
	National	**CD4066**	**1076**
	NEC America	μPD4066	
	RCA	CD4063	
		CD4066	
	SGS	HBF4066	
	Solitron	CM4066	
	SSS	SCL4066	
	Toshiba	TC4066	
♦N5065	Motorola	MC1358	
	RCA	CA3065	
	Sprague	ULN-2165	
N5070	RCA	CA3070	
♦N5070	Sprague	ULN-2124	
♦N5071	Fairchild	μA781	
	Sprague	ULN-2127	
♦N5072	Fairchild	μA746	
	Sprague	ULN-2114	
♦N521	Motorola	MC7521	
♦N5556	Motorola	MC1456	
N5558	Exar	XR1458	
	Silicon G	SG1458	
N5558F	Motorola	MC1458	
N5570	Fairchild	μA780	
♦N5595	Motorola	MC1495	
N5596	Motorola	MC1496	
	Silicon G	SG1496	
♦N5709	Signetics	μA709	
♦N5710	Signetics	μA710	
♦N5711	Signetics	μA711	
♦N5723	Signetics	μA723	
♦N5733	Signetics	μA733	
♦N5741	Signetics	μA741	
♦N5747	Signetics	μA747	
♦N5748	Signetics	μA748	
N8H16	National	DM54H20	
N8H70	National	DM74H10	
	TI	SN74H11	
N8H80	National	DM74H00	
	TI	SN74H00	
N8H90	National	DM74H04	
	TI	SN74H04	
N8T09	Raytheon	RC8T09	
N8T10	National	DM8551	
	Raytheon	RC8T10	
	TI	SN74173	
N8T13	Fairchild	8T13	
	Motorola	MC8T13	
	TI	N8T13	
		SN75121	
N8T14	Fairchild	8T14	
	Motorola	MC8T14	
	National	DS75122	
	TI	N8T14	
		SN75122	
N8T22	AMD	9601	
	National	DM8601	
	TI	SN74122	
N8T23	Fairchild	8T23	
	Motorola	MC8T23	
	National	DS75123	
	TI	N8T23	
		SN75123	
N8T24	Fairchild	8T24	
	Motorola	MC8T24	

♦ Discontinued

The manufacturers report their devices can be used as direct replacements.
Performance details often differ, so compare the specifications considering your requirements.

Signetics (cont'd)

Manufacturer Device	Replacement Source	Device	IC Master Page
N8T24	National	DS75124	
	TI	N8T24	
		SN75124	
N8T25	National	DS3625	
N8T26	TI	N8T26	
N8T26A	AMD	N8T26A	
	Motorola	MC6880A	
		MC8T26A	
	National	DS8826A	
	TI	N8T26A	
N8T28	AMD	N8T28	
	Motorola	MC8T28	
	Nitron	MC6889	
N8T34	National	DS8834	
N8T37	Motorola	MC3437	
	National	DS8837	
N8T38	Motorola	MC3438	
	National	DS8838	
N8T380	National	DS8836	
N8T51	National	DS8856	
N8T54	National	DM7448	
N8T59	National	DS8857	
N8T74	Fairchild	9374	
N8T95	Motorola	MC8T95	
	National	DM8095	
N8T96	Motorola	MC8T96	
	National	DM8096	
N8T97	Motorola	MC8T97	
	National	DM8097	
N8T98	Motorola	MC8T98	
	National	DM7098	
		DM8098	
		DS8674	
N82S02	Raytheon	RC5330	
N82S09	Fairchild	93419	
N82S10	**Fairchild**	**93415**	**1240**
	TI	SN74S314	
N82S100	**Fairchild**	**93459**	**1269**
N82S101	**Fairchild**	**93458**	**1269**
N82S11	**AMI**	**S4025**	**1203**
	Fairchild	**93425**	**1240**
	TI	SN74S214	
N82S110	TI	SN74S314	
N82S111	TI	SN74S214	
N82S115	AMD	AM27S15	
	Harris	HM7647	
	NEC Micro	**μPB425**	**1621**
N82S116	MMI	6531	
	National	DM74S206	
	TI	SN74S200A	
		SN74S201	
N82S123	AMD	AM27S19	
	Harris	**HM7603**	**1284**
	Intersil	IM5610	
	MMI	**6331-1**	**1449**
	National	DM74S288	
		DM8578	
	TI	**SN74S288**	**1708**
N82S126	AMD	AM27S20	
	Fairchild	**93417**	**1258**
	Harris	HPROM1024A	
	MMI	**6300-1**	**1449**
	National	DM74S387	
	NEC Micro	μPB403	
	Raytheon	**29660**	**1664**
	TI	**SN74S387**	**1708**
N82S127	**MMI**	**6300-1**	**1449**
N82S129	AMD	AM27S21	
	Fairchild	**93427**	**1258**
	Harris	HPROM1024	
	Intersil	IM5623	
	MMI	**6301-1**	**1449**
	National	DM74S287	
	Raytheon	**29661**	**1664**
	TI	**SN54S287**	**1708**
N82S130	AMD	AM27S12	
	Fairchild	**93436**	**1260**
	Harris	**HM7620**	
			1284,1298
		HM7620A	
	Intel	3602	
	Intersil	IM5604	
	MMI	**6305-1**	**1449**
N82S130	**Raytheon**	**29610**	**1654**
	TI	SN74170	
N82S131	AMD	AM27S13	
	Fairchild	**93446**	**1260**
	Harris	**HM7621**	
			1284,1298
		HM7621A	
	Intel	3622	
	Intersil	IM5624	
	MMI	**6306-1**	**1449**
	National	DM74S571	
	Raytheon	**29611**	**1654**
N82S136	**Fairchild**	**93452**	**1264**
	Harris	**HM7642**	
			1284,1308
	MMI	**6352-1**	**1449**
	National	DM74S572	
	NEC Micro	**μPB406**	**1625**
	Raytheon	29640	
N82S137	**Fairchild**	**93453**	**1264**
	Harris	**HM7643**	
			1284,1308
	Intel	3625	
	MMI	**6353-1**	**1449**
	National	DM74S573	
	NEC Micro	**μPB426**	**1625**
	Raytheon	29641	
	TI	**SN74S476**	**1713**
N82S140	**Fairchild**	**93438**	**1262**
	Harris	**HM7640**	
			1284,1304
	Intersil	IM5606	
	MMI	**6340-1**	**1449**
	National	DM87S295	
	NEC Micro	**μPB405**	**1621**
	Raytheon	**29624**	**1658**
	TI	**SN74S475**	**1708**
N82S141	**Fairchild**	**93448**	**1262**
	Harris	**HM7641**	
			1284,1304
	Intersil	IM5625	
	MMI	**6341-1**	**1449**
	National	DM87S296	
	NEC Micro	**μPB425**	**1621**
	Raytheon	**29625**	**1658**
	TI	**SN74S474**	**1708**
N82S146	**MMI**	**63S480**	**1453**
	National	DM74S473	
	Raytheon	**29620**	**1656**
	TI	**SN74S473**	**1708**
N82S147	**MMI**	**5349-1**	**1449**
		63S481	**1453**
		6349-1	**1449**
	National	DM74S472	
	Raytheon	**29621**	**1656**
	TI	**SN74S472**	**1708**
N82S16	**Fairchild**	**93421**	**1252**
	MMI	6531	
	Raytheon	RC5340	
N82S17	Fairchild	93411	
	MMI	6530	
	National	DM74S206	
N82S177	National	DM74S206	
	TI	SN74S300	
		SN74S301	
N82S180	**Harris**	**HM7680**	**1322**
	Intel	3608	
	MMI	**6380-1**	**1449**
	National	DM85S229	
	Raytheon	**29630**	**1660**
N82S181	**Harris**	**HM7681**	**1322**
	Intel	3628	
	MMI	**6381-1**	**1449**
	National	DM85S228	
	Raytheon	**29631**	**1660**
N82S184	**Harris**	**HM7684**	**1333**
	MMI	**63S840**	**1453**
	Raytheon	29650	
N82S185	**MMI**	**63S841**	**1453**
	Raytheon	29651	
N82S190	**MMI**	**63S1680**	**1453**
	Supertex	**SM82S190**	**1705**
N82S191	**MMI**	**63S1681**	**1453**
	Supertex	**SM82S191**	**1705**
N82S195	Harris	HM7647	
N82S226	Fairchild	93416	
N82S226	Intersil	IM5603	
	TI	SN74187	
N82S229	**TI**	**SN74S287**	**1708**
N82S23	AMD	AM27S18	
	Harris	**HM7602**	**1284**
	MMI	**5330-1**	**1449**
		6330-1	**1449**
	National	DM74S188	
	TI	**SN74S188**	**1708**
N82S230	TI	SN74S270	
N82S231	TI	SN74S370	
N82S24	Intersil	IM5600	
	TI	SN54S301	
N82S25	Fairchild	74S289	
	National	DM74S289	
	TI	SN74S289	
N82S26	Fairchild	93416	
	Intersil	IM5603	
	NEC Micro	μPB403	
	TI	**SN74S387**	**1708**
N82S2708	**Harris**	**HM7608**	**1290**
	Raytheon	**29635**	**1662**
N82S29	**MMI**	**6301-1**	**1449**
	TI	**SN74S287**	**1708**
N82S30	National	DM8312	
N82S41	National	DM74LS386	
N82S52	National	DM8301	
N82S707	Motorola	MCM82707	
N82S708	Motorola	MCM82708	
N82S80	National	DM74LS196	
N82S81	National	DM74LS197	
N82S90	National	DM74LS196	
	TI	SN74S196	
N82S91	National	DM74LS197	
	TI	SN74S197	
N8200	Raytheon	RC8200	
N8201	Raytheon	RC8201	
N8202	Raytheon	RC8202	
N8203	Raytheon	RC8203	
N8206	TI	SN74S200A	
		SN74S201	
N8207	TI	SN74S300	
		SN74S301	
N82147	National	DM74147	
	TI	SN74147	
N82148	Fairchild	9318	
	National	DM74148	
	TI	SN74148	
N8223	Harris	HPROM8256	
	Intersil	IM5600	
	MMI	**6330-1**	**1449**
	National	DM8577	
	TI	**SN74S188**	**1708**
N8224	Intersil	IM5600	
	National	DM7488	
	TI	SN7488	
N8225	AMD	3101	
	Motorola	MCM4064	
	Raytheon	RC8225	
	TI	SN74S289	
N8230	Hitachi	HD8230	
	Motorola	MC7230	
	National	DM8312	
	Raytheon	RC8230	
	TI	SN29312	
N8231	Motorola	MC7230	
	Raytheon	RC8231	
N8232	Motorola	MC7230	
	Raytheon	RC8232	
N8233	Motorola	MC8233	
	Raytheon	RC8233	
N8234	Motorola	MC8234	
	Raytheon	RC8234	
N8241	Hitachi	HD8241	
	Motorola	MC7241	
		MC7242	
	National	DM74LS386	
	Raytheon	RC8241	
N8242	Motorola	MC7242	
	Raytheon	RC8242	
	TI	SN74LS266	
N8250	Motorola	MC7250	
		MC7251	
	Raytheon	RC8250	
N8251	Hitachi	HD8251	
	Motorola	MC7250	
N8251	Motorola	MC7251	
	Raytheon	RC8251	
N8252	Motorola	MC7250	
		MC7251	
	National	DM8301	
	Raytheon	RC8252	
	TI	SN29301	
N82523	National	DM74S188	
N8255	AMD	3101	
	Fairchild	74S289	
	MMI	6560	
	Motorola	MCM4064	
	Raytheon	RC8225	
	TI	SN74S289	
N8260	Motorola	MC7260	
	Raytheon	RC8260	
N8261	Hitachi	HD8261	
	Motorola	MC7261	
	Raytheon	RC8261	
N8262	Raytheon	RC8262	
N8263	Raytheon	RC8263	
N8264	Raytheon	RC8264	
N8266	Motorola	MC7266	
	Raytheon	RC8266	
N8267	Motorola	MC7267	
	Raytheon	RC8267	
N8268	Motorola	MC7268	
	TI	SN7480	
N8269	National	DM8200	
N8270	Fairchild	74178	
	Motorola	MC7270	
	Raytheon	RC8270	
	TI	SN74178	
N8271	Fairchild	74179	
	Motorola	MC7271	
	Raytheon	RC8271	
	TI	SN74179	
N8277	Motorola	MC7277	
	Raytheon	RC8277	
N8280	Fairchild	74176	
	Motorola	MC7280	
	National	DM8280	
	Raytheon	RC8280	
	TI	SN74176	
N8281	Motorola	MC7281	
	National	DM8281	
	Raytheon	RC8281	
	TI	SN54177	
N8284	Motorola	MC7284	
	Raytheon	RC8284	
N8285	Motorola	MC7285	
	Raytheon	RC8285	
N8288	Motorola	MC7288	
	National	DM8288	
N8290	Fairchild	74196	
	National	DM8290	
	Raytheon	RC8290	
	TI	SN74196	
N8291	Fairchild	74197	
	National	DM8291	
	Raytheon	RC8291	
	TI	SN74197	
N8292	Fairchild	74S196	
	National	DM74LS196	
	TI	SN74LS196	
N8293	Fairchild	74LS197	
	National	DM74LS197	
	TI	SN74LS197	
N83S27	**MMI**	**6300-1**	**1449**
N8415	National	DM1800	
N8455	Motorola	MC7440	
	National	DM7440	
	TI	SN7440	
N8470	Motorola	MC7410	
	National	DM7410	
	TI	SN7410	
N8471	Motorola	MC7412	
	National	DM74LS12	
	TI	SN7412	
N8480	National	DM7400	
	TI	SN7400	
N8481	Motorola	MC7403	
	National	DM7403	
	TI	SN7403	
N8490	Motorola	MC7404	
	National	DM7404	

◆ Discontinued

Bold face device numbers indicate manufacturers data is provided in the IC Master on the pages noted.

Signetics (cont'd)

Manufacturer Device	Replacement Source	Device	IC Master Page
N8490	TI	SN7404	
N8806	Motorola	MC7460	
	National	DM7406	
	TI	SN7460	
N8808	Motorola	MC7430	
	National	DM7430	
	TI	SN7430	
N8813	National	DM7425	
N8815	National	DM7425	
	TI	SN7425	
N8824	Motorola	MC7474	
	TI	SN7474	
N8825	Motorola	MC7470	
	TI	SN7470	
N8828	Motorola	MC7479	
	National	DM7474	
	TI	SN7474	
N8829	Motorola	MC7472	
	TI	SN74110	
N8840	Motorola	MC7450	
	National	DM7451	
	TI	SN7450	
N8848	Motorola	MC7453	
	TI	SN74H53	
N8859	National	DM7440	
	TI	SN7450	
N8875	Motorola	MC7427	
	National	DM7427	
	TI	SN7427	
N8879	TI	SN7410	
N8881	Motorola	MC7401	
	National	DM7401	
	TI	SN7401	
N8890	National	DM7404	
	TI	SN7404	
N8891	National	DM7405	
	TI	SN7405	
N93415	**Fairchild**	**93415**	**1240**
	Fujitsu	MBM93415	
N93425	Fairchild	93425A	
N9602	AMD	9602	
SE5009	PMI	DAC-08	
SE529	National	LM161	
SE531	Raytheon	RM4531	
SE532	TI	LM158	
SE550	National	LM550	
SE5532	**Exar**	**XR5532**	**929**
SE5532A	Exar	XR5532A	
SE5533	**Exar**	**XR5533**	**929**
SE5533A	Exar	XR5533A	
SE5534	Datel	AM-453M	
	Exar	**XR5534**	**929**
	TI	SE5534	
SE5534A	Exar	XR5534A	
	TI	SE5534A	
SE554A	TI	SE5534A	
SE555	AMD	SE555	
	Exar	XR555	
		XR555M	
	Intersil	SE555	
	Motorola	MC1555	
	National	LM555	
	Raytheon	RM555	
	RCA	CA555	
	Silicon G	SG555	
	TI	SE555	
SE556	Exar	XR556M	
	Motorola	MC3556	
	National	SE556	
	Raytheon	RM556	
	Silicon G	SG556	
	TI	SE556	
SE565	National	LM565	
SE566	National	LM566	
SE567	National	LM567	
SE5733	TI	μA733	
SE592	Motorola	MC1733	
		SE592	
SN74LS08	Hitachi	HD74LS08	
SP380	National	DS8640	
SU536	Intersil	SU536	
S3532	TI	LM158	
S5556	Silicon G	SG1556	
S5596	Silicon G	SG1596	
♦S5709	Signetics	μA709	
♦S5710	Signetics	μA710	
♦S5711	Signetics	μA711	
♦S5723	Signetics	μA723	
♦S5733	Signetics	μA733	
♦S5741	Signetics	μA741	
S7280	National	DM7280	
S7281	National	DM7281	
S7290	National	DM7290	
S7291	National	DM7291	
S8H16	National	DM54H20	
S8H70	National	DM54H10	
	TI	SN54H11	
S8H80	National	DM54H00	
	TI	SN54H00	
S8H90	National	DM54H04	
	TI	SN54H04	
S8T09	Raytheon	RM8T09	
S8T10	National	DM7551	
	Raytheon	RM8T10	
	TI	SN54173	
S8T13	Fairchild	8T13	
	TI	SN55121	
S8T14	Fairchild	8T14	
	TI	SN55122	
S8T22	Fairchild	9601	
	National	DM9601	
	TI	SN29601	
S8T26	AMD	S8T26	
S8T28	AMD	S8T28	
S8T54	National	DM5448	
S8T95	National	DM7095	
S8T96	National	DM7096	
S8T97	National	DM7097	
S8T98	National	DM7098	
S82LS29	**TI**	**SN54S287**	**1706**
S82S06	Raytheon	RM5340	
	TI	SN54S201	
S82S07	Raytheon	RM5330	
	TI	SN54S301	
S82S09	Fairchild	93419	
S82S10	**Fairchild**	**93415**	**1240**
S82S100	**Fairchild**	**93459**	**1269**
S82S101	**Fairchild**	**93458**	**1269**
S82S11	**Fairchild**	**93425**	**1240**
S82S115	AMD	AM27S15	
	Harris	HM7647	
S82S123	AMD	AM27S19	
	Harris	**HM7603**	**1284**
	MMI	**5331-1**	**1449**
	National	DM54S288	
		DM7578	
	TI	DM54S288	
		SN54S288	**1708**
S82S126	AMD	AM27S20	
	Fairchild	**93417**	**1258**
	Harris	**HM7610**	
			1284,1292
		HM7610A	
		HPROM1024A	
	Intersil	IM5603	
	MMI	**5300-1**	**1449**
	National	DM54S387	
	Raytheon	**29660**	**1664**
	TI	**SN54S387**	**1708**
S82S127	**MMI**	**5300-1**	**1449**
S82S129	AMD	AM27S21	
	Fairchild	**93427**	**1258**
	Harris	**HM7611**	
			1284,1292
		HM7611A	
		HPROM1024	
	Intel	3621	
	Intersil	IM5623	
	MMI	**5301-1**	**1449**
	National	DM54S287	
	Raytheon	**29661**	**1664**
	TI	**SN54S287**	**1708**
S82S130	AMD	AM27S12	
	Fairchild	**93436**	**1260**
	Harris	**HM7620**	
			1284,1298
		HM7620A	
	Intel	3602	
	Intersil	IM5604	
S82S130	**MMI**	**5305-1**	**1449**
	National	DM54S570	
	Raytheon	**29610**	**1654**
S82S131	AMD	AM27S13	
	Fairchild	**93446**	**1260**
	Harris	**HM7621**	
			1284,1298
		HM7621A	
	Intel	3622	
	Intersil	IM5624	
	MMI	**5306-1**	**1449**
	National	DM54S571	
		DM74S571	
	Raytheon	**29611**	**1654**
S82S136	**Fairchild**	**93452**	**1264**
	Harris	**HM7642**	
			1284,1308
	Intel	3605	
	MMI	**5352-1**	**1449**
	National	DM54S572	
	Raytheon	29640	
	TI	**SN54S477**	**1713**
		SN54S571	
S82S137	**Fairchild**	**93453**	**1264**
	Harris	**HM7643**	
			1284,1308
	Intel	3625	
	MMI	**5353-1**	**1449**
	National	DM54S573	
	Raytheon	29641	
	TI	**SN54S476**	**1713**
S82S140	**Fairchild**	**93438**	**1262**
	Harris	**HM7640**	
			1284,1304
	Intel	3604	
	Intersil	IM5606	
	MMI	**5340-1**	**1449**
	National	DM77S295	
	Raytheon	**29624**	**1658**
	TI	**SN54S475**	**1708**
S82S141	**Fairchild**	**93448**	**1262**
	Harris	**HM7641**	
			1284,1304
	Intel	3624	
	Intersil	IM5625	
	MMI	**5341-1**	**1449**
	National	DM77S296	
	Raytheon	**29625**	**1658**
	TI	**SN54S474**	**1708**
S82S146	**MMI**	**53S480**	**1453**
		5348-1	**1449**
	National	DM54S473	
	Raytheon	**29620**	**1656**
	TI	**SN54S473**	**1708**
S82S147	**MMI**	**53S481**	**1453**
	National	DM54S472	
	Raytheon	**29621**	**1656**
	TI	DM54S472	
S82S16	**Fairchild**	**93421**	**1252**
♦S82S16	National	DM54S200	
	TI	SN54S201	
S82S17	Fairchild	93411	
♦S82S17	National	DM54S206	
	TI	SN54S301	
S82S180	**Harris**	**HM7680**	**1322**
	Intel	3608	
	MMI	**5380-1**	**1449**
	National	DM75S229	
	Raytheon	**29630**	**1660**
S82S181	**Harris**	**HM7681**	**1322**
	Intel	3628	
	MMI	**5381-1**	**1449**
	National	DM75S228	
	Raytheon	**29631**	**1660**
S82S184	**Harris**	**HM7684**	**1333**
	MMI	**53S840**	**1453**
	Raytheon	29650	
S82S185	**Harris**	**HM7685**	**1333**
	MMI	**53S841**	**1453**
	Raytheon	29651	
S82S190	**MMI**	**53S1680**	**1453**
	Supertex	**MM82S190**	**1706**
S82S191	**MMI**	**53S1681**	**1453**
	Supertex	**MM82S191**	**1705**
S82S226	TI	SN54187	
S82S229	**TI**	**SN54S287**	**1708**
S82S23	AMD	AM27S08	
		AM27S18	
	Harris	**HM7602**	**1284**
	Intersil	IM5600	
	MMI	**5330-1**	**1449**
	National	DM54S188	
	TI	**SN54S188**	**1708**
S82S230	TI	SN54S270	
S82S231	TI	SN54S370	
S82S25	TI	SN54S289	
		SN54S301	
S82S26	AMD	82S26	
	TI	**SN54S387**	**1708**
S82S27	**MMI**	**5300-1**	**1449**
S82S2708	**Harris**	**HM7608**	**1290**
	Raytheon	**29635**	**1662**
S82S30	Fairchild	93S12	
S82S41	National	DM54LS386	
S82S62	Fairchild	93S62	
S82S707	Motorola	MCM82707	
S82S708	Motorola	MCM82708	
S82S80	National	DM54LS196	
S82S81	National	DM54LS197	
S82S90	National	DM54LS196	
S82S91	National	DM54LS197	
S8200	Raytheon	RM8200	
S8201	Raytheon	RM8201	
S8202	Raytheon	RM8202	
S8203	Raytheon	RM8203	
S8207	TI	SN54S301	
S82147	National	DM54147	
S82148	Fairchild	9318	
	National	DM54148	
S8223	Harris	HPROM8256	
	Intersil	IM5600	
	MMI	**5330-1**	**1449**
	National	DM7577	
	TI	**SN54S188**	**1708**
S8224	National	DM5488	
	TI	SN5488A	
S8225	TI	SN54S289	
S8230	Fairchild	9312	
	National	DM9312	
	Raytheon	RM8230	
	TI	SN39312	
S8231	Fairchild	9313	
	Raytheon	RM8231	
S8241	National	DM54LS386	
	Raytheon	RM8241	
S8242	Fairchild	54LS266	
	Raytheon	RM8242	
	TI	SN54LS266	
S8250	Raytheon	RM8250	
S8251	Raytheon	RM8251	
S8252	Fairchild	9301	
	National	DM9301	
	Raytheon	RM8252	
	TI	SN39301	
S8260	Raytheon	RM8260	
S8261	Raytheon	RM8261	
S8262	Raytheon	RM8262	
S8263	Raytheon	RM8263	
S8264	Raytheon	RM8264	
S8266	Raytheon	RM8266	
S8267	Raytheon	RM8267	
S8268	TI	SN5480	
S8269	National	DM7200	
S8270	Fairchild	54178	
	Raytheon	RM8270	
	TI	SN54178	
S8271	Fairchild	54179	
	Raytheon	RM8271	
	TI	SN54179	
S8277	Fairchild	9328	
	Raytheon	RM8277	
S8280	Fairchild	54176	
	Raytheon	RM8280	
	TI	SN54176	
S8281	Fairchild	54177	
	Raytheon	RM8281	
	TI	SN54177	
S8288	National	DM7288	
S8290	Fairchild	54196	
	Raytheon	RM8290	
	TI	SN54196	
S8291	Fairchild	54197	

♦ Discontinued

The manufacturers report their devices can be used as direct replacements.
Performance details often differ, so compare the specifications considering your requirements.

Signetics (cont'd)

Manufacturer Device	Replacement Source	Device	IC Master Page
S8291	Raytheon	RM8291	
	TI	SN54197	
S8292	National	DM54LS196	
	TI	SN54LS196	
S8293	National	DM54LS197	
	TI	SN54LS197	
S8455	National	DM5440	
	TI	SN5440	
S8470	National	DM5410	
	TI	SN5410	
S8471	National	DM54LS12	
	TI	SN5412	
S8480	National	DM5400	
	TI	SN5400	
S8481	National	DM5403	
	TI	SN5403	
S8490	National	DM5404	
	TI	SN5404	
S8806	National	DM5460	
	TI	SN5460	
S8808	National	DM5430	
	TI	SN5430	
S8815	National	DM5425	
	TI	SN5425	
S8828	National	DM5474	
	TI	SN5474	
S8840	National	DM5451	
	TI	SN5450	
S8848	National	DM54LS54	
	TI	SN54H53	
S8859	National	DM5440	
S8875	National	DM5427	
	TI	SN5427	
S8881	National	DM5401	
	TI	SN5401	
S8890	National	DM5404	
	TI	SN5404	
S8891	National	DM5405	
	TI	SN5405	
TBA396	Sprague	ULN-2219	
TBA520	Plessey	TBA520	
TBA530	Plessey	TBA530	
TBA540	Plessey	TBA540	
TBA550	Plessey	TBA550	
TBA560	Plessey	TBA560	
TBA750	Plessey	TBA750	
TBA920	Plessey	TBA920	
TBA990	Plessey	TBA990	
TCA800	Plessey	TCA800	
♦TDA1034	**Signetics**	**NE5534**	**1117**
UDN5711	Sprague	UDN-5711	
UDN5712	Sprague	UDN-5712	
UDN5713	Sprague	UDN-5713	
UDN5714	Sprague	UDN-5714	
ULN-6128	Exar	XR6128	
ULN2001	**Exar**	**XR2201**	**931**
	Silicon G	SG2001	
	Sprague	ULN-2001	
ULN2002	**Exar**	**XR2202**	**931**
	Silicon G	SG2002	
	Sprague	ULN-2002	
ULN2003	**Exar**	**XR2203**	**931**
	Silicon G	SG2003	
	Sprague	ULN2003	
ULN2004	**Exar**	**XR2204**	**931**
	Sprague	ULN-2004	
ULN2111	Motorola	MC1357	
	RCA	CA2111	
	Sprague	ULN-2111	
10100	Fairchild	F10100	
	Motorola	MC10100	
	NEC America	μPB10100	
10101	Fairchild	F10101	
	Hitachi	HD10101	
	Motorola	MC10101	
	NEC America	μPB10101	
1010130	Fairchild	F10130	
	Hitachi	HD10130	
	Motorola	MC10130	
10102	Fairchild	F10102	
	Hitachi	HD10102	
	Motorola	MC10102	
	NEC America	μPB10102	
10103	Fairchild	F10103	
	Motorola	MC10103	
	NEC America	μPB10103	
10104	Fairchild	F10104	
	Hitachi	HD10104	
	Motorola	MC10104	
10105	Fairchild	F10105	
	Hitachi	HD10105	
	Motorola	MC10105	
	National	DM10105	
	NEC America	μPB10105	
10106	Fairchild	F10106	
	Hitachi	HD10106	
	Motorola	MC10106	
	National	DM10106	
	NEC America	μPB10106	
10107	Fairchild	F10107	
	Hitachi	HD10107	
	Motorola	MC10107	
	NEC America	μPB10107	
10109	Fairchild	F10109	
	Hitachi	HD10109	
	Motorola	MC10109	
	National	DM10109	
	NEC America	μPB10109	
10110	Fairchild	F10110	
	Hitachi	HD10110	
	Motorola	MC10110	
	NEC America	μPB10110	
10111	Fairchild	F10111	
	Hitachi	HD10111	
	Motorola	MC10111	
	National	DM10111	
	NEC America	μPB10111	
10112	National	DM10112	
10113	Fairchild	F10113	
	Motorola	MC10113	
10114	Fairchild	F10114	
	Motorola	MC10114	
10115	Fairchild	F10115	
	Motorola	MC10115	
	National	DM10115	
	NEC America	μPB10115	
10116	Fairchild	F10116	
	Hitachi	HD10116	
	Motorola	MC10116	
	National	DM10116	
10117	Fairchild	F10117	
	Hitachi	HD10117	
	Motorola	MC10117	
	National	DM10117	
	NEC America	μPB10117	
10118	Fairchild	F10118	
	Hitachi	HD10118	
	Motorola	MC10118	
	National	DM10118	
	NEC America	μPB10118	
10119	Fairchild	F10119	
	Hitachi	HD10119	
	Motorola	MC10119	
	National	DM10119	
10121	Fairchild	F10121	
	Hitachi	HD10121	
	Motorola	MC10121	
	National	DM10121	
10123	Fairchild	F10123	
	Motorola	MC10123	
10124	Fairchild	F10124	
	Hitachi	HD10124	
	Motorola	MC10124	
	National	DM10124	
	NEC America	μPB10124	
10125	Fairchild	F10125	
	Hitachi	HD10125	
	Motorola	MC10125	
10129	Motorola	MC10129	
10130	Fairchild	F10130	
	Motorola	MC10130	
10131	Fairchild	F10131	
	Hitachi	HD10131	
	Motorola	MC10131	
	NEC America	μPB10131	
10132	Fairchild	F10132	
	Hitachi	HD10132	
	Motorola	MC10132	
	NEC America	μPB10132	
10133	Fairchild	F10133	
	Hitachi	HD10133	
	Motorola	MC10133	
	NEC America	μPB10133	
10134	Fairchild	F10134	
	Hitachi	HD10134	
	Motorola	MC10134	
10135	Fairchild	F10135	
	Motorola	MC10135	
10136	Fairchild	F10136	
	Hitachi	HD10136	
	Motorola	MC10136	
10137	Fairchild	F10137	
	Motorola	MC10137	
10139	Motorola	MCM10139	
	TI	SN10139	
10140	TI	SN10140	
10141	Fairchild	F10141	
	Motorola	MCM10141	
		MC10141	
10144	Fairchild	F10410	
	Motorola	MC10144	
	NEC America	μPB10144	
	Raytheon	RC10144	
	TI	SN10144	
10145	Fairchild	F10145	
	Hitachi	HD10145	
	Motorola	MCM10145	
		MC10145	
	TI	SN10145	
10147	Fujitsu	MB7047	
10148	Hitachi	HD10148	
	NEC America	μPB10148	
	TI	SN10148	
10149	Fairchild	10149	
♦10149	Motorola	MCM10149	
		MC10149	
10158	Fairchild	F10158	
	Motorola	MC10158	
	NEC America	μPB10158	
10159	Fairchild	F10159	
	Motorola	MC10159	
10160	Fairchild	F10160	
	Hitachi	HD10160	
	Motorola	MC10160	
10161	Fairchild	F10161	
	Hitachi	HD10161	
	Motorola	MC10161	
	NEC America	μPB10161	
10162	Fairchild	F10162	
	Hitachi	HD10162	
	Motorola	MC10162	
	NEC America	μPB10162	
10164	Fairchild	F10164	
	Hitachi	HD10164	
	Motorola	MC10164	
	NEC America	μPB10164	
	TI	SN10164	
10165	Fairchild	F10165	
	Hitachi	HD10165	
	Motorola	MC10165	
10170	Fairchild	F10170	
	Motorola	MC10170	
10171	Fairchild	F10171	
	Motorola	MC10171	
10172	Fairchild	F10172	
	Motorola	MC10172	
10173	Fairchild	F10173	
	Motorola	MC10173	
10174	Fairchild	F10174	
	Hitachi	HD10174	
	Motorola	MC10174	
	NEC America	μPB10174	
	TI	SN10174	
10175	Fairchild	F10175	
	Hitachi	HD10175	
	Motorola	MC10175	
10176	Fairchild	F10176	
	Motorola	MC10176	
10179	Fairchild	F10179	
	Hitachi	HD10179	
	Motorola	MC10179	
10180	Fairchild	F10180	
	Hitachi	HD10180	
	Motorola	MC10180	
	NEC America	μPB10180	
10181	Fairchild	F10181	
	Hitachi	HD10181	
	Motorola	MC10181	
	NEC Micro	μPB10181	
10189	Motorola	MC10189	
10191	Motorola	MC10191	
10192	Fairchild	F10192	
10210	Fairchild	F10210	
	Motorola	MC10210	
10211	Fairchild	F10211	
	Motorola	MC10211	
10212	Fairchild	F10212	
	Motorola	MC10212	
1103	TI	TMS1103	
11031	Motorola	MC10131	
1702	Intel	1702	
21F02	**Fairchild**	**21021**	**1275**
	Intel	2102	
21L02	Fairchild	21026	
2101	AMD	91L02	
	Fairchild	3538	
	Intel	2101	
	NEC Micro	**μPD2101**	**1586**
2102	AMD	2102	
	Fairchild	**2102**	**1275**
		21021	**1275**
		21022	**1275**
	National	MM2102	
	NEC Micro	**μPD2102**	**1591**
2111	Intel	2111	
	NEC Micro	**μPD2111**	**1595**
2112	Intel	2112	
	TI	TMS4043	
♦2115	**Intel**	**2115**	**1416**
♦2125	**Intel**	**2125**	**1416**
♦2352	SGS	M142	
♦2400	AMI	S8773	
♦2441	AMI	S8773	
♦2451	AMI	S8773	
♦2461	AMI	S8773	
♦2462	AMI	S8773	
♦25L01	Mostek	MK4007	
♦2501	Mostek	MK4007	
♦2502	Synertek	SY1402	
♦2503	SGS	M136	
	Synertek	SY1403	
♦2504	Synertek	SY1404	
♦2505	AMD	AM2505	
♦2512	AMD	AM2806	
	Nortec	2512	
♦2513	GI	RO3-2513	
♦2517	AMD	1507	
2518	Fairchild	3349	
♦2518	TI	TMS3112	
♦2521	AMD	AM2521	
	TI	TMS3128	
♦2524	AMD	AM2807	
♦2525	AMD	AM2808	
♦2526	AMI	S8564	
♦2527	Synertek	SY2527	
2530	Fairchild	3515	
♦2532	Fairchild	3347	
		3357	
	Mostek	MK1007	
	TI	TMS3120	
♦2533	AMD	AM2833	
	Synertek	SY2533	
♦2536	GI	AY3-1014A	
		AY3-1015	
		AY5-1013A	
	TI	TMS6011	
♦2548	Nortec	6003	
2600	EA	4600	
♦2601	**NEC Micro**	**μPD2101AL**	**1586**
♦2607	EA	EA2308A	
	TI	TMS4700	
2608	Motorola	MCM6830	
♦2608	TI	TMS4700	
2609	Motorola	MCM6570	
♦2611	**NEC Micro**	**μPD2111AL**	**1595**
2613	Fujitsu	MBM4044	
	TI	TMS4044	
♦2614	Intersil	IM7114	
		2114	
	TI	TMS4045	
2616	**AMI**	**S4216B**	**1209**
	Fairchild	3516E	

♦ Discontinued

Bold face device numbers indicate manufacturers data is provided in the IC Master on the pages noted.

Signetics (cont'd)

Manufacturer Device	Replacement Source	Device	IC Master Page
2616	Intel	2316B	
2617	AMD	9216	
♦2627	TI	TMS4027	
♦2630	Intersil	7116	
♦2632	TI	TMS4732	
2633	**AMI**	**S68332**	**1216**
♦2633	TI	TMS4732	
2650	Intersil	2650	
	National	INS2650	
2651	National	INS2651	
2652	National	INS2652	
	SMC	COM5025	
2656	National	INS2656	
♦2660	Mostek	MK4096	
	TI	TMS4027	
2665	**AMI**	**S4264**	**1212**
2670	National	MM5270	
♦2680	TI	TMS4060	
2690	AMD	9016	
	Fujitsu	MB8116	
♦2690	TI	TMS4116	
2708	Fujitsu	MB8518	
	TI	TMS2708	
2716	Fujitsu	MBM2716	
3415	**AMI**	**S4015**	**1203**
4027	Fairchild	M4027	
	Fujitsu	MB8227	
54H00	Fairchild	54H00	
	National	DM54H00	
	Raytheon	54H00	
	TI	SN54H00	
54H01	Fairchild	54H01	
	National	DM54H01	
	Raytheon	54H01	
	TI	SN54H01	
54H04	Fairchild	54H04	
	National	DM54H04	
	Raytheon	54H04	
	TI	SN54H04	
54H05	Fairchild	54H05	
	National	DM54H05	
	Raytheon	54H05	
	TI	SN54H05	
54H08	Fairchild	54H08	
	National	DM54H08	
54H10	Fairchild	54H10	
	National	DM54H10	
	Raytheon	54H10	
	TI	SN54H10	
54H101	Fairchild	54H101	
	TI	SN54H101	
54H102	Fairchild	54H102	
	TI	SN54H102	
54H103	Fairchild	54H103	
	National	DM54H103	
	TI	SN54H103	
54H106	Fairchild	54H106	
	National	DM54H106	
	TI	SN54H106	
54H108	Fairchild	54H108	
	National	DM54H108	
	TI	SN54H108	
54H11	Fairchild	54H11	
	National	DM54H11	
	Raytheon	54H11	
	TI	SN54H11	
54H20	Fairchild	54H20	
	National	DM54H20	
	Raytheon	54H20	
	TI	SN54H20	
54H21	Fairchild	54H21	
	National	DM54H21	
54H22	Fairchild	54H22	
	National	DM54H22	
	Raytheon	54H22	
	TI	SN54H22	
54H30	Fairchild	54H30	
	National	DM54H30	
	TI	SN54H30	
54H40	Fairchild	54H40	
	National	DM54H40	
	Raytheon	54H40	
	TI	SN54H40	
54H50	Fairchild	54H50	
	National	DM54H50	
	TI	SN54H50	
54H51	Fairchild	54H51	
	National	DM54H51	
	TI	SN54H51	
54H52	Fairchild	54H52	
	National	DM54H52	
	TI	SN54H52	
54H53	Fairchild	54H53	
	National	DM54H53	
	TI	SN54H53	
54H54	Fairchild	54H54	
	National	DM54H54	
	TI	SN54H54	
54H55	Fairchild	54H55	
	National	DM54H55	
	TI	SN54H55	
54H60	Fairchild	54H60	
	National	DM54H60	
	TI	SN54H60	
54H61	Fairchild	54H61	
	National	DM54H61	
	TI	SN54H61	
54H62	Fairchild	54H62	
	National	DM54H62	
	TI	SN54H62	
54H71	Fairchild	54H71	
	National	DM54H71	
	TI	SN54H71	
54H72	Fairchild	54H72	
		54H73	
	National	DM54H72	
	TI	SN54H72	
54H73	Fairchild	54H73	
	National	DM54H73	
	TI	SN54H73	
54H74	Fairchild	54H74	
	National	DM54H74	
	Raytheon	54H74	
	TI	SN54H74	
54H76	Fairchild	54H76	
	National	DM54H76	
	TI	SN54H76	
54LS00	Fairchild	54LS00	
	Motorola	SN54LS00	
	National	DM54LS00	
	Raytheon	54LS00	
	TI	SN54LS00	
54LS01	National	DM54LS01	
	Raytheon	54LS01	
	TI	SN54LS01	
54LS02	Fairchild	54LS02	
	Motorola	SN54LS02	
	National	DM54LS02	
	Raytheon	54LS02	
	TI	SN54LS02	
54LS03	Fairchild	54LS03	
	Motorola	SN54LS03	
	National	DM54LS03	
	Raytheon	54LS03	
	TI	SN54LS03	
54LS04	Fairchild	54LS04	
	Motorola	SN54LS04	
	National	DM54LS04	
	Raytheon	54LS04	
	TI	SN54LS04	
54LS05	Fairchild	54LS05	
	Motorola	SN54LS05	
	National	DM54LS05	
	Raytheon	54LS05	
	TI	SN54LS05	
54LS08	Fairchild	54LS08	
	Motorola	SN54LS08	
	National	DM54LS08	
	Raytheon	54LS08	
	TI	SN54LS08	
54LS09	Fairchild	54LS09	
	Motorola	SN54LS09	
	National	DM54LS09	
	Raytheon	54LS09	
	TI	SN54LS09	
54LS10	Fairchild	54LS10	
	Motorola	SN54LS10	
	National	DM54LS10	
	Raytheon	54LS10	
54LS10	TI	SN54LS10	
54LS107	Fairchild	54LS107	
	Motorola	SN54LS107A	
	National	DM54LS107	
	Raytheon	54LS107	
	TI	SN54LS107A	
54LS109	Fairchild	54LS109	
	Motorola	SN54LS109	
	National	DM54LS109	
	Raytheon	54LS109	
	TI	SN54LS109	
54LS11	Fairchild	54LS11	
	Motorola	SN54LS11	
	National	DM54LS11	
	Raytheon	54LS11	
	TI	SN54LS11	
54LS112	Fairchild	54LS112	
	Motorola	SN54LS112A	
	National	DM54LS112	
	Raytheon	54LS112	
	TI	SN54LS112	
54LS113	Fairchild	54LS113	
	Motorola	SN54LS113A	
	National	DM54LS113	
	Raytheon	54LS113	
	TI	SN54LS113	
54LS114	Fairchild	54LS114	
	Motorola	SN54LS114A	
	National	DM54LS114	
	Raytheon	54LS114	
	TI	SN54LS114A	
54LS12	Motorola	SN54LS12	
	National	DM54LS12	
	Raytheon	54LS12	
	TI	SN54LS12	
54LS125	Fairchild	54LS125	
	National	DM54LS125	
	Raytheon	54LS125	
	TI	SN54LS125A	
54LS126	Fairchild	54LS126	
	Motorola	SN54LS126	
	National	DM54LS126	
	Raytheon	54LS126	
	TI	SN54LS126A	
54LS13	Fairchild	54LS13	
	Motorola	SN54LS13	
	National	DM54LS13	
	Raytheon	54LS13	
	TI	SN54LS13	
54LS132	Fairchild	54LS132	
	Motorola	SN54LS132	
	National	DM54LS132	
	Raytheon	54LS132	
	TI	SN54LS132	
54LS136	Fairchild	54LS136	
	Motorola	SN54LS136	
	Raytheon	54LS136	
	TI	SN54LS136	
54LS138	Fairchild	54LS138	
	Motorola	SN54LS138	
	National	DM54LS138	
	Raytheon	54LS138	
	TI	SN54LS138	
54LS139	Fairchild	54LS139	
	Raytheon	54LS139	
54LS14	Fairchild	54LS14	
	Motorola	SN54LS14	
	National	DM54LS14	
	Raytheon	54LS14	
	TI	SN54LS14	
54LS15	Fairchild	54LS15	
	Motorola	SN54LS15	
	National	DM54LS15	
	Raytheon	54LS15	
	TI	SN54LS15	
54LS151	AMD	SN54LS151	
	Fairchild	54LS151	
	Motorola	SN54LS151	
	National	DM54LS151	
	Raytheon	54LS151	
	TI	SN54LS151	
54LS153	AMD	SN54LS153	
	Fairchild	54LS153	
	Motorola	SN54LS153	
	National	DM54LS153	
	Raytheon	54LS153	
54LS153	TI	SN54LS153	
54LS154	National	DM54LS154	
54LS157	AMD	SN54LS157	
	Fairchild	54LS157	
	Motorola	SN54LS157	
	National	DM54LS157	
	Raytheon	54LS157	
	TI	SN54LS157	
54LS158	Fairchild	54LS158	
	Motorola	SN54LS158	
	National	DM54LS158	
	Raytheon	54LS158	
	TI	SN54LS158	
54LS160	Fairchild	54LS160	
	Raytheon	54LS160	
54LS161	AMD	SN54LS161	
	Fairchild	54LS161	
	Motorola	SN54LS161A	
	National	DM54LS161	
	Raytheon	54LS161	
	TI	SN54LS161A	
54LS162	Fairchild	54LS162	
	Raytheon	54LS162	
54LS163	AMD	SN54LS163	
	Fairchild	54LS163	
	Motorola	SN54LS163A	
	National	DM54LS163	
	Raytheon	54LS163	
	TI	SN54LS163A	
54LS164	AMD	SN54LS164	
	Fairchild	54LS164	
	Motorola	SN54LS164A	
	National	DM54LS164	
	Raytheon	54LS164	
	TI	SN54LS164A	
54LS170	AMD	SN54LS170	
	Fairchild	54LS170	
	Motorola	SN54LS170	
	National	DM54LS170	
	Raytheon	54LS170	
	TI	SN54LS170	
54LS173	Fairchild	54LS173	
	National	DM54LS173	
	TI	SN54LS173	
54LS174	AMD	SN54LS174	
	Fairchild	54LS174	
	National	DM54LS174	
	Raytheon	54LS174	
	TI	SN54LS174	
54LS175	AMD	SN54LS175	
	Fairchild	54LS175	
	Motorola	SN54LS175	
	National	DM54LS175	
	Raytheon	54LS175	
	TI	SN54LS175	
54LS181	AMD	SN54LS181	
	Fairchild	54LS181	
	Motorola	SN54LS181	
	Raytheon	54LS181	
	TI	SN54LS181	
54LS190	AMD	SN54LS190	
	Fairchild	54LS190	
	Motorola	SN54LS190	
	National	DM54LS190	
	Raytheon	54LS190	
	TI	SN54LS190	
54LS191	AMD	SN54LS191	
	Fairchild	54LS191	
	Motorola	SN54LS191	
	National	DM54LS191	
	Raytheon	54LS191	
	TI	SN54LS191	
54LS192	AMD	SN54LS192	
	Fairchild	54LS192	
	Motorola	SN54LS192	
	National	DM54LS192	
	Raytheon	54LS192	
	TI	SN54LS192	
54LS193	AMD	SN54LS193	
	Fairchild	54LS193	
	Motorola	SN54LS193	
	National	DM54LS193	
	Raytheon	54LS193	
	TI	SN54LS193	
54LS194A	Fairchild	54LS28	
	Raytheon	54LS194A	

♦ Discontinued

The manufacturers report their devices can be used as direct replacements.
Performance details often differ, so compare the specifications considering your requirements.

Signetics (cont'd)

Manufacturer Device	Replacement Source	Device	IC Master Page
54LS195A	AMD	SN54LS195A	
	Fairchild	54LS195	
	Motorola	SN54LS195A	
	Raytheon	54LS195A	
	TI	SN54LS195A	
54LS196	Raytheon	54LS196	
54LS197	Raytheon	54LS197	
54LS20	Fairchild	54LS20	
	Motorola	SN54LS20	
	National	DM54LS20	
	Raytheon	54LS20	
	TI	SN54LS20	
54LS21	Fairchild	54LS21	
	Motorola	SN54LS21	
	National	DM54LS21	
	Raytheon	54LS21	
	TI	SN54LS21	
54LS22	Fairchild	54LS22	
	Motorola	SN54LS22	
	National	DM54LS22	
	Raytheon	54LS22	
	TI	SN54LS22	
54LS221	National	DM54LS221	
	Raytheon	54LS221	
	TI	SN54LS221	
54LS248	Motorola	SN54LS248	
54LS251	AMD	SN54LS251	
	Fairchild	54LS251	
	Motorola	SN54LS251	
	Raytheon	54LS251	
	TI	SN54LS251	
54LS253	AMD	SN54LS253	
	Fairchild	54LS253	
	Motorola	SN54LS253	
	National	DM54LS253	
	Raytheon	54LS253	
	TI	SN54LS253	
54LS257	Fairchild	54LS257	
	Motorola	SN54LS257A	
	National	DM54LS257	
	Raytheon	54LS257	
	TI	SN54LS257A	
54LS26	Fairchild	54LS26	
	Motorola	SN54LS26	
	National	DM54LS26	
	Raytheon	54LS26	
	TI	SN54LS26	
54LS260A	Motorola	SN54LS260A	
54LS261	Raytheon	54LS261	
	TI	SN54LS261	
54LS266	Fairchild	54LS266	
	Motorola	SN54LS266	
	Raytheon	54LS266	
	TI	SN54LS266	
54LS27	Fairchild	54LS27	
	Motorola	SN54LS27	
	National	DM54LS27	
	Raytheon	54LS27	
	TI	SN54LS27	
54LS279	Fairchild	54LS279	
	Motorola	SN54LS279	
	National	DM54LS279	
	Raytheon	74LS279	
	TI	SN54LS279	
54LS28	Fairchild	54LS28	
	Raytheon	54LS28	
	TI	SN54LS28	
54LS283	Fairchild	54LS283	
	Raytheon	54LS283	
54LS290	Fairchild	54LS290	
	Motorola	SN54LS290	
	TI	SN54LS290	
54LS293	Fairchild	54LS293	
	Motorola	SN54LS293	
	TI	SN54LS293	
54LS295A	Fairchild	54LS295	
	Raytheon	54LS295A	
54LS30	Fairchild	54LS30	
	Motorola	SN54LS30	
	National	DM54LS30	
	Raytheon	54LS30	
	TI	SN54LS30	
54LS32	Fairchild	54LS32	
54LS32	Motorola	SN54LS32	
	National	DM54LS32	
	Raytheon	54LS32	
	TI	SN54LS32	
54LS33	Fairchild	54LS33	
	Raytheon	54LS33	
	TI	SN54LS33	
54LS365	Fairchild	54LS365	
	Motorola	SN54LS365	
	Raytheon	54LS365	
	TI	SN54LS365	
54LS366	Fairchild	54LS366	
	Motorola	SN54LS366	
	Raytheon	54LS366	
	TI	SN54LS366	
54LS367	Fairchild	54LS367	
	Motorola	SN54LS367	
	Raytheon	54LS367	
	TI	SN54LS367	
54LS368	Fairchild	54LS368	
	Motorola	SN54LS368	
	Raytheon	54LS368	
	TI	SN54LS368	
54LS37	Fairchild	54LS37	
	Motorola	SN54LS37	
	National	DM54LS37	
	Raytheon	54LS37	
	TI	SN54LS37	
54LS373	Motorola	SN54LS373	
54LS375	Motorola	SN74LS375	
	TI	SN54LS375	
54LS38	Fairchild	54LS38	
	Motorola	SN54LS38	
	National	DM54LS38	
	Raytheon	54LS38	
	TI	SN54LS38	
54LS386	Raytheon	SN54LS386	
	TI	SN54LS386	
54LS395	Fairchild	54LS395	
	National	DM54LS395	
	Raytheon	54LS395	
	TI	SN54LS395	
54LS40	Fairchild	54LS40	
	Motorola	SN54LS40	
	National	DM54LS40	
	Raytheon	54LS40	
	TI	SN54LS40	
54LS42	Fairchild	54LS42	
	Motorola	SN54LS42	
	National	DM54LS42	
	Raytheon	54LS42	
	TI	SN54LS42	
54LS51	Fairchild	54LS51	
	Motorola	SN54LS51	
	National	DM54LS51	
	Raytheon	54LS51	
	TI	SN54LS51	
54LS54	Fairchild	54LS54	
	Motorola	SN54LS54	
	National	DM54LS54	
	Raytheon	54LS54	
	TI	SN54LS54	
54LS55	Fairchild	54LS55	
	Motorola	SN54LS55	
	National	DM54LS55	
	Raytheon	54LS55	
	TI	SN54LS55	
54LS670	Fairchild	54LS670	
	Motorola	SN54LS670	
	National	DM54LS670	
	Raytheon	54LS670	
	TI	SN54LS670	
54LS73	Fairchild	54LS73	
	Motorola	SN54LS73A	
	National	DM54LS73	
	Raytheon	54LS73	
	TI	SN54LS73A	
54LS74	Fairchild	54LS74	
	Motorola	SN54LS74A	
	National	DM54LS74	
	Raytheon	54LS74	
	TI	SN54LS74A	
54LS75	Motorola	SN54LS75	
	National	DM54LS75	
	Raytheon	54LS75	
	TI	SN54LS75	
54LS76	Fairchild	54LS76	
	Motorola	SN54LS76A	
	National	DM54LS76	
	Raytheon	54LS76	
	TI	SN54LS76	
54LS78	Fairchild	54LS78	
	Motorola	SN54LS78A	
	National	DM54LS78	
	Raytheon	54LS78	
	TI	SN54LS78	
54LS83	Fairchild	54LS83	
	Raytheon	54LS83A	
54LS85	Fairchild	54LS85	
	Motorola	SN54LS85	
	National	DM54LS85	
	Raytheon	54LS85	
	TI	SN54LS85	
54LS86	Fairchild	54LS86	
	Motorola	SN54LS86	
	Raytheon	54LS86	
	TI	SN54LS86	
54LS89	Motorola	SN54LS89	
54LS90	Fairchild	54LS90	
	Motorola	SN54LS90	
	Raytheon	54LS90	
	TI	SN54LS90	
54LS92	Motorola	SN54LS92	
	Raytheon	54LS92	
	TI	SN54LS92	
54LS93	Fairchild	54LS93	
	Motorola	SN54LS93	
	Raytheon	54LS93	
	TI	SN54LS93	
54LS95B	Fairchild	54LS95	
	Raytheon	54LS95B	
54LS96	TI	SN54LS96	
54S00	Fairchild	54S00	
	TI	SN54S00	
54S02	Fairchild	54S02	
	TI	SN54S02	
54S04	Fairchild	54S04	
	TI	SN54S04	
54S05	Fairchild	54S05	
	TI	SN54S05	
54S08	Fairchild	54S08	
	TI	SN54S08	
54S09	Fairchild	54S09	
	TI	SN54S09	
54S11	Fairchild	54S11	
	TI	SN54S11	
54S139	AMD	SN54S139	
	Fairchild	54S139	
	TI	SN54S139	
54S140	AMD	SN54S140	
	TI	SN54S140	
54S15	Fairchild	54S15	
	TI	SN54S15	
54S151	AMD	SN54S151	
	Fairchild	54S151	
	TI	SN54S151	
54S153	AMD	SN54S153	
	Fairchild	54S153	
	TI	SN54S153	
54S157	AMD	SN54S157	
	Fairchild	54S157	
	TI	SN54S157	
54S158	AMD	SN54S158	
	Fairchild	54S158	
	TI	SN54S158	
54S181	AMD	SN54S181	
	Fairchild	93S41	
	TI	SN54S181	
54S22	Fairchild	54S22	
	National	DM54S22	
	TI	SN54S22	
54S251	AMD	SN54S251	
	Fairchild	54S251	
	TI	SN54S251	
54S253	AMD	SN54S253	
	Fairchild	54S253	
54S257	AMD	SN54S257	
	Fairchild	54S257	
	TI	SN74S257	
54S258	AMD	SN54S258	
	Fairchild	54S258	
	TI	SN54S258	
54S301	TI	SN54S301	
54S32	Fairchild	54S32	
	TI	SN54S32	
54S37	TI	SN54S37	
54S85	TI	SN54S85	
54S86	Fairchild	54S86	
	TI	SN54S86	
5400	Fairchild	5400	
	Motorola	MC5400	
	National	DM5400	
	TI	SN5400	
5401	Fairchild	5401	
	Motorola	MC5401	
	National	DM5401	
	Raytheon	5401	
	TI	SN5401	
5402	Fairchild	5402	
	Motorola	MC5402	
	National	DM5402	
	TI	SN5402	
5403	Fairchild	5403	
	Motorola	MC5403	
	National	DM5403	
	TI	SN5403	
5404	Fairchild	5404	
	Motorola	MC5404	
	National	DM5404	
	TI	SN5404	
5405	Fairchild	5405	
	Motorola	MC5405	
	National	DM5405	
	TI	SN5405	
5406	Fairchild	5406	
	Motorola	MC5406	
	National	DM5406	
	TI	SN5406	
5407	Fairchild	5407	
	Motorola	MC5407	
	National	DM5407	
	TI	SN5407	
5408	Fairchild	5408	
	Motorola	MC5408	
	National	DM5408	
	TI	SN5408	
5409	Fairchild	5409	
	Motorola	MC5409	
	National	DM5409	
	TI	SN5409	
5410	Fairchild	5410	
	Motorola	MC5410	
	National	DM5410	
	TI	SN5410	
54100	Motorola	MC54100	
	TI	SN54100	
54107	Fairchild	54107	
	Motorola	MC54107	
	National	DM54107	
	TI	SN54107	
54109	Fairchild	9024	
	National	DM54109	
	TI	SN54109	
5411	Fairchild	5411	
	National	DM5411	
	TI	SN5411	
54116	Fairchild	54116	
	TI	SN54116	
5412	Fairchild	5412	
	TI	SN5412	
54121	Fairchild	54121	
	Motorola	MC54121	
	National	DM54121	
	TI	SN54121	
54123	AMD	SN54123	
	Fairchild	54123	
	Motorola	MC54123	
	National	DM54123	
	TI	SN54123	
54125	Fairchild	54125	
	National	DM54125	
	TI	SN54125	
54126	Fairchild	54126	
	National	DM54126	
	TI	SN54126	
5413	Fairchild	5413	
	Motorola	MC5413	

♦ Discontinued

Bold face device numbers indicate manufacturers data is provided in the IC Master on the pages noted.

Signetics (cont'd)

Manufacturer Device	Replacement Source	Device	IC Master Page
5413	National	DM5413	
	TI	SN5413	
54132	Fairchild	54132	
	Motorola	MC54132	
	National	DM54132	
	TI	SN54132	
5414	Fairchild	5414	
	Motorola	MC5414	
	National	DM5414	
	TI	SN5414	
54145	Fairchild	54145	
	Motorola	MC54145	
	National	DM54145	
	TI	SN54145	
54147	National	DM54147	
	TI	SN54147	
54148	Fairchild	9318	
	National	DM54148	
	TI	SN54148	
54150	Fairchild	54150	
	Motorola	MC54150	
	National	DM54150	
	TI	SN54150	
54151	Fairchild	54151	
	Motorola	MC54151	
	National	DM54151	
	TI	SN54151	
54152	Fairchild	54152	
	Motorola	MC54152	
	TI	SN54152	
54153	Fairchild	54153	
	Motorola	MC54153	
	National	DM54153	
	TI	SN54153	
54154	AMD	SN54154	
	Fairchild	54154	
	Motorola	MC54154	
	National	DM54154	
	TI	SN54154	
54155	Fairchild	54155	
	Motorola	MC54155	
	National	DM54155	
	Raytheon	54155	
	TI	SN54155	
54156	Fairchild	54156	
	Motorola	MC54156	
	National	DM54156	
	TI	SN54156	
54157	AMD	SN54157	
	Fairchild	54157	
	Motorola	MC54157	
	National	DM54157	
	TI	SN54157	
5416	Fairchild	5416	
	Motorola	MC5416	
	National	DM5416	
	TI	SN5416	
54160	AMD	SN54160	
	Fairchild	54160	
	Motorola	MC54160	
	National	DM54160	
	TI	SN54160	
54161	AMD	SN54161	
	Fairchild	54161	
	Motorola	MC54161	
	National	DM54161	
	TI	SN54161	
54162	AMD	SN54162	
	Fairchild	54162	
	Motorola	MC54162	
	National	DM54162	
	TI	SN54162	
54163	AMD	SN54163	
	Fairchild	54163	
	Motorola	MC54163	
	National	DM54163	
	TI	SN54163	
54164	AMD	SN54164	
	Fairchild	54164	
	National	DM54164	
	TI	SN54164	
54165	Fairchild	54165	
	Motorola	MC54165	
54165	National	DM54165	
	TI	SN54165	
54166	Fairchild	54166	
	National	DM54166	
	TI	SN54166	
5417	Fairchild	5417	
	Motorola	MC5417	
	National	DM5417	
	TI	SN5417	
54170	Fairchild	54170	
	National	DM54170	
	TI	SN54170	
54174	AMD	SN74174	
	Fairchild	54174	
	Motorola	MC54174	
	National	DM54174	
	TI	SN54174	
54175	AMD	SN54175	
	Fairchild	54175	
	Motorola	MC54175	
	National	DM54175	
	TI	SN54175	
54176	Fairchild	54176	
	Motorola	MC54176	
	National	DM54176	
	TI	SN54176	
54177	Fairchild	54177	
	Motorola	MC54177	
	National	DM54177	
	TI	SN54177	
54180	Fairchild	54180	
	Motorola	MC54180	
	National	DM54180	
	TI	SN54180	
54181	AMD	SN54181	
	Fairchild	54181	
	Motorola	MC54181	
	National	DM54181	
	TI	SN54181	
54182	AMD	SN54182	
	Fairchild	54182	
	Motorola	MC54182	
	National	DM54182	
	TI	SN54182	
54190	Fairchild	54190	
	Motorola	MC54190	
	National	DM54190	
	TI	SN54190	
54191	Fairchild	54191	
	Motorola	MC54191	
	National	DM54191	
	TI	SN54191	
54192	AMD	SN54192	
	Fairchild	54192	
	Motorola	MC54192	
	National	DM54192	
	TI	SN54192	
54193	AMD	SN54193	
	Fairchild	54193	
	Motorola	MC54193	
	National	DM54193	
	TI	SN54193	
54194	AMD	SN54194	
	Fairchild	54194	
	Motorola	MC54194	
	National	DM54194	
	TI	SN54194	
54195	AMD	SN54195	
	Fairchild	54195	
	Motorola	MC54195	
	National	DM54195	
	TI	SN54195	
54196	Fairchild	54196	
	Motorola	MC54196	
	National	DM54196	
	TI	SN54196	
54197	Fairchild	54197	
	Motorola	MC54197	
	National	DM54197	
	TI	SN54197	
54198	Fairchild	54198	
	National	DM54198	
	TI	SN54198	
54199	Fairchild	54199	
	National	DM54199	
	TI	SN54199	
5420	Fairchild	5420	
	Motorola	MC5420	
	National	DM5420	
	TI	SN5420	
5421	Fairchild	5421	
54221	AMD	SN54221	
5426	Fairchild	5426	
	Motorola	MC5426	
	National	DM5426	
	TI	SN5426	
54279	Fairchild	54279	
	TI	SN54279	
54298	Fairchild	54298	
	Motorola	MC54298	
	TI	SN54298	
5430	Fairchild	5430	
	Motorola	MC5430	
	National	DM5430	
	TI	SN5430	
5432	Fairchild	5432	
	National	DM5432	
	TI	SN5432	
5437	Fairchild	5437	
	Motorola	MC5437	
	National	DM5437	
	TI	SN5437	
5438	Fairchild	5438	
	Motorola	MC5438	
	National	DM5438	
	TI	SN5438	
5440	Fairchild	5440	
	Motorola	MC5440	
	National	DM5440	
	TI	SN5440	
5442	Fairchild	5442	
	Motorola	MC5442	
	National	DM5442	
	TI	SN5442	
5443	Fairchild	5443	
	Motorola	MC5443	
	TI	SN5443	
5444	Fairchild	5444	
	Motorola	MC5444	
	TI	SN5444	
5445	Fairchild	5445	
	Motorola	MC5445	
	National	DM5445	
	TI	SN5445	
5446	Fairchild	5446	
	Motorola	MC5446	
	National	DM5446	
	TI	SN5446	
5447	Fairchild	5447	
	Motorola	MC5447	
	National	DM5447	
	TI	SN5447	
5448	Fairchild	5448	
	Motorola	MC5448	
	National	DM5448	
	TI	SN5448	
5450	Fairchild	5450	
	Motorola	MC5450	
	National	DM5450	
	TI	SN5450	
5451	Fairchild	5451	
	Motorola	MC5451	
	National	DM5451	
	TI	SN5451	
5453	Fairchild	5453	
	Motorola	MC5453	
	National	DM5453	
	TI	SN5453	
5454	Fairchild	5454	
	Motorola	MC5454	
	National	DM5454	
	TI	SN5454	
5460	Fairchild	5460	
	Motorola	MC5460	
	National	DM5460	
	TI	SN5460	
5472	Fairchild	5472	
	Motorola	MC5472	
	National	DM5472	
	TI	SN5472	
5473	Fairchild	5473	
	Motorola	MC5473	
5473	National	DM5473	
	TI	SN5473	
5474	Fairchild	5474	
	Motorola	MC5474	
	National	DM5474	
	TI	SN5474	
5475	Fairchild	5475	
	Motorola	MC5475	
	National	DM5475	
	TI	SN5475	
5476	Fairchild	5476	
	Motorola	MC5476	
	National	DM5476	
	TI	SN5476	
5477	Fairchild	5477	
	Motorola	MC5477	
	TI	SN5477	
5480	Fairchild	5480	
	Motorola	MC5480	
	TI	SN5480	
5485	Fairchild	5485	
	Motorola	MC5485	
	National	DM5485	
	TI	SN5485	
5486	Fairchild	5486	
	Motorola	MC5486	
	National	DM5486	
	TI	SN5486	
5490	Fairchild	5490	
	Motorola	MC5490	
	National	DM5490	
	TI	SN5490	
5491	Fairchild	5491	
	Motorola	MC5491	
	National	DM5491	
	TI	SN5491	
5492	Fairchild	5492	
	Motorola	MC5492	
	National	DM5492	
	TI	SN5492	
5495	Fairchild	5495	
	Motorola	MC5495	
	National	DM5495	
	TI	SN5495	
5496	Fairchild	5496	
	Motorola	MC5496	
	National	DM5496	
	TI	SN5496	
55325	Silicon G	SG55325	
	TI	SN55325	
55450	Silicon G	SG55450	
	TI	SN55450	
55451	Silicon G	SG55451	
	TI	SN55451	
55452	Silicon G	SG55452	
	TI	SN55452	
55453	Silicon G	SG55453	
	TI	SN55453	
55454	Silicon G	SG55454	
	TI	SN55454	
72S180	National	DM85S229	
72S52	National	DM8301	
7293	National	DM74LS197	
74H00	Fairchild	74H00	
	National	DM74H00	
	NEC America	μPB74H00	
	Raytheon	74H00	
	TI	SN74H00	
74H01	Fairchild	74H01	
	National	DM74H01	
	NEC America	μPB74H01	
	Raytheon	74H01	
	TI	SN74H01	
74H04	Fairchild	74H04	
	National	DM74H04	
	NEC America	μPB74H04	
	Raytheon	74H04	
	TI	SN74H04	
74H05	Raytheon	74H05	
	TI	SN74H05	
74H08	Fairchild	74H08	
	National	DM74H08	
74H10	Fairchild	74H10	
	National	DM74H10	
	NEC America	μPB74H10	
	Raytheon	74H10	

♦ Discontinued

The manufacturers report their devices can be used as direct replacements.
Performance details often differ, so compare the specifications considering your requirements.

Signetics (cont'd)

Manufacturer Device	Replacement Source	Device	IC Master Page
74H10	TI	SN74H10	
74H102	Fairchild	74H102	
	TI	SN74H102	
74H103	Fairchild	74H103	
	National	DM74H103	
	TI	SN74H103	
74H106	Fairchild	74H106	
	National	DM74H106	
	TI	SN74H106	
74H108	Fairchild	74H108	
	National	DM74H108	
	TI	SN74H108	
74H11	Fairchild	74H11	
	National	DM74H11	
	Raytheon	74H11	
	TI	SN74H11	
74H20	Fairchild	74H20	
	National	DM74H20	
	NEC America	μPB74H20	
	Raytheon	74H20	
	TI	SN74H20	
74H21	Fairchild	74H21	
	National	DM74H21	
	TI	SN74H21	
74H22	Fairchild	74H22	
	National	DM74H22	
	Raytheon	74H22	
	TI	SN74H22	
74H30	Fairchild	74H30	
	National	DM74H30	
	NEC America	μPB74H30	
	TI	SN74H30	
74H40	Fairchild	74H40	
	National	DM74H40	
	NEC America	μPB74H40	
	Raytheon	74H40	
	TI	SN74H40	
74H50	Fairchild	74H50	
	National	DM74H50	
	TI	SN74H50	
74H51	Fairchild	74H51	
	National	DM74H51	
	NEC America	μPB74H51	
	TI	SN74H51	
74H52	Fairchild	74H52	
	National	DM74H52	
	TI	SN74H52	
74H53	Fairchild	74H53	
	National	DM74H53	
	TI	SN74H53	
74H54	Fairchild	74H54	
	National	DM74H54	
	TI	SN74H54	
74H55	Fairchild	74H55	
	National	DM74H55	
	TI	SN74H55	
74H60	Fairchild	74H60	
	National	DM74H60	
	TI	SN74H60	
74H61	Fairchild	74H61	
	TI	SN74H61	
74H62	Fairchild	74H62	
	National	DM74H62	
	TI	SN74H62	
74H71	Fairchild	74H71	
	National	DM74H71	
	TI	SN74H71	
74H72	Fairchild	74H72	
	National	DM74H72	
	TI	SN74H72	
74H73	Fairchild	74H73	
	National	DM74H73	
	TI	SN74H73	
74H74	Fairchild	74H74	
	National	DM74H74	
	Raytheon	74H74	
	TI	SN74H74	
74H76	Fairchild	74H76	
	National	DM74H76	
	TI	SN74H76	
74LS00	Fairchild	74LS00	
	Hitachi	HD74LS00	
	Motorola	SN74LS00	
74LS00	National	DM74LS00	
	NEC America	μPB74LS00	
	Raytheon	74LS00	
	TI	SN74LS00	
74LS01	Fairchild	SN74LS109A	
	Hitachi	HD74LS01	
	National	DM74LS01	
	Raytheon	74LS01	
	TI	SN74LS01	
74LS02	Fairchild	74LS02	
	Hitachi	HD74LS02	
	Motorola	SN74LS02	
	National	DM74LS02	
	NEC America	μPB74LS02	
	Raytheon	74LS02	
	TI	SN74LS02	
74LS03	Fairchild	74LS03	
	Hitachi	HD74LS03	
	Motorola	SN74LS03	
	National	DM74LS03	
	NEC America	μPB74LS03	
	Raytheon	74LS03	
	TI	SN74LS03	
74LS04	Fairchild	74LS04	
	Hitachi	HD74LS04	
	Motorola	SN74LS04	
	National	DM74LS04	
	NEC America	μPB74LS04	
	Raytheon	74LS04	
	TI	SN74LS04	
74LS05	Fairchild	74LS05	
	Hitachi	HD74LS05	
	Motorola	SN74LS05	
	National	DM74LS05	
	NEC America	μPB74LS05	
	Raytheon	74LS05	
	TI	SN74LS05	
74LS08	Fairchild	74LS08	
	Motorola	SN74LS08	
	National	DM74LS08	
	NEC America	μPB74LS08	
	Raytheon	74LS08	
	TI	SN74LS08	
74LS09	Fairchild	74LS09	
	Hitachi	HD74LS09	
	Motorola	SN74LS09	
	National	DM74LS09	
	Raytheon	74LS09	
	TI	SN74LS09	
74LS10	Fairchild	74LS10	
	Hitachi	HD74LS10	
	Motorola	SN74LS10	
	National	DM74LS10	
	NEC America	μPB74LS10	
	Raytheon	74LS10	
	TI	SN74LS10	
74LS107	Fairchild	74LS107	
	Hitachi	HD74LS107	
	Motorola	SN74LS107A	
	National	DM74LS107	
	Raytheon	74LS107	
	TI	SN74LS107	
74LS109	Fairchild	74LS109	
	National	DM74LS109	
	NEC America	μPB74LS109	
	Raytheon	74LS109	
	TI	SN74LS109A	
74LS11	Fairchild	74LS11	
	Hitachi	HD74LS11	
	Motorola	SN74LS11	
	National	DM74LS11	
	NEC America	μPB74LS11	
	Raytheon	74LS11	
	TI	SN74LS11	
74LS112	Hitachi	HD74LS112	
	Motorola	SN74LS112A	
	National	DM74LS112	
	NEC America	μPB74LS112	
	Raytheon	74LS112	
	TI	SN74LS112	
74LS113	Fairchild	74LS113	
	Hitachi	HD74LS113	
	Motorola	SN74LS113A	
	National	DM74LS113	
	NEC America	μPB74LS113	
	Raytheon	74LS113	
74LS113	TI	SN74LS113	
74LS114	Fairchild	74LS114	
	Hitachi	HD74LS114	
	Motorola	SN74LS114A	
	National	DM74LS114	
	Raytheon	74LS114	
	TI	SN74LS114A	
74LS12	Fairchild	74LS12	
	Hitachi	HD74LS12	
	Motorola	SN74LS12	
	National	DM74LS12	
	Raytheon	74LS12	
	TI	SN74LS12	
74LS125	Fairchild	74LS125	
	National	DM74LS125	
	Raytheon	74LS125	
	TI	SN74LS125A	
74LS126	Fairchild	74LS126	
	Motorola	SN74LS126	
	National	DM74LS126	
	Raytheon	74LS126	
	TI	SN74LS126A	
74LS13	Fairchild	74LS13	
	Hitachi	HD74LS13	
	Motorola	SN74LS13	
	National	DM74LS13	
	Raytheon	74LS13	
	TI	SN74LS13	
74LS132	Fairchild	74LS132	
	Hitachi	HD74LS132	
	Motorola	SN74LS132	
	National	DM74LS132	
	Raytheon	74LS132	
	TI	SN74LS132	
74LS136	Fairchild	74LS136	
	Hitachi	HD74LS136	
	Motorola	SN74LS136	
	National	DM74LS136	
	Raytheon	74LS136	
	TI	SN74LS136	
74LS138	AMD	SN74LS138	
	Fairchild	74LS138	
	Hitachi	HD74LS138	
	Motorola	SN74LS138	
	National	DM74LS138	
	NEC America	μPB74LS138	
	Raytheon	74LS138	
	TI	SN74LS138	
74LS139	AMD	SN54LS139	
		SN74LS139	
	Fairchild	54LS139	
		74LS139	
	Hitachi	HD74LS139	
	Motorola	SN54LS139	
		SN74LS139	
	National	DM54LS139	
		DM74LS139	
	NEC America	μPB74LS139	
	Raytheon	54LS139	
		74LS139	
	TI	SN54LS139	
		SN74LS139	
74LS14	Fairchild	74LS14	
	Hitachi	HD74LS14	
	Motorola	SN74LS14	
	National	DM74LS14	
	Raytheon	74LS14	
	TI	SN74LS14	
74LS145	TI	SN74LS145	
74LS15	Fairchild	74LS15	
	Hitachi	HD74LS15	
	Motorola	SN74LS15	
	National	DM74LS15	
	Raytheon	74LS15	
	TI	SN74LS15	
74LS151	AMD	SN74LS151	
	Fairchild	74LS151	
	Hitachi	HD74LS151A	
	Motorola	SN74LS151	
	National	DM74LS151	
	NEC America	μPB74LS151	
	Raytheon	74LS151	
	TI	SN74LS151	
74LS152	Fairchild	74LS152	
	Raytheon	74LS152	
74LS153	AMD	SN74LS153	
74LS153	Fairchild	74LS153	
	Hitachi	HD74LS153	
	Motorola	SN74LS153	
	National	DM74LS153	
	NEC America	μPB74LS153	
	Raytheon	74LS153	
	TI	SN74LS153	
74LS154	National	DM74LS154	
74LS155	Fairchild	74LS155	
	Hitachi	HD74LS155	
	Motorola	SN74LS155	
	National	DM74LS155	
	NEC America	μPB74LS155	
	Raytheon	74LS155	
	TI	SN74LS155	
74LS156	Fairchild	74LS156	
	Hitachi	HD74LS156	
	Motorola	SN74LS156	
	National	DM74LS156	
	Raytheon	74LS156	
	TI	SN74LS156	
74LS157	AMD	SN74LS157	
	Fairchild	74LS157	
	Motorola	SN74LS157	
	National	DM74LS157	
	NEC America	μPB74LS157	
	Raytheon	74LS157	
	TI	SN74LS157	
74LS158	AMD	SN74LS158	
	Fairchild	74LS158	
	Hitachi	HD74LS158	
	Motorola	SN74LS158	
	National	DM74LS158	
	Raytheon	74LS158	
	TI	SN74LS158	
74LS160	AMD	SN74LS160	
	Fairchild	74LS160	
	Motorola	SN74LS160A	
	National	DM74LS160	
	Raytheon	74LS160	
	TI	SN74LS160A	
74LS160A	Hitachi	HD74LS160A	
74LS161	AMD	SN74LS161	
	Fairchild	74LS161	
	Motorola	SN74LS161A	
	National	DM74LS161	
	NEC America	μPB74LS161	
	Raytheon	74LS161	
	TI	SN74LS161A	
74LS161A	Hitachi	HD74LS161A	
74LS162	AMD	SN74LS162	
	Fairchild	74LS162	
	Motorola	SN74LS162A	
	National	DM74LS162	
	Raytheon	74LS162	
	TI	SN74LS162A	
74LS162A	Hitachi	HD74LS162A	
74LS163	AMD	SN74LS163	
	Fairchild	74LS163	
	Motorola	SN74LS163A	
	National	DM74LS163	
	Raytheon	74LS163	
	TI	SN74LS163A	
74LS163A	Hitachi	HD74LS163A	
74LS164	AMD	SN74LS164	
	Fairchild	74LS164	
	Hitachi	HD74LS164	
	Motorola	SN74LS164A	
	National	DM74LS164	
	NEC America	μPB74LS164	
	Raytheon	74LS164	
	TI	SN74LS164A	
74LS170	AMD	SN74LS170	
	Fairchild	74LS170	
	Motorola	SN74LS170	
	National	DM74LS170	
	Raytheon	74LS170	
	TI	SN74LS170	
74LS173	Fairchild	74LS173	
	National	DM74LS173	
	TI	SN74LS173	
74LS174	AMD	SN74LS174	
	Fairchild	74LS174	
	Hitachi	HD74LS174	
	Motorola	SN74LS174	
	National	DM74LS174	

♦ Discontinued

Bold face device numbers indicate manufacturers data is provided in the IC Master on the pages noted.

Signetics (cont'd)

Manufacturer Device	Replacement Source	Device	IC Master Page
74LS174	Raytheon	74LS174	
	TI	SN74LS174	
74LS175	AMD	SN74LS175	
	Fairchild	74LS175	
	Hitachi	HD74LS175	
	Motorola	SN74LS175	
	National	DM74LS175	
	NEC America	μPB74LS175	
	Raytheon	74LS175	
	TI	SN74LS175	
74LS181	AMD	SN74LS181	
	Fairchild	74LS181	
	Motorola	SN74LS181	
	Raytheon	74LS181	
	TI	SN74LS181	
74LS190	AMD	SN74LS190	
	Fairchild	74LS190	
	Motorola	SN74LS190	
	National	DM74LS190	
	Raytheon	74LS190	
	TI	SN74LS190	
74LS191	AMD	SN74LS191	
	Fairchild	74LS191	
	Motorola	SN74LS191	
	National	DM74LS191	
	Raytheon	74LS191	
	TI	SN74LS191	
74LS192	AMD	SN74LS192	
	Fairchild	74LS192	
	Motorola	SN74LS192	
	National	DM74LS192	
	NEC America	μPB74LS192	
	Raytheon	74LS192	
	TI	SN74LS192	
74LS193	AMD	SN74LS193	
	Fairchild	74LS193	
	Motorola	SN74LS193	
	National	DM74LS193	
	NEC America	μPB74LS193	
	Raytheon	74LS193	
	TI	SN74LS193	
74LS194A	AMD	SN74LS194A	
	Fairchild	74LS194	
	Hitachi	HD74LS194A	
	Motorola	SN74LS194	
	National	DM74LS194	
	NEC America	μPB74LS194	
	Raytheon	74LS194A	
	TI	SN74LS194A	
74LS195A	AMD	SN74LS195A	
	Fairchild	74LS195	
	Hitachi	HD74LS195A	
	Motorola	SN74LS195	
	National	DM74LS195	
	NEC America	μPB74LS195	
	Raytheon	74LS195A	
	TI	SN74LS195A	
74LS196	Fairchild	74LS196	
	Motorola	SN74LS196	
	National	DM74LS196	
	Raytheon	74LS196	
	TI	SN74LS196	
74LS197	Fairchild	74LS197	
	Motorola	SN74LS197	
	National	DM74LS197	
	Raytheon	74LS197	
	TI	SN74LS197	
74LS20	Fairchild	74LS20	
	Hitachi	HD74LS20	
	Motorola	SN74LS20	
	National	DM74LS20	
	NEC America	μPB74LS20	
	Raytheon	74LS20	
	TI	SN74LS20	
74LS21	Fairchild	74LS21	
	Hitachi	HD74LS21	
	Motorola	SN74LS21	
	National	DM74LS21	
	NEC America	μPB74LS21	
	Raytheon	74LS21	
	TI	SN74LS21	
74LS22	Fairchild	74LS22	
	Hitachi	HD74LS22	
74LS22	Motorola	SN74LS22	
	National	DM74LS22	
	Raytheon	74LS22	
	TI	SN74LS22	
74LS221	Motorola	SN74LS221	
	National	DM74LS221	
	Raytheon	74LS221	
	TI	SN74LS221	
74LS240	AMD	SN74LS240	
	Fairchild	74LS240	
	MMI	**74LS240**	**768**
	Motorola	SN74LS240	
	Raytheon	**74LS240**	**522**
	TI	SN74LS240	
74LS241	AMD	SN74LS241	
	Fairchild	74LS241	
	MMI	**74LS241**	**768**
	Motorola	SN74LS241	
	Raytheon	**74LS241**	**525**
	TI	SN74LS241	
74LS242	AMD	SN74LS242	
	Fairchild	74LS242	
	Motorola	SN74LS242	
	Raytheon	**74LS242**	**528**
	TI	SN74LS242	
74LS243	AMD	SN74LS243	
	Fairchild	74LS243	
	Motorola	SN74LS243	
	Raytheon	**74LS243**	**528**
	TI	SN74LS243	
74LS244	AMD	SN74LS244	
	Fairchild	74LS244	
	MMI	**74LS244**	**768**
	Motorola	SN74LS244	
	Raytheon	**74LS244**	**525**
	TI	SN74LS244	
74LS245	Motorola	SN74LS245	
74LS251	AMD	SN74LS251	
	Fairchild	74LS251	
	Hitachi	HD74LS251	
	Motorola	SN74LS251	
	National	DM74LS251	
	NEC America	μPB74LS251	
	Raytheon	74LS251	
	TI	SN74LS251	
74LS253	AMD	SN74LS253	
	Fairchild	74LS253	
	Hitachi	HD74LS253	
	Motorola	SN74LS253	
	National	DM74LS253	
	NEC America	μPB74LS253	
	Raytheon	74LS253	
	TI	SN74LS253	
74LS257	AMD	SN74LS257	
	Fairchild	74LS257	
	Hitachi	HD74LS257	
	Motorola	SN74LS257A	
	National	DM74LS257	
	NEC America	μPB74LS257	
	Raytheon	74LS257	
	TI	SN74LS257A	
74LS258	AMD	SN74LS258	
	Fairchild	74LS258	
	Motorola	SN74LS258A	
	National	DM74LS258	
	NEC America	μPB74LS258	
	Raytheon	74LS258	
	TI	SN74LS258A	
74LS26	Fairchild	74LS26	
	Hitachi	HD74LS26	
	Motorola	SN74LS26	
	National	DM74LS26	
	Raytheon	74LS26	
	TI	SN74LS26	
74LS260	Fairchild	74LS260	
74LS261	Raytheon	74LS261	
	TI	SN74LS261	
74LS266	Fairchild	74LS266	
	Motorola	SN74LS266	
	Raytheon	74LS266	
	TI	SN74LS266	
74LS27	Fairchild	74LS27	
	Hitachi	HD74LS27	
	Motorola	SN74LS27	
	National	DM74LS27	
	NEC America	μPB74LS27	
74LS27	Raytheon	74LS27	
	TI	SN74LS27	
74LS273	AMD	SN74LS273	
	Fairchild	74LS273	
	TI	SN74LS273	
74LS279	Fairchild	74LS279	
	Motorola	SN74LS279	
	National	DM74LS279	
	NEC America	μPB74LS279	
	Raytheon	74LS279	
	TI	SN74LS279	
74LS28	Fairchild	74LS28	
	Raytheon	74LS28	
	TI	SN74LS28	
74LS283	Fairchild	74LS283	
	Motorola	SN74LS283	
	National	DM74LS283	
	Raytheon	74LS283	
	TI	SN74LS283	
74LS290	Fairchild	74LS290	
	Motorola	SN74LS290	
	National	DM74LS290	
	TI	SN74LS290	
74LS293	Fairchild	74LS293	
	Motorola	SN74LS293	
	National	DM74LS293	
	TI	SN74LS293	
74LS295	Fairchild	74LS295	
	Motorola	SN74LS295	
	NEC America	μPB74LS295	
	Raytheon	74LS295A	
	TI	SN74LS295B	
74LS295A	Raytheon	74LS295A	
74LS298	Fairchild	74LS298	
	Hitachi	HD74LS298	
	Motorola	SN74LS298	
	Raytheon	74LS298	
	TI	SN74LS298	
74LS30	Fairchild	74LS30	
	Hitachi	HD74LS30	
	Motorola	SN74LS30	
	National	DM74LS30	
	NEC America	μPB74LS30	
	Raytheon	74LS30	
	TI	SN74LS30	
74LS32	Fairchild	74LS32	
	Hitachi	HD74LS32	
	Motorola	SN74LS32	
	National	DM74LS32	
	NEC America	μPB74LS32	
	Raytheon	74LS32	
	TI	SN74LS32	
74LS33	Fairchild	74LS33	
	Raytheon	74LS33	
	TI	SN74LS33	
74LS365	Fairchild	74LS365	
	Motorola	SN74LS365	
	National	DM74LS365	
	NEC America	μPB74LS365	
	Raytheon	74LS365	
	TI	SN74LS365	
74LS366	Fairchild	74LS366	
	Motorola	SN74LS366	
	National	DM74LS366	
	NEC America	μPB74LS366	
	Raytheon	74LS366	
	TI	SN74LS366	
74LS367	Fairchild	74LS367	
	Hitachi	HD74LS367	
	Motorola	SN74LS367	
	National	DM74LS367	
	NEC America	μPB74LS367	
	Raytheon	74LS367	
	TI	SN74LS367	
74LS368	Fairchild	74LS368	
	Hitachi	HD74LS368	
	Motorola	SN74LS368	
	National	DM74LS368	
	NEC America	μPB74LS368	
	Raytheon	74LS368	
	TI	SN74LS368	
74LS37	Fairchild	74LS37	
	Hitachi	HD74LS37	
	Motorola	SN74LS37	
	National	DM74LS37	
	NEC America	μPB74LS37	
74LS37	Raytheon	74LS37	
	TI	SN74LS37	
74LS373	AMD	SN74LS373	
	Fairchild	74LS373	
	MMI	**74LS373**	**505**
	Motorola	SN74LS373	
	Raytheon	**74LS373**	**543**
	TI	SN74LS373	
74LS375	Fairchild	74LS375	
	Motorola	SN74LS375	
	NEC America	μPB74LS375	
	Raytheon	74LS375	
	TI	SN74LS375	
74LS377	AMD	SN74LS377	
	Fairchild	74LS377	
	Raytheon	**74LS377**	**549**
	TI	SN74LS377	
74LS378	AMD	SN74LS378	
	Fairchild	74LS378	
	TI	SN74LS378	
74LS38	Fairchild	74LS38	
	Hitachi	HD74LS38	
	Motorola	SN74LS38	
	National	DM74LS38	
	NEC America	μPB74LS38	
	Raytheon	74LS38	
	TI	SN74LS38	
74LS386	Hitachi	HD74LS386	
	Motorola	SN74LS386	
	National	DM74LS386	
	Raytheon	74LS386	
	TI	SN74LS386	
74LS395	Fairchild	74LS395	
	National	DM74LS395	
	Raytheon	74LS395	
	TI	SN74LS395	
74LS40	Fairchild	74LS40	
	Hitachi	HD74LS40	
	Motorola	SN74LS40	
	National	DM74LS40	
	NEC America	μPB74LS40	
	Raytheon	74LS40	
	TI	SN74LS40	
74LS42	Fairchild	74LS42	
	Hitachi	HD74LS42	
	Motorola	SN74LS42	
	National	DM74LS42	
	NEC America	μPB74LS42	
	Raytheon	74LS42	
	TI	SN74LS42	
74LS48	Motorola	SN74LS48	
74LS51	Fairchild	74LS51	
	Hitachi	HD74LS51	
	Motorola	SN74LS51	
	National	DM74LS51	
	NEC America	μPB74LS51	
	Raytheon	74LS51	
	TI	SN74LS51	
74LS54	Fairchild	74LS54	
	Hitachi	HD74LS54	
	Motorola	SN74LS54	
	National	DM74LS54	
	NEC America	μPB74LS54	
	Raytheon	74LS54	
	TI	SN74LS54	
74LS55	Fairchild	74LS55	
	Hitachi	HD74LS55	
	Motorola	SN74LS55	
	National	DM74LS55	
	NEC America	μPB74LS55	
	Raytheon	74LS55	
	TI	SN74LS55	
74LS670	Fairchild	74LS670	
	Motorola	SN74LS670	
	National	DM74LS670	
	Raytheon	74LS670	
	TI	SN74LS670	
74LS73	Fairchild	74LS73	
	Hitachi	HD74LS73	
	Motorola	SN74LS73A	
	National	DM74LS73	
	Raytheon	74LS73	
	TI	SN74LS73A	
74LS74	Fairchild	74LS74	
	Hitachi	HD74LS74A	
	Motorola	SN74LS74A	

♦ Discontinued

The manufacturers report their devices can be used as direct replacements.
Performance details often differ, so compare the specifications considering your requirements.

Signetics (cont'd)

Manufacturer Device	Replacement Source	Replacement Device	IC Master Page
74LS74	National	DM74LS74	
	NEC America	μPB74LS74	
	Raytheon	74LS74	
	TI	SN74LS74A	
74LS75	Motorola	SN74LS75	
	National	DM74LS75	
	Raytheon	74LS75	
	TI	SN74LS75	
74LS76	Fairchild	74LS76	
	Hitachi	HD74LS76	
	Motorola	SN74LS76A	
	National	DM74LS76	
	Raytheon	74LS76	
	TI	SN74LS76	
74LS78	Fairchild	74LS78	
	Hitachi	HD74LS78	
	Motorola	SN74LS78A	
	National	DM74LS78	
	Raytheon	74LS78	
	TI	SN74LS78	
74LS83	Fairchild	74LS83	
	Motorola	SN74LS83A	
	National	DM74LS83	
		DM74LS83A	
	Raytheon	74LS83	
		74LS83A	
	TI	SN74LS83A	
74LS85	Fairchild	74LS85	
	Motorola	SN74LS85	
	National	DM74LS85	
	Raytheon	74LS85	
	TI	SN74LS85	
74LS86	Fairchild	74LS86	
	Hitachi	HD74LS86	
	Motorola	SN74LS86	
	NEC America	μPB74LS86	
	Raytheon	74LS86	
	TI	SN74LS86	
74LS89	Motorola	SN74LS89	
74LS90	Fairchild	74LS90	
	Motorola	SN74LS90	
	Raytheon	74LS90	
	TI	SN74LS90	
74LS92	Fairchild	74LS92	
	Hitachi	HD74LS92	
	Motorola	SN74LS92	
	Raytheon	74LS92	
	TI	SN74LS92	
74LS93	Fairchild	74LS93	
	Motorola	SN74LS93	
	Raytheon	74LS93	
	TI	SN74LS93	
74LS95B	Fairchild	74LS95	
	Hitachi	HD74LS95B	
	Motorola	SN74LS95	
	Raytheon	74LS95B	
	TI	SN74LS95B	
74LS96	TI	SN74LS96	
74S00	Fairchild	74S00	
	Hitachi	HD74S00	
	Mitsubishi	M5S000	
	National	DM74S00	
	TI	SN74S00	
74S02	Fairchild	74S02	
	National	DM74S02	
	TI	SN74S32	
74S03	Fairchild	74S03	
	Hitachi	HD74S03	
	Mitsubishi	M5S003	
	National	DM74S03	
	TI	SN74S03	
74S04	Fairchild	74S04	
	Hitachi	HD74S04	
	Mitsubishi	M5S004	
	National	DM74S04	
	TI	SN74S04	
74S05	Fairchild	74S05	
	Hitachi	HD74S05	
	Mitsubishi	M5S005	
	National	DM74S05	
	TI	SN74S05	
74S08	Fairchild	74S08	
	TI	SN74S08	
74S09	Fairchild	74S09	
	Signetics	74S09	
	TI	SN74S09	
74S10	Fairchild	74S10	
	Hitachi	HD74S10	
	Mitsubishi	M5S010	
	National	DM74S10	
	TI	SN74S10	
74S11	Fairchild	74S11	
	Hitachi	HD74S11	
	Mitsubishi	M5S011	
	National	DM74S11	
	TI	SN74S11	
74S112	Fairchild	74S112	
	Hitachi	HD74S112	
	Mitsubishi	M5S112	
	Motorola	SN74S112	
	National	DM74S112	
	TI	SN74S112	
74S113	Fairchild	74S113	
	Hitachi	HD74S113	
	Mitsubishi	M5S113	
	Motorola	SN74S113	
	National	DM74S113	
	TI	SN74S113	
74S114	Fairchild	74S114	
	Hitachi	HD74S114	
	Mitsubishi	M5S114	
	National	DM74S114	
	TI	SN74S114	
74S133	Fairchild	74S133	
	Hitachi	HD74S133	
	Mitsubishi	M5S133	
	National	DM74S133	
	TI	SN74S133	
74S134	Fairchild	74S134	
	Hitachi	HD74S134	
	National	DM74S134	
	TI	SN74S134	
74S135	Fairchild	74S135	
	Hitachi	HD74S135	
	National	DM74S135	
	TI	SN74S135	
74S138	AMD	SN74S138	
	Fairchild	74S138	
	Mitsubishi	M5S138	
	National	DM74S138	
	TI	SN74S138	
74S139	AMD	SN74S139	
	Fairchild	74S139	
	National	DM74S139	
	TI	SN74S139	
74S140	Fairchild	74S140	
	Hitachi	HD74S140	
	National	DM74S140	
	TI	SN74S140	
74S15	Fairchild	74S15	
	Hitachi	HD74S15	
	Mitsubishi	M5S015	
	National	DM74S15	
	TI	SN74S15	
74S151	AMD	SN74S151	
	Fairchild	74S151	
	Hitachi	HD74S151	
	Mitsubishi	M5S151	
	National	DM74S151	
	TI	SN74S151	
74S153	AMD	SN74S153	
	Fairchild	74S153	
	Mitsubishi	M5S153	
	National	DM74S153	
	TI	SN74S153	
74S157	AMD	SN74S157	
	Fairchild	74S157	
	Mitsubishi	M5S157	
	National	DM74S157	
	TI	SN74S157	
74S158	AMD	SN74S158	
	Fairchild	74S158	
	Mitsubishi	M5S158	
	National	DM74S158	
	TI	SN74S158	
74S174	AMD	SN74S174	
	Fairchild	74S174	
	Hitachi	HD74S174	
	Mitsubishi	M5S174	
74S174	National	DM74S174	
	TI	SN74S174	
74S175	AMD	SN74S175	
	Fairchild	74S175	
	Hitachi	HD74S175	
	Mitsubishi	M5S175	
	National	DM74S175	
	TI	SN74S175	
74S181	AMD	SN74S181	
	Fairchild	93S141	
		93S41	
	Hitachi	HD74S181	
	Mitsubishi	M5S181	
	TI	SN74S181	
74S182	Fairchild	93S42	
	Hitachi	HD74S182	
	Mitsubishi	M5S182	
	National	DM74S182	
	TI	SN74S182	
74S194	AMD	SN74S194	
	Fairchild	74S194	
	TI	SN74S194	
74S195	AMD	SN74S195	
	Fairchild	93S00	
♦74S195	TI	SN74S195	
74S196	TI	SN74S196	
74S197	TI	SN74S197	
74S20	Fairchild	74S20	
	Hitachi	HD74S20	
	Mitsubishi	M5S020	
	National	DM74S20	
	TI	SN74S20	
74S200	National	DM74S200	
	NEC Micro	μPB2206	
	TI	SN74S200A	
		SN74S201	
74S201	MMI	6531	
	TI	SN74S201	
74S22	Fairchild	74S22	
	Hitachi	HD74S22	
	Mitsubishi	M5S22	
	National	DM74S22	
	TI	SN74S22	
74S251	AMD	SN74S251	
	Fairchild	74S251	
	Hitachi	HD74S251	
	Mitsubishi	M5S251	
	National	DM74S251	
	TI	SN74S251	
74S253	AMD	SN74S253	
	Fairchild	74S253	
	National	DM74S253	
74S257	AMD	SN74S257	
	Fairchild	74S257	
	Mitsubishi	M5S257	
	National	DM74S257	
	TI	SN74S257	
74S258	AMD	SN74S258	
	Fairchild	74S258	
	Mitsubishi	M5S258	
	TI	SN74S258	
74S280	Fairchild	74S280	
	National	DM74S280	
	TI	SN74S280	
74S301	Raytheon	RC5330	
	TI	SN74S300	
		SN74S301	
74S32	Fairchild	74S32	
74S37	TI	SN74S37	
74S40	Fairchild	74S40	
	Hitachi	HD74S40	
	Mitsubishi	M5S040	
	National	DM74S40	
	TI	SN74S40	
74S51	Fairchild	74S51	
	Mitsubishi	M5S051	
	National	DM74S51	
	TI	SN74S51	
74S64	Fairchild	74S64	
	Hitachi	HD74S64	
	National	DM74S64	
	TI	SN74S64	
74S65	Fairchild	74S65	
	Hitachi	HD74S65	
	National	DM74S65	
	TI	SN74S65	
74S85	Mitsubishi	M5S085	
	TI	SN74S85	
74S86	Fairchild	74S86	
	Hitachi	HD74S86	
	National	DM74S86	
	TI	SN74S86	
74S89	Fairchild	74S289	
7400	Fairchild	7400	
	Hitachi	HD7400	
	Mitsubishi	M53200	
	Motorola	MC7400	
	National	DM7400	
	NEC America	μPB7400	
	TI	SN7400	
	Toshiba	TC7400	
	TRW	7400	
7401	Fairchild	7401	
	Hitachi	HD7401	
	Mitsubishi	M53201	
	Motorola	MC7401	
	National	DM7401	
	TI	SN7401	
	TRW	7401	
7402	Fairchild	7402	
	Hitachi	HD7402	
	Mitsubishi	M53202	
	Motorola	MC7402	
	National	DM7402	
	NEC America	μPB7402	
	TI	SN7402	
	TRW	7402	
7403	Fairchild	7403	
	Hitachi	HD7403	
	Mitsubishi	M53203	
	Motorola	MC7403	
	National	DM7403	
	TI	SN7403	
	TRW	7403	
7404	Fairchild	7404	
	Hitachi	HD7404	
	Mitsubishi	M53204	
	Motorola	MC7404	
	National	DM7404	
	NEC America	μPB7404	
	TI	SN7404	
	Toshiba	TC7404	
	TRW	7404	
7405	Fairchild	7405	
	Hitachi	HD7405	
	Mitsubishi	M53205	
	Motorola	MC7405	
	National	DM7405	
	NEC America	μPB7405	
	TI	SN7405	
	TRW	7405	
7406	Fairchild	7406	
	Hitachi	HD7406	
	Mitsubishi	M53206	
	Motorola	MC7406	
	National	DM7406	
	TI	SN7406	
	TRW	7406	
7407	Fairchild	7407	
	Hitachi	HD7407	
	Mitsubishi	M53207	
	Motorola	MC7407	
	National	DM7407	
	TI	SN7407	
	TRW	7407	
7408	Fairchild	7408	
	Hitachi	HD7408	
	Mitsubishi	M53208	
	Motorola	MC7408	
	National	DM7408	
	TI	SN7408	
	Toshiba	TC7408	
	TRW	7408	
7409	Fairchild	7409	
	Hitachi	HD7409	
	Mitsubishi	M53209	
	Motorola	MC7409	
	National	DM7409	
	TI	SN7409	
	TRW	7409	
7410	Fairchild	7410	
	Hitachi	HD7410	

♦ Discontinued

Bold face device numbers indicate manufacturers data is provided in the IC Master on the pages noted.

Signetics (cont'd)

Manufacturer Device	Replacement Source	Device	IC Master Page
7410	Mitsubishi	M53210	
	Motorola	MC7410	
	National	DM7410	
	NEC America	μPB7410	
	TI	SN7410	
		SN7427	
	Toshiba	TC7410	
	TRW	7410	
74100	Motorola	MC74100	
	TI	SN74100	
74107	Fairchild	74107	
	Hitachi	HD74107	
	Mitsubishi	M53307	
	Motorola	MC74107	
	National	DM74107	
	NEC America	μPB74107	
	TI	SN74107	
74109	Fairchild	9024	
	National	DM74109	
	TI	SN74109	
7411	Fairchild	7411	
	Hitachi	HD7411	
	National	DM7411	
74116	Fairchild	74116	
	TI	SN74116	
7412	Fairchild	7412	
	Hitachi	HD7412	
	TI	SN7412	
	TRW	7412	
74121	Fairchild	74121	
	Hitachi	HD74121	
	Mitsubishi	M53321	
	Motorola	MC74121	
	National	DM74121	
	TI	SN74121	
	TRW	74121	
74122	Fairchild	74122	
	Mitsubishi	M53322	
	Motorola	MC74122	
	TI	SN74122	
74123	AMD	SN74123	
	Fairchild	74123	
	Mitsubishi	M53323	
	Motorola	MC74123	
	National	DM74123	
	NEC America	μPB74123	
	TI	SN74123	
	TRW	74123	
74125	Fairchild	74125	
	Hitachi	HD74125	
	Mitsubishi	M53325	
	National	DM74125	
	TI	SN74125	
74126	Fairchild	74126	
	Hitachi	HD74126	
	Mitsubishi	M53326	
	National	DM74126	
	TI	SN74126	
74128	TI	SN74128	
7413	Fairchild	7413	
	Mitsubishi	M53213	
	Motorola	MC7413	
	National	DM7413	
	NEC America	μPB7413	
	TI	SN7413	
	TRW	7413	
74132	Fairchild	74132	
	Hitachi	HD74132	
	Mitsubishi	M53332	
	Motorola	MC74132	
	National	DM74132	
	TI	SN74132	
7414	Fairchild	7414	
	Hitachi	HD7414	
	Mitsubishi	M53214	
	Motorola	MC7414	
	National	DM7414	
	TI	SN7414	
74145	Fairchild	74145	
	Mitsubishi	M53345	
	Motorola	MC74145	
	National	DM74145	
	TI	SN74145	
74145	TRW	74145	
74147	Hitachi	HD74147	
	Mitsubishi	M53347	
	National	DM74147	
	NEC America	μPB74147	
	TI	SN74147	
74148	Fairchild	9318	
	Hitachi	HD74148	
	Mitsubishi	M53348	
	National	DM74148	
	NEC America	μPB74148	
	TI	SN74148	
74150	Fairchild	74150	
	Hitachi	HD74150	
	Mitsubishi	M53350	
	Motorola	MC74150	
	National	DM74150	
	NEC America	μPB74150	
	TI	SN74150	
	TRW	74150	
74151	Fairchild	74151	
	Hitachi	HD74151	
	Mitsubishi	M53351	
	Motorola	MC74151	
	National	DM74151	
	NEC America	μPB74151	
	TI	SN74151	
	TRW	74151	
74153	Fairchild	74153	
	Mitsubishi	M53353	
	Motorola	MC74153	
	National	DM74153	
	NEC America	μPB74153	
	TI	SN74153	
	TRW	74153	
74154	AMD	SN74154	
	Fairchild	74154	
	Mitsubishi	M53354	
	Motorola	MC74154	
	National	DM74154	
	NEC America	μPB74154	
	TI	SN74154	
	TRW	74154	
74155	Fairchild	74155	
	Mitsubishi	M53355	
	Motorola	MC74155	
	National	DM74155	
	NEC America	μPB74155	
	TI	SN74155	
	TRW	74155	
74156	Fairchild	74156	
	Hitachi	HD74156	
	Mitsubishi	M53356	
	Motorola	MC74156	
	National	DM74156	
	NEC America	μPB74156	
	TI	SN74156	
	TRW	74156	
74157	AMD	SN74157	
	Fairchild	74157	
	Hitachi	HD74157	
	Mitsubishi	M53357	
	Motorola	MC74157	
	National	DM74157	
	NEC America	μPB74157	
	TI	SN74157	
74158	Mitsubishi	M53358	
7416	Fairchild	7416	
	Hitachi	HD7416	
	Mitsubishi	M53216	
	Motorola	MC7416	
	National	DM7416	
	TI	SN7416	
	TRW	7416	
74160	AMD	SN74160	
	Fairchild	74160	
	Hitachi	HD74160	
	Mitsubishi	M53360	
	Motorola	MC74160	
	National	DM74160	
	TI	SN74160	
	TRW	74160	
74161	AMD	SN74161	
	Fairchild	74161	
	Hitachi	HD74161	
	Mitsubishi	M53361	
74161	Motorola	MC74161	
	National	DM74161	
	NEC America	μPB74161	
	TI	SN74161	
	TRW	74161	
74162	AMD	SN74162	
	Fairchild	74162	
	Hitachi	HD74162	
	Mitsubishi	M53362	
	Motorola	MC74162	
	National	DM74162	
	TI	SN74162	
	TRW	74162	
74163	AMD	SN74163	
	Fairchild	74163	
	Hitachi	HD74163	
	Mitsubishi	M53363	
	Motorola	MC74163	
	National	DM74163	
	TI	SN74163	
	TRW	74163	
74164	AMD	74164	
	Fairchild	74164	
	Hitachi	HD74164	
	Mitsubishi	M53364	
	National	DM74164	
	NEC America	μPB74164	
	TI	SN74164	
74165	Fairchild	74165	
	Mitsubishi	M53365	
	Motorola	MC74165	
	National	DM74165	
	TI	SN74165	
74166	Fairchild	74166	
	Hitachi	HD74166	
	Mitsubishi	M53366	
	National	DM74166	
	TI	SN74166	
7417	Fairchild	7417	
	Hitachi	HD7417	
	Mitsubishi	M53217	
	Motorola	MC7417	
	National	DM7417	
	TI	SN7417	
	TRW	7417	
74170	Fairchild	74170	
	Mitsubishi	M53370	
	National	DM74170	
	NEC America	μPB74170	
	TI	SN74170	
74172	TI	SN74172	
74174	AMD	SN74174	
	Fairchild	74174	
	Hitachi	HD74174	
	Mitsubishi	M53374	
	Motorola	MC74174	
	National	DM74174	
	TI	SN74174	
74175	AMD	SN74175	
	Fairchild	74175	
	Hitachi	HD74175	
	Mitsubishi	M53375	
	Motorola	MC74175	
	National	DM74175	
	NEC America	μPB74175	
	TI	SN74175	
74176	Fairchild	74176	
	Mitsubishi	M53376	
	Motorola	MC74176	
	National	DM74176	
	TI	SN74176	
74177	Fairchild	74177	
	Mitsubishi	M53377	
	Motorola	MC74177	
	National	DM74177	
	TI	SN74177	
74180	Fairchild	74180	
	Hitachi	HD74180	
	Mitsubishi	M53380	
	Motorola	MC74180	
	National	DM74180	
	NEC America	μPB74180	
	TI	SN74180	
	TRW	74180	
74181	AMD	SN74181	
	Fairchild	74181	
74181	Mitsubishi	M53381	
	Motorola	MC74181	
	National	DM74181	
	NEC America	μPB74181	
	TI	SN74181	
74182	AMD	SN74182	
	Fairchild	74182	
	Mitsubishi	M53382	
	Motorola	MC74182	
	National	DM74182	
	NEC America	μPB74182	
	TI	SN74182	
74190	Fairchild	74190	
	Hitachi	HD74190	
	Mitsubishi	M53390	
	Motorola	MC74190	
	National	DM74190	
	TI	SN74190	
74191	Fairchild	74191	
	Hitachi	HD74191	
	Mitsubishi	M53391	
	Motorola	MC74191	
	National	DM74191	
	TI	SN74191	
74192	AMD	SN74192	
	Fairchild	74192	
	Mitsubishi	M53392	
	Motorola	MC74192	
	National	DM74192	
	NEC America	μPB74192	
	TI	SN74192	
74193	AMD	SN74193	
	Fairchild	74193	
	Mitsubishi	M53393	
	Motorola	MC74193	
	National	DM74193	
	NEC America	μPB74193	
	TI	SN74193	
74194	AMD	SN74194	
	Fairchild	74194	
	Hitachi	HD74194	
	Motorola	MC74194	
	National	DM74194	
	TI	SN74194	
74195	AMD	SN74195	
	Fairchild	74195	
	Motorola	MC74195	
	National	DM74195	
	NEC America	μPB74195	
	TI	SN74195	
74196	Fairchild	74196	
	Motorola	MC74196	
	National	DM74196	
	TI	SN74196	
74197	Fairchild	74197	
	Motorola	MC74197	
	National	DM74197	
	TI	SN74197	
74198	Fairchild	74198	
	Hitachi	HD74198	
	Mitsubishi	M53398	
	National	DM74198	
	NEC America	μPB74198	
	TI	SN74198	
74199	Fairchild	74199	
	Mitsubishi	M53399	
	National	DM74199	
	TI	SN74199	
7420	Fairchild	7420	
	Hitachi	HD7420	
	Mitsubishi	M53220	
	Motorola	MC7420	
	National	DM7420	
	NEC America	μPB7420	
	TI	SN7420	
	Toshiba	TC7420	
	TRW	7420	
74200	Raytheon	RC5340	
7421	Fairchild	7421	
74221	TI	SN74221	
7426	Fairchild	7426	
	Hitachi	HD7426	
	Motorola	MC7426	
	National	DM7426	
	TI	SN7426	
	TRW	7426	

◆ Discontinued

The manufacturers report their devices can be used as direct replacements.
Performance details often differ, so compare the specifications considering your requirements.

Signetics (cont'd)

Manufacturer Device	Replacement Source	Device	IC Master Page
7427	Fairchild	7427	
	Hitachi	HD7427	
	Mitsubishi	M53227	
	Motorola	MC7427	
	National	DM7427	
74279	Fairchild	74279	
	TI	SN74279	
7428	TI	SN7428	
74298	Fairchild	74298	
	Motorola	MC74298	
	TI	SN74298	
7430	Fairchild	7430	
	Hitachi	HD7430	
	Mitsubishi	M53230	
	Motorola	MC7430	
	National	DM7430	
	NEC America	μPB7430	
	TI	SN7430	
	TRW	7430	
7432	Fairchild	7432	
	Hitachi	HD7432	
	National	DM7432	
	TI	SN7432	
7433	TI	SN7433	
7437	Fairchild	7437	
	Mitsubishi	M53237	
	Motorola	MC7437	
	National	DM7437	
	NEC America	μPB7437	
	TI	SN7437	
	TRW	7437	
7438	Fairchild	7438	
	Mitsubishi	M53238	
	Motorola	MC7438	
	National	DM7438	
	NEC America	μPB7438	
	TI	SN7438	
	TRW	7438	
7439	Fairchild	7439	
7440	Fairchild	7440	
	Hitachi	HD7440	
	Mitsubishi	M53240	
	Motorola	MC7440	
	National	DM7440	
	NEC America	μPB7440	
	TI	SN7440	
	TRW	7440	
♦7441	Hitachi	HD7441	
	TI	SN74141	
7442	Fairchild	7442	
	Hitachi	HD7442	
	Mitsubishi	M53242	
	Motorola	MC7442	
	National	DM7442	
	NEC America	μPB7442	
	TI	SN7442	
7443	Fairchild	7443	
	Hitachi	HD7443	
	Mitsubishi	M53243	
	Motorola	MC7443	
	TI	SN7443	
7444	Fairchild	7444	
	Hitachi	HD7444	
	Mitsubishi	M53244	
	Motorola	MC7444	
	TI	SN7444	
7445	Fairchild	7445	
	Mitsubishi	M53245	
	Motorola	MC7445	
	National	DM7445	
	NEC America	μPB7445	
	TI	SN7445	
	TRW	7445	
7446	Fairchild	7446	
	Motorola	MC7446	
	National	DM7446	
	TI	SN7446	
7447	Fairchild	7447	
	Mitsubishi	M53247	
	Motorola	MC7447	
	National	DM7447	
	NEC America	μPB7447	
	TI	SN7447	
7448	Fairchild	7448	
	Mitsubishi	M53248	
	Motorola	MC7448	
	National	DM7448	
	TI	SN7448	
7450	Fairchild	7450	
	Hitachi	HD7450	
	Mitsubishi	M53250	
	Motorola	MC7450	
	National	DM7450	
	NEC America	μPB7450	
	TI	SN7450	
	TRW	7450	
7451	Fairchild	7451	
	Hitachi	HD7451	
	Motorola	MC7451	
	National	DM7451	
	NEC America	μPB7451	
	TI	SN7451	
	TRW	7451	
7453	Fairchild	7453	
	Hitachi	HD7453	
	Mitsubishi	M53253	
	Motorola	MC7453	
	National	DM7453	
	NEC America	μPB7453	
	TI	SN7453	
	TRW	7453	
7454	Fairchild	7454	
	Hitachi	HD2514	
	Motorola	MC7454	
	National	DM7454	
	NEC America	μPB7454	
	TI	SN7454	
	TRW	7454	
7460	Fairchild	7460	
	Hitachi	HD7460	
	Mitsubishi	M53260	
	Motorola	MC7460	
	National	DM7460	
	NEC America	μPB7460	
	TI	SN7460	
	TRW	7460	
7470	Fairchild	7470	
	Hitachi	HD7470	
	Mitsubishi	M53270	
	Motorola	MC7470	
	National	DM7470	
	TI	SN7470	
7472	Fairchild	7472	
	Hitachi	HD7472	
	Mitsubishi	M53272	
	Motorola	MC7472	
	National	DM7472	
	TI	SN7472	
	TRW	7472	
7473	Fairchild	7473	
	Hitachi	HD7473	
	Mitsubishi	M53273	
	Motorola	MC7473	
	National	DM7473	
	NEC America	μPB7473	
	TI	SN7473	
7474	Fairchild	7474	
	Hitachi	HD7474	
	Mitsubishi	M53274	
	Motorola	MC7474	
	National	DM7474	
	NEC America	μPB7474	
	TI	SN7474	
	TRW	7474	
7475	Fairchild	7475	
	Hitachi	HD7475	
	Mitsubishi	M53275	
	Motorola	MC7475	
	National	DM7475	
	TI	SN7475	
	TRW	7475	
7476	Fairchild	7476	
	Hitachi	HD7476	
	Mitsubishi	M53276	
	Motorola	MC7476	
	National	DM7476	
	NEC America	μPB7476	
	TI	SN7476	
	TRW	7476	
7477	Fairchild	7477	
	Motorola	MC7477	
	TI	SN7477	
7480	Fairchild	7480	
	Mitsubishi	M53280	
	Motorola	MC7480	
	NEC America	μPB7480	
	TI	SN7480	
7483	Fairchild	7483	
	Mitsubishi	M53283	
	Motorola	MC7483	
	National	DM7483	
	TI	SN7483	
7485	Fairchild	7485	
	Hitachi	HD7485	
	Mitsubishi	M53285	
	Motorola	MC7485	
	National	DM7485	
	NEC America	μPB7485	
	TI	SN7485	
	TRW	7485	
7486	Fairchild	7486	
	Hitachi	HD7486	
	Mitsubishi	M53286	
	Motorola	MC7486	
	National	DM7486	
	NEC America	μPB7486	
	TI	SN7486	
	TRW	7486	
7488	TI	SN7488A	
7489	Hitachi	HD7489	
	TI	SN7489	
7490	Fairchild	7490	
	Hitachi	HD7490	
	Mitsubishi	M53290	
	Motorola	MC7490	
	National	DM7490	
	TI	SN7490	
		SN7490A	
	TRW	7490	
7491	Fairchild	7491	
	Hitachi	HD7491	
	Mitsubishi	M53291	
	Motorola	MC7491	
	National	DM7491	
	NEC America	μPB7491	
	TI	SN7491	
		SN7491A	
7492	Fairchild	7492	
	Hitachi	HD7492	
	Mitsubishi	M53292	
	Motorola	MC7492	
	National	DM7492	
	TI	SN7492	
		SN7492A	
	TRW	7492	
7493	Fairchild	7493	
	Hitachi	HD7493	
	Mitsubishi	M53293	
	Motorola	MC7493	
	National	DM7493	
	TI	SN7493	
		SN7493A	
	TRW	7493	
7494	Fairchild	7494	
	Hitachi	HD7494	
	TI	SN7494	
7495	Fairchild	7495	
	Hitachi	HD7495	
	Mitsubishi	M53295	
	Motorola	MC7495	
	National	DM7495	
	TI	SN7495	
		SN7495A	
7496	Fairchild	7496	
	Hitachi	HD7496	
	Mitsubishi	M53296	
	Motorola	MC7496	
	National	DM7496	
	TI	SN7496	
	TRW	7496	
75S107	TI	SN75S107	
75S108	TI	SN75S108	
75107	AMD	SN75107	
	National	DS75107	
	Raytheon	RC75107	
75107	TI	SN75107	
75108	AMD	SN75108	
	National	DS75108	
	Raytheon	RC75108	
	TI	SN75108	
7520	AMD	SN7520	
	Motorola	MC7520	
	National	DS7520	
	Silicon G	SG7520	
	TI	SN7520	
♦7521	Motorola	MC7521	
	Silicon G	SG7521	
	TI	SN7520	
7522	Motorola	MC7522	
	National	DS7522	
	Silicon G	SG7522	
	TI	SN7522	
♦7523	Motorola	MC7523	
	Silicon G	SG7523	
	TI	SN7522	
75232	TI	SN75232	
75234	TI	SN75234	
7524	AMD	SN7524	
	Fairchild	75S24	
	Motorola	MC7524	
	National	DS7524	
	Silicon G	SG7524	
	TI	SN7524	
♦7525	AMD	SN7525	
	Motorola	MC7525	
		SN7525	
	Silicon G	SG7525	
	TI	SN7524	
7528	TI	SN7528	
75324	TI	SN75324	
75325	TI	SN75325	
75361	TI	SN75361	
75450	Fairchild	75450	
	National	DS75450	
	Raytheon	RC75450	
	Silicon G	SG75450	
	TI	SN75450	
75451	Fairchild	75451	
	National	DS75451	
	Raytheon	RC75451	
	Silicon G	SG75451	
	TI	SN75451	
75452	TI	SN75452	
75453	TI	SN75453	
75454	TI	SN75454	
7550	Hitachi	HD2506	
8080A	National	8080A	
82S10	**AMI**	**S4015**	**1203**
82S123	Intersil	IM5610	
93425	**AMI**	**S4025**	**1203**

Silicon General

Manufacturer Device	Replacement Source	Device	IC Master Page
SG101	AMD	LM101	
	Intersil	LM101	
	Motorola	LM101	
	National	**LM101**	**1035**
	RCA	CA101	
		CA748	
	Signetics	LM101	
	TI	LM101	
SG102	Motorola	LM110	
SG104	Motorola	LM104	
	TI	LM104	
SG105	AMD	LM105	
	Intersil	LM105	
	Motorola	LM105	
	National	LM105	
	Raytheon	LM105	
	TI	LM105	
SG107	AMD	LM107	
	Intersil	LM107	
	Motorola	LM107	
	National	LM107	
	Raytheon	LM107	
	RCA	CA107	
	Signetics	LM107	
	TI	LM107	
SG108	AMD	LM108	
	Intersil	LM108	

♦ Discontinued

Bold face device numbers indicate manufacturers data is provided in the IC Master on the pages noted.

Silicon General (cont'd)

Manufacturer Device	Replacement Source	Device	IC Master Page
SG108	Motorola	LM108	
	National	**LM108**	**1035**
	Raytheon	LM108	
	RCA	CA108	
	Signetics	LM108	
SG109	Motorola	LM109	
	National	LM109	
	Raytheon	LM109	
	Signetics	LM109	
	TI	LM109	
SG110	AMD	LM110	
	Intersil	LM110	
	Motorola	LM110	
	National	LM110	
SG111	AMD	LM111	
	Intersil	LM111	
	Motorola	LM111	
	National	LM111	
	Raytheon	LM111	
	RCA	CA111	
	TI	LM111	
SG124	Motorola	LM124	
	Signetics	LM124	
SG139	Motorola	MLM139	
	Signetics	LM139	
SG139A	PMI	CMP-04	
		PM139A	
SG1403	Motorola	MC1403	
SG1436	Motorola	MC1436	
SG1456	Motorola	MC1456	
	Signetics	MC1456	
	TI	MC1456	
SG1458	Exar	XR1458	
	Harris	**HA-2655**	**986**
	Motorola	MC1458	
	PMI	SSS1458	
	Raytheon	RC1458	
	RCA	CA1458	
	Signetics	MC1458	
	TI	MC1458	
SG1468	Motorola	MC1468	
SG1488	AMD	MC1488	
	Exar	XR1488	
	National	DS1488	
	Raytheon	RC1488	
	Signetics	MC1488	
SG1489	AMD	MC1489	
	Exar	XR1489	
	National	DS1489	
	Raytheon	RC1489	
	Signetics	MC1489	
SG1489A	Exar	XR1489	
	Signetics	MC1489A	
SG1495	Motorola	MC1495	
SG1496	Motorola	MC1496	
	Signetics	MC1496	
SG1501A	Motorola	MC1568	
SG1524	**Exar**	**XR1524**	**930**
	Signetics	SG1524	
	TI	SG1524	
SG1536	Motorola	MC1536	
SG1543	Exar	XR1543	
SG1556	Motorola	MC1556	
	TI	MC1556	
SG1558	Exar	XR1558	
	Harris	**HA-2650**	**986**
	Motorola	MC1558	
	PMI	SSS1558	
	Raytheon	RM1558	
	RCA	CA1558	
	Signetics	MC1558	
	TI	MC1558	
SG1595	Motorola	MC1595	
SG1596	Motorola	MC1596	
	Signetics	MC1496	
♦SG1741S	Motorola	SG1741S	
SG2001	**Exar**	**XR2201**	**931**
	Fairchild	9665	
	SGS	L201	
	Signetics	NE5501	
		ULN2001	
	Sprague	ULN-2001	
	TI	ULN2001	
SG2002	**Exar**	**XR2202**	**931**
	Fairchild	9666	
	SGS	L202	
	Signetics	NE5502	
		ULN2002	
	Sprague	ULN-2002	
	TI	ULN2002	
SG2003	**Exar**	**XR2203**	**931**
	Fairchild	9667	
	SGS	L203	
	Signetics	NE5503	
		ULN2003	
	Sprague	ULN-2003	
	TI	ULN2003	
SG201	AMD	LM201	
	Intersil	LM201	
	Motorola	LM201	
	National	LM201	
	RCA	CA201	
	Signetics	LM201	
	TI	LM201	
SG202	Motorola	LM210	
SG204	Motorola	LM204	
SG205	AMD	LM205	
	Intersil	LM205	
	Motorola	LM205	
	National	LM205	
	Raytheon	LM205	
SG207	AMD	LM207	
	Intersil	LM207	
	Motorola	LM207	
	National	LM207	
	Raytheon	LM207	
	RCA	CA207	
	Signetics	LM207	
	TI	LM207	
SG208	AMD	LM208	
	Intersil	LM208	
	Motorola	LM208	
	National	LM208	
	Raytheon	LM208	
	RCA	CA208	
	Signetics	LM208	
SG209	Motorola	LM209	
	National	LM209	
	Signetics	LM209	
	TI	SG209	
SG210	AMD	LM210	
	Intersil	LM210	
	Motorola	LM210	
	National	LM210	
SG211	AMD	LM211	
	Intersil	LM211	
	Motorola	LM211	
	National	LM211	
	Raytheon	LM211	
	RCA	CA211	
	Signetics	LM211	
	TI	LM211	
♦SG2206	**Exar**	**XR2206**	**924**
SG224	Motorola	LM224	
	Signetics	LM224	
SG239	RCA	CA239	
	Signetics	LM239	
SG239A	PMI	CMP-04	
		PM239A	
SG2501A	Motorola	MC1468	
SG2524	**Exar**	**XR2524**	**930**
	Signetics	SG2524	
	TI	SG2524	
SG2543	Exar	XR2543	
SG301	AMD	LM301	
	Motorola	LM301	
	National	LM301	
	Raytheon	LM301	
	RCA	CA301	
	Signetics	LM301	
	TI	LM301	
SG302	Motorola	LM310	
SG304	Motorola	LM304	
	Raytheon	LM304	
	TI	LM304	
SG305	AMD	LM305	
	Motorola	LM305	
	National	LM305	
	Raytheon	LM305	
SG305	TI	LM305	
SG3058	RCA	CA3058	
SG3059	RCA	CA3059	
SG307	AMD	LM307	
	Motorola	LM307	
	National	LM307	
	Raytheon	LM307	
	RCA	CA307	
	Signetics	LM307	
	TI	LM307	
SG3079	RCA	CA3079	
SG308	AMD	LM308	
	Motorola	LM308	
	National	LM308	
	Raytheon	LM308	
	RCA	CA308	
	Signetics	LM308	
SG3081	RCA	CA3081	
	Signetics	CA3081	
SG3082	RCA	CA3082	
	Signetics	CA3082	
SG3083	RCA	CA3083	
	Signetics	CA3083	
SG3086	Motorola	MC3386	
SG309	Motorola	LM309	
	National	LM309	
	Raytheon	LM309	
	Signetics	LM309	
	TI	LM309	
SG310	Motorola	LM310	
	National	LM310	
SG311	AMD	LM311	
	Motorola	LM311	
	National	LM311	
	Raytheon	LM311	
	RCA	CA311	
	Signetics	LM311	
	TI	LM311	
SG3183	Signetics	CA3183	
SG324	Motorola	LM324	
	RCA	CA324	
	Signetics	LM324	
SG339	Motorola	LM339	
	RCA	CA339	
	Signetics	LM339	
SG339A	PMI	CMP-04	
		PM339A	
SG340-12	Motorola	MC7812	
	Signetics	μA7812	
SG340-15	Motorola	MC7815	
	Signetics	μA7815	
SG340-18	Motorola	MC7818	
	Signetics	μA7818	
SG340-24	Motorola	MC7824	
	Signetics	μA7824	
SG340-5	Motorola	MC7805	
	Signetics	μA7805	
SG340-6	Motorola	MC7806	
	Signetics	μA7806	
SG340-8	Motorola	MC7808	
	Signetics	μA7808	
SG3501	Raytheon	RC555	
		RM555	
	RCA	CA555	
SG3501A	Motorola	MC1468	
SG3524	**Exar**	**XR3524**	**930**
	Signetics	SG3524	
	TI	SG3524	
SG3543	Exar	XR3543	
SG3821	Sprague	ULS-2045	
SG3851	Signetics	NE5501	
SG3852	Signetics	NE5502	
SG3853	Signetics	NE5503	
SG3886	Sprague	ULN-2086	
SG4250	National	LM4250	
SG4501	Motorola	MC1468	
SG555	Cherry	CS555	
	Exar	XR555	
	Motorola	MC1455	
		MC1555	
	RCA	CA555	
	Signetics	NE555	
		SE555	
	TI	NE555	
		SE555	
SG556	Exar	XR556	
SG556	Motorola	MC3456	
		MC3556	
	Signetics	NE556	
		SE556	
SG710	Motorola	MC1710	
	National	LM710	
	Raytheon	RC710	
		RM710	
	Signetics	μA710	
	TI	μA710	
SG711	Motorola	MC1711	
	National	LM711	
	Raytheon	RC711	
		RM711	
	Signetics	μA711	
	TI	μA711	
SG723	AMD	723	
	Intersil	723	
	Motorola	MC1723	
	National	LM723	
	Raytheon	RC723	
		RM723	
	RCA	CA723	
	Signetics	μA723	
	TI	μA723	
SG733	AMD	733	
	Motorola	MC1733	
	Raytheon	RC733	
		RM733	
	Signetics	μA733	
	TI	μA733	
SG741	AMD	741	
	Motorola	MC1741	
	National	**LM741**	**1035**
	PMI	SSS741	
	Raytheon	RC741	
		RM741	
	RCA	CA741	
	Signetics	μA741	
	TI	μA741	
SG747	AMD	747	
	Motorola	MC1747	
	National	LM747	
	PMI	SSS747	
	Raytheon	RC747	
		RM747	
	RCA	CA747	
	Signetics	μA747	
	TI	μA747	
SG748	AMD	748	
	Motorola	MC1748	
	Raytheon	RC748	
		RM748	
	RCA	CA748	
	Signetics	μA748	
	TI	μA748	
SG7520	National	DS7520	
	Signetics	7520	
	TI	SN7520	
SG7522	Motorola	MC7522	
	National	DS7522	
	Signetics	7522	
	TI	SN7522	
SG7523	Motorola	MC7523	
SG7524	Motorola	MC7524	
	National	DS7524	
	Signetics	SN7524	
SG7525	Motorola	MC7525	
SG7528	Motorola	MC7528	
	TI	SN7528	
SG7529	Motorola	MC7529	
SG7805	Motorola	MC7805	
SG7806	Motorola	MC7806	
SG7808	Motorola	MC7808	
SG7812	Motorola	MC7812	
SG7815	Motorola	MC7815	
SG7818	Motorola	MC7818	
SG7824	Motorola	MC7824	
♦SN7524	TI	SN7524	

Siliconix

DF320	Nitron	NC320
DF321	Nitron	NC321
DF322	Nitron	NC322

♦ Discontinued

The manufacturers report their devices can be used as direct replacements.
Performance details often differ, so compare the specifications considering your requirements.

Siliconix (cont'd)

Manufacturer Device	Replacement Source	Device	IC Master Page
DF331	Nitron	NC331	
DF332	Nitron	NC332	
DF341	Nitron	NC341	
DF342	Nitron	NC342	
DG126	Intersil	DG126	
	National	AH0126	
DG129	Intersil	DG129	
	National	AH0129	
DG133	Intersil	DG133	
	National	**AH0133**	**1076**
DG134	Intersil	DG134	
	National	**AH0134**	**1076**
DG139	Intersil	DG139	
	National	AH0139	
DG140	Intersil	DG140	
	National	AH0140	
DG142	Intersil	DG142	
	National	AH0142	
DG143	Intersil	DG143	
	National	AH0143	
DG144	Intersil	DG144	
	National	AH0144	
DG145	Intersil	DG145	
	National	AH0145	
DG146	Intersil	DG146	
	National	AH0146	
DG151	**National**	**AH0151**	**1076**
DG153	Intersil	DG153	
	National	AH0153	
DG154	Intersil	DG154	
	National	AM0154	
DG163	Intersil	DG163	
	National	AM0163	
DG164	Intersil	DG164	
	National	AM0164	
DG180	Intersil	DG180	
DG181	Intersil	DG181	
	Siliconix	**DG381**	**825**
DG182	Intersil	DG182	
	TI	TL182	
DG183	Intersil	DG183	
DG184	Intersil	DG184	
	Siliconix	**DG384**	**825**
DG185	Intersil	DG185	
	TI	TL185	
DG186	Intersil	DG186	
DG187	Intersil	DG187	
	Siliconix	**DG387**	**825**
DG188	Intersil	DG188	
	TI	TL188	
DG189	Intersil	DG189	
DG190	Intersil	DG190	
	Siliconix	**DG390**	**825**
DG191	Intersil	DG191	
	TI	TL191	
DG200	AD	AD7513	
	Micro Power	MP7513	
DG506	AD	AD7506	
	Harris	HI506	
	Intersil	IH5060	
	Micro Power	MP7506	
DG507	AD	AD7507	
	Micro Power	MP7507	
DG509	Harris	HI509A	
LD110	Intersil	LD110	
LD111	Intersil	LD111	
	Motorola	MC1405	
LD114	Intersil	LD114	
LM101	Motorola	LM101	
	RCA	CA101	
	TI	LM101	

Solid State Scientific

CL4041	National	CD4041	
	RCA	CD4041	
	Solitron	CM4041	
	SSS	SCL4041	
SCL4000	Mitel	SIL4000	
	Motorola	MC14000	
	National	CD4000	
	RCA	CD4000	
SCL4000	Solitron	CM4000	
	TI	TP4000	
SCL4001	Fairchild	F4001	
	Mitel	SIL4001	
		SIL4901	
	Motorola	MC14001	
	National	CD4001	
	NEC America	μPD4001	
	RCA	CD4001	
	SGS	HBF4001	
	Solitron	CM4001	
	TI	TP4001	
	Toshiba	TC4001	
SCL4002	Fairchild	F4002	
	Mitel	SIL4002	
	Motorola	MC14002	
	National	CD4002	
	NEC America	μPD4002	
	RCA	CD4002	
	SGS	HBF4002	
	Solitron	CM4002	
	TI	TP4002	
	Toshiba	TC4002	
SCL4006	Fairchild	F4006	
	Motorola	MC14006	
	National	CD4006	
	NEC America	μPD4006	
	RCA	CD4006	
	Solitron	CM4006	
SCL4007	Fairchild	F4007	
	Mitel	SIL4007	
	Motorola	MC14007	
	National	CD4007	
	RCA	CD4007	
	SGS	HBF4007	
	Solitron	CM4007	
	TI	TP4007	
	Toshiba	TC4007	
SCL4008	Fairchild	F4008	
	Motorola	MC14008	
	National	CD4008	
	RCA	CD4008	
	SGS	HBF4008	
	Solitron	CM4008	
	TI	TP4008	
	Toshiba	TC4008	
SCL4009	Mitel	SIL4009	
	National	CD4009	
	RCA	CD4009	
	SGS	HBF4009	
	Solitron	CM4009	
	TI	TP4009	
	Toshiba	TC4009	
SCL4010	Mitel	SIL4010	
	National	CD4010	
	RCA	CD4010	
	SGS	HBF4010	
	Solitron	CM4010	
	TI	TP4010	
	Toshiba	TC4010	
SCL4011	Fairchild	F4011	
	Mitel	SIL4011	
		SIL4911	
	Motorola	MC14011	
	National	CD4011	
	NEC America	μPD4011	
	RCA	CD4011	
	SGS	HBF4011	
	Solitron	CM4011	
	TI	TP4011	
	Toshiba	TC4011	
SCL4012	Fairchild	F4012	
	Mitel	SIL4012	
		SIL4912	
	Motorola	MC14012	
	National	CD4012	
	NEC America	μPD4012	
	RCA	CD4012	
	SGS	HBF4012	
	Solitron	CM4012	
	TI	TP4012	
	Toshiba	TC4012	
SCL4013	Fairchild	F4013	
	Mitel	SIL4013	
	Motorola	MC14013	
	National	CD4013	
SCL4013	NEC America	μPD4013	
	RCA	CD4013	
	SGS	HBF4013	
	Solitron	CM4013	
	TI	TP4013	
	Toshiba	TC4013	
SCL4014	Fairchild	F4014	
	Mitel	SIL4014	
	Motorola	MC14014	
	National	CD4014	
	NEC America	μPD4014	
	RCA	CD4014	
	SGS	HBF4014	
	Solitron	CM4014	
	TI	TP4014	
	Toshiba	TC4014	
SCL4015	Fairchild	F4015	
	Mitel	SIL4015	
	Motorola	MC14015	
	National	CD4015	
	NEC America	μPD4015	
	RCA	CD4015	
	SGS	HBF4015	
	Solitron	CM4015	
	TI	TP4015	
	Toshiba	TC4015	
SCL4016	AD	AD7516	
	Fairchild	F4016	
	Micro Power	MPS7516	
	Mitel	SIL4016	
	Motorola	MC14016	
	National	**CD4016**	**1076**
	RCA	CD4016	
		CD4066	
	Solitron	CM4016	
	TI	TP4016	
SCL4017	Fairchild	F4017	
	Mitel	SIL4017	
	Motorola	MC14017	
	National	CD4017	
	NEC America	μPD4017	
	RCA	CD4017	
	SGS	HBF4017	
	Solitron	CM4017	
	TI	TP4017	
	Toshiba	TC4017	
SCL4018	Fairchild	F4018	
	Mitel	SIL4018	
	National	CD4018	
	RCA	CD4018	
	SGS	HBF4018	
	Solitron	CM4018	
	TI	TP4018	
	Toshiba	TC4018	
SCL4019	Fairchild	F4019	
	Mitel	SIL4019	
	National	CD4019	
	NEC America	μPD4019	
	RCA	CD4019	
	SGS	HBF4019	
	Solitron	CM4019	
	TI	TP4019	
	Toshiba	TC4019	
SCL4020	Fairchild	F4020	
	Mitel	SIL4020	
	Motorola	MC14020	
	National	CD4020	
	NEC America	μPD4020	
	RCA	CD4020	
	SGS	HBF4020	
	Solitron	CM4020	
	TI	TP4020	
	Toshiba	TC4020	
SCL4021	Fairchild	F4021	
	Mitel	SIL4021	
	Motorola	MC14021	
	National	CD4021	
	NEC America	μPD4021	
	RCA	CD4021	
	Solitron	CM4021	
	TI	TP4021	
	Toshiba	TC4021	
SCL4022	Fairchild	F4022	
	Mitel	SIL4022	
	Motorola	MC14022	
	National	CD4022	
SCL4022	RCA	CD4022	
	SGS	HBF4022	
	Solitron	CM4022	
	TI	TP4022	
	Toshiba	TC4022	
SCL4023	Fairchild	F4023	
	Mitel	SIL4023	
		SIL4923	
	Motorola	MC14023	
	National	CD4023	
	NEC America	μPD4023	
	RCA	CD4023	
	SGS	HBF4023	
	Solitron	CM4023	
	TI	TP4023	
	Toshiba	TC4023	
SCL4024	Fairchild	F4024	
	Mitel	SIL4024	
	Motorola	MC14024	
	National	CD4024	
	NEC America	μPD4024	
	RCA	CD4024	
	SGS	HBF4024	
	Solitron	CM4024	
	TI	TP4024	
	Toshiba	TC4024	
SCL4025	Fairchild	F4025	
	Mitel	SIL4025	
		SIL4925	
	Motorola	MC14025	
	National	CD4025	
	NEC America	μPD4025	
	RCA	CD4025	
	SGS	HBF4025	
	Solitron	CM4025	
	TI	TP4025	
	Toshiba	TC4025	
SCL4026	RCA	CD4026	
	Solitron	CM4026	
SCL4027	Fairchild	F4027	
	Mitel	SIL4027	
	Motorola	MC14027	
	National	CD4027	
	NEC America	μPD4027	
	RCA	CD4027	
	SGS	HBF4027	
	Solitron	CM4027	
	TI	TP4027	
	Toshiba	TC4027	
SCL4028	Fairchild	F4028	
	Mitel	SIL4028	
	Motorola	MC14028	
	National	CD4028	
	NEC America	μPD4028	
	RCA	CD4028	
	SGS	HBF4028	
	Solitron	CM4028	
	TI	TP4028	
	Toshiba	TC4028	
SCL4029	Fairchild	F4029	
	Mitel	SIL4029	
	National	CD4029	
	NEC America	μPD4029	
	RCA	CD4029	
	SGS	HBF4029	
	Solitron	CM4029	
	TI	TP4029	
	Toshiba	TC4029	
SCL4030	Fairchild	F4030	
	Mitel	SIL4030	
	Motorola	MC14507	
	National	CD4030	
		CD4070	
		CD4507	
		MM74C86	
	NEC America	μPD4030	
	RCA	CD4030	
		CD4070	
	SGS	HBF4030	
	Solitron	CM4030	
	TI	TP4030	
		TP4507	
	Toshiba	TC4030	
SCL4033	RCA	CD4033	
	SGS	HBF4033	
	Solitron	CM4033	

♦ Discontinued

Bold face device numbers indicate manufacturers data is provided in the IC Master on the pages noted.

Solid State Scientific (cont'd)

Manufacturer Device	Replacement Source	Device	IC Master Page
SCL4034	Fairchild	F4034	
	Motorola	MC14034	
	National	CD4034	
	NEC America	μPD4034	
	RCA	CD4034	
	Solitron	CM4034	
	Toshiba	TC4034	
SCL4035	Fairchild	F4035	
	Mitel	SIL4035	
	Motorola	MC14035	
	National	CD4035	
	NEC America	μPD4035	
	RCA	CD4035	
	SGS	HBF4035	
	Solitron	CM4035	
	TI	TP4035	
	Toshiba	TC4035	
SCL4040	Fairchild	F4040	
	Mitel	SIL4040	
	Motorola	MC14040	
	National	CD4040	
	NEC America	μPD4040	
	RCA	CD4040	
	Solitron	CM4040	
	TI	TP4040	
	Toshiba	TC4040	
SCL4041	Fairchild	F4041	
	National	CD4041	
	RCA	CD4041	
	Solitron	CM4041	
	SSS	CL4041	
SCL4042	Fairchild	F4042	
	Mitel	SIL4042	
	Motorola	MC14042	
	National	CD4042	
	NEC America	μPD4042	
	RCA	CD4042	
	SGS	HBF4042	
	Solitron	CM4042	
	TI	TP4042	
	Toshiba	TC4042	
SCL4043	Fairchild	F4043	
	Mitel	SIL4043	
	Motorola	MC14043	
	National	CD4043	
	NEC America	μPD4043	
	RCA	CD4043	
	Solitron	CM4043	
	TI	TP4043	
	Toshiba	TC4043	
SCL4044	Fairchild	F4044	
	Mitel	SIL4043	
		SIL4044	
	Motorola	MC14044	
	National	CD4044	
	NEC America	μPD4044	
	RCA	CD4044	
	Solitron	CM4044	
	TI	TP4044	
	Toshiba	TC4044	
SCL4045	RCA	CD4045	
SCL4046	Fairchild	F4046	
	Mitel	SIL4046	
	Motorola	MC14046	
	National	CD4046	
	RCA	CD4046	
	Solitron	CM4046	
SCL4049	Fairchild	F4049	
	Mitel	SIL4049	
	Motorola	MC14049	
	National	CD4049	
	NEC America	μPD4049	
	RCA	CD4049	
	SGS	HBF4049	
	Solitron	CM4049	
	TI	TP4049	
	Toshiba	TC4049	
SCL4050	Fairchild	F4050	
	Mitel	SIL4050	
	Motorola	MC14050	
	National	CD4050	
	NEC America	μPD4050	
	RCA	CD4050	
SCL4050	SGS	HBF4050	
	Solitron	CM4050	
	TI	TP4050	
	Toshiba	TC4050	
SCL4051	Fairchild	F4051	
	Mitel	SIL4051	
	Motorola	MC14051	
	National	CD4051	
	NEC America	μPD4051	
	RCA	CD4051	
	Solitron	CM4051	
	TI	TP4051	
	Toshiba	TC4051	
SCL4052	Fairchild	F4052	
	Mitel	SIL4052	
	Motorola	MC14052	
	National	CD4052	
	NEC America	μPD4052	
	RCA	CD4052	
	Solitron	CM4052	
	TI	TP4052	
	Toshiba	TC4052	
SCL4053	Fairchild	F4053	
	Mitel	SIL4053	
	Motorola	MC14053	
	National	CD4053	
	NEC America	μPD4053	
	RCA	CD4053	
	Solitron	CM4053	
	Toshiba	TC4053	
SCL4060	Mitel	SIL4060	
	National	CD4060	
	RCA	CD4060	
SCL4066	Fairchild	F4066	
	Mitel	SIL4066	
	Motorola	MC14066	
	National	**CD4066**	**1076**
	NEC America	μPD4066	
	RCA	CD4063	
		CD4066	
	SGS	HBF4066	
	Signetics	N4066	
	Solitron	CM4066	
	Toshiba	TC4066	
SCL4068	Fairchild	F4068	
	Mitel	SIL4068	
		SIL4968	
	Motorola	MC14068	
	NEC America	μPD4068	
	RCA	CD4068	
	Solitron	CM4068	
	TI	TP4068	
	Toshiba	TC4068	
SCL4069	Fairchild	F4069	
	Harris	HD74C04	
	Mitel	SIL4069	
	Motorola	MC14069	
	National	CD4069	
		MM74C04	
	NEC America	μPD4069	
	RCA	CD4069	
	Solitron	CM4069	
	TI	TP4069	
	Toshiba	TC4069	
SCL4070	Fairchild	F4070	
	Mitel	SIL4070	
	National	CD4070	
		MM74C86	
	RCA	CD4070	
	Solitron	CM4070	
SCL4071	Fairchild	F4071	
	Mitel	SIL4071	
	Motorola	MC14071	
	National	CD4071	
	NEC America	μPD4071	
	RCA	CD4071	
	Solitron	CM4071	
	TI	TP4071	
	Toshiba	TC4071	
SCL4072	Fairchild	F4072	
	Mitel	SIL4072	
	Motorola	MC14072	
	RCA	CD4072	
	TI	TP4072	
	Toshiba	TC4072	
SCL4073 ♦	Fairchild	F4073	
SCL4073	Mitel	SIL4073	
	Motorola	MC14073	
	National	CD4073	
	NEC America	μPD4073	
	RCA	CD4073	
	Solitron	CM4073	
	TI	TP4073	
	Toshiba	TC4073	
SCL4075	Fairchild	F4075	
	Mitel	SIL4075	
	Motorola	MC14075	
	National	CD4075	
	NEC America	μPD4075	
	RCA	CD4075	
	TI	TP4075	
	Toshiba	TC4075	
SCL4076	Fairchild	F4076	
	Harris	HD74C173	
	Mitel	SIL4076	
	Motorola	MC14076	
	National	CD4076	
		MM74C173	
	RCA	CD4076	
	Solitron	CM4076	
SCL4077	Fairchild	F4077	
	Mitel	SIL4077	
	Motorola	MC14077	
	RCA	CD4077	
	Solitron	CM4077	
SCL4078	Fairchild	F4078	
	Mitel	SIL4078	
		SIL4978	
	Motorola	MC14078	
	NEC America	μPD4078	
	RCA	CD4078	
	Solitron	CM4078	
	Toshiba	TC4078	
SCL4081	Fairchild	F4081	
	Mitel	SIL4081	
	Motorola	MC14081	
	National	CD4081	
	NEC America	μPD4081	
	RCA	CD4081	
	Solitron	CM4081	
	TI	TP4081	
	Toshiba	TC4081	
SCL4082	Fairchild	F4082	
	Mitel	SIL4082	
	Motorola	MC14082	
	NEC America	μPD4082	
	RCA	CD4082	
	TI	TP4082	
	Toshiba	TC4082	
SCL4094	NEC America	μPD4094	
	RCA	CD4094	
SCL4402	RCA	CD4048	
SCL4412	RCA	CD4068	
SCL4445	RCA	CD4045	
	SGS	HBF4045	
	Solitron	CM4045	
SCL4449	RCA	CD4069	
SCL4502	Mitel	SIL4502	
	Motorola	MC14502	
	RCA	CD4502	
SCL4508	Mitel	SIL4508	
	Motorola	MC14508	
	NEC America	μPD4508	
	RCA	CD4508	
	Toshiba	TC4508	
SCL4510	Fairchild	F4510	
	Mitel	SIL4510	
	Motorola	MC14510	
	National	CD4510	
	NEC America	μPD4510	
	RCA	CD40192	
		CD4510	
	Toshiba	TC4510	
SCL4511	Fairchild	F4511	
	Mitel	SIL4511	
	Motorola	MC14511	
	National	CD4511	
	NEC America	μPD4511	
	RCA	CD4511	
	Solitron	CM4511	
	TI	TP4511	
SCL4512	Fairchild	F4512	
SCL4512	Mitel	SIL4512	
	Motorola	MC14512	
	National	CD4512	
	NEC America	μPD4512	
	TI	TP4512	
	Toshiba	TC4512	
SCL4514	Fairchild	F4514	
	Mitel	SIL4514	
	Motorola	MC14514	
	National	CD4514	
	NEC America	μPD4514	
	RCA	CD4514	
	Solitron	CM4514	
	Toshiba	TC4514	
SCL4515	Fairchild	F4515	
	Mitel	SIL4515	
	Motorola	MC14515	
	National	CD4515	
	NEC America	μPD4515	
	RCA	CD4515	
	Solitron	CM4515	
	Toshiba	TC4515	
SCL4516	Fairchild	F4516	
	Mitel	SIL4516	
	Motorola	MC14516	
	National	CD4516	
	NEC America	μPD4516	
	RCA	CD40193	
		CD4516	
	Toshiba	TC4516	
SCL4517	Motorola	MC14517	
	NEC America	μPD4517	
SCL4518	Fairchild	F4518	
	Mitel	SIL4518	
	Motorola	MC14518	
	National	CD4518	
	NEC America	μPD4518	
	RCA	CD4518	
	Solitron	CM4518	
	TI	TP4518	
	Toshiba	TC4518	
SCL4520	Fairchild	F4520	
	Mitel	SIL4520	
	Motorola	MC14520	
	National	CD4520	
	NEC America	μPD4520	
	RCA	CD4520	
	Solitron	CM4520	
	TI	TP4520	
	Toshiba	TC4520	
SCL4522	Fairchild	F4522	
	Motorola	MC14522	
	National	CD4522	
	NEC America	μPD4522	
	RCA	CD4018	
	TI	TP4522	
SCL4526	Fairchild	F4526	
	Motorola	MC14526	
	NEC America	μPD4526	
	TI	TP4526	
SCL4527	Motorola	MC14527	
	National	CD4527	
	RCA	CD4527	
SCL4528	Fairchild	F4528	
	Mitel	SIL4528	
	Motorola	MC14528	
	National	CD4528	
	NEC America	μPD4528	
	RCA	CD4098	
		CD4528	
	Toshiba	TC4528	
SCL4531	Fairchild	F4531	
	Motorola	MC14531	
	RCA	CD40101	
	TI	TP4531	
SCL4543	Motorola	MC14543	
	National	CD4543	
	RCA	CD4056	
SCL4555	Fairchild	F4555	
	Motorola	MC14555	
	NEC America	μPD4555	
	RCA	CD4555	
SCL4556	Fairchild	F4556	
	Motorola	MC14556	
	NEC America	μPD4556	
	RCA	CD4556	

♦ Discontinued

The manufacturers report their devices can be used as direct replacements.
Performance details often differ, so compare the specifications considering your requirements.

Solid State Scientific (cont'd)

Manufacturer Device	Replacement Source	Device	IC Master Page
SCL4581	Motorola	MC14581	
	RCA	CD40181	
	TI	TP4581	
SCL4582	Fairchild	F4582	
	Motorola	MC14582	
	RCA	CD40182	
	TI	TP4582	
SCL4584	Motorola	MC14584	
	National	CD4584	
		MM74C14	**262**
	NEC America	μPD4584	
	RCA	CD4016	
SCL4585	Motorola	MC14585	
	National	MM74C85	
	RCA	CD4063	
	Toshiba	TC4585	
♦SCL5437	Mostek	MK50040	

Solitron Devices

μA2556	Mostek	MK4007	
μA2656	Mostek	MK4007	
μA3556	Mostek	MK4007	
μA3656	Mostek	MK4007	
CM4000	Mitel	SIL4000	
	Motorola	MC14000	
	National	CD4000	
	RCA	CD4000	
	SSS	SCL4000	
	TI	TP4000	
CM4001	Fairchild	F4001	
	Mitel	SIL4001	
	Motorola	MC14001	
	National	CD4001	
	NEC America	μPD4001	
	RCA	CD4001	
	SGS	HBF4001	
	SSS	SCL4001	
	TI	TP4001	
	Toshiba	TC4001	
CM4002	Fairchild	F4002	
	Mitel	SIL4002	
	Motorola	MC14002	
	National	CD4002	
	NEC America	μPD4002	
	RCA	CD4002	
	SGS	HBF4002	
	SSS	SCL4002	
	TI	TP4002	
	Toshiba	TC4002	
CM4006	Fairchild	F4006	
	Motorola	MC14006	
	National	CD4006	
	RCA	CD4006	
	SSS	SCL4006	
CM4007	Fairchild	F4007	
	Mitel	SIL4007	
	Motorola	MC14007	
	National	CD4007	
	RCA	CD4007	
	SGS	HBF4007	
	SSS	SCL4007	
	TI	TP4007	
	Toshiba	TC4007	
CM4008	Fairchild	F4008	
	Motorola	MC14008	
	National	CD4008	
	RCA	CD4008	
	SGS	HBF4008	
	SSS	SCL4008	
	TI	TP4008	
	Toshiba	TC4008	
CM4009	Mitel	SIL4009	
	National	CD4009	
	RCA	CD4009	
	SGS	HBF4009	
	SSS	SCL4009	
	TI	TP4009	
	Toshiba	TC4009	
CM4010	Mitel	SIL4010	
	National	CD4010	
	RCA	CD4010	
CM4010	SGS	HBF4010	
	SSS	SCL4010	
	TI	TP4010	
	Toshiba	TC4010	
CM4011	Fairchild	F4011	
	Mitel	SIL4011	
	Motorola	MC14011	
	National	CD4011	
	NEC America	μPD4011	
	RCA	CD4011	
	SGS	HBF4011	
	SSS	SCL4011	
	TI	TP4011	
	Toshiba	TC4011	
CM4012	Fairchild	F4012	
	Mitel	SIL4012	
	Motorola	MC14012	
	National	CD4012	
	NEC America	μPD4012	
	RCA	CD4012	
	SGS	HBF4012	
	SSS	SCL4012	
	TI	TP4012	
	Toshiba	TC4012	
CM4013	Fairchild	F4013	
	Mitel	SIL4013	
	Motorola	MC14013	
	National	CD4013	
	NEC America	μPD4013	
	RCA	CD4013	
	SGS	HBF4013	
	SSS	SCL4013	
	TI	TP4013	
	Toshiba	TC4013	
CM4014	Fairchild	F4014	
	Mitel	SIL4014	
	Motorola	MC14014	
	National	CD4014	
	NEC America	μPD4014	
	RCA	CD4014	
	SGS	HBF4014	
	SSS	SCL4014	
	TI	TP4014	
	Toshiba	TC4014	
CM4015	Fairchild	F4015	
	Mitel	SIL4015	
	Motorola	MC14015	
	National	CD4015	
	NEC America	μPD4015	
	RCA	CD4015	
	SGS	HBF4015	
	SSS	SCL4015	
	TI	TP4015	
	Toshiba	TC4015	
CM4016	AD	AD7516	
	Fairchild	F4016	
	Micro Power	MP7516	
	Mitel	SIL4016	
	Motorola	MC14016	
	National	**CD4016**	**1076**
	RCA	CD4016	
		CD4066	
	SSS	SCL4016	
	TI	TP4016	
CM4017	Fairchild	F4017	
	Mitel	SIL4017	
	Motorola	MC14017	
	National	CD4017	
	NEC America	μPD4017	
	RCA	CD4017	
	SGS	HBF4017	
	SSS	SCL4017	
	TI	TP4017	
	Toshiba	TC4017	
CM4018	Fairchild	F4018	
	Mitel	SIL4018	
	National	CD4018	
	RCA	CD4018	
	SGS	HBF4018	
	SSS	SCL4018	
	TI	TP4018	
	Toshiba	TC4018	
CM4019	Fairchild	F4019	
	Mitel	SIL4019	
	Motorola	MC14519	
	National	CD4019	
CM4019	RCA	CD4019	
	SGS	HBF4019	
	SSS	SCL4019	
	TI	TP4019	
	Toshiba	TC4019	
CM4020	Fairchild	F4020	
	Mitel	SIL4020	
	Motorola	MC14020	
	National	CD4020	
	NEC America	μPD4020	
	RCA	CD4020	
	SGS	HBF4020	
	SSS	SCL4020	
	TI	TP4020	
	Toshiba	TC4020	
CM4021	Fairchild	F4021	
	Mitel	SIL4021	
	Motorola	MC14021	
	National	CD4021	
	NEC America	μPD4021	
	RCA	CD4021	
	SSS	SCL4021	
	TI	TP4021	
	Toshiba	TC4021	
CM4022	Fairchild	F4022	
	Mitel	SIL4022	
	Motorola	MC14022	
	National	CD4022	
	RCA	CD4022	
	SGS	HBF4022	
	SSS	SCL4022	
	TI	TP4022	
	Toshiba	TC4022	
CM4023	Fairchild	F4023	
	Mitel	SIL4023	
	Motorola	MC14023	
	National	CD4023	
	NEC America	μPD4023	
	RCA	CD4023	
	SGS	HBF4023	
	SSS	SCL4023	
	TI	TP4023	
	Toshiba	TC4023	
CM4024	Fairchild	F4024	
	Mitel	SIL4024	
	Motorola	MC14024	
	National	CD4024	
	RCA	CD4024	
	SGS	HBF4024	
	SSS	SCL4024	
	TI	TP4024	
	Toshiba	TC4024	
CM4025	Fairchild	F4025	
	Mitel	SIL4025	
	Motorola	MC14025	
	National	CD4025	
	NEC America	μPD4025	
	RCA	CD4025	
	SGS	HBF4025	
	SSS	SCL4025	
	TI	TP4025	
	Toshiba	TC4025	
CM4026	RCA	CD4026	
	SSS	SCL4026	
CM4027	Fairchild	F4027	
	Mitel	SIL4027	
	Motorola	MC14027	
	National	CD4027	
	NEC America	μPD4027	
	RCA	CD4027	
	SGS	HBF4027	
	SSS	SCL4027	
	TI	TP4027	
	Toshiba	TC4027	
CM4028	Fairchild	F4028	
	Mitel	SIL4028	
	Motorola	MC14028	
	National	CD4028	
	NEC America	μPD4028	
	RCA	CD4028	
	SGS	HBF4028	
	SSS	SCL4028	
	TI	TP4028	
	Toshiba	TC4028	
CM4029	Fairchild	F4029	
	Mitel	SIL4029	
CM4029	National	CD4029	
	NEC America	μPD4029	
	RCA	CD4029	
	SGS	HBF4029	
	SSS	SCL4029	
	TI	TP4029	
	Toshiba	TC4029	
CM4030	Fairchild	F4030	
	Mitel	SIL4030	
	National	CD4030	
	NEC America	μPD4030	
	RCA	CD4030	
		CD4070	
	SGS	HBF4030	
	SSS	SCL4030	
	TI	TP4030	
	Toshiba	TC4030	
CM4032	Motorola	MC14032	
	RCA	CD4032	
	Toshiba	TC4032	
CM4033	RCA	CD4033	
	SGS	HBF4033	
	SSS	SCL4033	
CM4034	Fairchild	F4034	
	Motorola	MC14034	
	National	CD4034	
	RCA	CD4034	
	SSS	SCL4034	
	Toshiba	TC4034	
CM4035	Fairchild	F4035	
	Mitel	SIL4035	
	Motorola	MC14035	
	National	CD4035	
	NEC America	μPD4035	
	RCA	CD4035	
	SGS	HBF4035	
	SSS	SCL4035	
	TI	TP4035	
	Toshiba	TC4035	
CM4036	RCA	CD4036	
CM4037	RCA	CD4037	
CM4038	Motorola	MC14038	
		MC14308	
	RCA	CD4038	
	Toshiba	TC4038	
CM4039	RCA	CD4039	
CM4040	Fairchild	F4040	
	Mitel	SIL4040	
	Motorola	MC14040	
	National	CD4040	
	NEC America	μPD4040	
	RCA	CD4040	
	SSS	SCL4040	
	TI	TP4040	
	Toshiba	TC4040	
CM4041	Fairchild	F4041	
	National	CD4041	
	RCA	CD4041	
	SSS	CL4041	
		SCL4041	
CM4042	Fairchild	F4042	
	Mitel	SIL4042	
	Motorola	MC14042	
	National	CD4042	
	NEC America	μPD4042	
	RCA	CD4042	
	SGS	HBF4042	
	SSS	SCL4042	
	TI	TP4042	
	Toshiba	TC4042	
CM4043	Fairchild	F4043	
	Mitel	SIL4043	
	Motorola	MC14023	
		MC14043	
	National	CD4023	
		CD4043	
	NEC America	μPD4043	
	RCA	CD4023	
		CD4043	
	SSS	SCL4023	
		SCL4043	
	TI	TP4043	
	Toshiba	TC4043	
CM4044	Fairchild	F4044	
	Mitel	SIL4044	
	Motorola	MC14044	

♦ Discontinued

Bold face device numbers indicate manufacturers data is provided in the IC Master on the pages noted.

Solitron Devices (cont'd)

Manufacturer Device	Replacement Source	Device	IC Master Page
CM4044	National	CD4044	
	NEC America	μPD4044	
	RCA	CD4044	
	SSS	SCL4044	
	TI	TP4044	
	Toshiba	TC4044	
CM4045	RCA	CD4045	
	SGS	HBF4045	
	SSS	SCL4445	
CM4046	Fairchild	F4046	
	Mitel	SIL4046	
	Motorola	MC14046	
	National	CD4046	
	RCA	CD4046	
	SSS	SCL4046	
CM4047	Fairchild	F4047	
	RCA	CD4047	
	Toshiba	TC4047	
CM4048	RCA	CD4048	
CM4049	Fairchild	F4049	
	Mitel	SIL4049	
	Motorola	MC14049	
	National	CD4049	
	NEC America	μPD4049	
	RCA	CD4049	
	SGS	HBF4049	
	SSS	SCL4049	
	TI	TP4049	
	Toshiba	TC4049	
CM4050	Fairchild	F4050	
	Mitel	SIL4050	
	Motorola	MC14050	
	National	CD4050	
	NEC America	μPD4050	
	RCA	CD4050	
	SGS	HBF4050	
	SSS	SCL4050	
	TI	TP4050	
	Toshiba	TC4050	
CM4051	Fairchild	F4051	
	Mitel	SIL4051	
	Motorola	MC14051	
	National	CD4051	
	RCA	CD4051	
	SSS	SCL4051	
	TI	TP4051	
	Toshiba	TC4051	
CM4052	Fairchild	F4052	
	Mitel	SIL4052	
	Motorola	MC14052	
	National	CD4052	
	RCA	CD4052	
	SSS	SCL4052	
	TI	TP4052	
	Toshiba	TC4052	
CM4053	Fairchild	F4053	
	Mitel	SIL4053	
	Motorola	MC14053	
	National	CD4053	
	RCA	CD4053	
	SSS	SCL4053	
	Toshiba	TC4053	
CM4066	Fairchild	F4066	
	Mitel	SIL4066	
	Motorola	MC14066	
	National	**CD4066**	**1076**
	NEC America	μPD4066	
	RCA	CD4063	
		CD4066	
	SGS	HBF4066	
	Signetics	N4066	
	SSS	SCL4066	
	Toshiba	TC4066	
CM4068	Fairchild	F4068	
	Mitel	SIL4068	
	Motorola	MC14068	
	RCA	CD4068	
	SSS	SCL4068	
	TI	TP4068	
	Toshiba	TC4068	
CM4069	Fairchild	F4069	
	Harris	HD74C04	
	Mitel	SIL4069	
CM4069	Motorola	MC14069	
	National	CD4069	
		MM74C04	
	NEC America	μPD4069	
	RCA	CD4069	
	SSS	SCL4069	
	TI	TP4069	
	Toshiba	TC4069	
CM4070	Fairchild	F4070	
	Mitel	SIL4070	
	National	CD4070	
		MM74C86	
	RCA	CD4070	
	SSS	SCL4070	
CM4071	Fairchild	F4071	
	Mitel	SIL4071	
	Motorola	MC14071	
	National	CD4071	
	NEC America	μPD4071	
	RCA	CD4071	
	SSS	SCL4071	
	TI	TP4071	
	Toshiba	TC4071	
CM4073	Fairchild	F4073	
	Mitel	SIL4073	
	Motorola	MC14073	
	National	CD4073	
	RCA	CD4073	
	SSS	SCL4073	
	TI	TP4073	
	Toshiba	TC4073	
CM4075	RCA	CD4075	
CM4076	Fairchild	F4076	
	Harris	HD74C173	
	Mitel	SIL4076	
	Motorola	MC14076	
	National	CD4076	
		MM74C173	
	RCA	CD4076	
	SSS	SCL4076	
CM4077	Fairchild	F4077	
	Mitel	SIL4077	
	Motorola	MC14077	
	RCA	CD4077	
	SSS	SCL4077	
CM4078	Fairchild	F4078	
	Mitel	SIL4078	
	Motorola	MC14078	
	RCA	CD4078	
	SSS	SCL4078	
	Toshiba	TC4078	
CM4081	Fairchild	F4081	
	Mitel	SIL4081	
	Motorola	MC14081	
	National	CD4081	
	NEC America	μPD4081	
	RCA	CD4081	
	SSS	SCL4081	
	TI	TP4081	
	Toshiba	TC4081	
CM4510	National	CD4510	
	RCA	CD4510	
CM4511	Fairchild	F4511	
	Mitel	SIL4511	
	Motorola	MC14511	
	National	CD4511	
	RCA	CD4511	
	SSS	SCL4511	
	TI	TP4511	
CM4514	Fairchild	F4514	
	Mitel	SIL4514	
	Motorola	MC14514	
	RCA	CD4514	
	SSS	SCL4514	
	Toshiba	TC4514	
CM4515	Mitel	SIL4515	
	Motorola	MC14515	
	RCA	CD4515	
	SSS	SCL4515	
	Toshiba	TC4515	
CM4516	National	CD4516	
CM4518	Fairchild	F4518	
	Mitel	SIL4518	
	Motorola	MC14518	
	National	CD4518	
	RCA	CD4518	
CM4518	SSS	SCL4518	
	TI	TP4518	
	Toshiba	TC4518	
CM4520	Fairchild	F4520	
	Mitel	SIL4520	
	Motorola	MC14520	
	National	CD4520	
	NEC America	μPD4520	
	RCA	CD4520	
	SSS	SCL4520	
	TI	TP4520	
	Toshiba	TC4520	
UC4250	Intersil	LM4250	
	National	LM4250	
	Silicon G	SG4250	
UC4741	PMI	SSS741	
	RCA	CA741	

Sprague Electric Company

Manufacturer Device	Replacement Source	Device	IC Master Page
CA3089	Signetics	CA3089	
UDN-2841	TI	UDN2841	
UDN-2842	TI	UDN2842	
UDN-2843	TI	UDN2843	
UDN-2844	TI	UDN2844	
UDN-2845	TI	UDN2845	
UDN-2846	TI	UDN2846	
UDN-5711	Motorola	MC1471	
	Signetics	UDN5711	
UDN-5712	Motorola	MC1472	
	Signetics	UDN5712	
UDN-5713	Motorola	MC1473	
	Signetics	UDN5713	
UDN-5714	Motorola	MC1474	
	Signetics	UDN5714	
UDN-6144	Dionics	DI502	
UDN-6164	Dionics	DI507	
UDN-6184	Dionics	DI512	
UDN-7183	Dionics	DI302	
UDN-7184	Dionics	DI302	
UDN-7185	Dionics	UDN-7186	
ULN-2001	**Exar**	**XR2201**	**931**
	Fairchild	9665	
	Motorola	MC1411	
		ULN-2001	
	SGS	L201	
	Signetics	NE5601	
		ULN2001	
	Silicon G	SG2001	
	TI	ULN2001	
ULN-2002	**Exar**	**XR2202**	**931**
	Fairchild	9666	
	Motorola	MC1412	
		ULN-2002	
	SGS	L202	
	Signetics	NE5502	
		ULN2002	
	Silicon G	SG2002	
	TI	ULN2002	
ULN-2003	**Exar**	**XR2203**	**931**
	Fairchild	9667	
	Motorola	MC1413	
		ULN-2003	
	SGS	L203	
	Signetics	NE5503	
		ULN2003	
	Silicon G	SG2003	
	TI	ULN2003	
ULN-2004	**Exar**	**XR2204**	**931**
	Fairchild	9668	
	Motorola	MC1416	
		ULN-2004	
	Signetics	NE5504	
		ULN2004	
	TI	ULN2004	
ULN-2021	Signetics	NE5501	
ULN-2022	Signetics	NE5502	
ULN-2023	Signetics	NE5503	
ULN-2024	Signetics	NE5504	
ULN-2064	TI	ULN2064	
ULN-2065	TI	ULN2065	
ULN-2111	Fairchild	μA2136	
	Motorola	MC1357	
	National	LM2111	
	RCA	CA2111	
♦ULN-2114	Fairchild	μA746	
	RCA	CA3072	
ULN-2124	Fairchild	μA780	
	RCA	CA3070	
ULN-2125	RCA	CA3120	
♦ULN-2126	Exar	XR4739	
	Fairchild	μA739	
	SGS	TBA231	
ULN-2127	Fairchild	μA781	
	RCA	CA3071	
♦ULN-2128	Fairchild	μA767	
♦ULN-2129	Motorola	MC1375	
♦ULN-2131	Fairchild	μA753	
ULN-2136	Fairchild	μA2136	
	Motorola	MC1356	
♦ULN-2137	Fairchild	μA720	
	RCA	CA3123	
♦ULN-2165	Fairchild	μA3065	
	Motorola	MC1358	
	RCA	CA3065	
ULN-2209	Fairchild	μA753	
♦ULN-2210	Exar	XR1310	
	Motorola	MC1310	
	RCA	CA1310	
ULN-2211	Motorola	MC1310	
	RCA	CA3011	
ULN-2212	RCA	CA3012	
ULN-2224	Motorola	MC1324	
ULN-2244	Fairchild	μA758	
	RCA	CA758	
♦ULN-2262	Fairchild	μA787	
	RCA	CA3126	
ULN-2264	Fairchild	μA3064	
	Motorola	MC1364	
	RCA	CA3064	
♦ULN-2266	RCA	CA3066	
♦ULN-2267	Fairchild	μA3067	
ULN-2269	RCA	CA3121	
ULN-2278	Fairchild	μA705	
ULN-2289	Fairchild	μA3089	
	RCA	CA3089	
ULN-2298	Motorola	MC1398	
	RCA	CA1398	
ULN-2741	**National**	**LM741**	**1035**
	RCA	CA741	
	TI	μA741	
♦ULN-2747	RCA	CA747	
	TI	μA747	
♦ULN-3006	Sprague	UGN-3201	
♦ULN-3007	Sprague	UGN-3203	
♦ULN-3008	Sprague	UGN-3501	
♦ULN-3100	Sprague	UGN-3600	
♦ULN-3101	Sprague	UGN-3601	
ULN-3303	Cherry	CS102-2	
ULN-3304	Cherry	CS102	
		MCC102	
ULN-3305	Cherry	CS122	
		MCC122	
ULN-3306	Cherry	CS122-2	
ULN-6118	**Exar**	**XR6118**	**931**
ULN-6128	Exar	XR6128	

Standard Microsystems Corporation

Manufacturer Device	Replacement Source	Device	IC Master Page
CG44100	Mostek	MK2002	
COM1671	Western	UC1671	
COM2017	**AMI**	**S1883**	**629**
	TI	TMS6011	
	Western	TR1602	
COM2502	**Fairchild**	**F6850**	**1887,1891**
	GI	AY3-1014A	
		AY3-1015	
	Western	TR1602A	
COM2505	GI	AY5-1013	
COM2601	**AMI**	**S2350**	**634**
COM5016	Western	BR1941	
COM5025	National	INS2652	
	Signetics	**2652**	**2306**
KR2376	GI	AY5-2376	
KR3600	GI	AY5-3600	

♦ Discontinued

The manufacturers report their devices can be used as direct replacements.
Performance details often differ, so compare the specifications considering your requirements.

IC MASTER

Manufacturer Device	Replacement Source	Device	IC Master Page
Synertek			
SY1103	AMI	S1103A	
SY1103A	AMI	S1103A	
	Intel	1103A	
	Rockwell	1103A	
SY21H02	Fairchild	3542	
SY21L02	**Fairchild**	**2102L**	**1275**
	Signetics	21L02	
SY2101	**Fairchild**	**2102**	**1275**
		21021	**1275**
		3538	
	Signetics	2101	
SY2102	Signetics	21F02	
SY2111	Signetics	2111	
SY2112	Signetics	2112	
SY2114	AMD	9114	
		9124	
	AMI	**S2114**	**1196**
	Fairchild	**2114**	**1281**
	Fujitsu	MB8114	
	Intel	2114	
	Rockwell	R2114	
	Signetics	**2614**	**1669**
	TI	TMS4045	
SY2316	**Signetics**	**2616**	**1670**
SY2316A	**AMI**	**S6831A**	
			1215,1806
	Mostek	MK31000	
SY2316B	**AMI**	**S4216B**	**1209**
		S6831B	
			1215,1806
	Mostek	MK34000	
	TI	TMS4732	
SY2332	**AMI**	**S68332**	**1216**
	Rockwell	R2332	
	Signetics	**2632**	**1672**
SY2364	**AMI**	**S4264**	**1212**
SY5101	**AMI**	**S5101**	**1206**
	SSS	SCM5101	
SY5102	SSS	SCM5102	
♦SY5280	Fujitsu	MB8107	
SY6502	MOS	MCS6502	
	Rockwell	R6502	
SY6503	MOS	MCS6503	
	Rockwell	R6503	
SY6504	MOS	MCS6504	
	Rockwell	R6504	
SY6505	MOS	MCS6505	
	Rockwell	R6505	
SY6506	Rockwell	R6506	
SY6507	Rockwell	R6507	
SY6512	MOS	MCS6512	
	Rockwell	R6512	
SY6513	Rockwell	R6513	
SY6514	MOS	MCS6514	
	Rockwell	R6514	
SY6515	MOS	SY6515	
	Rockwell	R6515	
SY6520	MOS	MCS6520	
	Rockwell	R6520	
SY6522	MOS	MCS6522	
SY6530	MOS	MCS6530	
	Rockwell	R6530	
SY6531	Rockwell	R6531	
SY6532	MOS	MCS6532	
	Rockwell	R6532	
SY6545	Rockwell	R6545	
SY6551	Rockwell	R6551	
S42364	Mostek	MK36000	
S6500/1	Rockwell	R6500/1	
Teledyne Crystalonics			
CDR125	Siliconix	D125	
Teledyne Philbrick			
1321	**Datel**	**AM-462-2**	**687**
	Harris	**HA-2625**	**980**
1322	**Datel**	**AM-452-2**	**687**
	Harris	**HA-2525**	**972**
1323	**Harris**	**HA-2705**	**988**
1324	**Harris**	**HA-2505**	**966**
1430	Datel	AM-500C	
1431	**Harris**	**HA-2065A**	**962**
4551	**Datel**	**MXD-807**	**683**
	Harris	HI507A	
4552	**Datel**	**MX-1606**	**683**
	Harris	HI506A	
4856	**Datel**	**SHM-IC-1**	**685**
	Harris	**HA-2425**	**1020**
Teledyne Semiconductor			
8700	**Datel**	**ADC-EK8B**	**662**
8701	**Datel**	**ADC-EK10B**	**662**
8702	**Datel**	**ADC-EK12B**	**662**
8703	Datel	ADC-ET8B	
8704	Datel	ADC-ET10B	
8705	Datel	ADC-ET12B	
8750	Datel	ADC-EK12D	
9400C	Datel	VFQ-1	
Telefunken			
TCA830	SGS	TCA830	
TDA1083	Sprague	ULN-2204	
TDA440	Plessey	TDA440	
	SGS	TDA440	
Texas Instruments			
µA702	Fairchild	µA702	
	Motorola	MC1712	
	NEC America	µPC51	
		µPC51A	
	Raytheon	RC702	
		RM702	
µA709	Fairchild	µA709	
	Motorola	MC1709	
	National	**LM709**	**1035**
	NEC America	µPC55A	
	Raytheon	RC709	
		RM709	
	Signetics	µA709	
	Toshiba	TA7502	
µA710	Fairchild	µA710	
	Motorola	MC1710	
	National	LM710	
	NEC America	µPC71	
	Raytheon	RC710	
		RM710	
	Signetics	µA710	
	Silicon G	SG710	
µA711	Fairchild	µA711	
	Motorola	MC1711	
	National	LM711	
	Raytheon	RC711	
		RM711	
	Signetics	µA711	
	Silicon G	SG711	
µA723	AMD	723	
	Fairchild	**µA723**	**934**
	Intersil	723	
	Motorola	MC1723	
	National	LM723	
	Raytheon	RC723	
		RM723	
	RCA	CA723	
	Signetics	µA723	
	Silicon G	SG723	
µA733	AMD	733	
	Fairchild	µA733	
	Motorola	MC1733	
	National	LM733	
	Raytheon	RC733	
		RM733	
	Signetics	µA733	
	Silicon G	SG733	
µA741	AMD	741	
	Fairchild	µA741	
	Intersil	741	
	Motorola	MC1741	
	National	**LM741**	**1035**
	NEC America	µPC151	
µA741	NEC America	µPC741	
	PMI	OP-02	
		PM741	
		SSS741	
	Raytheon	RC741	
		RM741	
	RCA	CA741	
	Signetics	µA741	
	Silicon G	SG741	
	Toshiba	TA7504	
µA747	AMD	747	
	Fairchild	µA747	
	Motorola	MC1747	
	National	LM747	
	NEC America	µPC251	
	PMI	PM747	
		SSS747	
	Raytheon	RC747	
		RM747	
	RCA	CA747	
	Silicon G	SG747	
µA748	AMD	748	
	Fairchild	µA748	
	Intersil	748	
	Motorola	MC1748	
	National	LM748	
	Raytheon	RC748	
		RM748	
	RCA	CA748	
	Signetics	µA748	
	Silicon G	SG748	
µA777	Fairchild	µA777	
	Intersil	777	
	Silicon G	SG777	
µA78L02	Signetics	µA78L02	
µA78L05	NEC America	µPC78L05	
	Signetics	µA78L05	
µA78L06	Signetics	µA78L06	
µA78L08	NEC America	µPC78L08	
	Signetics	µA78L08	
µA78L12	NEC America	µPC78L12	
	Signetics	µA78L12	
µA78L15	Signetics	µA78L15	
µA78M05	NEC America	µPC78M05	
	Signetics	µA78M05	
µA78M06	Signetics	µA78M06	
µA78M08	NEC America	µPC78M08	
µA78M12	NEC America	µPC78M12	
µA78M15	NEC America	µPC78M15	
µA7805	NEC America	µPC14305	
	Signetics	µA7805	
µA7806	Signetics	µA7806	
µA7808	NEC America	µPC14308	
	Signetics	µA7808	
µA7812	NEC America	µPC14312	
	Signetics	µA7812	
µA7815	NEC America	µPC14315	
	Signetics	µA7815	
µA7818	NEC America	µPC14318	
	Signetics	µ7818	
µA7824	NEC America	µPC14324	
	Signetics	µA7824	
µA79M05	Signetics	µA79M05	
µA79M06	Signetics	µA79M06	
µA79M08	Signetics	µA79M08	
µA79M12	Signetics	µA79M12	
µA79M15	Signetics	µA79M15	
µA79M24	Signetics	µA79M24	
µA7905	Signetics	µA7905	
µA7906	Signetics	µA7906	
µA7908	Signetics	µA7908	
µA7912	Signetics	µA7912	
µA7918	Signetics	µA7918	
µA7924	Signetics	µA7924	
LF155	AMD	LF155	
	Fairchild	µAF155	
	Intersil	LF155	
	Motorola	LF155	
	National	**LF155**	**1035**
	PMI	PM155	
	Raytheon	LF155	
	Signetics	LF155	
LF156	AMD	LF156	
	Fairchild	µAF156	
	Intersil	LF156	
	Motorola	LF156	
LF156	**National**	**LF156**	**1035**
	PMI	PM156	
	Raytheon	LF156	
	Signetics	LF156	
LF157	AMD	LF157	
	Fairchild	µAF157	
	Intersil	LF157	
	Motorola	LF157	
	National	**LF157**	**1035**
	PMI	PM157	
	Raytheon	LF157	
	Signetics	LF157	
LF255	AMD	LF255	
	Fairchild	µAF255	
	Intersil	LF255	
	Motorola	LF255	
	National	LF255	
	PMI	PM255	
	Raytheon	LF255	
	Signetics	LF255	
LF256	AMD	LF256	
	Fairchild	µAF256	
	Intersil	LF256	
	Motorola	LF256	
	National	LF256	
	PMI	PM256	
	Raytheon	LF256	
	Signetics	LF256	
LF257	AMD	LF257	
	Fairchild	µAF257	
	Intersil	LF257	
	Motorola	LF257	
	National	LF257	
	PMI	PM257	
	Raytheon	LF257	
	Signetics	LF257	
LF355	AMD	LF355	
	Fairchild	µAF355	
	Intersil	LF355	
	Motorola	LF355	
	National	LF355	
	PMI	PM355	
	Raytheon	LF355	
	Signetics	LF355	
LF356	AMD	LF356	
	Fairchild	µAF356	
	Intersil	LF356	
	Motorola	LF356	
	National	**LF356**	**1035,1073**
	PMI	PM356	
	Raytheon	LF356	
	Signetics	LF356	
LF357	**AMD**	LF357	
	Fairchild	µAF357	
	Intersil	LF357	
	Motorola	LF357	
	National	LF357	
	PMI	PM357	
	Raytheon	LF357	
	Signetics	LF357	
LM101	AMD	LM101	
	Fairchild	µA101	
	Intersil	LM101	
	Motorola	LM101	
	National	**LM101**	**1035**
	Raytheon	LM101	
	RCA	CA101	
	Signetics	LM101	
	Silicon G	SG101	
LM104	Motorola	LM104	
	Silicon G	SG104	
LM105	AMD	LM105	
	Intersil	LM105	
	Motorola	LM105	
	National	LM105	
	Raytheon	LM105	
	Silicon G	SG105	
LM106	AMD	LM106	
LM107	AMD	LM107	
	Fairchild	µA107	
	Intersil	LM107	
	Motorola	LM107	
	National	LM107	
	Raytheon	LM107	
	RCA	CA107	
	Signetics	LM107	

♦ Discontinued

Bold face device numbers indicate manufacturers data is provided in the IC Master on the pages noted.

Texas Instruments (cont'd)

Manufacturer Device	Replacement Source	Device	IC Master Page
LM107	Silicon G	SG107	
LM108	AMD	LM108	
	Raytheon	LM108	
	RCA	CA308	
	Silicon G	SG108	
LM111	AMD	LM111	
	Intersil	LM111	
	National	LM111	
	Raytheon	LM111	
	RCA	CA111	
	Signetics	LM111	
	Silicon G	SG111	
LM118	AMD	LM118	
LM301	AMD	LM301	
	Fairchild	μA301	
	Intersil	LM301	
	Motorola	LM301	
	National	LM301	
	Raytheon	LM301	
	RCA	CA301	
	Signetics	LM301	
	Silicon G	SG301	
	Toshiba	TA7506	
LM301A	NEC America	μPC157	
		μPC301A	
LM304	**Fairchild**	**μA304**	**934**
	Motorola	LM304	
	NEC America	μPC142	
	Silicon G	SG304	
LM305	AMD	LM305	
	Fairchild	**μA305**	**934**
	Intersil	LM305	
	Motorola	LM305	
	NEC America	μPC141	
	Raytheon	LM305	
	Silicon G	SG305	
LM306	AMD	LM306	
LM307	AMD	LM307	
	Fairchild	μA307	
	Intersil	LM307	
	Motorola	LM307	
	National	LM307	
	Raytheon	LM307	
	RCA	CA307	
	Signetics	LM307	
	Silicon G	SG307	
LM308	AMD	LM308	
	NEC America	μPC156A	
	Raytheon	LM308	
	Silicon G	SG308	
LM311	AMD	LM311	
	Fairchild	μA311	
	Intersil	LM311	
	Motorola	LM311	
	NEC America	μPC271	
		μPC311	
	Raytheon	μPC271	
		LM311	
	RCA	CA311	
	Signetics	LM311	
	Silicon G	SG311	
LM318	AMD	LM318	
	NEC America	μPC159A	
LM324	NEC America	μPC324	
LM339	NEC America	μPC339	
LM340-12	**National**	**LM340-12**	**1060**
	Silicon G	SG340-12	
LM340-15	**National**	**LM340-15**	**1060**
	Silicon G	SG340-15	
LM340-18	**National**	**LM340-18**	**1060**
	Silicon G	SG340-18	
LM340-24	**National**	**LM340-24**	**1060**
	Silicon G	SG340-24	
LM340-5	**National**	**LM340-5**	**1060**
	Silicon G	SG340-5	
LM340-6	**National**	**LM340-6**	**1060**
	Silicon G	SG340-6	
LM340-8	**National**	**LM340-8**	**1060**
	Silicon G	SG340-8	
LM358	NEC America	μPC358	
LM376	**Fairchild**	**μA376**	**934**
	NEC America	μPC305	
MC1458	Exar	XR1458	
MC1458	Fairchild	μA1458	
	Harris	**HA-2655**	**986**
	Motorola	MC1458	
	National	LM1458	
	NEC America	μPC1458	
	PMI	OP-14	
		SSS1458	
	Raytheon	RC1458	
		RC4558	
	RCA	CA1458	
	Signetics	MC1458	
	Silicon G	SG1458	
MC1489A	Signetics	MC1489A	
	Silicon G	SG1489A	
MC1558	Exar	XR1558	
	Fairchild	μA1558	
	Harris	**HA-2650**	**986**
	Motorola	MC1558	
	National	LM1558	
	PMI	PM1558	
		SSS1558	
	Raytheon	RM1558	
		RM4558	
	RCA	CA1558	
	Silicon G	SG1558	
MC3423	Motorola	MC3423	
MC3446	Motorola	MC3446A	
NE555	AMD	NE555	
	Cherry	CS555	
	Exar	XR555	
	Fairchild	μA555	
	Intersil	NE555	
	Motorola	MC1455	
	NEC America	μPC1555	
	Raytheon	RC555	
	RCA	CA555	
	Signetics	NE555	
	Silicon G	SG555	
NE556	Exar	XR556	
	Fairchild	μA556	
	Motorola	MC3456	
	Silicon G	SG556	
RC4136	Exar	XR4136	
	Raytheon	RC4136	
	Silicon G	SG4136C	
RC4558	Exar	XR4558	
	Motorola	MC4558	
	NEC America	μPC4558	
	Raytheon	RC4558	
RM4136	Exar	XR4136	
	Raytheon	RC4136	
	Silicon G	SG4136	
RM4558	Exar	XR4558	
	Motorola	MC4558	
	Raytheon	RM4558	
SE555	AMD	SE555	
	Exar	XR555M	
	Intersil	SE555	
	Motorola	MC1555	
	Raytheon	RM555	
	RCA	CA555	
	Signetics	SE555	
	Silicon G	SG555	
SG1524	**Exar**	**XR1524**	**930**
	Silicon G	**SG1524**	**1128**
SG2524	Exar	SR2524	
	Silicon G	**SG2524**	**1128**
SG3524	**Silicon G**	**SG3524**	**1128**
SG3624	**Exar**	**XR3524**	**930**
♦SN10101	Motorola	MC10101	
♦SN10102	Motorola	MC10102	
	NEC America	μPB10142	
♦SN10104	Motorola	MC10104	
♦SN10105	Motorola	MC10105	
♦SN10106	Motorola	MC10106	
♦SN10107	Motorola	MC10107	
♦SN10109	Motorola	MC10109	
♦SN10110	Motorola	MC10110	
♦SN10111	Motorola	MC10111	
♦SN10115	Motorola	MC10115	
♦SN10116	Motorola	MC10116	
♦SN10117	Motorola	MC10117	
♦SN10118	Motorola	MC10118	
♦SN10119	Motorola	MC10119	
♦SN10121	Motorola	MC10121	
♦SN10130	Motorola	MC10130	
♦SN10131	Motorola	MC10131	
♦SN10133	Motorola	MC10133	
SN10140	Signetics	10140	
SN10144	Motorola	MC10144	
	NEC America	μPB10144	
	Raytheon	RC10144	
	Signetics	10144	
SN10147	Fairchild	F10405	
SN10148	Hitachi	HD10148	
	Motorola	MCM10148	
	NEC America	μPB10148	
	Signetics	10148	
♦SN10160	Motorola	MC10160	
♦SN10161	Motorola	MC10161	
SN10164	Fairchild	F10164	
	Hitachi	HD10164	
	Motorola	MC10164	
	NEC America	μPB10164	
	Signetics	10164	
SN10174	Fairchild	F10174	
	Hitachi	HD10174	
	Motorola	MC10174	
	NEC America	μPB10174	
	Signetics	10174	
SN10175	Motorola	MC10175	
♦SN10179	Motorola	MC10179	
♦SN10181	Motorola	MC10181	
SN151800	Motorola	MC1800	
	National	DM1800	
SN151801	Motorola	MC1801	
	National	DM1801	
SN151802	Motorola	MC1802	
SN151803	Motorola	MC1803	
SN151804	Motorola	MC1804	
SN151805	Motorola	MC1805	
SN151806	Motorola	MC1806	
SN151807	Motorola	MC1807	
SN151808	Motorola	MC1808	
SN151809	Motorola	MC1809	
SN151810	Motorola	MC1810	
SN151811	Motorola	MC1811	
SN151812	Motorola	MC1812	
SN151820	Motorola	MC1820	
SN151900	Motorola	MC1900	
SN151901	Motorola	MC1901	
SN151902	Motorola	MC1902	
SN151904	Motorola	MC1904	
SN151905	Motorola	MC1905	
SN151906	Motorola	MC1906	
SN151907	Motorola	MC1907	
SN151908	Motorola	MC1908	
SN151909	Motorola	MC1909	
SN151910	Motorola	MC1910	
SN151911	Motorola	MC1911	
SN151912	Motorola	MC1912	
SN151920	Motorola	MC1920	
SN158093	Fairchild	9093	
	Motorola	MC853	
	National	DM9093	
SN158094	Fairchild	9094	
	Motorola	MC856	
	National	DM9094	
SN158097	Fairchild	9097	
	Motorola	MC855	
	National	DM9097	
SN158099	Fairchild	9099	
	Motorola	MC852	
	National	DM9099	
SN15830	Fairchild	930	
	Hitachi	HD2204	
	Motorola	MC830	
	National	DM930	
SN15831	Fairchild	931	
	Motorola	MC831	
SN15832	Fairchild	932	
	Hitachi	HD2201	
	Motorola	MC832	
	National	DM932	
SN15833	Fairchild	933	
	Hitachi	HD2202	
	Motorola	MC833	
	National	DM933	
SN15834	Motorola	MC834	
SN15835	Fairchild	935	
	Motorola	MC840	
	National	DM935	
SN15836	Fairchild	936	
	Hitachi	HD2206	
	Motorola	MC836	
	National	DM936	
SN15837	Fairchild	937	
	Motorola	MC837	
	National	DM937	
SN15838	Fairchild	9135	
	Motorola	MC835	
SN15844	Fairchild	944	
	Hitachi	HD2209	
	Motorola	MC844	
	National	DM944	
SN15845	Fairchild	945	
	Hitachi	HD2205	
	Motorola	MC845	
	National	DM945	
SN15846	Fairchild	946	
	Hitachi	HD2203	
	Motorola	MC846	
	National	DM946	
SN15848	Fairchild	948	
	Motorola	MC848	
	National	DM948	
SN15849	Fairchild	949	
	Motorola	MC849	
	National	DM949	
SN15850	Fairchild	950	
	Motorola	MC850	
SN15851	Fairchild	951	
	Motorola	MC851	
SN15857	Fairchild	9157	
	Motorola	MC857	
	National	DM957	
SN15858	Fairchild	9158	
	Motorola	MC858	
	National	DM958	
SN15861	Fairchild	961	
	Motorola	MC861	
	National	DM961	
SN15862	Fairchild	962	
	Hitachi	HD2207	
	Motorola	MC862	
	National	DM962	
SN15863	Fairchild	963	
	Motorola	MC863	
	National	DM963	
SN159093	Fairchild	9093	
	Motorola	MC953	
	Raytheon	RM993	
SN159094	Fairchild	9094	
	Motorola	MC956	
	Raytheon	RM994	
SN159097	Fairchild	9097	
	Motorola	MC955	
	Raytheon	RM997	
SN159099	Fairchild	9099	
	Motorola	MC952	
	Raytheon	RM999	
SN15930	Fairchild	930	
	Motorola	MC930	
	Raytheon	RM930	
SN15931	Fairchild	931	
	Motorola	MC931	
	Raytheon	RM931	
SN15932	Fairchild	932	
	Motorola	MC932	
	Raytheon	RM932	
SN15933	Fairchild	933	
	Motorola	MC933	
	Raytheon	RM933	
SN15934	Motorola	MC934	
	Raytheon	RM934	
SN15935	Fairchild	935	
	Motorola	MC940	
	Raytheon	RM935	
SN15936	Fairchild	936	
	Motorola	MC936	
	Raytheon	RM936	
SN15937	Fairchild	937	
	Motorola	MC937	
	Raytheon	RM937	
SN15938	Fairchild	9135	
	Motorola	MC935	
SN15944	Fairchild	944	
	Motorola	MC944	

♦ Discontinued

The manufacturers report their devices can be used as direct replacements.
Performance details often differ, so compare the specifications considering your requirements.

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Manufacturer Device	Replacement Source	Device	IC Master Page
SN15944	Raytheon	RM944	
SN15945	Fairchild	945	
	Motorola	MC945	
	Raytheon	RM945	
SN15946	Fairchild	946	
	Motorola	MC946	
	Raytheon	RM946	
SN15948	Fairchild	949	
	Motorola	MC948	
	Raytheon	RM948	
SN15949	Fairchild	949	
	Motorola	MC949	
	Raytheon	RM949	
SN15950	Fairchild	950	
	Motorola	MC950	
	Raytheon	RM950	
SN15951	Fairchild	951	
	Motorola	MC951	
	Raytheon	RM951	
SN15957	Fairchild	9157	
	Motorola	MC957	
SN15958	Fairchild	9158	
	Motorola	MC958	
SN15961	Fairchild	961	
	Motorola	MC961	
	Raytheon	RM961	
SN15962	Fairchild	962	
	Motorola	MC962	
	Raytheon	RM962	
SN15963	Fairchild	963	
	Motorola	MC963	
	Raytheon	RM963	
SN29000	Fairchild	9000	
SN29001	Fairchild	9001	
SN29002	National	DM9002	
SN29003	National	DM9003	
SN29004	National	DM9004	
SN29005	National	DM9005	
SN29006	National	DM9006	
SN29008	National	DM9008	
SN29009	National	DM9009	
SN29012	National	DM9012	
SN29016	National	DM9016	
SN29024	National	DM8024	
SN29300	AMD	9300	
	Fairchild	9300	
	National	DM8300	
	Raytheon	RM9300	
SN29301	AMD	9301	
	Fairchild	9301	
	National	DM8301	
		DM9301	
SN29308	AMD	9308	
	Fairchild	9308	
	Raytheon	RC9308	
		RM9308	
SN29309	AMD	9309	
	Fairchild	9309	
	National	DM8309	
SN29310	AMD	9310	
	Fairchild	9310	
	National	DM8310	
	Raytheon	RM9310	
SN29311	AMD	9311	
	Fairchild	9311	
	National	DM8311	
	Raytheon	RM9311	
SN29312	AMD	9312	
	Fairchild	9312	
	National	DM8312	
	Raytheon	RC9312	
		RM9312	
SN29316	AMD	9316	
	Fairchild	9316	
	National	DM8316	
	Raytheon	RM9316	
SN29318	AMD	9318	
	Fairchild	9318	
	National	DM8318	
SN29322	AMD	9322	
	Fairchild	9322	
	National	DM8322	
SN29334	Fairchild	9334	
SN29334	National	DM8334	
SN29601	AMD	9601	
	Fairchild	9601	
	Motorola	MC9601	
	National	DM8601	
	Raytheon	RF9601	
SN29602	National	DM8602	
	Raytheon	RM9322	
SN39000	Fairchild	9000	
SN39001	Fairchild	9001	
SN39024	National	DM9024	
SN39300	Fairchild	9300	
	National	DM9300	
SN39301	Fairchild	9301	
	National	DM9301	
SN39308	Fairchild	9308	
SN39309	Fairchild	9309	
	National	DM9309	
SN39310	Fairchild	9310	
	National	DM9310	
SN39311	Fairchild	9311	
	National	DM9311	
SN39312	Fairchild	9312	
	National	DM9312	
SN39316	Fairchild	9316	
	National	DM9316	
SN39318	Fairchild	9318	
	National	DM9318	
SN39322	Fairchild	9322	
	National	DM9322	
SN39334	Fairchild	9334	
	National	DM9334	
SN39601	Fairchild	9601	
	National	DM9601	
SN39602	Fairchild	9602	
	National	DM9602	
SN4LS160A	Fairchild	74LS160	
♦SN52L022	TI	TL022M	
♦SN52L044	TI	TL044M	
♦SN52101	TI	LM101	
SN52104	TI	LM104	
♦SN52105	TI	LM105	
♦SN52106	TI	LM106	
♦SN52107	TI	LM107	
♦SN52108	AMD	LM108	
	Intersil	LM108	
	Motorola	LM108	
	National	**LM108**	**1035**
	Raytheon	LM108	
	RCA	CA108	
	Silicon G	SG108	
♦SN52109	TI	LM109	
SN52110	AMD	LM110	
	Intersil	LM110	
	Motorola	LM110	
	National	LM110	
	Silicon G	SG110	
♦SN52111	TI	LM111	
♦SN52118	TI	LM118	
SN52197	Signetics	S8291	
♦SN52506	TI	TL506	
♦SN52510	TI	TL510	
♦SN52514	TI	TL514	
♦SN52555	TI	SE555	
♦SN52558	TI	MC1558	
♦SN52702	TI	TL702	
♦SN52702A	TI	μA702	
♦SN52709	TI	μA709	
♦SN52710	TI	TL710	
♦SN52711	TI	μA711	
♦SN52723	TI	μA723	
♦SN52733	TI	μA733	
SN52741	Sprague	ULS-2151	
♦SN52741	TI	μA741	
♦SN52747	TI	μA747	
♦SN52748	TI	μA748	
♦SN52771	Signetics	MC1556	
♦SN52777	TI	μA777	
♦SN52810	TI	TL810	
♦SN52811	TI	TL811	
♦SN52820	TI	TL820	
SN54H00	Fairchild	54H00	
	National	DM54H00	
	Raytheon	54H00	
	Signetics	54H00	
SN54H01	Fairchild	54H01	
SN54H01	National	DM54H01	
	Raytheon	54H01	
	Signetics	54H01	
SN54H04	Fairchild	54H04	
	National	DM54H04	
	Raytheon	54H04	
	Signetics	54H04	
SN54H05	Fairchild	54H05	
	National	DM54H05	
	Raytheon	54H05	
	Signetics	54H05	
SN54H10	Fairchild	54H10	
	National	DM54H10	
	Raytheon	54H10	
	Signetics	54H10	
SN54H101	Fairchild	54H101	
	Signetics	54H101	
SN54H102	Fairchild	54H102	
	Signetics	54H102	
SN54H103	Fairchild	54H103	
	National	DM54H103	
	Signetics	54H103	
SN54H106	Fairchild	54H106	
	National	DM54H106	
	Signetics	54H106	
SN54H108	Fairchild	54H108	
	National	DM54H108	
	Signetics	54H108	
SN54H11	Fairchild	54H11	
	National	DM54H11	
	Raytheon	54H11	
	Signetics	54H11	
SN54H15	Fairchild	54H15	
	Raytheon	54H15	
SN54H183	Fairchild	54H183	
SN54H20	Fairchild	54H20	
	National	DM54H20	
	Raytheon	54H20	
	Signetics	54H20	
SN54H21	Fairchild	54H21	
	National	DM54H21	
	Signetics	54H21	
SN54H22	Fairchild	54H22	
	National	DM54H22	
	Raytheon	54H22	
	Signetics	54H22	
SN54H30	Fairchild	54H30	
	National	DM54H30	
	Signetics	54H30	
SN54H40	Fairchild	54H40	
	National	DM54H40	
	Raytheon	54H40	
	Signetics	54H40	
SN54H50	Fairchild	54H50	
	National	DM54H50	
	Signetics	54H50	
SN54H51	Fairchild	54H51	
	National	DM54H51	
	Signetics	54H51	
SN54H52	Fairchild	54H52	
	National	DM54H52	
	Signetics	54H52	
SN54H53	Fairchild	54H53	
	National	DM54H53	
	Signetics	54H53	
SN54H54	Fairchild	54H54	
	National	DM54H54	
	Signetics	54H54	
SN54H55	Fairchild	54H55	
	National	DM54H55	
	Signetics	54H55	
SN54H60	Fairchild	54H60	
	National	DM54H60	
	Signetics	54H60	
SN54H61	Fairchild	54H61	
	National	DM54H61	
	Signetics	54H61	
SN54H62	Fairchild	54H62	
	National	DM54H62	
	Signetics	54H62	
SN54H71	Fairchild	54H71	
	National	DM54H71	
	Signetics	54H71	
SN54H72	Fairchild	54H72	
		54H73	
	National	DM54H72	
SN54H72	Signetics	54H72	
SN54H73	Fairchild	54H73	
	National	DM54H73	
	Signetics	54H73	
SN54H74	Fairchild	54H74	
	National	DM54H74	
	Raytheon	54H74	
	Signetics	54H74	
SN54H76	Fairchild	54H76	
	National	DM54H76	
	Signetics	54H76	
SN54H78	Fairchild	54H78	
	National	DM54H78	
SN54H87	Fairchild	54H87	
SN54LS00	Fairchild	54LS00	
	Motorola	SN54LS00	
	National	DM54LS00	
	Raytheon	54LS00	
	Signetics	54LS00	
SN54LS01	Motorola	SN54LS01	
	National	DM54LS01	
	Raytheon	54LS01	
	Signetics	54LS01	
SN54LS02	Fairchild	54LS02	
	Motorola	SN54LS02	
	National	DM54LS02	
	Raytheon	54LS02	
	Signetics	54LS02	
SN54LS03	Fairchild	54LS03	
	Motorola	SN54LS03	
	National	DM54LS03	
	Raytheon	54LS03	
	Signetics	54LS03	
SN54LS04	Fairchild	54LS04	
	Motorola	SN54LS04	
	National	DM54LS04	
	Raytheon	54LS04	
	Signetics	54LS04	
SN54LS05	Fairchild	54LS05	
	Motorola	SN54LS05	
	National	DM54LS05	
	Raytheon	54LS05	
	Signetics	54LS05	
SN54LS08	Fairchild	54LS08	
	Motorola	SN54LS08	
	National	DM54LS08	
	Raytheon	54LS08	
	Signetics	54LS08	
SN54LS09	Fairchild	54LS09	
	Motorola	SN54LS09	
	National	DM54LS09	
	Raytheon	54LS09	
	Signetics	54LS09	
SN54LS10	Fairchild	54LS10	
	Motorola	SN54LS10	
	National	DM54LS10	
	Raytheon	54LS10	
	Signetics	54LS10	
SN54LS107A	Fairchild	54LS107	
	Motorola	SN54LS107A	
	National	DM54LS107	
	Raytheon	54LS107	
	Signetics	54LS107	
SN54LS109A	Fairchild	54LS109	
	Motorola	SN54LS109A	
	National	DM54LS109	
	Raytheon	54LS109	
	Signetics	54LS109	
SN54LS11	Fairchild	54LS11	
	Motorola	SN54LS11	
	National	DM54LS11	
	Raytheon	54LS11	
	Signetics	54LS11	
SN54LS112A	Fairchild	54LS112	
	Motorola	SN54LS112A	
	National	DM54LS112	
	Raytheon	54LS112	
	Signetics	54LS112	
SN54LS113A	Fairchild	54LS113	
	Motorola	SN54LS113A	
	National	DM54LS113	
	Raytheon	54LS113	
	Signetics	54LS113	
SN54LS114A	Fairchild	54LS114	
	Motorola	SN54LS114A	
	National	DM54LS114	

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Bold face device numbers indicate manufacturers data is provided in the IC Master on the pages noted.

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Manufacturer Device	Replacement Source	Device	IC Master Page
SN54LS114A	Raytheon	54LS114	
	Signetics	54LS114	
SN54LS12	Motorola	SN54LS12	
	National	DM54LS12	
	Raytheon	54LS12	
	Signetics	54LS12	
SN54LS122	Motorola	SN54LS122	
	National	DM54LS122	
	Raytheon	54LS122	
SN54LS123	AMD	SN54LS123	
	Motorola	SN54LS123	
	National	DM54LS123	
	Raytheon	54LS123	
SN54LS125A	Fairchild	54LS125	
	Motorola	SN54LS125A	
	National	DM54LS125	
	Raytheon	54LS125	
	Signetics	54LS125	
SN54LS126A	Fairchild	54LS126	
	Motorola	SN54LS126A	
	National	DM54LS126	
	Raytheon	54LS126	
	Signetics	54LS126	
SN54LS13	Motorola	SN54LS13	
	National	DM54LS13	
	Raytheon	54LS13	
	Signetics	54LS13	
SN54LS132	Fairchild	54LS132	
	Motorola	SN54LS132	
	National	DM54LS132	
	Signetics	54LS132	
SN54LS136	Fairchild	54LS136	
	Motorola	SN54LS136	
	Raytheon	54LS136	
	Signetics	54LS136	
SN54LS138	AMD	SN54LS138	
	Fairchild	54LS138	
	Motorola	SN54LS138	
	National	DM54LS138	
	Raytheon	54LS138	
	Signetics	54LS138	
SN54LS139	AMD	SN54LS139	
	Fairchild	54LS139	
	Motorola	SN54LS139	
	National	DM54LS139	
	Raytheon	54LS139	
	Signetics	54LS139	
		74LS139	
SN54LS14	Fairchild	54LS14	
	Motorola	SN54LS14	
	National	DM54LS14	
	Raytheon	54LS14	
	Signetics	54LS14	
SN54LS148	AMD	SN54LS148	
SN54LS15	Fairchild	54LS15	
	Motorola	SN54LS15	
	National	DM54LS15	
	Raytheon	54LS15	
	Signetics	54LS15	
SN54LS151	AMD	SN54LS151	
	Fairchild	54LS151	
	Motorola	SN54LS151	
	National	DM54LS151	
	Raytheon	54LS151	
	Signetics	54LS151	
SN54LS152	Fairchild	54LS152	
	Motorola	SN54LS152	
	Raytheon	54LS152	
SN54LS153	AMD	SN54LS153	
	Fairchild	54LS153	
	Motorola	SN54LS153	
	National	DM54LS153	
	Raytheon	54LS153	
	Signetics	54LS153	
SN54LS155	Fairchild	54LS155	
	Motorola	SN54LS155	
	National	DM54LS155	
	Raytheon	54LS155	
		74LS155	
SN54LS156	Fairchild	54LS156	
	Motorola	SN54LS156	
	National	DM54LS156	
	Raytheon	54LS156	
SN54LS157	AMD	SN54LS157	
	Fairchild	54LS157	
	Motorola	SN54LS157	
	National	DM54LS157	
	Raytheon	54LS157	
	Signetics	54LS157	
SN54LS158	AMD	SN54LS158	
	Fairchild	54LS158	
	Motorola	SN54LS158	
	National	DM54LS158	
	Raytheon	54LS158	
	Signetics	54LS158	
SN54LS160A	AMD	SN54LS160	
	Fairchild	54LS160	
	Motorola	SN54LS160A	
	National	DM54LS160	
	Raytheon	54LS160	
SN54LS161A	AMD	SN54LS161	
	Fairchild	54LS161	
	Motorola	SN54LS161A	
	National	DM54LS161	
	Raytheon	54LS161	
	Signetics	54LS161	
SN54LS162A	AMD	SN54LS162	
	Fairchild	54LS162	
	Motorola	SN54LS162A	
	National	DM54LS162	
	Raytheon	54LS162	
SN54LS163A	AMD	SN54LS163	
	Fairchild	54LS163	
	Motorola	SN54LS163A	
	National	DM54LS163	
	Raytheon	54LS163	
	Signetics	54LS163	
SN54LS164	AMD	SN54LS164	
	Fairchild	54LS164	
	National	DM54LS164	
	Raytheon	54LS164	
	Signetics	54LS164	
SN54LS164A	Motorola	SN54LS164A	
SN54LS165	Fairchild	54LS165	
	Motorola	SN54LS165	
SN54LS166	Motorola	SN54LS166	
SN54LS168	AMD	SN54LS168	
	Fairchild	54LS168	
	Motorola	SN54LS168	
	National	DM54LS168	
SN54LS169	AMD	SN54LS169	
	Fairchild	54LS169	
	Motorola	SN54LS169	
	National	DM54LS169	
SN54LS170	AMD	SN54LS170	
	Fairchild	54LS170	
	Motorola	SN54LS170	
	National	DM54LS170	
	Raytheon	54LS170	
	Signetics	54LS170	
SN54LS173A	Fairchild	54LS173	
	Motorola	SN54LS173	
	National	DM54LS173	
	Signetics	54LS173	
SN54LS174	AMD	SN54LS174	
	Fairchild	54LS174	
	National	DM54LS174	
	Raytheon	54LS174	
	Signetics	54LS174	
SN54LS175	AMD	SN54LS175	
	Fairchild	54LS175	
	Motorola	SN54LS175	
	National	DM54LS175	
	Raytheon	54LS175	
	Signetics	54LS175	
SN54LS181	AMD	SN54LS181	
	Fairchild	54LS181	
	Motorola	SN54LS181	
	Raytheon	54LS181	
	Signetics	54LS181	
SN54LS189	Motorola	SN54LS189	
SN54LS190	AMD	SN54LS190	
	Fairchild	54LS190	
	Motorola	SN54LS190	
	National	DM54LS190	
	Raytheon	54LS190	
	Signetics	54LS190	
SN54LS191	AMD	SN54LS191	
	Fairchild	54LS191	
SN54LS191	Motorola	SN54LS191	
	National	DM54LS191	
	Raytheon	54LS191	
	Signetics	54LS191	
SN54LS192	AMD	SN54LS192	
	Fairchild	54LS192	
	Motorola	SN54LS192	
	National	DM54LS192	
	Raytheon	54LS192	
	Signetics	54LS192	
SN54LS193	AMD	SN54LS193	
	Fairchild	54LS193	
	Motorola	SN54LS193	
	National	DM54LS193	
	Raytheon	54LS193	
	Signetics	54LS193	
SN54LS194A	AMD	SN54LS194A	
	Fairchild	54LS194	
	Motorola	SN54LS194A	
	Raytheon	54LS194A	
SN54LS195A	AMD	SN54LS195A	
	Fairchild	54LS195	
	Motorola	SN54LS195A	
	Raytheon	54LS195A	
	Signetics	54LS195A	
SN54LS196	Fairchild	54LS196	
	Motorola	SN54LS196	
	National	DM54LS196	
	Raytheon	54LS196	
SN54LS197	Fairchild	54LS197	
	Motorola	SN54LS197	
	National	DM54LS197	
	Raytheon	54LS197	
SN54LS20	Fairchild	54LS20	
	Motorola	SN54LS20	
	National	DM54LS20	
	Raytheon	54LS20	
	Signetics	54LS20	
SN54LS21	Fairchild	54LS21	
	Motorola	SN54LS21	
	National	DM54LS21	
	Raytheon	54LS21	
	Signetics	54LS21	
SN54LS22	Fairchild	54LS22	
	Motorola	SN54LS22	
	National	DM54LS22	
	Raytheon	54LS22	
	Signetics	54LS22	
SN54LS221	Motorola	SN54LS221	
	National	DM54LS221	
	Raytheon	54LS221	
	Signetics	54LS221	
SN54LS240	AMD	SN54LS240	
	Fairchild	54LS240	
	MMI	**54LS240**	**768**
	Motorola	SN54LS240	
	Raytheon	**54LS240**	**522**
SN54LS241	AMD	SN54LS241	
	Fairchild	54LS241	
	MMI	**54LS241**	**768**
	Motorola	SN54LS241	
	Raytheon	**54LS241**	**525**
SN54LS242	AMD	SN54LS242	
	Motorola	SN54LS242	
	Raytheon	**54LS242**	**528**
SN54LS243	AMD	SN54LS243	
	Motorola	SN54LS243	
	Raytheon	**54LS243**	**528**
SN54LS244	AMD	SN54LS244	
	MMI	**54LS244**	**768**
	Motorola	SN54LS244	
	Raytheon	**54LS244**	**525**
SN54LS245	**MMI**	**54LS245**	**774**
	Motorola	SN54LS245	
SN54LS247	Motorola	SN54LS247	
	National	DM54LS247	
SN54LS248	Motorola	SN54LS248	
	National	DM54LS248	
SN54LS249	Motorola	SN54LS249	
	National	DM54LS249	
SN54LS251	AMD	SN54LS251	
	Fairchild	54LS251	
	Motorola	SN54LS251	
	Raytheon	54LS251	
	Signetics	54LS251	
SN54LS253	AMD	SN54LS253	
SN54LS253	Fairchild	54LS253	
	Motorola	SN54LS253	
	National	DM54LS253	
	Raytheon	54LS253	
	Signetics	54LS253	
SN54LS257A	AMD	SN54LS257	
	Fairchild	54LS257	
	Motorola	SN54LS257A	
	National	DM54LS257	
	Raytheon	54LS257	
	Signetics	54LS257	
SN54LS258A	AMD	SN54LS258	
	Fairchild	54LS258	
	Motorola	SN54LS258A	
	Raytheon	54LS258	
	Signetics	54LS258	
SN54LS259	Fairchild	54LS259	
	Motorola	SN54LS259	
SN54LS26	Fairchild	54LS26	
	Motorola	SN54LS26	
	National	DM54LS26	
	Raytheon	54LS26	
	Signetics	54LS26	
SN54LS261	Raytheon	54LS261	
	Signetics	54LS261	
SN54LS266	Fairchild	54LS266	
	Motorola	SN54LS266	
	Raytheon	54LS266	
	Signetics	54LS266	
SN54LS27	Fairchild	54LS27	
	Motorola	SN54LS27	
	National	DM54LS27	
	Raytheon	54LS27	
	Signetics	54LS27	
SN54LS273	AMD	SN54LS273	
	MMI	**54LS273**	**509**
	Raytheon	**54LS273**	**531**
SN54LS279	Fairchild	54LS279	
	Motorola	SN54LS279	
	National	DM54LS279	
	Raytheon	74LS279	
	Signetics	54LS279	
SN54LS28	Fairchild	54LS28	
	Motorola	SN54LS28	
	Raytheon	54LS28	
	Signetics	54LS28	
SN54LS280	Fairchild	54LS280	
SN54LS281	AMD	SN54LS281	
SN54LS283	Fairchild	54LS283	
	MMI	54LS283	
	Motorola	SN54LS283	
	National	DM54LS283	
	Raytheon	54LS283	
SN54LS289	Motorola	SN54LS289	
SN54LS290	Fairchild	54LS290	
	Motorola	SN54LS290	
	Signetics	54LS290	
SN54LS293	Fairchild	54LS293	
	Motorola	SN54LS293	
	Signetics	54LS293	
SN54LS295B	Fairchild	54LS295	
	Motorola	SN54LS295A	
	Raytheon	54LS295A	
	Signetics	54LS295A	
SN54LS298	Fairchild	54LS298	
	Motorola	SN54LS298	
	Raytheon	54LS298	
SN54LS299	AMD	SN54LS299	
	Fairchild	54LS299	
	MMI	54LS299	
	Raytheon	**54LS299**	**533**
SN54LS30	Fairchild	54LS30	
	Motorola	SN54LS30	
	National	DM54LS30	
	Raytheon	54LS30	
	Signetics	54LS30	
SN54LS32	Fairchild	54LS32	
	Motorola	SN54LS32	
	National	DM54LS32	
	Raytheon	54LS32	
	Signetics	54LS32	
SN54LS322	MMI	54LS322	
	Motorola	SN54LS322	
	Raytheon	**54LS322**	**537**
SN54LS322A	AMD	AM25LS22	
		SN54LS322	

♦ Discontinued

The manufacturers report their devices can be used as direct replacements.
Performance details often differ, so compare the specifications considering your requirements.

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Manufacturer Device	Replacement Source	Device	IC Master Page
SN54LS322A	Raytheon	54LS322A	
SN54LS323	MMI	54LS323	
	Motorola	SN54LS323	
	Raytheon	**54LS323**	**540**
SN54LS323A	AMD	AM25LS23	
SN54LS33	Fairchild	54LS33	
	Motorola	SN54LS33	
	Raytheon	54LS33	
	Signetics	54LS33	
SN54LS352	Fairchild	54LS352	
	Motorola	SN54LS352	
	National	DM54LS352	
SN54LS353	Fairchild	54LS353	
	Motorola	SN54LS353	
	National	DM54LS353	
SN54LS363	MMI	54LS363	
SN54LS365A	Fairchild	54LS365	
	Motorola	SN54LS365A	
	Raytheon	54LS365	
	Signetics	54LS365A	
SN54LS366A	Fairchild	54LS366	
	Motorola	SN54LS366A	
	Raytheon	54LS366	
	Signetics	54LS366	
SN54LS367A	Fairchild	54LS367	
	Motorola	SN54LS367A	
	Raytheon	54LS367	
	Signetics	54LS367A	
SN54LS368A	Fairchild	54LS368	
	Motorola	SN54LS368A	
	Signetics	54LS368A	
SN54LS37	Fairchild	54LS37	
	Motorola	SN54LS37	
	National	DM54LS37	
	Raytheon	54LS37	
	Signetics	54LS37	
SN54LS373	AMD	SN54LS373	
	MMI	**54LS373**	**505**
	Motorola	SN54LS373	
	Raytheon	**54LS373**	**543**
SN54LS374	AMD	SN54LS374	
	MMI	**54LS374**	**505**
	Raytheon	**54LS374**	**543**
SN54LS375	Motorola	SN54LS375	
	Signetics	54LS375	
SN54LS377	AMD	SN54LS377	
	MMI	**54LS377**	**509**
	Raytheon	**54LS377**	**549**
SN54LS378	AMD	SN54LS378	
	Motorola	SN54LS378	
SN54LS379	AMD	AM25LS08	
		SN54LS379	
	Motorola	SN54LS379	
SN54LS38	Fairchild	54LS38	
	Motorola	SN54LS38	
	National	DM54LS38	
	Raytheon	54LS38	
	Signetics	54LS38	
SN54LS381	AMD	SN54LS381	
SN54LS384	AMD	AM25LS14	
		SN54LS384	
	Motorola	SN54LS384	
	Raytheon	**54LS244**	**525**
		54LS384	**551**
SN54LS385	AMD	AM25LS15	
		SN54LS385	
	Motorola	SN54LS385	
	Raytheon	**54LS385**	**554**
SN54LS386	Motorola	SN54LS386	
	Raytheon	54LS386	
	Signetics	54LS386	
SN54LS390	Fairchild	54LS390	
	Motorola	SN54LS390	
SN54LS393	Fairchild	54LS393	
	Motorola	SN54LS393	
SN54LS395A	Fairchild	54LS395	
	Motorola	SN54LS395A	
	National	DM54LS395	
	Raytheon	54LS395	
	Signetics	54LS395	
SN54LS399	AMD	AM25LS09	
		SN54LS399	
	Motorola	SN54LS399	
SN54LS40	Fairchild	54LS40	
	Motorola	SN54LS40	
	National	DM54LS40	
	Raytheon	54LS40	
	Signetics	54LS40	
SN54LS42	Fairchild	54LS42	
	Motorola	SN54LS42	
	National	DM54LS42	
	Raytheon	54LS42	
	Signetics	54LS42	
SN54LS424	AMD	SN54LS424	
SN54LS47	Motorola	SN54LS47	
SN54LS48	Motorola	SN54LS48	
SN54LS49	Motorola	SN54LS49	
SN54LS490	Fairchild	54LS490	
	Motorola	SN54LS490	
SN54LS51	Fairchild	54LS51	
	Motorola	SN54LS51	
	National	DM54LS51	
	Raytheon	54LS51	
	Signetics	54LS51	
SN54LS54	Fairchild	54LS54	
	Motorola	SN54LS54	
	National	DM54LS54	
	Raytheon	54LS54	
	Signetics	54LS54	
SN54LS55	Fairchild	54LS55	
	Motorola	SN54LS55	
	National	DM54LS55	
	Raytheon	54LS55	
	Signetics	54LS55	
SN54LS640	Motorola	SN54LS640	
SN54LS641	Motorola	SN54LS641	
SN54LS642	Motorola	SN54LS642	
SN54LS645	Motorola	SN54LS645	
SN54LS670	Fairchild	54LS670	
	Motorola	54LS670	
	National	DM54LS670	
	Raytheon	54LS670	
	Signetics	54LS670	
SN54LS73A	Fairchild	54LS73	
	Motorola	SN54LS73A	
	National	DM54LS73	
	Raytheon	54LS73	
	Signetics	54LS73	
SN54LS74A	Fairchild	54LS74	
	Motorola	SN54LS74A	
	National	DM54LS74	
	Raytheon	54LS74	
	Signetics	54LS74	
SN54LS75	Motorola	SN54LS75	
	National	DM54LS75	
	Raytheon	54LS75	
	Signetics	54LS75	
SN54LS76A	Motorola	SN54LS76A	
	National	DM54LS76	
	Raytheon	54LS76	
	Signetics	54LS76	
SN54LS77	Fairchild	54LS77	
	Motorola	SN54LS77	
	Raytheon	54LS77	
SN54LS78A	Motorola	SN54LS78A	
	National	DM54LS78	
	Raytheon	54LS78	
	Signetics	54LS78	
SN54LS83A	Fairchild	54LS83	
	Motorola	SN54LS83A	
	National	DM54LS83	
	Raytheon	54LS83A	
SN54LS85	Fairchild	54LS85	
	Motorola	SN54LS85	
	National	DM54LS85	
	Raytheon	54LS85	
	Signetics	54LS85	
SN54LS86	Fairchild	54LS86	
	Motorola	SN54LS86	
	Raytheon	54LS86	
	Signetics	54LS86	
SN54LS90	Fairchild	54LS90	
	Motorola	SN54LS90	
	Raytheon	54LS90	
	Signetics	54LS90	
SN54LS91	Raytheon	54LS91	
SN54LS92	Motorola	SN54LS92	
	Raytheon	54LS92	
	Signetics	S54LS92	
SN54LS92	Signetics	54LS92	
SN54LS93	Fairchild	54LS93	
	Motorola	SN54LS93	
	Raytheon	54LS93	
	Signetics	54LS93	
SN54LS95B	Fairchild	54LS95	
		54LS95B	
	Motorola	SN54LS95B	
	Raytheon	54LS95B	
SN54LS96	Signetics	54LS96	
SN54L00	National	DM54L00	
SN54L01	National	DM54L01	
SN54L02	National	DM54L02	
SN54L03	National	DM54L03	
SN54L04	National	DM54L04	
SN54L10	National	DM54L10	
SN54L123	National	DM54L123	
SN54L154	National	DM54L154A	
SN54L157	National	DM54L157A	
SN54L164	National	DM54L164	
SN54L192	National	DM54L192	
SN54L193	National	DM54L193	
SN54L20	National	DM54L20	
SN54L30	National	DM54L30	
SN54L368A	Raytheon	54LS368	
SN54L42A	National	DM54L42A	
SN54L51	National	DM54L51	
SN54L54	National	DM54L54	
SN54L55	National	DM54L55	
SN54L71	National	DM54L71	
SN54L72	National	DM54L72	
SN54L73	National	DM54L73	
SN54L74	National	DM54L74	
SN54L75	National	DM54L75	
SN54L78	National	DM54L78	
SN54L85	National	DM54L85	
SN54L86	National	DM54L86	
SN54L90	National	DM54L90	
SN54L91	National	DM54L91	
SN54L93	National	DM54L93	
SN54L95	National	DM54L95	
SN54L98	National	DM54L98	
SN54S00	Fairchild	54S00	
		9S00	
SN54S02	Fairchild	54S02	
	Signetics	54S02	
SN54S03	Fairchild	54S03	
SN54S04	Fairchild	54S04	
		9504A	
	Signetics	54S04	
SN54S05	Fairchild	54S05	
		9505A	
	Signetics	54S05	
SN54S08	Fairchild	54S08	
	Signetics	54S08	
SN54S09	Fairchild	54S09	
	Signetics	54S09	
SN54S10	Fairchild	54S10	
SN54S11	Fairchild	54S11	
	Signetics	54S11	
SN54S112	Fairchild	54S112	
	Motorola	SN54S112	
SN54S113	Fairchild	54S113	
	Motorola	SN54S113	
SN54S114	Fairchild	54S114	
SN54S13	Fairchild	54LS13	
SN54S132	Fairchild	54S132	
SN54S133	Fairchild	54S133	
SN54S134	Fairchild	54S134	
SN54S135	Fairchild	54S135	
SN54S138	AMD	SN54S138	
	Fairchild	54S138	
SN54S139	AMD	SN54S139	
	Fairchild	54S139	
	Signetics	54S139	
SN54S140	AMD	SN54S140	
	Fairchild	54S140	
	National	DM54S140	
	Signetics	54S140	
SN54S15	Fairchild	54S15	
	Signetics	54S15	
SN54S151	AMD	SN54S151	
	Fairchild	54S151	
	Signetics	54S151	
SN54S153	AMD	SN54S153	
	Fairchild	54S153	
SN54S153	Signetics	54S153	
SN54S157	AMD	SN54S157	
	Fairchild	54S157	
	Signetics	54S157	
SN54S158	AMD	SN54S158	
	Fairchild	54S158	
	Signetics	54S158	
SN54S174	AMD	SN54S174	
	Fairchild	54S174	
SN54S175	AMD	SN54S175	
	Fairchild	54S175	
SN54S181	AMD	SN54S181	
	Fairchild	54S181	
		93S41	
	Signetics	54S181	
SN54S182	Fairchild	93S42	
	MMI	54S182	
SN54S188	AMD	AM27S18	
	Harris	**HM7602**	**1284**
	MMI	5330	
		5330-1	**1449**
	National	DM59S188	
	Supertex	**MM74S188**	**1704**
SN54S189	AMD	AM27S03	
		SN54S189	
	National	DM54S189	
SN54S194	AMD	SN54S194	
	Fairchild	54S194	
SN54S195	AMD	SN54S195	
	Fairchild	93S00	
SN54S20	Fairchild	54S20	
SN54S200	**Fairchild**	**93421**	**1252**
♦SN54S200	MMI	5531	
	National	DM54S200	
	Raytheon	RM5340	
	Signetics	**54S200**	**1678**
	TI	SN54S201	
SN54S201	National	DM54S200	
SN54S206	**MMI**	**5205-1**	**1466**
	National	DM54S206	
	Raytheon	RM5330	
	TI	SN74S301	
SN54S214	**Fairchild**	**93425**	**1240**
SN54S22	Fairchild	54S22	
	National	DM54S22	
	Signetics	54S22	
SN54S240	AMD	SN54S240	
	MMI	**54S240**	**768**
	Raytheon	54S240	
SN54S241	AMD	SN54S241	
	MMI	**54S241**	**768**
		54S242	
	Raytheon	54S241	
SN54S244	**MMI**	**54S244**	**768**
SN54S251	AMD	SN54S251	
	Fairchild	54S251	
	Signetics	54S251	
SN54S257	AMD	SN54S257	
SN54S258	AMD	SN54S258	
	Fairchild	54S258	
	Signetics	54S258	
SN54S270	**MMI**	**5205-1**	**1466**
SN54S283	MMI	54S283	
SN54S287	AMD	AM27S21	
	Fairchild	**93427**	**1258**
	Harris	**HM7611**	
			1284,1292
		HM7611A	
	MMI	**5301-1**	**1449**
	National	DM54S287	
	Raytheon	**29661**	**1664**
SN54S288	AMD	AM27S19	
	Harris	**HM7603**	**1284**
	MMI	**5331-1**	**1449**
	National	DM545288	
		DM7578	
	Supertex	**MM74S288**	**1704**
SN54S289	AMD	AM27S02	
		SN54S289	
	National	DM54S289	
SN54S30	Fairchild	54S30	
SN54S301	Fairchild	93411	
	National	DM54S206	
SN54S314	Fairchild	93415	1240
SN54S32	Fairchild	54S32	
	Signetics	54S32	

♦ Discontinued

Bold face device numbers indicate manufacturers data is provided in the IC Master on the pages noted.

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Manufacturer Device	Replacement Source	Device	IC Master Page
SN54S37	Signetics	54S37	
SN54S370	**MMI**	**5206-1**	**1466**
SN54S373	**MMI**	**54S373**	**505**
SN54S374	**MMI**	**54S374**	**505**
SN54S381	MMI	54S381	
SN54S387	AMD	AM27S20	
	Fairchild	**93417**	**1258**
	Harris	**HM7610**	
			1284,1292
		HM7610A	
	MMI	**5300-1**	**1449**
	National	DM54S387	
	Raytheon	**29660**	**1664**
	Signetics	**S82S126**	**1680**
SN54S40	Fairchild	54S40	
SN54S412	AMD	SN54S412	
SN54S470	**MMI**	**5308-1**	**1449**
	National	DM59S470	
	Raytheon	**29600**	**1652**
SN54S471	**MMI**	**5309-1**	**1449**
	National	DM54S471	
	Raytheon	**29601**	**1652**
SN54S472	**MMI**	**5349-1**	**1449**
	National	DM54S472	
	Raytheon	**29621**	**1656**
SN54S473	**MMI**	**5348-1**	**1449**
	National	DM54S473	
	Raytheon	**29620**	**1656**
SN54S474	**Fairchild**	**93448**	**1262**
	MMI	**5341-1**	**1449**
	National	DM77S296	
	Raytheon	**29625**	**1658**
SN54S475	**Fairchild**	**93438**	**1262**
		93452	**1264**
	MMI	**5340-1**	**1449**
	National	DM77S295	
	Raytheon	**29624**	**1658**
SN54S476	**Fairchild**	**93453**	**1264**
	MMI	**53S441**	**1453**
	Raytheon	29641	
SN54S477	**MMI**	**53S440**	**1453**
	Raytheon	29640	
SN54S478	**MMI**	**5381-1**	**1449**
SN54S479	**MMI**	**5380-1**	**1449**
SN54S51	Fairchild	54S51	
SN54S64	Fairchild	54S64	
SN54S65	Fairchild	54S65	
		9S65	
SN54S74	Fairchild	54S74	
SN54S85	Signetics	54S85	
SN54S86	Fairchild	54S86	
	Signetics	54S86	
SN5400	Fairchild	5400	
	Motorola	MC5400	
	National	DM5400	
	Signetics	5400	
SN5401	Fairchild	5401	
	Motorola	MC5401	
	National	DM5401	
	Signetics	5401	
SN5402	Fairchild	5402	
	Motorola	MC5402	
	National	DM5402	
	Signetics	5402	
SN5403	Motorola	MC5403	
	National	DM5403	
	Raytheon	5403	
	Signetics	5403	
SN5404	Fairchild	5404	
	Motoroia	MC5404	
	National	DM5404	
	Signetics	5404	
SN5405	Fairchild	5405	
	Motorola	MC5405	
	National	DM5405	
	Signetics	5405	
SN5406	Fairchild	5406	
	Motorola	MC5406	
	National	DM5406	
	Signetics	5406	
SN5407	Fairchild	5407	
	Motorola	MC5407	
	National	DM5407	
SN5407	Signetics	5407	
SN5408	Fairchild	5408	
	Motorola	MC5408	
	National	DM5408	
	Signetics	5408	
SN5409	Fairchild	5409	
	Motorola	MC5409	
	National	DM5409	
	Signetics	5409	
SN5410	Fairchild	5410	
	Motorola	MC5410	
	National	DM5410	
	Signetics	5410	
SN54100	Motorola	MC54100	
	Signetics	54100	
SN54107	AMD	SN54107	
	Fairchild	54107	
		9N107	
	Motorola	MC54107	
	National	DM54107	
	Signetics	54107	
SN54109	Fairchild	9024	
	National	DM54109	
	Signetics	54109	
SN5411	Fairchild	5411	
	National	DM5411	
	Signetics	5411	
SN54116	Fairchild	54116	
	Signetics	54116	
SN5412	Fairchild	5412	
	Signetics	5412	
SN54120	Motorola	MC54120	
SN54121	Fairchild	54121	
		9603	
	Motorola	MC54121	
		MC9603	
	National	DM54121	
	Signetics	54121	
SN54122	Fairchild	54122	
	Motorola	MC54122	
SN54123	AMD	AM26123	
		SN54123	
	Fairchild	54123	
	Motorola	MC54123	
	National	DM54123	
	Signetics	54123	
SN54125	Fairchild	54125	
	National	DM54125	
		DM7093	
	Signetics	54125	
SN54126	Fairchild	54126	
	National	DM54126	
		DM7094	
	Signetics	54126	
SN54128	Signetics	54128	
SN5413	Fairchild	5413	
	Motorola	MC5413	
	National	DM5413	
	Signetics	5413	
SN54132	Fairchild	54132	
	Motorola	MC54132	
	National	DM54132	
	Signetics	54132	
SN5414	Fairchild	5414	
	Motorola	MC5414	
	National	DM5414	
	Signetics	5414	
SN54141	Motorola	MC54141	
	National	DM54141	
	Signetics	54141	
SN54145	Fairchild	54145	
	Motorola	MC54145	
	National	DM54145	
	Signetics	54145	
SN54147	National	DM54147	
	Signetics	54147	
SN54148	Fairchild	9318	
	National	DM54148	
	Signetics	54148	
SN54150	Fairchild	93150	
	Motorola	MC54150	
	National	DM54150	
	Signetics	54150	
♦SN54151	Fairchild	54151	
	Motorola	MC54151	
	National	DM54151	
♦SN54151	Signetics	54151	
	TI	SN54151A	
♦SN54152	Fairchild	54152	
	Motorola	MC54152	
	Signetics	54152	
	TI	SN54152A	
SN54153	AMD	SN54153	
	Fairchild	54153	
	Motorola	MC54153	
	National	DM54153	
	Signetics	54153	
SN54154	AMD	SN54154	
	Fairchild	54154	
		9311	
	Motorola	MC54154	
	National	DM54154	
	Signetics	54154	
SN54155	Fairchild	54155	
	Motorola	MC54155	
	National	DM54155	
	Signetics	54155	
SN54156	Fairchild	54156	
	Motorola	MC54156	
	National	DM54156	
	Signetics	54156	
SN54157	AMD	SN54157	
	Fairchild	54157	
		9322	
	Motorola	MC54157	
	National	DM54157	
		DM9322	
	Signetics	54157	
SN5416	Fairchild	5416	
	Motorola	MC5416	
	National	DM5416	
	Signetics	5416	
SN54160	AMD	SN54160	
	Fairchild	54160	
		9310	
	Motorola	MC54160	
	National	DM54160	
	Signetics	54160	
SN54161	AMD	SN54161	
	Fairchild	54161	
		9316	
	Motorola	MC54161	
	National	DM54161	
	Signetics	54161	
SN54162	AMD	SN54162	
	Fairchild	54162	
	Motorola	MC54162	
	National	DM54162	
	Signetics	54162	
SN54163	AMD	SN54163	
	Fairchild	54163	
	Motorola	MC54163	
	National	DM54163	
	Signetics	54163	
SN54164	AMD	SN54164	
	Fairchild	54164	
	National	DM54164	
		DM7570	
	Signetics	54164	
SN54165	Fairchild	54165	
	Motorola	MC54165	
	National	DM54165	
		DM7590	
	Signetics	54165	
SN54166	Fairchild	54166	
	National	DM54166	
	Signetics	54166	
SN54167	Motorola	MC54167	
SN5417	Fairchild	5417	
	Motorola	MC5417	
	National	DM5417	
	Signetics	5417	
SN54170	Fairchild	54170	
	National	DM54170	
	Signetics	54170	
SN54173	Fairchild	54173	
	National	DM54173	
		DM7551	
SN54174	AMD	SN54174	
		SN74174	
	Fairchild	54174	
	Motorola	MC54174	
SN54174	National	DM54174	
	Signetics	54174	
SN54175	AMD	SN54175	
	Fairchild	54175	
	Motorola	MC54175	
	National	DM54175	
	Signetics	54175	
SN54176	Fairchild	54176	
	Motorola	MC54176	
	National	DM54176	
		DM7280	
	Signetics	S8280	
		54176	
SN54177	Fairchild	54177	
	Motorola	MC54177	
	National	DM54177	
		DM7281	
	Signetics	S8281	
		54177	
SN54178	Fairchild	54178	
	Signetics	S8270	
SN54179	Fairchild	54179	
SN54180	Fairchild	54180	
	Motorola	MC54180	
	National	DM54180	
	Signetics	54180	
SN54181	AMD	SN54181	
		9341	
	Fairchild	54181	
		9341	
	Motorola	MC54181	
	National	DM54181	
	Signetics	54181	
SN54182	AMD	SN54182	
		9342	
	Fairchild	54182	
		9342	
	Motorola	MC54182	
	National	DM54182	
	Signetics	54182	
SN54184	National	DM54184	
SN54185	National	DM54185	
SN54185A	National	DM54185A	
SN54186	**Harris**	**HPROM0512**	**1346**
SN54187	Intersil	IM5603	
	MMI	**5200-1**	**1466**
	National	DM54187	
SN54188	AMD	AM27S18	
	Harris	**HM7602**	**1284**
	MMI	**5330-1**	**1449**
	National	DM7577	
SN54190	Fairchild	54190	
	Motorola	MC54190	
	National	DM54190	
	Signetics	54190	
SN54191	Fairchild	54191	
	Motorola	MC54191	
	National	DM54191	
	Signetics	54191	
SN54192	AMD	SN54192	
		9360	
	Fairchild	54192	
	Motorola	MC54192	
	National	DM54192	
		DM7560	
	Signetics	54192	
SN54193	AMD	SN54193	
		9366	
	Fairchild	54193	
	Motorola	MC54193	
	National	DM54193	
		DM7563	
	Signetics	54193	
SN54194	AMD	SN54194	
	Fairchild	54194	
	Motorola	MC54194	
	National	DM54194	
	Signetics	54194	
SN54195	AMD	SN54195	
	Fairchild	54195	
		9300	
	Motorola	MC54195	
	National	DM54195	
		DM9300	
	Signetics	54195	

♦ Discontinued

The manufacturers report their devices can be used as direct replacements.
Performance details often differ, so compare the specifications considering your requirements.

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Manufacturer Device	Replacement Source	Device	IC Master Page
SN54196	Fairchild	54196	
	Motorola	MC54196	
	National	DM54196	
	Signetics	S8290	
		54196	
SN54197	Fairchild	54197	
	Motorola	MC54197	
	National	DM54197	
	Signetics	54197	
SN54198	Fairchild	54198	
	National	DM54198	
	Signetics	54198	
SN54199	Fairchild	54199	
	National	DM54199	
	Signetics	54199	
SN5420	Fairchild	5420	
	Motorola	MC5420	
	National	DM5420	
	Signetics	S8819	
		5420	
♦SN54200	MMI	5531	
	TI	SN54S201	
SN54206	MMI	5530	
	National	DM54S206	
	TI	SN54S301	
SN5422	Fairchild	5422	
SN54221	AMD	SN54221	
SN5423	Fairchild	5423	
	Motorola	MC5423	
	National	DM5423	
SN5425	Fairchild	5425	
	Motorola	MC5425	
	National	DM5425	
SN54251	National	DM7121	
		SM54251	
SN54259	AMD	SN54259	
SN5426	Fairchild	5426	
	Motorola	MC5426	
	National	DM5426	
	Signetics	S8T18	
		5426	
SN5427	Fairchild	5427	
	Motorola	MC5427	
	National	DM5427	
SN54270	**MMI**	**5205-1**	**1466**
SN54278	Motorola	MC54278	
SN54279	Fairchild	54279	
	Motorola	MC54279	
	Signetics	54279	
SN54283	Fairchild	54283	
SN54284	National	DM7875A	
SN54285	National	DM7875B	
SN54290	Motorola	MC54290	
SN54293	Motorola	MC54293	
SN54298	Fairchild	54298	
	Motorola	MC54298	
	Signetics	54298	
SN5430	Fairchild	5430	
	Motorola	MC5430	
	National	DM5430	
	Signetics	S8808	
		5430	
SN5432	Fairchild	5432	
	National	DM5432	
	Signetics	5432	
SN54365	National	DM7095	
SN54366	National	DM7096	
SN54367	National	DM7097	
SN54368	National	DM7098	
SN5437	Fairchild	5437	
	Motorola	MC5437	
	National	DM5437	
	Signetics	5437	
SN54370	**MMI**	**5206-1**	**1466**
SN5438	Fairchild	5438	
	Motorola	MC5438	
	National	DM5438	
	Signetics	5438	
SN5440	Fairchild	5440	
	Motorola	MC5440	
	National	DM5440	
	Signetics	5440	
♦SN5442	Fairchild	5442	
♦SN5442	Motorola	MC5442	
	National	DM5442	
	Signetics	5442	
	TI	SN5442A	
SN54425	National	DM7093	
SN54426	National	DM7094	
♦SN5443	Fairchild	5443	
	Motorola	MC5443	
	Signetics	5443	
	TI	SN5443A	
♦SN5444	Fairchild	5444	
	Motorola	MC5444	
	Signetics	5444	
	TI	SN5444A	
SN5445	Fairchild	5445	
	Motorola	MC5445	
	National	DM5445	
	Signetics	5445	
♦SN5446	Fairchild	5446	
	Motorola	MC5446	
	National	DM5446	
	Signetics	5446	
	TI	SN5446A	
♦SN5447	Fairchild	5447	
	Motorola	MC5447	
	National	DM5447	
	Signetics	5447	
	TI	SN5447A	
SN5448	Fairchild	5448	
	Motorola	MC5448	
	National	DM5448	
	Signetics	5448	
SN5449	Fairchild	5449	
	Motorola	MC5449	
SN5450	Fairchild	5450	
	Motorola	MC5450	
	National	DM5450	
	Signetics	5450	
SN5451	Fairchild	5451	
	Motorola	MC5451	
	National	DM5451	
	Signetics	5451	
SN5453	Fairchild	5453	
	Motorola	MC5453	
	National	DM5453	
	Signetics	5453	
SN5454	Fairchild	5454	
	Motorola	MC5454	
	National	DM5454	
	Signetics	5454	
SN5460	Fairchild	5460	
	Motorola	MC5460	
	National	DM5460	
	Signetics	5460	
SN5470	Fairchild	5470	
	Motorola	MC5470	
	National	DM5470	
	Signetics	5470	
SN5472	Fairchild	5472	
	Motorola	MC5472	
	National	DM5472	
	Signetics	5472	
SN5473	Fairchild	5473	
	Motorola	MC5473	
	National	DM5473	
	Signetics	5473	
SN5474	Fairchild	5474	
	Motorola	MC5474	
	National	DM5474	
	Signetics	5474	
SN5475	Fairchild	5475	
	Motorola	MC5475	
	National	DM5475	
	Signetics	5475	
SN5476	Fairchild	5476	
	Motorola	MC5476	
	National	DM5476	
	Signetics	5476	
SN5477	Fairchild	5477	
	Motorola	MC5477	
	Signetics	5477	
SN5480	Fairchild	5480	
	Motorola	MC5480	
	Signetics	5480	
♦SN5481	Fairchild	93407	
	TI	SN5481A	
SN5482	Fairchild	5482	
	Motorola	MC5482	
♦SN5483	Fairchild	5483	
	National	DM5483	
	Signetics	5483	
	TI	SN5483A	
SN5485	Fairchild	5485	
	Motorola	MC5485	
	National	DM5485	
	Signetics	5485	
SN5486	Fairchild	5486	
	Motorola	MC5486	
	National	DM5486	
	Signetics	5486	
♦SN5488	Intersil	IM5600	
	MMI	**5230-1**	**1466**
	National	DM5488	
	TI	SN5488A	
♦SN5489	AMD	SN5489	
		5889	
	Fairchild	5489	
	MMI	5560	
	National	DM5489	
	TI	SN54S189	
♦SN5490	Fairchild	5490	
		9390	
	Motorola	MC5490	
	National	DM5490	
	Signetics	5490	
	TI	SN5490A	
♦SN5491	Fairchild	5491	
	Motorola	MC5491	
	National	DM5491	
	Signetics	5491	
	TI	SN5491A	
♦SN5492	Fairchild	5492	
	Motorola	MC5492	
	National	DM5492	
	Signetics	5492	
	TI	SN5492A	
♦SN5493	Fairchild	5493	
	Motorola	MC5493	
	National	DM5493	
	Signetics	5493	
	TI	SN5493A	
SN5494	Fairchild	5494	
	Motorola	MC5494	
	Signetics	5494	
♦SN5495	Fairchild	5495	
	Motorola	MC5495	
	National	DM5495	
	Signetics	5495	
	TI	SN5495A	
SN5496	Fairchild	5496	
	Motorola	MC5496	
	National	DM5496	
	Signetics	5496	
SN5497	Fairchild	5497	
	Motorola	MC5497	
♦SN5510	Motorola	MC1510	
SN55107	AMD	SN55107	
	Fairchild	55107	
	Motorola	MC55107	
	National	DS55107	
	Raytheon	RM55107	
	Silicon G	SG107	
SN55108	AMD	SN55108B	
	Fairchild	55108	
	Motorola	MC55108	
	National	DS55108	
	Raytheon	RM55108	
	Silicon G	SG108	
SN55109	AMD	SN55109	
	Fairchild	55109	
	Raytheon	RM55109	
	Silicon G	SG109	
SN55110	AMD	SN55110	
	Fairchild	55110	
	Raytheon	RM55110	
	Silicon G	SG110	
SN55112	Fairchild	55112	
SN55114	AMD	9614	
	Fairchild	96114	
SN55115	AMD	9615	
	Fairchild	96115	
SN55121	Fairchild	55121	
SN55121	National	DS55121	
SN55122	Fairchild	55122	
	National	DS55122	
SN55123	Fairchild	55123	
	Silicon G	SG123	
SN55124	Fairchild	55124	
	Silicon G	SG124	
SN55138	Silicon G	SG55138	
SN55154	Silicon G	SG55154	
SN55180	National	DS7800	
SN55182	AMD	DM7820	
	National	DS7820	
	Signetics	DS7820	
SN55183	AMD	DM7830	
	National	DS7830	
	Signetics	DS7830	
SN5520	AMD	SN5520	
		SN5521	
	National	DS5520	
	Silicon G	SG5520	
SN55207	Fairchild	55207	
	Silicon G	SG207	
SN55208	Fairchild	55208	
	Silicon G	SG208	
♦SN5521	AMD	SN5521	
	Silicon G	SG5521	
SN5522	Motorola	MC5522	
	National	DS5522	
	Silicon G	SG5522	
SN55224	Fairchild	55224	
SN55225	Fairchild	55225	
♦SN5523	Motorola	MC5523	
	Silicon G	SG5523	
SN55232	Fairchild	55232	
SN55233	Fairchild	55233	
SN55234	AMD	SN55234	
	Fairchild	55234	
SN55235	AMD	SN55235	
	Fairchild	55235	
SN55238	AMD	SN55238	
	Fairchild	55238	
SN55239	AMD	SN55239	
	Fairchild	55239	
	Silicon G	SG239	
SN5524	AMD	SN5524	
	Fairchild	5524	
	Motorola	MC5524	
	National	DS5524	
	Silicon G	SG5524	
SN55244	AMD	MC1544	
	Motorola	MC1544	
♦SN5525	AMD	SN5525	
	Fairchild	5525	
	Motorola	MC5525	
	Silicon G	SG5525	
SN5526	Silicon G	SG5526	
SN5527	Silicon G	SG5527	
SN5528	Fairchild	5528	
	Motorola	MC5528	
	National	DS5528	
	Silicon G	SG5528	
♦SN5529	Fairchild	5529	
	Motorola	MC5529	
	Silicon G	SG5529	
SN55325	AMD	SN55325	
	Fairchild	55325	
	Motorola	MC55325	
	National	DS55325	
	Raytheon	RM55325	
	Silicon G	SG55325	
SN55326	Fairchild	55326	
SN55327	Fairchild	55327	
♦SN5534	Fairchild	5534	
	National	DS5534	
	Silicon G	SG5534	
SN5535	Fairchild	5535	
	Silicon G	SG5535	
SN5536	Silicon G	SG5536	
SN55361	National	DS55361	
SN55365	National	DS55365	
SN55369	AMD	MMH0020	
	National	DS0026	
SN5537	Silicon G	SG5537	
♦SN5538	Fairchild	5538	
	National	DS5538	
	Silicon G	SG5538	

♦ Discontinued

Bold face device numbers indicate manufacturers data is provided in the IC Master on the pages noted.

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Manufacturer Device	Replacement Source	Device	IC Master Page
♦SN5539	Fairchild	5539	
	Silicon G	SG5539	
SN55450	Fairchild	55450	
	National	DS55450	
	Raytheon	RM55450	
	Silicon G	SG55450	
SN55451	Fairchild	55451	
	National	DS55451	
	Raytheon	RM55451	
	Silicon G	SG55451	
SN55452	Fairchild	55452	
	National	DS55452	
	Raytheon	RM55452	
	Silicon G	SG55452	
SN55453	Fairchild	55453	
	National	DS55453	
	Raytheon	RM55453	
	Silicon G	SG55453	
SN55454	Fairchild	55454	
	National	DS55454	
	Raytheon	RM55454	
	Silicon G	SG55454	
SN55460	Fairchild	55460	
	National	DS55460	
	Silicon G	SG55460	
SN55461	Fairchild	55461	
	National	DS55461	
	Silicon G	SG55461	
SN55462	Fairchild	55462	
	National	DS55462	
	Silicon G	SG55462	
SN55463	Fairchild	55463	
	National	DS55463	
	Silicon G	SG55463	
SN55464	Fairchild	55464	
	National	DS55464	
	Silicon G	SG55464	
SN55470	Fairchild	55470	
SN55471	Fairchild	55471	
	Silicon G	SG55471	
SN55472	Fairchild	55472	
	Silicon G	SG55472	
SN55473	Fairchild	55473	
	Silicon G	SG55473	
SN55474	Fairchild	55474	
	Silicon G	SG55474	
SN55480	National	DS7880	
SN55493	National	DS55493	
SN55494	National	DS55494	
♦SN56502	TI	TL441	
♦SN72L022	TI	TL022	
♦SN72L044	TI	TL044	
♦SN72301A	TI	LM301	
♦SN72304	Motorola	MLM304	
	TI	LM304	
♦SN72305	Motorola	MLM305	
	TI	LM305	
♦SN72306	TI	LM306	
♦SN72307	TI	LM307	
♦SN72308	AMD	LM308	
	Fairchild	μA308	
	Intersil	LM308	
	Motorola	LM308	
	Raytheon	LM308	
	RCA	CA308	
	Silicon G	SG308	
♦SN72309	TI	LM309	
♦SN72310	AMD	LM310	
	Fairchild	μA310	
	Intersil	LM310	
	Motorola	MLM310	
	Silicon G	SG310	
♦SN72311	TI	LM311	
♦SN72318	TI	LM318	
♦SN72376	TI	LM376	
♦SN72440	TI	TL440	
♦SN72506	TI	TL506	
♦SN72510	TI	TL510	
♦SN72514	TI	TL514	
♦SN72555	TI	NE555	
♦SN72558	TI	MC1458	
♦SN72560	TI	TL560	
♦SN72702	TI	TL702	
♦SN72709	TI	μA709	
♦SN72710	TI	TL710	
♦SN72711	TI	μA711	
♦SN72720	TI	TL720	
♦SN72723	Motorola	MC723	
	TI	μA723	
♦SN72733	TI	μA733	
SN72741	Sprague	ULN-2151	
♦SN72741	TI	μA741	
♦SN72747	TI	μA747	
♦SN72748	TI	μA748	
♦SN72777	TI	μA777	
♦SN72810	TI	TL810	
♦SN72811	TI	TL811	
♦SN72820	TI	TL820	
♦SN72905	Motorola	MC7905	
♦SN72906	Motorola	MC7906	
♦SN72908	Motorola	MC7908	
♦SN72912	Motorola	MC7912	
♦SN72915	Motorola	MC7915	
♦SN72918	Motorola	MC7818	
♦SN72924	Motorola	MC7824	
SN74H00	Fairchild	74H00	
	Motorola	MC74H00	
	National	DM74H00	
	NEC America	μPB74H00	
	Raytheon	74H00	
	Signetics	74H00	
SN74H01	Fairchild	74H01	
	Motorola	MC74H01	
	National	DM74H01	
	NEC America	μPB74H01	
	Raytheon	74H01	
	Signetics	74H01	
SN74H04	Fairchild	74H04	
	Motorola	MC74H04	
	National	DM74H04	
	NEC America	μPB74H04	
	Raytheon	74H04	
	Signetics	74H04	
SN74H05	Fairchild	74H05	
	Motorola	MC74H05	
	National	DM74H05	
	Raytheon	74H05	
	Signetics	74H05	
SN74H10	Fairchild	74H10	
	Motorola	MC74H10	
	National	DM74H10	
	NEC America	μPB74H10	
	Raytheon	74H10	
	Signetics	74H10	
SN74H101	Motorola	MC74H101	
	Signetics	74H101	
SN74H102	Fairchild	74H102	
	Motorola	MC74H102	
	Signetics	74H102	
SN74H103	Fairchild	74H103	
	National	DM74H103	
	Signetics	74H103	
SN74H106	Fairchild	74H106	
		9H106	
	National	DM74H106	
	Signetics	74H106	
SN74H108	Fairchild	74H108	
	Motorola	MC74H108	
	National	DM74H108	
	Signetics	74H108	
SN74H11	Fairchild	74H11	
	Motorola	MC74H11	
	National	DM74H11	
	Raytheon	74H11	
	Signetics	74H11	
SN74H15	Fairchild	74H15	
	Raytheon	74H15	
SN74H183	Fairchild	74H183	
	Hitachi	HD74H183	
SN74H20	Fairchild	74H20	
	Motorola	MC74H20	
	National	DM74H20	
	NEC America	μPB74H20	
	Raytheon	74H20	
	Signetics	74H20	
SN74H21	Fairchild	74H21	
	Motorola	MC74H21	
	National	DM74H21	
	Signetics	74H21	
SN74H22	Fairchild	74H22	
	Motorola	MC74H22	
	National	DM74H22	
	Raytheon	74H22	
	Signetics	74H22	
SN74H30	Fairchild	74H30	
	Motorola	MC74H30	
	National	DM74H30	
	NEC America	μPB74H30	
	Signetics	74H30	
SN74H40	Fairchild	74H40	
	Motorola	MC74H40	
	National	DM74H40	
	NEC America	μPB74H40	
	Raytheon	74H40	
	Signetics	74H40	
SN74H50	Fairchild	74H50	
	Motorola	MC74H50	
	National	DM74H50	
	Signetics	74H50	
SN74H51	Fairchild	74H51	
		9H51	
	Motorola	MC74H51	
	National	DM74H51	
	NEC America	μPB74H51	
	Signetics	74H51	
SN74H52	Fairchild	74H52	
	Motorola	MC74H52	
	National	DM74H52	
	Signetics	74H52	
SN74H53	Fairchild	74H53	
	Motorola	MC74H53	
	National	DM74H53	
	Signetics	74H53	
SN74H54	Fairchild	74H54	
	Motorola	MC74H54	
	National	DM74H54	
	Signetics	74H54	
SN74H55	Fairchild	74H55	
	Motorola	MC74H55	
	National	DM74H55	
	Signetics	74H55	
SN74H60	Fairchild	74H60	
	Motorola	MC74H60	
	National	DM74H60	
	Signetics	74H60	
SN74H61	Fairchild	74H61	
	Motorola	MC74H61	
	National	DM74H61	
	Signetics	74H61	
SN74H62	Fairchild	74H62	
	Motorola	MC74H62	
	National	DM74H62	
	Signetics	74H62	
SN74H71	Fairchild	74H71	
	Motorola	MC74H71	
	National	DM74H71	
	Signetics	74H71	
SN74H72	Fairchild	74H72	
	Motorola	MC74H72	
	National	DM74H72	
	Signetics	74H72	
SN74H73	Fairchild	74H73	
	Motorola	MC74H73	
	National	DM74H73	
	Signetics	74H73	
SN74H74	Fairchild	74H74	
	Motorola	MC74H74	
	National	DM74H74	
	Raytheon	74H74	
	Signetics	74H74	
SN74H76	Fairchild	74H76	
	Motorola	MC74H76	
	National	DM74H76	
	Signetics	74H76	
SN74H78	Fairchild	74H78	
	National	DM74H78	
SN74H87	Fairchild	74H87	
	Motorola	MC74H87	
SN74LS00	Fairchild	74LS00	
	Hitachi	HD74LS00	
	Motorola	SN74LS00	
	National	DM74LS00	
	NEC America	μPB74LS00	
	Raytheon	74LS00	
	Signetics	74LS00	
SN74LS01	Hitachi	HD74LS01	
	Motorola	SN74LS01	
	National	DM74LS01	
	Raytheon	74LS01	
	Signetics	74LS01	
SN74LS02	Fairchild	74LS02	
	Hitachi	HD74LS02	
	Motorola	SN74LS02	
	National	DM74LS02	
	NEC America	μPB74LS02	
	Raytheon	74LS02	
	Signetics	74LS02	
SN74LS03	Fairchild	74LS03	
	Hitachi	HD74LS03	
	Motorola	SN74LS03	
	National	DM74LS03	
	NEC America	μPB74LS03	
	Raytheon	74LS03	
	Signetics	74LS03	
SN74LS04	Fairchild	74LS04	
	Hitachi	HD74LS04	
	Motorola	SN74LS04	
	National	DM74LS04	
	NEC America	μPB74LS04	
	Raytheon	74LS04	
	Signetics	74LS04	
SN74LS05	Fairchild	74LS05	
	Hitachi	HD74LS05	
	Motorola	SN74LS05	
	National	DM74LS05	
	NEC America	μPB74LS05	
	Raytheon	74LS05	
	Signetics	74LS05	
SN74LS08	Fairchild	74LS08	
	Hitachi	HD74LS08	
	Motorola	SN74LS08	
	National	DM74LS08	
	NEC America	μPB74LS08	
	Raytheon	74LS08	
	Signetics	74LS08	
SN74LS09	Fairchild	74LS09	
	Hitachi	HD74LS09	
	Motorola	SN74LS09	
	National	DM74LS09	
	Raytheon	74LS09	
	Signetics	74LS09	
SN74LS10	Fairchild	74LS10	
	Hitachi	HD74LS10	
	Motorola	SN74LS10	
	National	DM74LS10	
	NEC America	μPB74LS10	
	Raytheon	74LS10	
	Signetics	74LS10	
SN74LS107A	Fairchild	74LS107	
	Hitachi	HD74LS107	
	Motorola	SN74LS107A	
	National	DM74LS107	
	Raytheon	74LS107	
	Signetics	74LS107	
SN74LS109A	Fairchild	74LS109	
	Motorola	SN74LS109A	
	National	DM74LS109	
	NEC America	μPB74LS109	
	Raytheon	74LS109	
	Signetics	74LS109	
SN74LS11	Fairchild	74LS11	
	Hitachi	HD74LS11	
	Motorola	SN74LS11	
	National	DM74LS11	
	NEC America	μPB74LS11	
	Raytheon	74LS11	
	Signetics	74LS11	
SN74LS112A	Fairchild	74LS112	
	Hitachi	HD74LS112	
	Motorola	SN74LS112A	
	National	DM74LS112	
	NEC America	μPB74LS112	
	Raytheon	74LS112	
	Signetics	74LS112	
SN74LS113A	Fairchild	74LS113	
	Hitachi	HD74LS113	
	Motorola	SN74LS113A	
	National	DM74LS113	
	NEC America	μPB74LS113	
	Raytheon	74LS113	
	Signetics	74LS113	

♦ Discontinued

The manufacturers report their devices can be used as direct replacements.
Performance details often differ, so compare the specifications considering your requirements.

Texas Instruments (cont'd)

Manufacturer Device	Replacement Source	Device	IC Master Page
SN74LS114A	Fairchild	74LS114	
	Hitachi	HD74LS114	
	Motorola	SN74LS114A	
	National	DM74LS114	
	Raytheon	74LS114	
	Signetics	74LS114	
SN74LS12	Hitachi	HD74LS12	
	National	DM74LS12	
	Raytheon	74LS12	
	Signetics	74LS12	
SN74LS122	Motorola	SN74LS122	
	National	DM74LS122	
	Raytheon	74LS122	
SN74LS123	AMD	SN74LS123	
	Hitachi	HD74LS123	
	Motorola	SN74LS123	
	National	DM74LS123	
	Raytheon	74LS123	
SN74LS125A	Fairchild	74LS125	
	Motorola	SN74LS125A	
	National	DM74LS125	
	Raytheon	74LS125	
	Signetics	74LS125	
SN74LS126A	Fairchild	74LS126	
	Motorola	SN74LS126A	
	National	DM74LS126	
	Raytheon	74LS126	
	Signetics	74LS126	
SN74LS13	Fairchild	74LS13	
	Hitachi	HD74LS13	
	Motorola	SN74LS13	
	National	DM74LS13	
	Raytheon	74LS13	
	Signetics	74LS13	
SN74LS132	Fairchild	74LS132	
	Hitachi	HD74LS132	
	Motorola	SN74LS132	
	National	DM74LS132	
	Raytheon	74LS132	
	Signetics	74LS132	
SN74LS136	Fairchild	74LS136	
	Hitachi	HD74LS136	
	Motorola	SN74LS136	
	National	DM74LS136	
	Raytheon	74LS136	
	Signetics	74LS136	
SN74LS138	AMD	SN74LS138	
	Fairchild	74LS138	
	Hitachi	HD74LS138	
	Motorola	SN74LS138	
	National	DM74LS138	
	NEC America	μPB74LS138	
	Raytheon	74LS138	
	Signetics	74LS138	
SN74LS139	AMD	SN74LS139	
	Fairchild	74LS139	
	Hitachi	HD74LS139	
	Motorola	SN74LS139	
	National	DM74LS139	
	NEC America	μPB74LS139	
	Raytheon	74LS139	
	Signetics	74LS139	
SN74LS14	Fairchild	74LS14	
	Hitachi	HD74LS14	
	Motorola	SN74LS14	
	National	DM74LS14	
	Raytheon	74LS14	
	Signetics	74LS14	
SN74LS145	Signetics	74LS145	
SN74LS148	AMD	SN74LS148	
SN74LS15	Fairchild	74LS15	
	Hitachi	HD74LS15	
	Motorola	SN74LS15	
	National	DM74LS15	
	Raytheon	74LS15	
	Signetics	74LS15	
SN74LS151	AMD	SN74LS151	
	Fairchild	74LS151	
	Hitachi	HD74LS151A	
	Motorola	SN74LS151	
	National	DM74LS151	
	NEC America	μPB74LS151	
	Raytheon	74LS151	
SN74LS151	Signetics	74LS151	
SN74LS152	Fairchild	74LS152	
	Hitachi	HD74LS152	
	Raytheon	74LS152	
SN74LS153	AMD	SN74LS153	
	Fairchild	74LS153	
	Hitachi	HD74LS153	
	Motorola	SN74LS153	
	National	DM74LS153	
	NEC America	μPB74LS153	
	Raytheon	74LS153	
	Signetics	74LS153	
SN74LS155	Fairchild	74LS155	
	Hitachi	HD74LS155	
	Motorola	SN74LS155	
	National	DM74LS155	
	NEC America	μPB74LS155	
	Raytheon	74LS155	
	Signetics	74LS155	
SN74LS156	Fairchild	74LS156	
	Hitachi	HD74LS156	
	Motorola	SN74LS156	
	National	DM74LS156	
	Raytheon	74LS156	
	Signetics	74LS156	
SN74LS157	AMD	SN74LS157	
	Fairchild	74LS157	
	Motorola	SN74LS157	
	National	DM74LS157	
	NEC America	μPB74LS157	
	Raytheon	74LS157	
	Signetics	74LS157	
SN74LS158	AMD	SN74LS158	
	Fairchild	74LS158	
	Hitachi	HD74LS158	
	Motorola	SN74LS158	
	National	DM74LS158	
	Raytheon	74LS158	
	Signetics	74LS158	
SN74LS160A	AMD	SN74LS160	
	Hitachi	HD74LS160A	
	Motorola	SN74LS160A	
	National	DM74LS160	
	Raytheon	74LS160	
	Signetics	74LS160A	
SN74LS161A	AMD	SN74LS161	
	Fairchild	74LS161	
	Hitachi	HD74LS161A	
	Motorola	SN74LS161A	
	National	DM74LS161	
	NEC America	μPB74LS161	
	Raytheon	74LS161	
	Signetics	74LS161A	
SN74LS162A	AMD	SN74LS162	
	Fairchild	74LS162	
	Hitachi	HD74LS162A	
	Motorola	SN74LS162A	
	National	DM74LS162	
	Raytheon	74LS162	
	Signetics	74LS162	
SN74LS163A	AMD	SN74LS163	
	Fairchild	74LS163	
	Hitachi	HD74LS163A	
	Motorola	SN74LS163A	
	National	DM74LS163	
	Raytheon	74LS163	
	Signetics	74LS163A	
SN74LS164	AMD	SN74LS164	
	Fairchild	74LS164	
	Hitachi	HD74LS164	
	Motorola	SN74LS164A	
	National	DM74LS164	
	NEC America	μPB74LS164	
	Raytheon	74LS164	
	Signetics	74LS164A	
SN74LS165	Fairchild	74LS165	
	Motorola	SN74LS165	
SN74LS166	Motorola	SN74LS166	
SN74LS168	AMD	SN74LS168	
	Fairchild	74LS168	
	Motorola	SN74LS168A	
	National	DM74LS168	
SN74LS169	AMD	SN74LS169	
	Fairchild	74LS169	
	Motorola	SN74LS169A	
	National	DM74LS169	
SN74LS170	AMD	SN74LS170	
	Fairchild	74LS170	
	Motorola	SN74LS170	
	National	DM74LS170	
	Raytheon	74LS170	
	Signetics	74LS170	
SN74LS173A	Fairchild	74LS173	
	Motorola	SN74LS173	
	National	DM74LS173	
	Signetics	74LS173	
SN74LS174	AMD	SN74LS174	
	Fairchild	74LS174	
	Hitachi	HD74LS174	
	Motorola	SN74LS174	
	National	DM74LS174	
	Raytheon	74LS174	
	Signetics	74LS174	
SN74LS175	AMD	SN74LS175	
	Fairchild	74LS175	
	Hitachi	HD74LS175	
	Motorola	SN74LS175	
	National	DM74LS175	
	NEC America	μPB74LS175	
	Raytheon	74LS175	
	Signetics	74LS175	
SN74LS181	AMD	SN74LS181	
	Fairchild	74LS181	
	Motorola	SN74LS181	
	Raytheon	74LS181	
	Signetics	74LS181	
SN74LS189	Motorola	SN74LS189	
SN74LS190	AMD	SN74LS190	
	Fairchild	74LS190	
	Motorola	SN74LS190	
	National	DM74LS190	
	Raytheon	74LS190	
	Signetics	74LS190	
SN74LS191	AMD	SN74LS191	
	Fairchild	74LS191	
	Motorola	SN74LS191	
	National	DM74LS191	
	Raytheon	74LS191	
	Signetics	74LS191	
SN74LS192	AMD	SN74LS192	
	Fairchild	74LS192	
	Motorola	SN74LS192	
	National	DM74LS192	
	NEC America	μPB74LS192	
	Raytheon	74LS192	
	Signetics	74LS192	
SN74LS193	AMD	SN74LS193	
	Fairchild	74LS193	
	Motorola	SN74LS193	
	National	DM74LS193	
	NEC America	μPB74LS193	
	Raytheon	74LS193	
	Signetics	74LS193	
SN74LS194A	AMD	SN74LS194	
		SN74LS194A	
	Fairchild	74LS194	
	Hitachi	HD74LS194A	
	Motorola	74LS194A	
	NEC America	μPB74LS194	
	Raytheon	74LS194A	
	Signetics	74LS194A	
SN74LS195A	AMD	SN74LS195A	
	Fairchild	74LS195	
	Hitachi	HD74LS195A	
	Motorola	SN74LS195A	
	NEC America	μPB74LS195	
	Raytheon	74LS195A	
	Signetics	74LS195A	
SN74LS196	Fairchild	74LS196	
	Motorola	SN74LS196	
	National	DM74LS196	
	Raytheon	74LS196	
	Signetics	74LS196	
SN74LS197	Fairchild	74LS197	
	Motorola	SN74LS197	
	National	DM74LS197	
	Raytheon	74LS197	
	Signetics	74LS197	
SN74LS20	Fairchild	74LS20	
	Hitachi	HD74LS20	
	Motorola	SN74LS20	
	National	DM74LS20	
SN74LS20	NEC America	μPB74LS20	
	Raytheon	74LS20	
	Signetics	74LS20	
SN74LS21	Fairchild	74LS21	
	Hitachi	HD74LS21	
	Motorola	SN74LS21	
	National	DM74LS21	
	NEC America	μPB74LS21	
	Raytheon	74LS21	
	Signetics	74LS21	
SN74LS22	Fairchild	74LS22	
	Hitachi	HD74LS22	
	Motorola	SN74LS22	
	National	DM74LS22	
	Raytheon	74LS22	
	Signetics	74LS22	
SN74LS221	Motorola	SN74LS221	
	National	DM74LS221	
	Raytheon	74LS221	
	Signetics	74LS221	
SN74LS240	AMD	SN74LS240	
	Fairchild	74LS240	
	MMI	**74LS240**	**768**
	Motorola	SN74LS240	
	Raytheon	**74LS240**	**522**
	Signetics	74LS240	
SN74LS241	AMD	SN74LS241	
	Fairchild	74LS241	
	MMI	**74LS241**	**768**
	Motorola	SN74LS241	
	Raytheon	**74LS241**	**525**
	Signetics	74LS241	
SN74LS242	AMD	SN74LS242	
	Fairchild	74LS242	
	Motorola	SN74LS242	
	Raytheon	**74LS242**	**528**
	Signetics	74LS242	
SN74LS243	AMD	SN74LS243	
	Fairchild	74LS243	
	Motorola	SN74LS243	
	Raytheon	**74LS243**	**528**
	Signetics	74LS243	
SN74LS244	AMD	SN74LS244	
	Fairchild	74LS244	
	MMI	**74LS244**	**768**
	Motorola	SN74LS244	
	Raytheon	**74LS244**	**525**
	Signetics	74LS244	
SN74LS245	**MMI**	**74LS245**	**774**
	Motorola	SN74LS245	
	Signetics	74LS245	
SN74LS247	Fairchild	74LS247	
	Hitachi	HD74LS247	
	Motorola	SN74LS247	
	National	DM74LS247	
SN74LS248	Fairchild	74LS248	
	Hitachi	HD74LS248	
	Motorola	SN74LS248	
	National	DM74LS248	
SN74LS249	Fairchild	74LS249	
	Hitachi	HD74LS249	
	Motorola	SN74LS249	
	National	DM74LS249	
SN74LS251	AMD	SN74LS251	
	Fairchild	74LS251	
	Hitachi	HD74LS251	
	Motorola	SN74LS251	
	National	DM74LS251	
	NEC America	μPB74LS251	
	Raytheon	74LS251	
	Signetics	74LS251	
SN74LS253	AMD	SN74LS253	
	Fairchild	74LS253	
	Hitachi	HD74LS253	
	Motorola	SN74LS253	
	National	DM74LS253	
	NEC America	μPB74LS253	
	Raytheon	74LS253	
	Signetics	74LS253	
SN74LS257A	AMD	SN74LS257	
	Fairchild	74LS257	
	Hitachi	HD74LS257	
	Motorola	SN74LS257A	
	National	DM74LS257	
	NEC America	μPB74LS257	
	Raytheon	74LS257	

♦ Discontinued

Bold face device numbers indicate manufacturers data is provided in the IC Master on the pages noted.

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Manufacturer Device	Replacement Source	Device	IC Master Page
SN74LS257A	Signetics	74LS257	
SN74LS258A	AMD	SN74LS258	
	Fairchild	74LS258	
	Motorola	SN74LS258A	
	National	DM74LS258	
	NEC America	μPB74LS258	
	Raytheon	74LS258	
	Signetics	74LS258	
SN74LS259	Fairchild	74LS259	
	Motorola	SN74LS259	
SN74LS26	Fairchild	74LS26	
	Hitachi	HD74LS26	
	Motorola	SN74LS26	
	National	DM74LS26	
	Raytheon	74LS26	
	Signetics	74LS26	
SN74LS261	Raytheon	74LS261	
	Signetics	74LS261	
SN74LS266	Fairchild	74LS266	
	Motorola	SN74LS266	
	Raytheon	74LS266	
	Signetics	74LS266	
SN74LS27	Fairchild	74LS27	
	Hitachi	HD74LS27	
	Motorola	SN74LS27	
	National	DM74LS27	
	NEC America	μPB74LS27	
	Raytheon	74LS27	
	Signetics	74LS27	
SN74LS273	AMD	SN74LS273	
	Fairchild	74LS273	
	MMI	**74LS273**	**509**
	Raytheon	**74LS273**	**531**
	Signetics	74LS273	
SN74LS279	Fairchild	74LS279	
	Motorola	SN74LS279	
	National	DM74LS279	
	NEC America	μPB74LS279	
	Raytheon	74LS279	
	Signetics	74LS279	
SN74LS28	Fairchild	74LS28	
	Motorola	SN74LS28	
	Raytheon	74LS28	
	Signetics	74LS28	
SN74LS280	Fairchild	74LS280	
SN74LS281	AMD	SN74LS281	
SN74LS283	Fairchild	74LS283	
	Hitachi	SN74LS283	
	MMI	74LS283	
	Motorola	SN74LS283	
	National	DM74LS283	
	Raytheon	74LS283	
	Signetics	74LS283	
SN74LS289	Motorola	SN74LS289	
SN74LS290	Fairchild	74LS290	
	Motorola	SN74LS290	
	National	DM74LS290	
	Signetics	74LS290	
SN74LS293	Fairchild	74LS293	
	Motorola	SN74LS293	
	National	DM74LS293	
	Signetics	74LS293	
SN74LS295B	Fairchild	74LS295	
	Motorola	SN74LS295	
	NEC America	μPB74LS295	
	Raytheon	74LS295A	
	Signetics	74LS295	
SN74LS298	Fairchild	74LS298	
	Hitachi	HD74LS298	
	Motorola	SN74LS298	
	Raytheon	74LS298	
	Signetics	74LS298	
SN74LS299	AMD	SN74LS299	
	Fairchild	74LS299	
	MMI	74LS299	
	Raytheon	**74LS299**	**533**
SN74LS30	Fairchild	74LS30	
	Hitachi	HD74LS30	
	Motorola	SN74LS30	
	National	DM74LS30	
	NEC America	μPB74LS30	
	Raytheon	74LS30	
	Signetics	74LS30	
SN74LS32	Fairchild	74LS32	
	Hitachi	HD74LS32	
	Motorola	SN74LS32	
	National	DM74LS32	
	NEC America	μPB74LS32	
	Raytheon	74LS32	
	Signetics	74LS32	
SN74LS322	AMD	SN74LS322	
	Fairchild	74LS322	
	MMI	74LS322	
	Motorola	SN74LS322	
	Raytheon	**74LS322**	**537**
SN74LS322A	AMD	AM25LS22	
	Raytheon	74LS322A	
SN74LS323	AMD	AM25LS23	
		SN74LS323	
	Fairchild	74LS323	
	MMI	74LS323	
	Motorola	SN74LS323	
	Raytheon	**74LS323**	**540**
SN74LS33	Fairchild	74LS33	
	Motorola	SN74LS33	
	Raytheon	74LS33	
	Signetics	74LS33	
SN74LS352	Fairchild	74LS352	
	Motorola	SN74LS352	
	National	DM74LS352	
SN74LS353	Fairchild	74LS353	
	Motorola	SN74LS353	
	National	DM74LS353	
SN74LS363	Signetics	74LS363	
SN74LS364	Signetics	74LS364	
SN74LS365A	Fairchild	74LS365	
	Motorola	SN74LS365A	
	National	DM74LS365	
	NEC America	μPB74LS365	
	Raytheon	74LS365	
	Signetics	74LS365A	
SN74LS366A	Fairchild	74LS366	
	Motorola	SN74LS366A	
	National	DM74LS366	
	NEC America	μPB74LS366	
	Raytheon	74LS366	
	Signetics	74LS366A	
SN74LS367	Hitachi	HD74LS367	
SN74LS367A	Fairchild	74LS367	
	Motorola	SN74LS367A	
	National	DM74LS367	
	NEC America	μPB74LS367	
	Raytheon	74LS367	
	Signetics	74LS367A	
SN74LS368	Hitachi	HD74LS368	
SN74LS368A	Fairchild	74LS368	
	Motorola	SN74LS368A	
	National	DM74LS368	
	NEC America	μPB74LS368	
	Raytheon	74LS368	
	Signetics	74LS368A	
SN74LS37	Fairchild	74LS37	
	Hitachi	HD74LS37	
	Motorola	SN74LS37	
	National	DM74LS37	
	NEC America	μPB74LS37	
	Raytheon	74LS37	
	Signetics	74LS37	
SN74LS373	AMD	SN74LS373	
	Fairchild	74LS373	
	MMI	**74LS373**	**505**
	Motorola	SN74LS373	
	Raytheon	**74LS373**	**543**
	Signetics	74LS373	
SN74LS374	AMD	SN74LS374	
	Fairchild	74LS374	
	MMI	**74LS374**	**505**
	National	DM74LS374	
	Raytheon	**74LS374**	**543**
	Signetics	74LS374	
SN74LS375	Fairchild	74LS375	
	Motorola	SN74LS375	
	NEC America	μPB74LS375	
	Raytheon	74LS375	
	Signetics	74LS375	
SN74LS377	AMD	SN74LS377	
	Fairchild	74LS377	
	MMI	**74LS377**	**509**
	Raytheon	**54LS377**	**549**
SN74LS377	**Raytheon**	**74LS377**	**549**
	Signetics	74LS377	
SN74LS378	AMD	SN74LS378	
	Fairchild	74LS378	
	Motorola	SN74LS378	
	Signetics	SN74LS378	
SN74LS379	AMD	AM25LS08	
		SN74LS379	
	Fairchild	74LS379	
	Motorola	SN74LS379	
SN74LS38	Fairchild	74LS38	
	Hitachi	HD74LS38	
	Motorola	SN74LS38	
	National	DM74LS38	
	NEC America	μPB74LS38	
	Raytheon	74LS38	
	Signetics	74LS38	
SN74LS381	AMD	SN74LS381	
SN74LS384	AMD	AM25LS14	
		SN74LS384	
	Fairchild	74LS384	
	Motorola	SN74LS384	
	Raytheon	**74LS384**	**551**
SN74LS385	AMD	AM25LS15	
		SN74LS385	
	Motorola	SN74LS385	
	Raytheon	**74LS385**	**554**
SN74LS386	Fairchild	74LS386	
	Hitachi	HD74LS386	
	Motorola	SN74LS386	
	National	DM74LS386	
	Raytheon	74LS386	
	Signetics	74LS386	
SN74LS390	Fairchild	74LS390	
	Motorola	SN74LS390	
SN74LS393	Fairchild	74LS393	
	Motorola	SN74LS393	
SN74LS395	Signetics	74LS395	
SN74LS395A	Fairchild	74LS395	
	Motorola	SN74LS395A	
	National	DM74LS395	
	Raytheon	74LS395	
SN74LS398	Motorola	SN74LS398	
SN74LS399	AMD	AM25LS09	
		SN74LS399	
	Motorola	SN74LS399	
SN74LS40	Fairchild	74LS40	
	Hitachi	HD74LS40	
	Motorola	SN74LS40	
	National	DM74LS40	
	NEC America	μPB74LS40	
	Raytheon	74LS40	
	Signetics	74LS40	
SN74LS42	Fairchild	74LS42	
	Hitachi	HD74LS42	
	Motorola	SN74LS42	
	National	DM74LS42	
	NEC America	μPB74LS42	
	Raytheon	74LS42	
	Signetics	74LS42	
SN74LS424	AMD	SN74LS424	
	NEC Micro	**μPB8224**	**2188**
SN74LS47	Hitachi	HD74LS47	
	Motorola	SN74S47	
SN74LS48	Hitachi	HD74LS48	
SN74LS49	Hitachi	HD74LS49	
	Motorola	SN74LS49	
SN74LS490	Fairchild	74LS490	
	Motorola	SN74LS490	
SN74LS51	Fairchild	74LS51	
	Hitachi	HD74LS51	
	Motorola	SN74LS51	
	National	DM74LS51	
	NEC America	μPB74LS51	
	Raytheon	74LS51	
	Signetics	74LS51	
SN74LS54	Fairchild	74LS54	
	Hitachi	HD74LS54	
	Motorola	SN74LS54	
	National	DM74LS54	
	NEC America	μPB74LS54	
	Raytheon	74LS54	
	Signetics	74LS54	
SN74LS55	Fairchild	74LS55	
	Hitachi	HD74LS55	
	Motorola	SN74LS55	
SN74LS55	National	DM74LS55	
	NEC America	μPB74LS55	
	Raytheon	74LS55	
	Signetics	74LS55	
SN74LS640	Motorola	SN74LS640	
	Signetics	8T125	
SN74LS641	Motorola	SN74LS641	
SN74LS642	Motorola	SN74LS642	
SN74LS645	Motorola	SN74LS645	
SN74LS670	Fairchild	74LS670	
	Motorola	SN74LS670	
	National	DM74LS670	
	Raytheon	74LS670	
	Signetics	74LS670	
SN74LS73A	Fairchild	74LS73	
	Hitachi	HD74LS73	
	Motorola	SN74LS73A	
	National	DM74LS73	
	Raytheon	74LS73	
	Signetics	74LS73	
SN74LS74A	Fairchild	74LS74	
	Hitachi	SN74LS74A	
	Motorola	SN74LS74A	
	National	DM74LS74	
	NEC America	μPB74LS74	
	Raytheon	74LS74	
	Signetics	74LS74	
SN74LS75	Fairchild	74LS75	
	Motorola	SN74LS75	
	National	DM74LS75	
	Raytheon	74LS75	
	Signetics	74LS75	
SN74LS76A	Hitachi	HD74LS76	
	Motorola	SN74LS76A	
	National	DM74LS76	
	Raytheon	74LS76	
	Signetics	74LS76	
SN74LS77	Motorola	SN74LS77	
SN74LS78	Fairchild	74LS78	
SN74LS78A	Hitachi	HD74LS78	
	Motorola	SN74LS78A	
	National	DM74LS78	
	Raytheon	74LS78	
	Signetics	74LS78	
SN74LS83A	Fairchild	74LS83	
	Hitachi	HD74LS83A	
	Motorola	SN74LS83A	
	National	DM74LS83	
		DM74LS83A	
	Raytheon	74LS83A	
	Signetics	74LS83	
		74LS83A	
SN74LS85	Fairchild	74LS85	
	Motorola	SN74LS85	
	National	DM74LS85	
	Raytheon	74LS85	
	Signetics	74LS85	
SN74LS86	Fairchild	74LS86	
	Hitachi	HD74LS86	
	Motorola	SN74LS86	
	NEC America	μPB74LS86	
	Raytheon	74LS86	
	Signetics	74LS86	
SN74LS90	Fairchild	74LS90	
	Motorola	SN74LS90	
	Raytheon	74LS90	
	Signetics	74LS90	
SN74LS91	Raytheon	74LS91	
SN74LS92	Fairchild	74LS92	
	Hitachi	HD74LS92	
	Motorola	SN74LS92	
	Raytheon	74LS92	
	Signetics	74LS92	
SN74LS93	Fairchild	74LS93	
	Motorola	SN74LS93	
	Raytheon	74LS93	
	Signetics	74LS93	
SN74LS95B	Fairchild	74LS95	
	Hitachi	HD74LS95B	
	Motorola	SN74LS95B	
	Raytheon	74LS95B	
	Signetics	74LS95B	
SN74LS96	Signetics	74LS96	
SN74L00	National	DM74L00	
SN74L01	National	DM74L01	
SN74L02	National	DM74L02	

♦ Discontinued

The manufacturers report their devices can be used as direct replacements.
Performance details often differ, so compare the specifications considering your requirements.

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Manufacturer Device	Replacement Source	Device	IC Master Page
SN74L03	National	DM74L03	
SN74L04	National	DM74L04	
SN74L10	National	DM74L10	
SN74L123	National	DM74L123	
SN74L154	National	DM74L154A	
SN74L157	National	DM74L157A	
SN74L164	National	DM74L164	
SN74L192	National	DM74L192	
SN74L193	National	DM74L193	
SN74L20	National	DM74L20	
SN74L30	National	DM74L30	
SN74L42	National	DM74L42A	
SN74L51	National	DM74L51	
SN74L54	National	DM74L54	
SN74L55	National	DM74L55	
SN74L71	National	DM74L71	
SN74L72	National	DM74L72	
SN74L73	National	DM74L73	
SN74L74	National	DM74L74	
SN74L75	National	DM74L75	
SN74L78	National	DM74L78	
SN74L85	National	DM74L85	
SN74L86	National	DM74L86	
SN74L90	National	DM74L90	
SN74L91	National	DM74L91	
SN74L93	National	DM74L93	
SN74L95	National	DM74L95	
SN74L98	National	DM74L98	
SN74S00	Fairchild	74S00	
	Hitachi	HD74S00	
	Mitsubishi	M5S000	
	National	DM74S00	
	Signetics	74S00	
SN74S02	Fairchild	74S02	
	Hitachi	HD74S02	
	MMI	**74S373**	**505**
	TI	SN74S373	
SN74S03	Fairchild	74S03	
	Hitachi	HD74S03	
	Mitsubishi	M5S003	
	National	DM74S03	
	Signetics	74S03	
SN74S04	Fairchild	74S04	
	Hitachi	HD74S04	
	Mitsubishi	M5S004	
	National	DM74S04	
	Signetics	74S04	
SN74S05	Fairchild	74S05	
	Hitachi	HD74S05	
	Mitsubishi	M5S005	
	National	DM74S05	
	Signetics	74S05	
SN74S08	Fairchild	74S08	
	Signetics	74S08	
SN74S09	Fairchild	74S09	
	Signetics	74S09	
SN74S10	Fairchild	74S10	
	Hitachi	HD74S10	
	Mitsubishi	M5S010	
	National	DM74S10	
	Signetics	74S10	
SN74S109	Fairchild	74S109	
SN74S11	Fairchild	74S11	
	Hitachi	HD74S11	
	Mitsubishi	M5S011	
	National	DM74S11	
	Signetics	74S11	
SN74S112	Fairchild	74S112	
	Hitachi	HD74S112	
	Mitsubishi	M5S112	
	Motorola	SN74S112	
	National	DM74S112	
	Signetics	74S112	
SN74S113	Fairchild	74S113	
	Hitachi	HD74S113	
	Mitsubishi	M5S113	
	Motorola	SN74S113	
	National	DM74S113	
	Signetics	74S113	
SN74S114	Fairchild	74S114	
	Hitachi	HD74S114	
	Mitsubishi	M5S114	
	National	DM74S114	
SN74S114	Signetics	74S114	
SN74S12	Hitachi	HD74S12	
	Motorola	SN74S12	
SN74S132	Fairchild	74S132	
SN74S133	Fairchild	74S133	
	Hitachi	HD74S133	
	Mitsubishi	M5S133	
	National	DM74S133	
	Signetics	74S133	
SN74S134	Fairchild	74S134	
	Hitachi	HD74S134	
	National	DM74S134	
	Signetics	74S134	
SN74S135	Fairchild	74S135	
	Hitachi	HD74S135	
	National	DM74S135	
	Signetics	74S135	
SN74S138	AMD	SN74S138	
	Fairchild	74S138	
	Mitsubishi	M5S138	
	National	DM74S138	
	Signetics	74S138	
SN74S139	AMD	SN74S139	
	Fairchild	74S139	
	National	DM74S139	
	Signetics	74S139	
SN74S140	Fairchild	74S140	
	Hitachi	HD74S140	
	National	DM74S140	
	Signetics	74S140	
SN74S15	Fairchild	74S15	
	Hitachi	HD74S15	
	Mitsubishi	M5S015	
	National	DM74S15	
	Signetics	74S15	
SN74S151	AMD	SN74S151	
	Fairchild	74S151	
	Hitachi	HD74S151	
	Mitsubishi	M5S151	
	National	DM74S151	
	Signetics	74S151	
SN74S153	AMD	SN74S153	
	Fairchild	74S153	
	Hitachi	HD74S153	
	Mitsubishi	M5S153	
	National	DM74S153	
	Signetics	74S153	
SN74S157	AMD	SN74S157	
	Fairchild	74S157	
	Hitachi	HD74S157	
	Mitsubishi	M5S157	
	National	DM74S157	
	Signetics	74S157	
SN74S158	AMD	SN74S158	
	Fairchild	74S158	
	Hitachi	HD74S158	
	Mitsubishi	M5S158	
	National	DM74S158	
	Signetics	74S158	
SN74S174	AMD	SN74S174	
	Fairchild	74S174	
	Hitachi	HD74S174	
	Mitsubishi	M5S174	
	National	DM74S174	
	Signetics	74S174	
SN74S175	AMD	SN74S175	
	Fairchild	74S175	
	Hitachi	HD74S175	
	Mitsubishi	M5S175	
	National	DM74S175	
	Signetics	74S175	
SN74S181	AMD	SN74S181	
	Fairchild	93S41	
	Hitachi	HD74S181	
	Mitsubishi	M5S181	
	Signetics	74S181	
SN74S182	Fairchild	93S42	
	Hitachi	HD74S182	
	Mitsubishi	M5S182	
	MMI	74S182	
	National	DM74S182	
	Signetics	74S182	
SN74S188	AMD	AM27S18	
	Harris	**HM7602**	**1284**
	MMI	6330	
		6330-1	**1449**
SN74S188	National	DM74S188	
	Signetics	**N82S23**	**1680**
	Supertex	**SM74S188**	**1704**
SN74S189	AMD	AM27S03	
		SN74S189	
	Fairchild	74S189	
	Hitachi	HD74S189	
	National	DM74S189	
SN74S194	AMD	SN74S194	
	Fairchild	74S194	
	Signetics	74S194	
SN74S195	AMD	SN74S195	
	Fairchild	93S00	
	National	DM74S195	
	Signetics	74S195	
SN74S197	Signetics	74S197	
SN74S20	Fairchild	74S20	
	Hitachi	HD74S20	
	Mitsubishi	M5S020	
	National	DM74S20	
	Signetics	74S20	
SN74S200	**Fairchild**	**93421**	**1252**
	MMI	6531	
	National	DM74S200	
	NEC Micro	μPB2200	
	Raytheon	RC5340	
	Signetics	**74S200**	**1678**
	TI	SN74S201	
SN74S201	MMI	6531	
	National	DM74S200	
	Signetics	**74S201**	**1678**
SN74S206	**MMI**	**6205-1**	**1466**
	National	DM74S206	
	Raytheon	RC5330	
	Signetics	**N82S17**	**1678**
	TI	SN74S301	
SN74S214	**Fairchild**	**93425**	**1240**
SN74S22	Fairchild	74S22	
	Hitachi	HD74S22	
	Mitsubishi	M5S22	
	National	DM74S22	
	Signetics	74S22	
SN74S240	AMD	SN74S240	
	Fairchild	74S240	
	MMI	**74S240**	**768**
	Raytheon	74S240	
SN74S241	AMD	SN74S241	
	Fairchild	74S241	
	MMI	**74S241**	**768**
	Raytheon	74S241	
SN74S244	Fujitsu	MB7047	
	MMI	**74S244**	**768**
SN74S251	AMD	SN74S251	
	Fairchild	74S251	
	Hitachi	HD74S251	
	Mitsubishi	M5S251	
	National	DM74S251	
	Signetics	74S251	
SN74S257	AMD	SN54S257	
		SN74S257	
	Fairchild	54S257	
		74S257	
	Hitachi	HD74S257	
	Mitsubishi	M5S257	
	National	DM74S257	
	Signetics	54S257	
		74S257	
SN74S258	AMD	SN74S258	
	Fairchild	74S258	
	Hitachi	HD74S258	
	Mitsubishi	M5S258	
	Signetics	74S258	
SN74S270	Intersil	IM5604	
	MMI	**6205-1**	**1466**
SN74S280	Hitachi	HD74S280	
	National	DM74S280	
	Signetics	74S280	
SN74S281	National	DM74S281	
SN74S283	MMI	74S283	
SN74S287	AMD	AM27S21	
	Fairchild	**93427**	**1258**
	Harris	**HM7611**	
			1284,1292
		HM7611A	
	Intel	3621-1	
	Intersil	IM5623	
SN74S287	**MMI**	**6301-1**	**1449**
	National	DM74S287	
	Raytheon	**29661**	**1664**
	Signetics	**N82S129**	**1680**
SN74S288	AMD	AM27S19	
	Harris	**HM7603**	**1284**
	MMI	**6331-1**	**1449**
	National	DM74S288	
		DM8578	
	Signetics	**N82S123**	**1680**
	Supertex	**SM74S288**	**1704**
SN74S289	AMD	SN74S289	
	Fairchild	74S289	
	Hitachi	HD74S289	
	National	DM74S289	
	NEC Micro	μPB2289	
	Signetics	**N82S25**	**1678**
		3101A	
SN74S30	Fairchild	74S30	
	Mitsubishi	M5S030	
	National	DM74S30	
SN74S301	Fairchild	93411	
	National	DM74S206	
	Signetics	**74S301**	**1678**
SN74S314	**Fairchild**	**93415**	**1240**
	Fujitsu	MBM93415	
SN74S32	Fairchild	74S02	
	National	DM74S02	
	Signetics	74S02	
SN74S37	Signetics	74S37	
SN74S370	**MMI**	**6206-1**	**1466**
SN74S373	**MMI**	**74S373**	**505**
	TI	SN74S02	
SN74S374	**MMI**	**74S374**	**505**
SN74S387	AMD	AM27S20	
	Harris	**HM7610**	
			1284,1292
		HM7610A	
	MMI	**6300-1**	**1449**
	National	DM74S387	
	NEC Micro	μPB403	
	Raytheon	**29660**	**1664**
	Signetics	**N82S126**	**1680**
SN74S40	Fairchild	74S40	
	Hitachi	HD74S40	
	Mitsubishi	M5S040	
	National	DM74S40	
	Signetics	74S40	
SN74S412	AMD	SN74S412	
	NEC Micro	**μPB8212**	**2172**
		μPD8212	
SN74S428	**NEC Micro**	**μPB8228**	**2193**
SN74S438	**NEC Micro**	**μPB8238**	**2193**
SN74S44	**NEC Micro**	**μPB425**	**1621**
SN74S470	**MMI**	**6308-1**	**1449**
	National	DM74S470	
	Raytheon	**29600**	**1652**
SN74S471	**MMI**	**6309-1**	**1449**
	National	DM74S471	
	Raytheon	**29601**	**1652**
SN74S472	**Harris**	**HM7649**	**1320**
	MMI	**6349-1**	**1449**
	National	DM74S472	
	Raytheon	**29621**	**1656**
SN74S473	**Harris**	**HM7648**	**1320**
	MMI	**6348-1**	**1449**
	National	DM74S473	
	Raytheon	**29620**	**1656**
SN74S474	**Fairchild**	**93448**	**1262**
	MMI	**6341-1**	**1449**
	National	DM87S296	
	Raytheon	**29625**	**1658**
SN74S475	Fairchild	93428	1262
		93452	1264
	MMI	**6340-1**	**1449**
	NEC Micro	**μPB405**	**1621**
	Raytheon	**29624**	**1658**
SN74S476	**Fairchild**	**93453**	**1264**
	MMI	**63S441**	**1453**
	Raytheon	29641	
SN74S477	**MMI**	**63S440**	**1453**
	Raytheon	29640	
SN74S478	**MMI**	**6381-1**	**1449**
	Signetics	**N82S181**	**1680**
SN74S479	**MMI**	**6380-1**	**1449**
	Signetics	**N82S180**	**1680**

♦ Discontinued

Bold face device numbers indicate manufacturers data is provided in the IC Master on the pages noted.

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Manufacturer Device	Replacement Source	Device	IC Master Page
SN74S51	Fairchild	74S51	
	Hitachi	HD74S51	
	Mitsubishi	M5S051	
	National	DM74S51	
	Signetics	74S51	
SN74S570	**Signetics**	**N82S130**	**1680**
SN74S571	Signetics	82S131	
SN74S64	Fairchild	74S64	
	Hitachi	HD74S64	
	National	DM74S64	
	Signetics	74S64	
SN74S65	Fairchild	74S65	
	Hitachi	HD74S65	
	National	DM74S65	
	Signetics	74S65	
SN74S74	Fairchild	74S74	
	Hitachi	HD74S74	
	Mitsubishi	M5S074	
	National	DM74S74	
	Signetics	74S74	
SN74S85	Mitsubishi	M5S085	
	Signetics	74S85	
SN74S86	Fairchild	74S86	
	Hitachi	HD74S86	
	National	DM74S86	
	Signetics	74S86	
SN7400	Fairchild	7400	
	Hitachi	HD7400	
	Mitsubishi	M53200	
	Motorola	MC7400	
	National	DM7400	
	NEC America	μPB7400	
	Signetics	7400	
	Toshiba	TC7400	
		TD3400	
	TRW	7400	
SN7401	Fairchild	7401	
	Hitachi	HD7401	
	Mitsubishi	M53201	
	Motorola	MC7401	
	National	DM7401	
	Signetics	7401	
	Toshiba	TD3401	
	TRW	7401	
SN7402	Fairchild	7402	
	Hitachi	HD7402	
	Mitsubishi	M53202	
	Motorola	MC7402	
	National	DM7402	
	NEC America	μPB7402	
	Signetics	7402	
	Toshiba	TD3402	
	TRW	7402	
SN7403	Fairchild	7403	
	Hitachi	HD7403	
	Mitsubishi	M53203	
	Motorola	MC7403	
	National	DM7403	
	Signetics	7403	
	Toshiba	TD3403	
	TRW	7403	
SN7404	Fairchild	7404	
	Hitachi	HD7404	
	Mitsubishi	M53204	
	Motorola	MC7404	
	National	DM7404	
	NEC America	μPB7404	
	Signetics	7404	
	Toshiba	TC7404	
		TD3404	
	TRW	7404	
SN7405	Fairchild	7405	
	Hitachi	HD7405	
	Mitsubishi	M53205	
	Motorola	MC7405	
	National	DM7405	
	NEC America	μPB7405	
	Signetics	7405	
	Toshiba	TD3405	
	TRW	7405	
SN7406	Fairchild	7406	
	Hitachi	HD7406	
	Mitsubishi	M53206	
SN7406	Motorola	MC7406	
	National	DM7406	
	Signetics	7406	
	Toshiba	TD3406	
	TRW	7406	
SN7407	Fairchild	7407	
	Hitachi	HD7407	
	Mitsubishi	M53207	
	Motorola	MC7407	
	National	DM7407	
	Signetics	7407	
	Toshiba	TD3407	
	TRW	7407	
SN7408	Fairchild	7408	
	Hitachi	HD7408	
	Mitsubishi	M53208	
	Motorola	MC7408	
	National	DM7408	
	Signetics	7408	
	Toshiba	TC7408	
		TD3408	
	TRW	7408	
SN7409	Fairchild	7409	
	Hitachi	HD7409	
	Mitsubishi	M53209	
	Motorola	MC7409	
	National	DM7409	
	Signetics	7409	
	Toshiba	TD3409	
	TRW	7409	
SN7410	Fairchild	7410	
	Hitachi	HD7410	
	Mitsubishi	M53210	
	Motorola	MC7410	
	National	DM7410	
	NEC America	μPB7410	
	Signetics	7410	
	TI	SN7427	
	Toshiba	TC7410	
		TD3410	
	TRW	7410	
SN74100	Motorola	MC74100	
	Signetics	74100	
♦SN74104	TI	SN29000	
♦SN74105	TI	SN29001	
SN74107	AMD	SN74107	
	Fairchild	74107	
	Hitachi	HD74107	
	Mitsubishi	M53307	
	Motorola	MC74107	
	National	DM74107	
	NEC America	μPB74107	
	Signetics	74107	
	Toshiba	TD34107	
SN74109	Fairchild	9024	
	National	DM74109	
	Signetics	74109	
SN74111	TRW	74111	
SN74116	Fairchild	74116	
	Signetics	74116	
SN7412	Fairchild	7412	
	Hitachi	HD7412	
	Motorola	MC7412	
	Signetics	7412	
	TRW	7412	
SN74120	Motorola	MC74120	
SN74121	Fairchild	74121	
		9603	
	Hitachi	HD74121	
	Mitsubishi	M53321	
	Motorola	MC74121	
	National	DM74121	
	Signetics	74121	
	Toshiba	TD34121	
	TRW	74121	
SN74122	Fairchild	74122	
	Mitsubishi	M53322	
	Motorola	MC74122	
	National	DM74122	
	Signetics	74122	
		8T22	
SN74123	AMD	AM26123	
		SN74123	
	Fairchild	74123	
	Hitachi	HD7123	
	Mitsubishi	M53323	
SN74123	Motorola	MC74123	
	National	DM74123	
	NEC America	μPB74123	
	Signetics	74123	
	TRW	74123	
SN74125	Fairchild	74125	
	Hitachi	HD74125	
	Mitsubishi	M53325	
	National	DM74125	
		DM8093	
	Signetics	74125	
SN74126	Fairchild	74126	
	Hitachi	HD74126	
	Mitsubishi	M53326	
	National	DM74126	
	Signetics	74126	
SN74128	Signetics	74128	
SN74129	National	DM74193	
SN7413	Fairchild	7413	
	Hitachi	HD7413	
	Mitsubishi	M53213	
	Motorola	MC7413	
	National	DM7413	
	NEC America	μPB7413	
	Signetics	7413	
	TRW	7413	
SN74132	Fairchild	74132	
	Hitachi	HD74132	
	Mitsubishi	M53332	
	Motorola	MC74132	
	National	DM74132	
	Signetics	74132	
SN74136	Hitachi	HD74136	
	Motorola	MC74136	
	TRW	74136	
SN7414	Fairchild	7414	
	Hitachi	HD7414	
	Mitsubishi	M53214	
	Motorola	MC7414	
	National	DM7414	
	Signetics	7414	
SN74141	Fairchild	74141	
	Hitachi	HD74141	
	Motorola	MC74141	
	National	DM74141	
		DM7441	
	NEC America	μPB74141	
	Signetics	74141	
		7441	
SN74145	Fairchild	74145	
	Hitachi	HD74145	
	Mitsubishi	M53345	
	Motorola	MC74145	
	National	DM74145	
	Signetics	74145	
	TRW	74145	
SN74147	Hitachi	HD74147	
	Mitsubishi	M53347	
	National	DM74147	
	NEC America	μPB74147	
	Signetics	74147	
SN74148	Fairchild	9318	
	Hitachi	HD74148	
	Mitsubishi	M53348	
	National	DM74148	
	NEC America	μPB74148	
	Signetics	74148	
SN74150	Fairchild	74150	
	Hitachi	HD74150	
	Mitsubishi	M53350	
	Motorola	MC74150	
	National	DM74150	
	NEC America	μPB74150	
	Signetics	74150	
	TRW	74150	
♦SN74151	Fairchild	74151	
	Hitachi	HD74151	
	Mitsubishi	M53351	
	Motorola	MC74151	
	National	DM74151	
	NEC America	μPB74151	
	Signetics	74151	
	TI	SN74151A	
	TRW	74151	
♦SN74152	Fairchild	74152	
	Motorola	MC74152	
♦SN74152	TRW	74152	
SN74153	AMD	SN74153	
	Fairchild	74153	
	Hitachi	HD74153	
	Mitsubishi	M53353	
	Motorola	MC74153	
	National	DM74153	
	NEC America	μPB74153	
	Signetics	74153	
	TRW	74153	
SN74154	AMD	SN74154	
	Fairchild	74154	
	Hitachi	HD74154	
	Mitsubishi	M53354	
	Motorola	MC74154	
	National	DM74154	
	NEC America	μPB74154	
	Signetics	74154	
	TRW	74154	
SN74155	Fairchild	74155	
	Mitsubishi	M53355	
	Motorola	MC74155	
	National	DM74155	
	NEC America	μPB74155	
	Signetics	74155	
	TRW	74155	
SN74156	Fairchild	74156	
	Hitachi	HD74156	
	Mitsubishi	M53356	
	Motorola	MC74156	
	National	DM74156	
	NEC America	μPB74156	
	Signetics	74156	
	TRW	74156	
SN74157	AMD	SN74157	
	Fairchild	74157	
		9322	
	Hitachi	HD74157	
	Mitsubishi	M53357	
	Motorola	MC74157	
	National	DM74157	
		DM8322	
	NEC America	μPB74157	
	Signetics	74157	
SN7416	Fairchild	7416	
	Hitachi	HD7416	
	Mitsubishi	M53216	
	Motorola	MC7416	
	National	DM7416	
	Signetics	7416	
	Toshiba	TD3416	
	TRW	7416	
SN74160	AMD	SN74160	
	Fairchild	74160	
		9310	
	Hitachi	HD74160	
	Mitsubishi	M53360	
	Motorola	MC74160	
	National	DM74160	
	Signetics	74160	
	TRW	74160	
SN74161	AMD	SN74161	
	Fairchild	74161	
		9316	
	Hitachi	HD74161	
	Mitsubishi	M53361	
	Motorola	MC74161	
	National	DM74161	
	NEC America	μPB74161	
	Signetics	74161	
	TRW	74161	
SN74162	AMD	SN74162	
	Fairchild	74162	
	Hitachi	HD74162	
	Mitsubishi	M53362	
	Motorola	MC74162	
	National	DM74162	
	Signetics	74162	
	TRW	74162	
SN74163	AMD	SN74163	
	Fairchild	74163	
	Hitachi	HD74163	
	Mitsubishi	M53363	
	Motorola	MC74163	
	National	DM74163	
	Signetics	74163	

♦ Discontinued

The manufacturers report their devices can be used as direct replacements.
Performance details often differ, so compare the specifications considering your requirements.

Texas Instruments (cont'd)

Manufacturer Device	Replacement Source	Device	IC Master Page
SN74163	TRW	74163	
SN74164	AMD	SN74164	
		74164	
	Fairchild	74164	
	Hitachi	HD74164	
	Mitsubishi	M53364	
	National	DM74164	
		DM8570	
	NEC America	μPB74164	
	Signetics	74164	
SN74165	Fairchild	74165	
	Mitsubishi	M53365	
	Motorola	MC74165	
	National	DM74165	
		DM8590	
	Signetics	74165	
SN74166	Fairchild	74166	
	Hitachi	HD74166	
	Mitsubishi	M53366	
	Motorola	MC74166	
	National	DM74166	
	Signetics	74166	
SN74167	Motorola	MC74167	
SN7417	Fairchild	7417	
	Hitachi	HD7417	
	Mitsubishi	M53217	
	Motorola	MC7417	
	National	DM7417	
	Signetics	7417	
	Toshiba	TD3417	
	TRW	7417	
SN74170	Fairchild	74170	
	Hitachi	HD74170	
	Mitsubishi	M53370	
	National	DM74170	
	NEC America	μPB74170	
	Signetics	74170	
SN74172	Signetics	74172	
SN74173	Fairchild	74173	
	National	DM74173	
		DM8551	
SN74174	AMD	SN74174	
	Fairchild	74174	
	Hitachi	HD74174	
	Mitsubishi	M53374	
	Motorola	MC74174	
	National	DM74174	
	Signetics	74174	
SN74175	AMD	SN74175	
	Fairchild	74175	
	Hitachi	HD74175	
	Mitsubishi	M53375	
	Motorola	MC74175	
	National	DM74175	
	NEC America	μPB74175	
	Signetics	74175	
SN74176	Fairchild	74176	
	Mitsubishi	M53376	
	Motorola	MC74176	
	National	DM74176	
		DM8280	
	Signetics	N8280	
		74176	
SN74177	Fairchild	74177	
	Mitsubishi	M53377	
	Motorola	MC74177	
	National	DM74177	
		DM8281	
	Signetics	N8281	
		74177	
SN74178	Fairchild	74178	
	Motorola	MC74178	
	Signetics	N8270	
SN74179	Fairchild	74179	
	Motorola	MC74179	
	Signetics	N8271	
SN74180	Fairchild	74180	
	Hitachi	HD74180	
	Mitsubishi	M53380	
	Motorola	MC74180	
	National	DM74180	
	NEC America	μPB74180	
	Signetics	74180	
SN74180	TRW	74180	
SN74181	AMD	SN74181	
		9341	
	Fairchild	74181	
		9341	
	Hitachi	HD74181	
	Mitsubishi	M53381	
	Motorola	MC74181	
	National	DM74181	
	NEC America	μPB74181	
	Signetics	74181	
SN74182	AMD	SN74182	
		9342	
	Fairchild	74182	
		9342	
	Hitachi	HD74182	
	Mitsubishi	M53382	
	Motorola	MC74182	
	National	DM74182	
	NEC America	μPB74182	
	Signetics	74182	
SN74184	National	DM74184	
	Toshiba	TD3503	
SN74185	Mitsubishi	M53385	
	National	DM74185	
SN74185A	National	DM74185A	
SN74186	**Harris**	**HPROM0512**	
			1346
SN74187	Intersil	IM5603	
	MMI	**6200-1**	**1466**
	National	DM74187	
	Signetics	N82S226	
SN74188	AMD	AM27S18	
	Harris	HPROM8256	
	Intersil	IM5600	
	MMI	**6330-1**	**1449**
	National	DM8577	
	Signetics	**N82S23**	**1680**
	TI	SN74188A	
SN74190	Fairchild	74190	
	Hitachi	HD74190	
	Mitsubishi	M53390	
	Motorola	MC74190	
	National	DM74190	
	Signetics	74190	
SN74191	Fairchild	74191	
	Hitachi	HD74191	
	Mitsubishi	M53391	
	Motorola	MC74191	
	National	DM74191	
	Signetics	74191	
SN74192	AMD	SN74192	
		9360	
	Fairchild	74192	
	Mitsubishi	M53392	
	Motorola	MC74192	
	National	DM74192	
		DM8560	
	NEC America	μPB74192	
	Signetics	74192	
	Toshiba	TD34192	
SN74193	AMD	SN74193	
		9366	
	Fairchild	74193	
	Mitsubishi	M53393	
	Motorola	MC74193	
	National	DM74193	
		DM8563	
	NEC America	μPB74193	
	Signetics	74193	
	Toshiba	TD34193	
SN74194	AMD	SN74194	
	Fairchild	74194	
	Hitachi	HD74194	
	Motorola	MC74194	
	National	DM74194	
	Signetics	74194	
SN74195	AMD	SN74195	
	Fairchild	74195	
		9300	
	Motorola	MC74195	
	National	DM74195	
		DM8300	
	NEC America	μPB74195	
	Signetics	74195	
SN74196	Fairchild	74196	
SN74196	Motorola	MC74196	
	National	DM74196	
	Signetics	N8290	
		74196	
SN74197	Fairchild	74197	
	Motorola	MC74197	
	National	DM74197	
	Signetics	N8291	
		74197	
SN74198	Fairchild	74198	
	Hitachi	HD74198	
	Mitsubishi	M53398	
	Motorola	MC74198	
	National	DM74198	
	NEC America	μPB74198	
	Signetics	74198	
SN74199	Fairchild	74199	
	Mitsubishi	M53399	
	Motorola	MC74199	
	National	DM74199	
	Signetics	74199	
SN7420	Fairchild	7420	
	Hitachi	HD7420	
	Mitsubishi	M53220	
	Motorola	MC7420	
	National	DM7420	
	NEC America	μPB7420	
	Signetics	7420	
	Toshiba	TC7420	
		TD3420	
	TRW	7420	
SN74200	MMI	6531	
	Raytheon	RC5340	
	Signetics	74200	
	TI	SN74S201	
SN74206	MMI	6530	
	National	DM74S206	
	Raytheon	RC5330	
	TI	SN74S301	
SN7421	Toshiba	TD3421	
SN7422	Fairchild	7422	
	Hitachi	HD7422	
SN74221	AMD	SN74221	
SN7423	Fairchild	7423	
	Motorola	MC7423	
	National	DM7423	
SN7425	Fairchild	7425	
	Mitsubishi	M53225	
	Motorola	MC7425	
	National	DM7425	
SN74251	National	DM74251	
SN74259	AMD	SN74259	
SN7426	Fairchild	7426	
	Hitachi	HD7426	
	Motorola	MC7426	
	National	DM7426	
	Signetics	N8T18	
		7426	
	Toshiba	TD3426	
	TRW	7426	
SN7427	Fairchild	7410	
		7427	
	Hitachi	HD7410	
	Mitsubishi	M53210	
	Motorola	MC7410	
		MC7427	
	National	DM7410	
		DM7427	
	NEC America	μPB7410	
	Signetics	7410	
	TI	SN7410	
	Toshiba	TC7410	
	TRW	7410	
SN74270	**MMI**	**6205-1**	**1466**
SN74278	Mitsubishi	M53478	
SN74279	Fairchild	74279	
	Signetics	74279	
SN7428	Signetics	7428	
SN74283	Fairchild	74283	
	Mitsubishi	M53483	
	NEC America	μPB74283	
SN74284	National	DM8875A	
SN74285	National	DM8875B	
SN74287	Fairchild	93426	
SN74290	Fairchild	74290	
	Mitsubishi	M53490	
SN74290	Motorola	MC74290	
	TRW	74290	
SN74293	Fairchild	74293	
	Mitsubishi	M53493	
	Motorola	MC74293	
	TRW	74293	
SN74298	Fairchild	74298	
	Motorola	MC74298	
	Signetics	74298	
SN7430	Fairchild	7430	
	Hitachi	HD7430	
	Mitsubishi	M53230	
	Motorola	MC7430	
	National	DM7430	
	NEC America	μPB7430	
	Signetics	7430	
	Toshiba	TD3430	
	TRW	7430	
SN7432	Fairchild	7432	
	Hitachi	HD7432	
	National	DM7432	
	Signetics	7432	
SN7433	Signetics	7433	
SN74365	National	DM8095	
SN74366	National	DM8096	
SN74367	National	DM8097	
SN74368	National	DM8098	
SN7437	Fairchild	7437	
	Hitachi	HD7437	
	Mitsubishi	M53237	
	Motorola	MC7437	
	National	DM7437	
	NEC America	μPB7437	
	Signetics	7437	
	Toshiba	TD3437	
	TRW	7437	
SN74370	**MMI**	**6206-1**	**1466**
SN7438	Fairchild	7438	
	Hitachi	HD7438	
	Mitsubishi	M53238	
	Motorola	MC7438	
	National	DM7438	
	NEC America	μPB7438	
	Signetics	7438	
	Toshiba	TD3438	
	TRW	7438	
SN74387	Fairchild	93416	
SN7440	Fairchild	7440	
	Hitachi	HD7440	
	Mitsubishi	M53240	
	Motorola	MC7440	
	National	DM7440	
	NEC America	μPB7440	
	Signetics	7440	
	Toshiba	TD3440	
	TRW	7440	
SN7441	Toshiba	TD3441	
♦SN7441A	National	DM7441A	
	TI	SN74141	
♦SN7442	Fairchild	7442	
	Hitachi	HD7442	
	Mitsubishi	M53242	
	Motorola	MC7442	
	National	DM7442	
	NEC America	μPB7442	
	Signetics	7442	
	TI	SN7442A	
	Toshiba	TD3442	
♦SN7443	Fairchild	7443	
	Hitachi	HD7443	
	Mitsubishi	M53243	
	Motorola	MC7443	
	Signetics	7443	
	TI	SN7443A	
♦SN7444	Fairchild	7444	
		9354	
	Hitachi	HD7444	
	Mitsubishi	M53244	
	Motorola	MC7444	
	Signetics	7444	
	TI	SN7444A	
SN7445	Fairchild	7445	
	Hitachi	HD7445	
	Mitsubishi	M53245	
	Motorola	MC7445	
	National	DM7445	

♦ Discontinued

Bold face device numbers indicate manufacturers data is provided in the IC Master on the pages noted.

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Manufacturer Device	Replacement Source	Device	IC Master Page
SN7445	NEC America	μPB7445	
	Signetics	7445	
	TRW	7445	
♦SN7446	Fairchild	7446	
	Hitachi	HD7446	
	Motorola	MC7446	
	National	DM7446	
	Signetics	7446	
	TI	SN7446A	
♦SN7447	Fairchild	7447	
	Hitachi	HD7447	
	Mitsubishi	M53247	
	Motorola	MC7447	
	National	DM7447	
	NEC America	μPB7447	
	Signetics	7447	
	TI	SN7447A	
	Toshiba	TD3447	
SN7448	Fairchild	7448	
	Mitsubishi	M53248	
	Motorola	MC7448	
	National	DM7448	
	Signetics	7448	
SN7449	Fairchild	7449	
	Motorola	MC7449	
SN7450	Fairchild	7450	
		9N50	
	Hitachi	HD7450	
	Mitsubishi	M53250	
	Motorola	MC7450	
	National	DM7450	
	NEC America	μPB7450	
	Signetics	7450	
	Toshiba	TD3450	
	TRW	7450	
SN7451	Fairchild	7451	
	Hitachi	HD7451	
	Motorola	MC7451	
	National	DM7451	
	NEC America	μPB7451	
	Signetics	7451	
	Toshiba	TD3451	
	TRW	7451	
SN7453	Fairchild	7453	
	Hitachi	HD7453	
	Mitsubishi	M53253	
	Motorola	MC7453	
	National	DM7453	
	NEC America	μPB7453	
	Signetics	7453	
	TRW	7453	
SN7454	Fairchild	7454	
	Hitachi	HD7454	
	Motorola	MC7454	
	National	DM7454	
	NEC America	μPB7454	
	Signetics	7454	
	TRW	7454	
SN745475	National	DM87S295	
SN7460	Fairchild	7460	
	Hitachi	HD7460	
	Mitsubishi	M53260	
	Motorola	MC7460	
	National	DM7460	
	NEC America	μPB7460	
	Signetics	7460	
	Toshiba	TD3460	
	TRW	7460	
SN7470	Fairchild	7470	
	Hitachi	HD7470	
	Mitsubishi	M53270	
	Motorola	MC7470	
	National	DM7470	
	Signetics	7470	
SN7472	Fairchild	7472	
	Hitachi	HD7472	
	Mitsubishi	M53272	
	Motorola	MC7472	
	National	DM7472	
	Signetics	7472	
	Toshiba	TD3472	
	TRW	7472	
SN7473	Fairchild	7473	
SN7473	Hitachi	HD7473	
	Mitsubishi	M53273	
	Motorola	MC7473	
	National	DM7473	
	NEC America	μPB7473	
	Signetics	7473	
	Toshiba	TD3473	
SN7474	Fairchild	7474	
	Hitachi	HD7474	
	Mitsubishi	M53274	
	Motorola	MC7474	
	National	DM7474	
	NEC America	μPB7474	
	Signetics	7474	
	Toshiba	TD3474	
	TRW	7474	
SN7475	Fairchild	7475	
	Hitachi	HD7475	
	Mitsubishi	M53275	
	Motorola	MC7475	
	National	DM7475	
	Signetics	7475	
	Toshiba	TD3475	
	TRW	7475	
SN7476	Fairchild	7476	
		9N76	
	Hitachi	HD7476	
	Mitsubishi	M53276	
	Motorola	MC7476	
	National	DM7476	
	NEC America	μPB7476	
	Signetics	7476	
	Toshiba	TD3476	
	TRW	7476	
♦SN7477	Fairchild	7477	
	Motorola	MC7477	
	Signetics	7477	
♦SN7480	Fairchild	7480	
	Mitsubishi	M53280	
	Motorola	MC7480	
	NEC America	μPB7480	
	Signetics	7480	
		8268	
	Toshiba	TD3480	
♦SN7481	Fairchild	93407	
	Hitachi	HM2501	
	Motorola	MC4004	
	TI	SN7481A	
	TRW	7481	
SN7482	Fairchild	7482	
	Hitachi	HD7482	
	Motorola	MC7482	
	National	DM7482	
♦SN7483	Fairchild	7483	
	Hitachi	HD7483	
	Mitsubishi	M53283	
	Motorola	MC7483	
	National	DM7483	
	Signetics	7483	
	TI	SN7483A	
♦SN7484	Mitsubishi	M53284	
	TI	SN7484A	
SN7485	Fairchild	7485	
	Hitachi	HD7485	
	Mitsubishi	M53285	
	Motorola	MC7485	
	National	DM7485	
	NEC America	μPB7485	
	Signetics	7485	
	TRW	7485	
SN7486	Fairchild	7486	
	Hitachi	HD7486	
	Mitsubishi	M53286	
	Motorola	MC7486	
	National	DM7486	
	NEC America	μPB7486	
	Signetics	7486	
	Toshiba	TD3486	
	TRW	7486	
♦SN7488	Intersil	IM5600	
	MMI	**6230-1**	**1466**
	Motorola	MCM4002	
	National	DM7488	
	TI	SN7488A	
SN7489	AMD	SN7489	
	Fairchild	7489	
SN7489	Hitachi	HM2502	
	Mitsubishi	M53289	
	National	DM7489	
	NEC Micro	μPB2089	
	TRW	7489	
♦SN7490	Fairchild	7490	
	Hitachi	HD7490	
	Mitsubishi	M53290	
	Motorola	MCM4023	
		MC7490	
	National	DM7490	
	Signetics	7490	
	TI	SN7490A	
	Toshiba	TD3490	
	TRW	7490	
♦SN7491	Fairchild	7491	
	Hitachi	HD7491	
	Mitsubishi	M53291	
	Motorola	MC7491	
	National	DM7491	
	NEC America	μPB7491	
	Signetics	7491	
	TI	SN7491A	
	Toshiba	TD3491	
♦SN7492	Fairchild	7492	
	Hitachi	HD2521	
		HD7492	
	Motorola	MC7492	
	National	DM7492	
	Signetics	7492	
	TI	SN7492A	
	Toshiba	TD3492	
	TRW	7492	
♦SN7493	Fairchild	7493	
	Hitachi	HD7493	
	Mitsubishi	M53293	
	Motorola	MC7493	
	National	DM7493	
	Signetics	7493	
	TI	SN7493A	
	Toshiba	TD3492	
	TRW	7493	
SN7494	Fairchild	7494	
	Hitachi	HD7494	
	Motorola	MC7494	
	Signetics	7494	
♦SN7495	Fairchild	7495	
	Hitachi	HD7495	
	Mitsubishi	M53295	
	Motorola	MC7495	
	National	DM7495	
	Signetics	7495	
	TI	SN7495A	
	Toshiba	TD3495	
SN7496	Fairchild	7496	
	Hitachi	HD7496	
	Mitsubishi	M53296	
	Motorola	MC7496	
	National	DM7496	
	Signetics	7496	
	TRW	7496	
SN7497	Fairchild	7497	
	Motorola	MC7497	
♦SN7510	Motorola	MC1410	
SN75107	AMD	SN75107	
	Fairchild	75107	
	Motorola	MC75107	
	National	DS75107	
	Raytheon	RC75107A	
SN75107A	Hitachi	HD75107A	
SN75108	AMD	SN74108	
	Fairchild	75108	
	Motorola	MC75108	
	National	DS75108	
	Raytheon	RC75108A	
SN75108A	Hitachi	HD75108A	
SN75109	AMD	SN75109	
	Fairchild	75109	
	Hitachi	HD75109	
	Raytheon	RC75109	
SN75110	AMD	SN75110	
	Fairchild	75110	
	Hitachi	HD75110	
	Motorola	MC75110	
	Raytheon	RC75110	
SN75112	Fairchild	75112	
SN75114	AMD	9614	
	Fairchild	9614	
SN75115	AMD	9615	
	Fairchild	9615	
SN75121	Fairchild	75121	
	Motorola	MC8T13	
	National	DS75121	
SN75122	Fairchild	75122	
	Motorola	MC8T14	
	National	DS75122	
SN75123	Fairchild	75123	
	Motorola	MC8T23	
	National	DS75123	
SN75124	Fairchild	75124	
	Motorola	MC8T24	
SN75125	Motorola	MC75125	
	National	DS75125	
SN75127	Motorola	MC75127	
SN75128	Motorola	MC75128	
SN75129	Motorola	MC75129	
SN75138	Silicon G	SG75138	
SN75140	Motorola	MC75140	
SN75150	Fairchild	75150	
	Raytheon	RC75150	
SN75152	Fairchild	9627	
SN75154	Fairchild	75154	
	Hitachi	HD75154	
	National	DS75154	
	Raytheon	RC75154	
SN75180	National	DS8800	
SN75182	AMD	DM8820	
	National	DS8820	
	Signetics	DS8820	
SN75183	AMD	DM8830	
	National	DS8830	
	Signetics	DS8830	
SN75188	AMD	MC1488	
	Hitachi	HD75188	
	Motorola	MC1488	
	National	DS1488	
	Signetics	MC1488	
SN75189	AMD	MC1489	
	Hitachi	HD75189	
	Motorola	MC1489	
	National	DS1489	
	Signetics	MC1489	
SN75189A	Exar	XR1489A	
SN7520	AMD	SN7520	
		SN7521	
	Motorola	MC7520	
	National	DS7520	
	Signetics	7520	
	Silicon G	SG7520	
SN75207	AMD	SN75207	
	Fairchild	75207	
SN75208	AMD	SN75208	
	Fairchild	75208	
♦SN7521	AMD	SN7521	
	Motorola	MC7521	
	National	DS7521	
	Signetics	7521	
	Silicon G	SG7521	
SN7522	Signetics	7522	
	Silicon G	SG7522	
SN75224	Fairchild	75224	
SN7523	Signetics	7523	
	Silicon G	SG7523	
SN75234	AMD	SN75234	
	Fairchild	75S234	
SN75235	AMD	SN75235	
	Motorola	MC75235	
SN75238	AMD	SN75238	
	Fairchild	75238	
SN75239	AMD	SN75239	
SN7524	AMD	SN7524	
		7525	
	Fairchild	7524	
	Hitachi	HA1902	
	Motorola	MC7524	
	National	75S24	
	Signetics	7524	
	Silicon G	SG7524	
♦SN7525	AMD	SN7525	
	Motorola	MC7525	
	Signetics	7525	
	Silicon G	SG7525	

♦ Discontinued

The manufacturers report their devices can be used as direct replacements.
Performance details often differ, so compare the specifications considering your requirements.

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Manufacturer Device	Replacement Source	Device	IC Master Page
SN7528	Fairchild	7528	
	Motorola	MC7528	
	National	DS7528	
	Silicon G	SG7528	
♦SN7529	Motorola	MC7529	
	Silicon G	SG7529	
SN75324	National	DS75324	
	Raytheon	RC75324	
SN75325	AMD	SN75325	
	Fairchild	75325	
	Motorola	MC75325	
	National	DS75325	
	Raytheon	RC75325	
	Silicon G	SG75325	
SN75326	Fairchild	75326	
SN75327	Fairchild	75327	
♦SN7534	National	DS7534	
	Silicon G	SG7534	
♦SN7535	Fairchild	7535	
	Silicon G	SG7535	
SN75361	National	DS75361	
SN75362	National	DS75362	
SN75365	Motorola	MC75365	
	National	DS75365	
SN75368	Motorola	MC75368	
SN75369	AMD	MH0026	
	Motorola	MMH0026	
	National	DS0026	
♦SN7538	National	DS7538	
	Silicon G	SG7538	
♦SN7539	Silicon G	SG7539	
SN75450	Fairchild	75450	
	Hitachi	HD2574	
	Motorola	MC75450	
	National	DS75450	
	Raytheon	RC75450	
	Signetics	75450	
	Silicon G	SG75450	
SN75450A	Hitachi	HD75450A	
SN75451	Fairchild	75451	
	Hitachi	HD2575	
	Motorola	MC75451	
	National	DS75451	
	Raytheon	RC75451	
	Signetics	75451	
	Silicon G	SG75451	
SN75451A	Hitachi	HD75451A	
SN75452	Fairchild	75452	
	Hitachi	HD75452	
	Motorola	MC75452	
	National	DS75452	
	Raytheon	RC75452	
	Signetics	75452	
	Silicon G	SG75452	
SN75453	Fairchild	75453	
	Hitachi	HD2578	
		HD75453	
	Motorola	MC75453	
	National	DS75453	
	Raytheon	RC75453	
	Signetics	75453	
	Silicon G	SG75453	
SN75454	Fairchild	75454	
	Hitachi	HD2579	
		HD75454	
	Motorola	MC75454	
	National	DS75454	
	Raytheon	RC75454	
	Signetics	75454	
	Silicon G	SG75454	
SN75460	Fairchild	75460	
	Motorola	MC75460	
	National	DS75460	
	Silicon G	SG75460	
SN75461	Fairchild	75461	
	Motorola	MC75461	
	National	DS75461	
	Silicon G	SG75461	
SN75462	Fairchild	75462	
	Motorola	MC75462	
	National	DS75462	
	Silicon G	SG75462	
SN75463	Fairchild	75463	
SN75463	Motorola	MC75463	
	National	DS75463	
	Silicon G	SG75463	
SN75464	Fairchild	75464	
	Motorola	MC75464	
	National	DS75464	
		SG75464	
	Silicon G	SG75464	
SN75466	Motorola	MC1411	
	Signetics	NE5501	
	Sprague	ULN-2021	
SN75467	Motorola	MC1412	
	Signetics	NE5502	
	Sprague	ULN-2022	
SN75468	Motorola	MC1413	
	Signetics	NE5503	
	Sprague	ULN-2023	
SN75469	Signetics	NE5504	
	Sprague	ULN-2024	
SN75470	Fairchild	75470	
	Silicon G	SG75470	
SN75471	Fairchild	75471	
	Silicon G	SG7541	
SN75472	Fairchild	75472	
	Silicon G	SG7542	
SN75473	Fairchild	75473	
	Silicon G	SG7543	
SN75474	Fairchild	75474	
	Silicon G	SG7544	
SN75475	Motorola	MC1472	
SN75476	Sprague	UDN-5711	
SN75477	Sprague	UDN-5712	
SN75478	Sprague	UDN-5713	
SN75479	Sprague	UDN-5714	
SN75480	National	DS8880	
SN75491	Fairchild	75491	
	Motorola	MC75491	
	National	DS75491	
SN75492	Fairchild	75492	
	Motorola	MC75492	
	National	DS75492	
SN75493	National	DS75493	
SN75494	National	DS75494	
SN76001	SGS	TBA820	
SN76104	Fairchild	μA732	
SN76111	Fairchild	μA767	
	RCA	CA758	
SN76115	Motorola	MC1310	
	RCA	CA1310	
	Sprague	ULN-2110	
		ULN-2210	
SN76116	Fairchild	μA758	
	RCA	CA758	
	Sprague	ULN-2244	
SN76131	Exar	XR4739	
	Fairchild	μA739	
	SGS	TBA231	
SN76149	Exar	XR4739	
	Fairchild	μA749	
SN76177	Sprague	ULN-2277	
SN76226	Sprague	ULN-2216	
SN76227	Plessey	SL1327	
	Sprague	ULN-2217	
SN76228	Sprague	ULN-2218	
SN76242	Fairchild	μA780	
	RCA	CA3070	
	Sprague	ULN-2124	
SN76243	Fairchild	μA781	
	Sprague	ULN-2127	
SN76246	Fairchild	μA746	
	RCA	CA3071	
	Sprague	ULN-2114	
		ULN-2228	
SN76266	RCA	CA3066	
SN76267	Fairchild	μA3067	
	RCA	CA3067	
SN76298	Motorola	MC1398	
	RCA	CA1398	
	Sprague	ULN-2298	
♦SN76502	TI	TL441	
SN76514	Motorola	MC1496	
SN76530	Motorola	MC1330	
SN76544	Plessey	SL76544	
SN76564	Fairchild	3064	
	Motorola	MC1364	
	RCA	CA3064	
SN76564	Sprague	ULN-2264	
SN76565	Motorola	MC1364	
SN76591	Fairchild	μA1391	
	Motorola	MC1391	
SN76594	Fairchild	μA1394	
	Motorola	MC1394	
SN76600	Motorola	MC1350	
SN76635	Fairchild	μA720	
	Sprague	ULN-2137	
SN76642	Motorola	MC1357	
	Sprague	ULN-2113	
SN76643	Fairchild	2136	
	Signetics	ULN2111	
	Sprague	ULN-2111	
SN76650	Motorola	MC1352	
	RCA	CA1352	
SN76651	Motorola	MC1351	
SN76665	Fairchild	μA3064	
	Motorola	MC1364	
	RCA	CA3065	
	Sprague	ULN-2165	
SN76666	Fairchild	μA3065	
	Motorola	MC1358	
	Sprague	ULN-2165	
SN76669	Fairchild	μA2136	
	Motorola	MC1356	
	Sprague	ULN-2136	
SN76675	Fairchild	μA3075	
	Motorola	MC1375	
SN76676	RCA	CA3076	
SN76678	Fairchild	μA753	
	Sprague	ULN-2209	
SN76689	Fairchild	μA3089	
	RCA	CA3089	
	Sprague	ULN-2289	
TL072	**Exar**	**XR072**	**926**
	PMI	OP-25	
TL074	**Exar**	**XR074**	**926**
TL081	PMI	OP-16	
TL082	**Exar**	**XR082**	**927**
TL083	**Exar**	**XR083**	**927**
TL084	**Exar**	**XR084**	**927**
TL089	**Harris**	**HA-2905**	**996**
TL430	Signetics	TL430	
TL484	Motorola	TL484	
TL485	Motorola	TL485	
TL494	Motorola	TL494	
TL495	Motorola	TL495	
TL514	Motorola	MC1514	
	Raytheon	RC1414	
		RM1514	
TL720	National	LM1414	
TMS0803	GI	C-593	
TMS0851	GI	CF-593	
♦TMS1103	Signetics	1103	
♦TMS2101	Fairchild	3538	
	NEC Micro	**μPD2101**	**1586**
♦TMS2102	**NEC Micro**	**μPD2102**	**1591**
♦TMS2300	AMI	S8773	
♦TMS2500	AMI	S8773	
TMS2516	**AMI**	**S4716**	**1220**
♦TMS2600	AMI	S8773	
	National	MM4230	
		MM5230	
TMS2708	AMD	2708	
	EA	EA2708	
	Fairchild	**2708**	**1282**
	Fujitsu	MB8518	
	Intel	2708	
	Motorola	MCM2708	
	National	MM2708	
TMS2716	Fujitsu	MBM2716	
	Motorola	**TMS2716**	**1486**
♦TMS2800	National	MM4210	
♦TMS2900	AMI	S8773	
TMS3112	Fairchild	3348	
TMS3114	AMD	3114	
TMS3120	Fairchild	3347	
	SGS	M142	
♦TMS3121	Fairchild	3342	
♦TMS3133	Fairchild	3355	
♦TMS3304	Motorola	MC1141	
TMS3409	Fairchild	3357	
	Mostek	MK1007	
	Plessey	MP3409	
	SGS	M142	
♦TMS3412	AMI	S1685	
♦TMS3414	AMI	S1685	
TMS3417	Fairchild	3342	
	Plessey	MP3417	
TMS40L45	**Fairchild**	**2114**	**1281**
	Rockwell	R2114	
♦TMS4000	GI	RO5-8192	
TMS4027	Fairchild	M4027	
	Fujitsu	MB8227	
	Intersil	IM7027	
		MK4027	
	Mostek	MK4027	
	Motorola	**MCM4027**	**1522**
	NEC Micro	μPD414	
♦TMS4030	Intel	2107A	
TMS4033	**Fairchild**	**21021**	**1275**
♦TMS4033	National	MM2102	
	NEC Micro	**μPD2102**	**1591**
	SGS	M330	
♦TMS4034	**Fairchild**	**21022**	**1275**
	National	MM2102	
	NEC Micro	**μPD2102**	**1591**
	Signetics	2102	
♦TMS4035	**Fairchild**	**2102**	**1275**
	National	MM2101	
	Signetics	2102	
♦TMS4039	**NEC Micro**	**μPD2101**	**1586**
♦TMS4042	**NEC Micro**	**μPD2111**	**1595**
TMS4044	AMD	4044	
	Fujitsu	MBM4044	
	Intersil	7141	
	Mitsubishi	**M5T4044**	**1432**
TMS4045	AMD	9114	
		9124	
	AMI	**S2114**	**1196**
	Fujitsu	MB8114	
	Intel	2114	
	Intersil	IM7114	
		2114	
	NEC Micro	**μPD2114**	**1604**
TMS4050	AMD	9050	
	NEC Micro	μPD418	
TMS4051	NEC Micro	μPD418	
TMS4060	AMD	9060	
	EA	EA4060	
	Fujitsu	MB8107	
	Intel	2107	
	National	**MM5280**	**270**
	NEC Micro	**μPD411**	**1547**
TMS4062	Intersil	6002	
	Nortec	6002	
♦TMS4070	Intersil	7116	
	Zilog	Z6116	
♦TMS4100	SMC	CG4100	
TMS4116	AMD	9016	
	Fairchild	**F16K**	**1272**
	Fujitsu	MB8116	
	Intel	2116	
	Intersil	7116	
	Mostek	MK4116	
	Motorola	**MCM4116**	**1505**
	NEC Micro	**μPD416**	**1562**
	Signetics	**2690**	**1676**
TMS4700	Mostek	MK30000	
TMS4732	**AMI**	**S68332**	**1216**
	NEC Micro	**μPD2332**	**1637**
	Signetics	**2632**	**1672**
	SMC	ROM4732	
	Supertex	**CM3200**	**1706**
TMS4764	**AMI**	**S4264**	**1212**
♦TMS4800	EA	EA4800	
		EA4900	
	Mostek	MK28000	
♦TMS5000	SMC	KR3600	
♦TMS5001	GI	AY5-3600	
♦TMS54071	Mostek	MK4116	
♦TMS6010	AMI	S1757	
	GI	AY5-1013A	
	SMC	COM2502	
TMS6011	**AMI**	**S1883**	**629**
	GI	AY3-1014A	
		AY3-1015	
	RCA	CDP1854	
	SMC	COM2017	
	Western	TR1602	
♦TMS7001	Intersil	IM7001	

♦ Discontinued

Bold face device numbers indicate manufacturers data is provided in the IC Master on the pages noted.

Texas Instruments (cont'd)

Manufacturer Device	Replacement Source	Device	IC Master Page
TMS8080	AMD	9080	
	Intel	8080	
	NEC Micro	**μPD8080AF**	**2119**
TMS8080A	**National**	**INS8080A**	**238**
	NEC Micro	**μPD8080A**	**2119**
TMS9900	**AMI**	**S9900**	**1840**
TMS9901	**AMI**	**S9901**	**1844**
TMS9902	**AMI**	**S9902**	**1846**
TMS9903	**AMI**	**S9903**	**1848**
TMS9940	**AMI**	**S9940**	**1850**
TMS9980	**AMI**	**S9980**	**1851**
	SMC	UPC9980	
TP4000	Mitel	SIL4000	
	Motorola	MC14000	
	National	CD4000	
	RCA	CD400	
		CD4000	
	Solitron	CM4000	
	SSS	SCL4000	
TP4001	Fairchild	F4001	
	Mitel	SIL4001	
	Motorola	MC14001	
	National	CD4001	
	NEC America	μPD4001	
	RCA	CD4001	
	Solitron	CM4001	
	SSS	SCL4001	
	Toshiba	TC4001	
TP4002	Fairchild	F4002	
	Mitel	SIL4002	
	Motorola	MC14002	
	National	CD4002	
	NEC America	μPD4002	
	RCA	CD4002	
	SGS	HBF4002	
	Solitron	CM4002	
	SSS	SCL4002	
	Toshiba	TC4002	
TP4007	Fairchild	F4007	
	Mitel	SIL4007	
	Motorola	MC14007	
	National	CD4007	
	RCA	CD4007	
	SGS	HBF4007	
	Solitron	CM4007	
	SSS	SCL4007	
	Toshiba	TC4007	
TP4008	Fairchild	F4008	
	Motorola	MC14008	
	National	CD4008	
	RCA	CD4008	
	SGS	HBF4008	
	Solitron	CM4008	
	SSS	SCL4008	
	Toshiba	TC4008	
TP4009	Mitel	SIL4009	
	National	CD4009	
	RCA	CD4009	
	SGS	HBF4009	
	Solitron	CM4009	
	SSS	SCL4009	
	Toshiba	TC4009	
TP4010	Mitel	SIL4010	
	National	CD4010	
	RCA	CD4010	
	SGS	HBF4010	
	Solitron	CM4010	
	SSS	SCL4010	
	Toshiba	TC4010	
TP4011	Fairchild	F4011	
	Mitel	SIL4011	
	Motorola	MC14011	
	National	CD4011	
	NEC America	μPD4011	
	RCA	CD4011	
	SGS	HBF4011	
	Solitron	CM4011	
	SSS	SCL4011	
	Toshiba	TC4011	
TP4012	Fairchild	F4012	
	Mitel	SIL4012	
	Motorola	MC14012	
	National	CD4012	
TP4012	NEC America	μPD4012	
	RCA	CD4012	
	SGS	HBF4012	
	Solitron	CM4012	
	SSS	SCL4012	
	Toshiba	TC4012	
TP4013	Fairchild	F4013	
	Mitel	SIL4013	
	Motorola	MC14013	
	National	CD4013	
	NEC America	μPD4013	
	RCA	CD4013	
	SGS	HBF4013	
	Solitron	CM4013	
	SSS	SCL4013	
	Toshiba	TC4013	
TP4014	Fairchild	F4014	
	Mitel	SIL4014	
	Motorola	MC14014	
	National	CD4014	
	NEC America	μPD4014	
	RCA	CD4014	
	SGS	HBF4014	
	Solitron	CM4014	
	SSS	SCL4014	
	Toshiba	TC4014	
TP4015	Fairchild	F4015	
	Mitel	SIL4015	
	Motorola	MC14015	
	National	CD4015	
	NEC America	μPD4015	
	RCA	CD4015	
	SGS	HBF4015	
	Solitron	CM4015	
	SSS	SCL4015	
	Toshiba	TC4015	
TP4016	AD	AD7516	
	Fairchild	F4016	
	Micro Power	MPS7516	
	Mitel	SIL4016	
	Motorola	MC14016	
	National	**CD4016**	**1076**
	RCA	CD4016	
		CD4066	
	Solitron	CM4016	
	SSS	SCL4016	
TP4017	Fairchild	F4017	
	Mitel	SIL4017	
	Motorola	MC14017	
	National	CD4017	
	NEC America	μPD4017	
	RCA	CD4017	
	SGS	HBF4017	
	Solitron	CM4017	
	SSS	SCL4017	
	Toshiba	TC4017	
TP4018	Fairchild	F4018	
	Mitel	SIL4018	
	National	CD4018	
	RCA	CD4018	
	SGS	HBF4018	
	Solitron	CM4018	
	SSS	SCL4018	
	Toshiba	TC4018	
TP4019	Fairchild	F4019	
	Mitel	SIL4019	
	National	CD4019	
	RCA	CD4019	
	SGS	HBF4019	
	Solitron	CM4019	
	SSS	SCL4019	
	Toshiba	TC4019	
TP4020	Fairchild	F4020	
	Mitel	SIL4020	
	Motorola	MC14020	
	National	CD4020	
	NEC America	μPD4020	
	RCA	CD4020	
	SGS	HBF4020	
	Solitron	CM4020	
	SSS	SCL4020	
	Toshiba	TC4020	
TP4021	Fairchild	F4021	
	Mitel	SIL4021	
	Motorola	MC14021	
	National	CD4021	
TP4021	NEC America	μPD4021	
	RCA	CD4021	
	Solitron	CM4021	
	SSS	SCL4021	
	Toshiba	TC4021	
TP4022	Fairchild	F4022	
	Mitel	SIL4022	
	Motorola	MC14022	
	National	CD4022	
	RCA	CD4022	
	SGS	HBF4022	
	Solitron	CM4022	
	SSS	SCL4022	
	Toshiba	TC4022	
TP4023	Fairchild	F4023	
	Mitel	SIL4023	
	Motorola	MC14023	
	National	CD4023	
	NEC America	μPD4023	
	RCA	CD4023	
	SGS	HBF4023	
	Solitron	CM4023	
	SSS	SCL4023	
	Toshiba	TC4023	
TP4024	Fairchild	F4024	
	Mitel	SIL4024	
	Motorola	MC14024	
	National	CD4024	
	RCA	CD4024	
	SGS	HBF4024	
	Solitron	CM4024	
	SSS	SCL4024	
	Toshiba	TC4024	
TP4025	Fairchild	F4025	
	Mitel	SIL4025	
	Motorola	MC14025	
	National	CD4025	
	NEC America	μPD4025	
	RCA	CD4025	
	SGS	HBF4025	
	Solitron	CM4025	
	SSS	SCL4025	
	Toshiba	TC4025	
TP4027	Fairchild	F4027	
	Mitel	SIL4027	
	Motorola	MC14027	
	National	CD4027	
	NEC America	μPD4027	
	RCA	CD4027	
	SGS	HBF4027	
	Solitron	CM4027	
	SSS	SCL4027	
	Toshiba	TC4027	
TP4028	Fairchild	F4028	
	Mitel	SIL4028	
	Motorola	MC14028	
	National	CD4028	
	NEC America	μPD4028	
	RCA	CD4028	
	SGS	HBF4028	
	Solitron	CM4028	
	SSS	SCL4028	
	Toshiba	TC4028	
TP4029	Fairchild	F4029	
	Mitel	SIL4029	
	National	CD4029	
	NEC America	μPD4029	
	RCA	CD4029	
	SGS	HBF4029	
	Solitron	CM4029	
	SSS	SCL4029	
	Toshiba	TC4029	
TP4030	Fairchild	F4030	
	Mitel	SIL4030	
	National	CD4030	
	NEC America	μPD4030	
	RCA	CD4030	
	SGS	HBF4030	
	Solitron	CM4030	
	SSS	SCL4030	
	Toshiba	TC4030	
TP4035	Fairchild	F4035	
	Mitel	SIL4035	
	Motorola	MC14035	
	National	CD4035	
	NEC America	μPD4035	
TP4035	RCA	CD4035	
	SGS	HBF4035	
	Solitron	CM4035	
	SSS	SCL4035	
	Toshiba	TC4035	
TP4040	Fairchild	F4040	
	Mitel	SIL4040	
	National	CD4040	
	NEC America	μPD4040	
	RCA	CD4040	
	Solitron	CM4040	
	SSS	SCL4040	
	Toshiba	TC4040	
TP4042	Fairchild	F4042	
	Mitel	SIL4042	
	Motorola	MC14042	
	National	CD4042	
	NEC America	μPD4042	
	RCA	CD4042	
	SGS	HBF4042	
	Solitron	CM4042	
	SSS	SCL4042	
	Toshiba	TC4042	
TP4043	Fairchild	F4043	
	Mitel	SIL4043	
	Motorola	MC14043	
	National	CD4043	
	NEC America	μPD4043	
	RCA	CD4043	
	Solitron	CM4043	
	SSS	SCL4043	
	Toshiba	TC4043	
TP4044	Fairchild	F4044	
	Mitel	SIL4044	
	Motorola	MC14044	
	National	CD4044	
	NEC America	μPD4044	
	RCA	CD4044	
	Solitron	CM4044	
	SSS	SCL4044	
	Toshiba	TC4044	
♦TP4047	Fairchild	F4047	
	Motorola	MC14047	
	RCA	CD4047	
	Solitron	CM4047	
	Toshiba	TC4047	
TP4049	Fairchild	F4049	
	Mitel	SIL4049	
	Motorola	MC14049	
	National	CD4049	
	NEC America	μPD4049	
	RCA	CD4049	
	SGS	HBF4049	
	Solitron	CM4049	
	SSS	SCL4049	
	Toshiba	TC4049	
TP4050	Fairchild	F4050	
	Mitel	SIL4050	
	Motorola	MC14050	
	National	CD4050	
	NEC America	μPD4050	
	RCA	CD4050	
	SGS	HBF4050	
	Solitron	CM4050	
	SSS	SCL4050	
	Toshiba	TC4050	
TP4051	Fairchild	F4051	
	GI	MEM4051	
	Mitel	SIL4051	
	Motorola	MC14051	
	National	CD4051	
	RCA	CD4051	
	Solitron	CM4051	
	SSS	SCL4051	
	Toshiba	TC4051	
TP4052	Fairchild	F4052	
	Mitel	SIL4052	
	Motorola	MC14052	
	National	CD4052	
	RCA	CD4052	
	Solitron	CM4052	
	SSS	SCL4052	
	Toshiba	TC4052	
TP4053	RCA	CD4053	
TP4068	Fairchild	F4068	
	Mitel	SIL4068	

♦ Discontinued

The manufacturers report their devices can be used as direct replacements.
Performance details often differ, so compare the specifications considering your requirements.

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Manufacturer Device	Replacement Source	Device	IC Master Page
TP4068	Motorola	MC14068	
	RCA	CD4068	
	Solitron	CM4068	
	SSS	SCL4068	
	Toshiba	TC4068	
TP4069	Fairchild	F4069	
	Harris	HD74C04	
	Mitel	SIL4069	
	Motorola	MC14069	
	National	CD4069	
		MM74C04	
	NEC America	μPD4069	
	RCA	CD4069	
	Solitron	CM4069	
	SSS	SCL4069	
	Toshiba	TC4069	
♦TP4070	Fairchild	F4070	
	Mitel	SIL4070	
	National	CD4070	
		MM74C86	
	RCA	CD4070	
	Solitron	CM4070	
	SSS	SCL4070	
TP4071	Fairchild	F4071	
	Mitel	SIL4071	
	Motorola	MC14071	
	National	CD4071	
	NEC America	μPD4071	
	RCA	CD4071	
	Solitron	CM4071	
	SSS	SCL4071	
	Toshiba	TC4071	
TP4072	Fairchild	F4072	
	Mitel	SIL4072	
	Motorola	MC14072	
	RCA	CD4072	
	SSS	SCL4072	
	Toshiba	TC4072	
TP4073	Fairchild	F4073	
	Mitel	SIL4073	
	Motorola	MC14073	
	National	CD4073	
	RCA	CD4073	
	Solitron	CM4073	
	SSS	SCL4073	
	Toshiba	TC4073	
TP4075	Fairchild	F4075	
	Mitel	SIL4075	
	Motorola	MC14075	
	National	CD4075	
	RCA	CD4075	
	SSS	SCL4075	
	Toshiba	TC4075	
♦TP4076	Fairchild	F4076	
	Harris	HD74C173	
	Mitel	SIL4076	
	Motorola	MC14076	
	National	CD4076	
		MM74C173	
	RCA	CD4076	
	Solitron	CM4076	
	SSS	SCL4076	
TP4078	Motorola	MC14078	
	RCA	CD4078	
TP4081	Fairchild	F4081	
	Mitel	SIL4081	
	Motorola	MC14081	
	National	CD4081	
	NEC America	μPD4081	
	RCA	CD4081	
	Solitron	CM4081	
	SSS	SCL4081	
	Toshiba	TC4081	
TP4082	Fairchild	F4082	
	Mitel	SIL4082	
	Motorola	MC14082	
	RCA	CD4082	
	SSS	SCL4082	
	Toshiba	TC4082	
♦TP4085	Fairchild	F4085	
	RCA	CD4085	
♦TP4093	Fairchild	F4093	
	Motorola	MC14093	
♦TP4093	National	CD4093	
	RCA	CD4093	
♦TP4099	Fairchild	F4099	
	National	CD4099	
	RCA	CD4099	
TP4315	RCA	CD4069	
TP4320	RCA	CD4067	
TP4360	Fairchild	F40160	
	Motorola	MC14160	
	National	MM74C160	
TP4361	Fairchild	F40161	
	Motorola	MC14161	
	National	MM74C161	
TP4362	Fairchild	F40162	
	Motorola	MC14162	
	National	MM74C162	
TP4363	Fairchild	F40163	
	Motorola	MC14163	
	National	MM74C163	
TP4507	Motorola	MC14507	
	National	CD4070	
		CD4507	
		MM74C86	
	RCA	CD4030	
		CD4070	
	SSS	SCL4030	
TP4511	Fairchild	F4511	
	Mitel	SIL4511	
	Motorola	MC14511	
	National	CD4511	
	RCA	CD4511	
	Solitron	CM4511	
	SSS	SCL4511	
TP4512	Fairchild	F4512	
	Mitel	SIL4512	
	Motorola	MC14512	
	National	CD4512	
	NEC America	μPD4512	
	SSS	SCL4512	
	Toshiba	TC4512	
TP4516	Fairchild	F4516	
♦TP4516	Mitel	SIL4516	
	Motorola	MC14516	
	National	CD4516	
	RCA	CD40193	
		CD4516	
	SSS	SCL4516	
	Toshiba	TC4516	
TP4518	Fairchild	F4518	
	Mitel	SIL4518	
	Motorola	MC14518	
	National	CD4518	
	RCA	CD4518	
	Solitron	CM4518	
	SSS	SCL4518	
	Toshiba	TC4518	
TP4519	Fairchild	F4519	
	Motorola	MC14519	
	National	CD4519	
	NEC America	μPD4519	
	RCA	CD4019	
TP4520	Fairchild	F4520	
	Mitel	SIL4520	
	Motorola	MC14520	
	National	CD4520	
	NEC America	μPD4520	
	RCA	CD4520	
	Solitron	CM4520	
	SSS	SCL4520	
	Toshiba	TC4520	
TP4522	Fairchild	F4522	
	Motorola	MC14522	
	National	CD4522	
	RCA	CD4018	
	SSS	SCL4522	
TP4526	Fairchild	F4526	
	Motorola	MC14526	
	SSS	SCL4526	
TP4531	Fairchild	F4531	
	Motorola	MC14531	
	RCA	CD40101	
	SSS	SCL4531	
TP4581	Motorola	MC14581	
	RCA	CD40181	
	SSS	SCL4581	
TP4582	Fairchild	F4582	
TP4582	Motorola	MC14582	
	RCA	CD40182	
	SSS	SCL4582	
ULN-2001	Signetics	ULN2001	
ULN-2004	Signetics	ULN2004	
ULN2001	**Exar**	**XR2201**	**931**
	Fairchild	9665	
	SGS	L201	
	Silicon G	SG2001	
	Sprague	ULN-2001	
ULN2002	**Exar**	**XR2202**	**931**
	Fairchild	9666	
	SGS	L202	
	Signetics	ULN2002	
	Silicon G	SG2002	
	Sprague	ULN-2002	
ULN2003	**Exar**	**XR2203**	**931**
	Fairchild	9667	
	SGS	L203	
	Signetics	ULN2003	
	Silicon G	SG2003	
	Sprague	ULN-2003	
ULN2004	**Exar**	**XR2204**	**931**
	Fairchild	9668	
	Sprague	ULN-2004	

Toshiba

Manufacturer Device	Replacement Source	Device	IC Master Page
TA7613	Sprague	ULN-2204	
TC4001	Fairchild	F4001	
	Mitel	SIL4001	
	Motorola	MC14001	
	National	CD4001	
	NEC America	μPD4001	
	RCA	CD4001	
	SGS	HBF4001	
	Solitron	CM4001	
	SSS	SCL4001	
	TI	TP4001	
TC4002	Fairchild	F4002	
	Mitel	SIL4002	
	Motorola	MC14002	
	National	CD4002	
	NEC America	μPD4002	
	RCA	CD4002	
	SGS	HBF4002	
	Solitron	CM4002	
	SSS	SCL4002	
	TI	TP4002	
TC4007	Fairchild	F4007	
	Mitel	SIL4007	
	Motorola	MC14007	
	National	CD4007	
	RCA	CD4007	
	SGS	HBF4007	
	Solitron	CM4007	
	SSS	SCL4007	
	TI	TP4007	
TC4008	Fairchild	F4008	
	Motorola	MC14008	
	National	CD4008	
	RCA	CD4008	
	SGS	HBF4008	
	Solitron	CM4008	
	SSS	SCL4008	
	TI	TP4008	
TC4009	Mitel	SIL4009	
	National	CD4009	
	RCA	CD4009	
	SGS	HBF4009	
	Solitron	CM4009	
	SSS	SCL4009	
	TI	TP4009	
TC4010	Mitel	SIL4010	
	National	CD4010	
	RCA	CD4010	
	SGS	HBF4010	
	Solitron	CM4010	
	SSS	SCL4010	
	TI	TP4010	
TC4011	Fairchild	F4011	
	Mitel	SIL4011	
	Motorola	MC14011	
	National	CD4011	
	NEC America	μPD4011	
TC4011	RCA	CD4011	
	SGS	HBF4011	
	Solitron	CM4011	
	SSS	SCL4011	
	TI	TP4011	
TC4012	Fairchild	F4012	
	Mitel	SIL4012	
	Motorola	MC14012	
	National	CD4012	
	NEC America	μPD4012	
	RCA	CD4012	
	SGS	HBF4012	
	Solitron	CM4012	
	SSS	SCL4012	
	TI	TP4012	
TC4013	Fairchild	F4013	
	Mitel	SIL4013	
	Motorola	MC14013	
	National	CD4013	
	NEC America	μPD4013	
	RCA	CD4013	
	SGS	HBF4013	
	Solitron	CM4013	
	SSS	SCL4013	
	TI	TP4013	
TC4014	Fairchild	F4014	
	Mitel	SIL4014	
	Motorola	MC14014	
	National	CD4014	
	NEC America	μPD4014	
	RCA	CD4014	
	SGS	HBF4014	
	Solitron	CM4014	
	SSS	SCL4014	
	TI	TP4014	
TC4015	Fairchild	F4015	
	Mitel	SIL4015	
	Motorola	MC14015	
	National	CD4015	
	NEC America	μPD4015	
	RCA	CD4015	
	SGS	HBF4015	
	Solitron	CM4015	
	SSS	SCL4015	
	TI	TP4015	
TC4017	Fairchild	F4017	
	Mitel	SIL4017	
	Motorola	MC14017	
	National	CD4017	
	NEC America	μPD4017	
	RCA	CD4017	
	SGS	HBF4017	
	Solitron	CM4017	
	SSS	SCL4017	
	TI	TP4017	
TC4018	Fairchild	F4018	
	Mitel	SIL4018	
	National	CD4018	
	RCA	CD4018	
	SGS	HBF4018	
	Solitron	CM4018	
	SSS	SCL4018	
	TI	TP4018	
TC4019	Fairchild	F4019	
	Mitel	SIL4019	
	National	CD4019	
	RCA	CD4019	
	SGS	HBF4019	
	Solitron	CM4019	
	SSS	SCL4019	
	TI	TP4019	
TC4020	Fairchild	F4020	
	Mitel	SIL4020	
	Motorola	MC14020	
	National	CD4020	
	NEC America	μPD4020	
	RCA	CD4020	
	SGS	HBF4020	
	Solitron	CM4020	
	SSS	SCL4020	
	TI	TP4020	
TC4021	Fairchild	F4021	
	Mitel	SIL4021	
	Motorola	MC14021	
	National	CD4021	
	NEC America	μPD4021	

♦ Discontinued

Bold face device numbers indicate manufacturers data is provided in the IC Master on the pages noted.

Toshiba (cont'd)

Manufacturer Device	Replacement Source	Device	IC Master Page
TC4021	RCA	CD4021	
	Solitron	CM4021	
	SSS	SCL4021	
	TI	TP4021	
TC4022	Fairchild	F4022	
	Mitel	SIL4022	
	Motorola	MC14022	
	National	CD4022	
	RCA	CD4022	
	SGS	HBF4022	
	Solitron	CM4022	
	SSS	SCL4022	
	TI	TP4022	
TC4023	Fairchild	F4023	
	Mitel	SIL4023	
	Motorola	MC14023	
	National	CD4023	
	NEC America	μPD4023	
	RCA	CD4023	
	SGS	HBF4023	
	Solitron	CM4023	
	SSS	SCL4023	
	TI	TP4023	
TC4024	Fairchild	F4024	
	Mitel	SIL4024	
	Motorola	MC14024	
	National	CD4024	
	RCA	CD4024	
	SGS	HBF4024	
	Solitron	CM4024	
	SSS	SCL4024	
	TI	TP4024	
TC4025	Fairchild	F4025	
	Mitel	SIL4025	
	Motorola	MC14025	
	National	CD4025	
	NEC America	μPD4025	
	RCA	CD4025	
	SGS	HBF4025	
	Solitron	CM4025	
	SSS	SCL4025	
	TI	TP4025	
TC4027	Fairchild	F4027	
	Mitel	SIL4027	
	Motorola	MC14027	
	National	CD4027	
	NEC America	μPD4027	
	RCA	CD4027	
	SGS	HBF4027	
	Solitron	CM4027	
	SSS	SCL4027	
	TI	TP4027	
TC4028	Fairchild	F4028	
	Mitel	SIL4028	
	Motorola	MC14028	
	National	CD4028	
	NEC America	μPD4028	
	RCA	CD4028	
	SGS	HBF4028	
	Solitron	CM4028	
	SSS	SCL4028	
	TI	TP4028	
TC4029	Fairchild	F4029	
	Mitel	SIL4029	
	National	CD4029	
	NEC America	μPD4029	
	RCA	CD4029	
	SGS	HBF4029	
	Solitron	CM4029	
	SSS	SCL4029	
	TI	TP4029	
TC4030	Fairchild	F4030	
	Mitel	SIL4030	
	National	CD4030	
	NEC America	μPD4030	
	RCA	CD4030	
	SGS	HBF4030	
	Solitron	CM4030	
	SSS	SCL4030	
	TI	TP4030	
TC4032	Motorola	MC14032	
	RCA	CD4032	
	Solitron	CM4032	
TC4034	Fairchild	F4034	
	Motorola	MC14034	
	National	CD4034	
	RCA	CD4034	
	Solitron	CM4034	
	SSS	SCL4034	
TC4035	Fairchild	F4035	
	Mitel	SIL4035	
	Motorola	MC14035	
	National	CD4035	
	NEC America	μPD4035	
	RCA	CD4035	
	SGS	HBF4035	
	Solitron	CM4035	
	SSS	SCL4035	
	TI	TP4035	
TC4038	Motorola	MC14308	
	RCA	CD4038	
	Solitron	CM4038	
TC4040	Fairchild	F4040	
	Mitel	SIL4040	
	National	CD4040	
	NEC America	μPD4040	
	RCA	CD4040	
	Solitron	CM4040	
	SSS	SCL4040	
	TI	TP4040	
TC4042	Fairchild	F4042	
	Mitel	SIL4042	
	Motorola	MC14042	
	National	CD4042	
	NEC America	μPD4042	
	RCA	CD4042	
	SGS	HBF4042	
	Solitron	CM4042	
	SSS	SCL4042	
	TI	TP4042	
TC4043	Fairchild	F4043	
	Mitel	SIL4043	
	Motorola	MC14043	
	National	CD4043	
	NEC America	μPD4043	
	RCA	CD4043	
	Solitron	CM4043	
	SSS	SCL4043	
	TI	TP4043	
TC4044	Fairchild	F4044	
	Mitel	SIL4044	
	Motorola	MC14044	
	National	CD4044	
	NEC America	μPD4044	
	RCA	CD4044	
	Solitron	CM4044	
	SSS	SCL4044	
	TI	TP4044	
TC4047	Fairchild	F4047	
	RCA	CD4047	
	Solitron	CM4047	
TC4049	Fairchild	F4049	
	Mitel	SIL4049	
	Motorola	MC14049	
	National	CD4049	
	NEC America	μPD4049	
	RCA	CD4049	
	SGS	HBF4049	
	Solitron	CM4049	
	SSS	SCL4049	
	TI	TP4049	
TC4050	Fairchild	F4050	
	Mitel	SIL4050	
	Motorola	MC14050	
	National	CD4050	
	NEC America	μPD4050	
	RCA	CD4050	
	SGS	HBF4050	
	Solitron	CM4050	
	SSS	SCL4050	
	TI	TP4050	
TC4051	Fairchild	F4051	
	Mitel	SIL4051	
	Motorola	MC14051	
	National	CD4051	
	RCA	CD4051	
	Solitron	CM4051	
	SSS	SCL4051	
	TI	TP4051	
TC4052	Fairchild	F4052	
	Mitel	SIL4052	
	Motorola	MC14052	
	National	CD4052	
	RCA	CD4052	
	Solitron	CM4052	
	SSS	SCL4052	
	TI	TP4052	
TC4053	Fairchild	F4053	
	GI	MEM4053	
	Mitel	SIL4053	
	Motorola	MC14053	
	National	CD4053	
	RCA	CD4053	
	Solitron	CM4053	
	SSS	SCL4053	
TC4061	RCA	CD4061	
TC4066	Fairchild	F4066	
	Mitel	SIL4066	
	Motorola	MC14066	
	National	**CD4066**	**1076**
	NEC America	μPD4066	
	RCA	CD4063	
		CD4066	
	SGS	HBF4066	
	Signetics	N4066	
	Solitron	CM4066	
	SSS	SCL4066	
TC4068	Fairchild	F4068	
	Mitel	SIL4068	
	Motorola	MC14068	
	RCA	CD4068	
	Solitron	CM4068	
	SSS	SCL4068	
	TI	TP4068	
TC4069	Fairchild	F4069	
	Harris	HD74C04	
	Mitel	SIL4069	
	Motorola	MC14069	
	National	CD4069	
		MM74C04	
	NEC America	μPD4069	
	RCA	CD4069	
	Solitron	CM4069	
	SSS	SCL4069	
	TI	TP4069	
TC4071	Fairchild	F4071	
	Mitel	SIL4071	
	Motorola	MC14071	
	National	CD4071	
	NEC America	μPD4071	
	RCA	CD4071	
	Solitron	CM4071	
	SSS	SCL4071	
	TI	TP4071	
TC4072	Fairchild	F4072	
	Mitel	SIL4072	
	Motorola	MC14072	
	RCA	CD4072	
	SSS	SCL4072	
	TI	TP4072	
TC4073	Fairchild	F4073	
	Mitel	SIL4073	
	Motorola	MC14073	
	National	CD4073	
	RCA	CD4073	
	Solitron	CM4073	
	SSS	SCL4073	
	TI	TP4073	
TC4075	Fairchild	F4075	
	Mitel	SIL4075	
	Motorola	MC14075	
	National	CD4075	
	RCA	CD4075	
	SSS	SCL4075	
	TI	TP4075	
TC4078	Fairchild	F4078	
	Mitel	SIL4078	
	Motorola	MC14078	
	RCA	CD4078	
	Solitron	CM4078	
	SSS	SCL4078	
TC4081	Fairchild	F4081	
	Mitel	SIL4081	
	Motorola	MC14081	
	National	CD4081	
TC4081	NEC America	μPD4081	
	RCA	CD4081	
	Solitron	CM4081	
	SSS	SCL4081	
	TI	TP4081	
TC4082	Fairchild	F4082	
	Mitel	SIL4082	
	Motorola	MC14082	
	RCA	CD4082	
	SSS	SCL4082	
	TI	TP4082	
TC4508	Mitel	SIL4508	
	Motorola	MC14508	
	RCA	CD4508	
	SSS	SCL4508	
TC4510	Fairchild	F4510	
	Mitel	SIL4510	
	Motorola	MC14510	
	National	CD4510	
	RCA	CD40192	
		CD4510	
	SSS	SCL4510	
TC4512	Fairchild	F4512	
	Mitel	SIL4512	
	Motorola	MC14512	
	National	CD4512	
	NEC America	μPD4512	
	SSS	SCL4512	
	TI	TP4512	
TC4514	Fairchild	F4514	
	Mitel	SIL4514	
	Motorola	MC14514	
	National	CD4514	
	RCA	CD4514	
	Solitron	CM4514	
	SSS	SCL4514	
TC4515	Fairchild	F4515	
	Mitel	SIL4515	
	Motorola	MC14515	
	National	CD4515	
	RCA	CD4515	
	Solitron	CM4515	
	SSS	SCL4515	
TC4516	Fairchild	F4516	
	Mitel	SIL4516	
	Motorola	MC14516	
	National	CD4516	
	RCA	CD40193	
		CD4516	
	SSS	SCL4516	
TC4518	Fairchild	F4518	
	Mitel	SIL4518	
	Motorola	MC14518	
	National	CD4518	
	RCA	CD4518	
	Solitron	CM4518	
	SSS	SCL4518	
	TI	TP4518	
TC4520	Fairchild	F4520	
	Mitel	SIL4520	
	Motorola	MC14520	
	National	CD4520	
	NEC America	μPD4520	
	RCA	CD4520	
	Solitron	CM4520	
	SSS	SCL4520	
	TI	TP4520	
TC4528	Fairchild	F4528	
	Motorola	MC14528	
	NEC America	μPD4528	
	RCA	CD4528	
	SSS	SCL4528	
TC4532	Fairchild	F4532	
	Motorola	MC14532	
	RCA	CD4532	
TC4539	Fairchild	F4539	
	Motorola	MC14539	
	NEC America	μPD4539	
TC4583	Fairchild	F4583	
	Motorola	MC14583	
	RCA	CD40100	
TC4585	Motorola	MC14585	
	National	MM74C85	
	RCA	CD4063	
	SSS	SCL4585	
TC7400	Fairchild	7400	

♦ Discontinued

The manufacturers report their devices can be used as direct replacements.
Performance details often differ, so compare the specifications considering your requirements.

Toshiba (cont'd)

Manufacturer Device	Replacement Source	Device	IC Master Page
TC7400	Hitachi	HD7400	
	Mitsubishi	M53200	
	Motorola	MC7400	
	National	DM7400	
	NEC America	μPB7400	
	Signetics	7400	
	TI	SN7400	
	TRW	7400	
♦TC7404	Fairchild	7404	
	Hitachi	HD7404	
	Mitsubishi	M53204	
	Motorola	MC7404	
	National	DM7404	
	NEC America	μPB7404	
	Signetics	7404	
	TI	SN7404	
	TRW	7404	
♦TC7408	Fairchild	7408	
	Mitsubishi	M53208	
	Motorola	MC7408	
	National	DM7408	
	Signetics	7408	
	TI	SN7408	
	TRW	7408	
TC7410	Fairchild	7410	
	Hitachi	HD7410	
	Mitsubishi	M53210	
	Motorola	MC7410	
	National	DM7410	
	NEC America	μPB7410	
	Signetics	7410	
	TI	SN7410	
		SN7427	
	TRW	7410	
TC7420	Fairchild	7420	
	Hitachi	HD7420	
	Mitsubishi	M53220	
	Motorola	MC7420	
	National	DM7420	
	NEC America	μPB7420	
	Signetics	7420	
	TI	SN7420	
	TRW	7420	
TMM314	Fujitsu	MB8114	
TMM323	Fujitsu	MBM2716	
♦TMM414	Fujitsu	MB8107	
♦TMM415	Fujitsu	MB8227	
TMM416	Fujitsu	MB8116	

TRW

MPY16	MMI	MPY16	
7400	Fairchild	7400	
	Hitachi	HD7400	
	Mitsubishi	M53200	
	Motorola	MC7400	
	National	DM7400	
	NEC America	μPB7400	
	Signetics	7400	
	TI	SN7400	
	Toshiba	TC7400	
7401	Fairchild	7401	
	Mitsubishi	M53201	
	Motorola	MC7401	
	National	DM7401	
	Signetics	7401	
	TI	SN7401	
7402	Fairchild	7402	
	Hitachi	HD7402	
	Mitsubishi	M53202	
	Motorola	MC7402	
	National	DM7402	
	NEC America	μPB7402	
	Signetics	7402	
	TI	SN7402	
7403	Fairchild	7403	
	Hitachi	HD7403	
	Mitsubishi	M53203	
	Motorola	MC7403	
	National	DM7403	
	Signetics	7403	
	TI	SN7403	
7404	Fairchild	7404	
	Hitachi	HD7404	
	Mitsubishi	M53204	
	Motorola	MC7404	
	National	DM7404	
	NEC America	μPB7404	
	Signetics	7404	
	TI	SN7404	
	Toshiba	TC7404	
7405	Fairchild	7405	
	Hitachi	HD7405	
	Mitsubishi	M53205	
	Motorola	MC7405	
	National	DM7405	
	NEC America	μPB7405	
	Signetics	7405	
	TI	SN7405	
7406	Fairchild	7406	
	Hitachi	HD7406	
	Mitsubishi	M53206	
	Motorola	MC7406	
	National	DM7406	
	Signetics	7406	
	TI	SN7406	
7407	Fairchild	7407	
	Hitachi	HD7407	
	Mitsubishi	M53207	
	Motorola	MC7407	
	National	DM7407	
	Signetics	7407	
	TI	SN7407	
7408	Fairchild	7408	
	Mitsubishi	M53208	
	Motorola	MC7408	
	National	DM7408	
	Signetics	7408	
	TI	SN7408	
	Toshiba	TC7408	
7409	Fairchild	7409	
	Hitachi	HD7409	
	Mitsubishi	M53209	
	Motorola	MC7409	
	National	DM7409	
	Signetics	7409	
	TI	SN7409	
7410	Fairchild	7410	
	Hitachi	HD7410	
	Mitsubishi	M53210	
	Motorola	MC7410	
	National	DM7410	
	NEC America	μPB7410	
	Signetics	7410	
	TI	SN7410	
		SN7427	
	Toshiba	TC7410	
74111	TI	SN74111	
7412	Fairchild	7412	
	Hitachi	HD7412	
	Signetics	7412	
	TI	SN7412	
74121	Fairchild	74121	
	Hitachi	HD74121	
	Mitsubishi	M53321	
	Motorola	MC74121	
	National	DM74121	
	Signetics	74121	
	TI	SN74121	
74123	AMD	SN74123	
	Fairchild	74123	
	Mitsubishi	M53323	
	Motorola	MC74123	
	National	DM74123	
	NEC America	μPB74123	
	Signetics	74123	
	TI	SN74123	
7413	Fairchild	7413	
	Mitsubishi	M53213	
	Motorola	MC7413	
	National	DM7413	
	NEC America	μPB7413	
	Signetics	7413	
	TI	SN7413	
74136	Hitachi	HD74136	
	Motorola	MC74136	
	TI	SN74136	
74145	Fairchild	74145	
74145	Mitsubishi	M53345	
	Motorola	MC74145	
	National	DM74145	
	Signetics	74145	
	TI	SN74145	
74150	Fairchild	74150	
	Hitachi	HD74150	
	Mitsubishi	M53350	
	Motorola	MC74150	
	National	DM74150	
	NEC America	μPB74150	
	Signetics	74150	
	TI	SN74150	
74151	Fairchild	74151	
	Hitachi	HD74151	
	Mitsubishi	M53351	
	Motorola	MC74151	
	National	DM74151	
	NEC America	μPB74151	
	Signetics	74151	
	TI	SN74151	
74152	Fairchild	74152	
	Motorola	MC74152	
74153	Fairchild	74153	
	Mitsubishi	M53353	
	Motorola	MC74153	
	National	DM74153	
	NEC America	μPB74153	
	Signetics	74153	
	TI	SN74153	
74154	AMD	SN74154	
	Fairchild	74154	
	Mitsubishi	M53354	
	Motorola	MC74154	
	National	DM74154	
	NEC America	μPB74154	
	Signetics	74154	
	TI	SN74154	
74155	Fairchild	74155	
	Mitsubishi	M53355	
	Motorola	MC74155	
	National	DM74155	
	NEC America	μPB74155	
	Signetics	74155	
	TI	SN74155	
74156	Fairchild	74156	
	Hitachi	HD74156	
	Mitsubishi	M53356	
	Motorola	MC74156	
	National	DM74156	
	NEC America	μPB74156	
	Signetics	74156	
	TI	SN74156	
7416	Fairchild	7416	
	Hitachi	HD7416	
	Mitsubishi	M53216	
	Motorola	MC7416	
	National	DM7416	
	Signetics	7416	
	TI	SN7416	
74160	AMD	SN74160	
	Fairchild	74160	
	Hitachi	HD74160	
	Mitsubishi	M53360	
	Motorola	MC74160	
	National	DM74160	
	Signetics	74160	
	TI	SN74160	
74161	AMD	SN74161	
	Fairchild	74161	
	Hitachi	HD74161	
	Mitsubishi	M53361	
	Motorola	MC74161	
	National	DM74161	
	NEC America	μPB74161	
	Signetics	74161	
	TI	SN74161	
74162	AMD	SN74162	
	Fairchild	74162	
	Hitachi	HD74162	
	Mitsubishi	M53362	
	Motorola	MC74162	
	National	DM74162	
	Signetics	74162	
	TI	SN74162	
74163	AMD	SN74163	
74163	Fairchild	74163	
	Hitachi	HD74163	
	Mitsubishi	M53363	
	Motorola	MC74163	
	National	DM74163	
	Signetics	74163	
	TI	SN74163	
7417	Fairchild	7417	
	Hitachi	HD7417	
	Mitsubishi	M53217	
	Motorola	MC7417	
	National	DM7417	
	Signetics	7417	
	TI	SN7417	
74180	Fairchild	74180	
	Hitachi	HD74180	
	Mitsubishi	M53380	
	Motorola	MC74180	
	National	DM74180	
	NEC America	μPB74180	
	Signetics	74180	
	TI	SN74180	
7420	Fairchild	7420	
	Hitachi	HD7420	
	Mitsubishi	M53220	
	Motorola	MC7420	
	National	DM7420	
	NEC America	μPB7420	
	Signetics	7420	
	TI	SN7420	
	Toshiba	TC7420	
7426	Fairchild	7426	
	Hitachi	HD7426	
	Motorola	MC7426	
	National	DM7426	
	Signetics	7426	
	TI	SN7426	
74290	Fairchild	74290	
	Mitsubishi	M53490	
	Motorola	MC74290	
	TI	SN74290	
74293	Fairchild	74293	
	Mitsubishi	M53493	
	Motorola	MC74293	
	TI	SN74293	
7430	Fairchild	7430	
	Hitachi	HD7430	
	Mitsubishi	M53230	
	Motorola	MC7430	
	National	DM7430	
	NEC America	μPB7430	
	Signetics	7430	
	TI	SN7430	
7437	Fairchild	7437	
	Mitsubishi	M53237	
	Motorola	MC7437	
	National	DM7437	
	NEC America	μPB7437	
	Signetics	7437	
	TI	SN7437	
7438	Fairchild	7438	
	Mitsubishi	M53238	
	Motorola	MC7438	
	National	DM7438	
	NEC America	μPB7438	
	Signetics	7438	
	TI	SN7438	
7440	Fairchild	7440	
	Hitachi	HD7440	
	Mitsubishi	M53240	
	Motorola	MC7440	
	National	DM7440	
	NEC America	μPB7440	
	Signetics	7440	
	TI	SN7440	
7445	Fairchild	7445	
	Mitsubishi	M53245	
	Motorola	MC7445	
	National	DM7445	
	NEC America	μPB7445	
	Signetics	7445	
	TI	SN7445	
7450	Fairchild	7450	
	Hitachi	HD7450	
	Mitsubishi	M53250	
	Motorola	MC7450	

♦ Discontinued

Bold face device numbers indicate manufacturers data is provided in the IC Master on the pages noted.

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TRW (cont'd)			
7450	National	DM7450	
	NEC America	μPB7450	
	Signetics	7450	
	TI	SN7450	
7451	Fairchild	7451	
	Hitachi	HD7451	
	Motorola	MC7451	
	National	DM7451	
	NEC America	μPB7451	
	Signetics	7451	
	TI	SN7451	
7453	Fairchild	7453	
	Hitachi	HD7453	
	Mitsubishi	M53253	
	Motorola	MC7453	
	National	DM7453	
	NEC America	μPB7453	
	Signetics	7453	
	TI	SN7453	
7454	Fairchild	7454	
	Hitachi	HD7454	
	Motorola	MC7454	
	National	DM7454	
	NEC America	μPB7454	
	Signetics	7454	
	TI	SN7454	
7460	Fairchild	7460	
	Hitachi	HD7460	
	Mitsubishi	M53260	
	Motorola	MC7460	
	National	DM7460	
	NEC America	μPB7460	
	Signetics	7460	
	TI	SN7460	
7472	Fairchild	7472	
	Hitachi	HD7472	
	Mitsubishi	M53272	
	Motorola	MC7472	
	National	DM7472	
	Signetics	7472	
	TI	SN7472	
7474	Fairchild	7474	
	Hitachi	HD7474	
	Mitsubishi	M53274	
	Motorola	MC7474	
	National	DM7474	
	NEC America	μPB7474	
	Signetics	7474	
	TI	SN7474	
7475	Fairchild	7475	
	Hitachi	HD7475	
	Mitsubishi	M53275	
	Motorola	MC7475	
	National	DM7475	
	Signetics	7475	
	TI	SN7475	
7476	Fairchild	7476	
	Mitsubishi	M53276	
	Motorola	MC7476	
	National	DM7476	
	NEC America	μPB7476	
	Signetics	7476	
	TI	SN7476	
7481	TI	SN7481	
7485	Fairchild	7485	
	Hitachi	HD7485	
	Mitsubishi	M53285	
	Motorola	MC7485	
	National	DM7485	
	NEC America	μPB7485	
	Signetics	7485	
	TI	SN7485	
7486	Fairchild	7486	
	Hitachi	HD7486	
	Mitsubishi	M53286	
	Motorola	MC7486	
	National	DM7486	
	NEC America	μPB7486	
	Signetics	7486	
	TI	SN7486	
7489	AMD	SN7489	
	Fairchild	7489	
	Mitsubishi	M53289	
7489	National	DM7489	
	TI	SN7489	
7490	Fairchild	7490	
	Hitachi	HD7490	
	Mitsubishi	M53290	
	Motorola	MC7490	
	National	DM7490	
	Signetics	7490	
	TI	SN7490	
7492	Fairchild	7492	
	Hitachi	HD7492	
	Mitsubishi	M53292	
	Motorola	MC7492	
	National	DM7492	
	Signetics	7492	
	TI	SN7492	
7493	Fairchild	7493	
	Hitachi	HD7493	
	Mitsubishi	M53293	
	Motorola	MC7493	
	National	DM7493	
	Signetics	7493	
	TI	SN7493	
7496	Fairchild	7496	
	Hitachi	HD7496	
	Mitsubishi	M53296	
	Motorola	MC7496	
	National	DM7496	
	Signetics	7496	
	TI	SN7496	
Western Digital			
BR1941	SMC	COM5016	
FD1771	National	INS1771	
♦RM1701	Intel	2107	
	TI	TMS4060	
♦RM4096	Mostek	MK4096	
TR1402	SMC	COM2502	
TR1402A	GI	AY5-1013A	
	SMC	COM2502H	
TR1602	**AMI**	**S1883**	**629**
	GI	AY3-1014A	
		AY3-1015	
		AY5-1013A	
	RCA	CDP1854	
	SMC	COM2017	
		COM2502	
	TI	TMS6011	
TR1863	SMC	COM8017	
UC1671	National	INS1671	
	SMC	COM1671	
Zilog			
Z6116	AMD	9016	
	Fairchild	**F16K**	**1272**
	Fujitsu	MB8116	
	Intel	2117	
	Intersil	7116	
	Mostek	MK4116	
	Motorola	**MCM4116**	**1505**
	NEC Micro	**μPD416**	**1562**
Z80-CPU	Mostek	MK3880	
Z80-CTC	Mostek	MK3882	
Z80-DMA	Mostek	MK3883	
Z80-PIO	Mostek	MK3881	
Z80-SIO	Mostek	MK3884	
6104	Mostek	MK4104	

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Instrumentation Systems, (412) 243-1282
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Tasco, Inc., (206) 543-1414
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Digital Elect Mktg. Pty. Ltd., Tel: 438-2444
Malvern, Victoria
Digital Elect. (Victoria)
Intl **Austria, Wien**
Bacher Elektronische Gerate GMBH, Tel: 83-63-96-0
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Simac Electronics sprl, Tel: 02-6724556
Intl **Denmark, Valby**
Paratron A/S, Tel: 01-74-44-66
Intl **Finland, Helsinki**
Havulinna OY, Tel: 90-755-4144
Intl **France, Paris**
Datel Systems, SARL, Tel: 620-06-74
Intl **Germany, Munchen**
Datalek Systems GMBH, Tel: 089-77-60-95
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Kaytronics, Tel: 334450
Smitronix Int'l, Tel: 536238
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Sirces, Tel: 747649-730932
3G Electronics S.R.L., Tel: 544291
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Datel KK, Tel: 793-1031
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Simac Electronics b.v., Tel: 040-533725
Intl **New Zealand, Aukland**
David Reid Ltd., Tel: 492-189
Intl **Norway, Oslo**
Morgenstierne Co A/S
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Commercial Laborun, Lda., Tel: 62925
Intl **South Africa, Johannesburg**
Peter Jones Elect. Equip., Tel: 22-3658
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Aupoca Elec Y Sist, Tel: 257-48-98
Madrid
Aupoca Elec L Sist, Tel: 457-53-12
Intl **Sweden, Stockholm**
Martinson & Company AB, Tel: 08-63 11 05
Intl **Switzerland, Zurich**
Traco Electronics Co. Ltd., Tel: 01-201-0711
Intl **Taiwan, Taipei**
Multitech International Corp., Tel: 02-7681232
Intl **United Kingdom, Andover, Hants**
Datel UK Ltd., Tel: 0264-51055

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Multilek, Inc., (613) 825-4553
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Multilek, Inc., (416) 245-4622

Delco Electronics

Delco Electronics Division
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Kokomo, Indiana 46901
(317) 459-1271
William J. Gressman

Delco Electronics Division
4600 Park Road
Charlotte, North Carolina 28209
(704) 527-4444
Anthony E. Manes

Dionics

Dionics Inc.
65 Rushmore Street
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Tel: (516) 997-7474
TWX: 510-222-0974

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Contiflex AG, Tel: 26 60 17-17

Electronic Arrays

Electronic Arrays, Inc.
550 E. Middlefield Road
Mountain View, California 94043
(415) 964-4321
TWX: (910) 379-6985

Specific product information:
LSI Products ..... Mike Cassidy
Memory Products ..... Maurice O'Shea
Literature:
Marketing Services
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Customer Service
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Intl **France, Paris**
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Intl **Germany, Munchen**
Electronic Array GmbH, Tel: 089/7853112
Intl **Holland, Breda**
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Analog Devices, Ltd., Tel: 01 941 0466
Intl **Yugoslavia, Maribor**
Ellyptic AG, Tel: (062) 31041

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Arrow Electronics, (609) 235-1900
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Sterling Electronics, (201) 442-8000
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Arrow Electronics, (201) 797-5800
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Arrow Electronics, (216) 464-2000
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Arrow Electronics, (513) 253-9176
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Arrow Electronics, (414) 764-6600
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E. V. Johanssen Elektronik A-S,
Tel: (451) 83-9022
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Intl **Germany, Munchen**
Dema Electronische, Tel: 089-288018
Intl **Italy, Milano**
Eltronic S.R.L., Tel: 313364
Intl **Japan, Tokyo**
Nissho Electronics Corp., Tel: (03) 544-8311
Intl **Netherlands, Breda**
Famatra Benelux, Tel: 076/133457
Intl **Norway, Oslo**
Henaco A/S, Tel: (02) 157550
Intl **Sweden, Sundbyberg**
AB Electroflex, Tel: Stockholm (8) 289290
Intl **Switzerland, Zurich**
Rotronic AG, Tel: (01) 523211

Essex International

Essex International, Inc.
301 Alpha Drive
Pittsburgh, Pennsylvania 15328
(412) 782-0200
(412) 963-7203

Exar

Exar Integrated Systems
750 Palomar Avenue
Sunnyvale, California 94086
(408) 732-7290
TWX: 910-339-9233

Specific product information:
Earl Kiyan
Application engineering:
Joel Silverman, Perry Mostaan
Literature:
Sharon Hites, Debbie Spotts
Price and delivery:
Sharon Hites, Debbie Spotts
Follow-up an order:
Sharon Hites, Debbie Spotts
All other information:
Sharon Hites, Debbie Spotts

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Phoenix Sales, (203) 438-9644
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Janus, (312) 298-9330
IO **Cedar Rapids**
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Electronic Innovators, (612) 884-7471
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Independence
Dytronix, (816) 373-6600
NC **Raleigh**
Component Sales, (919) 782-8433
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TN **Jefferson City**
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Technical Marketing Inc., (713) 777-9228
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Rayo Electronica ARL, Tel: 37 98 90
Intl **Australia, Prospect**
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Intl **Denmark, Copenhagen**
Mer-el A/S Tel: (01) 20 7444 44
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SW Instruments, Tel: 73 82 65/ 76 24 86
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Tekelec/Airtronic, Tel: (1) 027 75 35
Intl **Germany, Korshenbroich**
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Intl **Netherlands, Zoetermeer**
Tekelic/Airtronic V.B., Tel: 079-310100
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Elico Fastronix S A, Tel: 415 66 54
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Radar, (206) 282-2511
Sterling Electronics, (206) 762-9100
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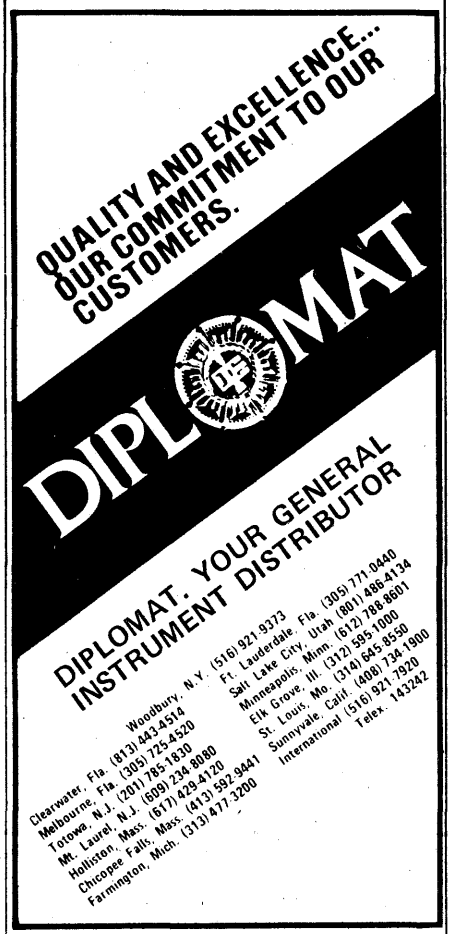
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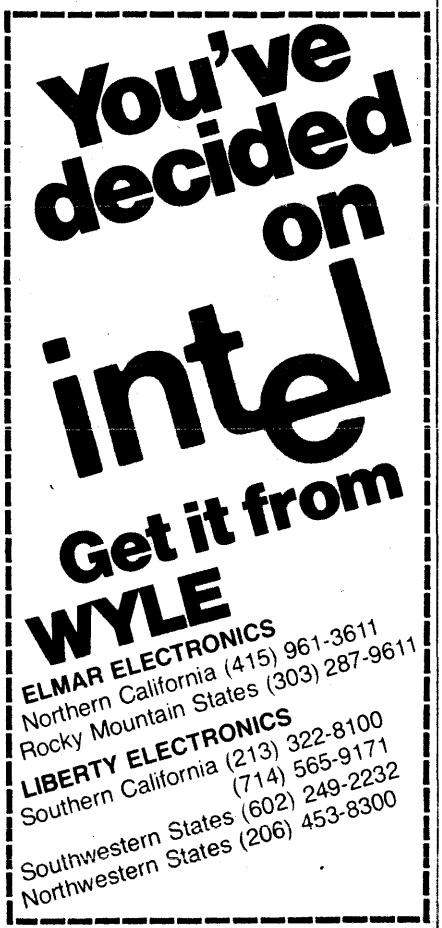
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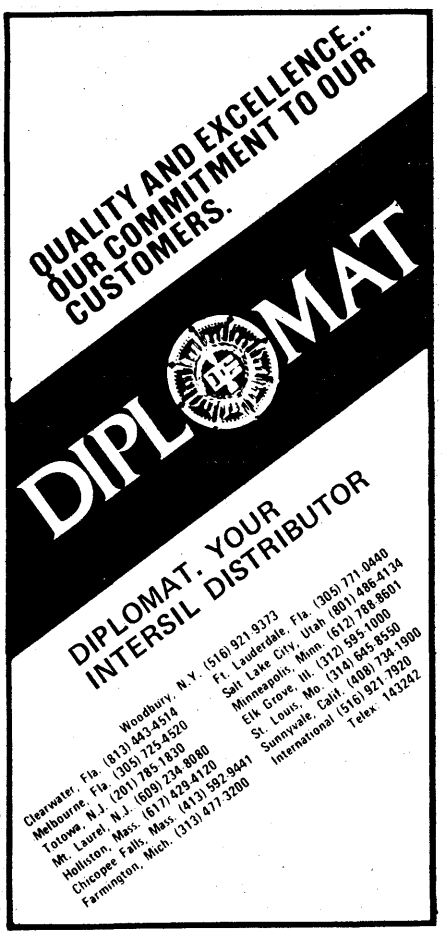
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Veeco Lambda Ltd., (514) 697-6520
Toronto, Ontario
Veeco Lambda Ltd., (416) 486-0794

Intl **England, High Wycombe, Bucks**
Lambda Electronics, Tel: High Wycombe 36386/7/8

Intl **France, Gometz le Chatel**
Lambda Electronique S.A., Tel: 012-1487

Intl **Germany, Aachen**
Lambda Netzgerate GmbH., Tel: 078-41-5527

GERMANY, MUNCHEN
Astronic GmbH
Tel: 089-3040 11
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IsLambda Electronics Ltd., Tel: 240-672

Intl **Japan, Yokohama**
Nemic, Tel: 03-490-5831

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Mexitek, S.A., Tel: 5-36-09-10 or 5-43-03-77

LSI Computer Systems

LSI Computer Systems, Inc.
1235 Walt Whitman Road
Melville, New York 11746
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TWX: 510-226-7833

Specific product information:
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Applications engineering:
Ronald Colino
Literature:
Shari Chassen
Price and delivery:
Shari Chassen
Follow-up an order:
Shari Chassen
All other information:
Shari Chassen

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REMCO, (205) 883-9260

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Components, Inc., (513) 866-0661

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Nuclex, Tel: 46-9549

Intl **France, Boulogne**
International Semiconductor Corp.,
Tel: 6045275+

Intl **Germany, Munchen**
Solicomp, Tel: 089/69 65 66/67

Intl **Italy, Milano**
Skylab, Tel: 688.38.06

Intl **Japan, Tokyo**
Corton Trading Company,
Tel: (03) 44907141/2

Intl **United Kingdom, London**
ADCO Industrial Components,
Tel: 01-995-8495

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Maruman Integrated Circuits
122 Midas Way
Sunnyvale, California 94086
(408) 739-0560

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Western Micro Technology, (408) 737-1660

Master Logic Corp.

Master Logic Corporation
716 E. Evelyn
Sunnyvale, CA 94086
(408) 732-7777

Specific product information:
Stephen R. Allen
Application engineering:
Stephen R. Allen
Literature:
Stephen R. Allen
Price and delivery:
Stephen R. Allen
Follow-up an order:
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All other information:
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Matrox

Matrox Electronic Systems Ltd.
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Satt Electronlund AB, Tel: 040-22 20 00

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Literature:
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Midwest Marketing Associates, (513) 433-2511

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Microel, Tel: 1-9070824

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Intl **Japan, Tokyo**
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Scancopter AS, Tel: 02-69 4490

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S'Electronics

Intl **Spain, Madrid**
Compania Electronica de Technicas, Tel: 254-98 31

Intl **Sweden, Vallingby**
Scancopter, Tel: 08/38 00 65

Intl **Switzerland, Zurich**
Telemeter Electronic AG, Tel: 01/25 78 72

Intl **Taiwan, Taipei**
Tai I Trading Co., Ltd., Tel: 393 61111

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All Inquiries: Marketing Department
.....ext. 20, 21, 24

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Bob Anderson Company, (602) 266-2070

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MA **Needham Heights**
Wood Sales Co., (617) 444-1601

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A. B. Andrews & Co., Inc., (919) 549-0563

NH **Wilton**
Wood Sales Co., (603) 654-2961

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Rical Associates, (201) 945-5250

NY **Syracuse**
T-^{2} Electronics, (315) 463-8592
Victor
T-^{2} Electronics, (716) 924-9101

OH **Centerville**
Charles V. Clark, (513) 435-3000
Cleveland
Del Steffen & Associates, (216) 461-8333
Dayton
Del Steffen & Associates, (513) 293-3146

OR **Portland**
Northwest Marketing Associates (503) 297-2581

VA **Vinton**
A. B. Andrews & Co., Inc.

WA **Bellevue**
Northwest Marketing Associates, (206) 455-5846

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Santa Clara, California 95050
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TWX: (910) 338-0154

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Literature:
Standard Products Division ..... ext. 314

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San Jose
Electro-Ventures, (408) 997-0955
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CO **Parker**
Component Sales, (303) 841-2650

FL **Coral Springs**
H.A. Inc., (305) 752-7520

IL **Chicago**
Industry Representatives Inc., (312) 647-7755

IN **Indianapolis**
Electro Reps Inc. (317) 255-4147

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Dynamic Sales, (617) 272-5676

MD **Baltimore**
Stemler Associates, (301) 944-8262

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Ontek, Inc., (716) 464-8636
Tuckahoe
Spectrum Sales, (914) 793-1660

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The Cunningham Company, (512) 459-8947
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The Cunningham Company, (214) 233-4303
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The Cunningham Company, (713) 461-4197

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AMPEC Engineering Co.

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Distributors

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Whitney Distributors, (301) 944-8080

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Marketing
Application engineering:
Marketing
Literature:
Marketing
Follow-up an order:
Customer Service ..... (514) 534-2321
All other information:
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Scott Electronics, (216) 291-2600
Columbus
Scott Electronics, (614) 236-8619
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Scott Electronics, (513) 294-0539

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Scott Electronics, (412) 828-1073

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Houston
W. Reese Assoc., (713) 621-3134

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Intl **Ireland, Shannon**
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Mitel Semiconductor, Tel: 01-119302

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Intl **Puerto Rico, Katano**
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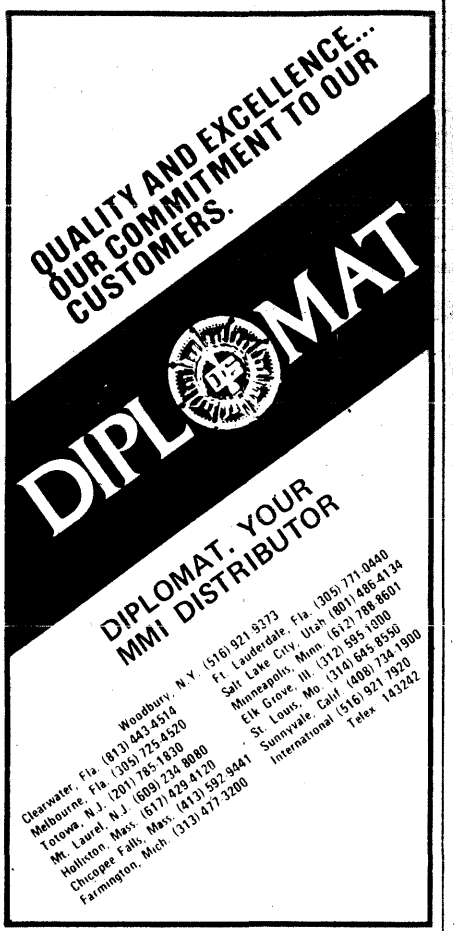
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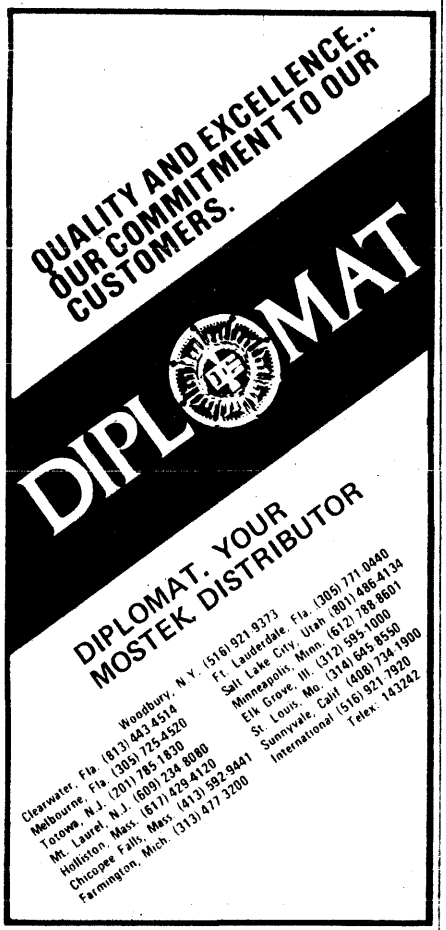
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Specific product information:
Larry Hatt
Application engineering:
Vern Reinhardt
Literature:
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Price and delivery:
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Follow-up an order:
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3120 Central Expressway
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Diane Michel
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Novonics

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Nucleonic Products Co.

Nucleonic Products Co.
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Canoga Park, California 91303
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TWX: (910) 494-1954

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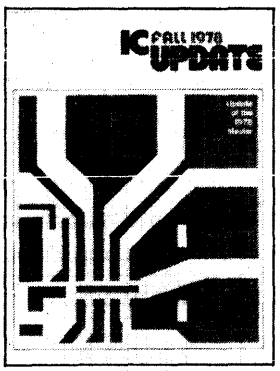
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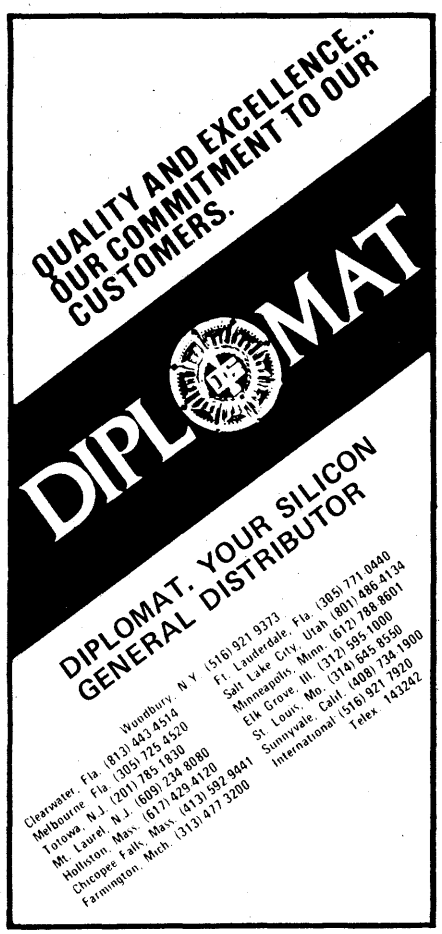
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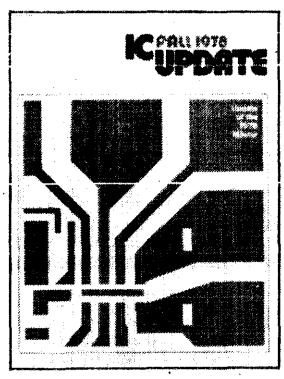
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Mississauga, Ontario
Hamilton/Avnet, (416) 677-7432
Ottawa, Ontario
Future Elec., (514) 735-5775
Hamilton/Avnet, (613) 226-1700
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Future Elec., (416) 677-7820

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Future Electronics
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Intl **England, Chadderton**
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ENGLAND
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Oy Findip AB
Tel: 90-502 255
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Silicon Systems Inc.

Silicon Systems Inc.
16692 Hale Avenue
Irvine, CA 92714
(714) 979-0941
TWX: 910-595-2809

Specific product information ..... Jim Meyer
Application engineering ..... Bill Loesch
Literature ..... Dianna Archuleta
Price and delivery ..... Jim Meyer

Sales Offices & Representatives

CA **Placentia**
Adams Associates, (714) 996-0310

MA **Burlington**
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NY **Hicksville**
Lorac Sales, Inc., (516) 681-8746

Siltronics

Sitronics, Ltd.
P.O. Box 11236, Station H
Ottawa, Ontario, Canada K2H7T9
(613) 820-2931

Distributors

MA **Westwood**
George Urban Assoc., (617) 329-4068

Solid State Microtechnology for Music

Solid State Music
21021A Walsh Avenue
Santa Clara, Calif. 95050
(408) 248-0917

Specific product information: ..... John Burgoon
Application engineering: ..... Ron Dow
Literature: ..... Receptionist
Price and delivery: ..... John Burgoon
Follow-up an order: ..... John Burgoon

Sales Offices & Representatives

Intl **Italy, Milano**
Comprel S. R. L. Tel: (02) 92.80.809

Intl **Japan, Tokyo**
Nippon Imex Tel: 321-4415

Solid State Scientific, Inc.

Solid State Scientific, Inc.
Montgomeryville Industrial Center
Montgomeryville, Pennsylvania 18936
(215) 855-8400
TWX: (510) 661-7267

All other information:
All inquiries: Sales Department

Sales Offices & Representatives

AL **Huntsville**
Rep Inc., (205) 881-9270

AZ **Scottsdale**
Semper Fi Sales Co., (602) 945-4556

CA **El Segundo**
Varigon Assoc., (213) 322-1120
Irvine
Solid State Scientific, (714) 955-1411
Mountain View
Thresum Assoc., (415) 965-9180
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Sherman Oaks
Solid State Scientific, (213) 995-6666

CO **Englewood**
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CT **Lakeville**
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Solid State Scientific, (312) 884-7131

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MI **Livonia**
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MN **Bloomington**
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Midtec Assoc., (314) 837-5200

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NJ **Cherry Hill**
Solid State Scientific, (609) 429-8710

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Quality Components Inc., (315) 682-6633
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ERA Inc., (516) 822-9890

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SAI, (412) 782-5120

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Rep Inc., (615) 475-4105

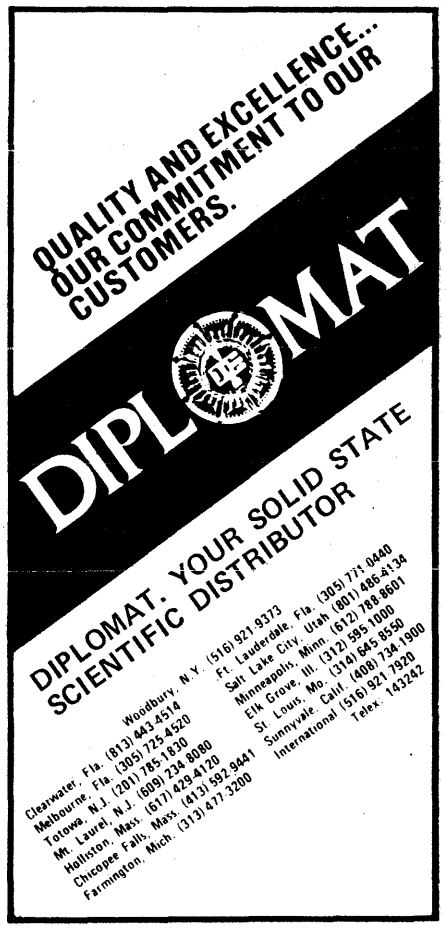
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Solitron Devices, Inc.
Semiconductor Division
8808 Balboa Avenue
San Diego, California 92123
(714) 278-8780

Specific product information:
Randy Chapman

Application engineering:
Jim Everett

Literature:
Customer Service

Price and delivery:
Customer Service

Follow-up an order:
Customer Service

All other information:
Customer Service

Sales Offices & Representatives

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Instant Component Service, Tel: 95-1566
Intl **Denmark, Copenhagen**
E. V. Johanssen Elektronik A/S, Tel: (01) 83 90 22
Intl **Finland, Helsinki**
Oy Fintronic AB, Tel: 90/601155
Intl **France, Bagneux**
Acetel, Tel: 664 10 50
Intl **Germany, Munchen**
Bitronic GmbH, Tel: 089/470 2098
Intl **Holland, Rotterdam**
Nedelko B.V. Electronics, Tel: 010-293166
Intl **Kong Kong, Kowloon**
International Sales Corp., Tel: 3-433 549
Intl **Israel, Tel-Aviv**
Electronic Microsystems, Ltd., Tel: 03-412403
Intl **Italy, Milano**
Kimates S.P.A., Tel: (02) 8562
Intl **Japan, Tokyo**
Hirel Company, Ltd., Tel: (03) 357-8201
Intl **Mexico, Cuernavaca**
Solidev Mexicana, S.A.
Intl **Norway, Oslo**
Nordisk Elektronik (Norge) A/S, Tel: (02) 55 38 93
Intl **Sweden, Djursholm**
Integrerad Elektronik AB, Tel: 08/753 03 30
Intl **Switzerland, Mutschellen**
Stolz AG, Tel: 057-54655
Intl **United Kingdom**
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Distronic Ltd., Tel: 32947/39701

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Intermark Electronics, (714) 540-1322
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Hall-Mark Elec. Corp., (305) 855-4020
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Victor Kim Electronic, (808) 533-7132
IL **Elk Grove Village**
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OHM/Electronics, (312) 359-5500
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Hall-Mark Elec. Corp., (314) 291-5350
NC **Raleigh**
Hall-Mark Elec. Corp., (919) 832-4465
Winston-Salem
Kirkman Electronics., (919) 722-9131
NY **Buffalo**
Summit Distributors, (716) 884-3450
Elmsford
Zeus Components, (914) 592-4120
Farmingdale
Harrison Electronics, (516) 293-7990
Hauppage
Jaco Elec., Inc., (516) 273-5500
North Bellemore
Hygrade Electronics, (516) 785-6200
OH **Columbus**
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Dayton
Arrow Electronics, (513) 253-9176
Hall-Mark Elec. Corp., (513) 294-0437
Koehlke Components, (513) 294-0154
OK **Tulsa**
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Hall-Mark Elec. Corp., (918) 835-8458
PA **Huntingdon Valley**
Hall-Mark Elec. Corp., (215) 355-7300
TX **Austin**
Hall-Mark Elec. Corp., (512) 837-2814
Dallas
Component Specialties, (214) 357-6511
Hall-Mark Elec. Corp., (214) 234-4721
R. V. Weatherford Co., (214) 243-1571
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Component Spec., Inc., (713) 771-7237
Hall-Mark Elec. Corp., (713) 781-6100
R. V. Weatherford Co., (713) 688-7406
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Hall-Mark Elec. Corp., (414) 476-1270
Can **Dorval, Quebec**
Intl. Rectifier C. Ltd., (514) 631-4696
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SWITZERLAND
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Sprague Electric Company

Sprague Electric Company
Semiconductor Division
115 Northeast Cutoff
Worcester, Massachusetts 01606
(617) 853-5000
Telex: 920467

Specific product information:

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Camera	B. Marshall
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Transistor Arrays	G. Tully
Operational Amplifiers	G. Tully
Display Driver	G. Tully
MOS	G. Tully

Application engineering:
Same as above
Literature:
647 Marshall Street, North Adams, Massachusetts 01247, (413) 664-4411 ..... ext. 2572
Price and delivery:
Same as product information:
Place an order:
Same as above
Follow-up an order:
Same as above

Sales Offices & Representatives

Contact these offices for names of distributors

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Sprague Electric Company, (602) 279-5435
CA **Burlingame**
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Inglewood
Sprague Eectric Company, (213) 649-2600
San Diego
KCE Corp., (714) 278-7640
CO **Denver**
William J. Purdy Company, (303) 777-1411
CT **Trumbull**
Sprague Electric Company, (203) 261-2551
DC **Washington**
Sprague Electric Company, (Gov't sales only) (202) 337-7820
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IL **Chicago**
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Sprague Electric Company, (312) 296-6620
IN **Indianapolis**
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Sprague Electric Company, (206) 632-7761
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Sprague Electric of Canada, (416) 766-6123
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Sprague Electric (U.K.) Ltd., Tel: 44627
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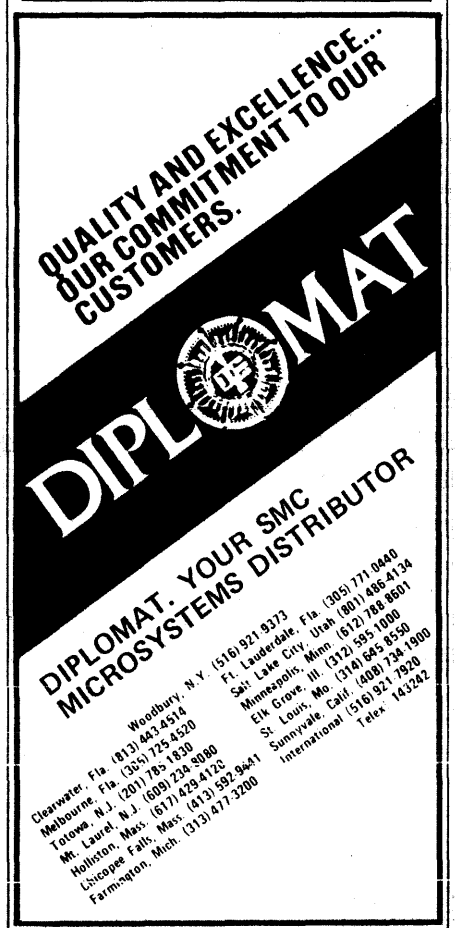
Standard Microsystems

Standard Microsystems Corporation
35 Marcus Boulevard
Hauppauge, New York 11787
(516) 273-3100
TWX: (510) 227-8898

Specific product information:
Brian Cayton
Application engineering:
Brian Cayton
Literature:
Addie Macedo
Price and delivery:
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All other information:
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Intl **Finland, Helsinki**
Havulinna Oy, Tel: (90) 661-451
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Tekelec Airtronic, Tel: 027-75-35
Intl **Great Britain, London**
Rastra Electronics, Ltd., Tel: (1) 7483143
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R.N. Electronics Ltd., Tel: (03) 471659
Intl **Japan, Tokyo**
Teijin Advanced Products Corp.,
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Dimos AG, Tel: (51) 626140
Intl **West Germany, Munchen**
Atlantik Elektronik GmbH, Tel: (89)
7853112



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Diplomat Electronics, Inc., (408) 734-1900
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CO **Westminster**
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Bell Indutries, Electronics Distributor Div.,
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FL **Clearwater**
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Hammond Electronics, Inc., (305) 849-6060
IL **Elk Grove Village**
Diplomat Electronics, Inc., (312) 595-1000
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Mar-Con Sales, (312) 675-6450
IN **Indianapolis**
Sheridan Sales Co., (317) 297-3146
MA **Burington**
RC Components, (617) 273-1860
Zeus/New England, Inc., (617) 273-0750
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Diplomat Electronics, Inc., (415) 592-9441
Holliston
Diplomat Electronics, Inc., (617) 429-4120
MD **Baltimore**
Whitney Distributors, Inc., (301) 944-8080
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Sheridan Sales Co., (313) 477-3800
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Sheridan Sales Co., (616) 942-2504
MN **Minneapolis**
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MO **Florissant**
Sheridan Sales Co., (314) 837-5200
St. Louis
Diplomat Electronics, Inc., (314) 645-8550
NC **Greensboro**
Hammond Electronics, Inc., (919) 275-6391
NJ **Mt. Laurel**
Diplomat Electronics, Inc., (609) 234-8080
Totowa
Diplomat Electronics, Inc., (201) 785-1830
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NY **Elmsford**
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Zeus Components Corp., (516) 752-9551
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L-DUN Electronics, (716) 328-0830
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Diplomat Electronics, Inc., (516) 921-9373
OH **Cincinnati**
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Sheridan Sales Co., (216) 461-3300
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Sheridan Sales Co., (513) 223-3332
PA **Hatboro**
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Sheridan Sales Co., (412) 351-4000
SC **Greenville**
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Quality Components, Inc., (214) 387-4949
Houston
Quality Components, Inc., (713) 772-7100
UT **Salt Lake City**
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Future Electronics
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Bacher Elektronische. Tel: (222) 837152
Intl **France, Serves**
Tekelec Airtronic, Tel: 027-7535
Intl **Great Britain, London**
Rastra Electronics, Ltd., Tel: (1) 7483143

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Teijin Advanced Prod. Corp., Tel: (506) 4670-6
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Intl **Norway, Oslo**
EGA A/S, Tel: (2) 221900
Intl **Switzerland, Zurich**
Dimos AG, Tel: (51) 626140
Intl **West Germany, Munchen**
Atlantik Elektronik GmbH, Tel: (89) 7853112

Supertex, Inc.

Supertex Inc.
1225 Bordeaux Drive
Sunnyvale, California 94086
(408) 744-0100
TWX: 910-339-3988

Specific product information ..... Diane Lowe
Application engineering ..... Bob Chao
Literature ..... Renee Colgate
Price and delivery ..... Diane Lowe
Follow-up an order ..... Diane Lowe
All other information ..... Renee Colgate

Sales Offices & Representatives

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Orion Sales, (714) 566-0360
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Epitron International, (408) 354-1415
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Supertex, Inc., (408) 744-0100
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Orion Sales, (714) 832-9687
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Sieger Assoc., (312) 991-6161
MA **Lowell**
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Hytech, (214) 234-3375
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Sundance Sales Inc., (713) 495-4778
WA **Lynwood**
Systems Specialists, (206) 775-6603
Intl **Japan, Chiyoda-Ku**
Systems Marketing, Inc., Tel: (03) 254-2751
Intl **Hong Kong**
Supertex Ltd.
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Taeil Trading Company, Tel: 22-6741
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Infratron, Tel: (040) 81578

Synertek Inc.

Syntertek Inc .
P.O. Box 552
3001 Stender Way
Santa Clara, California 95051
(408) 988-5600
TWX: 910-338-0135

Specific product information:
Memory Products Marketing 988-5611
Application engineering:
Applications 988-5616
Literature:
Literature Desk 988-5632
Price and delivery:
Customer Service (to 999 pcs) 988-5641
Memory Products (over 999 pcs) 988-5611
Microprocessor Products (over 999 pcs) 988-5616
All other information 988-5600

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Dyne-A-Mark Corp., (305) 831-2097
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Ontec, Inc., (716) 464-8636
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Ontec, Inc., (716) 464-8636
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OH **Beachwood**
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Sheridan Sales Co., (513) 761-5432

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Houston
Quality Components, Inc., (713) 772-7100

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Cairon Electric, (801) 487-7451
Century Electronics, (801) 972-6969
Kierulff Electronics, (801) 973-6913

WA **Seattle**
Sterling Electronics, (206) 762-9100
Tukwila
Kierulff Eectronics, (206) 575-4420

WI **Milwaukee**
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Arrow Electronics, (414) 764-6600

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W. Stolz AG
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Irvine, California 92714
(714) 754-7566
Telex: 681410

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Teledyne Crystalonics
147 Sherman Street
Cambridge, Massachusetts 02140
(617) 491-1670

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Application Engineering:
Alan Alaimo
Literature:
Susan McTighe
Price and delivery:
W. J. Kilgarriff
Follow-up an order:
Karen Mason
All other information:
W. J. Kilgarriff

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V. G. Sales, (305) 831-8688

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KS **Olathe**
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MD **Rockville**
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MO **Hazelwood**
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G.E. Electronics, Tel: 01-7270711/3 & 5008

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Intl **Germany, Heilbronn**
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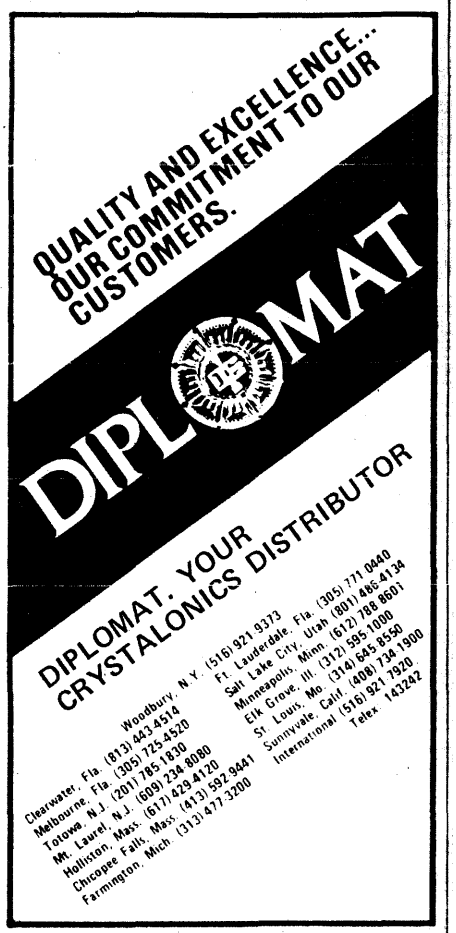
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MCA Tronix, Tel: 70/548890

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Pyttronics, (301) 792-7000

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Tory Sales, (201) 935-5454

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Components Plus, (516) 231-9200
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Woodbury
Diplomat Elec., (516) 921-9373

OH **Englewood**
Argent Ind., (513) 836-8633

TX **Austin**
Quality Components, (512) 458-4181
Dallas
Solid State, (214) 352-2601
Quality Components, (214) 387-4949
Houston
Quality Components, (713) 772-7100

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Intl **Israel, Tel-Aviv**
STG International, Tel: 53459

Intl **Italy, Milano**
Kimates, Tel: 02-8562

Intl **Netherlands, Scheveningen**
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Intl **Spain, Barcelona**
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Intl **Sweden, Vallingby**
Svensk Tele Industri AB, Tel: 890435

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Teledyne Philbrick

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TWX: (710) 348-6726

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Sales Department
Application engineering:
Sales Department
Literature:
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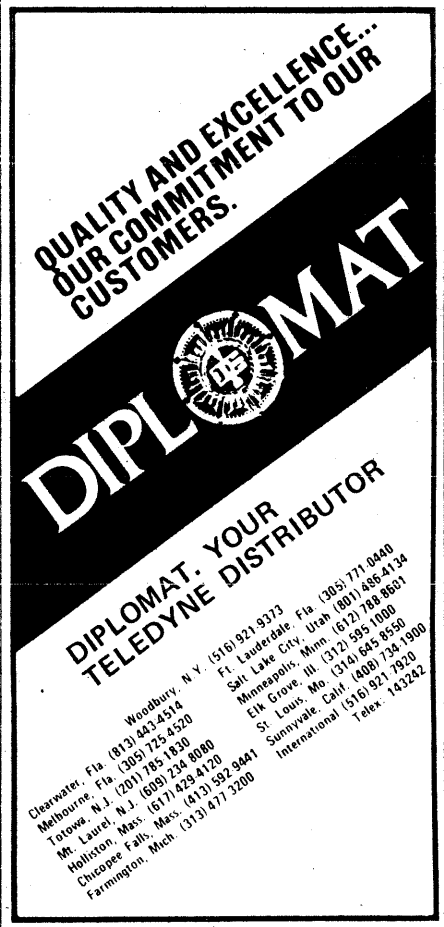
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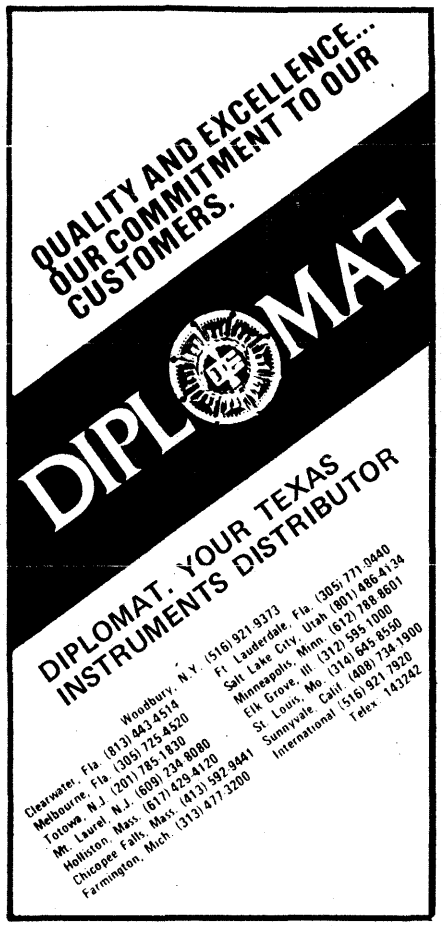
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